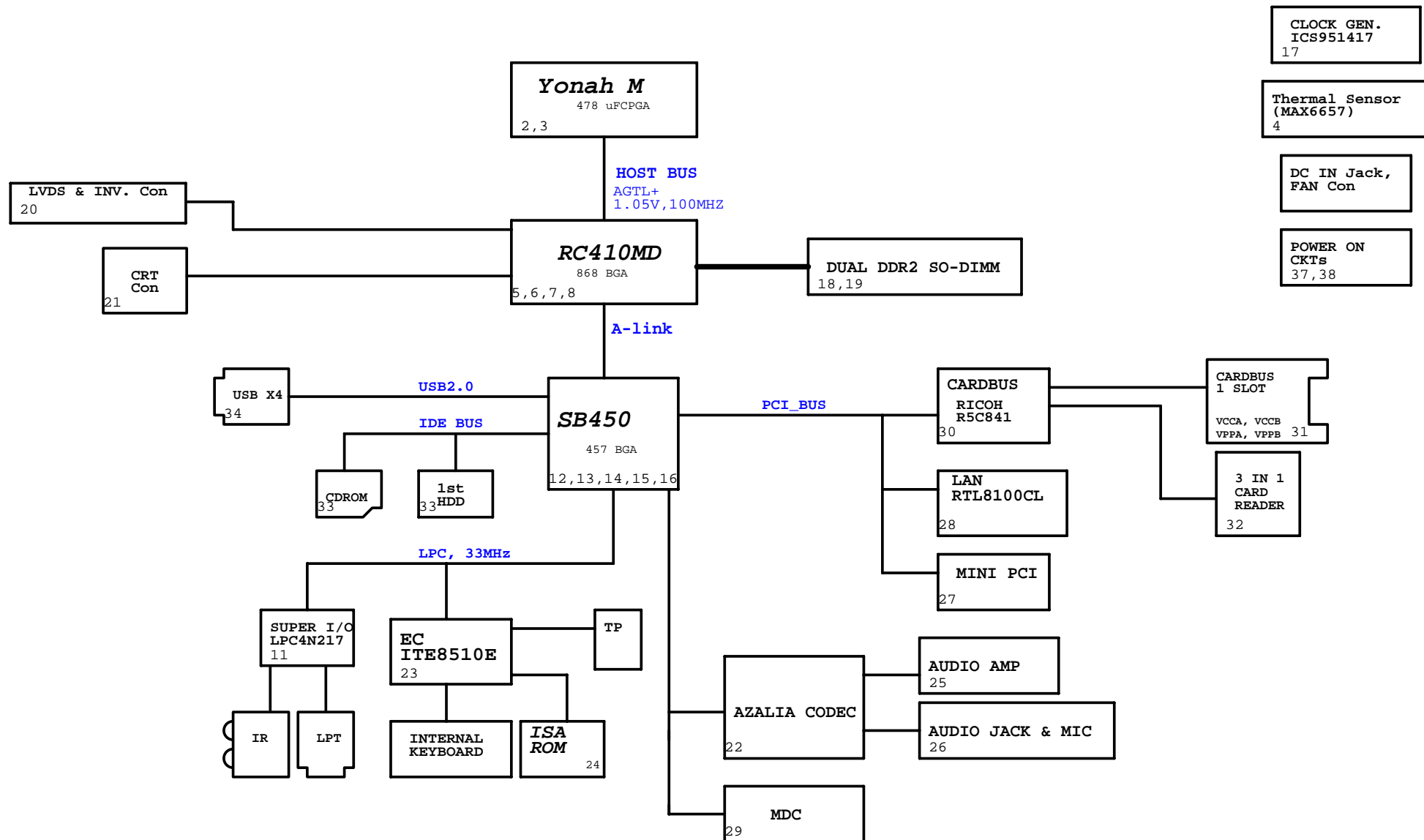
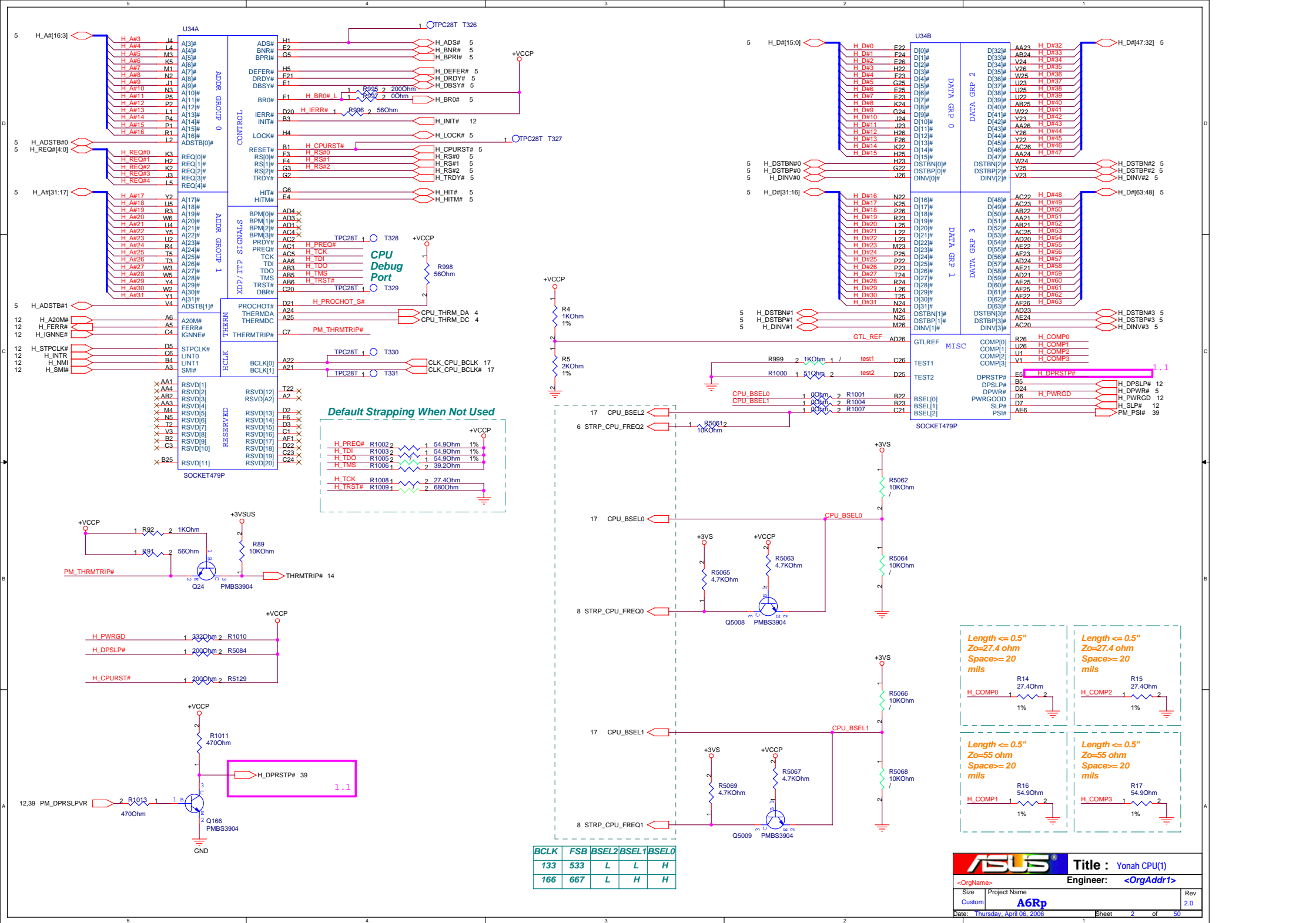
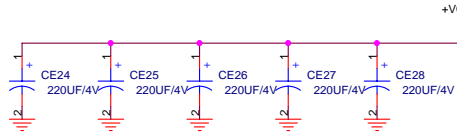


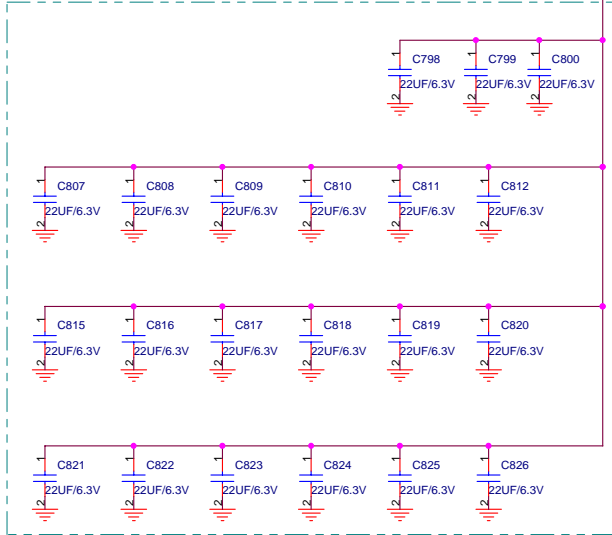
Yonah/RC410MD/IXP450 BLOCK DIAGRAM



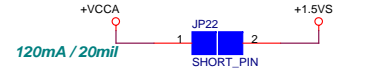
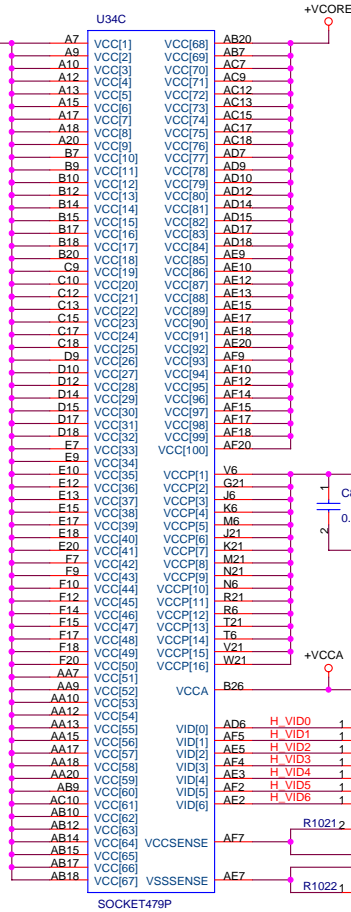




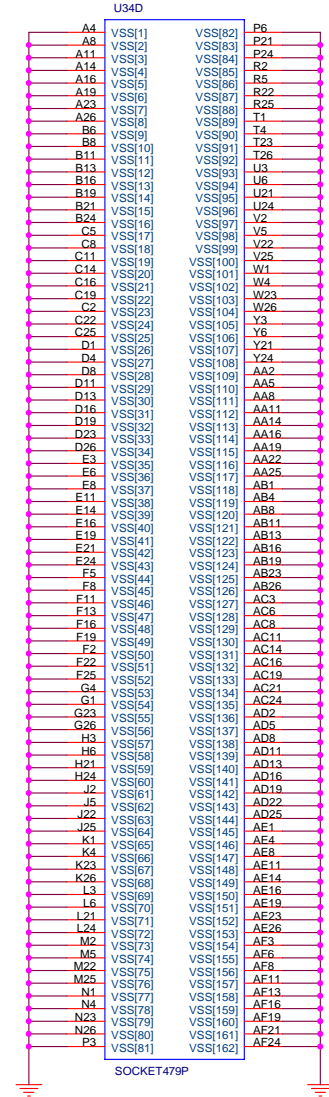
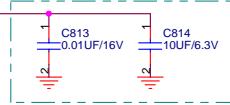
**CPU +VCORE
Mid-Frequency
Capacitors**



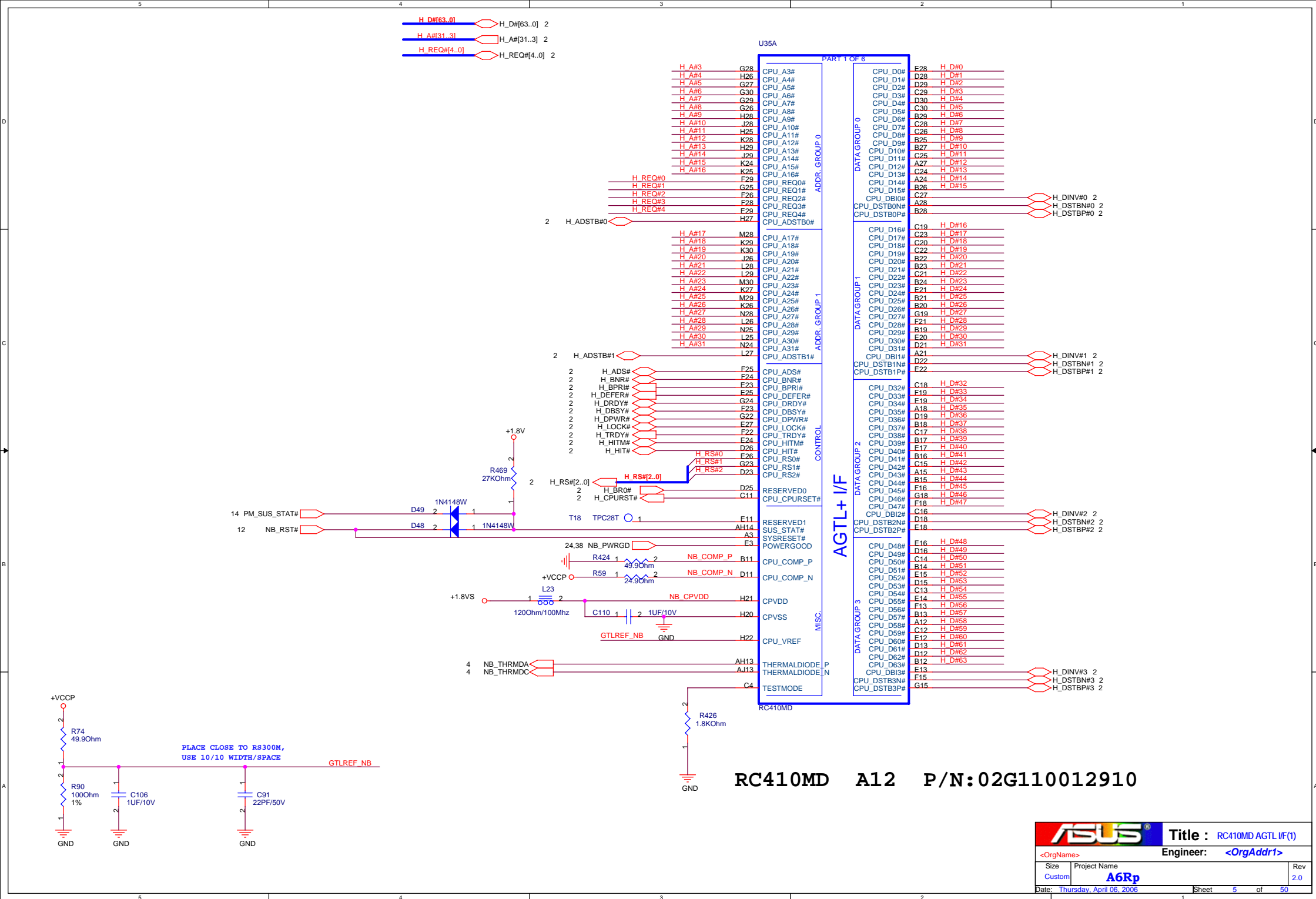
+VCORE Low-Freq Capacitor
Intel: 330UF *6
ATI: 330UF *6
R1F: 330UF *4
A7J: 330UF *5
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
ATI: 10UF *26
R1F: 22UF *16
A7J: 22UF*29 use 19
A6RF: 22UF*21 use 21
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4
A7J: 220UF *1, 0.1UF *6
A6RF: 220UF *1, 0.1UF *6

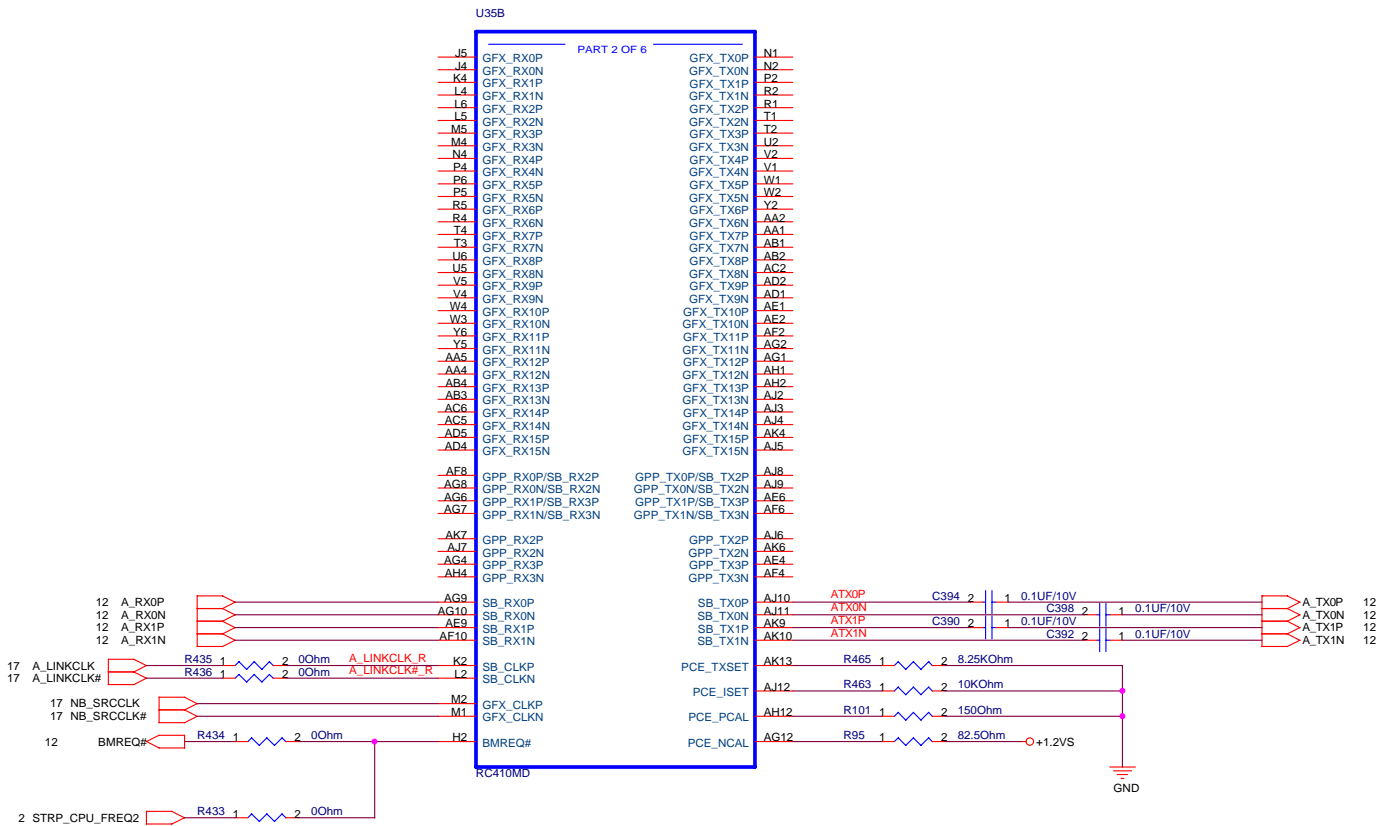


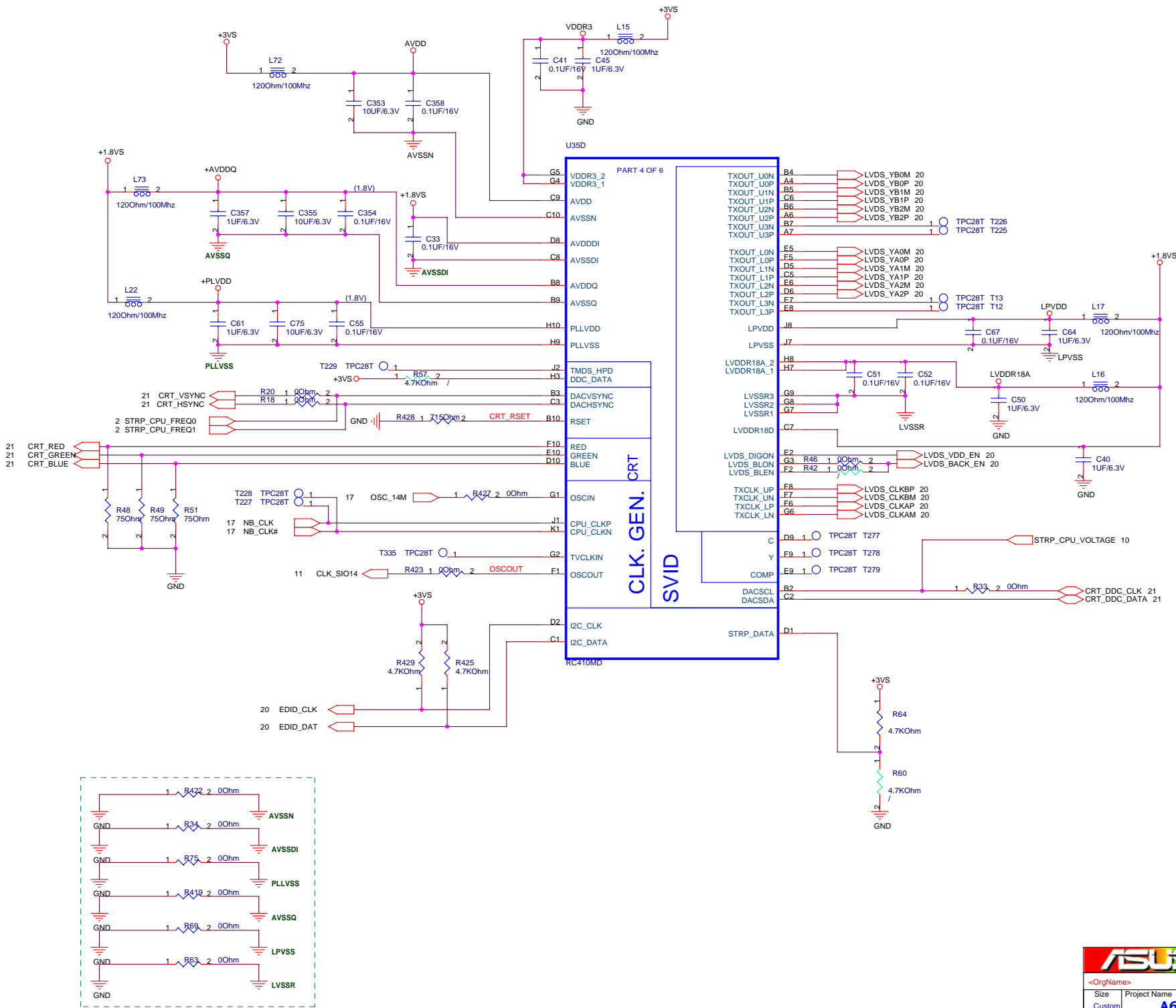
**+VCCA
Decoupling
Capacitors**

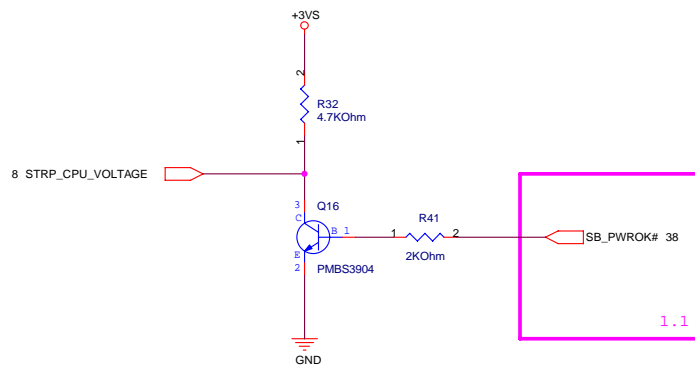


Custom	Aokp	2.0
Date: Thursday, April 06, 2006	Sheet 4 of 50	





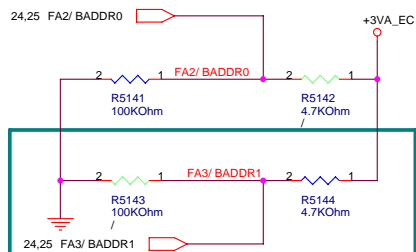




STRP_CPU_VOLTAGE: CPU VCC
0: MOBILE CPU
1: DESKTOP CPU
DEFAULT:0

FA2/ BADDR0 & FA3/ BADDR1

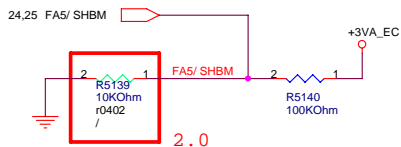
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved



Note: Sampled at VSTBY Power Up Reset

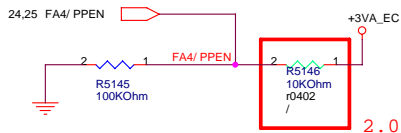
FA5/ SHBM

0: Disable Shared Memory with Host BIOS
 1: Enable Shared Memory with Host BIOS



FA4/ PPEN

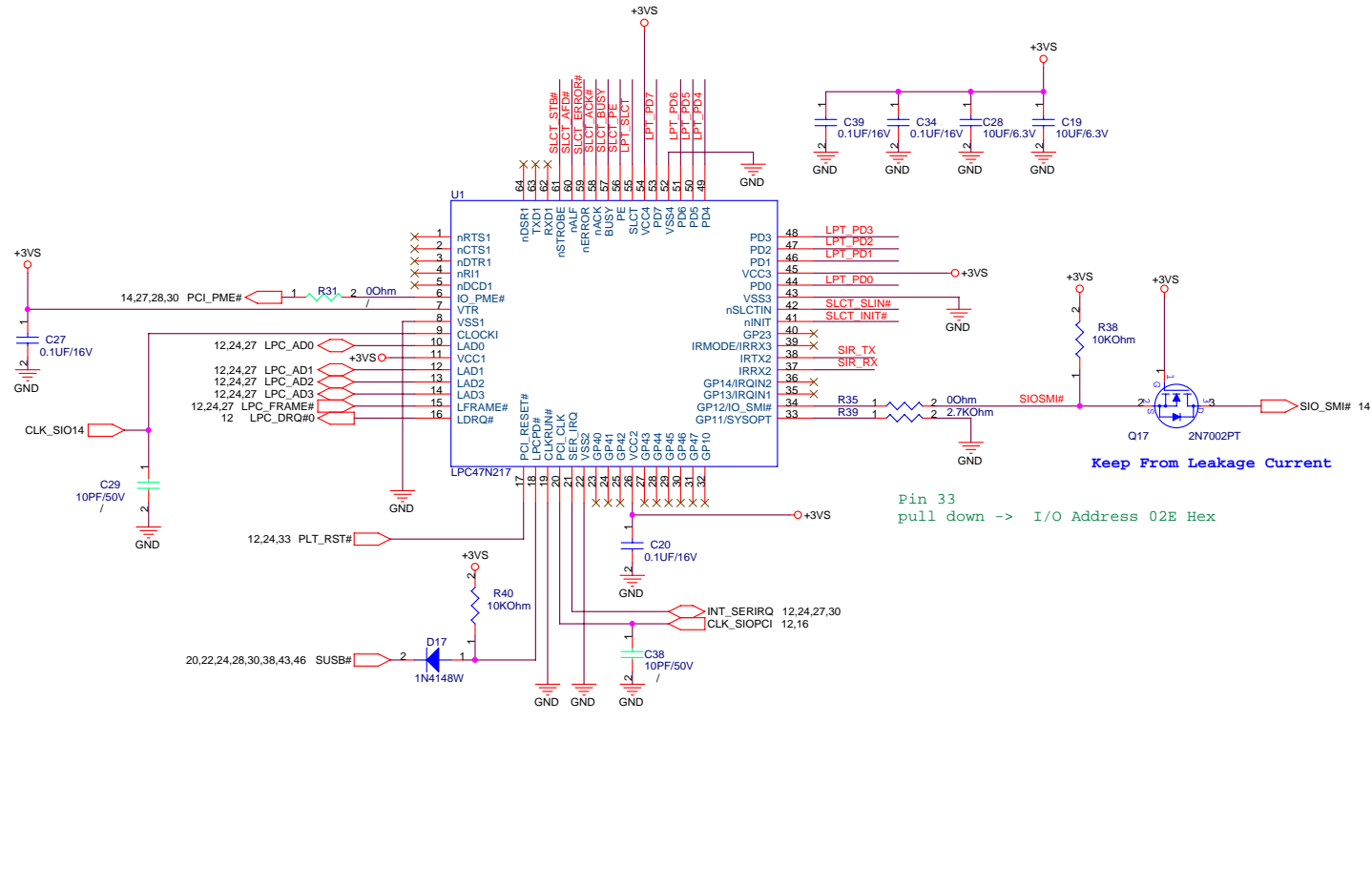
0: Normal
 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



1.1

EC Hardware Strapping

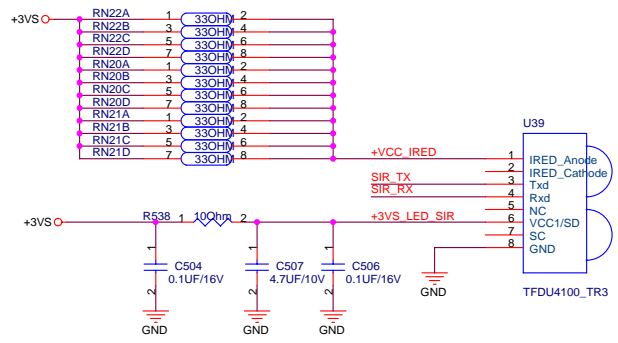
Super I/O



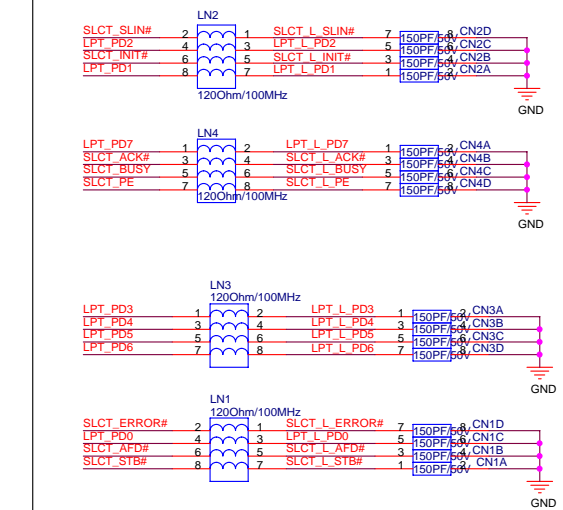
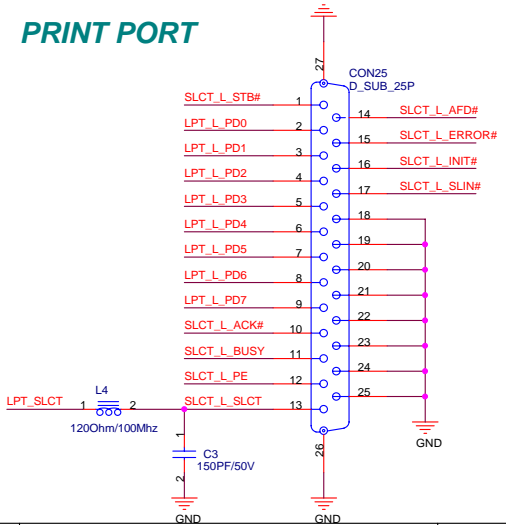
Pin 33
pull down -> I/O Address 02E Hex

Keep From Leakage Current

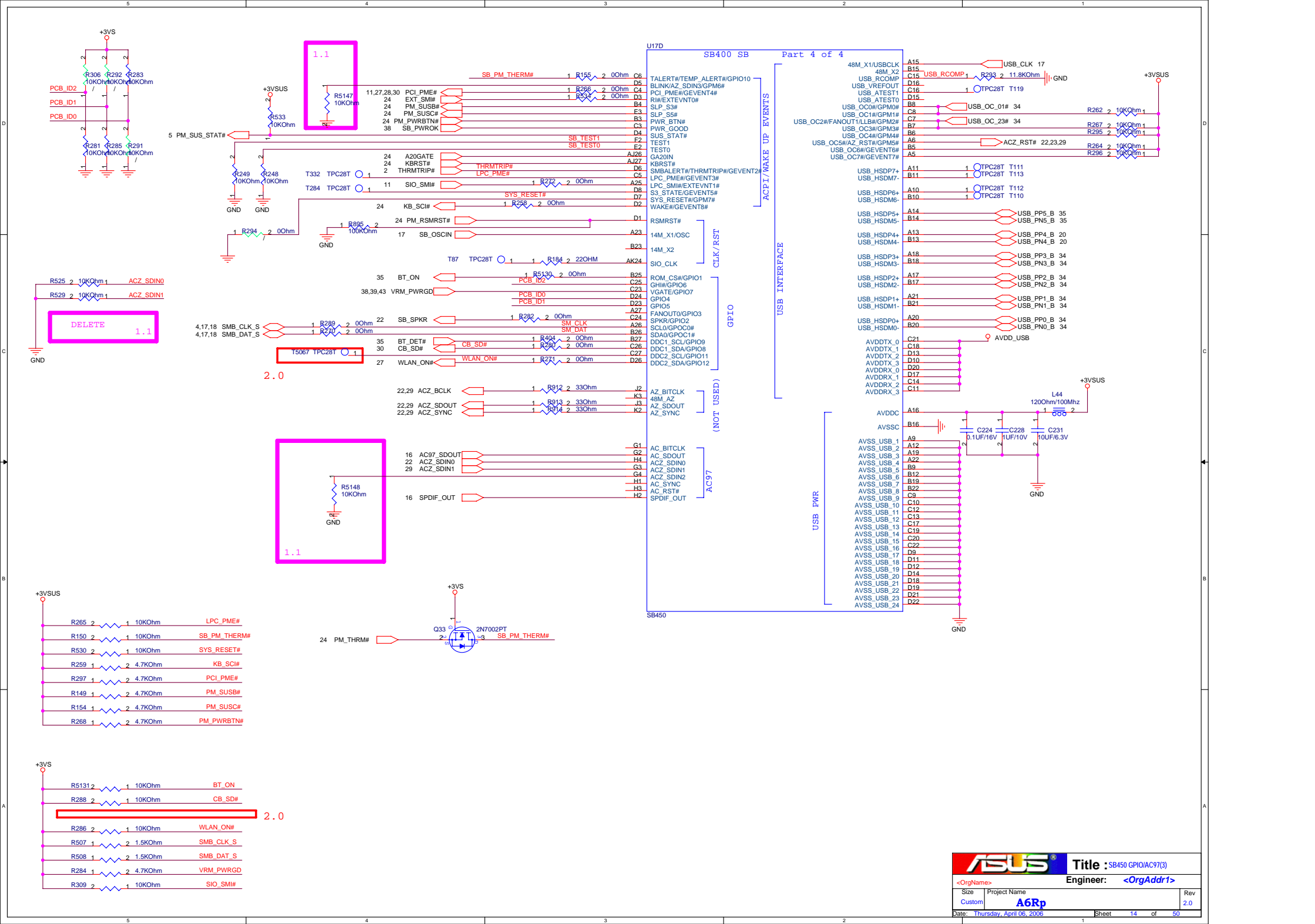
SIR

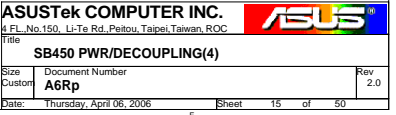


PRINT PORT

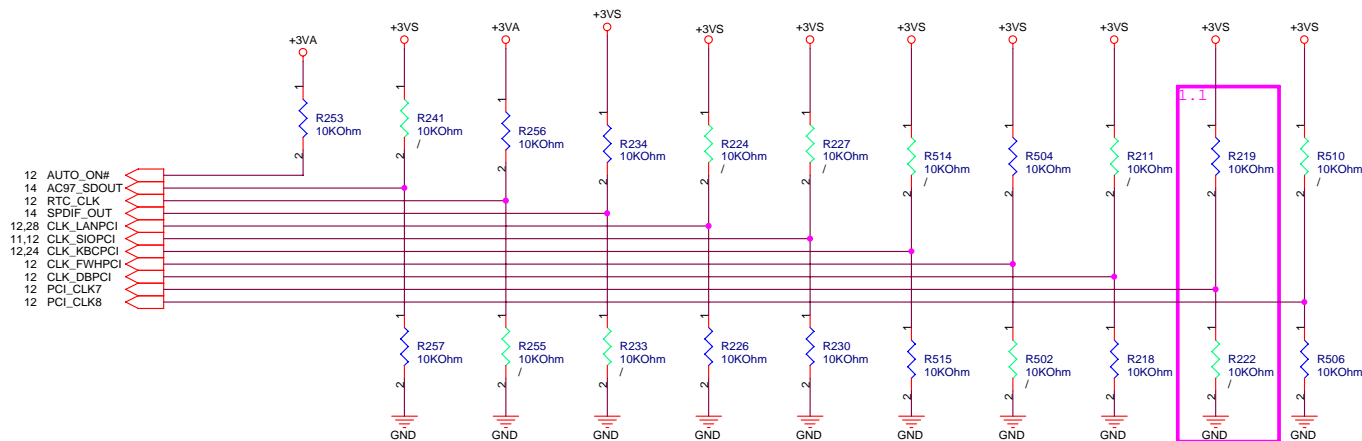








REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz		USB PHY PWRDOWN DISABLE	USE USB PLL		CPU I/F = K8	ROM TYPE H,H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz	SEE NOTE1	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	SEE NOTE2	CPU I/F = P4	H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM	

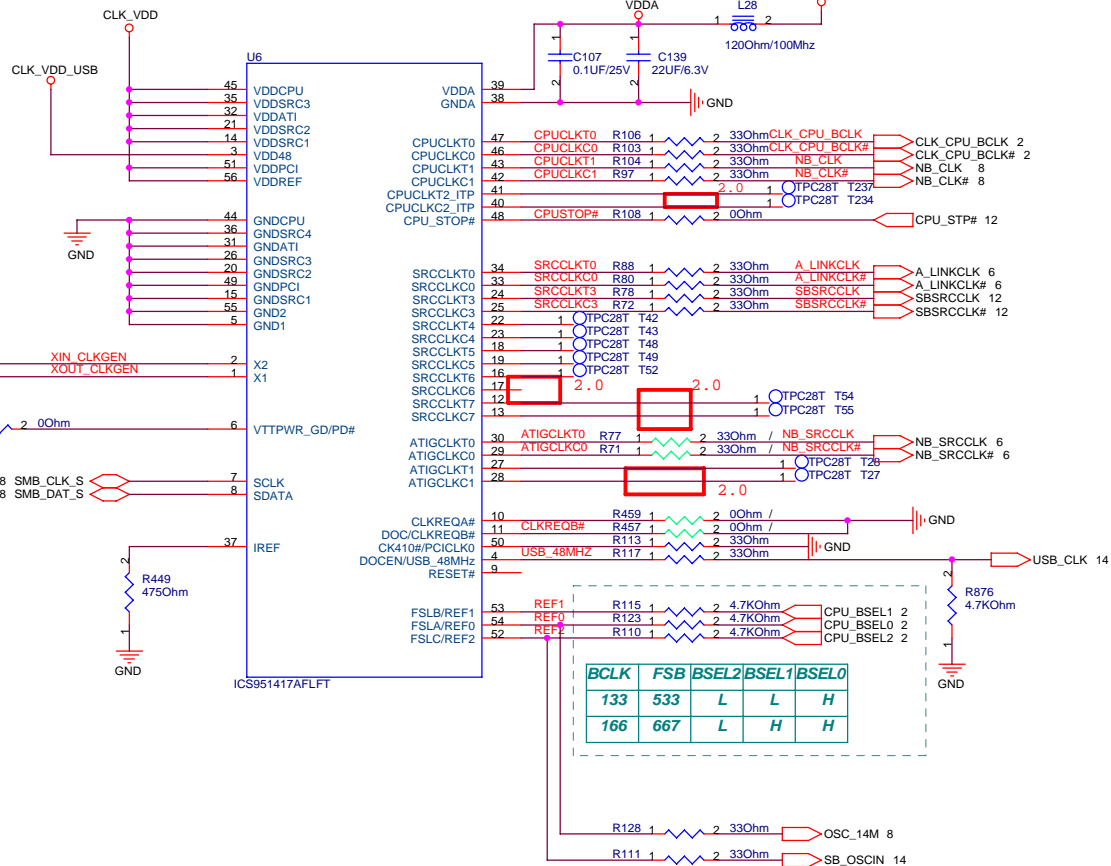
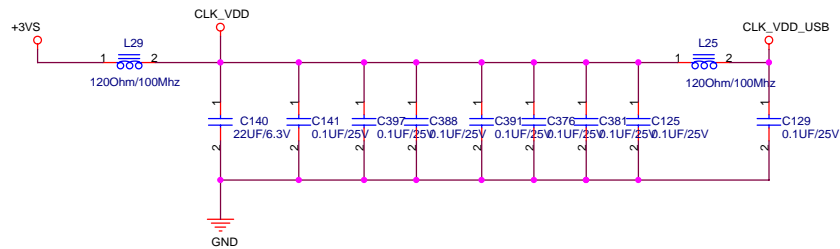
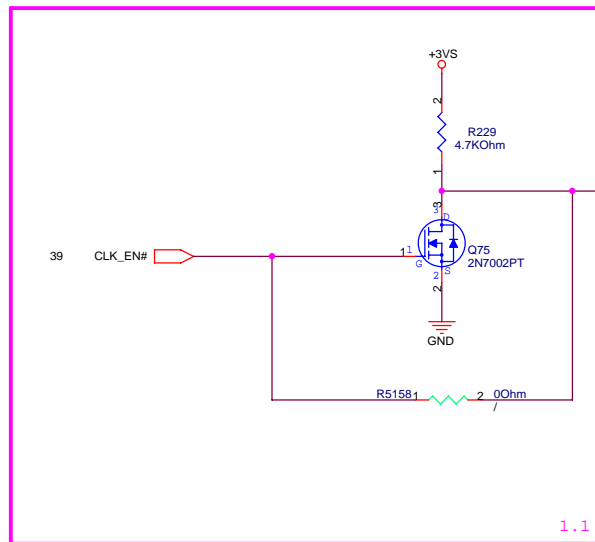
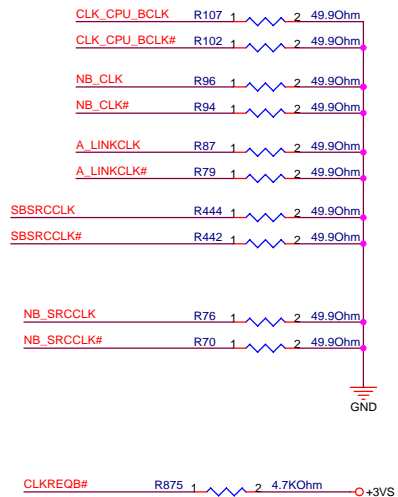
NOTE
1. USB CLK STRAPPING CHANGE

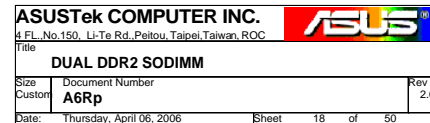
	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

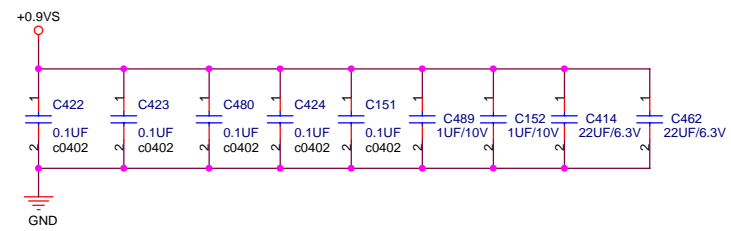
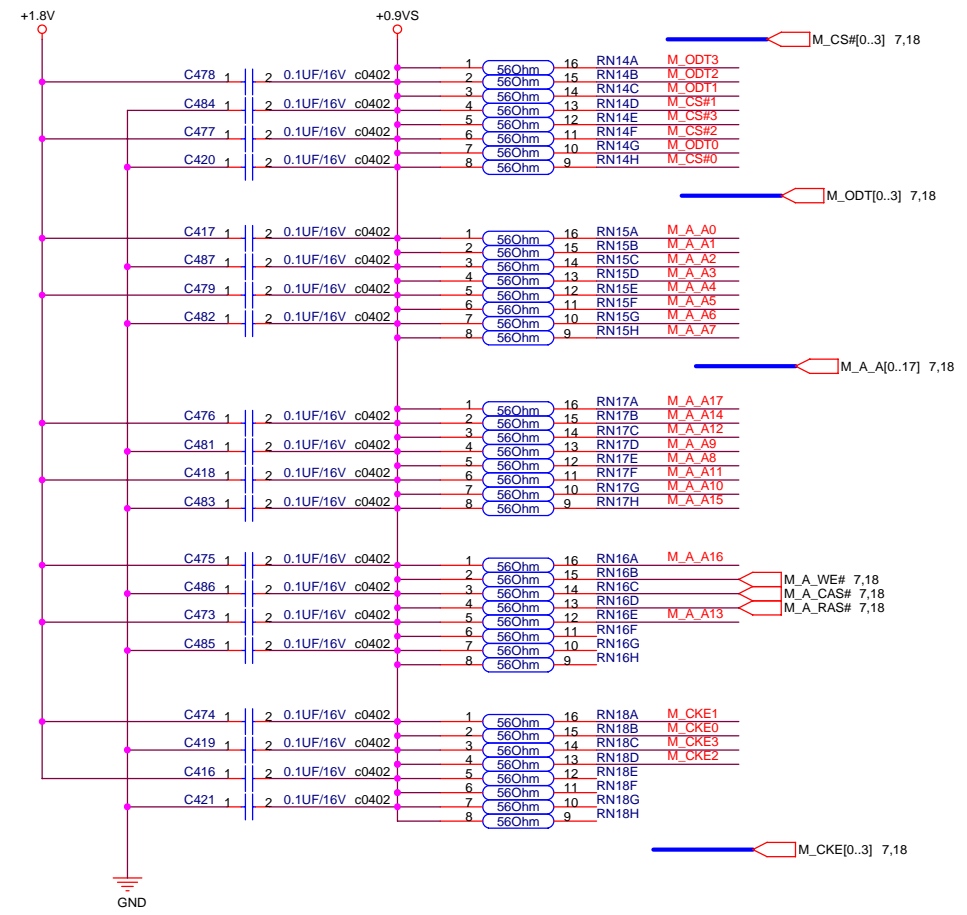
2. 14MHz CLOCK TYPE STRAPPING

	A11-A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

PLACE termination close to source IC



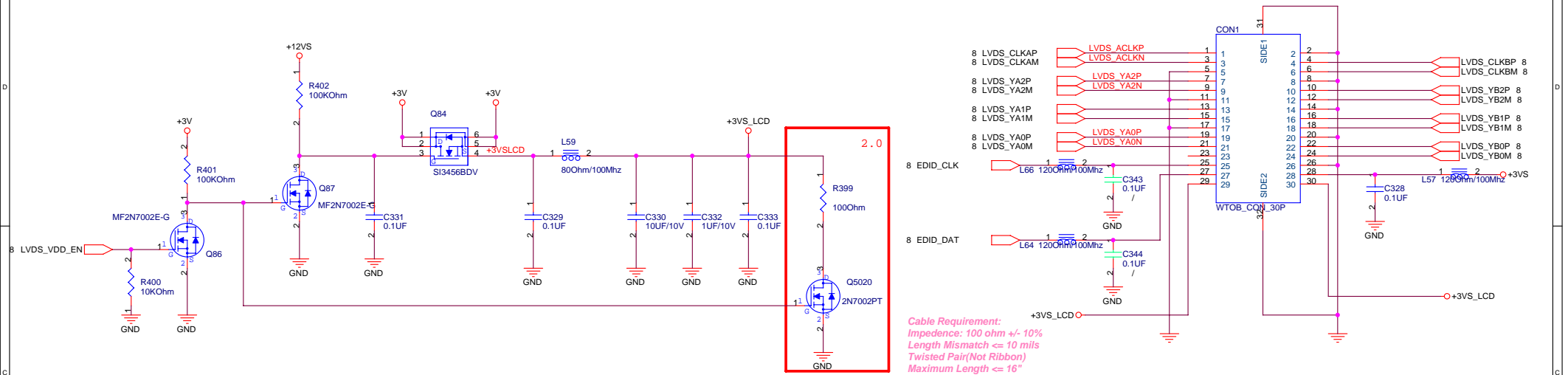




LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)

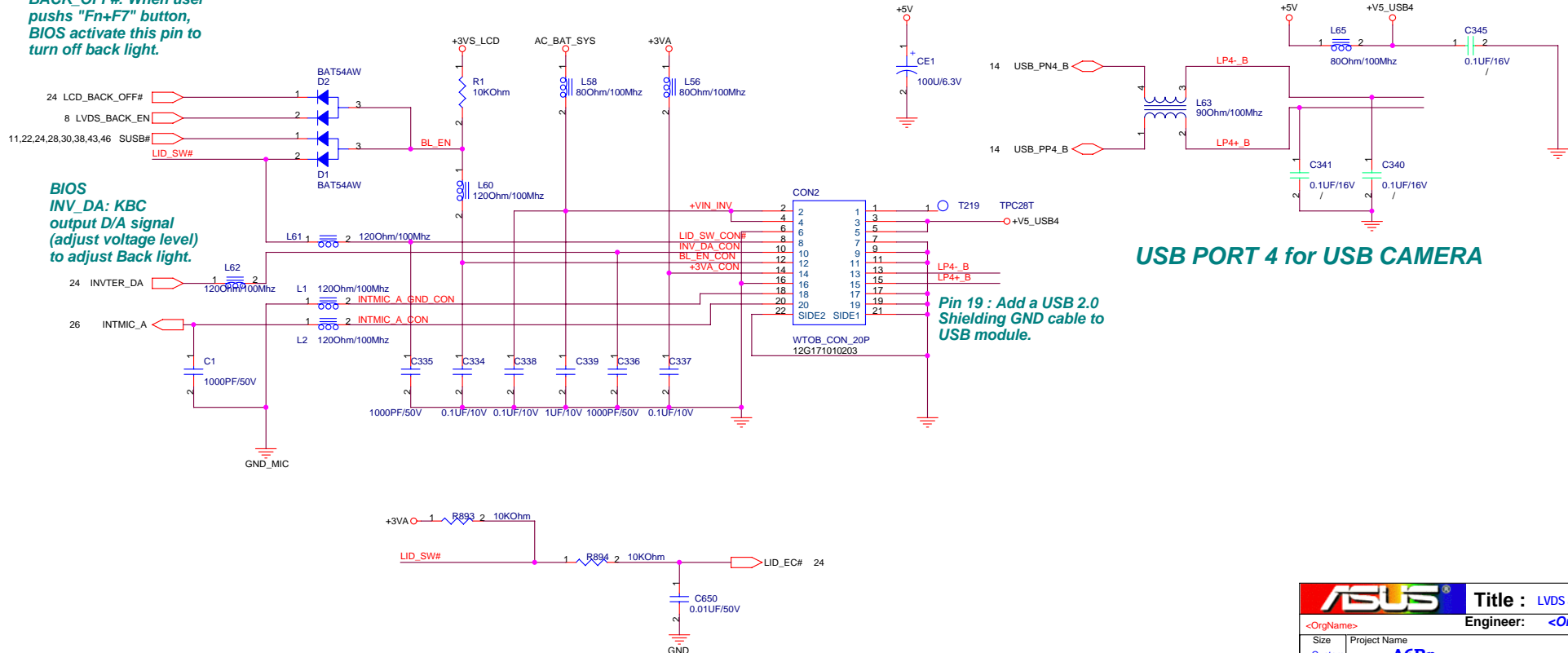
LCD LVDS Interface

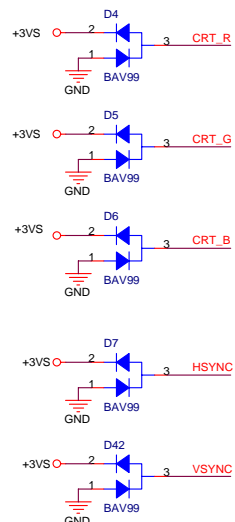


INVERTER Interface

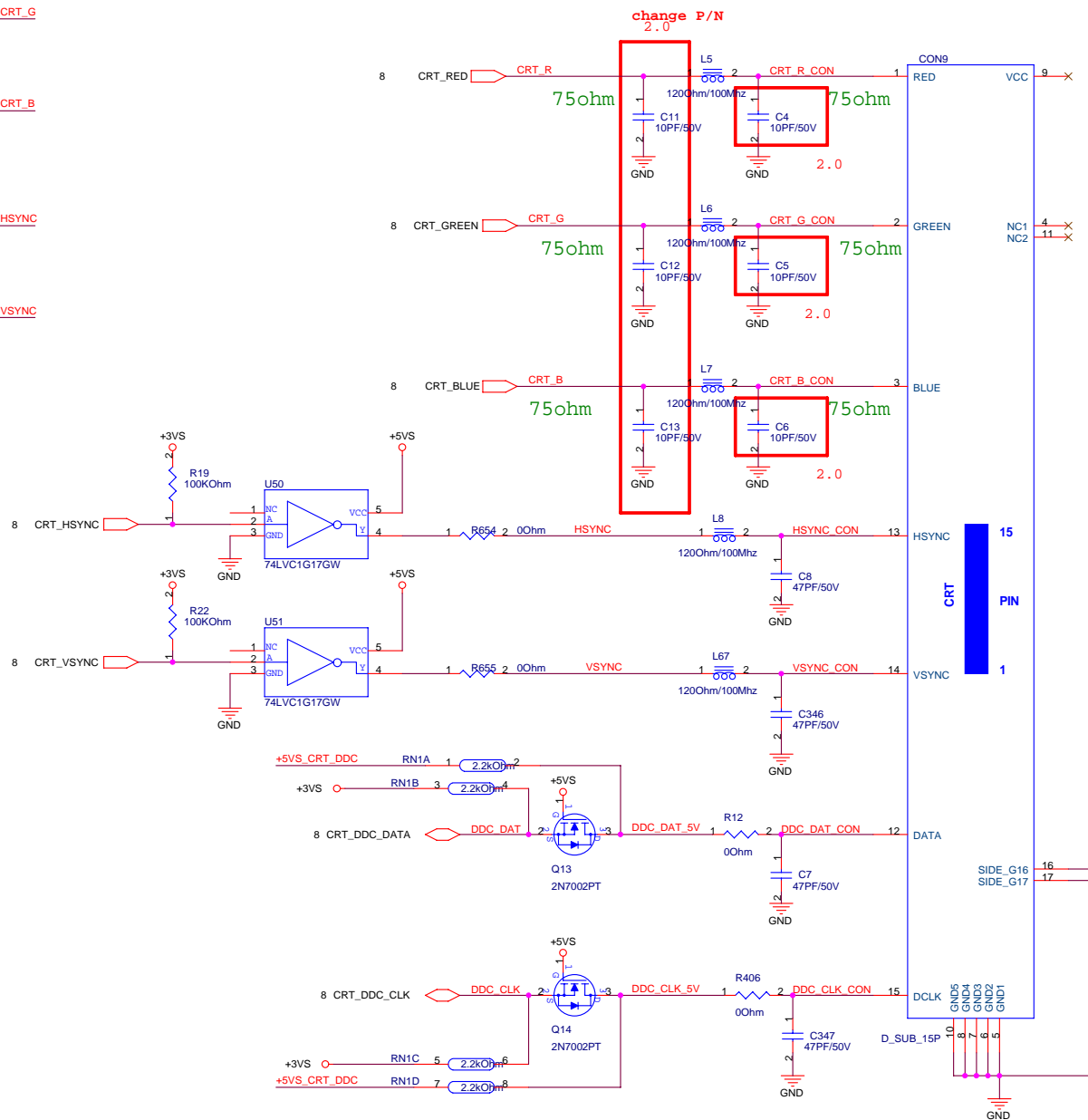
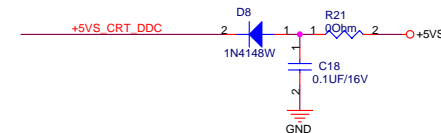
BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.

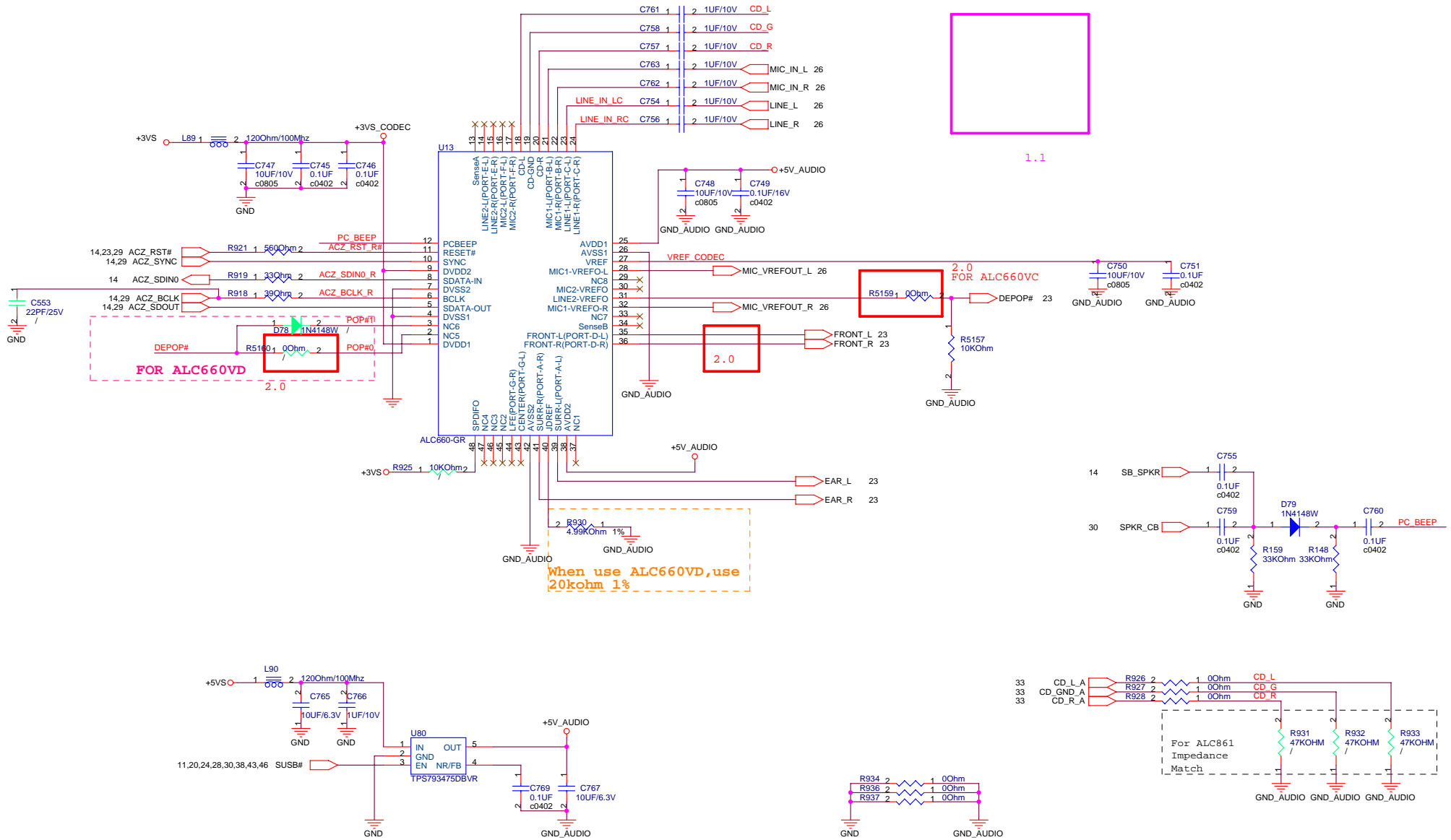
BIOS INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

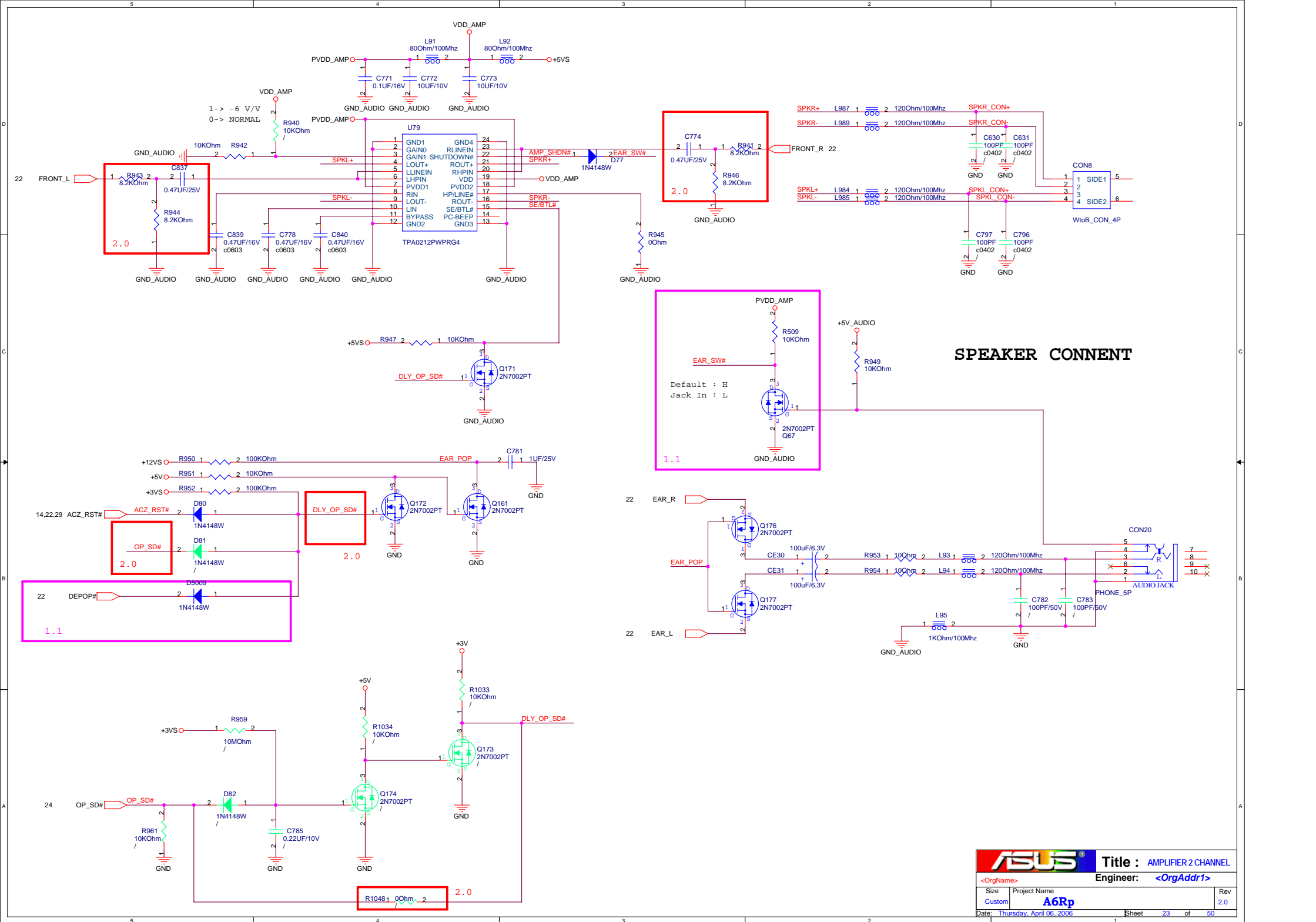




PLACE ESD
Diodes near
VGA port

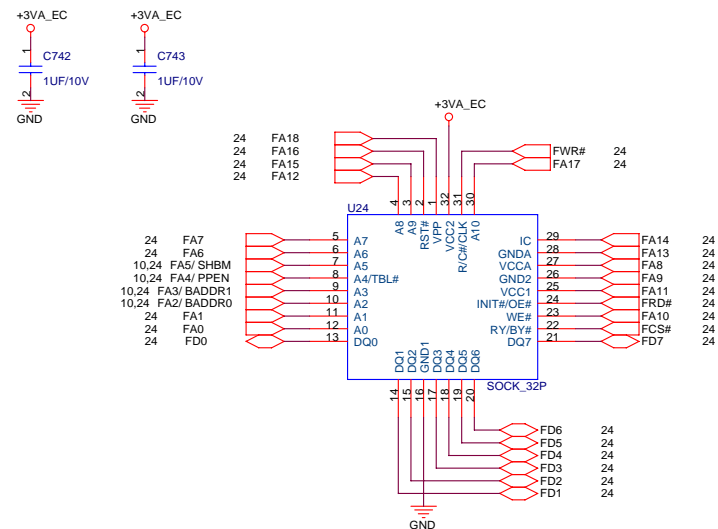


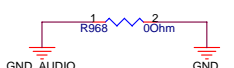
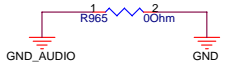
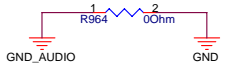
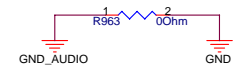
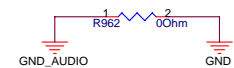




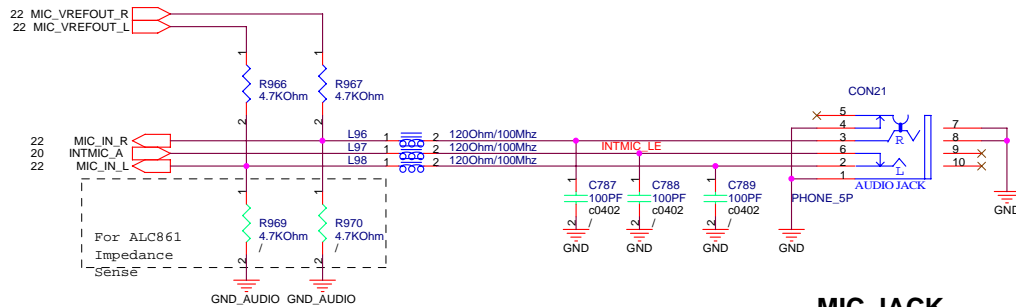
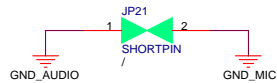
PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

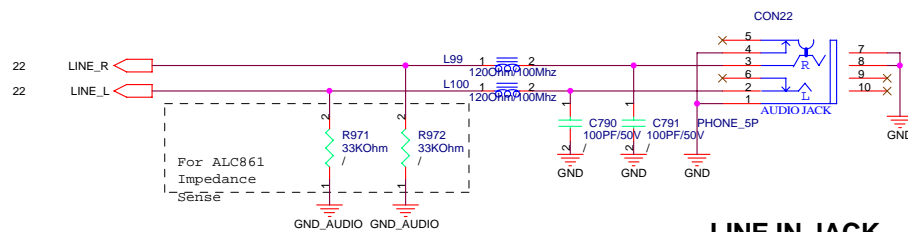




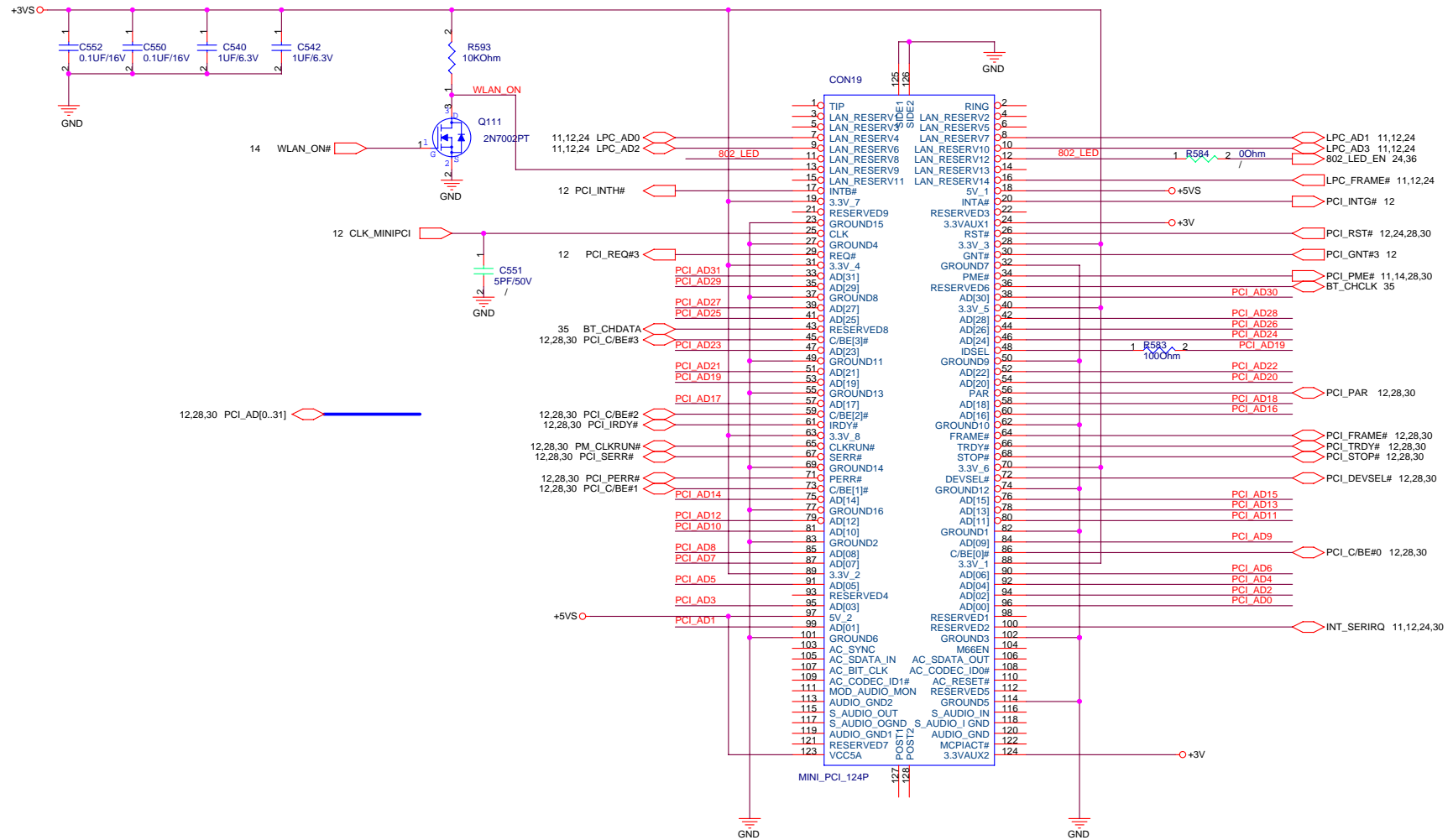
INTMIC_A:GND_AUDIO : W/P/X = 12/5/15mils

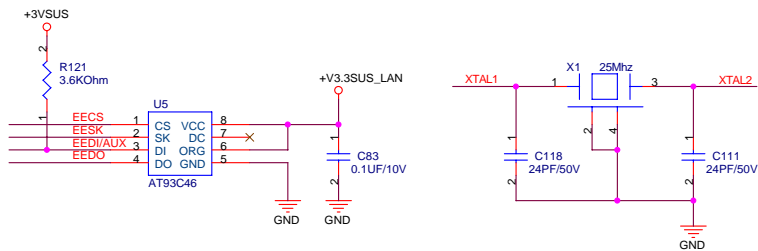


MIC JACK

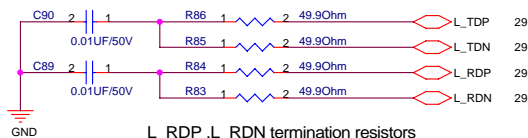


LINE IN JACK

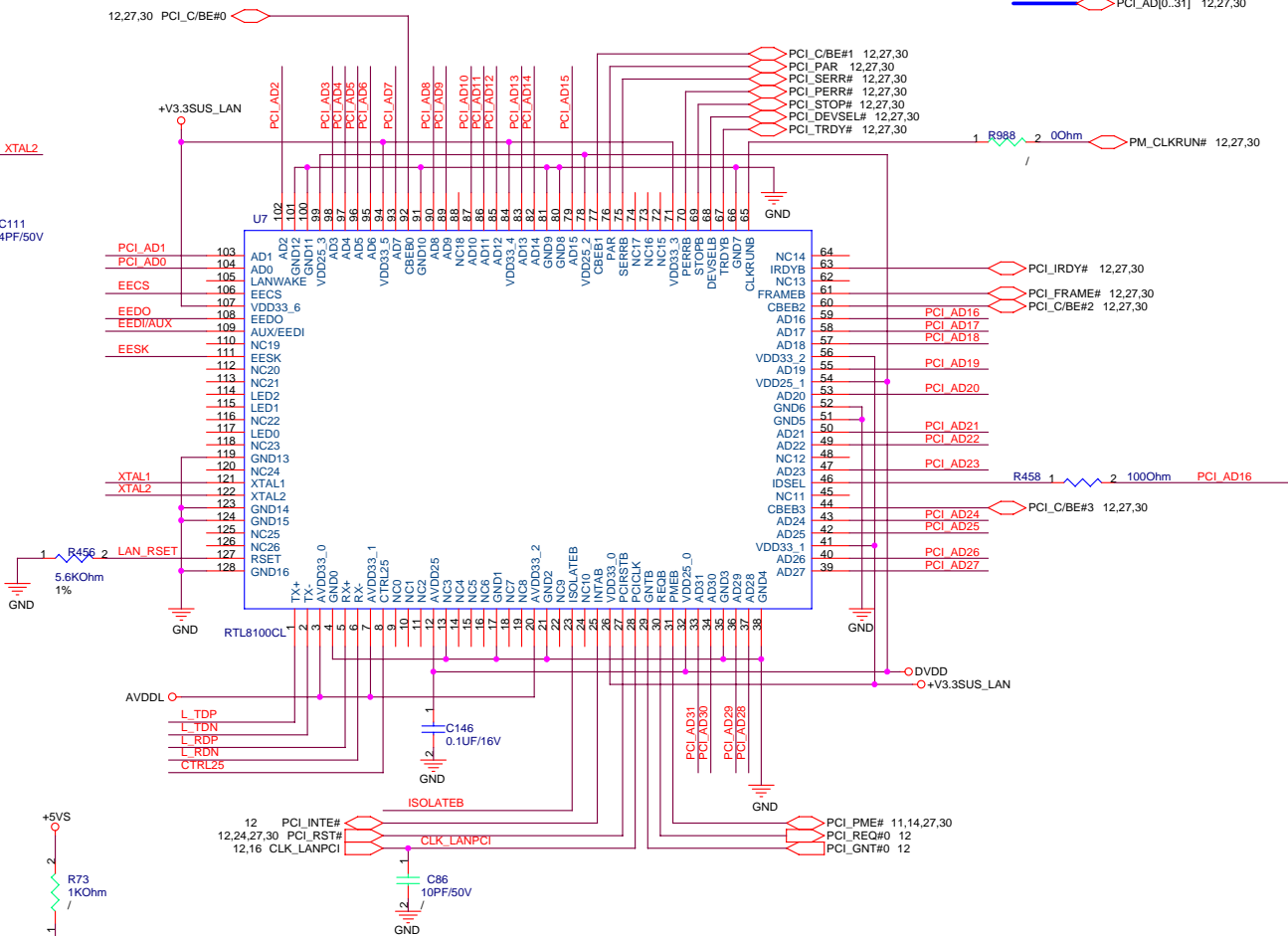
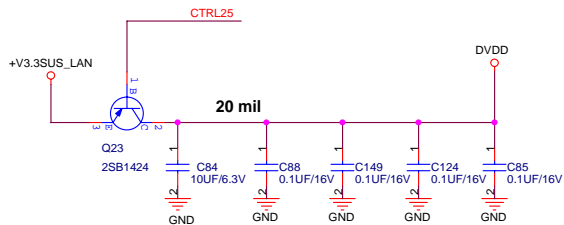
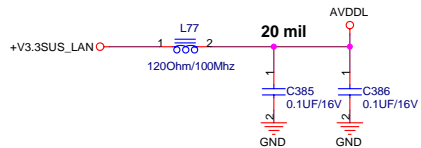


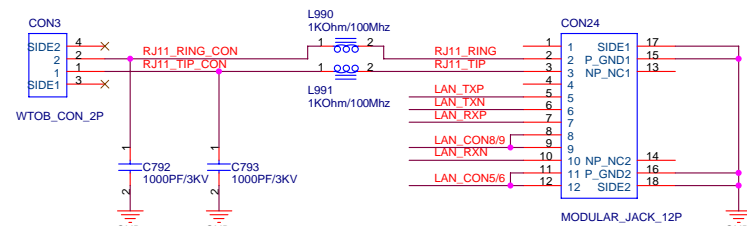
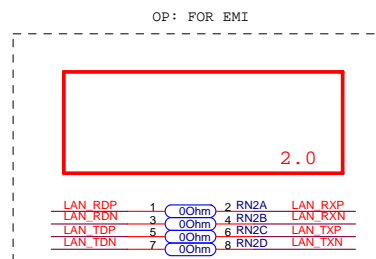


L_TDP ,L_TDN termination resistors
should be near chip



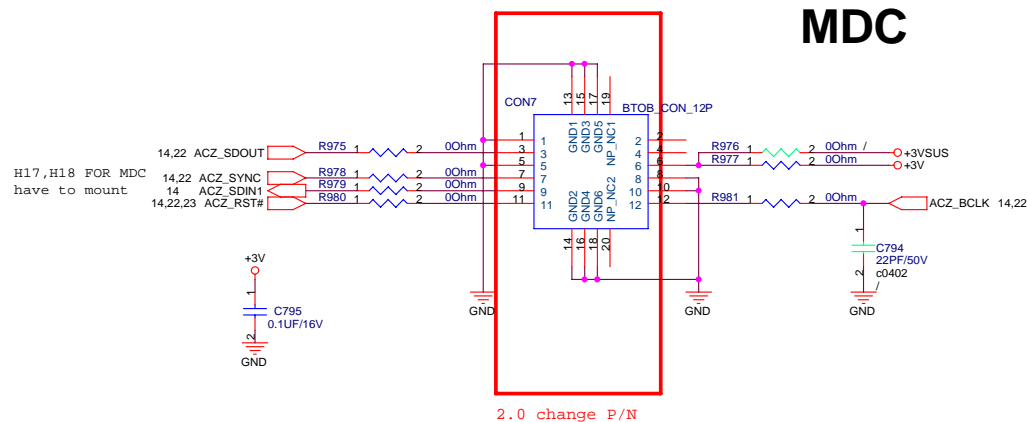
L_RDP ,L_RDN termination resistors
should be near transformer-U32

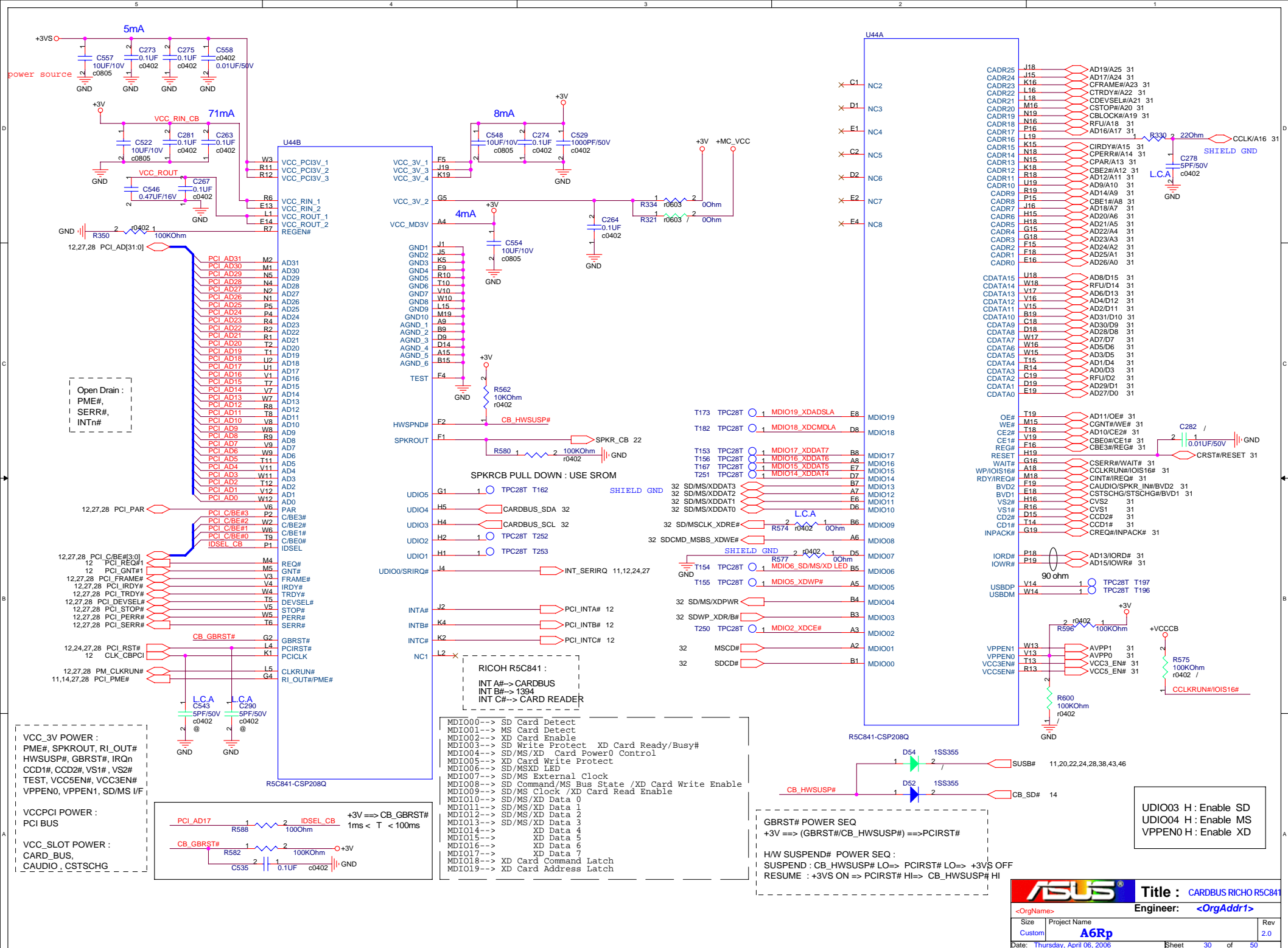


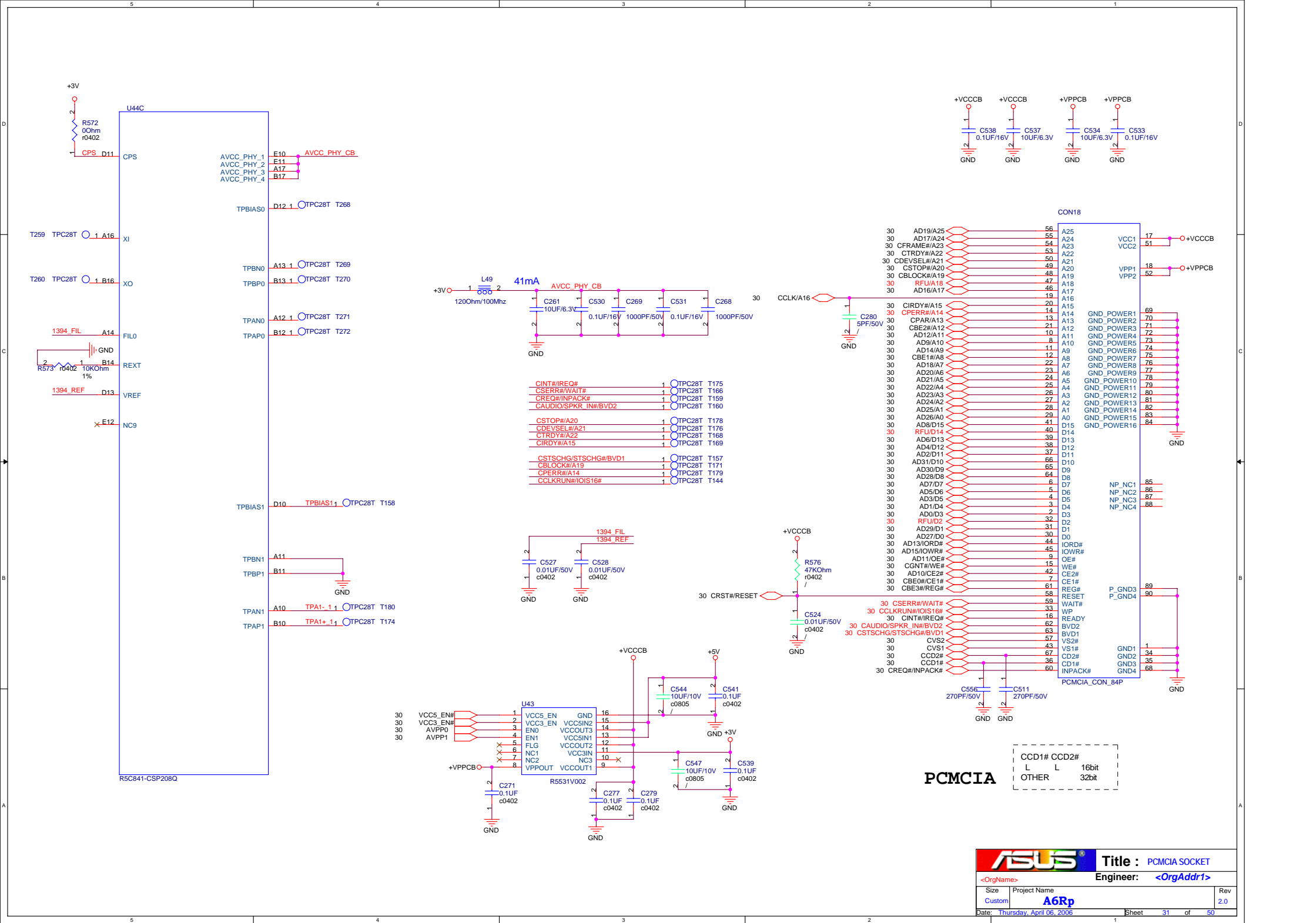


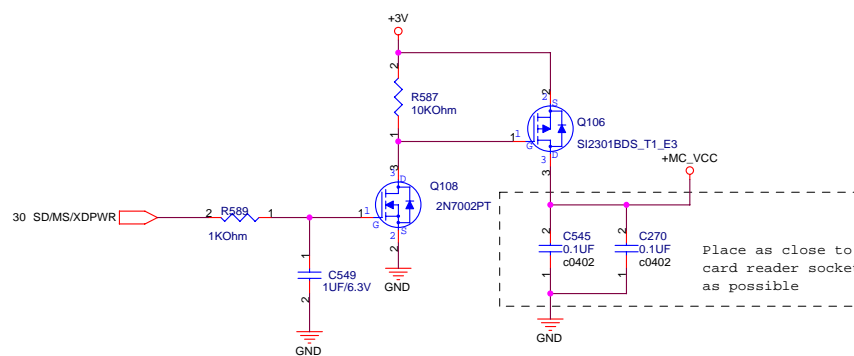
MDC

MDC



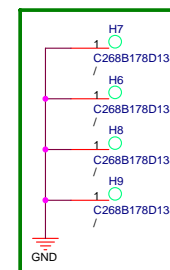
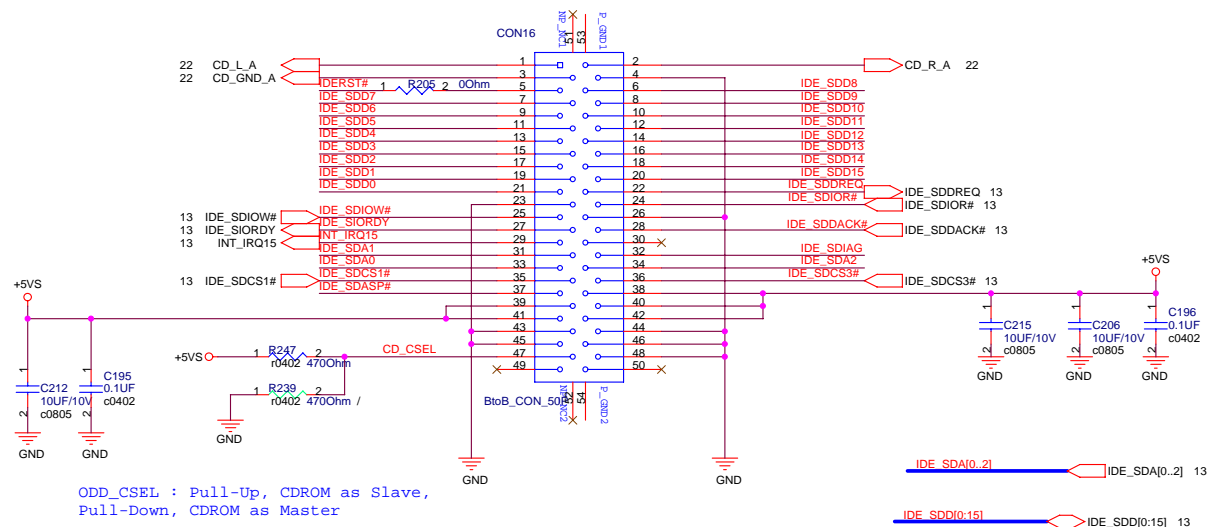




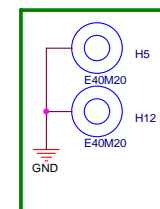


[illegible]

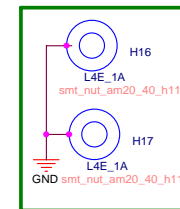
CD-ROM



CPU

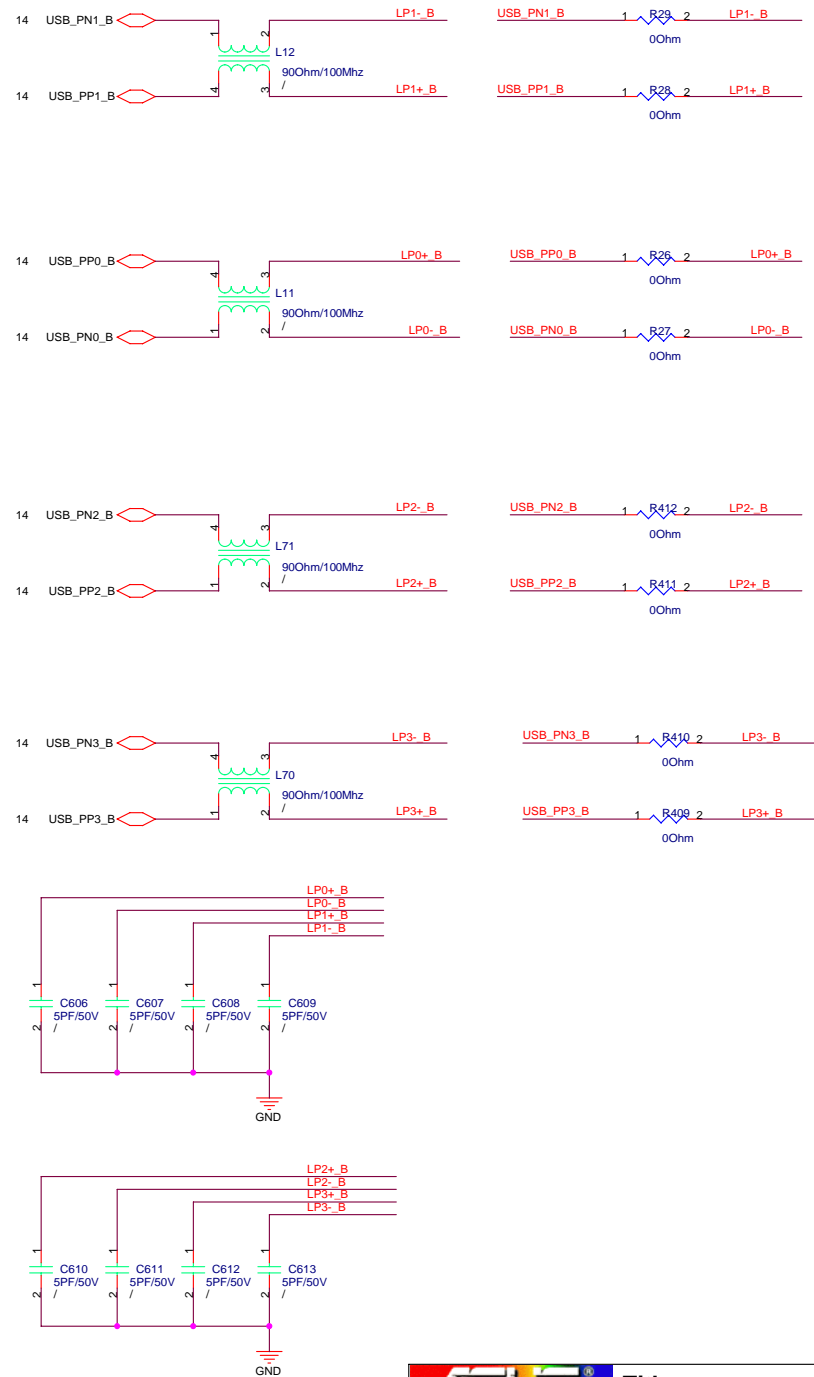
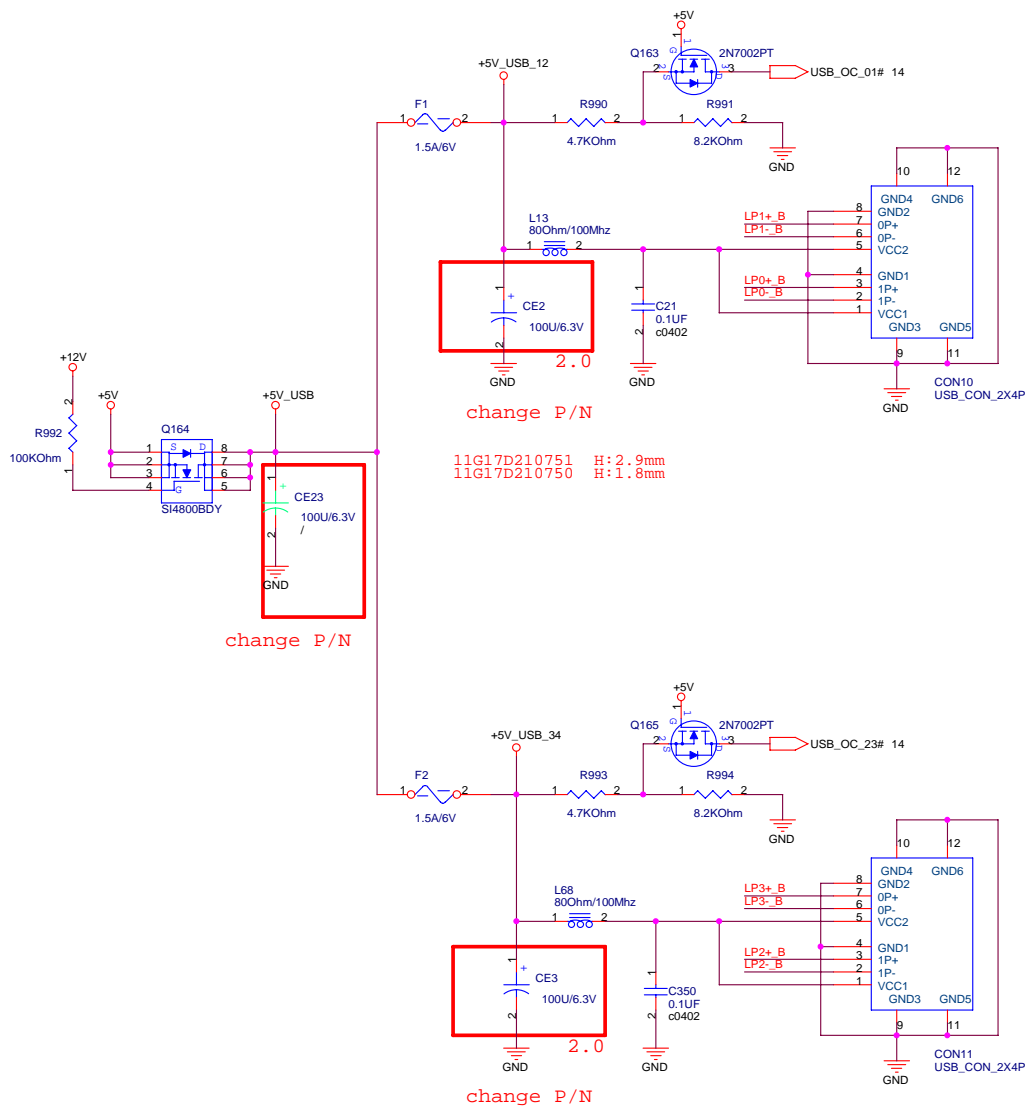


VGA

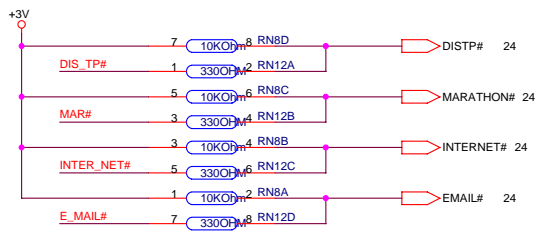
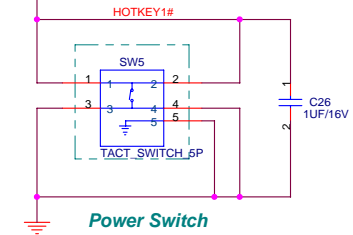
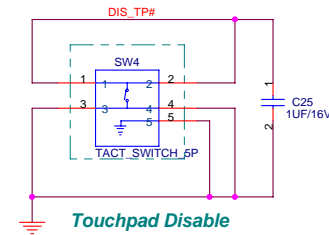
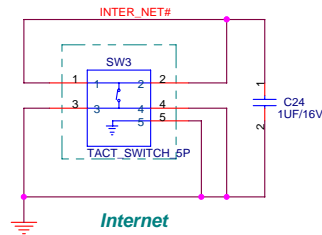
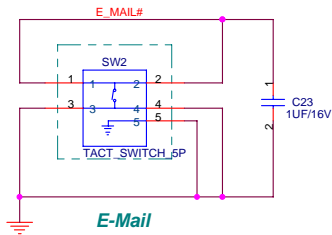
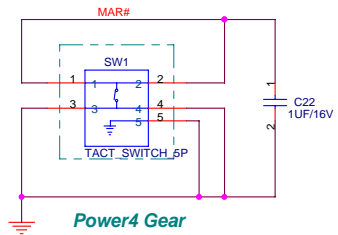


MDC

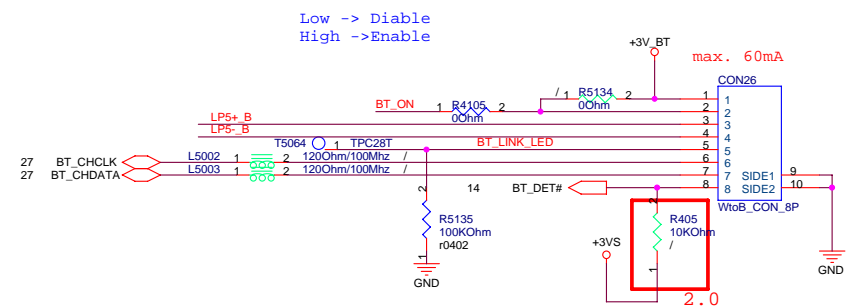
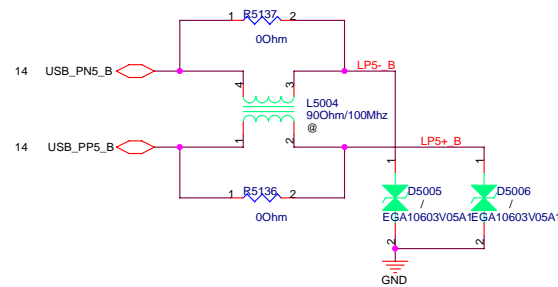
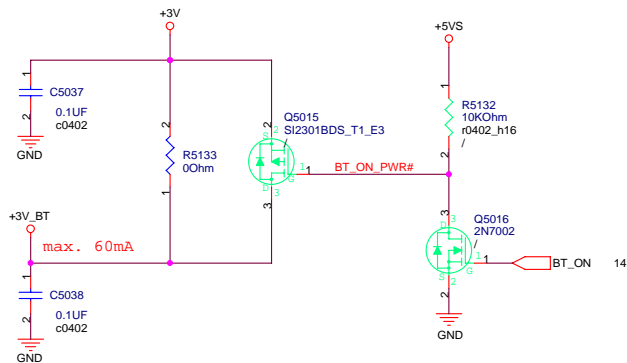
USB

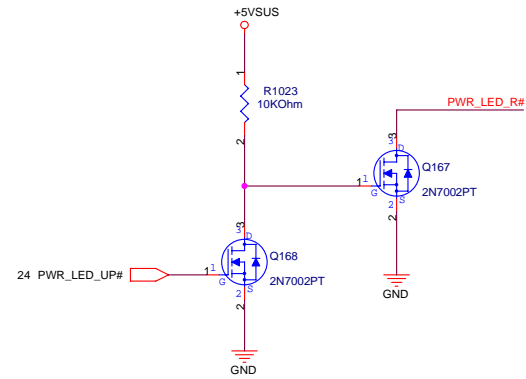


FUNCTION KEY

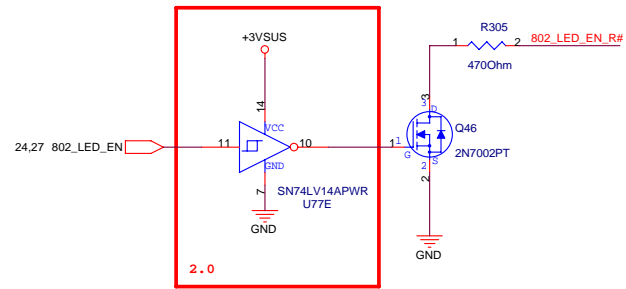


BT ON/OFF Control

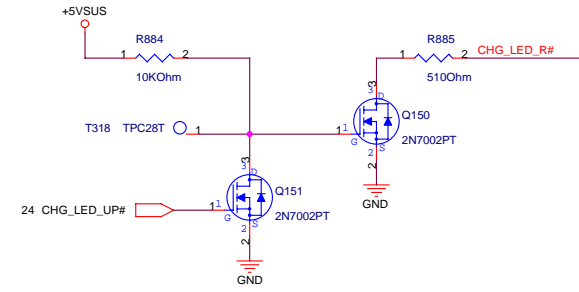




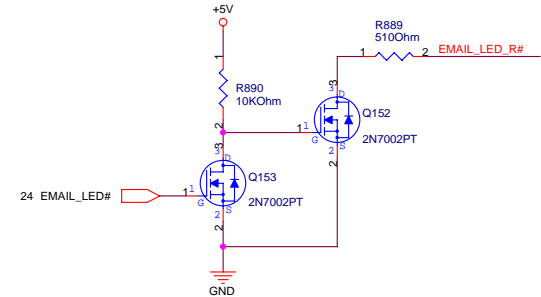
POWER_LED



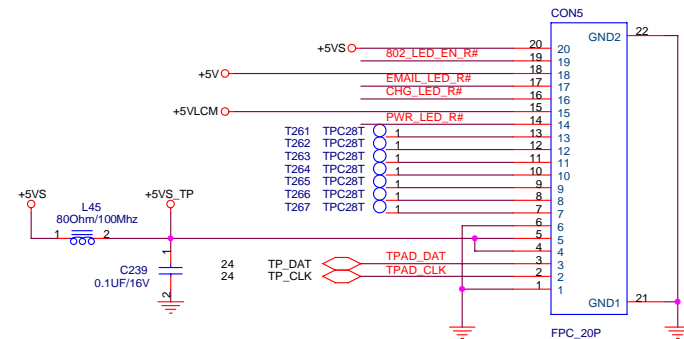
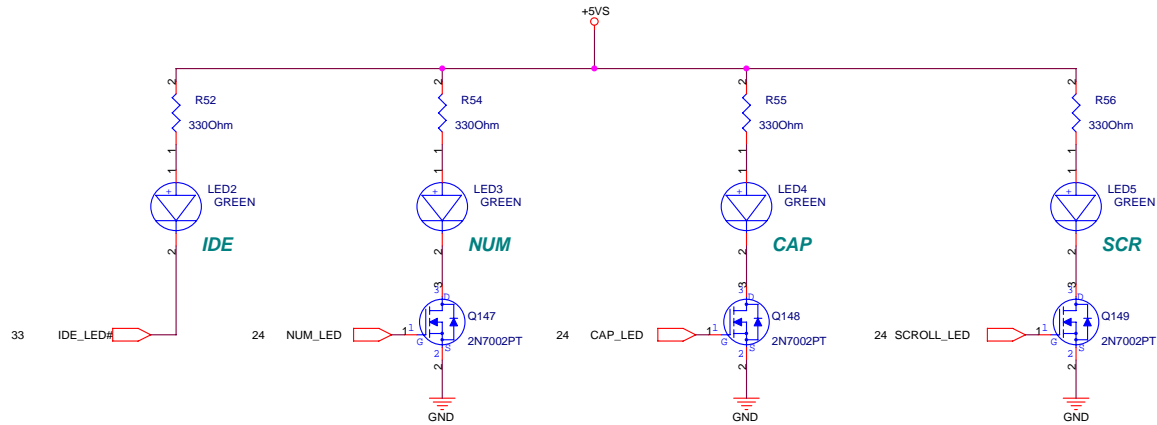
802_LED



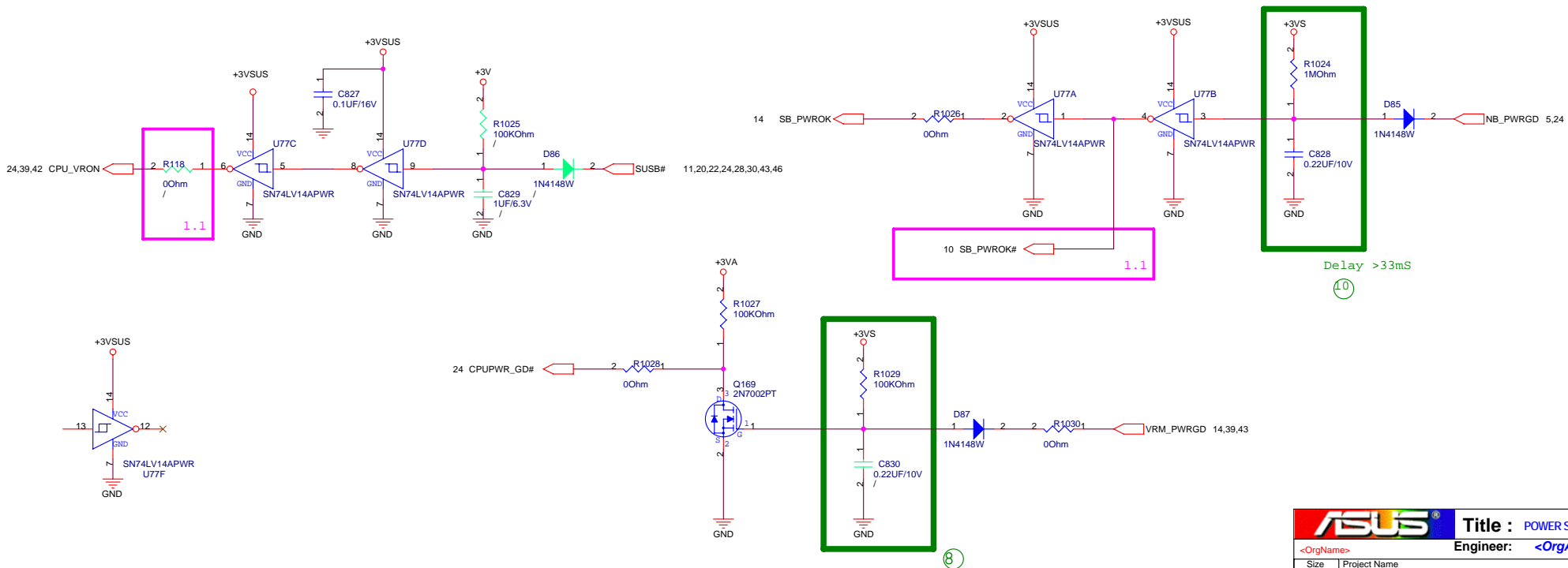
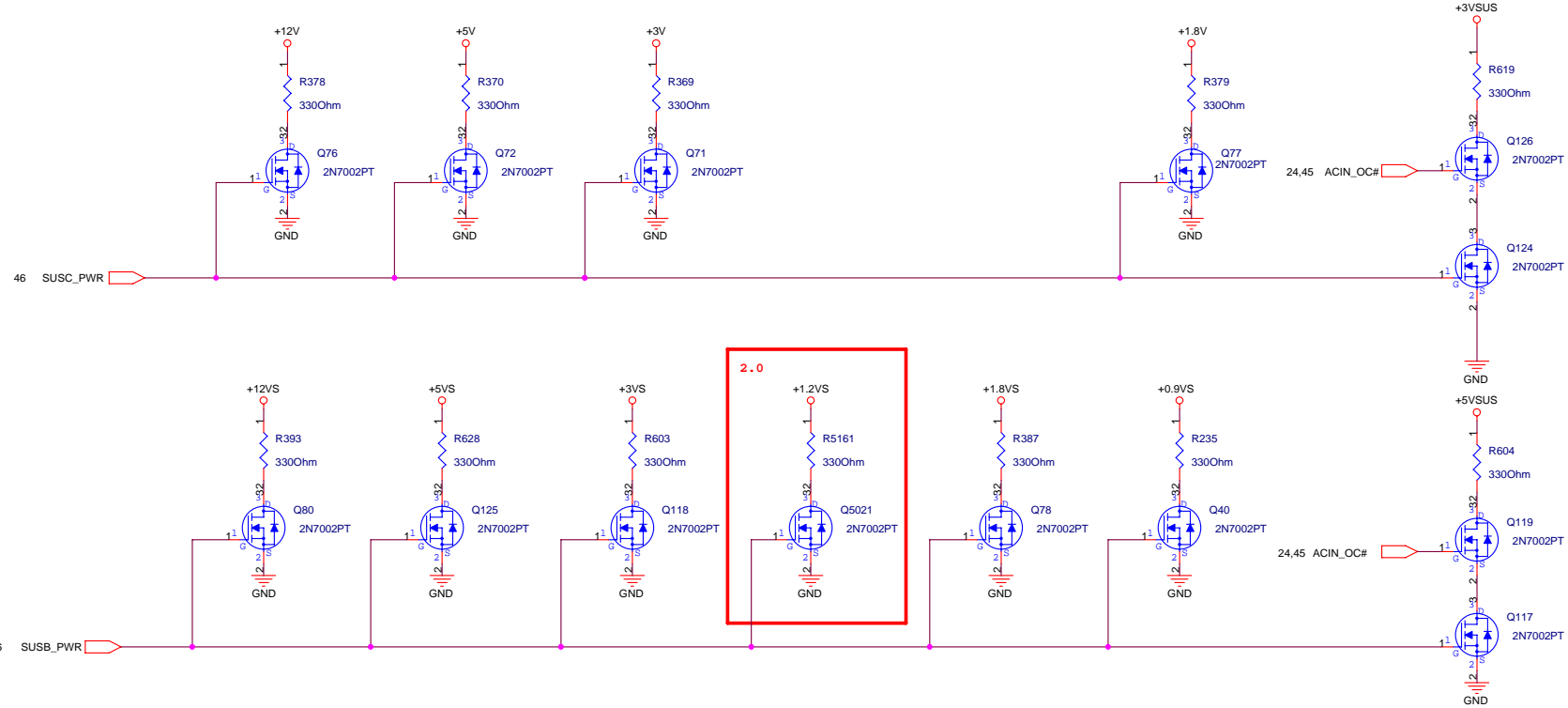
CHG_LED

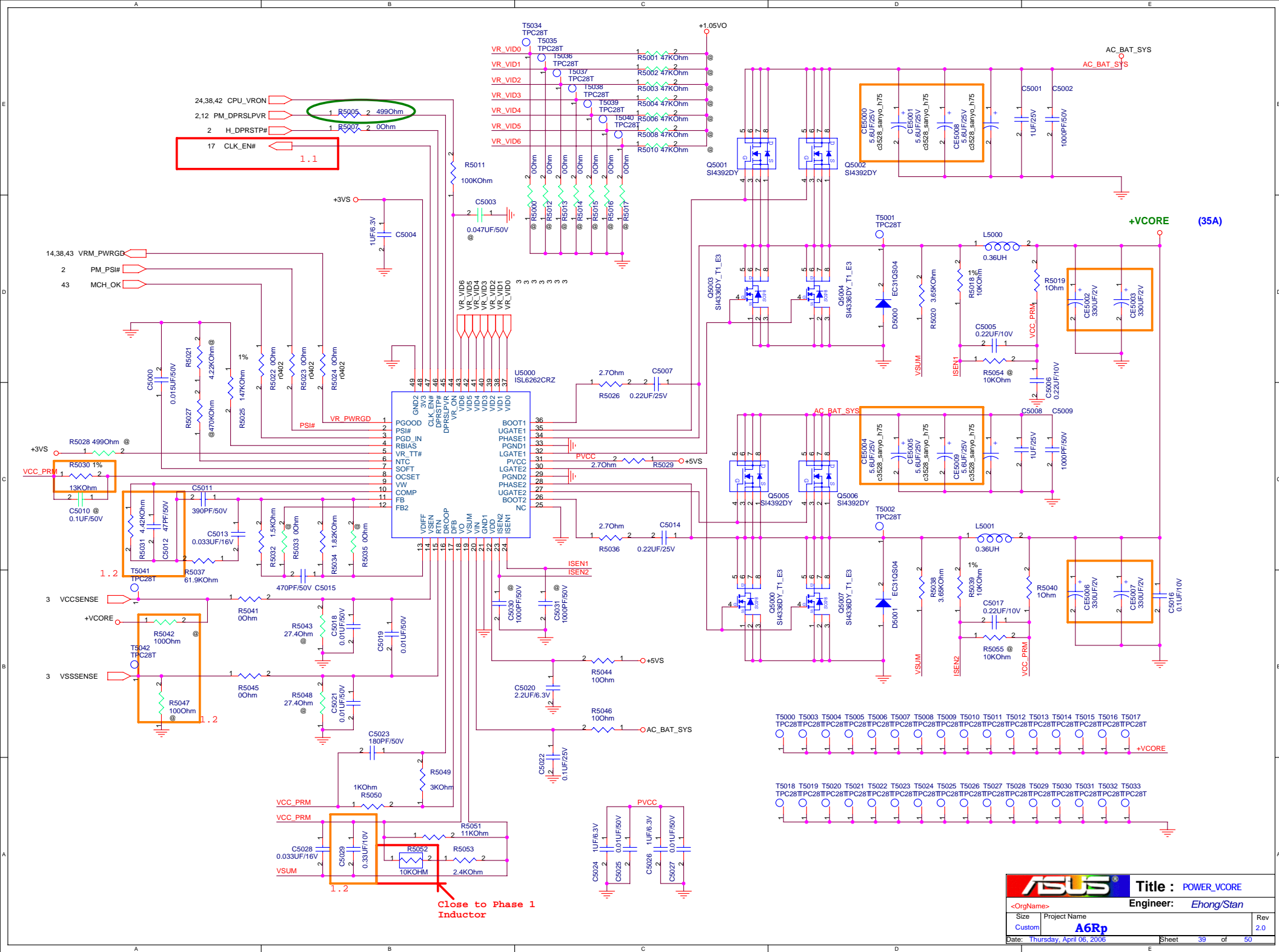


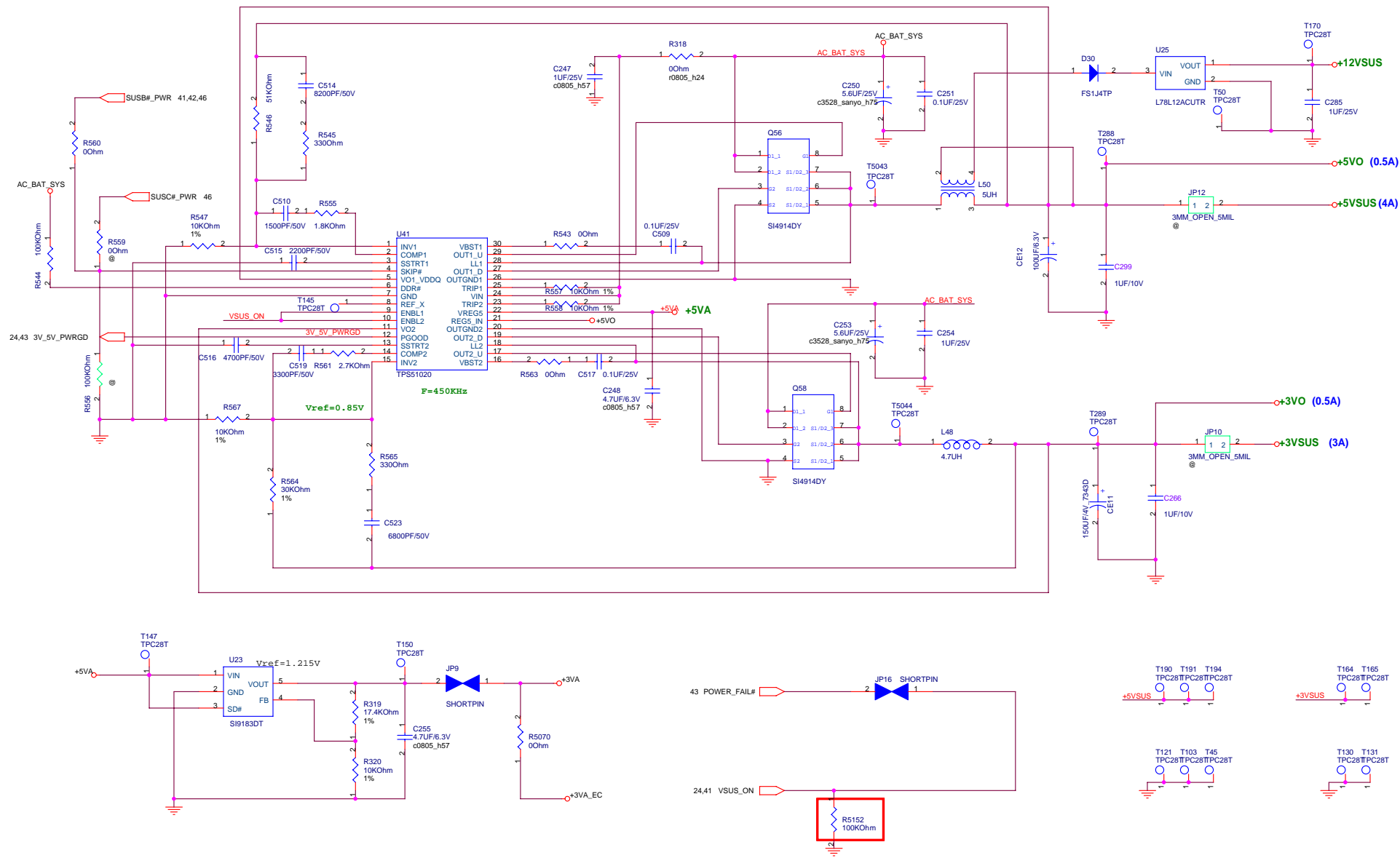
EMAIL_LED

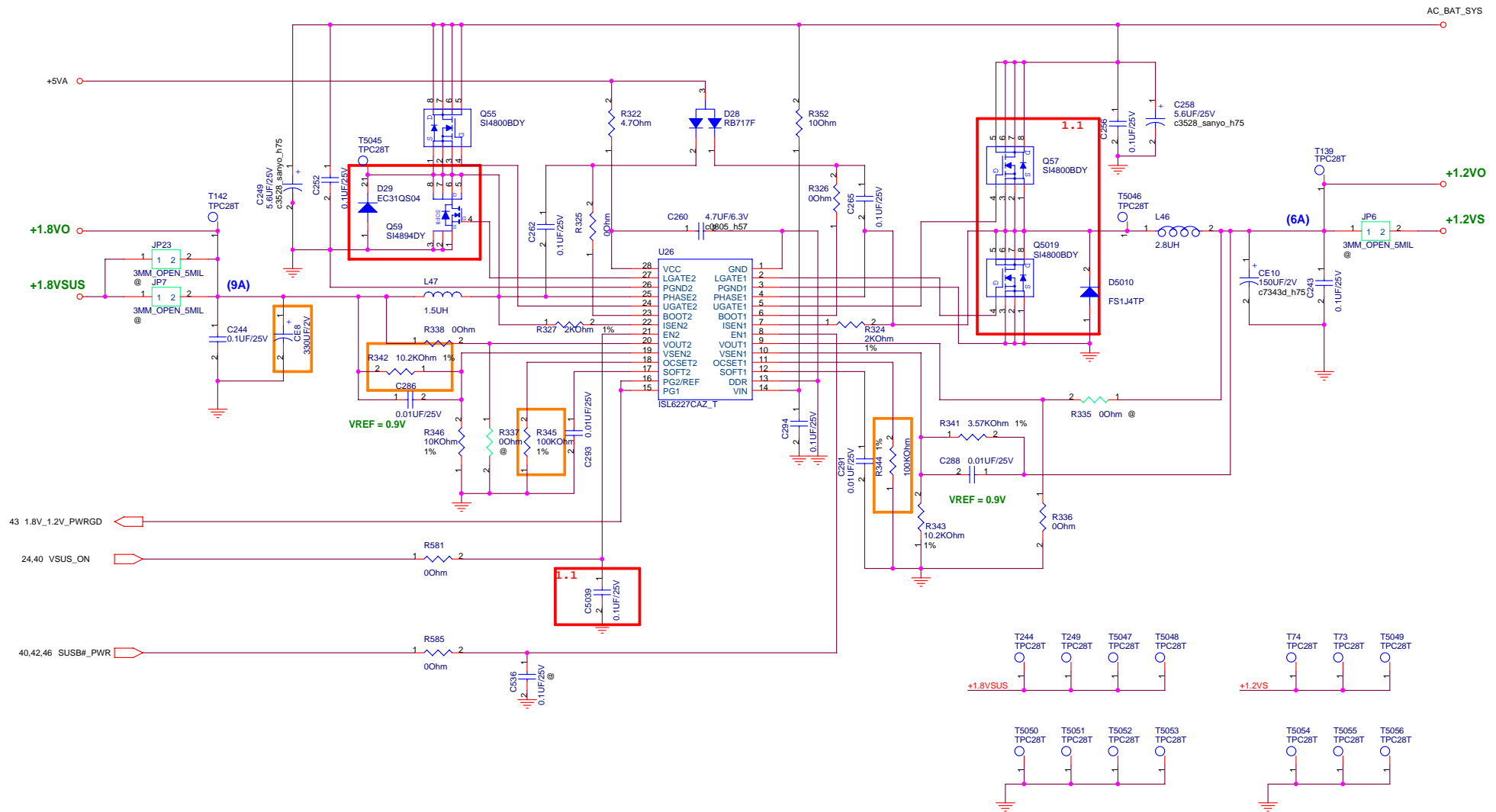


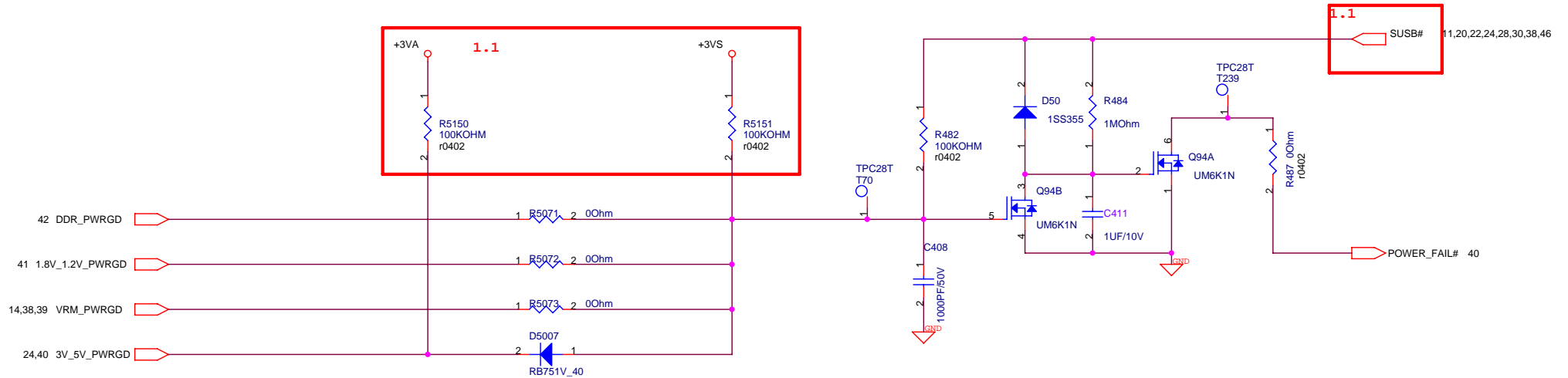
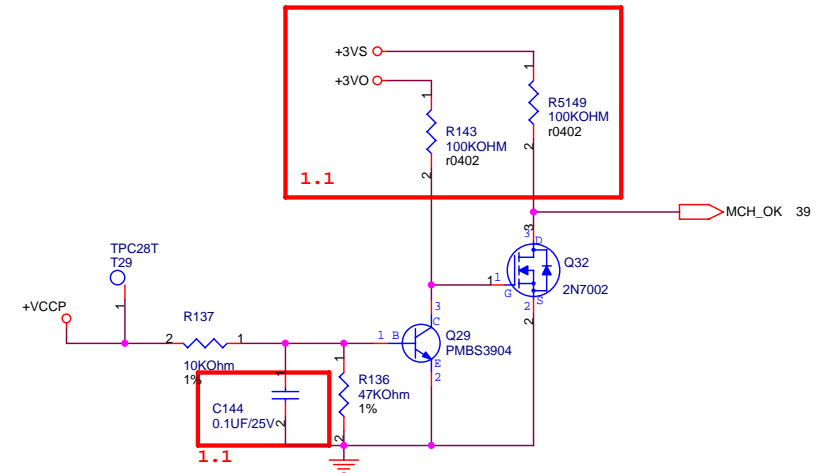
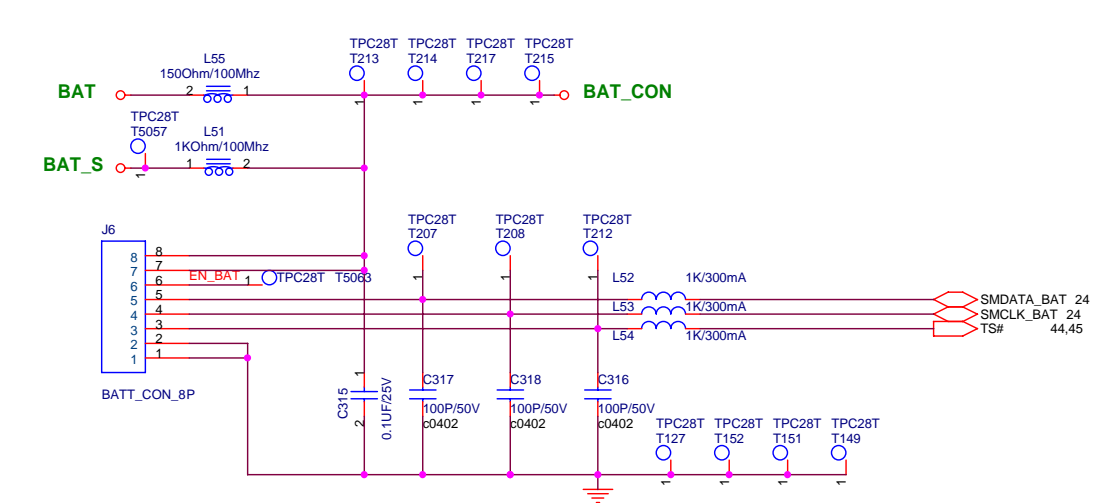


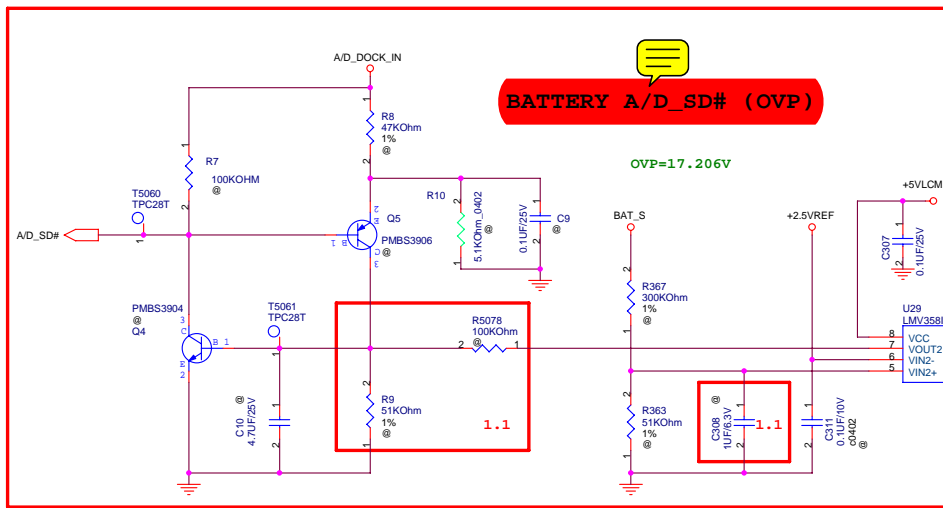




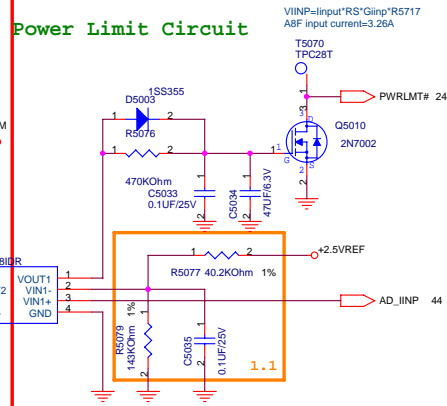




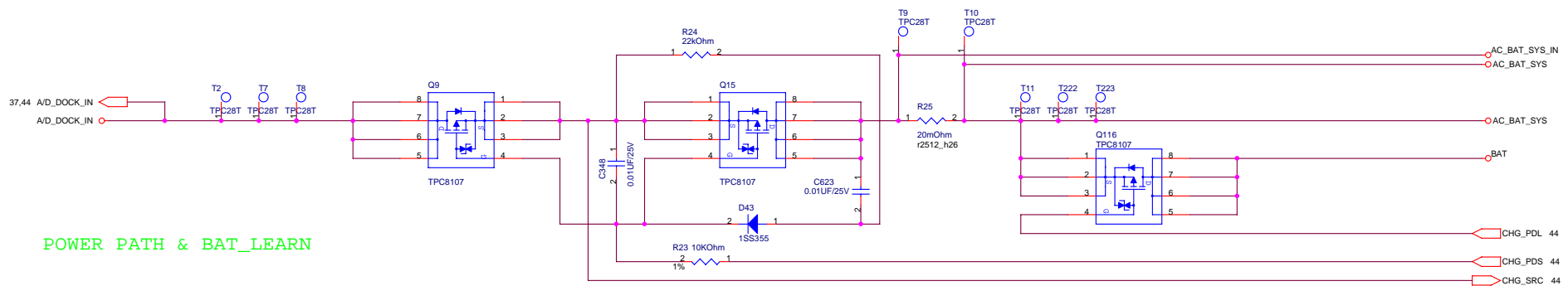
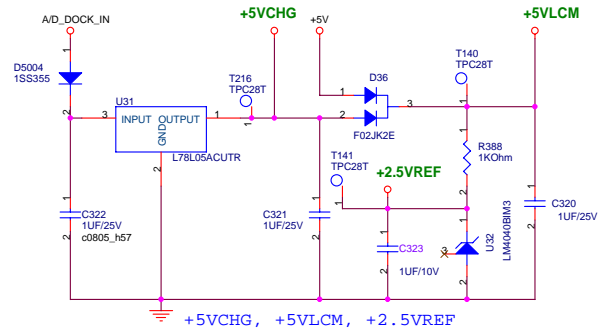
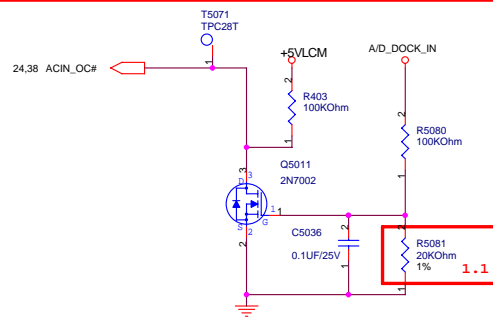
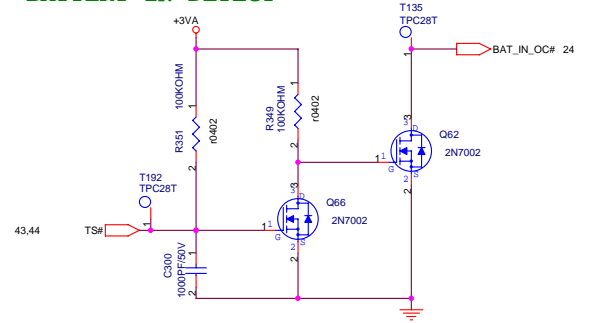


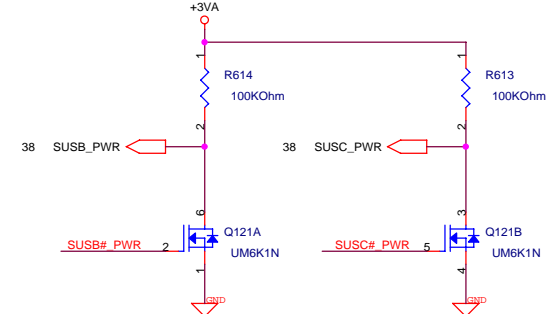
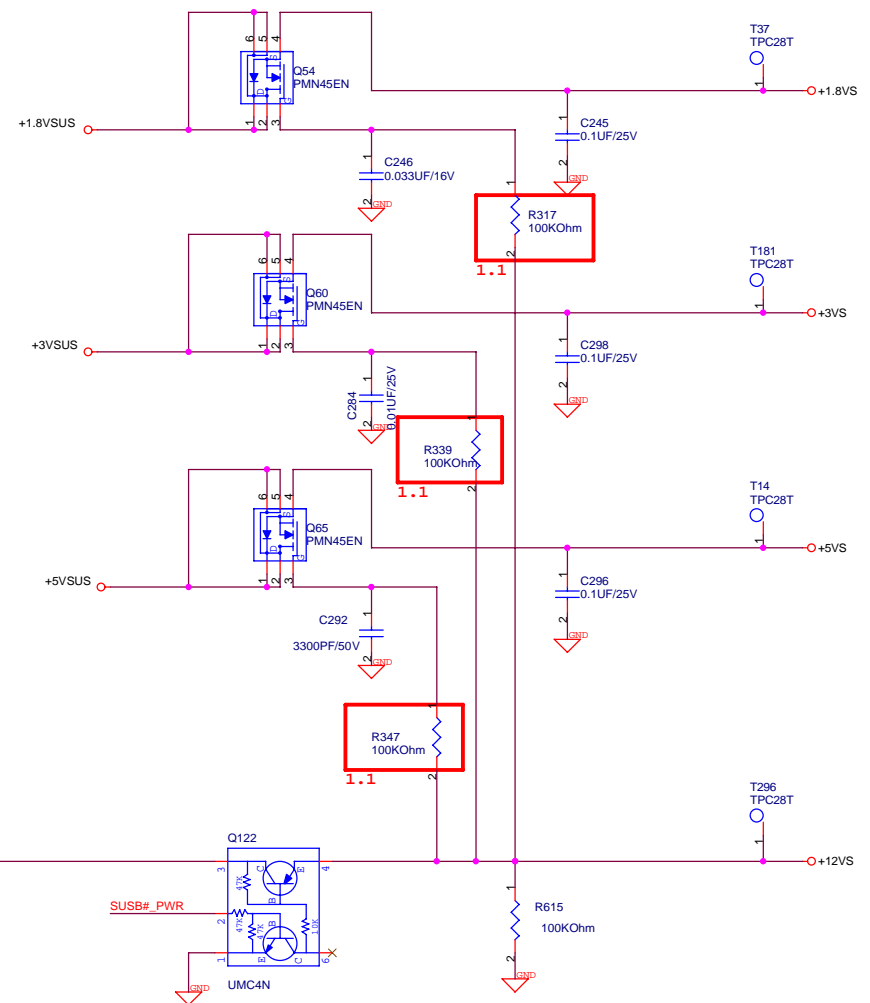
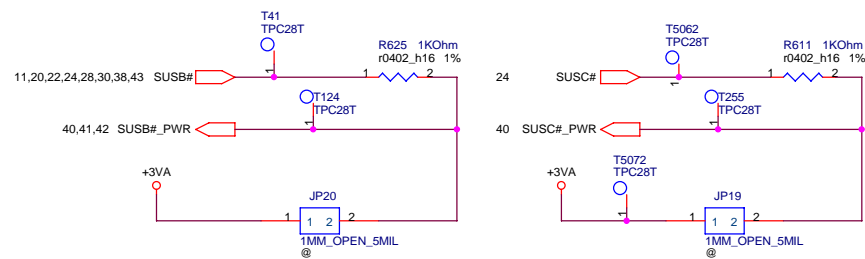
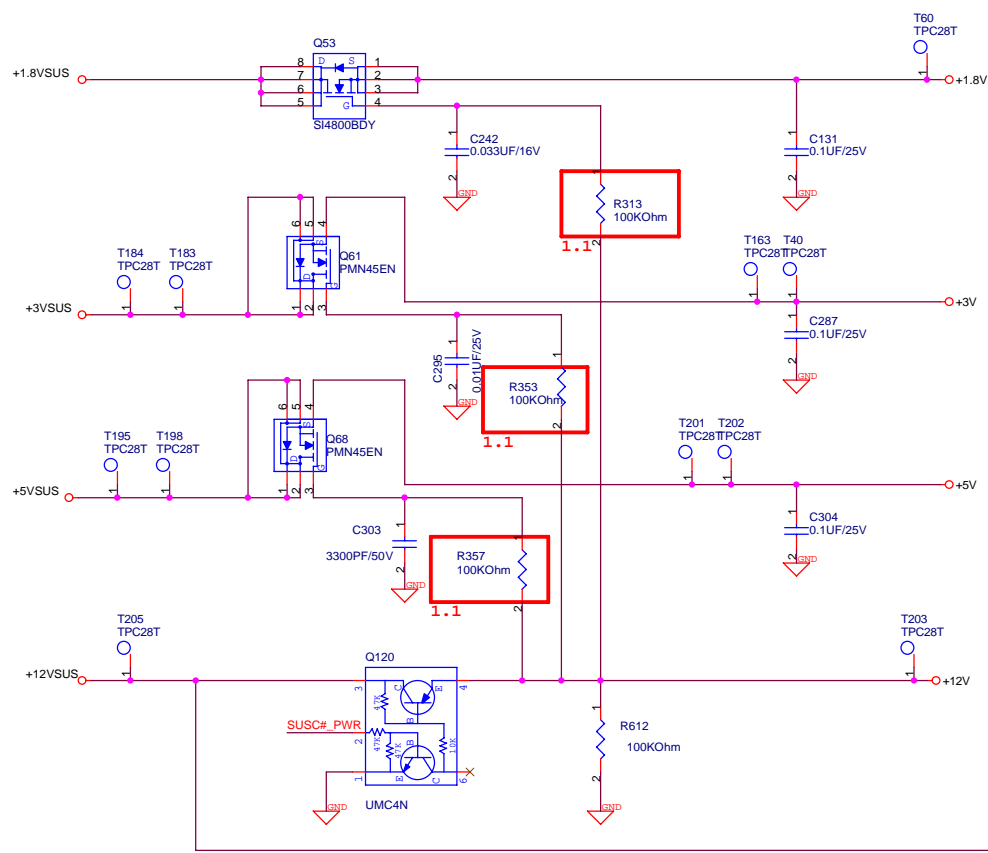


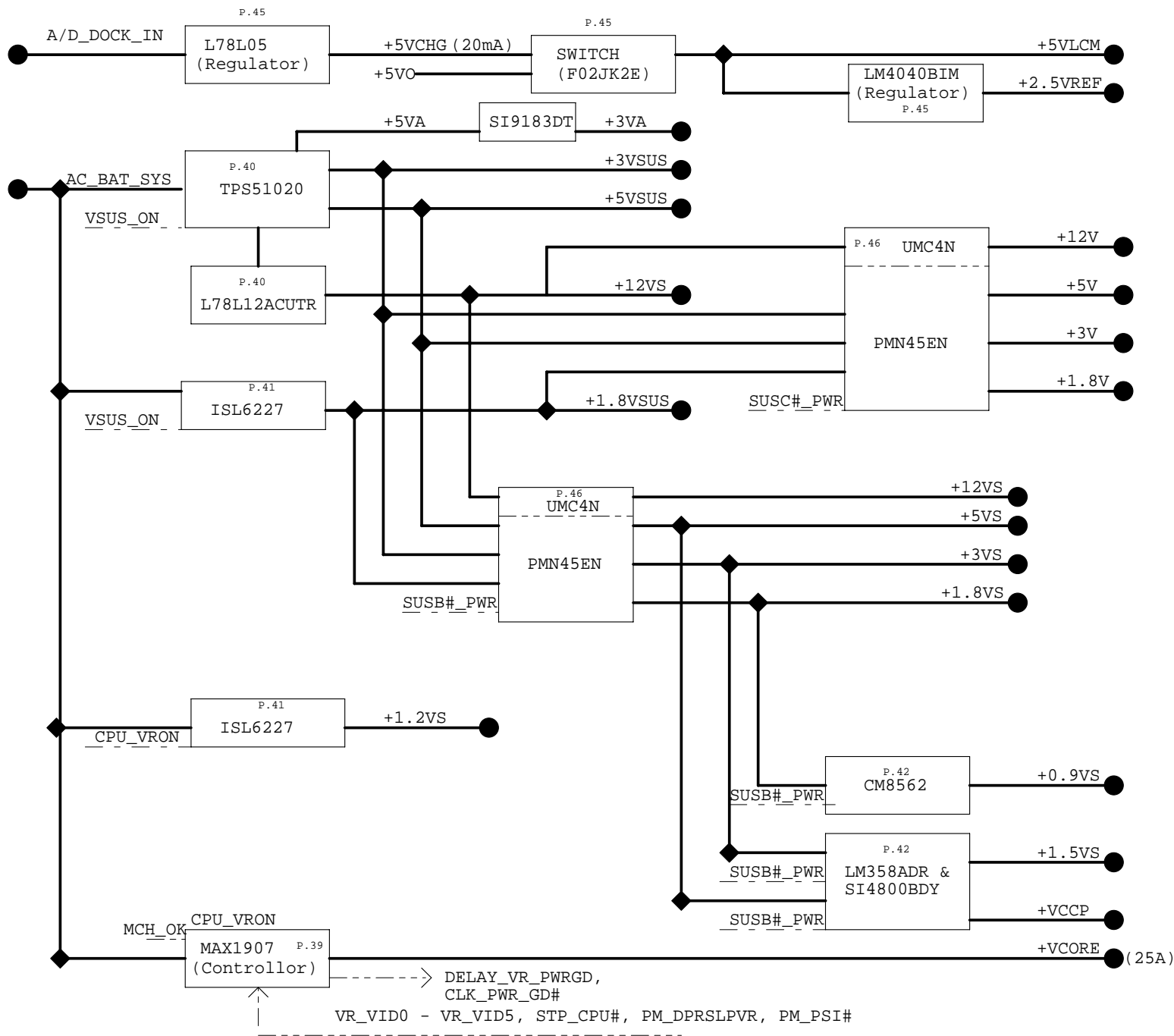
Power Limit Circuit



BATTERY IN DETECT







PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	C
CARDBUS	AD17	1	A
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	FWH_WP#
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	802_LED_EN
GPIO 12	I/O	S0	WLAN_ON#
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Rev	Date	Description
1.0	05/03/01	1. Initial release.

Rev	Date	Description

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