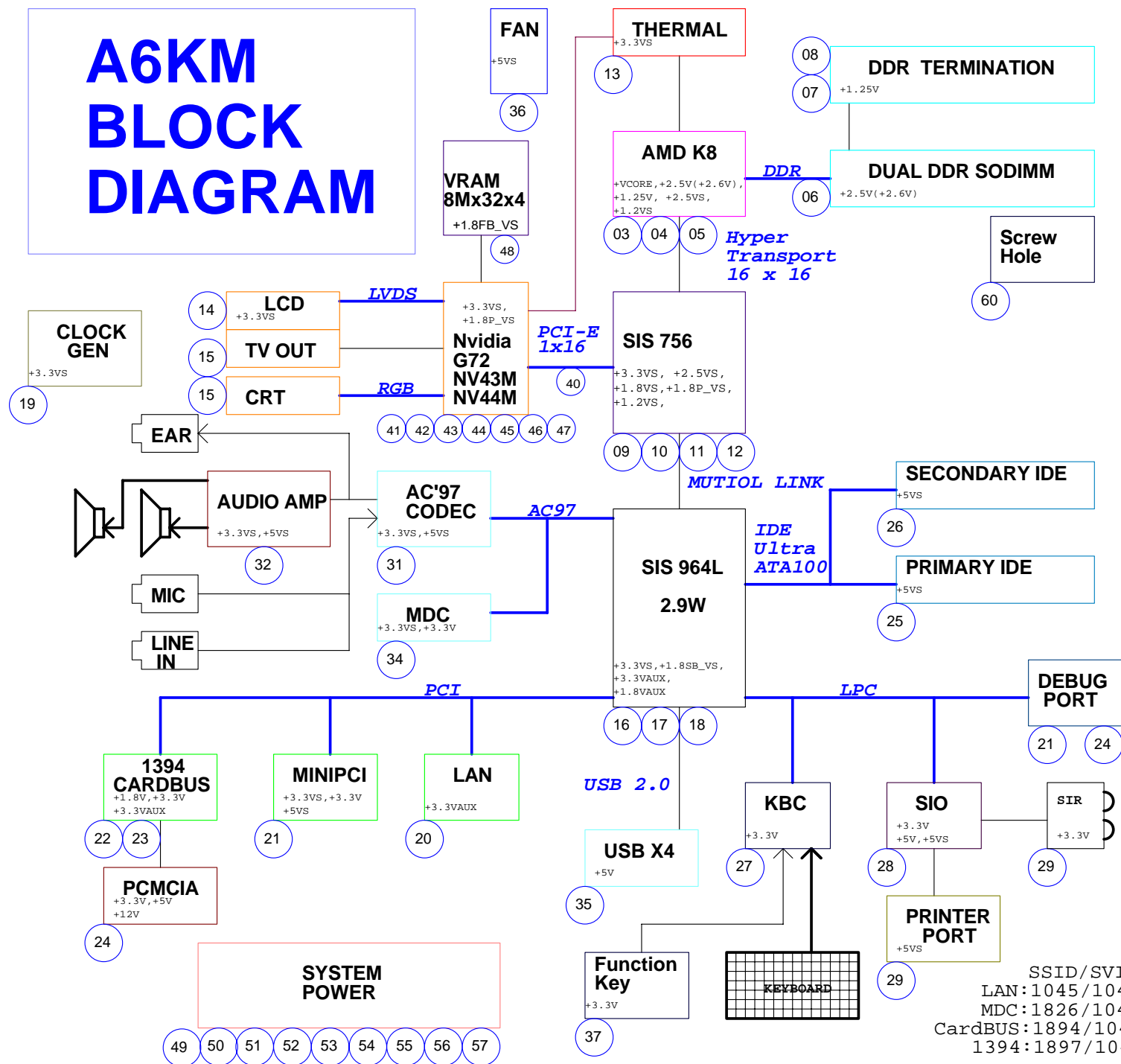


A6KM BLOCK DIAGRAM



FILE LIST 01

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-AMD K8(HOST)
- 04_CPU-AMD K8(DDR)
- 05_CPU-AMD K8(POWER)
- 06_DDR CON
- 07_DDR BYPASS & BUFFER
- 08_DDR TERMINATOR
- 09_SiS756-1(Host/PEI-E)
- 10_SiS756-2 (for MuTIOL)
- 11_SiS756-3 (GND)
- 12_SiS756-4 (Power)
- 13_THERMAL
- 14_LVDS & BACKLIGHT
- 15_CRT/TV CONNECTOR
- 16_SIS964L (1) PCI/ZIP/IDE
- 17_SIS964L (2) LPC/GPIO
- 18_SIS964L (3) USB
- 19_CLOCK-ICS953805BF
- 20_LAN-RTL8100CL
- 21_MINIPCI
- 22_CB1394-R5C593 (1)
- 23_CB1394-R5C593 (2)
- 24_PCPCIA SOCKET
- 25_IDE-HDD
- 26_IDE-ODD
- 27_KBC-M38857
- 28_SIO-SMSC LPC47N417&BIOS
- 29_IR & LPT_PORT
- 30_Discharge circuit
- 31_CODEC-ALC650
- 32_AUDIO AMP
- 33_MIC
- 34_MDC & RJ45 & RJ11
- 35_USB
- 36_BT-UGP25
- 37_FAN&Audio DJ
- 38_FUNCTION KEY
- 39_PWR & RESET SEQ
- 40_PCPCIA Debug MUX
- 41_PCI-E AC Coupling
- 42_G72/NV43/NV44 PEX I/F
- 43_G72/NV43/NV44 Strapping
- 44_G72/NV43/NV44 VGA/TV OUT
- 45_G72/NV43/NV44 LVDS I/F
- 46_G72/NV43/NV44 Spread Spectrum
- 47_G72/NV43/NV44 FB I/F (A)
- 48_G72/NV43/NV44 FB I/B (C)
- 49_VRAM(A)
- 50_VRAM(C)
- 51_VGA core
- 52_Vcore
- 53_1.25V&1.2V
- 54_2.5V&1.8V
- 55_SYSTEM
- 56_LOAD SWITCH
- 57_CHARGER
- 58_PIC16C54
- 59_BATLOW/SD#
- 60_SCREWHOLE
- 61_POWER SEQUENCE
- 62_GPIO SETTING
- 63_SECOND SOURCE
- 64_Review List
- 65_A6KM Revision

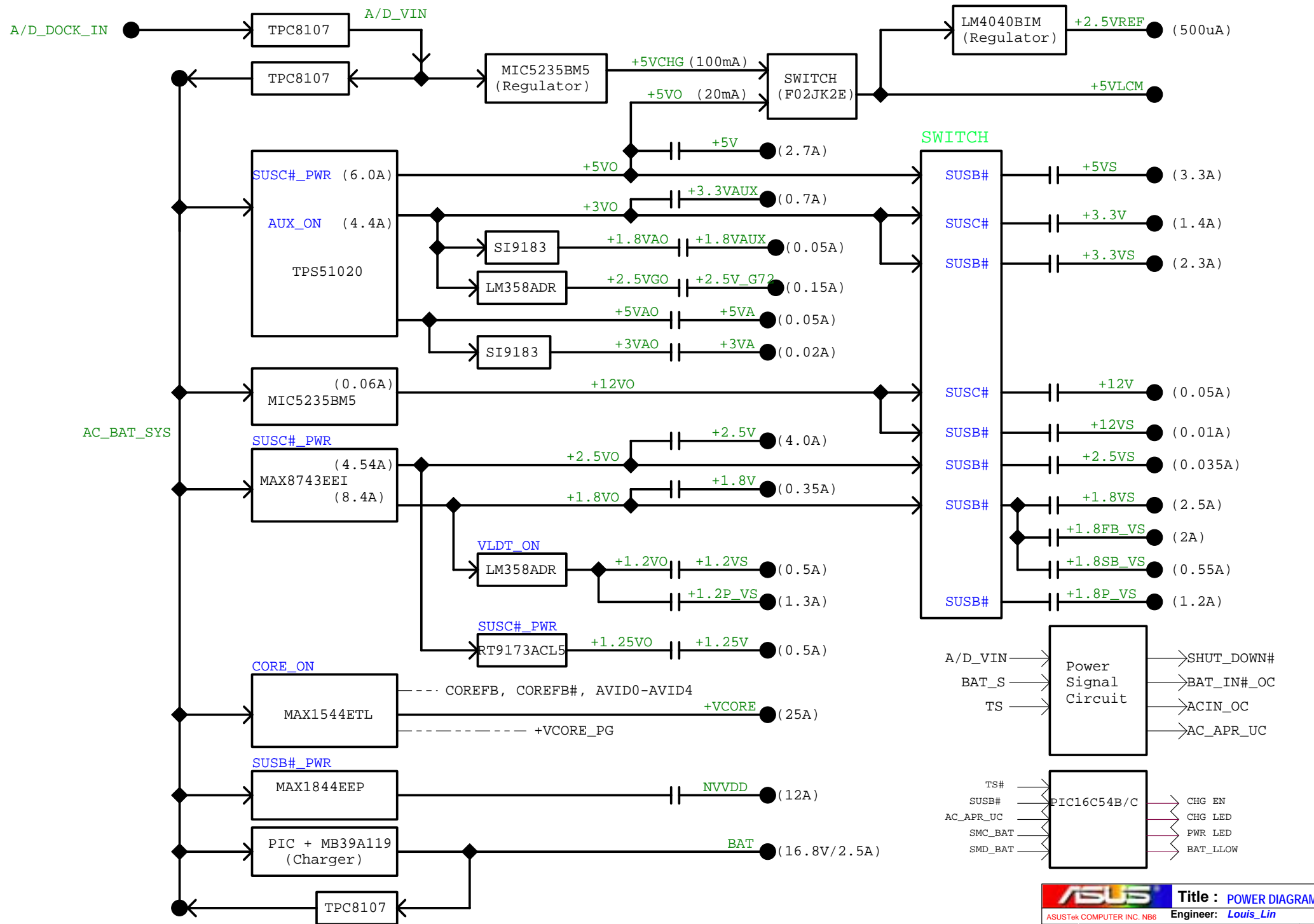
ASUS Title : BLOCK DIAGRAM

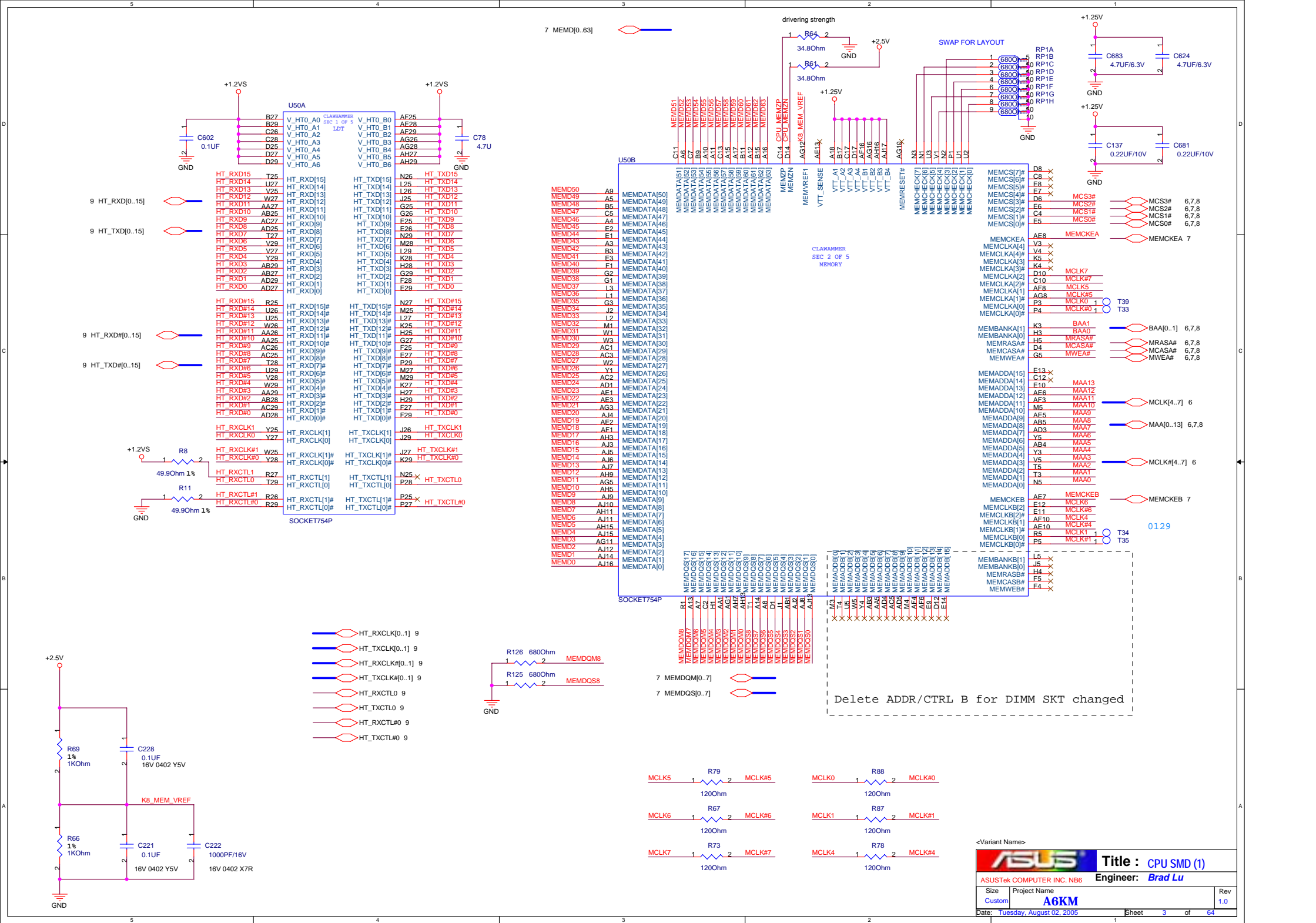
ASUSTek COMPUTER INC. NB6 Engineer: Allen_CD_Wu

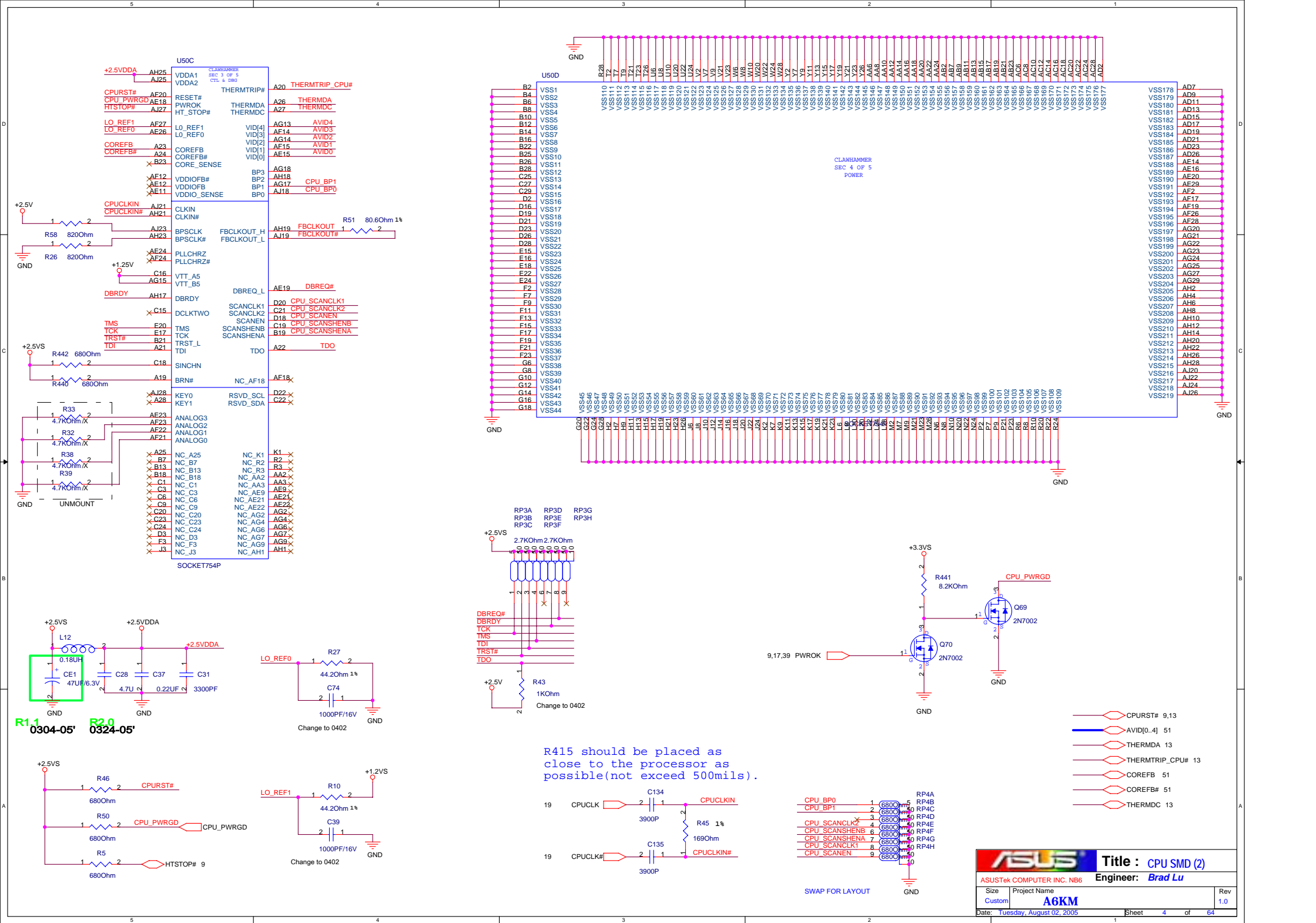
Size Project Name Rev

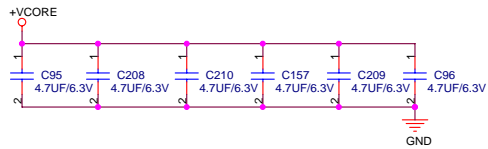
Custom A6KM 1.0

Date: Tuesday, August 02, 2005 Sheet 1 of 64







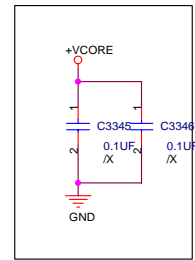
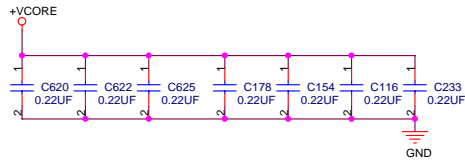


Link plane for EMI

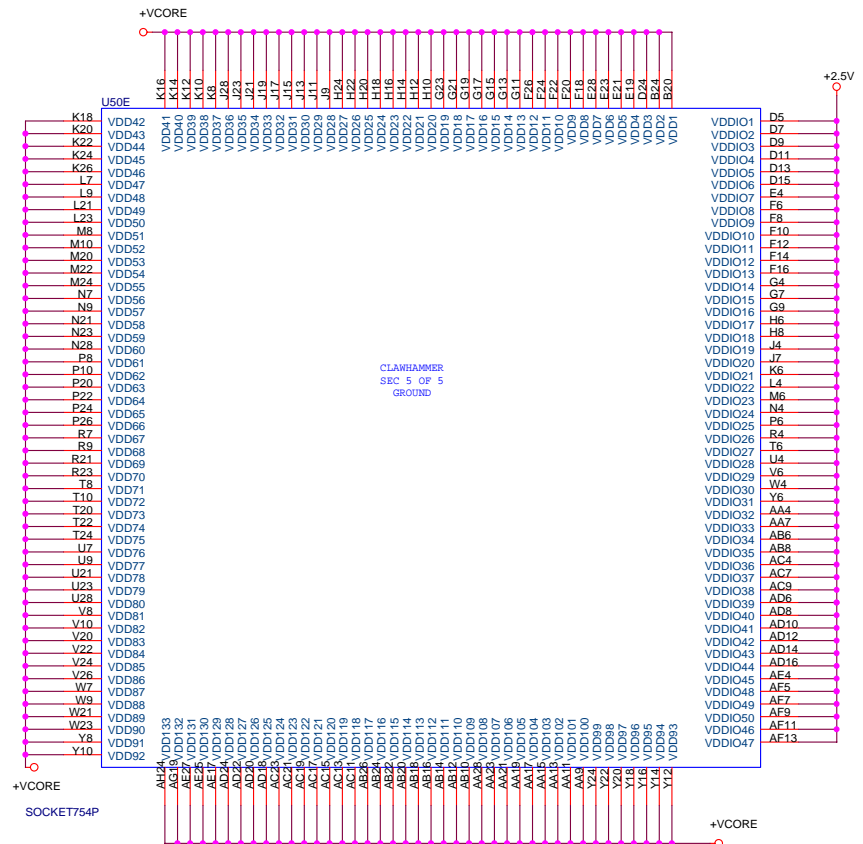
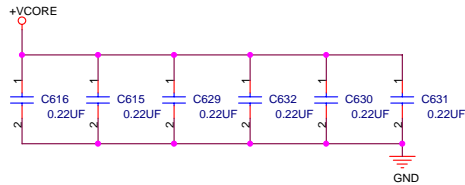


+2.5V (VDDIO, MAX) : 3A
 +1.2VS (VLT, MAX) : 500mA
 +1.25V (VTT, MAX) : 250mA
 +V CORE (VDD, MAX) : 27A
 +2.5VS (VDDA, MAX) : 35mA

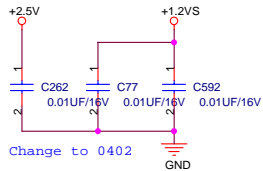
VDDIO: Up to 2.6V to support DDR400(3A)



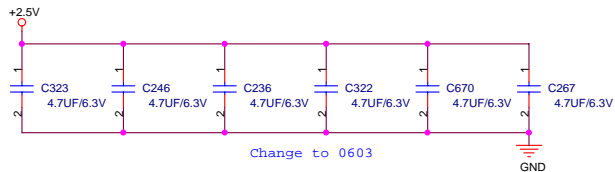
CHANGE4
 R1.1 for EMI



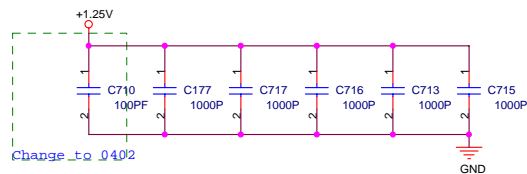
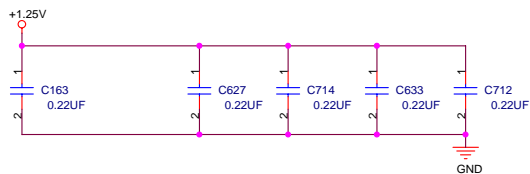
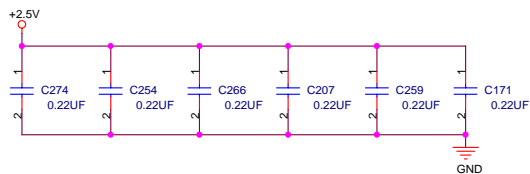
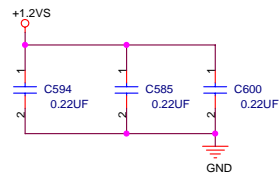
CLAWHAMMER
 SEC 5 OF 5
 GROUND



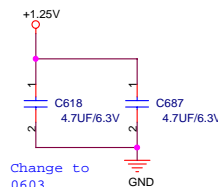
Change to 0402



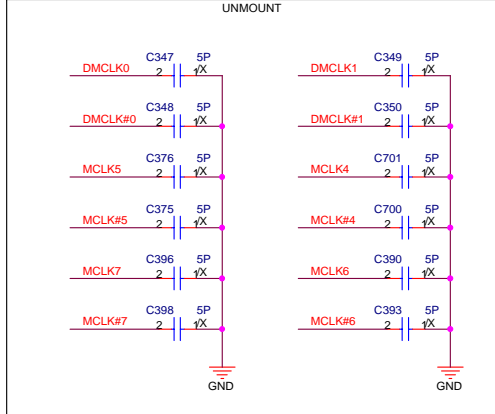
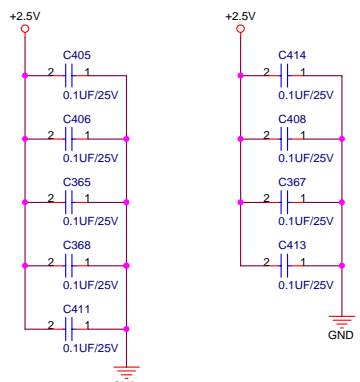
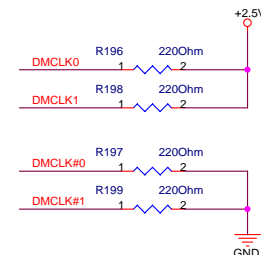
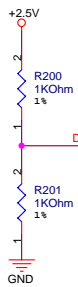
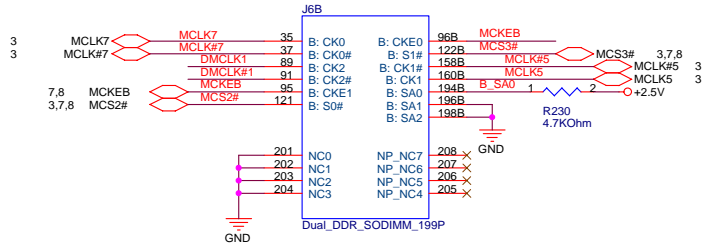
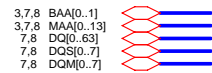
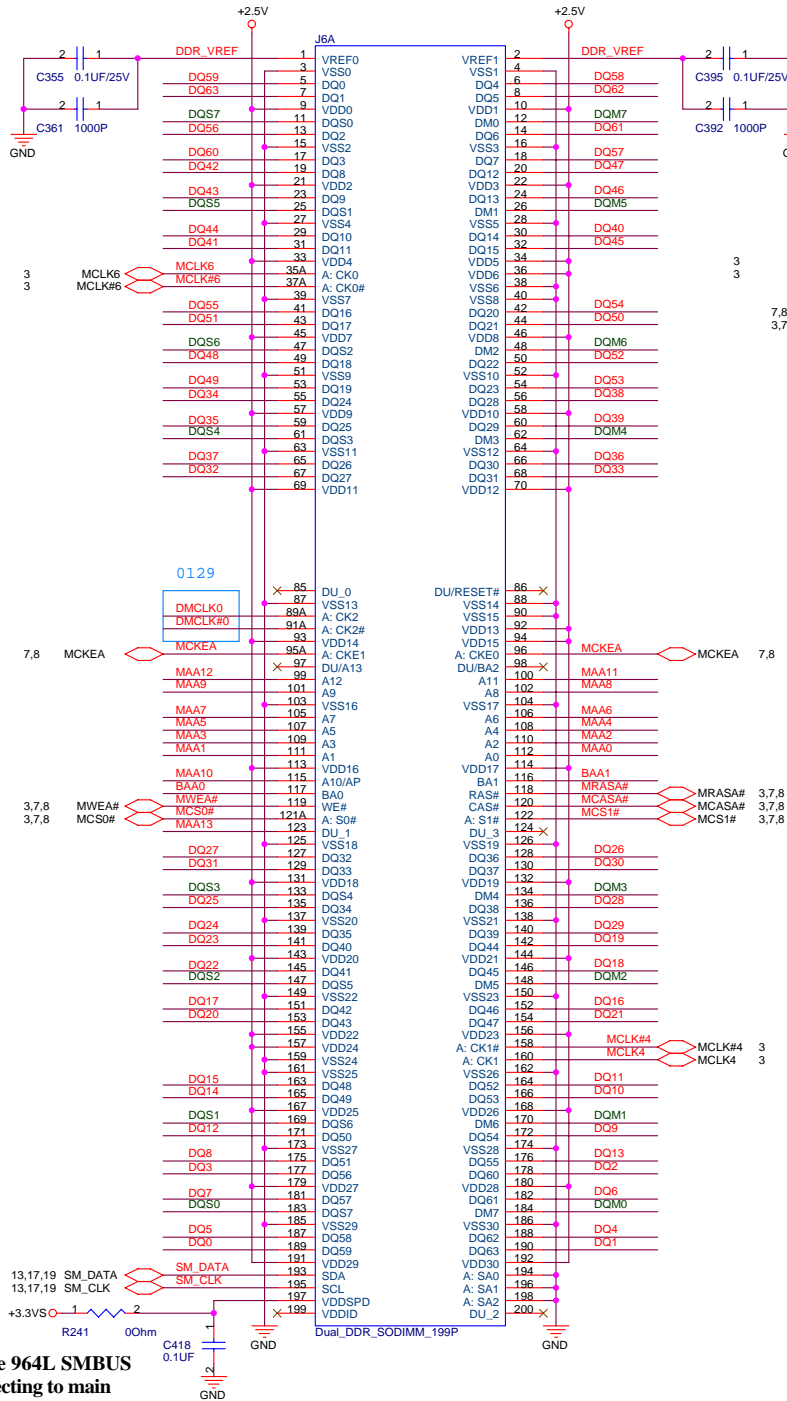
Change to 0603

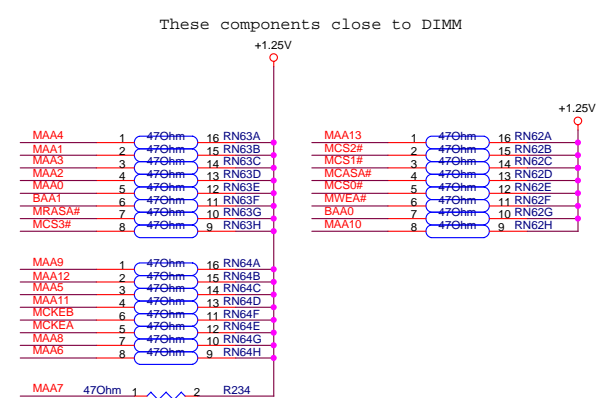
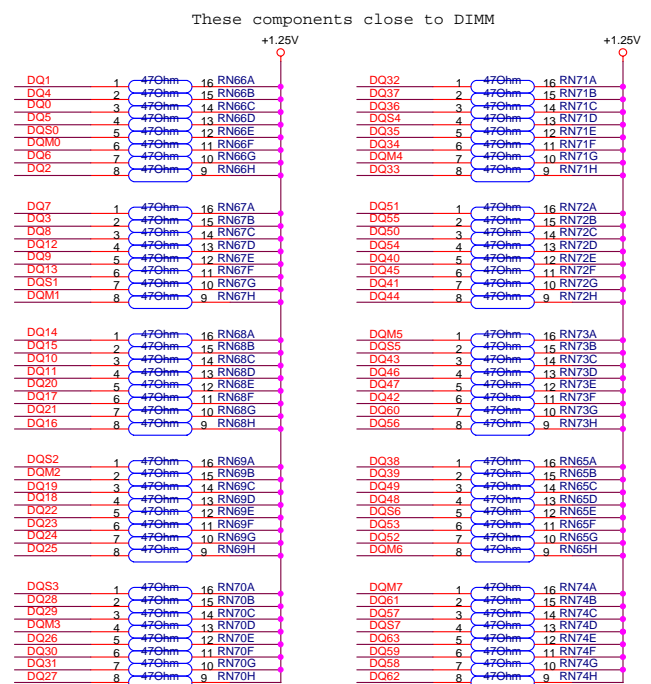
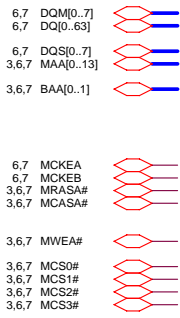


Change to 0402

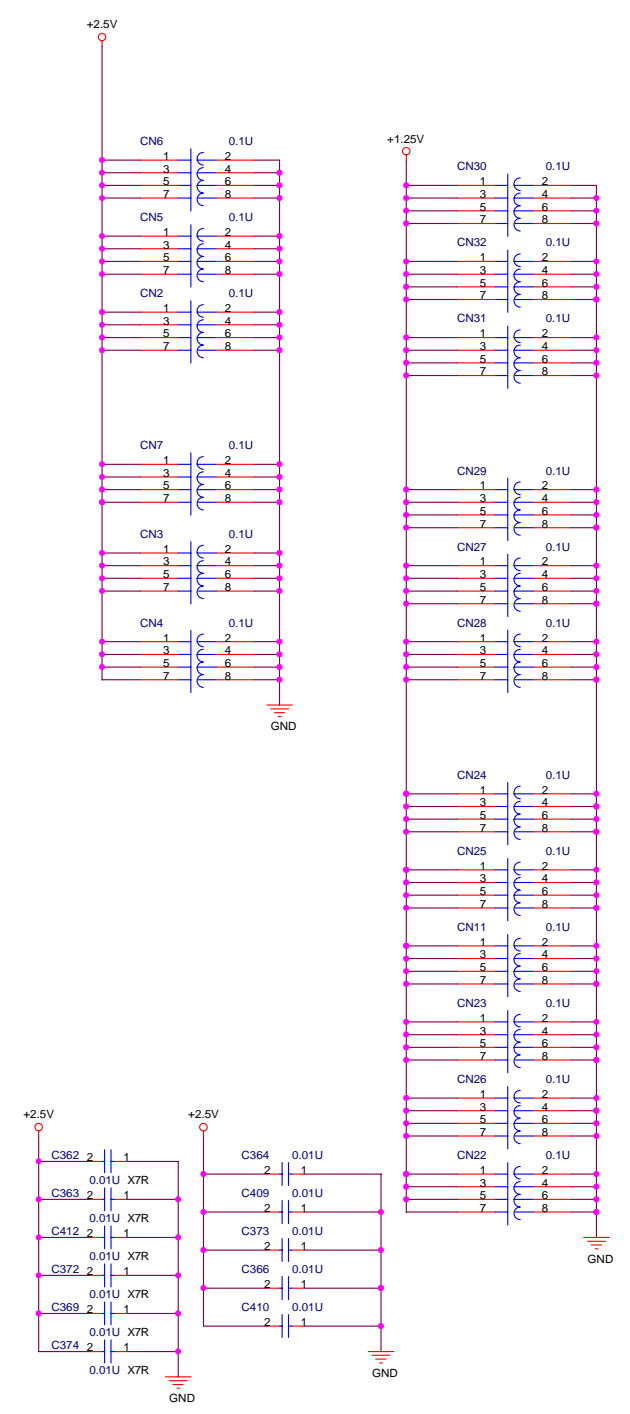


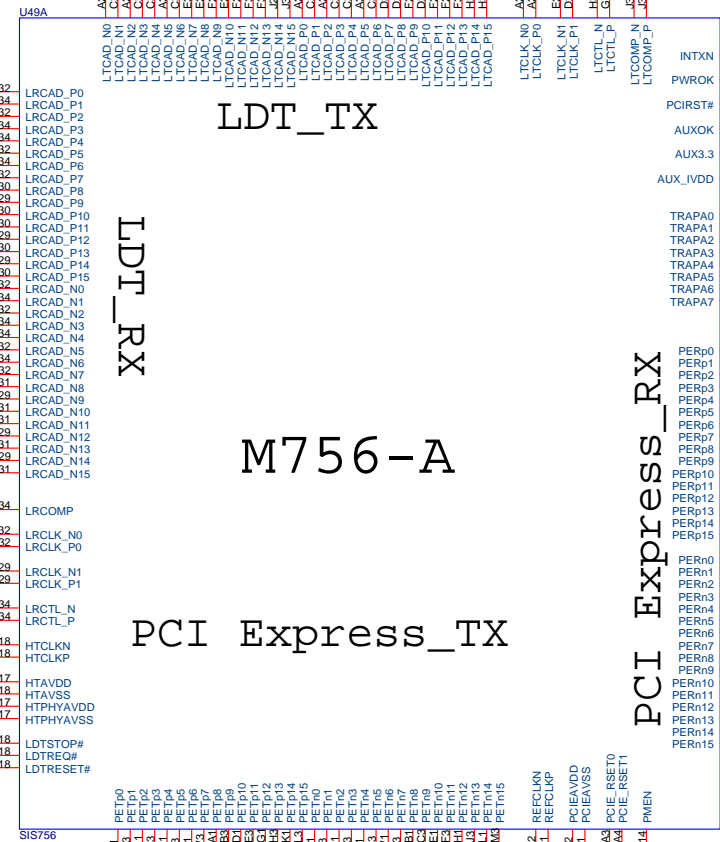
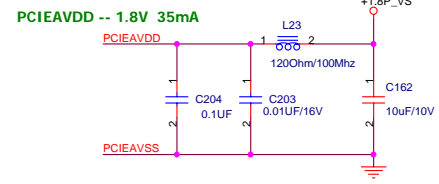
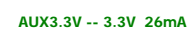
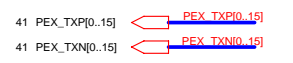
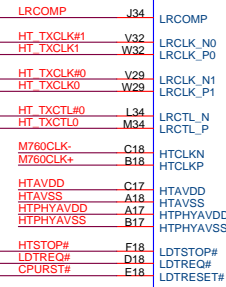
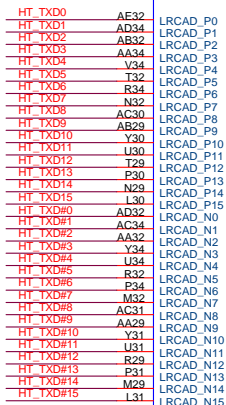
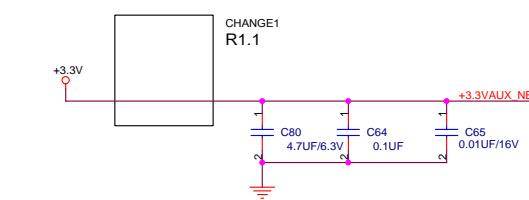
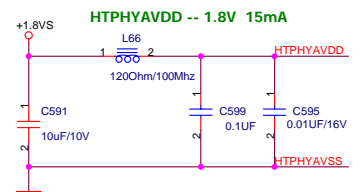
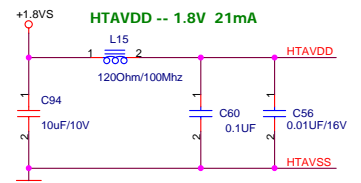
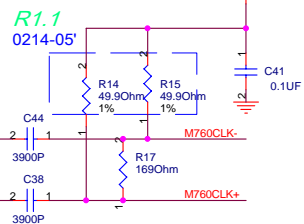
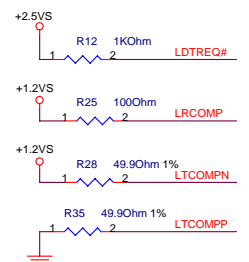
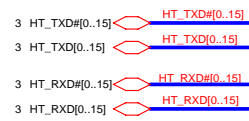
Change to
 0603





CHANGE3
R1.1





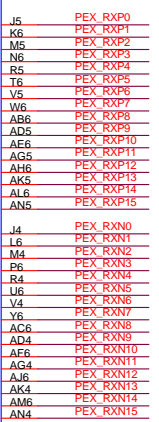
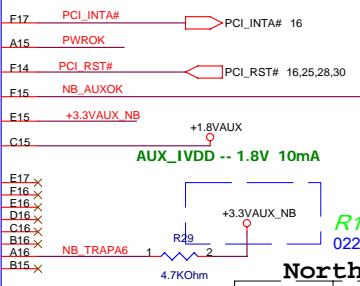
LDT_TX

HT_TX

M756-A

PCI Express_TX

PCI Express_RX

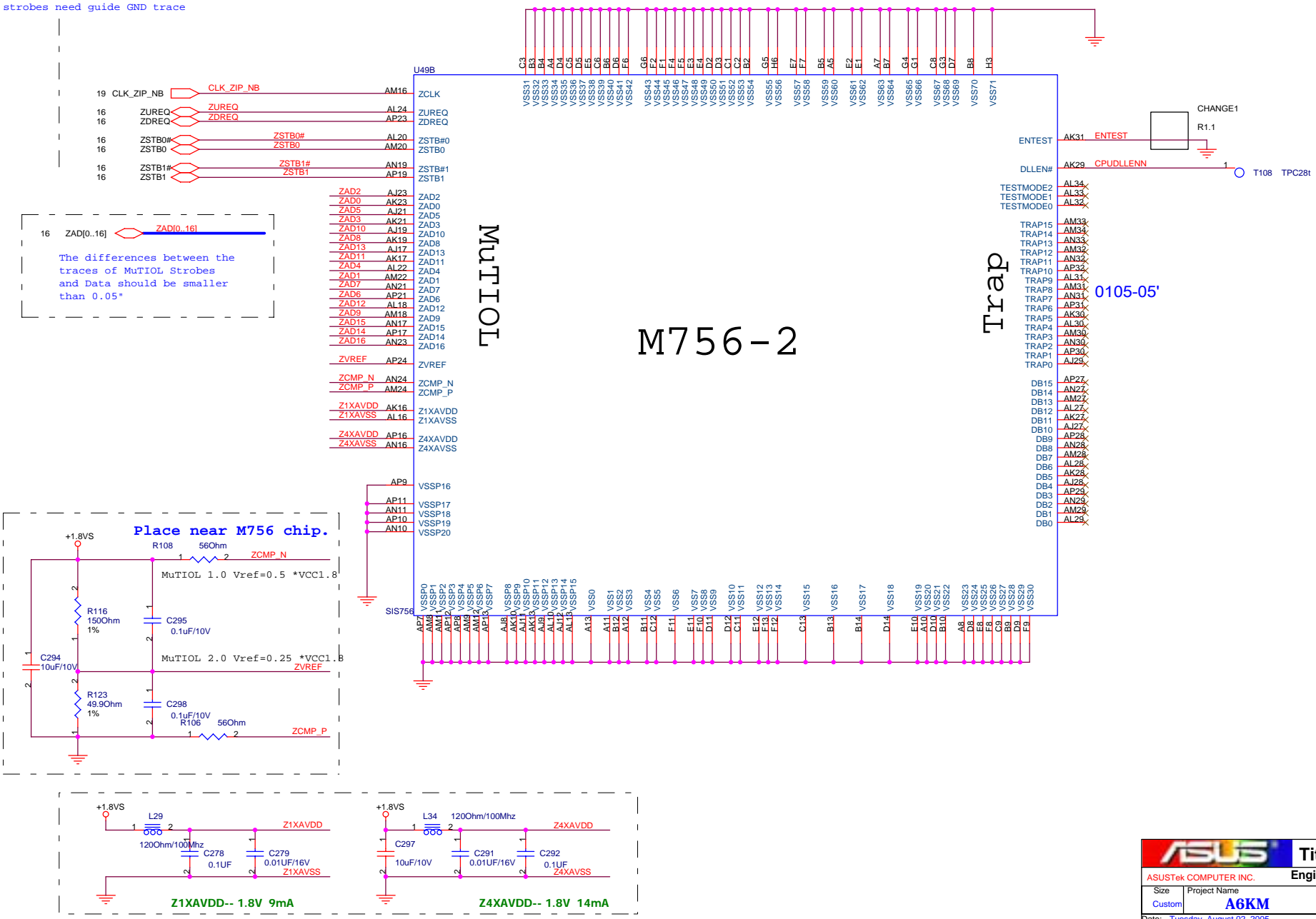


North Bridge Hardware Trap

Symbol	Description	Default
DLLEN-	0: Disable 1: Enable	Internal Pull Down
TMODE0	0: Normal 1: Test Mode	Internal Pull Down
TMODE1	0: Mode 0 1: Mode 1	Internal Pull Down
TMODE2	0: Enable 1: Disable	Internal Pull Down
TRAP[1..0]	00: 133 MHz 01: 166/200 MHz 10: 66 MHz 11: 100 MHz	Internal Pull Down
TRAP2	0: Serial mode 1: ASL Serial Mode Initialization Enable	Internal Pull Down
TRAP[4..3]	Reserved	Internal Pull Down
TRAP5	0: Serial mode 1: PCIE PLL Bypass	Internal Pull Down
TRAP6	0: Serial mode 1: PCIE Symlock Test	Internal Pull Down
TRAP[8..7]	0: Serial mode 1: PCIE TX Fix Out	Internal Pull Down
TRAP[11..9]	000: divide 1 / divide 1 001: divide 2 / divide 2 010: divide 3 / divide 3 011: divide 4 / divide 4 100: divide 4 / divide 5	Internal Pull Down
TRAP[13..12]	00: PLL2X 200MHz 01: PLL2X 800MHz 10: PLL2X 1000MHz	Internal Pull Down
TRAP14	0: by logic decoded 1: by trapped	Internal Pull Down
TRAP15	0: by logic decoded 1: by trapped	Internal Pull Down
TRAPA[1..0]	00: divide 1 01: divide 2 10: divide 3 11: divide 4 100: divide 5	Internal Pull Down
TRAPA[4..2]	000: divide 1 001: divide 2 010: divide 3 011: divide 4 100: divide 5	Internal Pull Down
TRAPA[6..5]	00: PLL1X Gain 01: PLL1X 200MHz 10: PLL1X 250MHz (Recomm. Value: 10)	Internal Pull Down
TRAP7	For Internal Test	Internal Pull Down

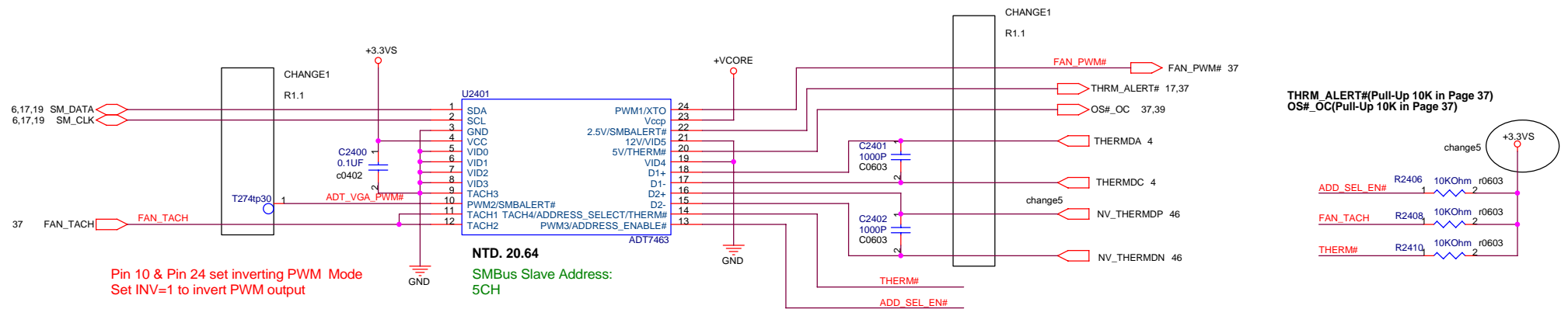
The differences between the traces of MuTIOL Strokes and Data in each group should be smaller than 0.05", and strokes need guide GND trace

The differences between the traces of MuTIOL Strokes and Data should be smaller than 0.05"



M756-3

Ground



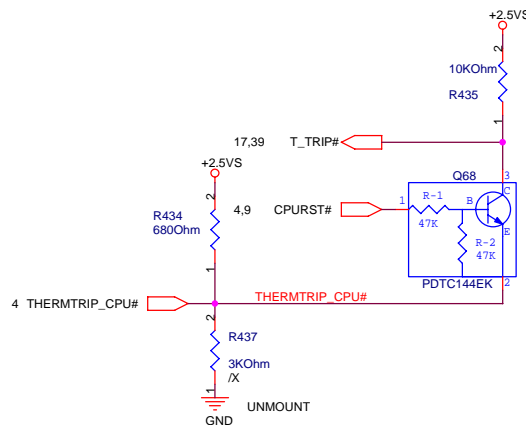
Pin 13 State	Pin 14 State	Address
0	LOW(10Kohm to GND)	0101100(58)
0	LOW(10Kohm Pull-UP)	0101101(5A)
1	Don't Care	0101110(5C) (Default)

THERMAL

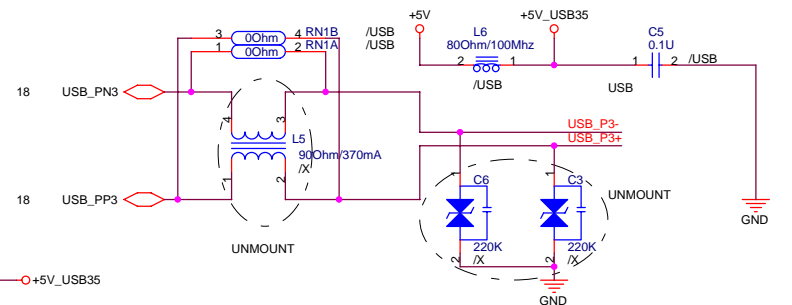
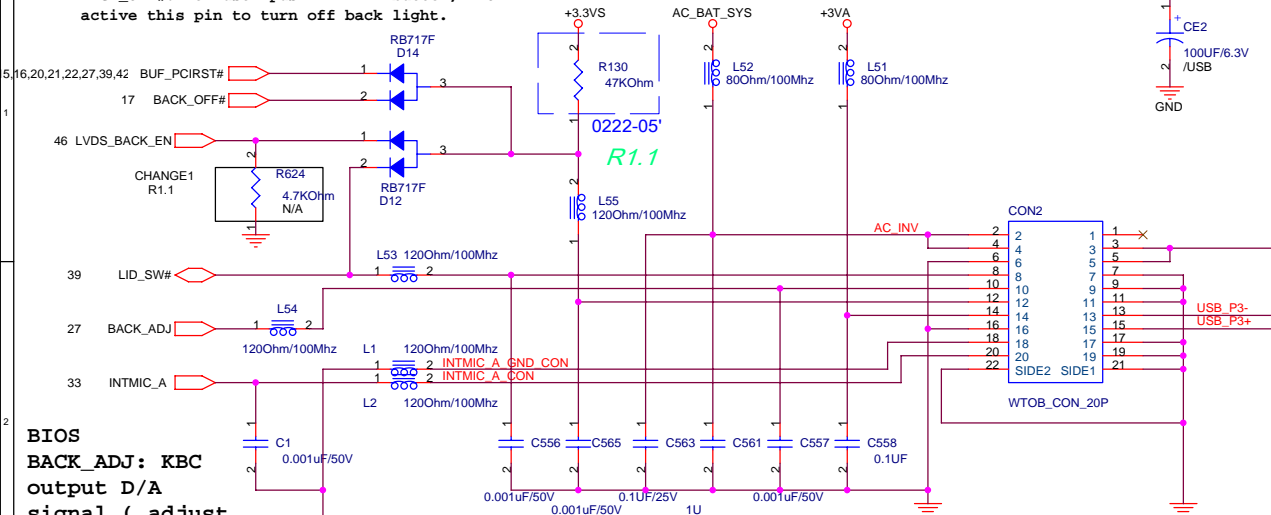
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
12 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
12 mils
-----OTHER SIGNALS

Avoid BPSB,Power



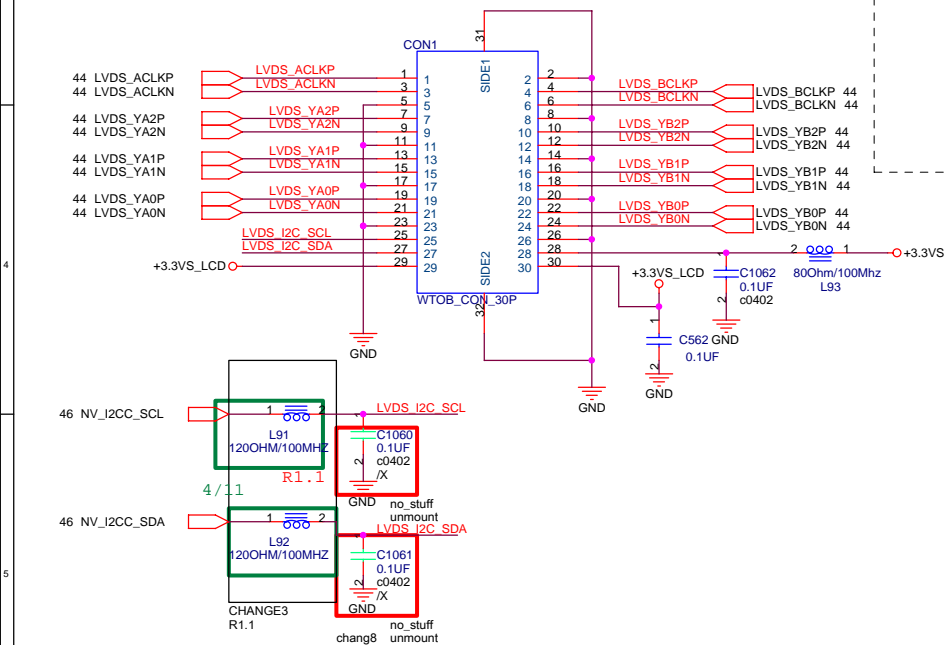
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS
active this pin to turn off back light.



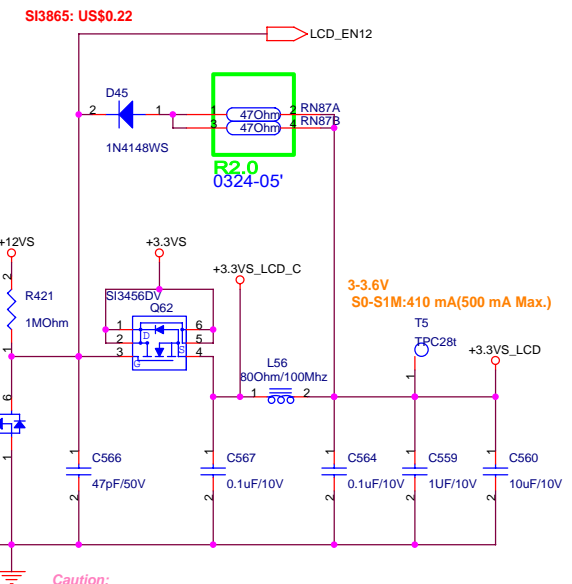
USB PORT 3 for CAMERA

BIOS
BACK_ADJ: KBC
output D/A
signal (adjust
voltage level)
to adjust Back
light.

A3K used D1 R:1.0
Inverter Board

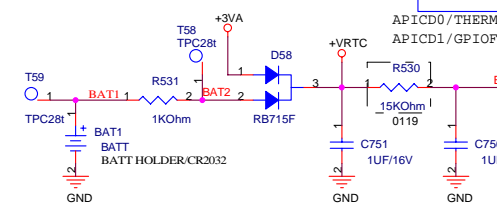


LCD Power

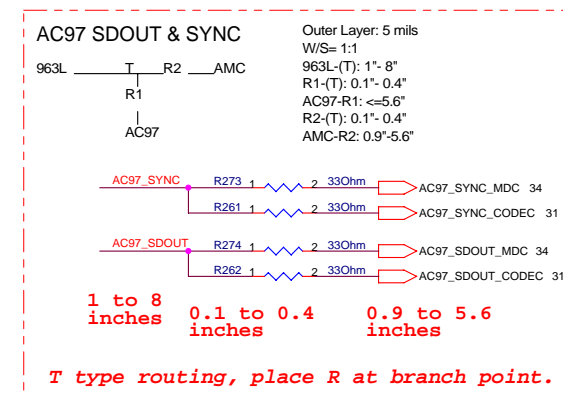
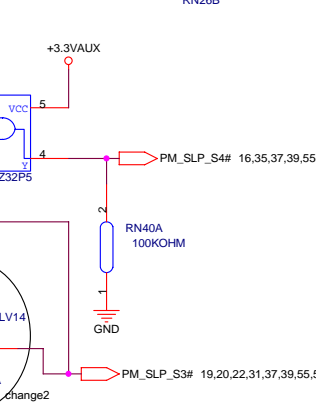
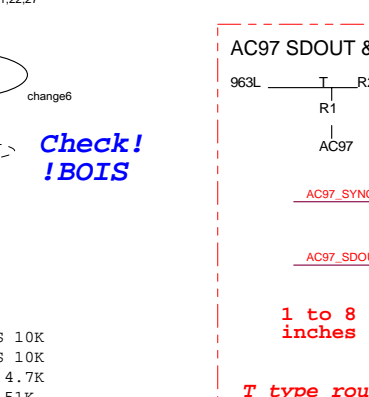
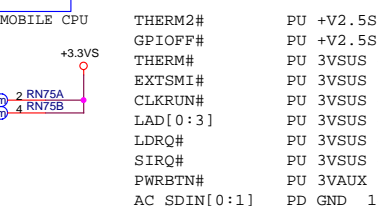


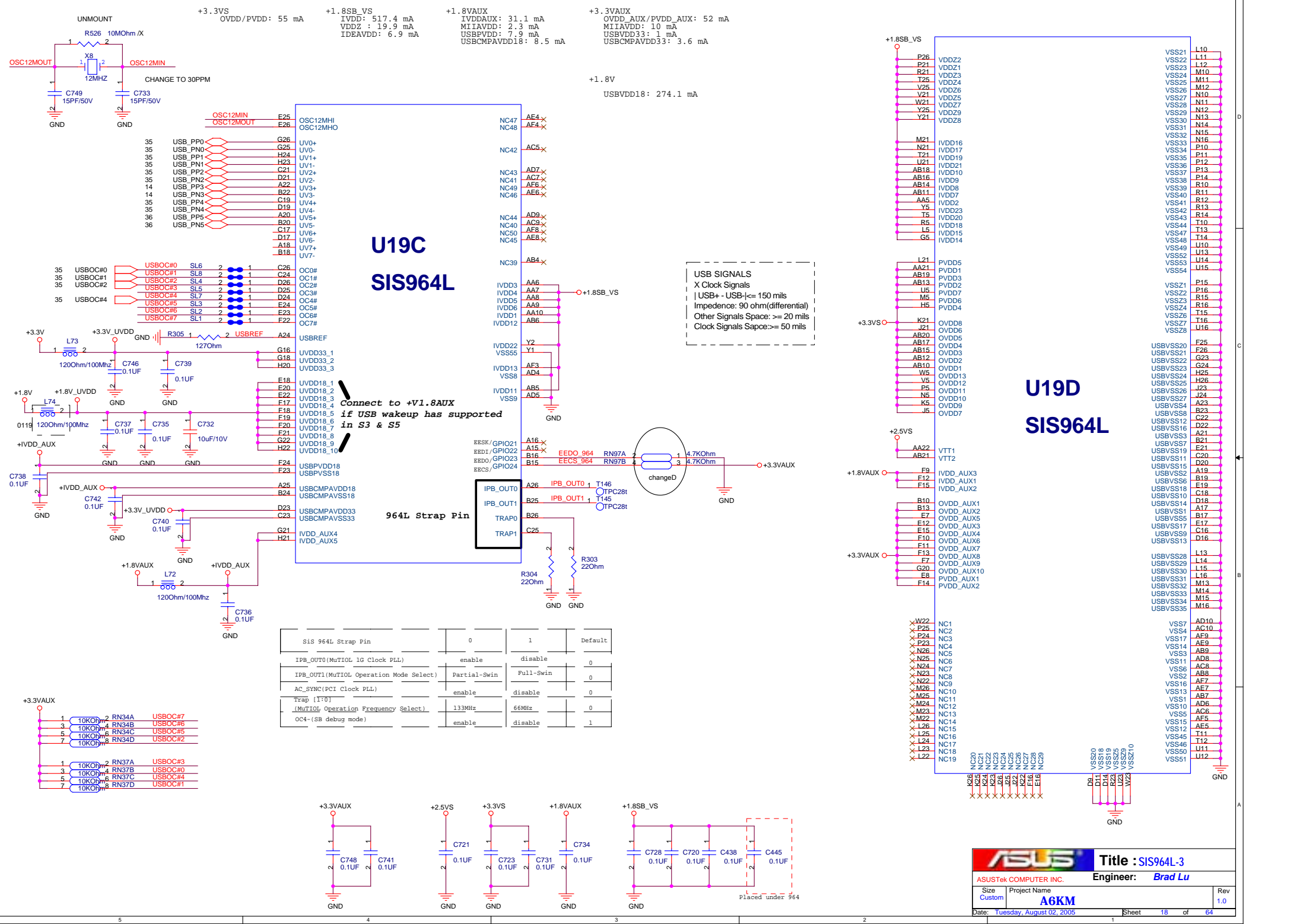
Caution:
Must
tune
R1404 &
C1415 to
meet
Panel
Spec

ASUS		Title : LVDS & BACKLIGHT	
ASUSTek COMPUTER INC. NB6		Engineer: Brad Lu	
Size	Project Name	Rev	
Custom	A6KM	1.0	
Date: Tuesday, August 02, 2005	Sheet 14 of 64		



U19B
SIS964L





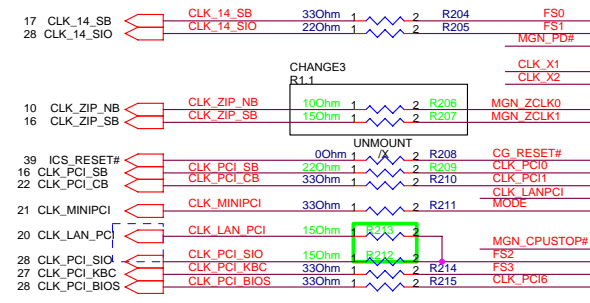
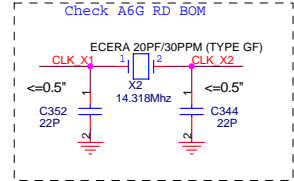
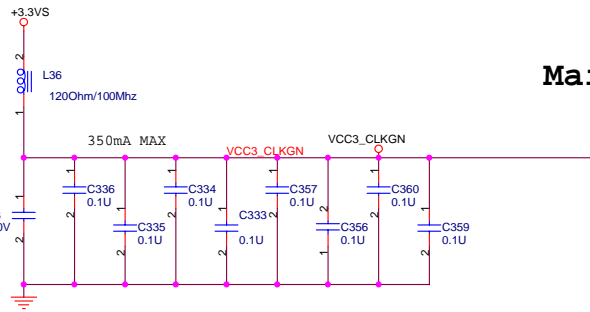
Main Clock Generator

CLK33 GROUP:
 In L3
 Breakout:
 Group Space >= 25 mils
 Length Match: same as CLK66

CLK66 GROUP:
 In L3
 Breakout:
 (<=0.3")
 Group Space >= 25 mils
 Length Match: +/- 100 mils

Check A6G RD BOM

Damping Resistors
 Place near to the
 Clock Outputs.

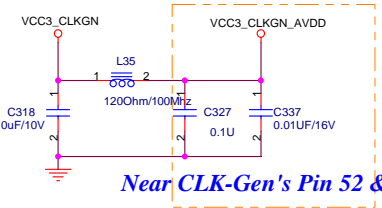
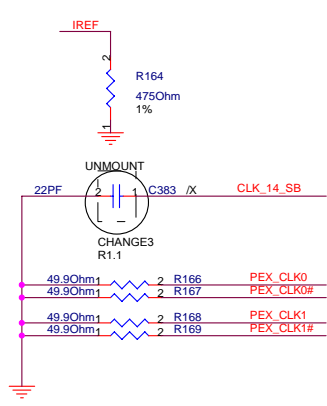
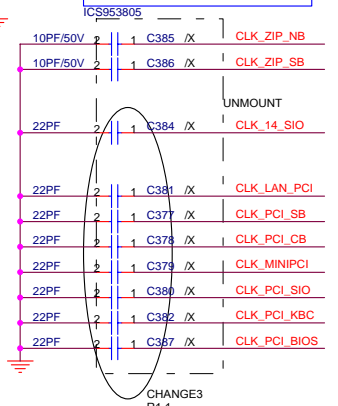
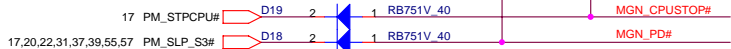
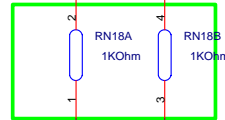


Watch out length mismatch!

0324-05'

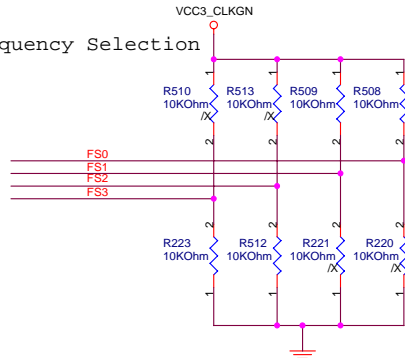
BIOS need to disable PIN 26,27,SRCLK, PCIE2-4

R2.0
 0324-05'



Near CLK-Gen's Pin 52 & 49.

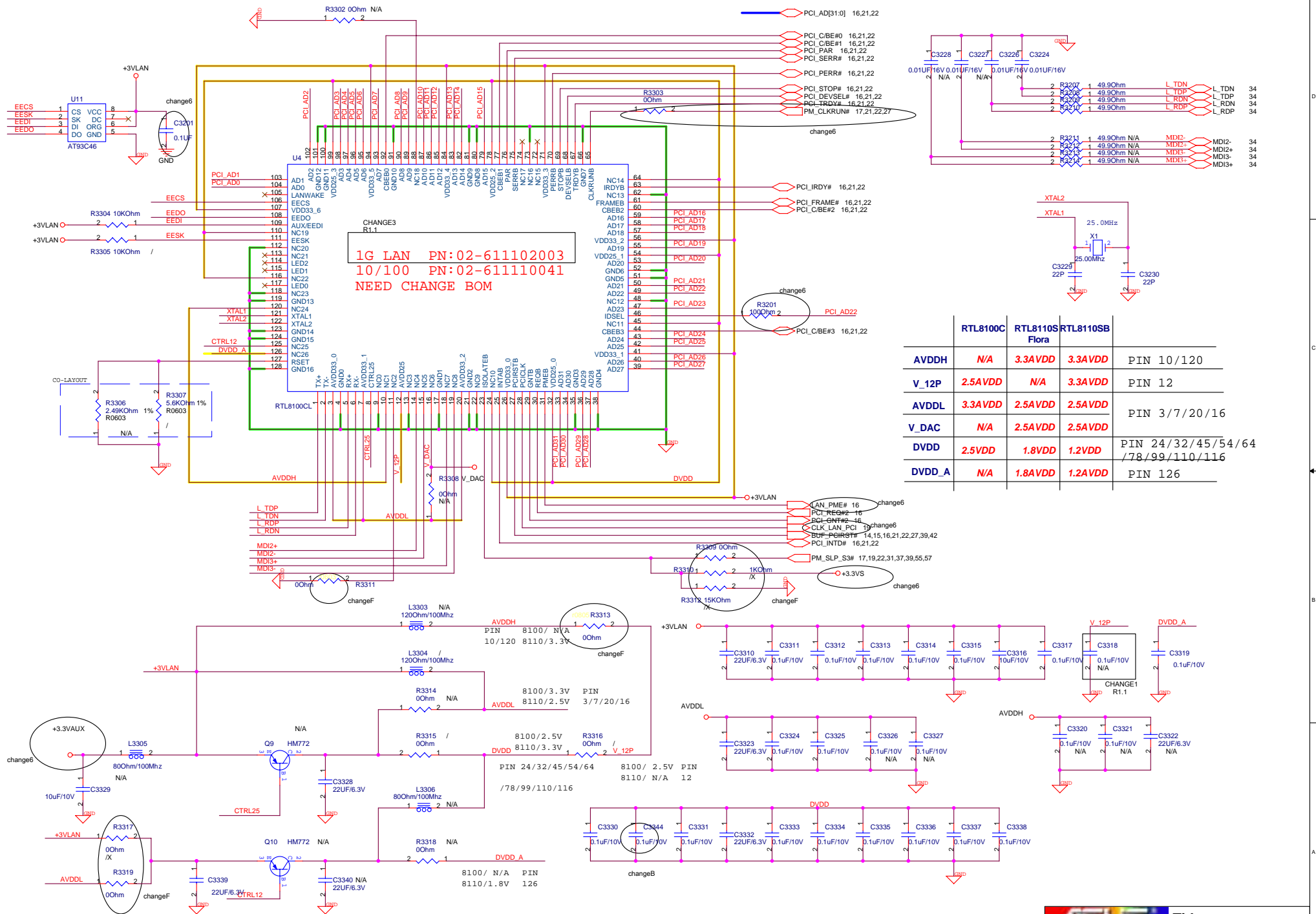
Frequency Selection



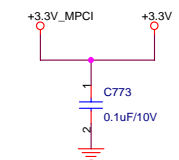
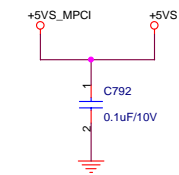
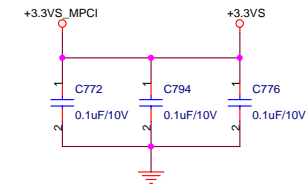
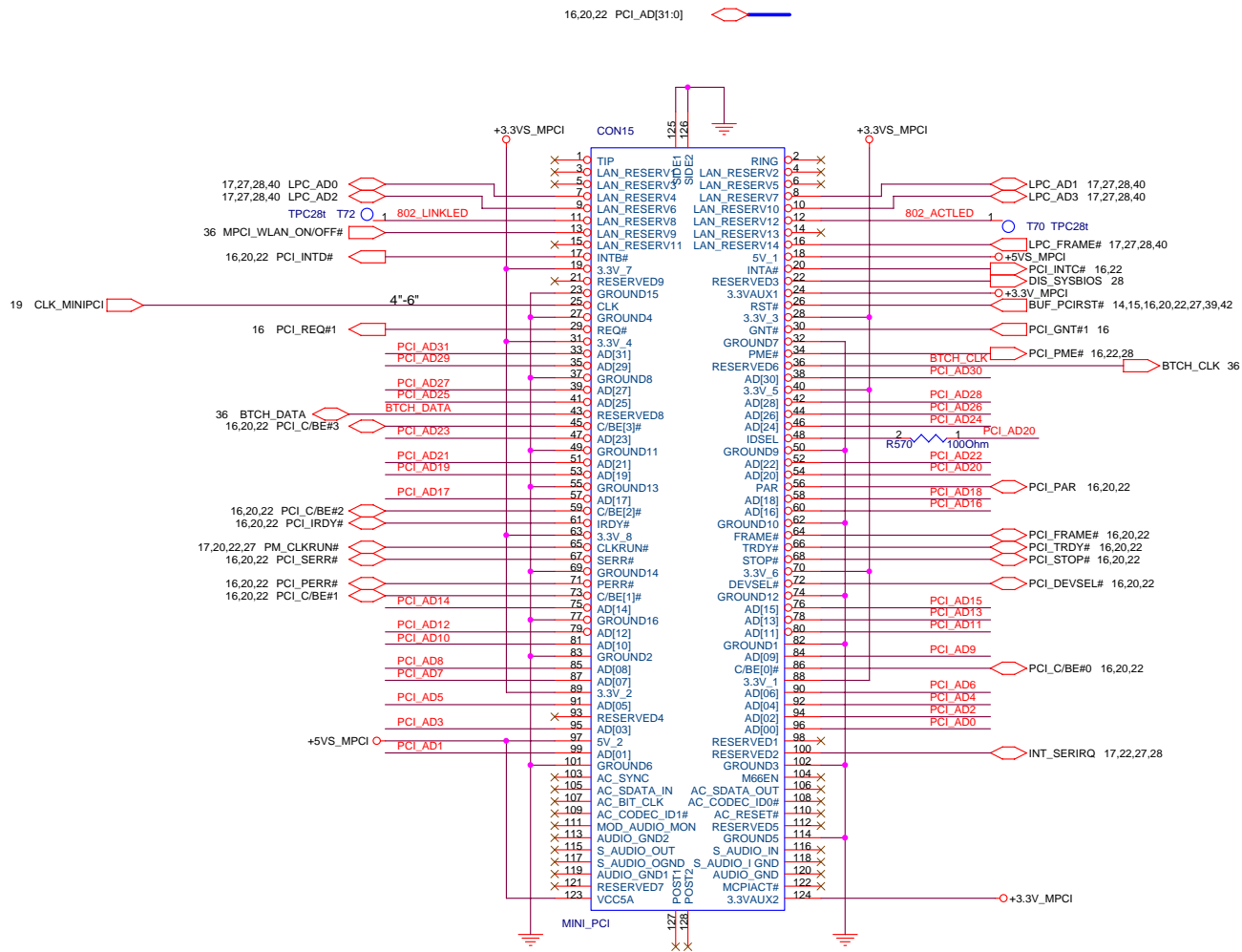
CLK Table for SiS M756 (ICS-953805)

SiS M760 CLOCK											
(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	NB_CLK (MHz)	ZCLK (MHz)	PCIE_X (MHz)	PCIE_L (MHz)	PCIE_H (MHz)	PCIE_L (MHz)	PCIE_H (MHz)
0	0	0	0	100	100	133.33	100.00	33.33	33.33	33.33	33.33
0	0	0	1	133.33	133.33	133.33	100.00	33.33	33.33	33.33	33.33
0	0	1	0	166.66	166.66	133.33	100.00	33.33	33.33	33.33	33.33
0	0	1	1	200.00	200.00	133.33	100.00	33.33	33.33	33.33	33.33
0	1	0	0	250.00	250.00	133.33	100.00	33.33	33.33	33.33	33.33
0	1	0	1	266.66	266.66	133.33	100.00	33.33	33.33	33.33	33.33
0	1	1	0	100.00	125.00	133.33	100.00	33.33	33.33	33.33	33.33
0	1	1	1	133.33	166.66	133.33	100.00	33.33	33.33	33.33	33.33
1	0	0	0	166.66	222.22	133.33	100.00	33.33	33.33	33.33	33.33
1	0	0	1	200.00	250.00	133.33	100.00	33.33	33.33	33.33	33.33
1	0	1	0	250.00	333.33	133.33	100.00	33.33	33.33	33.33	33.33
1	0	1	1	266.66	400.00	133.33	100.00	33.33	33.33	33.33	33.33
1	1	0	0	202.00	202.00	134.66	100.00	33.66	33.66	33.66	33.66
1	1	0	1	204.00	204.00	136.00	100.00	34.00	34.00	34.00	34.00
1	1	1	0	206.00	206.00	137.33	100.00	34.33	34.33	34.33	34.33
1	1	1	1	208.00	208.00	138.66	100.00	34.66	34.66	34.66	34.66

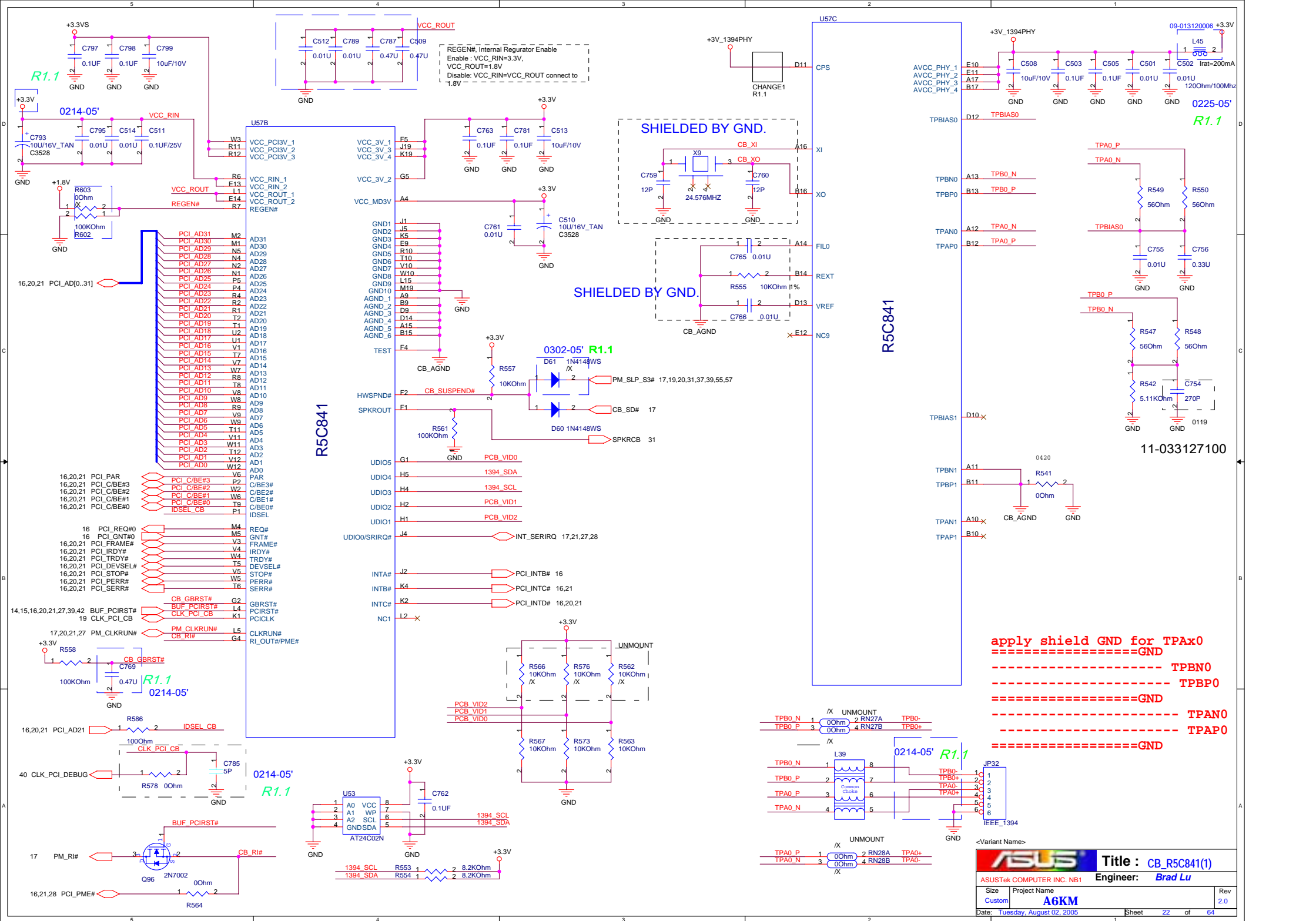
Trap Default



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126



Intel Calexico(802.11a+802.11b)
 802.11b
 Tx: 500-526 mA
 Rx: 280-299 mA
 Sleep: 30 mA
 802.11a
 Tx: 435-475 mA
 Rx: 310-327 mA
 Sleep: 30 mA



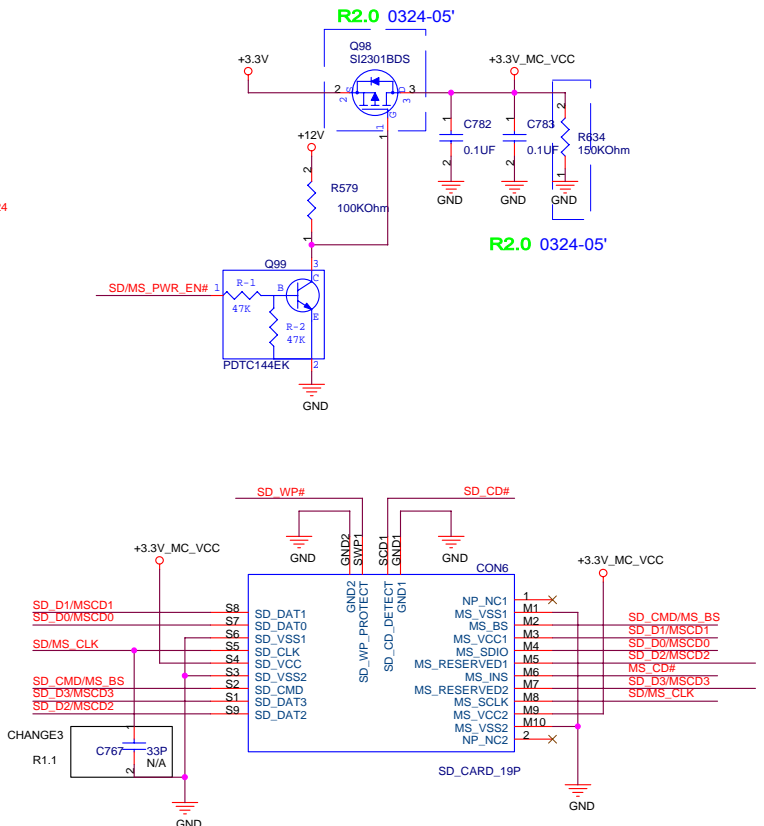
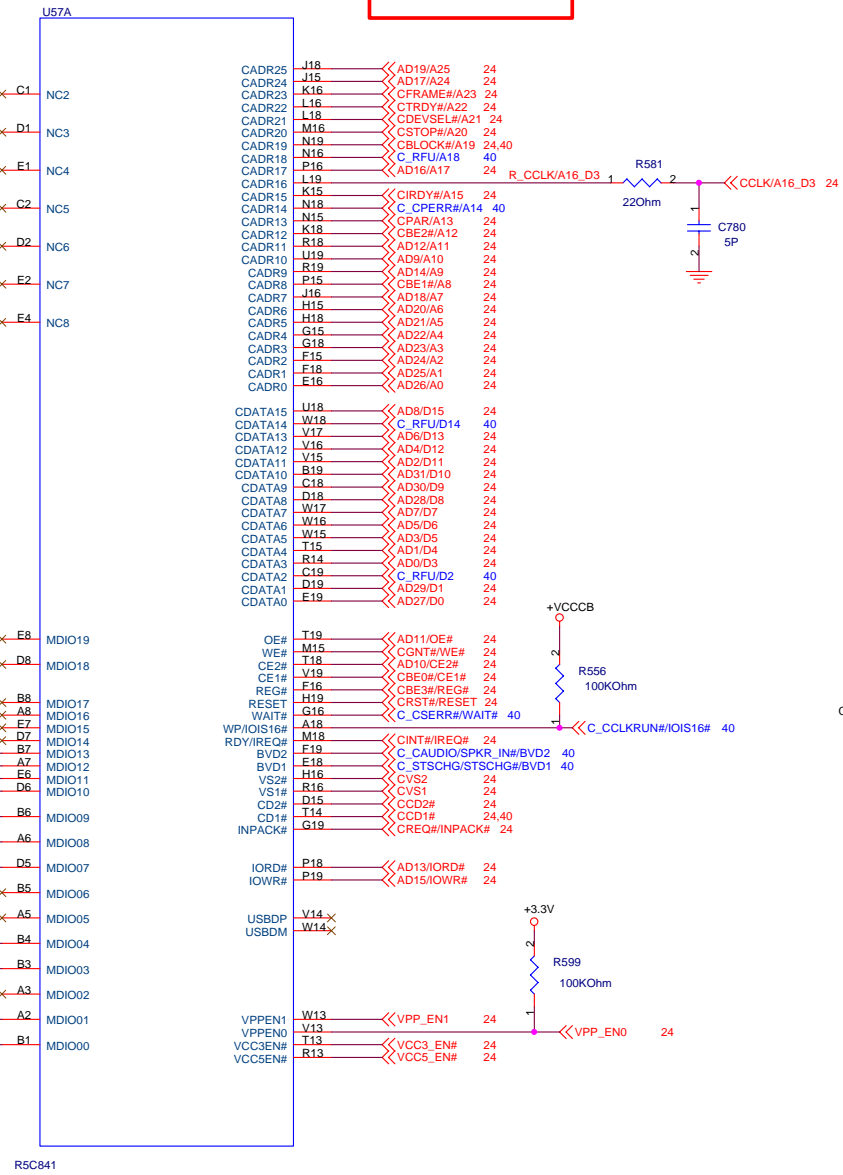
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

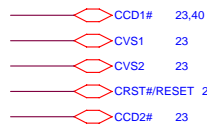
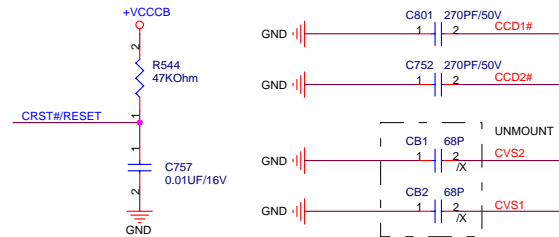
[2] AS CLOSE AS POSSIBLE
TO DEVICE TERMINALS.

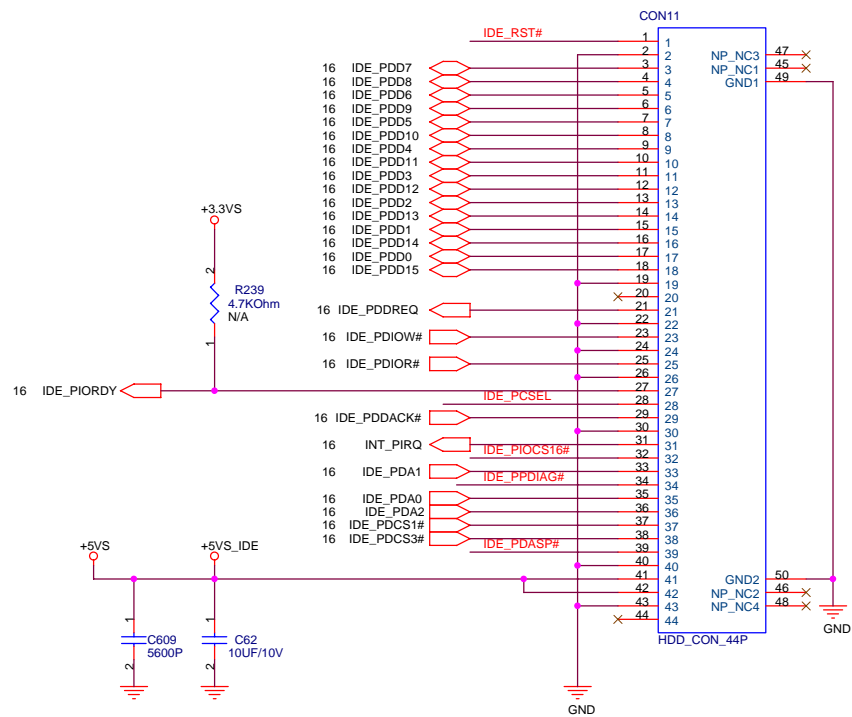
藍色pin腳名稱的訊號
是要經由MUX分離的訊號
以避免841的假的LPC訊號
跟SYSTEM的LPC訊號相衝突

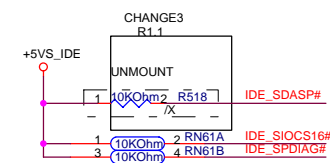
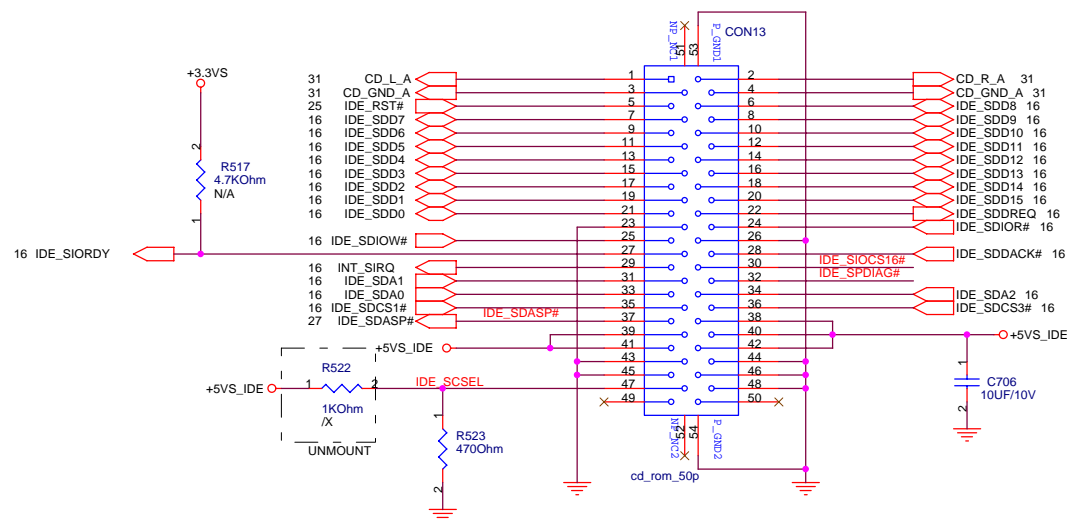
SD D3/MSCD3
SD D2/MSCD2
SD D1/MSCD1
SD D0/MSCD0
SD/MS_CLK [2] R554 220Ohm
SD CMD/MS_BS
SD/MS_PWR_EN#
SD_WP#
MS_CD#
SD_CD#



CON14







P23,P43
exchanged by
BIOS's request

Daisy-Chain in layout

- 17,21,22,28 INT_SERIRQ
- 19 CLK_PCI_KBC
- 14,15,16,20,21,22,39,42 BUF_PCIRST#
- 17,21,28,40 LPC_FRAME#
- 17,21,28,40 LPC_AD3
- 17,21,28,40 LPC_AD2
- 17,21,28,40 LPC_AD1
- 17,21,28,40 LPC_ADO

S0-S3: (2.5 mA Typ, 7 mA Max.)

LxWxH=14x14x1.7

P54,P55,P43,P50 are
wake-up event inputs when KBC
in standby mode

Audio DJ pin depends on
Keyboard Matrix.

Follow M6N

A3N follow M6N
Keyboard Matrix

BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell

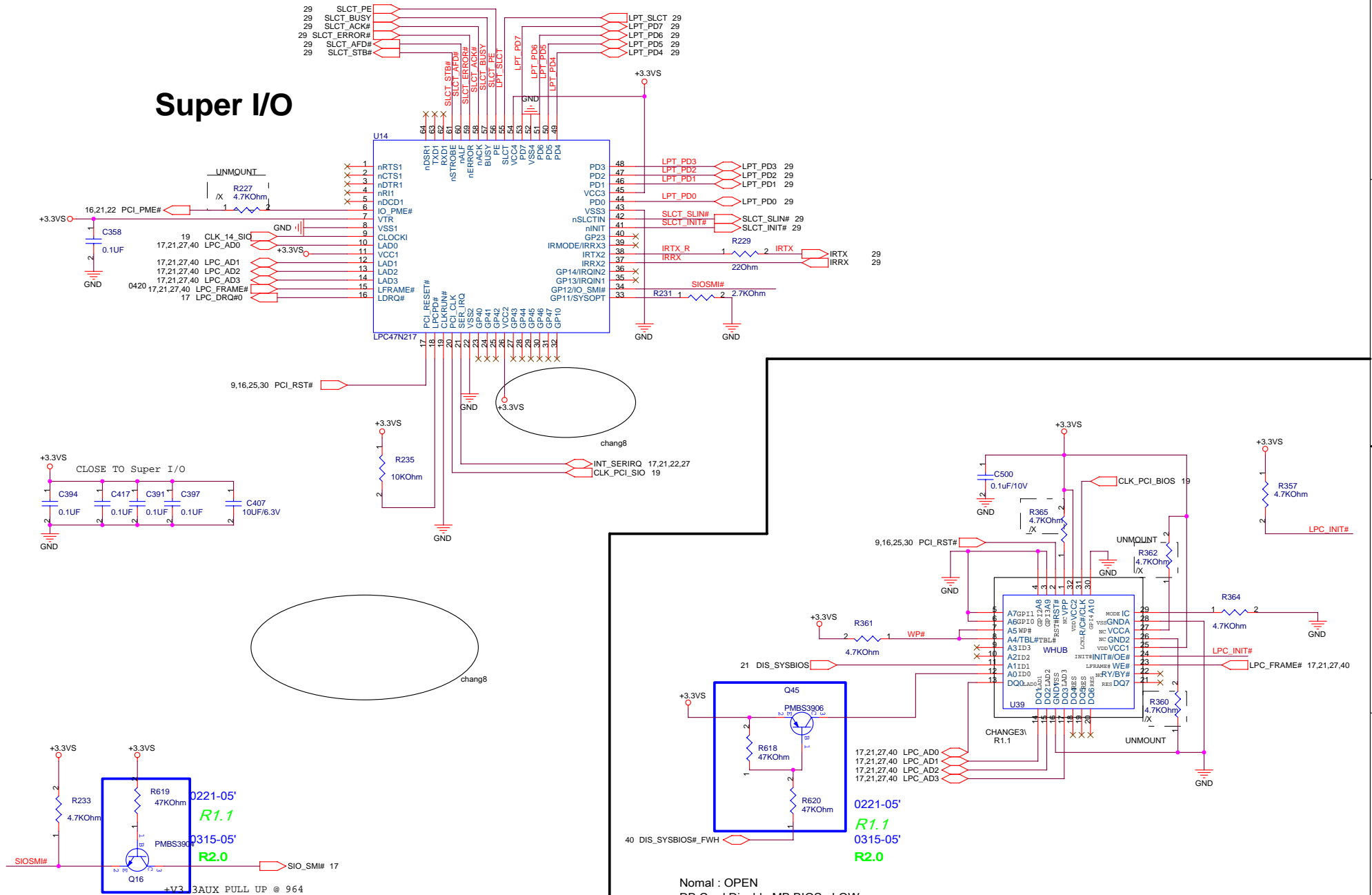
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%

P21: Power button
overwrite disable.
Only can be pulled
down as default
value than can be
used as a input.

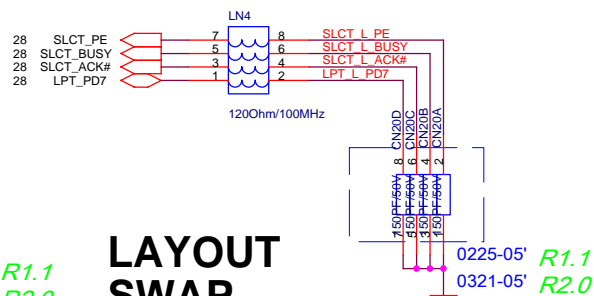
P54,P55,P43,P50 are
wake-up event inputs when
KBC in standby mode

K/B	US	UK	JP
KEYDETECT1	H	L	L
KEYDETECT2	H	H	L

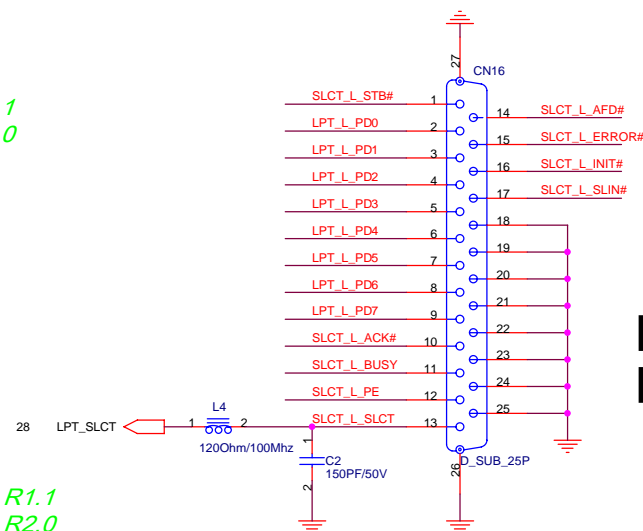
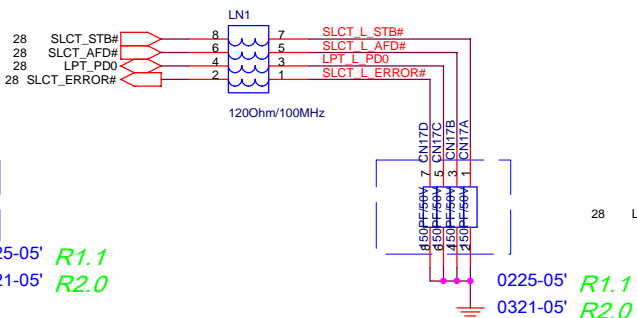
Super I/O



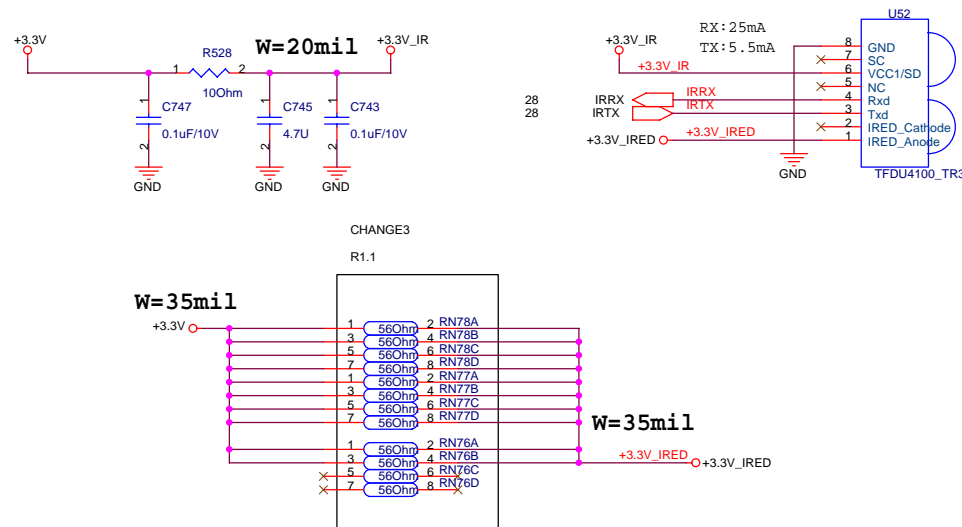
Normal : OPEN
DB Card Disable MB BIOS : LOW
DB Card Enable MB BIOS : HI
ID[0:3] : internal Pull-down 20K~100K

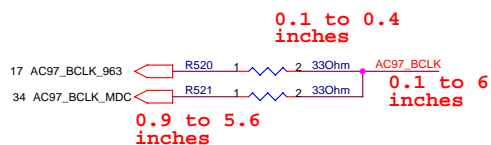
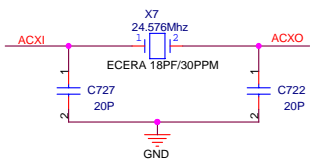


LAYOUT SWAP

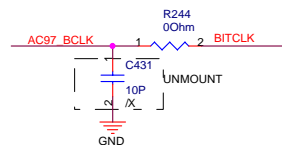


PRINT PORT

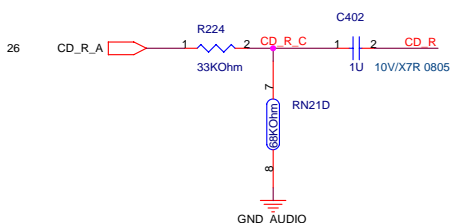
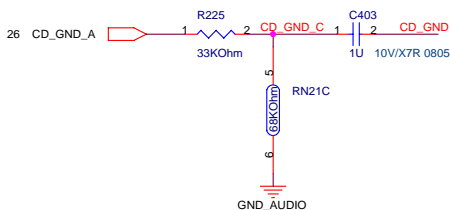
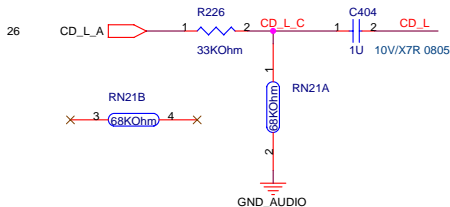
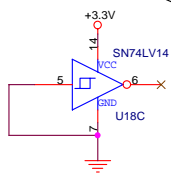




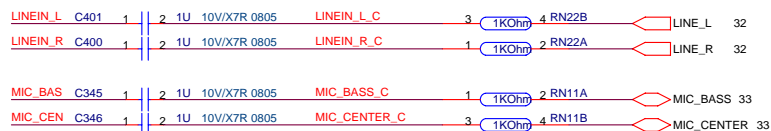
T type routing, place R at branch point.



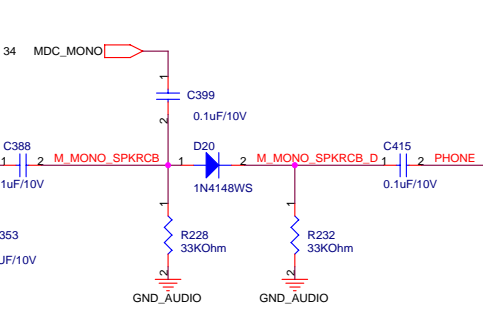
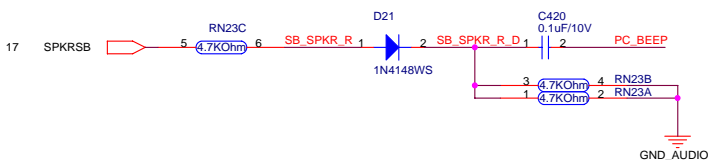
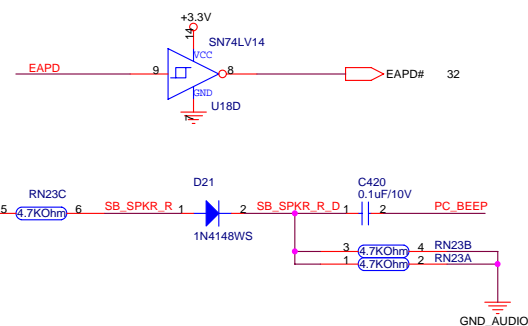
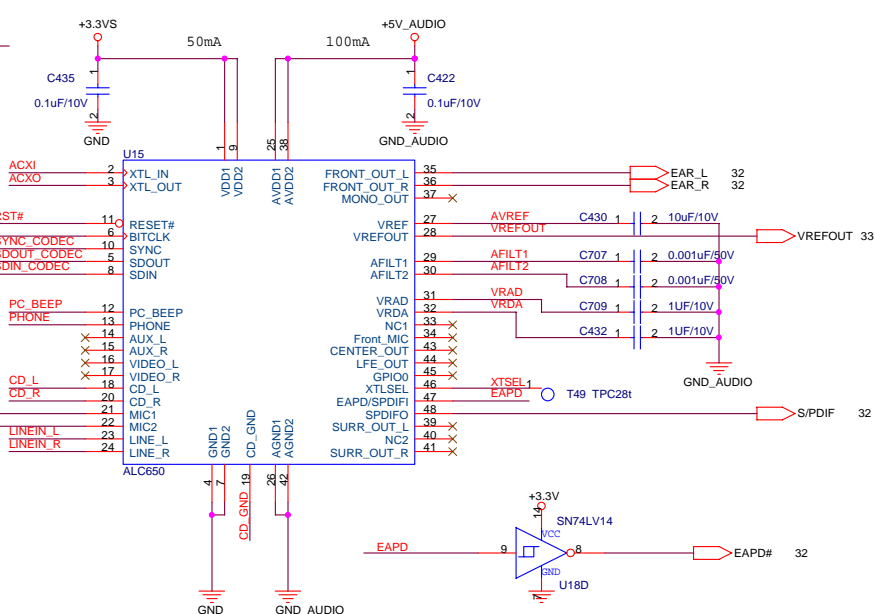
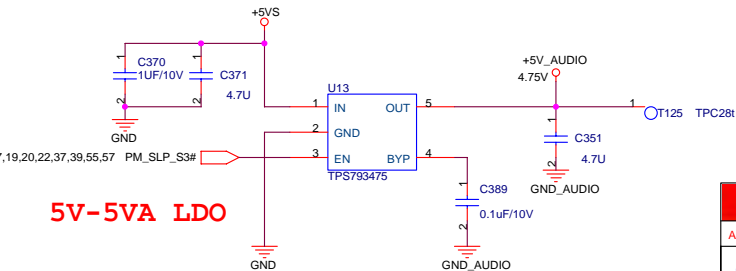
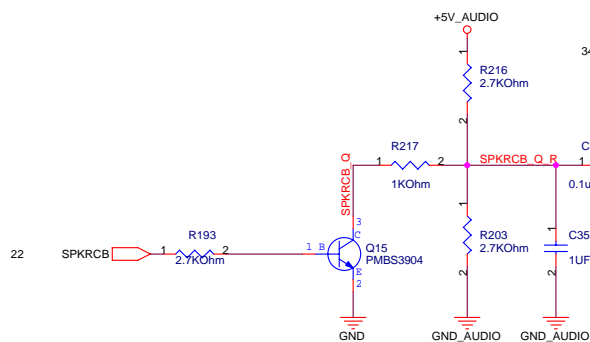
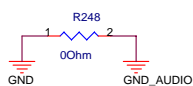
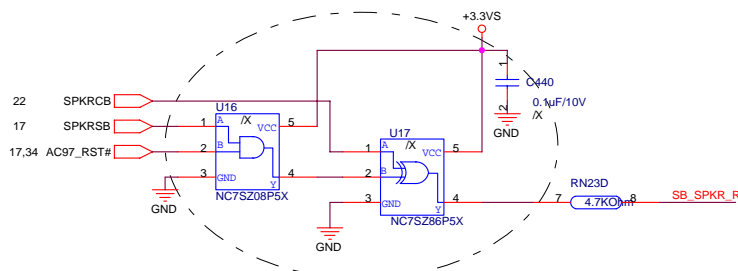
AC97	AC97_SDIN0
MDC	AC97_SDIN1

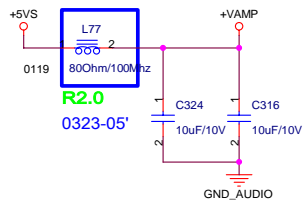
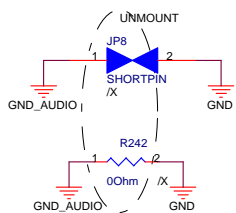
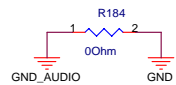


swap for layout



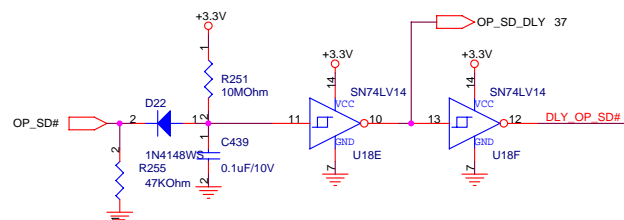
UNMOUNT



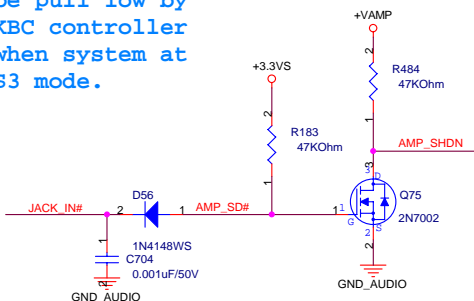


$f(\text{highpass}) = \frac{1}{2 \times 3.14 \times R \times C} = 73$
 $R = 32 \text{ Ohm}$ for Headphone, so $C = 68\mu\text{F}$
 But in order to reduce component type, use $100\mu\text{F}/6.3\text{V}$ (11-041210721), but $100\mu\text{F}$ is too big for A3N, so change to $47\mu\text{F}$.

LOSS U3202A~D



For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.

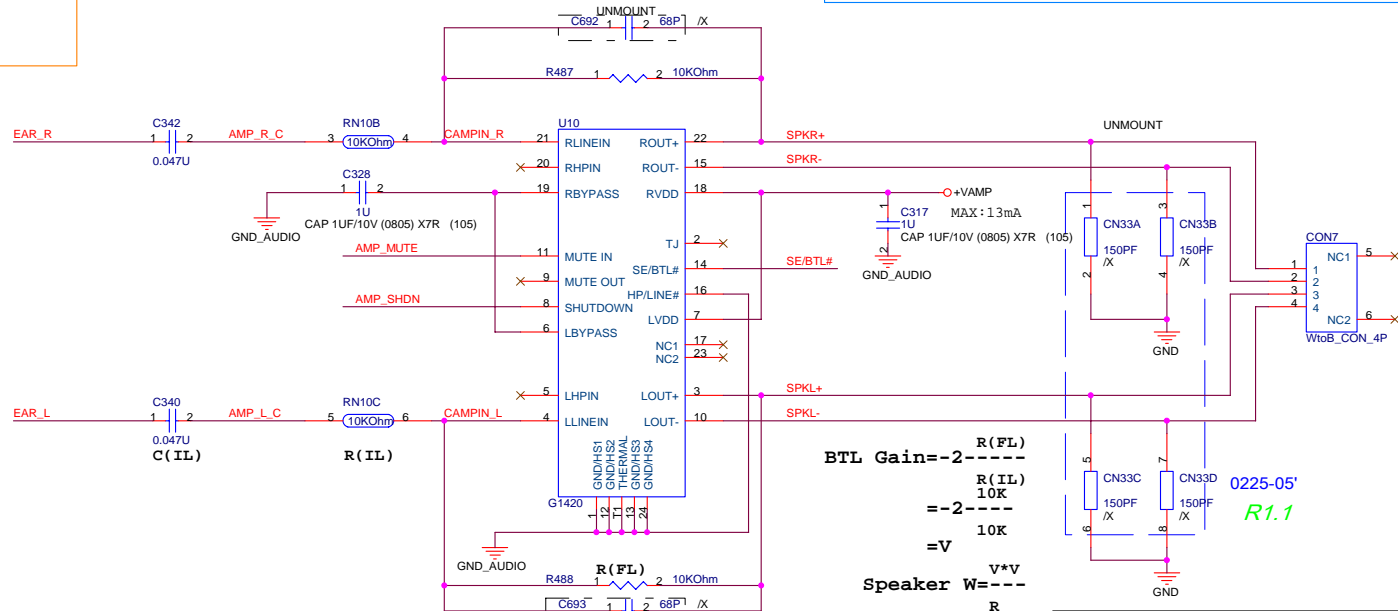
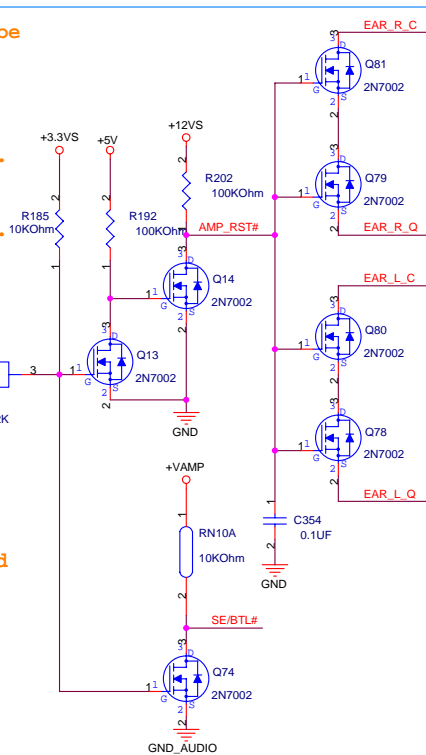


$$f(\text{highpass}) = \frac{1}{2 \times 3.14 \times C(\text{IL}) \times R(\text{IL})} = 500$$

$$f(\text{lowpass}) = \frac{1}{2 \times 3.14 \times C(150\text{P}) \times R(10\text{K})} = 106\text{K}$$

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

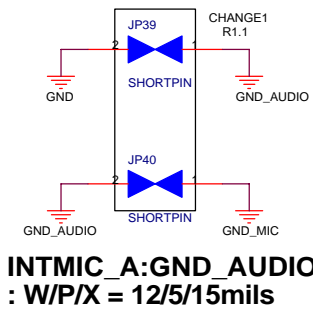
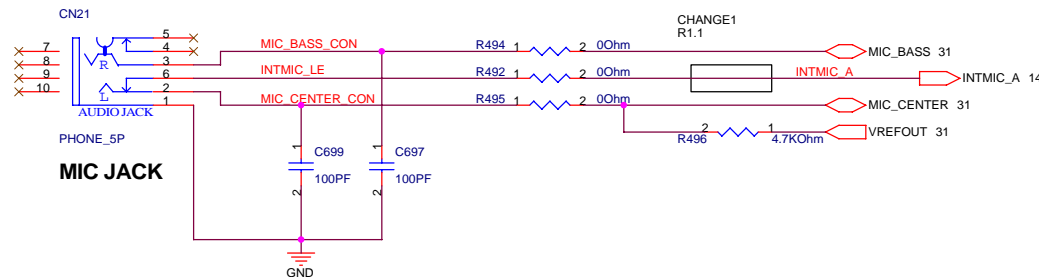
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.



BTL Gain = $-\frac{R(\text{FL})}{R(\text{IL})} = -\frac{10\text{K}}{10\text{K}} = -1$
 $\text{Speaker } W = \frac{V^2}{R} = \frac{4\text{ohm}}{2 \times 2} = 1\text{W}$
 Can use 1W(4ohm) speaker

MIC OP CIRCUIT

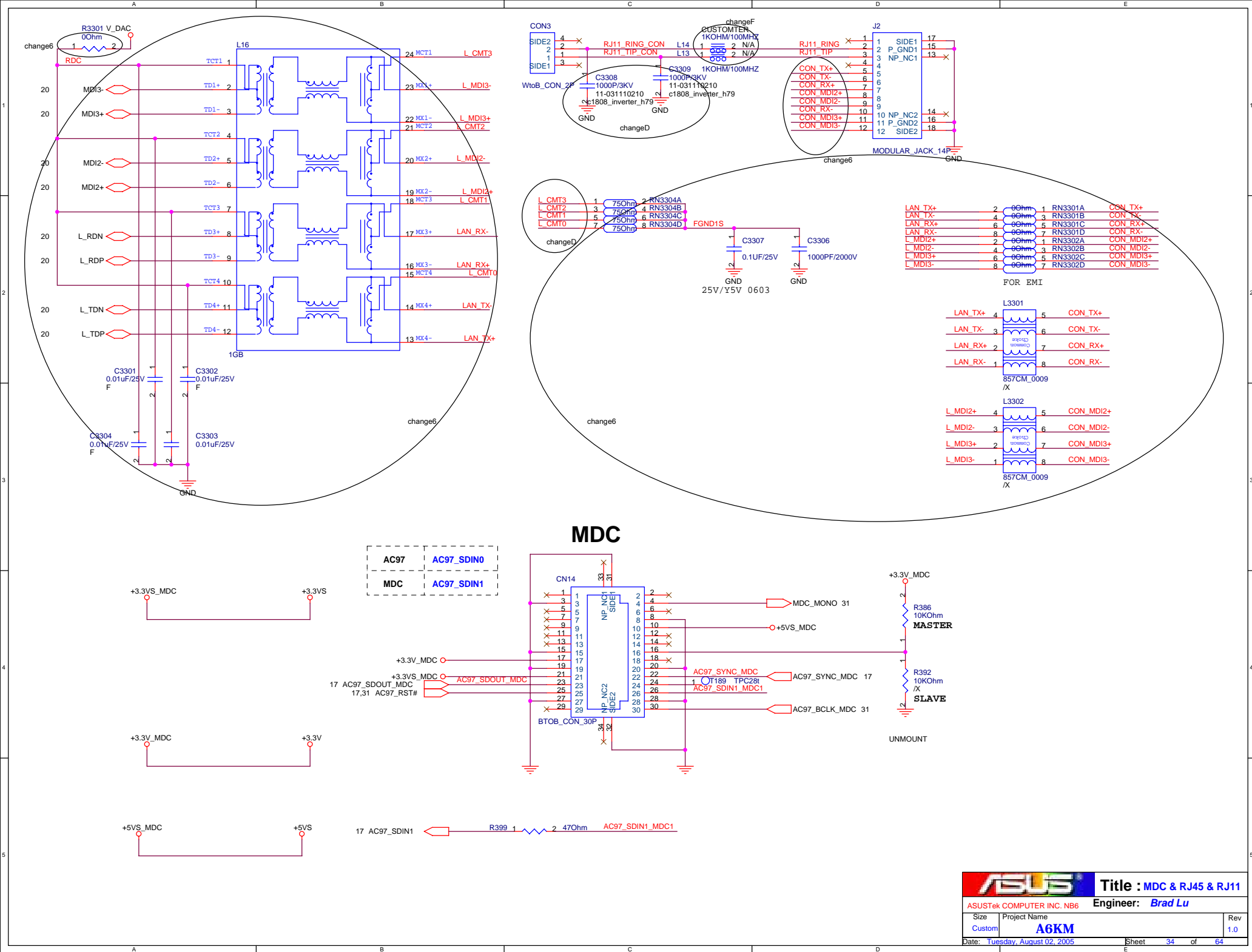
MIC JACK

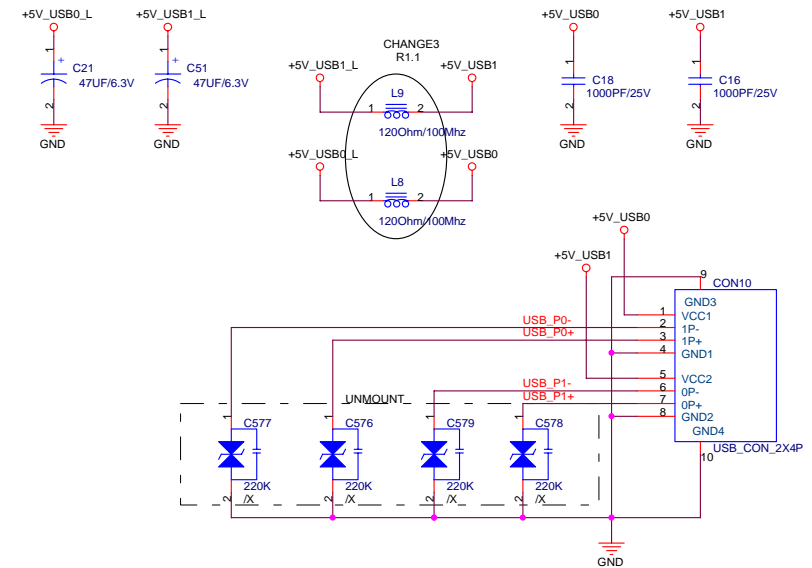
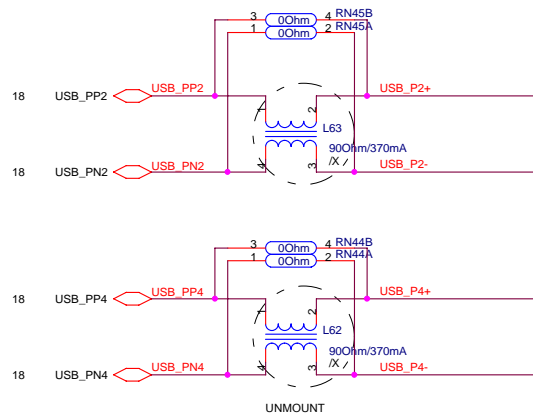
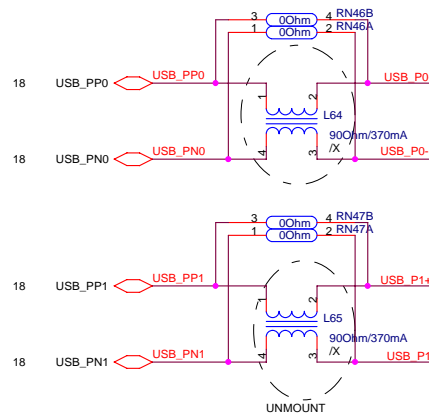
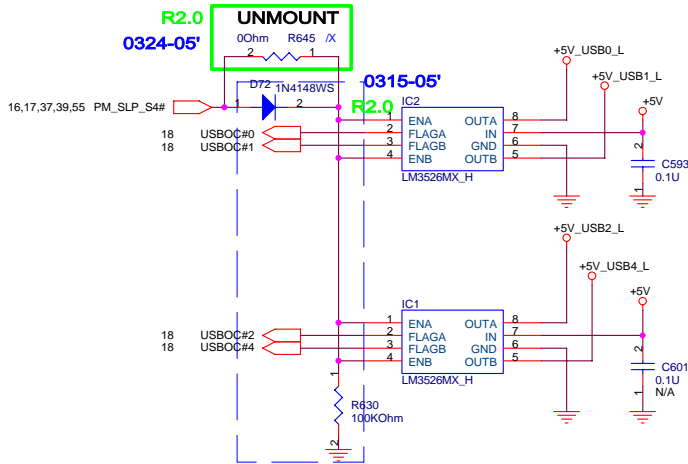


R111 & R112
change to
09-013103013
in R1.2 BOM

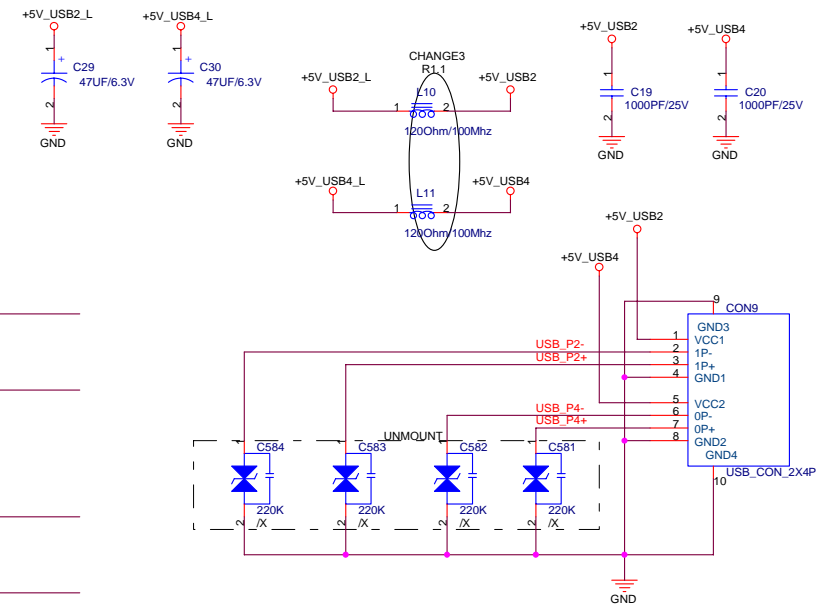
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

ASUS		Title : MIC	
ASUSTek COMPUTER INC. NB6		Engineer: Brad Lu	
Size Custom	Project Name A6KM	Date: Tuesday, August 02, 2005	Rev 1.0
Sheet 33 of 64			

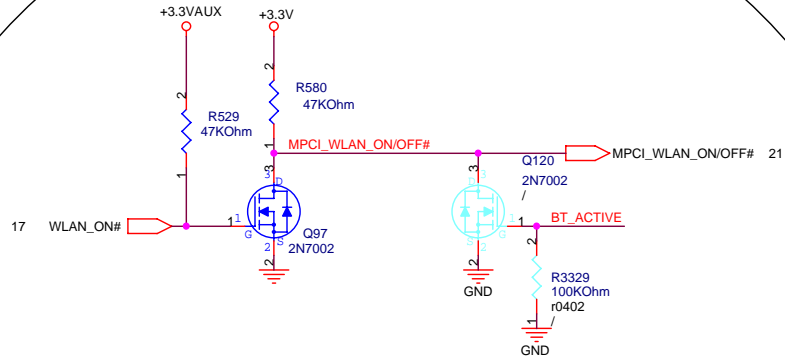




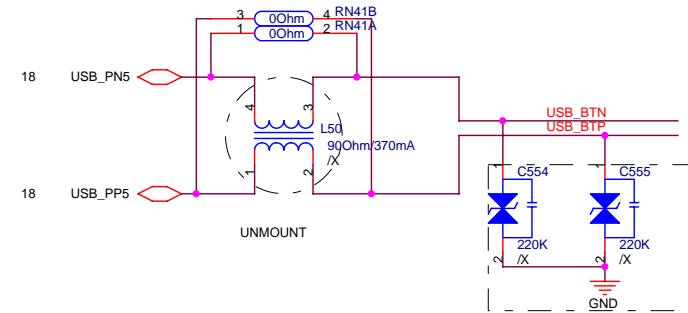
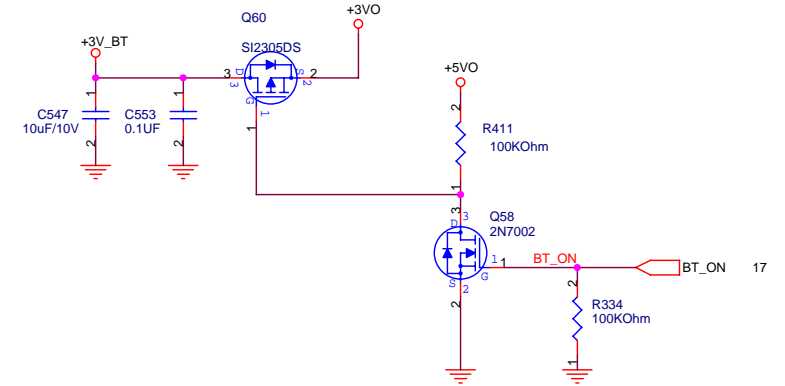
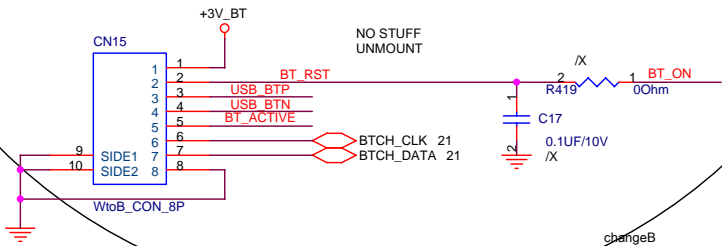
USB PORT 0 & PORT 1



USB PORT 2 & PORT 4



Bluetooth Module Connector



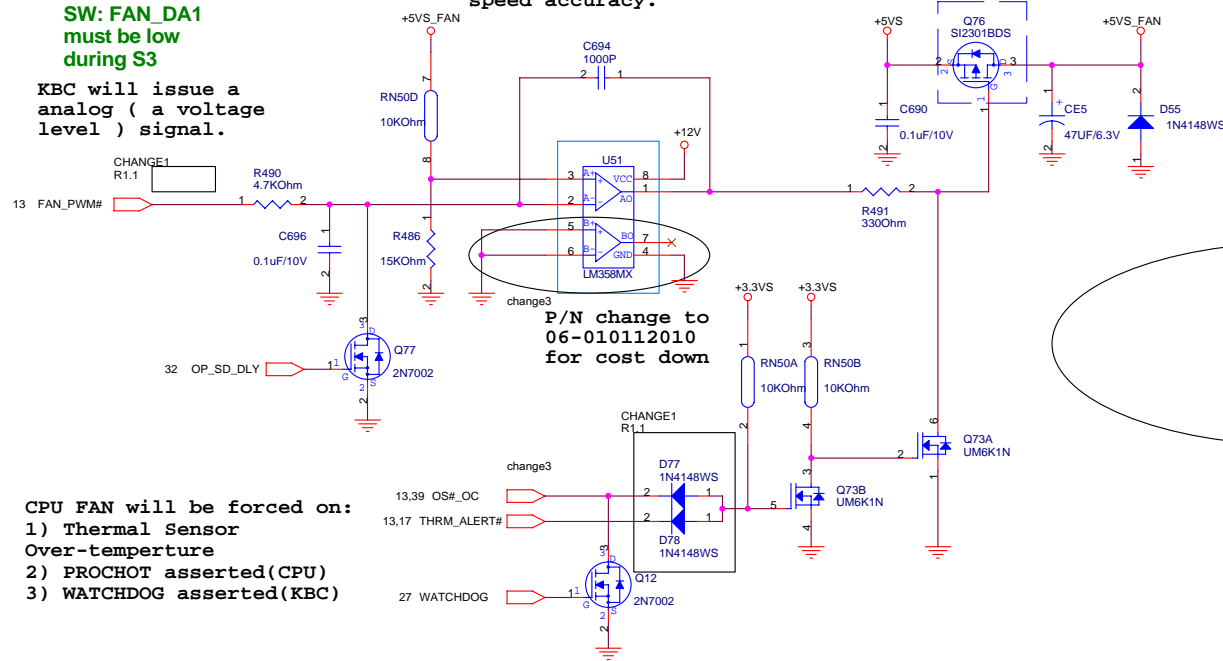
USB PORT 5 for Bluetooth Module

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.

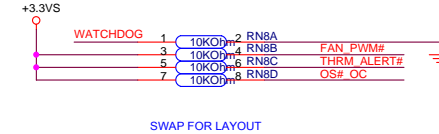


When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

CPU FAN will be forced on:

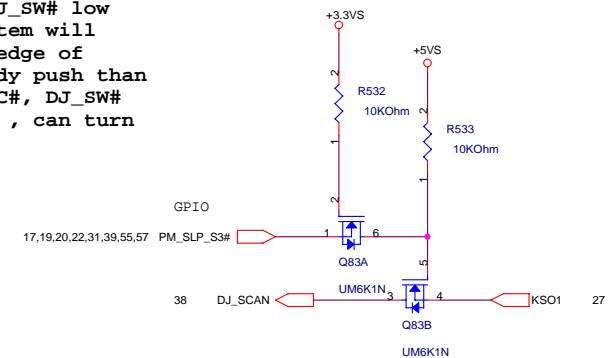
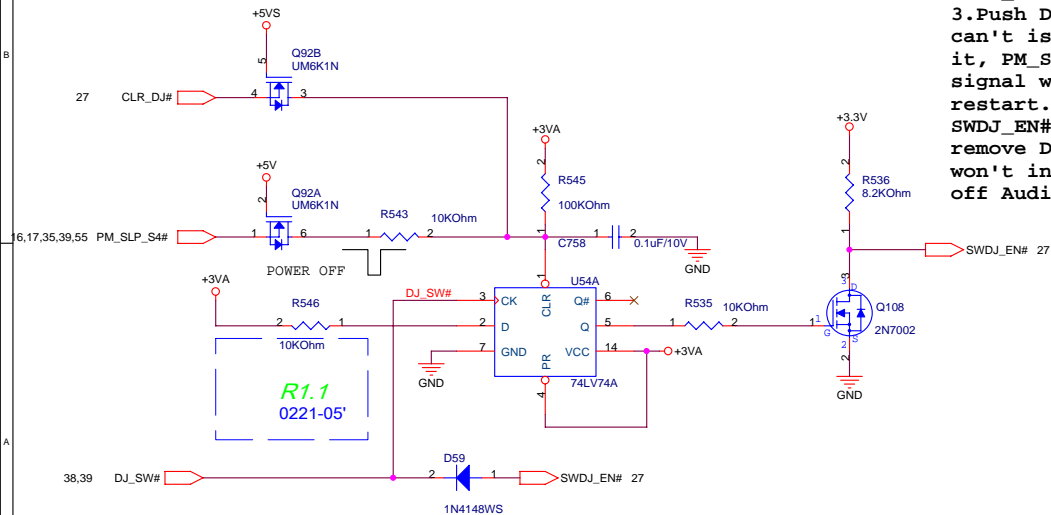
- 1) Thermal Sensor
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

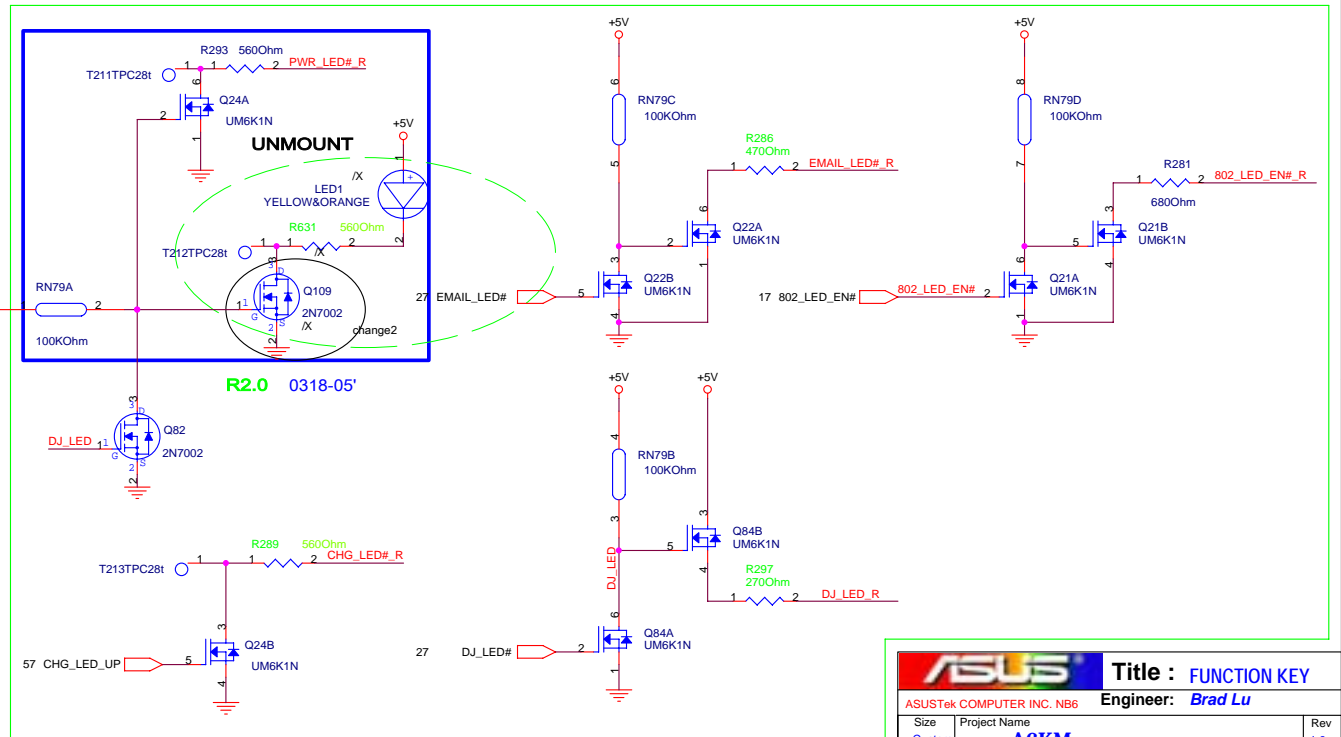
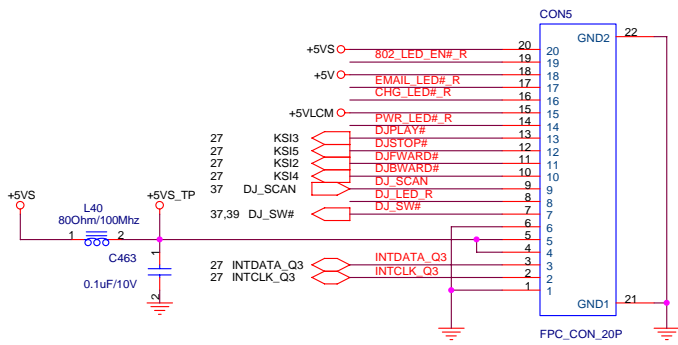
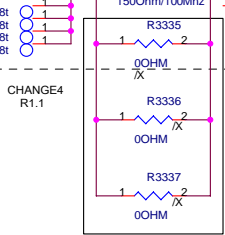
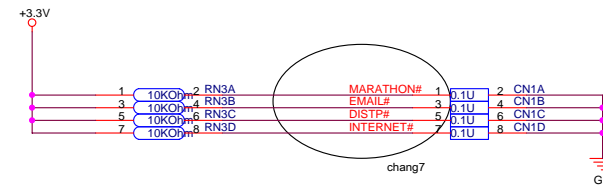
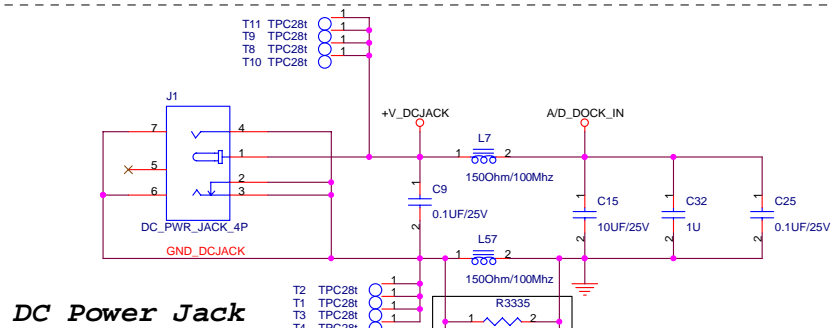
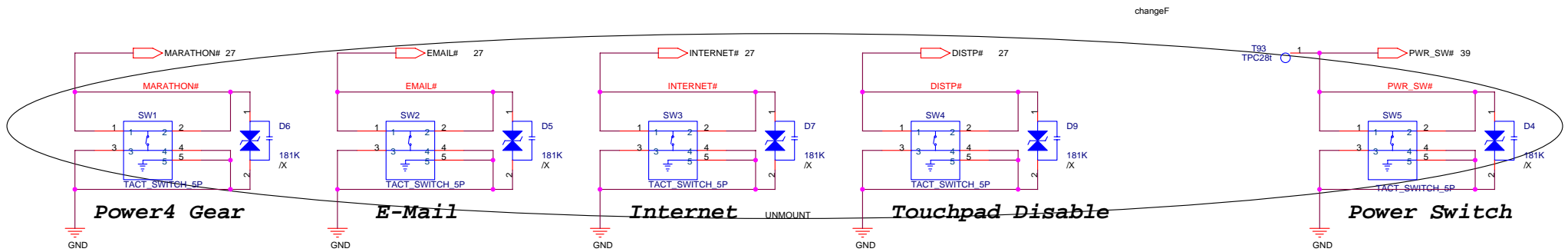


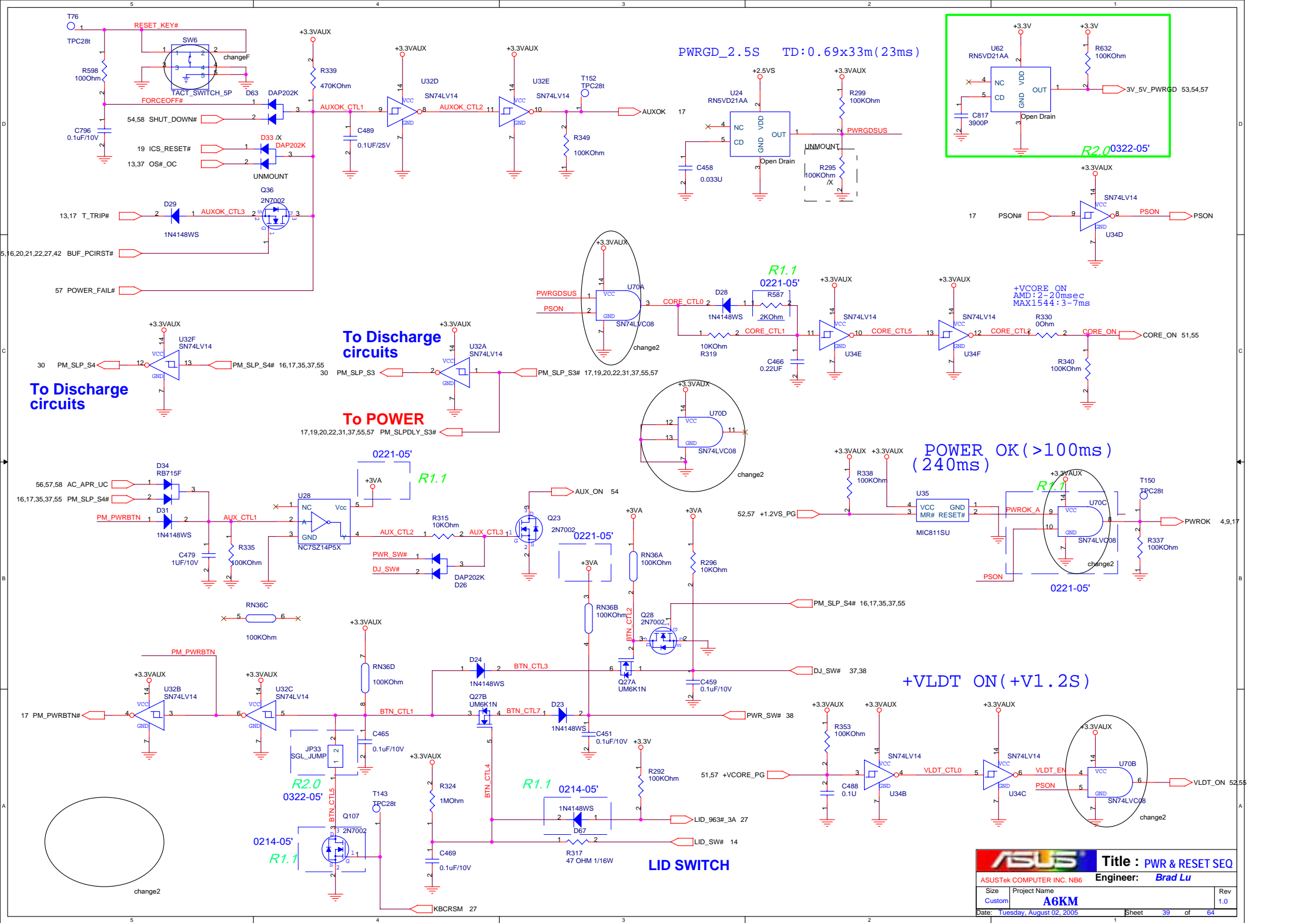
SWDJ_EN# function :

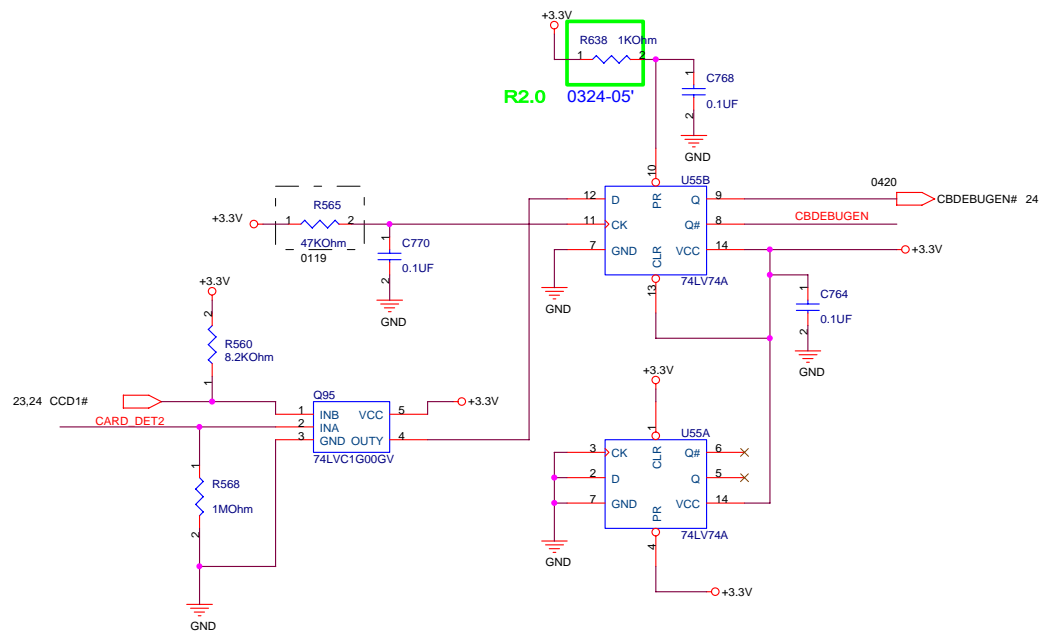
- 1.Push DJ_SW#, turn on Audio DJ.
- 2.PM_SLP_S4# will keep high.
- 3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

Audio DJ







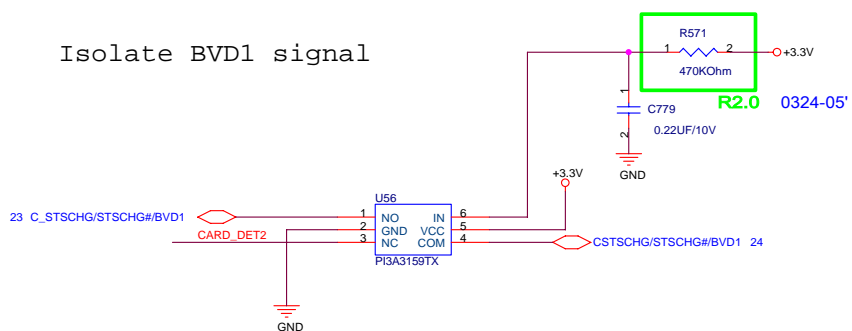


PCMCIA DEBUG PORT

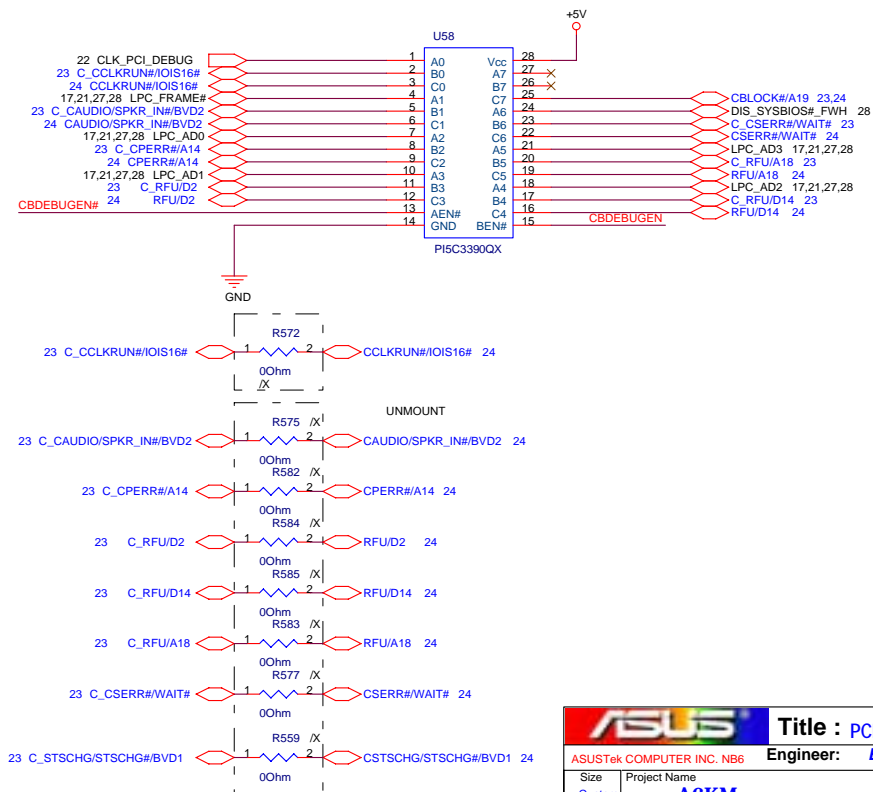
Isolate card bus control and slot signal when debug card plug in

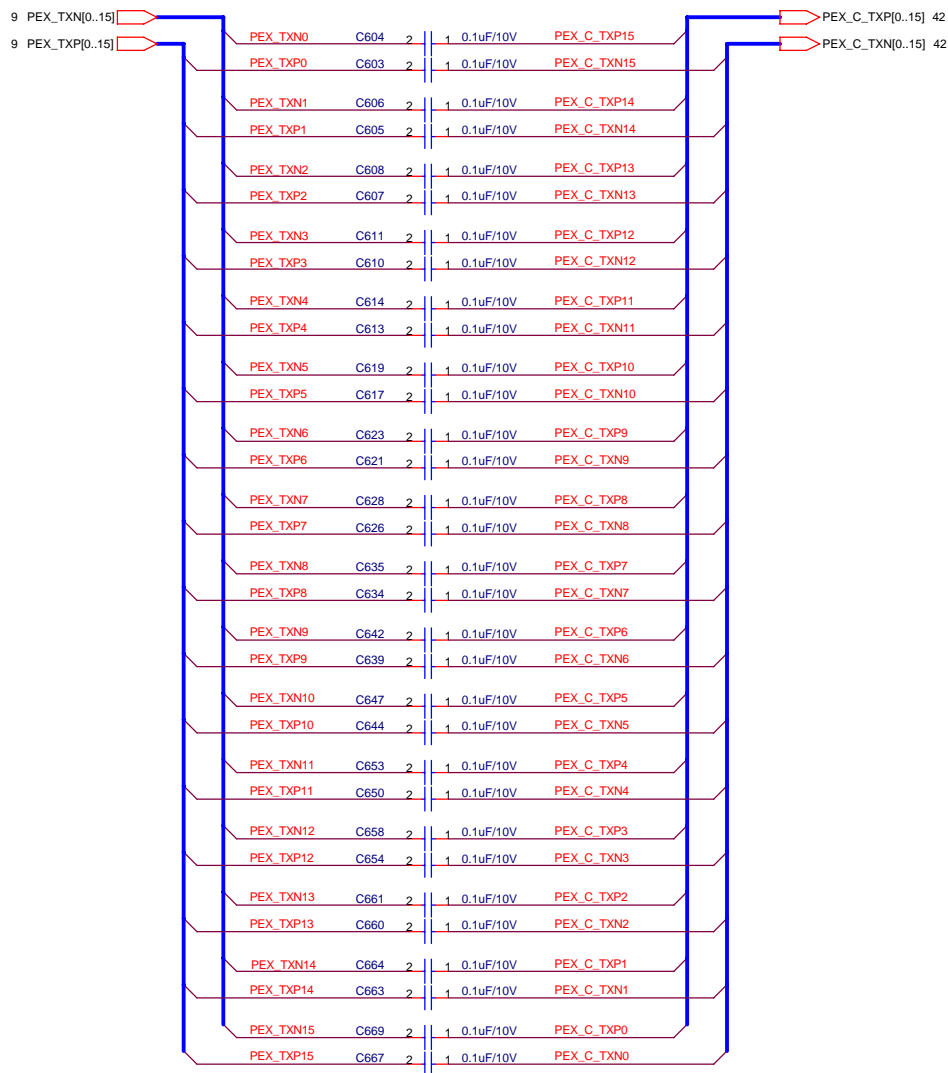
RC value may need to tuned for each product.

Isolate BVD1 signal



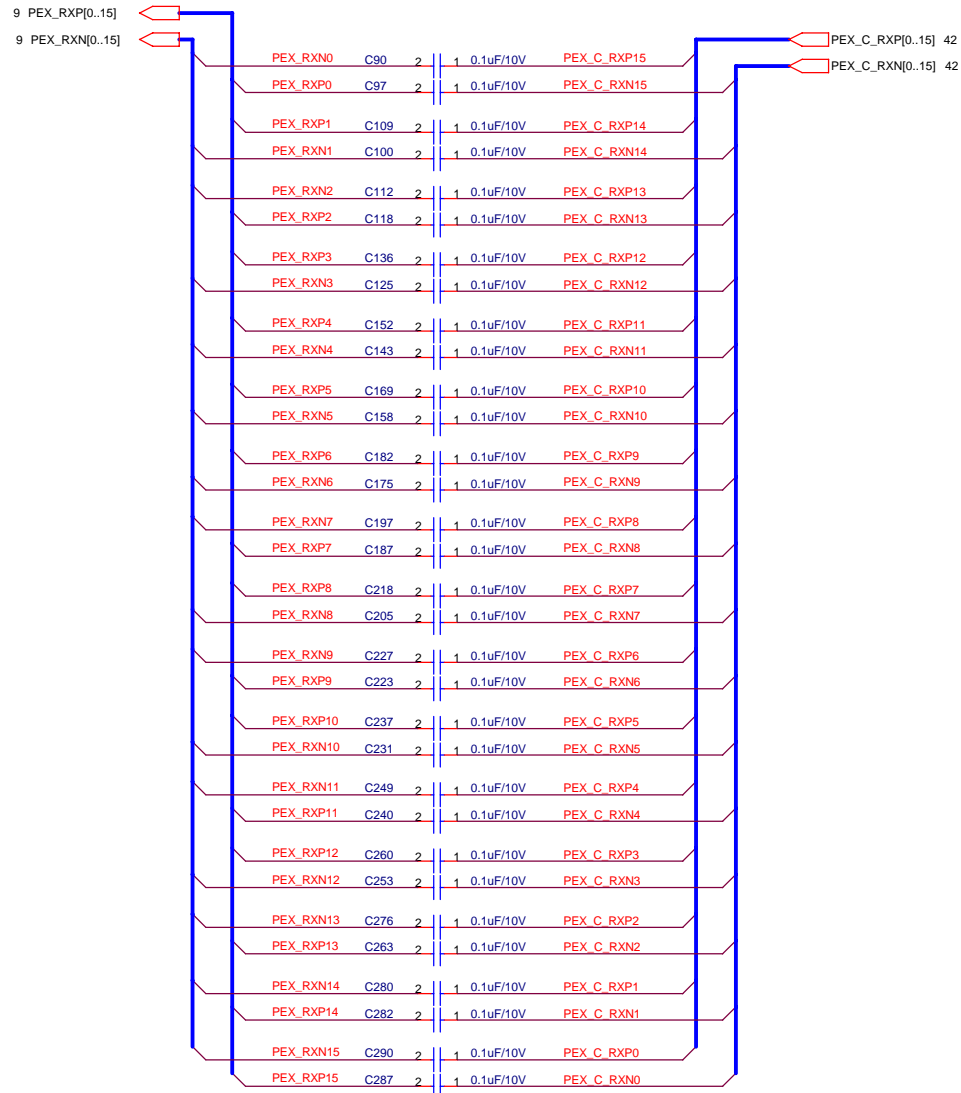
When +3V on, select BVD1 to CARD_DET2 for RC delay time





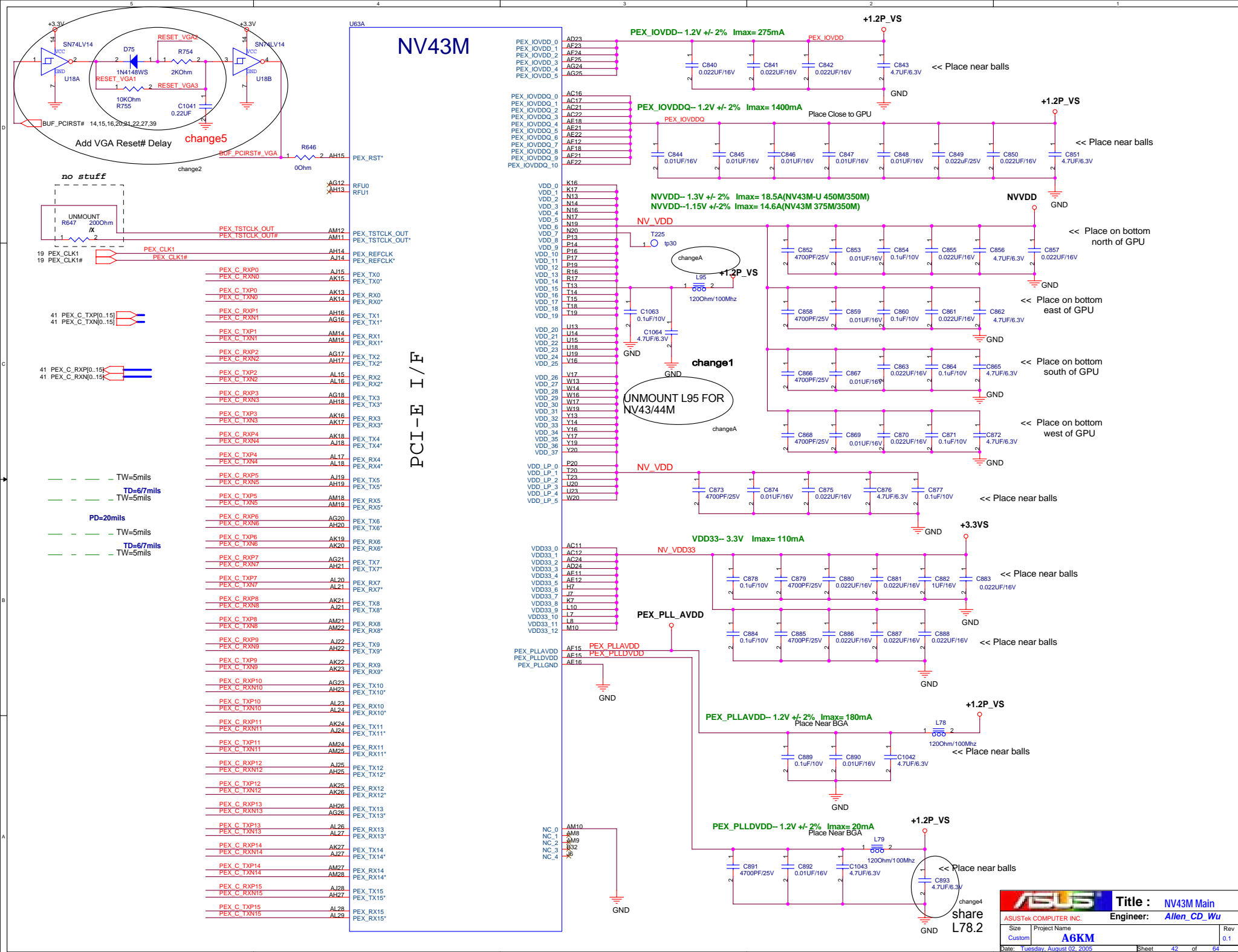
PLACE these 0402 AC coupling caps close to sis756.

TX P&N [0..15] PIN SWAP FOR LAYOUT

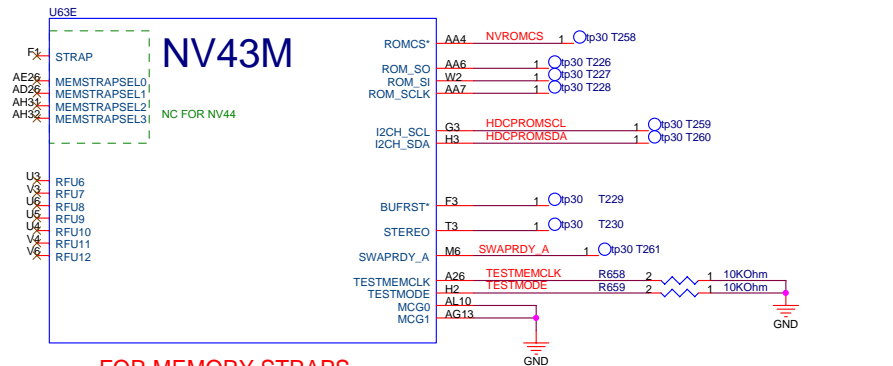


PLACE these 0402 AC coupling caps close to nv44m

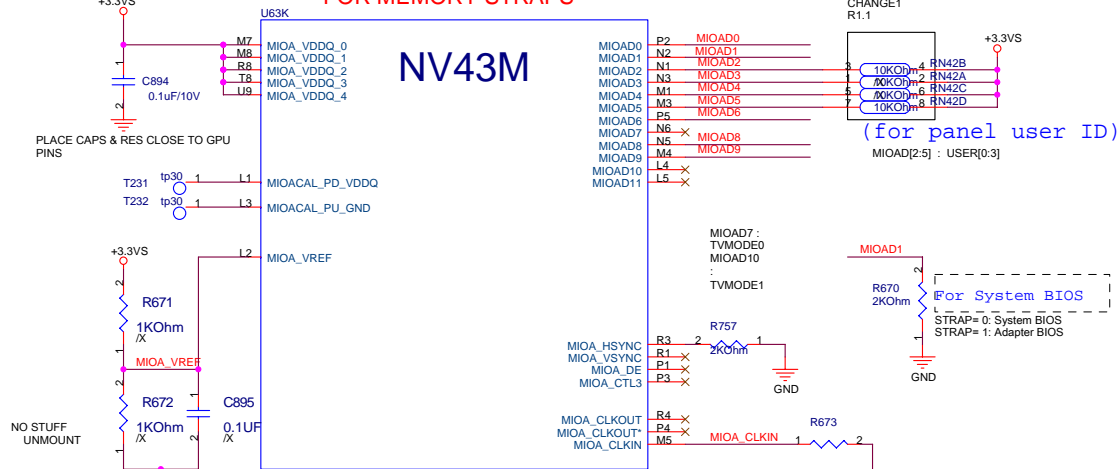
RX P&N 0.2.7.9.11.13.14.15 PIN SWAP FOR LAYOUT



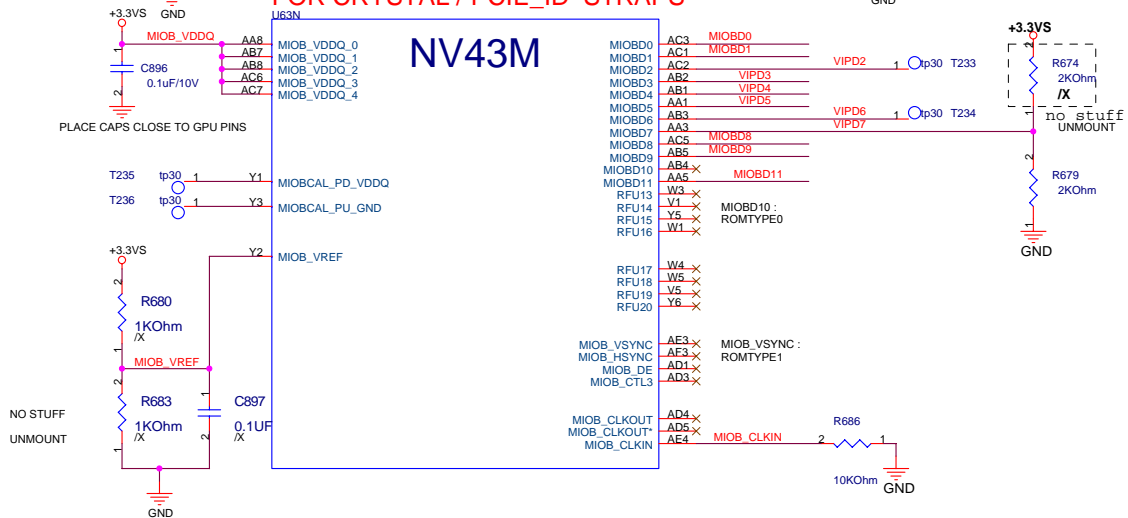
FOR MEMORY STRAPS



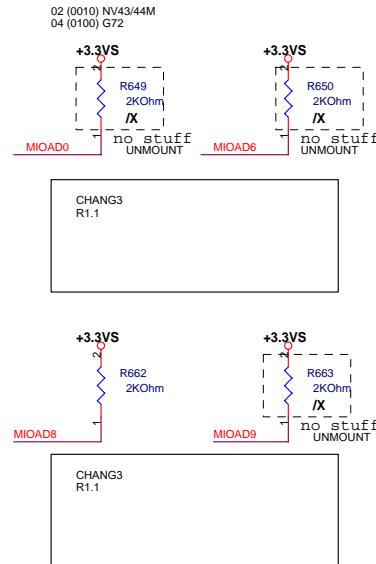
FOR MEMORY STRAPS



FOR CRYSTAL / PCIE_ID STRAPS



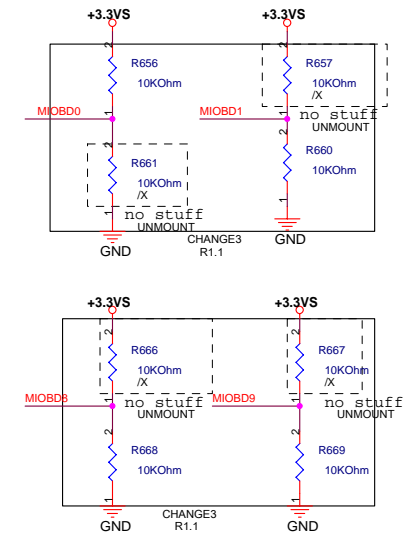
3G O PADCFG STRP



MEM TYPE STRAP

NV43M memory strap setting:
01 (0001) 8MX32 DDR 128-bit 1.8V I/O
04 (0100) 4MX32 DDR 128-bit 1.8V I/O Samsung
05 (0101) 4MX32 DDR 128-bit 1.8V I/O Hynix
09 (1001) 8MX32 DDR 64-bit 1.8V I/O
0C (1100) 4MX32 DDR 64-bit 1.8V I/O Samsung
0D (1101) 4MX32 DDR 64-bit 1.8V I/O Hynix

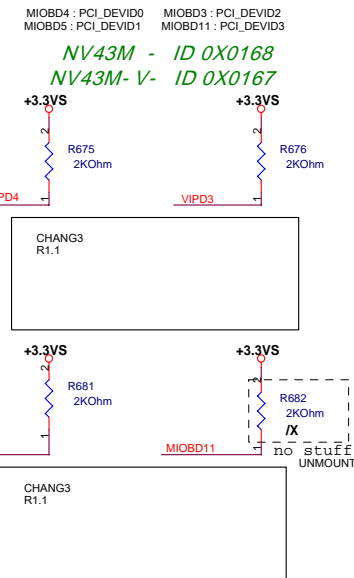
MIOBD0: RAMCFG0 MIOBD1: RAMCFG1
MIOBD8: RAMCFG2 MIOBD9: RAMCFG3

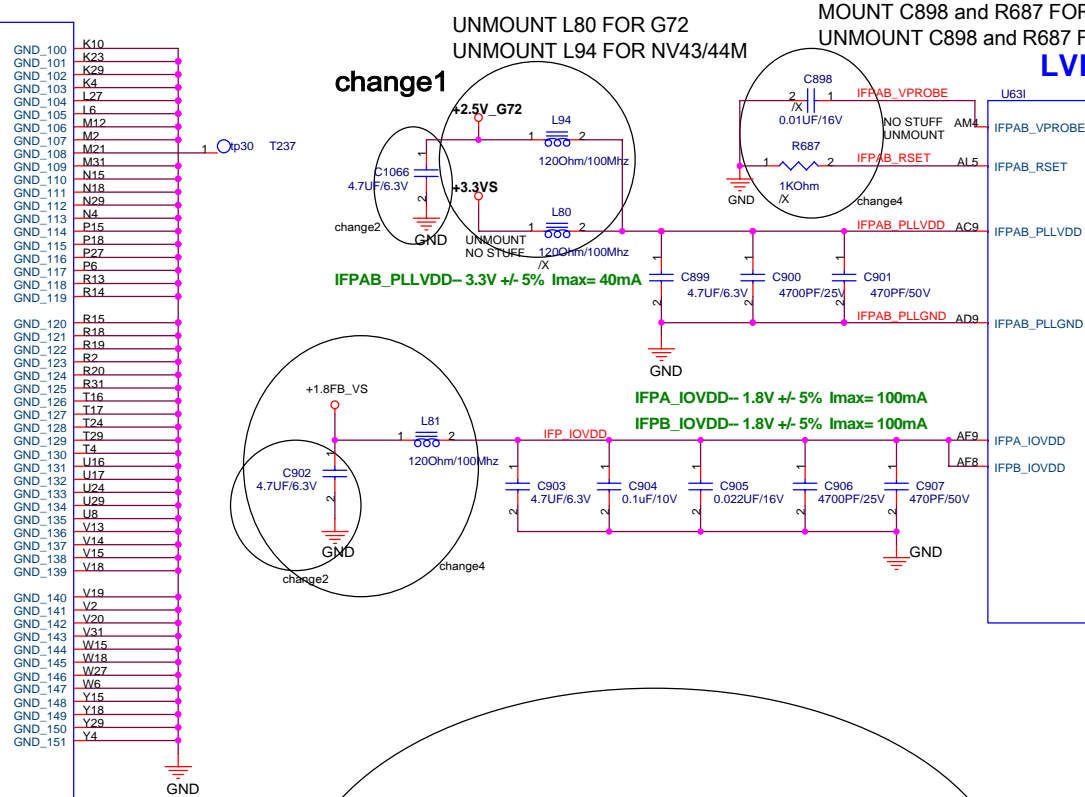
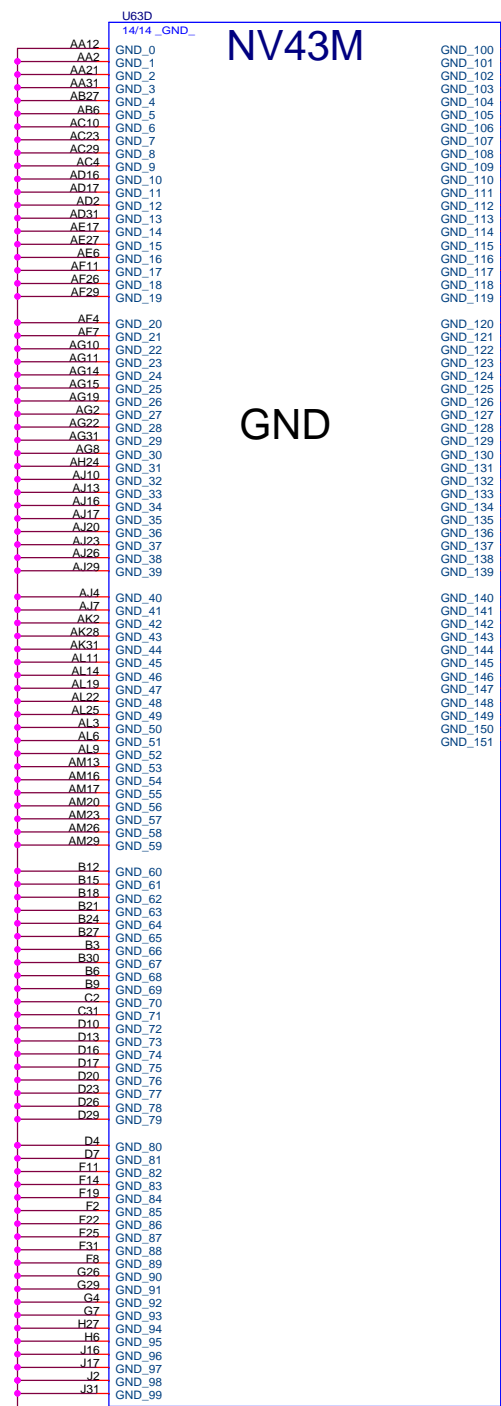


MEM TYPE STRAP

NV44M memory strap setting:
01 (0001) 8MX32 DDR 64-bit 1.8V I/O
04 (0100) 4MX32 DDR 64-bit 1.8V I/O Samsung
05 (0101) 4MX32 DDR 64-bit 1.8V I/O Hynix
09 (1001) 8MX32 DDR 32-bit 1.8V I/O
0C (1100) 4MX32 DDR 32-bit 1.8V I/O Samsung
0D (1101) 4MX32 DDR 32-bit 1.8V I/O Hynix

(PCI_DEVICE_ID)

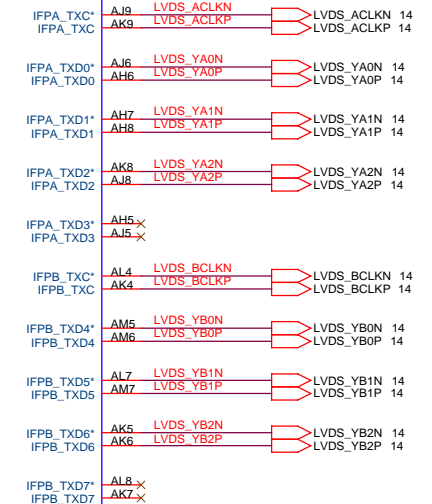




MOUNT C898 and R687 FOR NV44
UNMOUNT C898 and R687 FOR G72

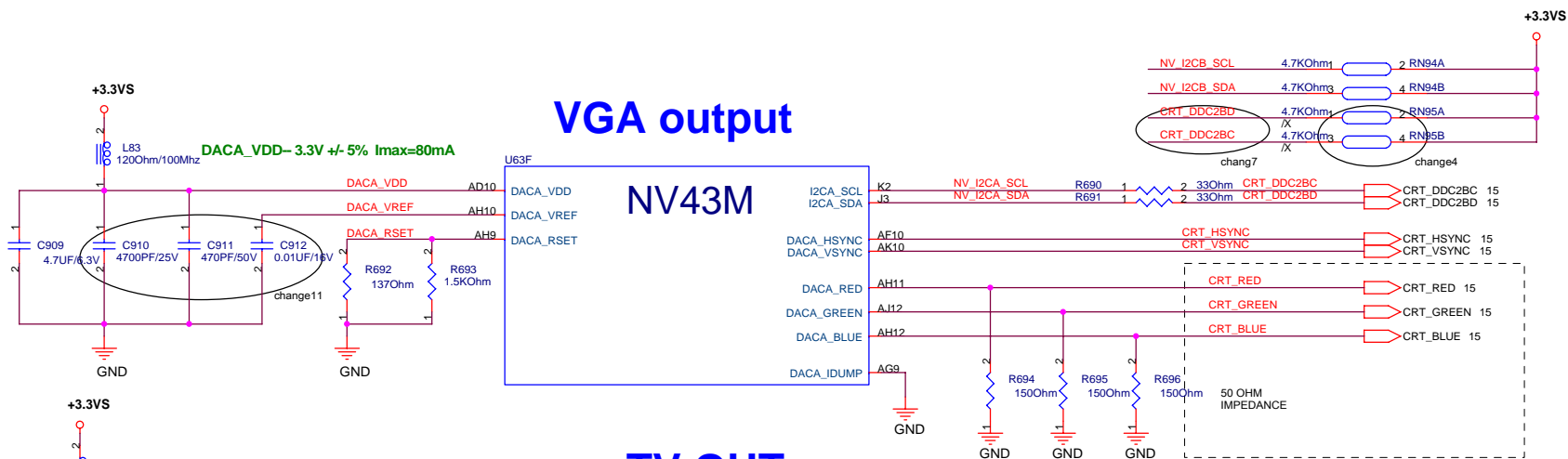
LVDS/Panel control

NV43M

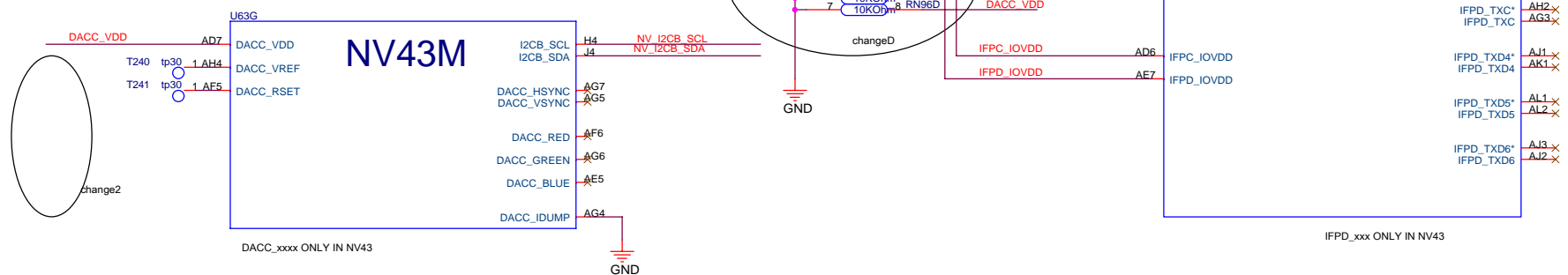
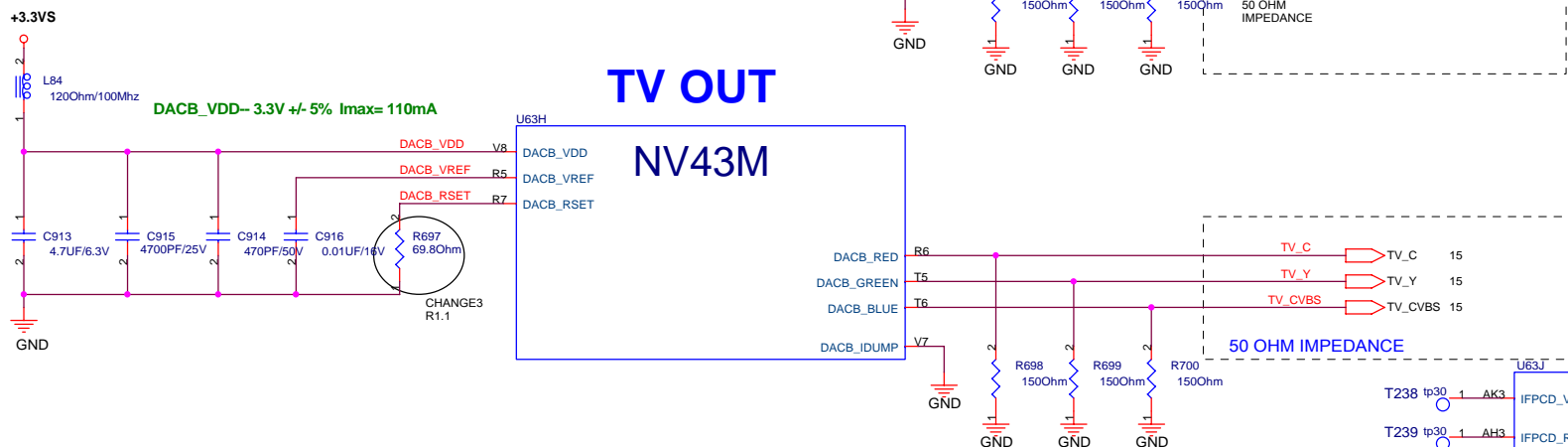


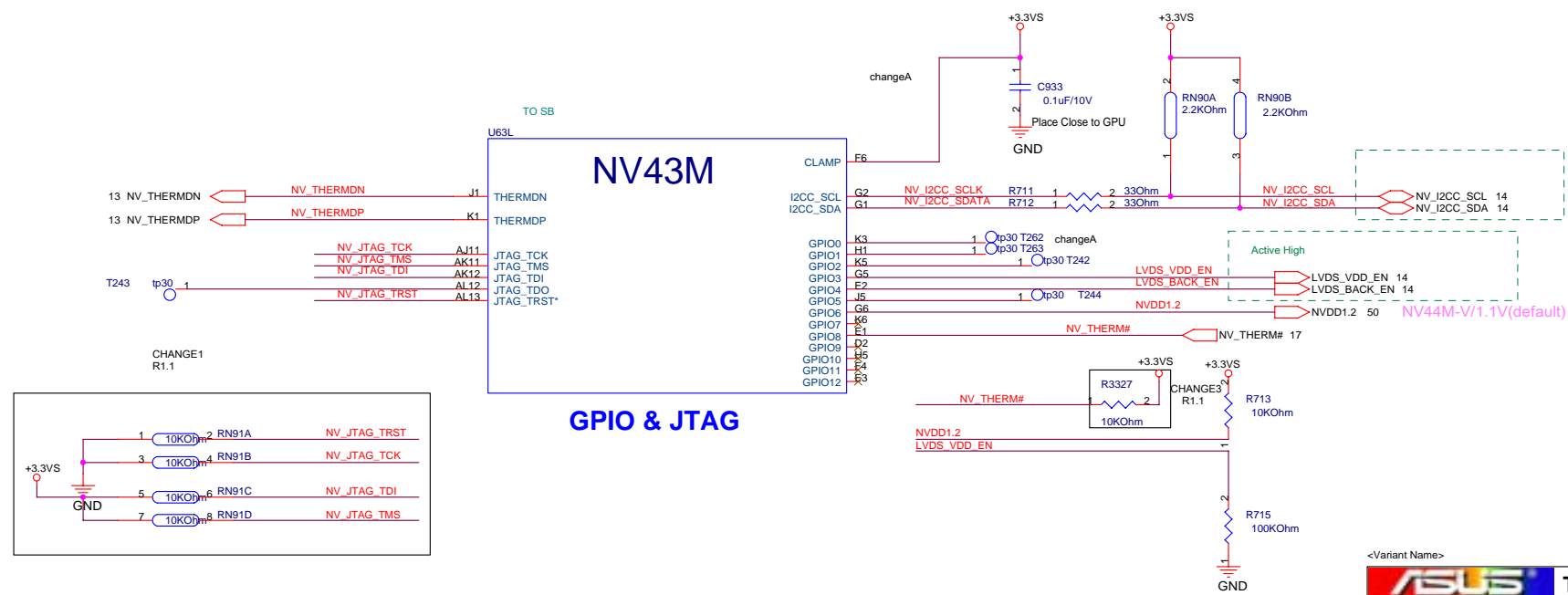
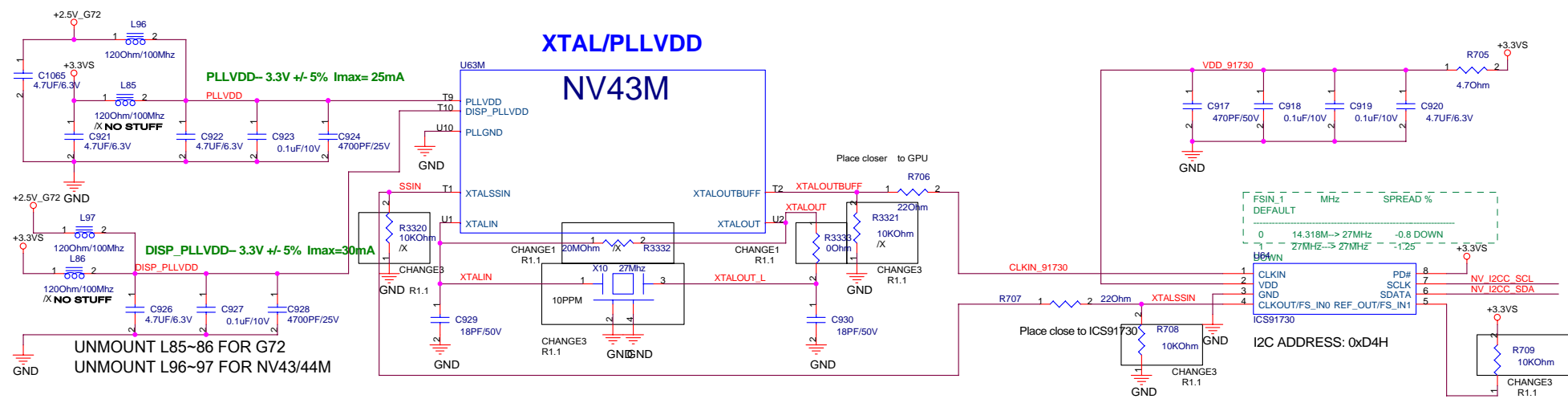
<Variant Name>

		Title : NV43M LVDS	
ASUSTek COMPUTER INC.		Engineer: Allen_CD_Wu	
Size Custom	Project Name A6KM	Rev 0.1	
Date: Tuesday, August 02, 2005		Sheet 44 of 64	



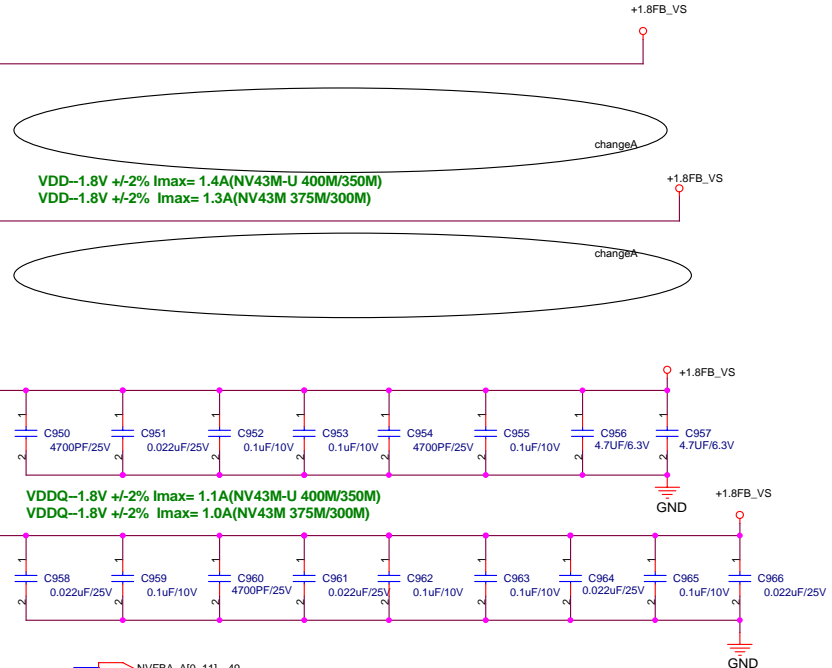
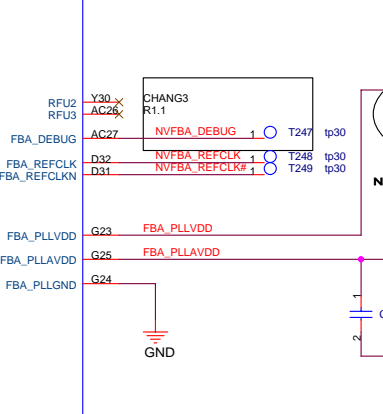
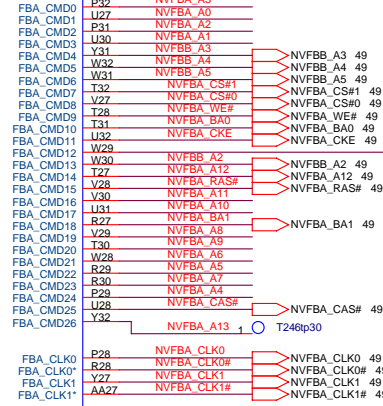
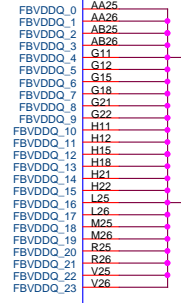
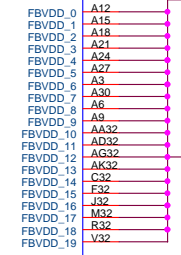
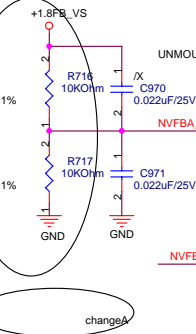
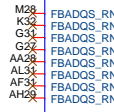
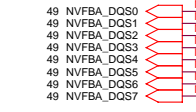
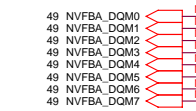
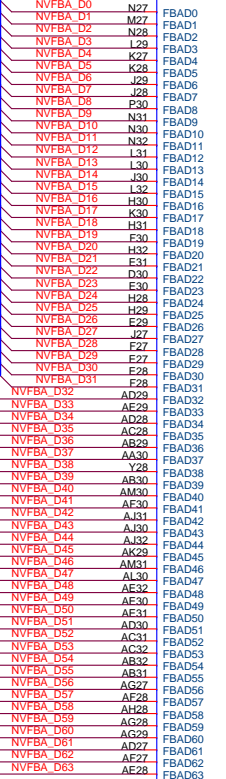
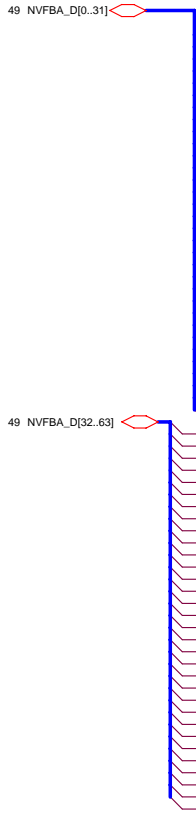
MOUNT RN95 FOR NV44
UNMOUNT RN95 FOR G72

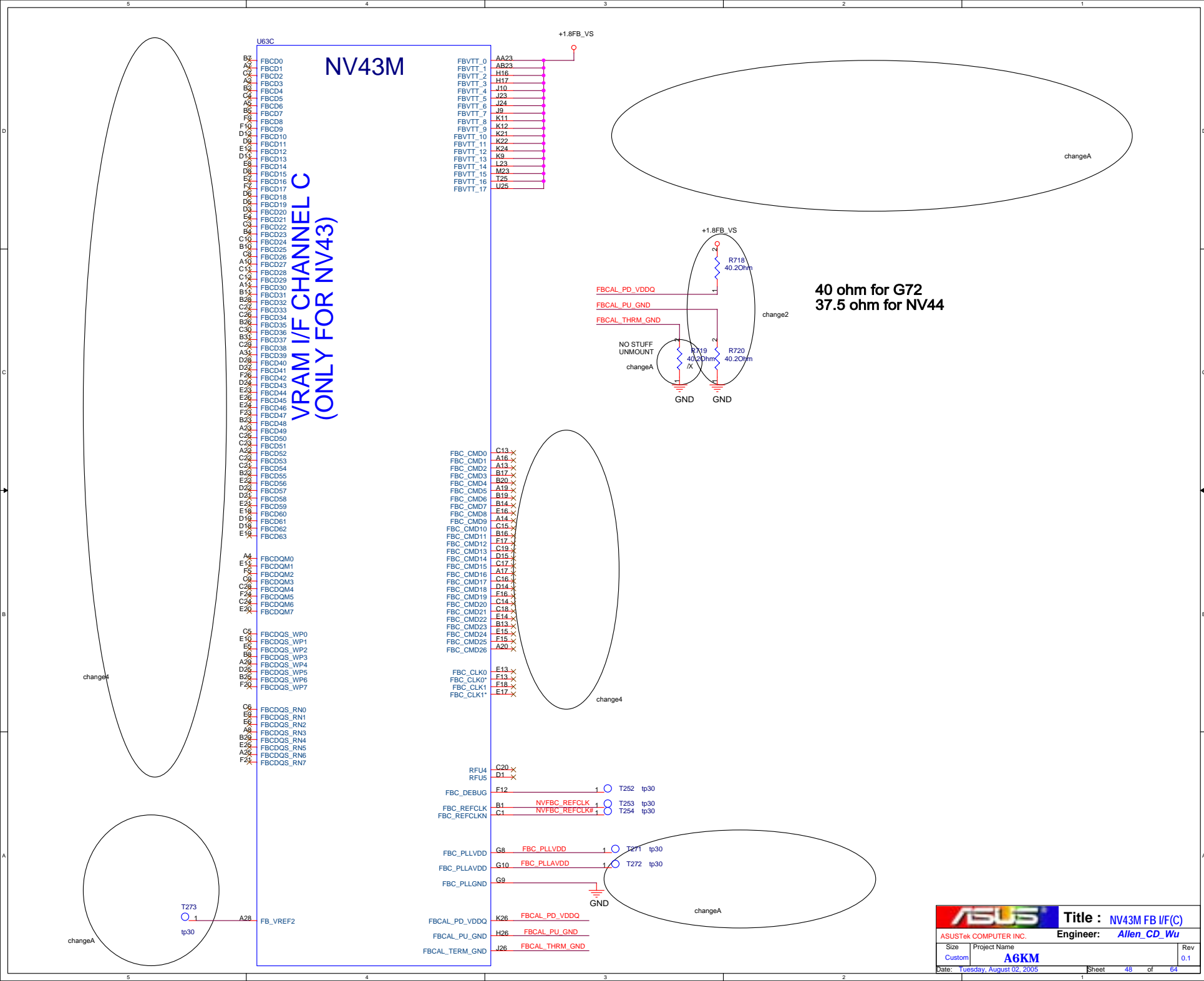




NV43M

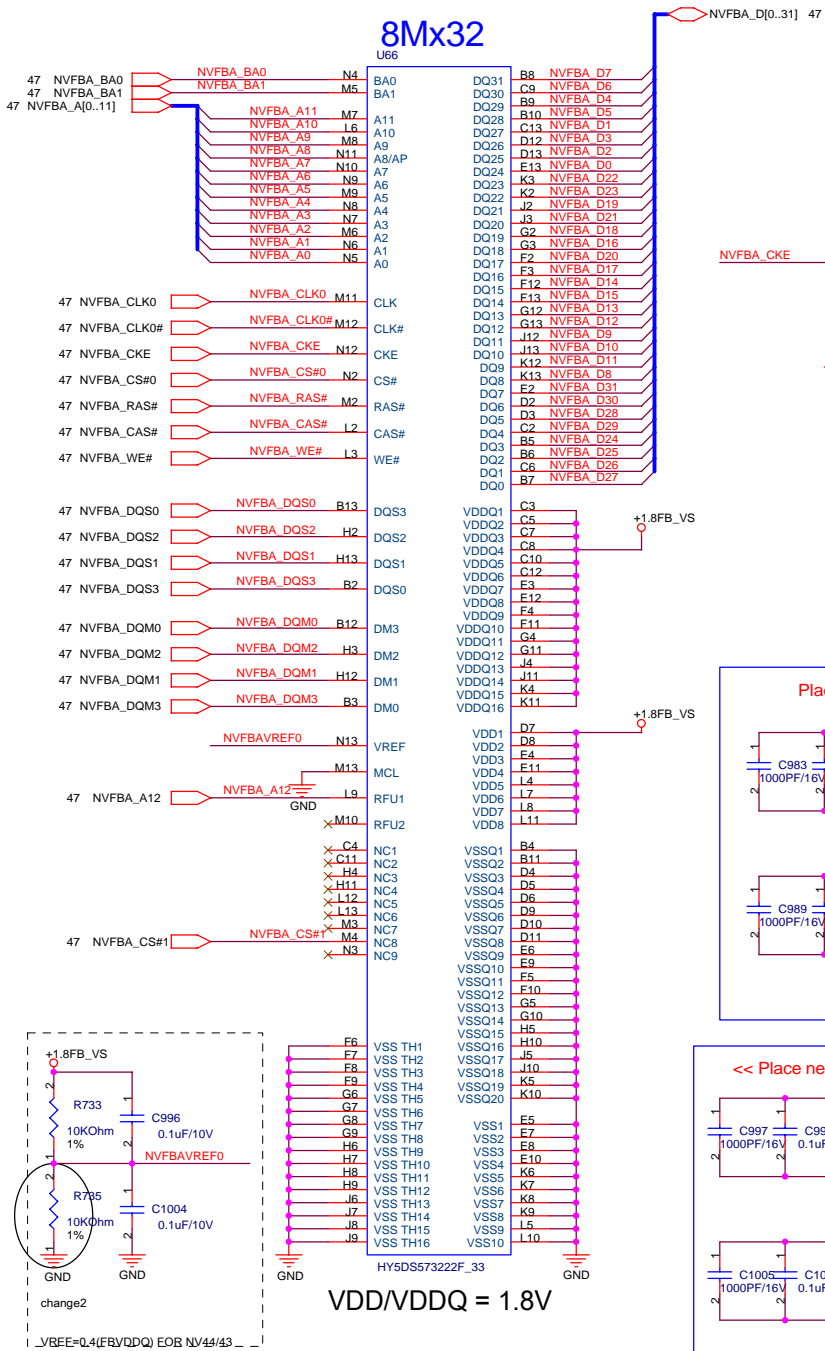
VRAM I/F Channel A





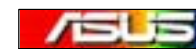
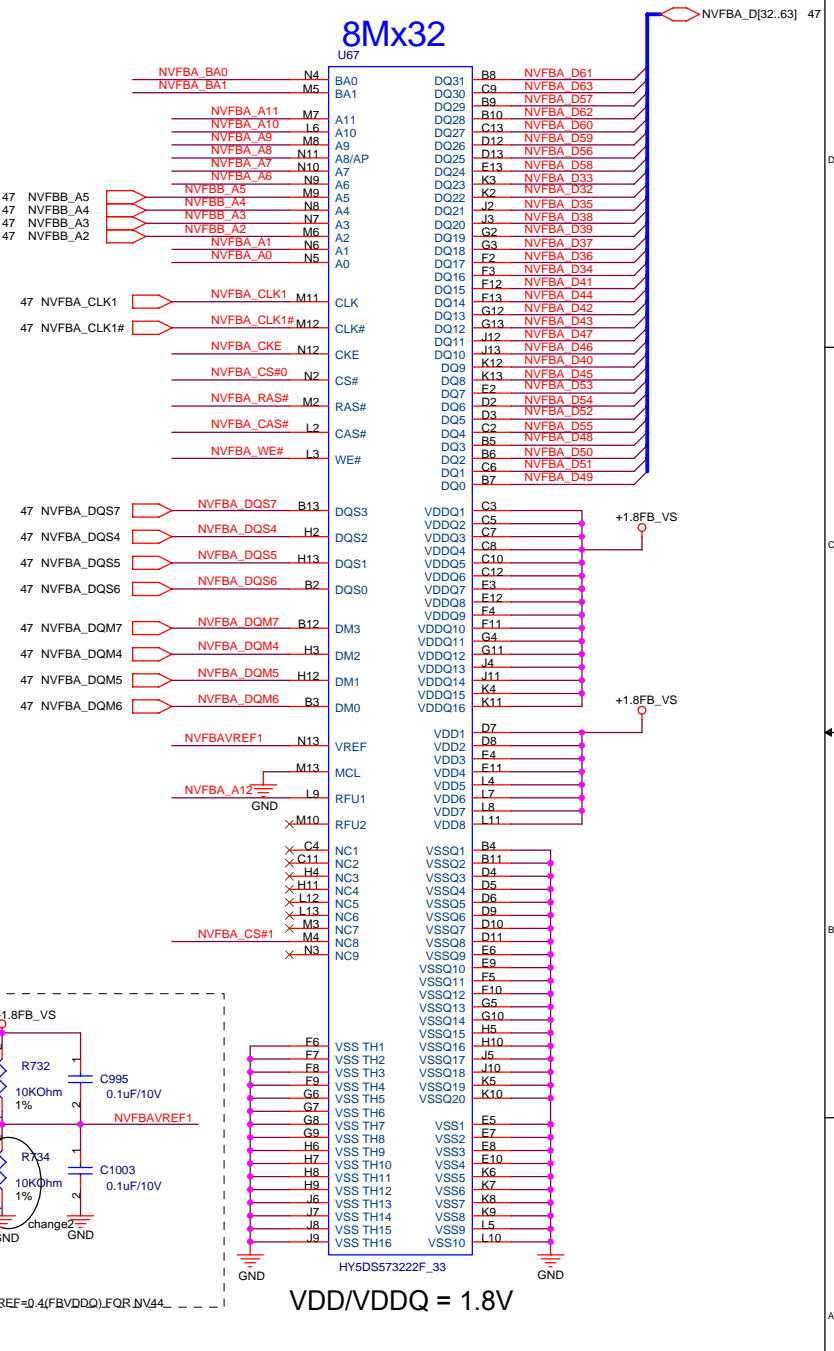
8Mx32

U66



8Mx32

U67



Title : NV43M VRAM(A)

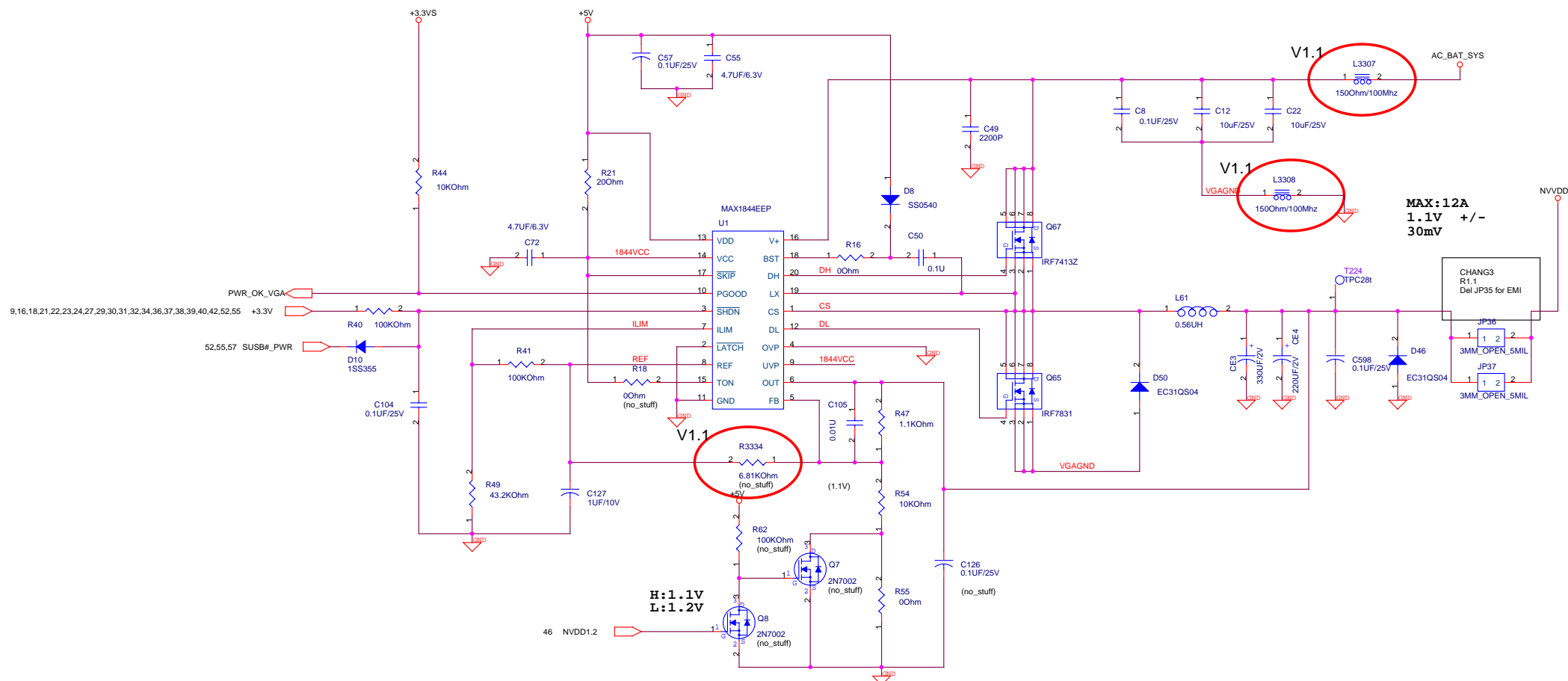
ASUSTek COMPUTER INC.

Engineer: Allen_CD_Wu

Size
CustomProject Name
A6KMRev
0.1

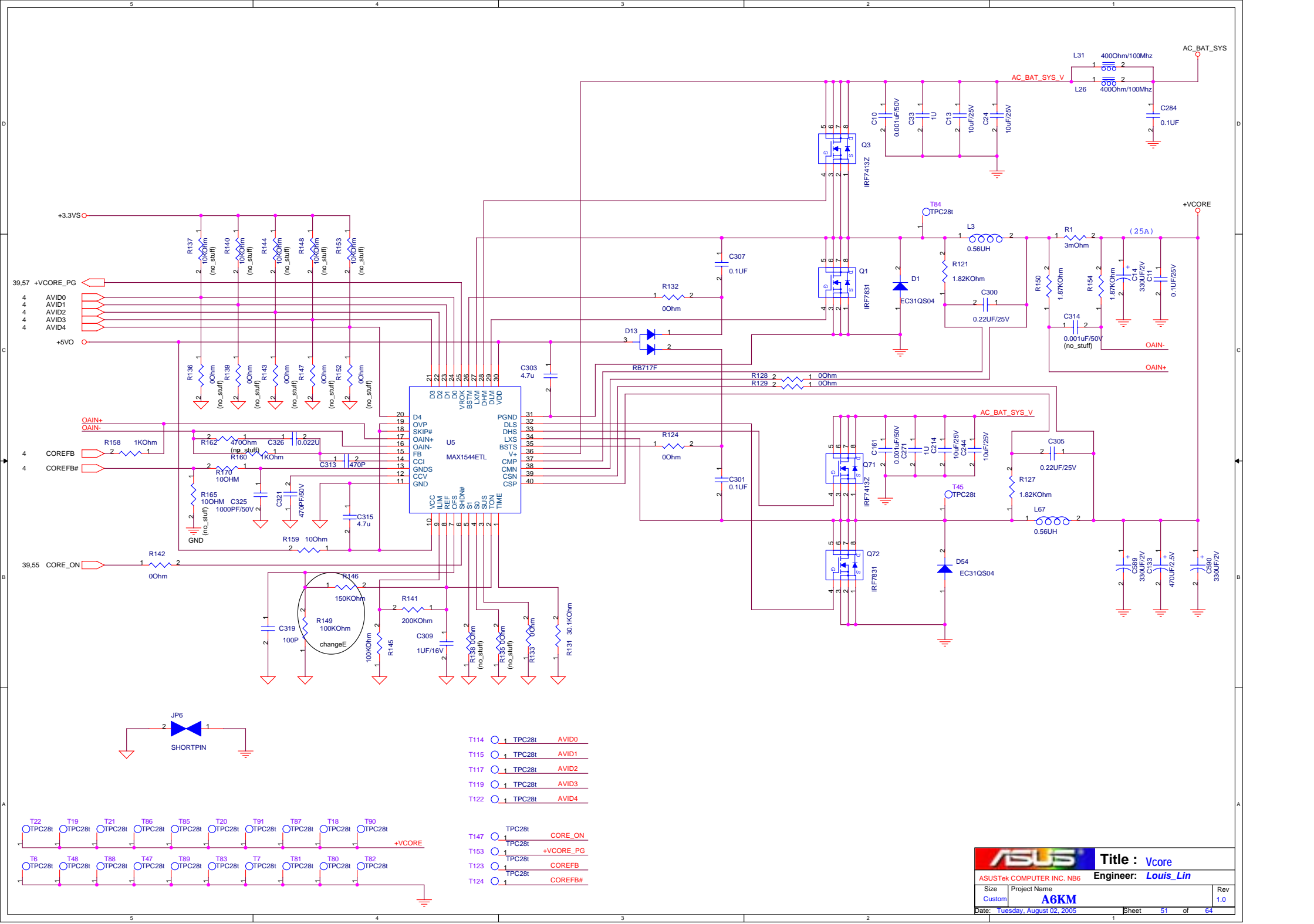
Date: Tuesday, August 02, 2005

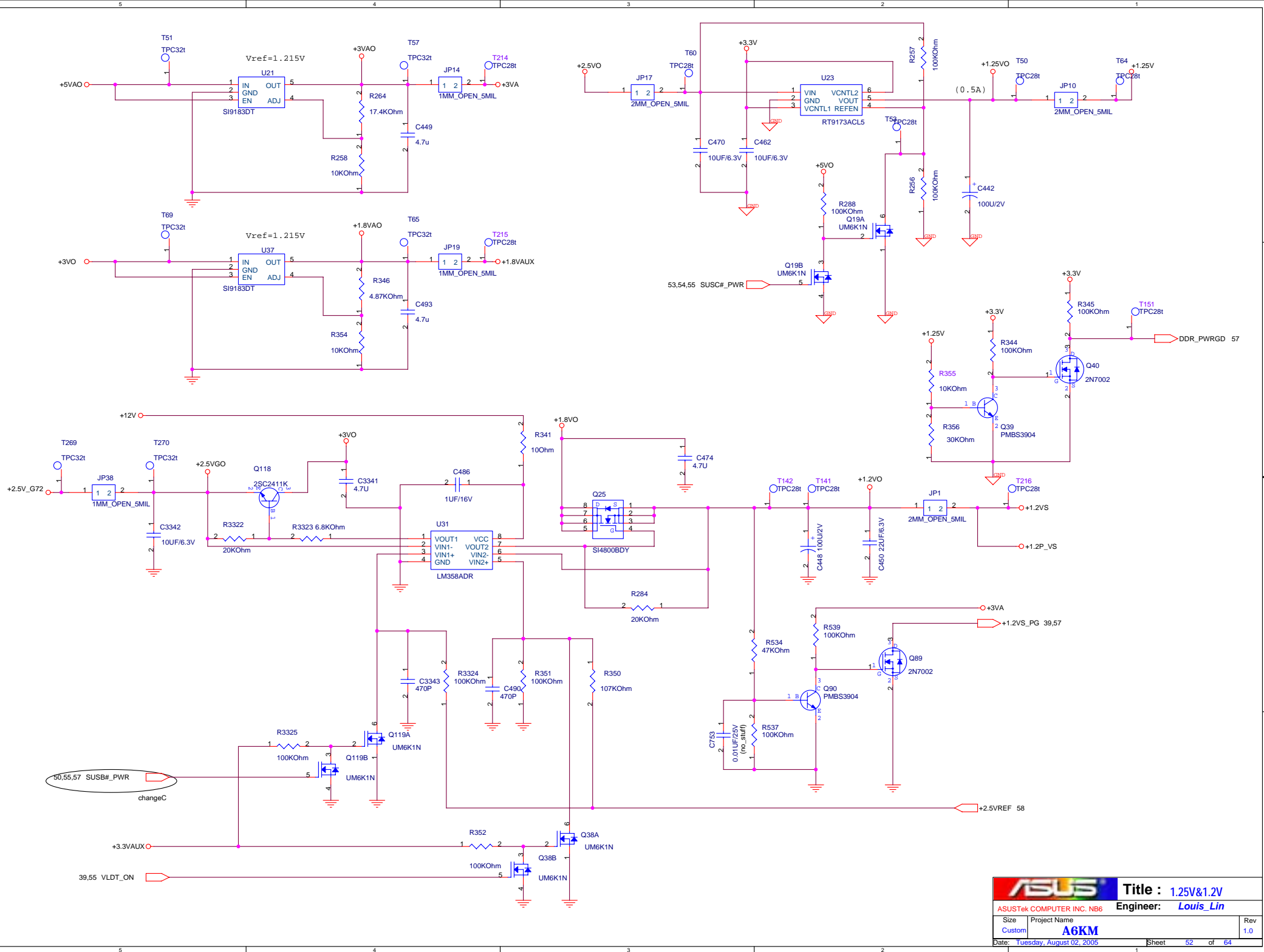
Sheet 49 of 64

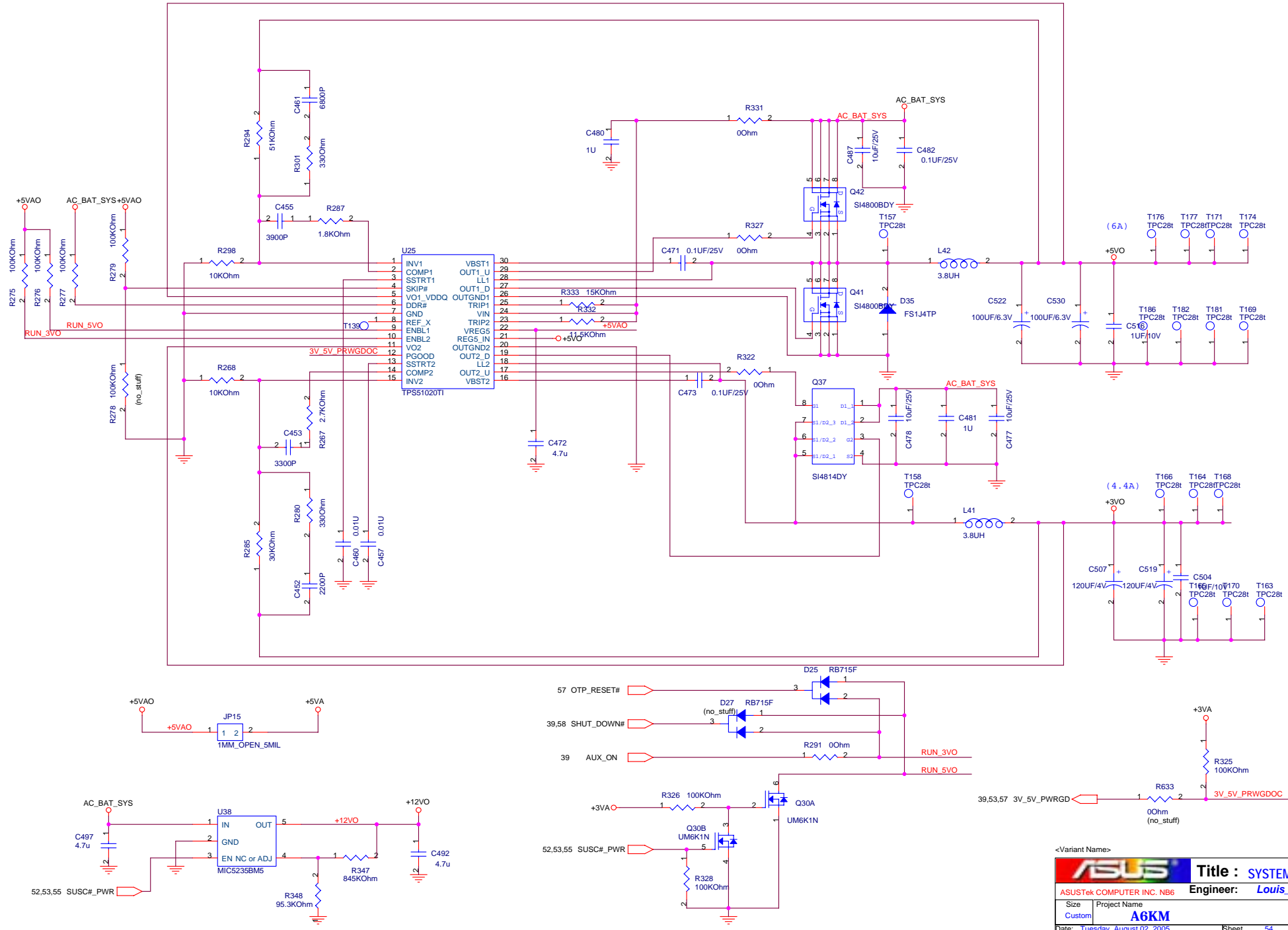


<Variant Name>

		Title : VGACORE	
ASUSTek COMPUTER INC. NB6		Engineer: Louis_Lin	
Size	Project Name	A6KM	1.0
Custom			
Date: Tuesday, August 02, 2005		Sheet	50 of 64

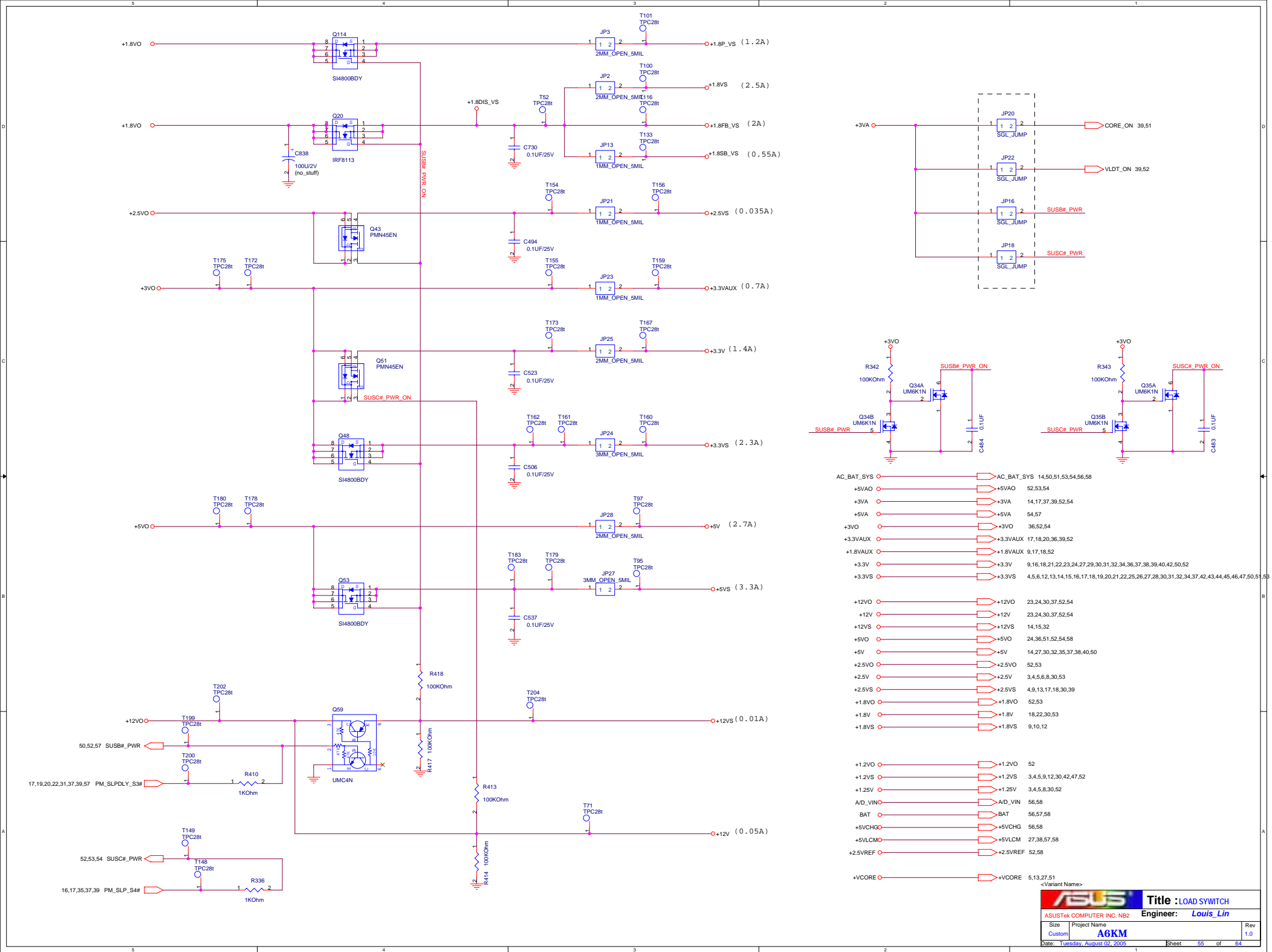






<Variant Name>

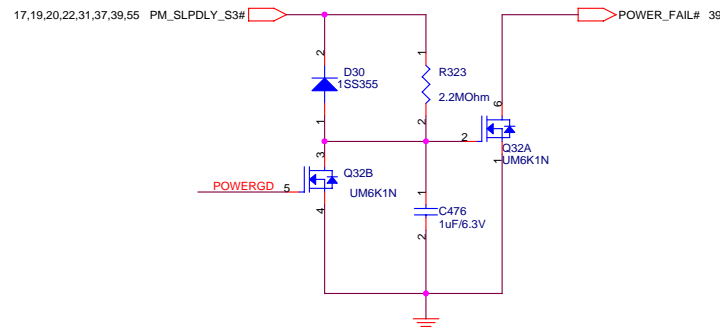
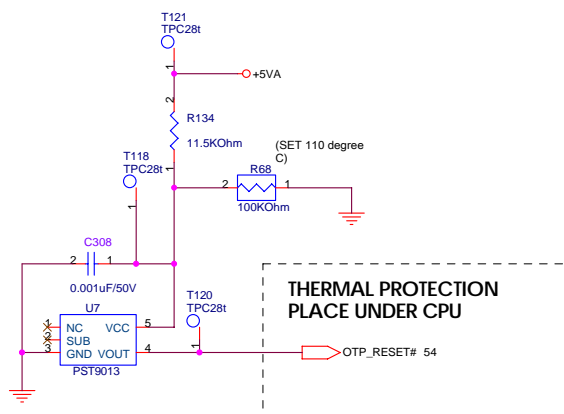
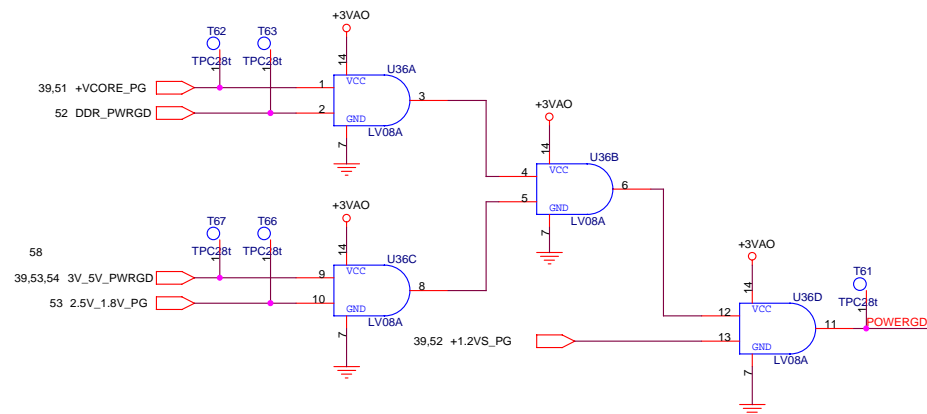
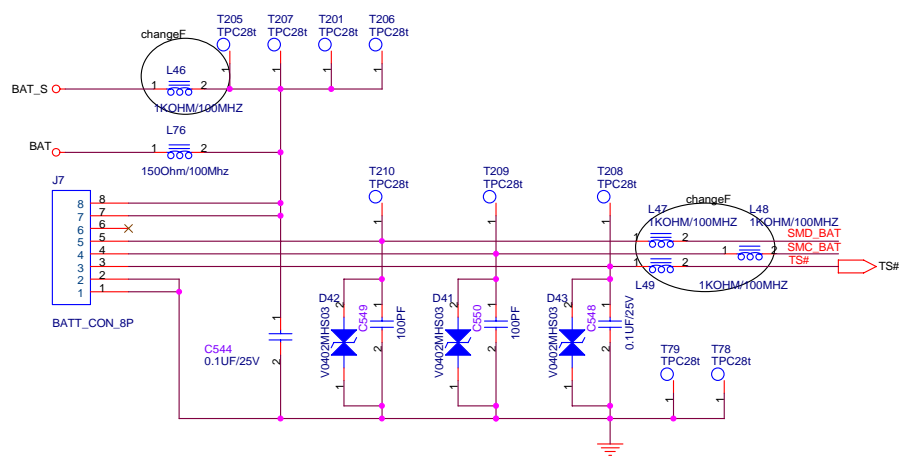
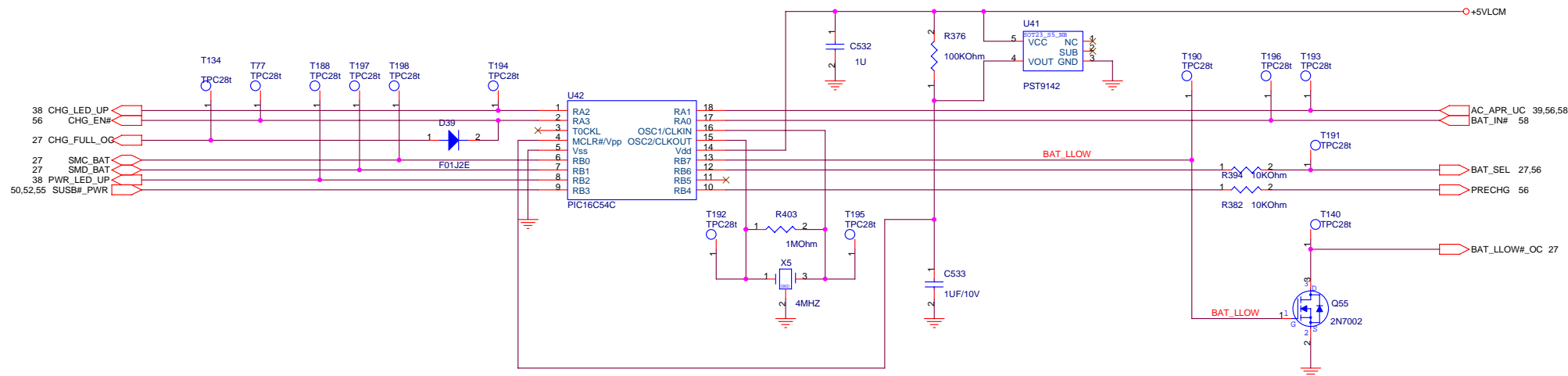
ASUS		Title : SYSTEM
ASUSTek COMPUTER INC. NB6		Engineer: Louis Lin
Size	Project Name	Rev
Custom	A6KM	1.0
Date: Tuesday, August 02, 2005		Sheet 54 of 64



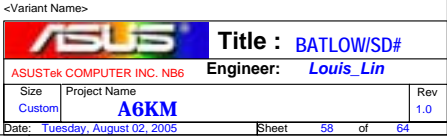
$$R(h_i) = (5/3.062 - 1) * 100K = 63.3K$$

$$R(h_i) = (5/1.145 - 1) * 10K = 336.68K$$

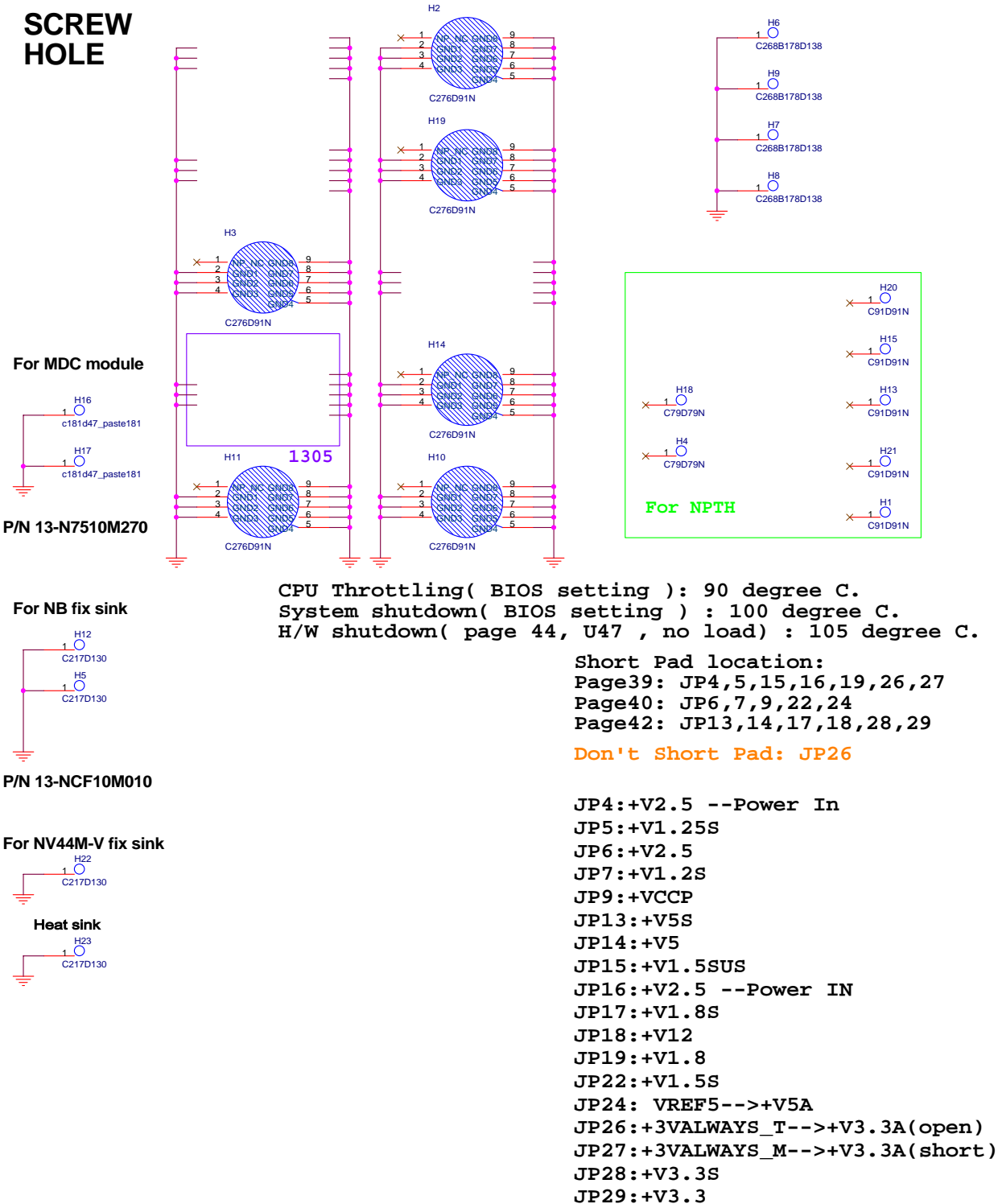




<Variant Name>



SCREW HOLE



PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 20 mils

37.5 OHM WIDTH

TOP/BOT 12 mils

42 OHM WIDTH

TOP/BOT 10 mils

55 OHM WIDTH

TOP/BOT 5 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 9 mils/ 5 mils

90 OHM WIDTH/SPACE

TOP/BOT 7 mils/ 10 mils

100 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

PCI_GNT#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

IDSEL

CB&1394 PCI_AD21

MINIPCI PCI_AD20

LAN PCI_AD16

PCI_INT#

CB&1394 PCI_INTB/A/D#

MINIPCI PCI_INTC/D#

LAN PCI_INTC#

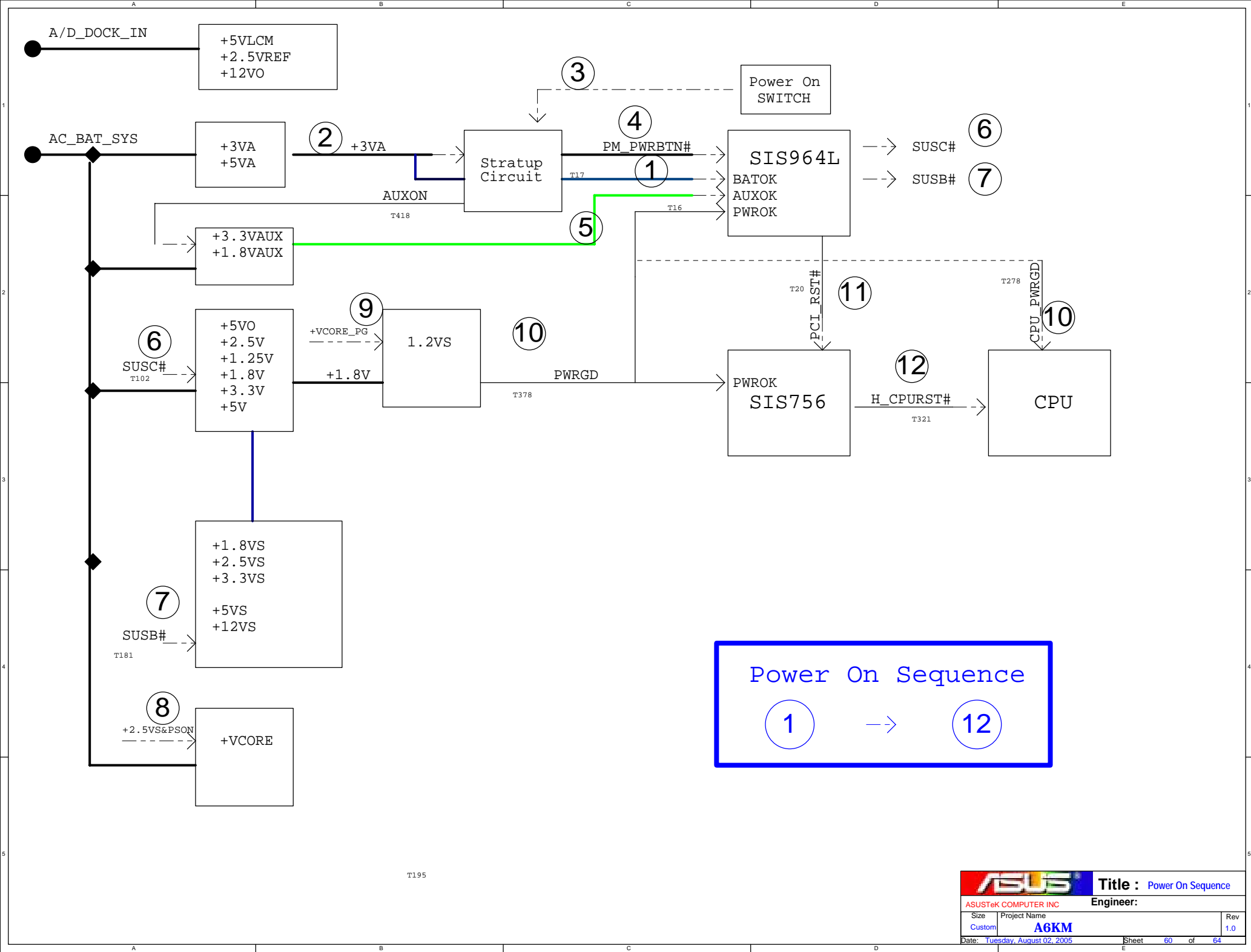
POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

ASUS		Title : SCREW HOLE
ASUSTek COMPUTER INC. NB6		Engineer:
Size	Project Name	Rev
Custom	A6KM	1.0
Date: Tuesday, August 02, 2005	Sheet 59 of 64	



PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN_RTL8100CL	AD22	2	D
CARD READER	AD21	0	B
CARDBUS	AD21	0	C
1394	AD21	0	D
MINIPCI (802.11a/b/g)	AD20	1	C,D

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor (SA56004)	0101110x (5C)
PIC	1001001x (92)

SIS964L GPIO	SIGNAL NAME	I/O	Volt
GPIO 0		P-U	+3.3VS
GPIO 1	NV_THERM#	INPUT	+3.3VS
GPIO 2	THRM_ALERT#	INPUT	+3.3VS
GPIO 3	EXTSMI#	INPUT	+3.3VS
GPIO 4	PM_CLKRUN#	OUTPUT	+3.3VS
GPIO 5		P-U	+3.3VS
GPIO 6	CPUFAN_SPD_A	INPUT	+3.3VS
GPIO 7	BACK_OFF#	OUTPUT	+3.3VAUX
GPIO 8	PM_RI#	INPUT	+3.3VAUX
GPIO 9	KBDSCI_3A	INPUT	+3.3VAUX
GPIO 10	LID_963#_3A	INPUT	+3.3VAUX
GPIO 11	PM_STPPCI#	OUTPUT	+3.3VAUX
GPIO 12	PM_STPCPU#	OUTPUT	+3.3VAUX
GPIO 13	SIO_SMI#	INPUT	+3.3VAUX
GPIO 14	S3AUXSW#	OUTPUT	+3.3VAUX
GPIO 15	BT_ON	P-L	+3.3VAUX
GPIO 16	802_LED_EN#	OUTPUT	+3.3VAUX
GPIO 17	WLAN_ON#	OUTPUT	+3.3VAUX
GPIO 18	CB_SD#	OUTPUT	+3.3VAUX
GPIO 19	SM_CLK	OUTPUT	+3.3VS
GPIO 20	SM_DATA	I/O	+3.3VS
GPIO 21		NC	+3.3VAUX
GPIO 22		NC	+3.3VAUX
GPIO 23		P-L	+3.3VAUX
GPIO 24		P-U	+3.3VAUX

KBC GPIO	A6K	
P23	OP_SD#	
P22	BAT_LEARN	
P21	(KB_P21)	
P20	KBCRSM	
P42	(WATCHDOG)	
P43	CHG_FULL_OC	
P44	KB_CPURST	
P45	KB_GATEA20	
P46	KBCSCI	
P47	PM_CLKRUN#	
P50	KBC_BAT_LLOW#	
P51	KEYDETECT1	
P52	KEYDETECT2	
P53	CLR_DJ#	
P54	BAT_SEL	
P55	BAT1_IN#_OC	
P56	(FAN_DA1)	
P57	ADJ_BL	
P67	DJ_LED#	
P66	SWDJ_EN#	
P65	+VCORE	
P64	ACIN_OC	
P63	DISTP	
P62	MARATHON#	
P61	INTERNET#	
P60	EMAIL#	
P75	(KB_CLK)	
P74	(MS_CLK)	
P73	TPAD_CLK	
P72	(KB_DAT)	
P71	(MS_DAT)	
P70	TPAD_DAT	
P77	BAT_SMC	
P76	BAT_SMD	
P27	SCROLLLOCK#	
P26	NUM_LED#	
P25	CAP_LED#	
P24	SET_PLTRSTNS#	
P40	EXT_SMI	
P41	EMAIL_LED#	

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
	07-016202032	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-0931111041	10-0931111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407 *11-03B110623 for Power RD Request
	11-031210621	
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

REVISION LIST

POWER INTERFACE

SIGNALS TYPE POWER

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.55V	27.3A
+1.25V	1.25V	0.725A
NVVDD	1.1/1.2V	8.62A
+2.5V	2.5V	5.55A
+1.8VAUX	1.8V	50mA
+1.2P_VS	1.2V	1.875A
+1.2VS	1.2V	635mA
+1.8VS	1.8V	2.521A
+1.8V	1.8V	415 mA
+1.8FB_VS	1.8V	2A
+2.5VS	2.5V	0.035A
+3.3V	3.3V	1.925A
+3.3VS	3.3V	2.955A
+5VS	5V	4.7A
+5V	5V	3.865A
+5VA	5V	0.05A
+12V	12V	0.05A
+12VS	12V	0.01A
+3.3VAUX	3.3V	0.417A
+3VA	3.3V	0.02A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 22 mils
IN1/IN3 16 mils

37.5 OHM WIDTH

TOP/BOT 13.5 mils
IN1/IN3 10 mils

42 OHM WIDTH

TOP/BOT 11 mils
IN1/IN3 8.5 mils

55 OHM WIDTH

TOP/BOT 6 mils
IN1/IN3 5 mils

75 OHM WIDTH

TOP/BOT 2.5 mils
IN1/IN3 2 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 8 mils/ 4 mils
IN1/IN3 8 mils/ 3.5 mils

90 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 5 mils
IN1/IN3 5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 4 mils/ 6 mils
IN1/IN3 4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

IDSEL

CB&1394 PCI_AD21

MINIPCI PCI_AD20

LAN PCI_AD22

PCIe Device

PEG

NVIDIA NV44M

PCIe Giga NIC

N/A

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP

L2 VCC

L3 IN1

L4 IN2

L5 GND

L6 BOT

SIGNAL IN: AVIDT[0:4] PAGE 49
CORE_ON
COREFB
COREFB#

OUT: +VCORE_PG

POWER IN: AC_BAT_SYS
+5V0
+3.3VS

OUT: +VCORE

SIGNAL IN: VLDT_ON PAGE 50
+2.5VREF
SUSC#_PWR
DDR_PWRGD
+1.2VS_PG

POWER IN: +5VAO
+12V
+3VO
+3VAUX
+2.5V0
+1.25V
+3.3V
+5V0
+1.8V0

OUT: +3VA
+1.8VAUX
+1.25V
+1.2VS
+1.2P_VS

SIGNAL IN: SUSC#_PWR PAGE 51
OUT: 2.5V_1.8V_PG

POWER IN: AC_BAT_SYS
+3.3VS
+5VAO
OUT: +2.5V
+1.8V

SIGNAL IN: SUSC#_PWR PAGE 52
OTP_RESET#
SHUT_DOWN#
AUX_ON

OUT: 3V_5V_PWRGD

POWER IN: AC_BAT_SYS
+3VA
+3.3VS
+VCC_GMCH_CORE
+5VAO

OUT: +5VA
+5V0
+12V0
+3VQ

Reversion from A6KM R1.0
change1: P.9 Del R30, R431 Change R71->125 for SPEC
P.10 Del R101
P.13 Del R218, R219, R2400~R2405, R2407, R2409, R2411
P.14 Del D45, RN87 Mount R624 Change C566->1uF Add R3330, R3331, Q121
P.20 Mount C3318
P.22 Del R363
P.23 Del R552 Mount C767-> 33pF
P.24 Del R569, R574, R591, R592
P.29 Change RN78, RN77, RN76->
P.33 Change R476, R478-> SHORTPIN JP39, JP40
P.35 Change L8, L9, L10, L11->
P.37 Del R2418 D16->D77, D78
P.43 Unmount RN42
P.46 Add RN91, R3332, R3333

P.9 Del R31, R433
P.33 Del R477
P.46 Change R3332->20MOhm
P.14 Add C3345, R3334
P.14 Del C3345, R3334
P.14 Add D45, RN87 Del R3330, R3331, Q121 Add L3307 for EMI.

CHANG2 P.56 Change L75 symbol for factory.
0728-05 P.50 Add L3308 for EMI.
P.43 Add R3335~R3342 for G72 insurance.
P.47 Del T247 for EMI layout change

CHANG3 P.50 Del JP35 for EMI layout change
0801-05 P.43 Del R3335~R3342.
P.47 Add T247 for VGA debug

CHANG3 P.59 H16, H17, H12, H5, H22, H23 -> SMD
0801-05 P.8 CHANGE RN62~74-> 10-312470004030
P.9 R71->124 Ohm
P.23 C767-> 33pF
P.29 RN76~RN78-> 10-064805600
P.35 L8~L11-> 09-013120102
P.19 R206-> 10-003401000 R207->10-003401500
P.20 U4 Giga LAN description -> 02-611102003
P.16 R237, R240 ->10-004405626
P.46 X10->07-010222706
P.14 L91, L92->09-013120006
P.45 R697->10-003416908
P.28 R518->10-004401030
P.46 R3320, R3321, R708, R709 and R3327->10-004401030
P.43 R666~R669, R656, R657, R660, R661->10-004401030
P.49 C988, C994, C1002, C1010->11-032147550
P.15 R423, R424->10-003402200
P.28 U39->12-043000323
P.19 UNMOUNT C377~384, C387

CHANG4 P.38 Add R3335~R3337 for EMI
0802-05 P.5 Add C3345~C3346 for EMI