

Compal Confidential

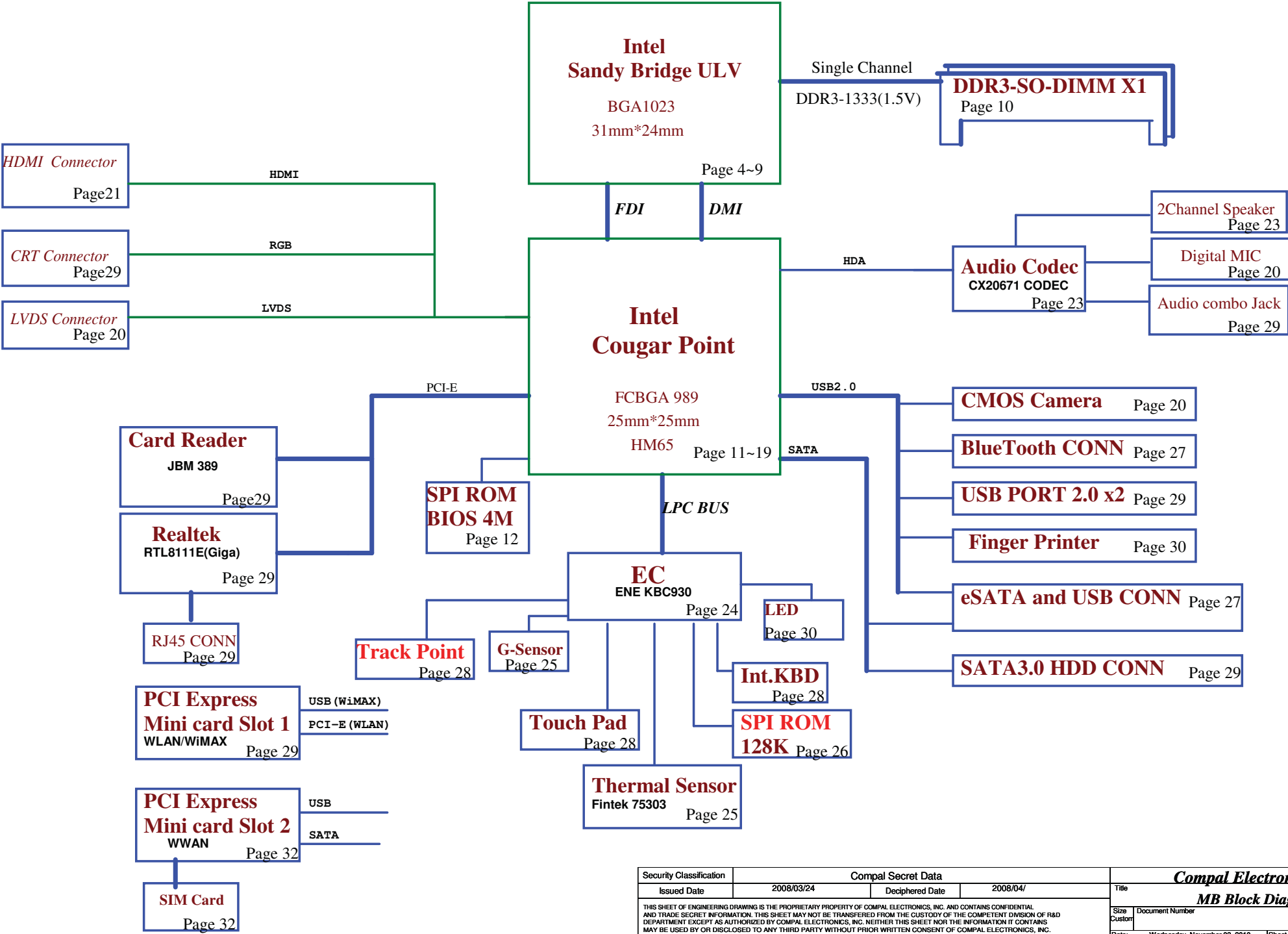
LA7041- Edge Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

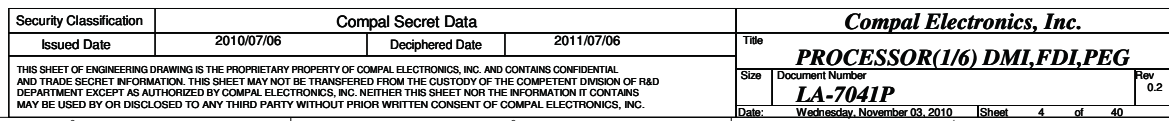
2010-10-05

REV: 0.2

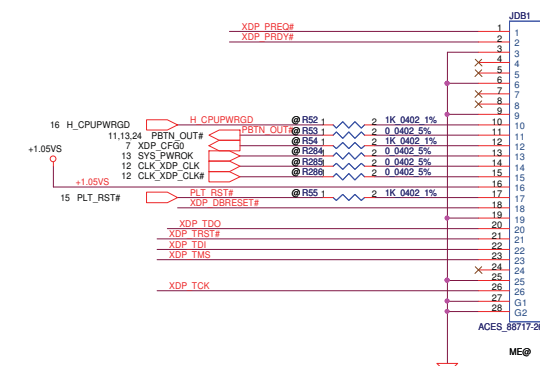
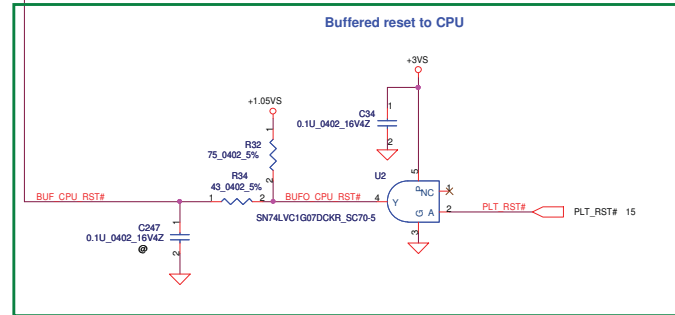
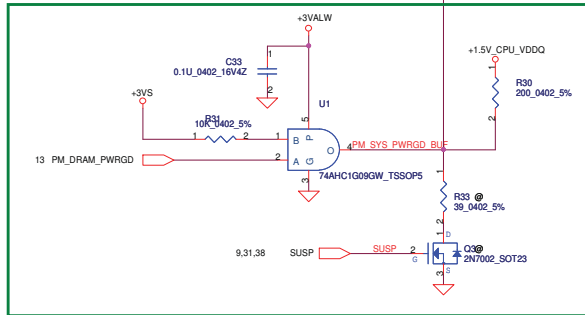
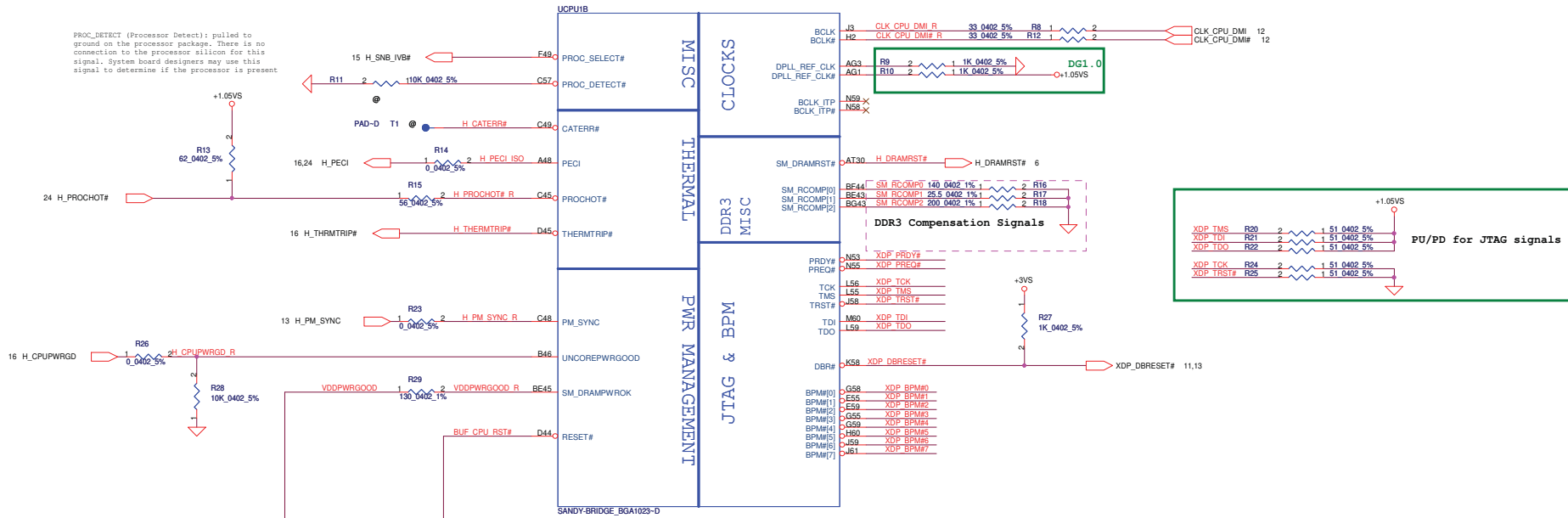
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				Size	Document Number	Rev
				Custom	<Doc>	0.2
Date: Wednesday, November 03, 2010				Sheet	1 of 40	

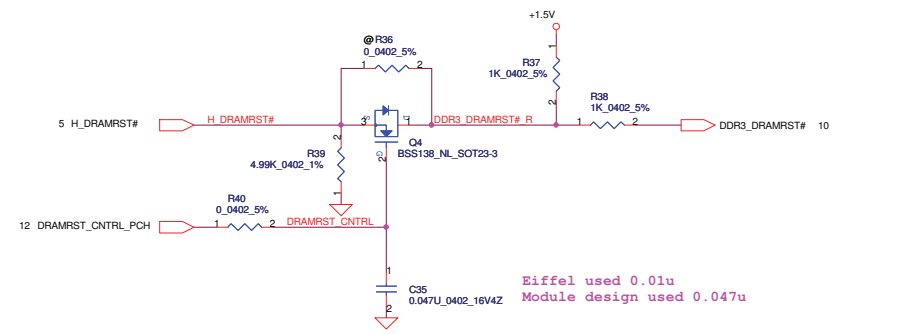
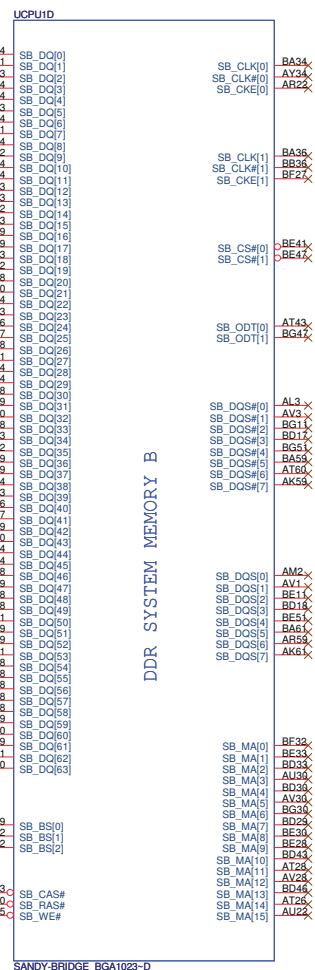


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				Date: Wednesday, November 03, 2010	Sheet 2 of 40
				MB Block Diagram	
				0.2	



PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present





Security Classification	Compal Secret Data			Compal Electronics, Inc. PROCESSOR(3/6) DDRIII		
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CFG Straps for Processor

Intel 12/28 recommend to add 1k pull down

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	CFG2
*1: (Default) Normal Operation; Lane # definition matches socket pin map definition	0: Lane Reversed

Display Port Presence Strap

CFG4	CFG4
*1 : Disabled; No Physical Display Port attached to Embedded Display Port	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps

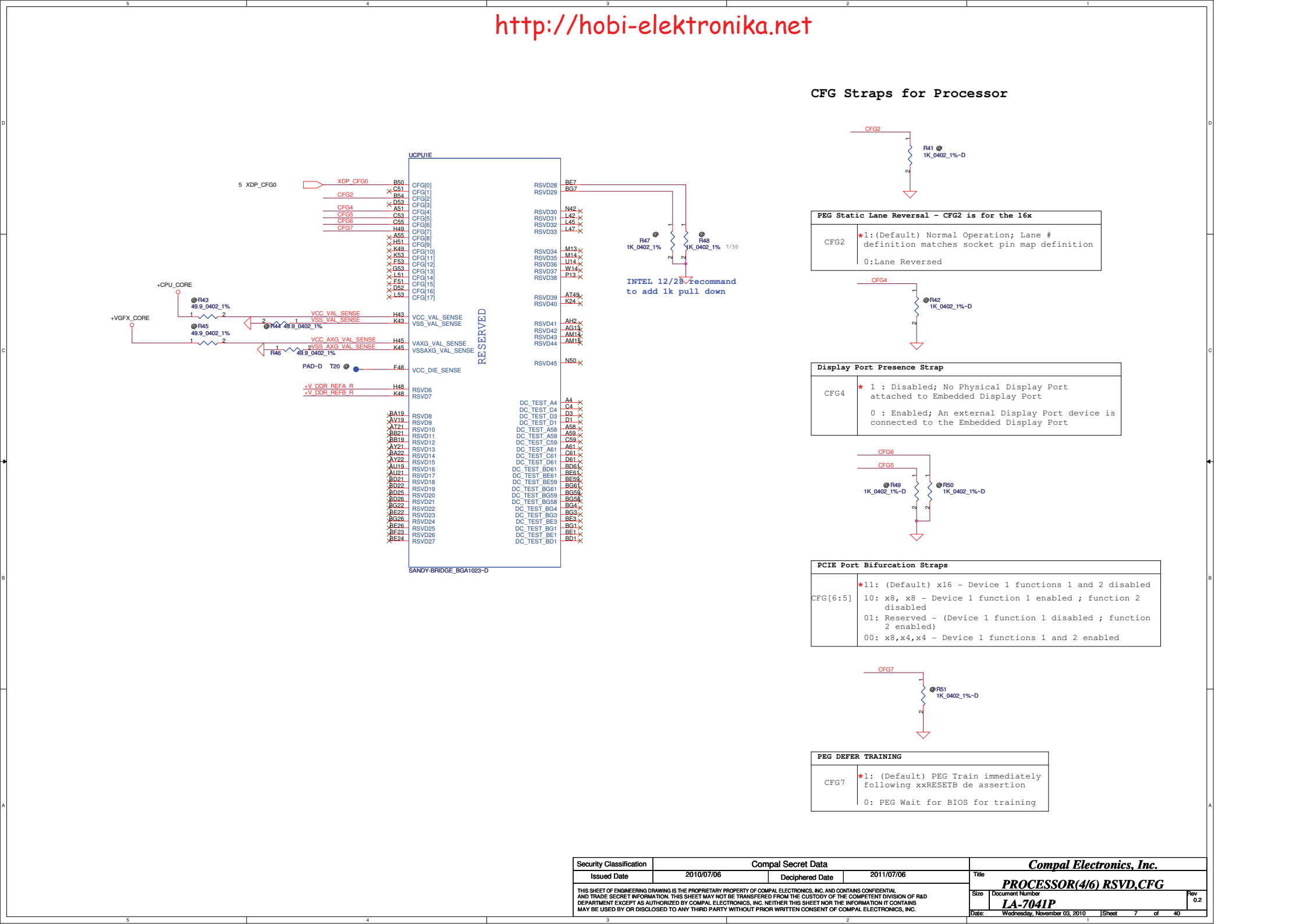
CFG[6:5]	CFG[6:5]
*11: (Default) x16 - Device 1 functions 1 and 2 disabled	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING

CFG7	CFG7
*1: (Default) PEG Train immediately following xxRESETB de assertion	0: PEG Wait for BIOS for training

SANDY BRIDGE BGA1023-D

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	PROCESSOR(4/6) RSVD,CFG	
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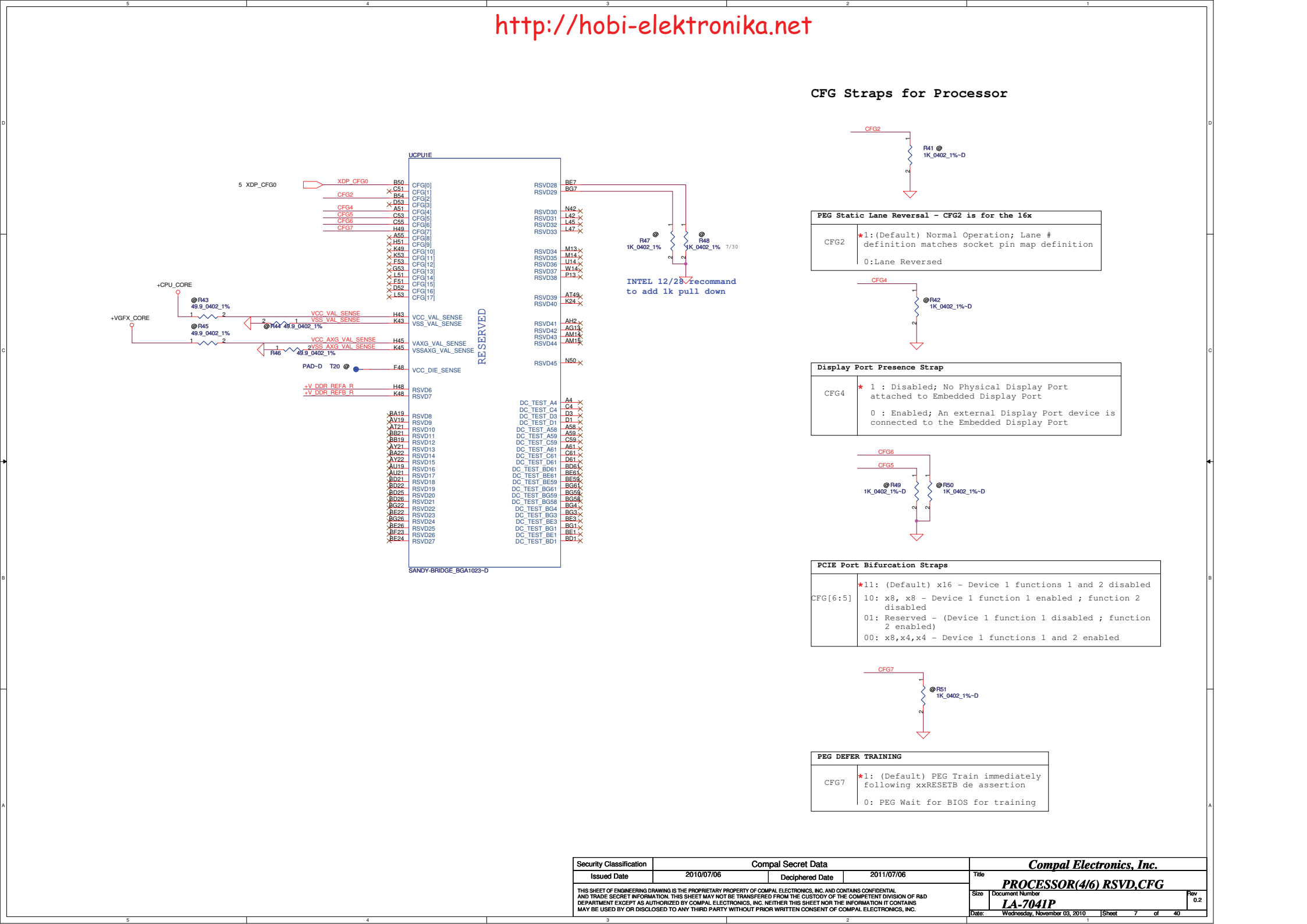
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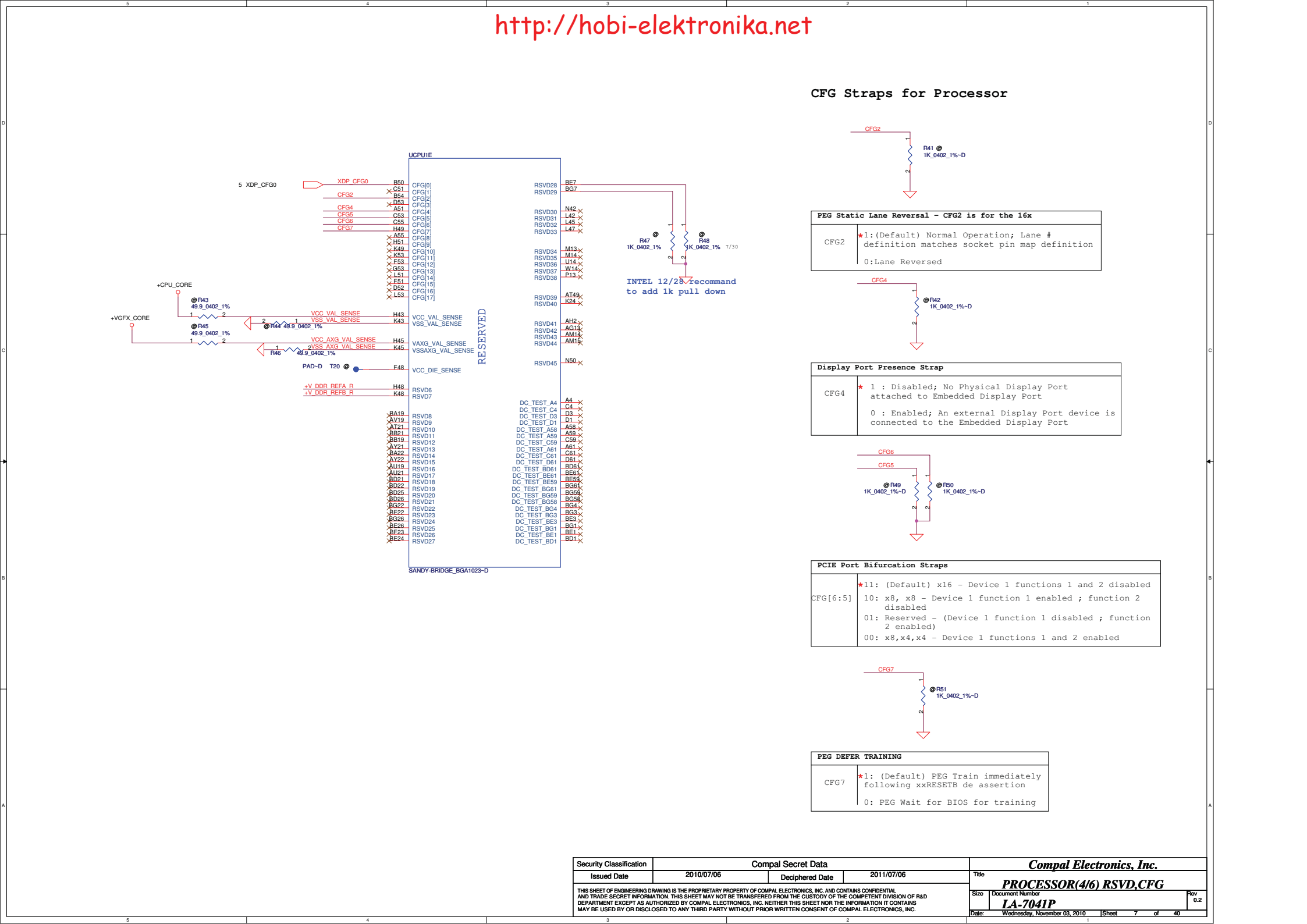
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CFG Straps for Processor

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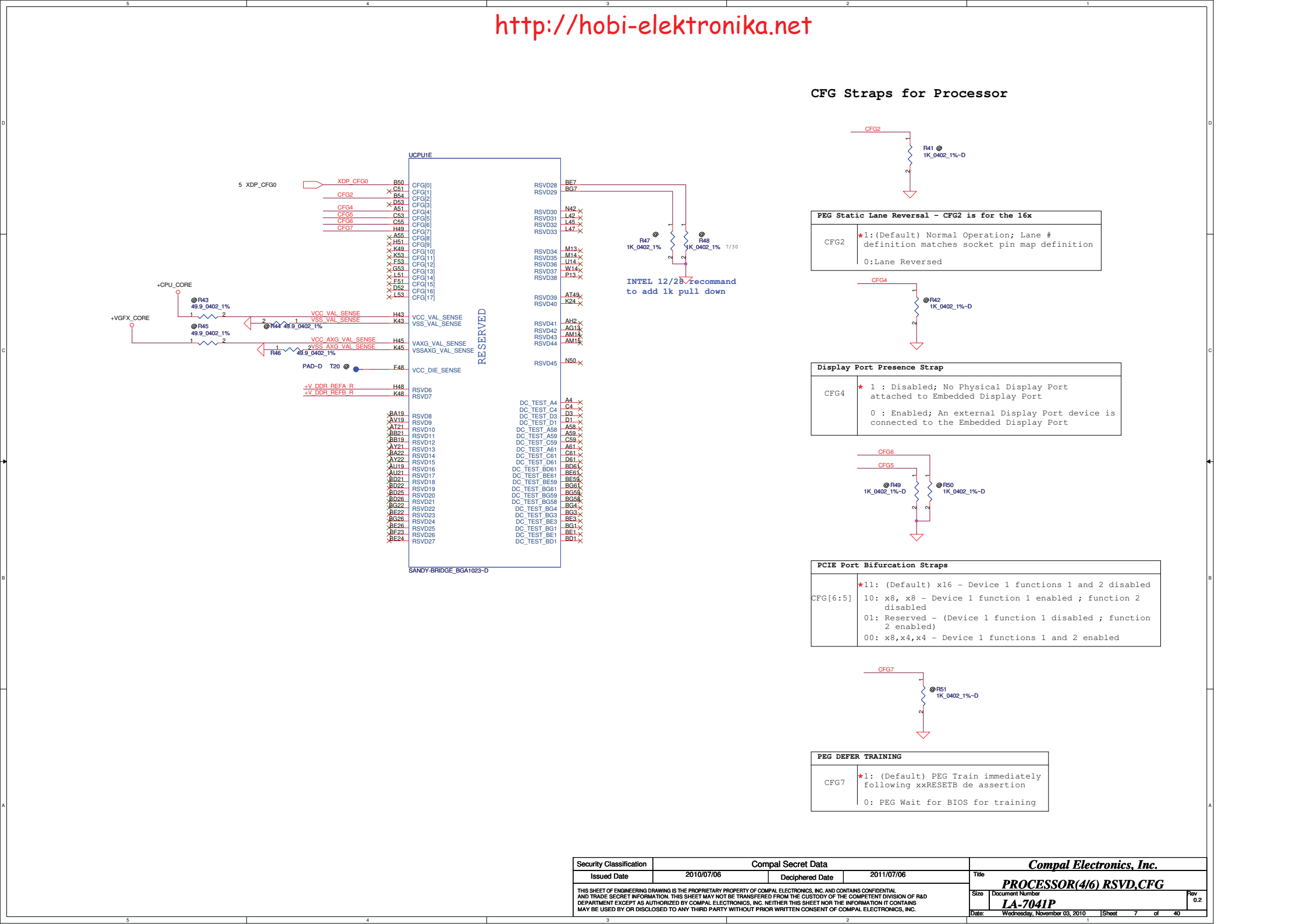
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CFG Straps for Processor

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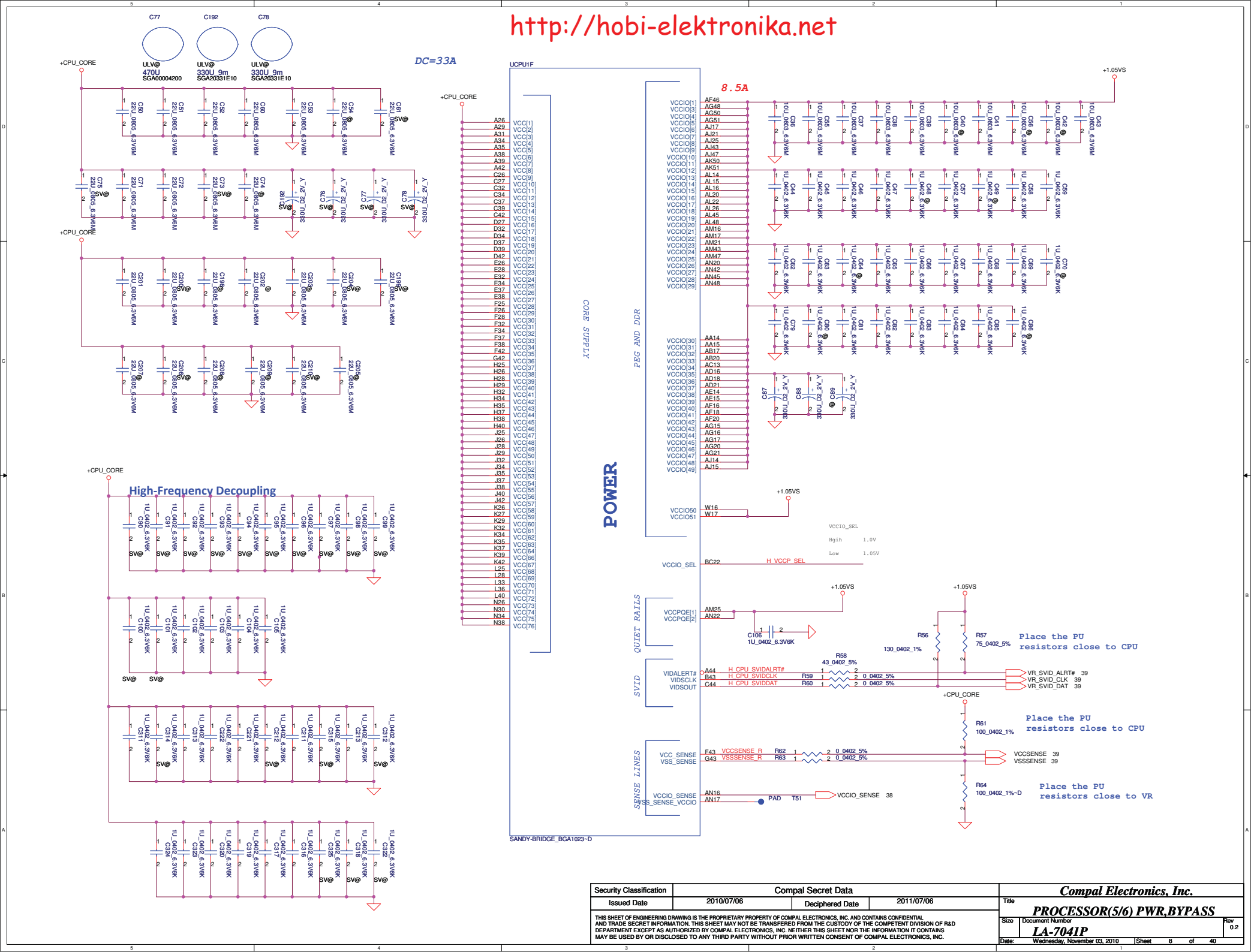
CFG7

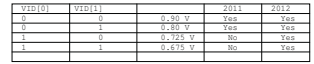
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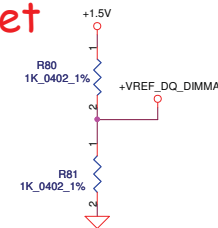
CFG4

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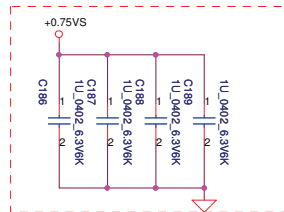
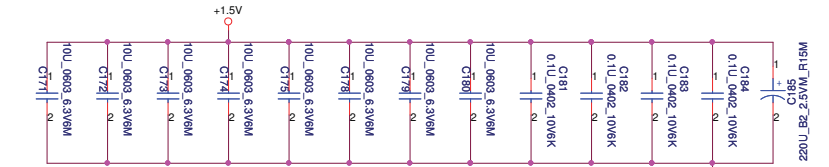
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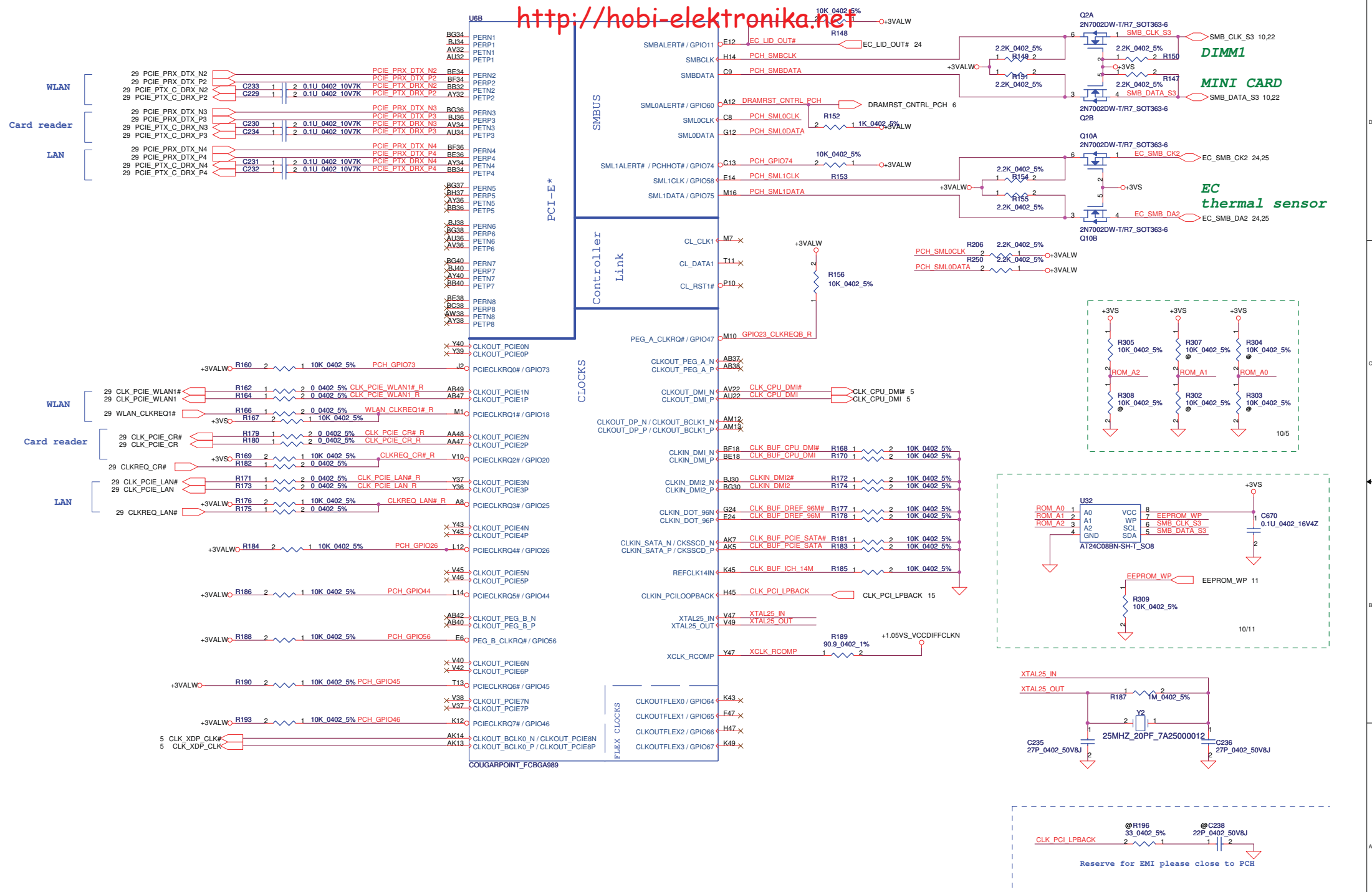


Layout Note:
Place near DIMM

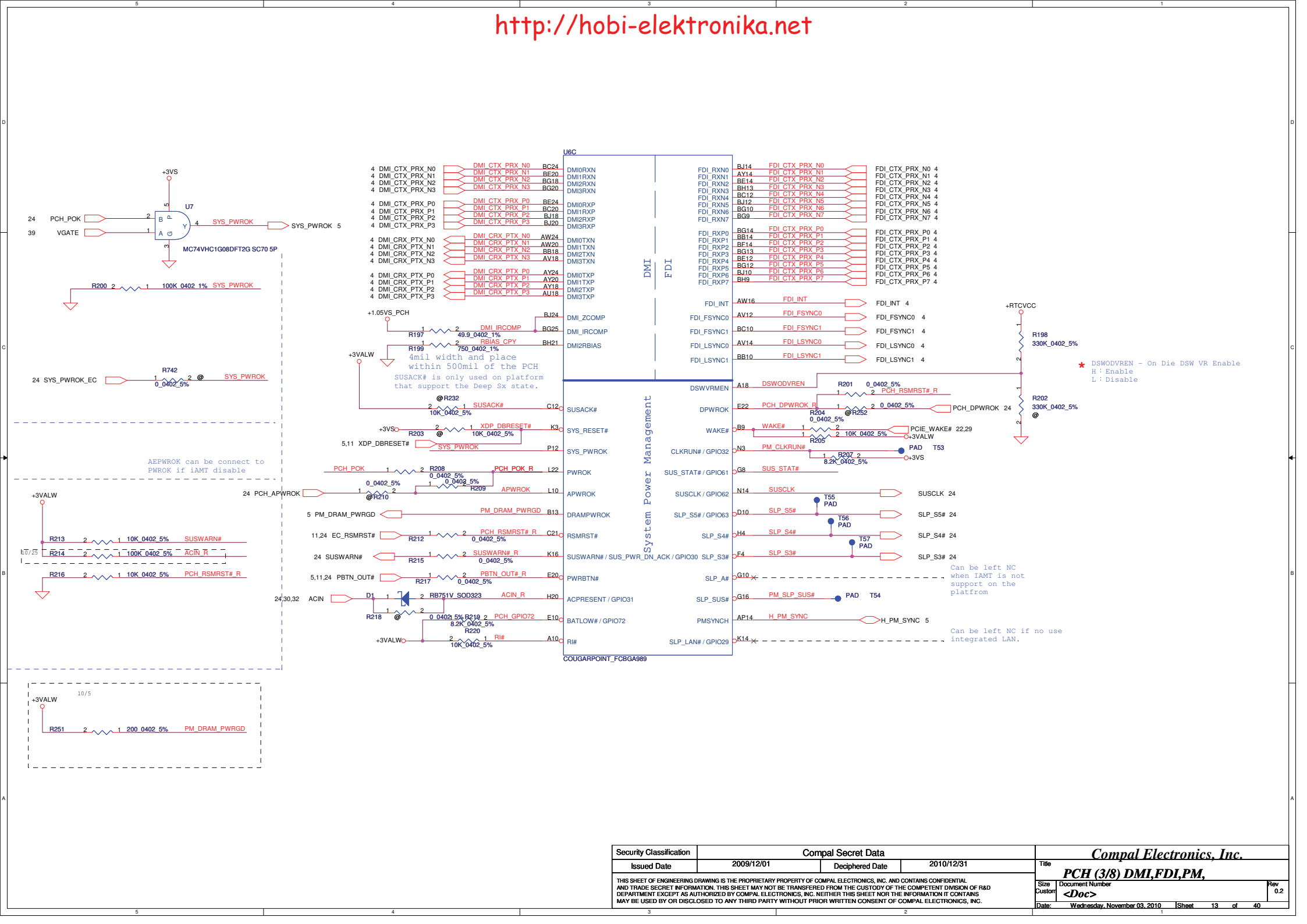


Compal Electronics, Inc.
DDRIII-SODIMM SLOT1

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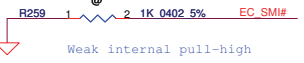
Security Classification		Compal Secret Data		Compal Electronics, Inc.									
Issued Date		2009/12/01		Deciphered Date		2010/12/31		Title		PCH (2/8) PCIE, SMBUS, CLK			
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								<Doc>				0.2	
								Date:		Wednesday, November 03, 2010		Sheet 12 of 40	



6/24 Change to @ follow module design and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable

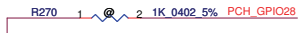
H ; Disable
L ; Enable



Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator

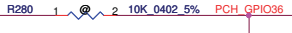
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



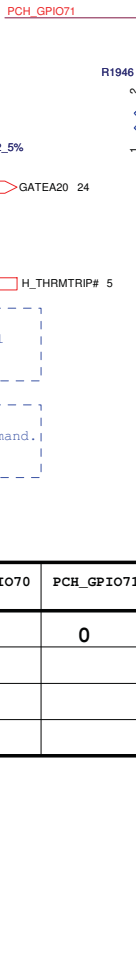
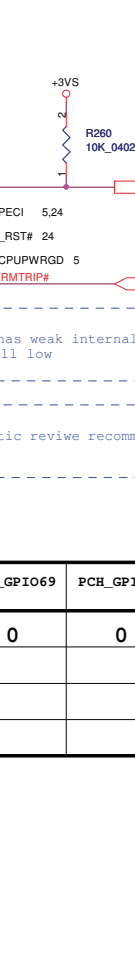
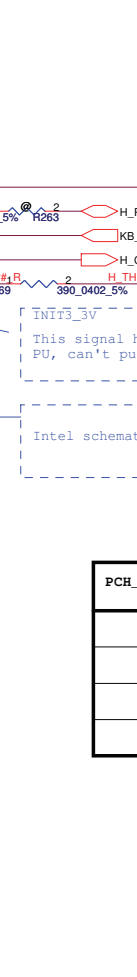
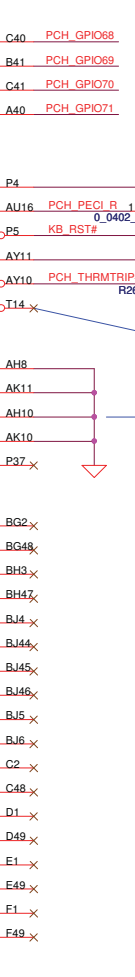
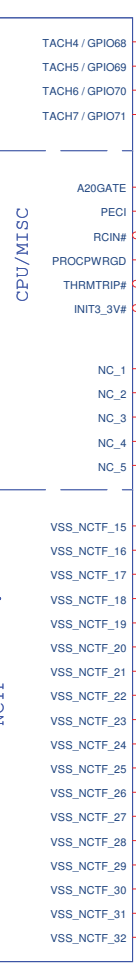
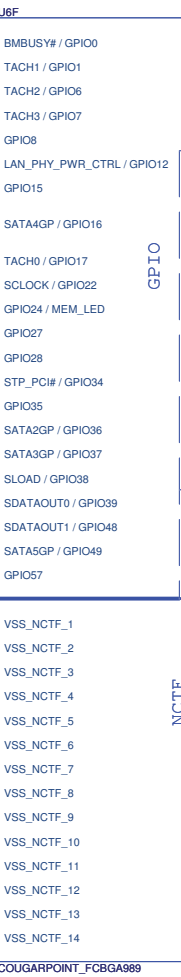
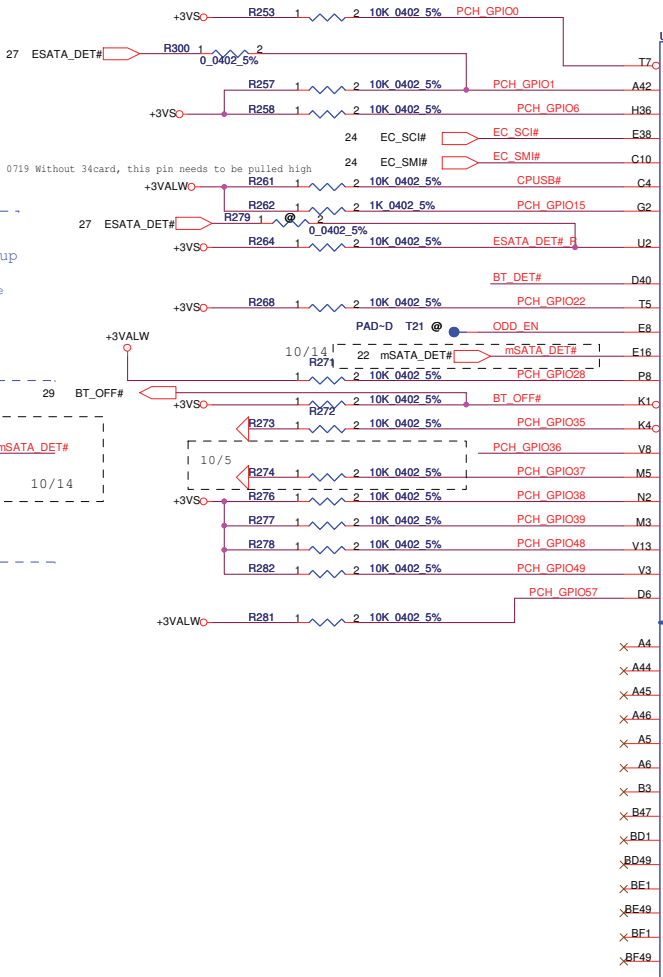
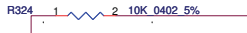
24 mSATA_PH



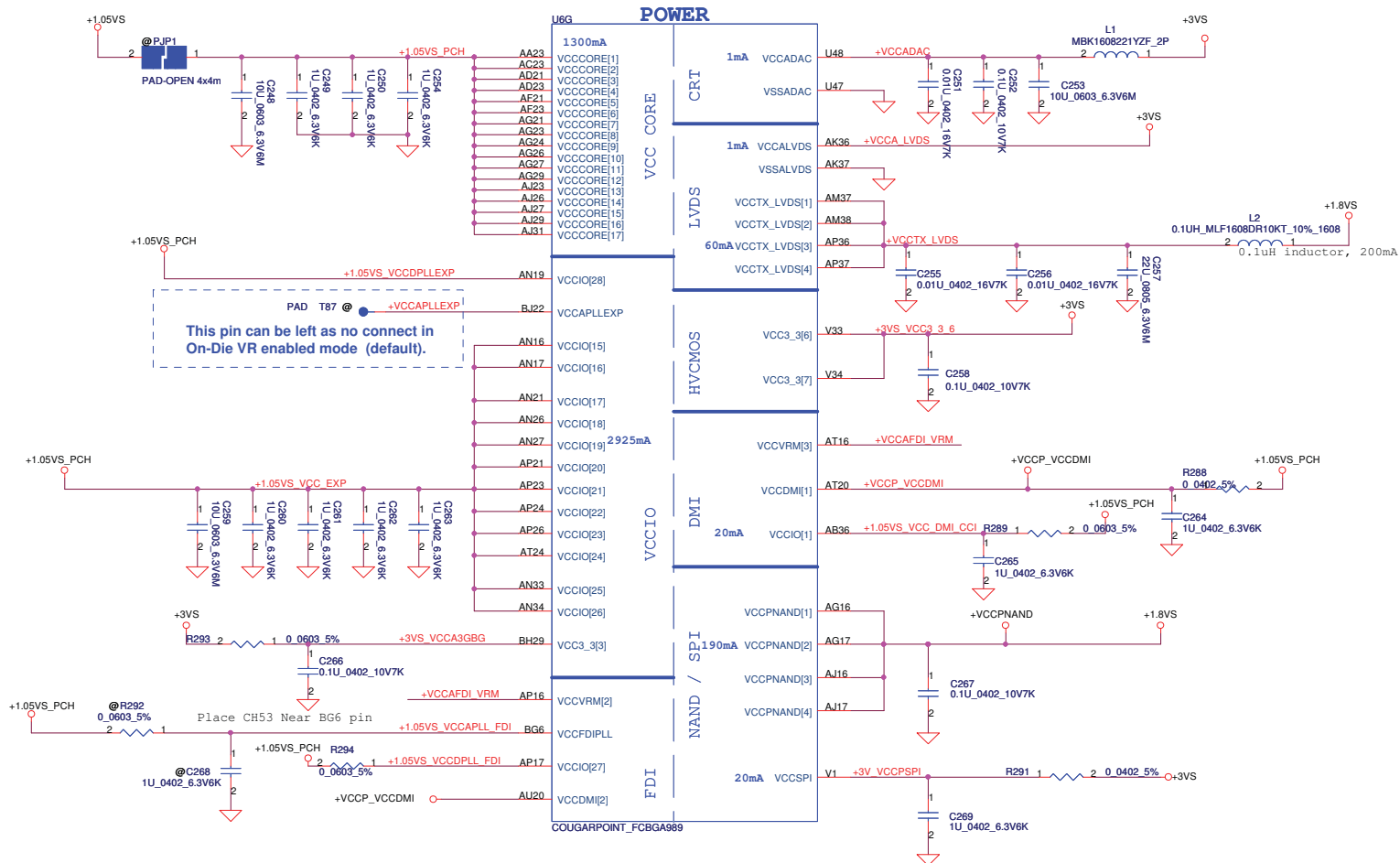
PCH_GPIO36



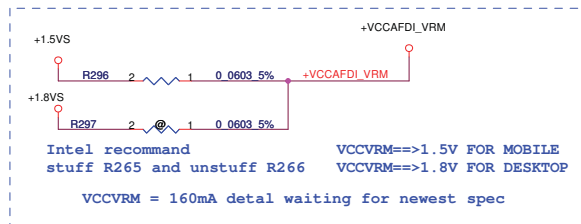
PCH_GPIO36



PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA

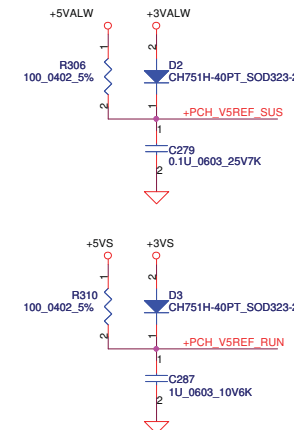


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

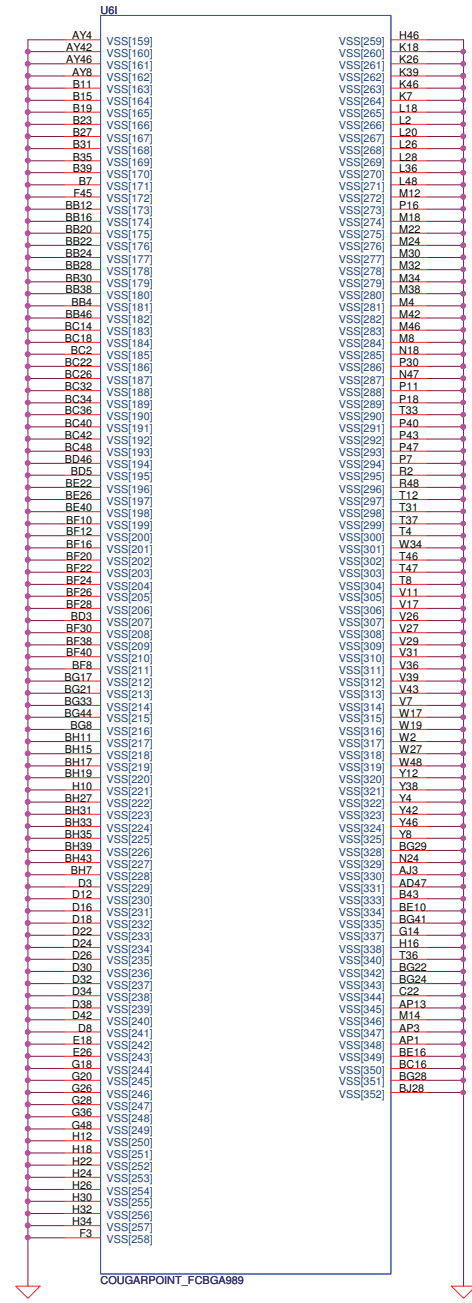
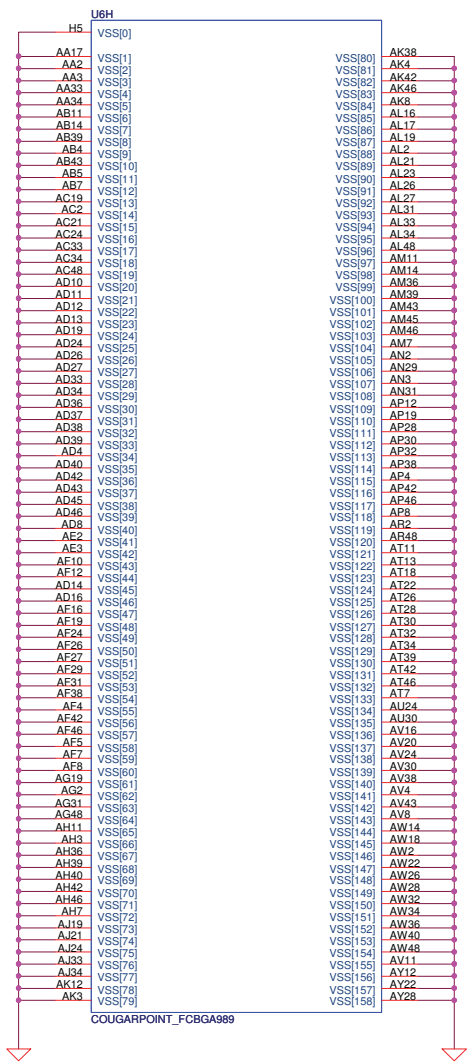


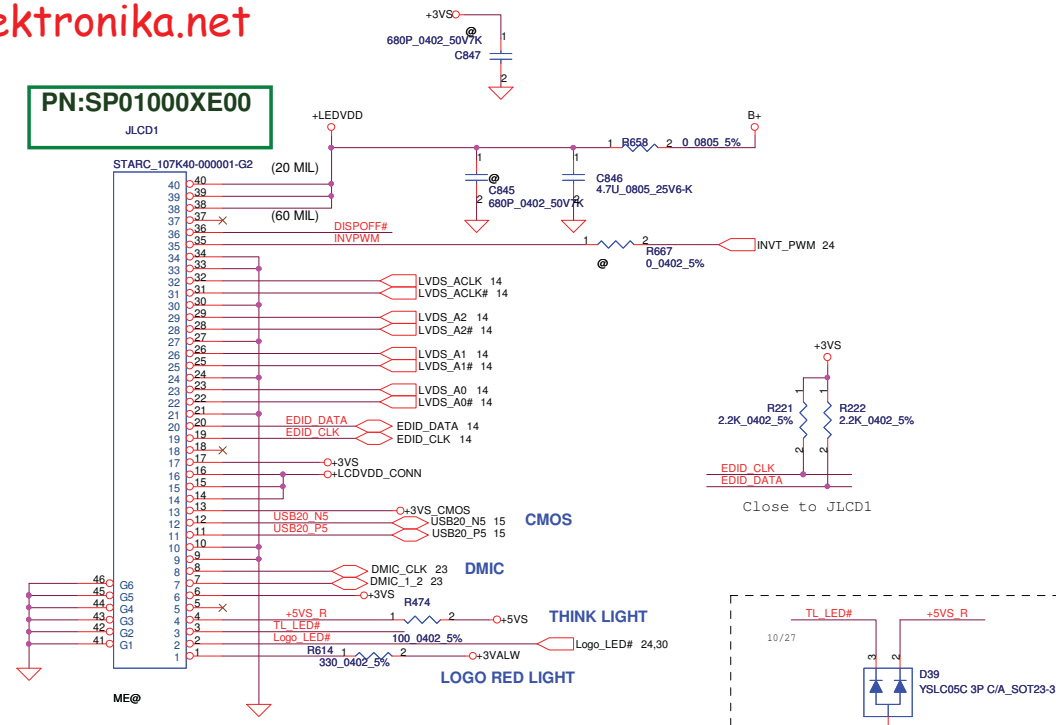
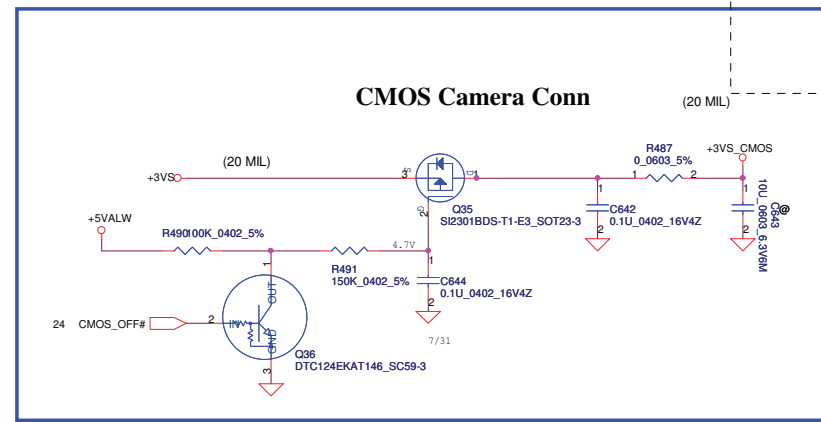
Intel recommend VCCVRM==>1.5V FOR MOBILE
stuff R265 and unstuff R266 VCCVRM==>1.8V FOR DESKTOP
VCCVRM = 160mA detail waiting for newest spec

```
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
```

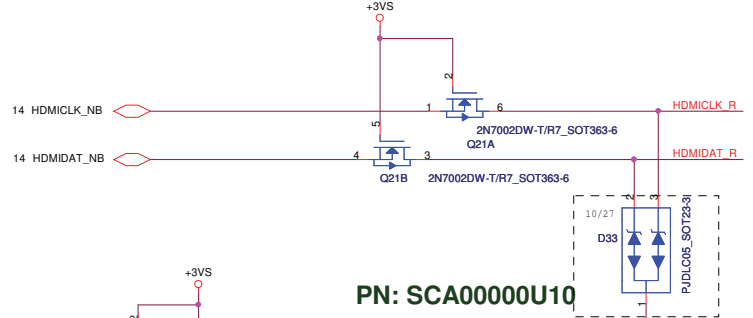
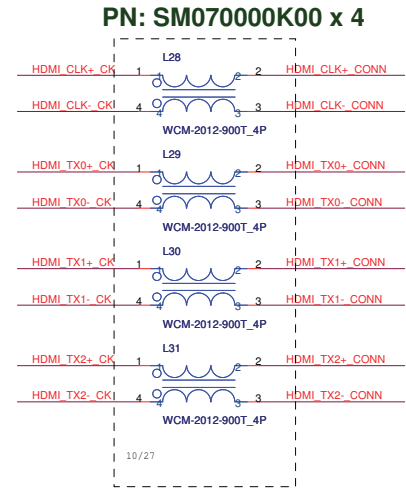
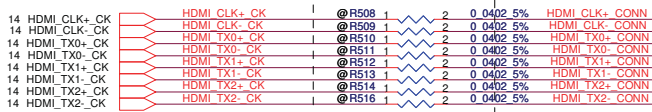
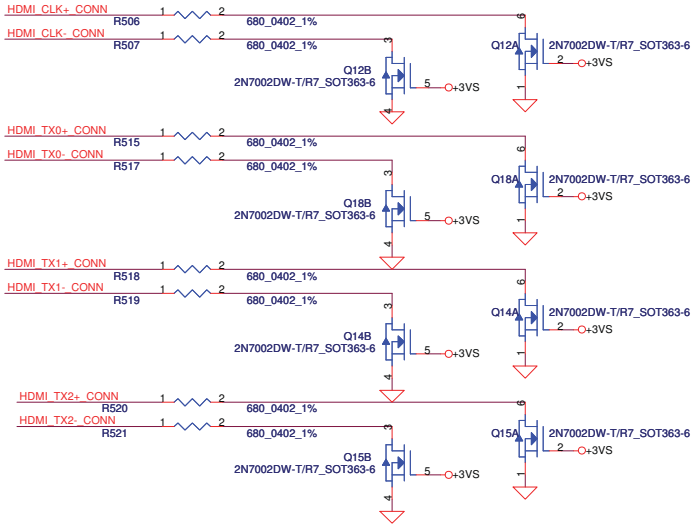


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> PCH (8/9) PWR		
Issued Date	2009/12/01	Deciphered Date	2010/12/31			
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				Size Custom	Document Number <Doc>	

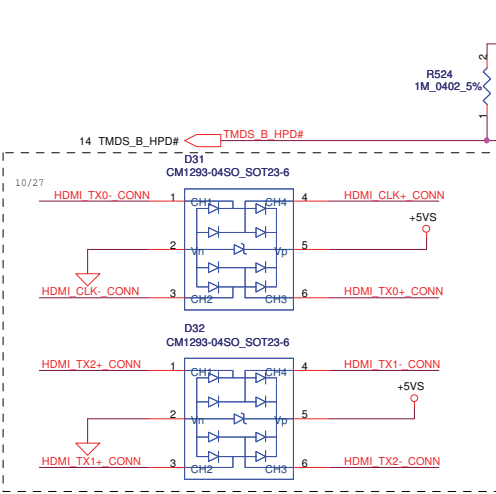


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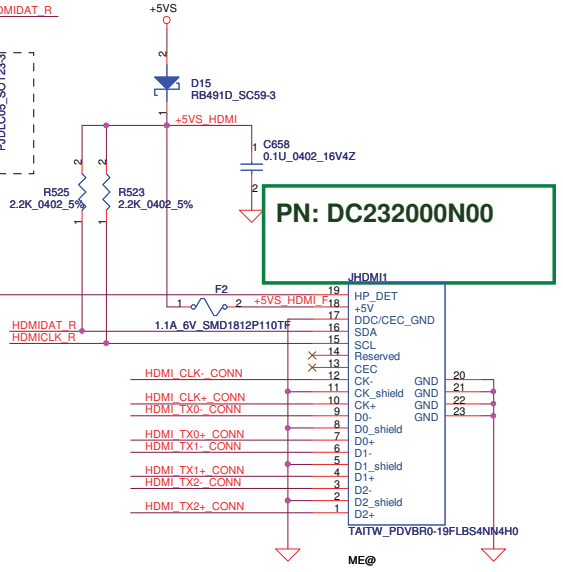
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



PN: SCA00000U10



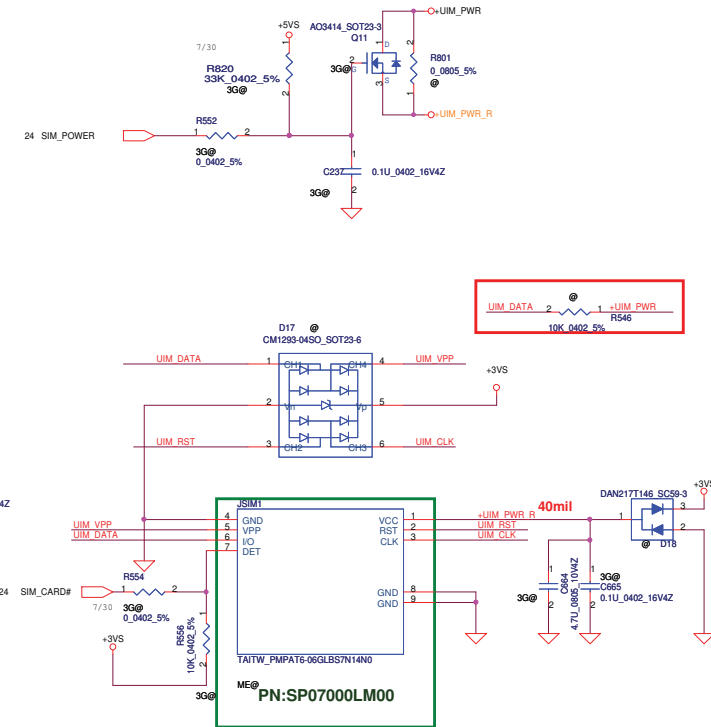
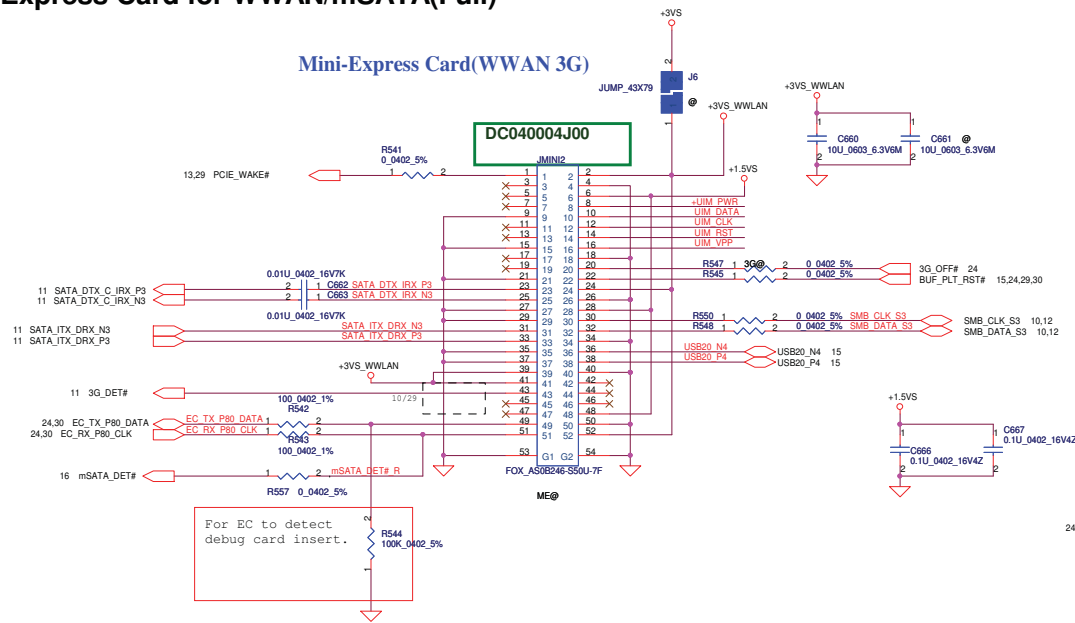
PN: SC300001G00 x 2



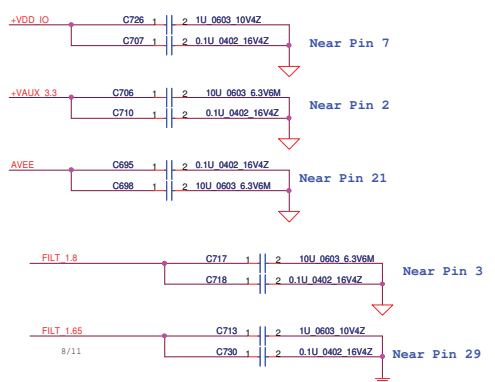
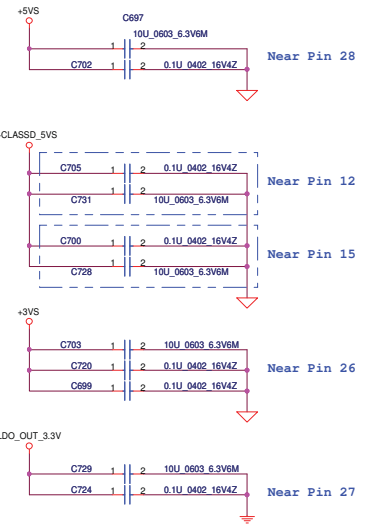
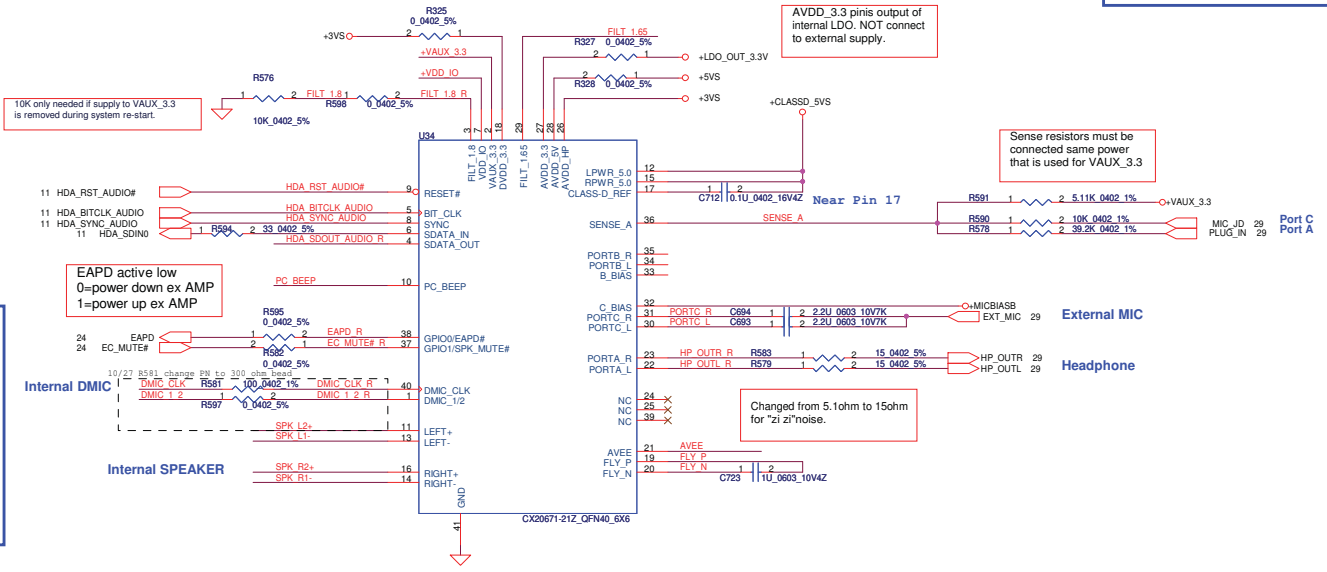
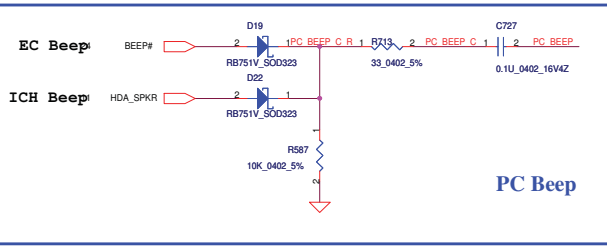
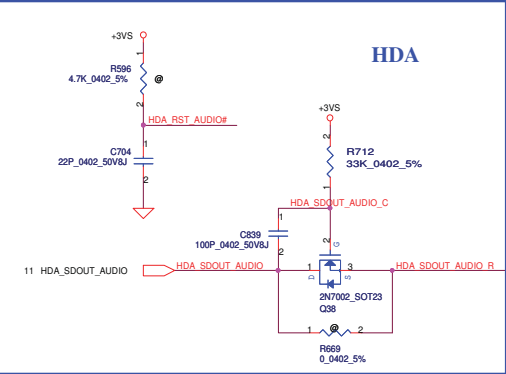
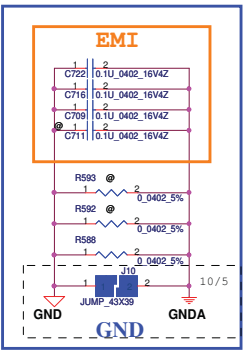
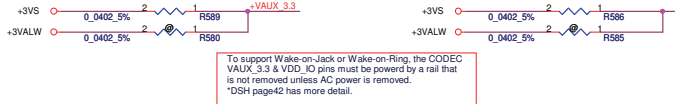
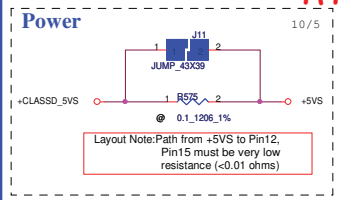
PN: DC232000N00

Mini-Express Card for WWAN/mSATA(Full)

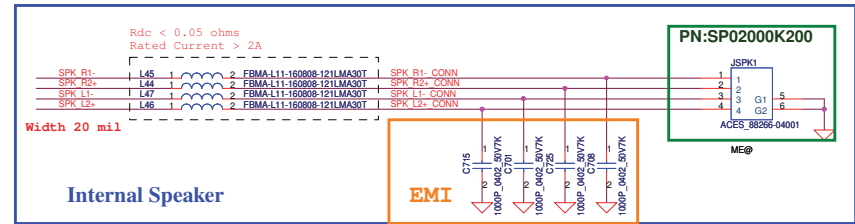
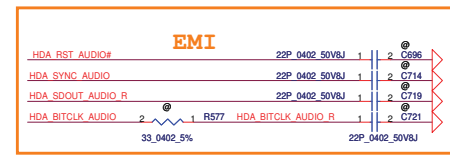
Mini-Express Card(WWAN 3G)



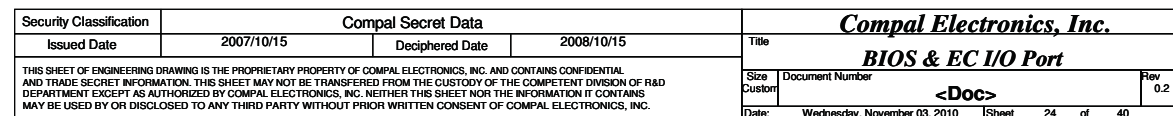
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

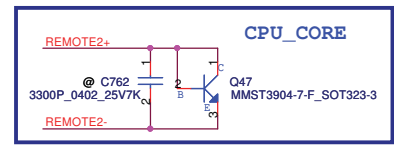
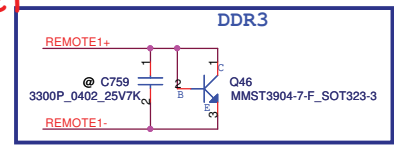
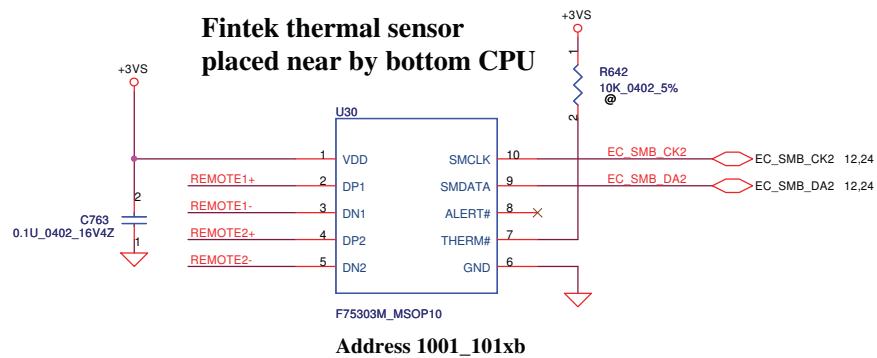
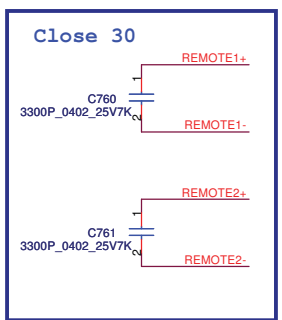


Decoupling CAP

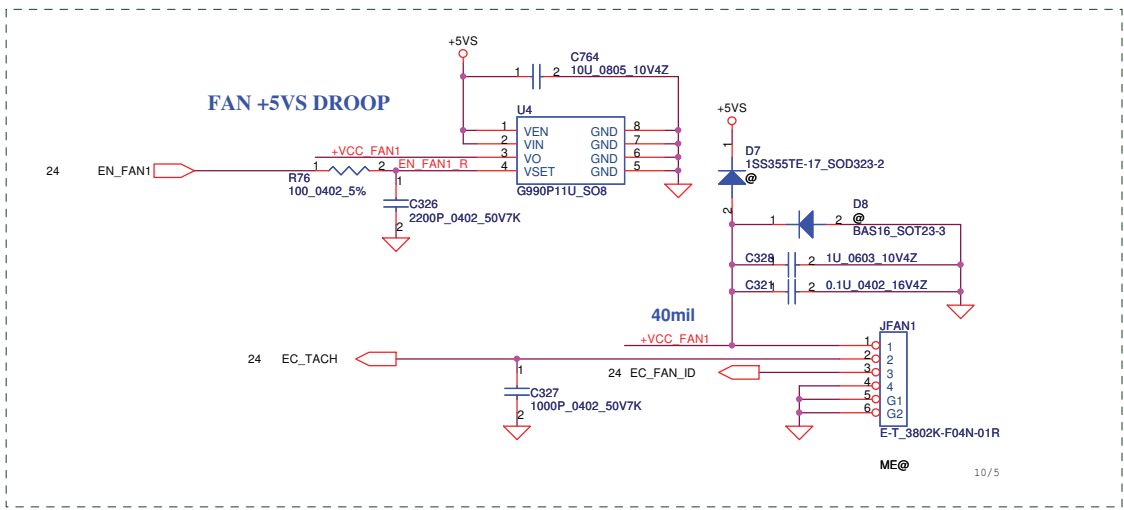


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Size C	Document Number	LA-5751P	Rev	0.2
Date: Wednesday, November 03, 2010		Sheet	23	of 40

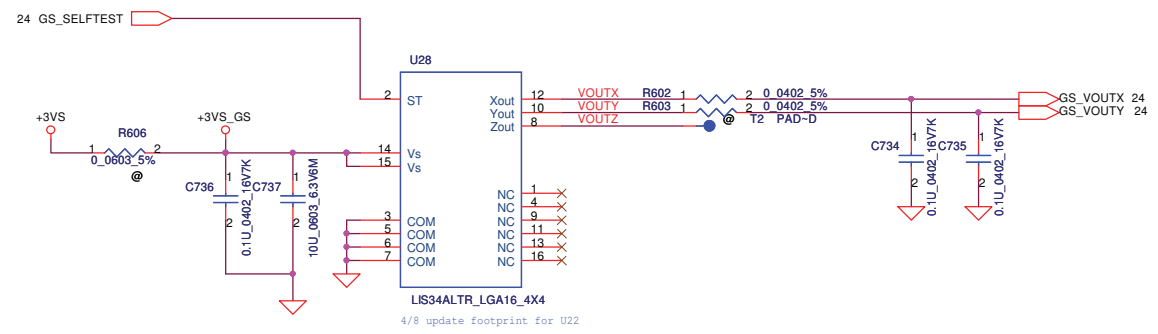
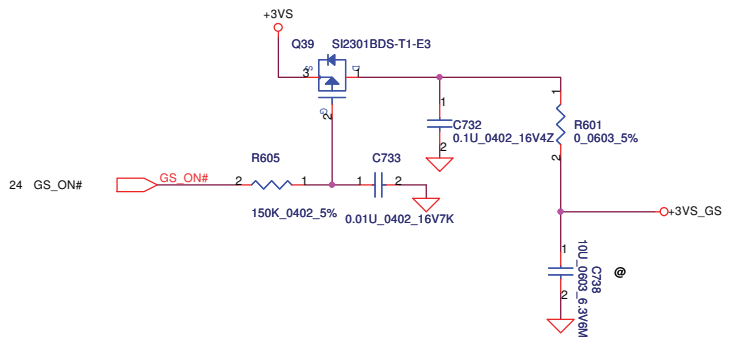




REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

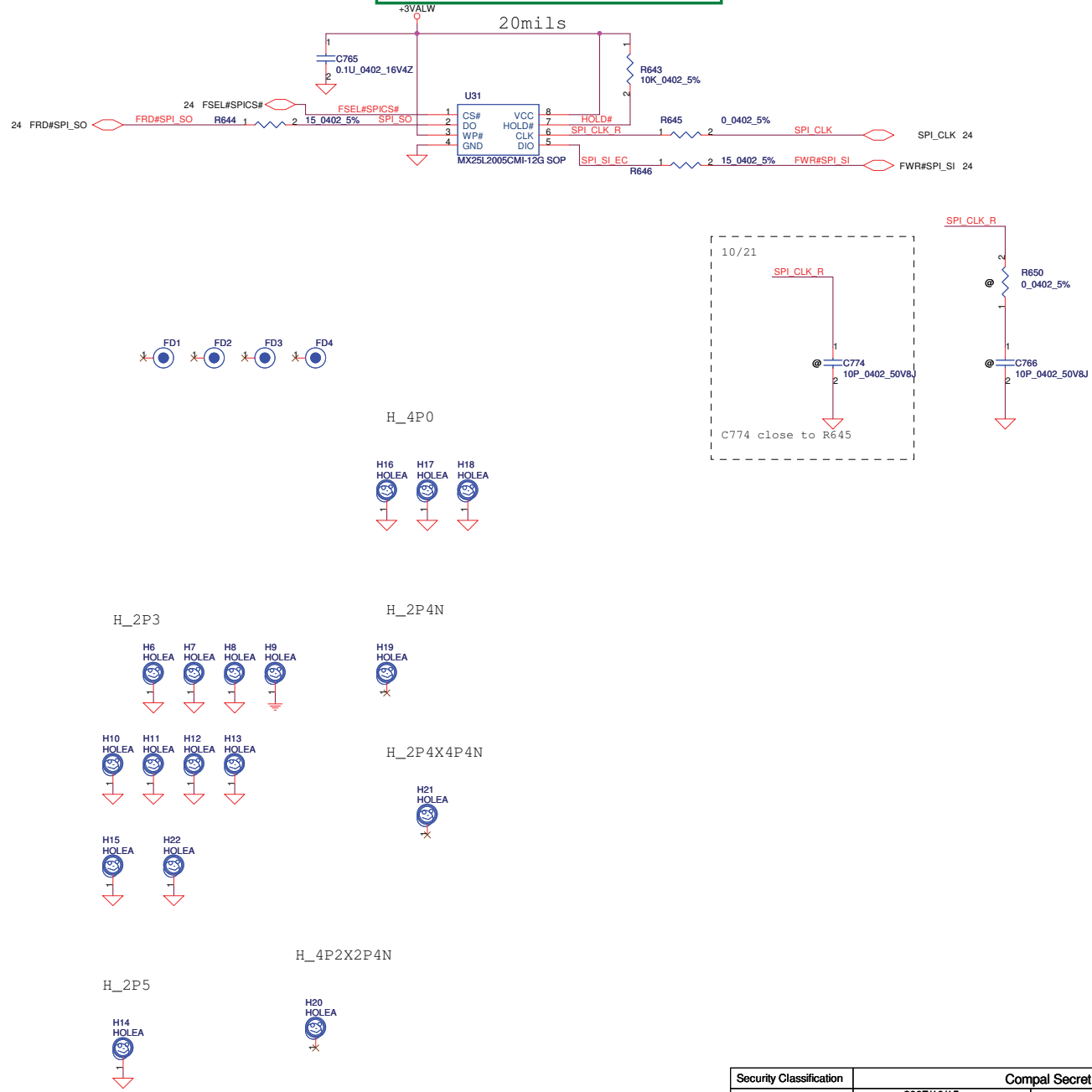


APS G-Sensor

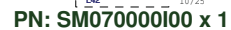


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4/8 update footprint for U22				Size
				Document Number
				Rev
				0.2
				<Doc>
				Date: Wednesday, November 03, 2010
				Sheet 25 of 40

FOR EC 128KB SPI ROM
(150mil PACKAGE)
PN:SA00002C100

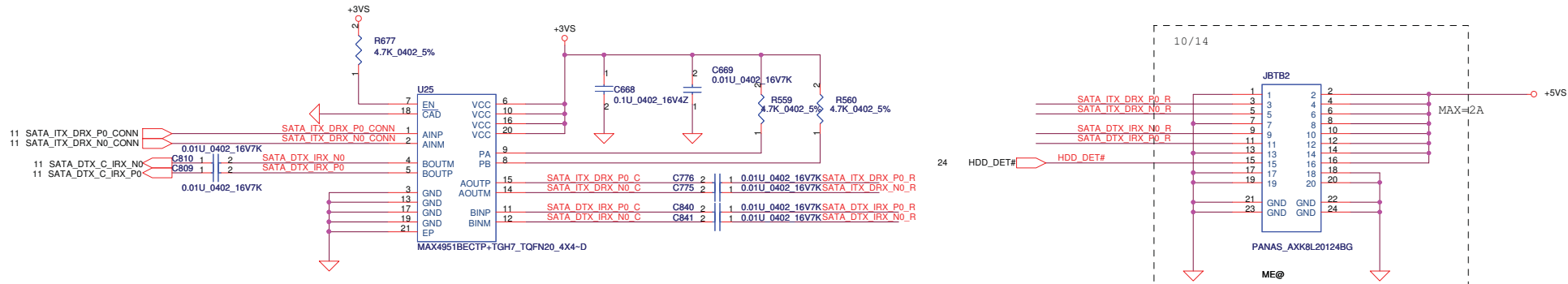


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size		Document Number		Rev	
Custom		LA-5751P		0.2	
Date:		Wednesday, November 03, 2010		Sheet	
				26 of 40	

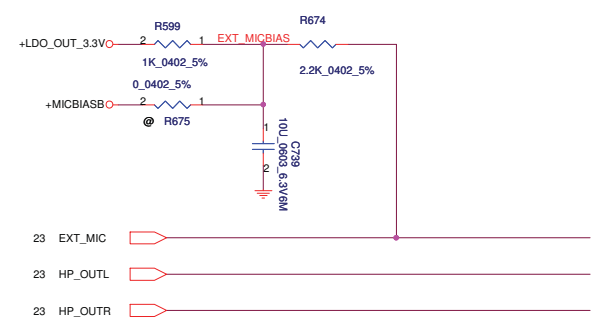


USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

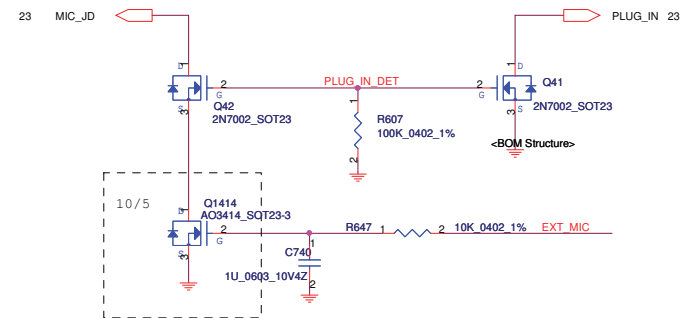
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		USB ports/E-SATA		
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				Date:	Wednesday, November 03, 2010	Sheet	27	of



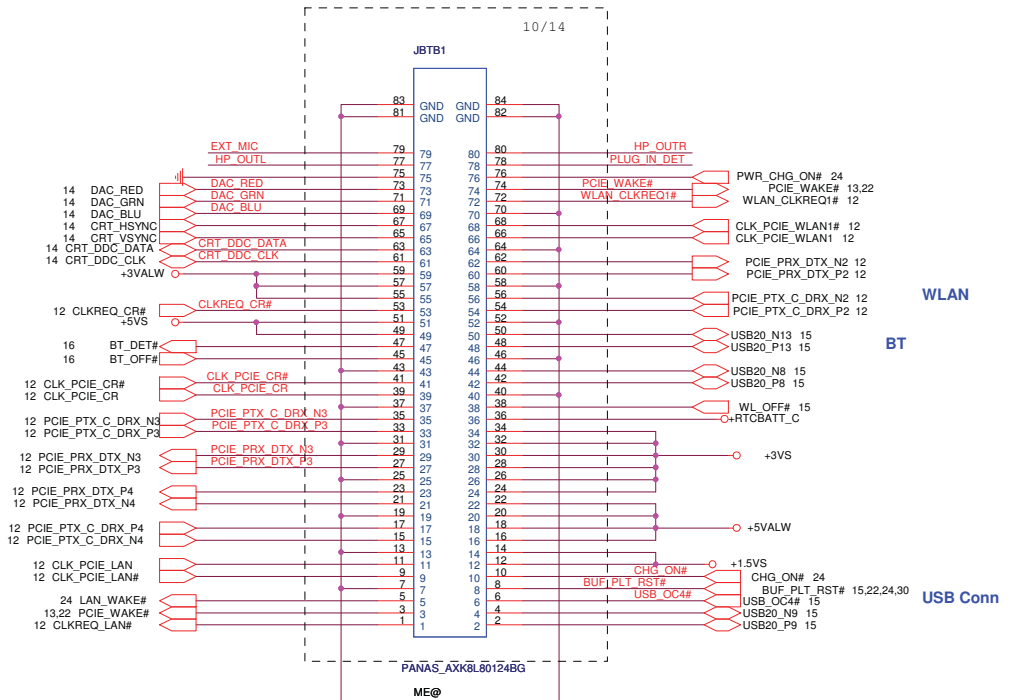
COMBO JACK



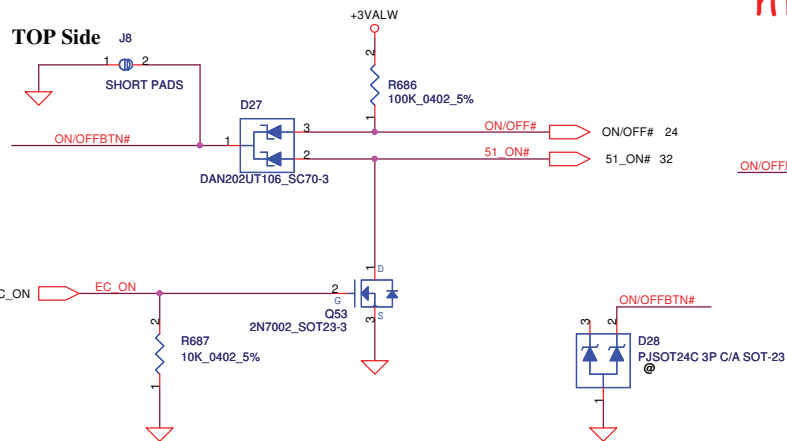
Detection



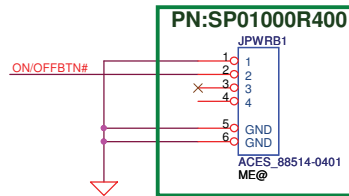
CRT
BT
CARD READER
LAN



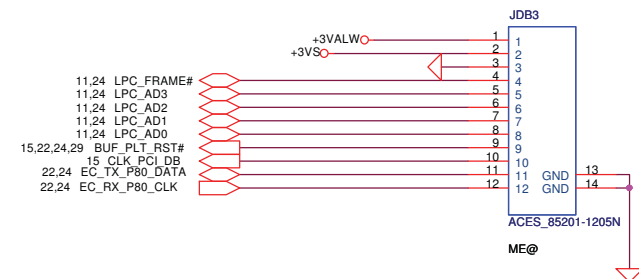
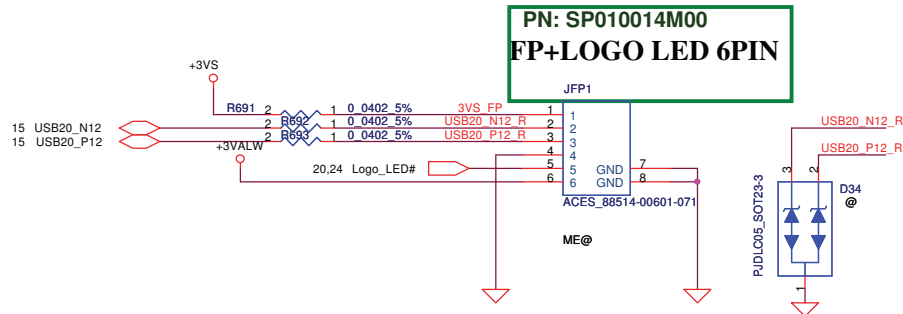
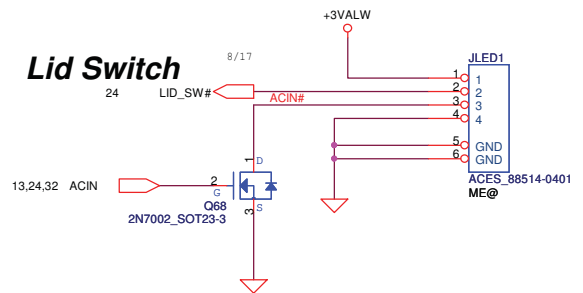
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2007/10/15	Deciphered Date	2008/10/15	Title			
					HDD/IO BTB Connector			
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					Custom			<Doc>
					Date:	Wednesday, November 03, 2010		Sheet



Power Bottom Board Conn. 4pin

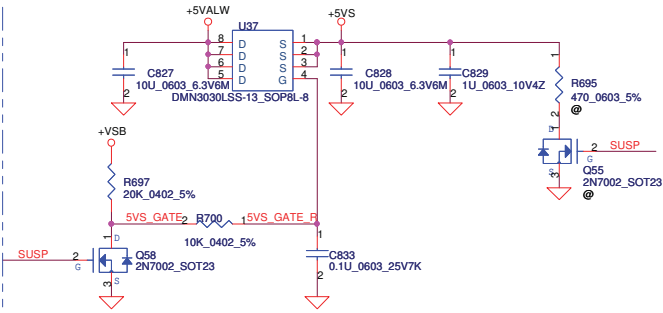


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

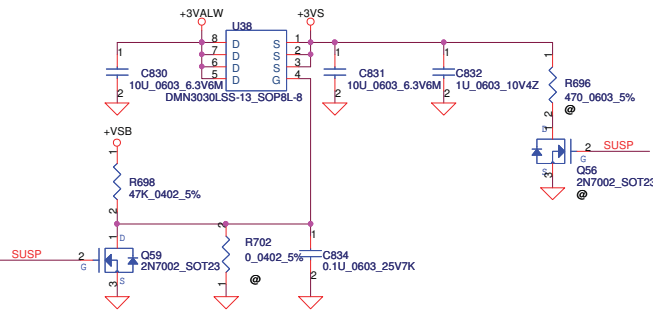


Security Classification		Compal Secret Data				Compal Electronics, Ltd.							
Issued Date		2008/03/25		Deciphered Date		2008/04/		Title					
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						Size Custom	Document Number			<Doc>		Rev 0.2	
						Date:	Wednesday, November 03, 2010			Sheet	30	of	40

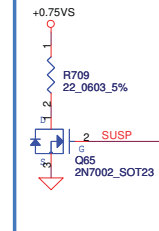
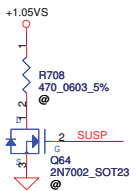
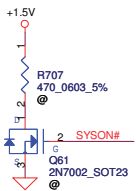
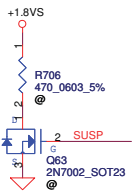
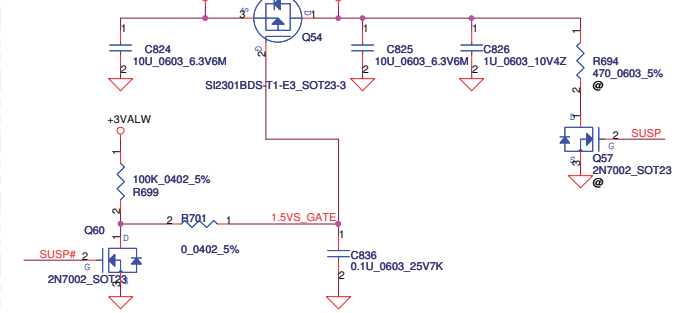
+5VALW TO +5VS



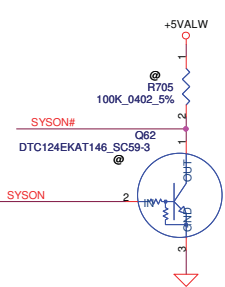
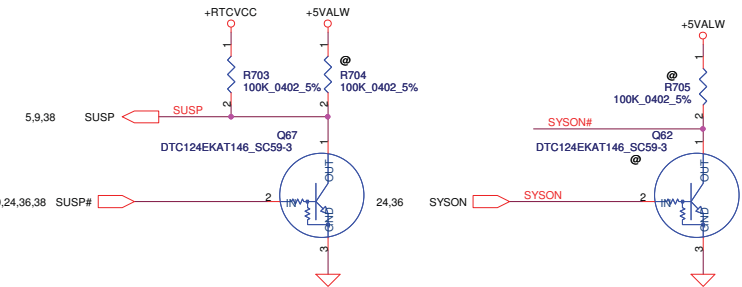
+3VALW TO +3VS

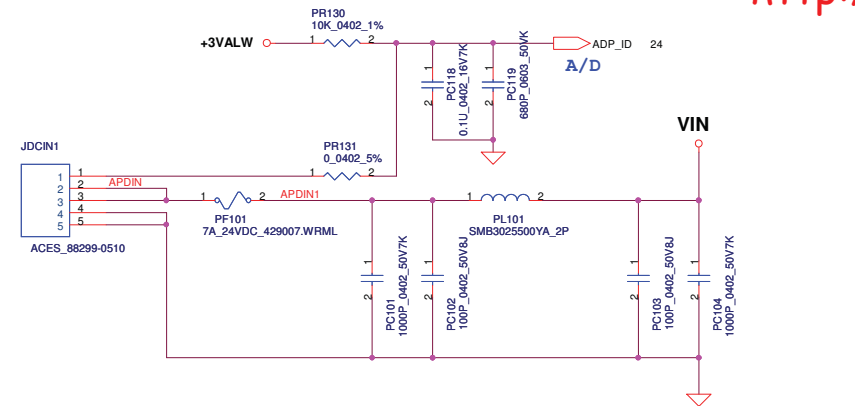


+1.5V to +1.5VS



For Intel S3 Power Reduction.





ACIN

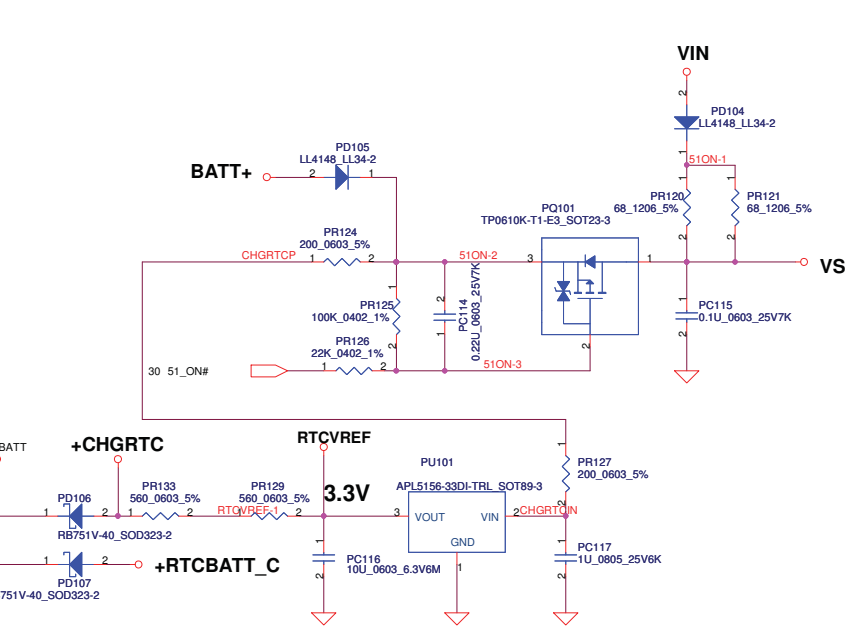
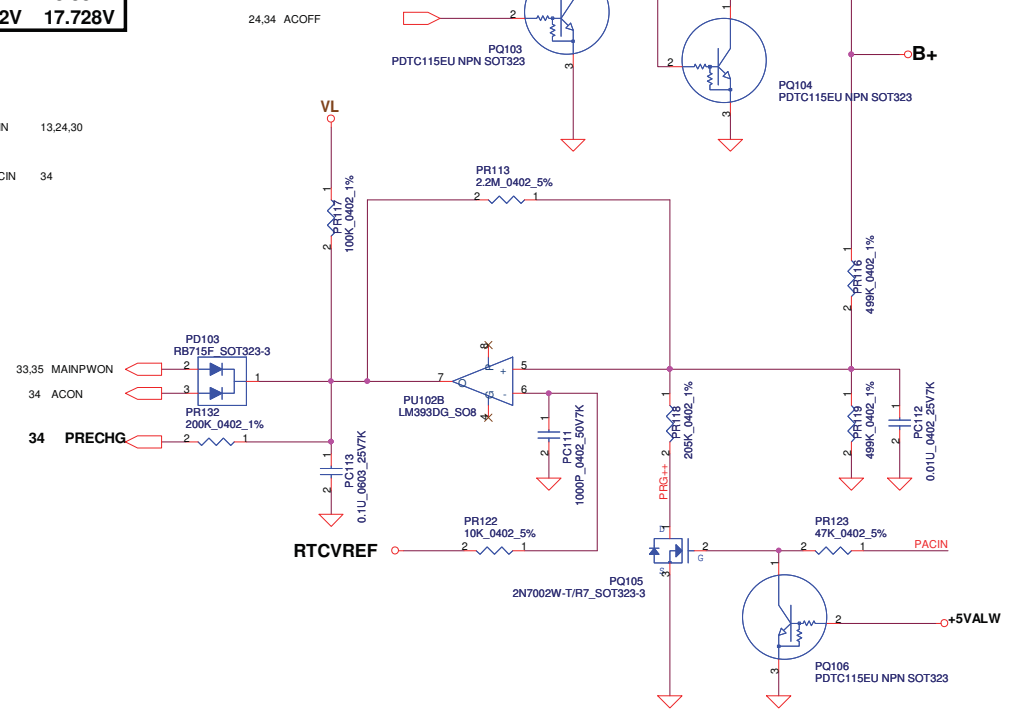
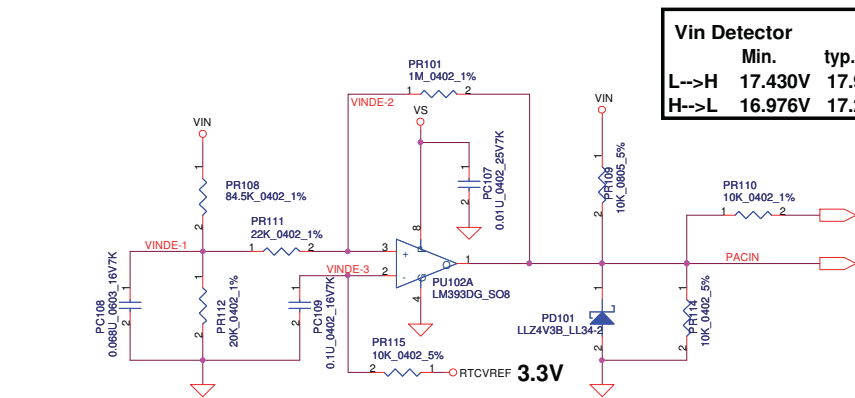
	Precharge detector		
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

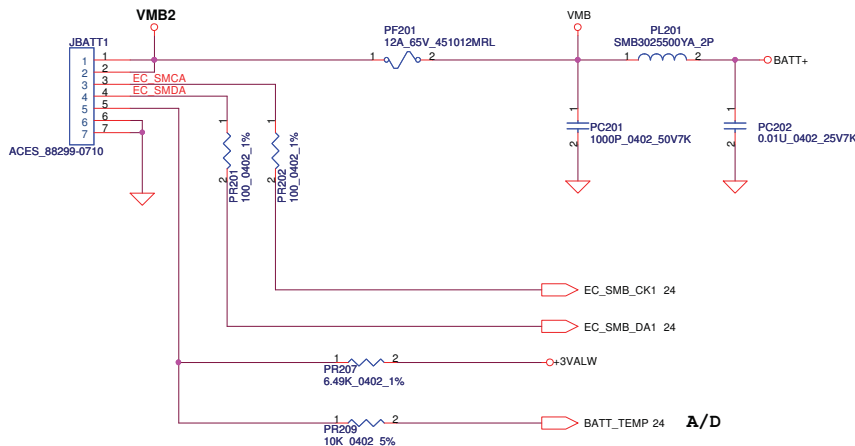
BATT ONLY

	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

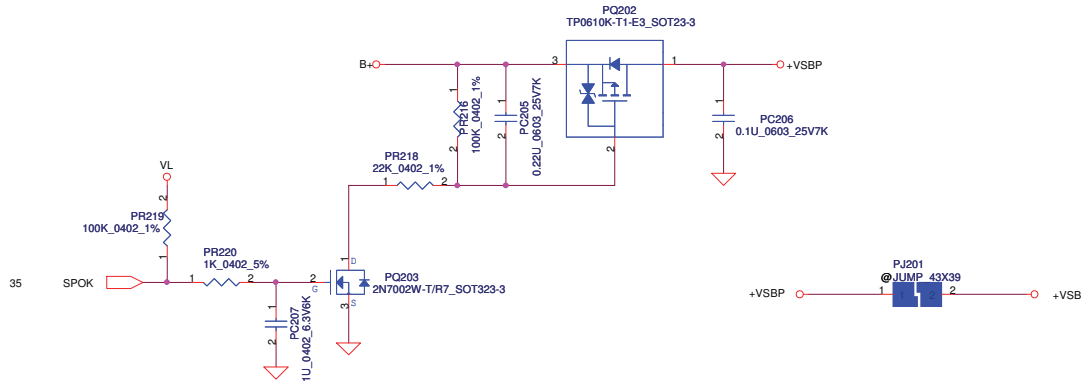
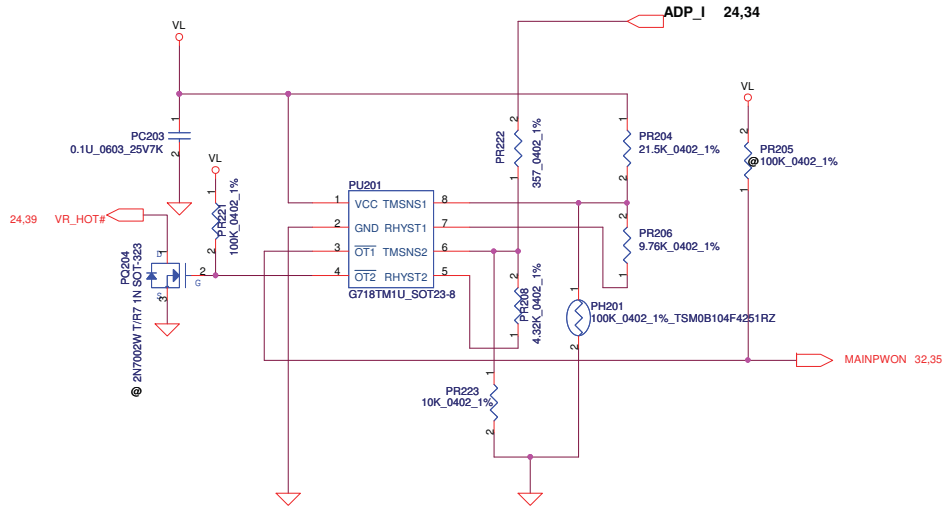
Vin Detector

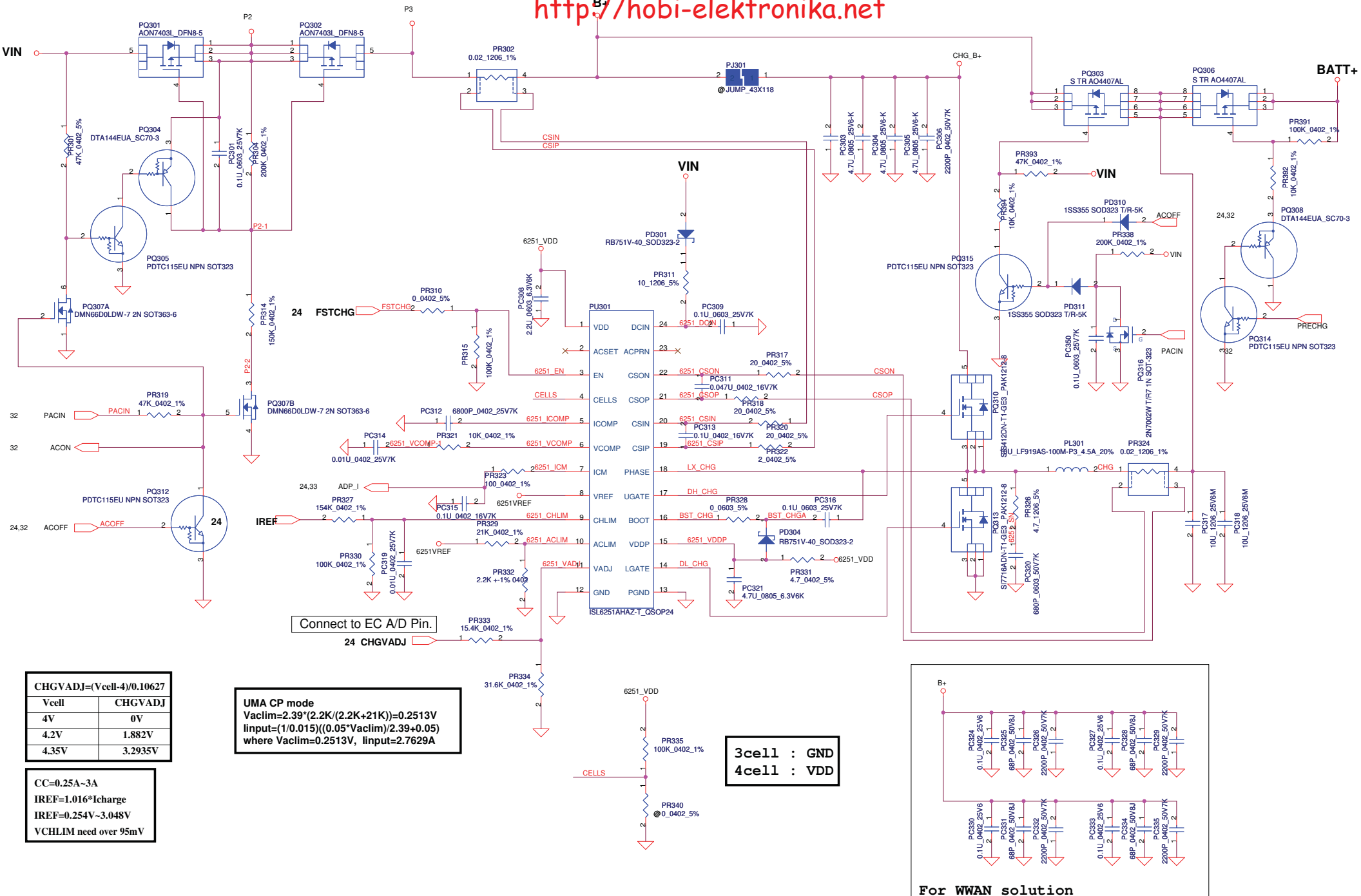
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V





PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



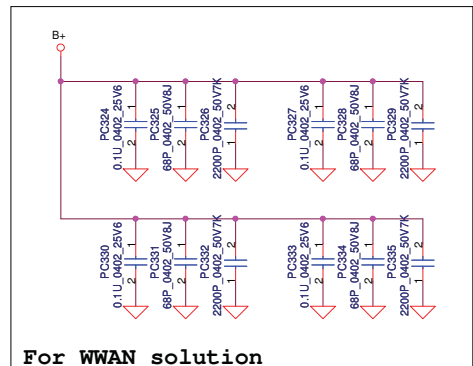


CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

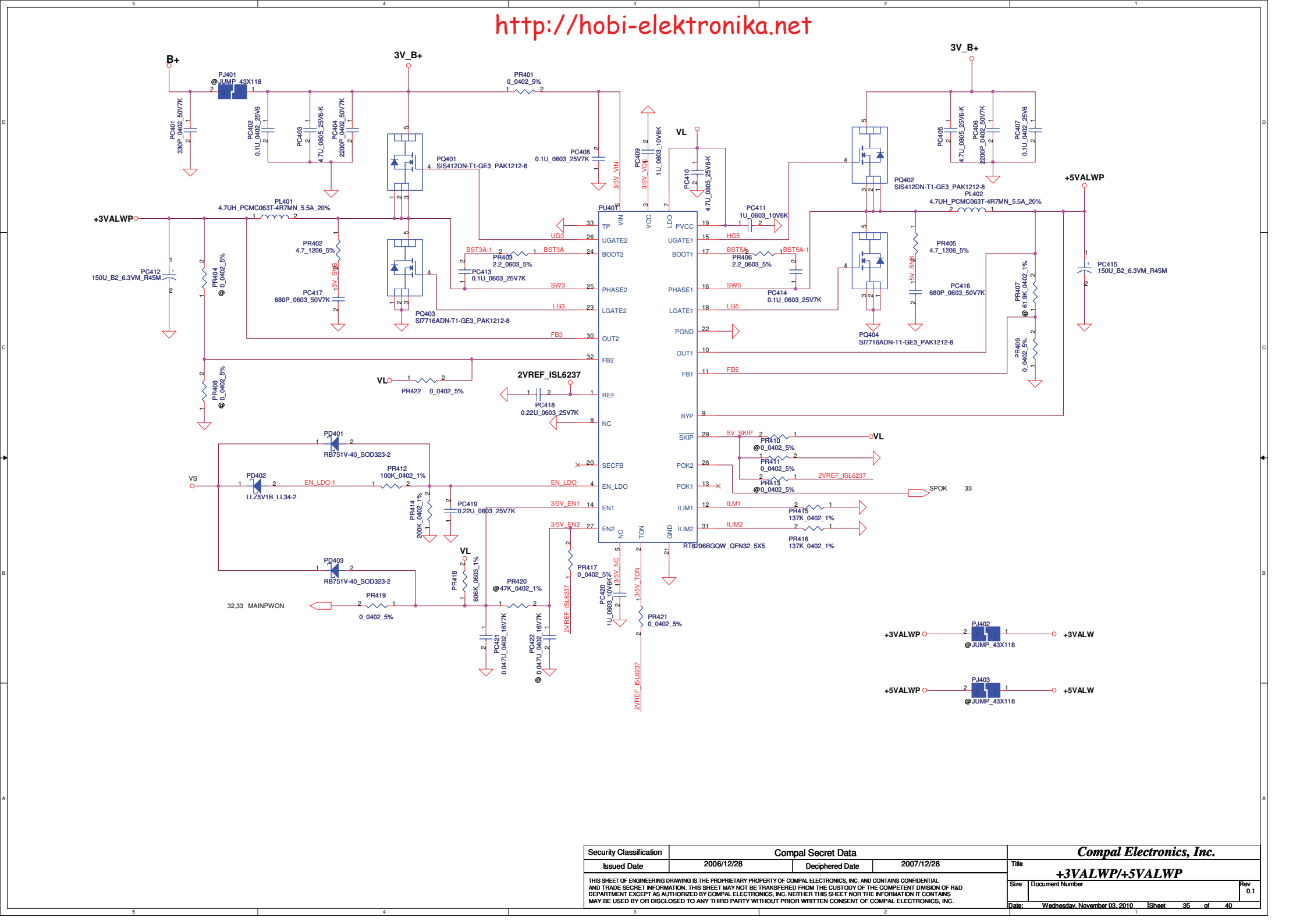
CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

UMA CP mode
 $V_{acim}=2.39 \cdot (2.2K / (2.2K + 21K)) = 0.2513V$
 $I_{inpu} = (1/0.015) \cdot ((0.05 \cdot V_{acim}) / (2.39 + 0.05))$
 where $V_{acim}=0.2513V$, $I_{inpu}=2.7629A$

3cell : GND
4cell : VDD



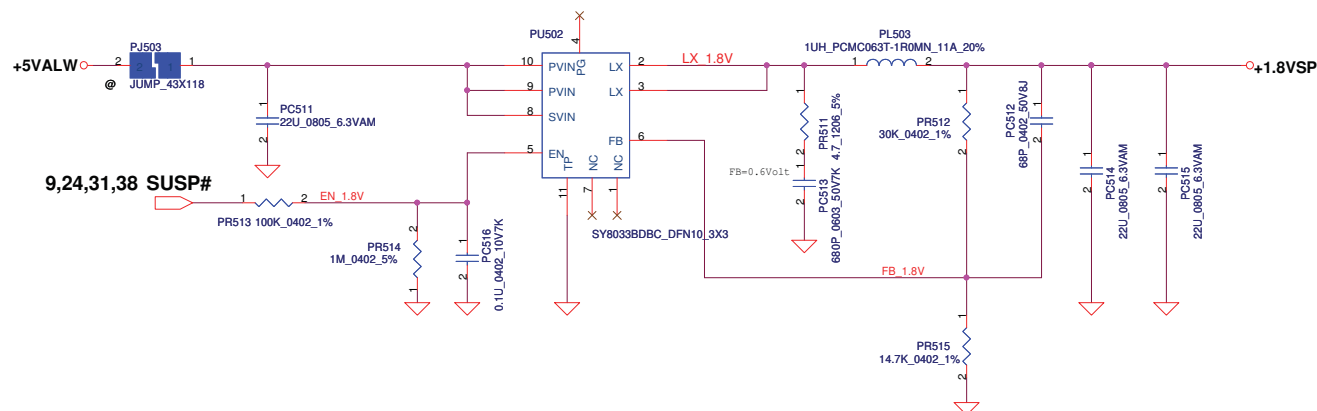
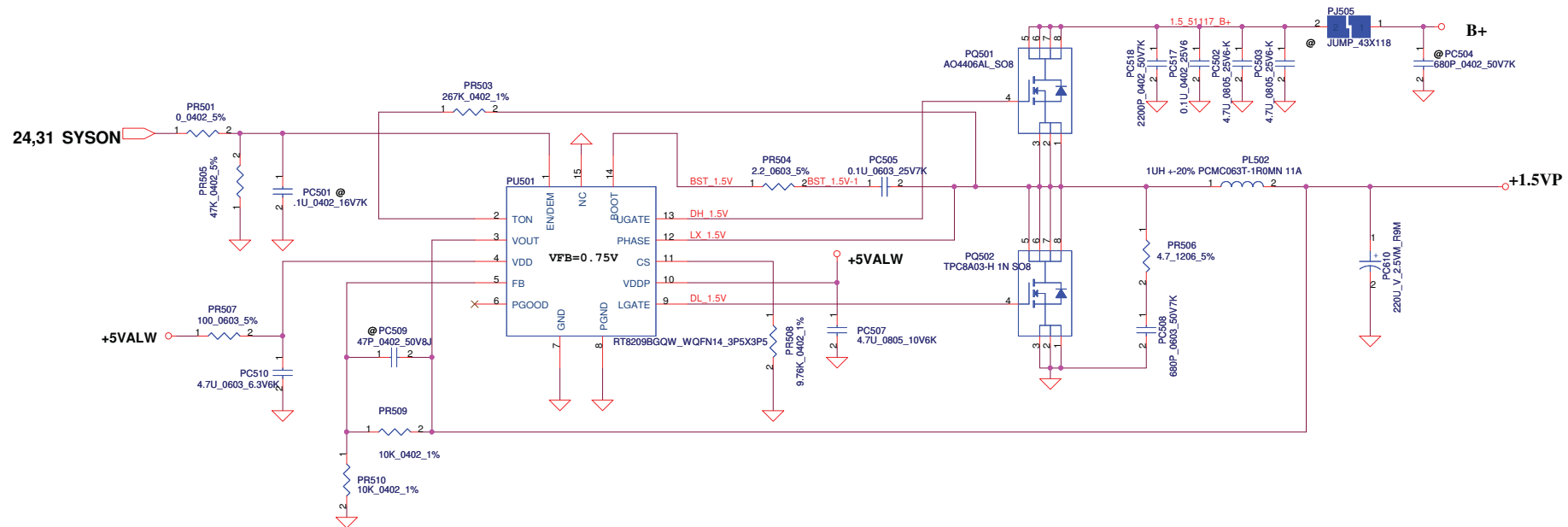
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	CHARGER
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				Date	Wednesday, November 03, 2010
				Sheet	34 of 40
				Rev	0.2



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Component List:

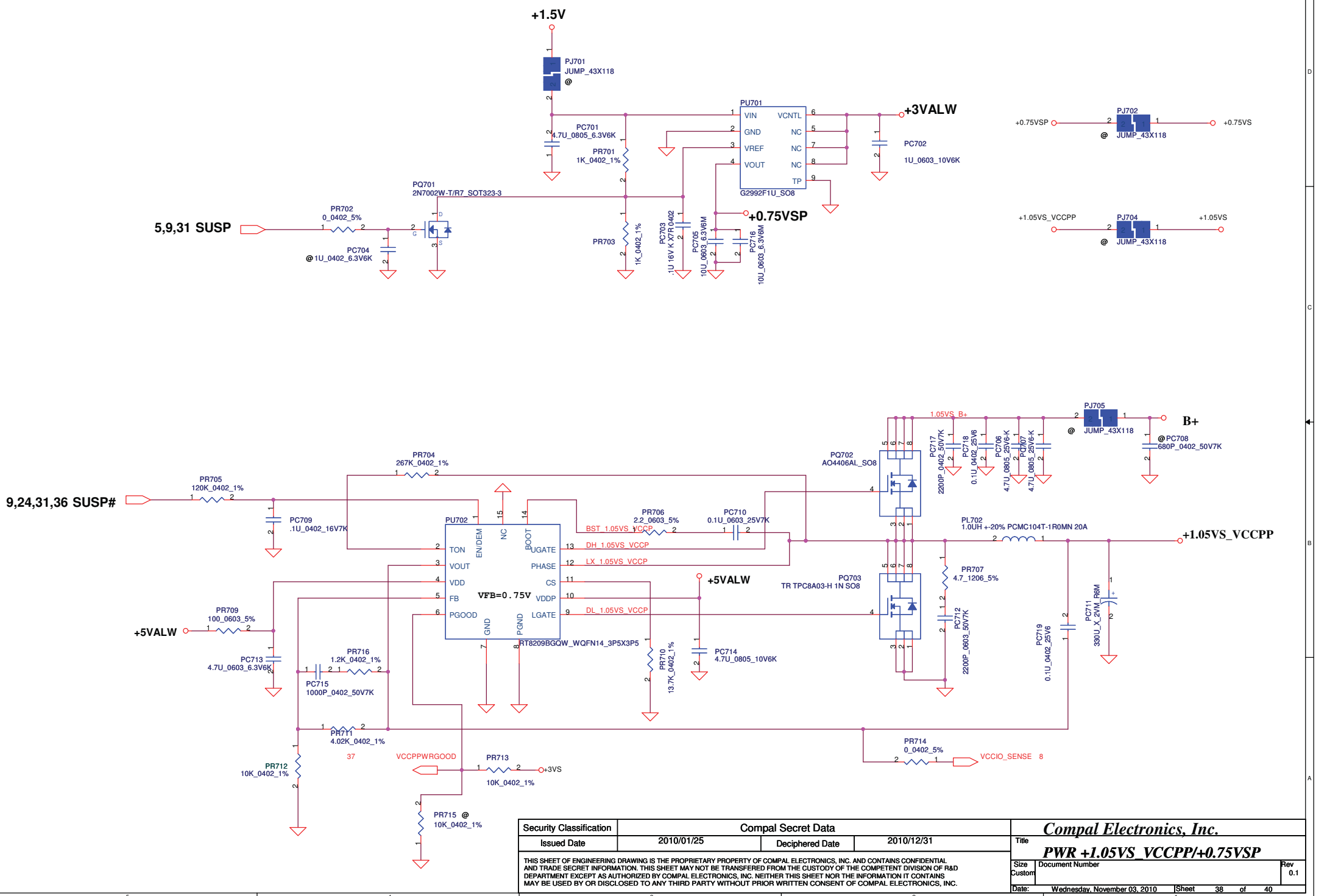
Ref	Value	Part Number
PC401	330P_0402_50V7K	
PC402	0.1U_0402_25V6	
PC403	4.7U_0805_25V6-K	
PC404	220P_0402_50V7K	
PC405	4.7U_0805_25V6-K	
PC406	220P_0402_50V7K	
PC407	0.1U_0402_25V6	
PC408	0.1U_0603_25V7K	
PC409	1U_0603_10V6K	
PC410	4.7U_0805_25V6-K	
PC411	1U_0603_10V6K	
PC412	150U_B2_6.3VM_R45M	
PC413	0.1U_0603_25V7K	
PC414	0.1U_0603_25V7K	
PC415	150U_B2_6.3VM_R45M	
PC416	680P_0603_50V7K	
PC417	680P_0603_50V7K	
PC418	0.22U_0603_25V7K	
PC419	0.22U_0603_25V7K	
PC420	0.047U_0402_16V7K	
PC421	0.047U_0402_16V7K	
PC422	0.047U_0402_16V7K	
PR401	0.0402_5%	
PR402	4.7_1206_5%	
PR403	2.2_0603_5%	
PR404	2.2_0603_5%	
PR405	4.7_1206_5%	
PR406	2.2_0603_5%	
PR407	0.0402_5%	
PR408	0.0402_5%	
PR409	0.0402_5%	
PR410	0.0402_5%	
PR411	0.0402_5%	
PR412	100K_0402_1%	
PR413	0.0402_5%	
PR414	0.0402_5%	
PR415	137K_0402_1%	
PR416	137K_0402_1%	
PR417	0.0402_5%	
PR418	806K_0603_1%	
PR419	0.0402_5%	
PR420	47K_0402_1%	
PR421	0.0402_5%	
PR422	0.0402_5%	
PL401	4.7UH_PCMC063T-4R7MN_5.5A_20%	
PL402	4.7UH_PCMC063T-4R7MN_5.5A_20%	
PQ401	SIS412DN-T1-GE3_PAK1212-8	
PQ402	SIS412DN-T1-GE3_PAK1212-8	
PQ403	SI7716ADN-T1-GE3_PAK1212-8	
PQ404	SI7716ADN-T1-GE3_PAK1212-8	
PD401	RB751V-40_SOD323-2	
PD402	LLZ5V1B_LL34-2	
PD403	RB751V-40_SOD323-2	
PU401	RT8206BGQW_QFN32_5X5	



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Size	Custom	Document Number		Rev	0.1
Date:	Wednesday, November 03, 2010	Sheet	36	of	40

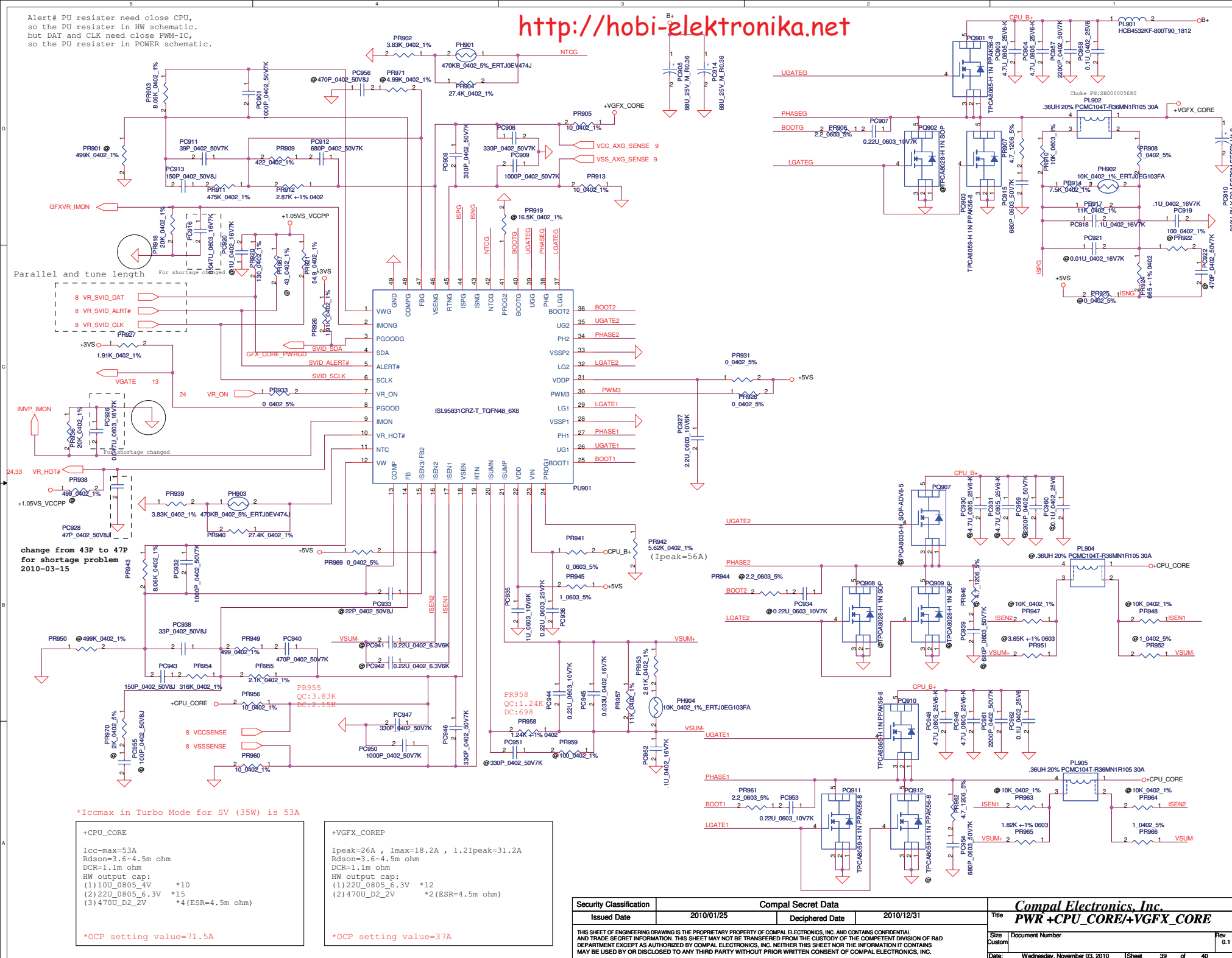
Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR + VCCSAP		
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title		
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				Date: Wednesday, November 03, 2010	Sheet 37 of 40	



Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

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Parallel and tune length

For shortage changed

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

change from 43P to 47P for shortage problem 2010-03-15

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*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 100U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

*OCP setting value=37A

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