

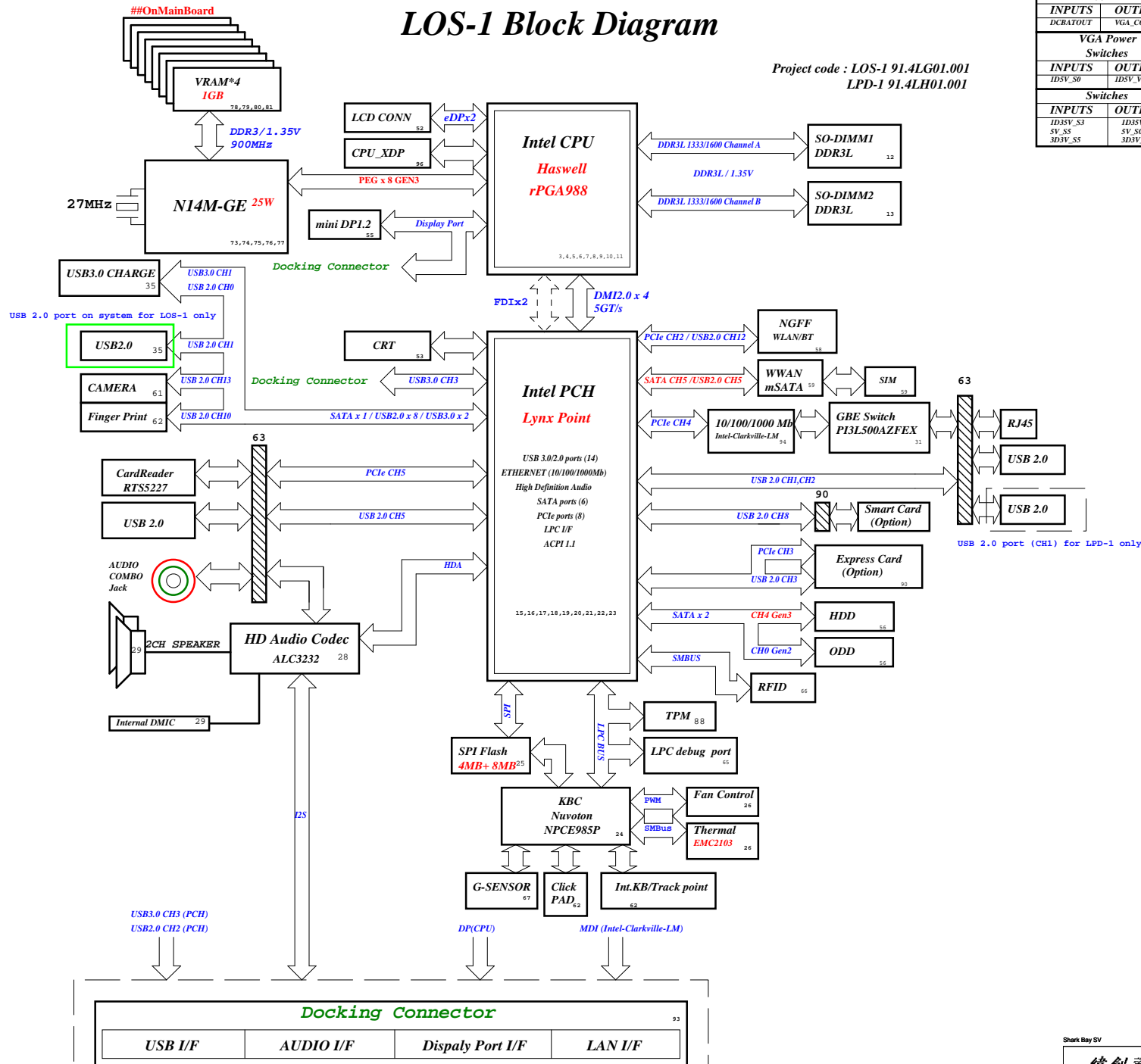
LOS-1 DIS/UMA Schematics

Intel Haswell(rPGA989)

Intel PCH(Lynx Point)

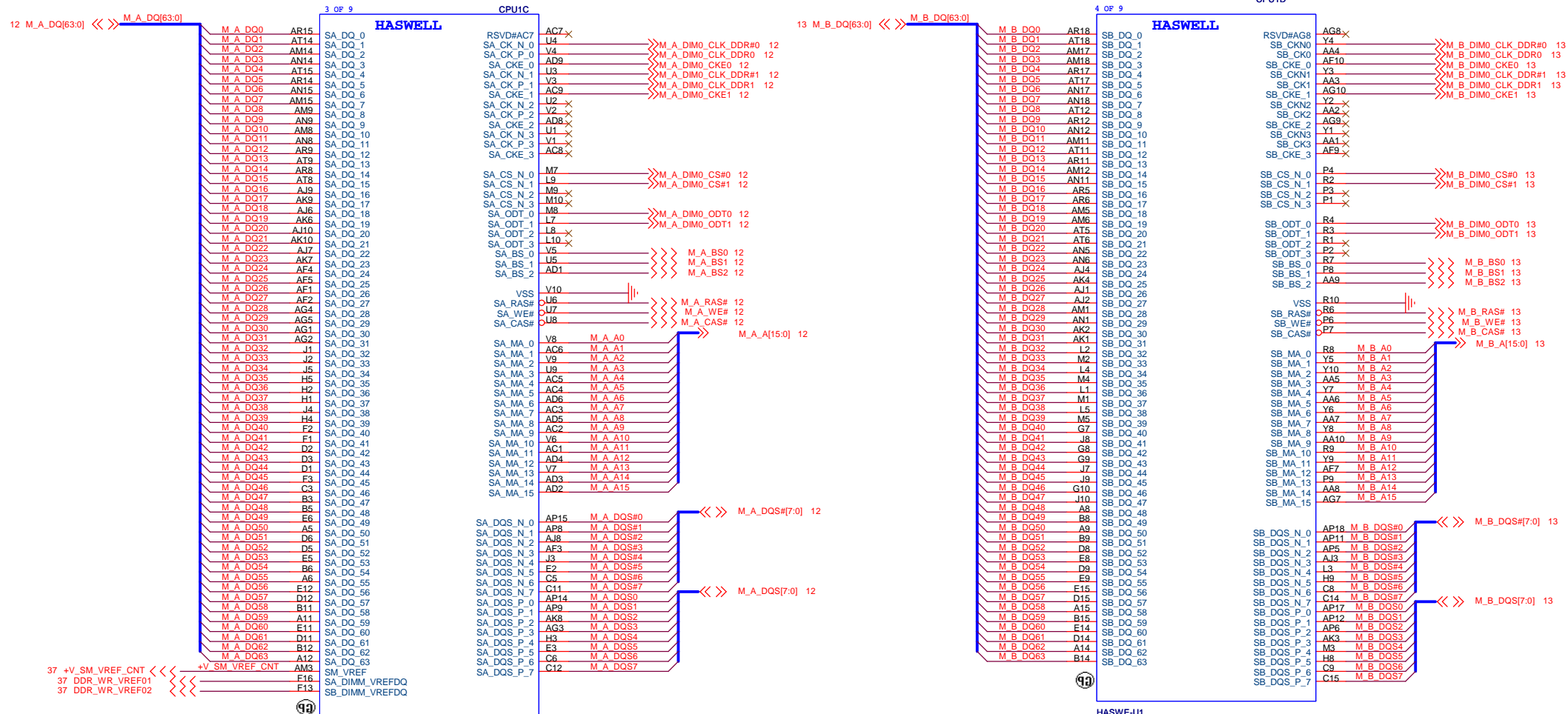
LOS-1 Block Diagram

Project code : LOS-1 91.4LG01.001
LPD-1 91.4LH01.001



	VGA RT8812A 82			CHARGER BQ24760 4	
	INPUTS	OUTPUTS		INPUTS	OUTPUTS
	DCRATOUT	VGA_CORE		AD+ BT+	DCRATOUT
	VGA Power Switches 83			SYSTEM DC/DC TPS51225	
	INPUTS	OUTPUTS		INPUTS	OUTPUTS
	ID5V_S0	ID5V_VGA_S0			5V_AUX_S5 3D3V_AUX_S5 5V_PWR 3D3V_PWR
	Switches 36			DCRATOUT	
	INPUTS	OUTPUTS		CPU DC/DC TPS51631 46,4	
	ID35V_S3 5V_S5 3D3V_S5	ID35V_S0 5V_S0 3D3V_S0		INPUTS	OUTPUTS
				DCRATOUT	VCC_CORE
				SYSTEM DC/DC TPS51211DSCR 5	
				INPUTS	OUTPUTS
				DCRATOUT	ID5V_S0
				SYSTEM DC/DC TPS51211DSCR 4	
				INPUTS	OUTPUTS
				DCRATOUT	ID6V5_LAN
				SYSTEM LDO TPS79318DBVR 5	
				INPUTS	OUTPUTS
				3D3V_S5	ID8V_S0
				SYSTEM DC/DC TPS51216 4	
				INPUTS	OUTPUTS
				DCRATOUT	ID35V_S3 0D675V_S0 ID0K_VREF_S3
				PCB LAYER	
				L1: TOP	L5: VCC
				L2: GND	L6: Signal
				L3: Signal	L7: GND
				L4: Signal	L8: BOTTOM

SSID = CPU



HASWE-U1
62.10040.921

HASWE-U1

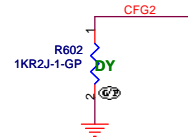
62.10040.921

Main: 62.10040.921
2nd: 62.10040.941

SSID = CPU

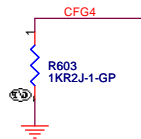
PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



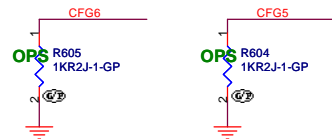
eDP Enable

CFG4	1:Disable 0:Enable
------	-----------------------

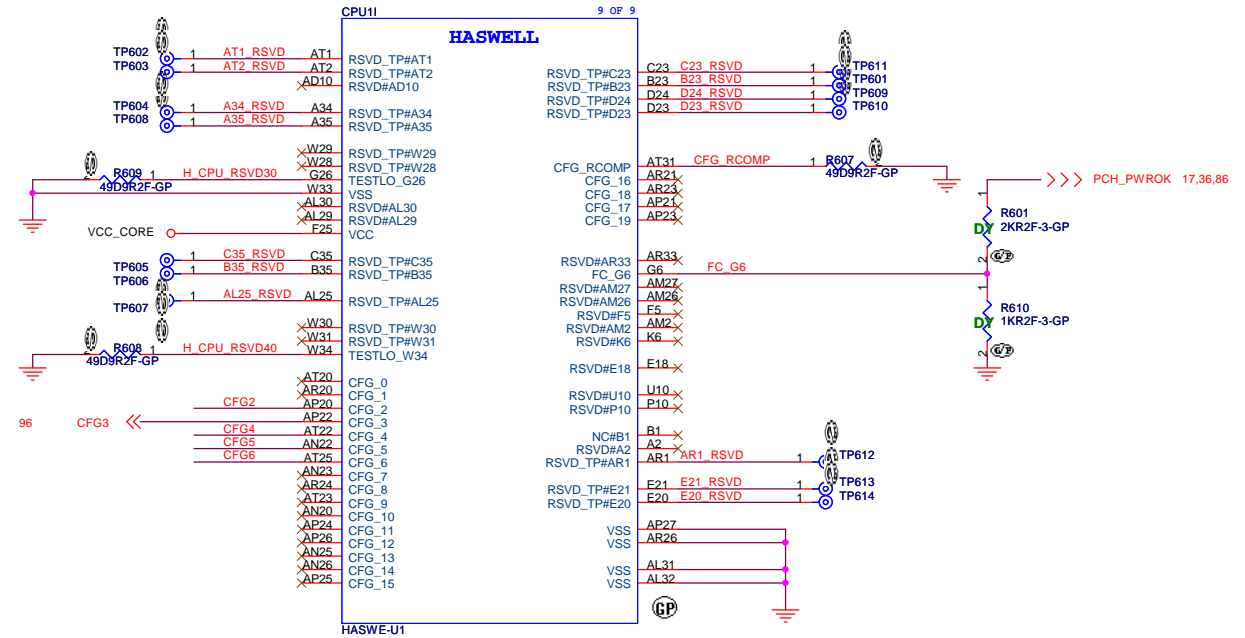


CFG[6:5] : PEG Bifurcation

CFG[6:5]	11 : Func 1 Disabled, Func 2 Disabled (x16,---,---) 10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---) 01 : Func 1 Disabled, Func 2 Enabled 00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)
----------	---



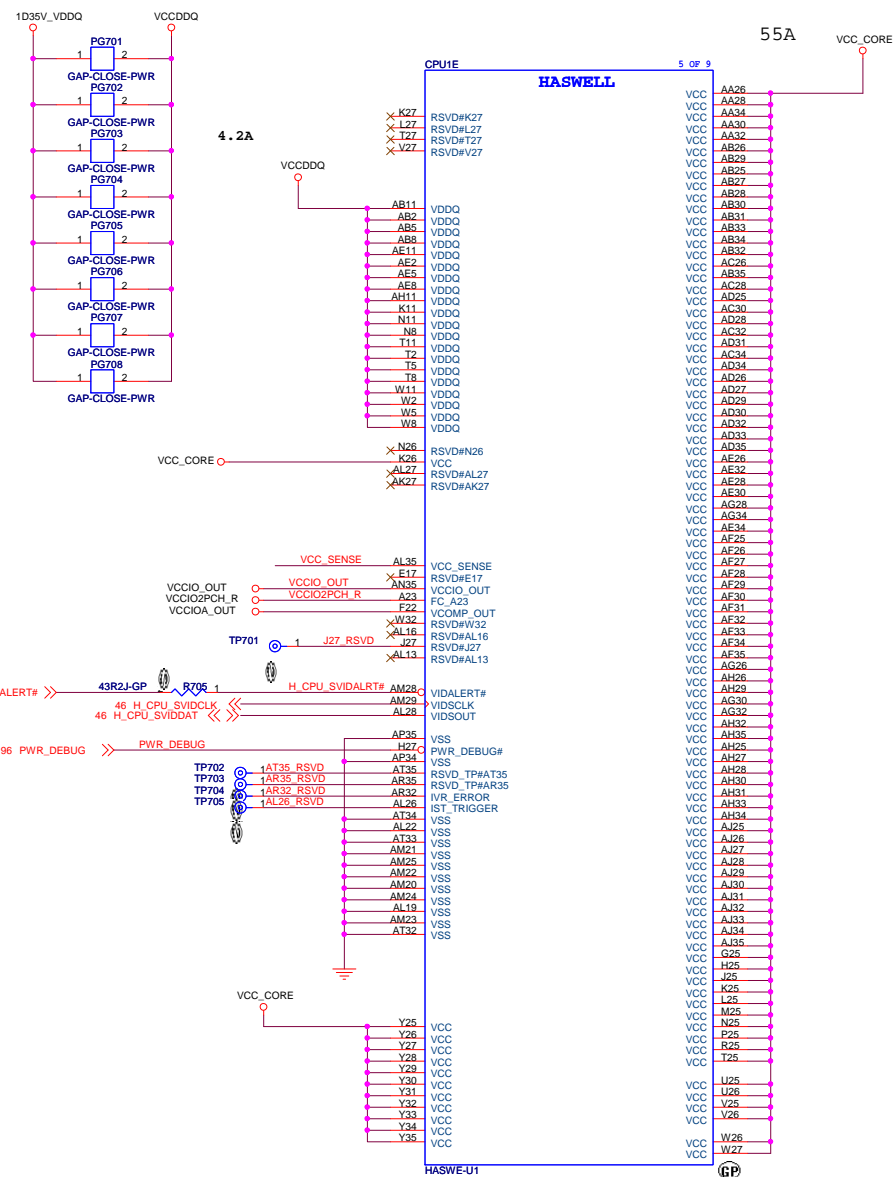
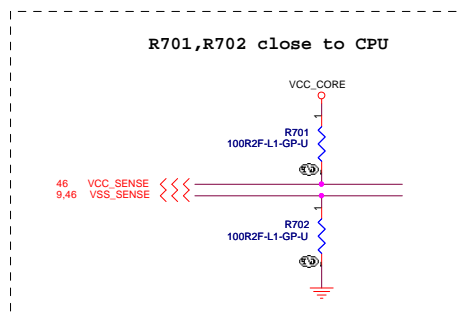
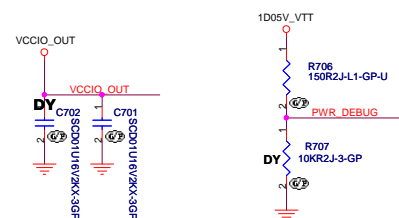
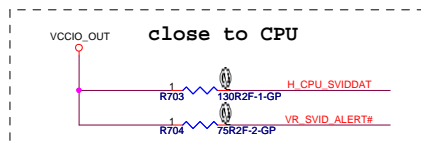
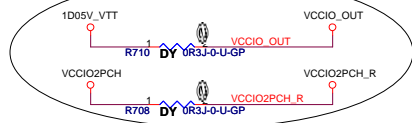
	PEG x16	PEG x8
R605	DY	ASM
R604	DY	ASM



62.10040.921

SSID = CPU

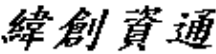
For Next GEN CPU



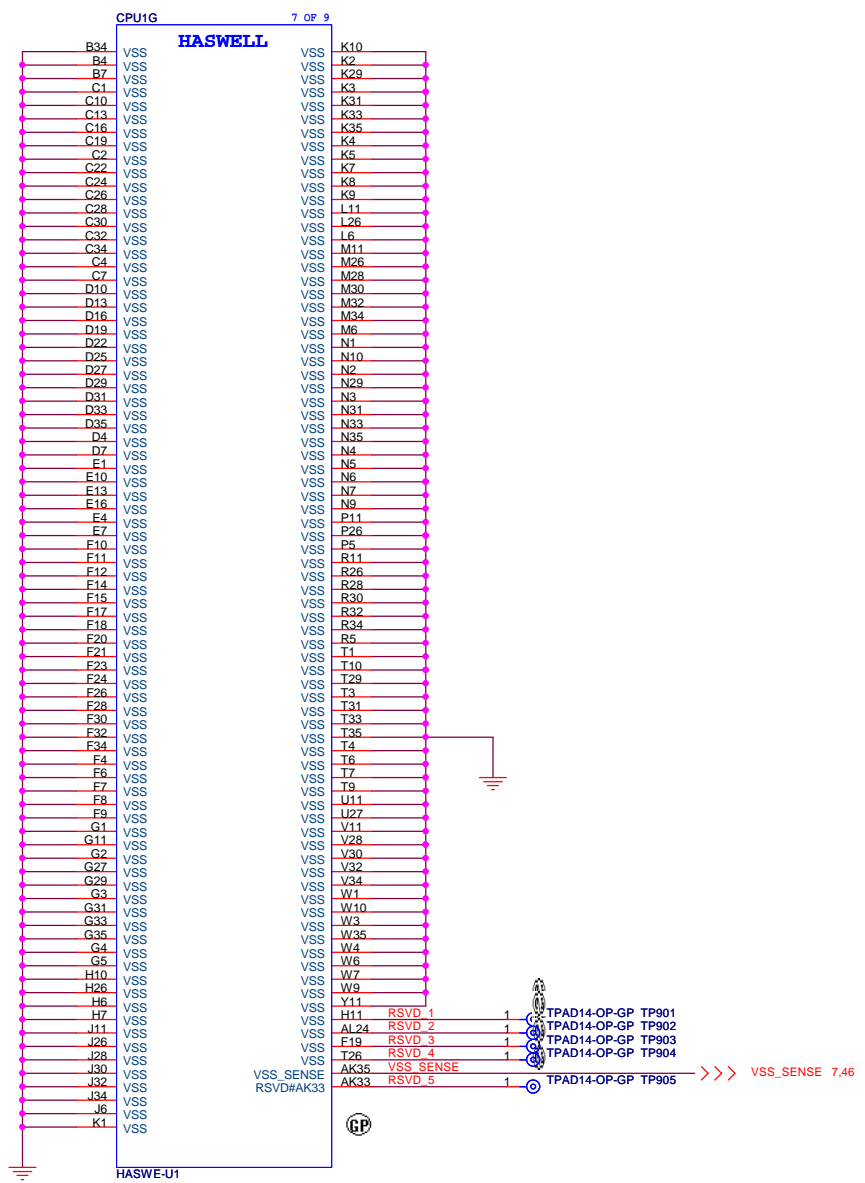
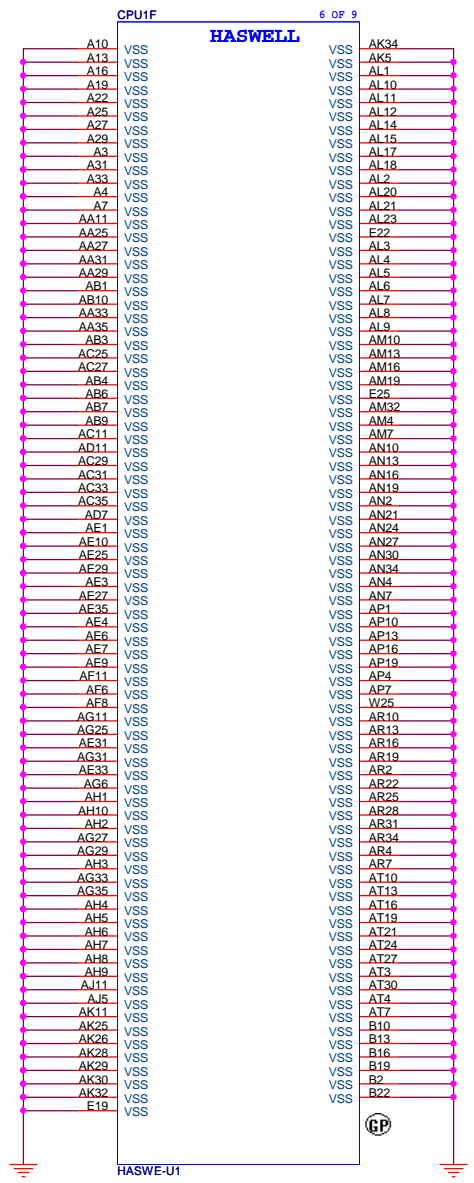
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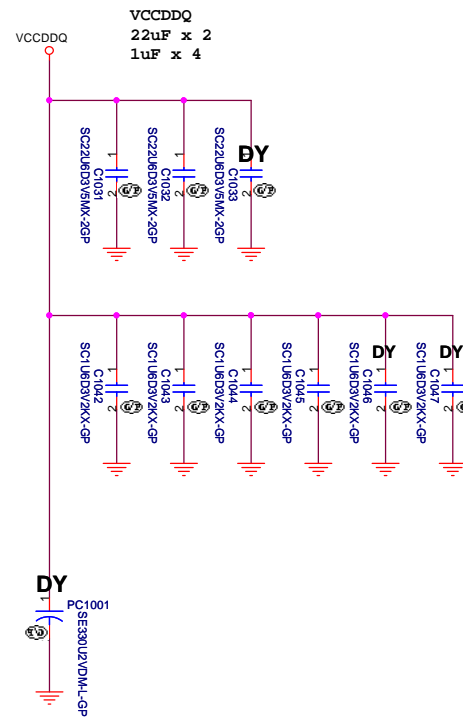
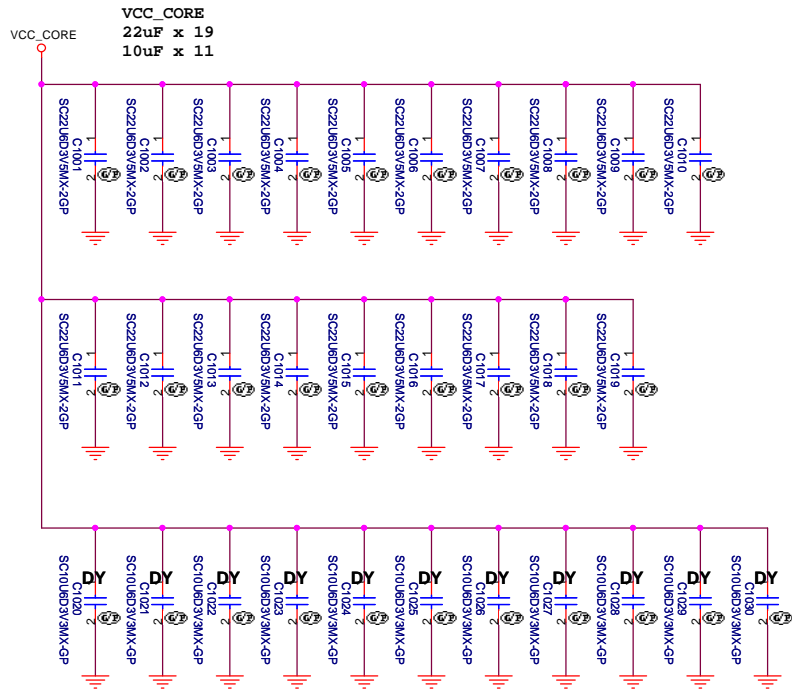
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Title			
CPU (VCC_GFXCORE)			
Size A4	Document Number		Rev
	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013		Sheet 8 of 102

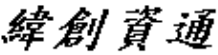
SSID = CPU



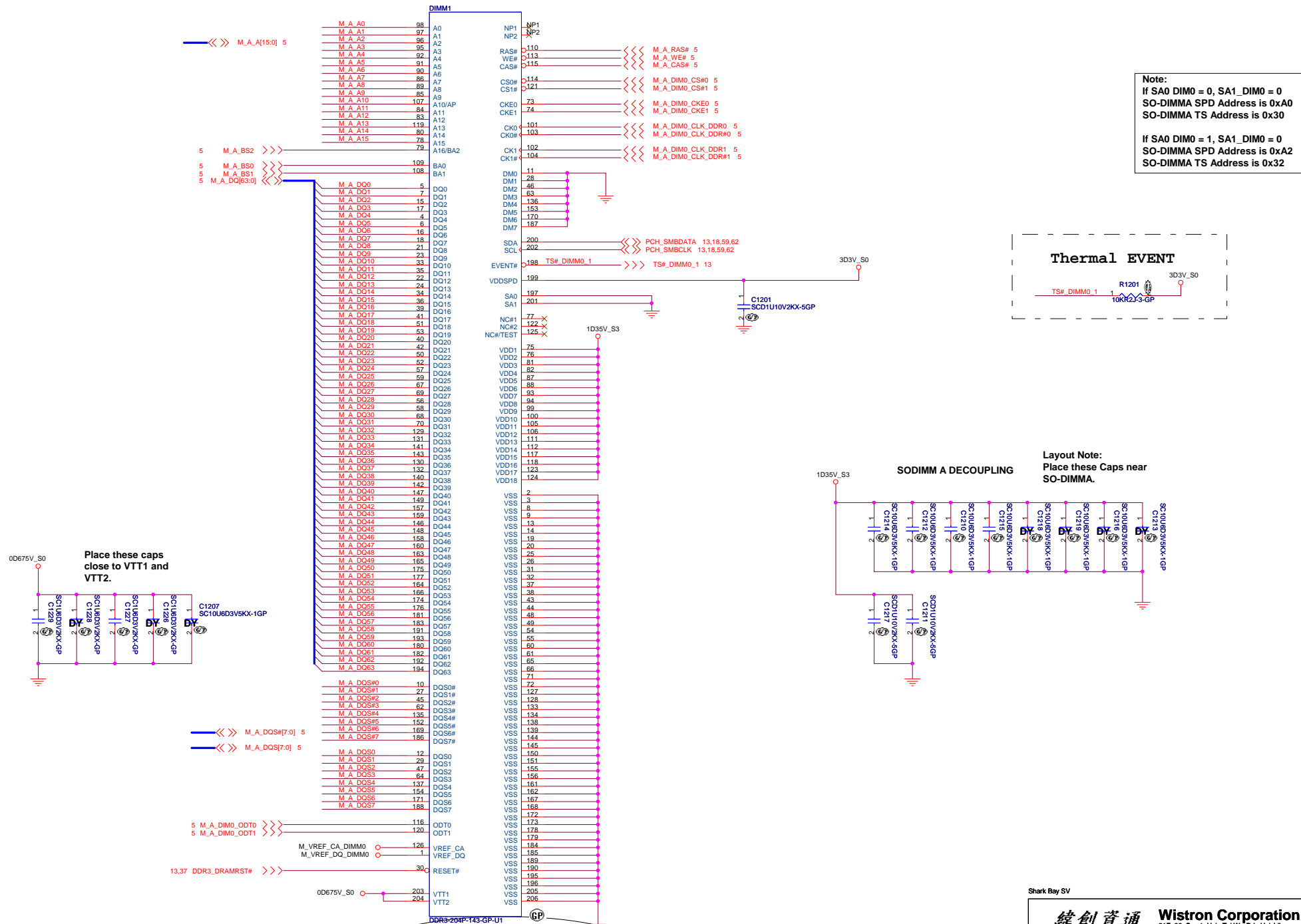


(Reserved)

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Title			
CPU (Power CAP2)			
Size A4	Document Number		Rev
	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013		Sheet 11 of 102

SSID = MEMORY



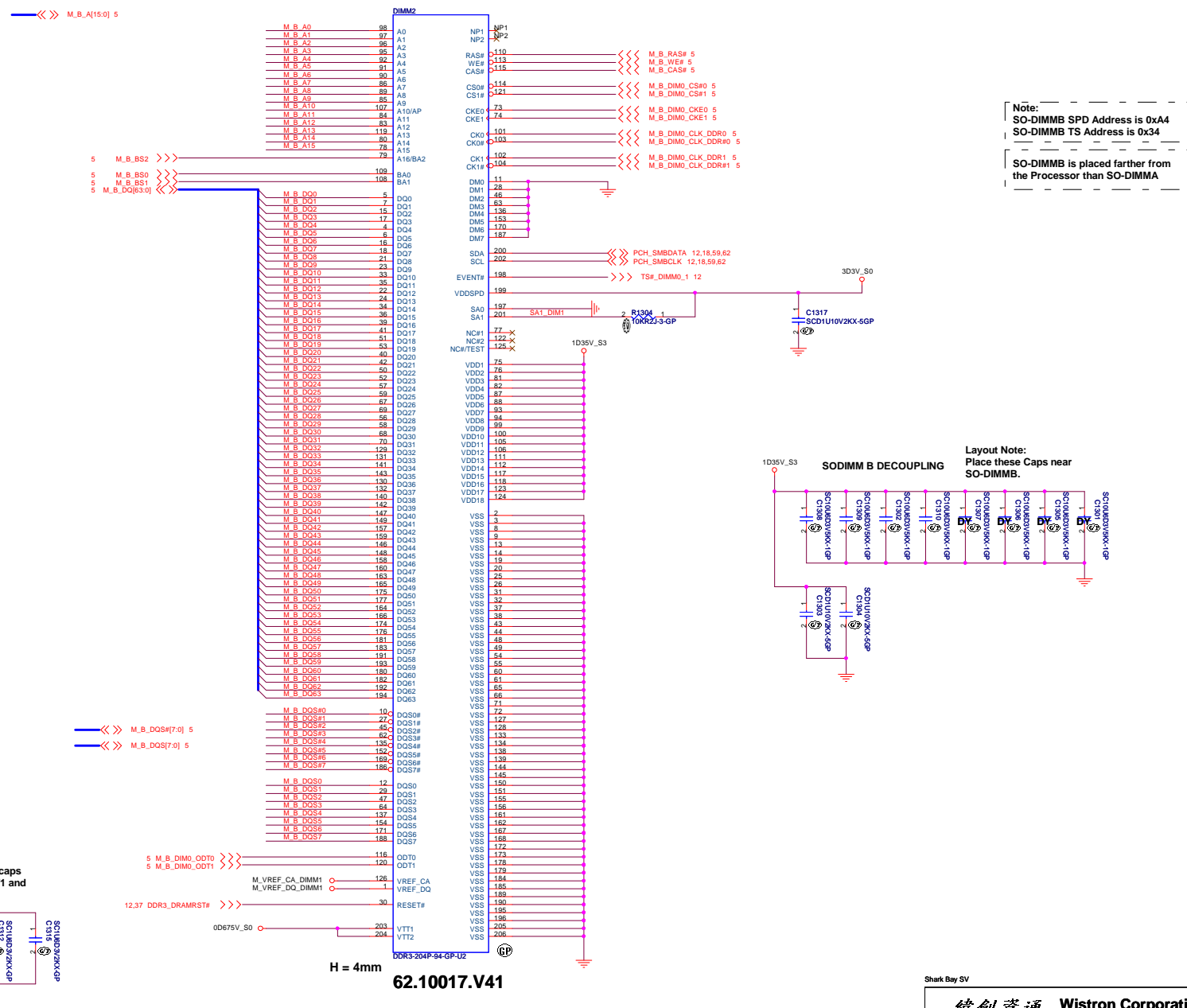
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Title			
DDR3-SODIMM1			
Size	Document Number		Rev
Custom	LOS1 UMA/DIS		SI
Date:	Tuesday, July 16, 2013	Sheet 12 of	102

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near
SO-DIMMB.

Place these caps close to VTT1 and VTT2.

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(Reserved)

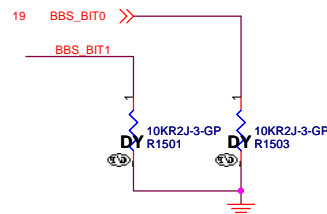
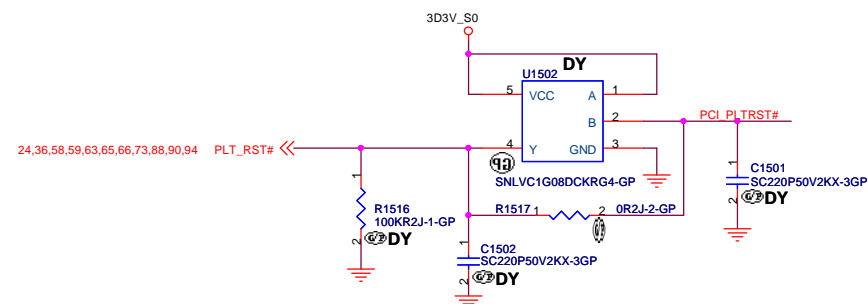
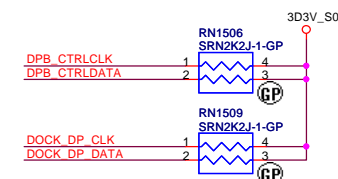
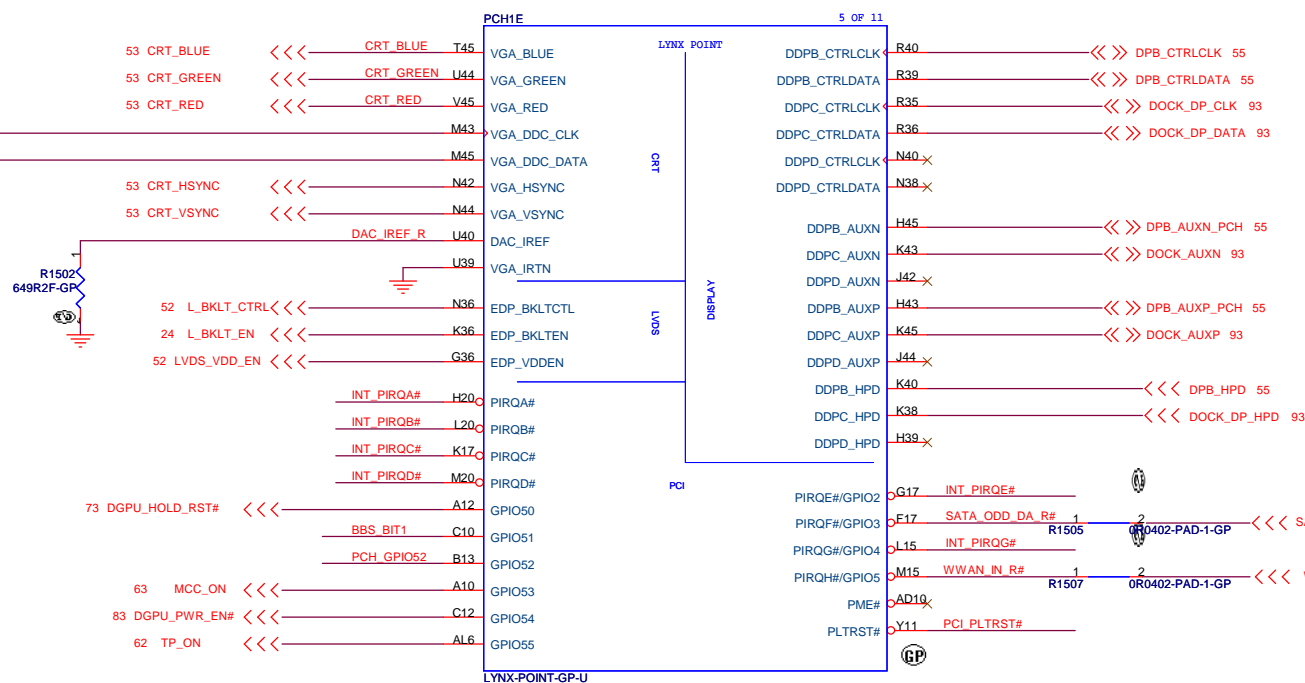
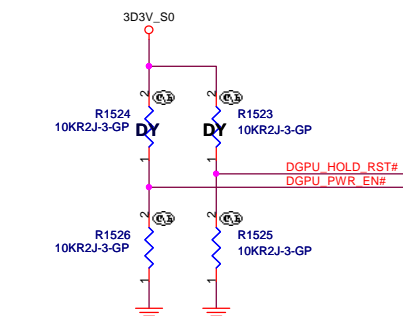
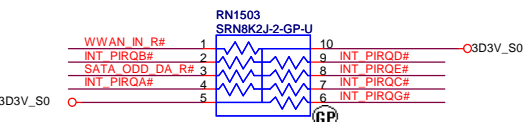
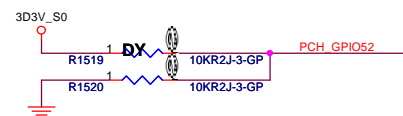
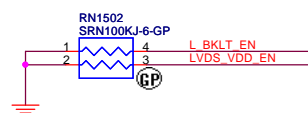
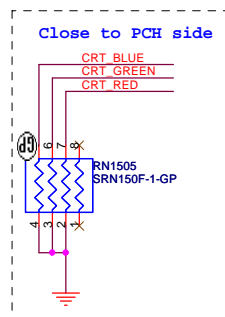
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Title <div>SODIMM3 & SODIMM4</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>14</div> of <div>102</div>

SSID = PCH

DDB: System Mini-DP

DDC: DOcking DP



BOOT BIOS Strap		
GPI051	SATA1GF/GPI019	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Shark Bay SW

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Title

PCH (CRT/DDI/PCI)

Size

Document Number	
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LOS1 UMA/DIS

Rev

Date: Tuesday, July 16, 2013

Sheet 15 of 102

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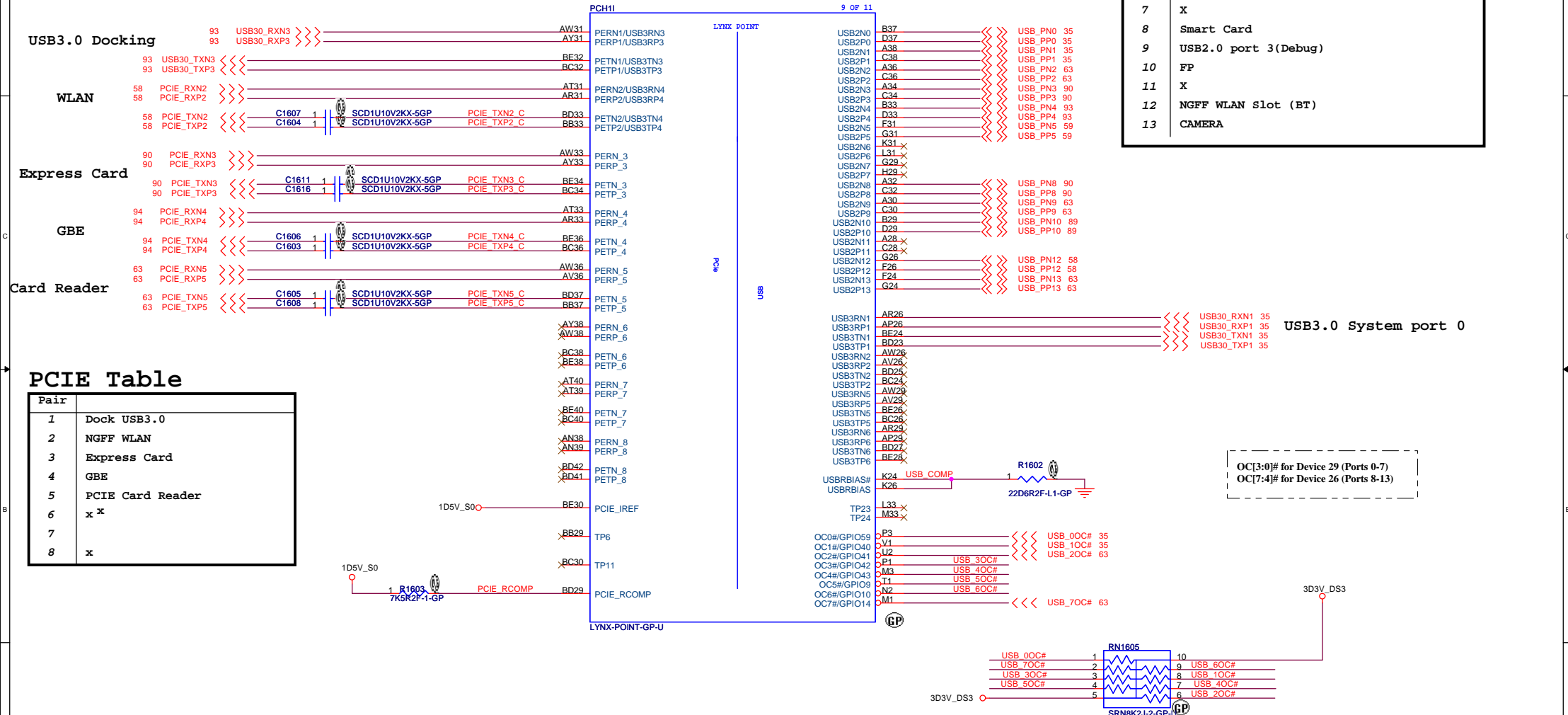
SSID = PCH

USB3.0 Table

Pair	Device
1	USB3.0 System port 0
2	X
3	USB3.0 DOCKING
4	X
5	X
6	X

USB2.0 Table

Pair	Device
0	USB3.0 port 0(AOU)
1	USB2.0 port 1 (OS1 system) (PD1 RJ45 BD)
2	USB2.0 port 2
3	Express Card
4	USB3.0 DOCKING
5	NGFF WWAN
6	X
7	X
8	Smart Card
9	USB2.0 port 3(Debug)
10	FP
11	X
12	NGFF WLAN Slot (BT)
13	CAMERA



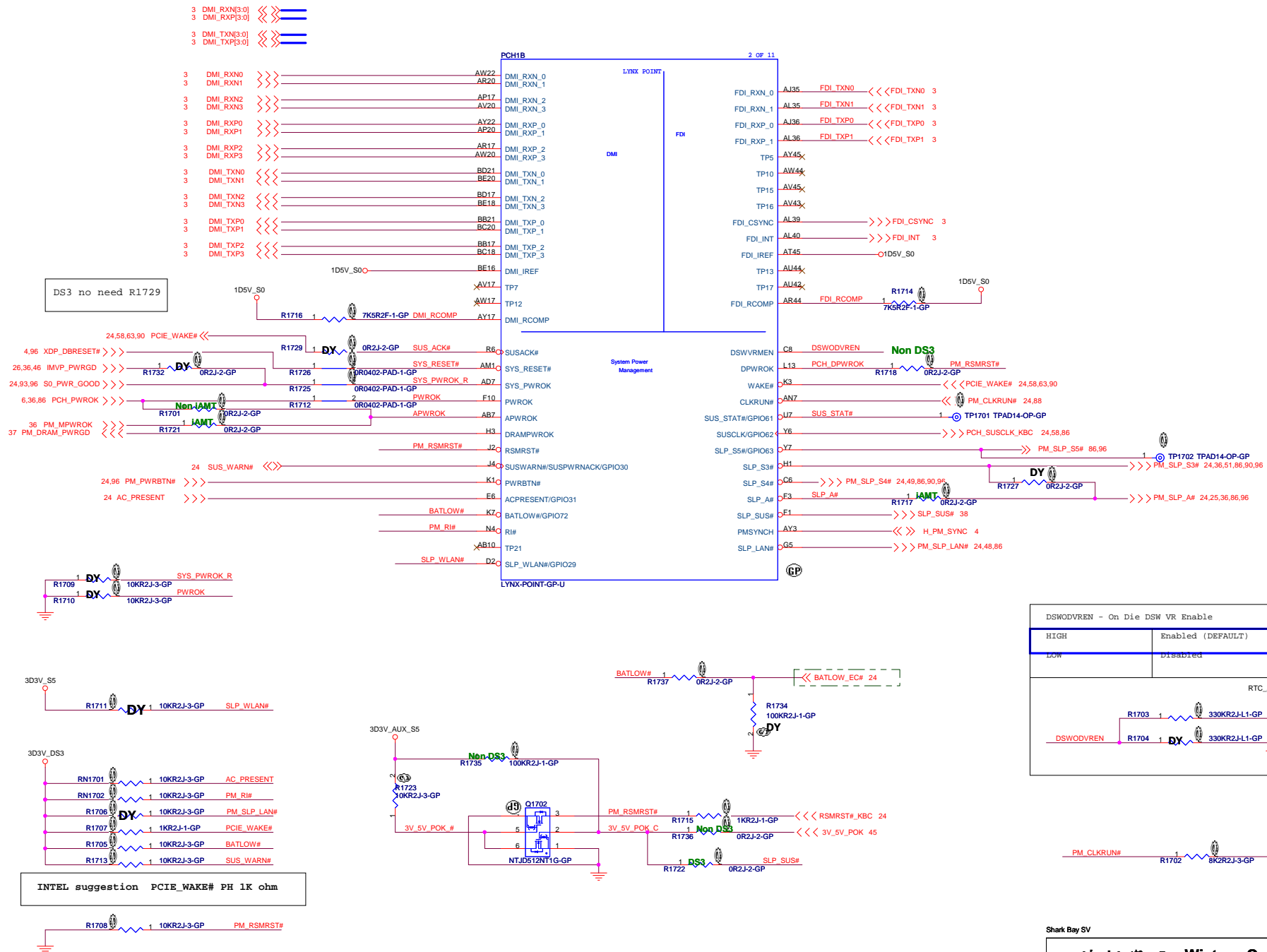
Need to Check

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Title			
PCH (PCIE/USB)			
Size A3	Document Number		Rev
	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013	Sheet 16 of	102

SSID = PCH

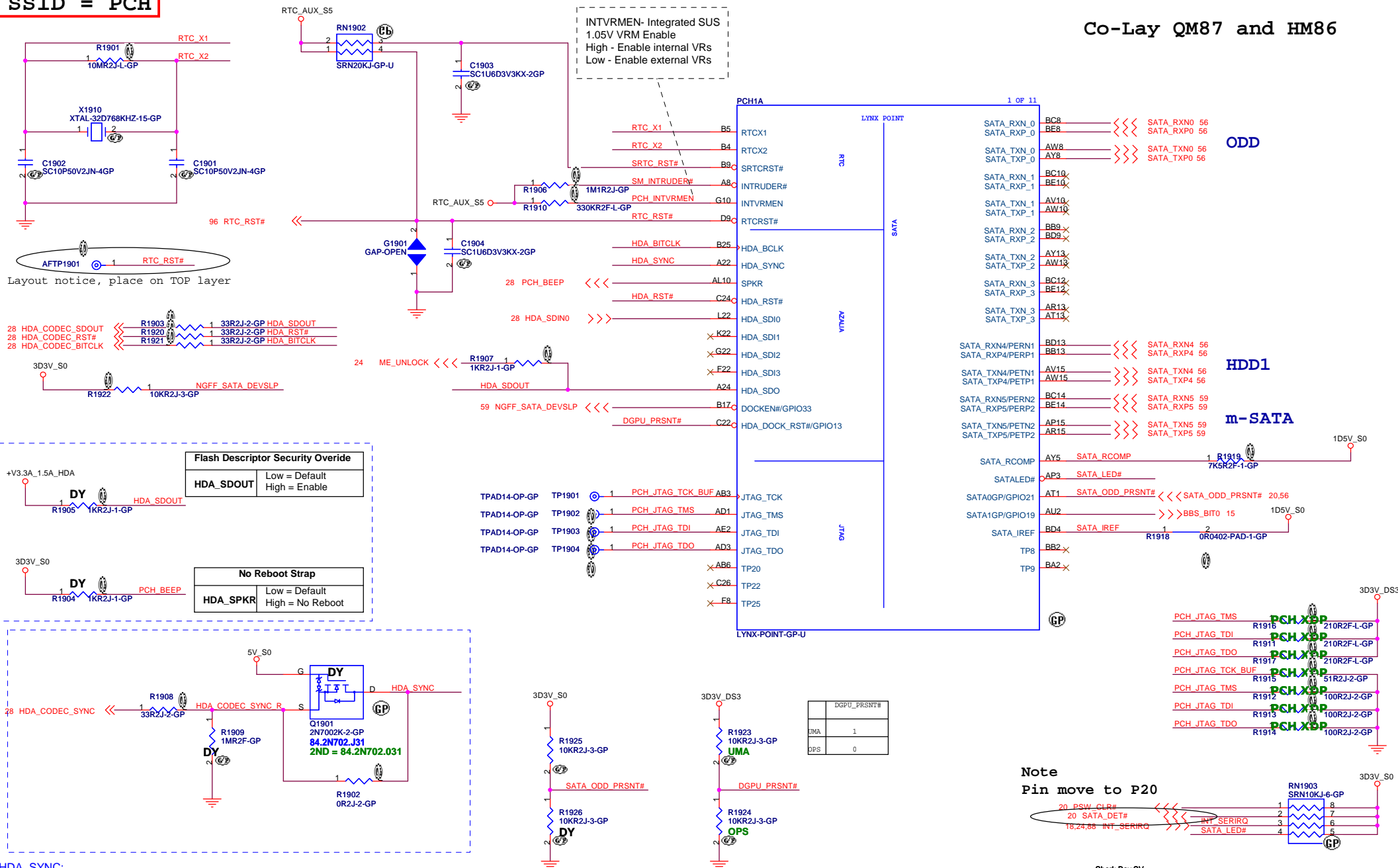


DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram illustrates the connection of the DSWODVREN signal to the RTC_AUX1 pin. The DSWODVREN signal is connected to the R1704 pin of the DSX component. The R1703 pin of the DSX component is connected to the RTC_AUX1 pin through a 330K resistor. The R1704 pin of the DSX component is connected to ground through a 330K resistor.

SSID = PCH

Co-Lay QM87 and HM86



HDA_SYNC:
HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase.

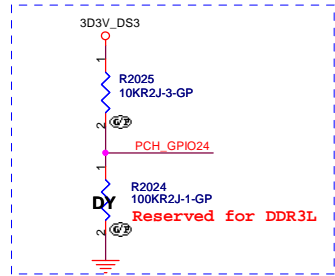
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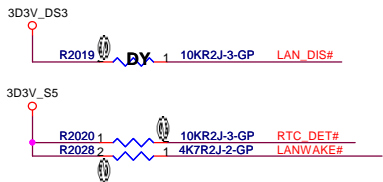
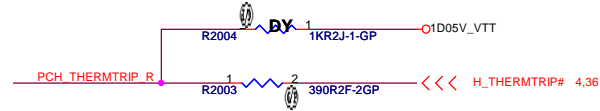
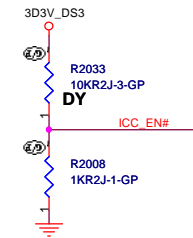
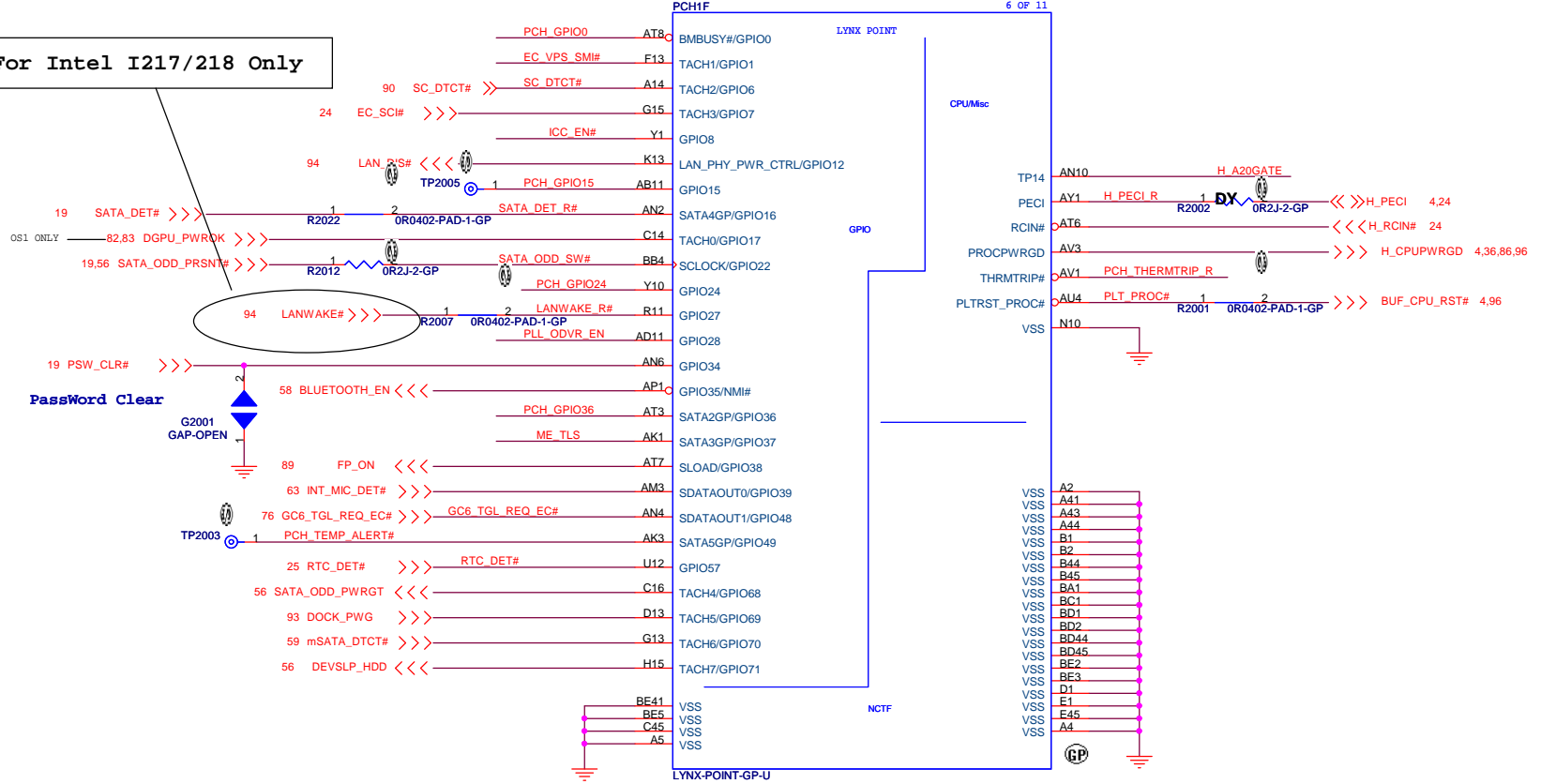
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (RTC/SATA/HDA/JTAG)
Size A3 Document Number: LOS1 UMA/DIS
Date: Tuesday, July 16, 2013 Sheet 19 of 102
Rev -1

SSID = PCH

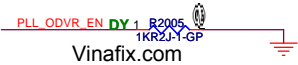


For Intel I217/218 Only



PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2005 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2005 STUFFED)

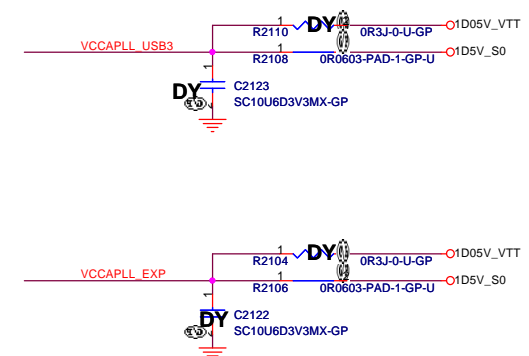
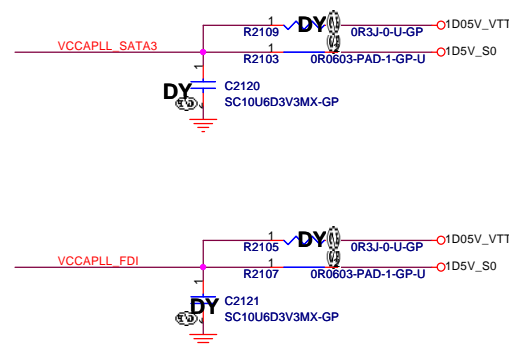
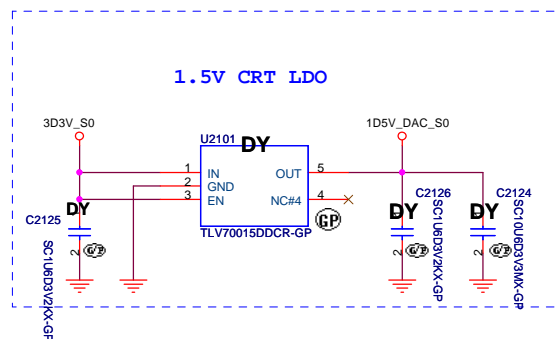
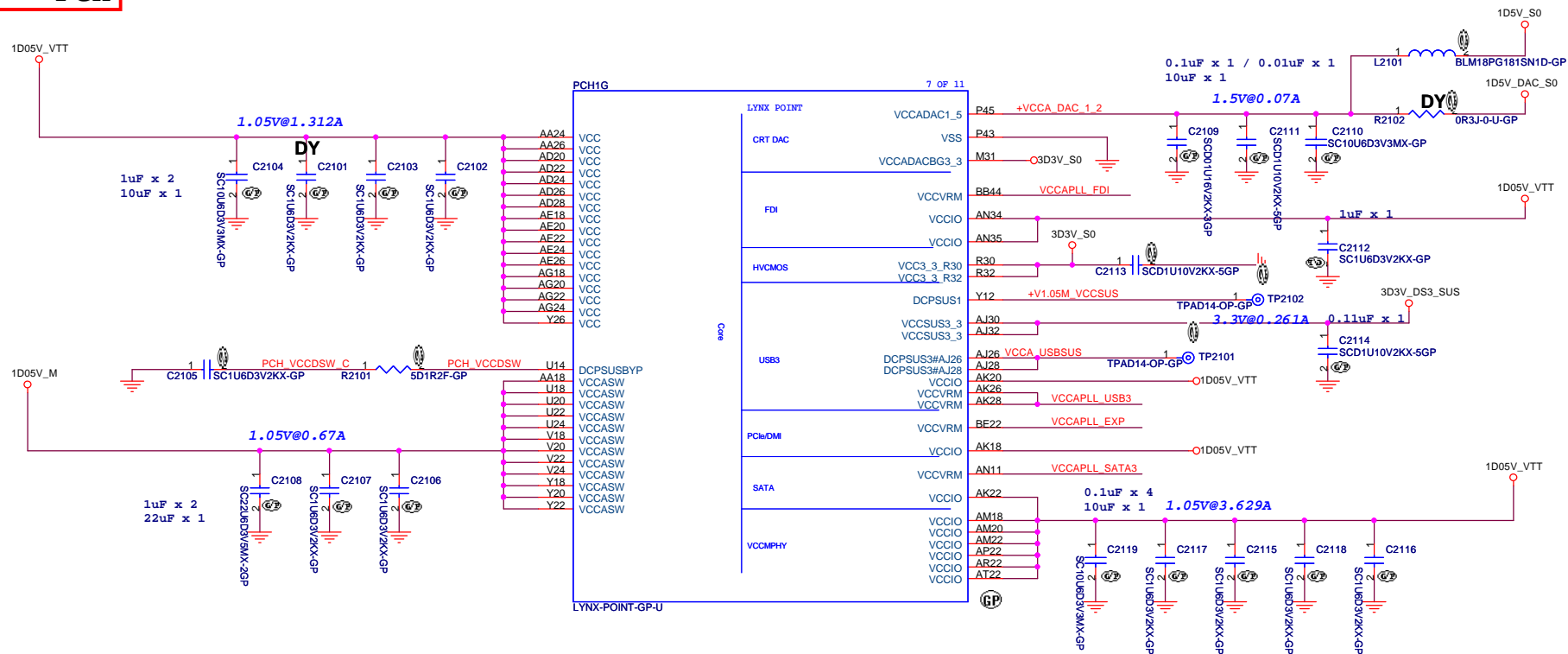


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Title	PCH (GPIO/CPU)		
Size A3	Document Number	Rev -1	
Date: Tuesday, July 16, 2013	Sheet 20	of	102

SSID = PCH

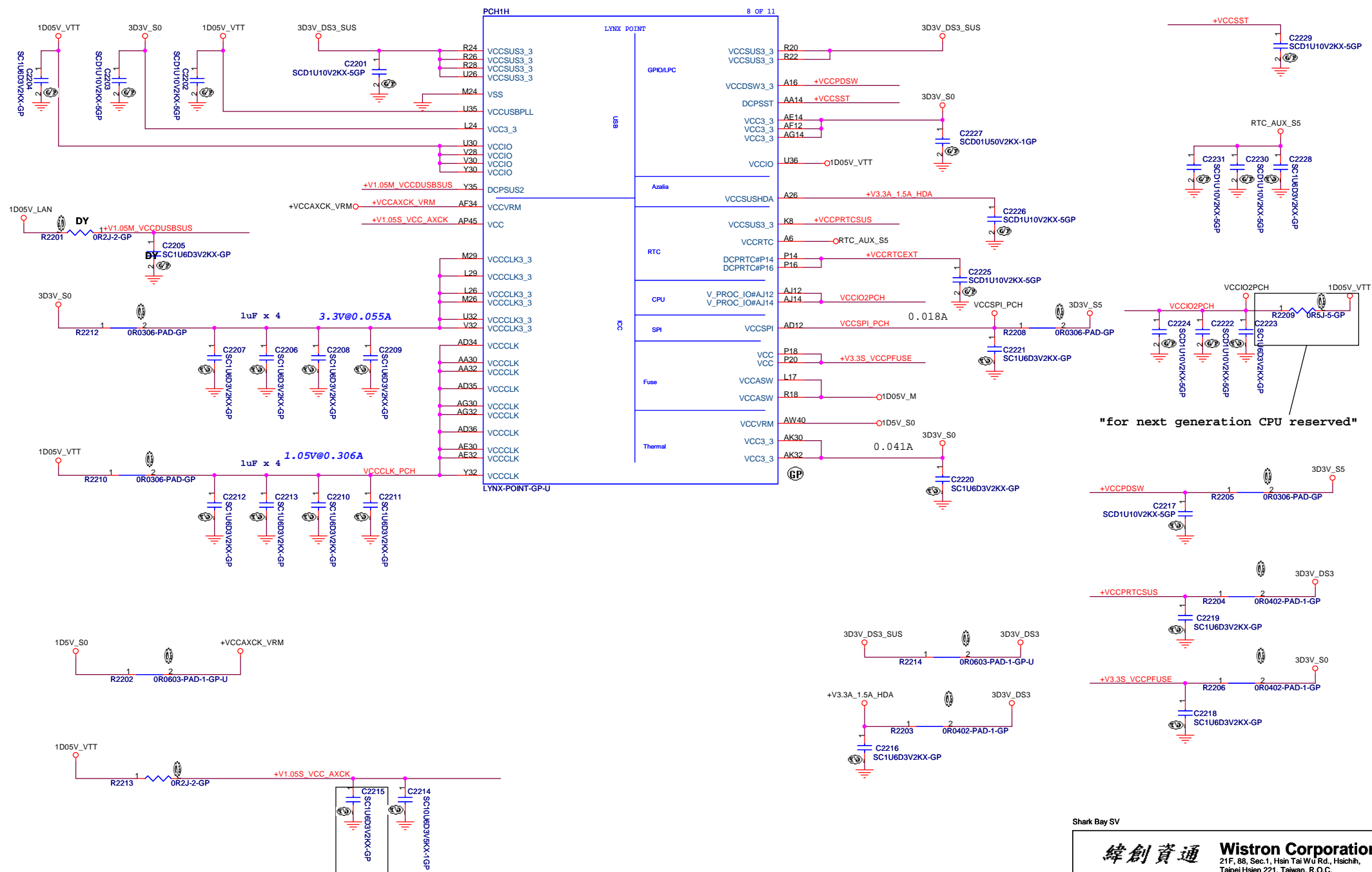


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Title			
PCH (POWER1)			
Size A3	Document Number		Rev
	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013	Sheet 21 of	102

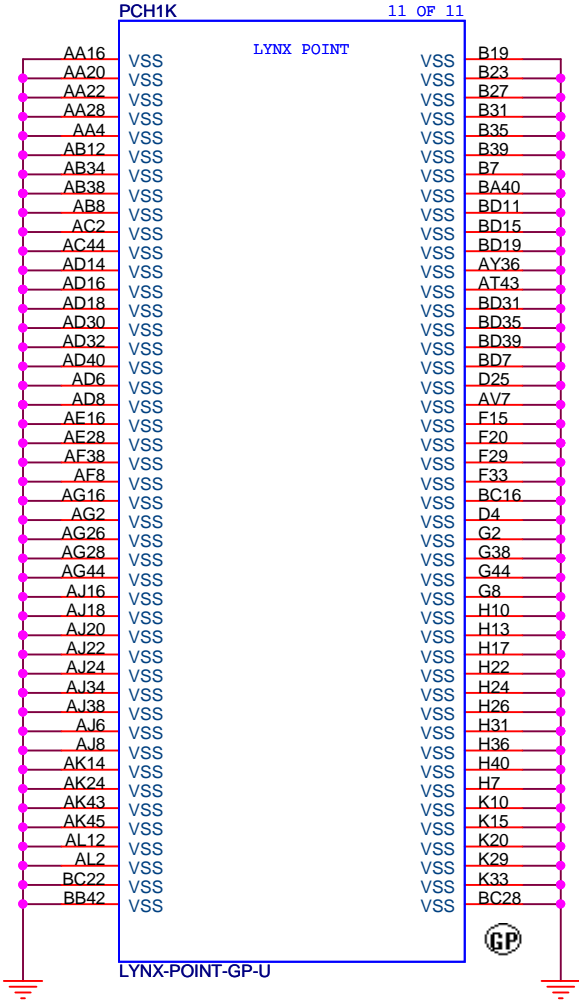
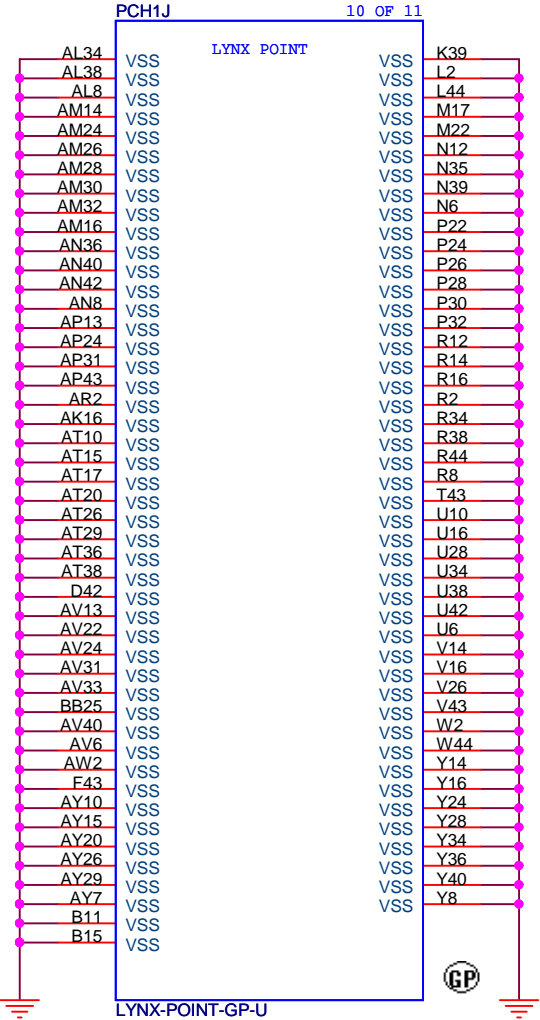
SSID = PCH



C2215 should be close PCH

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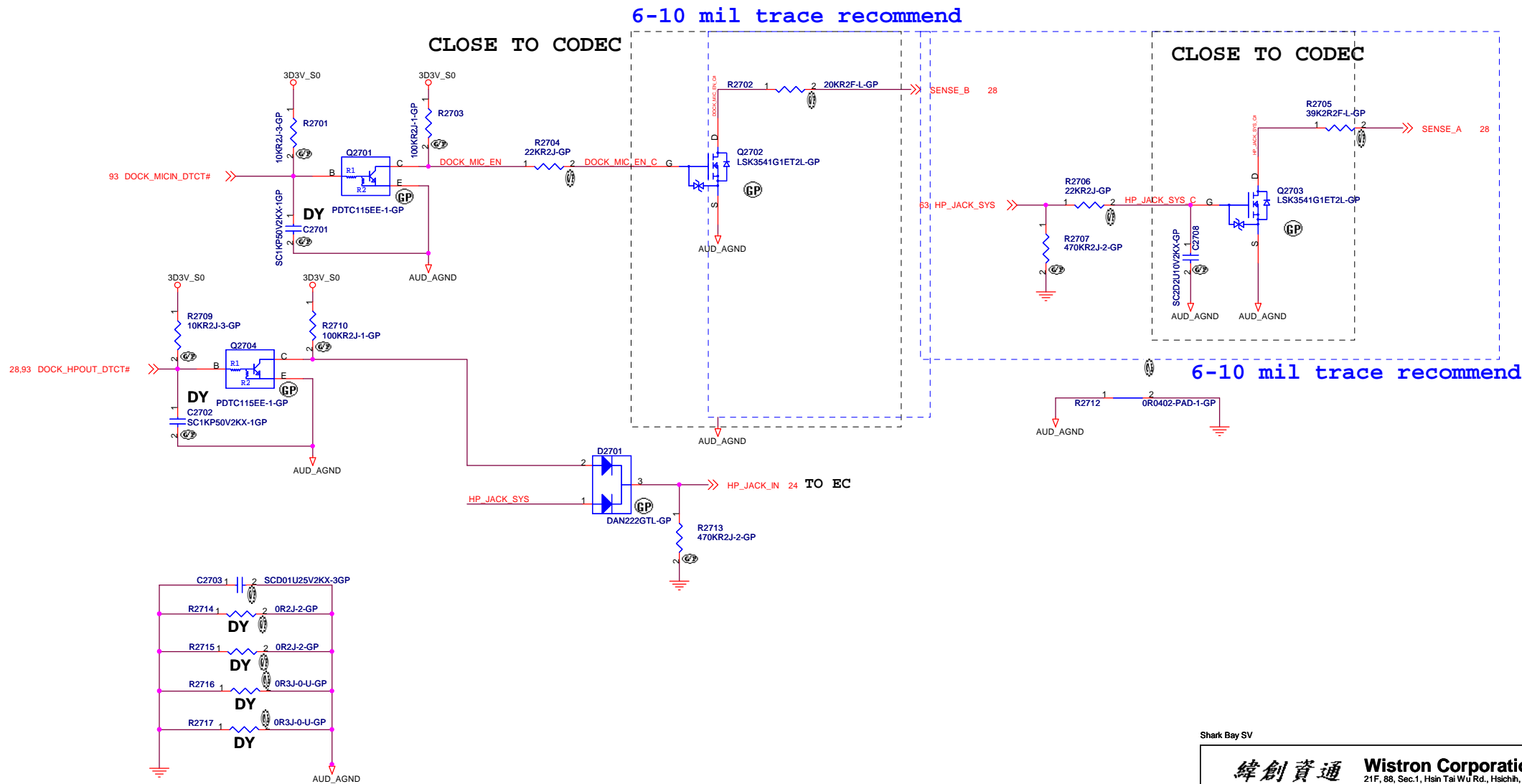
SSID = PCH



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Title		
PCH (VSS)		
Size	Document Number	Rev
A4	LOS1 UMA/DIS	-1
Date:	Tuesday, July 16, 2013	Sheet 23 of 102



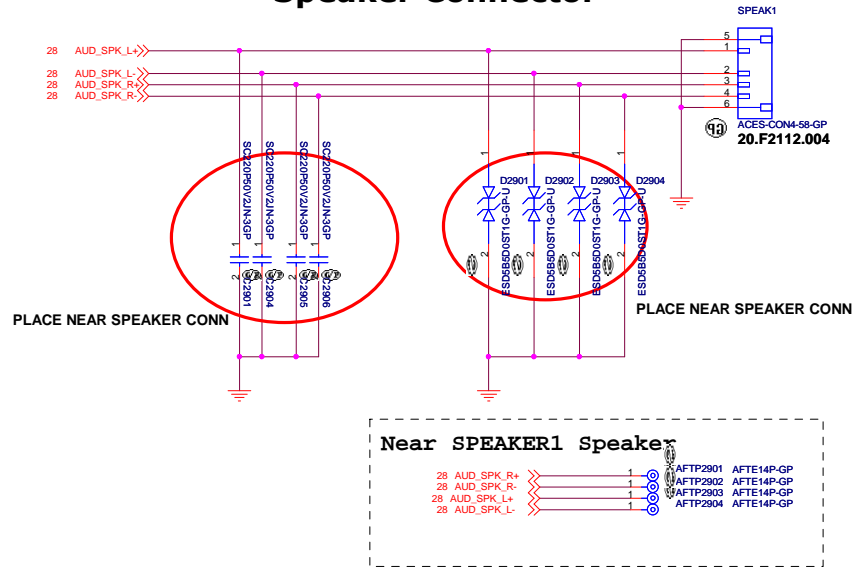
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Audio Jack Sense			
Size	Document Number	Rev	
Custom	LOS1 UMA/DIS	-1	
Date:	Tuesday, July 16, 2013	Sheet	27 of 102

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SSID = AUDIO

Speaker Connector




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Title		
SPEAKER/COMBO JACK		
Size	Document Number	Rev
Custom	LOS1 UMA/DIS	SD
Date	Tuesday, July 16, 2013	Sheet 29 of 102

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Title			
LAN RTL8111G			
Size	Document Number		Rev
Custom	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013		Sheet 30 of 102

D

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Title		
RJ45+Transformer		
Size	Document Number	Rev
A4	LOS1 UMA/DIS	SD
Date:	Tuesday, July 16, 2013	Sheet 31 of 102

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Wistron Corporation

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Title

MEDIA CARD CONTROLLER

Size
A3

Document Number

LOS1 UMA/DIS

Rev
-1

Date: Tuesday, July 16, 2013

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5

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(Blanking)

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Title <div>CARD Reader</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>33</div> of <div>102</div>

5

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D

C

C

B

B

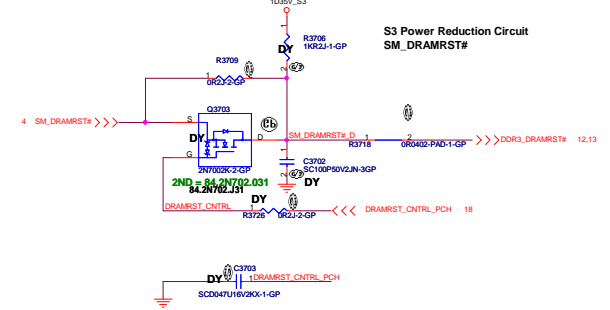
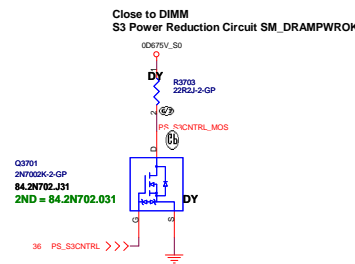
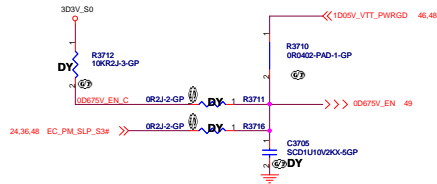
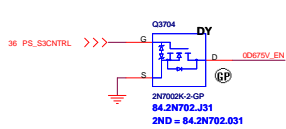
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A

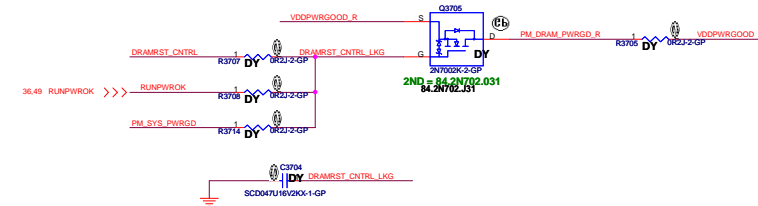
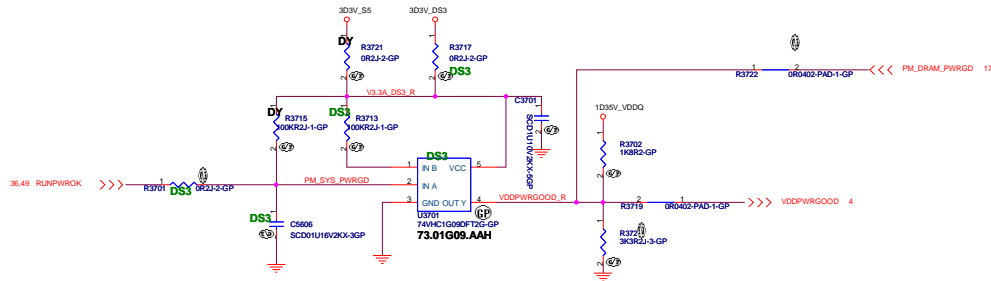
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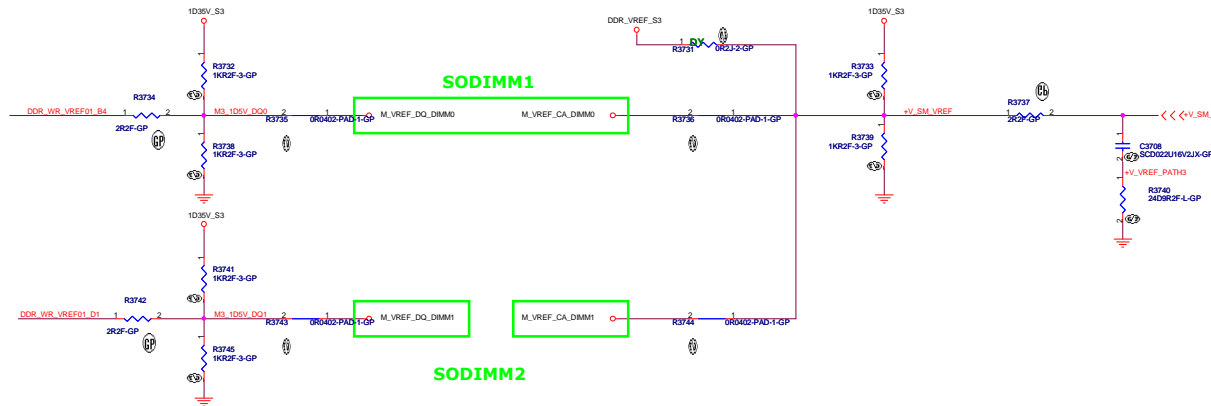
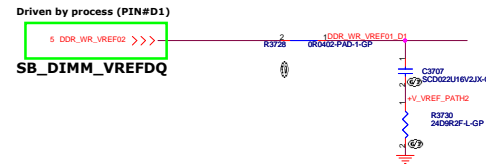
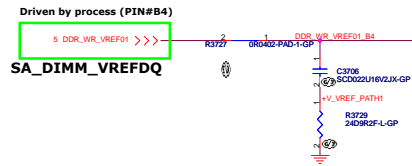
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>USB2.0 & 3.0 CONN</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>	Sheet <div>34</div>	of <div>102</div>

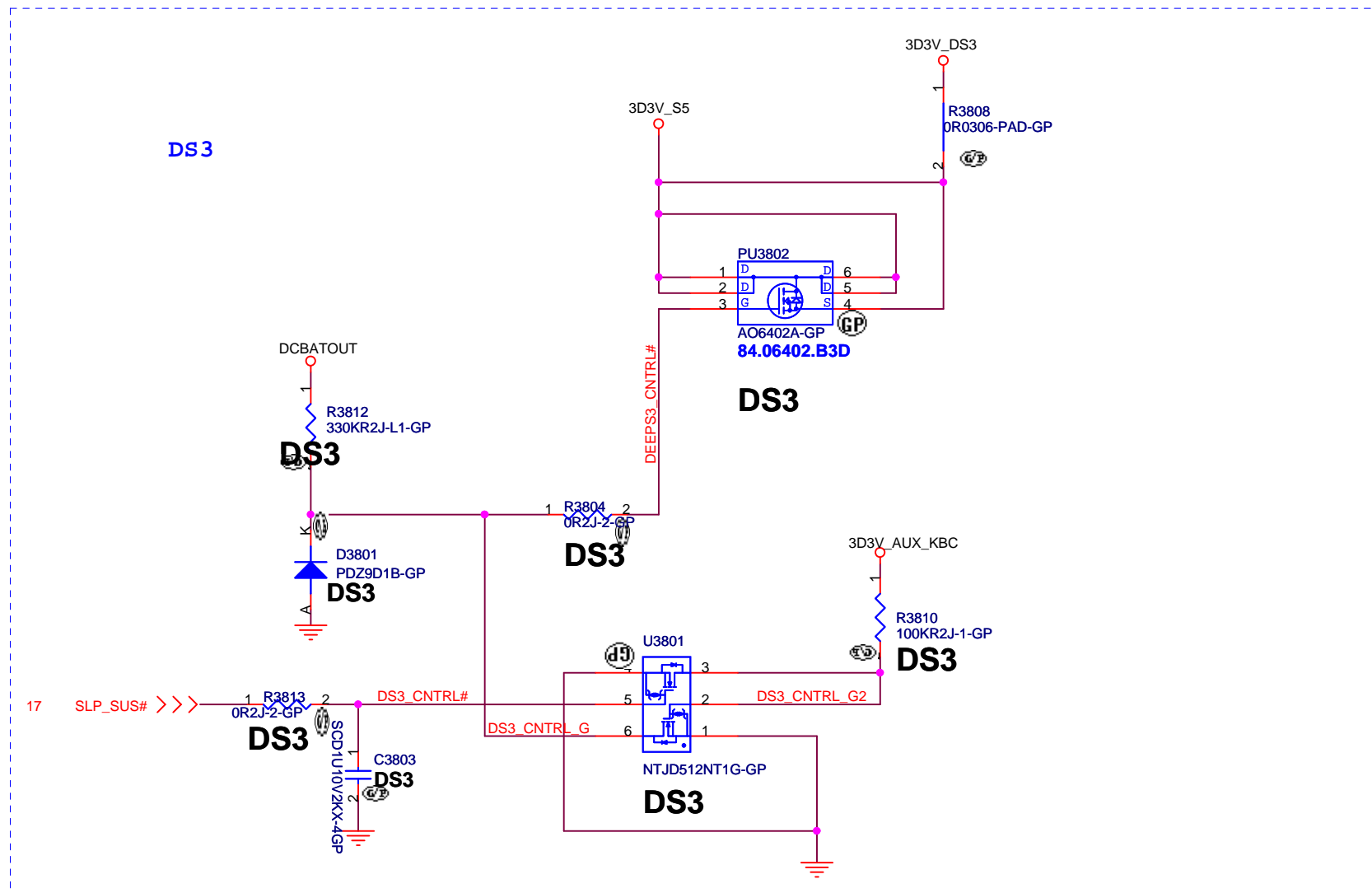


Close to CPU
SM_DRAMPWROK Topology for platforms supporting Deep S3



VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation





Shark Bay SV

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Deep S3 Power

Size
A4

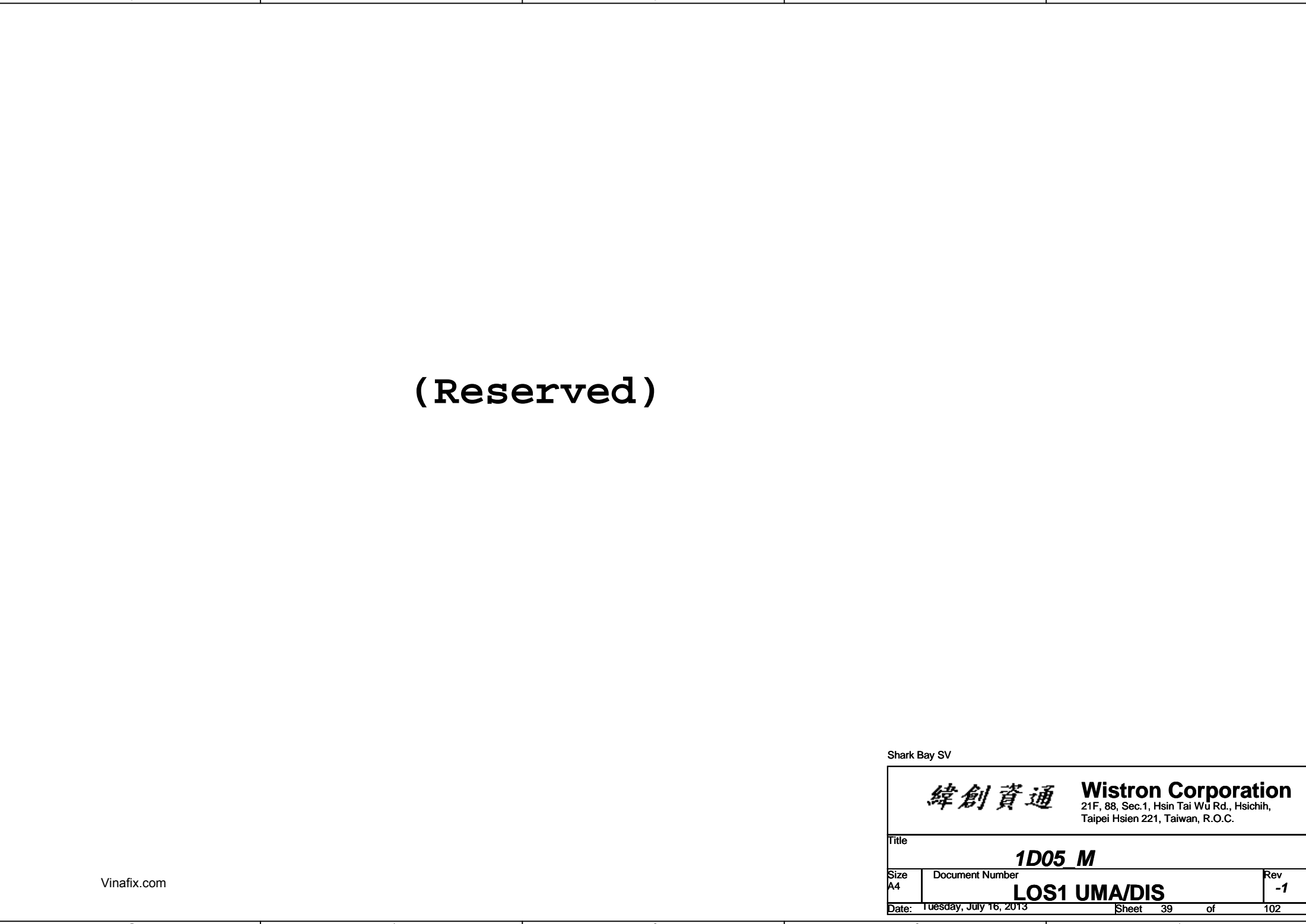
Document Number

LOS1 UMA/DIS


Rev
-1

Date: Tuesday, July 16, 2013

Sheet 38 of 102

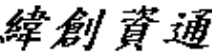


Shark Bay SV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05 M			
Size A4	Document Number LOS1 UMA/DIS		Rev -1
Date: Tuesday, July 16, 2013	Sheet	39	of 102

(Reserved)

Shark Bay SV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby(1/2)			
Size A4	Document Number LOS1 UMA/DIS		Rev -1
Date: Tuesday, July 16, 2013	Sheet	40	of 102

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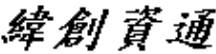
B

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(Reserved)

Shark Bay SV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby(2/2)			
Size A4	Document Number		Rev -1
LOS1 UMA/DIS			
Date: Tuesday, July 16, 2013	Sheet	41	of 102

AC ADT	ACDC_ID	#65W_AC	#90W_AC	System Power Limit
130W	$1.663V < ID \leq 2.109V$	L	L	90W
90W	$1.172V < ID < 1.618V$	L	L	90W
65W	$0.693V < ID \leq 1.134V$	L	H	65W
45W	$0.234V < ID \leq 0.663V$	H	H	45W

Note
have extraneous cost impact

Need to connect to KBC

to KBC/DOCK/Charger

45W: 1.7V
65W: 3.3V

This Cap should be placed close PU4201
.Source and Gate as possible.

Enlarge this trace to 8mil or more if possible.
To reduce the trace inductance

10/17 PC3802 Need change to 78.47424.21L in SIT
Confirm with PWR team

44.93 DOCKED0# >>>
UnDocked--> DOCKED0# = AD_JK_F
Docked --> DOCKED0# = 0V

to DOCK

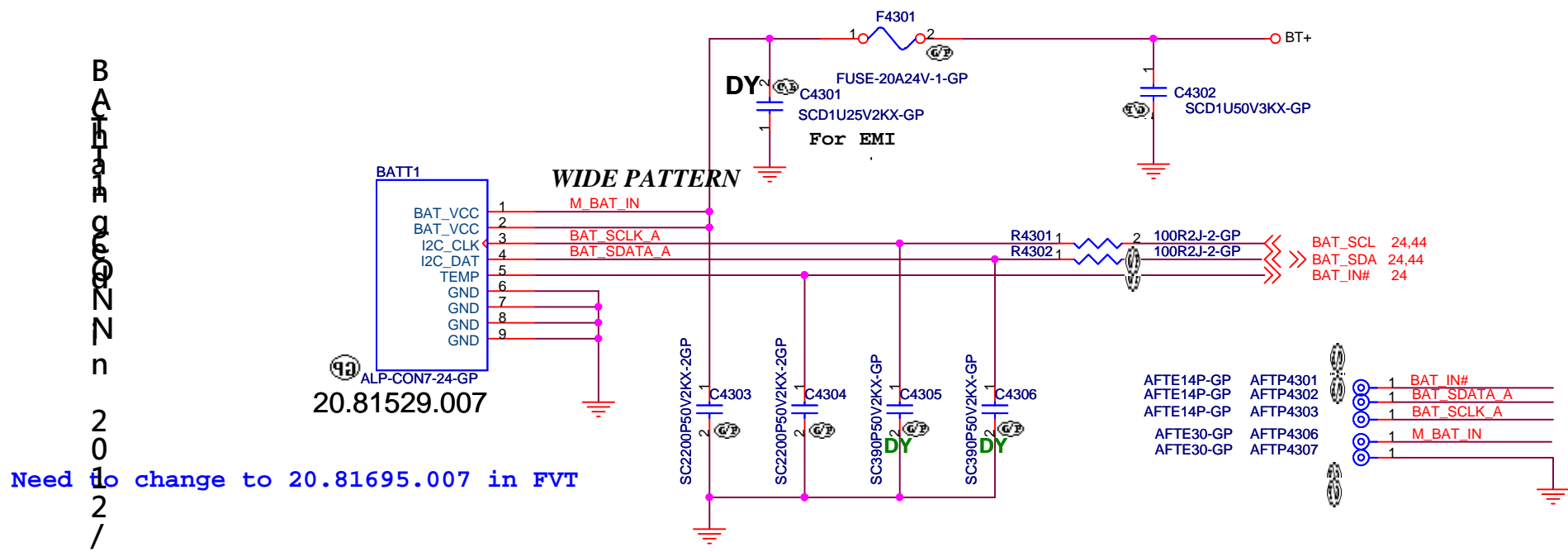
PLACE NEAR CONNECTOR

Shark Bay SV

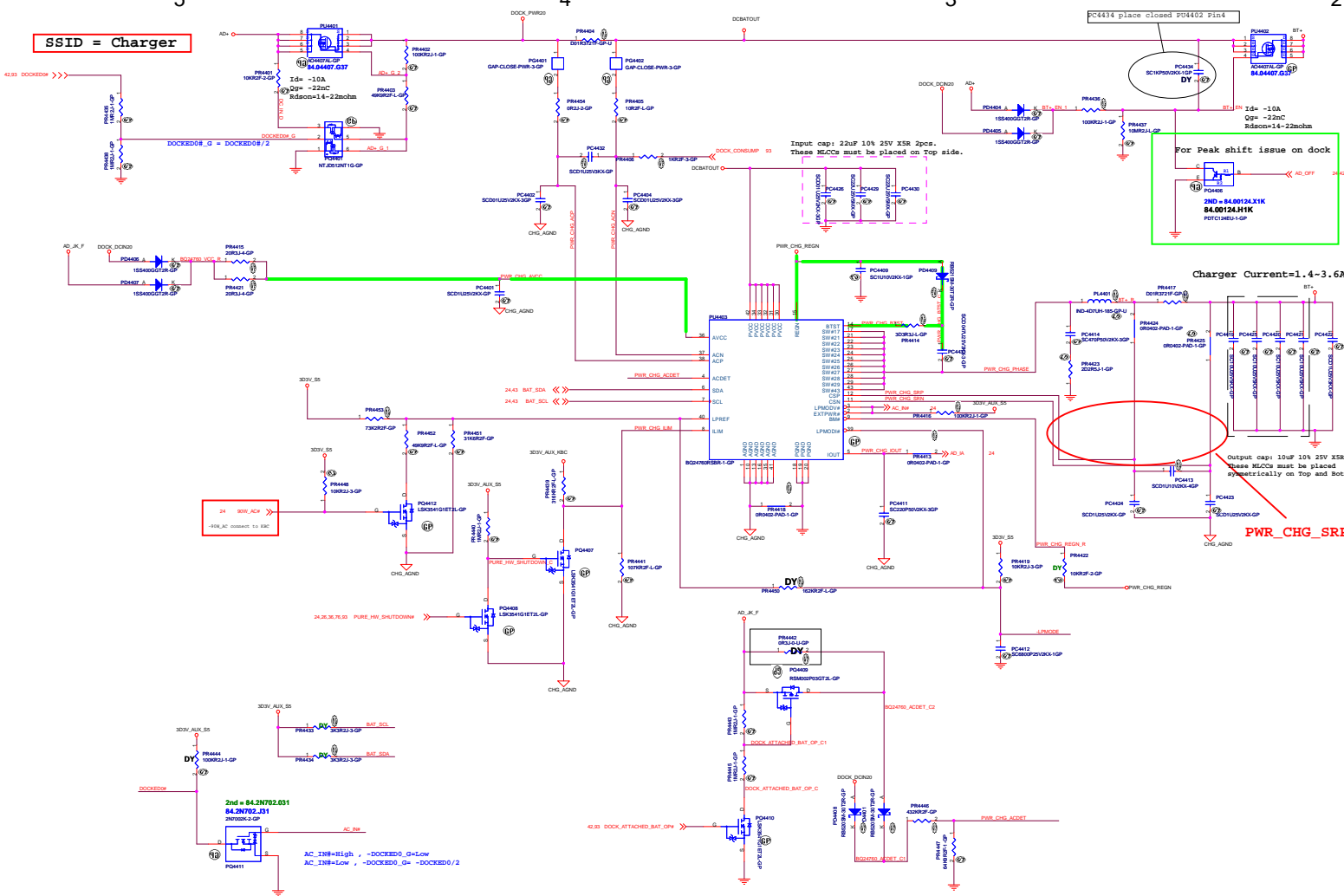
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DCIN JACK			
Size	Document Number	Rev	
Custom	LOS1 UMA/DIS	-1	
Date:	Tuesday, July 16, 2013	Sheet	42 of 102

BATT Connector

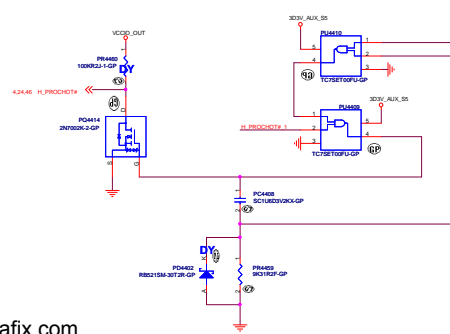


SSID = Charger



Protect circuit for Intel Recommendations

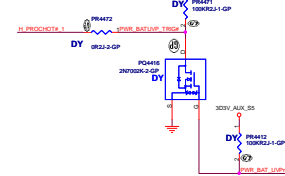
10ms One-shot circuit



for AC over current



for DC Low Voltage



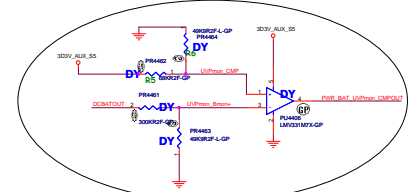
11/24 add the POWER schematic back

Battery	V _{IN}	R ₅	R ₆
6 Cell	10V	58K	49.9K
4 Cell	13V	38.3K	49.9K

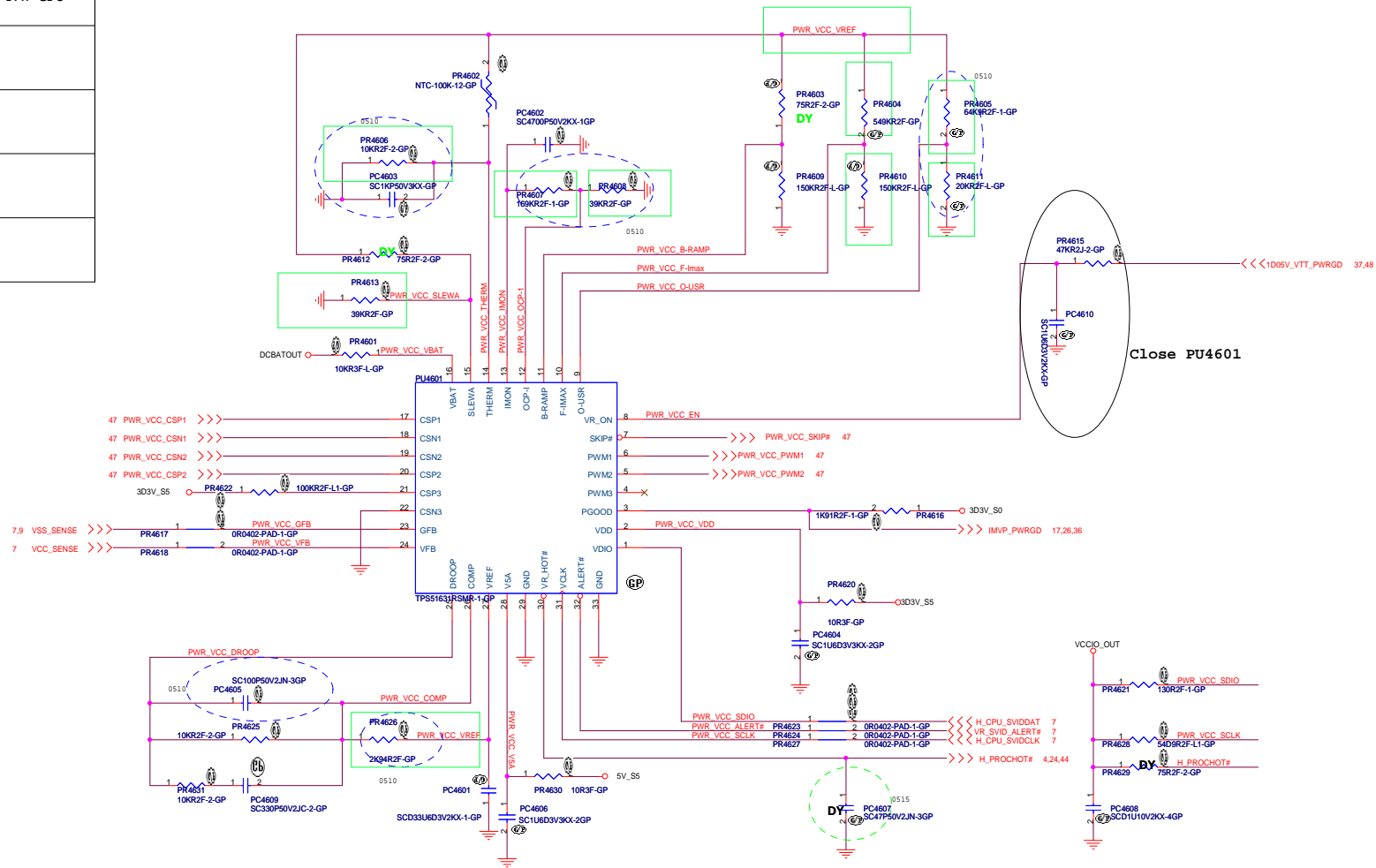
Vinafx.com

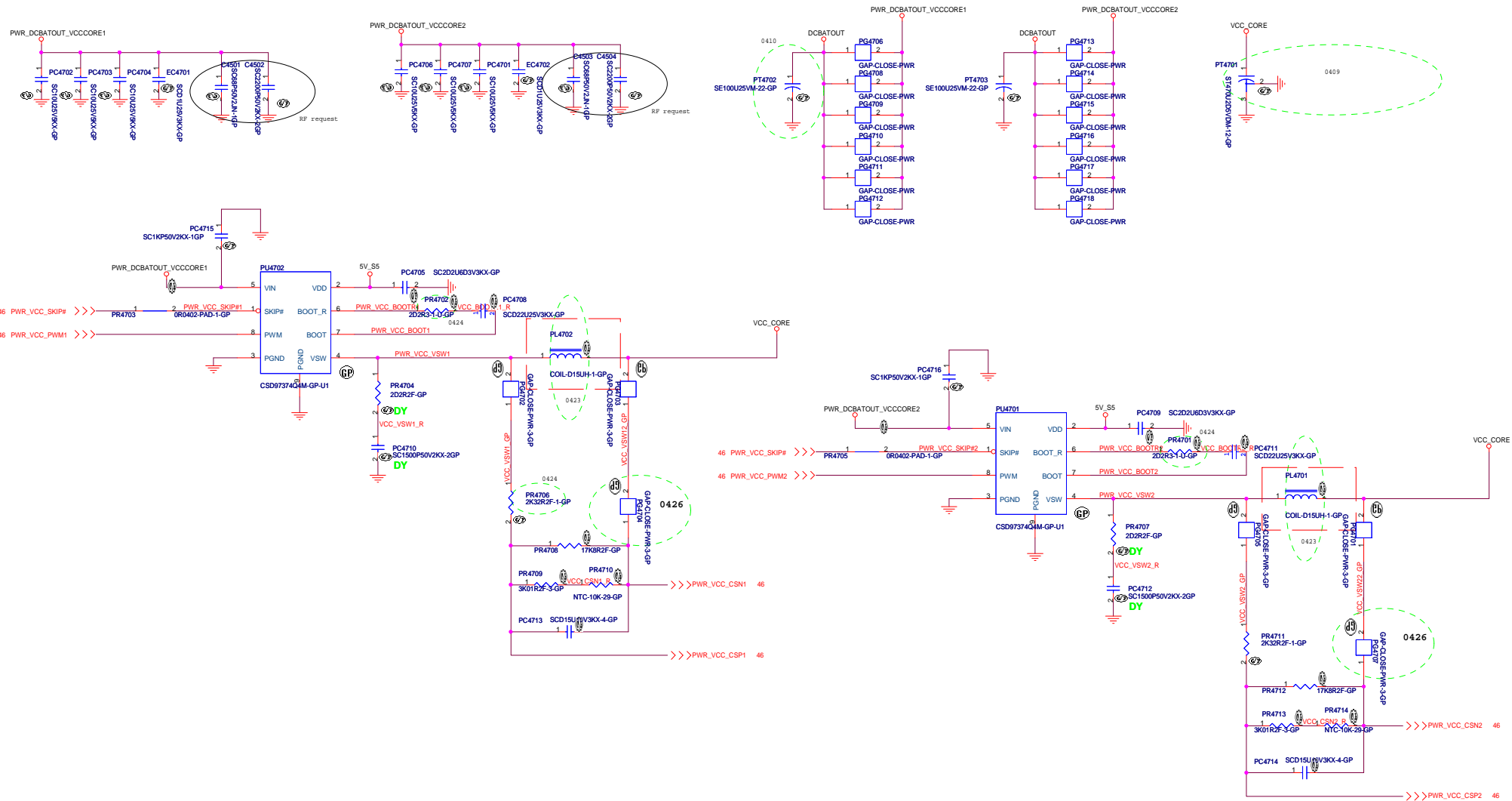
- 20A=800mils or Copper Shape
- 10A=400mils or Copper Shape
- 7A=280mils or Copper Shape
- 4A=160mils or Copper Shape
- 1A= 40mils
- 0.5A= 20mils
- Others = 10mils

DUMMY

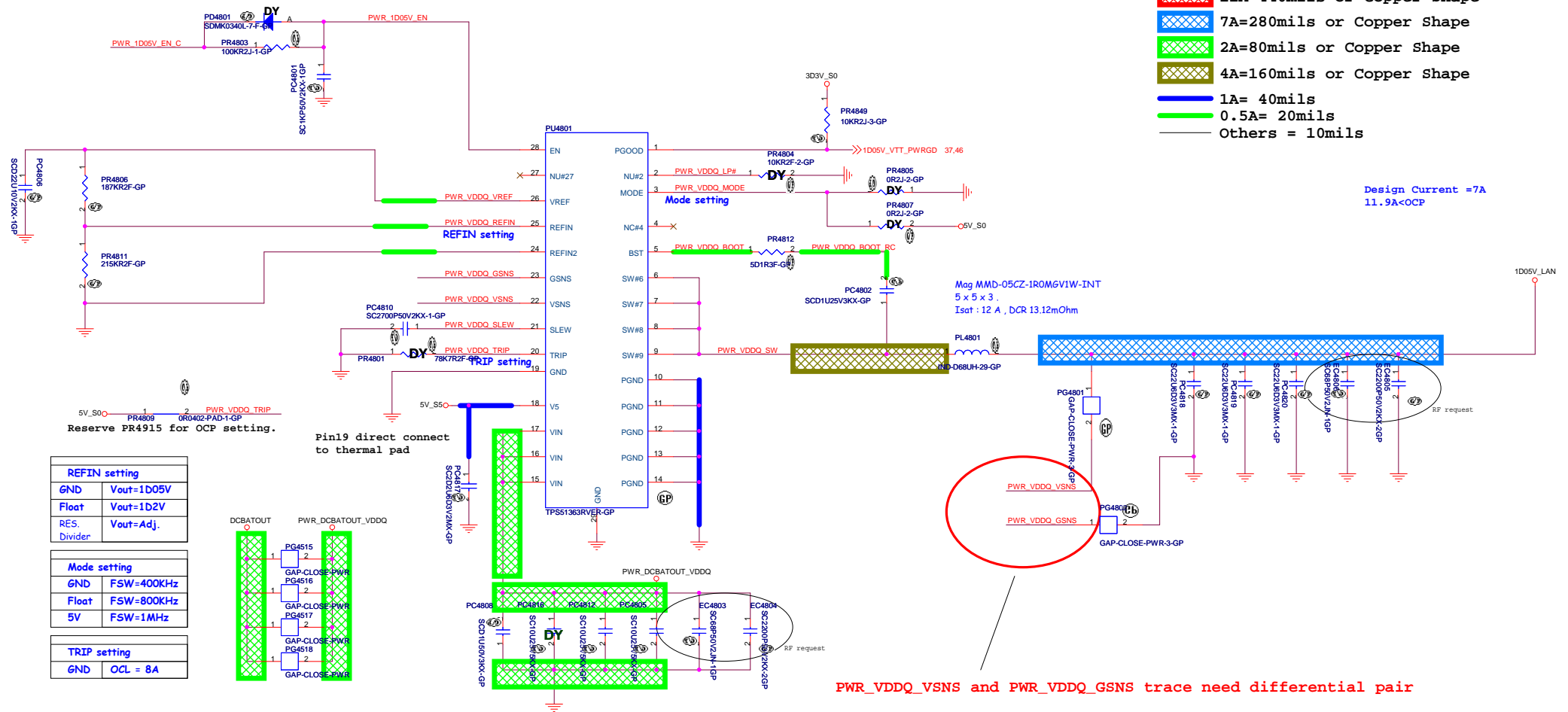
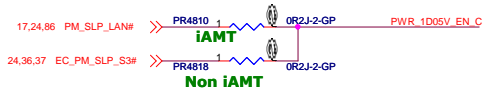


	37W CPU	47W CPU
PR4607	64.17835.6DL 178K	
PR4605	64.48735.6DL 487K	
PR4604	64.54935.6DL 549K	
PR4608	64.39025.6DL 39K	





```
SSID = PWR.Plane.Regulator_1p05v
```

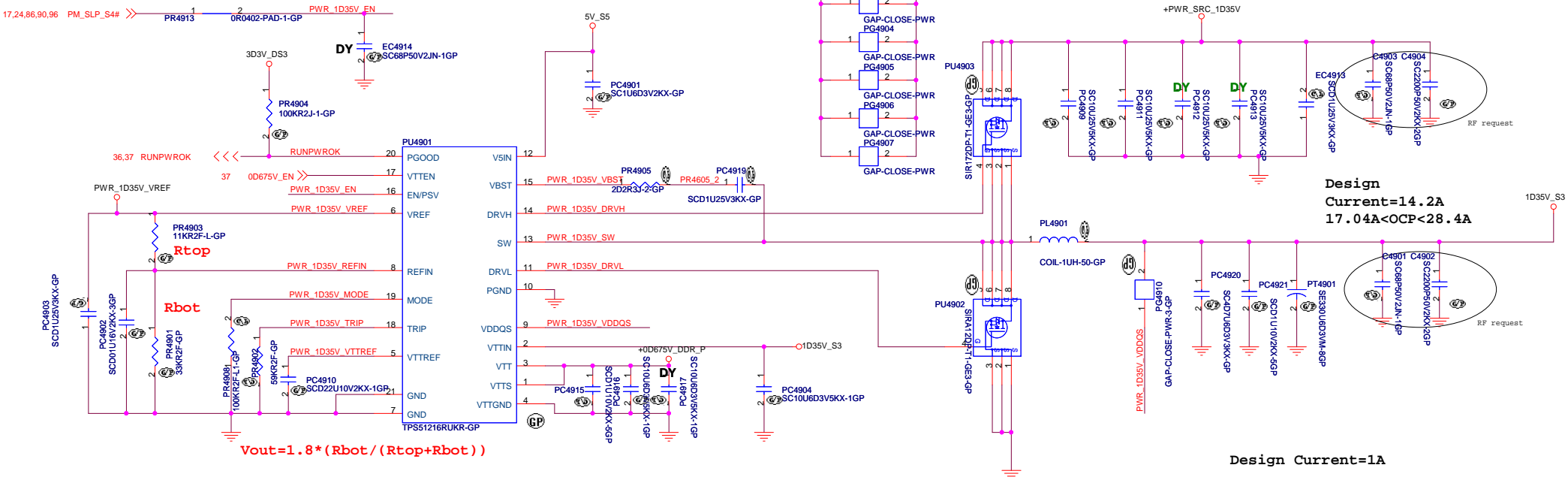


REFIN setting	
GND	Vout=1D05V
Float	Vout=1D2V
RES. Divider	Vout=Adj.

Mode setting	
GND	FSW=400KHz
Float	FSW=800KHz
5V	FSW=1MHz

TRIP setting	
GND	OCL = 8A

SSID = PWR.Plane.Regulator lp35v0p675v



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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TPS51216 1.35V/0.675V			
Size	Document Number	Rev	
Custom		SD	
LOS1 UMA/DIS			
Date:	Tuesday, July 16, 2013	Sheet	49 of 102

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D8V_S0			
Size	Document Number		Rev
A4	LOS1 UMA/DIS		-1
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For p83 VRAM+PCH

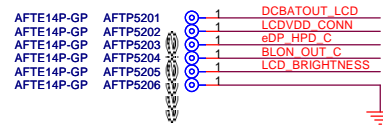
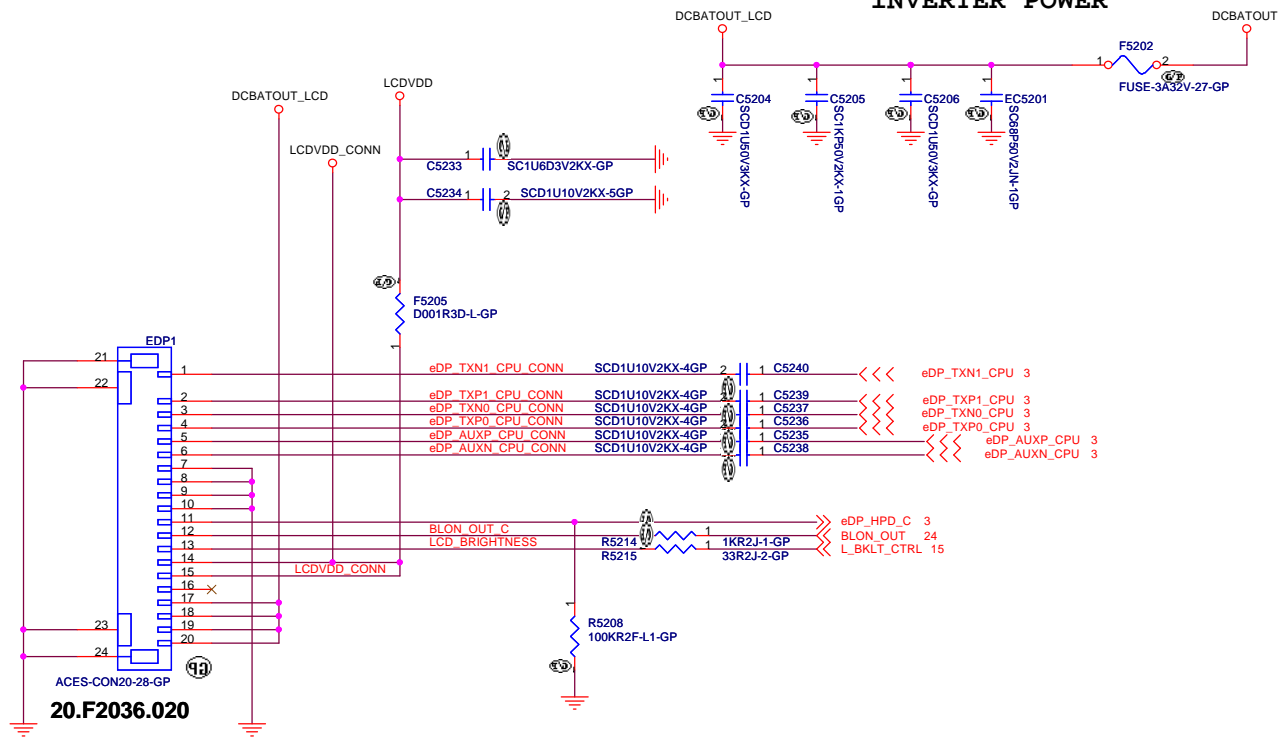
1.5V FOR GPU/GDDR3 ONLY



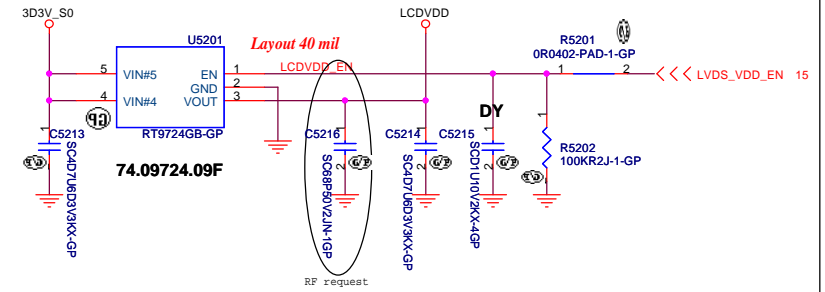
OS1 Only

$$V_{out} = 0.704V * (R1 + R2) / R2$$

INVERTER POWER



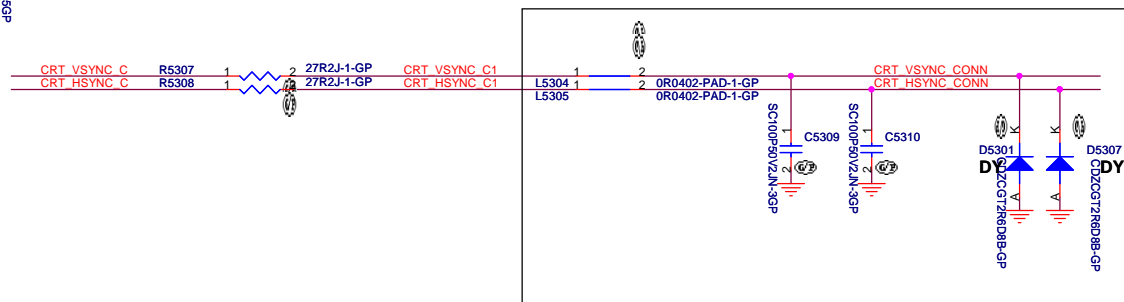
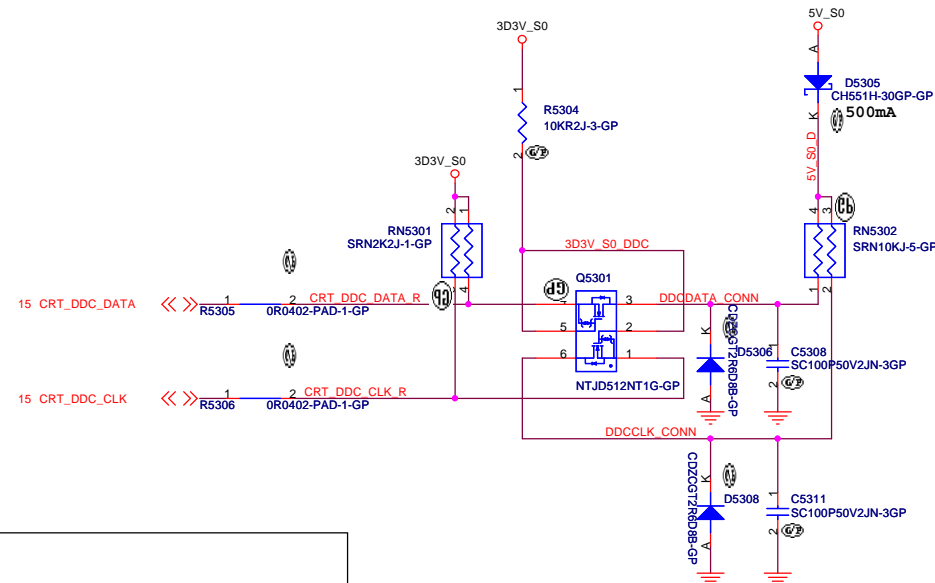
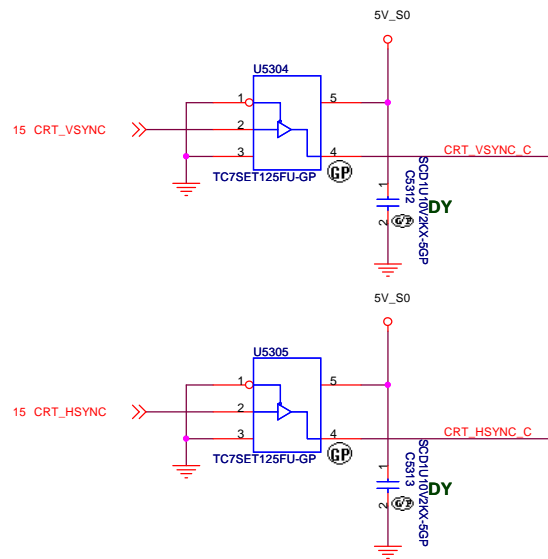
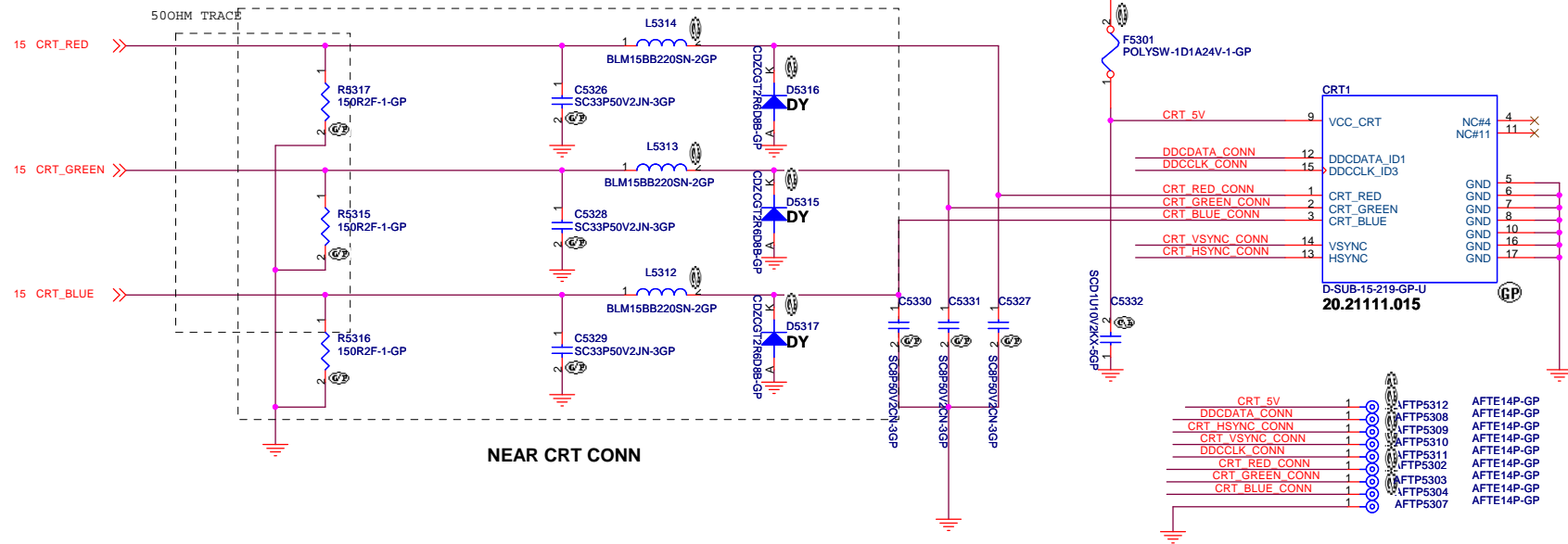
LCD POWER



Shark Bay SV

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			LCD Connector
Size	Document Number	Rev	
A3	LOS1 UMA/DIS	-1	
Date:	Tuesday, July 16, 2013	Sheet	52 of 102

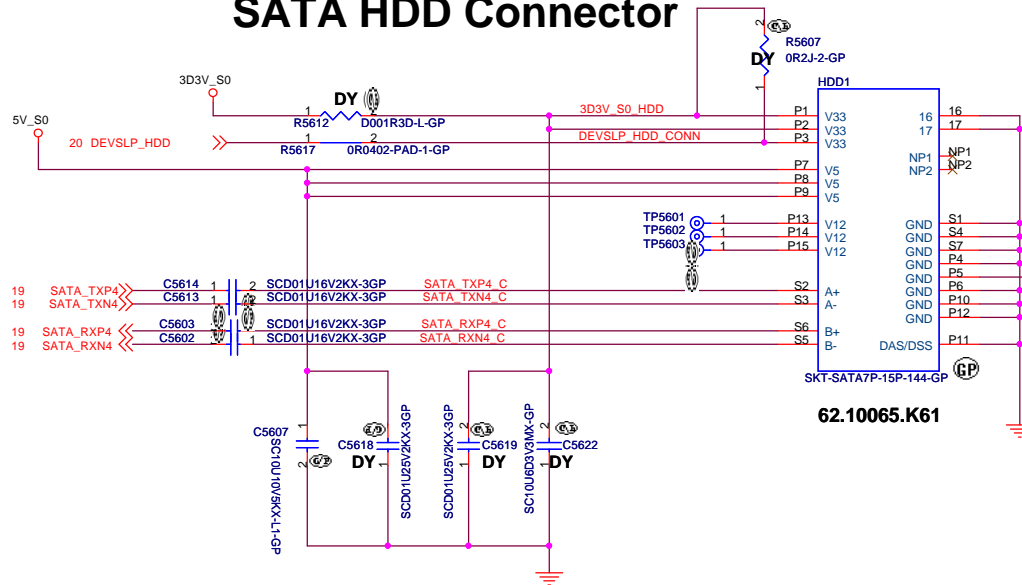


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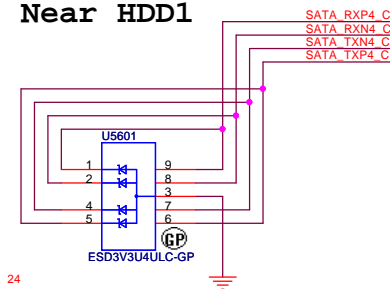
Shark Bay SV

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
HDMI Level Shifter/Connector			
Size	Document Number		Rev
Custom	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013	Sheet	54 of 102

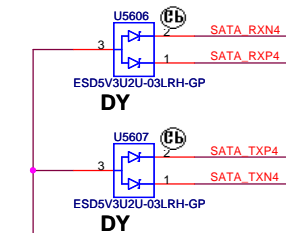
SATA HDD Connector



Near HDD1

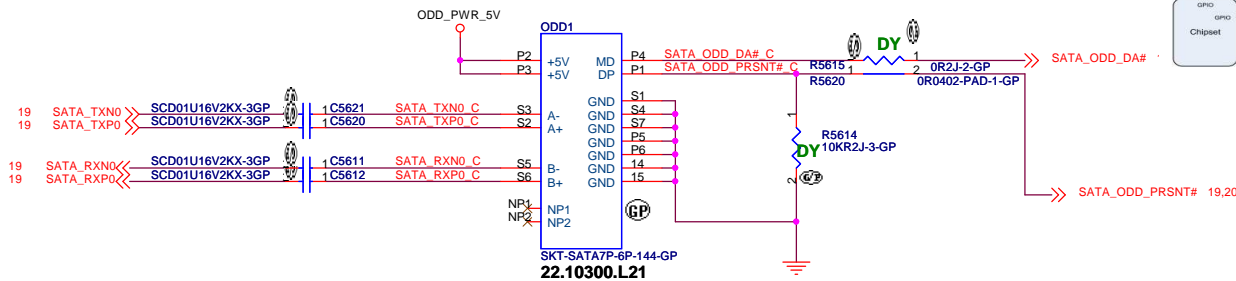


Near PCH

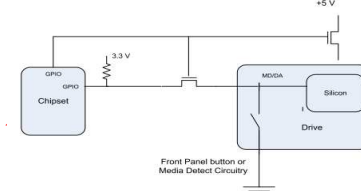


ODD Connector

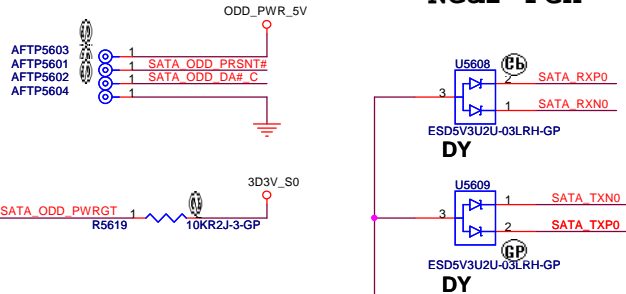
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



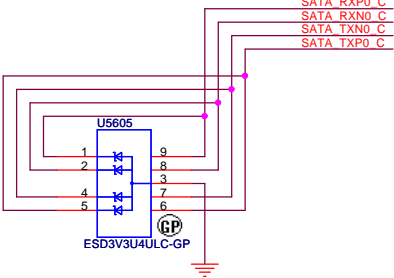
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



Near PCH

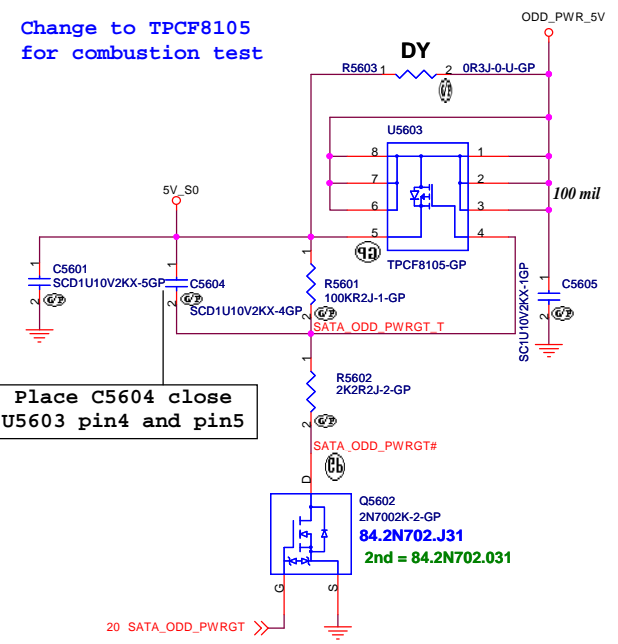


Near ODD1



SATA Zero Power ODD

Change to TPCF8105
for combustion test



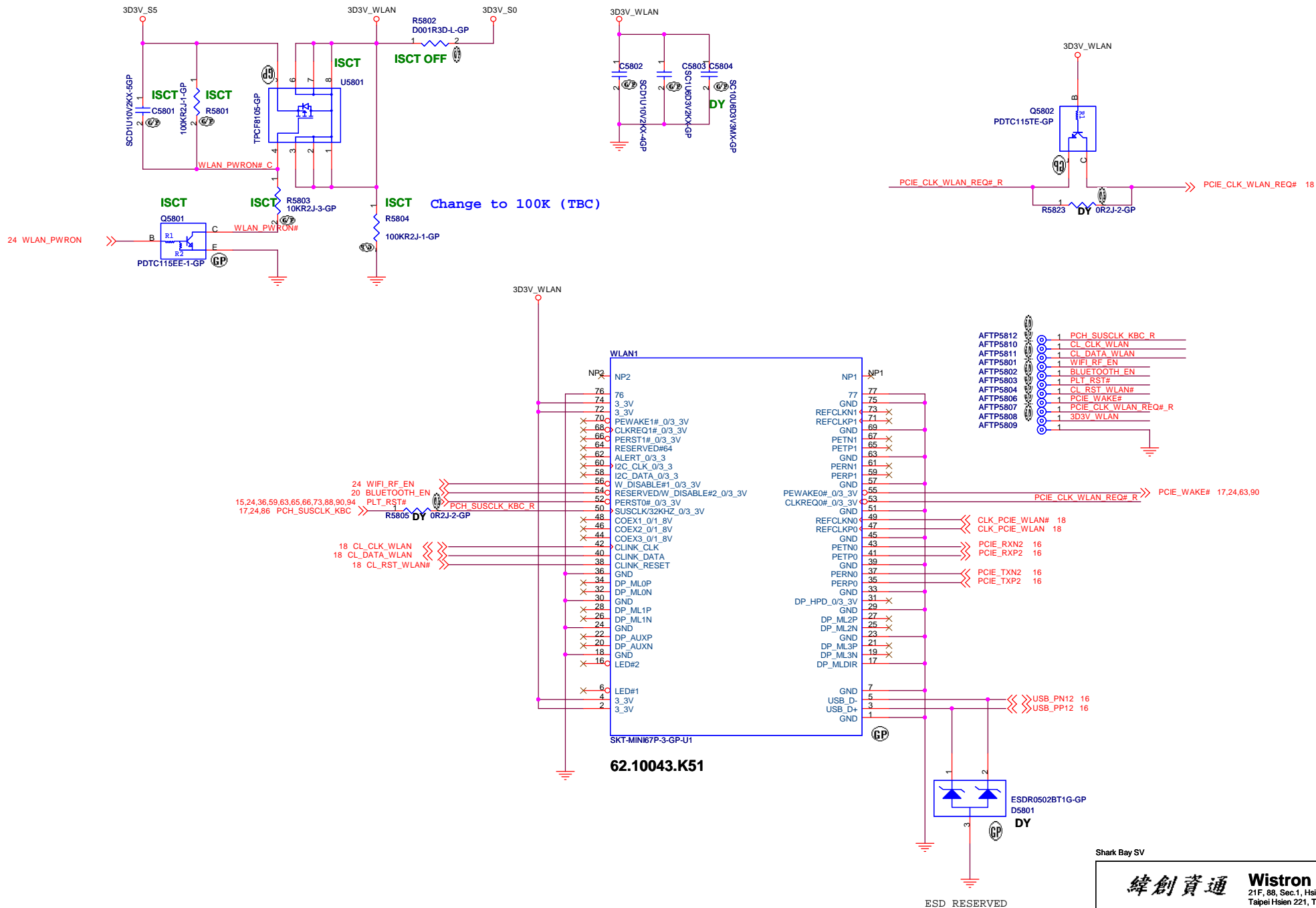
Place C5604 close
U5603 pin4 and pin5

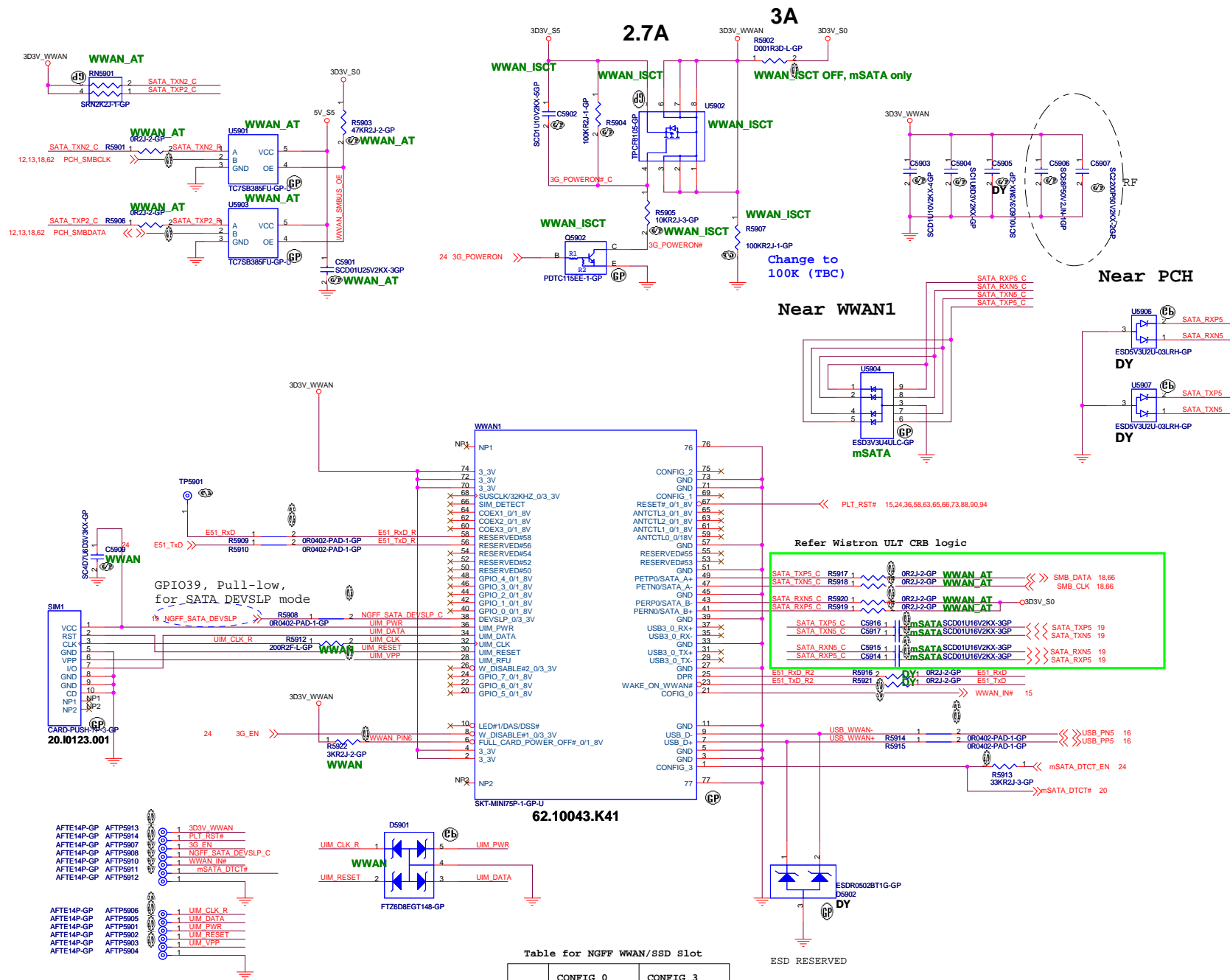
Shark Bay SV

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDD/ODD	
Size A3	Document Number LOS1 UMA/DIS
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SUPPORT ZERO SATA ODD
Vinafix.com

(Reserved)





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Shark Bay SV

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Title <div>BULETOOTH</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>60</div> of <div>102</div>

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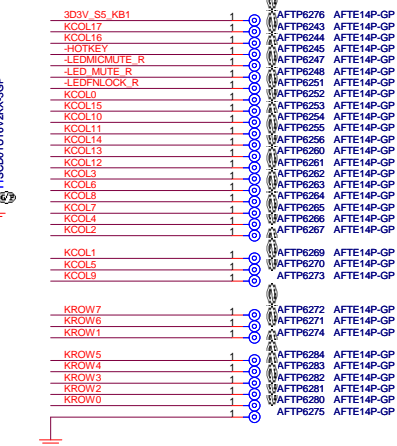
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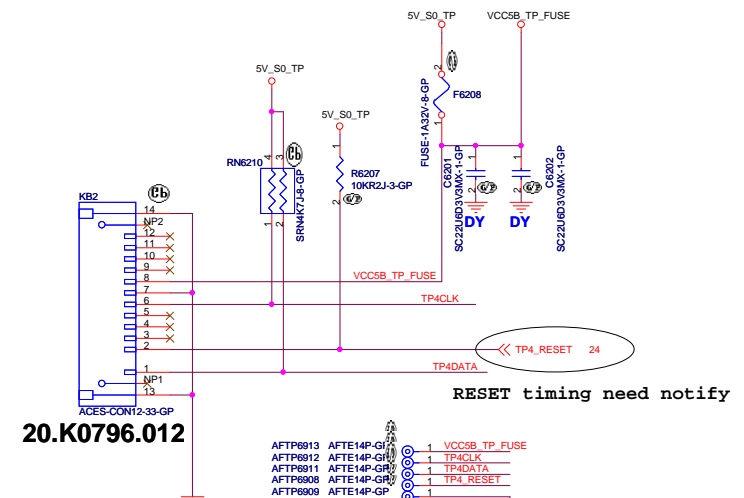
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<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CAM/MIC/HALL SENSOR IF		
Size	Document Number	Rev
A4	LOS1 UMA/DIS	-1
Date:	Tuesday, July 16, 2013	Sheet 61 of 102

[illegible][illegible]

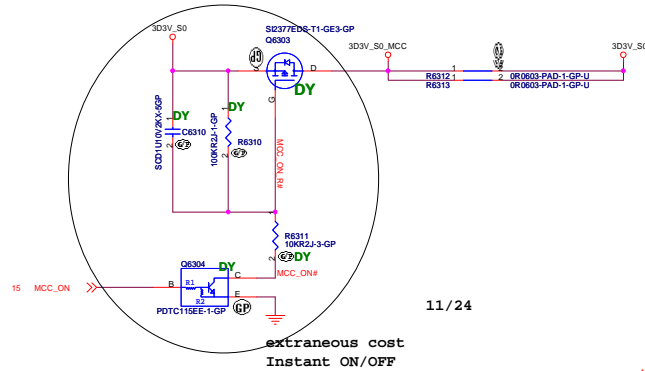
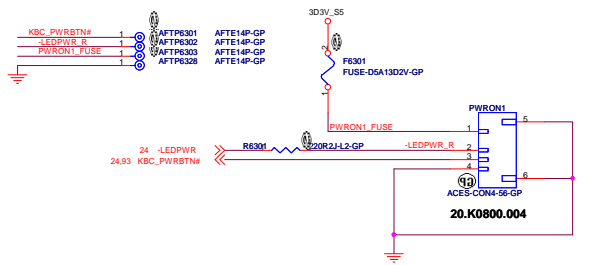
need add, AFTP for KROW 0,2,3,4



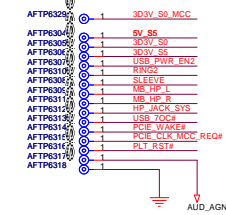
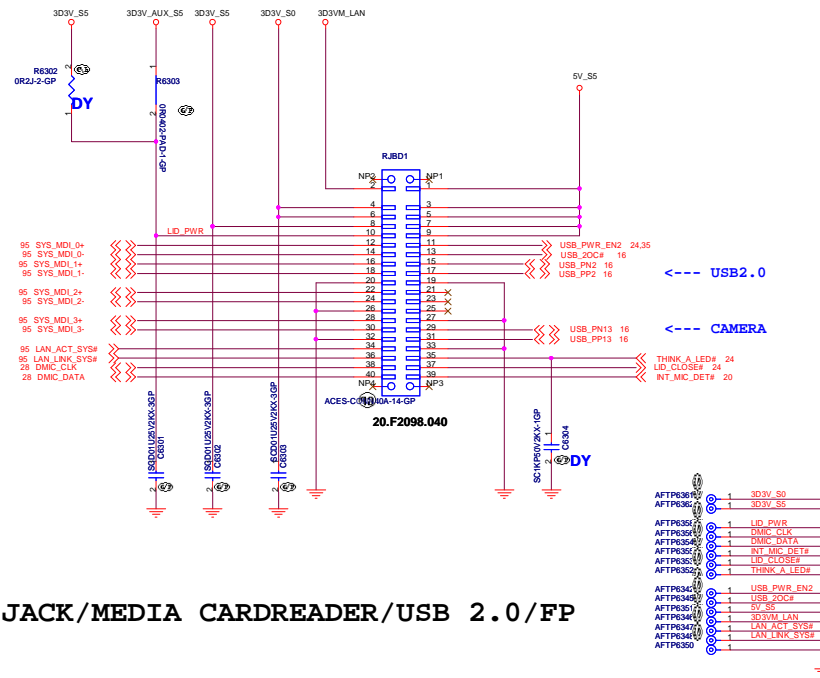
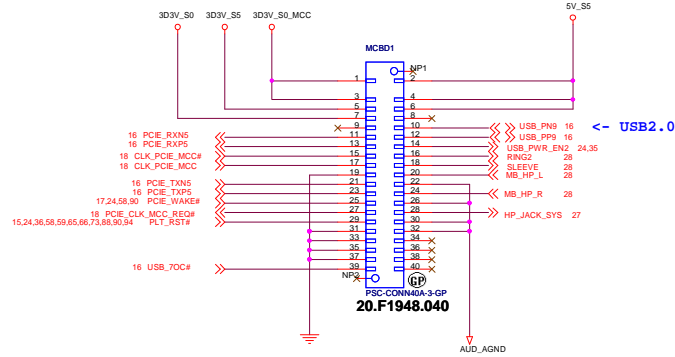
Shark Bay SV		 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		KeyBoard/TrackPoint/Touch Pad	
Size	Document Number	Rev	
Custom	LOS1 UMA/DIS	-1	
Date:	1060509, July 16, 2013	Sheet	62 of 102

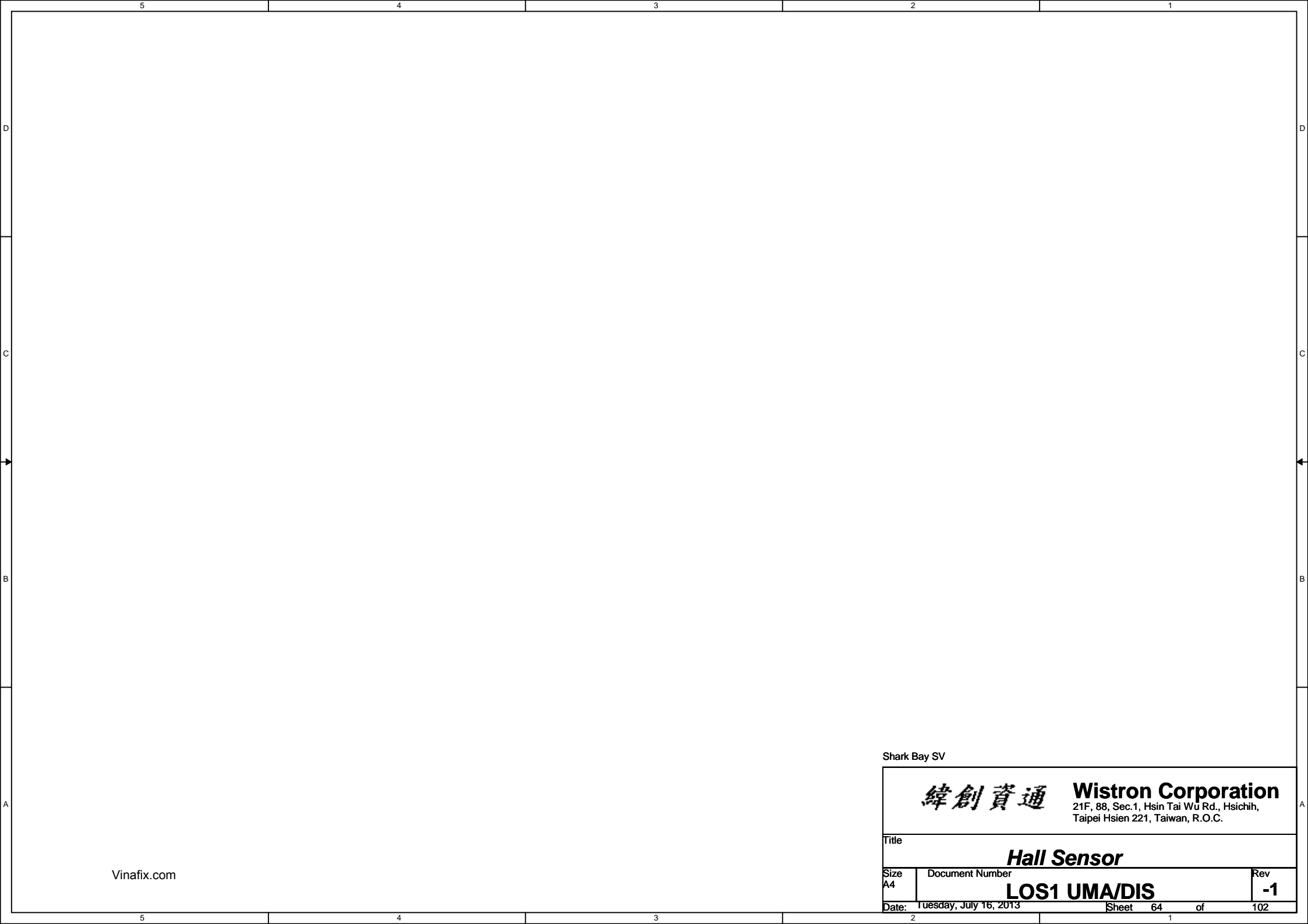
RJ45/USB 2.0 IF/CAMERA/LED

POWER Button



AUDIO JACK/MEDIA CARDREADER/USB 2.0/FP

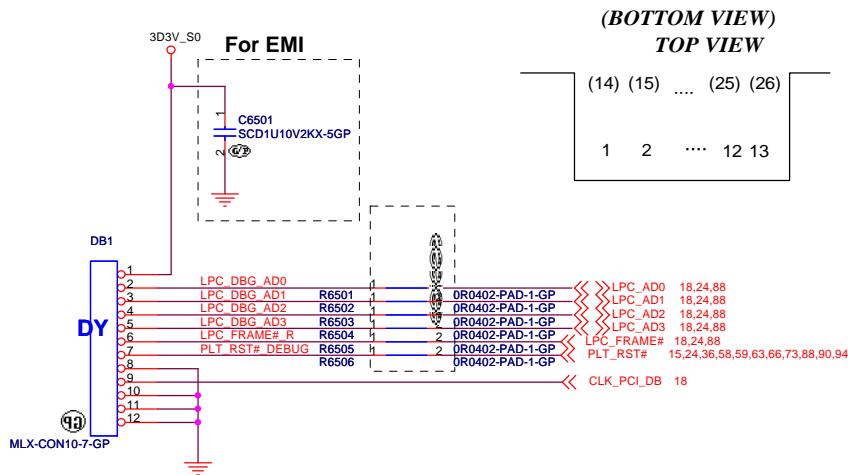


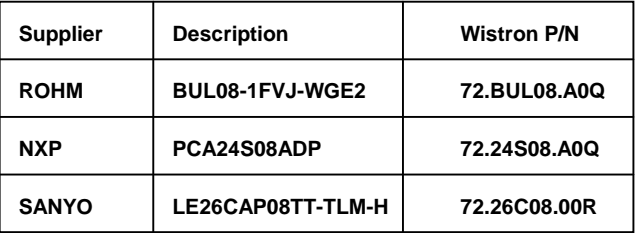


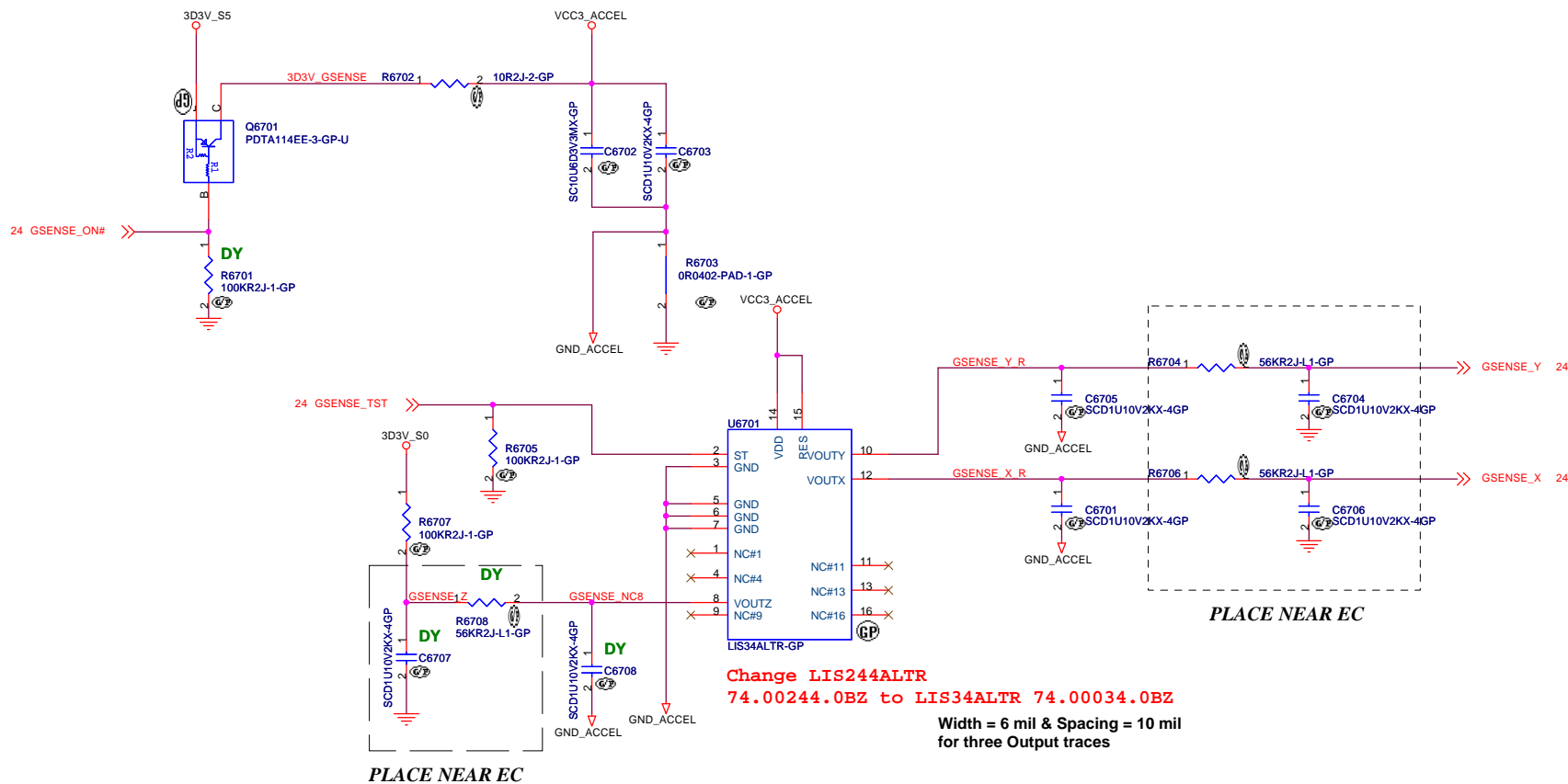
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<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Hall Sensor</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>64</div> of <div>102</div>

LPC Debug Board







	LIS244AL	LIS34AL	NO ACC.
R6701	NO-ASM	ASM	ASM
R957	ASM	ASM	ASM
U6701	ASM	NO-ASM	NO-ASM
Q6701	ASM	NO-ASM	NO-ASM
R885	10-OHM	NO-ASM	NO-ASM
C829	ASM	NO-ASM	NO-ASM
C969	ASM	NO-ASM	NO-ASM
C830	ASM	NO-ASM	NO-ASM
C847	ASM	NO-ASM	NO-ASM
R970	56K	NO-ASM	NO-ASM
C956	ASM	NO-ASM	NO-ASM
R969	56K	NO-ASM	NO-ASM
C938	ASM	NO-ASM	NO-ASM
C704	NO-ASM	NO-ASM	NO-ASM
R344	NO-ASM	NO-ASM	NO-ASM
C703	NO-ASM	NO-ASM	NO-ASM
R125	ASM	ASM	ASM

Table

	Supplier	Vendo P/N	WISTRON P/N
1	ST	LIS34ALTR	74.00034.0BZ 41R0828AA
2	Kionix	KXTC8-2850	74.KXTC8.0BZ

Layout Comment :

(1) Place C586, C588, Q17, R415, R417, C584, C585, R420 close to U34.

(2) Avoid routing under DCDC switching area.

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G- Sensor	
Size: A3 Date: Tuesday, July 16, 2013	Document Number: LOS1 UMA/DIS Sheet: 67 of 102
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Thunderbolt (1/5)</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>68</div> of <div>102</div>

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Shark Bay SV

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (2/5)

Size

Document Number

Rev

A4

LOS1 UMA/DIS

-1

Date:

Tuesday, July 16, 2013

Sheet

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102

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Title <div>Thunderbolt (3/5)</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>70</div> of <div>102</div>

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Reserved

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Title <div>Thunderbolt (4/5)</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>	Sheet <div>71</div>	of <div>102</div>

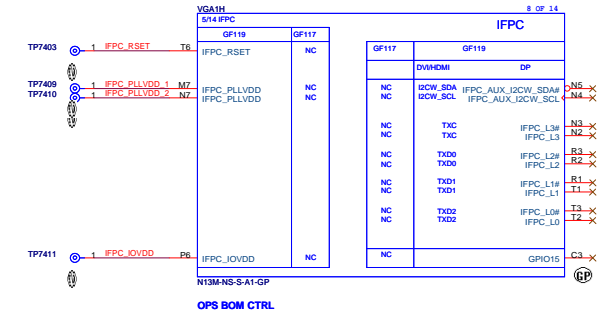
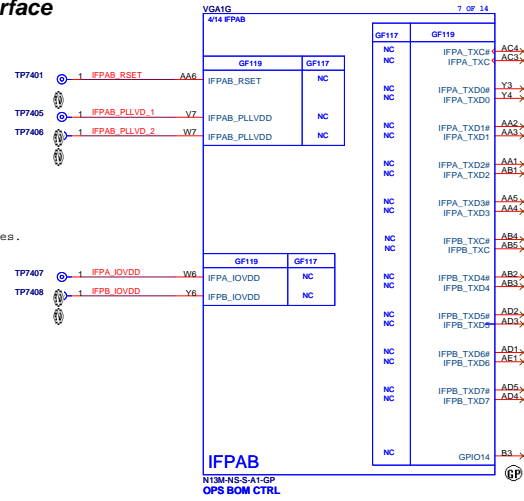
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Shark Bay SV

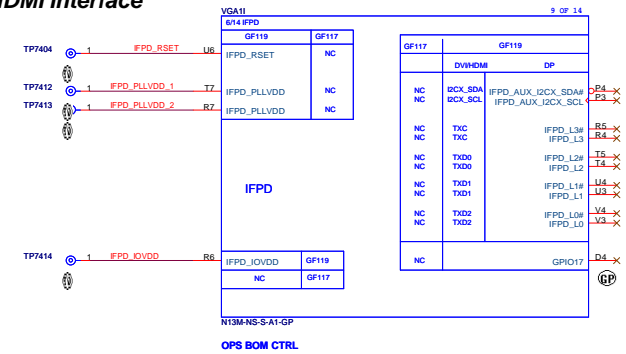
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LOS1 UMA/DIS</div>	Rev <div>-1</div>
Date <div>Tuesday, July 16, 2013</div>		Sheet <div>72</div> of <div>102</div>

LVDS Interface

SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.



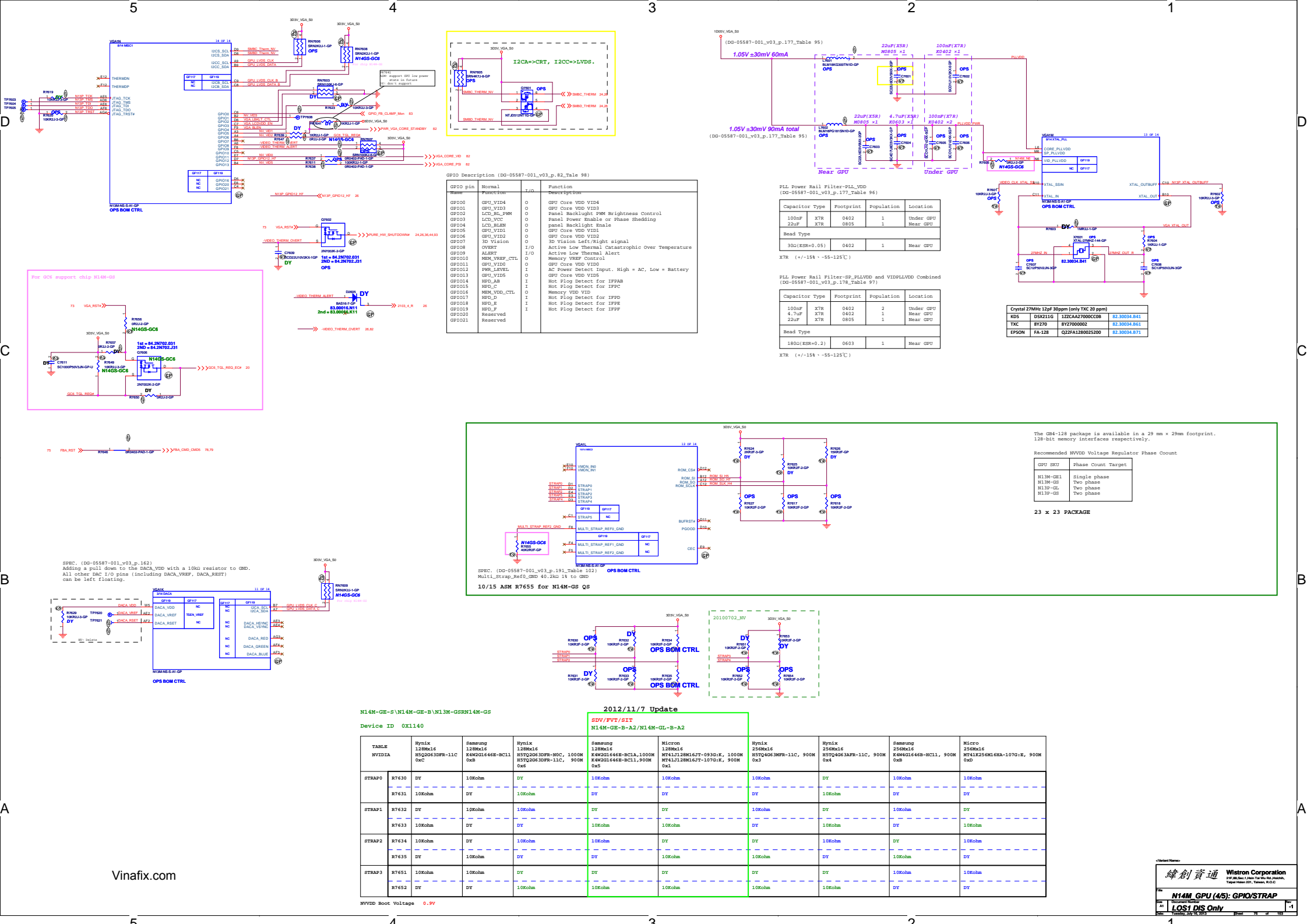
HDMI Interface



<Core Design>

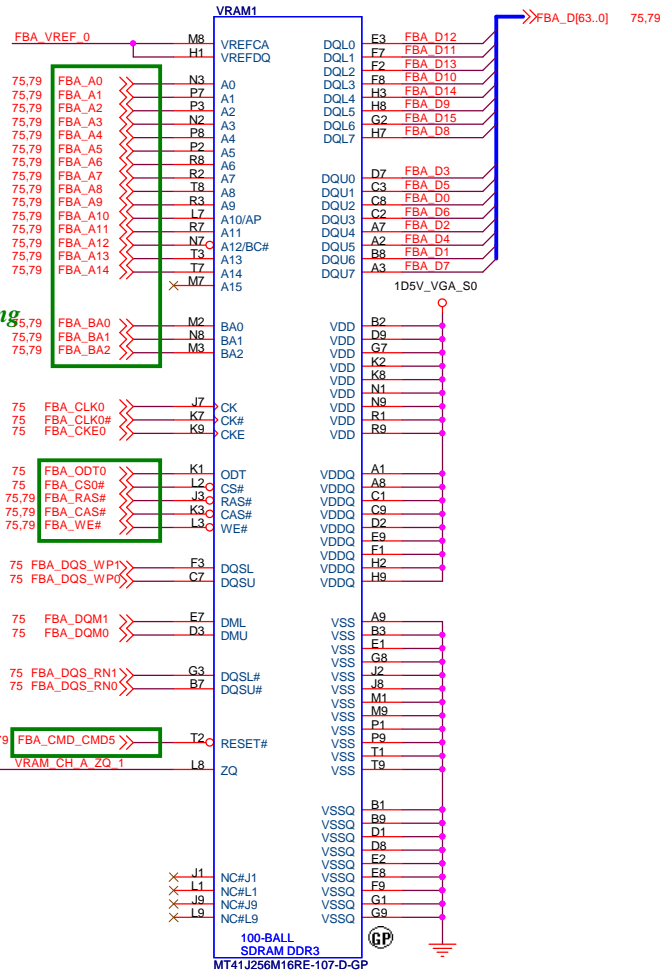
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsinchu,
Taippei Hsien 301, Taiwan, R.O.C.

Title **N14M_GPU (2/5): DIGITALOUT**
Size A2 Document Number **LOS1 Dis Only** Rev -1
Date: Tuesday, July 16, 2013 Sheet 74 of 103

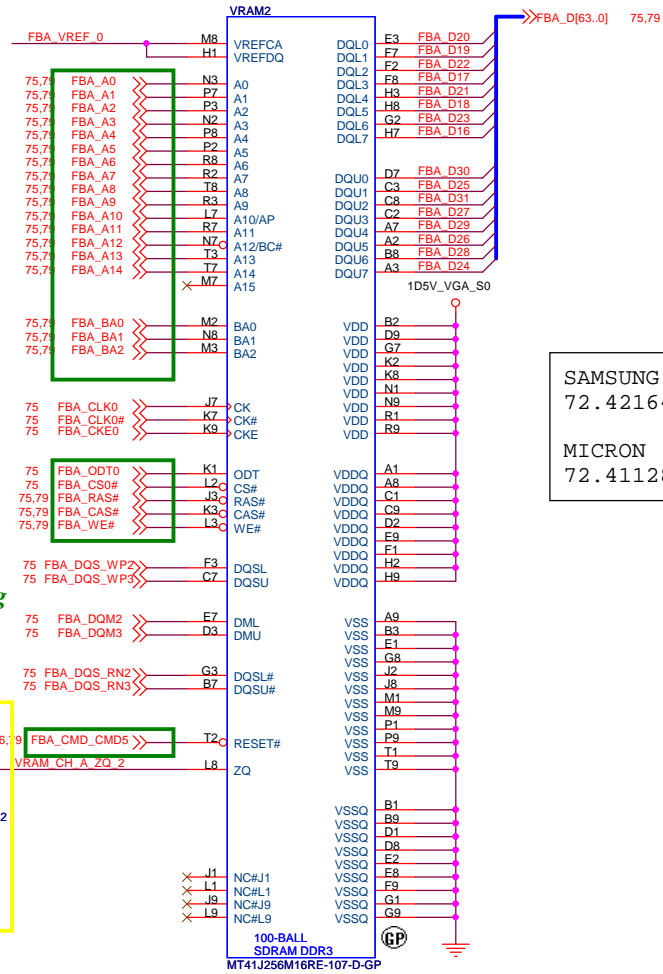


VIDEO FRAME BUFFER PORT A

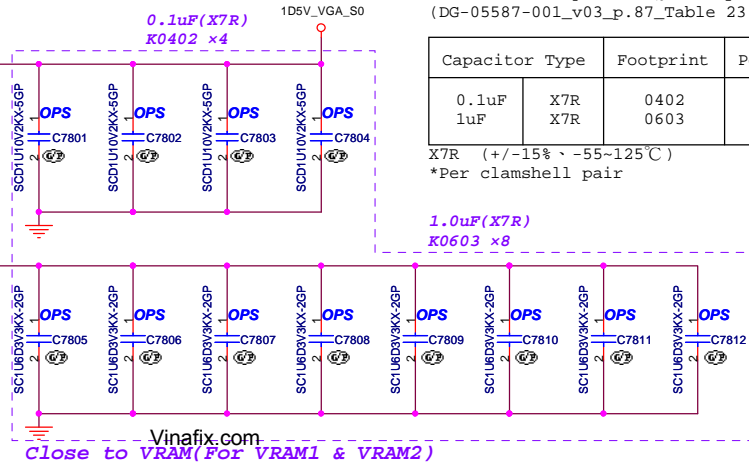
FB CMD mapping Mode D-N13x



FB CMD mapping Mode D-N13x

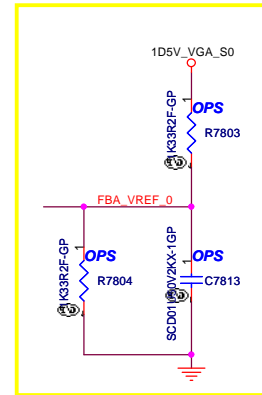


SAMSUNG K4W2G1646E-BC1A
72.42164.N0U
MICRON MT41J128M16JT-093G:K
72.41128.I0U



Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair



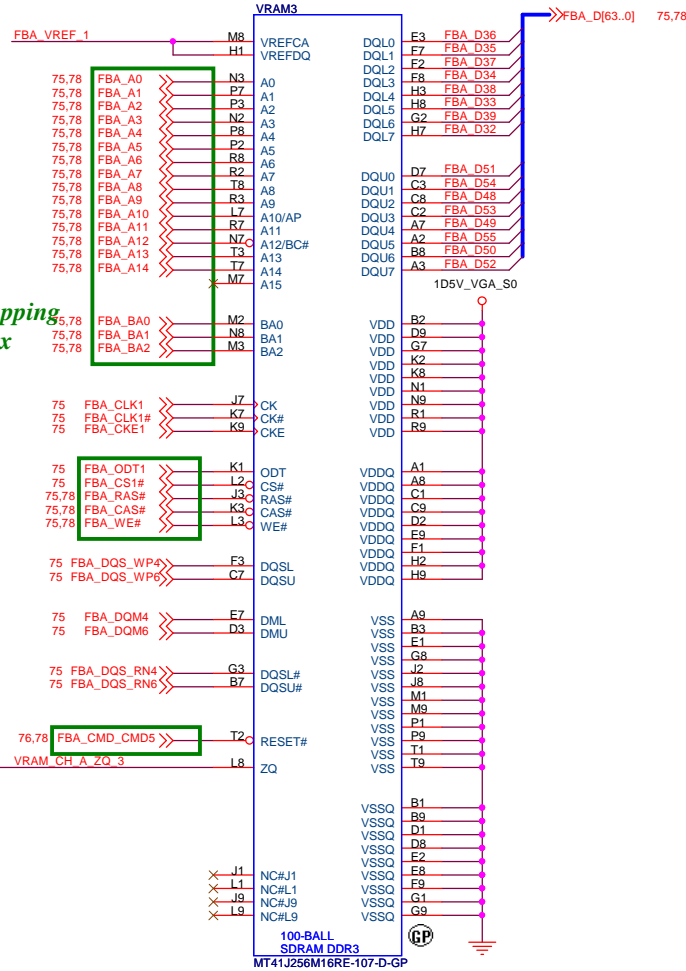
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CHANNEL-A_VRAM1,2 (1/4)
Size A3 Document Number OS1/PD1 UMA/DIS Rev -1
Date: Tuesday, July 16, 2013 Sheet 78 of 103

VIDEO FRAME BUFFER PORT A

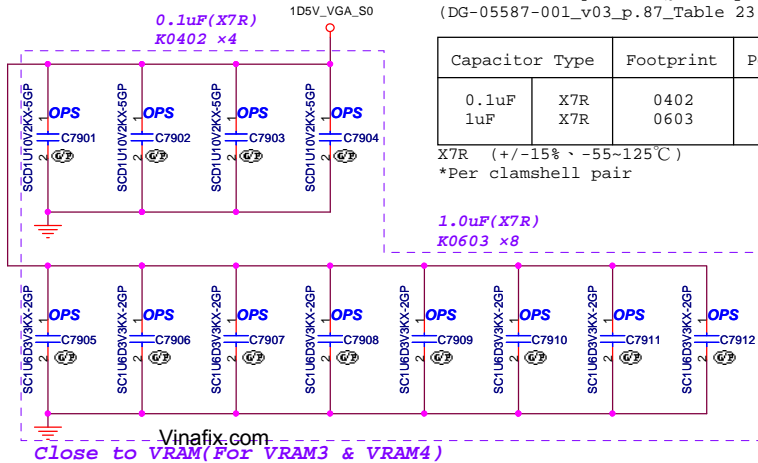
FB CMD mapping
Mode D-N13x



72.41256.D0U OPS BOM CTRL
Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

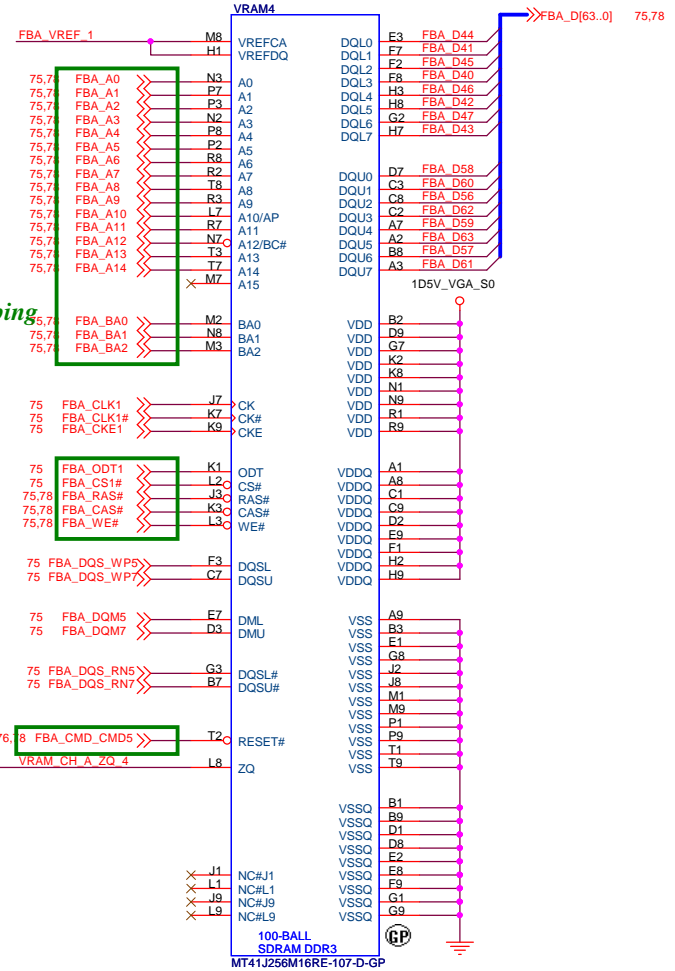
Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair

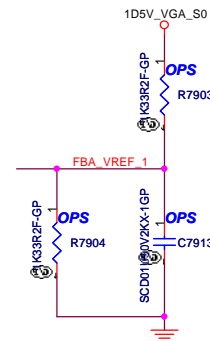


Vinafix.com
Close to VRAM(For VRAM3 & VRAM4)

FB CMD mapping
Mode D-N13x



72.41256.D0U OPS BOM CTRL



<Core Design>

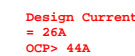
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHANNEL-A_VRAM3,4 (2/4)		
Size	Document Number	Rev	-1
A3	LOS1 DIS Only		
Date:	Tuesday, July 16, 2013	Sheet	79 of 103

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<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,	
Taipei Hsien 221, Taiwan, R.O.C.		Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A2	Document Number OS1/PD1 UMA/DIS		Rev -1
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JV10-CS			
緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NCP81172_VGA_CORE			
Size	Document Number	LOS1 DIS Only	Rev -1
Date:	Tuesday, July 16, 2013	Sheet 62 of	103

1.05V to 1.05V_VGA_S0 Transfer



5

4

3

2

1

D

D

C

C

B

B

A

A

(Reserved)

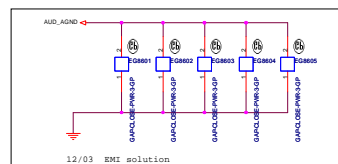
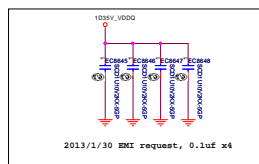
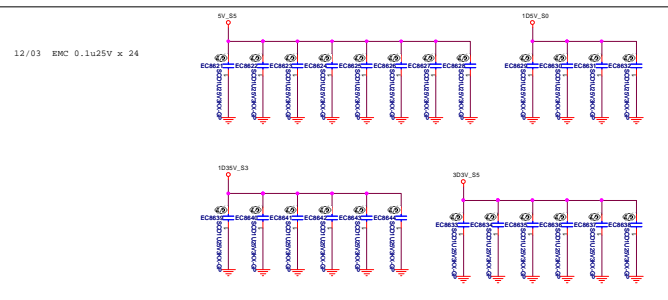
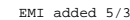
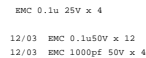
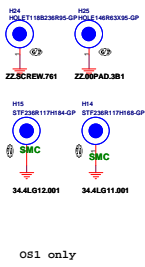
Shark Bay SV

<div>緯創資通</div>		<div>Wistron Corporation</div>			
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
<div>Switchable GFX LCD(1/2)</div>					
Size	Document Number		Rev		
A4	LOS1 UMA/DIS		-1		
Date:	Tuesday, July 16, 2013				
Sheet		84	of 102		

(Reserved)

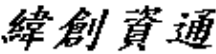
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Title			
CRT Switch			
Size	Document Number		Rev
A3	LOS1 UMA/DIS		-1
Date:	Tuesday, July 16, 2013	Sheet	85 of 102



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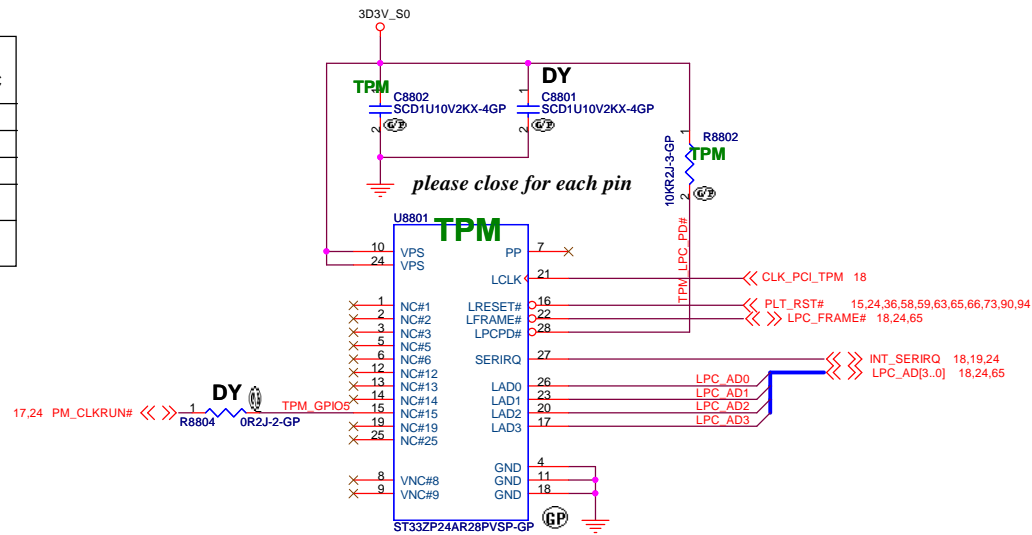
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NFC			
Size A4	Document Number LOS1 UMA/DIS		Rev -1
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TCPA

	NO TPM	ST Micro ST33ZP24AR28PVSC
U8801	NO_ASM	ASM
C8802	NO_ASM	ASM
R8802	NO_ASM	ASM
R1839	ASM	NO_ASM
R1840	NO_ASM	ASM

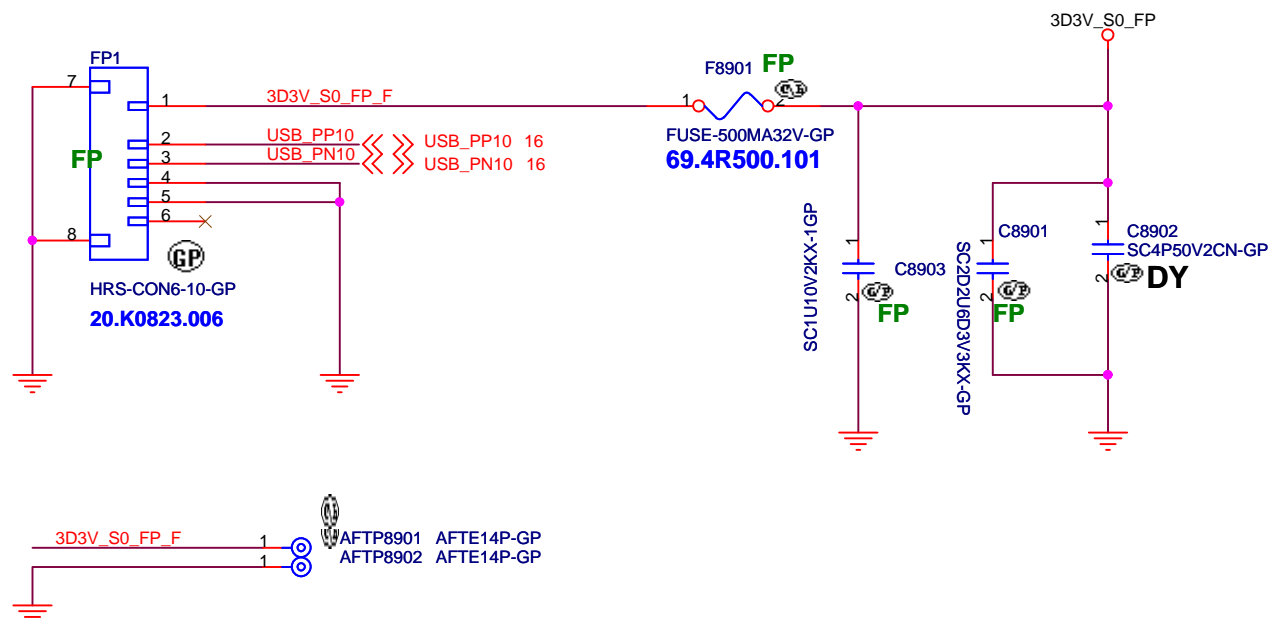
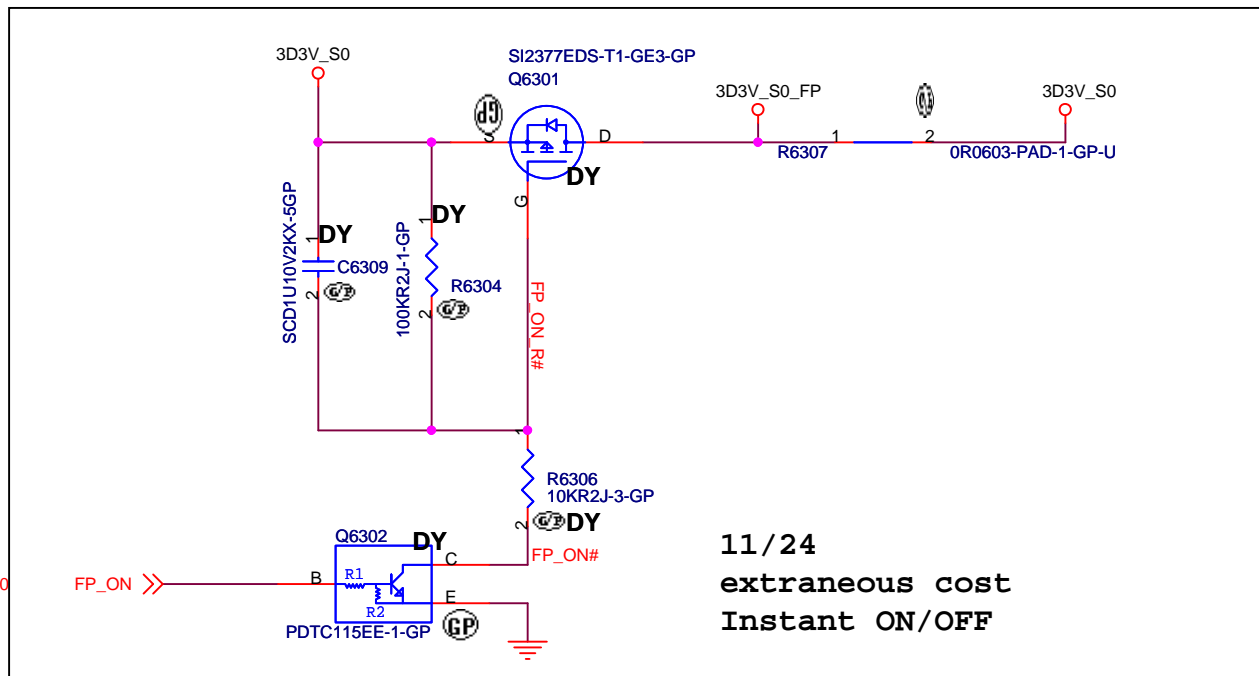
↑
LOGIC



71.03324.F0W

NEW TPM for SVT

2012/11/5 update TPM for new FW



Vinafix.com

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緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Finger Printer

Size
A4

Document Number

LOS1 UMA/DIS

Rev
-1

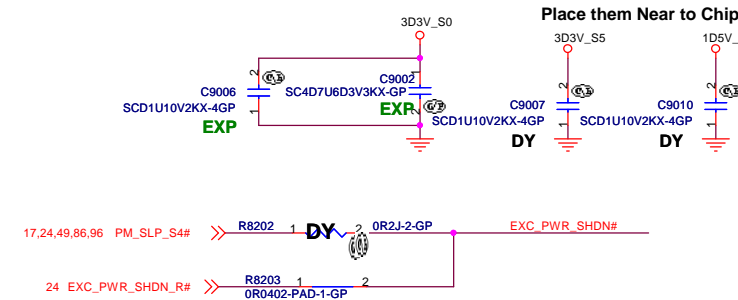
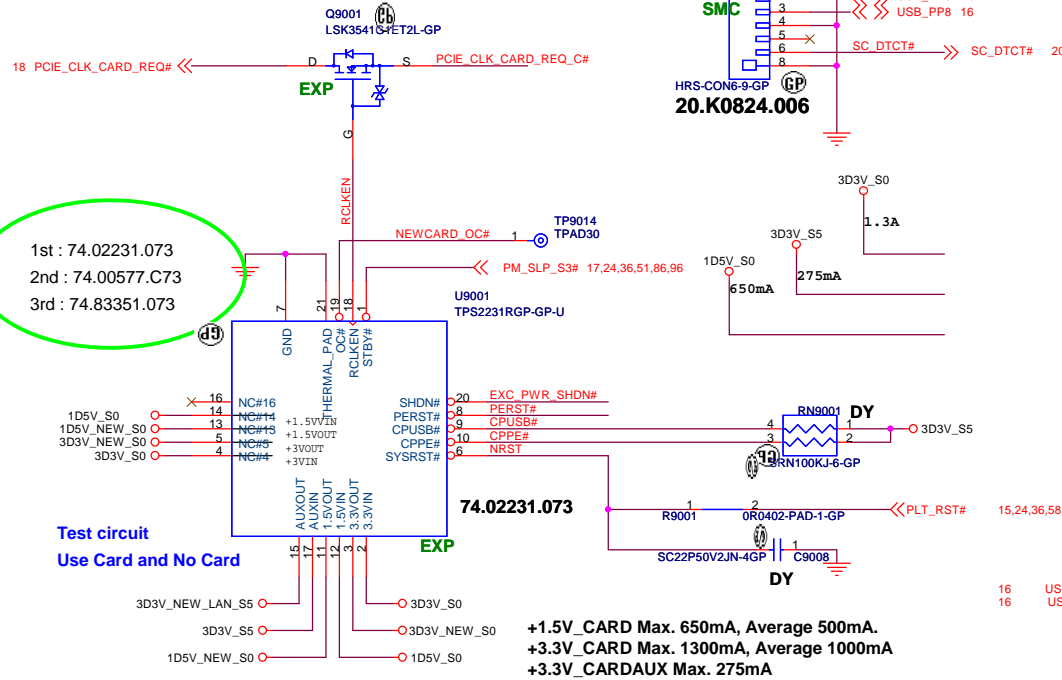
Date: Tuesday, July 16, 2013

Sheet 89 of 102

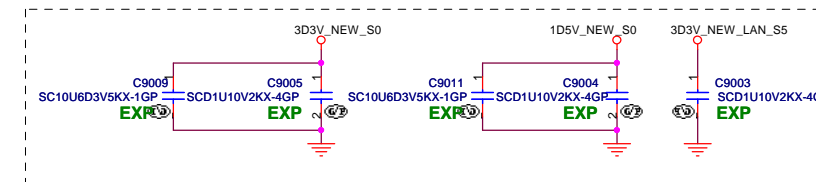
EXPRESSCARD

SMART CARD CONN

EXPRESS CARD SKT



Place them Near to Connector



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Express Card		
Size A3	Document Number	Rev -1
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5

4

3

2

1

D

D

C

C

B

B

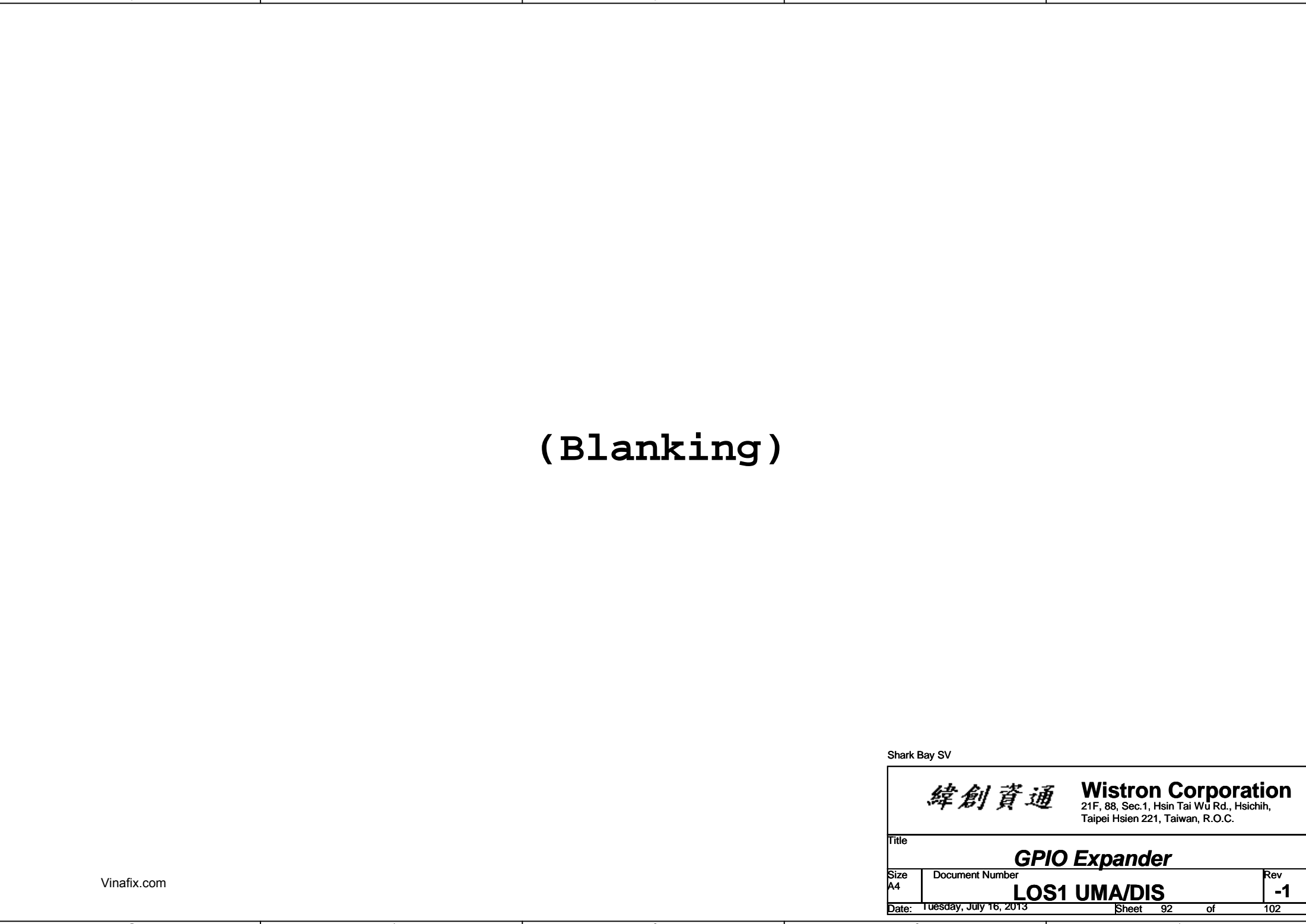
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A

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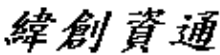
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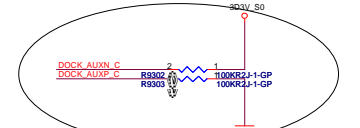
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
Smart Card Socket					
Size	Document Number		Rev		
	LOS1 UMA/DIS		-1		
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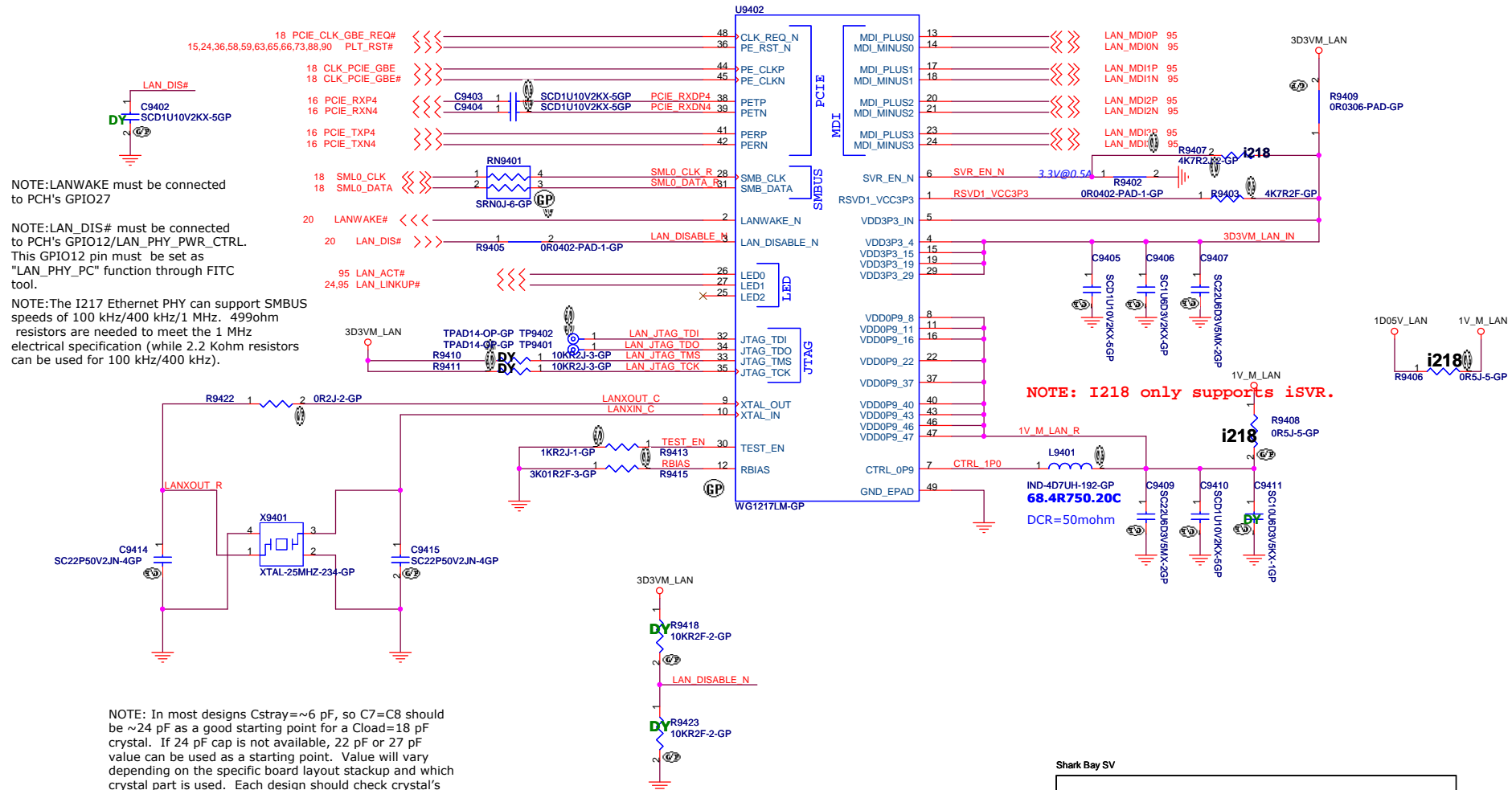
Shark Bay SV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>GPIO Expander</i>			
Size A4	Document Number LOS1 UMA/DIS		Rev -1
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Shark Bay SV		 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Neichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DOCKING CONNECTOR			
LOS1 UMA/D3			
Size A2	Document Number	Sheet	Rev -1
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LAN intel I217

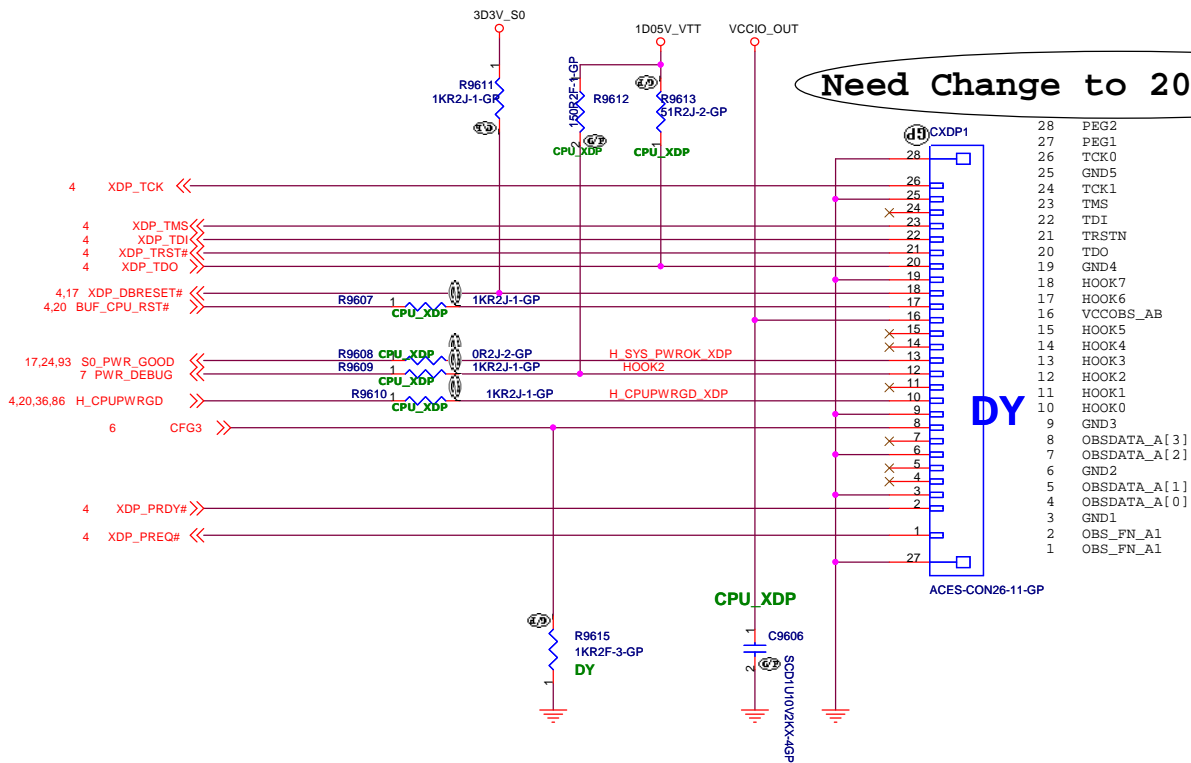


Crystal 25MHz 18pF 30ppm			
KDS	DSX211G	1ZZCAA25000CC08	82.30020.N81
TXC	8Y250	8Y25000004	82.20026.191
EPSON	FA-128	Q22FA1280023800	82.30020.P21

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LAN INTEL I217	
Size	Document Number
A3	LOS1 UMA/DIS
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CPU XDP CONNECTOR 26PIN

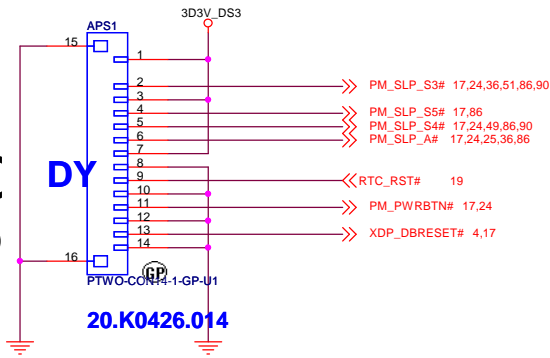


DY

PCH_XDP 26Pin Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	Open	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

APS Connector



20.K0426.014

Shark Bay SV

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Title

CPU XDP

Size A3

Document Number

LOS1 UMA/DIS

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Rev -1

PCH Strapping

Name	Schematics	Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

PCIE Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN
LANE7	Thunderbolot
LANE8	

SATA Table

SATA	
Pair	Device
0	HDD1
1	M-SATA
2	ODD
3	ESATA
4	N/A
5	N/A

USB Table

Pair	Device
0	USB port 1
1	USB port 2
2	USB port3 (usb charger)
3	X
4	BLUETOOTH
5	Fingerprint
6	X
7	X
8	Mini Card2 (WWAN)
9	USB port4(ESATA),on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	NFC

2012/08/06 Change page.44, 45, 82 to Power team soultion

Shark Bay SV

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size
B

Document Number
LOS1 UMA/DIS

Rev
-1

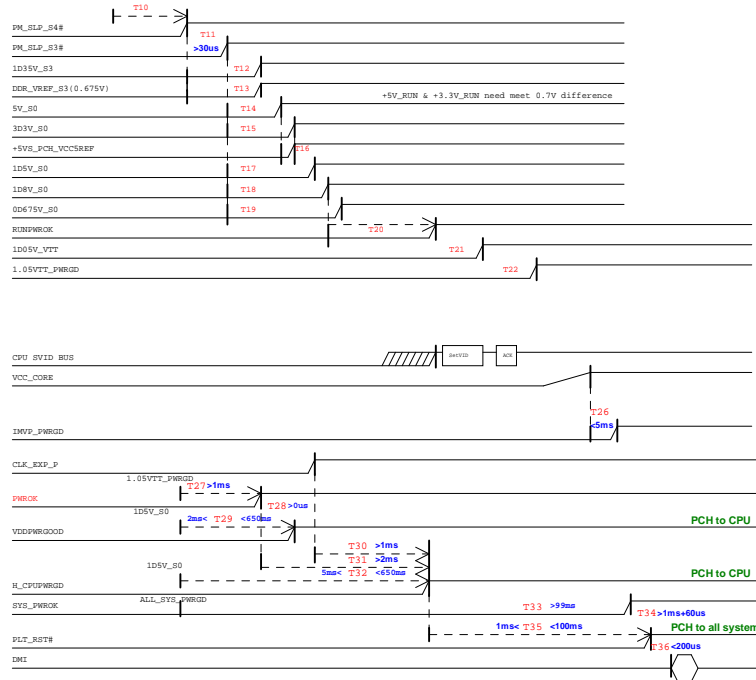
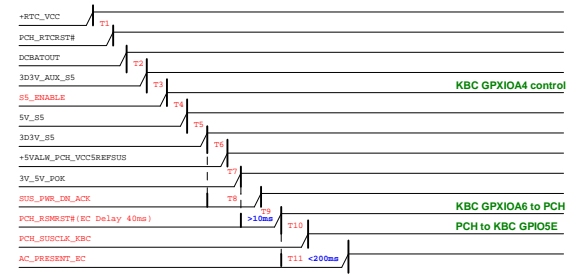
Date: Tuesday, July 16, 2013

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Intel-Power Up Sequence

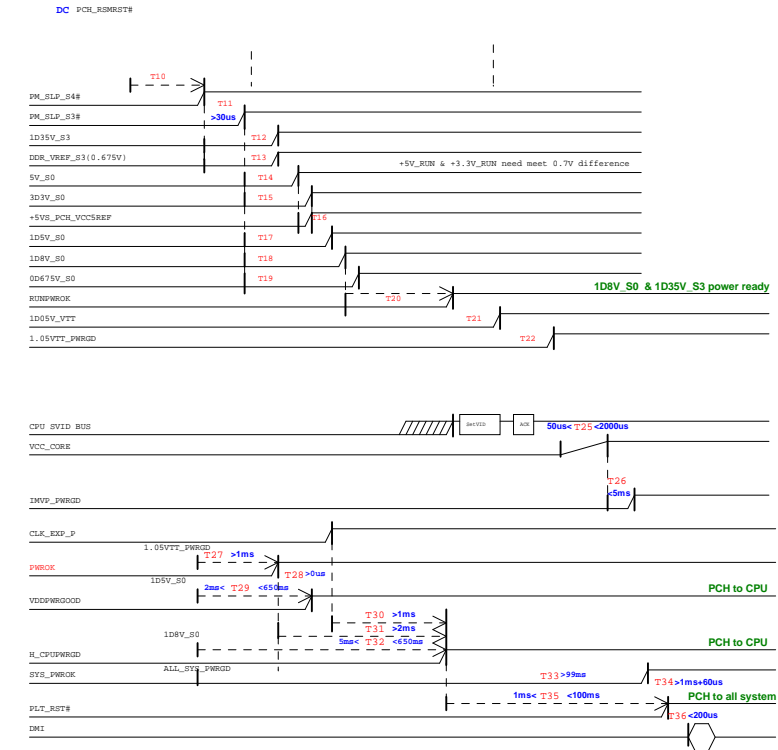
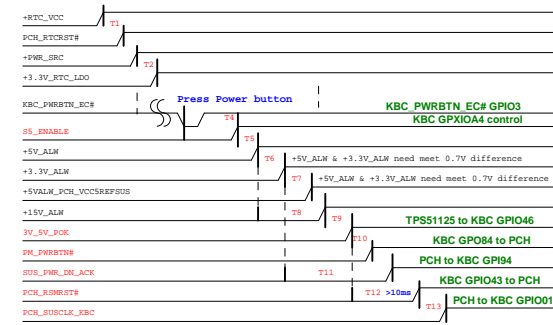
(AC mode)

red word: KBC GPIO

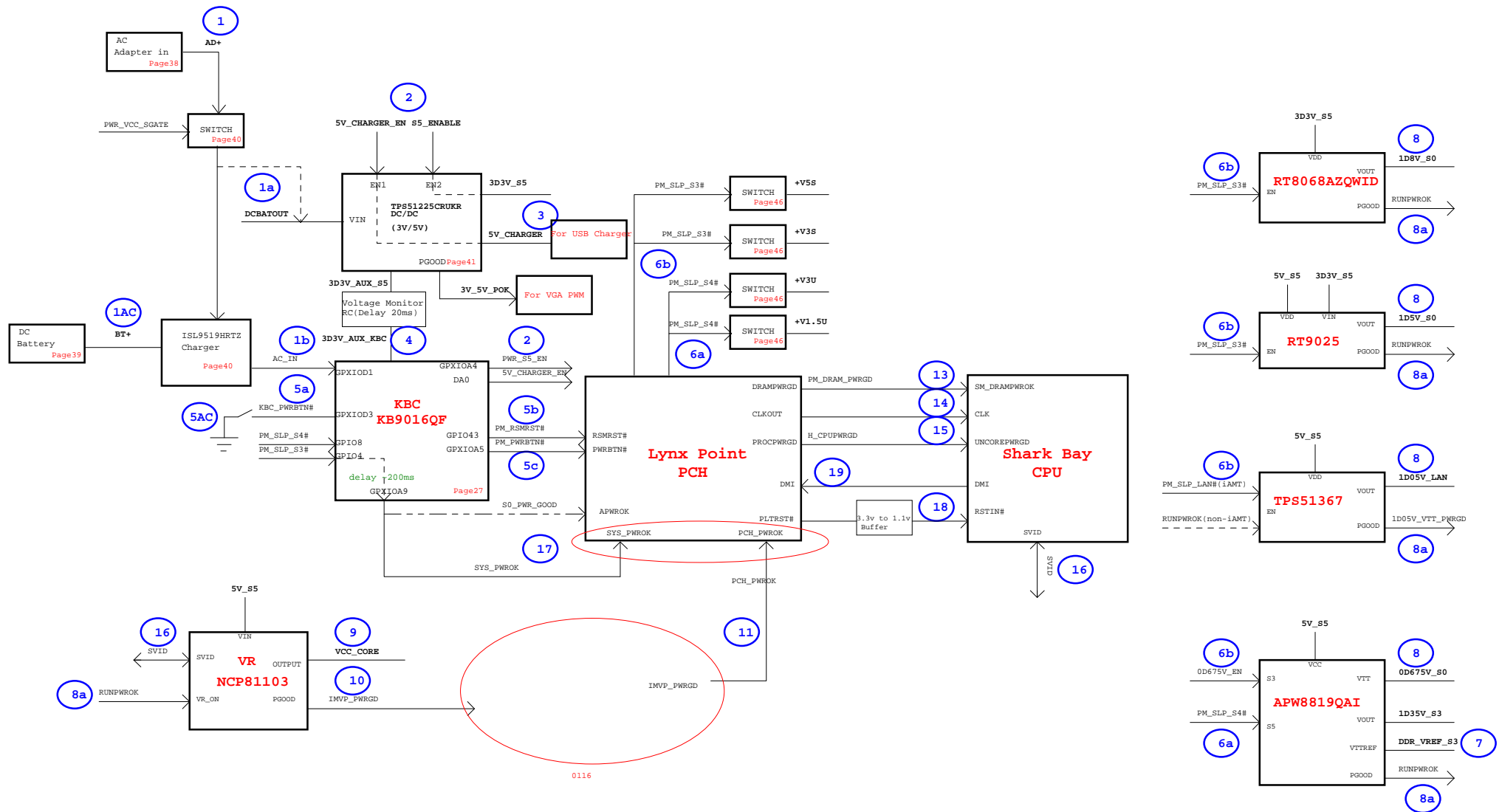


(DC mode)

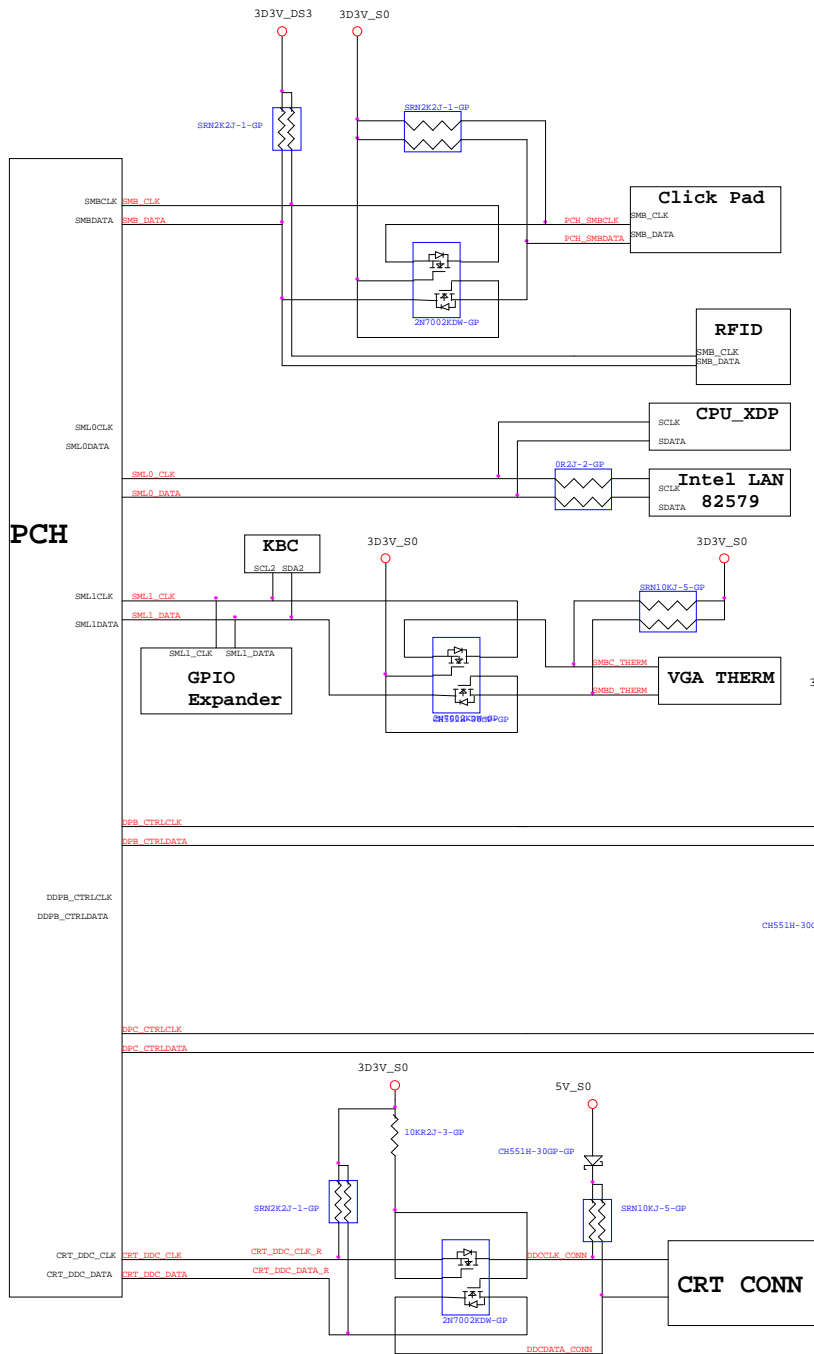
red word: KBC GPIO



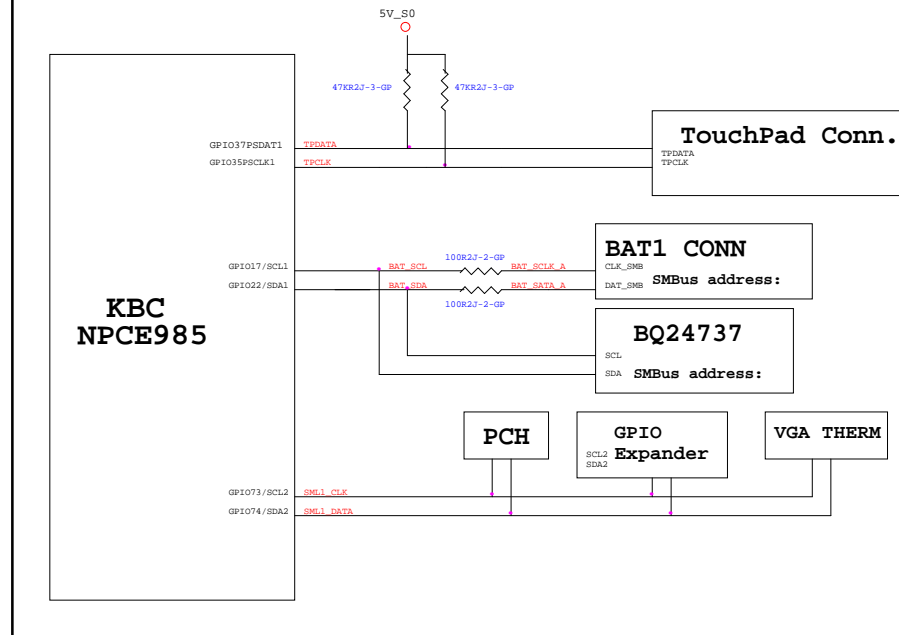
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



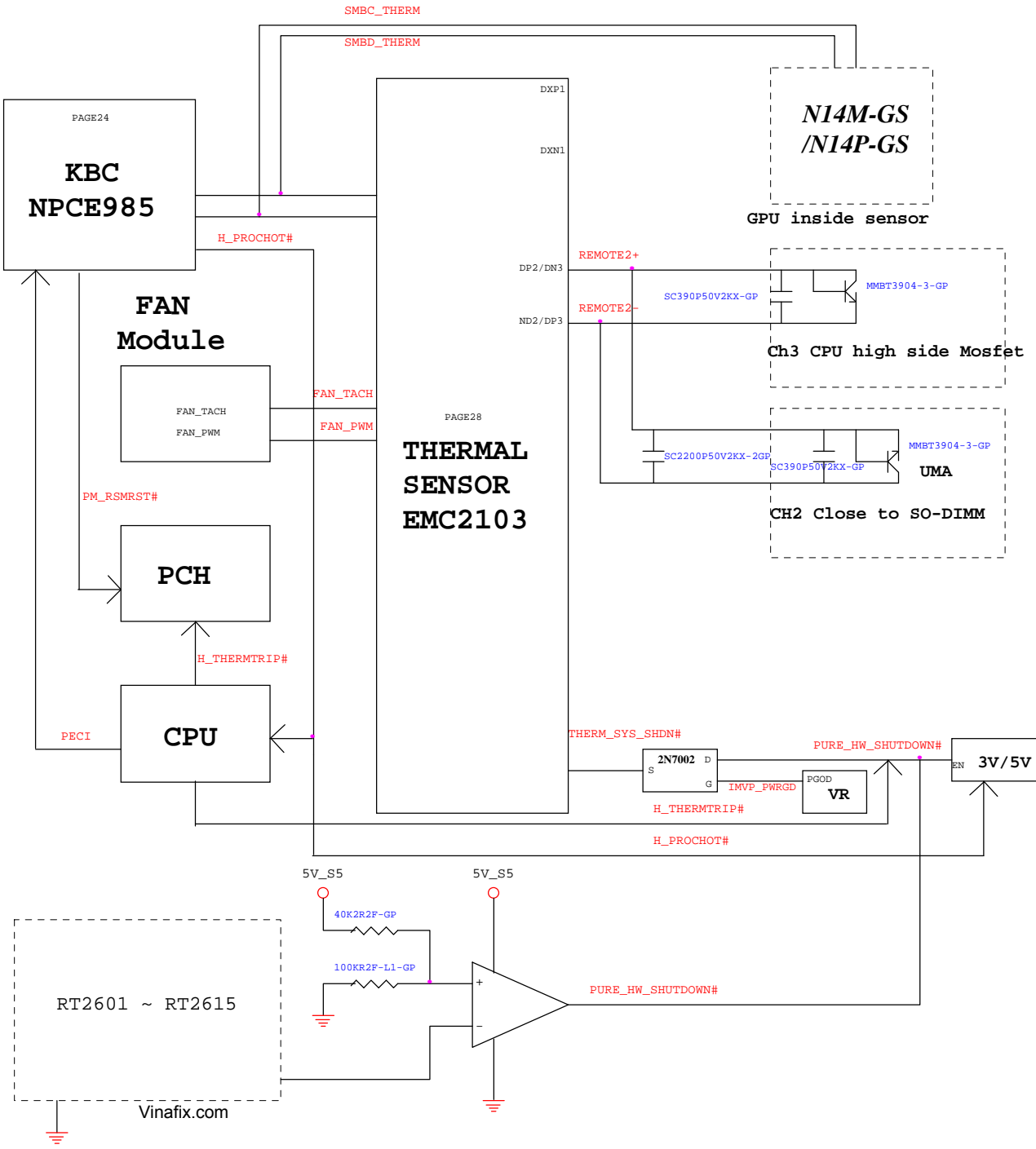
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

