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NEC:Rodem-MA Rodem-VS

MSI:MS-7402N1

Version:10



CPU: Conroe family processors in LGA775 Package.

System Chipset:

NVIDIA MCP73PV single-chip

On Board Device:

BIOS -- SPI Flash 8M

LAN -- Broadcom 5787M

Super I/O -- SMSC5617

AUDIO -- Realtek HD ALC262


Main Memory:

signal-channel DDR-II * 2 (667MHZ)

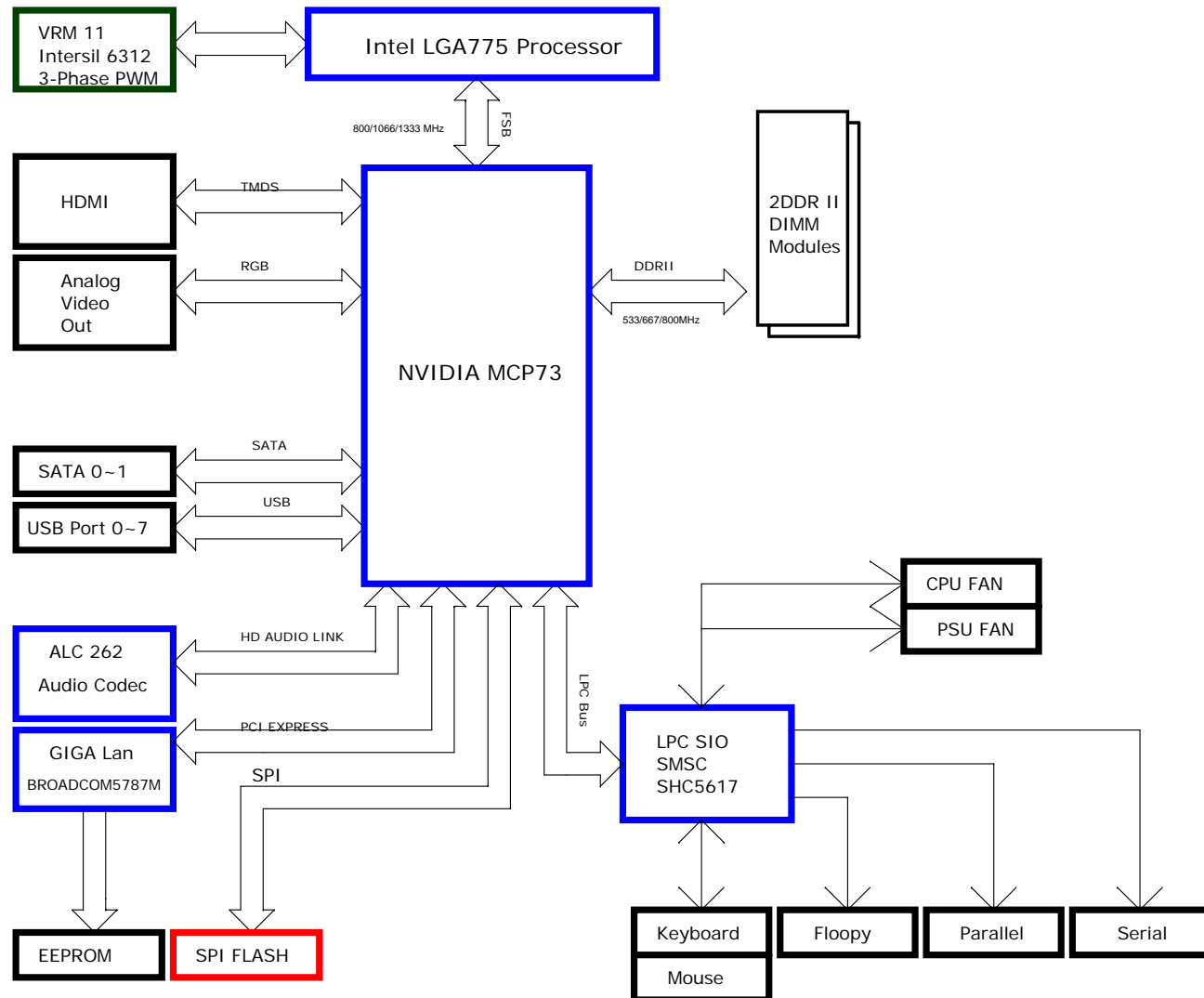
Intersil PWM:

Controller: Intersil ISL6312 (3 Phases)

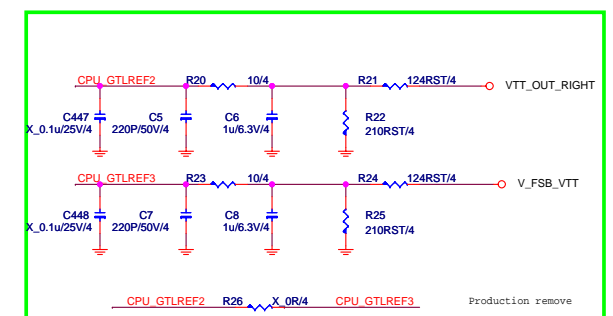
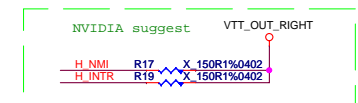
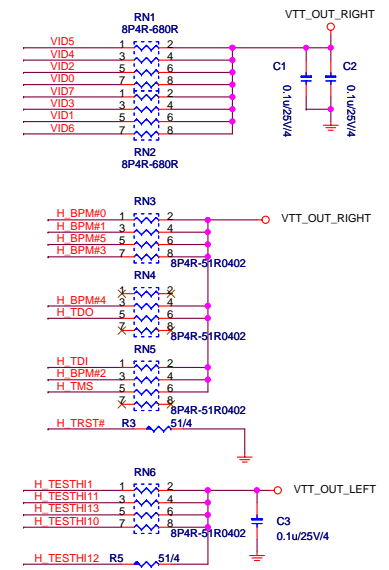
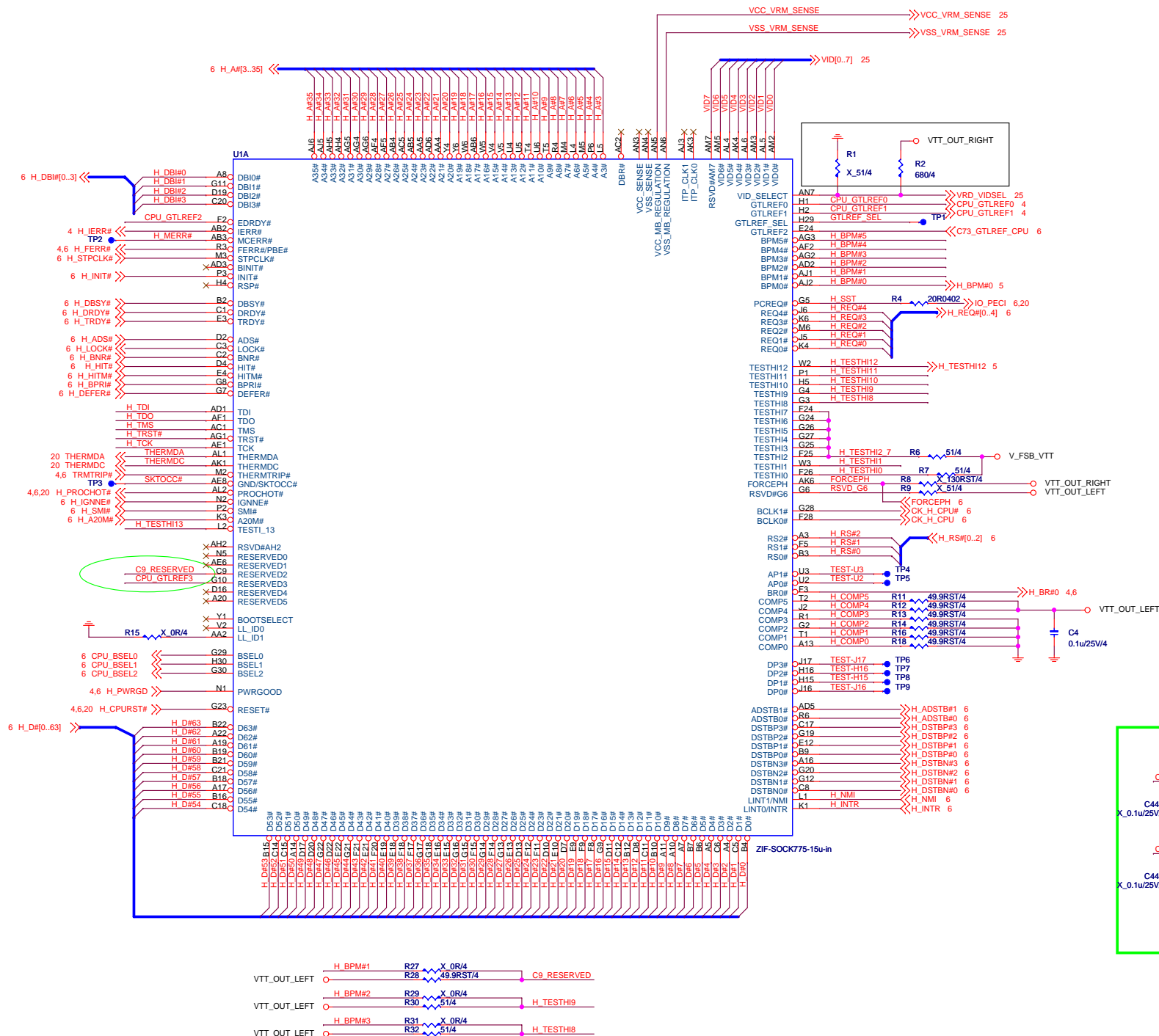
	ERP NUMBER	Orcad Configure	BOM
0C	601-7402-01S	Cfg-7402-MA	
0C	601-7402-02S	Cfg-7402-VS	

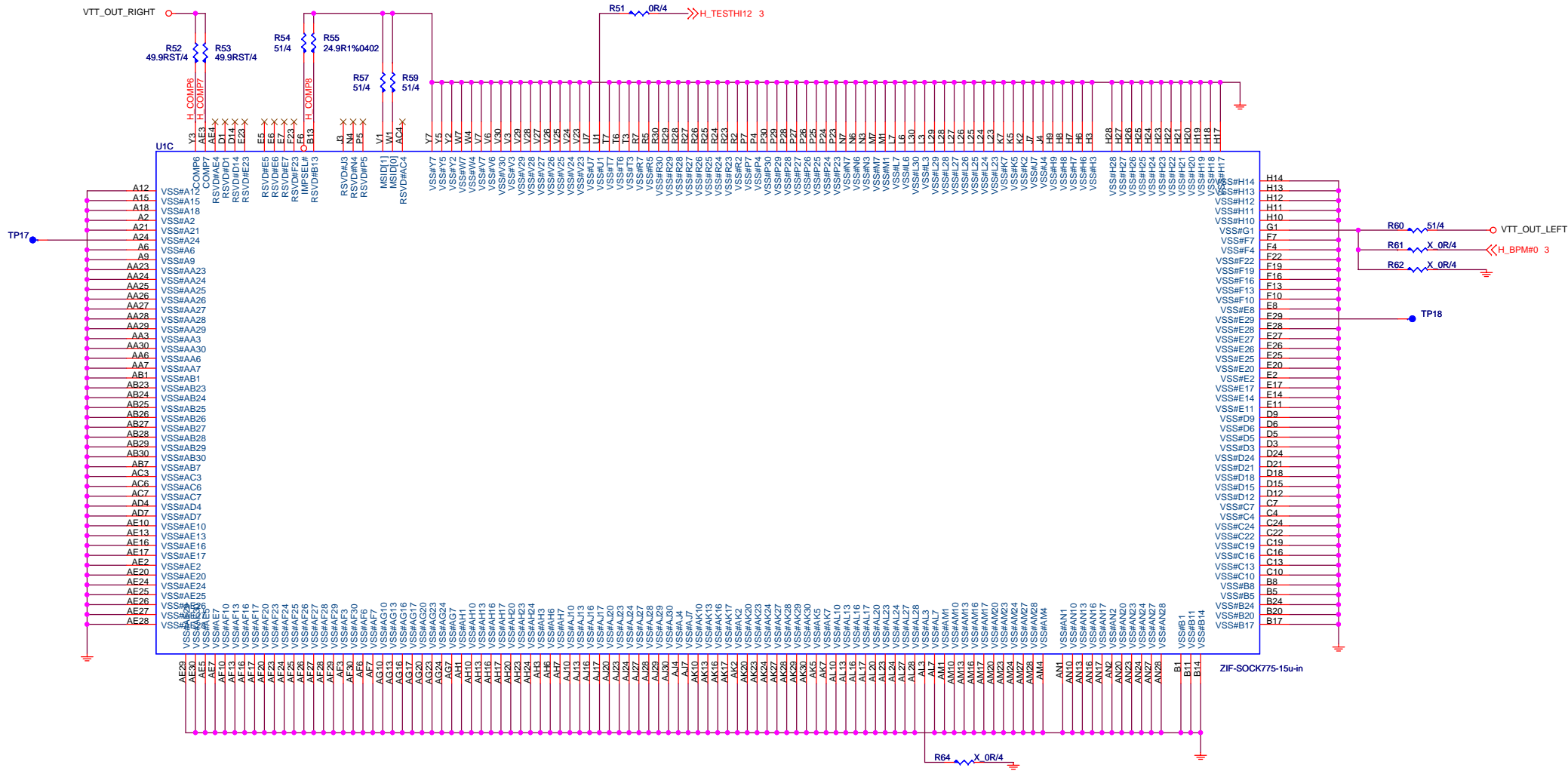
 MICRO-START INT'L CO.,LTD.			
Title: COVER SHEET			
Size	Document Number	Rev	
	MS-7402	10	
Date: Friday, October 19, 2007	Sheet	1	of 31

Block Diagram

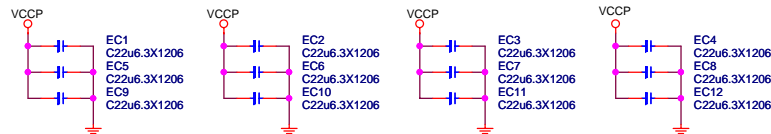


CPU SIGNAL BLOCK

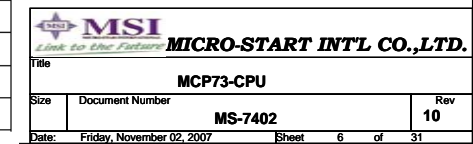


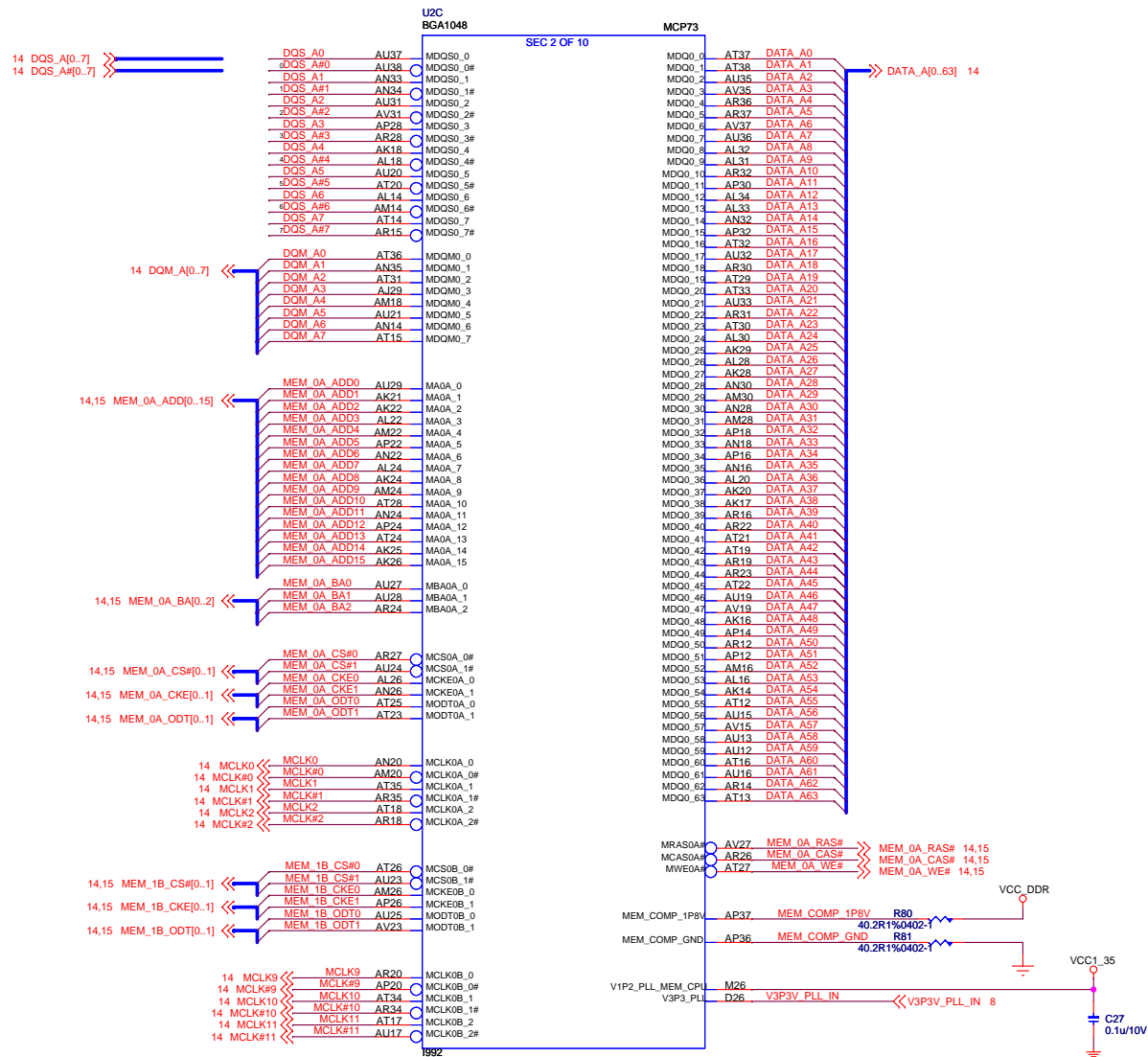


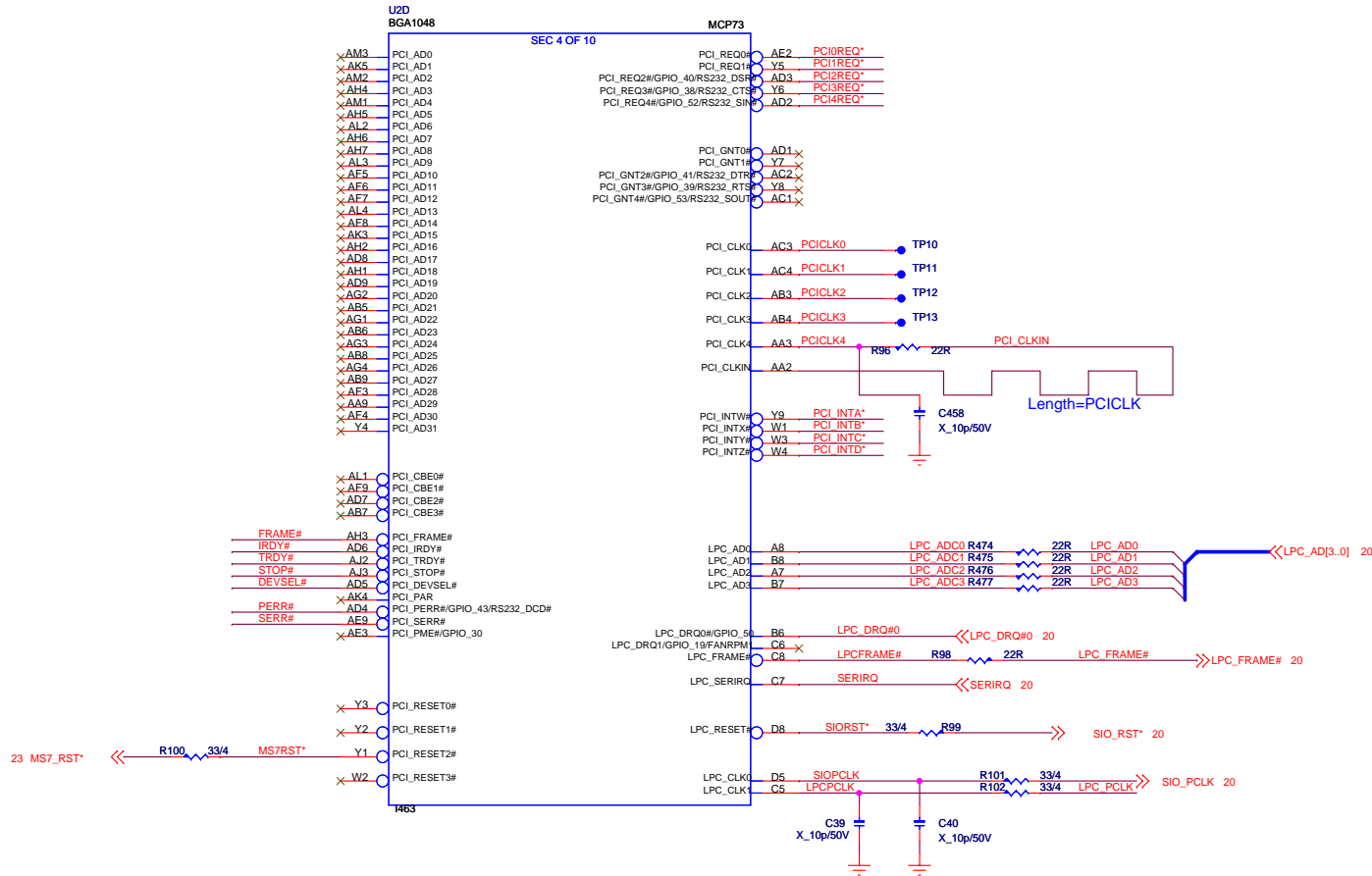
CPU DECOUPLING CAPACITORS



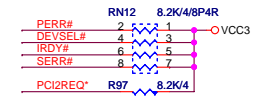
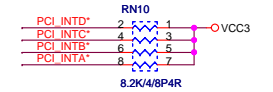
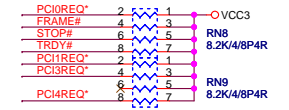
Place these caps within socket cavity



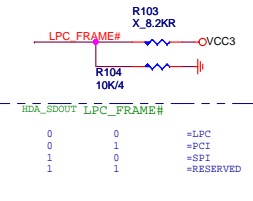




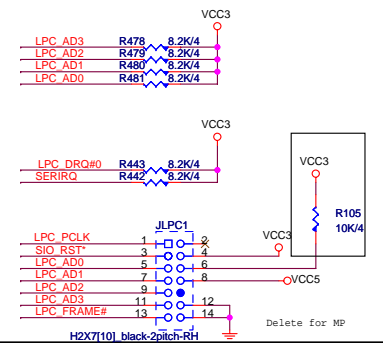
PCI PULLUP resistor

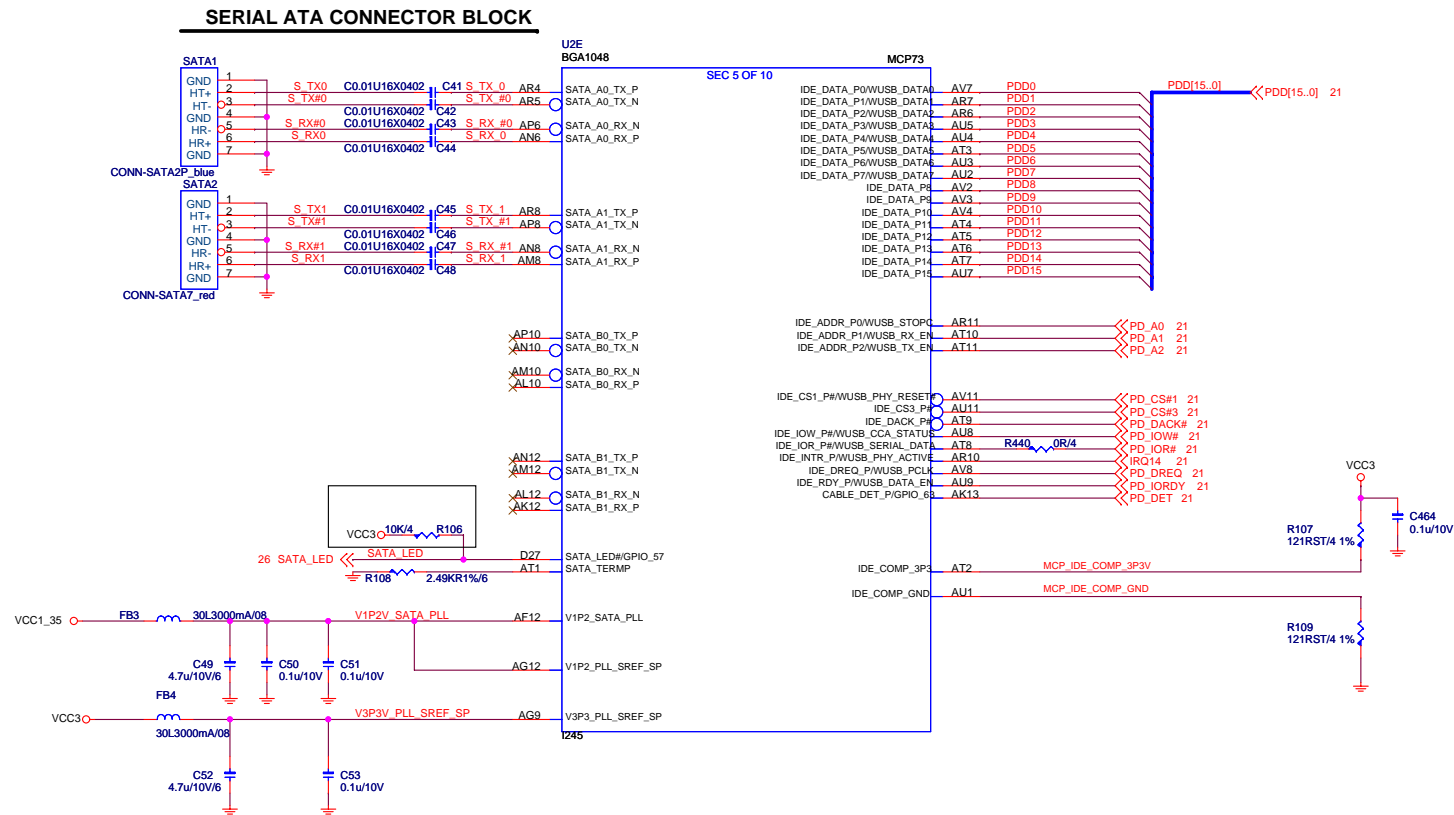


ROM mode strapping

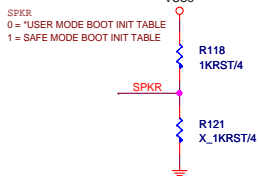
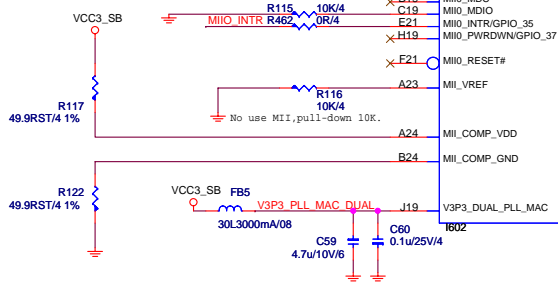
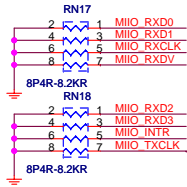
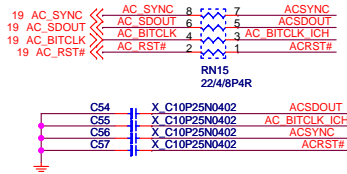


LPC DEBUG PORT



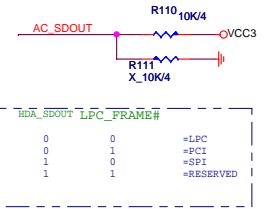


Codec damping resistor/EMI caps

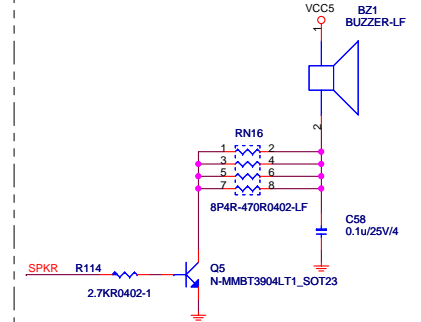


HDA_RESET#	Networking select	0: MII 1: ROM/EEP	Select an MII interface or an ROM/EEP interface for PNC.
		0: 14.31810 MHz 1: 24 MHz	Selects the Super I/O clock to be either 14.31810 MHz or 24 MHz.

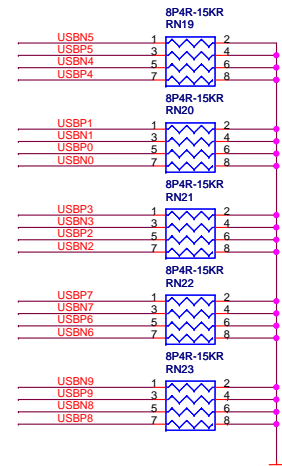
ROM mode strapping



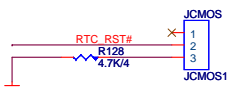
SPEAKER



For USB differential resistor

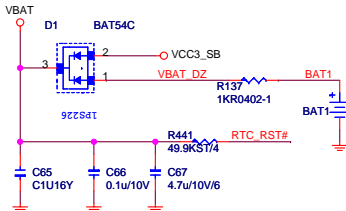


CLEAR CMOS JUMPER

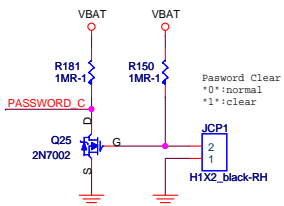


CMOS CLEAR	NORMAL	CLEAR
JBAT1	(1-2)	(2-3)

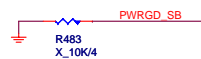
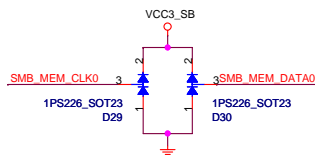
BATTERY



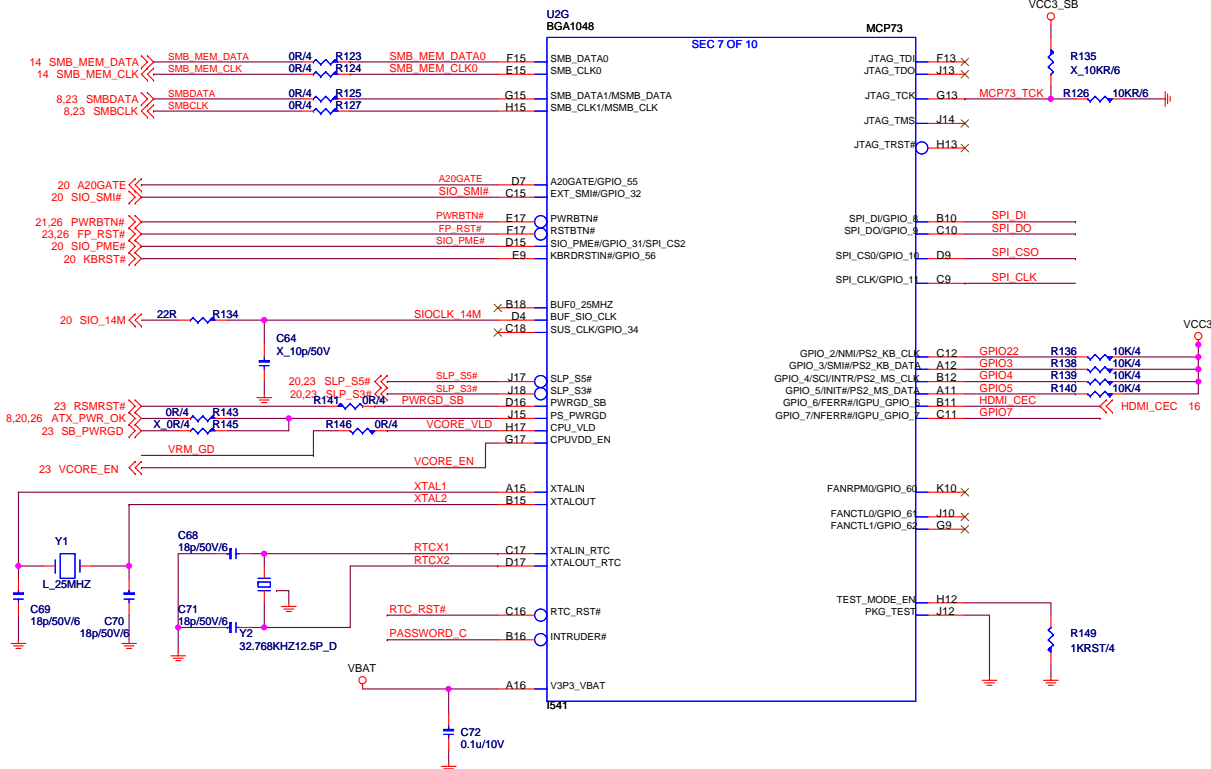
Clear password



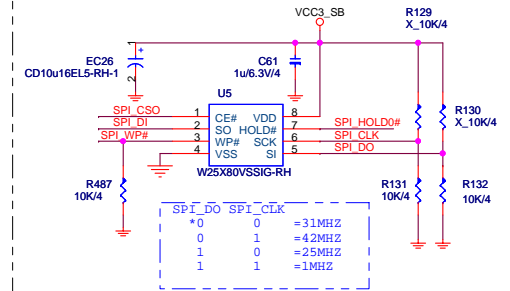
SMB ESD Protection Diodes



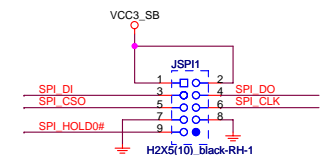
NVIDIA AP NOTICE



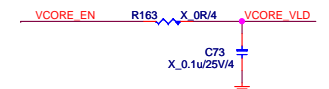
SPI FLASH ROM



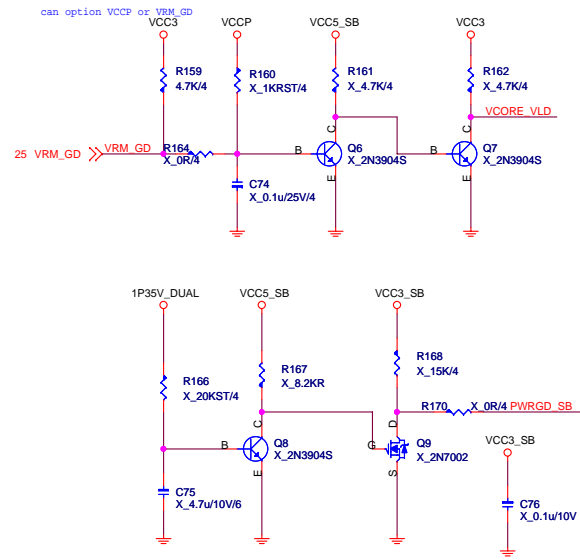
SPI DEBUG PORT

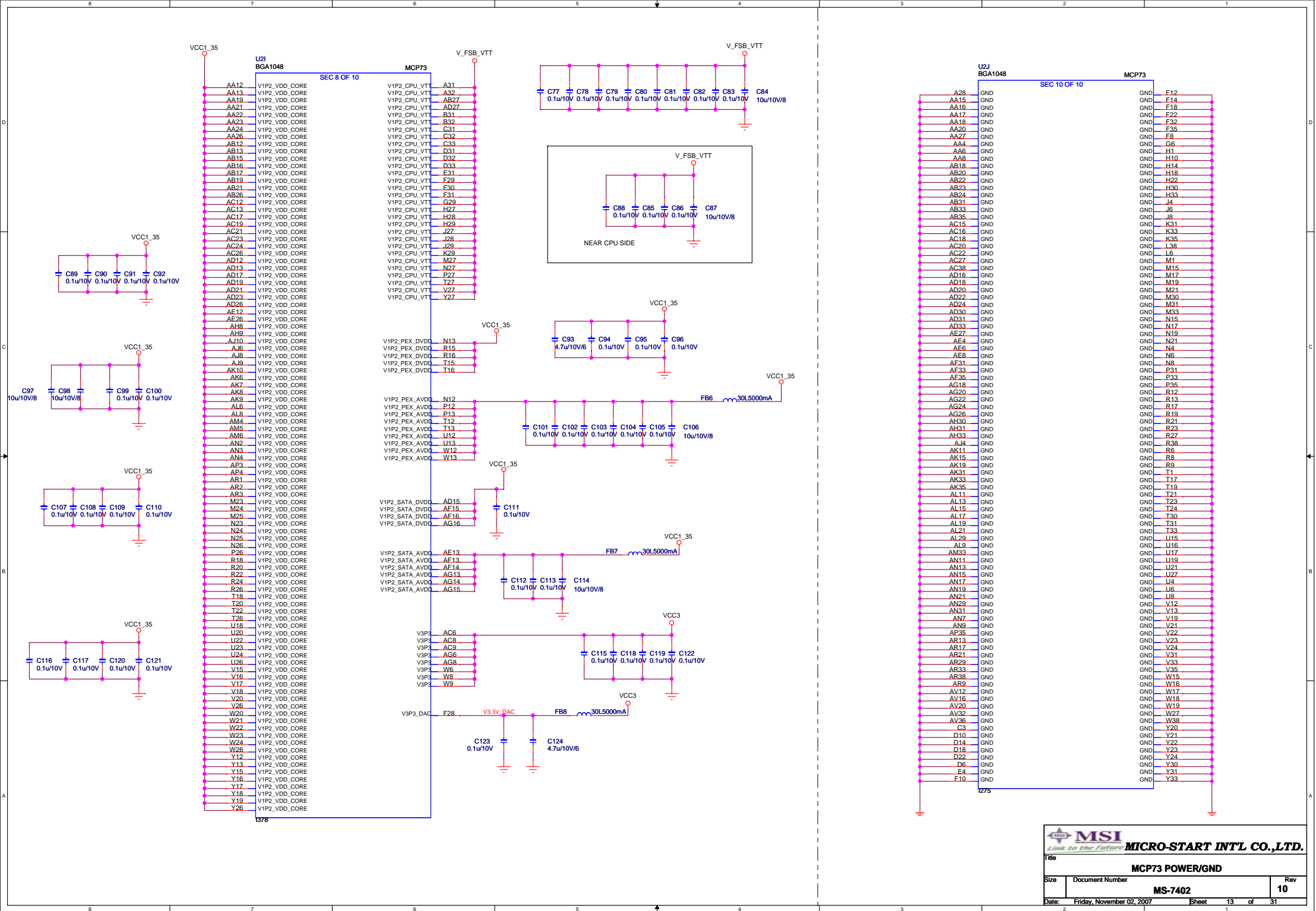


Part Number : N31-2051451-H06
Place close to SPI ROM





Vcore power-on sequence control circuit





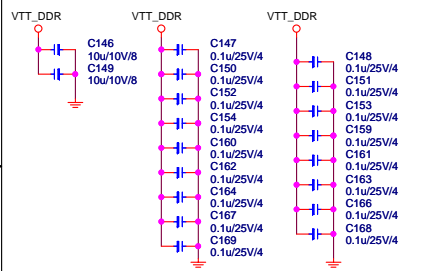


		MICRO-START INT'L CO.,LTD.
<i>Link to the Future</i>		
Title <div style="text-align: center; font-weight: normal;">DIMM1 DIMM2</div>		
Size	Document Number <div style="text-align: center; font-weight: normal;">MS-7402</div>	Rev <div style="text-align: center; font-weight: normal;">10</div>
Date: Friday, November 02, 2007 Sheet 14 of 31		

The top diagram illustrates the decoupling capacitor placement for a DDR memory module. It shows a circuit with two power pins, VCC_DDR and VTT_DDR, connected by four parallel capacitors. The capacitors are labeled C127, C128, C129, and C130, each with a value of 0.1u/25V/4. The capacitors are connected in parallel between the VCC_DDR and VTT_DDR pins.

The bottom diagram illustrates the decoupling capacitor placement for another DDR memory module. It shows a circuit with two power pins, VCC_DDR and VTT_DDR, connected by four parallel capacitors. The capacitors are labeled C131, C132, C133, and C134, each with a value of 0.1u/25V/4. The capacitors are connected in parallel between the VCC_DDR and VTT_DDR pins.

DIMM1/DIMM2 VTT decoupling



VCC_DDR

C172 10u/10V/8
C178 10u/10V/8
C318 10u/10V/8

VCC_DDR

C174 1u/16V/6
C177 1u/16V/6
C180 1u/16V/6

VCC_DDR

C173 0.1u/25V/4
C176 0.1u/25V/4
C179 0.1u/25V/4
C181 0.1u/25V/4
C182 0.1u/25V/4

VCC_DDR

C184
10u/10V/8

C187
10u/10V/8

VCC_DDR

C185
1u/16V/6

C188
1u/16V/6

C191
1u/16V/6

VCC_DDR

C183
0.1u/25V/4

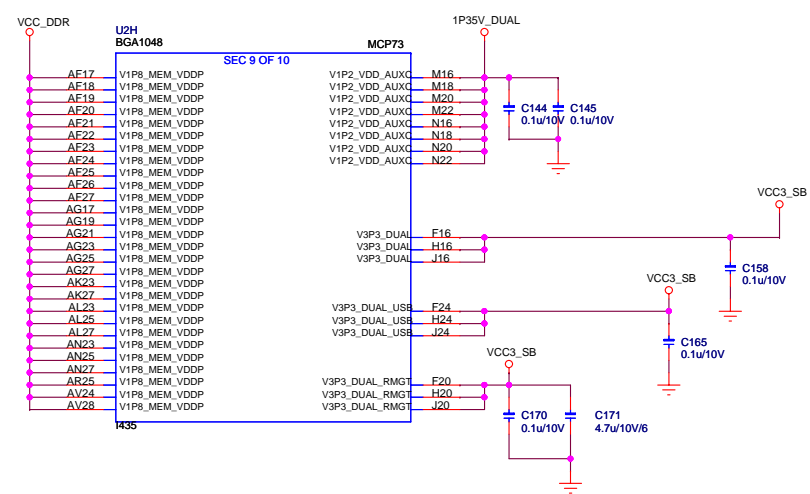
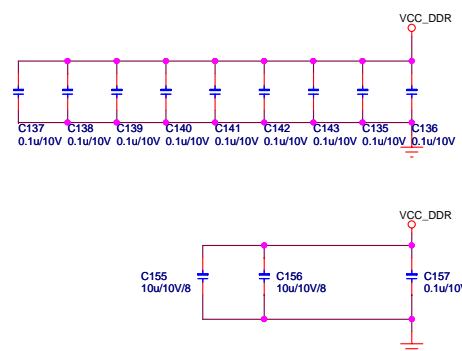
C186
0.1u/25V/4

C189
0.1u/25V/4

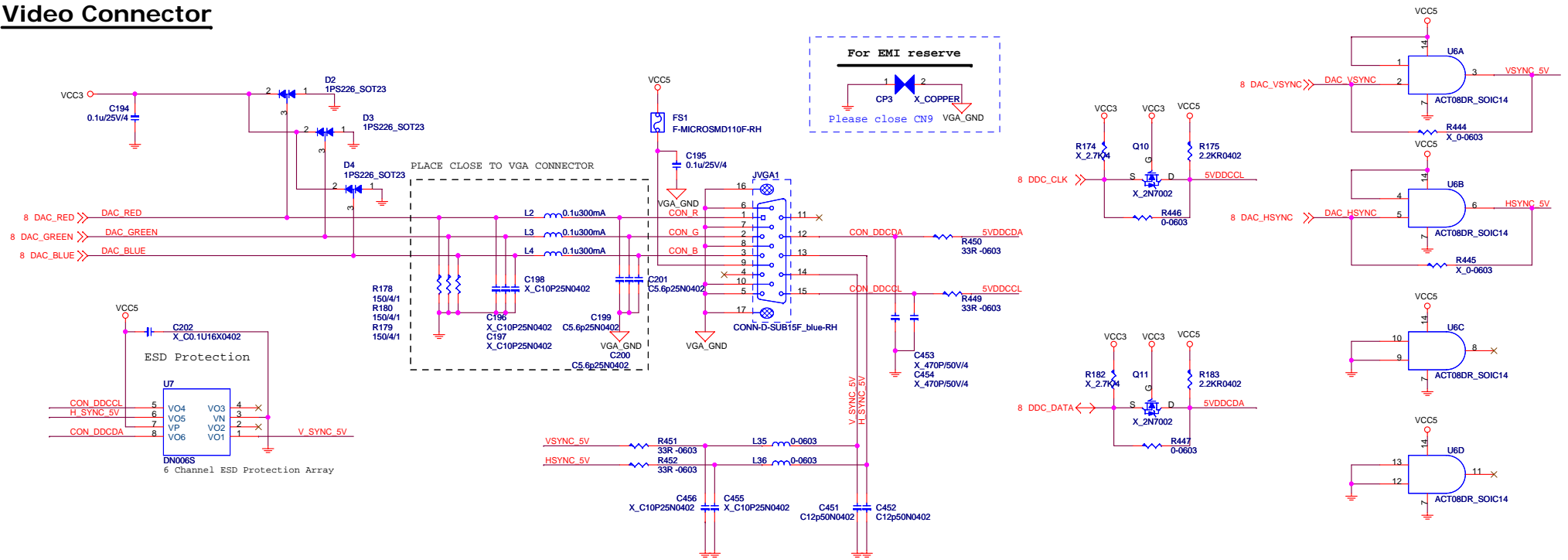
C192
0.1u/25V/4

C193
0.1u/25V/4

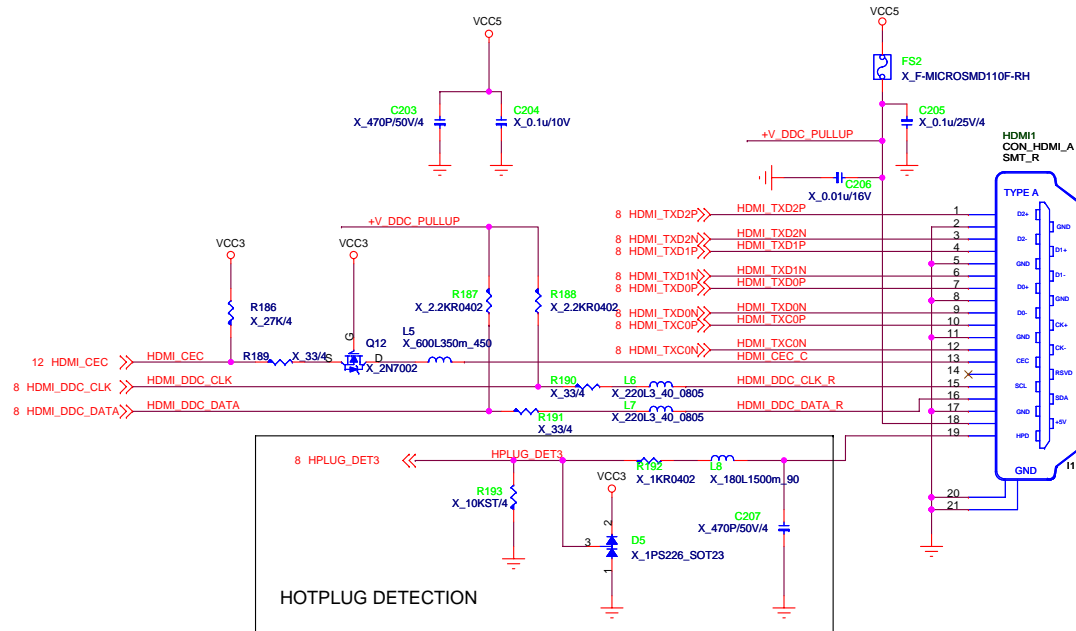
Pin	Memory Address	Output Signal
1	MEM_0A_ADD1	RN24
2	MEM_0A_ADD2	47/4/8P4R
3		
4		
5		
6	MEM_0A_ADD5	
7	MEM_0A_ADD6	RN25
8	MEM_0A_ADD4	47/4/8P4R
9	MEM_0A_ADD3	
10	MEM_0A_ADD11	
11	MEM_0A_ADD7	RN26
12	MEM_0A_ADD9	47/4/8P4R
13	MEM_0A_ADD8	
14	MEM_0A_BA2	
15	MEM_0A_ADD14	
16	MEM_0A_ADD15	RN27
17	MEM_0A_ADD12	47/4/8P4R
18	MEM_0A_ADD0	
19	MEM_0A_BA1	
20	MEM_0A_ADD10	RN28
21	MEM_0A_BA0	47/4/8P4R
22	MEM_0A_CS#1	
23	MEM_1B_ODT1	RN29
24	MEM_0A_ODT4	47/4/8P4R
25	MEM_1B_CS#1	
26	MEM_0A_CS#0	
27	MEM_0A_RAS#	RN30
28	MEM_0A_WE#	47/4/8P4R
29	MEM_1B_CS#0	
30		
31	MEM_0A_CKE0	
32	MEM_0A_CKE1	RN31
33	MEM_1B_CKE0	47/4/8P4R
34	MEM_1B_CKE1	
35	MEM_0A_CAS#	
36	MEM_0A_ODT0	RN32
37	MEM_0A_ODT0	47/4/8P4R
38	MEM_0A_ADD13	



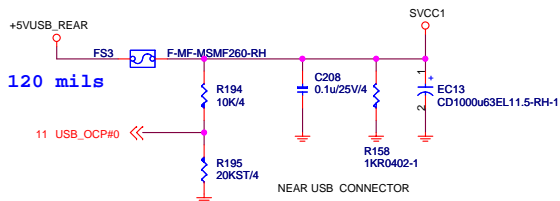
Video Connector



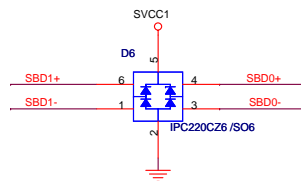
HDMI Connector



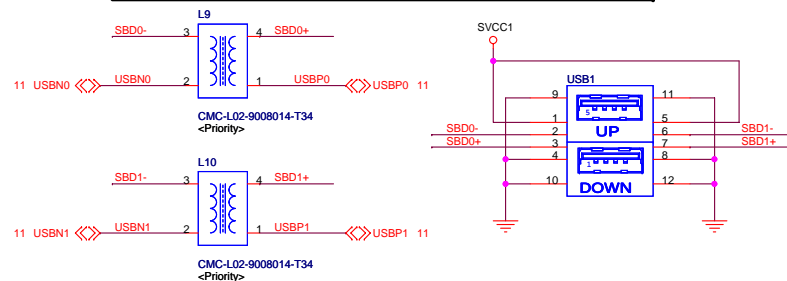
POWER CIRCUIT FOR USB PORT 0,1



ESD Protection



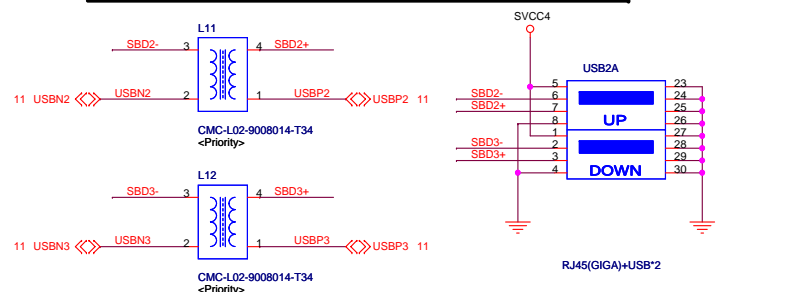
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



NEAR USB CONNECTOR

N53-08M0011-F02

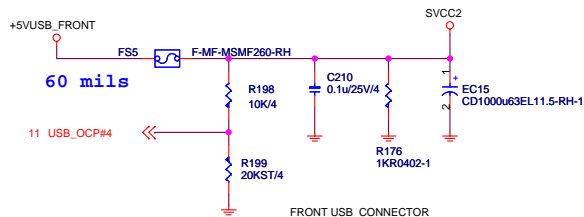
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



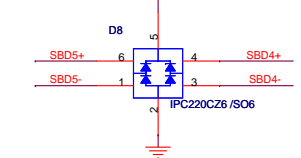
NEAR USB CONNECTOR

RJ45(GIGA)+USB*2

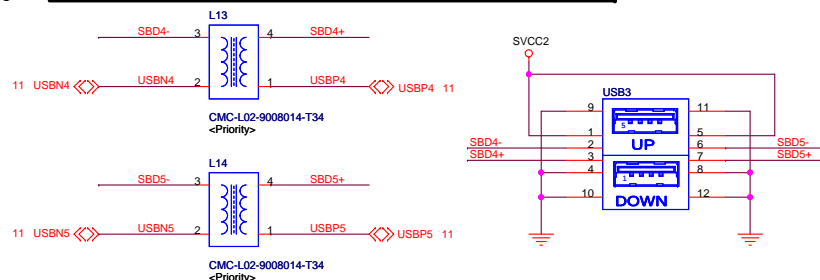
POWER CIRCUIT FOR USB PORT 6,7



ESD Protection

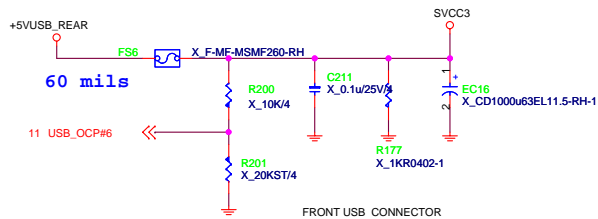


FRONT PANEL USB CONNECTOR FOR USB PORT6,7

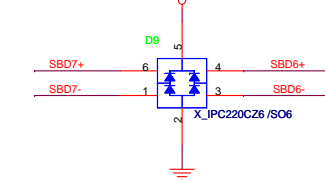


NEAR USB CONNECTOR

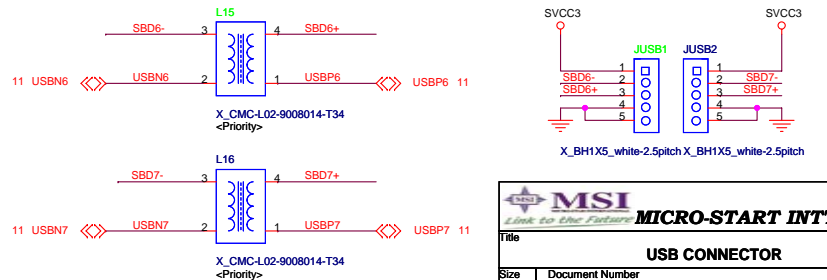
POWER CIRCUIT FOR USB PORT 2,3




ESD Protection



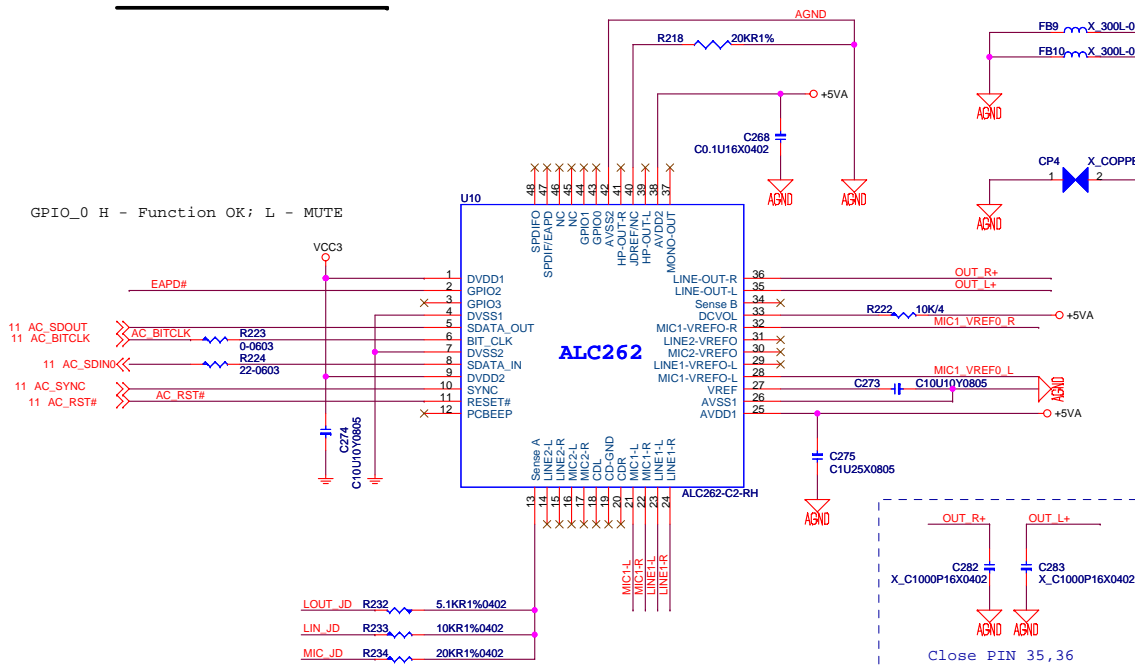
Memory card reader USB CONNECTOR FOR USB PORT 2,3



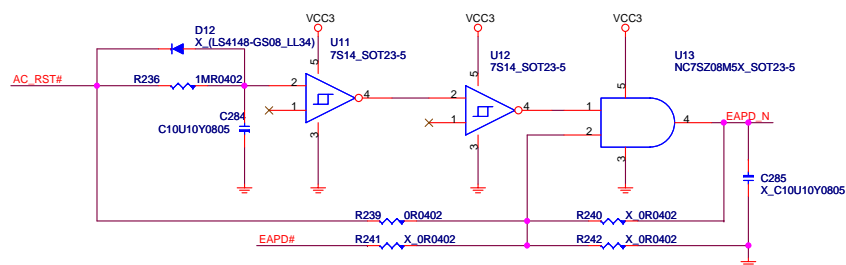
NEAR USB CONNECTOR

 MICRO-START INT'L CO.,LTD.		
USB CONNECTOR		
Size	Document Number	Rev
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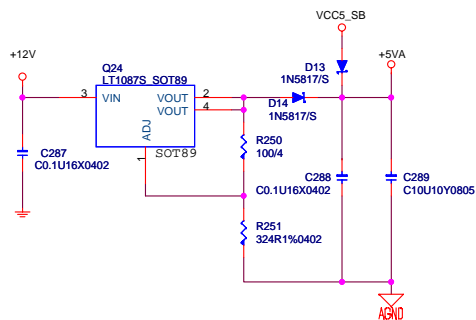
Reltek HD ALC262



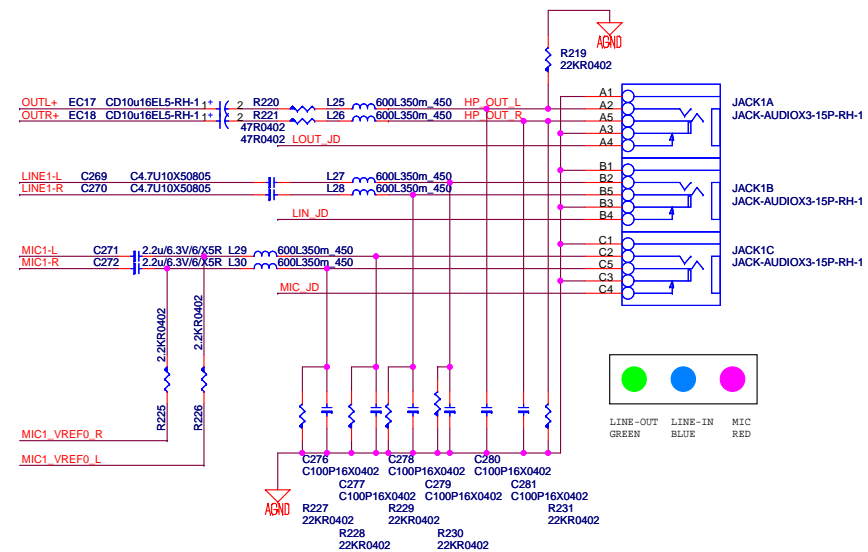
POP noise circuit



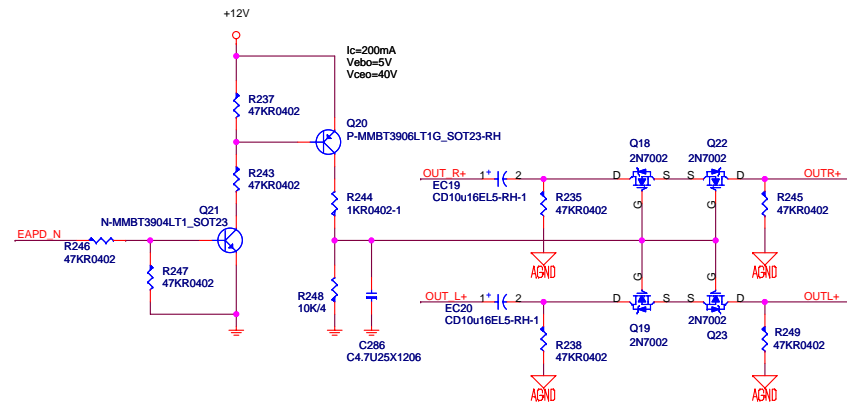
AUDIO CODE REGULATORS

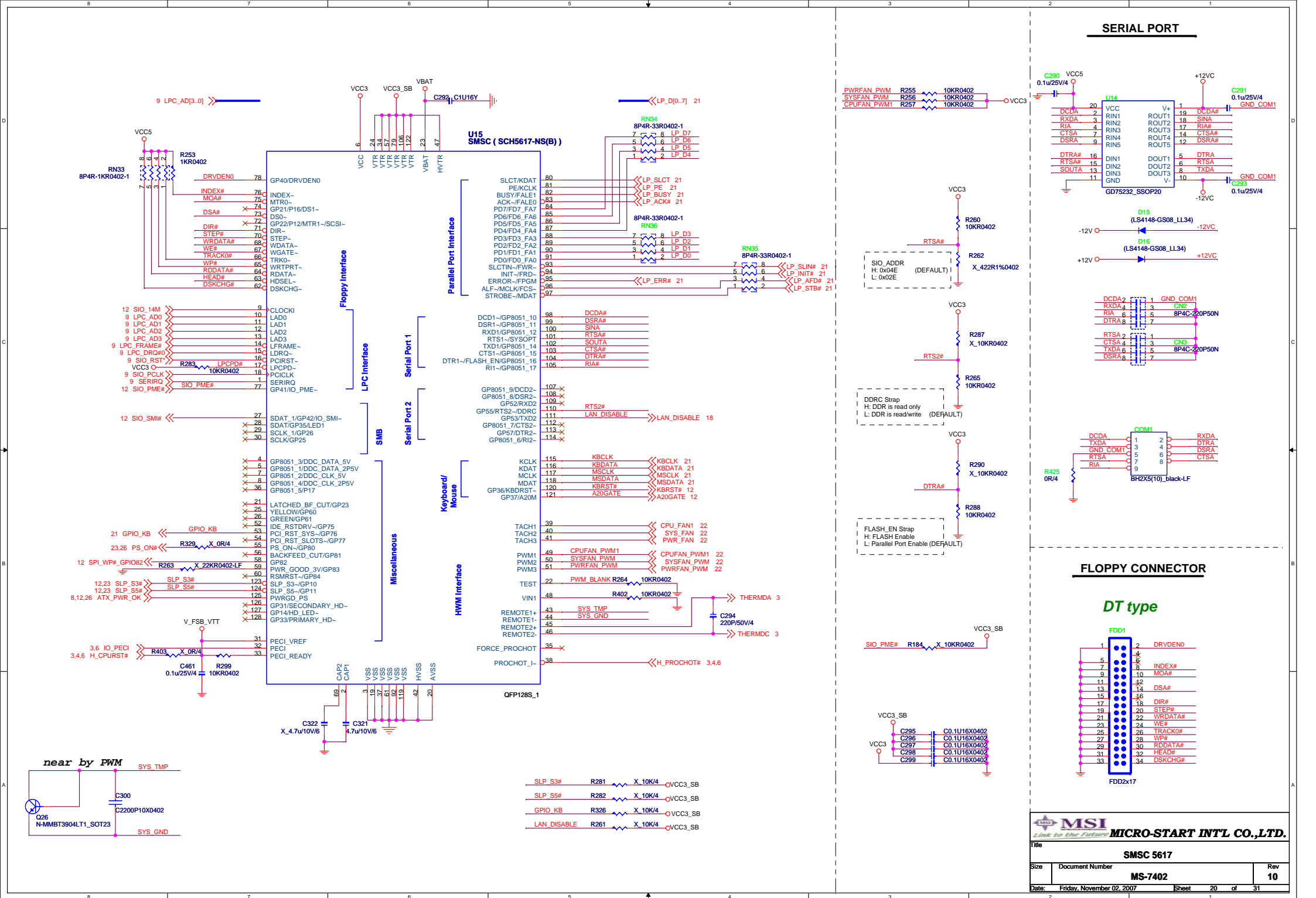


PHONE JACK.

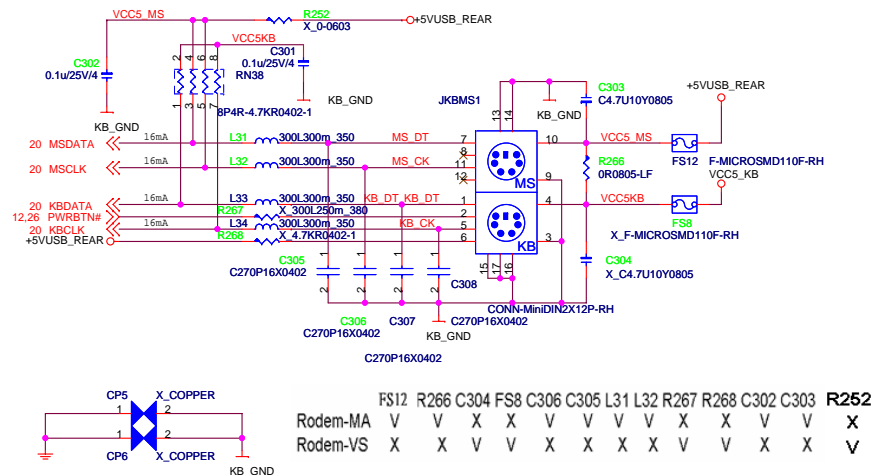


Smooth pop noise circuit for Line-out

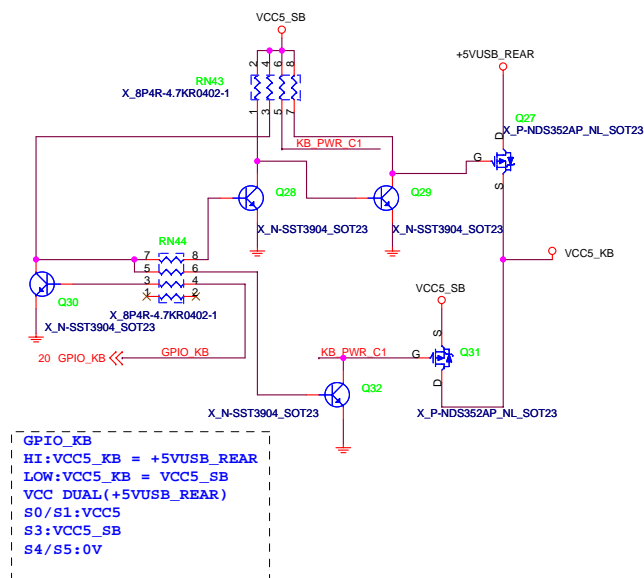




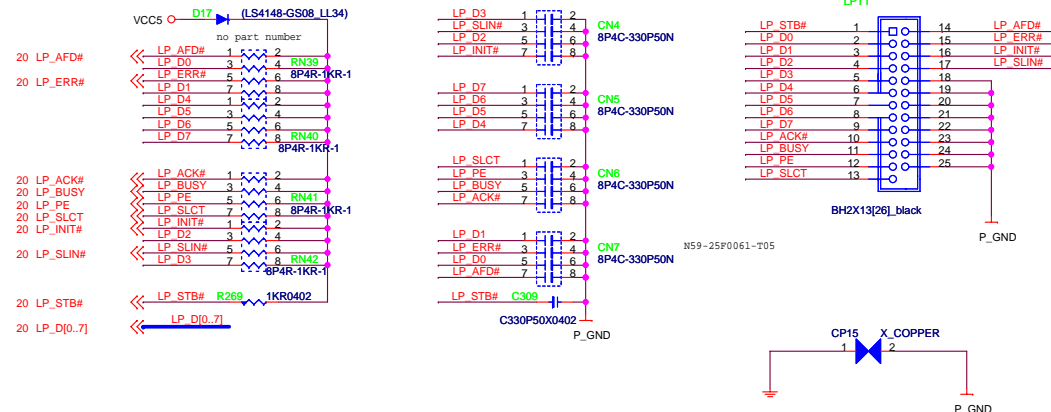
PS2 KEYBOARD & MOUSE CONNECTOR



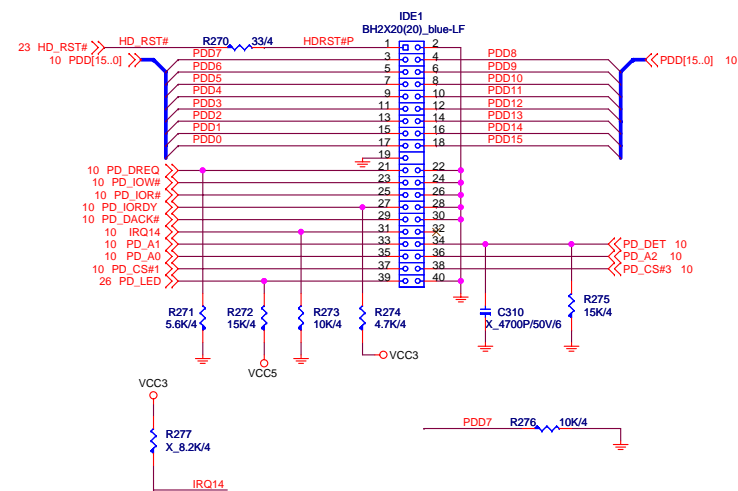
K/B Power supply function for Rodem-VS



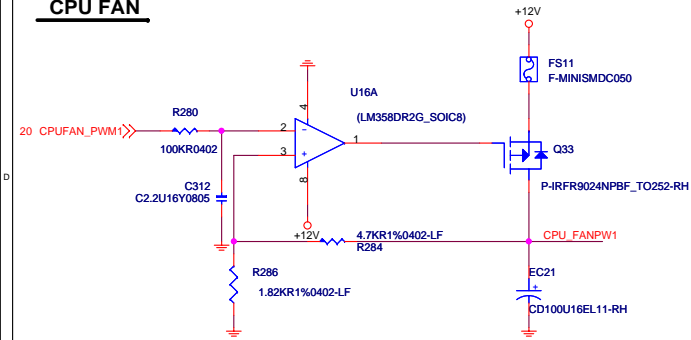
PARALLAL PORT



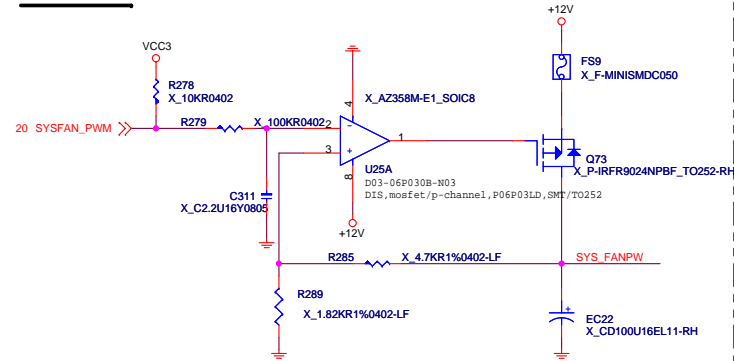
IDE connector



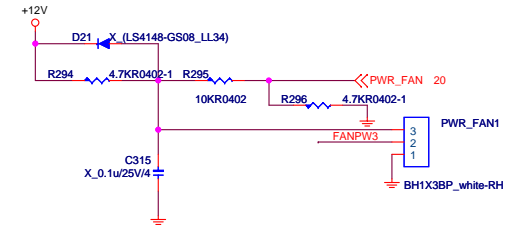
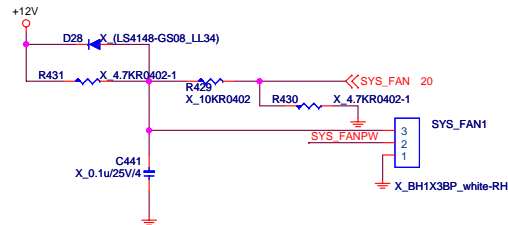
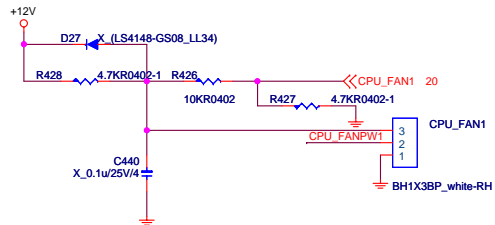
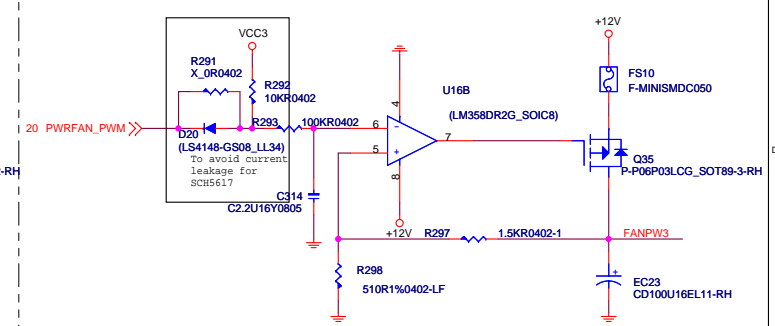
CPU FAN



SYS FAN



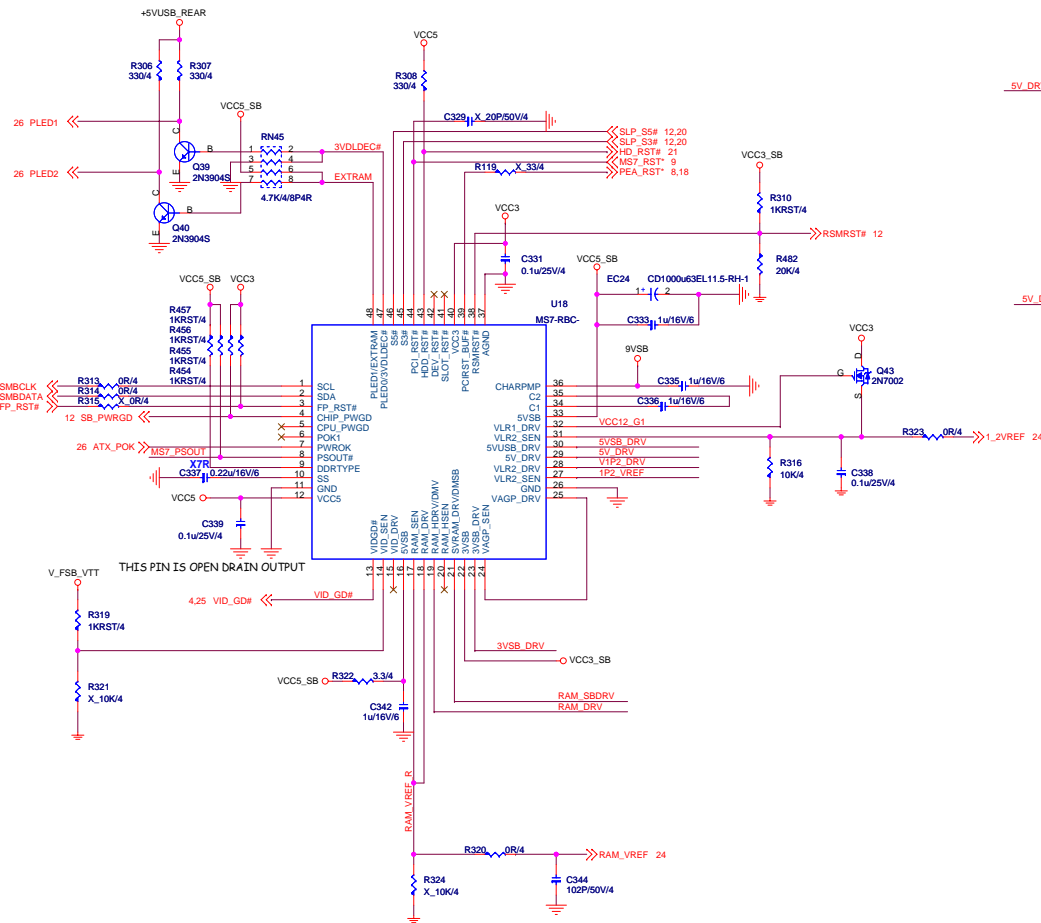
PWR FAN



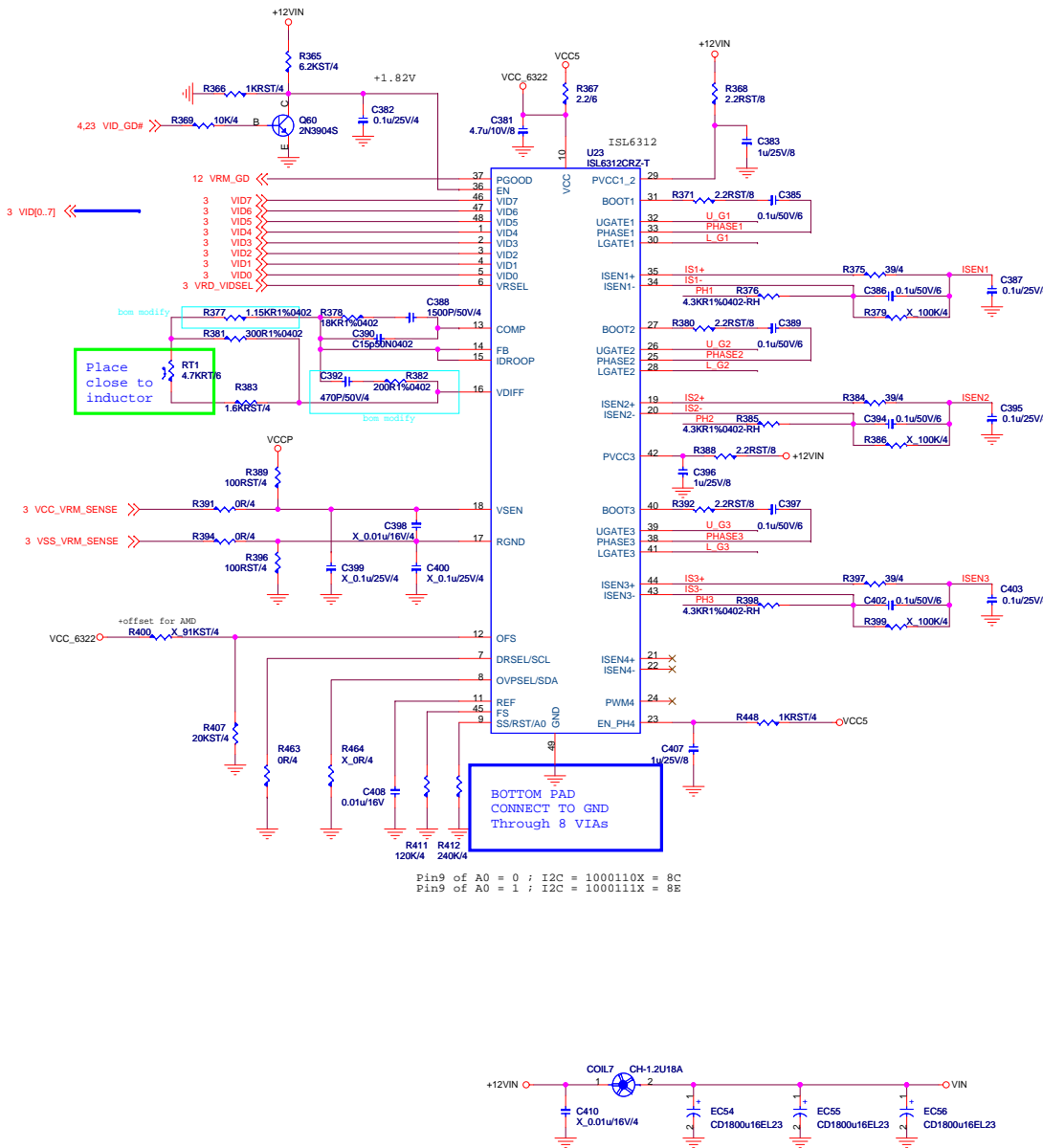
VDIMM LINEAR OR PWM SELECT	
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
EXTERNAL PWM OR LINEAR REGULATOR	PULL HIGH

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

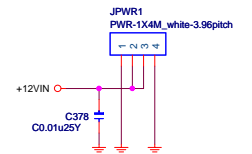
DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

[illegible][illegible]

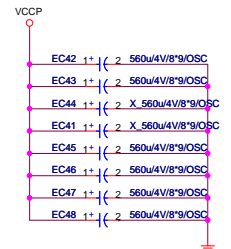
Voltage Regular Module



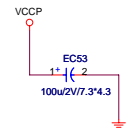
ATX12V Power Connector



OS-CON Capacitors

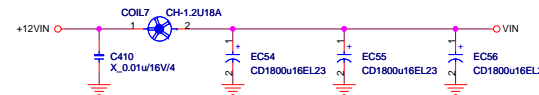


SP Capacitors



TPD:06B

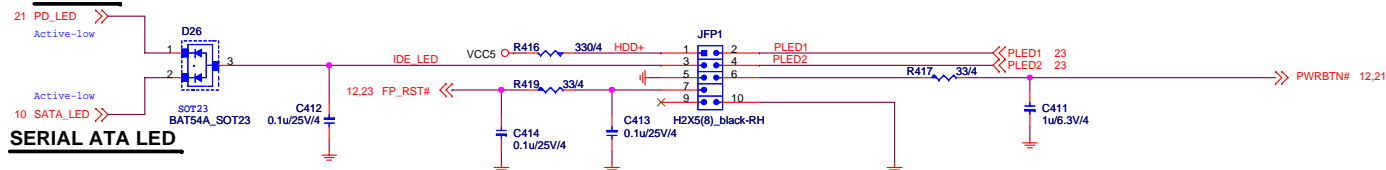
CP25,CP26,CP27,CP28 PLACE ON THE SOLDER SIDE, CLOSE TO INDUCTOR



ATX connector / Front Panel

Front Panel

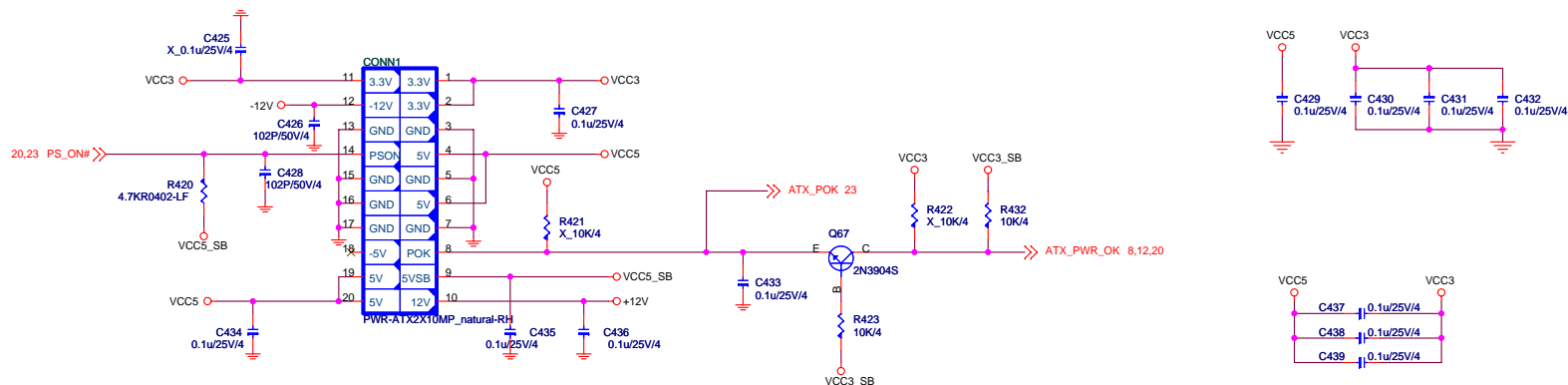
IDE LED



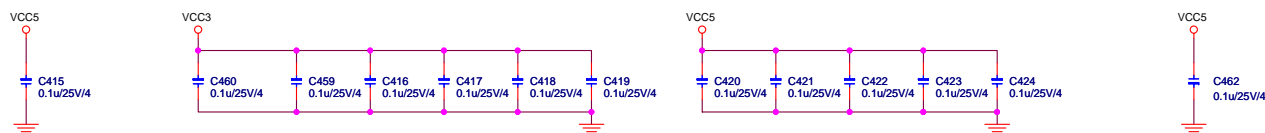
ME switch cable color
dification

Switch+	white
Switch-	black
PLED1(+)	blue
PLED1(-)	green
HD(+)	yellow
HD(-)	brown

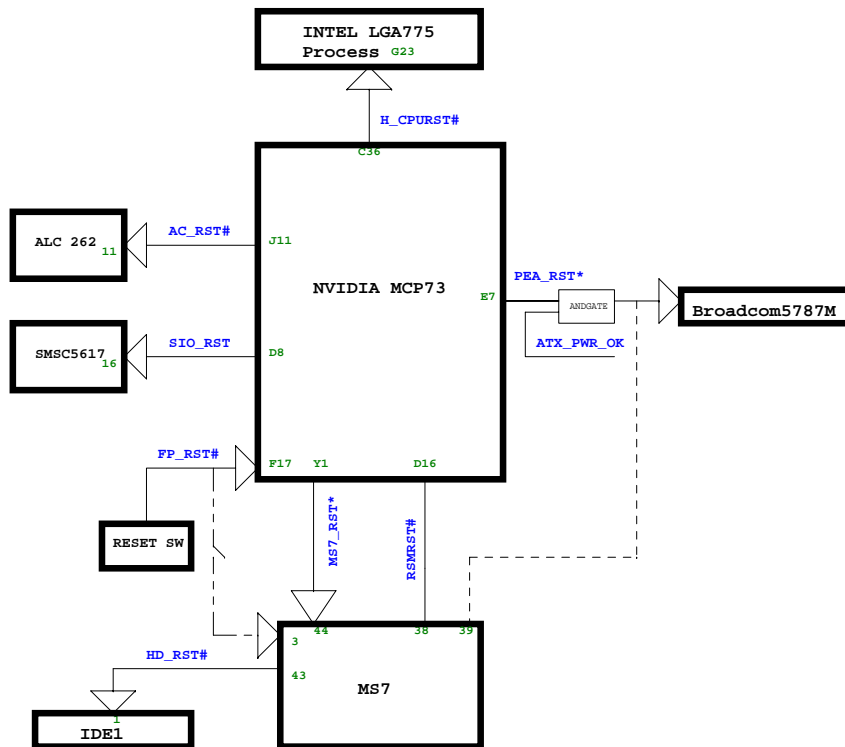
ATX Connector



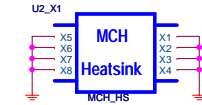
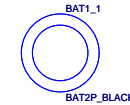
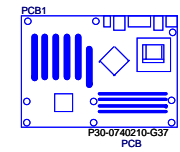
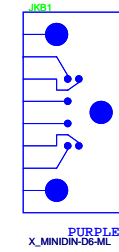
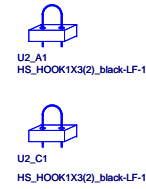
For EMI reserve



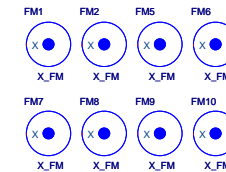
RESET MAP



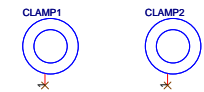
MANUAL PARTS



Optics Orientation Holes



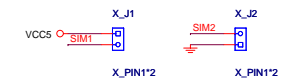
For power cable holder and FP:
HOLES315D189



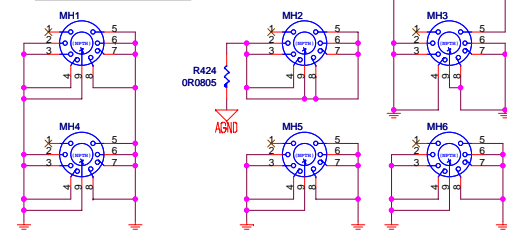
Jumper setting



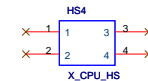
Simulation



Mounting Holes

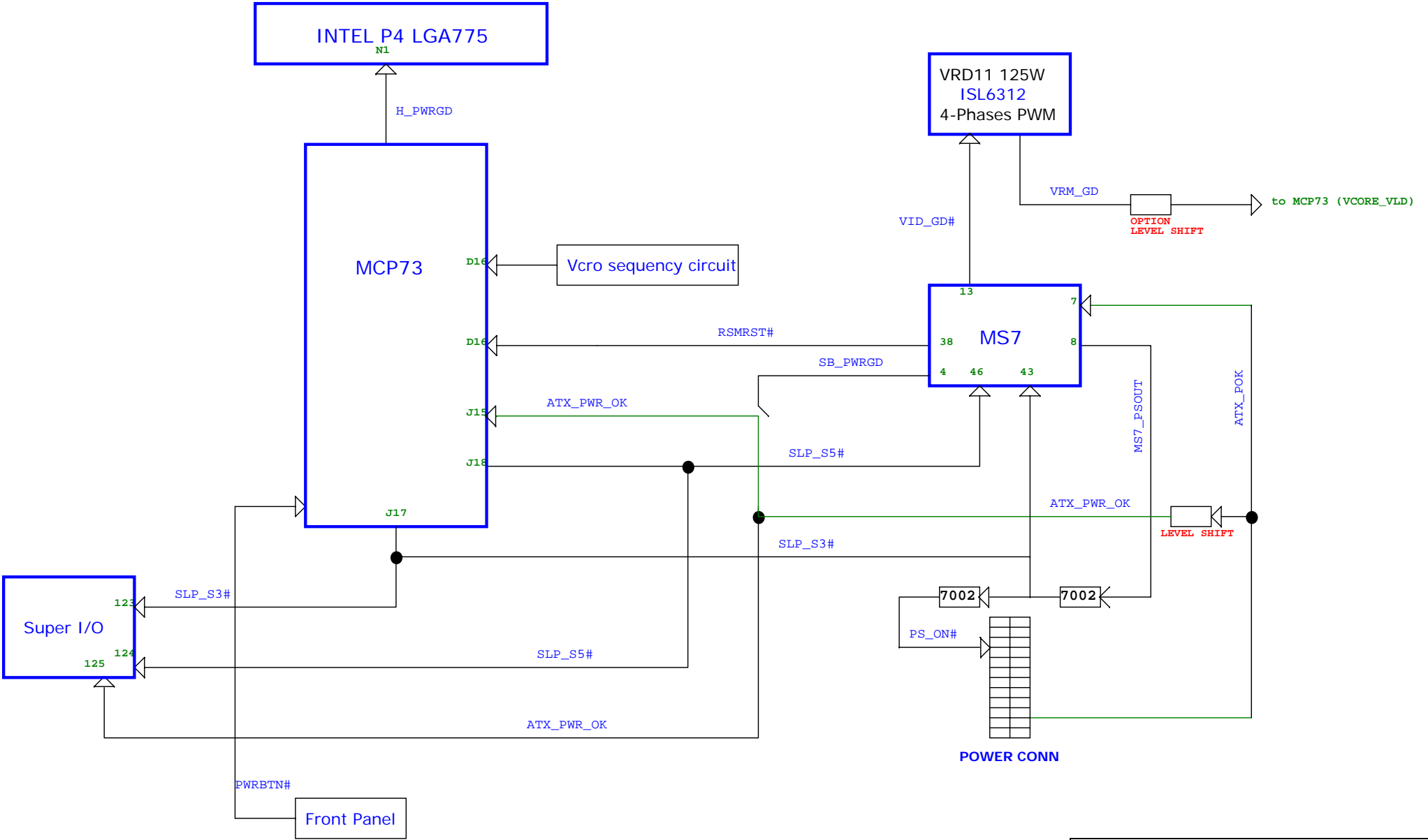


CPU Cooling Holes



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PWROK MAP



NVIDIA MCP73

GPIO Pin	Default States	Function	Change default	Pin-out
GPIO 2	GPIO INPUT	Pull-up to VCC3 with 10K		C1
GPIO 3	GPIO INPUT	Pull-up to VCC3 with 10K		C2
GPIO 4	GPIO INPUT	Pull-up to VCC3 with 10K		C3
GPIO 5	GPIO INPUT	Pull-up to VCC3 with 10K		C4
GPIO 6	GPIO INPUT	HDMI_CEC,Pull-up to VCC3 with 10K		C5
GPIO 7	GPIO INPUT	pull_up to VCC3 with 10K		C6
GPIO 8	TER FUNCT.	SPI_DI		C7
GPIO 9	TER FUNCT.	SPI_DO		C8
GPIO 10	TER FUNCT.	SPI_DCS0		C9
GPIO 11	TER FUNCT.	SPI_CLK		CA
GPIO 19	GPIO INPUT	NC		D2
GPIO 20	PRI FUNCT.	H_PROCHOT#,pull-up to VTT_OUT_RIHGHT with 10K		D3
GPIO 21	PRI FUNCT.	WAKE_UP#		D4
GPIO 22	PRI FUNCT.	AC_SDINO		D5
GPIO 23	PRI FUNCT.	Pull-up to VCC3_SB with 10K directly	SEC Function,GPIO OUTPUT	D6
GPIO 24	PRI FUNCT.	NC		D7
GPIO 25	PRI FUNCT.	OC#0 connect to USB connector		D8
GPIO 26	PRI FUNCT.	OC#2 connect to USB connector		D9
GPIO 27	PRI FUNCT.	OC#4 connect to USB connector		DA
GPIO 28	PRI FUNCT.	OC#6 connect to USB connector		DB
GPIO 29	PRI FUNCT.	LPM_LAN,pull_up 3VDUAL with 10K	SEC Function,GPIO OUTPUT	DC
GPIO 30	PRI FUNCT.	PME#,Pull-up to 3VDUAL with 8.2K		DD
GPIO 31	PRI FUNCT.	SIO_PME#,Internal pull-up to 3VDUAL		DE
GPIO 32	PRI FUNCT.	SIO_SMI#,Internall pull-up to 3VDUAL		DF
GPIO 34	PRI FUNCT.	SUS_CLK		E1
GPIO 35	PRI FUNCT.	Pull-low to GND with 10K	SEC Function,GPIO OUTPUT	E2
GPIO 36	PRI FUNCT.	Connect to GND		E3
GPIO 37	PRI FUNCT.	NC		E4
GPIO 38	GPIO INPUT	PCI3REQ#,Pull-up to VCC3 with 8.2K		E5
GPIO 39	GPIO OUTPUT	NC		E6
GPIO 40	GPIO INPUT	PCI2REQ#,Pull-up to VCC3 with 8.2K		E7
GPIO 41	GPIO OUTPUT	NC		E8
GPIO 42	PRI FUNCT.	PCICLKRUN#		E9
GPIO 43	GPIO INPUT	PERR#,Pull-up to VCC3 with 8.2K		EA
GPIO 44	PRI FUNCT.	ACSYNC		EB
GPIO 45	PRI FUNCT.	ACSDOUT,Pull-up to VCC3 with 8.2K		EC
GPIO 50	PRI FUNCT.	LPC_DRQ#0,Pull-up to VCC3 with 10K		F1
GPIO 52	GPIO INPUT	PCI4REQ#,Pull-up to VCC3 with 8.2K		F3
GPIO 53	GPIO OUTPUT	NC		F4
GPIO 55	PRI FUNCT.	A2OGATE,Pull-up to VCC3 with 8.2K		F6
GPIO 56	PRI FUNCT.	KBRST#,Pull-up to VCC3 with 8.2K		F7
GPIO 57	PRI FUNCT.	SATA_LED,Pull-up to VCC3 with 8.2K		F8
GPIO 58	PRI FUNCT.	Thermtrip#		F9
GPIO 59	PRI FUNCT.	Therm#		FA
GPIO 60	PRI FUNCT.	NC		FB
GPIO 61	PRI FUNCT.	NC		FC
GPIO 62	PRI FUNCT.	NC		FD
GPIO 63	PRI FUNCT.	PD_DET,Pull-down to GND with 15K		FE

PRI FUNCT.:Primary Function
SEC FUNCT.:Second Function
TER FUNCT.:Tertiary Function

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 2	0A2H	MCLK_A9/MCLK_A9# MCLK_A10/MCLK_A10# MCLK_A11/MCLK_A11#

SIO SCH5617


PIN NAME	PIN#	USAGE	Input/Output
GP57	113	GPIO_KB	OUTPUT
GP42	27	SIO_SMI#	OUTPUT
GP41	77	SIO_PME#	OUTPUT
GP82	58	SPI_WP#_GPIO82	OUTPUT

SMBus DISTRIBUTION

SMBus	Power	Load
SMBCLK	3VDUAL	MCP73,MS7,PWM
SMB_MEM_CLK	VCC3	DIMM

JUMPER SETTING

JBAT1	(1-2)Normal	(2-3)Clear
JCP1	(1-2) open clear	(1-2)short normal
JCMOS	(1-2) Normal	(2-3) Clear



MICRO-START INT'L CO.,LTD.

Title GPIO & JUMPER SETTING		
Size	Document Number MS-7402	Rev 10
Date: Sunday, October 21, 2007 Sheet 29 of 31		

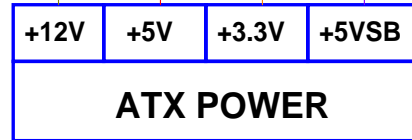
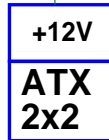
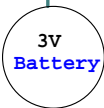
INTEL 775		
0.8375V - 1.6000V Core	-	84A
1.2V FSB Vtt	-	5.3A

MCP73		
V1P2_CPU_VTT	-	800mA
H_VCCPLL	-	200 mA
V1P2_SATA_PLL	-	75mA
V1P2_VDD_CORE	-	5.7A
V1P2_PEX_DVDD	-	450mA
V1P2_PEX_AVDD	-	1.8A
V1P2_VDD_AUXC	-	25mA
3P3_DUAL_RMGT	-	35mA
V3P3_DUAL	-	50mA
3P3_DUAL_USB	-	75mA
V3P3_BAT	-	3mA
V1P2_PLL_MEM_CPU	-	60mA
V1P2_PEX0/1_PLL	-	170mA
V1P2_SATA_DVDD	-	95mA
V1P2_SATA_AVDD	-	380mA
V3P3	-	340mA
V3P3_DAC	-	130mA
V3P3_HDMI_IO	-	60mA

Audio		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

SPI		
+3.3V (S0,S1)	-	30mA

5VAudio		
+5VR	-	500mA



ISL6322		
VCCP	VRM 11	
0.8375V-1.6000V	84A	
3-Phase	Switch	

W83310DS		
VTT_DDR	0.9V	Linear 1A

MS7 Regulator		
V_FSB_VTT	1.2V	Linear 10A

3VDUAL		
3.3V	Linear	1.5A
5VUSB_REAR/FRONT		
5V	Linear	2A / 2A
5VSB		500mA
5VDIMM		
5V		11.24A
5VSB		700mA

LT1087		
1P35V_DUAL	Linear	300mA

LT1087		
CPU_VCC_PLL	3.3V	Linear 200mA

MS11 Regulator		
VCC1_35	1.2V	Switch 15A

MS11 Regulator		
VCC_DDR	1.8V	Switch 20A

DDR DIMM & TERMINATOR		
0.9V VTT_DDR	-	1A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA
MCP73		
V3P3_HDMI_PLL	-	10mA
V3P3_PLL	-	30mA
V1P8_MEM_VDDP	-	2.4A
V1P2_PEX0/1_PLL	-	45mA
V1P2_PLL_SREF_SP	-	10mA
V3P3_PLL_COREPLL	-	5mA
V3P3_VPLL	-	5mA
V3P3_XREF0/1_XS0/1	-	21mA
V3P3_PLL_SREF_SP	-	15mA
V3P3_DUAL_PLL_MAC	-	5mA

PCI Express x1 slot(BCM5787M)		
VLAN12	-	590mA
VLAN25	-	235mA
VDD	-	7mA

USB		
+5V (S0,S1)	-	4.0A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

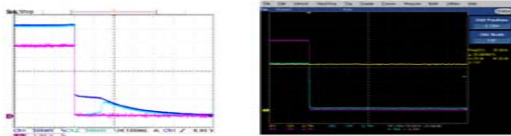
SIO		
3VDUAL	-	10mA

0A====>0B 2007.06.14

- 1.change super I/O from SMSC5017 to SMSC5617(for future CPU have support PECI)
- 2.del ALARM signal(page11)(SMSC5617 limitation)
- 3.del R135 & signal SUSCLK(page12)(SMSC5617 limitation)
- 4.del signal HWM_INT and rename to GPIO7(page12)(SMSC5617 limitation)
- 5.SPI WP# change to SPI_WP#_GPIO82(page12)(for spi rom hardware write protect)
- 6.BOM R43 62ohm change to 200ohm(nvidia checklist v05 request)
- 7.BOM R69,R70,R73,R75 33ohm change to 0ohm & R71,R72,R74,R76 unmount(nvidia checklist v05 request)
- 8.change U21 library to N-SOP8L_150PAD90 (for solder issue)
- 9.JCMOS reverse 180 degree (for mechanical request)
- 10.CLEAR PASSWORD connect to MCP73's pin:B16 intruder#
- 11.del CP2 & add C462,modify CP16&CP17 GND to GND for EMI
- 12.HS4 change to dummy net
- 13.BOM BAT1_1 change to N91-01F0151-L06(BOM error)
- 14.BOM H4 change to E24-6406200-K23(BOM error)
- 15.BOM FS9 remove(BOM redundant)
- 16.BOM R465 change to 1K ohm & R350 unmount (1.35V modify to 1.2V for mcp73 ver:A01 bug)
- 17.BOM del R487,R148 & add R142 (for cancel hardware spi protect function)
- 18.VS-BOM del SCREW L&2 (for nec req.)
- 19.BOM SPI ROM change to 8Mb (for bios code over 4Mb)
- 20.BOM R36 change to 0402, CLAMP change to level 60,R466 change to 2K,R112&R113 mount 10K(for BOM error)
- 21.BOM super i/o 5617 change part number to B02-0561704-S32

0B====>0C 2007.8.23

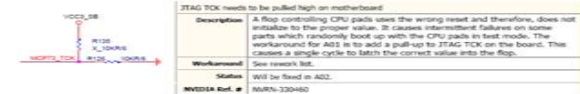
- 1.Remove R41,already internal pull-high.
- 2.Change R423 and R422 connect to VCC3_SB,remove R421.



3. Change 1.35V_DUAL power solution, the current only 300mA,so,just to use1087 is already enough.



- 4.Reserve pull-high JTAG_TCK,NVIDIA ERRATA.



- 5.EC28 change to 1000uF (LESR=31m ohm) to improve FSB VTT and VCC DDR power.
- 6.Change FS11,FS10 poly-fuse to 0.5A.0.5A is enough to meet cooling FAN spec.
- 7.Change V3P3_HDMI_PLL(B30 pin) to VCC3 directly, NV suggestion.
- 8.Add a 0.1uF cap at MCP73 ball AT2 (VCC3 to GND) and refer to NV new design guide, change IDE second layout to GND.
- 9.Remove R112 resistor, we don't have MII RGMII function.



- 10.Chane 14MHz.24MHz strap pin, remove R112risistor and pull down R155.



- 11.Delete below circuit, it is surplus ,short MS-17 pin 17,18 to produce RAM_VREF directly.



- 12.Change MCP73 - 1.5VDUAL Power design, PLL current only 200mA,It use 1087 regulator is enough.



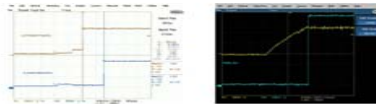
- 13.Follow NEC SPEC, only support one JUSB, change JUSB2_L16 to un-mount.
- 14.USB full-speed signal fail,R120 change to 910 ohm ,EC15 change to 1000uF ,need to confirm in next version.
- 15.Modify +5VUSB_FRONT placement and Change FS3,FS4, FS5,FS6 to 2.6A (low Rs.) to meet voltage drop. (NEC spec 250mV).
- 16.Audio R.L reverse



- 17.Phase VRM solution

- R407 -> 20KR
- R377 -> 1.15KR
- R381 -> 300R
- R378 -> 18KR
- C390 -> 15pF
- C392 -> 470pF
- R382 -> 200R
- R378, 385, 398 -> 4.3KR
- EC44, 41 -> N/C
- EC1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12 22uF/X5R

18. Change EC31,EC32,EC37,EC38,EC39 to 820uF
- 19.WP# function - remove R142 ,R487 and R148 mount, guarantee G3 to S5 states is low ,BIOS try to programming WP# pin.
- 20.Un-mount R160,C74,Q6,R161,Q7,R162,mount R159,R146 to follow NV SPEC.



- 1.H/V SYNC rising time over spec ,C451,C452 change to 12pF follow NV Bring_UP V6

SPI ROM vendor recommend, change SMT filter cap to EL cap.

- 23.Follow NV MBC ,add pull-high resistor at MCP73 pin C29 (HDCP_ROM_SDATA).
- 24.Due to layout factor, change FS6,R306,R307 power source to +5VUSB_FRONT.
- 25.JUSB1,JUSB2 pin5 connect to GND.
26. Add discharge resistor R158,R173,R176,R177.
27. follow NV Bring Up V6 ,change L2,L3L4to 100nH,C199~C201 change to 5.6PF.
- 28.Remove R44 - already internal pull-up.

0c====>10 2007.10.10

1. Add SIO pin 48(input pin) pull down resistor



- 2.Due to SMSC5617 limitation, add a pull up resistor for Rodem-VS MS can't to setup GPIO issue

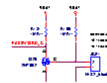


- 3.Follow DRD spec, remove JUSB1 circuit for MA,stuff JUSB1 circuit for VS.
- 4.Delete all Mini-PCIE circuit.
- 5.Add back pull-up resistor 200 ohm for H_PWRGD (MCP73_Bring_Up_Support_V10)

Amendment to Required Board Level Changes 6-2 : Do not remove the pull up resistor on CPU_FERR# and CPU_PWRGD. CPU_PWRGD needs a 200 ohms pull up resistor to CPU VTT power rail.

6. fine tuning D-sub signal
change a)L2,L3,L4 to 0.1uH
b)C199,C200,C201 change to 5.6PF
c)L35,L36 change to 0ohm
- 7.Due to MCP73 INTRUDER (clear password) pin only accept low active to recorder states, so add a inverter circuit to solve it.

Clear password



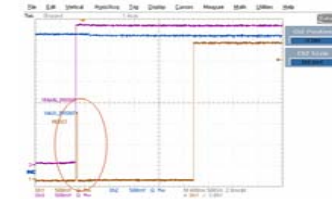
- 8.Add back LAN power control circuit to reduce power consumption

Power control for power consumption




- 9.Add R316 to improve VCC1_35 ripple current.
- 10.Change PEA_RST to MS7 PCI_RST for WOL can not wake up issue.
- 1)remove R84
- 2)add R119 between PEA_RST and MS7 pin39

Problem waveform



- 11.Delete R212 ,R133, BUFO_25MHZ,it is no use.
- 12.Delete R82 and short with VCC1_35 directly.
- 13.Delete C62,no use.
- 14 Add C359,C373 6.8pF to improve VCC1_35,VCC_DDR dynamic voltage.
- 15.Remove SMBUS of SIO.
- 16.Follow SMSC new datasheet, remove C323
- 17.Reserve SIO PME pull-up
- 19.Delete C63 ,doesn't use.
- 20.Delete D23, doesn't use.
- 21.Add C190 to improve ripple current.
22. Remove Jump 2.0mm location:JSP11
- 23.Change FSB_POWER source to 1.35V
- 24.Reserve FRONT USB pin header

- 25.Add C58 for Beep issue

		
Link to the Future		
MICRO-START INT'L CO.,LTD.		
Title		
HISTORY		
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	MS-7402	10
Date:	Friday, November 02, 2007	Sheet 31 of 31