MS-7395 ATX Version: 0A

CPU: P4,LGA775(Prescott),(Smithfield),(CedarMill),(Presler), (Conroe),(Kentsfield);Wolfdale(Conroe next gen) ; Yorkfield (Kentsfield next gen)

System Chipset:

Intel Bearlake - Q/G/P (G33, P35, Q35/33North Bridge)
Intel ICH9 (co-lay ICH9R South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111B CO-LAY RTL8111C (PCIE)
HD Audio Codec -- ALC888

PCIE to PATA/SATA Bridge -- JMB363

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X 1 SLOT * 1

PCI SLOT * 4

PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

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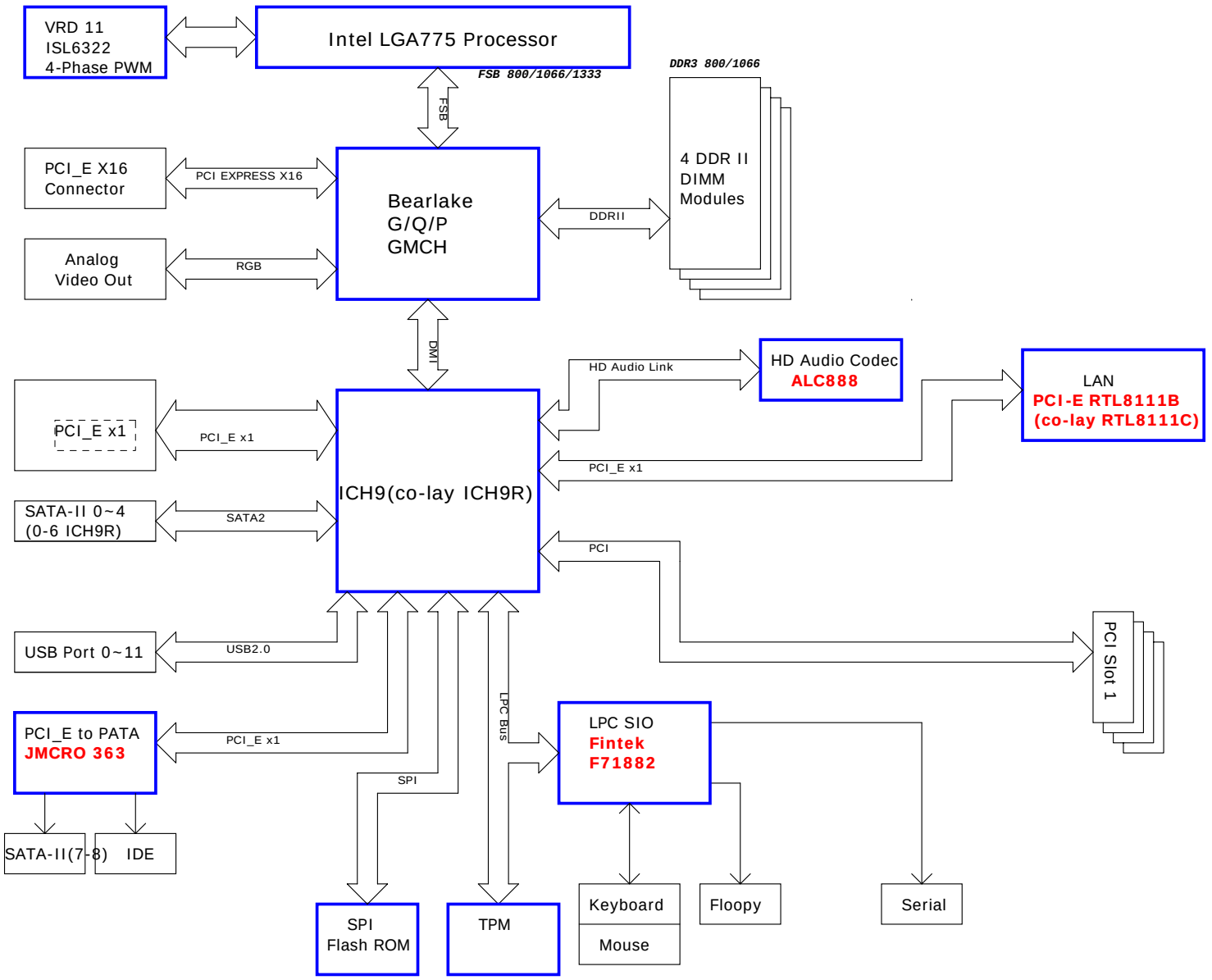
MS-7395

Size: Custom | Document Description: COVER SHEET | Rev: 0A

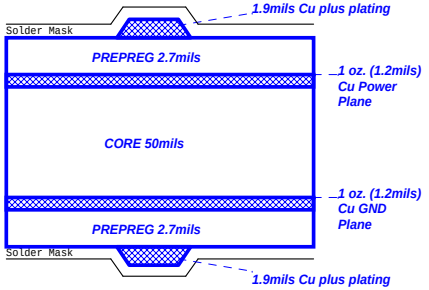
Date: Wednesday, August 15, 2007 | Sheet 1 of 33

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

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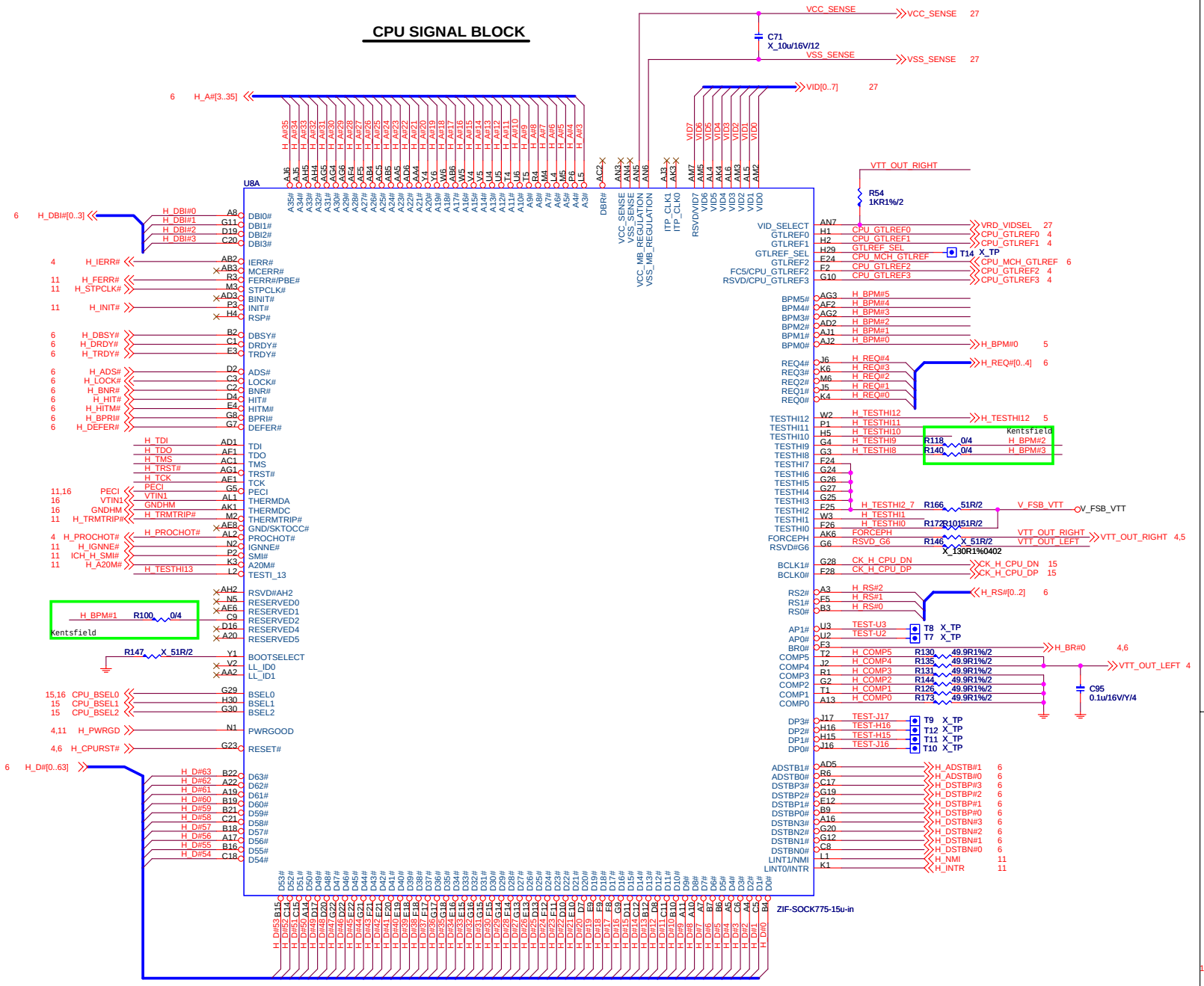
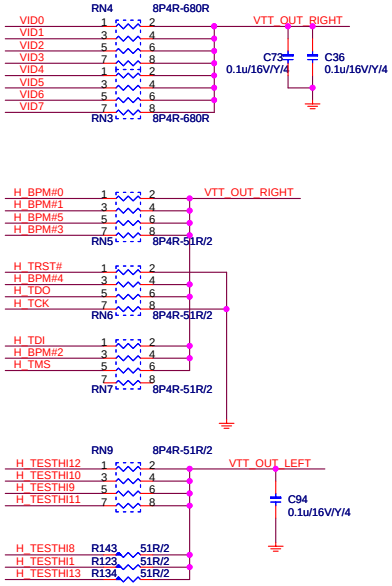
MS-7395		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 2 of 33	

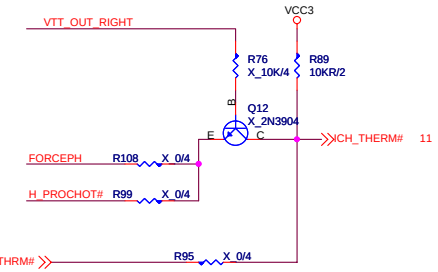
CPU SIGNAL BLOCK



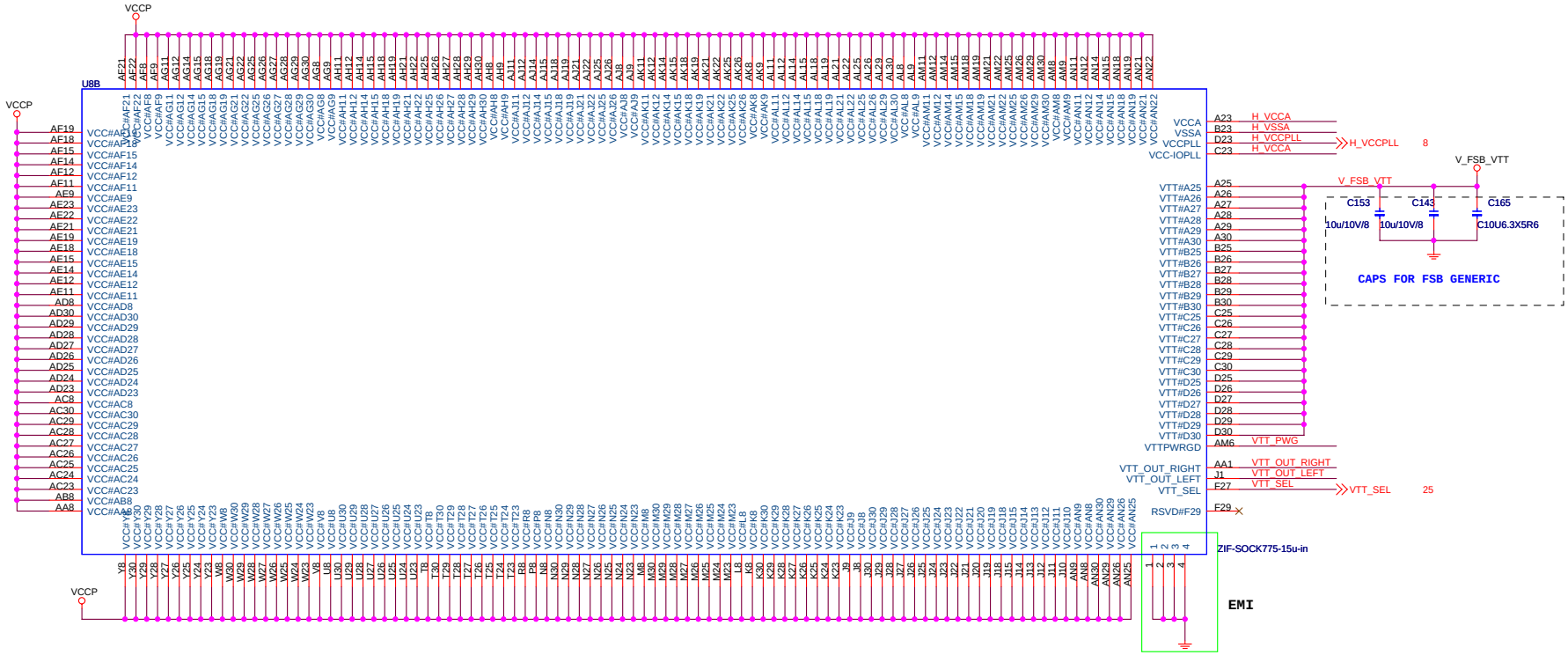
PULL HIGHT PULL DOWN



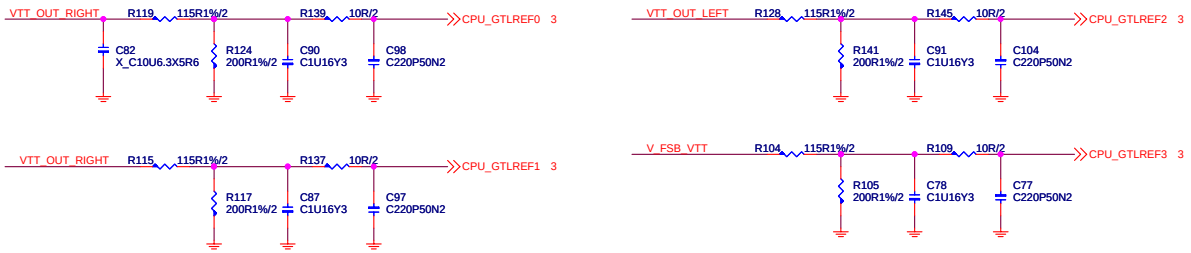
Thermal TRIP



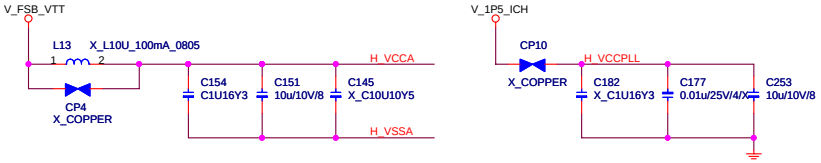
MICRO-STAR INT'L CO.,LTD		
MS-7395		
Size: Custom	Document Description: LGA775 - Signal	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 3 of 33	



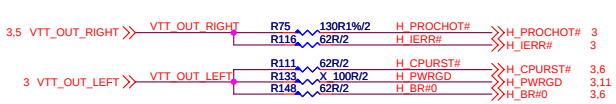
*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)



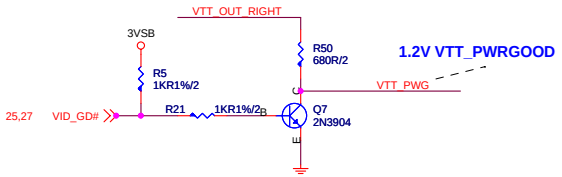
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

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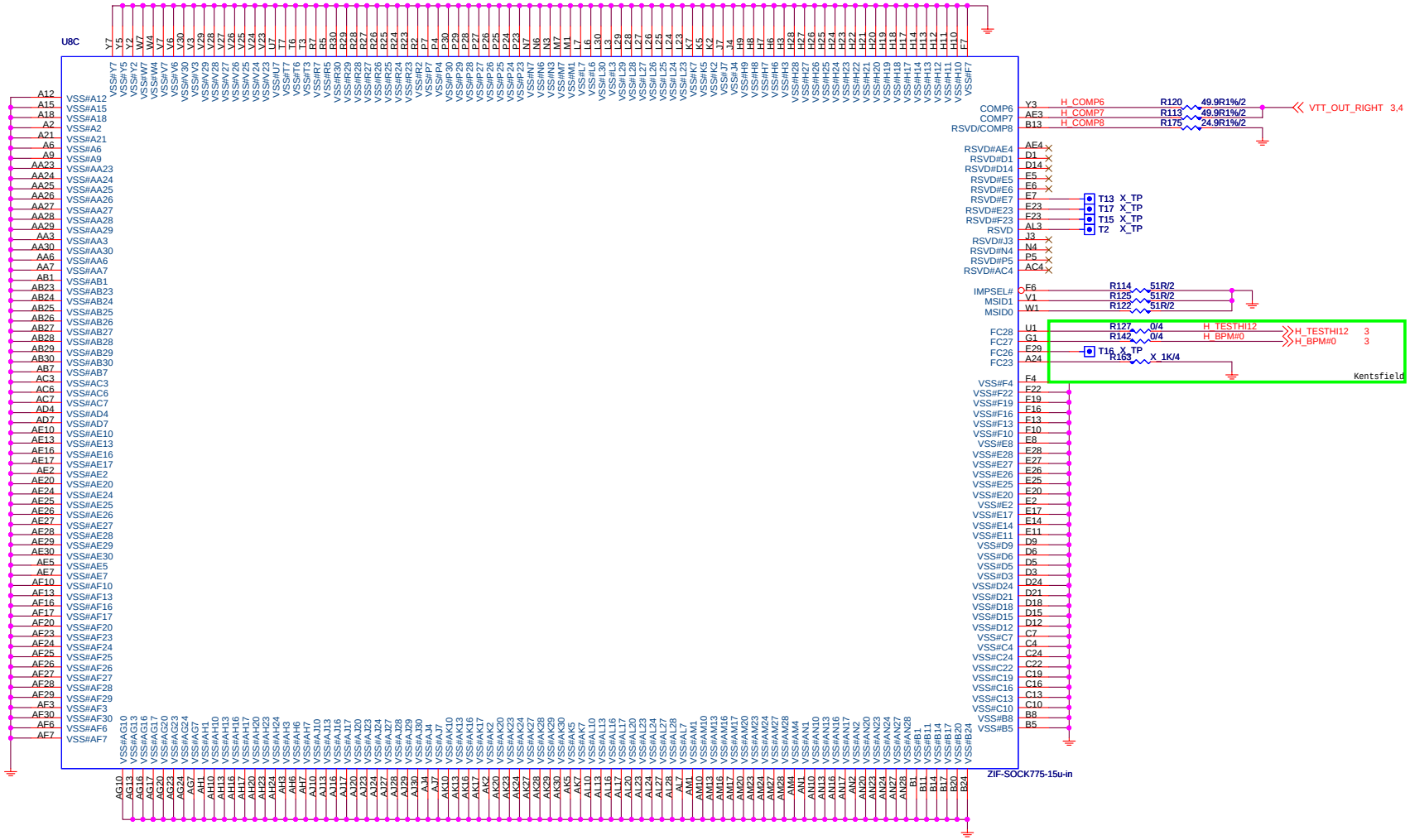
MS-7395

Size	Document Description	Rev
Custom	LGA775 - Power	0A

Date: Wednesday, August 15, 2007 Sheet 4 of 33



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MS-7395			
Size: Custom	Document Description: LGA775 - GND		Rev: 0A
Date: Wednesday, August 15, 2007		Sheet 5 of 33	

U1MCH

U12B

FSB

BRLK_B_CRB

1 OF 7

U12A

PCIE

DMI

EXP_COMPO

EXP_COMPI

2 OF 7

BRLK_B_CRB

U12E

VGA

MISC

5 OF 7

BRLK_B_CRB

PIN	H	L	Description
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

*GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V (At VTT=1.2V)

HXSWING SHOULD BE 1/4*VTT

CL_VREF_MCH = 0.349V
Close to GMCH

Non-Graphic sku

Reserved for non-Graphic sku

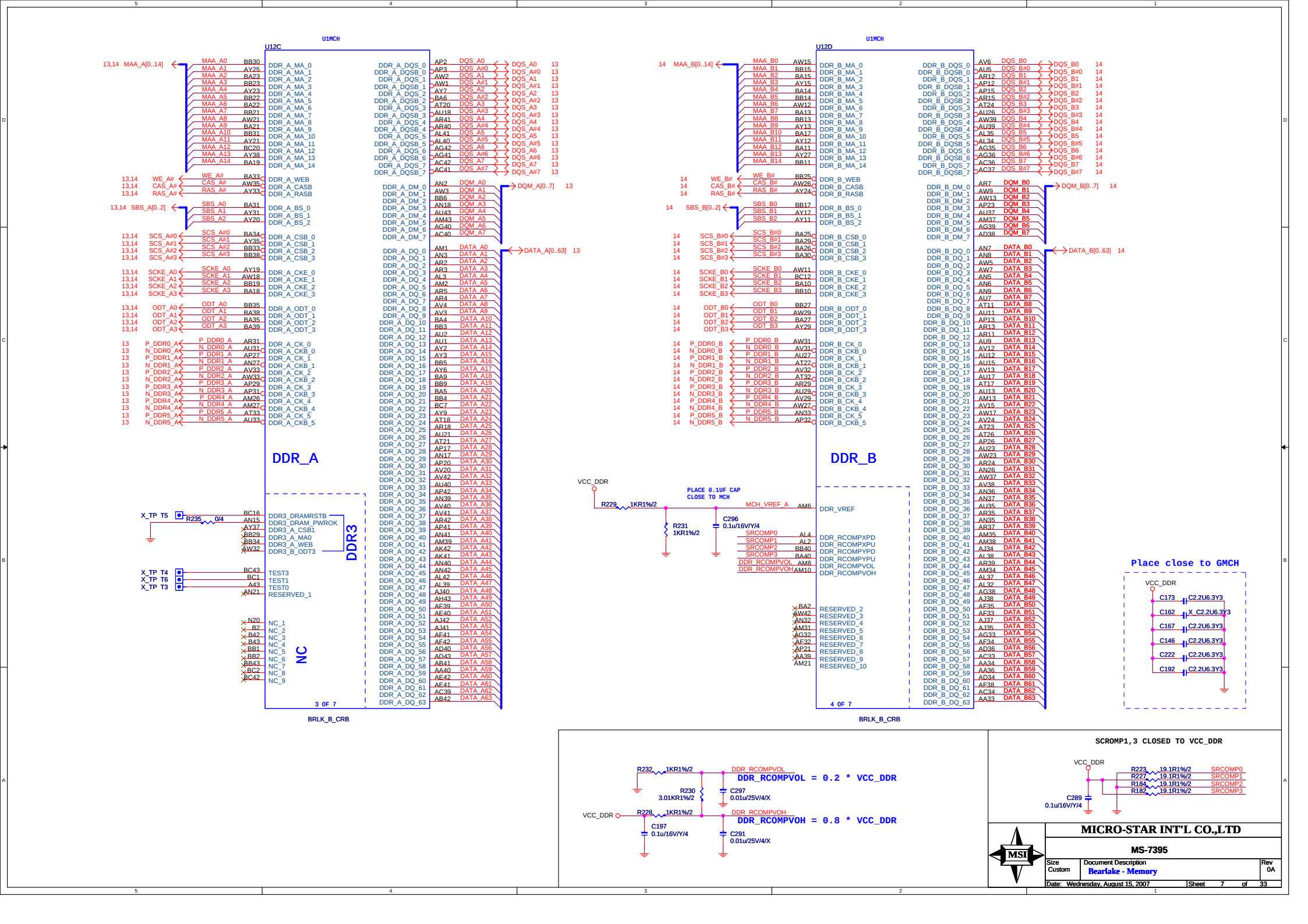
Close to GMCH.
Change to 0-ohm for non-Graphic sku

MICRO-STAR INT'L CO.,LTD

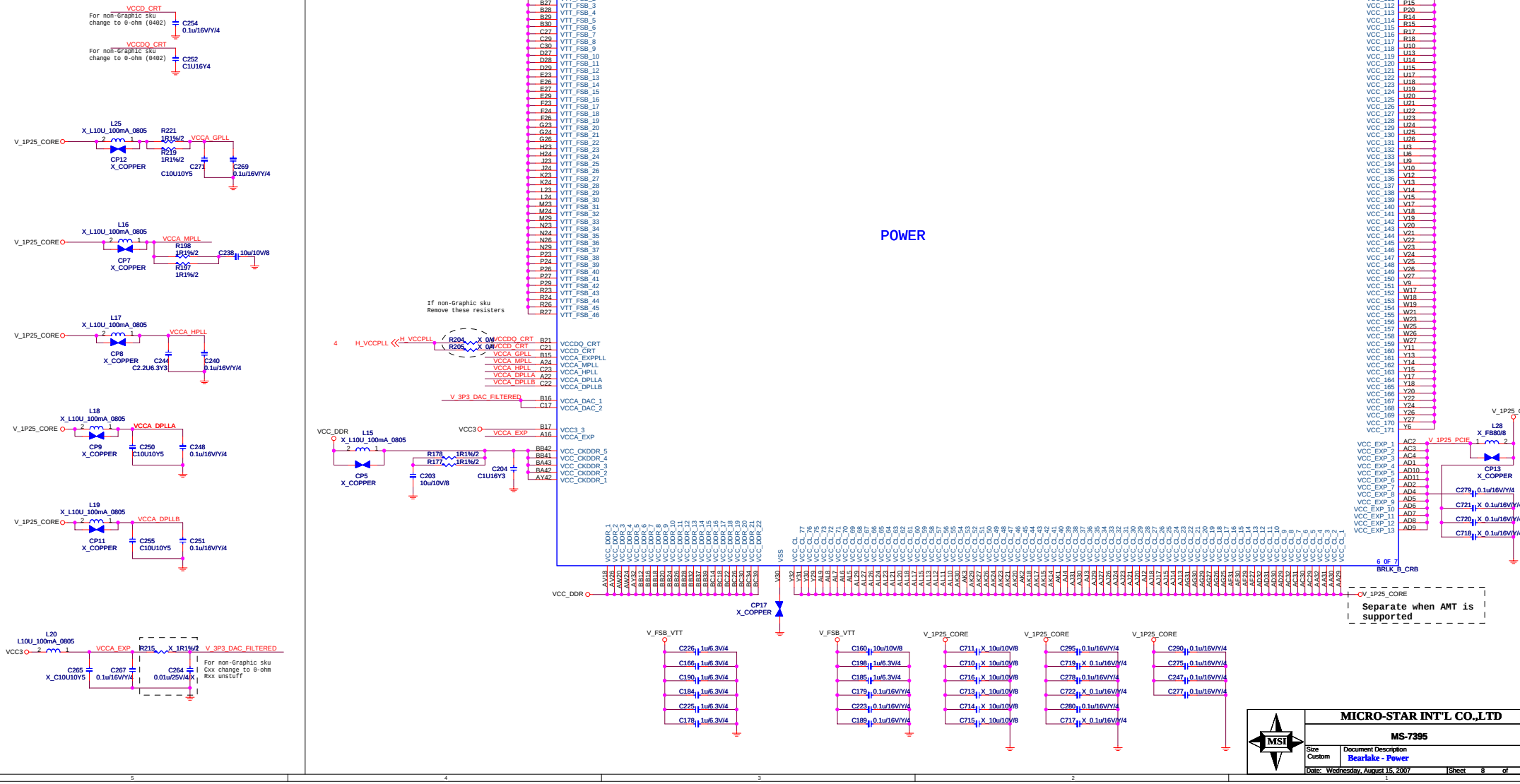
MS-7395

Size: Custom | Document Description: Bearlake - FSB, PCIE, DMI, VGA, MSIC | Rev: 0A

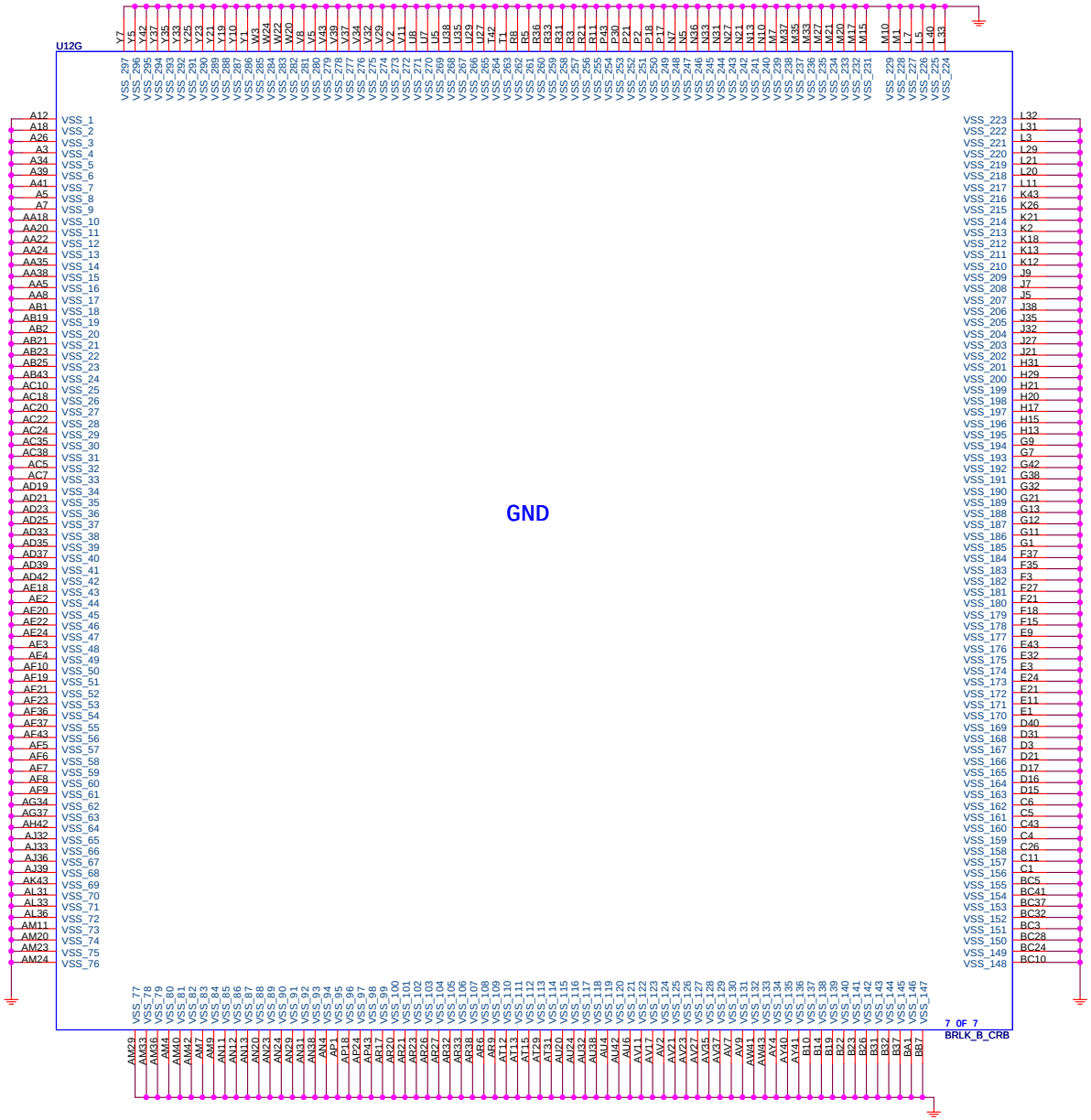
Date: Wednesday, August 15, 2007 | Sheet 6 of 33


U1MCH
U12C
DDR_A
DDR3
NC
3 OF 7
BRLK_B_CRB
U1MCH
U12D
DDR_B
DDR_VREF
RESERVED_2
RESERVED_3
RESERVED_4
RESERVED_5
RESERVED_6
RESERVED_7
RESERVED_8
RESERVED_9
RESERVED_10
4 OF 7
BRLK_B_CRB
PLACE 0.1UF CAP
CLOSE TO MCH
VCC_DDR
R229 1KR1%/2
R231 1KR1%/2
C296 0.1u/16V/Y/4
MCH_VREF_A
SRCOMP0
SRCOMP1
SRCOMP2
SRCOMP3
DDR_RCOMPVOL
DDR_RCOMPVOH
DDR_RCOMPXPD
DDR_RCOMPXPU
DDR_RCOMPYPD
DDR_RCOMPYPU
DDR_RCOMPVOL
DDR_RCOMPVOH
Place close to GMCH
C173 C2.2U6.3Y3
C162 X_C2.2U6.3Y3
C167 C2.2U6.3Y3
C146 C2.2U6.3Y3
C222 C2.2U6.3Y3
C192 C2.2U6.3Y3
R232 1KR1%/2
R230 3.01KR1%/2
R228 1KR1%/2
C197 0.1u/16V/Y/4
C297 0.01u/25V/4/X
C291 0.01u/25V/4/X
DDR_RCOMPVOL = 0.2 * VCC_DDR
DDR_RCOMPVOH = 0.8 * VCC_DDR
SCROMP1,3 CLOSED TO VCC_DDR
R223 19.1R1%/2
R227 19.1R1%/2
R184 19.1R1%/2
R182 19.1R1%/2
C289 0.1u/16V/Y/4
MICRO-STAR INT'L CO.,LTD
MS-7395
Size Custom
Document Description
Bearlake - Memory
Rev 0A
Date: Wednesday, August 15, 2007
Sheet 7 of 33

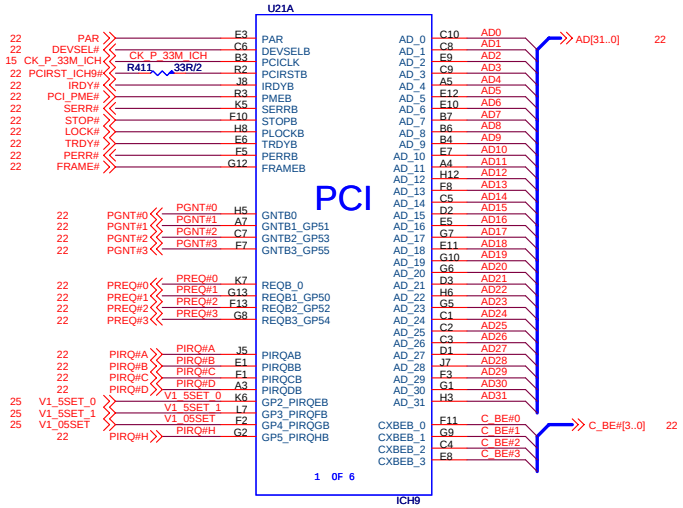
NB POWER

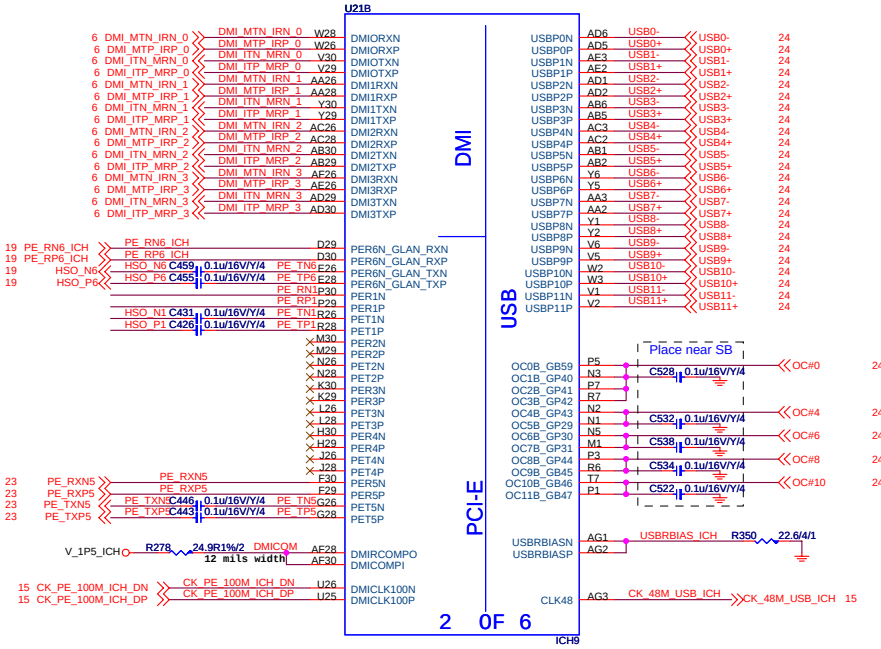


MICRO-STAR INT'L CO.,LTD	
MS-7395	
Size: Custom	Document Description: Bearlake - Power
Rev: 0A	
Date: Wednesday, August 15, 2007	Sheet 8 of 33



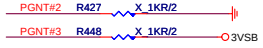
MICRO-STAR INT'L CO.,LTD	
MS-7395	
Size: Custom	Document Description: Bearlake - GND
Rev: 0A	
Date: Wednesday, August 15, 2007	Sheet 9 of 33





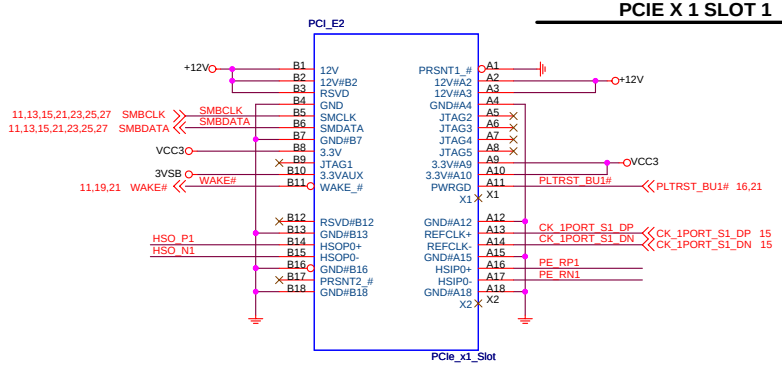
SB STRAPPING RESISTOR

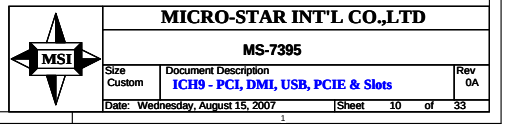
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

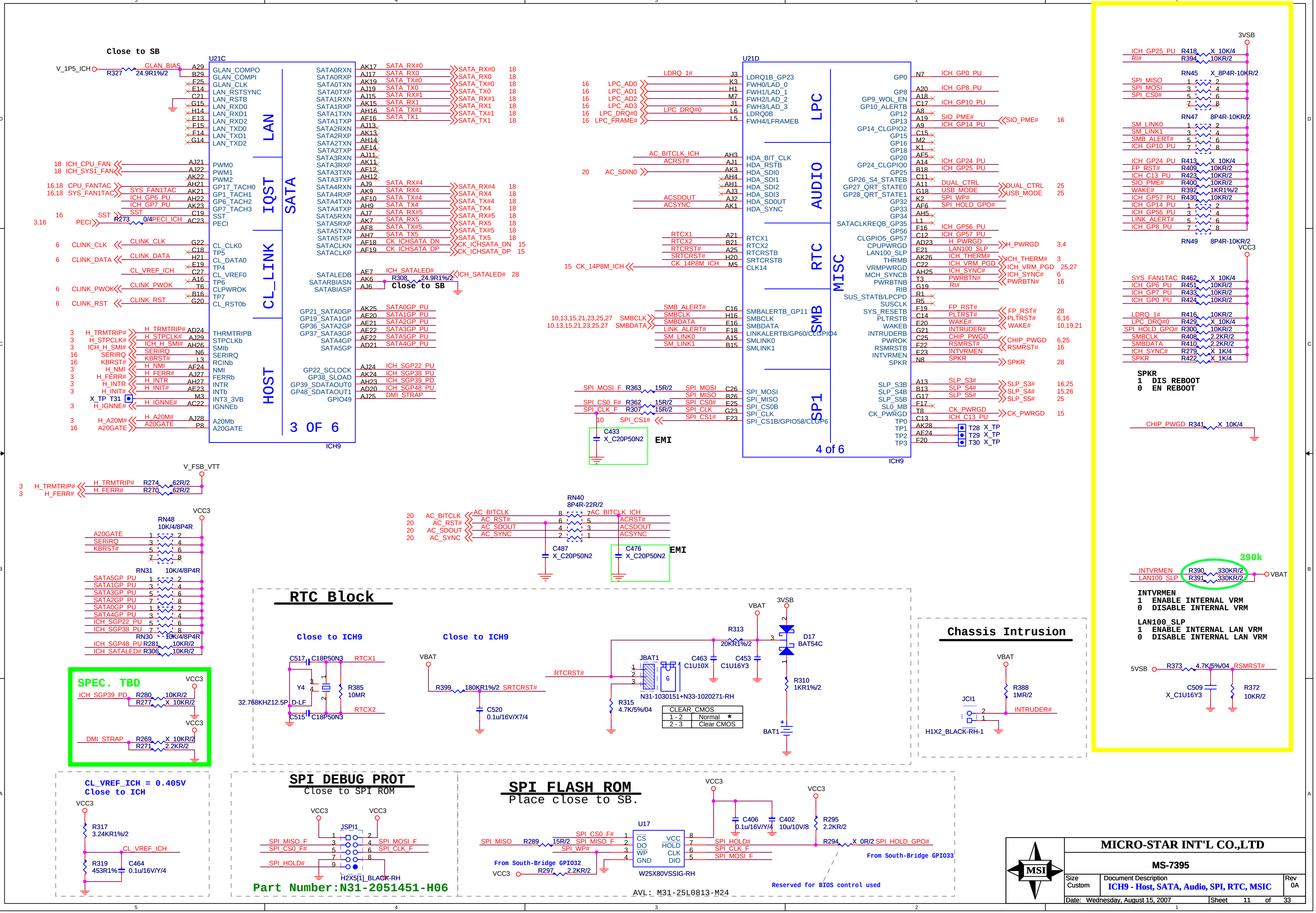


SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

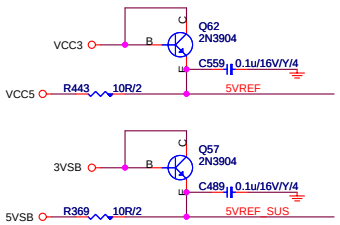
PCIE X 1 SLOT 1



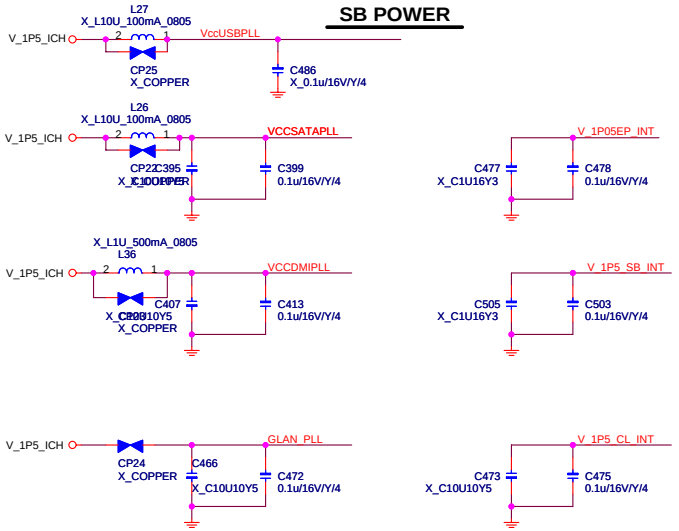


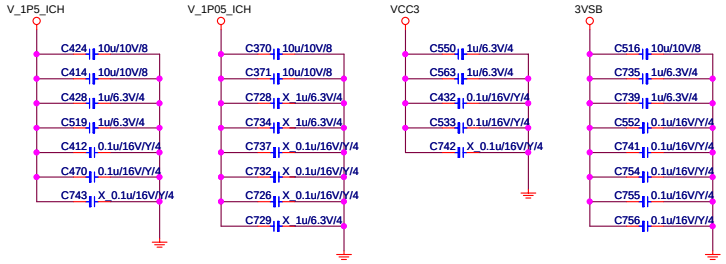

Close to SB
U21C
LAN
IQST
SATA
CL_LINK
HOST
3 OF 6
ICH9
U21D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
EMI
SPKR
1 DIS REBOOT
0 EN REBOOT
390k
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
SPEC. TBD
RTC Block
Close to ICH9
CLEAR CMOS
1 - 2 Normal *
2 - 3 Clear CMOS
Chassis Intrusion
CL_VREF_ICH = 0.405V
Close to ICH
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
SPI FLASH ROM
Place close to SB.
From South-Bridge GPIO32
From South-Bridge GPIO33
Reserved for BIOS control used
AVL: M31-25L0813-M24
MICRO-STAR INT'L CO.,LTD
MS-7395
Size
Custom
Document Description
ICH9 - Host, SATA, Audio, SPI, RTC, MISC
Rev
0A
Date: Wednesday, August 15, 2007
Sheet 11 of 33

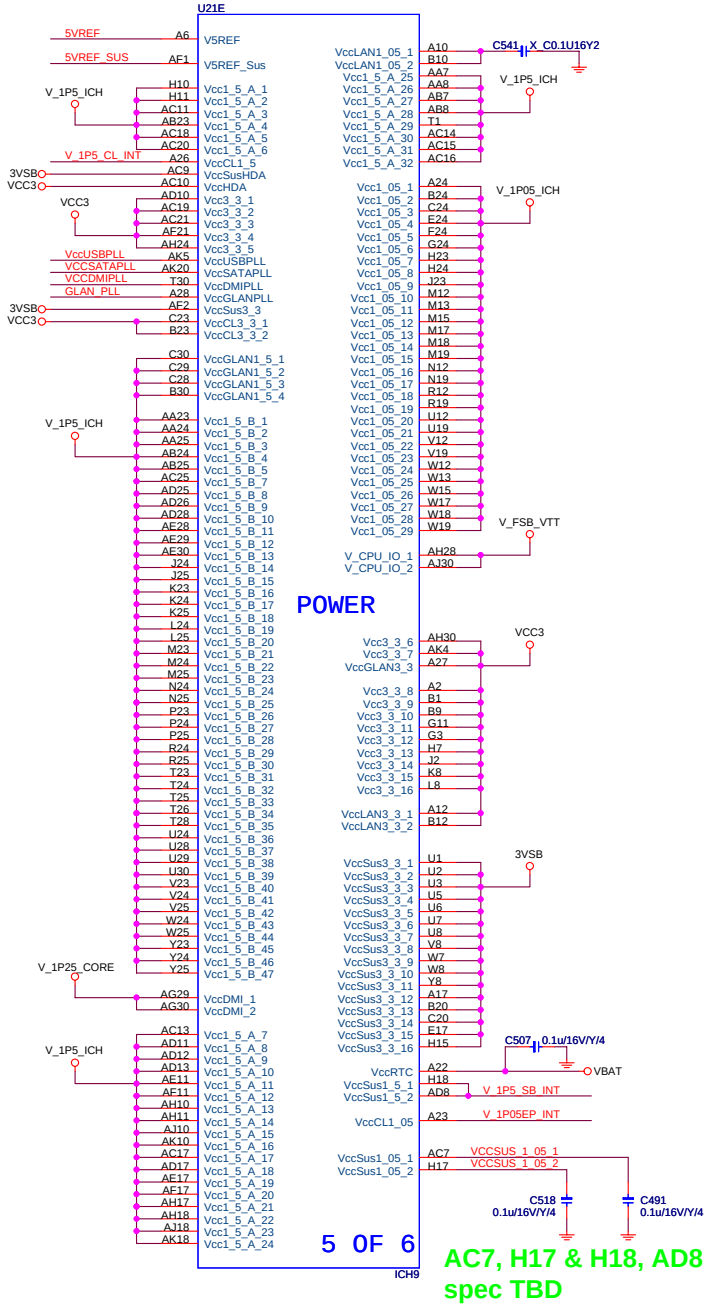
5VREF & 5VREF_SUS Sequencing Circuit

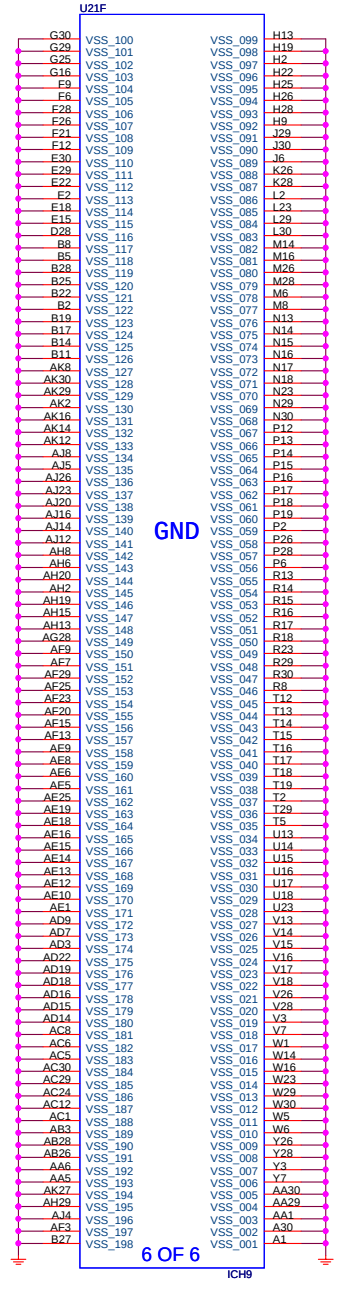


SB POWER

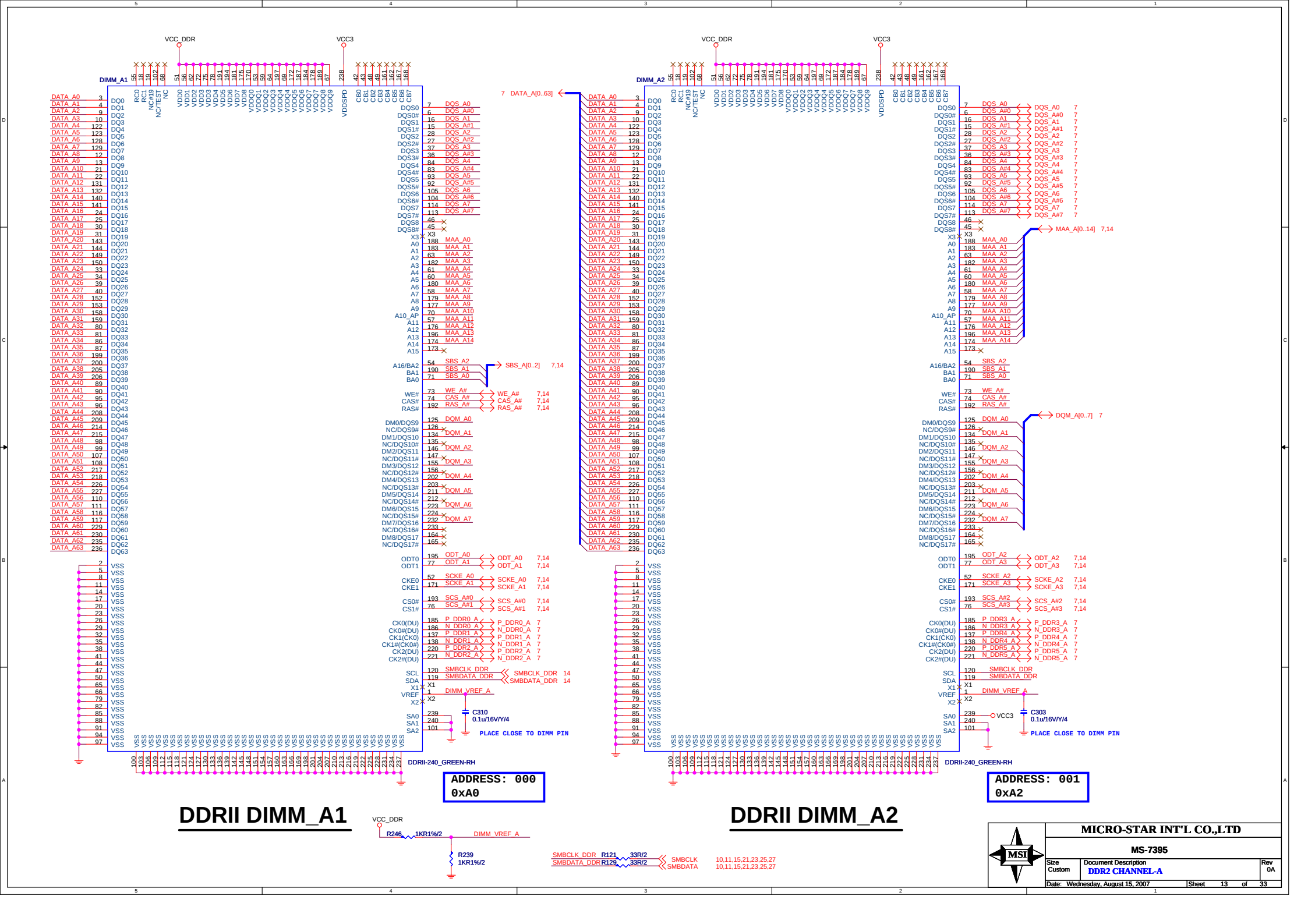


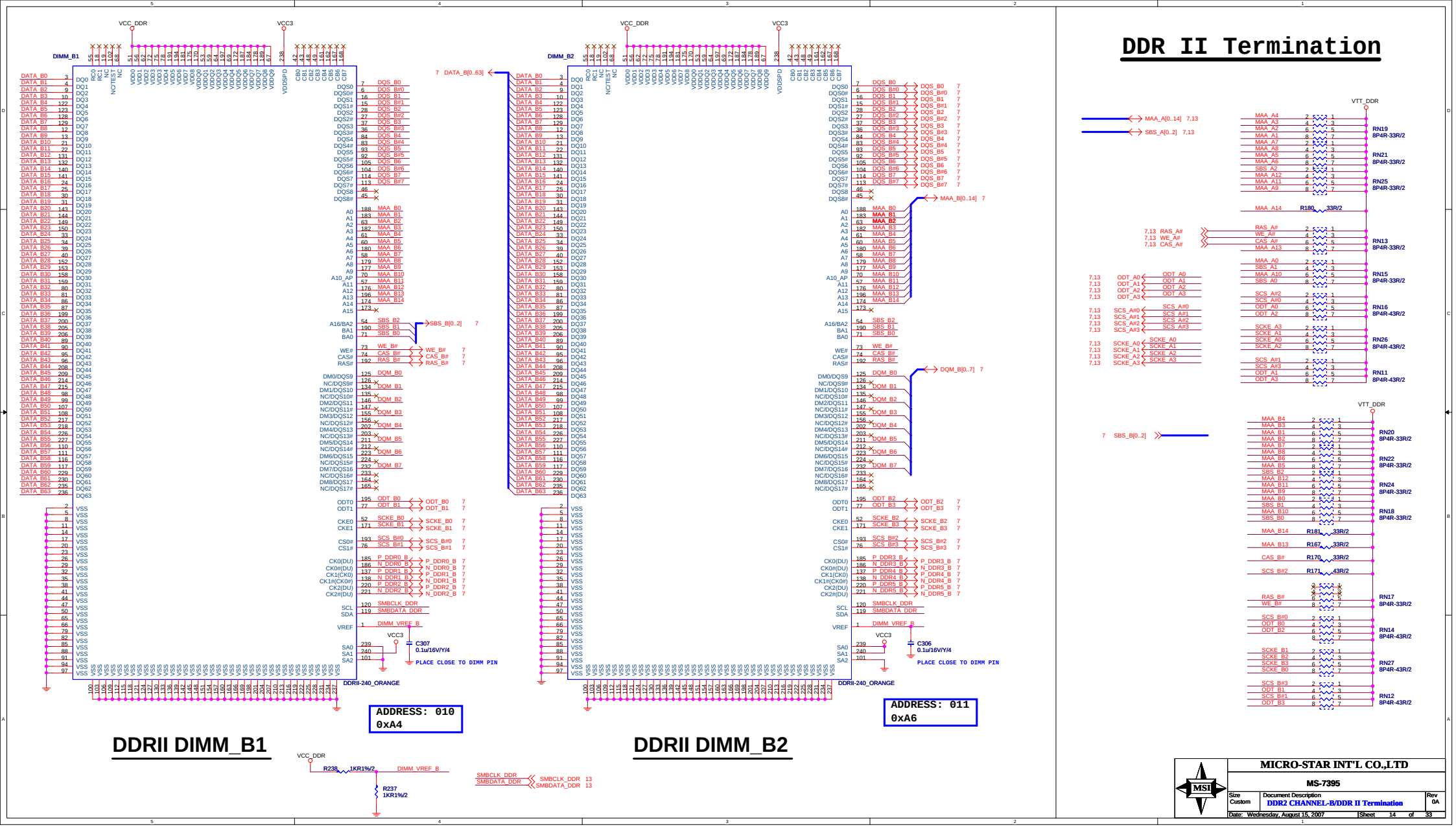


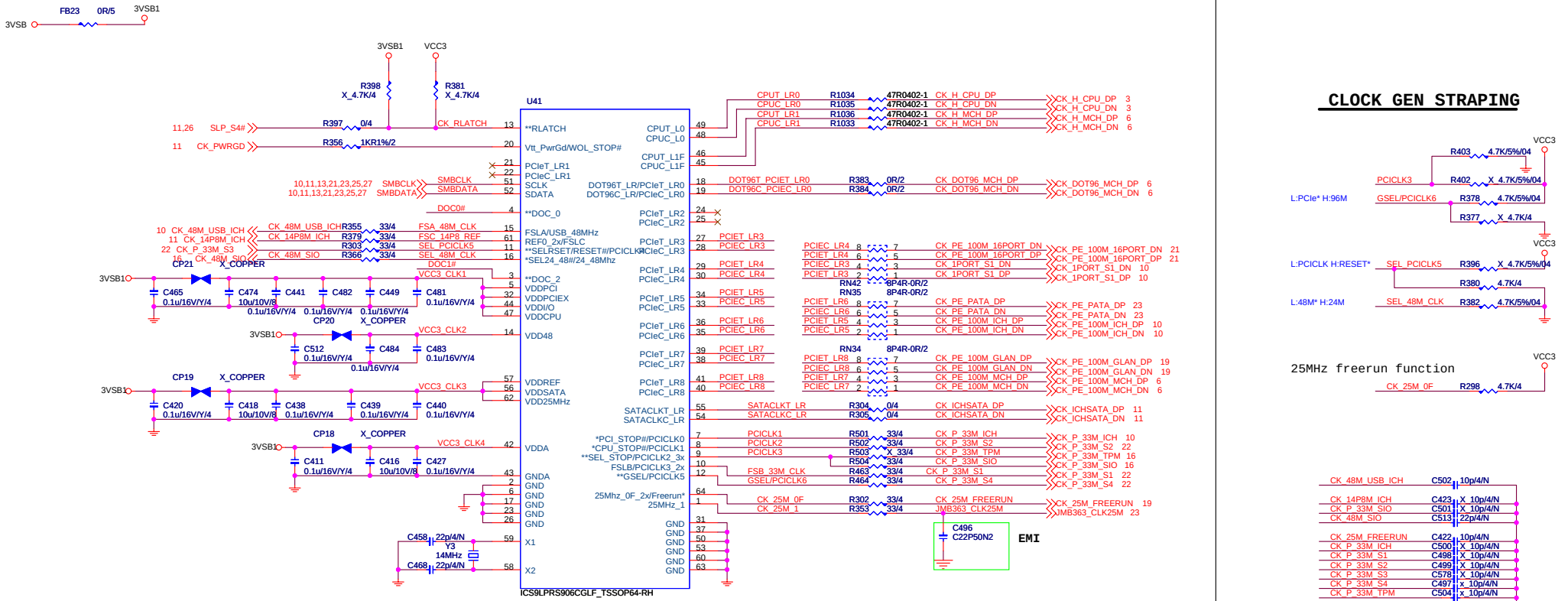




MICRO-STAR INT'L CO.,LTD		
MS-7395		
Size: Custom	Document Description: ICH9 - Power, GND	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 12 of 33	


DIMM_A1
DIMM_A2
VCC_DDR
VCC3
DDRII-240_GREEN-RH
C310
0.1u/16V/Y/4
C303
PLACE CLOSE TO DIMM PIN
ADDRESS: 000
0xA0
ADDRESS: 001
0xA2
DDRII DIMM_A1
DDRII DIMM_A2
R246 1KR1%/2
R239
1KR1%/2
DIMM_VREF_A
R121 33R/2
R129 33R/2
SMBCLK_DDR
SMBDATA_DDR
SMBCLK
SMBDATA
10,11,15,21,23,25,27
MICRO-STAR INT'L CO.,LTD
MS-7395
Size
Custom
Document Description
DDR2 CHANNEL-A
Rev
0A
Date: Wednesday, August 15, 2007
Sheet 13 of 33


DDR II Termination
DDRII DIMM_B1
DDRII DIMM_B2
DIMM_B1
DIMM_B2
VCC_DDR
VCC3
VTT_DDR
DDRII-240_ORANGE
ADDRESS: 010
0xA4
ADDRESS: 011
0xA6
PLACE CLOSE TO DIMM PIN
C307
0.1u/16V/Y/4
C306
0.1u/16V/Y/4
R238 1KR1%/2
R237 1KR1%/2
DIMM_VREF_B
MICRO-STAR INT'L CO.,LTD
MS-7395
DDR2 CHANNEL-B/DDR II Termination
Size Custom
Rev 0A
Date: Wednesday, August 15, 2007
Sheet 14 of 33

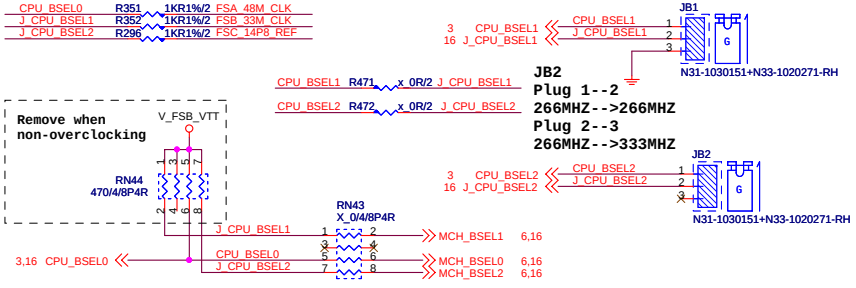


CLOCK GEN STRAPING

25MHz freerun function

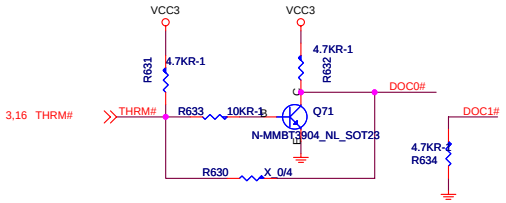
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
0	0	1	133 MHz (533)
0	1	0	200 MHz (800)

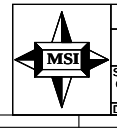
JB1
Plug 1--2
200MHZ-->200MHZ
Plug 2--3
200MHZ-->266MHZ



JB2
Plug 1--2
266MHZ-->266MHZ
Plug 2--3
266MHZ-->333MHZ

JB1
Open
JB2
Plug 1--2 or 2--3 or Open
333MHZ-->400MHZ



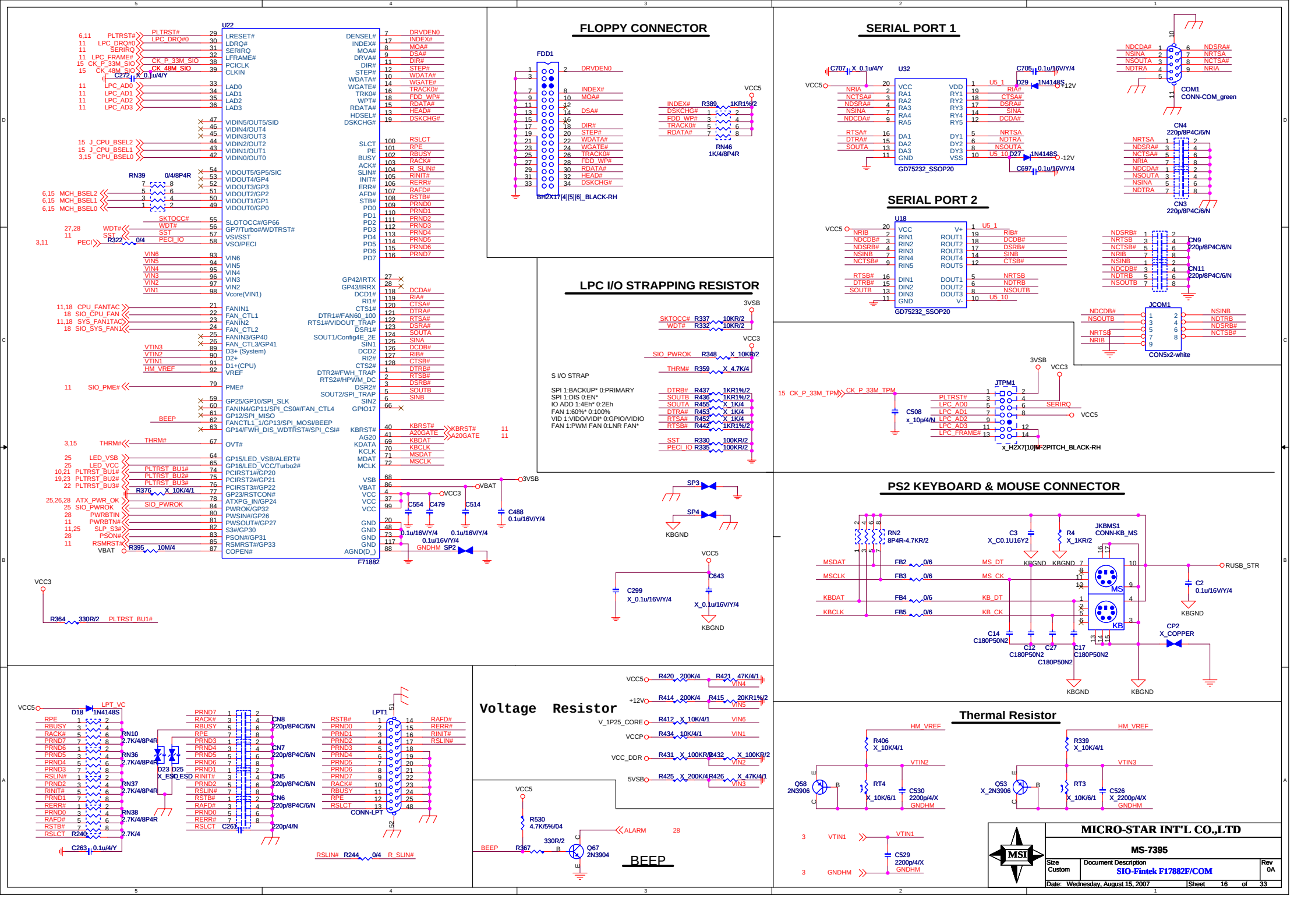


MICRO-STAR INT'L CO.,LTD

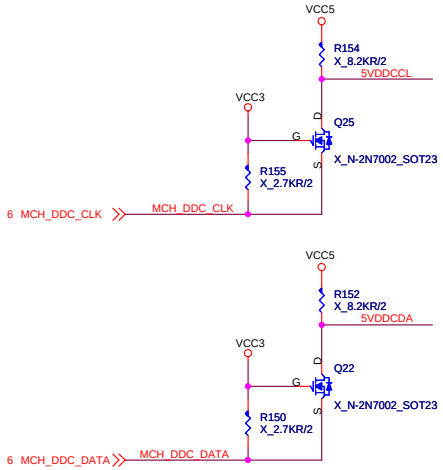
MS-7395

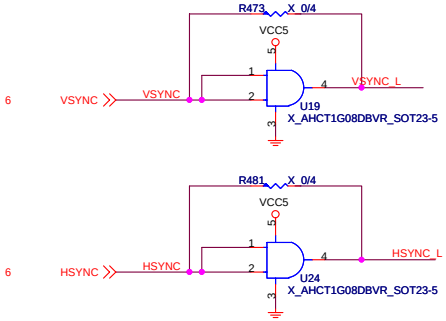
Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS900	0A

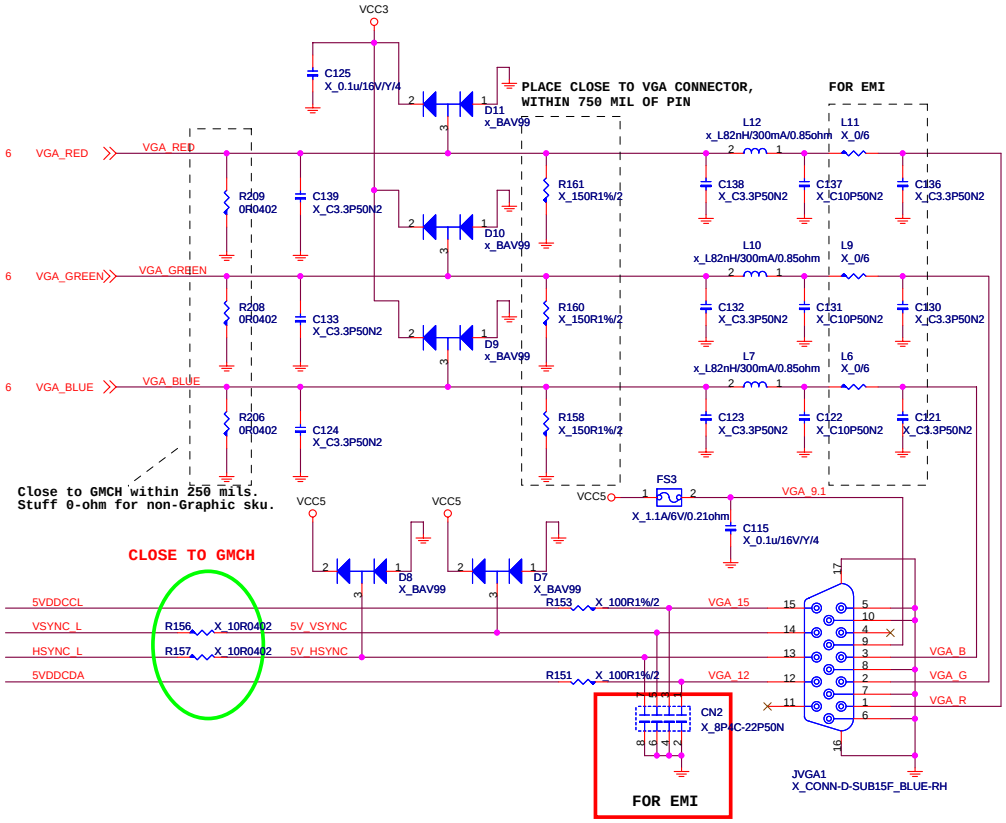
Date: Wednesday, August 15, 2007 Sheet 15 of 33


FLOPPY CONNECTOR
SERIAL PORT 1
SERIAL PORT 2
LPC I/O STRAPPING RESISTOR
PS2 KEYBOARD & MOUSE CONNECTOR
Thermal Resistor
Voltage Resistor
BEEP
U22
F71882
FDD1
BH2X17[4][5][6]_BLACK-RH
U32
GD75232_SSOP20
U18
GD75232_SSOP20
COM1
CONN-COM_green
CN4
220p/8P4C/6N
CN3
220p/8P4C/6N
CN9
220p/8P4C/6N
CN11
220p/8P4C/6N
JCOM1
CON5x2-white
JTPM1
X_H2X7[10]M-2PITCH_BLACK-RH
JKBMS1
CONN-KB_MS
CONN-LPT
MICRO-STAR INT'L CO.,LTD
MS-7395
SIO-Fintek F17882F/COM
Wednesday, August 15, 2007
Sheet 16 of 33

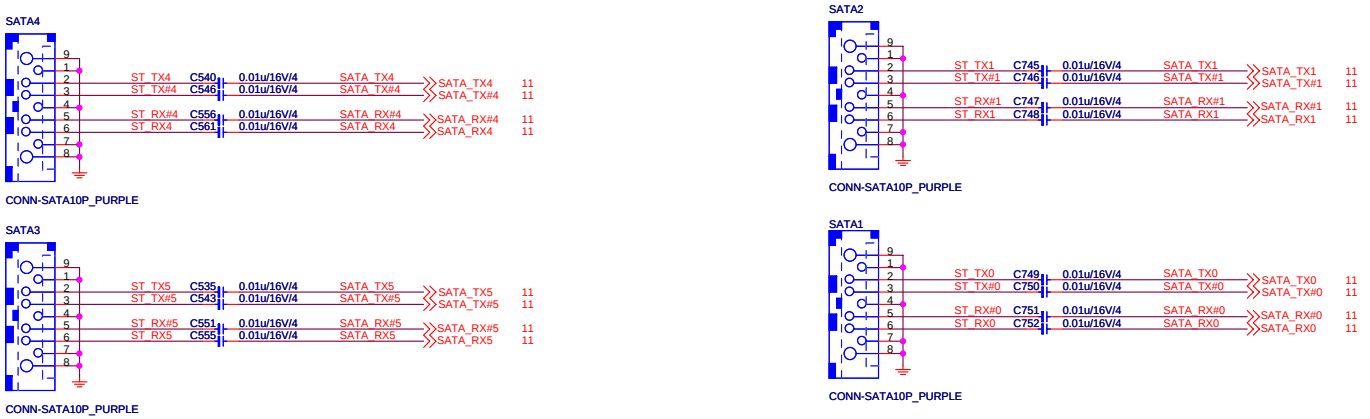
Video Connector



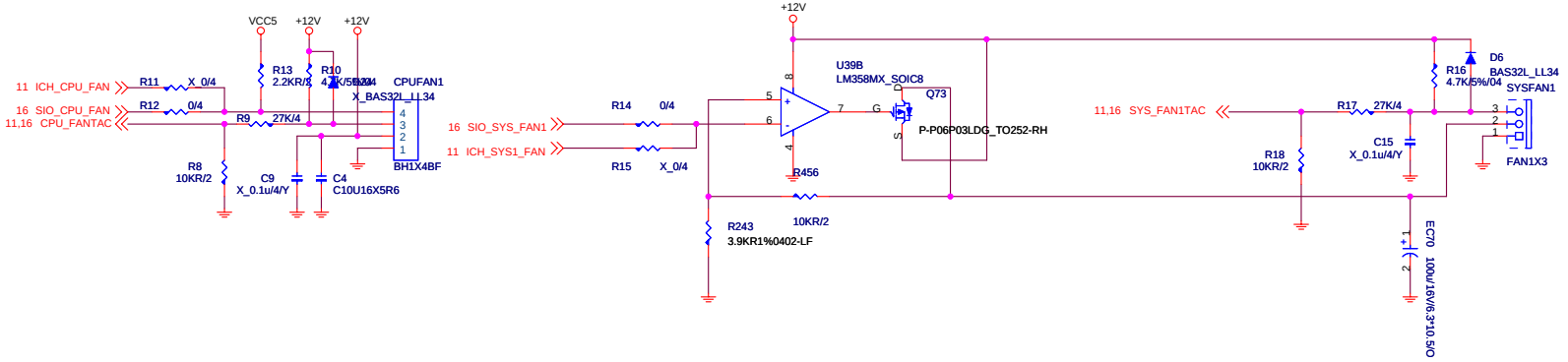




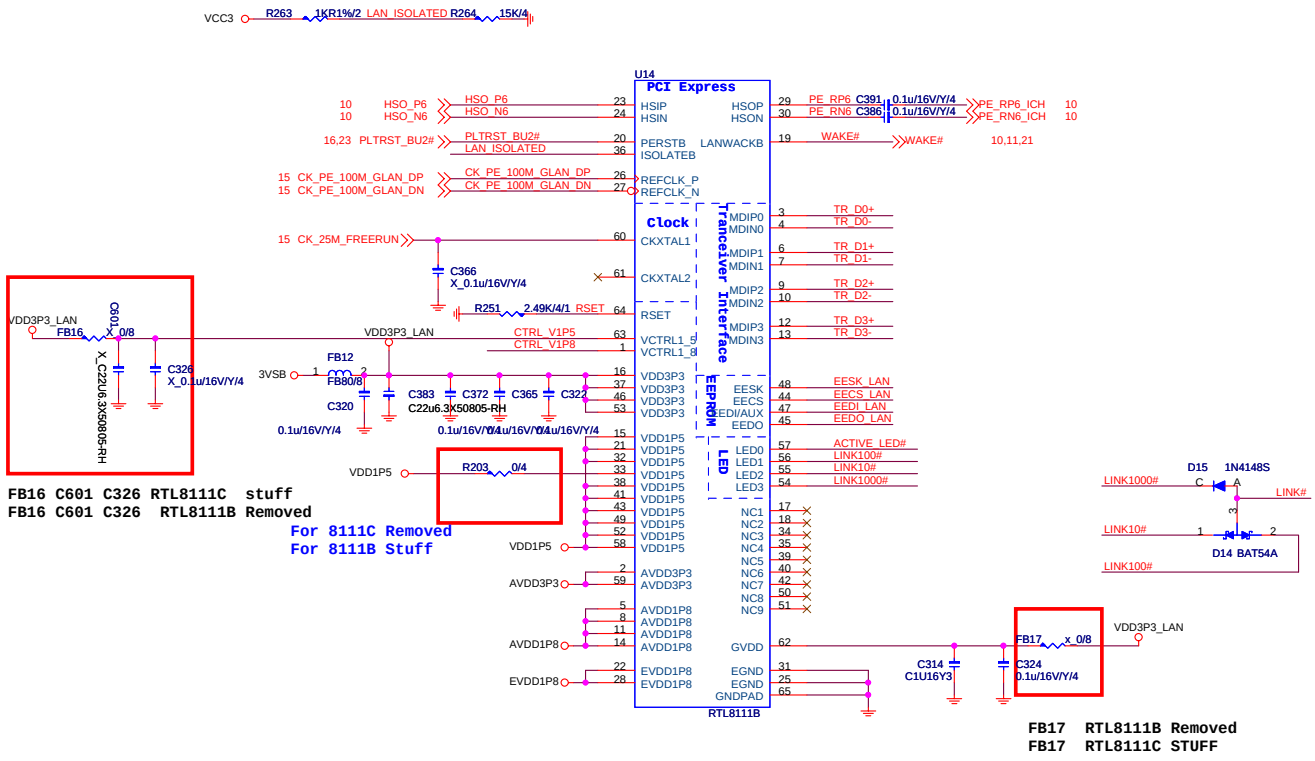
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7395	
Size: Custom	Document Description: VGA	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 17 of 33	



FAN-COUNTROL CIRCUIT

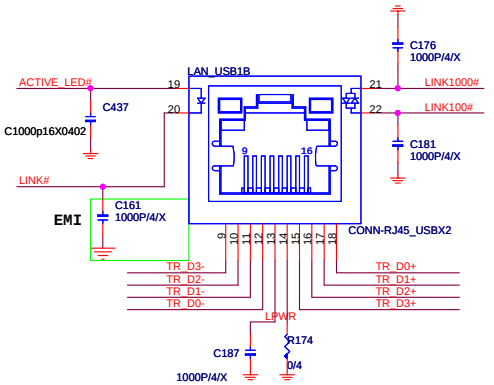


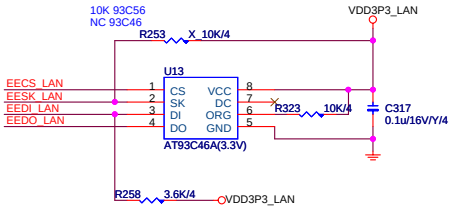
MICRO-STAR INT'L CO.,LTD		
MS-7395		
Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 18 of 33	



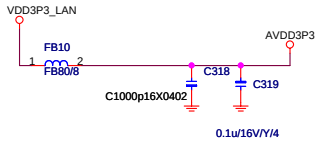
FB16 C601 C326 RTL8111C stuff
FB16 C601 C326 RTL8111B Removed
For 8111C Removed
For 8111B Stuff

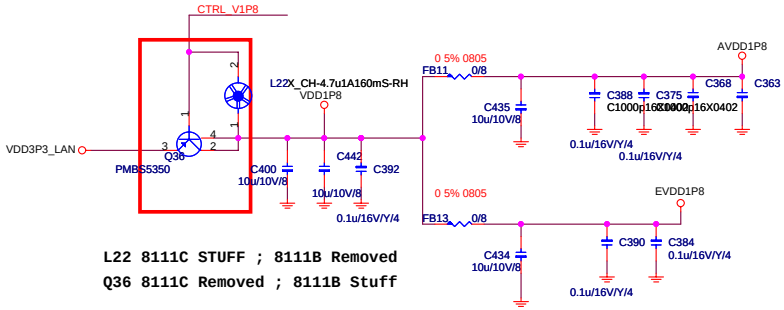
FB17 RTL8111B Removed
FB17 RTL8111C STUFF



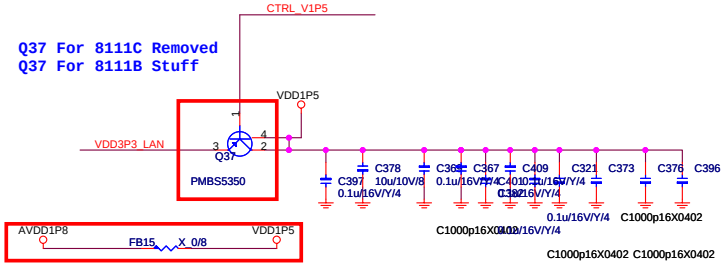


PCIE LAN(RTL8111B) POWER





L22 8111C STUFF ; 8111B Removed
Q36 8111C Removed ; 8111B Stuff

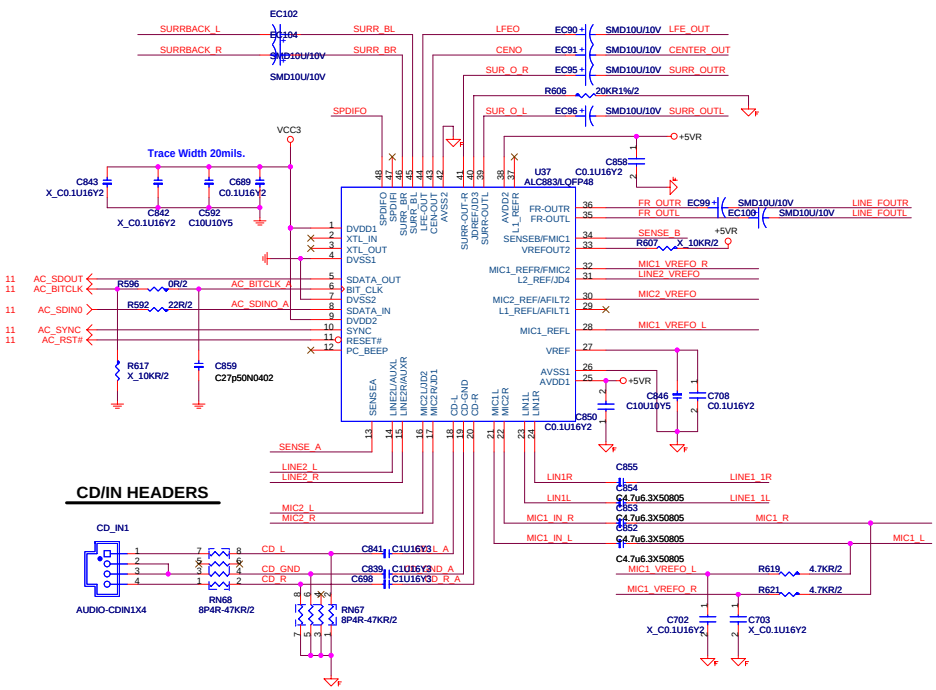


Q37 For 8111C Removed
Q37 For 8111B Stuff

FB15 For 8111C Stuff
FB15 For 8111B Removed

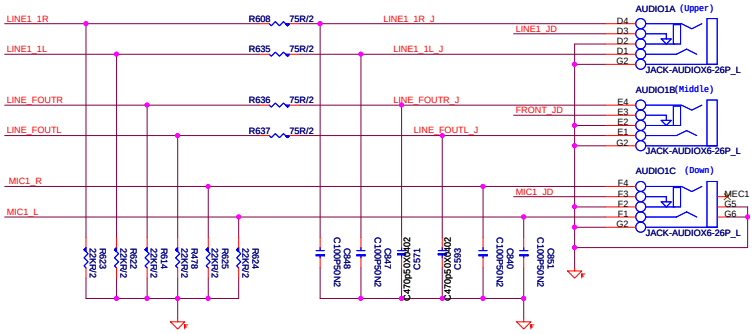
MICRO-STAR INT'L CO.,LTD		
MS-7395		
Size: Custom	Document Description: PCIE_LAN_RTL8111B	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 19 of 33	

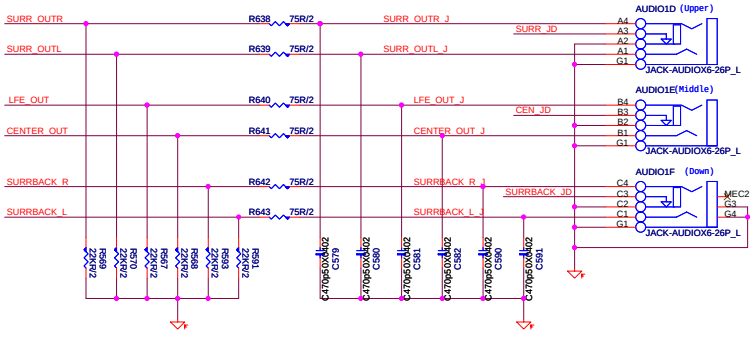
ALC888 CODEC



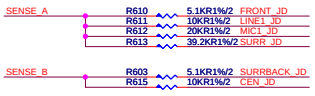
CD/IN HEADERS

ALC883 JACK

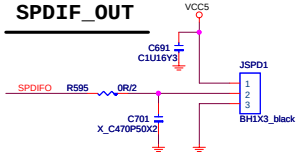




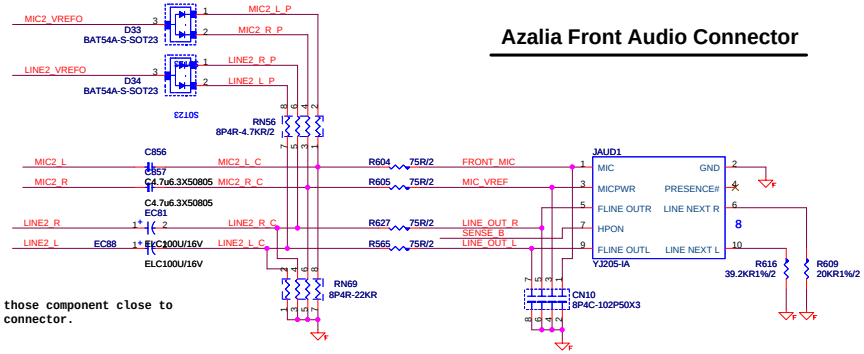
ALC883 JACK DETECT



SPDIF_OUT

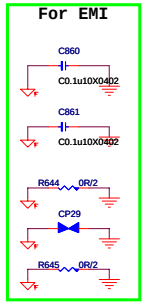


Azalia Front Audio Connector

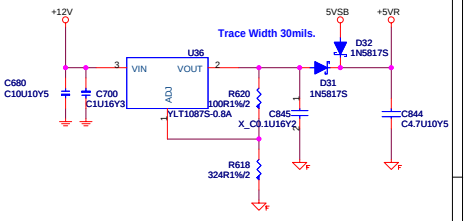


Place those component close to audio connector.

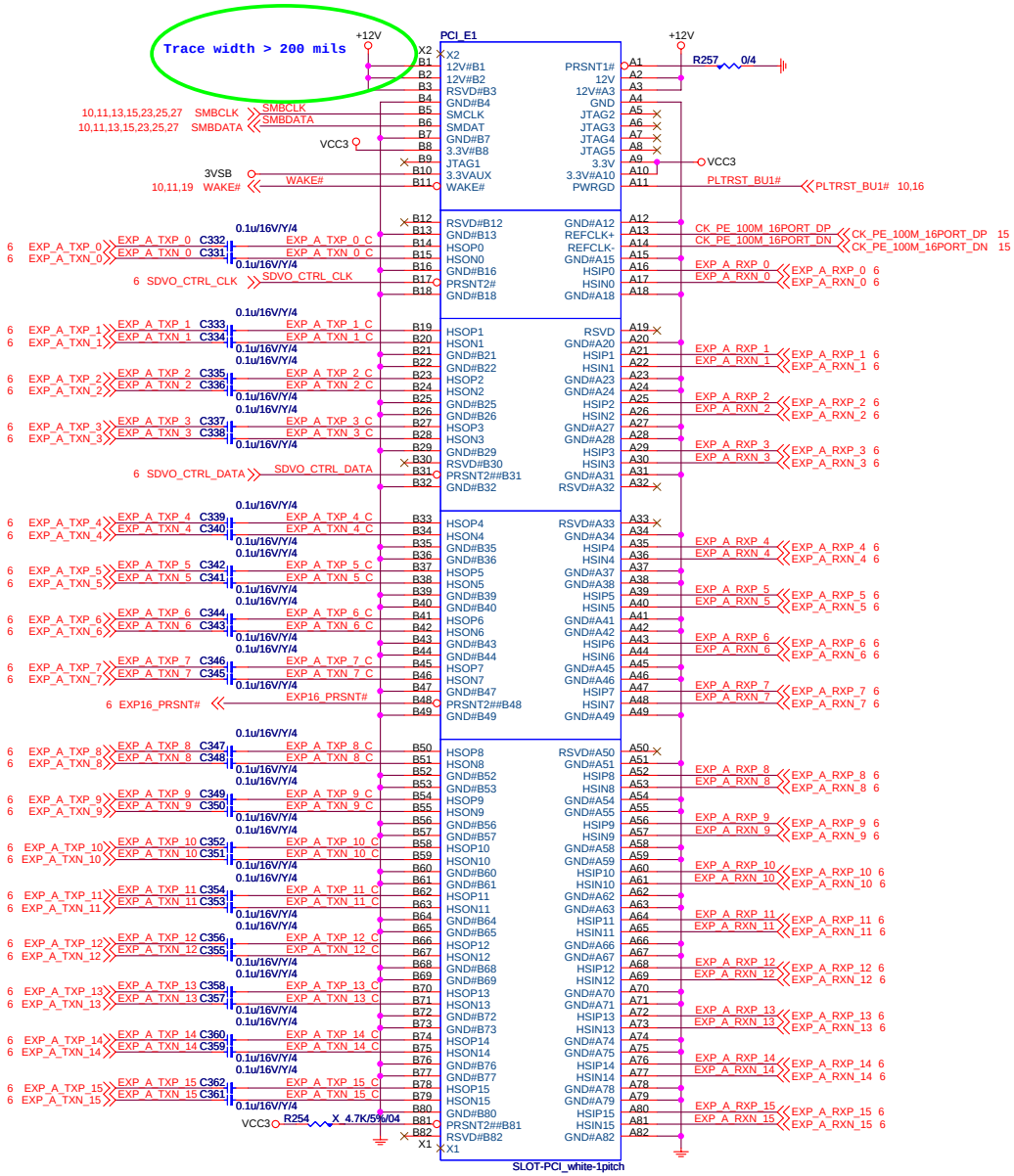
For EMI



AUDIO CODE REGULATORS

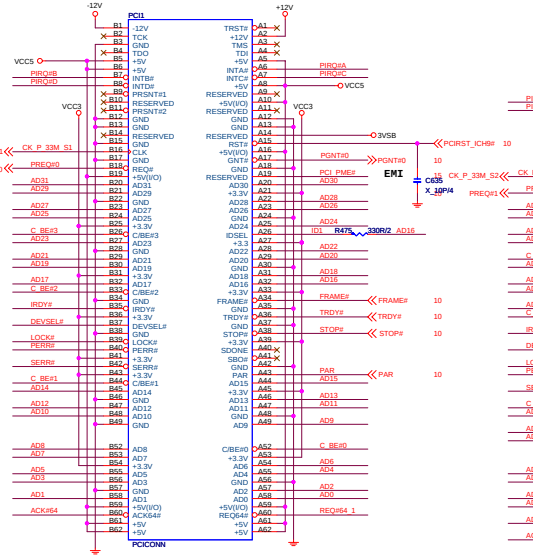


PCI_Express X16 Slot

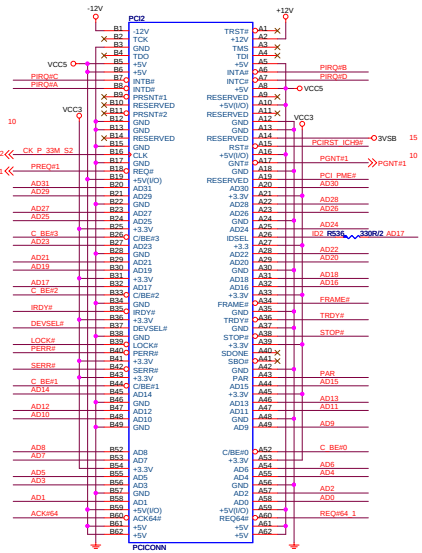


MICRO-STAR INT'L CO.,LTD	
MS-7395	
Size: Custom	Document Description: PCIE x16, x4, x1 & Bus Switch
Rev: 0A	
Date: Wednesday, August 15, 2007	Sheet 21 of 33

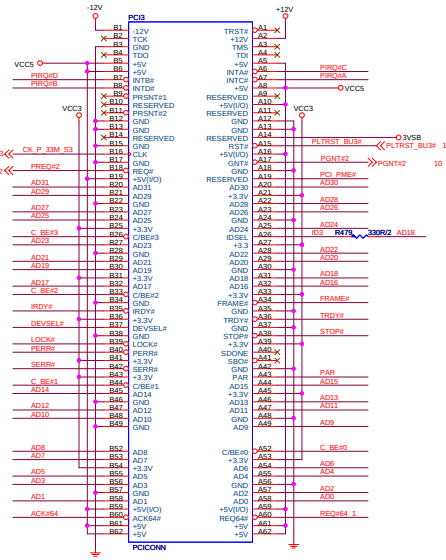
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



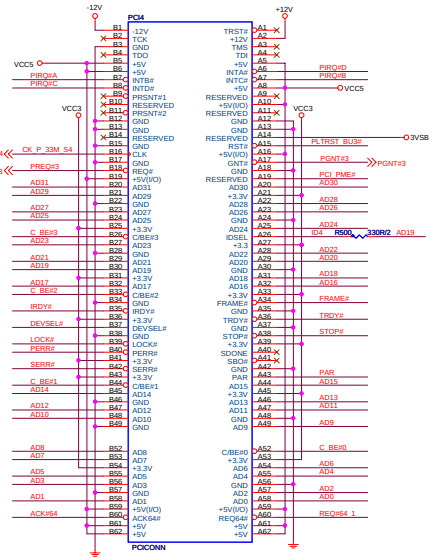
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



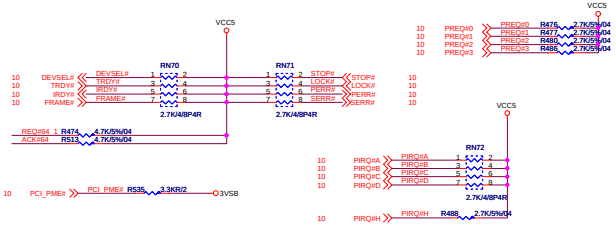
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



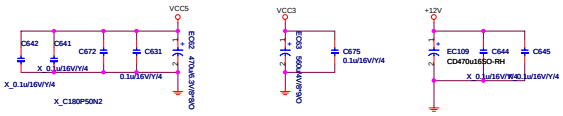
PCI SLOT 4 (PCI VER: 2.2 COMPLY)



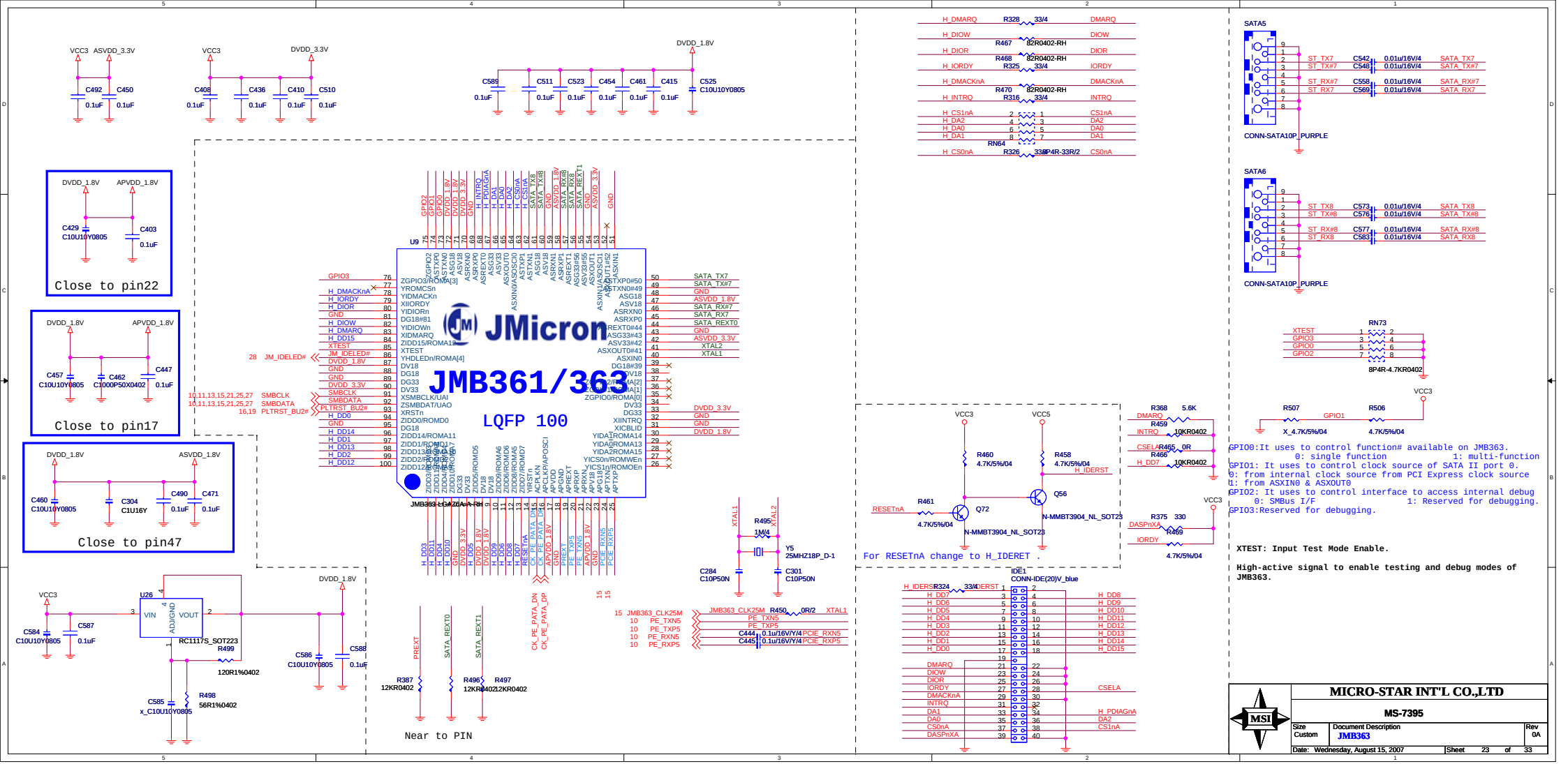
PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MSI	MICRO-STAR INT'L CO.,LTD
	MS-7395
Size: Custom	Document Description: PCI Slot 1 & 2 & 3 & 4 — Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 22 of 33



GPIO0:It uses to control function# available on JMB363.
0: single function 1: multi-function
GPIO1: It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
GPIO2: It uses to control interface to access internal debug
0: SMBus I/F 1: Reserved for debugging.
GPIO3:Reserved for debugging.

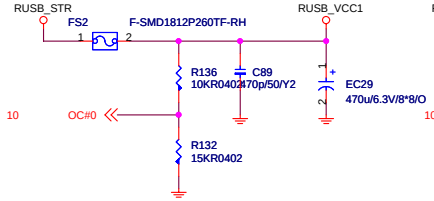
XTEST: Input Test Mode Enable.

High-active signal to enable testing and debug modes of JMB363.

Rear USB Connector

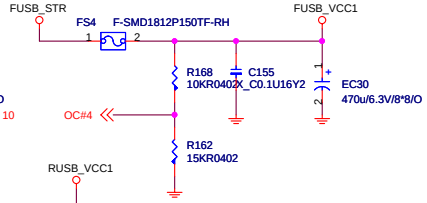
USB POWER FOR PORT 0,1

NEAR CONNECTOR

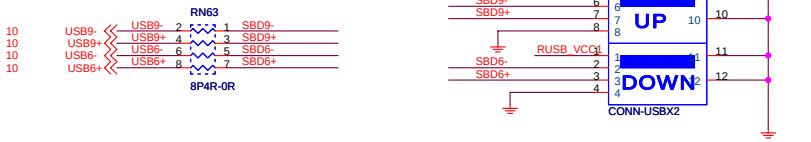


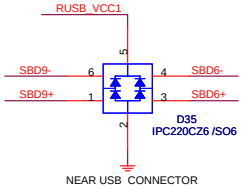
USB POWER FOR PORT 6,7,8,9

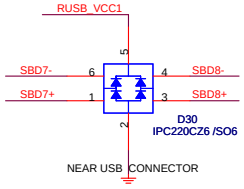
NEAR CONNECTOR



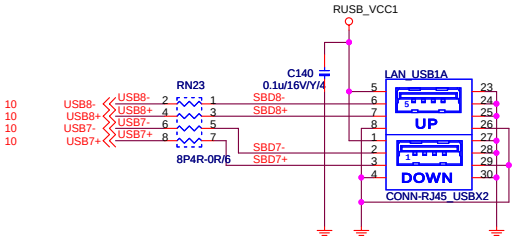
REAR USB PORT 0,1

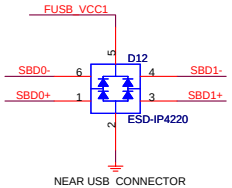




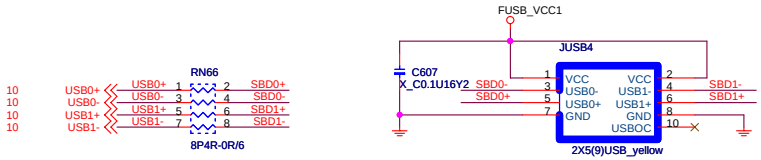


REAR USB PORT 2,3 (With LAN)





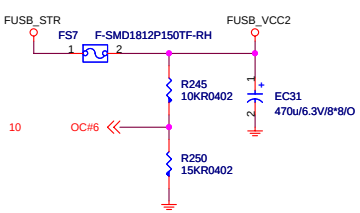
FRONT USB PORT 0,1



Front USB Connector

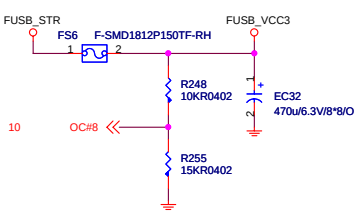
USB POWER FOR PORT 6,7

NEAR CONNECTOR



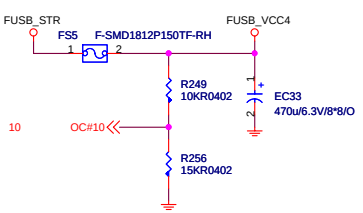
USB POWER FOR PORT 6,7

NEAR CONNECTOR

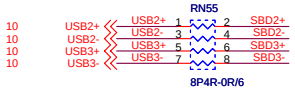


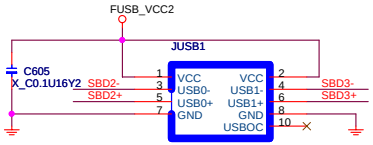
USB POWER FOR PORT 6,7

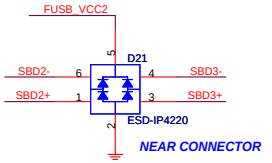
NEAR CONNECTOR



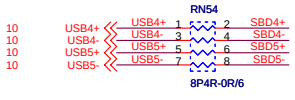
FRONT USB PORT 2,3

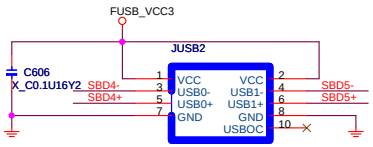


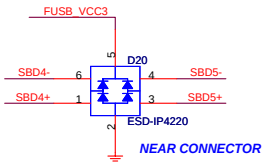




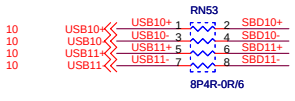
FRONT USB PORT 4,5

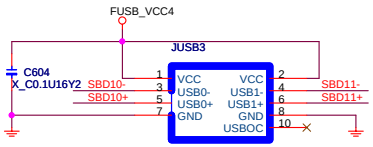


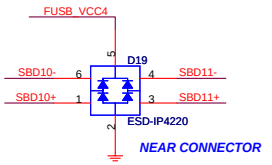




FRONT USB PORT 10,11





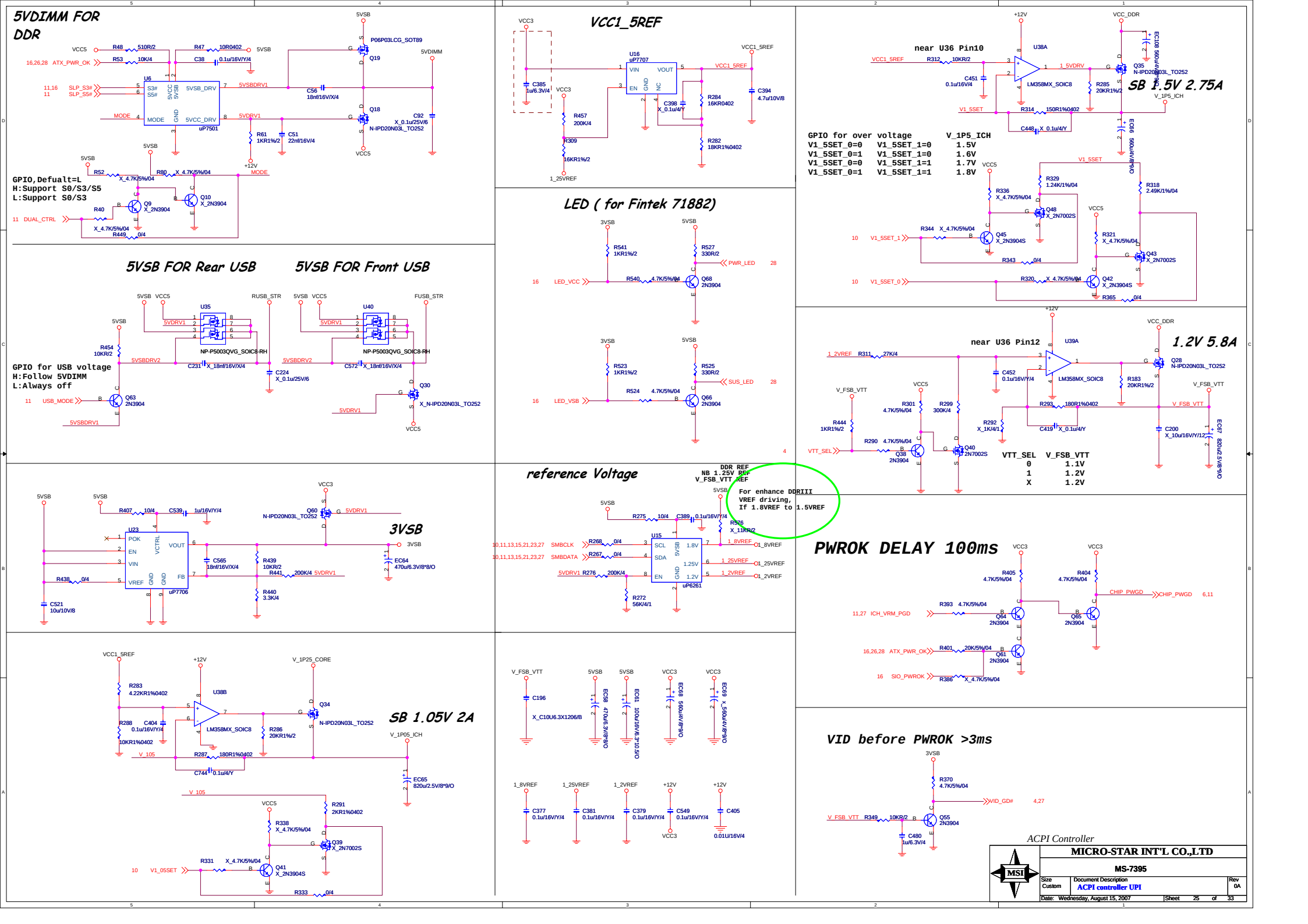


MICRO-STAR INT'L CO.,LTD

MS-7395

Size	Document Description	Rev
Custom	USB Connector	0A

Date: Wednesday, August 15, 2007 Sheet 24 of 33


5VDIMM FOR DDR
GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3
5VSB FOR Rear USB
5VSB FOR Front USB
GPIO for USB voltage
H:Follow 5VDIMM
L:Always off
VCC1_5REF
LED (for Fintek 71882)
reference Voltage
DDR REF
NB 1.25V REF
V_FSB_VTT REF
For enhance DDRIII
VREF driving,
If 1.8VREF to 1.5VREF
near U36 Pin10
SB 1.5V 2.75A
GPIO for over voltage V_1P5_ICH
V1_5SET_0=0 V1_5SET_1=0 1.5V
V1_5SET_0=1 V1_5SET_1=0 1.6V
V1_5SET_0=0 V1_5SET_1=1 1.7V
V1_5SET_0=1 V1_5SET_1=1 1.8V
near U36 Pin12
1.2V 5.8A
VTT_SEL V_FSB_VTT
0 1.1V
1 1.2V
X 1.2V
3VSB
PWROK DELAY 100ms
SB 1.05V 2A
VID before PWROK >3ms
ACPI Controller
MICRO-STAR INT'L CO.,LTD
MS-7395
Size Custom
Document Description ACPI controller UPI
Rev 0A
Date: Wednesday, August 15, 2007
Sheet 25 of 33

DDR II 1.8V POWER

Iripple=21*0.6*0.8/1=10.08A
2.22*3*1.7=11.322A>10.08A

D3 S-BAT54C_SOT23
+12V
5VDIMM
R96 X_0/6
D4 X_BAT54A
R82 2.2/8
C61 1u/25V/X/8
2.2R/0805
R1027
C76 0R0805
R110
1u/25V/X/8
U7 Vref VCC BOOT PHASE UG LG GND FB uP6103
1_8VREF
R112 2KR1%/2
R577 X_10KR1%/2
R577 for DDRIII VREF
(1.8VREF to 1.5VREF)
C74 0.1u/16V/Y/4
R86 3.01KR1%/2
C63 X_0.01U/16V/4
C281 X_0.01U/16V/4
R236 X_1K/4/1
CLOSED DDR POWER PIN4
5VSB
R98 1KR1%/2
C524 0.1u/16V/Y/4
Q15 2N7002S
11,15 SLP_S4#
R70 1KR1%/2
Q13 2N3904
Q17 2N3904
R419 20KR1%/2
ATX_PWR_OK 16,25,28
5VDIMM_IN
C108 10u/10V/8
C105 0.1u/16V/Y/4
EC80 470u/6.3V/8*8/O
EC82 470u/6.3V/8*8/O
EC83 X_470u/6.3V/8*8/O
CHOKE2 CH-1.2U18A
C103 X_0.01U/16V/4
C102 1000P/16V/4
5VDIMM
Q23 P70N02LDG
Q24 P70N02LDG
R1029 0R0805
R93 X_1K/4/1
VCC_DDR
CHOKE3 CH-1.1U25A
R169 2.2/8
C152 3.3n/50V/X/4
C168 1u/10V/6
EC73 560u/4V/8*9/O
EC74 560u/4V/8*9/O
EC75 560u/4V/8*9/O
9.4A+4.3A+2.75A+5.8A=22.25A
Irms(MAX) of VCC_DDR=22A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

DDR VTT Power

3VSB
U10 VREF2 ENABLE VCNTL BOOT_SEL VIN GND VREF1 VOUT GND
W83310DS
1.25V/2.9A
DDRVTT_R
EC103 560u/4V/8*9/O
R185 1K/6/1
R186 1K/6/1
EC87 100u/16V/6.3*10.5/O
EC92 560u/4V/8*9/O
VTT_DDR
C220 X_0.1u/16V
C158 0.1u/16V/Y/4
C207 0.1u/16V/Y/4
C237 0.1u/16V/Y/4
de- VCC_DDR high frequency noise.

NB 1.25V POWER

+12V
D13 X_BAT54A
R187 2.2/8
C229 1u/25V/X/8
U11 Vref VCC BOOT PHASE UG LG GND FB uP6103
1_25VREF
R200 2KR1%/2
C245 0.1u/16V/Y/4
R196 3.01KR1%/2
C235 X_0.01U/16V/4
C276 X_0.01U/16V/4
R199 X_1K/4/1
VCC3_IN
C274 10u/10V/8
C259 0.1u/16V/Y/4
EC85 470u/6.3V/8*9/O
EC84 470u/6.3V/8*9/O
CHOKE4 CH-1.2u8A6m-RH
VCC5
C239 X_0.01U/16V/4
Q33 P60N03LDG
Q31 P70N02LDG
R1031 0R0805
R1021 0R0805
C242 1u/25V/X/8
2.2R/0805
R201
R233 X_1K/4/1
CHOKE5 V_1P25_CORE
CH-1.2u18A4m-RH
C298 X_100PF/10V/6
R207 2.2/8
C258 3.3n/50V/X/4
C243 1u/10V/6
EC76 820u/2.5V/8*9/O
EC78 820u/2.5V/8*9/O
EC79 820u/2.5V/8*9/O
C285 X_100PF/10V/6
16.3A
Irms(MAX) of VCC1_25=16.3A
Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A

CHANNEL B V_SM_VTT DECOUPLING CAPS

VCC_DDR VTT_DDR
C208 X_0.1u/16V/Y/4
C209 X_0.1u/16V/Y/4
C210 X_0.1u/16V/Y/4
C211 X_0.1u/16V/Y/4
C219 0.1u/16V/Y/4
C393 0.1u/16V/Y/4
C236 X_C1U16Y3
C156 C1U16Y3
C169 C1U16Y3
C266 1000PF/10V/6
C213 0.1u/16V/Y/4
C216 0.1u/16V/Y/4
C221 0.1u/16V/Y/4
EC94 X_100PF/10V/6
C286 X_560u/4V/8*9/O
C287 1000PF/50V/4
C288 X_100PF/10V/6
C293 X_100PF/10V/6
C194 180p/50V/Y/4
C175 180p/50V/Y/4
C206 180p/50V/Y/4
C135 180p/50V/Y/4
C141 180p/50V/Y/4
C129 X_C4.7U35Y6
C127 X_C4.7U35Y6
C330 x_0.1u/16V/Y/4
C328 x_0.1u/16V/Y/4
C329 x_0.1u/16V/Y/4
C387 x_0.1u/16V/Y/4
C311 x_0.1u/16V/Y/4
C316 x_0.1u/16V/Y/4

CHANNEL A V_SM_VTT DECOUPLING CAPS

C163 180p/50V/Y/4
C150 0.1u/16V/Y/4
C205 180p/50V/Y/4
C186 180p/50V/Y/4
C157 0.1u/16V/Y/4
C214 C10U6.3X5R6
C218 C10U6.3X5R6

For EMI

VTT_DDR
C149 180p/50V/Y/4
C172 0.1u/16V/Y/4
C212 180p/50V/Y/4
C114 0.1u/16V/Y/4
+12V
C116 X_0.1u/16V/Y/4
C117 X_0.1u/16V/Y/4
VCC_DDR
C246 180p/50V/Y/4
C257 180p/50V/Y/4
C262 180p/50V/Y/4
C268 180p/50V/Y/4
V_1P25_CORE
C188 X_0.1u/16V/Y/4
C294 X_100PF/10V/6
C134 0.1u/16V/Y/4
C232 0.1u/16V/Y/4
C174 0.1u/16V/Y/4
C256 0.1u/16V/Y/4
C180 0.1u/16V/Y/4
C300 0.1u/16V/Y/4
C195 0.1u/16V/Y/4
C302 0.1u/16V/Y/4

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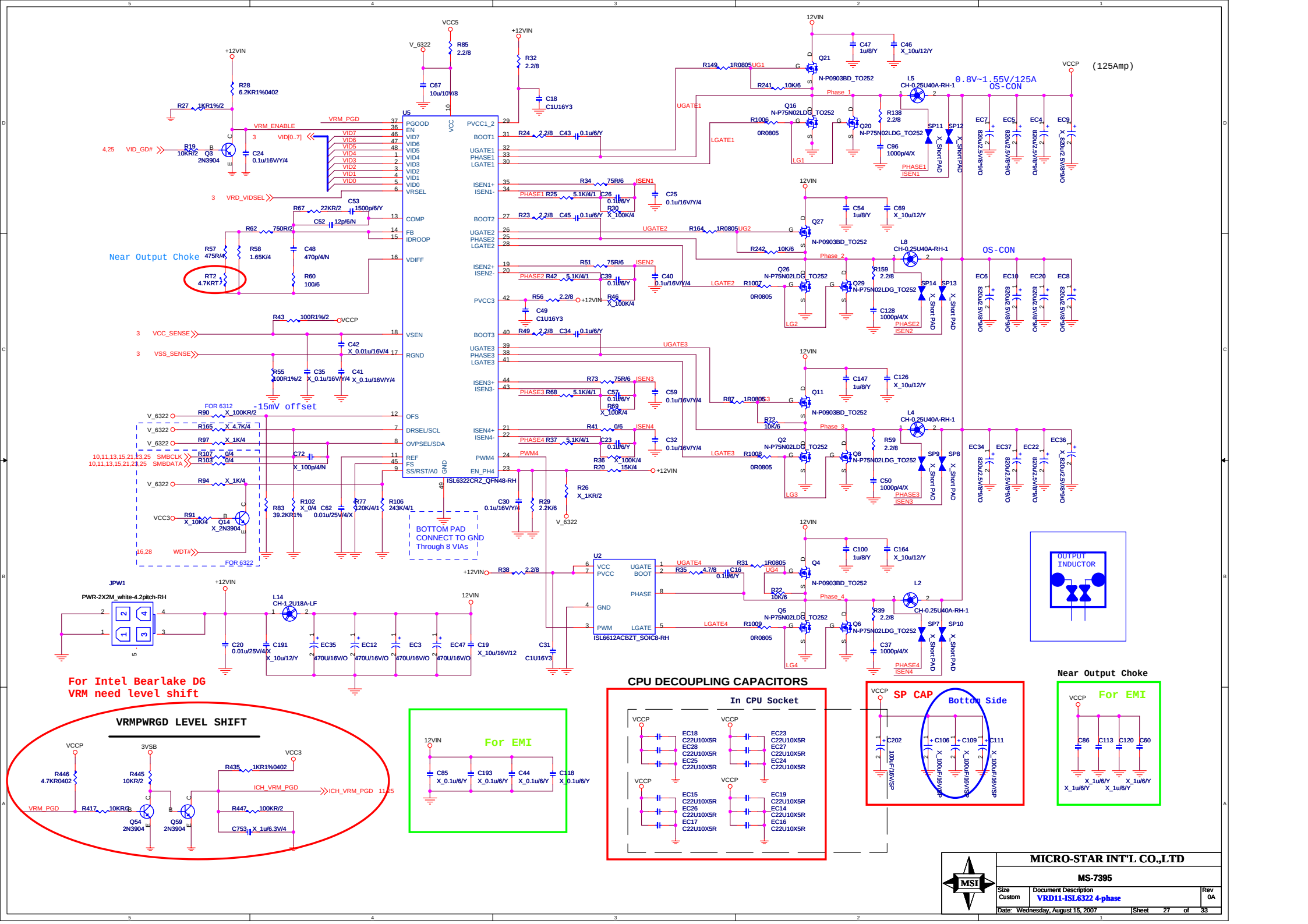
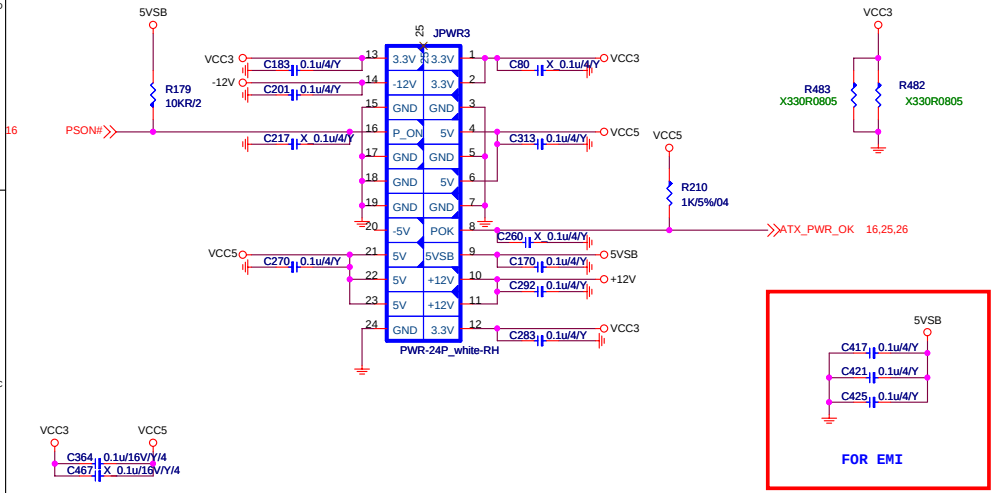
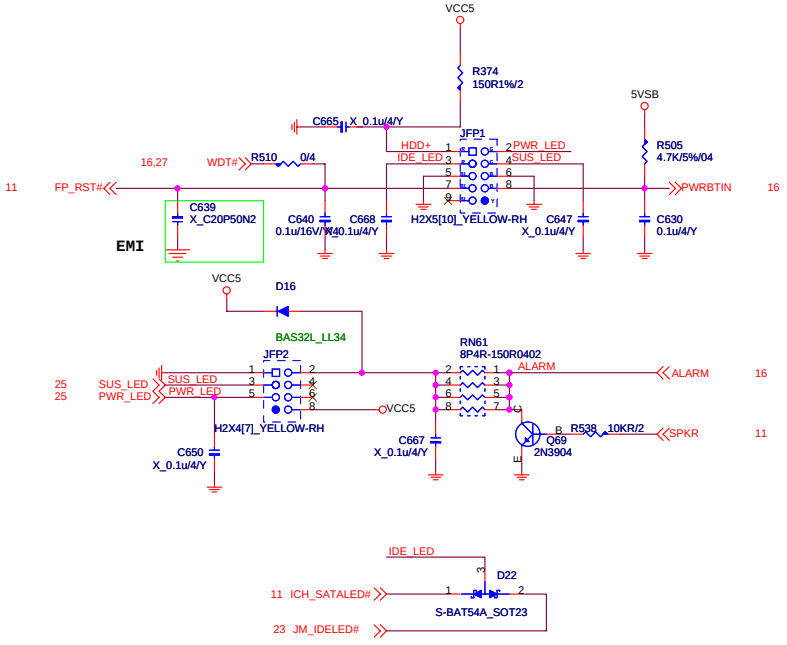
MS-7395
Size: Custom
Document Description: NB Core Power & DDR Power
Rev: 0A
Date: Wednesday, August 15, 2007
Sheet 26 of 33


U5
ISL6322CRZ_QFN48-RH
U2
ISL6612ACBZT_SOIC8-RH
Q21
Q16
Q20
Q27
Q26
Q29
Q11
Q2
Q8
Q4
Q5
Q6
L5
L8
L4
L2
CH-0.25U40A-RH-1
0.8V~1.55V/125A
OS-CON
(125Amp)
Near Output Choke
-15mV offset
FOR 6312
FOR 6322
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
OUTPUT
INDUCTOR
JPW1
PWR-2X2M_white-4.2pitch-RH
L14
CH-1.2U18A-LF
For Intel Bearlake DG
VRM need level shift
VRMPWRGD LEVEL SHIFT
For EMI
CPU DECOUPLING CAPACITORS
In CPU Socket
SP CAP
Bottom Side
Near Output Choke
For EMI
MICRO-STAR INT'L CO.,LTD
MS-7395
VRD11-ISL6322 4-phase
Wednesday, August 15, 2007
Sheet 27 of 33

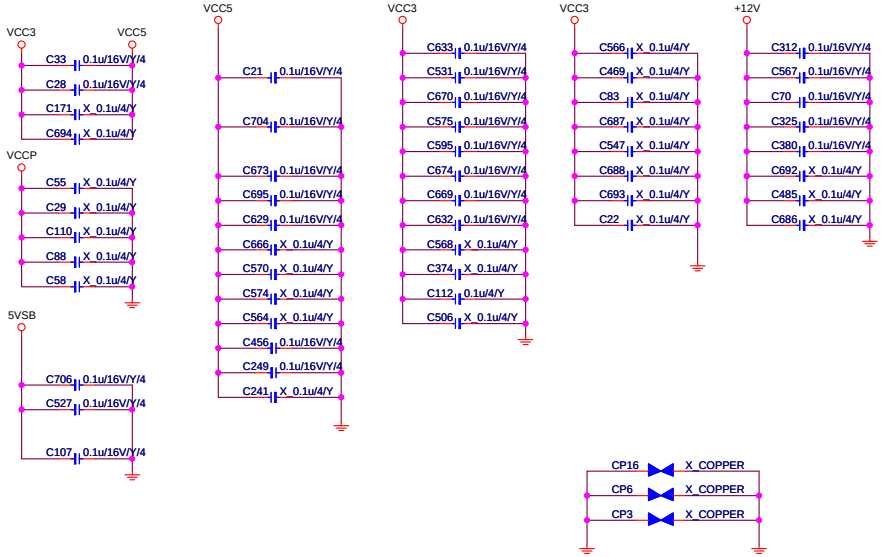
ATX POWER CONNECTOR



FRONT PANNEL



Cap. for EMI & Power



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	MS-7395	
Size: Custom	Document Description: ATX PWR-Connector & Front Panel	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 28 of 33	

Optical Fiducial Marks-120

FM14 FM11 FM15 FM2 FM12 FM13 FM8 FM9 FM10

X_FM X_FM X_FM X_FM X_FM X_FM X_FM X_FM X_FM

Optical Fiducial Marks-100

FM7 FM16 FM3 FM6 FM4 FM5 FM17 FM18 FM19

X_OPTICS X_OPTICS X_OPTICS X_OPTICS X_OPTICS X_OPTICS X_OPTICS X_OPTICS X_OPTICS

Mounting Holes

MH3 MH6 MH2 EMI KBGND MH5 MH4 MH7 MH8 MH9 MH10

Simulation

SIP2 SIP3 SIM2 VCC5 SIM1

X_PIN1*2 X_PIN1*2

BATTERY1

BATTERY-CR2032

HT1

MEC1 MEC2 MEC3 MEC4 MEC5 MEC6 MEC7

x_HS-0800342-RH

Resistor for P35/G33 of VGA Part

G33-R1 OPT X_150R1%/2

OnVGA1.3 OPT X_1.3KR1%/2

VCCA_C1 OPT X_0.01U/16V/4

VCCCRT_C1 OPT X_1u/6.3V/4

VCCCRT_C2 OPT X_0.1u/6.3V/4

For G33

NB_G33 OPT X_Intel G33

G33_logo OPT X_Intel G33

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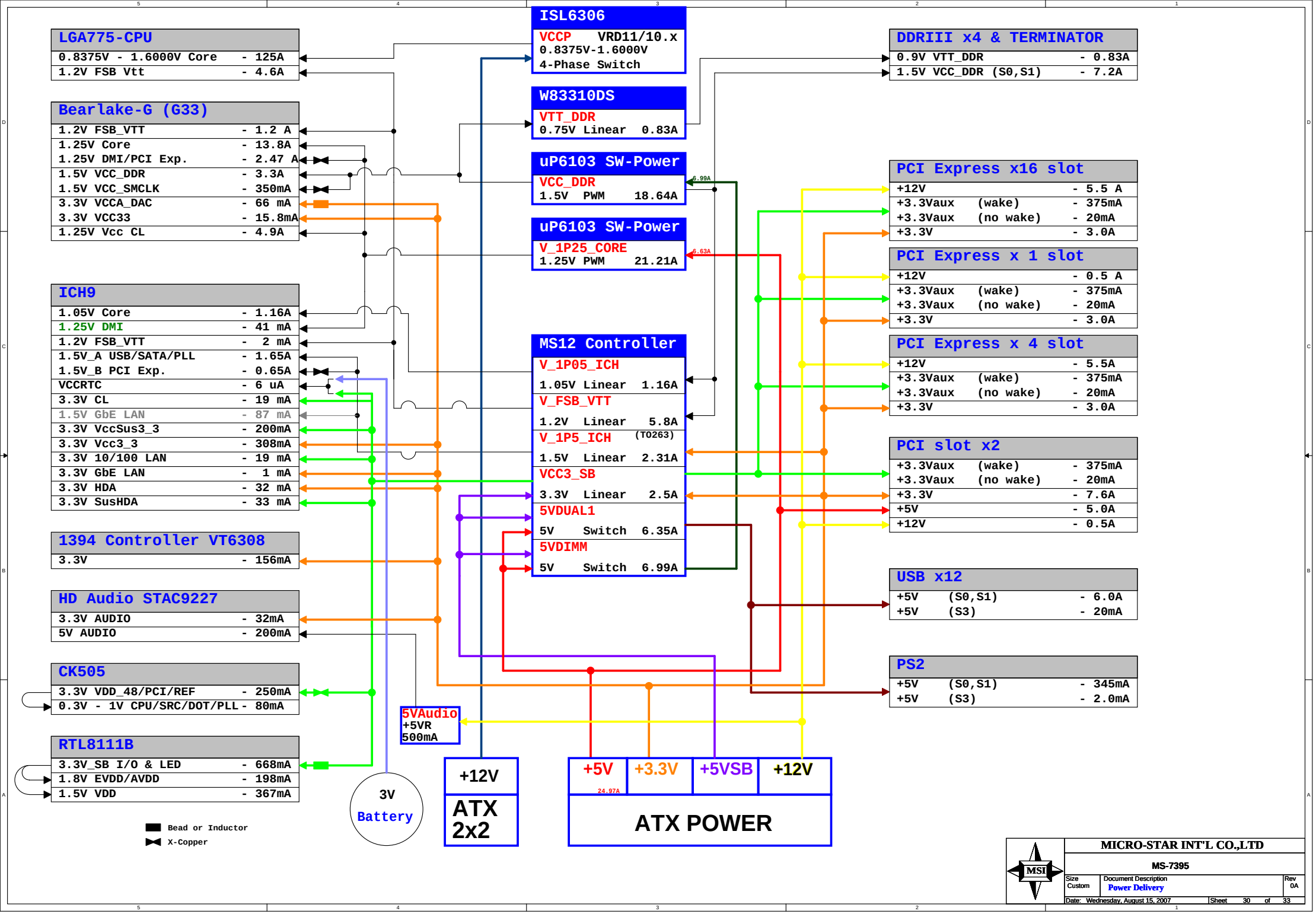
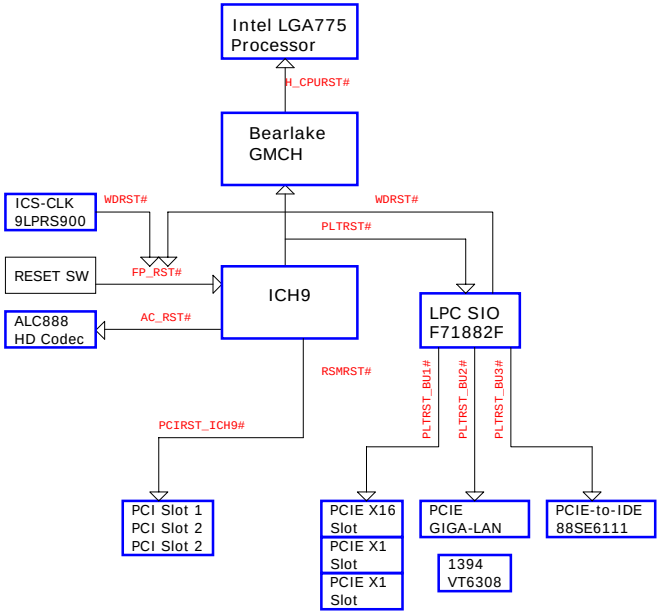
MS-7395

Size Custom | Document Description: Manual Parts & Option Parts | Rev 0A

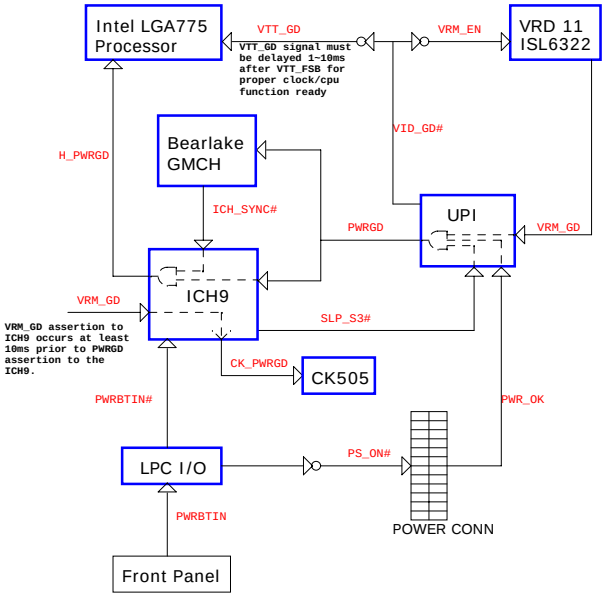
Date: Wednesday, August 15, 2007 | Sheet 29 of 33


LGA775-CPU
0.8375V - 1.6000V Core - 125A
1.2V FSB Vtt - 4.6A
Bearlake-G (G33)
1.2V FSB_VTT - 1.2 A
1.25V Core - 13.8A
1.25V DMI/PCI Exp. - 2.47 A
1.5V VCC_DDR - 3.3A
1.5V VCC_SMCLK - 350mA
3.3V VCCA_DAC - 66 mA
3.3V VCC33 - 15.8mA
1.25V Vcc CL - 4.9A
ICH9
1.05V Core - 1.16A
1.25V DMI - 41 mA
1.2V FSB_VTT - 2 mA
1.5V_A USB/SATA/PLL - 1.65A
1.5V_B PCI Exp. - 0.65A
VCCRTC - 6 uA
3.3V CL - 19 mA
1.5V GbE LAN - 87 mA
3.3V VccSus3_3 - 200mA
3.3V Vcc3_3 - 308mA
3.3V 10/100 LAN - 19 mA
3.3V GbE LAN - 1 mA
3.3V HDA - 32 mA
3.3V SusHDA - 33 mA
1394 Controller VT6308
3.3V - 156mA
HD Audio STAC9227
3.3V AUDIO - 32mA
5V AUDIO - 200mA
CK505
3.3V VDD_48/PCI/REF - 250mA
0.3V - 1V CPU/SRC/DOT/PLL - 80mA
RTL8111B
3.3V_SB I/O & LED - 668mA
1.8V EVDD/AVDD - 198mA
1.5V VDD - 367mA
Bead or Inductor
X-Copper
ISL6306
VCCP VRD11/10.x
0.8375V-1.6000V
4-Phase Switch
W83310DS
VTT_DDR
0.75V Linear 0.83A
uP6103 SW-Power
VCC_DDR
1.5V PWM 18.64A
6.99A
uP6103 SW-Power
V_1P25_CORE
1.25V PWM 21.21A
6.63A
MS12 Controller
V_1P05_ICH
1.05V Linear 1.16A
V_FSB_VTT
1.2V Linear 5.8A
V_1P5_ICH (TO263)
1.5V Linear 2.31A
VCC3_SB
3.3V Linear 2.5A
5VDUAL1
5V Switch 6.35A
5VDIMM
5V Switch 6.99A
5VAudio
+5VR
500mA
3V
Battery
+12V
ATX
2x2
+5V
24.97A
+3.3V
+5VSB
+12V
ATX POWER
DDRIII x4 & TERMINATOR
0.9V VTT_DDR - 0.83A
1.5V VCC_DDR (S0,S1) - 7.2A
PCI Express x16 slot
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x 1 slot
+12V - 0.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x 4 slot
+12V - 5.5A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI slot x2
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 7.6A
+5V - 5.0A
+12V - 0.5A
USB x12
+5V (S0,S1) - 6.0A
+5V (S3) - 20mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
MICRO-STAR INT'L CO.,LTD
MS-7395
Size Custom
Document Description
Power Delivery
Rev 0A
Date: Wednesday, August 15, 2007
Sheet 30 of 33

RESET MAP



PWROK MAP



12V

5V

3.3V

1.5VREF

NB 1.25V Core

VDDR

SB 1.5V

V_FSB_VTT

VID_GD

VTT_PWGD

VRM_EN

CPU VCore

VRMGD to SB

CK_PGD

CHIP_GD

PL_RST

PCI_RST

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7395	
Size: Custom	Document Description: Reset Map & PWROK Map	Rev: 0A
Date: Wednesday, August 15, 2007	Sheet 31 of 33	

ICH8

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2/3_FANTAC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	P/N_DDR0_A	P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A	P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B	P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B	P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394

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MS-7395

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Date: Wednesday, August 15, 2007 | Sheet 32 of 33

HW 7360 Ver.0A Change to Ver.0B List:
1.Remove Q54 and R374and short Q54 B,C pin for power sequence.(page26)
2.U24 power change from VCC3 to 3VSB for power sequence.(page26)
3.Change EC42 from 470u to 820u for V_FSB_VTT power noise.(page26)
4.Change EC52 from 470u to 820u for SB1_05 power noise.(page26)
5.Change EC53 from 470u to 820u for SB1_5 power noise.(page26)
5.CPU_GTLREF resistor value R119 , R115, R128, R104 change from 50ohm to 100ohm for pull-up(intel suggestion)(page4)
6.CPU_GTLREF resistor value R124 , R117 , R141 , R105 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page4)
7.MCH_GTLREF resistor value R190 change from 50ohm to 100ohm for pull-pu.(intel suggestion)(page6)
8.MCH_GTLREF resistor value R195 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page6)
9.SRCOMP[3:0] R223 , R227 , R184 , R182 change from 20ohm to 19.1ohm.(intel suggestion)(page7)
10.DDR2 termination RN16 , RN26 , RN11 , RN14 , RN27 , RN12 , R171 change from 39ohm to 43ohm.(intel suggestion)(page14)
11.Add CK_DOT96_MCH_DP pull-high 1.25V and CK_DOT96_MCH_DN pull-down for non-graphic SKU.(intel suggestion)(page6)
12.RIRQ[H:A] pull-up 2.7Kohm to VCC5.(intel suggestion)(page22)
13.USB have two group [5:0] EHCI#1,[6:11EHCI#2 , please one group to real and one group to front.(intel suggestion)(page24)
14.Audio VREFOUT_E and VREFOUT_F swap.(for schematic error)(page20)
15.Audio BASS and CEN_OUT swap.(for schematic error)(page20)

7395 OA Modify from 7360 1.0

1.Change Marvell 88se6111 to JMICRO 363
2.Remove 1394
3.Remove PCIE*1 SLOT PCI_E3, PCI_E4
4.Add PCI SLOT PCI3, PCI4
5.Add 8111B CO-LAY 8111C CIRCUIT
6. Change CPU FAN-----Smart FAN
  SYS FAN1-------- DC MODE FAN
  SYS FAN2, SYS FAN3---------- FULL SPEED, no sense
7.Add COM2 support circuit
8.Change VRM11 3 Phase 12pcs to 4 Phase 12 pcs
9.add TPM Support circuit
10.clk-gen: change pin 11 from WDT# to PCI CLK.(PAGE15)
11.Change NB,SB heatsink to E31-0800342-A21
12. pin31,pin25 connect to GND through cp.(page 19)
13. chang R193,R194 to 51+/- 5%.follow intel design guide (page 6)
14. chang R101 to 130 +/- 5%.follow intel design guide (page 3)
15. Remove c273.
16. oc# divide resistor form R1=27k,R2=51K to R1=10K,R2=15K .(page 24)
17. Remove lan chip reversed 25M crystla for layout
18.Change choke4 to L04-12A7141-T15
Change choke5 to L04-12A7171-W15(1.25 V Core power)
19. Change audio coupling cap from DIP TO SMD.
20. Change ALL EL CAP TO OSC
21. Add OC CIRCUIT BY USING JUMP
22.Removeing ICH9-R CO-LAY CIRCUIT
23. Change PCIRST#, PLTRST# Delivery!
24. Change vcc_1p25 regulator from VCC5.