MS-7392

Version： 2.2

CPU:

Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel - MCH (North Bridge) P31
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI EEPROM
HD Codec -- ALC888
LPC Super I/O -- F71882
LAN-- REALTEK RTL8111C/8111B
CLOCK -- ICS9LPRS908DGLF

Main Memory:

DDR II * 4 (Max 4GB)

Expansion Slots:

PCI2.3 SLOT * 3
PCI EXPRESS X1 SLOT * 2
PCI EXPRESS X16 SLOT

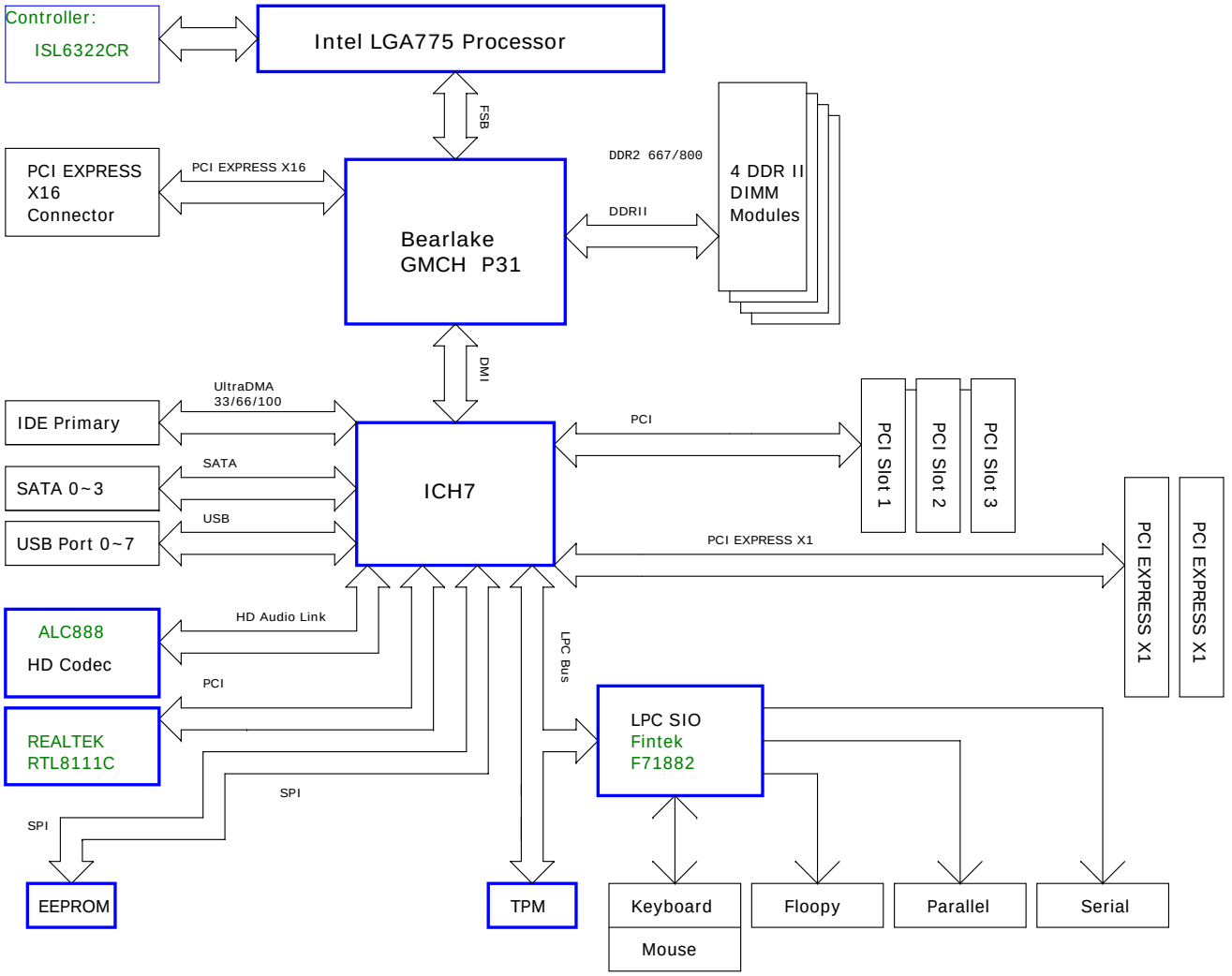
INTELSIL PWM:

Controller: INTELSIL - ISL6322CR

MICRO-STAR INt'L CO., LTD.

Title: COVER SHEET		
Size	Document Number: MS-7392	Rev: 2.2
Date: Wednesday, April 30, 2008	Sheet 1 of 35	

Block Diagram



MSI MICRO-STAR INt'L CO., LTD.

Title	BLOCK DIAGRAM	
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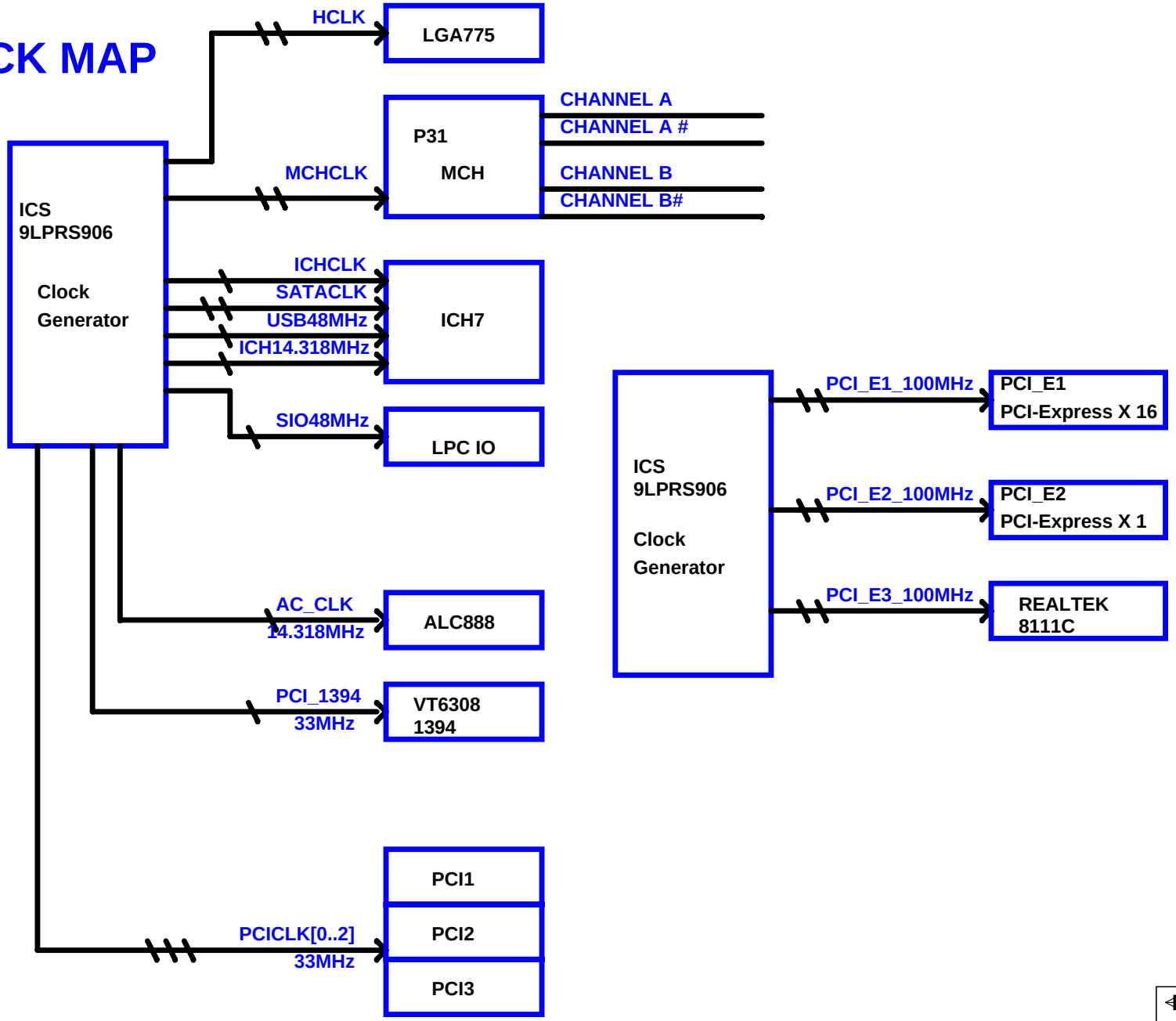
CLOCK MAP



MICRO-STAR INt'L CO., LTD.

Title	CLOCK MAP	
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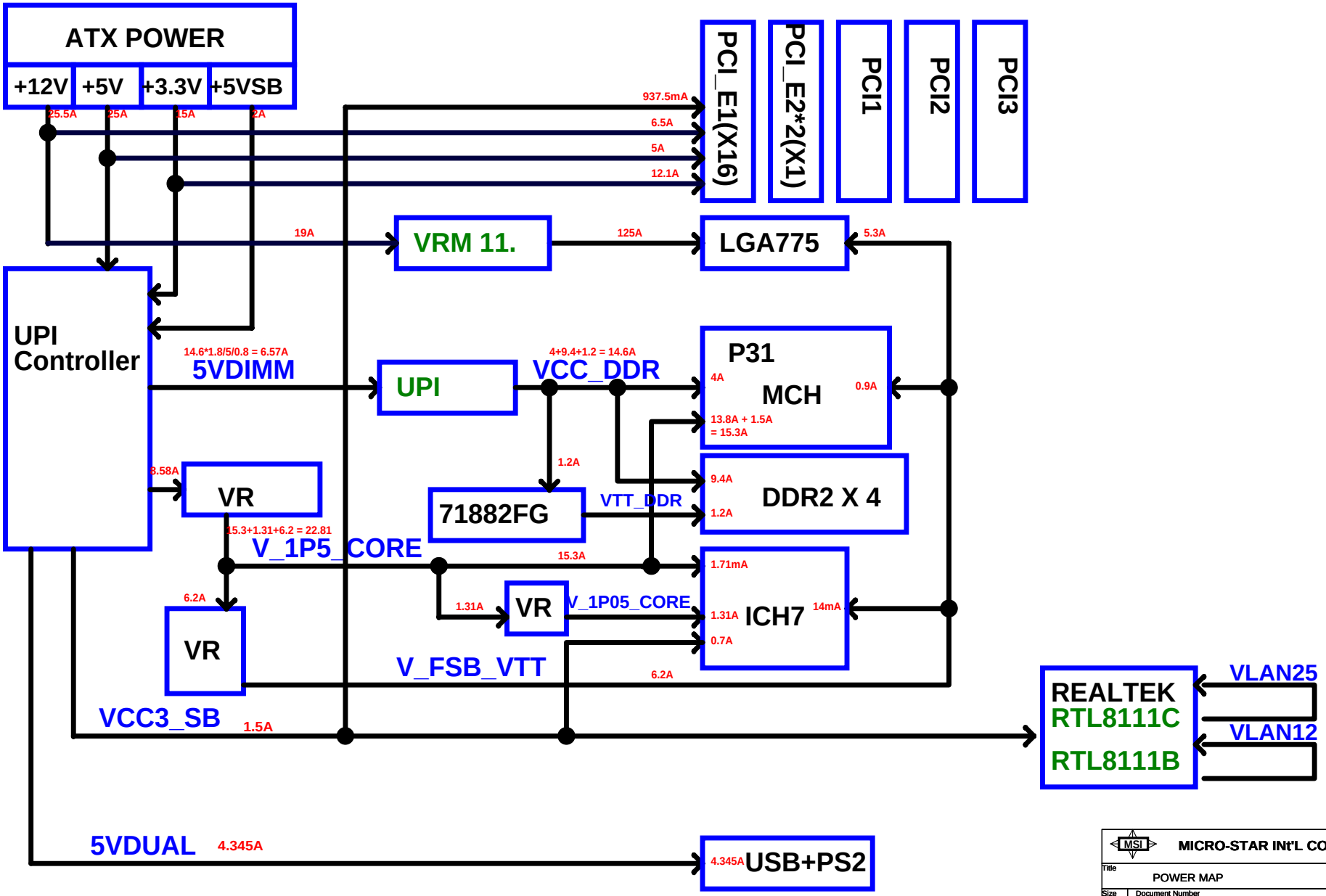
POWER MAP



MSI	MICRO-STAR INt'L CO., LTD.	
Title	POWER MAP	
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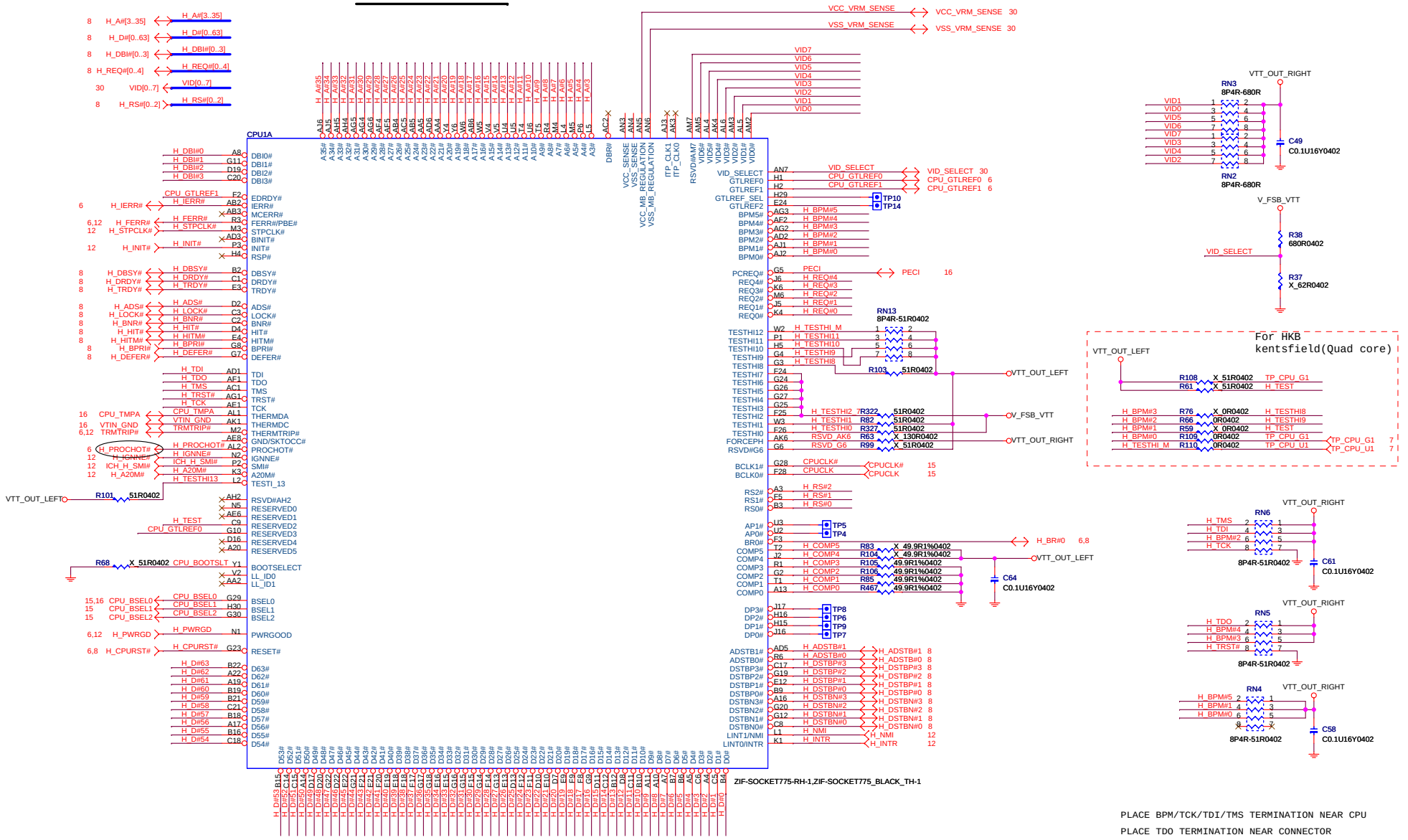
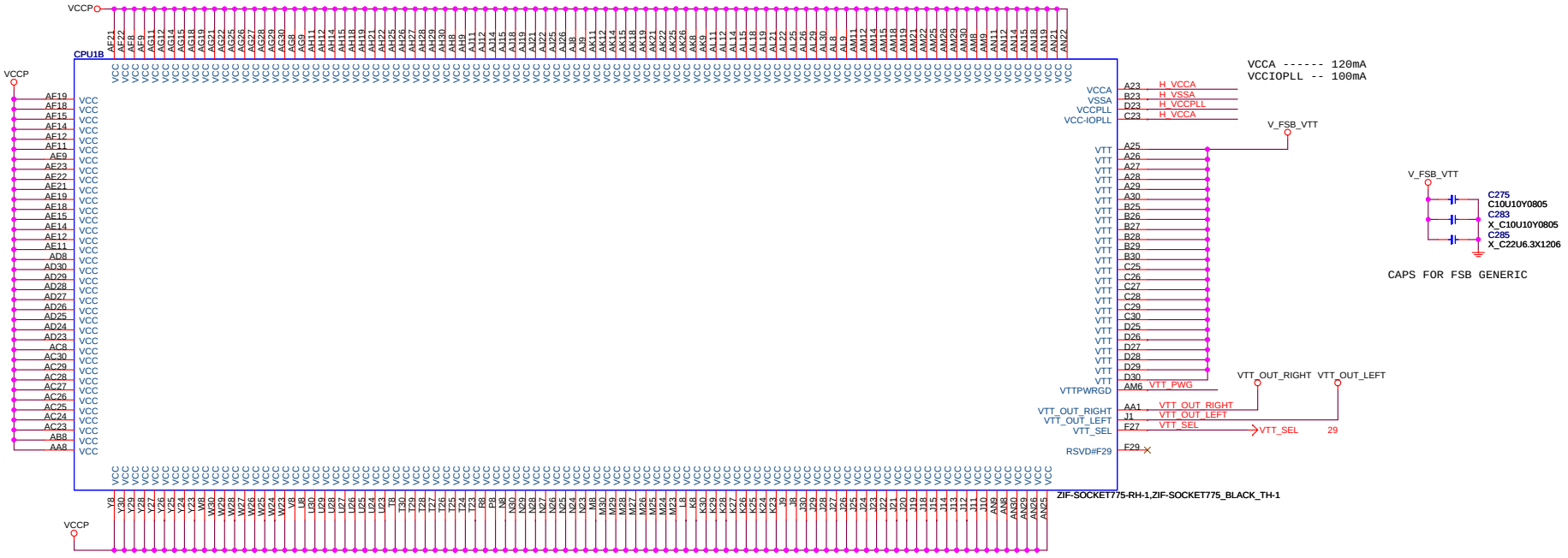
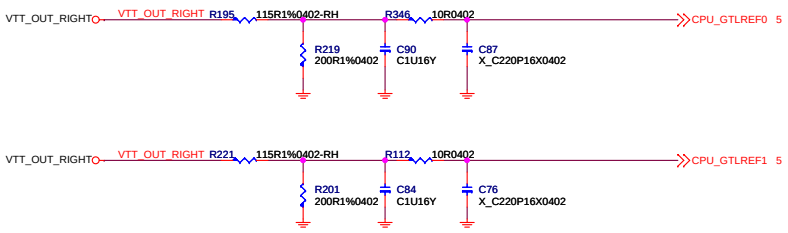
CPU SIGNAL BLOCK



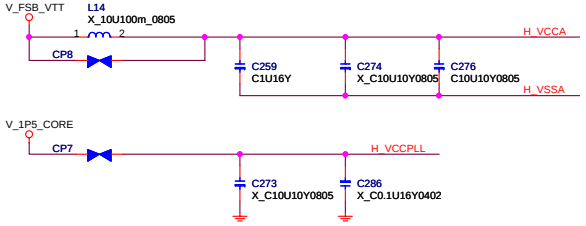


GTLREF VOLTAGE SHOULD BE0.635*VTT

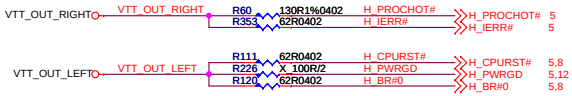
57.6ohm and 100ohm divider



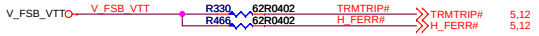
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

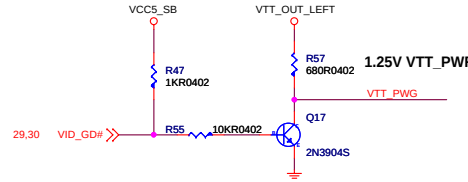


PLACE AT CPU END OF ROUTE



PLACE AT ICH END OF ROUTE





VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

MICRO-STAR INt'L CO., LTD.

Title	Intel LGA775 CPU - Power	
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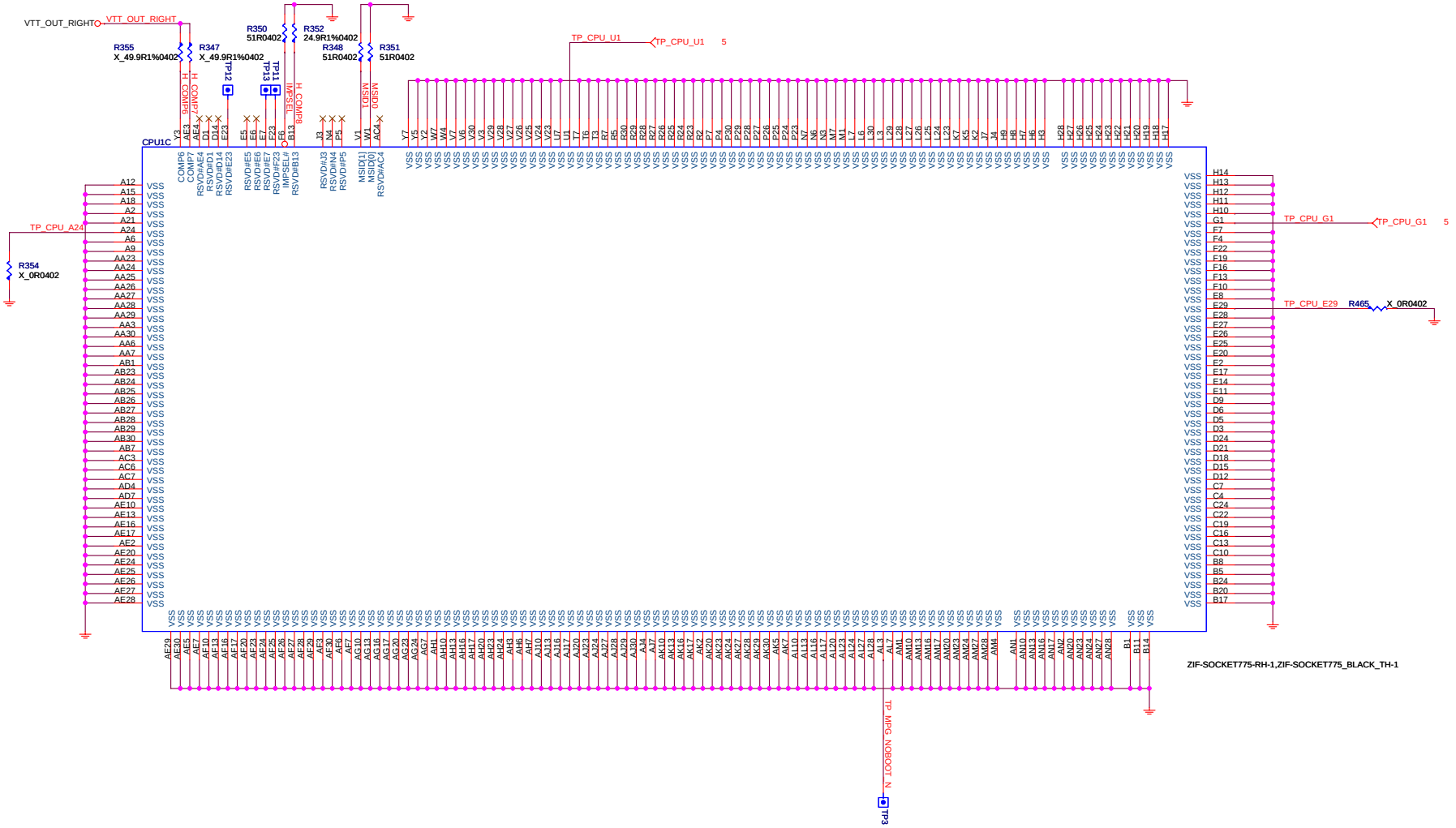
	2005 Performance FMB platform 1	2005 Mainstream/Value FMB platform 2	2006 65W FMB platform 3
MSID1	0	0	0
MSID0	0	NC	NC



MSI MICRO-STAR INt'L CO., LTD.

Title: Intel LGA775 CPU - GND

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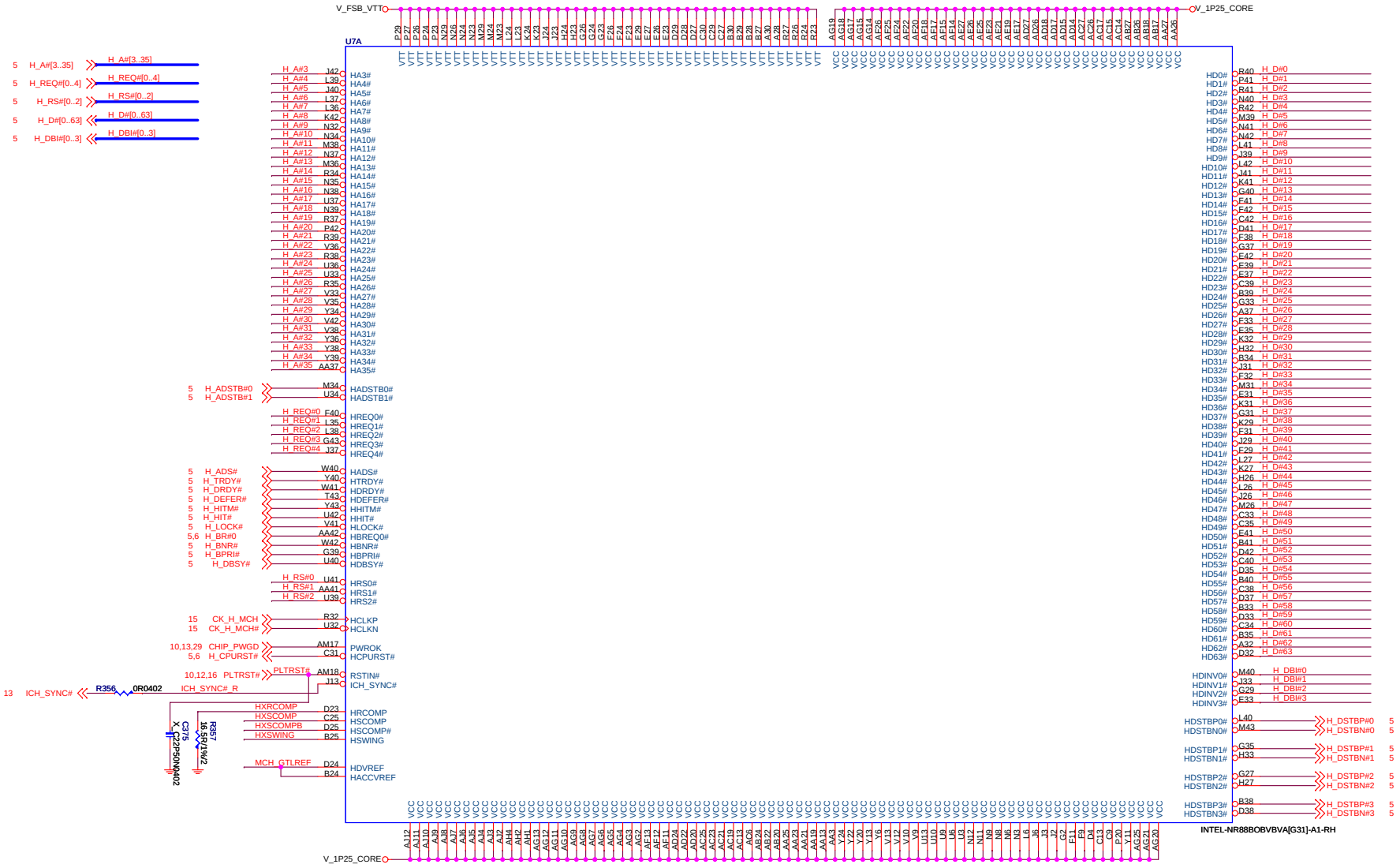
Date: Tuesday, April 29, 2008 | Sheet 7 of 35

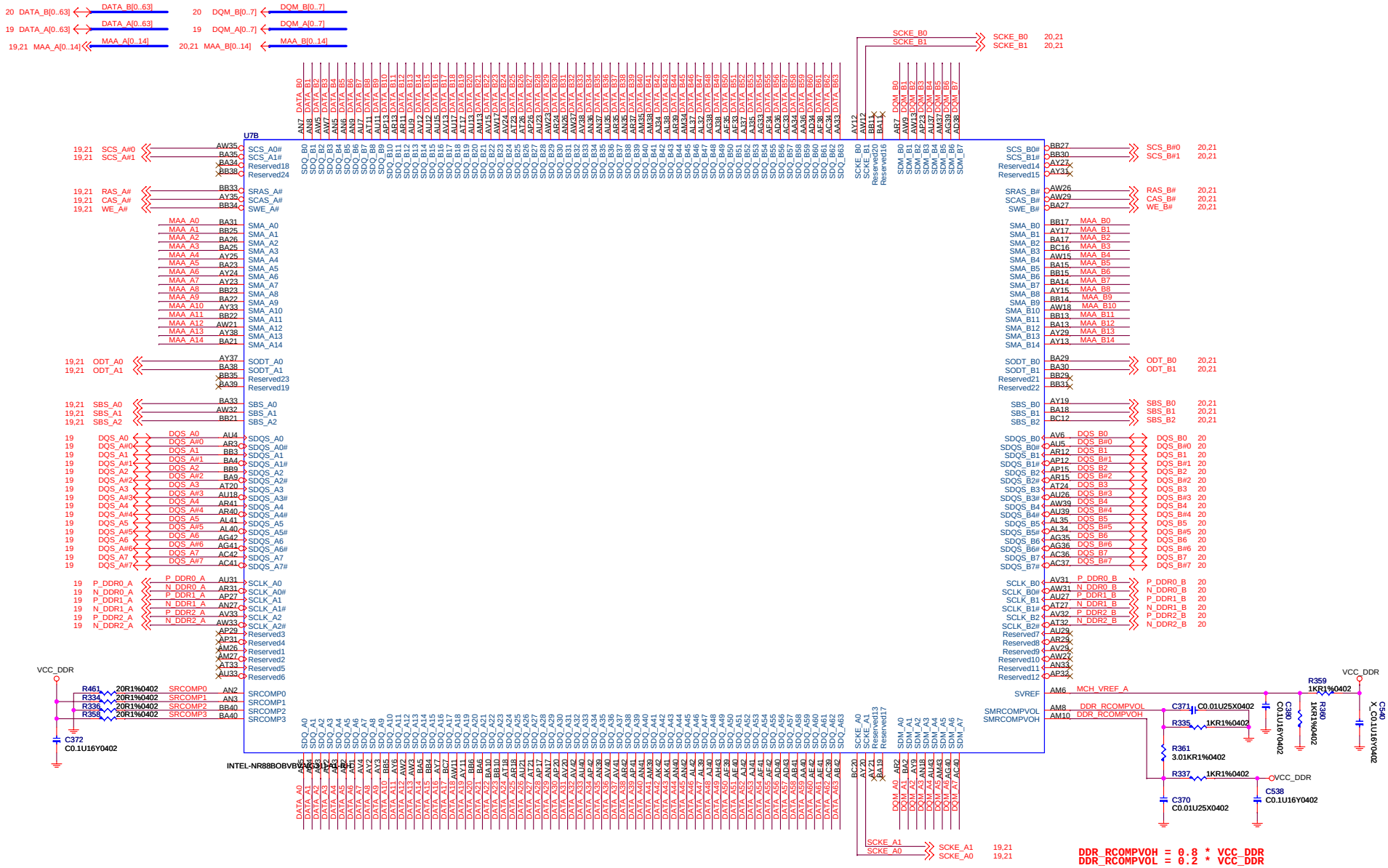


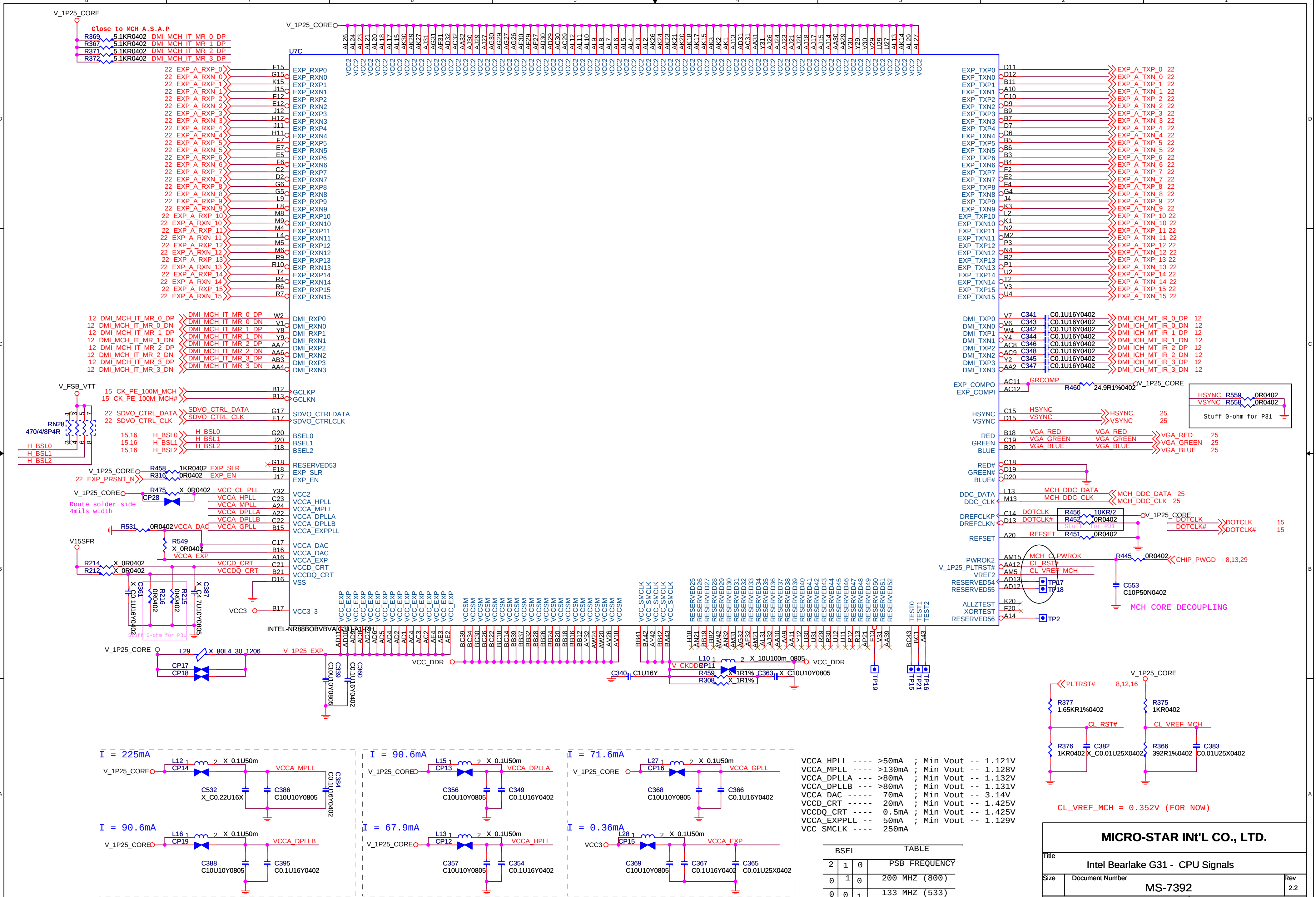
MSI MICRO-STAR INt'L CO., LTD.

Title: Intel Bearlake G31 - CPU Signals

Size	Document Number	Rev
	MS-7392	2.2

Date: Friday, May 16, 2008 Sheet 8 of 35


U7B
INTEL-NR88BOBVBV
DDR_RCOMPVOH = 0.8 * VCC_DDR
DDR_RCOMPVOL = 0.2 * VCC_DDR
PLACE 0.1UF CAP CLOSE TO MCH
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G31 - CPU Signals
MS-7392
Rev 2.2
Friday, May 16, 2008
Sheet 9 of 35



VCCA_HPLL ---- >50mA ; Min Vout -- 1.121V
VCCA_MPLL ---- >130mA ; Min Vout -- 1.128V
VCCA_DPLLA --- >80mA ; Min Vout -- 1.132V
VCCA_DPLLB --- >80mA ; Min Vout -- 1.131V
VCCA_DAC ----- 70mA ; Min Vout -- 3.14V
VCCD_CRT ----- 20mA ; Min Vout -- 1.425V
VCCDQ_CRT ---- 0.5mA ; Min Vout -- 1.425V
VCCA_EXPPLL -- 50mA ; Min Vout -- 1.129V
VCC_SMCLK ---- 250mA

BSEL TABLE

2	1	0	PSB FREQUENCY
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

MICRO-STAR INt'L CO., LTD.

Title: Intel Bearlake G31 - CPU Signals

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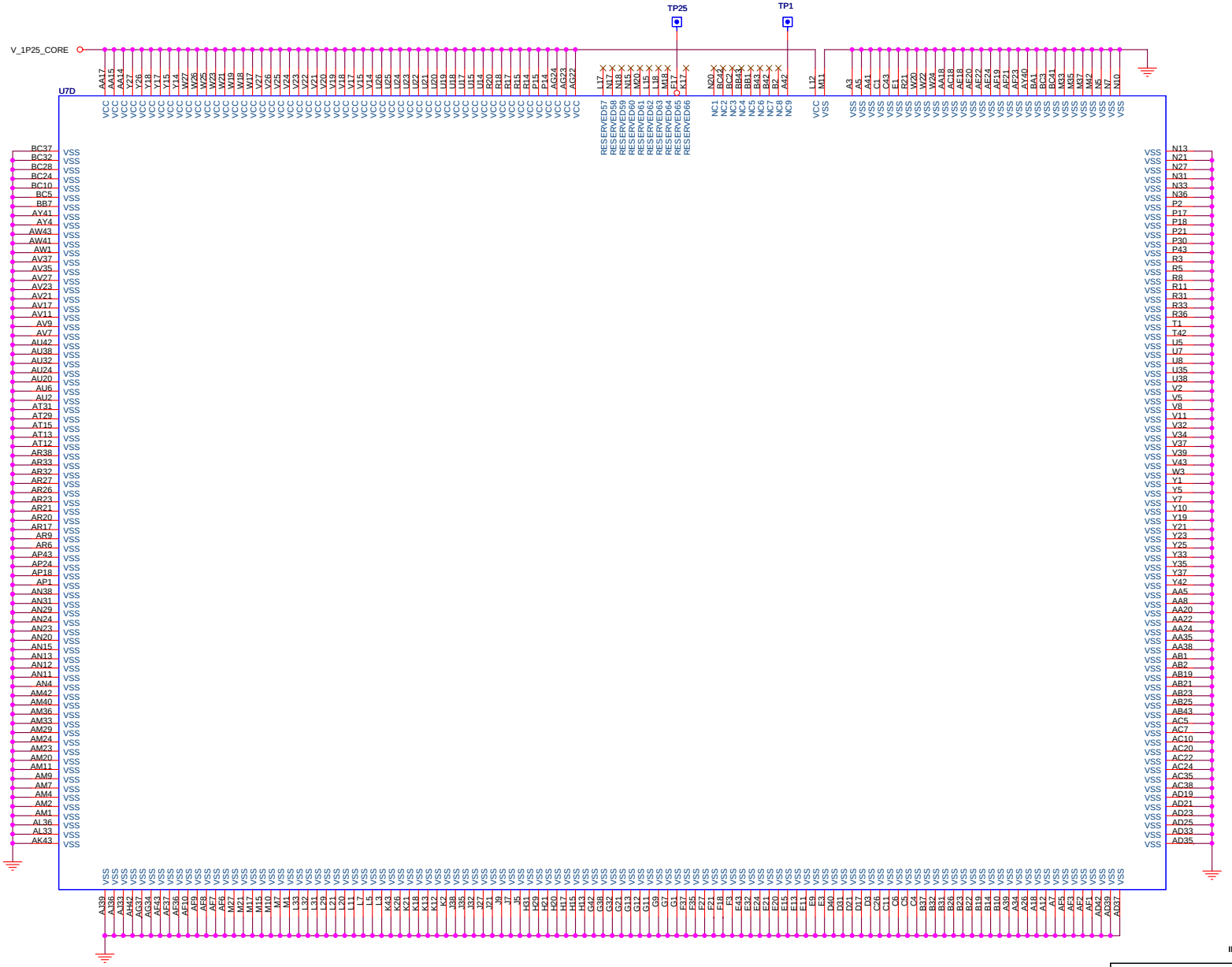
Date: Friday, May 16, 2008 | Sheet 10 of 35



Place close to GMCH

VCC_DDR

C408 C2.2U6.3Y
C409 X_C2.2U6.3Y
C410 X_C2.2U6.3Y
C411 C2.2U6.3Y
C412 C2.2U6.3Y

MCH CORE DECOUPLING

V_1P25_CORE

C401 C10U10Y0805
C400 X_C10U10Y0805
C487 C0.1U16Y0402
C390 X_C10U10Y0805
C403 C0.1U16Y0402
C406 C0.1U16Y0402
C496 X_C10U10Y0805
C513 X_C10U10Y0805
C402 C0.1U16Y0402

5020 Parts

V_1P25_CORE

C586 X_C10U10Y0805
C587 X_C10U10Y0805
C590 X_C10U10Y0805
C591 X_C10U10Y0805
C592 X_C10U10Y0805

V_FSB_VTT

C588 X_C0.1U16X-1
C589 X_C0.1U16X-1

INTEL-NR88BOBVBVA[G31]-A1-RH

MICRO-STAR INt'L CO., LTD.

Title	Intel Bearlake G31 - CPU Signals	
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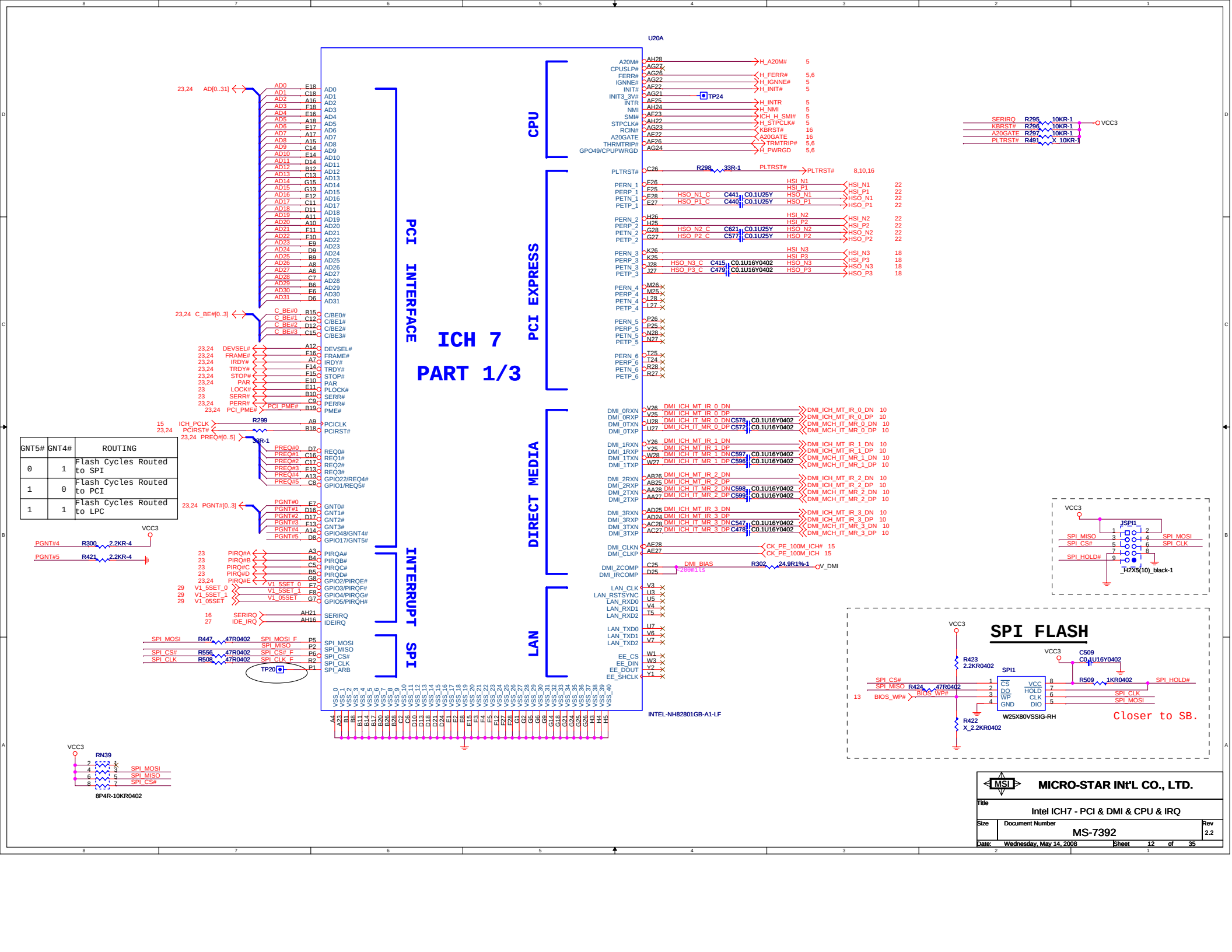
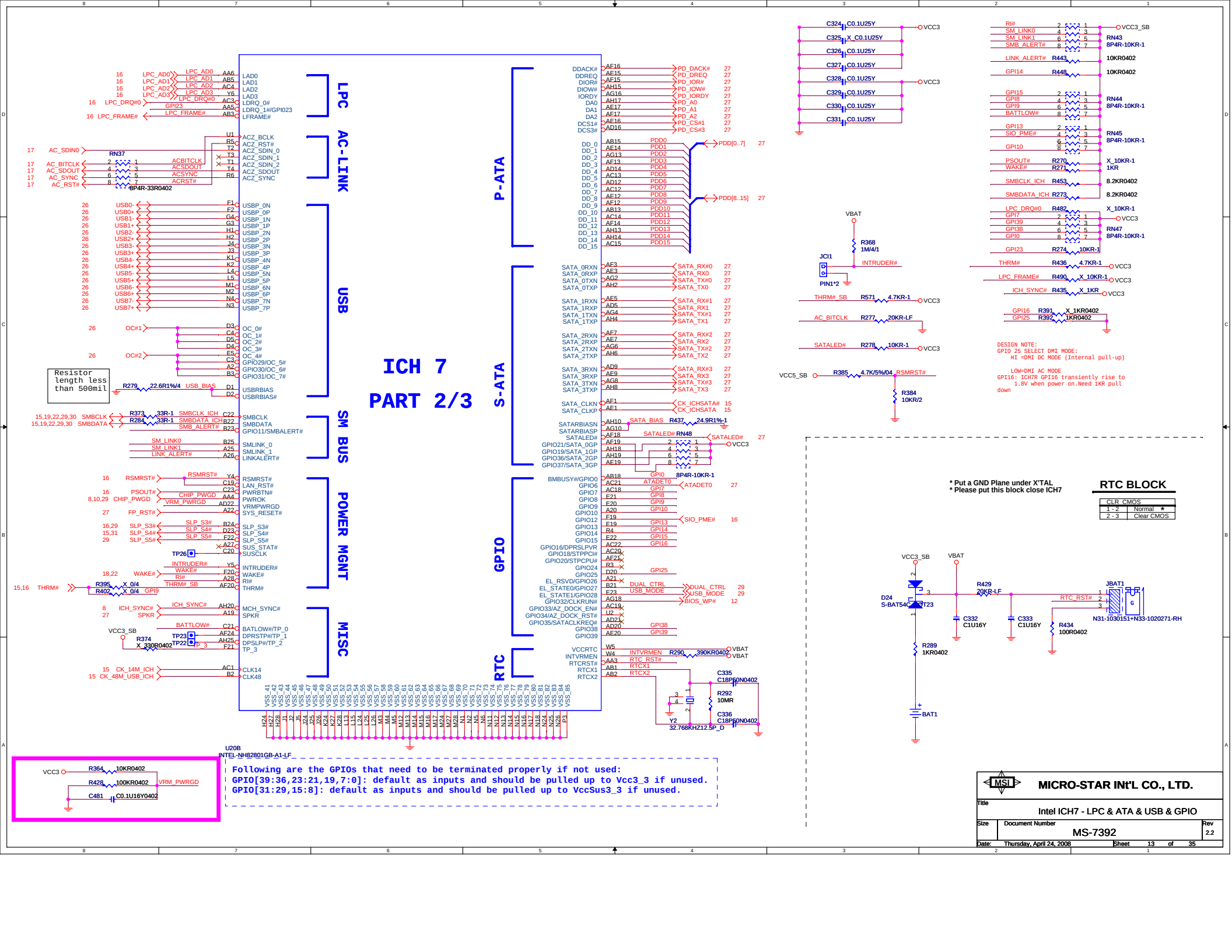


GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC


ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
Resistor length less than 500mil
U20B
INTEL-NH82801GB-A1-LF
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
* Put a GND Plane under X'TAL
* Please put this block close ICH7
RTC BLOCK
CLR_CMOS
1 - 2 Normal
2 - 3 Clear CMOS
DESIGN NOTE:
GPIO 25 SELECT DMI MODE:
HI =DMI DC MODE (Internal pull-up)
LOW=DMI AC MODE
GPI16: ICH7R GPI16 transiently rise to 1.8V when power on.Need 1KR pull down
MICRO-STAR INt'L CO., LTD.
Intel ICH7 - LPC & ATA & USB & GPIO
MS-7392
2.2
Thursday, April 24, 2008
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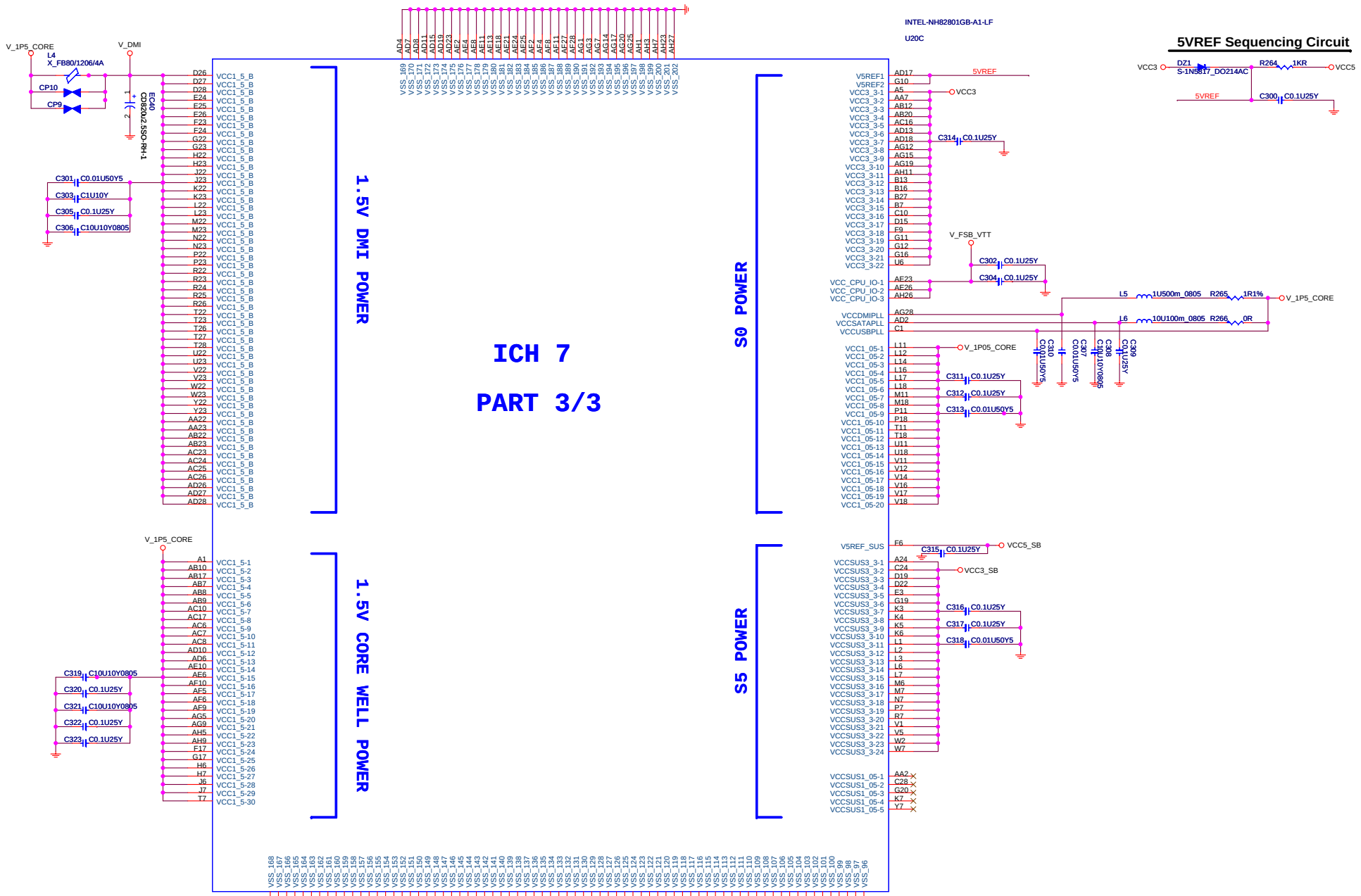

MSI	MICRO-STAR INt'L CO., LTD.
Title	Intel ICH7 - POWER
Size	Document Number: MS-7392
Rev	2.2
Date:	Friday, April 25, 2008
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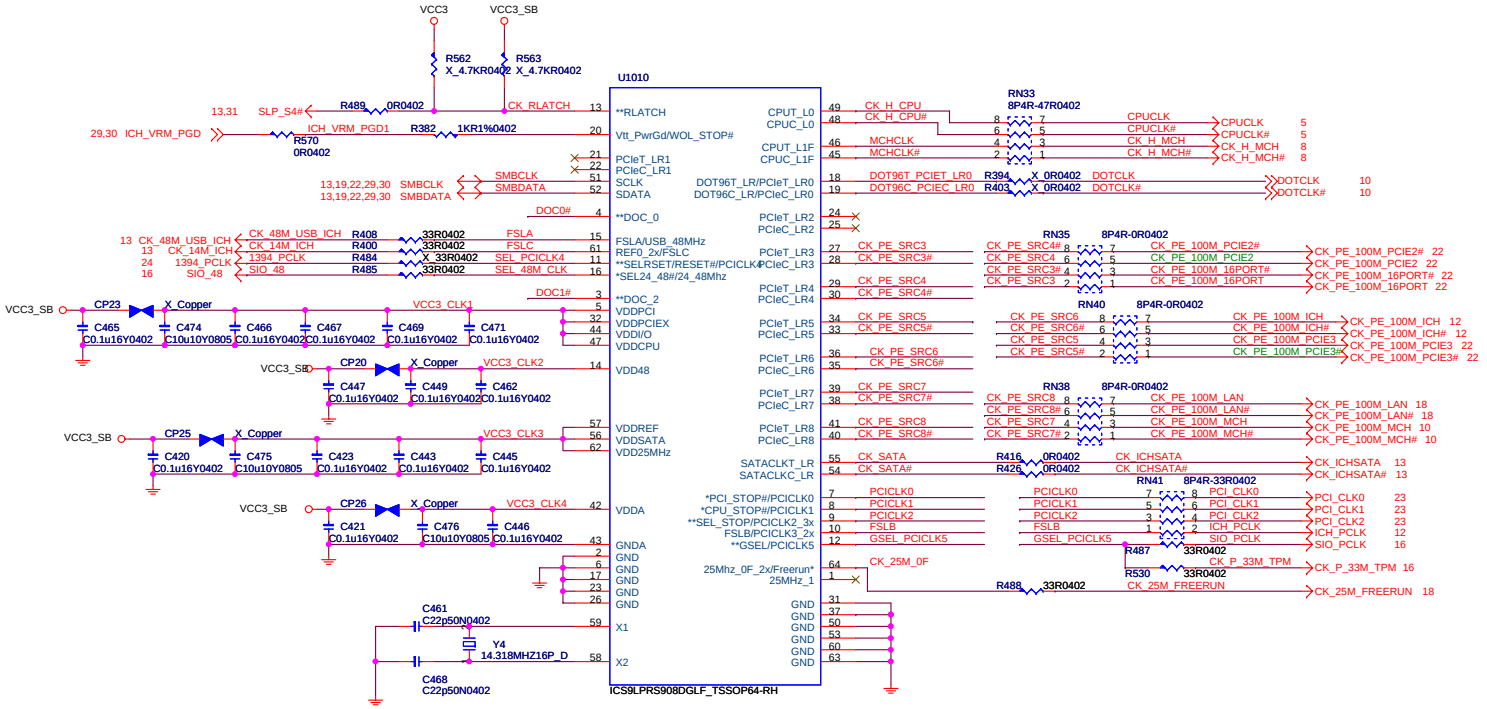
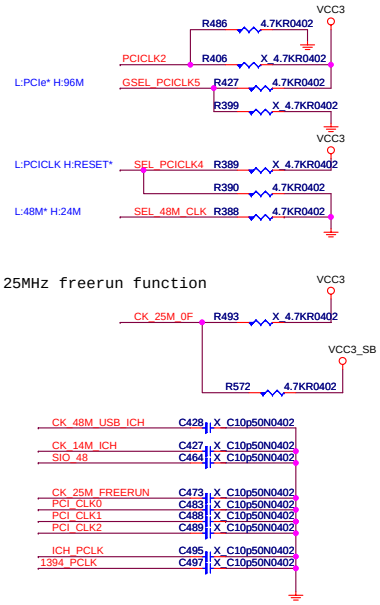
Clock Generator - ICS9LPRS906CGLF



CLOCK GEN STRAPING



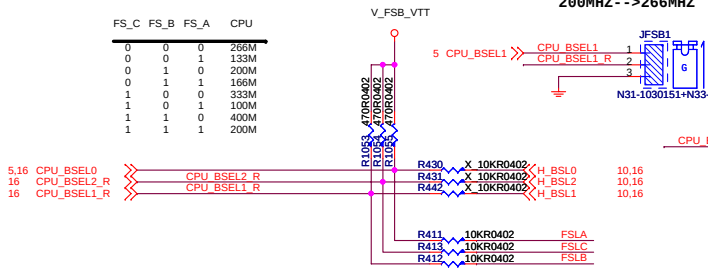
CPU Frequency Selection

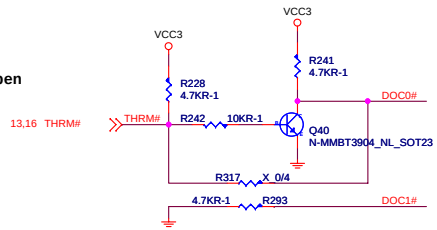
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

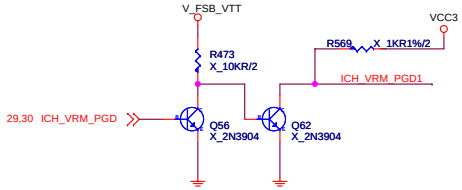
JFSB1
Plug 1--2
200MHZ-->200MHZ
Plug 2--3
200MHZ-->266MHZ

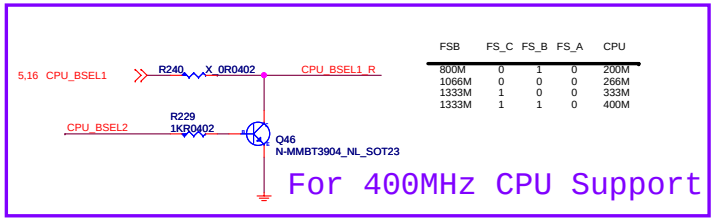
JFSB2
Plug 1--2
266MHZ-->266MHZ
Plug 2--3
266MHZ-->333MHZ

JFSB1
Open
JFSB2
Plug 1--2 or 2--3 or Open
333MHZ-->400MHZ



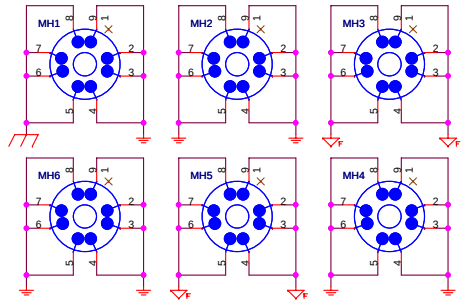




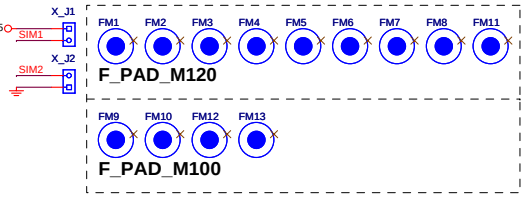


FSB	FS_C	FS_B	FS_A	CPU
800M	0	1	0	200M
1066M	0	0	0	266M
1333M	1	0	0	333M
1333M	1	1	0	400M

Mounting Holes



Optics Orientation Holes



MSI **MICRO-STAR INt'L CO., LTD.**

Title	Clock - ICS9LPRS906CGLF	
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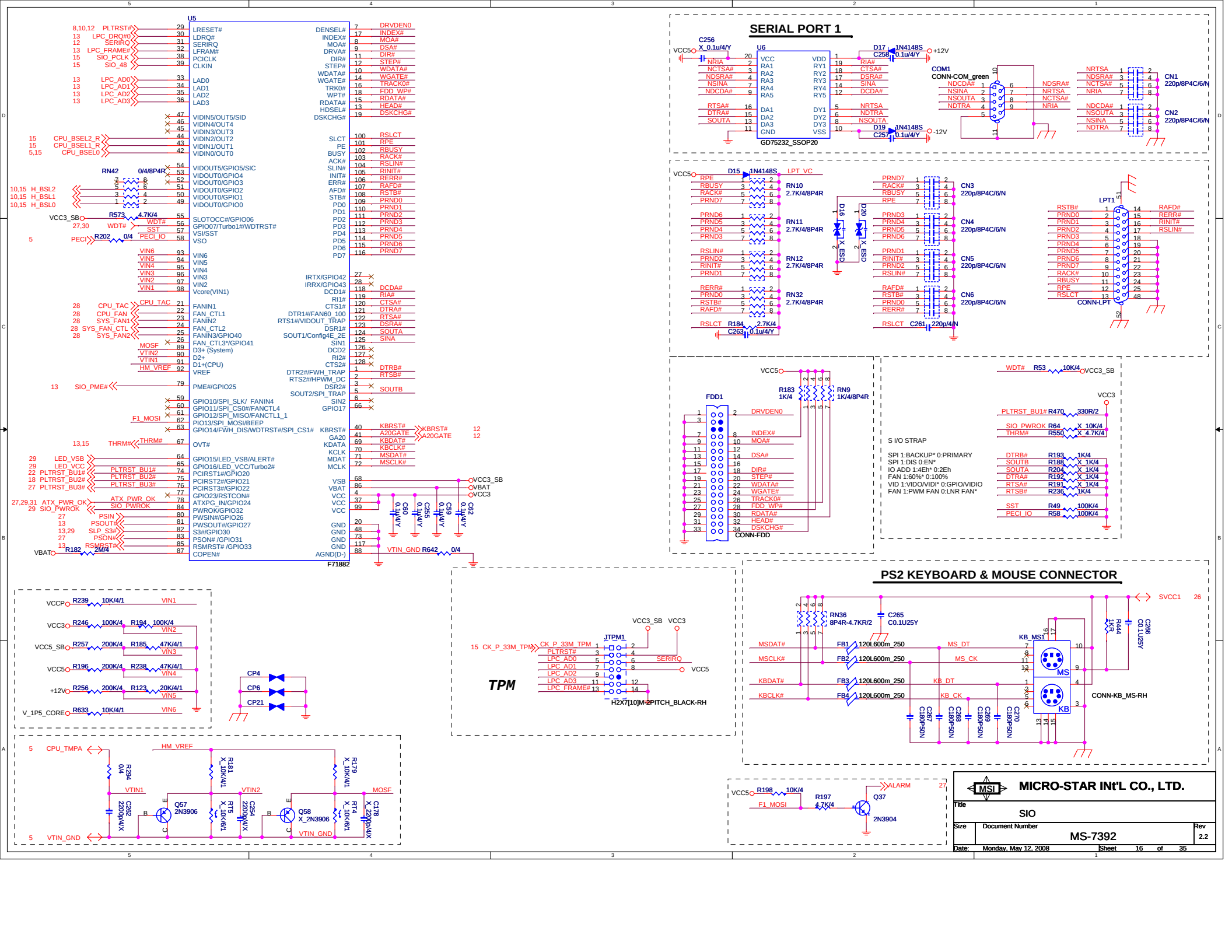
U5
F71882
SERIAL PORT 1
U6
GD75232_SSOP20
COM1
CONN-COM_green
CN1
CN2
CN3
CN4
CN5
CN6
220p/8P4C/6/N
LPT1
CONN-LPT
FDD1
CONN-FDD
S I/O STRAP
SPI 1:BACKUP* 0:PRIMARY
SPI 1:DIS 0:EN*
IO ADD 1:4Eh* 0:2Eh
FAN 1:60%* 0:100%
VID 1:VIDO/VIDI* 0:GPIO/VIDIO
FAN 1:PWM FAN 0:LNR FAN*
PS2 KEYBOARD & MOUSE CONNECTOR
CONN-KB_MS-RH
TPM
JTPM1
H2X7[10]M-2PITCH_BLACK-RH
Q57 2N3906
Q58 X_2N3906
Q37 2N3904
MICRO-STAR INt'L CO., LTD.
Title
SIO
Size
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2.2
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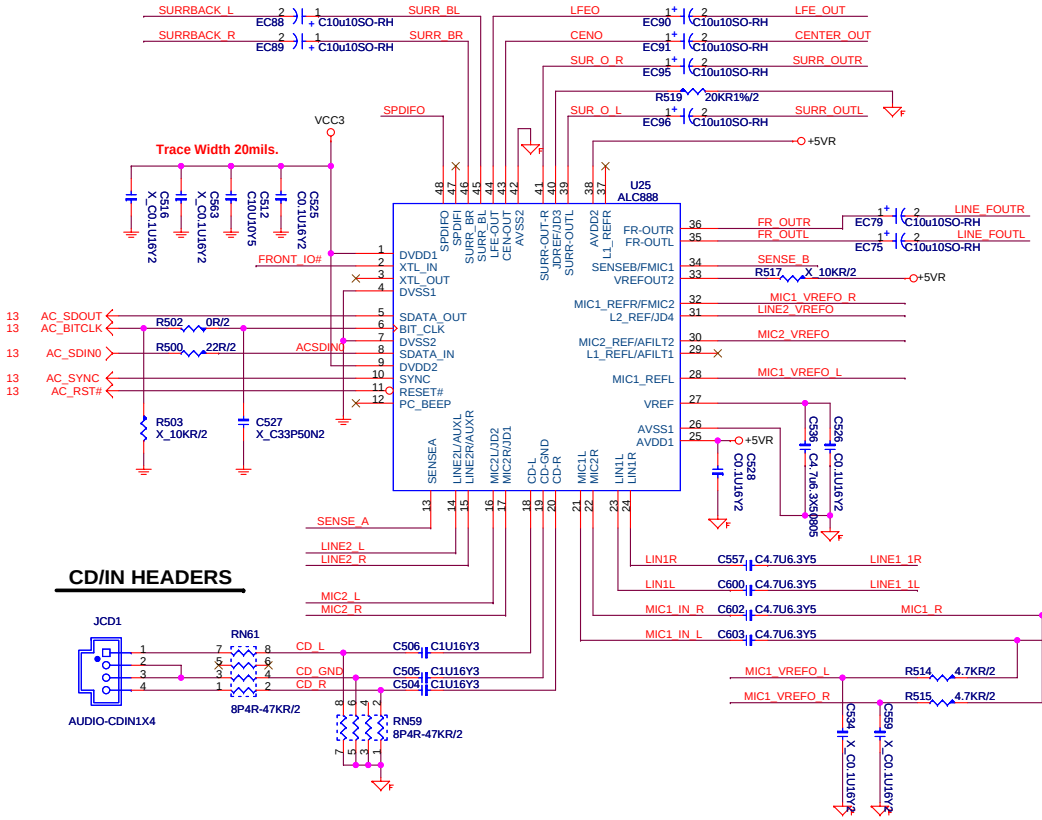
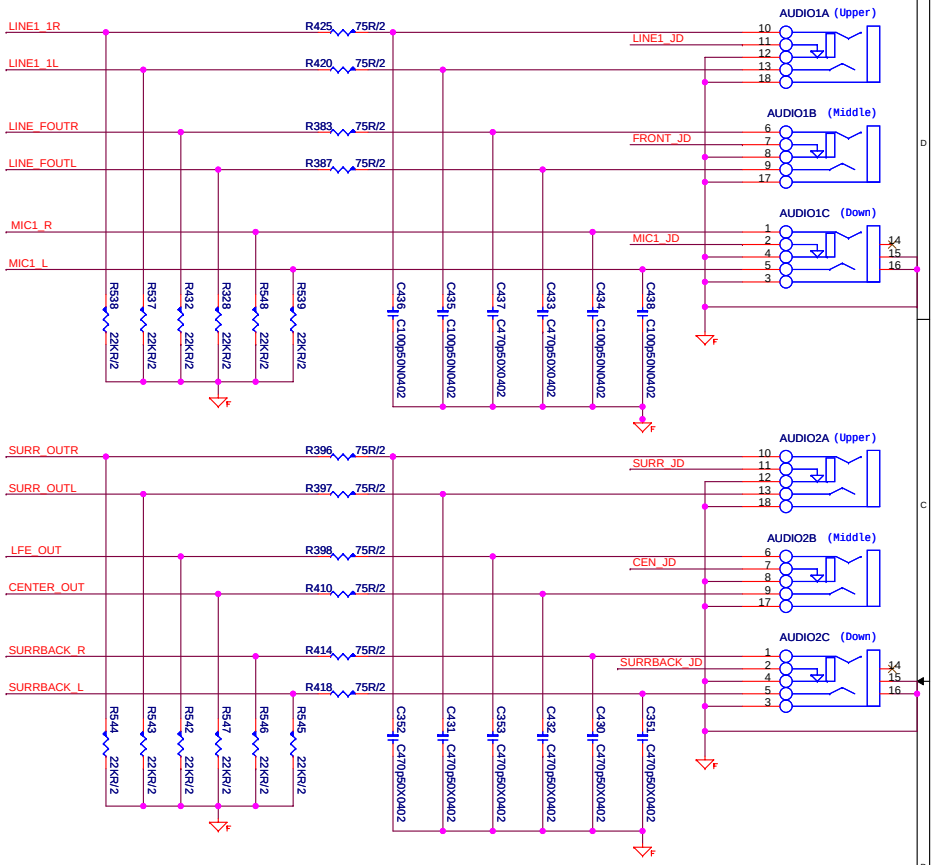
ALC888 CODEC

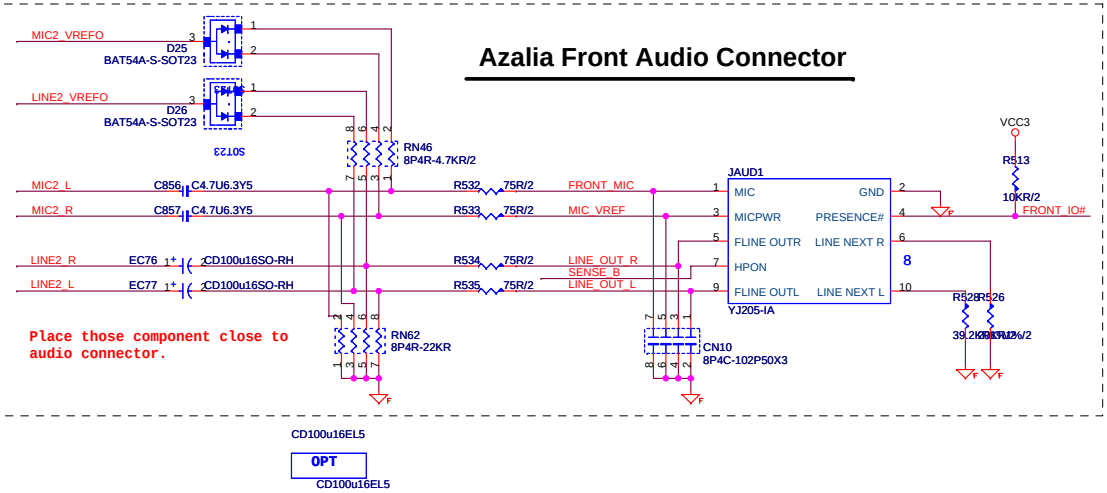


CD/IN HEADERS

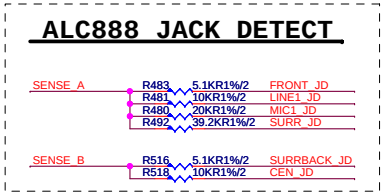
ALC888 JACK



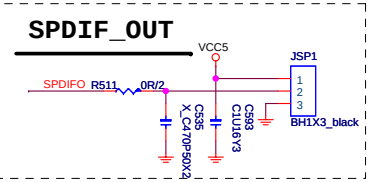
Azalia Front Audio Connector

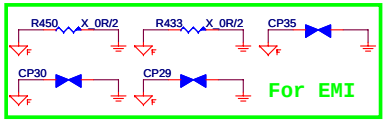


ALC888 JACK DETECT

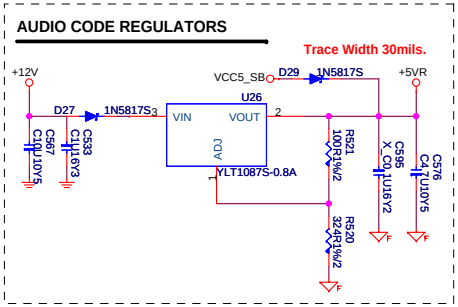


SPDIF_OUT





AUDIO CODE REGULATORS



MSI MICRO-STAR INt'L CO., LTD.

Title: LPC SUPER I/O & CONNECTORS

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R477 R205 D30 C601
C364 For 8111C only

C186,C187
For 8111B only

C224close to PIN63
C601 close to C224

RTL8111C-VBO-GR

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0201-S42
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	

Q21
For 8111B only

L30 C264
For 8111C only

R479 For 8111C only

R478 For 8111B only

Q22,C221,C299
For 8111B only

MICRO-STAR INt'L CO., LTD.

Title: LAN RTL8111C/8111B

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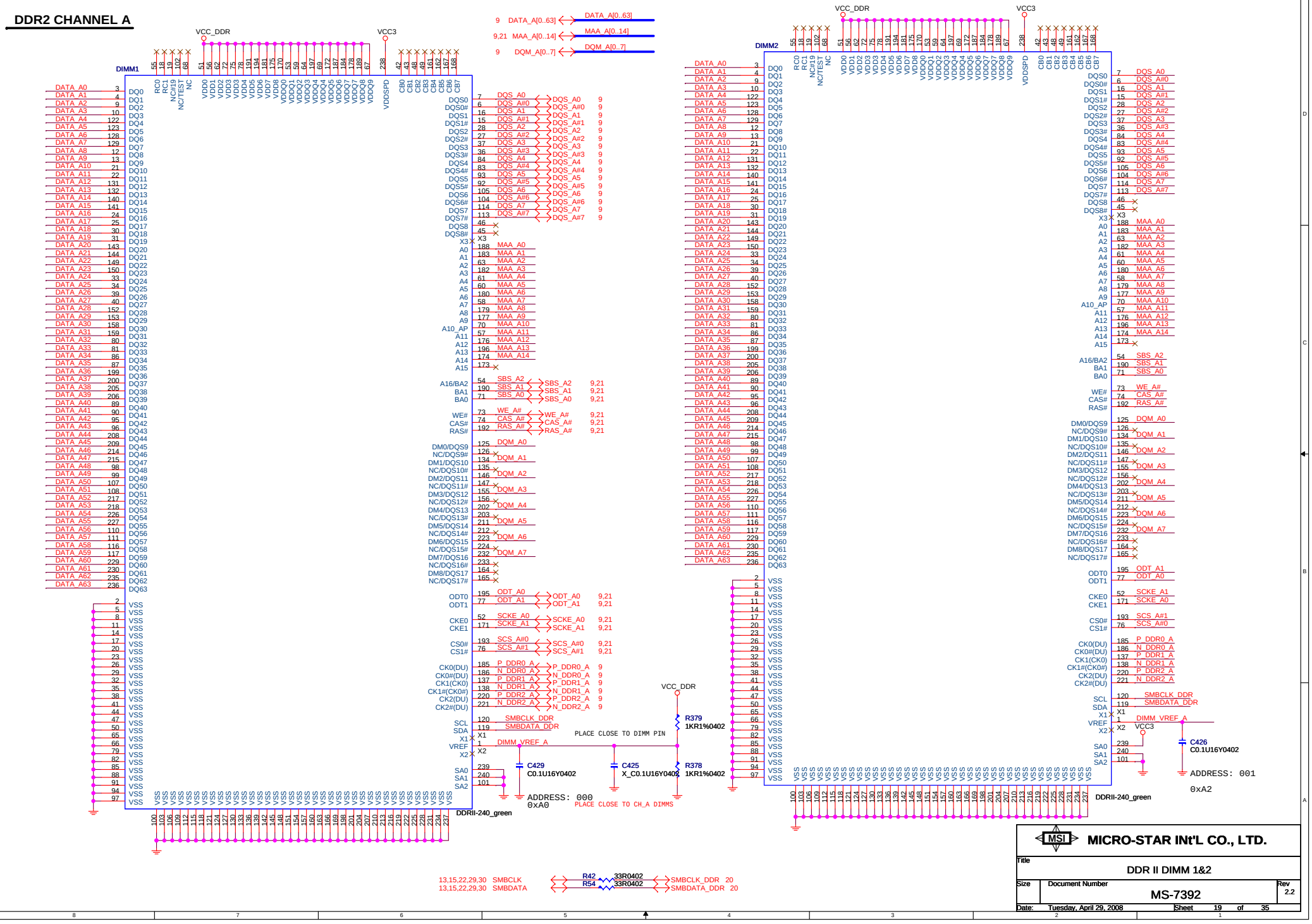
DDR2 CHANNEL A



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Title	DDR II DIMM 1&2	
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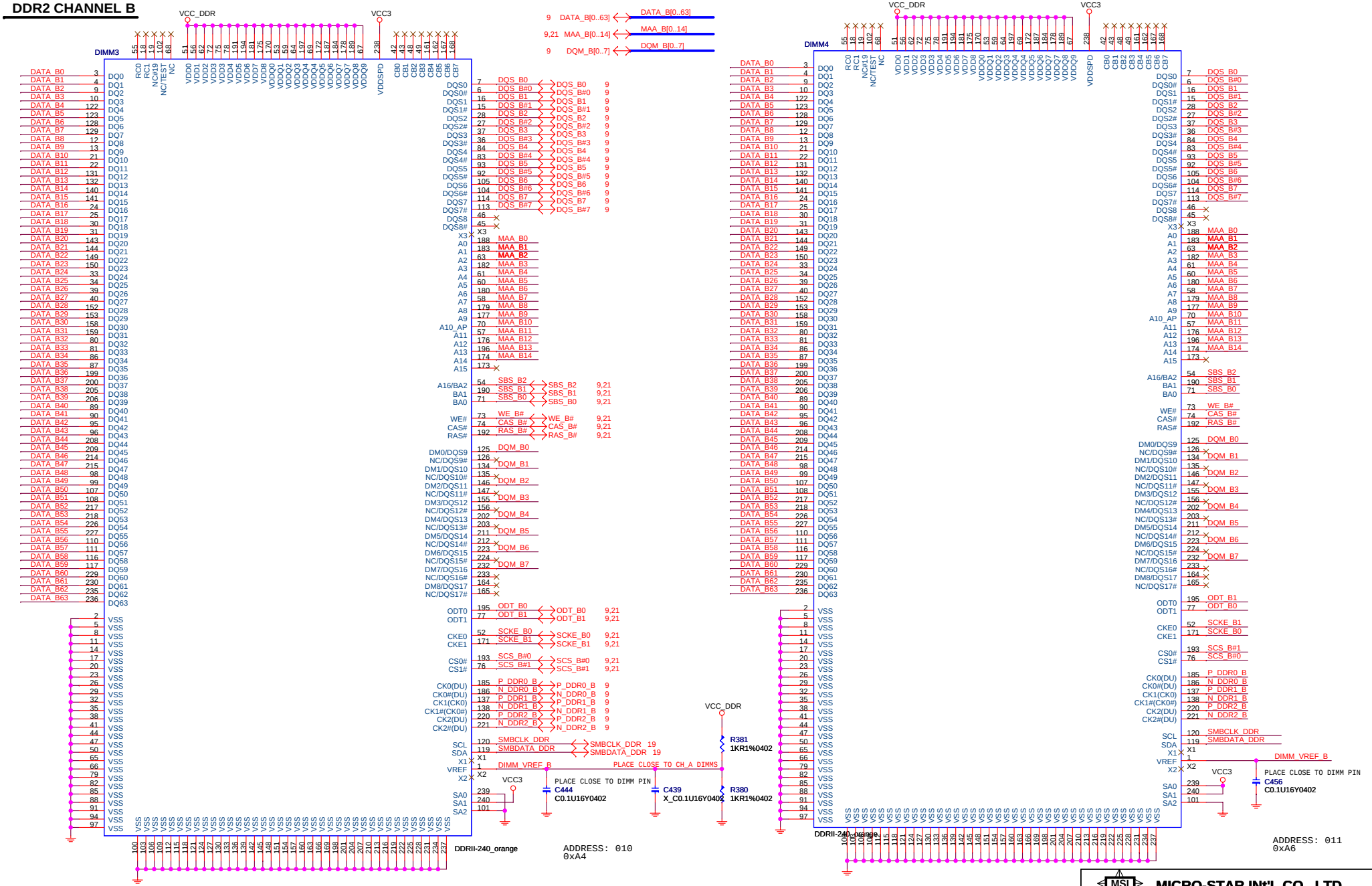
DDR2 CHANNEL B



MSI	MICRO-STAR INt'L CO., LTD.	
Title	DDR II DIMM 3&4	
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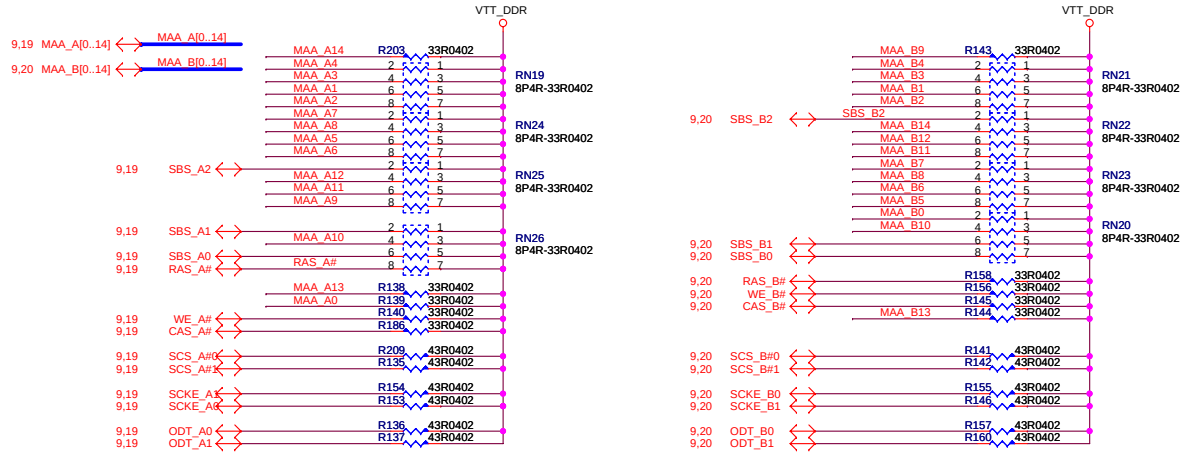
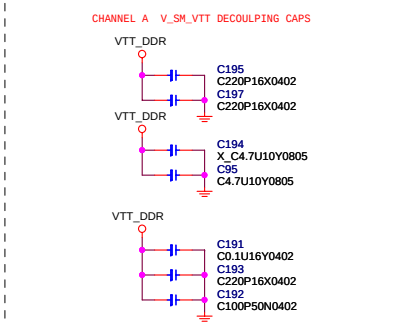
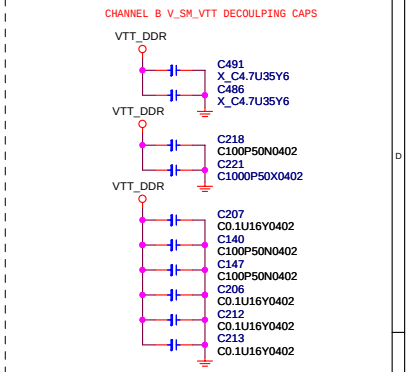
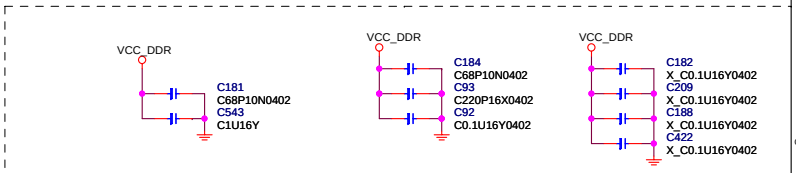
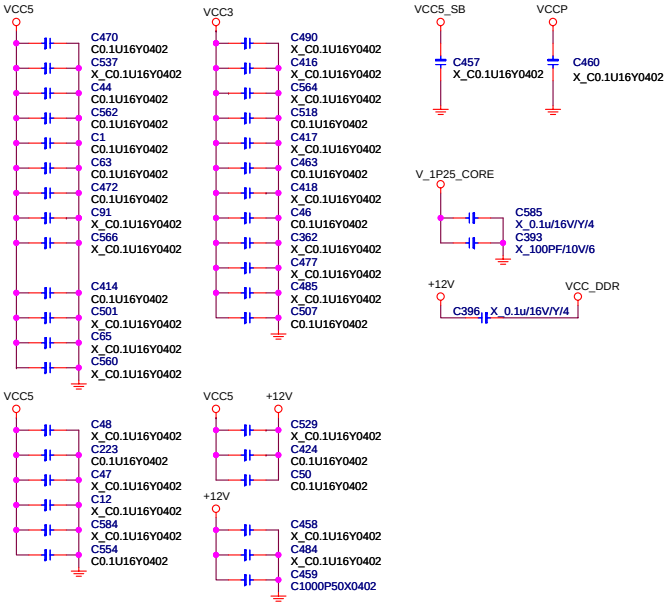


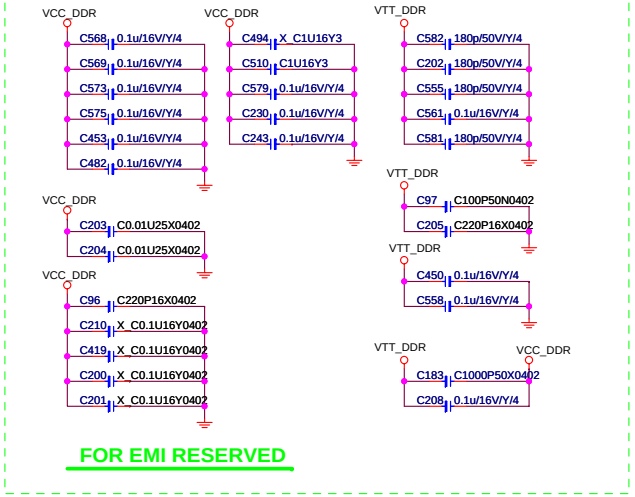






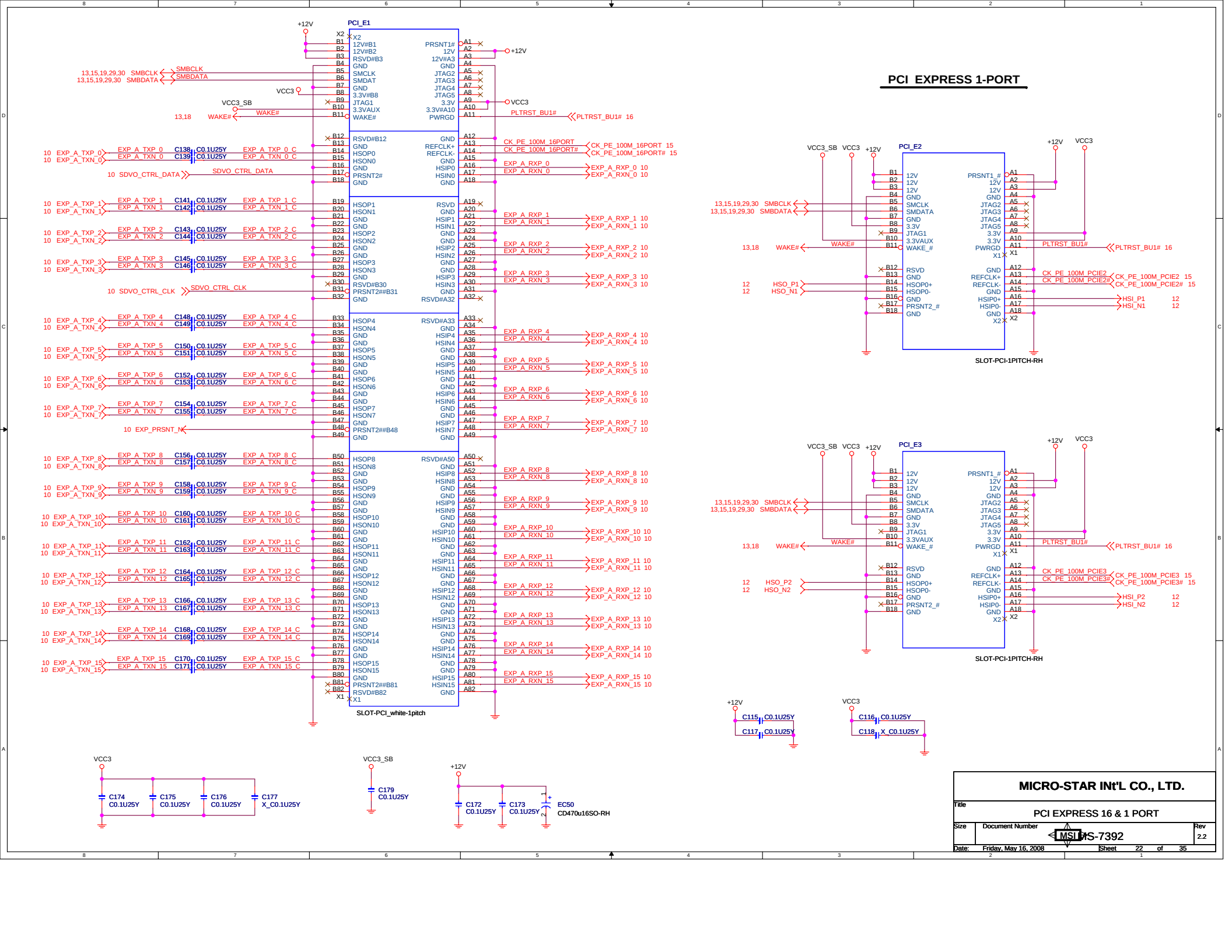
FOR EMI RESERVED





FOR EMI RESERVED

<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	DDR II VTT DECOUPLING	
Size	Document Number MS-7302	Rev 2.2
Date: Thursday, April 24, 2008	Sheet 21 of 35	


PCI EXPRESS 1-PORT
PCI_E1
SLOT-PCI_white-1pitch
PCI_E2
SLOT-PCI-1PITCH-RH
PCI_E3
SLOT-PCI-1PITCH-RH
MICRO-STAR INt'L CO., LTD.
PCI EXPRESS 16 & 1 PORT
MS-7392
Friday, May 16, 2008
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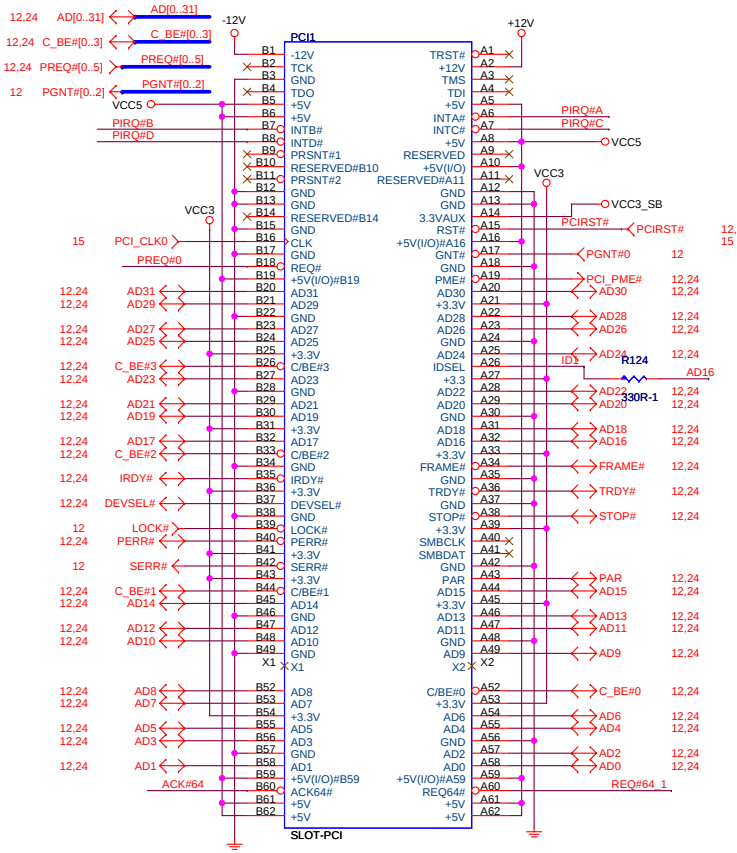
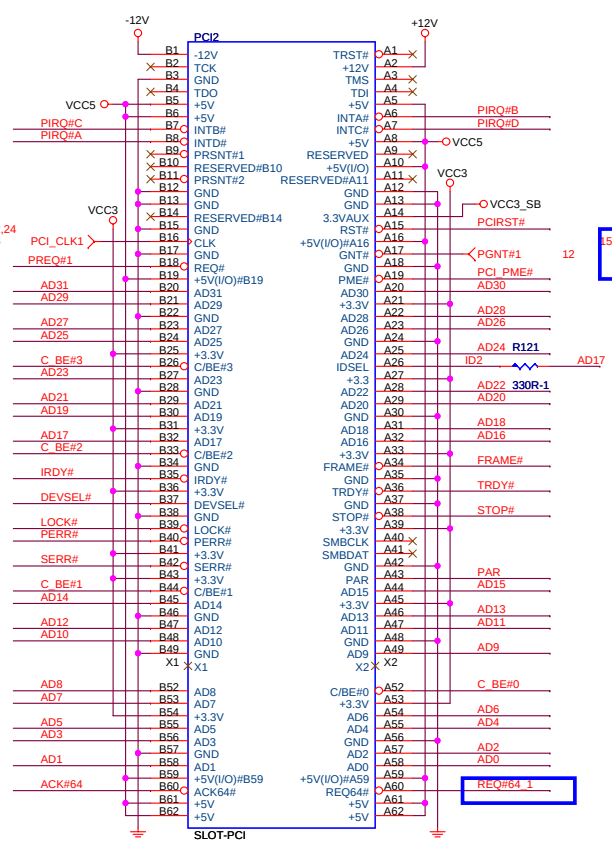
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



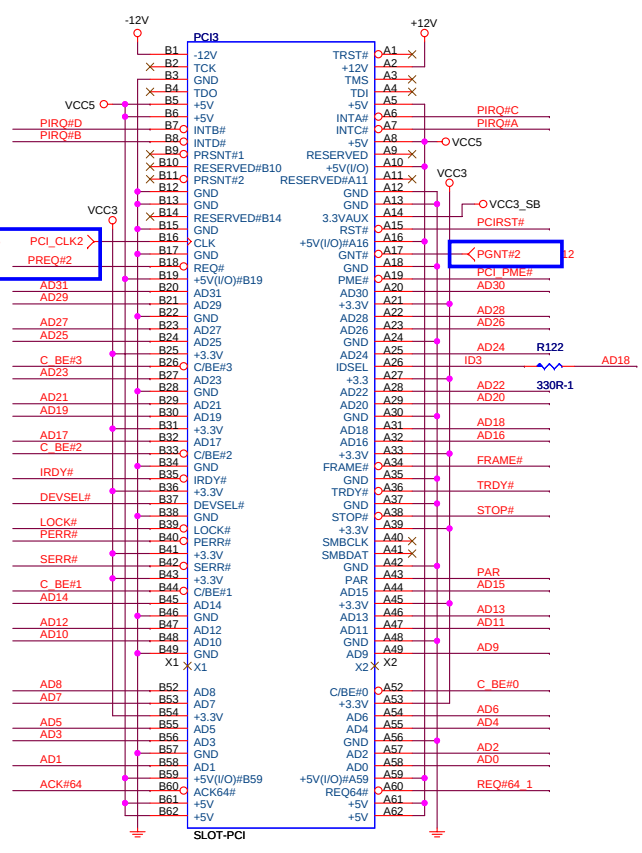
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



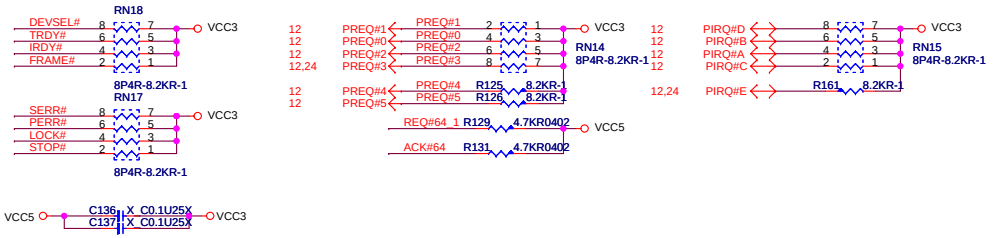
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

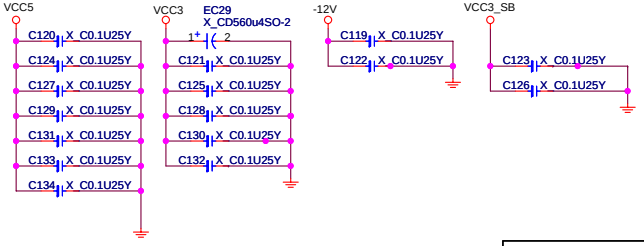
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS

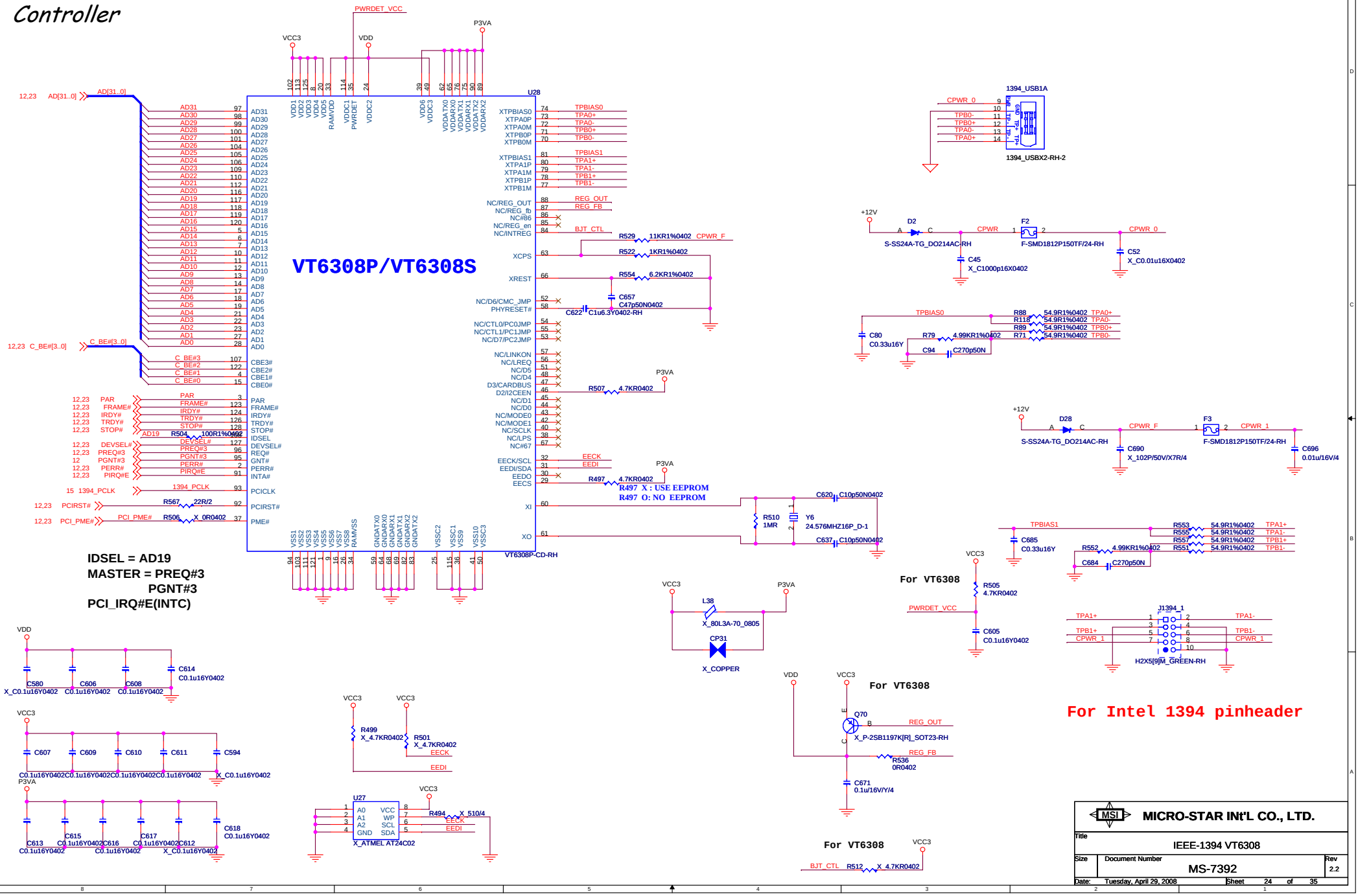




MICRO-STAR INt'L CO., LTD.

Title	PCI 1~ 4 Slots	
Size	Document Number: MS-7392	Rev: 2.2
Date: Friday, April 25, 2008	Sheet 23 of 35	

1394a OHCI Link Layer Controller



MSI	MICRO-STAR INt'L CO., LTD.
Title	IEEE-1394 VT6308
Size	Document Number: MS-7392
Rev	2.2
Date:	Tuesday, April 29, 2008
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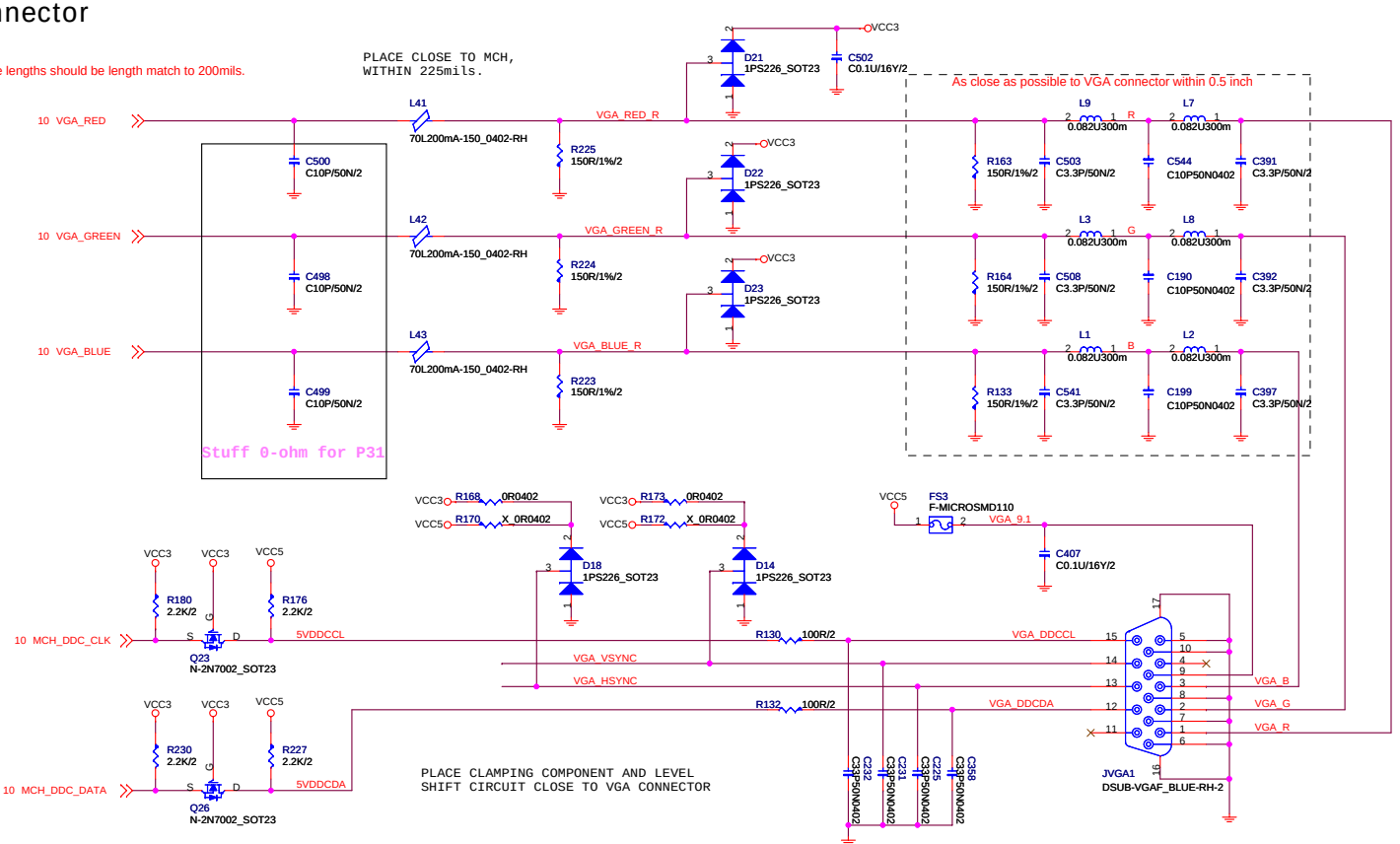
Video Connector

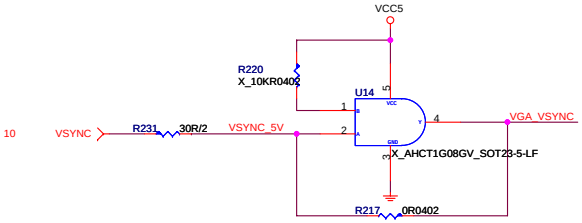
Thw R ,G ,B route lengths should be length match to 200mils.

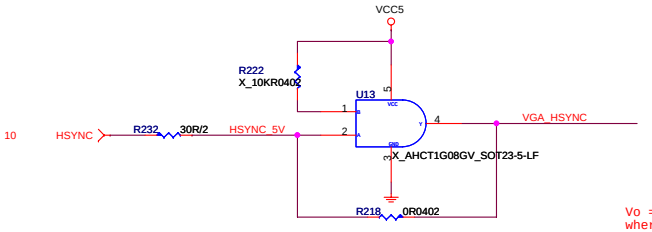
PLACE CLOSE TO VGA CONNECTOR

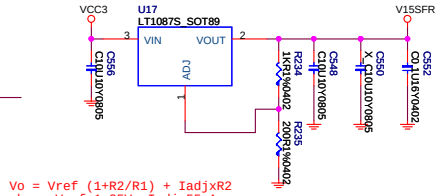
PLACE CLOSE TO MCH, WITHIN 225mils.

As close as possible to VGA connector within 0.5 inch



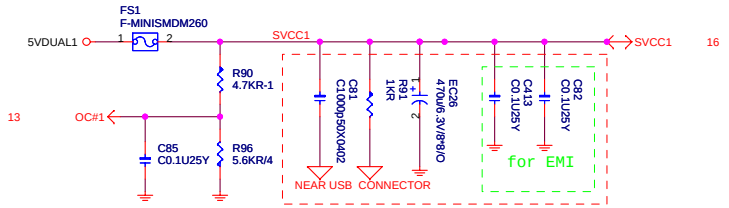




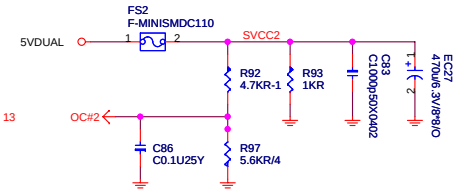


MSI	MICRO-STAR INt'L CO., LTD.	
Title	ATA33/66/100 IDE & SATA Connectors	
Size	Document Number MS-7392	Rev 2.2
Date: Thursday, April 24, 2008	Sheet 25 of 35	

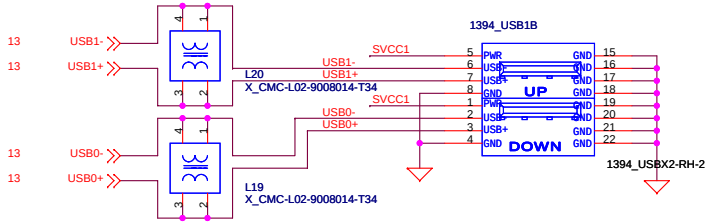
POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



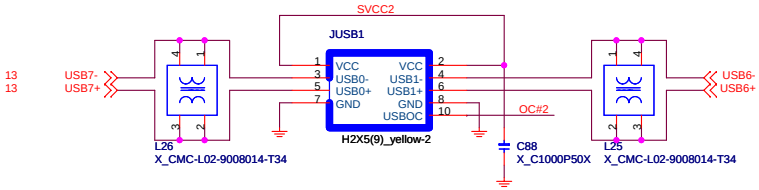
POWER CIRCUIT FOR USB PORT (FRONT)



REAR PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

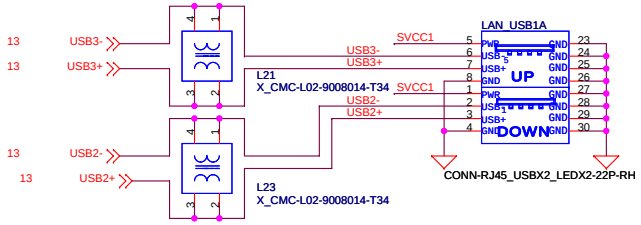


CD470U10EL11.5

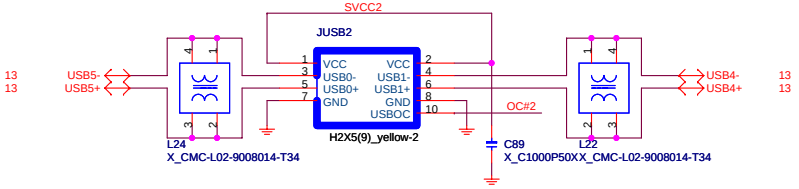
0PT

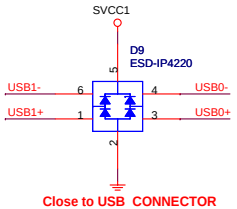
CD470U10EL11.5

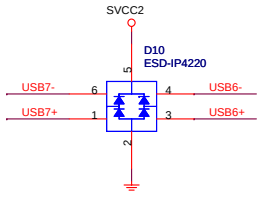
REAR PANEL USB CONNECTOR FOR USB PORT 2,3

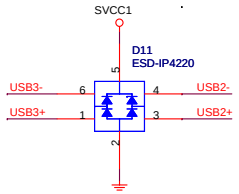


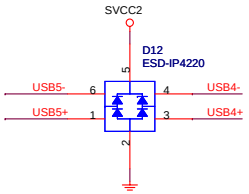
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

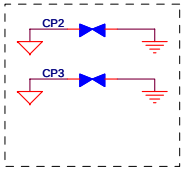












MICRO-STAR INt'L CO., LTD.		
Title: USB Connectors		
Size	Document Number: MS-7392	Rev: 2.2
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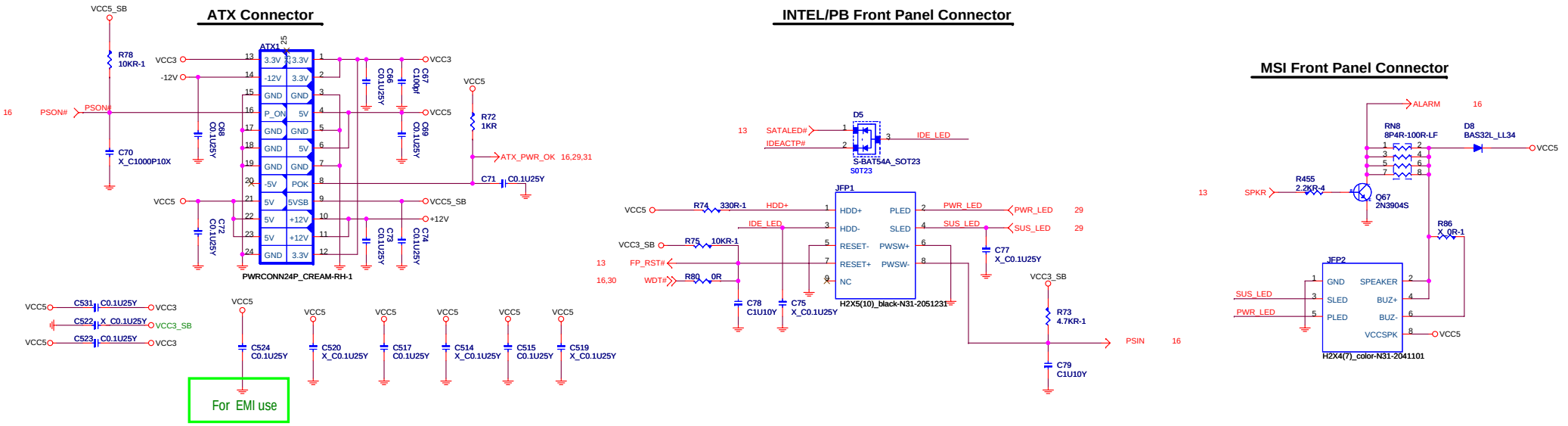
ATX Connector
VCC5_SB
R78
10KR-1
VCC3
-12V
ATX1
PWRCONN24P_CREAM-RH-1
PSON#
C70
X_C1000P10X
C68
C0.1U25Y
C72
C0.1U25Y
C56
C0.1U25Y
C67
C100pf
C69
C0.1U25Y
C73
C0.1U25Y
C74
C0.1U25Y
R72
1KR
ATX_PWR_OK
C71
C0.1U25Y
VCC5_SB
+12V
C531
C0.1U25Y
C522
X_C0.1U25Y
C523
C0.1U25Y
VCC3_SB
C524
C0.1U25Y
C520
X_C0.1U25Y
C517
C0.1U25Y
C514
X_C0.1U25Y
C515
C0.1U25Y
C519
X_C0.1U25Y
For EMI use
INTEL/PB Front Panel Connector
SATALED#
IDEACTP#
D5
S-BAT54A_SOT23
IDE_LED
JFP1
H2X5(10)_black-N31-2051231
HDD+
HDD-
RESET-
RESET+
NC
PLED
SLED
PWSW+
PWSW-
R74
330R-1
R75
10KR-1
R80
0R
FP_RST#
WDT#
PWR_LED
SUS_LED
C77
X_C0.1U25Y
C78
C1U10Y
C75
X_C0.1U25Y
R73
4.7KR-1
PSIN
C79
C1U10Y
MSI Front Panel Connector
ALARM
RN8
8P4R-100R-LF
D8
BAS32L_LL34
SPKR
R455
2.2KR-4
Q67
2N3904S
R86
X_0R-1
JFP2
H2X4(7)_color-N31-2041101
GND
SPEAKER
SLED
BUZ+
PLED
BUZ-
VCCSPK
SUS_LED
PWR_LED
ATA 33/66/100 IDE Connectors
PDD[0..7]
PDD[8..15]
HDRST#
R113
33R-1
IDE1
CONN-IDE(20)V_blue
PD_DREQ
PD_IOW#
PD_IOR#
PD_IORDY
PD_DACK#
IDE_IRQ
PD_A1
PD_A0
PD_CS#1
IDEACTP#
ATADET0
PD_A2
PD_CS#3
20K/4/1
R114
10KR-1
R115
4.7KR-1
R116
C106
X_C4700p25X2
R117
10KR-1
R95
4.7KR-1
R98
4.7KR-1
R94
4.7KR-1
PLTRST_BU3#
Q69
2N3904S
Q71
2N3904S
SERIAL ATA CONNECTOR BLOCK
SATA1
SATA2
SATA3
SATA4
SATA7P_PURPLE-P-RH
SATA_RX0
SATA_RX#0
SATA_TX#0
SATA_TX0
SATA_RX1
SATA_RX#1
SATA_TX#1
SATA_TX1
SATA_RX2
SATA_RX#2
SATA_TX#2
SATA_TX2
SATA_RX3
SATA_RX#3
SATA_TX#3
SATA_TX3
MICRO-STAR INt'L CO., LTD.
Title
ATX Connector & Front Panel
Size
Document Number
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Date: Wednesday, April 30, 2008
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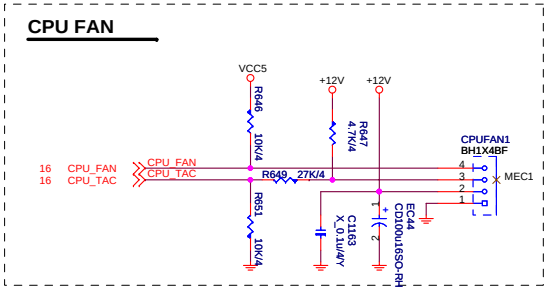
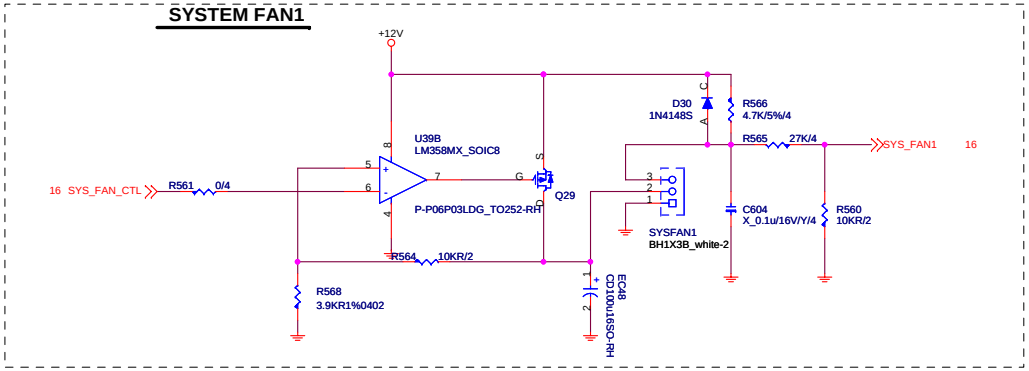
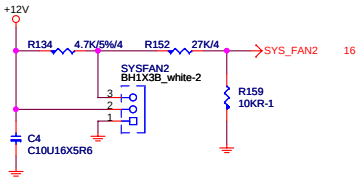
CPU FAN



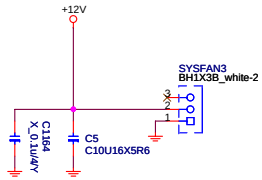
SYSTEM FAN1



SYSTEM FAN2

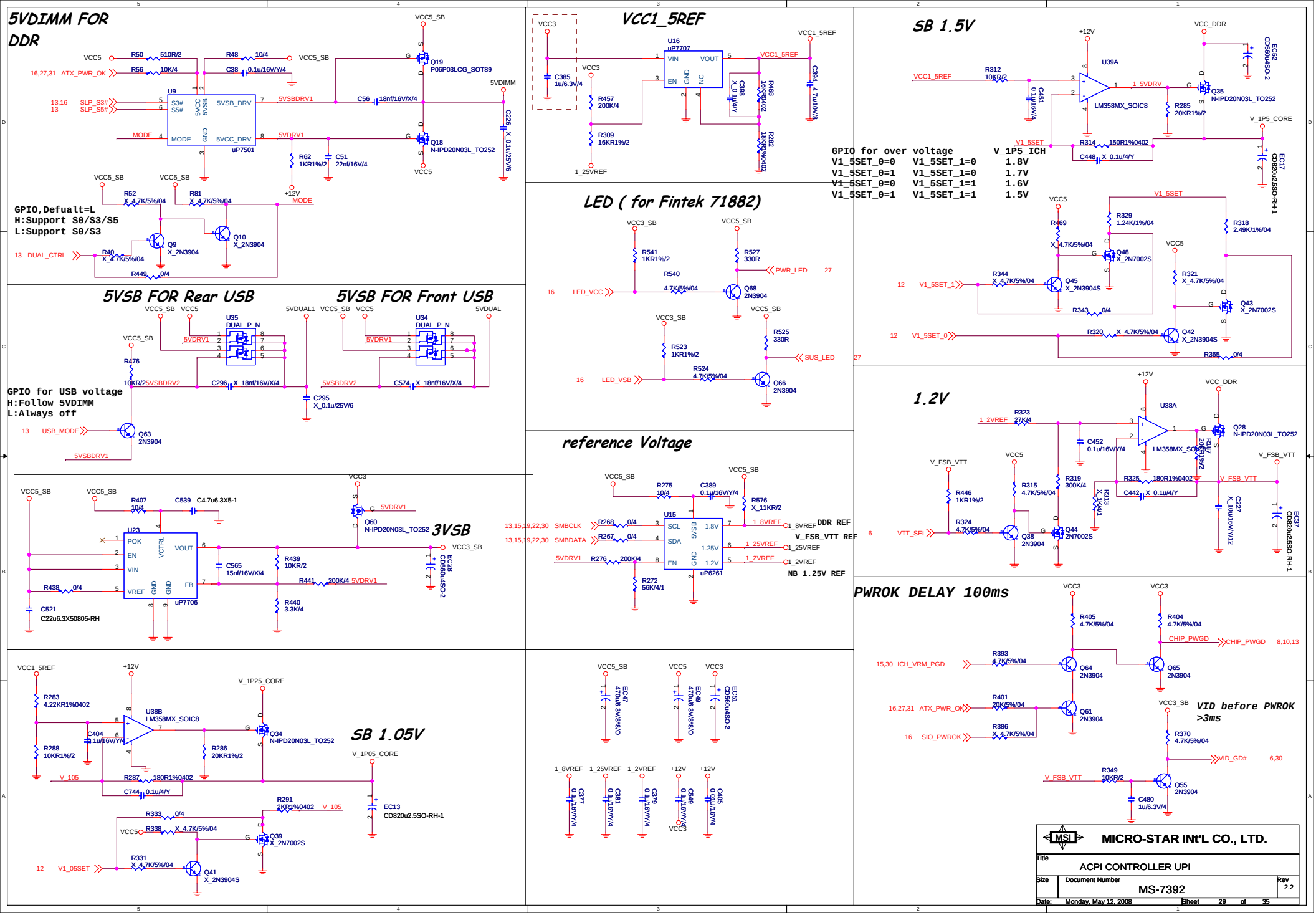


SYSTEM FAN3



MSI **MICRO-STAR INt'L CO., LTD.**

Title	FWH & LPC Debug Port	
Size	Document Number MS-7392	Rev 2.2
Date: Friday, April 25, 2008	Sheet 28 of 35	


5VDIMM FOR DDR
GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3
5VSB FOR Rear USB
5VSB FOR Front USB
GPIO for USB voltage
H:Follow 5VDIMM
L:Always off
3VSB
VCC1_5REF
LED (for Fintek 71882)
reference Voltage
DDR REF
V_FSB_VTT REF
NB 1.25V REF
SB 1.5V
GPIO for over voltage V_1P5_ICH
V1_5SET_0=0 V1_5SET_1=0 1.8V
V1_5SET_0=1 V1_5SET_1=0 1.7V
V1_5SET_0=0 V1_5SET_1=1 1.6V
V1_5SET_0=1 V1_5SET_1=1 1.5V
1.2V
PWROK DELAY 100ms
VID before PWROK >3ms
SB 1.05V
MICRO-STAR INT'L CO., LTD.
ACPI CONTROLLER UPI
MS-7392
Monday, May 12, 2008
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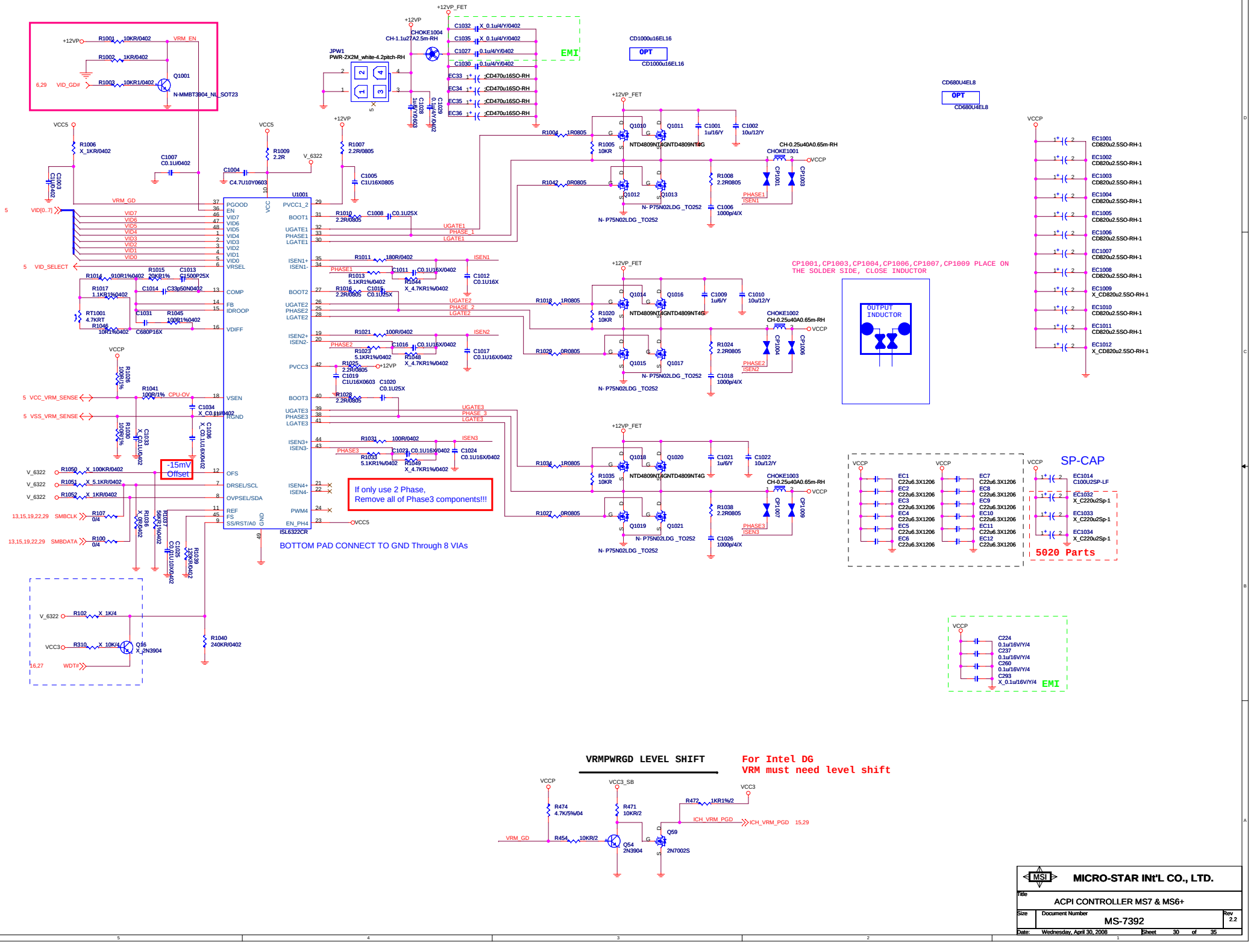
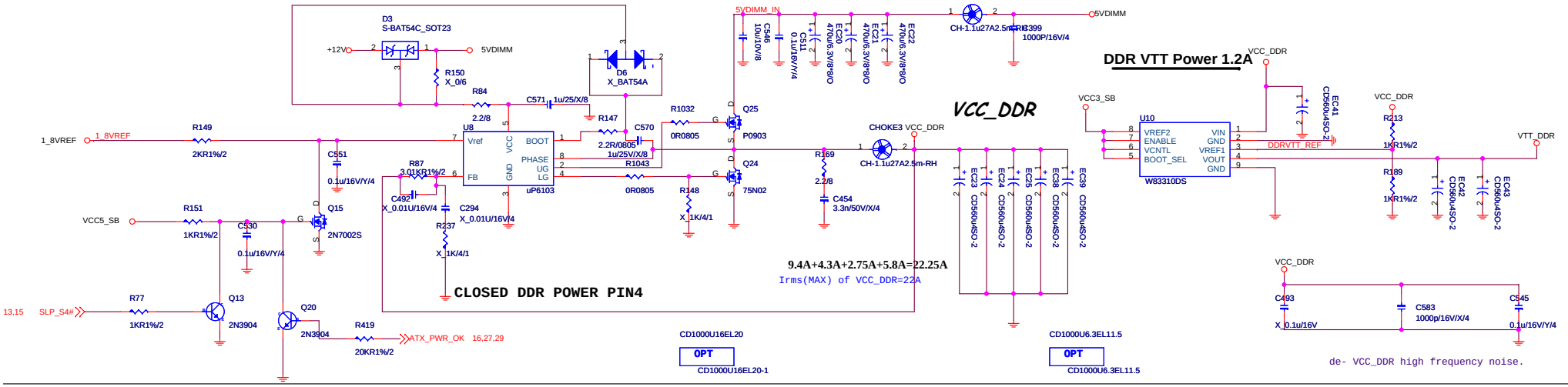

VRM_EN
Q1001
N-MMBT3904_NL_SOT23
6,29 VID_GD#
+12VP
+12VP_FET
CHOKE1004
CH-1.1u27A2.5m-RH
JPW1
PWR-2X2M_white-4.2pitch-RH
EMI
CD1000u16EL16
OPT
CD680U4EL8
U1001
ISL6322CR
PGOOD
EN
VID7
VID6
VID5
VID4
VID3
VID2
VID1
VID0
VRSEL
VID[0..7]
VID_SELECT
VRM_GD
PVCC1_2
BOOT1
UGATE1
PHASE1
LGATE1
ISEN1+
ISEN1-
BOOT2
UGATE2
PHASE2
LGATE2
ISEN2+
ISEN2-
PVCC3
BOOT3
UGATE3
PHASE3
LGATE3
ISEN3+
ISEN3-
ISEN4+
ISEN4-
PWM4
EN_PH4
COMP
FB
IDROOP
VDIFF
VSEN
RGND
OFS
DRSEL/SCL
OVPSEL/SDA
REF
FS
SS/RST/A0
GND
VCC
VCC_VRM_SENSE
VSS_VRM_SENSE
CPU-OV
-15mV Offset
SMBCLK
SMBDATA
WDT#
Q16 X_2N3904
Q1010 Q1011 Q1012 Q1013
Q1014 Q1016 Q1015 Q1017
Q1018 Q1020 Q1019 Q1021
NTD4809NT4G
N- P75N02LDG _TO252
CHOKE1001 CH-0.25u40A0.65m-RH
CHOKE1002 CH-0.25u40A0.65m-RH
CHOKE1003 CH-0.25u40A0.65m-RH
CP1001 CP1003 CP1004 CP1006 CP1007 CP1009
PHASE1 ISEN1
PHASE2 ISEN2
PHASE3 ISEN3
CP1001,CP1003,CP1004,CP1006,CP1007,CP1009 PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR
OUTPUT INDUCTOR
If only use 2 Phase,
Remove all of Phase3 components!!!
BOTTOM PAD CONNECT TO GND Through 8 VIAs
SP-CAP
5020 Parts
VRMPWRGD LEVEL SHIFT
For Intel DG
VRM must need level shift
VCC3_SB
VCC3
ICH_VRM_PGD 15,29
MICRO-STAR INt'L CO., LTD.
ACPI CONTROLLER MS7 & MS6+
MS-7392
Rev 2.2
Wednesday, April 30, 2008
Sheet 30 of 35

DDR II 1.8V POWER

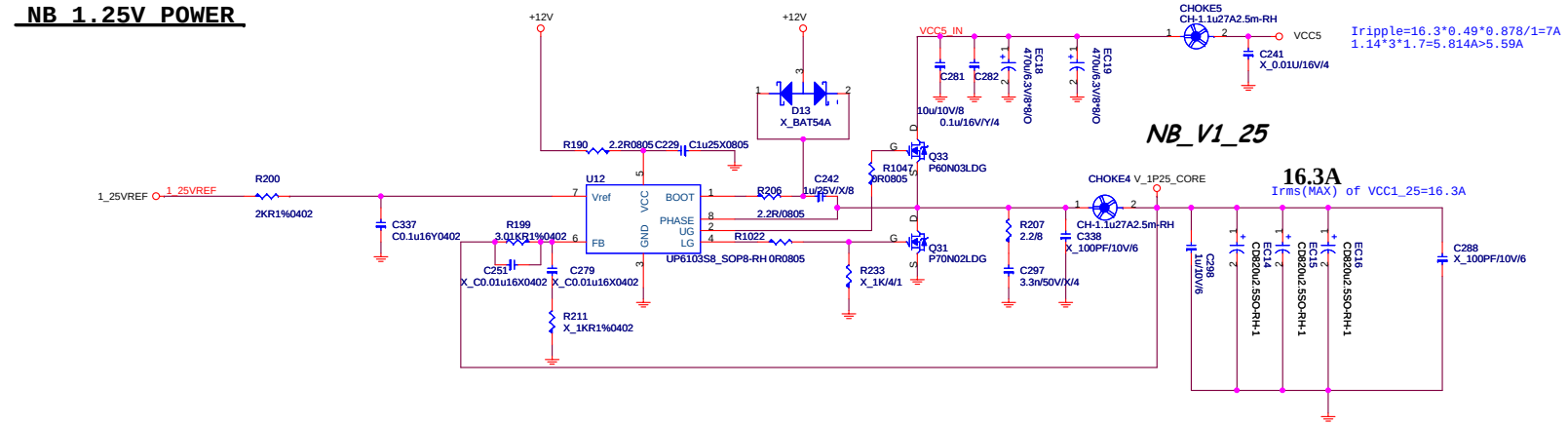
Iripple=21*0.6*0.8/1=10.08A
2.22*3*1.7=11.322A>10.08A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



NB 1.25V POWER

Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A



MSI	MICRO-STAR INt'L CO., LTD.	
Title	GMCH VCORE	
Size	Document Number MS-7392	Rev 2.2
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Auto-BOM Manual Parts

PCB1
PCB
PCB-7392

BATTERY1
BATTERY-CR2032

Auto-BOM Option Parts

RTL8111B
OPT
X_RTL8111B

ICH7
OPT
X_ICH7

G31
OPT
X_G31

P31-R1
OPT
X_0R0402

OnVGA1.3
OPT
X_1.3KR1%/2

G31-C1
OPT
X_C0.1U16Y0402

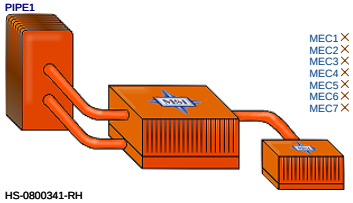
USB
OPT
X_USB

P31 HEATSINK ICH7 HEATSINK

HT_U7
OPT
P31 HEATSINK

HT_U20
OPT
ICH7 HEATSINK

PIPE1



MEC1 MEC1
MEC2 MEC2
MEC3 MEC3
MEC4 MEC4
MEC5 MEC5
MEC6 MEC6
MEC7 MEC7

HS-0800341-RH

MSI	MICRO-STAR INt'L CO., LTD.	
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2.0 Change 2.1list:

1. Power team change :
   Remove EC1009、EC1012、R1050;R1037=56K1%; RT1001=4.7K; R1046=10R1%
   R1017=1.1K1%; R1014=910R1%; C1031=680p; R1045=100R; C1014=33p。(page 30)
2. Add CK_25M_0F Pullup to VCC3_SB.(Page 15)
3. Add a test point for ICH SUSCLK signal
4. Add IDE reset for lever shift
5. Change CHOCK to new footprint for PM request;
6. Audio : Realtek power solution, D27 1N5817 from U26 Vout move to Vin

2.1 Change 2.2 List:

1. 增加F71882 SLOTOCC#通過4.7K上拉3VSB
2. 增加OC Jump , Page15
3. 修改C521和C539的容值

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ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	PIRQ#E
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	PIRQ#F
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	PIRQ#G
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	PIRQ#H
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	JAUD2_EN#
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	SMB_ALERT#
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	0	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	N/A	PGNT#5
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	1	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	1	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	PREQ#4
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC (NO CHANGE)
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	1	NC
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	0	NC
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	0	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	0	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	OC#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	1	BIOS_WP#
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	1	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	0	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	1	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	PGNT#4
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO W83627EHF(CONTINUE)

GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP44	DTRB#	81	DTRB#	OUT8	UART B Data Terminal Ready.
GP45	RTSB#	80	RTSB#	OUT8	UART B Request To Send.
GP46	DSRB#	79	DSRB#	INt	Data Set Ready.
GP47	CTSB#	78	CTSB#	INt	Clear To Send.
GP50	EN_VRM10/WDTO#	77	STRAPPED DOWN	INcd	defined as VID transition voltage level
GP51	RSMRST#	75	RSMRST#	OD12	Resume reset signal output.
GP52	SUSB#	73	SLP_S3#	INt	System S3 states input.
GP53	PSON#	72	PSON#	OD12	This pin generates the PWRCTL# signal while the power failure.
GP56	PSIN	68	PSIN	INtd	Panel Switch Input.
GP57	PSOUT#	67	PSOUT#	OD12	Panel Switch Output.
GP60	RIA#	57	RIA#	INt	Ring Indicator.
GP61	DCDA#	56	DCDA#	INt	Data Carrier Detect.
GP62	SOUTA/PENKBC	54	SOUTA	OUT8	UART A Serial Output.
GP63	SINA	53	SINA	INt	Serial Input.
GP64	DTRA#/PENROM	52	DTRA#	OUT8	UART A Data Terminal Ready.
GP65	RTSA#/HEFRAS	51	RTSA#	OUT8	UART A Request To Send.
GP66	DSRA#	50	DSRA#	INt	Data Set Ready.
GP67	CTSA#	49	CTSA#	INt	Clear To Send.

FWH

GPIO	PIN	POWER	TOL	SIGNAL NAME
FGPI0	6	MAIN	3.3V	ATADET0
FGPI1	5	MAIN	3.3V	PULL UP
FGPI2	4	MAIN	3.3V	PULL UP
FGPI3	3	MAIN	3.3V	PULL UP
FGPI4	30	MAIN	3.3V	PULL DOWN

Note: FWH GPs should only be used for static options, do not put dynamic nets on these

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
LAN	PIRQ#E	PREQ#4 PGNT#4	AD20	PCI_LAN
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1
PCI3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD18	PCI_CLK2
PCI4	PIRQ#D PIRQ#A PIRQ#B PIRQ#C	PREQ#3 PGNT#3 PREQ#5 PGNT#5	AD19 AD21	PCI_CLK3 PCI_CLK4

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM 1	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM 2	A2H	P_DDR3_A/N_DDR3_A P_DDR4_A/N_DDR4_A P_DDR5_A/N_DDR5_A
DIMM 3	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B
DIMM 4	A6H	P_DDR3_B/N_DDR3_B P_DDR4_B/N_DDR4_B P_DDR5_B/N_DDR5_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

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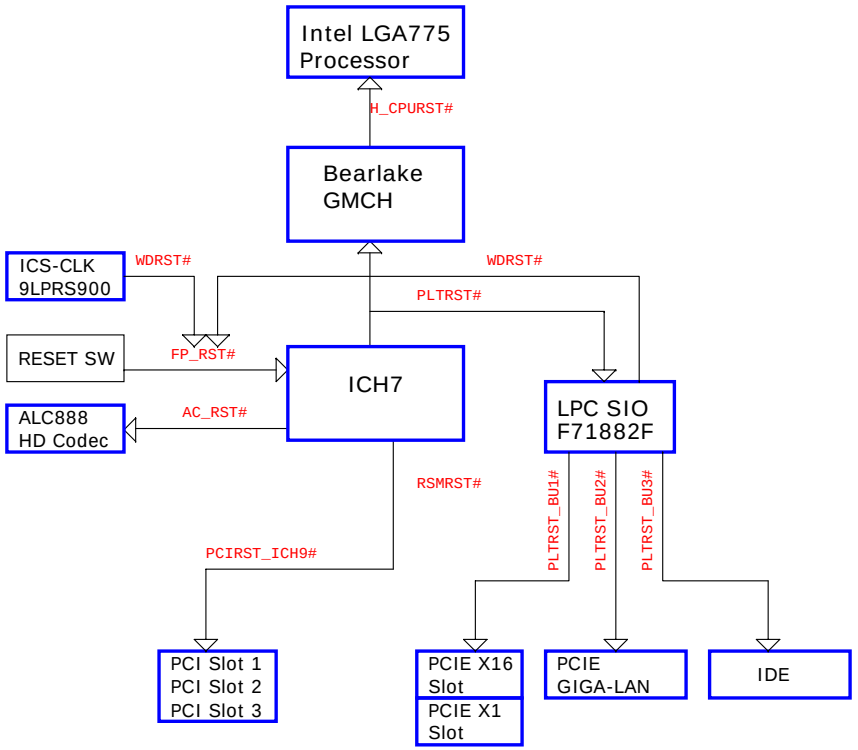
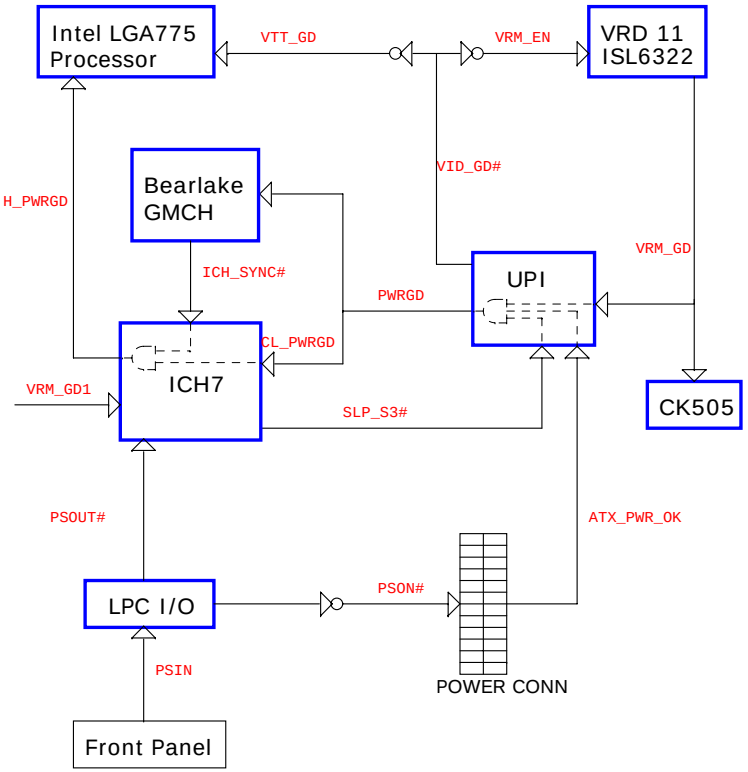
RESET MAP



PWROK MAP



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