VL390 FOR uBTX

CPU:

AMD AM3

System Chipset:

AMD - RS780(North Bridge)
AMD - SB710 (South Bridge)

On Board Chipset:

BIOS - SPI
Azalia CODEC - Realtek ALC662(Default)/888
LPC Super I/O -- ITE8720
CLOCK GEN --SLG8LP625
LAN-Realtek 8111CP
TMP - INFINEON/SLB9635T

Main Memory:

DDR III * 4

Expansion Slots:

PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI 2.3 Slot * 2

Intersil PWM:

Controller - Intersil 6323 3 Phase

MSI MICRO-START INT'L CO.,LTD.

Title: COVER SHEET		
Size: Custom	Document Number: VL390	Rev: 0A
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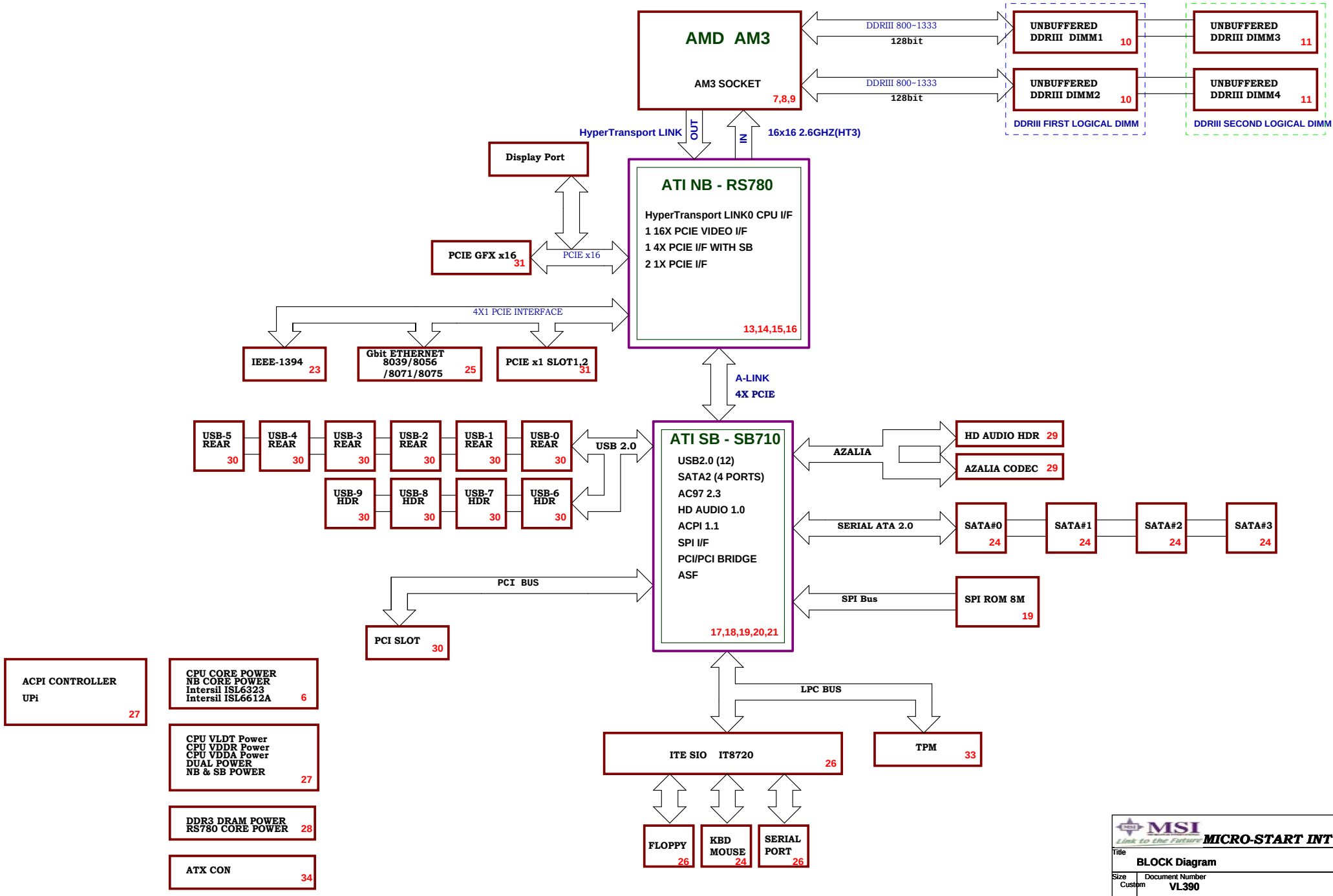
Project RS-780 BLOCK DIAGRAM



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SB700/710 GPIO Config

GPIO Name	Type	Function description	Pin
CLK_REQ0#/SATA_IS3#/GPIO0	3.3V	Not connected(internal pull-down)	
SPKR/GPIO2		SPKR	
FANOUT0/GPIO3		Not connected (internal PU to +3.3V_S0)	
SMARTVOLT/SATA_IS2#/GPIO4		CPU_PRESENT#:CPU present detect	
SHUTDOWN#/GPIO5		R377 10KR to GND	
CLK_REQ3#/SATA_IS1#/GPIO6		Note1	
DDC1_SDA/GPIO8		Note1	
DDC1_SCL/GPIO9		Note1	
SATA_IS0#/GPIO10		Note1	
SPI_DO/GPIO11		SPI_DATAOUT	
BMREQ#/REQ5#/GPIO68		SPI_DATAIN	
LAN_RST#/GPIO13		Reserve TP	
ROM_RST#/GPIO14		Not connected (defaults to output driven low)	
GPIO[30:15]/IDE_D[15:0]		Not connected	
SPI_HOLD#/GPIO31		SPI_HOLD_L	
SPI_CS#/GPIO32		SPI_CS#	
CLK_REQ1#/GPIO39		Not connected (internal pull-down).	
CLK_REQ2#/GPIO40		Not connected (internal pull-down)	
PCICLK5/GPIO41		Terminated with a strapping resistor	
AZ_SDIN0/GPIO42		SDATA_IN_R	
AZ_SDIN1/GPIO43		Not connected (internal pull-down)	
AZ_SDIN2/GPIO44		Not connected (internal pull-down)	
AZ_SDIN3/GPIO46		Not connected (internal pull-down)	
SPI_CLK/GPIO47		SPI_CLK	
GPIO[49:48]/ FANOUT[2:1]]		Not connected (internal pull-up to +3.3V_S0)	
GPIO[52:50]/ FANIN[2:0]		Note1	
GPIO[60:53]/ VIN[7:0]		Note1	
GPIO[63:61]/ TEMPIN[2:0]		Note1	
GPIO64/ TALERT#/ TEMPIN3		TALERT#	
GPIO65/ BMREQ#/ REQ5#		Note1	
GPIO66/ LLB#		LC_SENSE	
GPIO67/ SATA_ACT#		SATA_LED#	
GPIO68/ LDRQ1#/ GNT5#		Reserve TP54	
GPIO[71:70]/ REQ[4:3]#		Not connected (internal pull-up to +3.3V_S0)	
GPIO[73:72]/ GNT[4:3]#		Not connected (defaults to output HIGH).	
GPOC0#/ SCL0		SCLK	
GPOC1#/ SDA0		SDATA	
GPOC2#/ SCL1		SCLK1	
GPOC3#/ SDA1		SDATA1	
USB_OC[5:0]#/GPM[5:0]#		OC#[6::1]	
SYS_RESET#/GPM7#		FP_RST#	
AZ_DOCK_RST#/GPM8#		Not connected (internal pull-up to +3.3V_S5).	
SLP_S2/GPM9#		GFX16_PCIERST#	

NOTE1

Configured for one of these options:
"10-k? 5% pull-up resistor to +3.3V_S0.
"10-k? 5% pull-down resistor.
"Configured GPIO to output mode.
"Configured for internal pull-up or pull-down resistor.

SIO IT8720 GPIO Config

GPIO Name	Type	Function description	Pin
VDIMM_STR_EN / PCIRST3#/GP10	3.3V	Not connected(internal pull-down)	
SPKR/GPIO2		SPKR	
FANOUT0/GPIO3		Not connected (internal PU to +3.3V_S0)	
SMARTVOLT/SATA_IS2#/GPIO4		CPU_PRESENT#:CPU present detect	
SHUTDOWN#/GPIO5		R377 10KR to GND	
CLK_REQ3#/SATA_IS1#/GPIO6		Note1	
DDC1_SDA/GPIO8		Note1	
DDC1_SCL/GPIO9		Note1	
SATA_IS0#/GPIO10		Note1	
SPI_DO/GPIO11		SPI_DATAOUT	
BMREQ#/REQ5#/GPIO68		SPI_DATAIN	
LAN_RST#/GPIO13		Reserve TP	
ROM_RST#/GPIO14		Not connected (defaults to output driven low)	
GPIO[30:15]/IDE_D[15:0]		Not connected	
SPI_HOLD#/GPIO31		SPI_HOLD_L	
SPI_CS#/GPIO32		SPI_CS#	
CLK_REQ1#/GPIO39		Not connected (internal pull-down).	
CLK_REQ2#/GPIO40		Not connected (internal pull-down)	
PCICLK5/GPIO41		Terminated with a strapping resistor	
AZ_SDIN0/GPIO42		SDATA_IN_R	
AZ_SDIN1/GPIO43		Not connected (internal pull-down)	
AZ_SDIN2/GPIO44		Not connected (internal pull-down)	
AZ_SDIN3/GPIO46		Not connected (internal pull-down)	
SPI_CLK/GPIO47		SPI_CLK	
GPIO[49:48]/ FANOUT[2:1]]		Not connected (internal pull-up to +3.3V_S0)	
GPIO[52:50]/ FANIN[2:0]		Note1	
GPIO[60:53]/ VIN[7:0]		Note1	
GPIO[63:61]/ TEMPIN[2:0]		Note1	
GPIO64/ TALERT#/ TEMPIN3		TALERT#	
GPIO65/ BMREQ#/ REQ5#		Note1	
GPIO66/ LLB#		LC_SENSE	
GPIO67/ SATA_ACT#		SATA_LED#	
GPIO68/ LDRQ1#/ GNT5#		Reserve TP54	
GPIO[71:70]/ REQ[4:3]#		Not connected (internal pull-up to +3.3V_S0)	
GPIO[73:72]/ GNT[4:3]#		Not connected (defaults to output HIGH).	
GPOC0#/ SCL0		SCLK	
GPOC1#/ SDA0		SDATA	
GPOC2#/ SCL1		SCLK1	
GPOC3#/ SDA1		SDATA1	
USB_OC[5:0]#/GPM[5:0]#		OC#[6::1]	
SYS_RESET#/GPM7#		FP_RST#	
AZ_DOCK_RST#/GPM8#		Not connected (internal pull-up to +3.3V_S5).	
SLP_S2/GPM9#		GFX16_PCIERST#	

MSI Live for the Future MICRO-START INT'L CO.,LTD.

Title: GPIO Configuration

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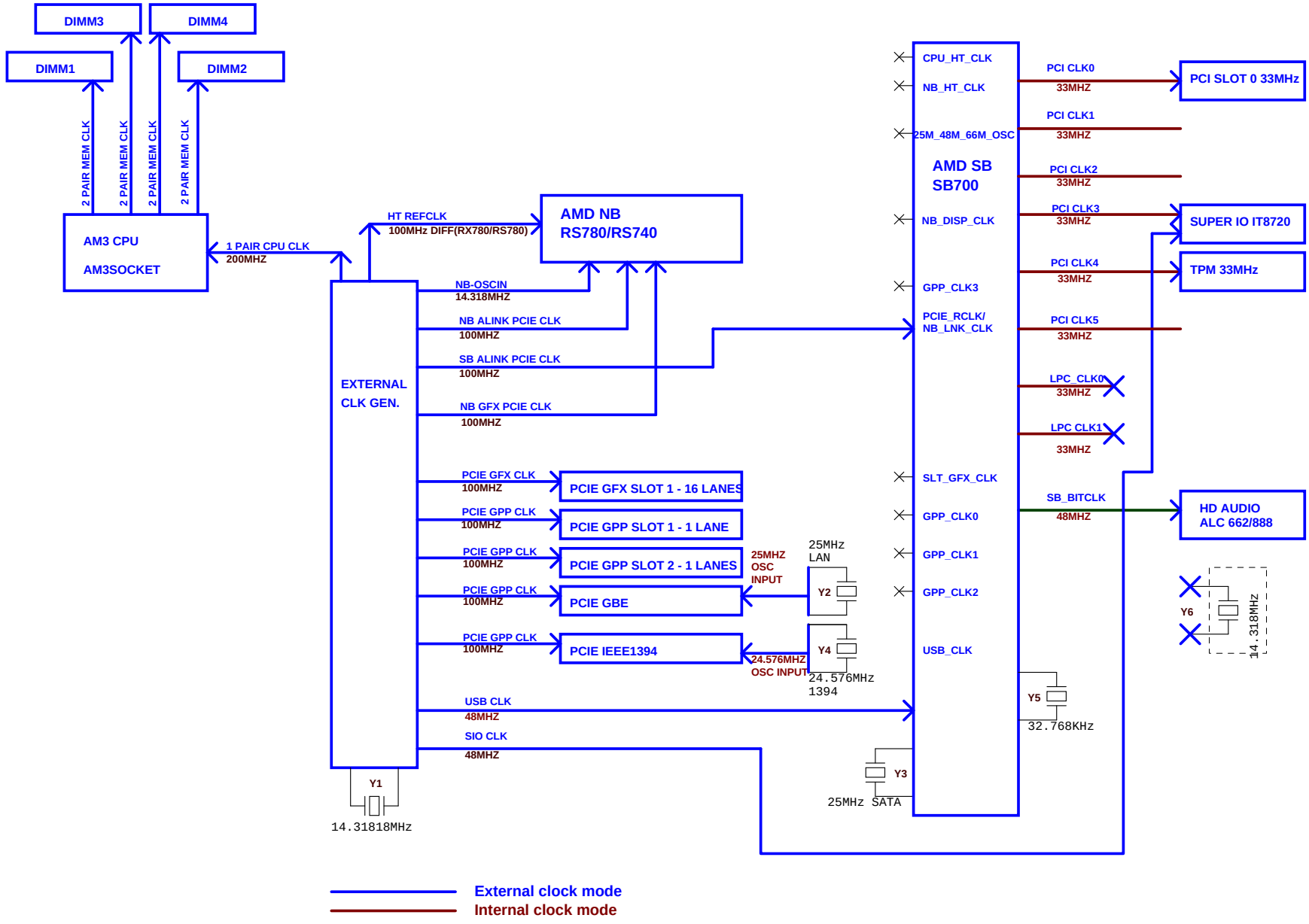

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Title: Clock Distribution Chart

Size	Document Number	Rev
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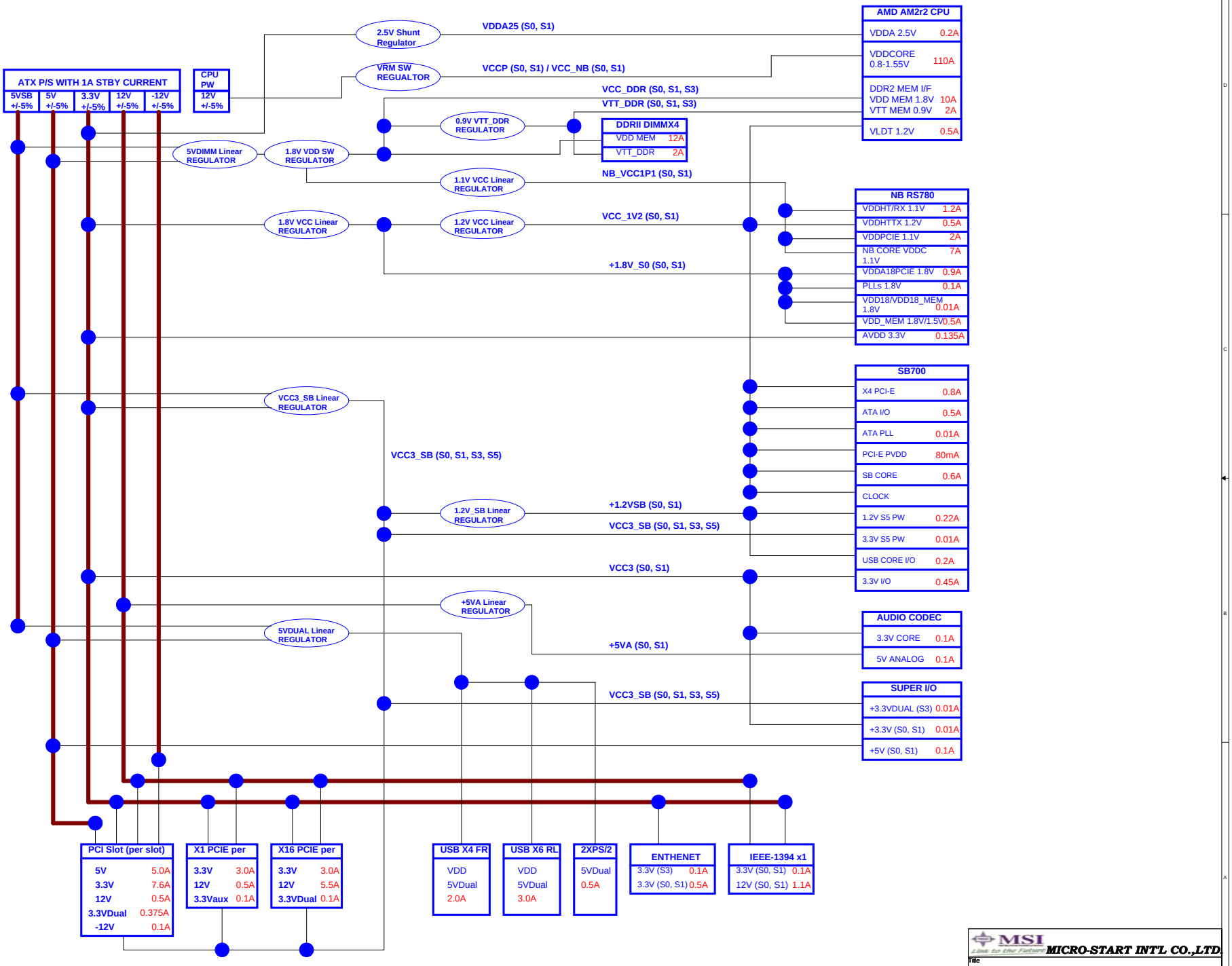
Power Deliver Chart



MSI MICRO-START INT'L CO.,LTD.

Title	Power Deliver Chart	
Size: C	Document Number: VL390	Rev: 0A
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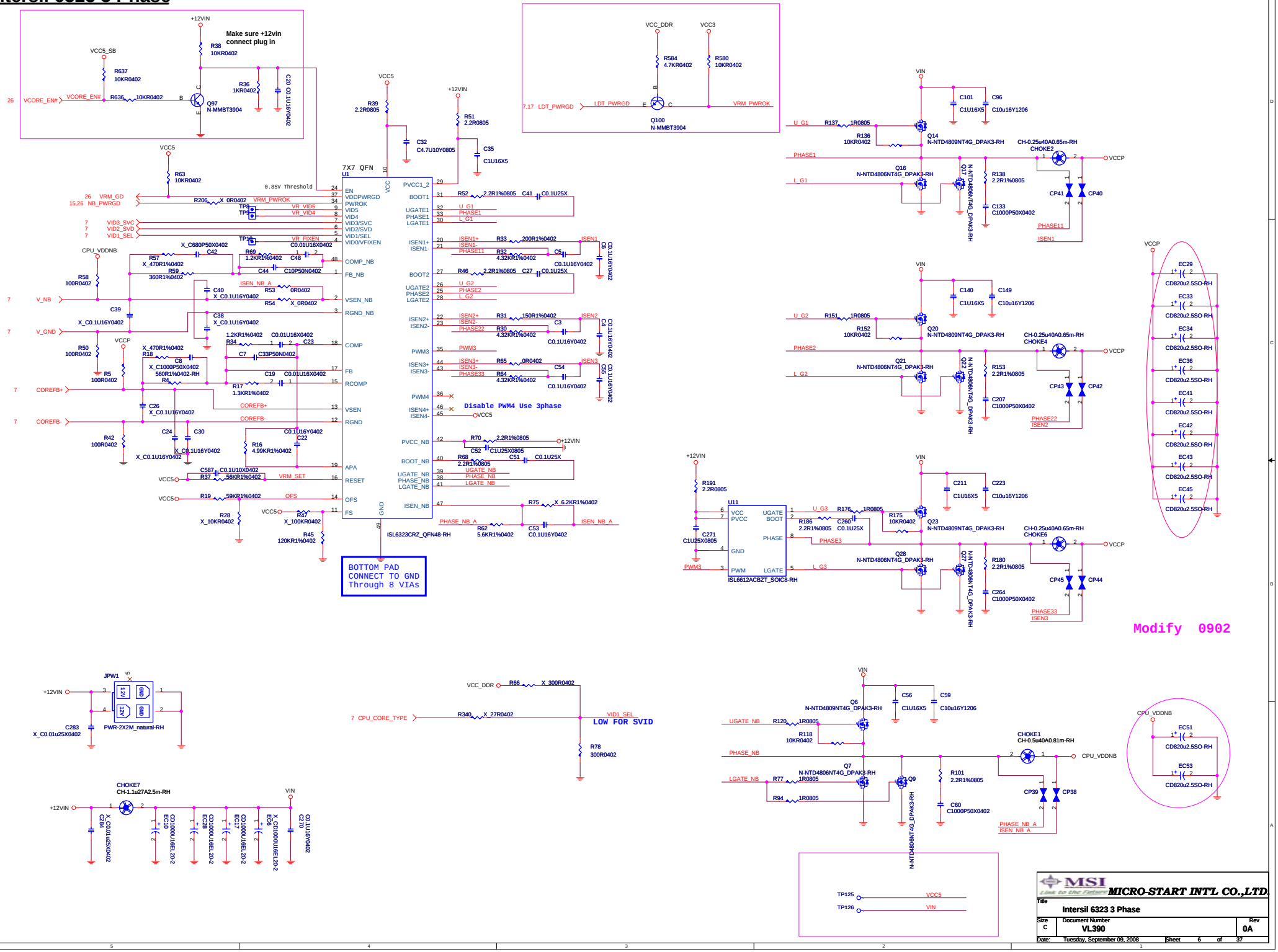
Intersil 6323 3 Phase



Title	Intersil 6323 3 Phase
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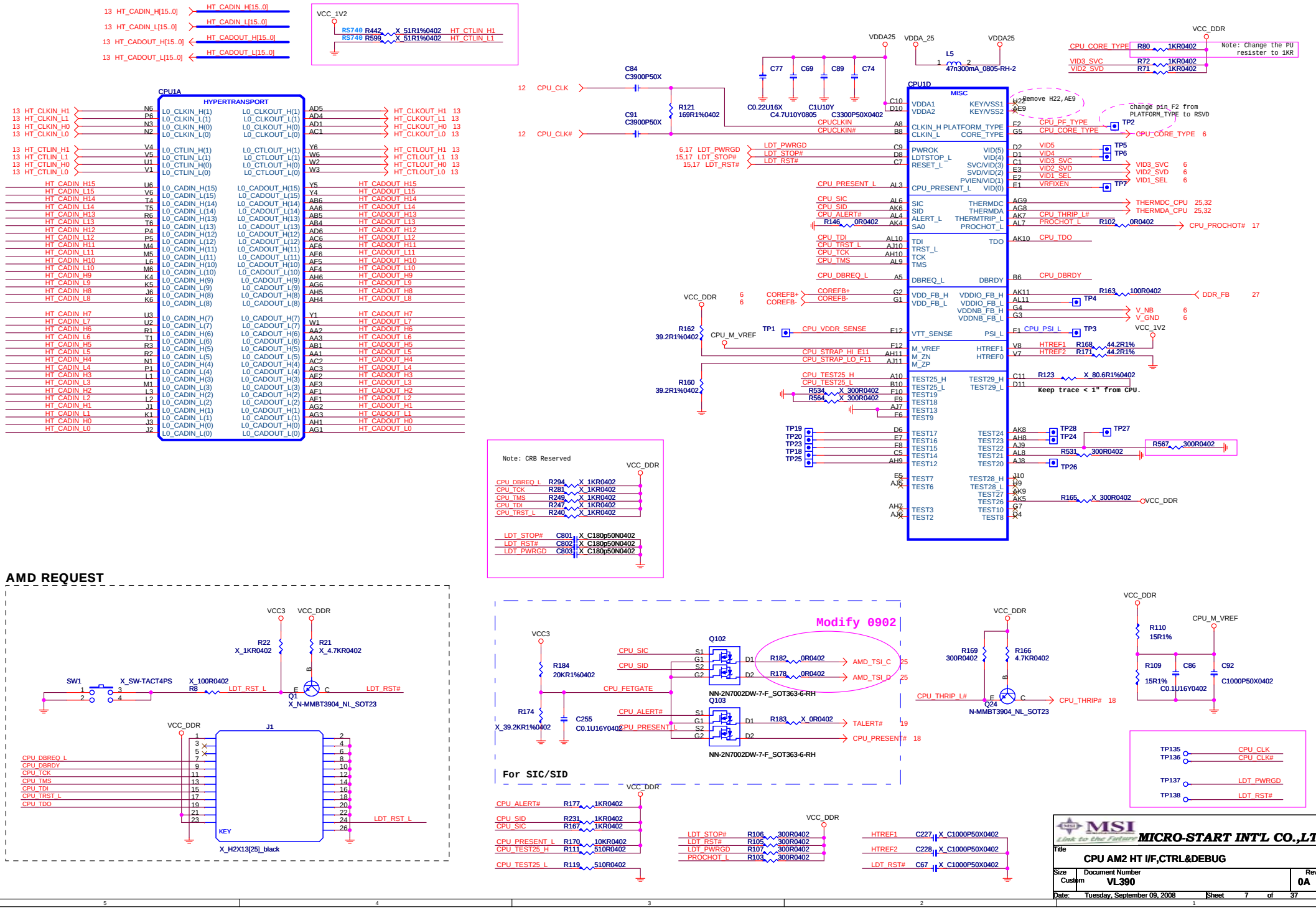
MSI MICRO-STAR INT'L CO.,LTD.


13 HT_CADIN_H[15..0]
HT_CADIN_H[15..0]
13 HT_CADIN_L[15..0]
HT_CADIN_L[15..0]
13 HT_CADOUT_H[15..0]
HT_CADOUT_H[15..0]
13 HT_CADOUT_L[15..0]
HT_CADOUT_L[15..0]
VCC_1V2
RS740 R442 X_51R1%0402 HT_CTLIN_H1
RS740 R599 X_51R1%0402 HT_CTLIN_L1
CPU1A
HYPERTRANSPORT
HT_CLKIN_H1 HT_CLKIN_L1 HT_CLKIN_H0 HT_CLKIN_L0
HT_CTLIN_H1 HT_CTLIN_L1 HT_CTLIN_H0 HT_CTLIN_L0
HT_CADIN_H15 HT_CADIN_L15 HT_CADIN_H14 HT_CADIN_L14 HT_CADIN_H13 HT_CADIN_L13 HT_CADIN_H12 HT_CADIN_L12 HT_CADIN_H11 HT_CADIN_L11 HT_CADIN_H10 HT_CADIN_L10 HT_CADIN_H9 HT_CADIN_L9 HT_CADIN_H8 HT_CADIN_L8
HT_CADIN_H7 HT_CADIN_L7 HT_CADIN_H6 HT_CADIN_L6 HT_CADIN_H5 HT_CADIN_L5 HT_CADIN_H4 HT_CADIN_L4 HT_CADIN_H3 HT_CADIN_L3 HT_CADIN_H2 HT_CADIN_L2 HT_CADIN_H1 HT_CADIN_L1 HT_CADIN_H0 HT_CADIN_L0
HT_CLKOUT_H1 HT_CLKOUT_L1 HT_CLKOUT_H0 HT_CLKOUT_L0
HT_CTLOUT_H1 HT_CTLOUT_L1 HT_CTLOUT_H0 HT_CTLOUT_L0
HT_CADOUT_H15 HT_CADOUT_L15 HT_CADOUT_H14 HT_CADOUT_L14 HT_CADOUT_H13 HT_CADOUT_L13 HT_CADOUT_H12 HT_CADOUT_L12 HT_CADOUT_H11 HT_CADOUT_L11 HT_CADOUT_H10 HT_CADOUT_L10 HT_CADOUT_H9 HT_CADOUT_L9 HT_CADOUT_H8 HT_CADOUT_L8
HT_CADOUT_H7 HT_CADOUT_L7 HT_CADOUT_H6 HT_CADOUT_L6 HT_CADOUT_H5 HT_CADOUT_L5 HT_CADOUT_H4 HT_CADOUT_L4 HT_CADOUT_H3 HT_CADOUT_L3 HT_CADOUT_H2 HT_CADOUT_L2 HT_CADOUT_H1 HT_CADOUT_L1 HT_CADOUT_H0 HT_CADOUT_L0
CPU1D
MISC
CPU_CLK
CPU_CLK#
C84 C3900P50X
C91 C3900P50X
R121 169R1%0402
C77 C0.22U16X
C69 C4.7U10Y0805
C89 C1U10Y
C74 C3300P50X0402
VDDA25
VDDA_25
L5 47n300mA_0805-RH-2
CPU_CORE_TYPE R80 1KR0402
VID3_SVC R72 1KR0402
VID2_SVD R71 1KR0402
VCC_DDR
Note: Change the PU resister to 1KR
Remove H22,AE9
Change pin F2 from PLATFORM_TYPE to RSVD
CPUCLKIN CPUCLKIN# PWROK LDTSTOP_L RESET_L CPU_PRESENT_L
CPU_PF_TYPE CPU_CORE_TYPE VID5 VID4 VID3_SVC VID2_SVD VID1_SEL VRFIXEN
TP2 TP5 TP6 TP7
LDT_PWRGD LDT_STOP# LDT_RST#
6,17 LDT_PWRGD 15,17 LDT_STOP# 15,17 LDT_RST#
CPU_SIC CPU_SID CPU_ALERT# R146 0R0402
CPU_TDI CPU_TRST_L CPU_TCK CPU_TMS
CPU_DBREQ_L CPU_DBRDY CPU_TDO
THERMDC_CPU 25,32
THERMDA_CPU 25,32
CPU_THRIP_L# PROCHOT_L R102 0R0402 CPU_PROCHOT# 17
VCC_DDR 6 6
COREFB+ COREFB-
R162 39.2R1%0402
R160 39.2R1%0402
CPU_M_VREF
TP1
CPU_VDDR_SENSE
CPU_STRAP_HI_E11
CPU_STRAP_LO_F11
CPU_TEST25_H CPU_TEST25_L R534 X_300R0402 R564 X_300R0402
VDD_FB_H VDD_FB_L VDDIO_FB_H VDDIO_FB_L VDDNB_FB_H VDDNB_FB_L VTT_SENSE PSI_L
R163 100R0402 DDR_FB 27
TP4
V_NB 6
V_GND 6
CPU_PSI_L TP3
VCC_1V2
HTREF1 R168 44.2R1% HTREF2 R171 44.2R1%
R123 X_80.6R1%0402
Keep trace < 1" from CPU.
TP19 TP20 TP23 TP18 TP25
TEST25_H TEST25_L TEST19 TEST18 TEST13 TEST9
TEST17 TEST16 TEST15 TEST14 TEST12
TEST7 TEST6
TEST3 TEST2
TEST29_H TEST29_L
TEST24 TEST23 TEST22 TEST21 TEST20
TEST28_H TEST28_L TEST27 TEST26 TEST10 TEST8
TP28 TP24 TP27 TP26
R531 300R0402
R567 300R0402
R165 X_300R0402 VCC_DDR
Note: CRB Reserved
VCC_DDR
CPU_DBREQ_L R294 X_1KR0402
CPU_TCK R281 X_1KR0402
CPU_TMS R249 X_1KR0402
CPU_TDI R247 X_1KR0402
CPU_TRST_L R240 X_1KR0402
LDT_STOP# C801 X_C180p50N0402
LDT_RST# C802 X_C180p50N0402
LDT_PWRGD C803 X_C180p50N0402
AMD REQUEST
VCC3 VCC_DDR
R22 X_1KR0402
R21 X_4.7KR0402
SW1 X_SW-TACT4PS
X_100R0402 R8
LDT_RST_L
Q1 X_N-MMBT3904_NL_SOT23
LDT_RST#
VCC_DDR
J1
CPU_DBREQ_L CPU_DBRDY CPU_TCK CPU_TMS CPU_TDI CPU_TRST_L CPU_TDO
KEY
X_H2X13[25]_black
LDT_RST_L
Modify 0902
VCC3
R184 20KR1%0402
R174 X_39.2KR1%0402
C255 C0.1U16Y0402
CPU_SIC CPU_SID CPU_FETGATE CPU_ALERT# CPU_PRESENT_L
Q102
Q103
NN-2N7002DW-7-F_SOT363-6-RH
R182 0R0402 AMD_TSI_C 25
R178 0R0402 AMD_TSI_D 25
R183 X_0R0402 TALERT# 19
CPU_PRESENT# 18
For SIC/SID
VCC_DDR
CPU_ALERT# R177 1KR0402
CPU_SID R231 1KR0402
CPU_SIC R167 1KR0402
CPU_PRESENT_L R170 10KR0402
CPU_TEST25_H R111 510R0402
CPU_TEST25_L R119 510R0402
LDT_STOP# R106 300R0402
LDT_RST# R105 300R0402
LDT_PWRGD R107 300R0402
PROCHOT_L R103 300R0402
HTREF1 C227 X_C1000P50X0402
HTREF2 C228 X_C1000P50X0402
LDT_RST# C67 X_C1000P50X0402
VCC_DDR
R169 300R0402
R166 4.7KR0402
CPU_THRIP_L#
Q24 N-MMBT3904_NL_SOT23
CPU_THRIP# 18
VCC_DDR
R110 15R1%
CPU_M_VREF
R109 15R1%
C86 C0.1U16Y0402
C92 C1000P50X0402
TP135 CPU_CLK
TP136 CPU_CLK#
TP137 LDT_PWRGD
TP138 LDT_RST#
MSI
MICRO-START INT'L CO.,LTD.
Title
CPU AM2 HT I/F,CTRL&DEBUG
Size Custom
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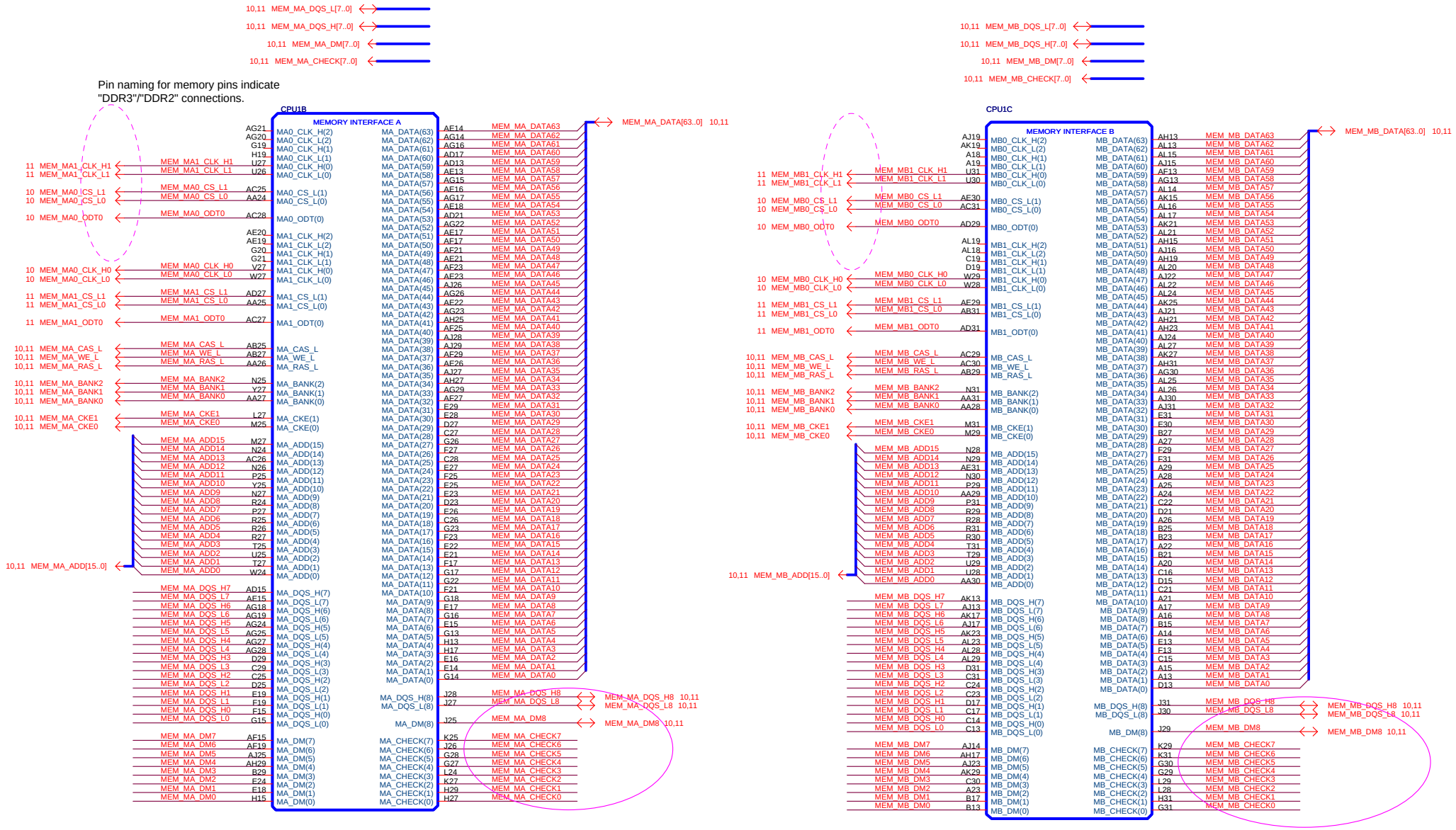

MICRO-START INT'L CO.,LTD.

Title: CPU AM2 DDR MEMORY I/F

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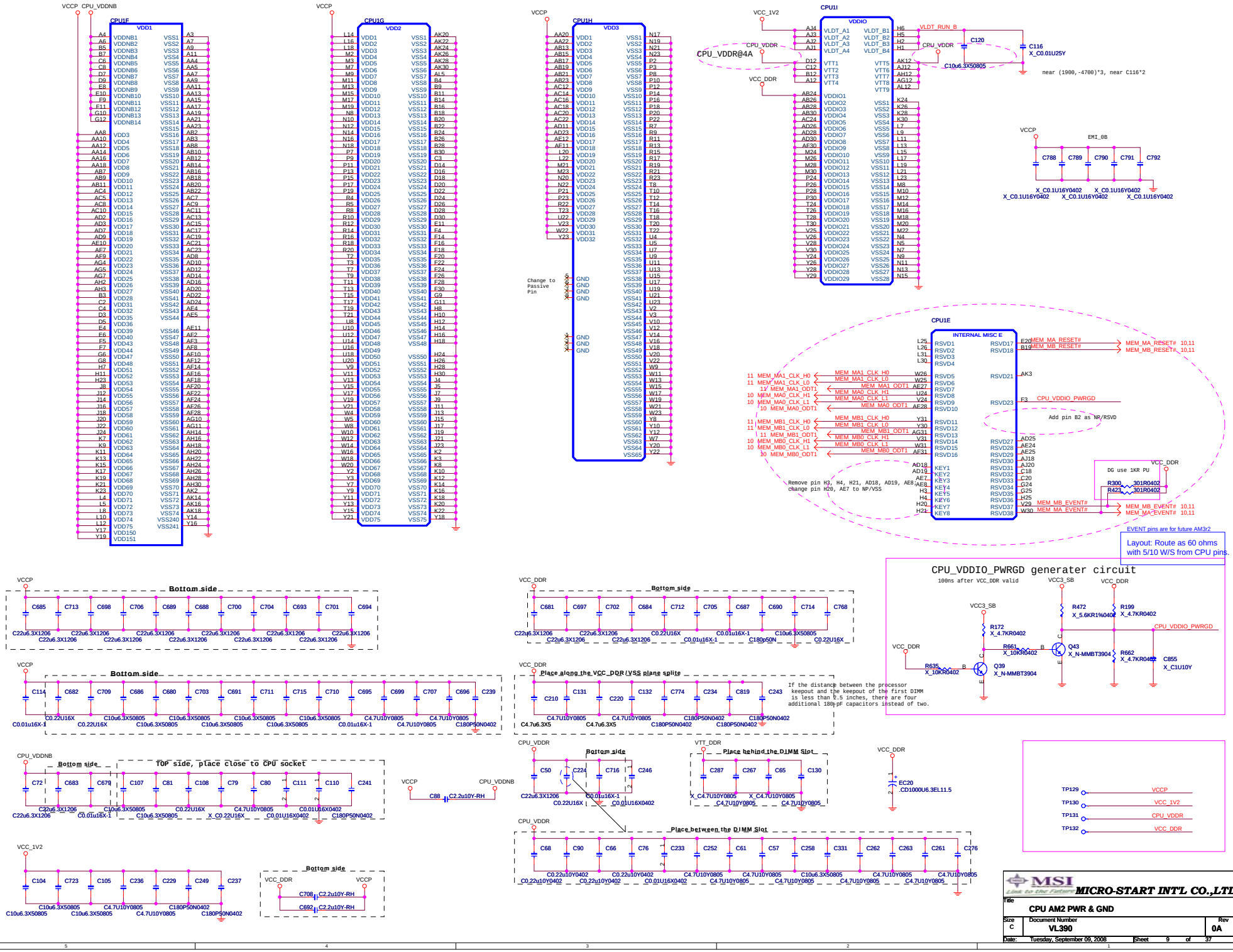
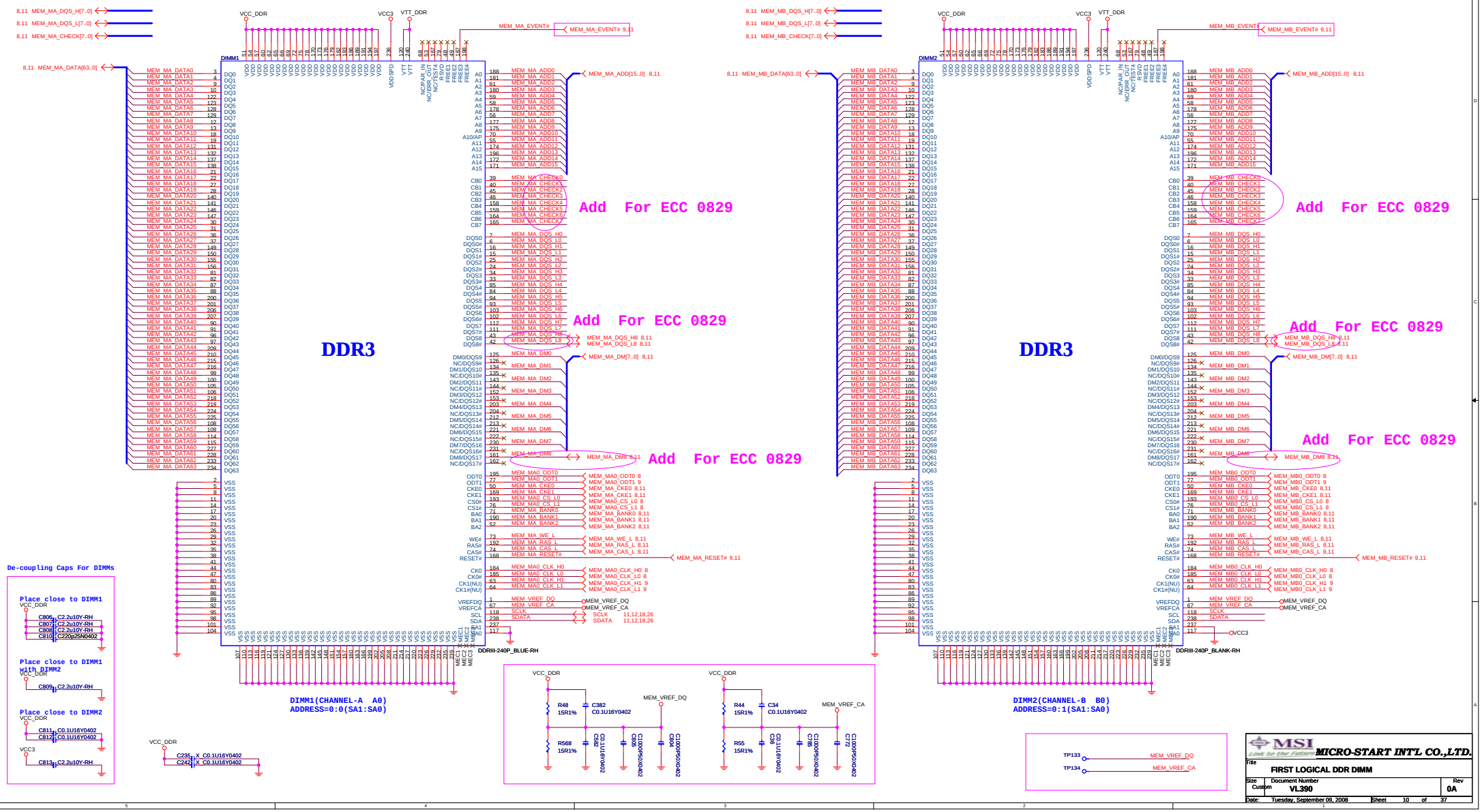
CPU AM2 PWR & GND




DDR3
DDR3
DIMM1
DIMM2
DDRIII-240P_BLUE-RH
DDRIII-240P_BLANK-RH
DIMM1(CHANNEL-A A0)
ADDRESS=0:0(SA1:SA0)
DIMM2(CHANNEL-B B0)
ADDRESS=0:1(SA1:SA0)
Add For ECC 0829
Add For ECC 0829
Add For ECC 0829
Add For ECC 0829
Add For ECC 0829
Add For ECC 0829
De-coupling Caps For DIMMs
Place close to DIMM1
Place close to DIMM1 with DIMM2
Place close to DIMM2
MEM_VREF_DQ
MEM_VREF_CA
MICRO-START INT'L CO.,LTD.
FIRST LOGICAL DDR DIMM
VL390
0A
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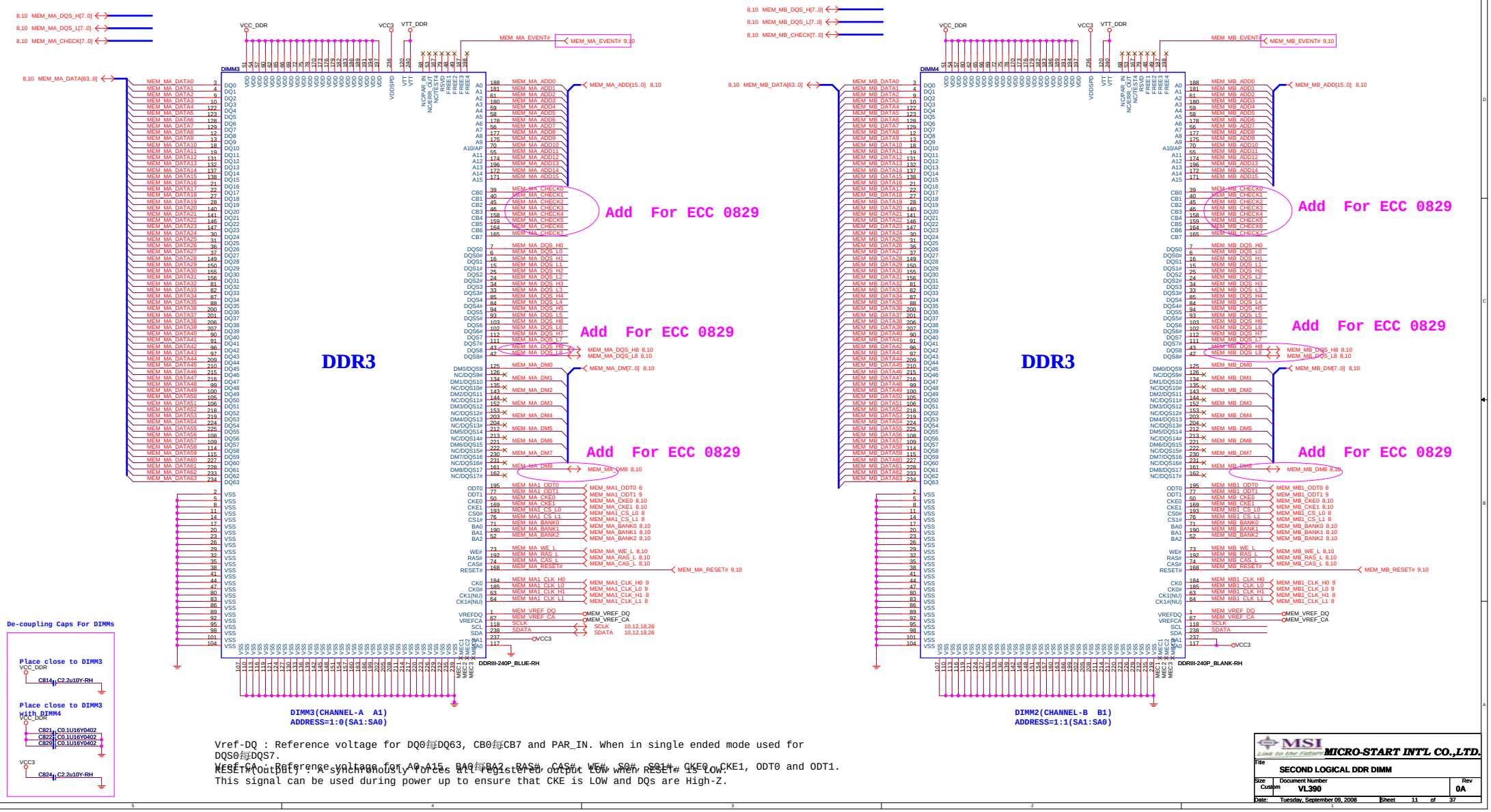

Vref-DQ : Reference voltage for DQ0每DQ63, CB0每CB7 and PAR_IN. When in single ended mode used for DQS0每DQS7.

Vref-CA : Reference voltage for A0-A15, BA0每BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET# (optional) : Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

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Title: SECOND LOGICAL DDR DIMM

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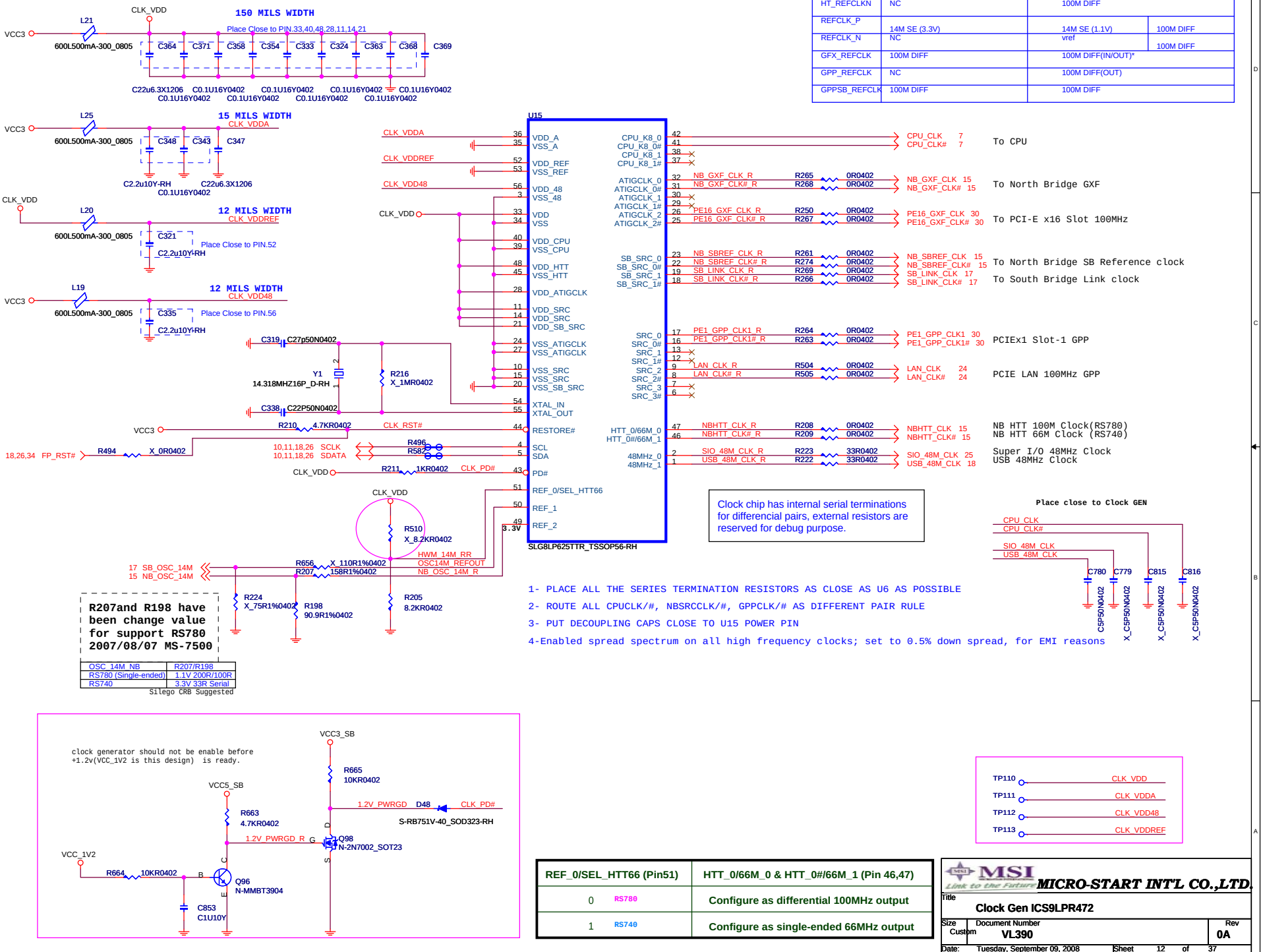
Clock Gen SLG8LP625

NB CLOCK INPUT TABLE

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

NB CLOCKS	RS740	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	
HT_REFCLKN	NC	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	



R207and R198 have been change value for support RS780 2007/08/07 MS-7500

OSC_14M_NB	R207/R198
RS780 (Single-ended)	1.1V 200R/100R
RS740	3.3V 33R Serial

Silego CRB Suggested

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U6 AS POSSIBLE
2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U15 POWER PIN
4-Enabled spread spectrum on all high frequency clocks; set to 0.5% down spread, for EMI reasons

REF_0/SEL_HTT66 (Pin51)	HTT_0/66M_0 & HTT_0#/66M_1 (Pin 46,47)
0 RS780	Configure as differential 100MHz output
1 RS740	Configure as single-ended 66MHz output

MICRO-START INT'L CO.,LTD.

Title	Clock Gen ICS9LPR472	
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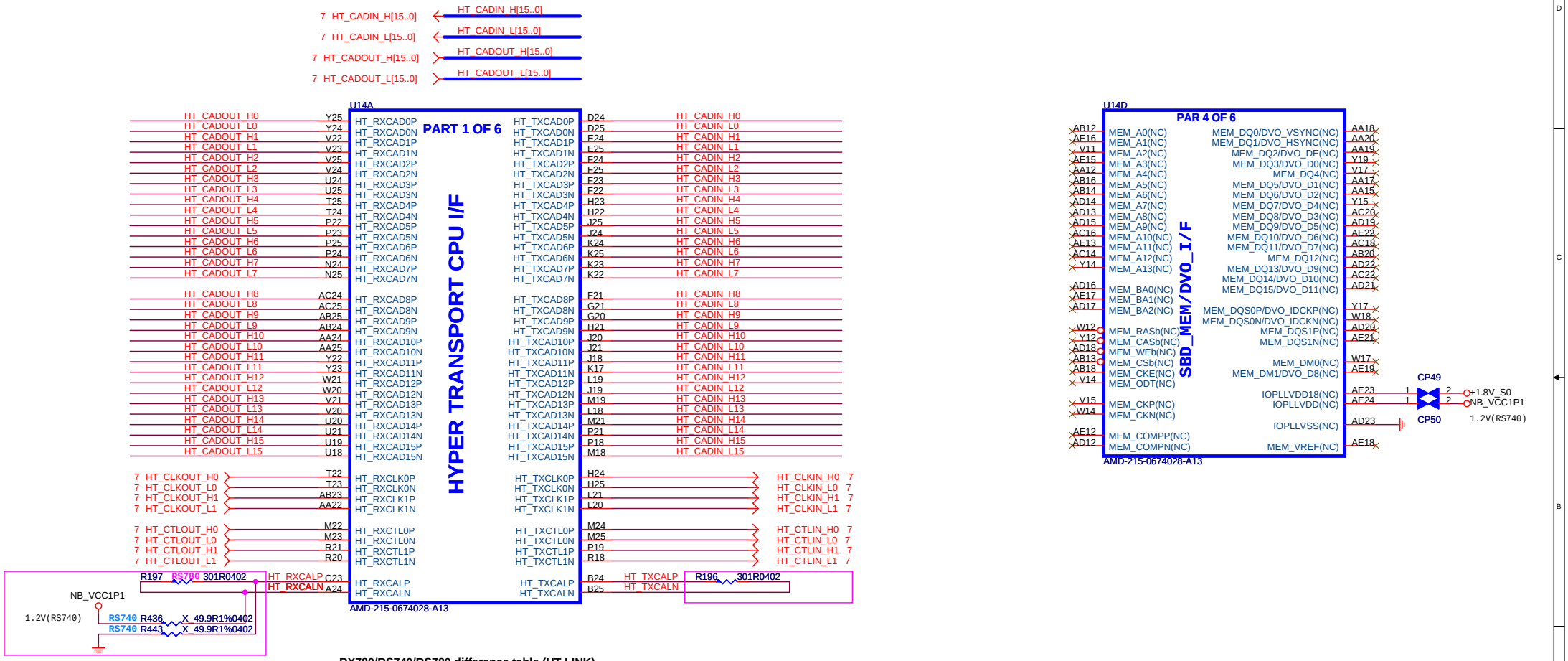
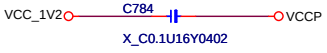
RS780-HT LINK I/F



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RS780
HT_RXCALP	49.9R (GND)	301R
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP HT_TXCALN	100R	301R

Decoupling Cap for HT.



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Title: RS780-HT LINK I/F

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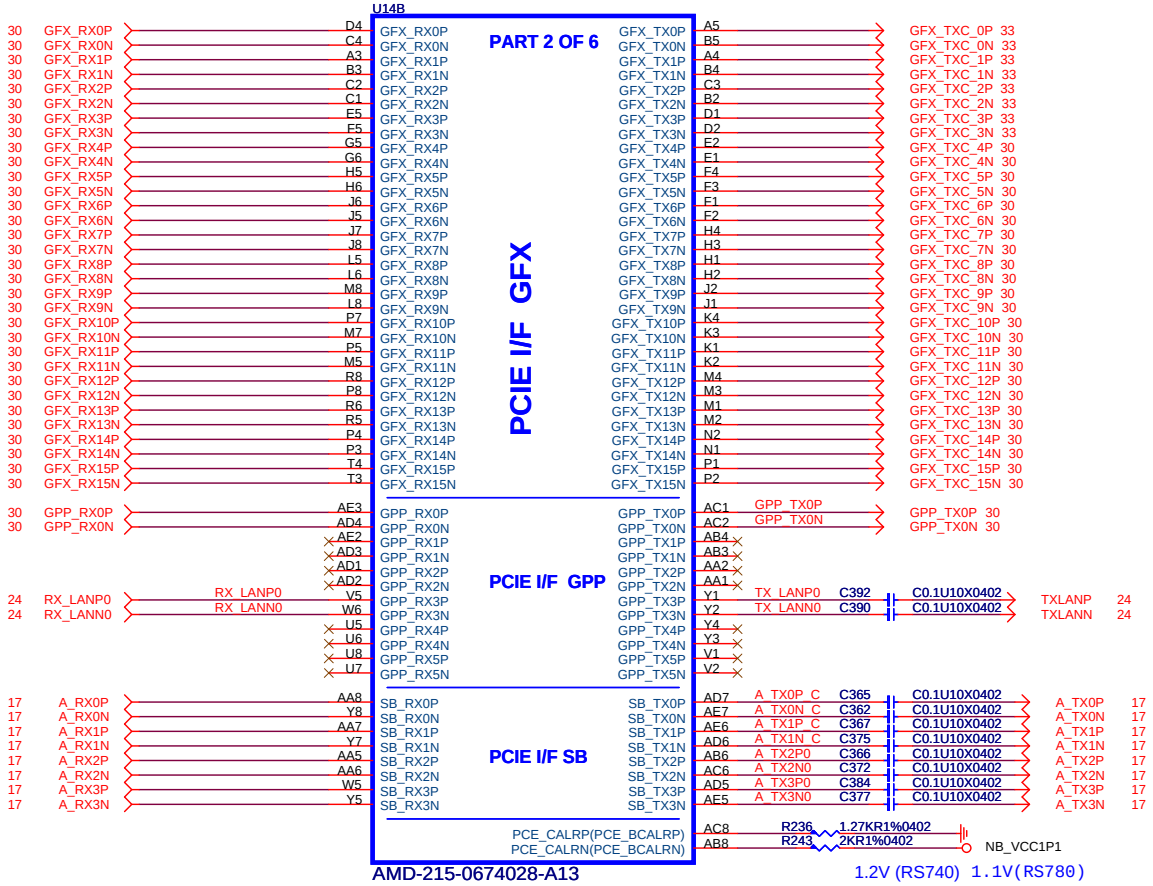
RS780-PCIE I/F



RS780/RS740 GPP difference table

	RS740	RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780/RS740 GPP Routing table

	RS740	RX780/RS780
PCIE1_X1 CONNECTOR	GPP0	GPP0
PCIE1_X2 CONNECTOR	GPP1	GPP1
GIGABIT ETHERNET	GPP3	GPP3

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Title: RS780-PCIE I/F

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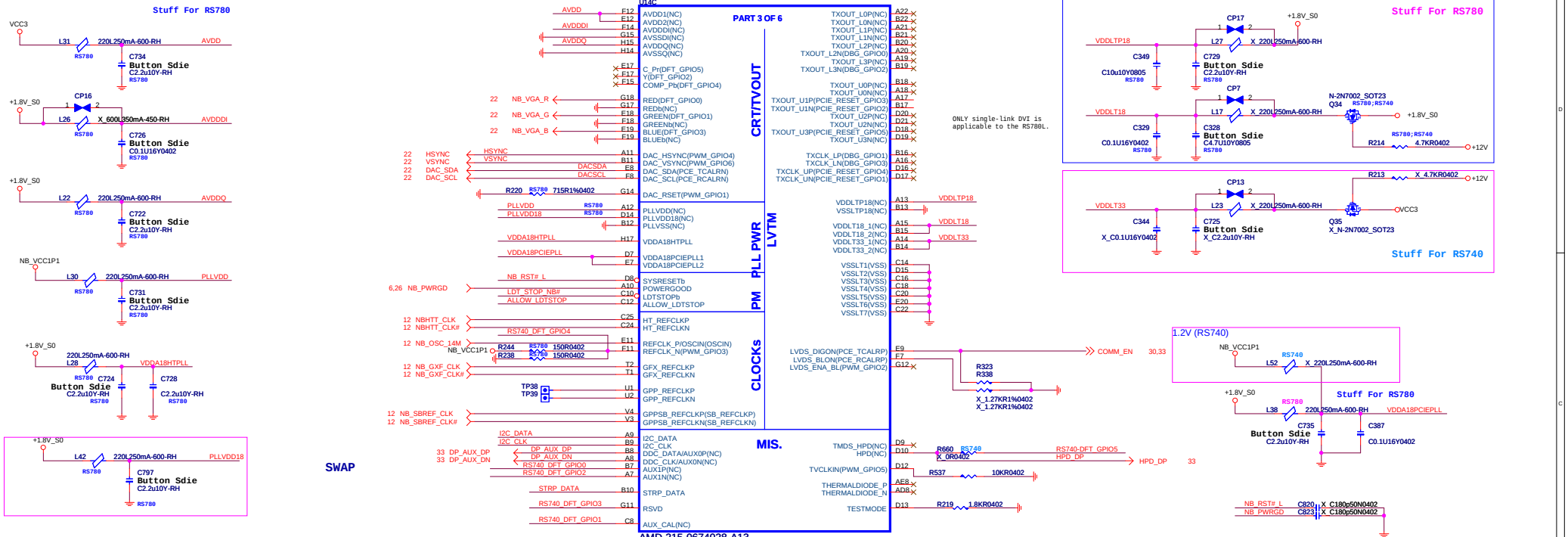
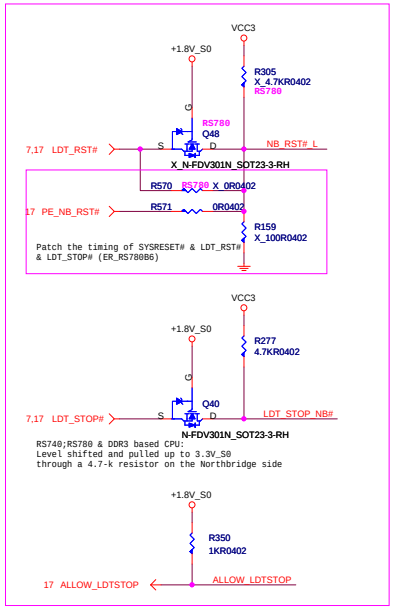
RS780-SYSTEM I/F

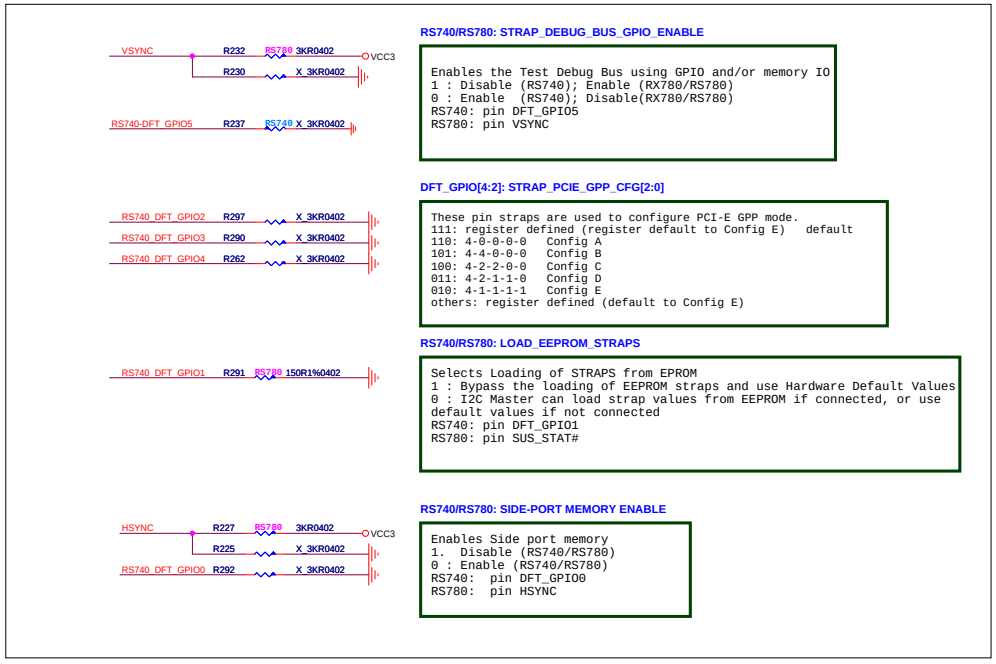


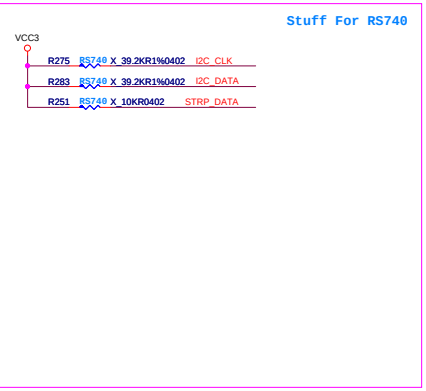
SWAP

RS740/RS780 difference table (Control signal)

	RS740	RS780
NB_PWRGD IN	3.3V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	3.3V IN







MICRO-START INT'L CO.,LTD.

Title: RS780-SYSTEM I/F

Size	Document Number	Rev
C	VL390	0A

Date: Tuesday, September 09, 2008 Sheet 15 of 37

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U14F
AMD-215-0674028-A13

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10

VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

120 MILS WIDTH

NB_VCC1P1 — L16 RS780 220L2A-50-RH — VDDHTRXNB — Bottom side
C305 C301 C312 C721
C0.1U16Y0402 C0.1U25Y
C4.7U10Y0805 C0.1U16Y0402

70 MILS WIDTH

Bottom side
C308 C302 C304 C303 C720
C4.7U10Y0805 C0.1U16Y0402 C0.1U25Y
C0.1U16Y0402 X_C0.1U16Y0402

VCC_1V2 — L14 X_200L400_350_0805 CP6 — VDDHTTXNB — 45 MILS WIDTH — Bottom side
C292 C297 C298 C299 C296 C719
C0.1U16Y0402 C0.1U16Y0402 C0.1U25Y
C4.7U10Y0805 X_C0.1U16Y0402 C0.1U16Y0402

+1.8V_S0 — L29 RS780 220L2A-50-RH — VDD18NB — 20 MILS WIDTH
C350 C351 C352 C353 C360 C733
C4.7U10Y0805 C0.1U16Y0402 C0.1U25Y
C4.7U10Y0805 C0.1U16Y0402 C0.1U16Y0402

+1.8V_S0 — CP52 — VDDG18 — 15 MILS WIDTH — Bottom side
C730 C1U10Y
RS780 without Side-port: Connected to GND plane

U14E
AMD-215-0674028-A13

PART 5/6

POWER

J17	VDDHT_1	VDDPCIE_1 A6
K16	VDDHT_2	VDDPCIE_2 B6
L16	VDDHT_3	VDDPCIE_3 C6
M16	VDDHT_4	VDDPCIE_4 D6
P16	VDDHT_5	VDDPCIE_5 E6
R16	VDDHT_6	VDDPCIE_6 F6
T16	VDDHT_7	VDDPCIE_7 G7
		VDDPCIE_8 H8
H18	VDDHTRX_1	VDDPCIE_9 J9
G19	VDDHTRX_2	VDDPCIE_10 K9
F20	VDDHTRX_3	VDDPCIE_11 M9
E21	VDDHTRX_4	VDDPCIE_12 L9
D22	VDDHTRX_5	VDDPCIE_13 P9
B23	VDDHTRX_6	VDDPCIE_14 R9
A23	VDDHTRX_7	VDDPCIE_15 T9
		VDDPCIE_16 V9
AE25	VDDHTTX_1	VDDPCIE_17 U9
AD24	VDDHTTX_2	
AC23	VDDHTTX_3	VDDC_1 K12
AB22	VDDHTTX_4	VDDC_2 J14
AA21	VDDHTTX_5	VDDC_3 U16
Y20	VDDHTTX_6	VDDC_4 J11
W19	VDDHTTX_7	VDDC_5 K15
V18	VDDHTTX_8	VDDC_6 M12
U17	VDDHTTX_9	VDDC_7 L14
T17	VDDHTTX_10	VDDC_8 L11
R17	VDDHTTX_11	VDDC_9 M13
P17	VDDHTTX_12	VDDC_10 M15
M17	VDDHTTX_13	VDDC_11 N12
		VDDC_12 N14
J10	VDDA18PCIE_1	VDDC_13 P11
P10	VDDA18PCIE_2	VDDC_14 P13
K10	VDDA18PCIE_3	VDDC_15 P14
M10	VDDA18PCIE_4	VDDC_16 R12
L10	VDDA18PCIE_5	VDDC_17 R15
W9	VDDA18PCIE_6	VDDC_18 T11
H9	VDDA18PCIE_7	VDDC_19 T15
T10	VDDA18PCIE_8	VDDC_20 U12
R10	VDDA18PCIE_9	VDDC_21 T14
Y9	VDDA18PCIE_10	VDDC_22 J16
AA9	VDDA18PCIE_11	
AB9	VDDA18PCIE_12	VDD_MEM1(NC) AE10
AD9	VDDA18PCIE_13	VDD_MEM2(NC) AA11
AE9	VDDA18PCIE_14	VDD_MEM3(NC) Y11
U10	VDDA18PCIE_15	VDD_MEM4(NC) AD10
		VDD_MEM5(NC) AB10
F9	VDDG18_1(VDD18_1)	VDD_MEM6(NC) AC10
G9	VDDG18_2(VDD18_2)	
AE11	VDD18_MEM1(NC)	VDDG33_1(NC) H11
AD11	VDD18_MEM2(NC)	VDDG33_2(NC) H12

RS780 without Side-port: Connected to GND plane

NB_VCC1P1 — L39 X_30L3_15_0805 — NB_VDDPCIE — CP21

NB_VDDPCIE — Bottom side — 300 MILS WIDTH
C736 C389 C393 C394 C395
C0.1U25Y C0.1U16Y0402 C1U10Y C1U10Y C4.7U10Y0805

Bottom side — 300 MILS WIDTH — NB_VCC1P1
C727 C309 C311 C317 C310 C316 C315 C306 C307
C0.1U25Y C0.1U16Y0402 C0.1U16Y0402 C0.1U16Y0402 C0.1U16Y0402 C10u10Y0805
C0.1U16Y0402 C0.1U16Y0402 C0.1U16Y0402 C10u10Y0805

Bottom side — 15 MILS WIDTH — RS780 — VCC3
C732 C0.1U16Y0402 — C391 C0.1U16Y0402

TP107 VDDHTRXNB
TP108 VDDHTTXNB
TP109 VDD18NB

VCC3 — D38 BAV99-7-F_SOT23-LF — D39 /N BAV99-7-F_SOT23-LF
R143 X_0R0805 /N
R144 0R0805 — +1.8V_S0

VDDC 1.1V@13A
VDD18 1.8V@10 mA (Pin G9,F9)
VDD33 3.3 V at 60 mA (Pin H11,H12)
VDDA18PCIE 1.8 V at 700 mA
VDDA18PCIEPLL 1.8 V (RS780/RX780) or 1.2 V (RS740) at 120 mA (Pin D7,E7)
VDDHT 1.1 V at 600 mA
VDDHTRX 1.1 V at 700 mA
VDDHTTX 1.2 V at 400 mA
VDDA18HTPLL 1.8 V at 20 mA (Pin H17)
PLLVDD18 1.8 V at 20 mA (Pin D14) Combine with H17
PLLVDD 1.2 V (RS740) or 1.1 V (RS780) at 65 mA (Pin A12)
AVDD 3.3 V at 110 mA (Pin E12,F12)
AVDDQ 1.8 V at 4 mA (Pin H15)
AVDDDI 1.8 V at 20 mA(Pin F14)
VDDLT33 3.3 V at 180 mA (Pin A14,B14) RS740 only
VDDLT18 1.8 V at 300 mA (Pin A15,B15)
VDDLTP18 1.8 V at 15 mA (Pin A13)

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Title: RX780-POWER

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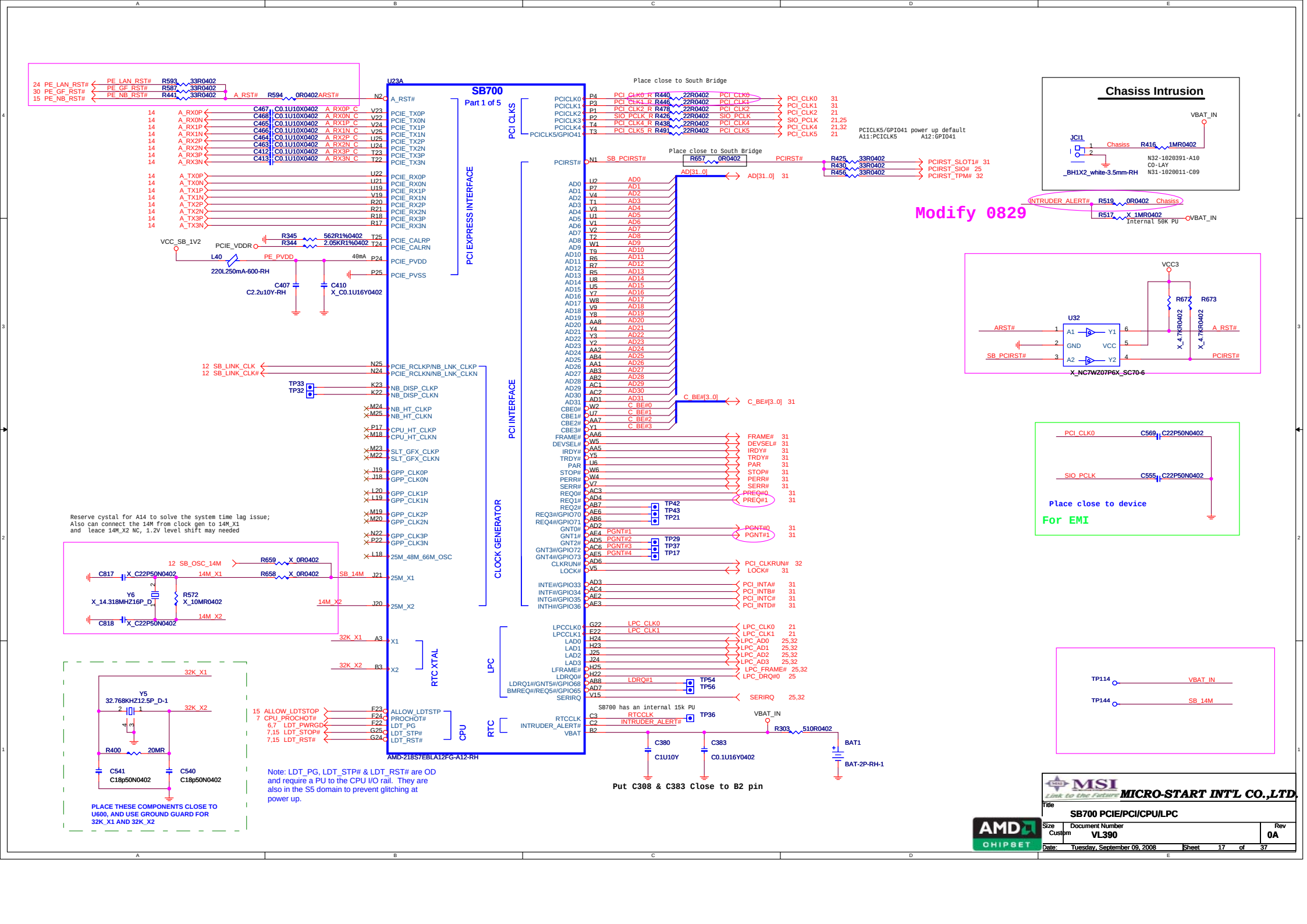
AMD CHIPSET


SB700
Part 1 of 5
U23A
AMD-218S7EBLA12FG-A12-RH
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
Place close to South Bridge
Chasiss Intrusion
Modify 0829
Place close to device
For EMI
Reserve cystal for A14 to solve the system time lag issue;
Also can connect the 14M from clock gen to 14M_X1
and leace 14M_X2 NC, 1.2V level shift may needed
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
SB700 has an internal 15k PU
Put C308 & C383 Close to B2 pin
PCICLK5/GPIO41 power up default
A11:PCICLK5 A12:GPIO41
MICRO-START INT'L CO.,LTD.
SB700 PCIE/PCI/CPU/LPC
VL390
0A
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R418,R422,R212,R565,R655 may be removed

VCC3

KBRST# R382 1KR0402
SDATA_IN_R R428 10KR0402
SCLK R375 2.2KR0402
SDATA R374 2.2KR0402
SUS_STAT# R565 X_10KR0402
CPU_THRIP# R212 4.7KR0402
LC_SENSE R469 X_10KR0402

VCC3_SB

SCLK1 R427 2.2KR0402
SDATA1 R439 2.2KR0402
RSMRST# R413 10KR0402
RI# R418 10KR0402
SUS_STAT# R424 10KR0402
SB_PWRON# R422 1KR0402
LPC_SMI# R655 X_10KR0402

SB_GPIO5 R377 10KR0402

SB_PWRGD C825 X_C180p50N0402

SCLK C484 X_C22P50N0402
SDATA C483 X_C22P50N0402
SCLK1 C584 X_C22P50N0402
SDATA1 C573 X_C22P50N0402

AZ_BIT_CLK C585 X_C22P50N0402

RN33 8P4R-22R0402
28 AZ_SDOUT — AZ_SDATA_OUT_R
28 AZ_BIT_CLK — AZ_BITCLK_R
28 AZ_SYNC — AZ_SYNC_R
28 AZ_SDIN — SDATA_IN_R
21,28 AZ_RST# — AZ_RST_R
R429 22R0402

VCC3_SB

RN11 8P4R-10KR0402
OC#1
OC#2
OC#3
OC#4
R574 10KR0402 OC#5
R591 10KR0402 OC#6

VCC3_SB VCC3_SB VCC3_SB

R444 X_2.2KR0402
R419 X_2.2KR0402
R420 X_2.2KR0402
SB_TEST2
SB_TEST1
SB_TEST0
R437 X_10KR0402
R417 X_10KR0402
R421 X_10KR0402

NB_PWRGD
A12 Open Drain
A11 Push pull

RSMRST# not de-asserted until at least 10 ms after S5_3.3V is valid.
RSMRST# ramp up time (10% to 90%) ≒ 50 ms

U23D

SB700 Part 4 of 5

31 PCI_PME# — RI# — PCI_PME#/GEVENT4# E1
RI#/EXTEVNT0# E2
30 GFX16_PCIERST# — SLP_S2/GPM9# H7
25,26 SLP_S3# — SLP_S3# F5
26,27 SLP_S5# — SLP_S5# G1
25 SB_PWRON# — SB_PWRON# — PWR_GOOD H2
26 SB_PWRGD — PWR_BTN# H1
SUS_STAT# — SUS_STAT# K3
SB_TEST2 — TEST2 H5
SB_TEST1 — TEST1 H4
SB_TEST0 — TEST0 H3
25 A20GATE — A20GATE — GA20IN/GEVENT0# Y15
25 KBRST# — KBRST# — KBRST#/GEVENT1# W15
25 LPC_PME# — LPC_PME#/GEVENT3# K4
25 LPC_SMI# — LPC_SMI# — LPC_SMI#/EXTEVNT1# K24
27 S3_STATE — S3_STATE — S3_STATE/GEVENT5# F1
12,26,34 FP_RST# — SYS_RESET#/GPM7# J2
24,30 WAKE# — WAKE#/GEVENT8# H6
BLINK/GPM6# F2
7 CPU_THRIP# — CPU_THRIP# — SMBALERT#/THRMTRIP#/GEVENT2# J6
26 WD_PWRGD — WD_PWRGD — NB_PWRGD W14
25 IO_RSMRST# — IO_RSMRST# R412 0R0402 RSMRST# — RSMRST# D3
C547 X_C1000P50X0402

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC C8 USB_48M_CLK — USB_48M_CLK 12
USB_RCOMP G8 USB_RCOMP R409 11.8KR1%0402

USB MISC

USB_48M_CLK
C536
C22P50N0402
Place close to SB

USB 1.1

USB_FSDP13+ E6
USB_FSDM13- E7
USB_FSDP12+ E7
USB_FSDM12- E8
USB_HSDP11+ H11
USB_HSDM11- J10
USB_HSDP10+ E11
USB_HSDM10- F11

USB 2.0

USB_HSDP9+ A11 — USB9+ 29
USB_HSDM9- B11 — USB9- 29
USB_HSDP8+ C10 — USB8+ 29
USB_HSDM8- D10 — USB8- 29
USB_HSDP7+ G11 — USB7+ 29
USB_HSDM7- H12 — USB7- 29
USB_HSDP6+ E12 — USB6+ 29
USB_HSDM6- E14 — USB6- 29
USB_HSDP5+ C12 — USB5+ 29
USB_HSDM5- D12 — USB5- 29
USB_HSDP4+ B12 — USB4+ 29
USB_HSDM4- A12 — USB4- 29
USB_HSDP3+ G12 — USB3+ 29
USB_HSDM3- G14 — USB3- 29
USB_HSDP2+ H14 — USB2+ 29
USB_HSDM2- H15 — USB2- 29
USB_HSDP1+ A13 — USB1+ 29
USB_HSDM1- B13 — USB1- 29
USB_HSDP0+ B14 — USB0+ 29
USB_HSDM0- A14 — USB0- 29

USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 STACK4 USB4
USB4 STACK4 USB3
USB3 STACK4 USB2
USB2 STACK4 USB1
USB1 LAN USB BOTTOM
USB0 LAN USB TOP

SATA_IS0#/GPIO10 AE18
CLK_REQ3#/SATA_IS1#/GPIO6 AD18
7 CPU_PRESENT# — R522 0R0402 — SMARTVOLT/SATA_IS2#/GPIO4 AA19
CLK_REQ0#/SATA_IS3#/GPIO0 W17
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39 V17
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40 W20
34 SPKR — SPKR/GPIO2 W21
10,11,12,26 SCLK — SCLK — SCL0/GPOC0# AA18
10,11,12,26 SDATA — SDATA — SDA0/GPOC1# W18
24,30,31,32 SCLK1 — SCLK1 — SCL1/GPOC2# K1
24,30,31,32 SDATA1 — SDATA1 — SDA1/GPOC3# K2
DDC1_SCL/GPIO9 AA20
19 SPI_WP# — DDC1_SDA/GPIO8 Y18
LC_SENSE — LLB#/GPIO66 C1
SB_GPIO5 — SHUTDOWN#/GPIO5 Y19
DDR3_RST#/GEVENT7# G5

GPIO

TP34
OC#6 — USB_OC6#/IR_TX1/GEVENT6# B9
USB_OC5#/IR_TX0/GPM5# B8
29 OC#5 — USB_OC4#/IR_RX0/GPM4# A8
29 OC#4 — USB_OC3#/IR_RX1/GPM3# A9
29 OC#3 — USB_OC2#/GPM2# E5
29 OC#2 — USB_OC1#/GPM1# F8
29 OC#1 — USB_OC0#/GPM0# E4

USB OC

AZ_BITCLK_R — AZ_BITCLK M1
AZ_SDATA_OUT_R — AZ_SDOUT M2
SDATA_IN_R — AZ_SDIN0/GPIO42 J7
AZ_SDIN1/GPIO43 J8
AZ_SDIN2/GPIO44 L8
AZ_SDIN3/GPIO46 M3
AZ_SYNC_R — AZ_SYNC I6
AZ_RST_R — AZ_RST# M4
AZ_DOCK_RST#/GPM8# L5

HD AUDIO

KSO_16/EC_GPIO8 A18 — GPIO8
KSO_17/EC_GPIO9 B18 — ISOLATEBR — 24 R360 10KR0402 R367 10KR0402
EC_PWM0/EC_GPIO10 F21
SCL2/EC_GPIO11 D21
SDA2/EC_GPIO12 F19
SCL3_LV/EC_GPIO13 E20
SDA3_LV/EC_GPIO14 F21
EC_PWM1/EC_GPIO15 E19
EC_PWM2/EC_GPIO16 D19 — SB_GP16 21
EC_PWM3/EC_GPO17 E18 — SB_GP17 21

STRAP pin to define use LPC or SPI ROM

VCC3_SB
VCC3
R361 X_10KR0402
R941 X_0R0402
GPIO8
DSM_GPO# 24

Add 0902

KSI_0/EC_GPIO18 G20
KSI_1/EC_GPIO19 G21
KSI_2/EC_GPIO20 D25
KSI_3/EC_GPIO21 D24
KSI_4/EC_GPIO22 C25
KSI_5/EC_GPIO23 C24
KSI_6/EC_GPIO24 B25
KSI_7/EC_GPIO25 C23

KSO_0/EC_GPIO26 B24
KSO_1/EC_GPIO27 B23
KSO_2/EC_GPIO28 A23
KSO_3/EC_GPIO29 C22
KSO_4/EC_GPIO30 A22
KSO_5/EC_GPIO31 B22
KSO_6/EC_GPIO32 B21
KSO_7/EC_GPIO33 A21
KSO_8/EC_GPIO34 D20
KSO_9/EC_GPIO35 C20
KSO_10/EC_GPIO36 A20
KSO_11/EC_GPIO37 B20
KSO_12/EC_GPIO38 B19
KSO_13/EC_GPIO39 A19
KSO_14/EC_GPIO40 D18
KSO_15/EC_GPIO41 C18

EMBEDDED CTRL

H19 PS2_DAT/EC_GPIO0
H20 PS2_CLK/EC_GPIO1
H21 SPI_CS2#/EC_GPIO2
F25 IDE_RST#/F_RST#/EC_GPO3
D22 PS2KB_DAT/EC_GPIO4
E24 PS2KB_CLK/EC_GPIO5
E25 PS2M_DAT/EC_GPIO6
D23 PS2M_CLK/EC_GPIO7

EMBEDDED CTRL

AMD-218S7EBLA12FG-A12-RH

TP145 — USB_48M_CLK

MSI MICRO-START INT'L CO.,LTD.

Title: SB700 ACPI/GPIO/USB/AUDIO

Size: Custom | Document Number: VL390 | Rev: 0A

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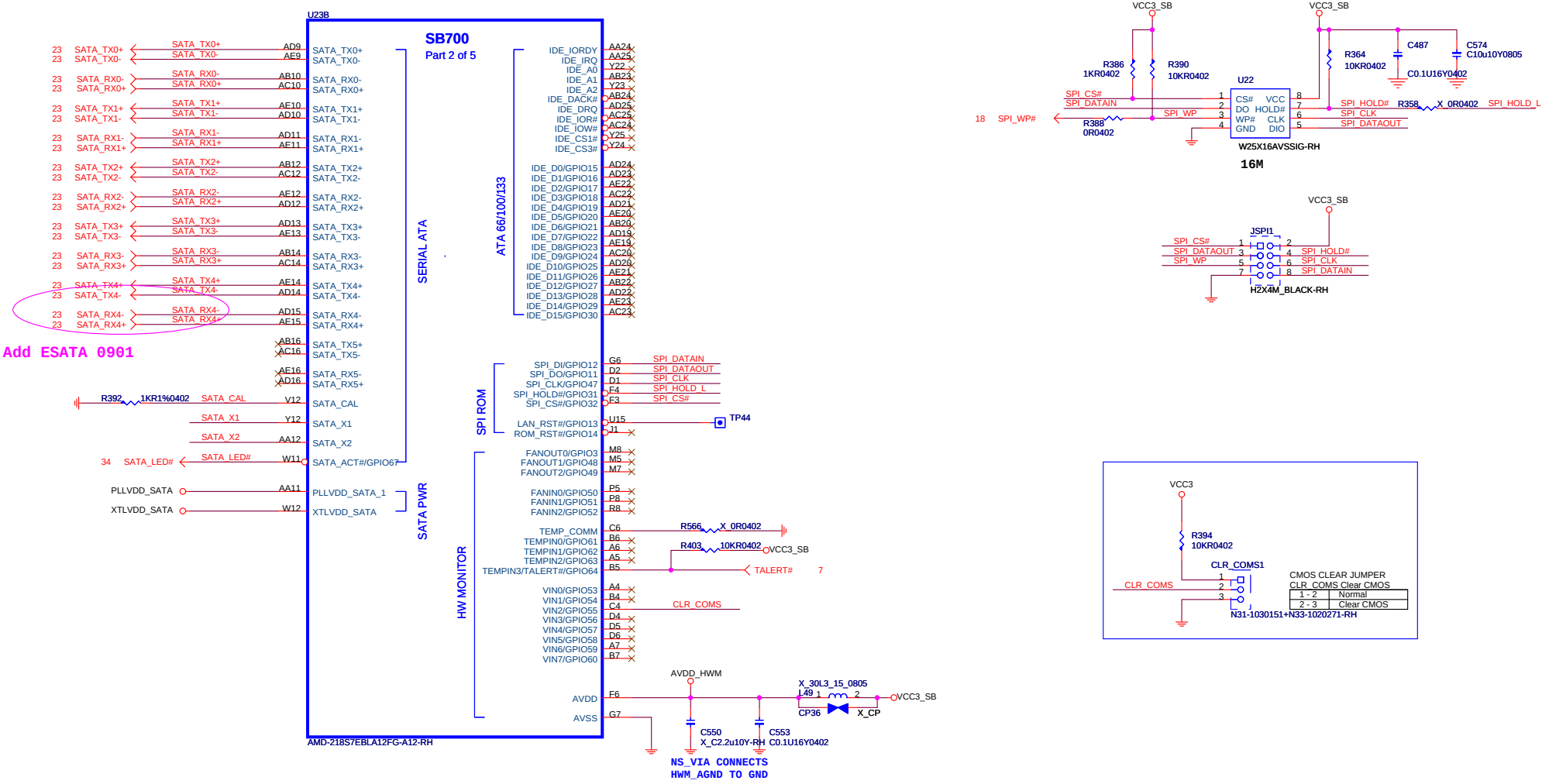

MICRO-START INT'L CO.,LTD.

Title: SB600 SATA/IDE/HWM/SPI

Size	Document Number	Rev
Custom	VL390	0A

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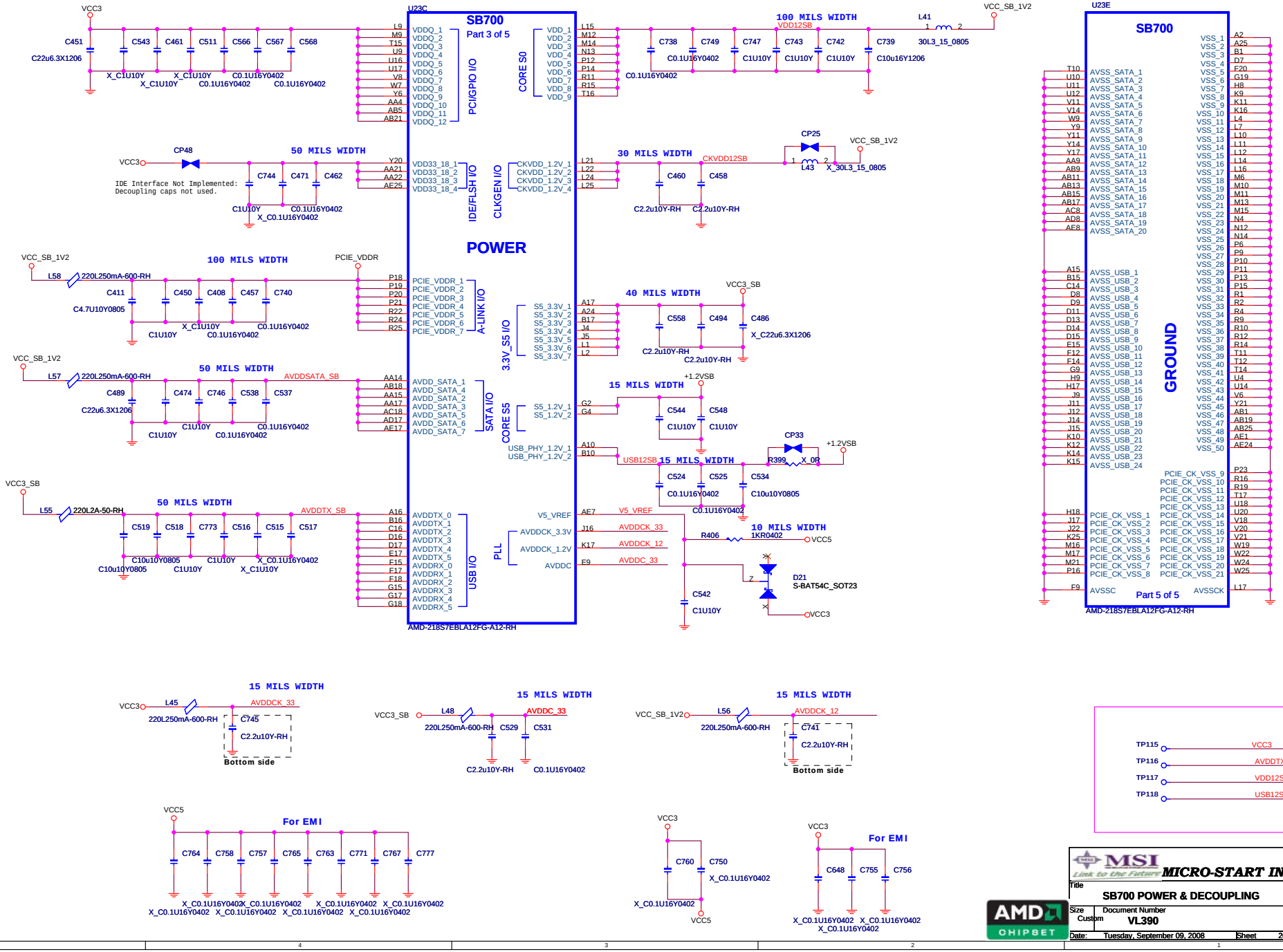
SB700
Part 3 of 5
POWER
AMD-218S7EBLA12FG-A12-RH
SB700
GROUND
Part 5 of 5
AMD-218S7EBLA12FG-A12-RH
100 MILS WIDTH
50 MILS WIDTH
30 MILS WIDTH
40 MILS WIDTH
15 MILS WIDTH
10 MILS WIDTH
For EMI
Bottom side
IDE Interface Not Implemented:
Decoupling caps not used.
MICRO-START INT'L CO.,LTD.
SB700 POWER & DECOUPLING
VL390
0A
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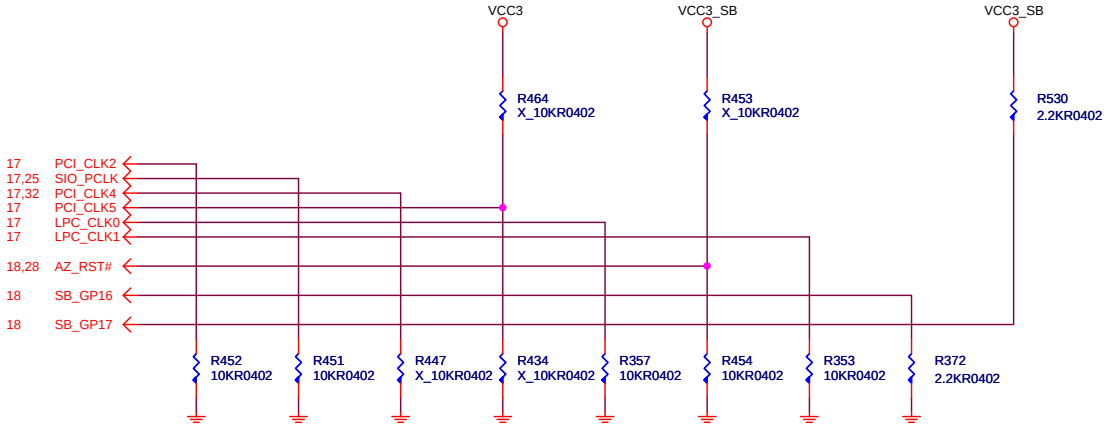
REQUIRED STRAPS



	PCI_CLK2	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	ENABLE PCI MEM BOOT (A11) IMC ENABLED (A12)	Internal Clock Generator	INTERNAL RTC	IMC ENABLED (A11) ENABLE PCI MEM BOOT (A12)	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED	
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT	

MSI Link to the Future MICRO-START INT'L CO.,LTD.

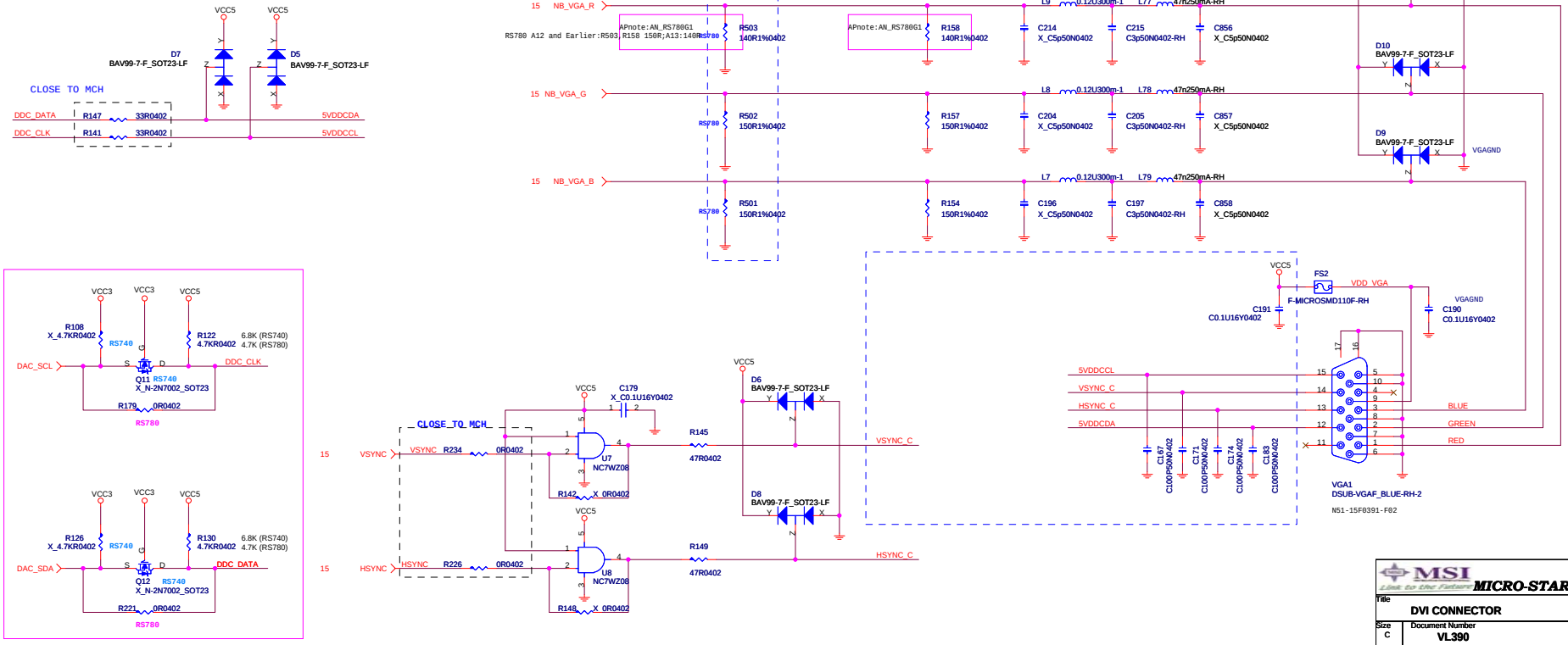
Title: SB700 STRAPS

Size: B | Document Number: VL390 | Rev: 0A

Date: Tuesday, September 09, 2008 | Sheet 21 of 37

AMD CHIPSET

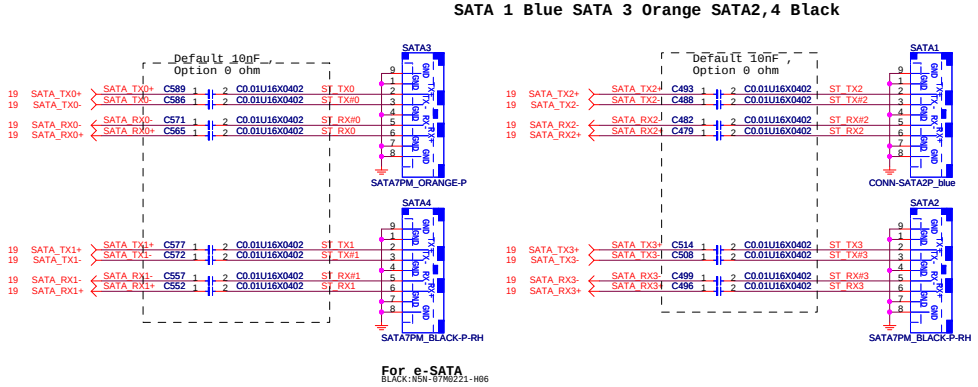
VGA CONNECTOR



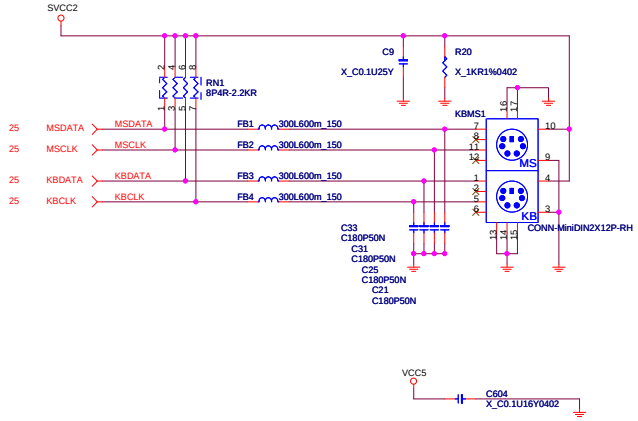
Title	DVI CONNECTOR
Size	C
Document Number	VL390
Rev	0A
Date	Tuesday, September 09, 2008
Sheet	22 of 37

MSI MICRO-STAR INT'L CO.,LTD.

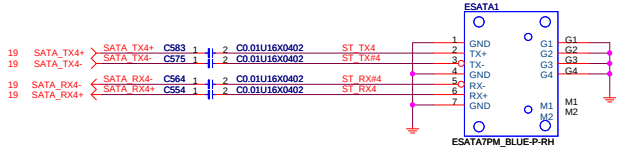
SERIAL ATA CONNECTOR BLOCK



PS2 KEYBOARD & MOUSE CONNECTOR

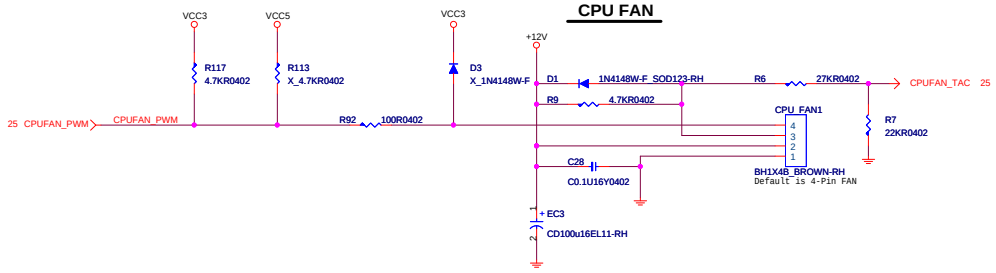


ESATA

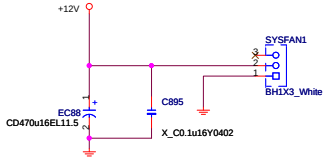


PWM FAN CONTROL

CPU FAN



SYSTEM FAN



MSI MICRO-STAR INT'L CO.,LTD.

Title: SATA & COM1 & LPT

Size	Document Number	Rev
C	VL390	0A

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CHOKE10 close to
U30 Pin 1 within 0.5cm

R668 Place near
Pin64 of U30

2.49k for 8111CP ?

Pay attention to the This Pin

C862 , C863
CLOSE TO CHOKE1

MDIx+/-
Reference to GND plan.

C864 use 0.01uF
for better EMI performace.

B06-8111C3C-R09

RTL8111CP-VB-GR

BIOS pull high/low on Pin36
ISOLATE to leave/enter DSM.

4K/93C66/10ms-SOIC8

8111CP uses 93C66 and keep R607

Left => YELLOW

Right => Orange / Green

N58-22F0181-F02

MICRO-START INT'L CO.,LTD.	
Title	LAN 8111CP
Size: Custom	Document Number: VL390
Rev	0A
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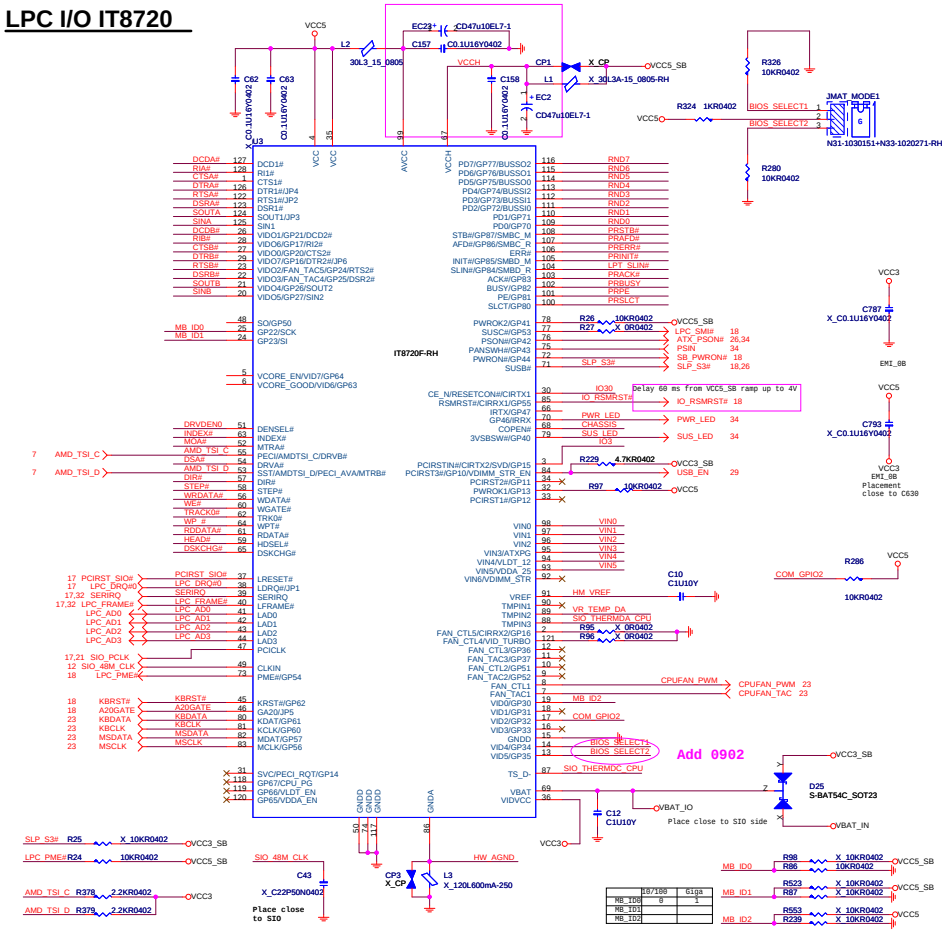
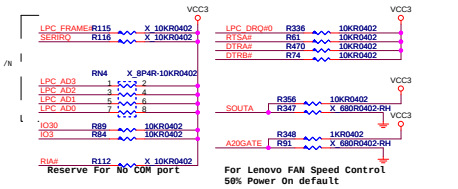
LPC I/O IT8720



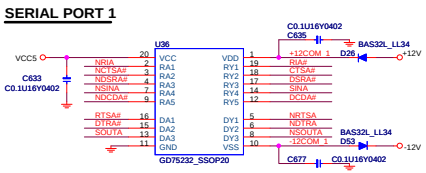
SUPER I/O STRAPPING RESISTOR



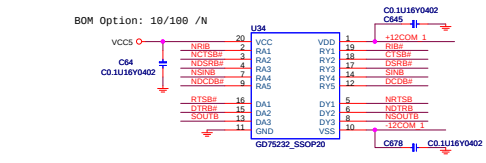
Power On Strapping Options

Symbol	PIN	value	Description
Flashsel1_EN (LPC_DRQ#0)	38	1	Disabled.
		0	Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
VIDO_EN (RTSA#)	122	1	Disable VIDOUT pins(except VID06 & VID07)
		0	Enable VIDOUT pins
CHIP SEL (SOUTA)	124	--	Chip selection in configuration.
K8PWR_EN (DTRA#)	126	1	K8 POWER SEQUENCE FUNCION IS DISABLED
		0	K8 POWER SEQUENCE FUNCION IS ENABLED
FAN_CTL SEL (SOUTA/A20GATE)	124/46	11	The default value of EC Index 15h / 16h / 17h is 40h (50%)
		10	The default value of EC Index 15h / 16h / 17h is 7Fh(Fan off)
		01	The default value of EC Index 15h / 16h / 17h is 00h(Fan full speed)
		00	The default value of EC Index 15h / 16h / 17h is 20h(75%)
SVID_EN (DTRB#)	29	1	Parallel VIDOutput(Only for Parallel VID input)
		0	Serial VIDOutput(Only for Parallel VID input)
WDT_EN (A20GATE)	46	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK

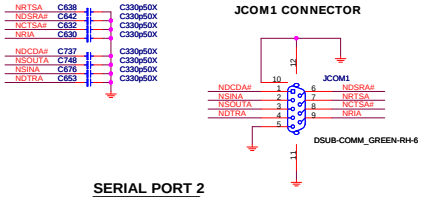
SERIAL PORT 1



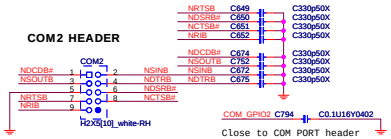
SERIAL PORT 2



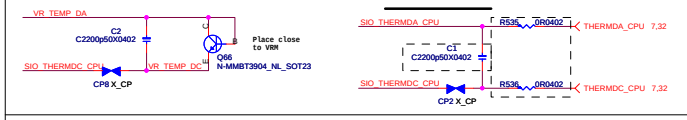
JCOM1 CONNECTOR



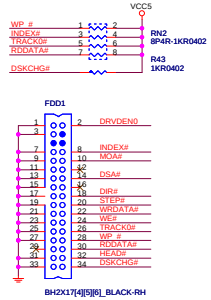
COM2 HEADER



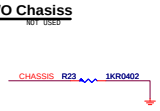
TEMP SENSOR



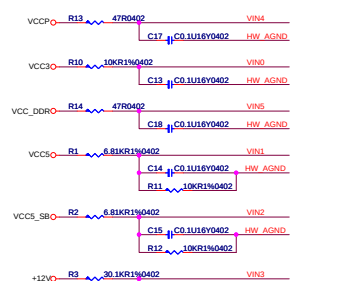
FLOPPY CONNECTOR

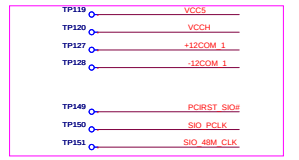


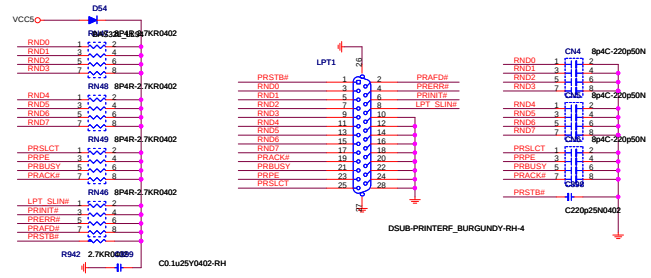
Super I/O Chasiss



Thermal Resistor







Title	LPC I/O IT8720	
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MSI — MICRO-STAR INT'L CO.,LTD.

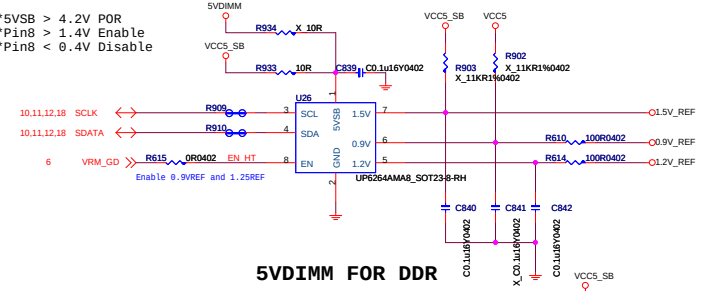
LPC_DRQ#0

REFERENCE VOLTAGE

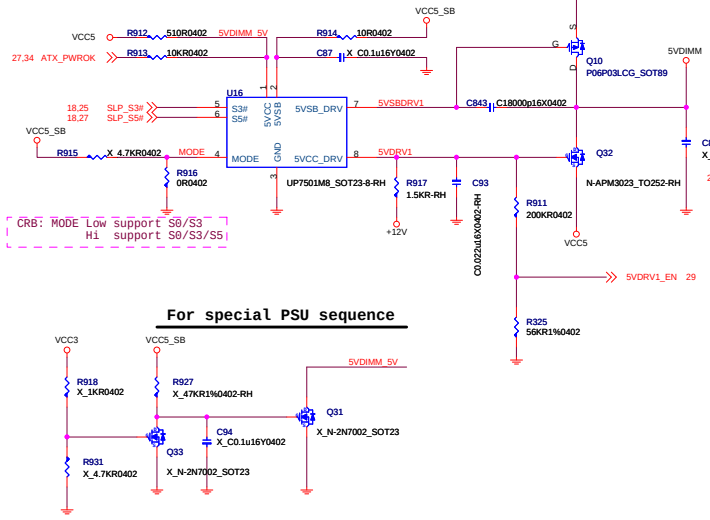
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS

*5VSB > 4.2V POR
*Pin8 > 1.4V Enable
*Pin8 < 0.4V Disable

???NEW rev UPI/uP6264BMA8 I34-0626419-U33 ???

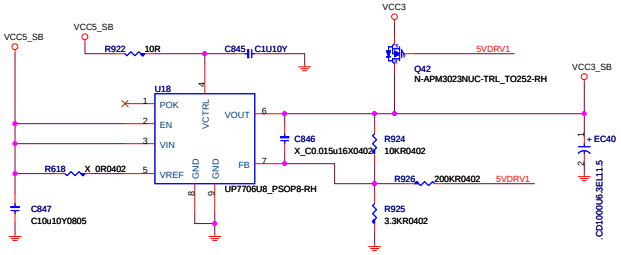


5VDIMM FOR DDR



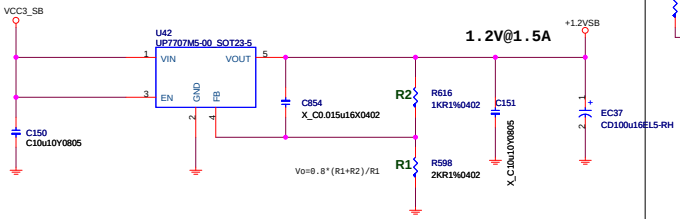
For special PSU sequence

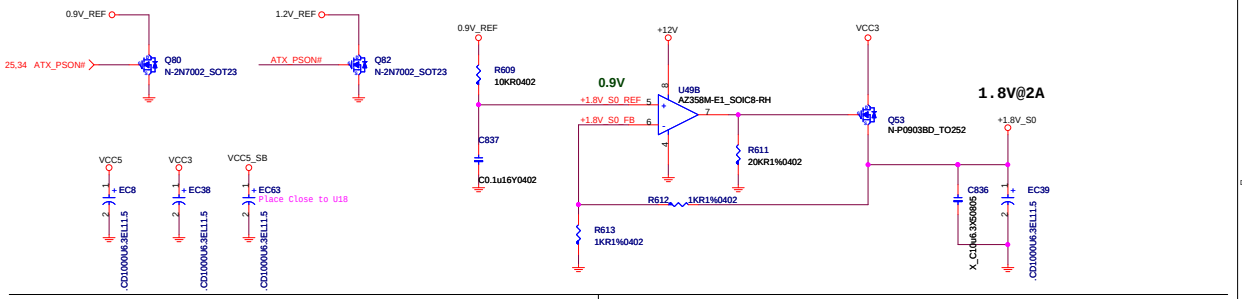
3VDUAL POWER



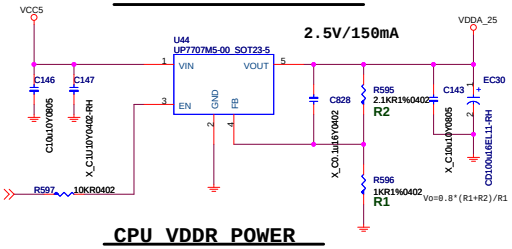
1.2VDUAL POWER

For SB +1.2V_SUS Power Rail

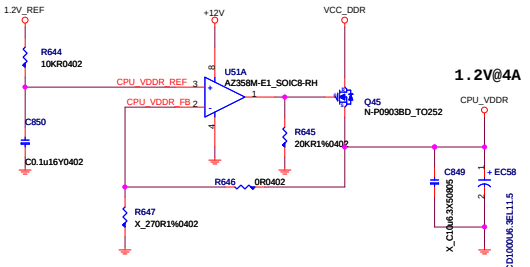




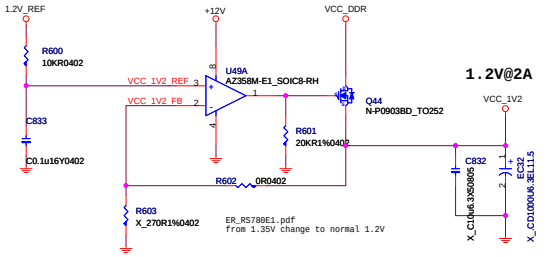
CPU VDDA_25 POWER



CPU VDDR POWER

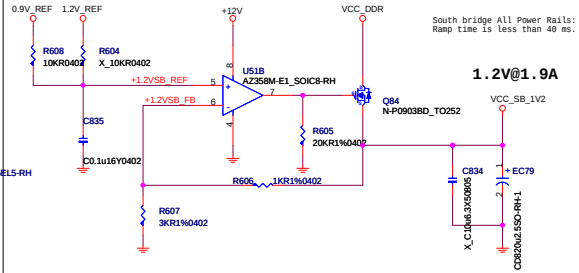


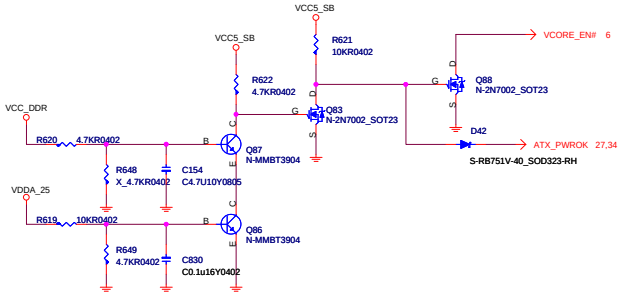
VCC_1V2 POWER



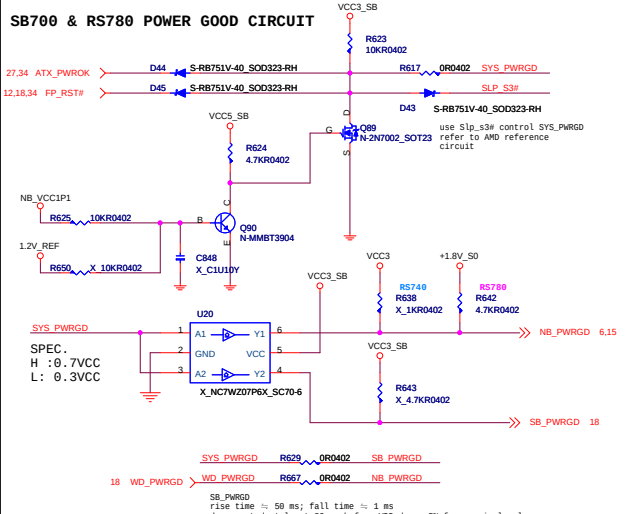
VCC_SB_1V2 POWER

For SB +1.2V_S5 Power Rail

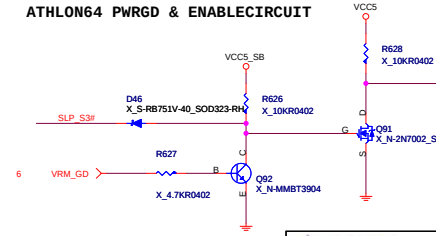




SB700 & RS780 POWER GOOD CIRCUIT



ATHLON64 PWRGD & ENABLECIRCUIT



MSI Link to the Future
MICRO-START INT'L CO.,LTD.

Title: ACPI Controller UPI

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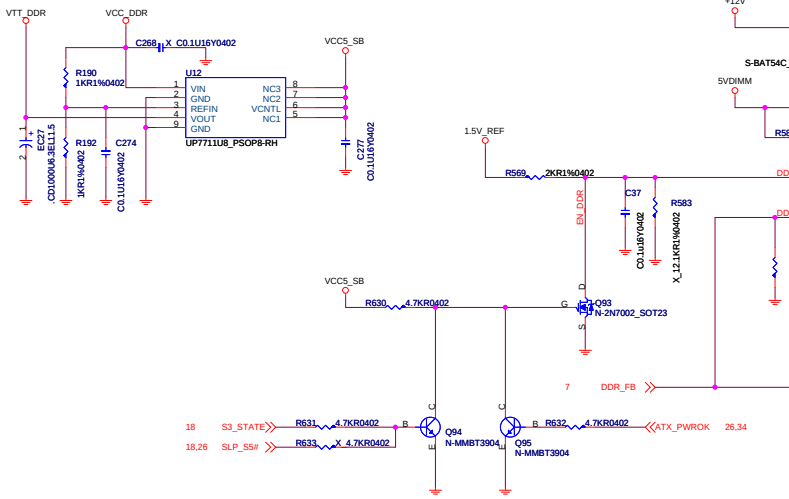
VTT_DDR POWER

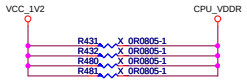
0.75V@2A



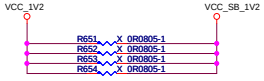
DDR III 1.5V POWER

1.5V@10A+10A

Combining VLDT and VDDR For cost down ;
All capacitors for VLDT and VDDR must be included

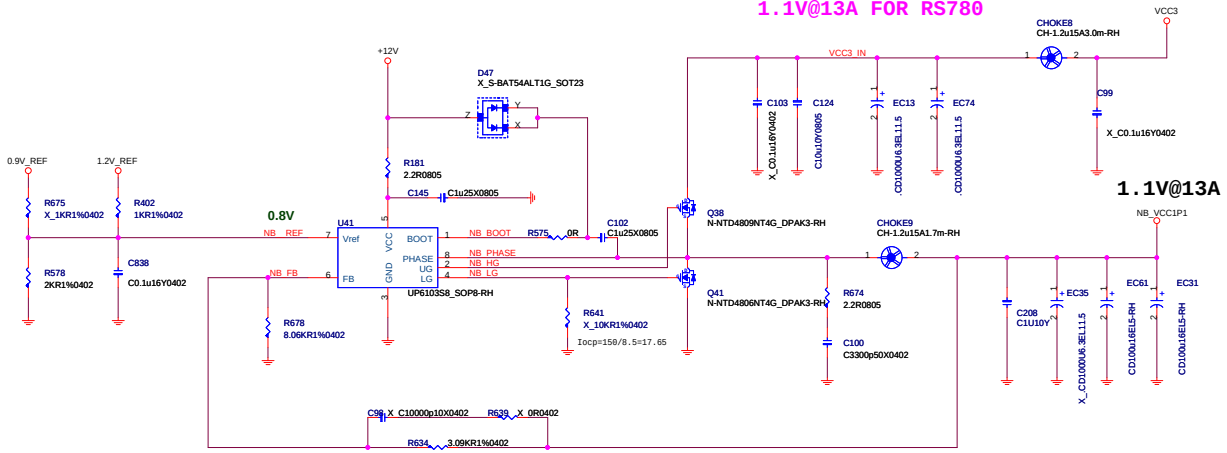


Combining VCC_1V2 andVCC_SB_1V2 For cost down



NB_VCC1P1 POWER

1.1V@13A FOR RS780

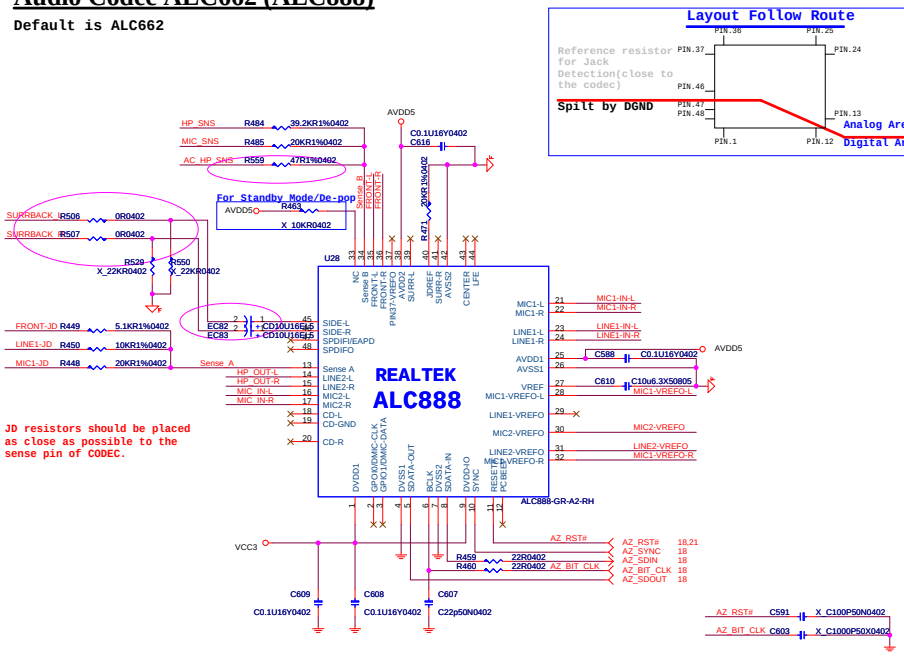


1.1V@13A

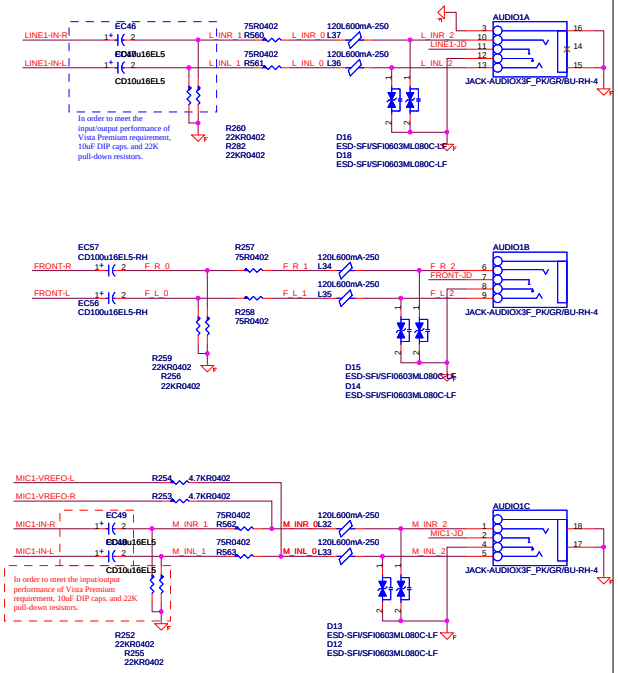
MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: NB Core Power & DDR Power		
Size: Custom	Document Number: VL390	Rev: 0A
Date: Tuesday, September 09, 2008	Sheet 27 of 37	

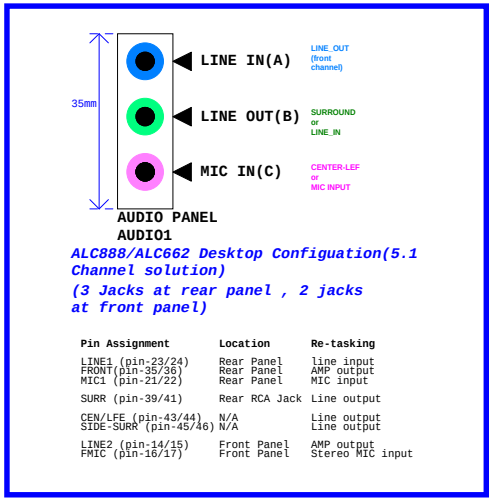
Audio Codec ALC662 (ALC888)

Default is ALC662



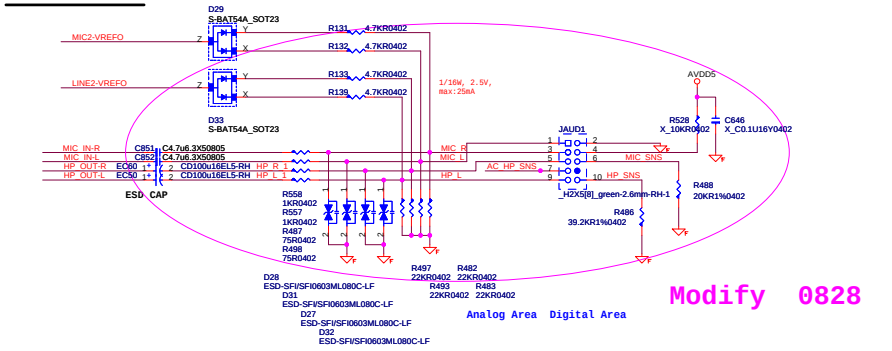
Rear Phone Jack



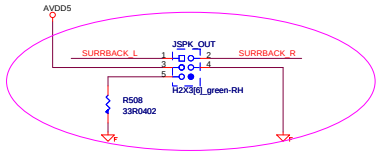


Pin Assignment	Location	Re-tasking
LINE1 (pin-23/24)	Rear Panel	line input
FRONT(pin-35/36)	Rear Panel	AMP output
MIC1 (pin-21/22)	Rear Panel	MIC input
SURR (pin-39/41)	Rear RCA Jack	Line output
CEN/LFE (pin-43/44)	N/A	Line output
SIDE-SURR (pin-45/46)	N/A	Line output
LINE2 (pin-14/15)	Front Panel	AMP output
FMIC (pin-16/17)	Front Panel	Stereo MIC input

Front Audio Jack

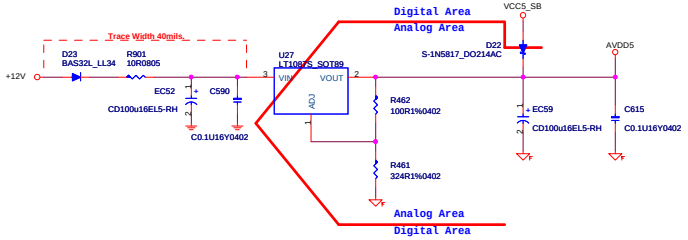


JSPK_OUT HEADER

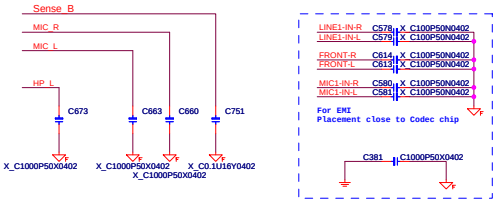


c610 change to X5R;C591 leave empty;R449 change to 1%
EC61,EC62 change to C851,C8524.7uX5R;R557,R558 change to 1KR;
D33,,R139,R133,R482,R483 leave empty;
R253,R254 change to 4.7KR and connect to M_INR_0/M_INL_0;
R256,R259 connect to F_R_0/F_L_0

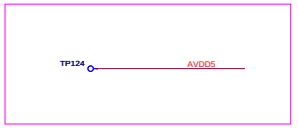
Audio Power



EMI



Tied at one point only under the codec or near the codec

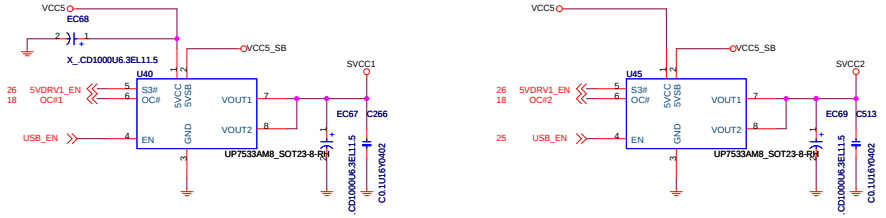


MSI MICRO-START INTL CO.,LTD.

Title	ALC888	
Size: Custom	Document Number: VL390	Rev: 0A
Date: Tuesday, September 09, 2008	Sheet 28 of 37	

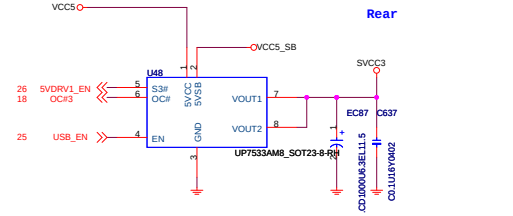
POWER CIRCUIT FOR USB PORT 2,3,4,5

Rear



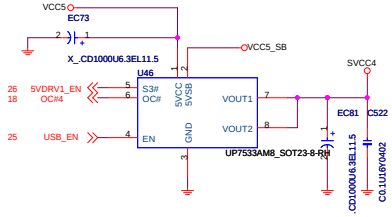
POWER CIRCUIT FOR USB PORT 0,1

Rear



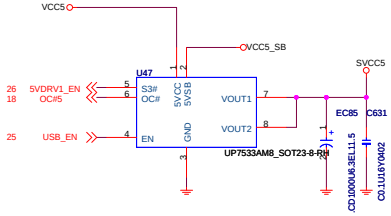
POWER CIRCUIT FOR USB PORT 6,7

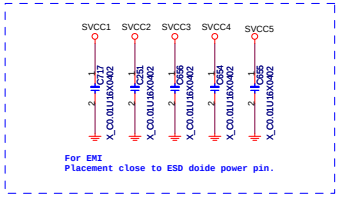
Front



POWER CIRCUIT FOR USB PORT 8,9

Front

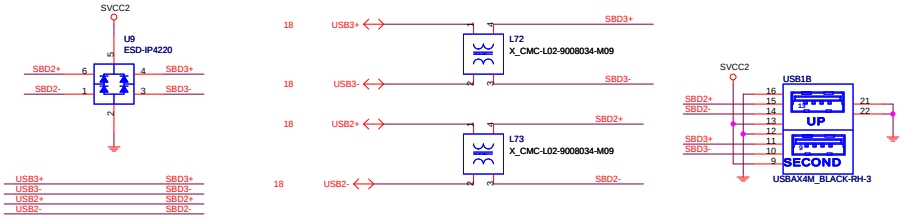


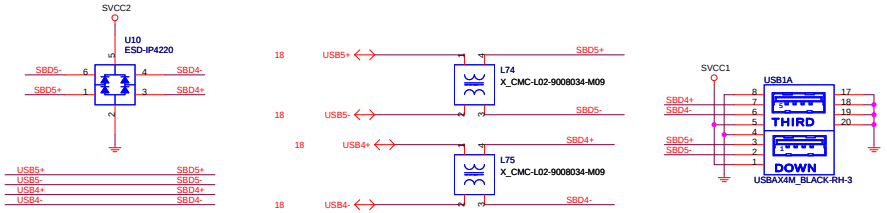


REAR PANEL USB CONNECTOR FOR USB PORT 2,3,4,5

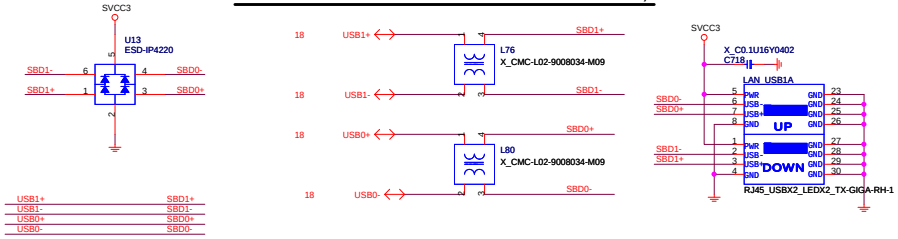
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22





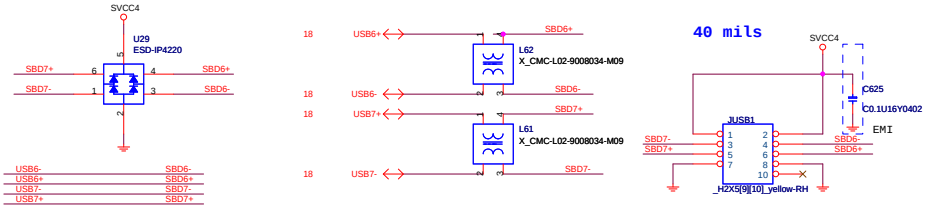
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

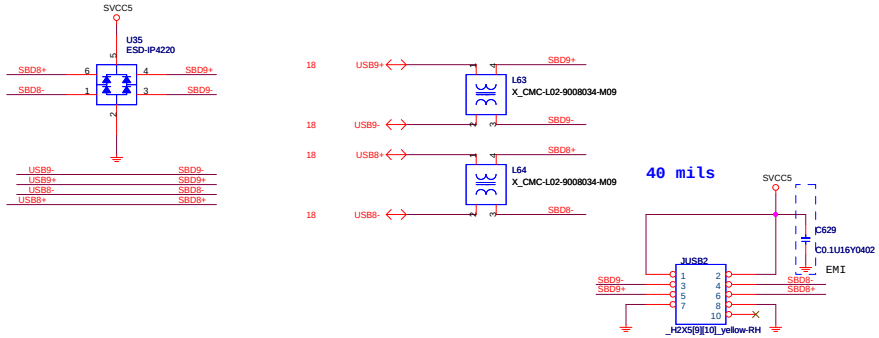
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22



Modify USB Pinhead

USB CARD READER + IR MODULE FOR USB PORT 8,9



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Title	USB CONNECTORS	
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PCI Express Slot x16/x1

PCI EXPRESS x16 Slot

PCI EXPRESS 1 Slot-1

Modify 0901

From Clock Gen

SLOT-PCI164P_BLACK-2PITCH-RH-13

SLOT-PCI36_WHITE-2PITCH-RH-4

Placement Between at PCIE_X1

Placement Close To PCIE16_X1

Connected to A_RST# ANDed with Southbridge GPIO (S5 domain).

U54 NC7SZ08M5X_SOT23-5-RH

Q110 N-2N7002_SOT23

MICRO-START INT'L CO.,LTD.

Title	PCI EXPRESS X16 & X1 SLOT	
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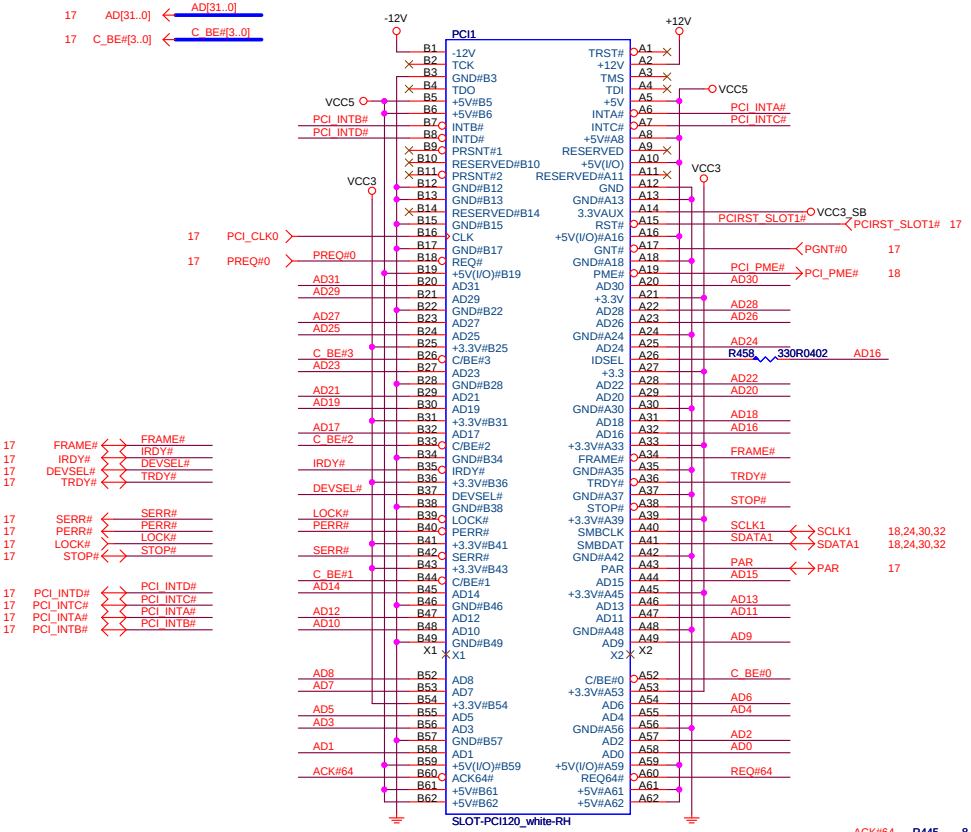
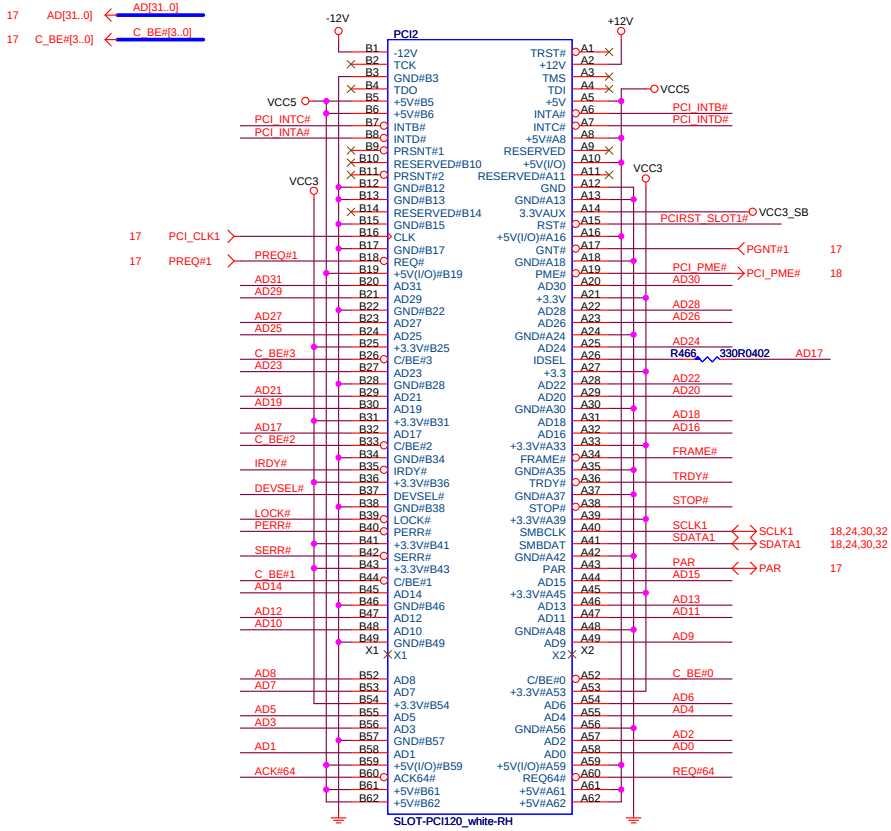
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



PCI SLOT 2 (PCI VER: 2.3 COMPLY)

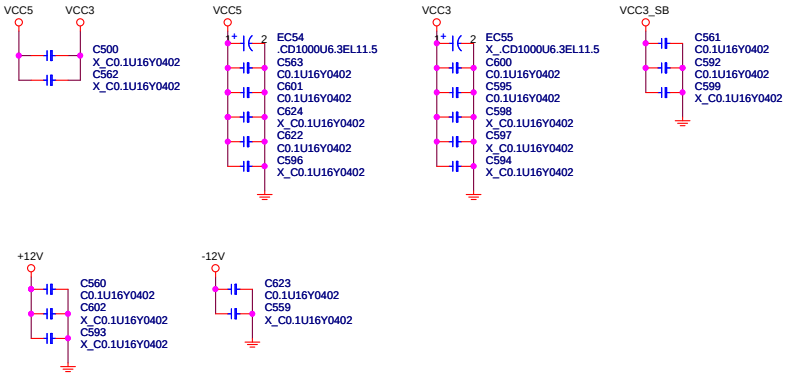


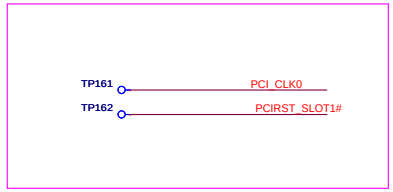
PCI PULL-UP / DOWN RESISTORS

IDSEL = AD16
MASTER = PREQ#0
PCI_INT A, B, C, D

IDSEL = AD17
MASTER = PREQ#1
PCI_INT B, C, D, A

PCI SLOT DECOUPLING CAPACITORS





MICRO-START INT'L CO.,LTD.

Title: PCI SLOT 1		
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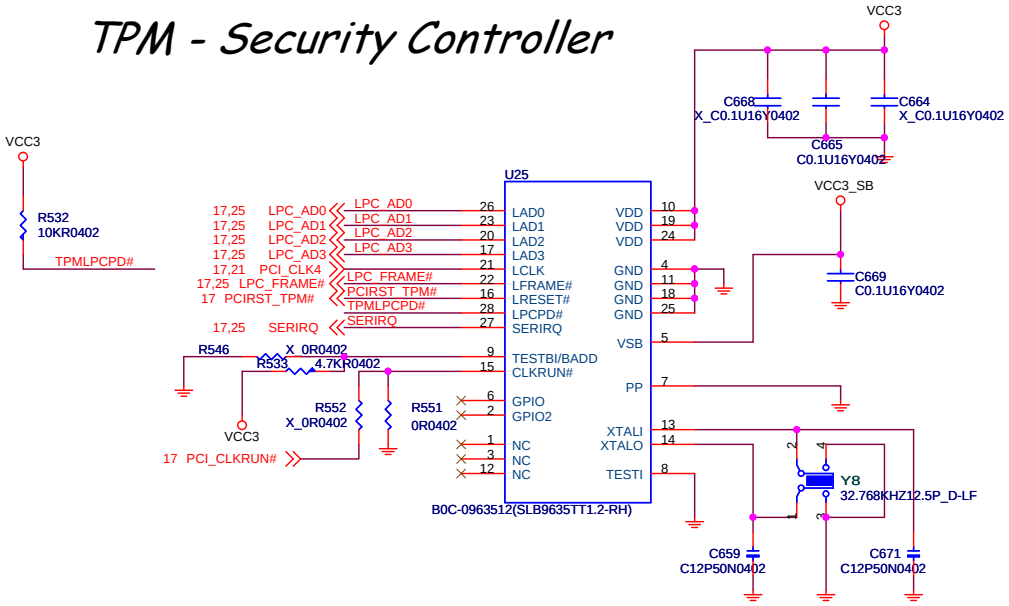
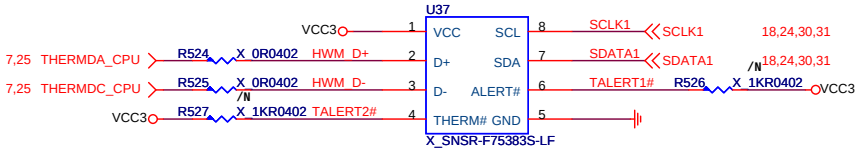
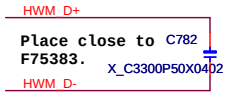
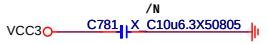
TPM - Security Controller

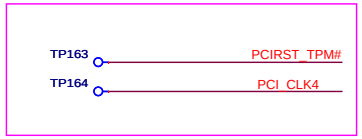


CPU Thermo Sense









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Title: TMP/Asset ID/HWM W83201G		
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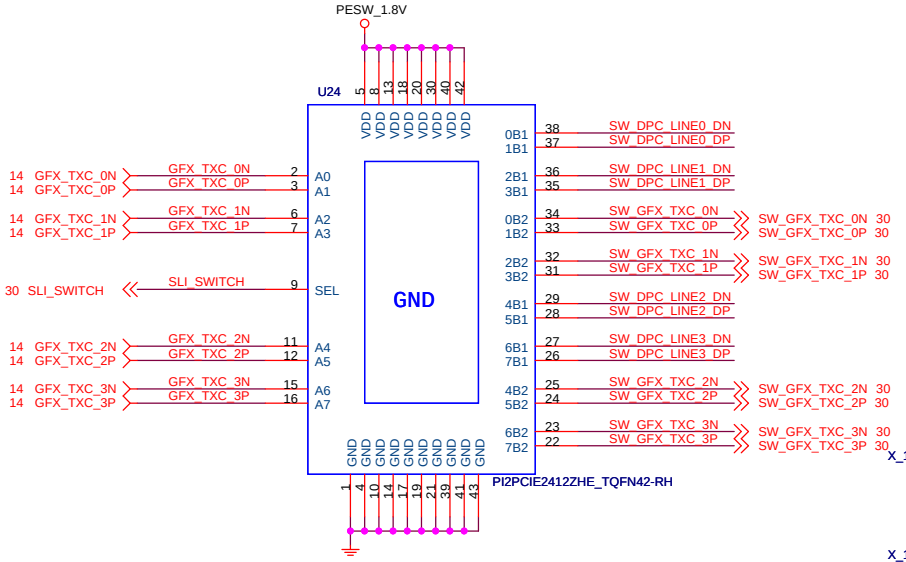
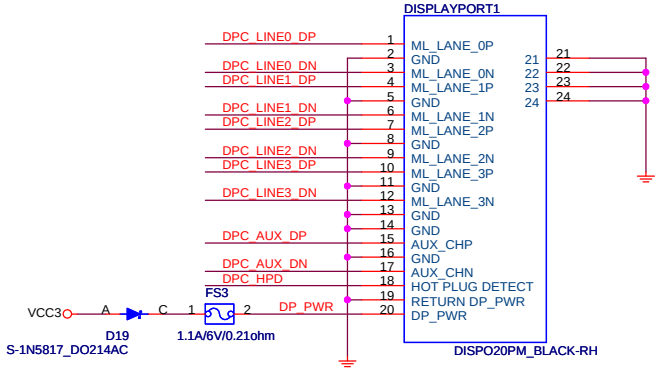
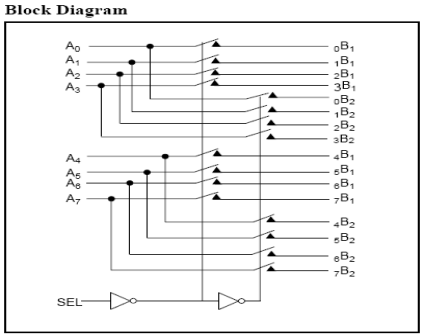


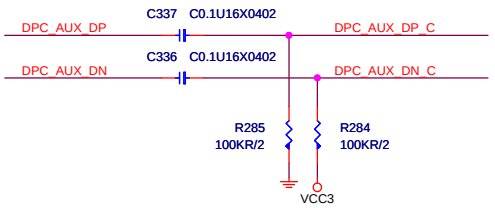


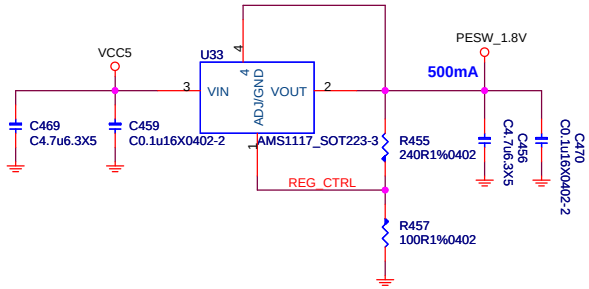


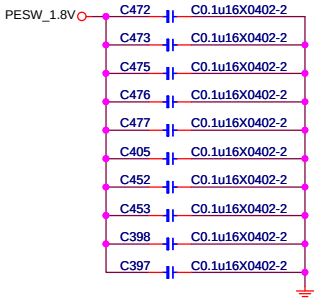
Truth Table

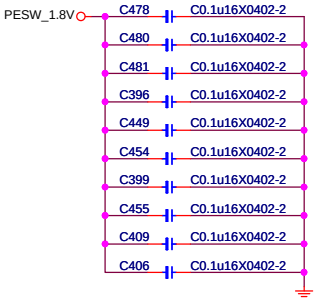
Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

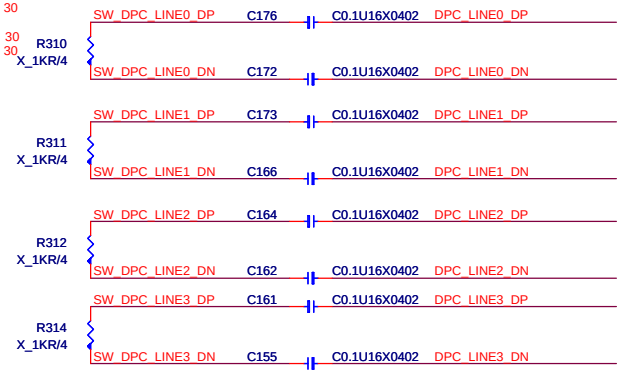
Switch circuit for secondary displayport

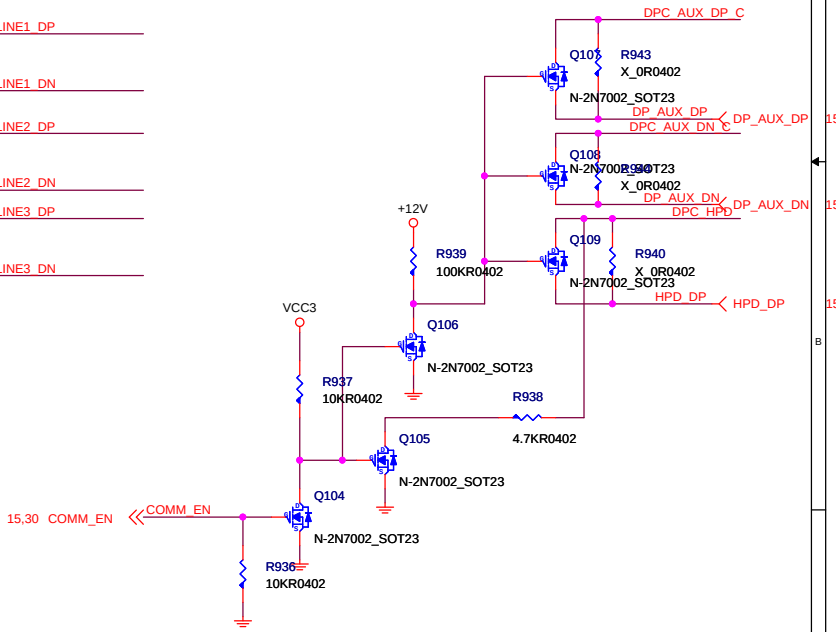












Title	<Title>		
Size: Custom<Doc>	Document Number		Rev: <RevCode>
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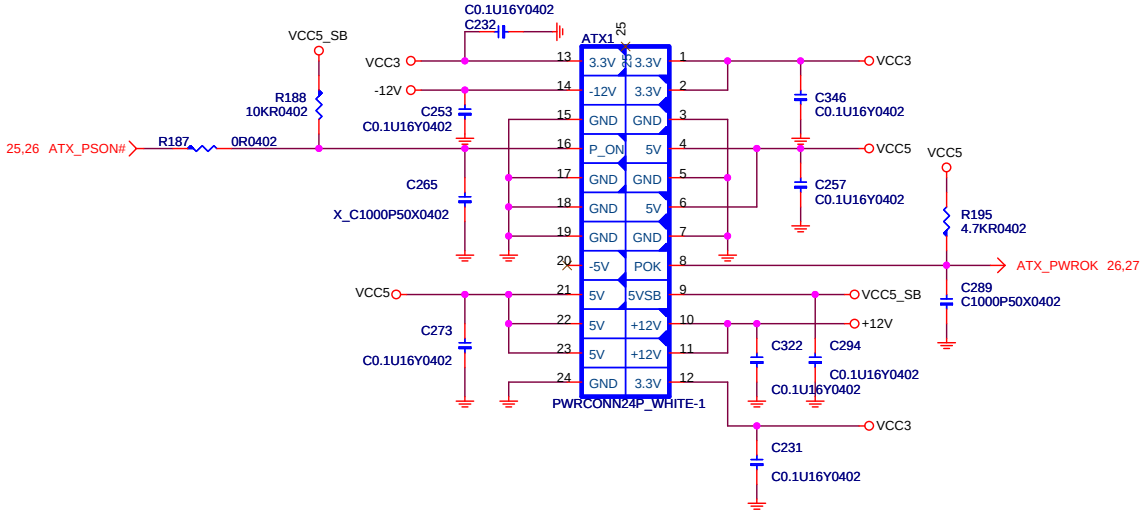
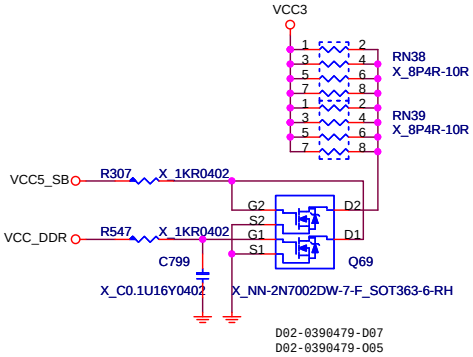
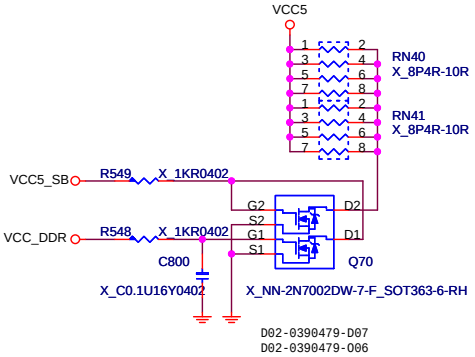
ATX CONNECTOR

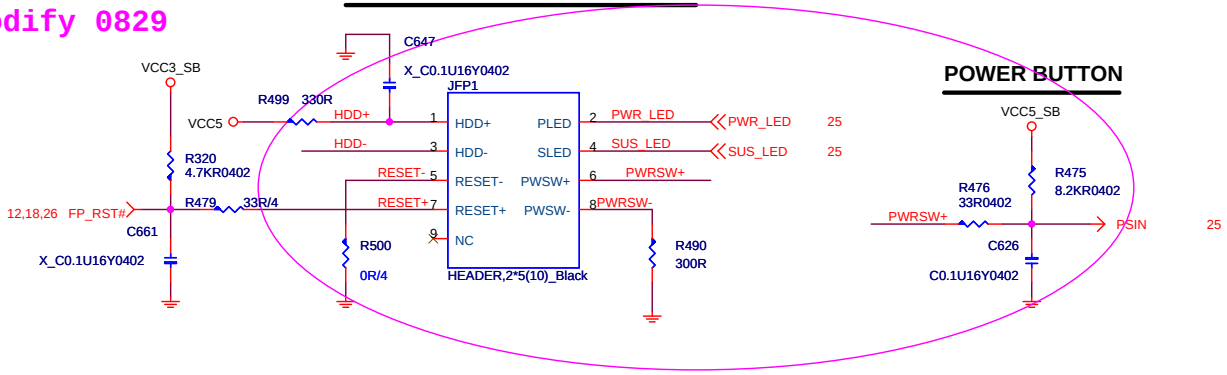






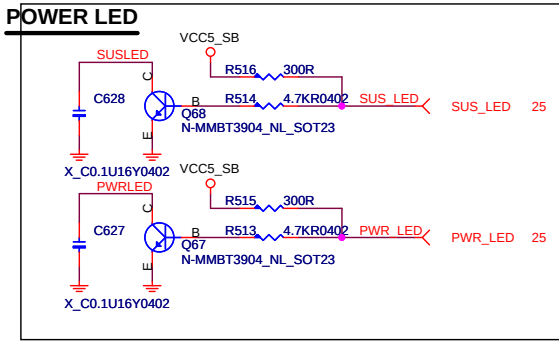
Modify 0829

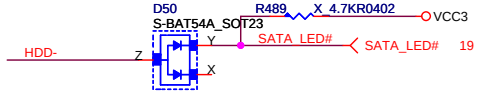
NEC Front Panel Connector



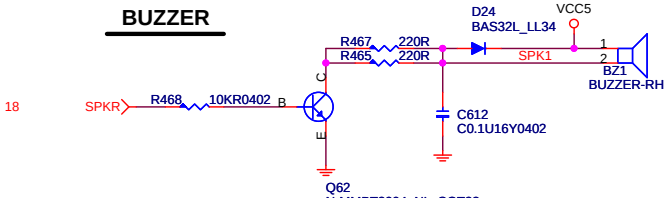
POWER BUTTON

POWER LED





BUZZER



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: ATX & FRONT PANEL		
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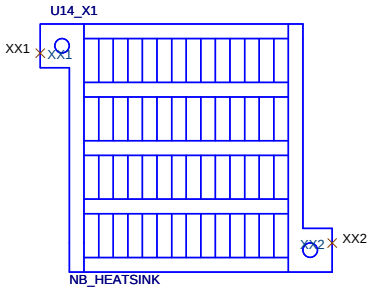
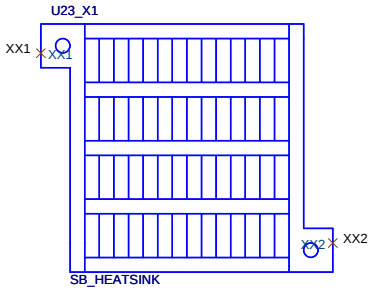
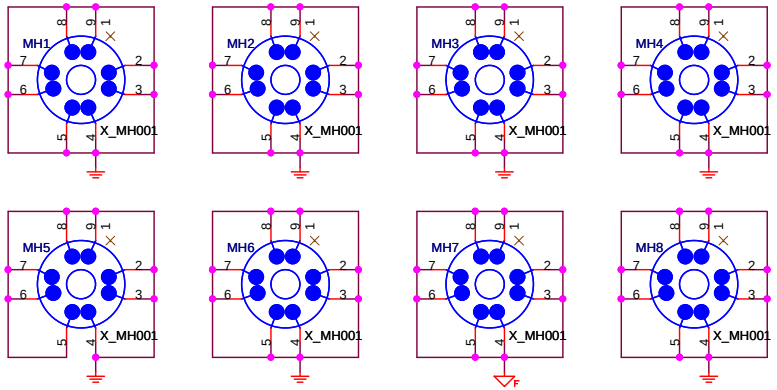
HEAT SINK







MANUAL PART

AVL:
D06-0100161-F52
D06-0100101-P01

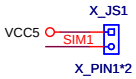
BAT1_X1
BAT-BCR2032P-RH

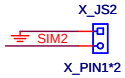
PCB1

P30-073890A-E48
P30-073890A-G37
P30-073890B-E48
P30-073890B-G37
P30-073890C-E48
P30-073890C-G37

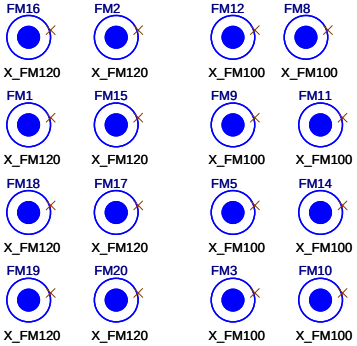
P30-0737711-E48

Simulation





Optics Orientation Holes



MSI MICRO-START INT'L CO.,LTD.
Link to the Future

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MODIFY HISTORY

1,(page 7,8,9)change to AM3 socket :(Have to apply AM3 library and footprint)
  (1) add pin B2 as NP/RSVD
  (2) change pin F3 from RSVD to M_VDDIO_PWRGD
  (3) change pin W30 from RSVD to MA_EVENT#
  (4) change pin V29 from RSVD to MB_EVENT#
  (5) change pin A12,B12,C12,D12,AG12,AH12,AJ12,AK12,AL12 from VTT to VDDR
  (6) change pin H20, AE7 to NP/VSS
  (7) remove pin H3, H4, H21, H22, AD18, AD19, AE8, AE9
  (8) change pin F2 from PLATFORM_TYPE to RSVD

2,(page 7)
  (1) CPU_CORE_TYPE PU reister change to 1KR refer to CRB
  (2) Reserve R567 300R to cnnetct TEST22 to GND
  (3) Reserve R240,R247,R249,R281,R294 HDT PU resisters
  (4) Reserve C801,C802,C803
  (5) Reserve R442,R599 for RS740 HT1.0

3,(page 8,9) change to DDR3
  (1) W26,W25 change to MEM_MA1_CLK0;U24,V24 change to MEM_MA0_CLK1
  (2) Y31,Y30 change to MEM_MB1_CLK0;V31,W31 change to MEM_MB0_CLK1
  (3) AE27 change to MEM_MA1_ODT1;AE28 change to MEM_MA0_ODT1
  (4) AG31 change to MEM_MB1_ODT1;AF31 change to MEM_MB0_ODT1
  (5) E20 change to MEM_MA_RESET#; B19 change to MEM_MB_RESET#
  (6) Reserve MEM_MA_DQS_8 , MEM_MA_DM8 and MEM_MB_DQS_8,MEM_MB_DM8

4,(page 10,11,) change to DDR3
  (1) Placement A0,B0,A1,B1
  (2) DIMM1,DIMM3 PN:N13-2400421-L06(Blue);DIMM2,DIMM4 PN:N13-2400631-F02 (GREEN)

5,(pag 6) Modify VRM_EN circuit;Reserve LDT_PWRGD to VRM_PWROK,VID_SEL circuit;Add C587

6,(page 12) Remove the termination resisters and decouping caps

7,(page 13) R196,R197 change to 301R1%;Reserve R436,R443 for RS740

7,(page 14) Lan TX/RX pairs connect to GPP3 to co-lay RS740

8,(page 15)
  (1) ball B8 is RS780 (DDC_DATA0) and RS740 (BMREQ#),
      ball A8 as it is used as DDC_CLK0 for RS780 and DDC_DATA for RS740
  (2) Reserve LDT_RST#,LDT_STOP# level-shift circuit for RS740;
      Reserve R570,R571,R159,to Patch the timing of SYSRESET# & LDT_RST#
      & LDT_STOP# (Errata:ER_RS780B6 ERN # RS780-024))
  (3) Add R472 and power rail VDDG_NB;R305 change to 1KR
  (4) Reserce L52 to pin7,D7 for RS740;Remove CP20
  (5) Leave empty R275,R283,R251 for RS740 only
  (6) Add L42,C797;leave empty R246
  (7)modify the I2C_CLK/I2C_DATA,SDA0_AUX0P/SCL0_AUX0N Pull-up and level shift topology
  (8) COMM_EN connect to Pin F9

9,(page 16)
  (1) For RS780 without Side-port:For VDDMEMNB stuff R723=0R and leave the LC filter empty;
  (2) Reserve CP29,R529 for RS740 co-lay
  (3) Stuff D38,R144 for POWER UP SEQUENCE
  (4) Remove VDDMEMNB LC filers,remove R529,C326 with no side-port memory
  (5) Remove CP8,L18 and short NB_VCC1P1 to SB VDDC pins

10,(page 17)
  (1) Reserve cystal circuit(Y6,C817,C818,R572) for A14 to solve the system time lag issue;
  (2) Modify A_RST# topology:add R441,R587,R590,R591,R592,R593
  (3) Remove R432,R442,C575,C556,C570(PCI_CLK1 & CK_P_33M_1394)
  (4) Reserve PGNT#1,PGNT#2 as TP

11,(pag 18)
  (1) USB OC[0::6]# PU RN11,R574;
  (2) Pin D3 RSMRST# connect to SIO Pin 85; (Reserve:remove R412,stuff R413=22KR,C547=2.2uF
      to meet timing requirement);
  (3) KRRST# PU resister R382 change to 1KR;Reserve R655(ITE suggest)
  (4) Add R117;Reserve R212,R655

12,(pag 19) Reserve C574;SPI rom change to M31-25X1613-W03

12,(pag 20) Modify the SB power rail from VCC_1V2 to VCC_SB_1V2

13,(page 22)
  (1) Change termination R on RED channel R158,R503 to 140R follow AN_RS780G1(For A13)
  (2) add R179,R221,leave R108,R126,Q11,Q12 empty ,R122,R130 change to 4.7KR;
      (For RS 780 level shifter not requried)
  (3) the VGA1 PN change from N51-15F0391-F02 to N51-15F0391-A10(the pin is same but outside of board different)
  (4) leave empty Q8,Q13,C95 for RS740 only and R104,R128 change to 4.7KR
  (5) Add Q59,Leave empty D2,reserve R201,R81 change to10KR,R85 change to 200KR
  (6) Leave shunt R empty R204,R201,R215,R218,R538,R540,R539

14,(pag 23) Clock Gen change to SLG8LP625

15,(pag 24) Remove LPT1 circuit;SATA4 change to black N5N-07M0221-H06 for e-SATA

16,(pag 25) LAN change to Broadcom BCM5784/5764/5906(all co-lay),defualt 5906 M

17,(pag 26) Super IO change to IT8720;Floppy leave empty default;COM1 header change to Rear COM port

18,(pag 27) The ACPI solution change to UPI;System power generater circuit;the NB,SB PWRGD sequence

19,(pag 28) The VCC_DDR (PWM)and NB_VCC1P1 (Linear) circuit;CPU_VDDR(1.2V) generater

20,(pag 29) Remove the CD-IN header;ADD SPIDIF OUT header

21,(pag 30)
  (1) USB power regulater modify to UP7533;
  (2) Stuff Common choke L12-181D017-CA8 and L12-900D017-CA8

22,(pag 31) ADD PCIE1_X2 Slot;Reserve R579,R581 for RS740

23,(pag 32) Remove PCI2 slot ;Add PREQ#2 PU R528

24,(pag 34) Remove U20 circuit;Add D36 and leave R478 empty

24,(pag 35) NB heatsink change to HS_43_44X31_24

NOTICE

3,(page 18)
  Configer GPIO5 to output mode or internal PU/PD can Leave R377 empty ;??
  R360,R367 can leave empty

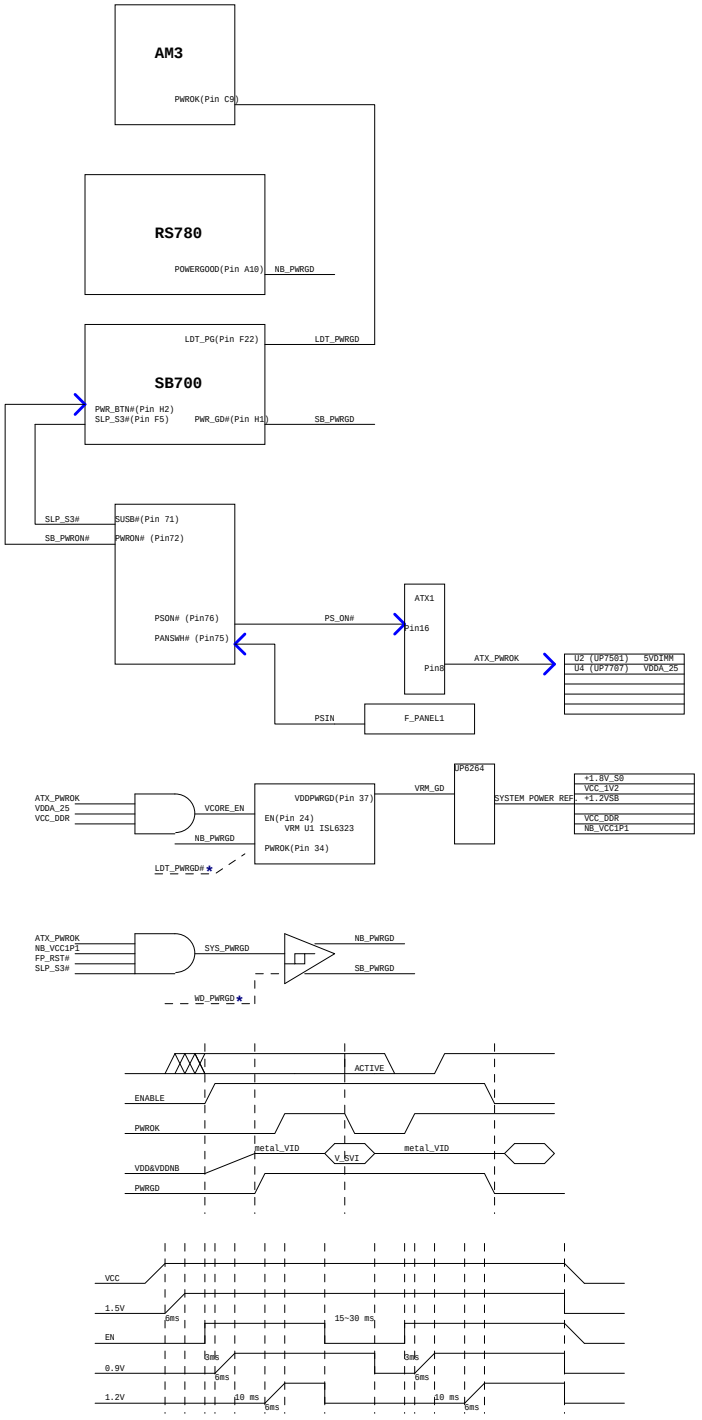
4,(page 17,22)
  (1) PCICLK5/GPIO41 power up default&enabled register changed between A11 and A12
  (2) LPC_CLK0&AZ_RST# the straps for the PCI ROM BOOT and IMC enable should be verified

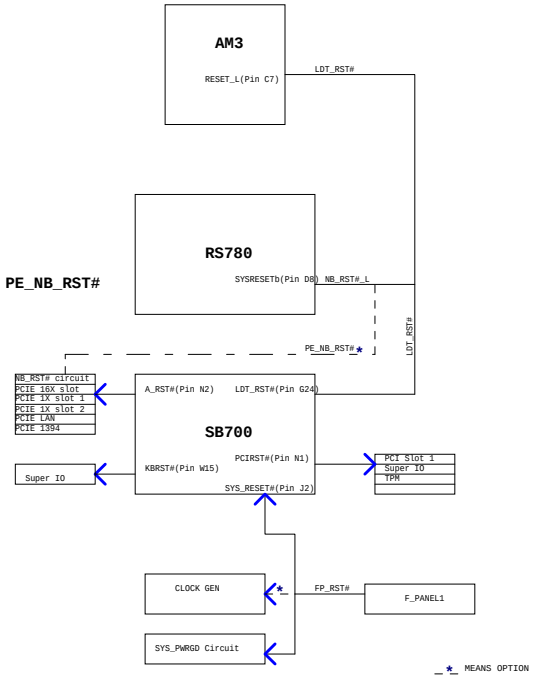
5,(page 23) Make sure NB&SB PCIE PHY 100M REF CLOCK from the SRC PLLs rather than SB_SRC PLL
  Follow APnote PA_RS7X0A2

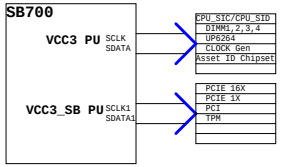
BOM

1, No AM3 socket PN,in the sche use AM2 PN N12-9400040-F02

2, CHIPSET: RS780 Ver A13PN. B01-RS78085-A08 乙SB700 Ver A12 PN. B01-SB70035-A082







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BOM

For AMD check

6R165,R534,R564l eave empty
9stuff
C713,C706,C688,C704,C694,C680,C703,C691,C711,C696,C682,C72,C81,C108,C110,C702,C684,C714,C210,C132,C712,C768,C50,C252,C57,C66,C236,C249
Add C239,C241,C819,C243,C261,C246,C104,C105,C723
remove C242,C244

16stuff C307,C309,C311,C316,C797L29,L31,L22,L42

12Add 369L19,L20L21,L25

1, page 22 D9,D10,D11 placed close to CRT connector;
Stuff U7,U8 and leave emtpy R142,R148

remve RX780 parts

6,reserve Q9

17,remove Q58,Q60,Q61,R466,R464,R408,C546

31,modify all the PU to 8.2KR to VCC3;leave empty PREQ#[0:5] PU R

17~19,Remove Reserved R378,R383,R506,R507,R508,R509,R401

18,remove R117,R385 duplicate with R638,R642
Remove WAKE ON LAN Circuit
15,remove VDDG_NB power(R472,R479) and use VCC3,remove R301,R246,R241,R298,R217

23,remove W83391TG,RN8,FS1

25,Modify SYS_TEM to VR_TEMP_DA(remove RT1,R35,C11 chagne to 2200pF)
Remove BIOS WRITE PROTECT Circuit

15,remove DISPLAY PORT

9,Modify CPU_VDDIO_PWRGD

7,VDDIO_FB R163 connect to DDR_FB

12,clock generator should not be enable before VCC_1V2 is ready.

25, Add AMDTSI circuit

VCC

EN

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