Compal Confidential

AAP11/AAP21

Schematic Document

SKL-H paltform with Nvidia N16E-GS/GT/GX

Rev: 1.0(A00) PVT

2015/07/21

@ : Nopop Component

EMI@ /@EMI@ : EMI pop/unpop part
ESD@ /@ESD@ : ESD pop/unpop part
RF@ /@RF@ : RF pop/unpop part

CONN@ : Connector Component

AOAC@ : Intel AOAC
DS3/NODS3: deepS3
TBT@: ThunderBolt
PD@: Power Delivery

DIS@ : Discrete Part
N16EGS@:N16E-GS(2G)
N16EGT@:N16E-GT(3G)
N16EGX@:N16E-GX(4G)
2G@:2G VRAM
3G@:3G VRAM
4G@:4G VRAM

DAX PCB
DAZ18F00100
PCB 18F LA-B752P REV0 M/B 8
R1@

DAX PCB
DAZ18F00101
PCB 18F LA-B752P REV0 M/B 8
R3@

12L

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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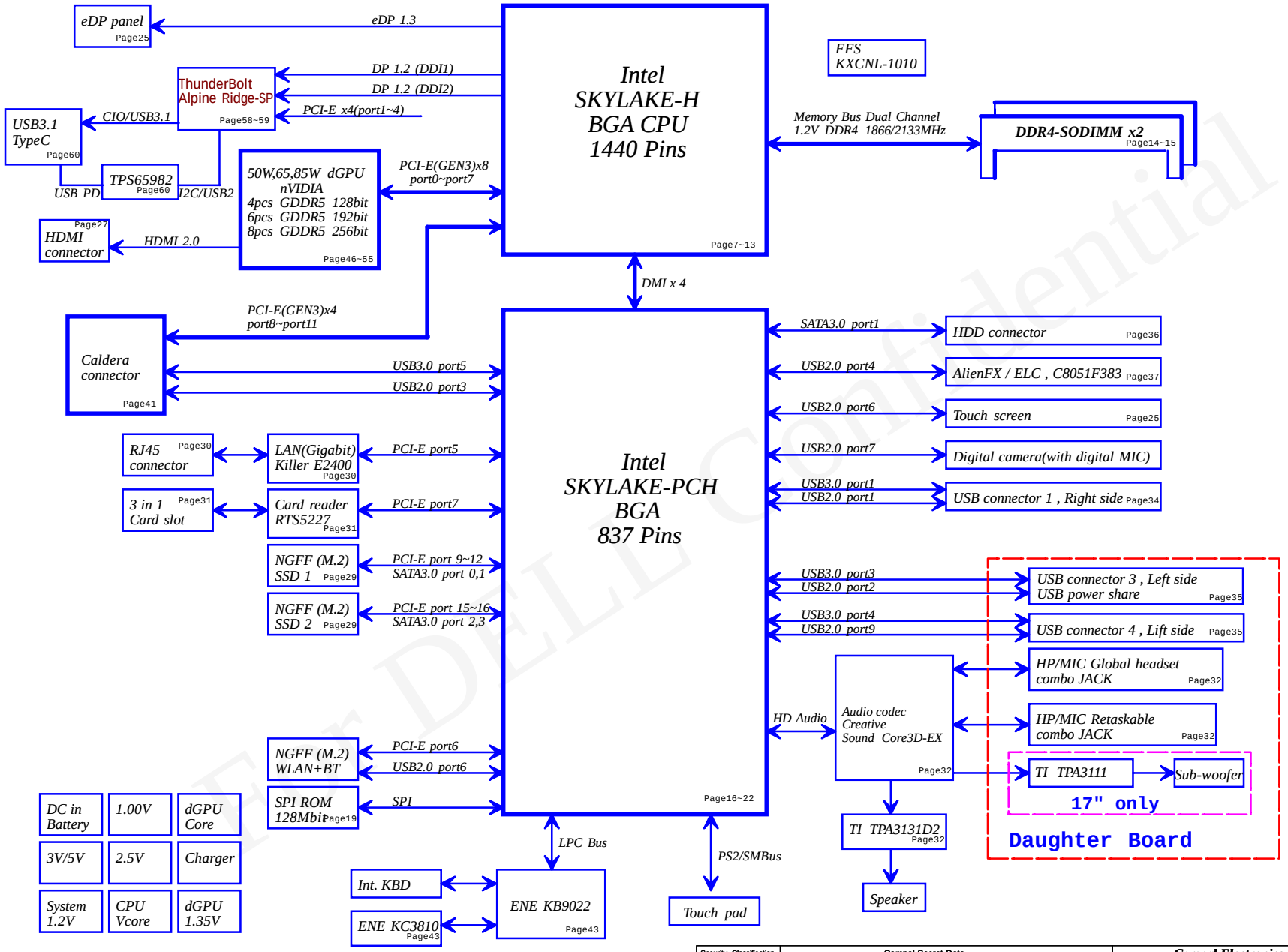
Title: *Cover Sheet*

Size	Document Number	Rev
Custom	*LA-C912P*	0.1

Date: Wednesday, July 22, 2015 Sheet 1 of 78

SKL+NV Block Diagram



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Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	Block diagram		
Size	Document Number	LA-C912P	Rev 0.1
Date: Wednesday, July 22, 2015	Sheet 2 of 78		

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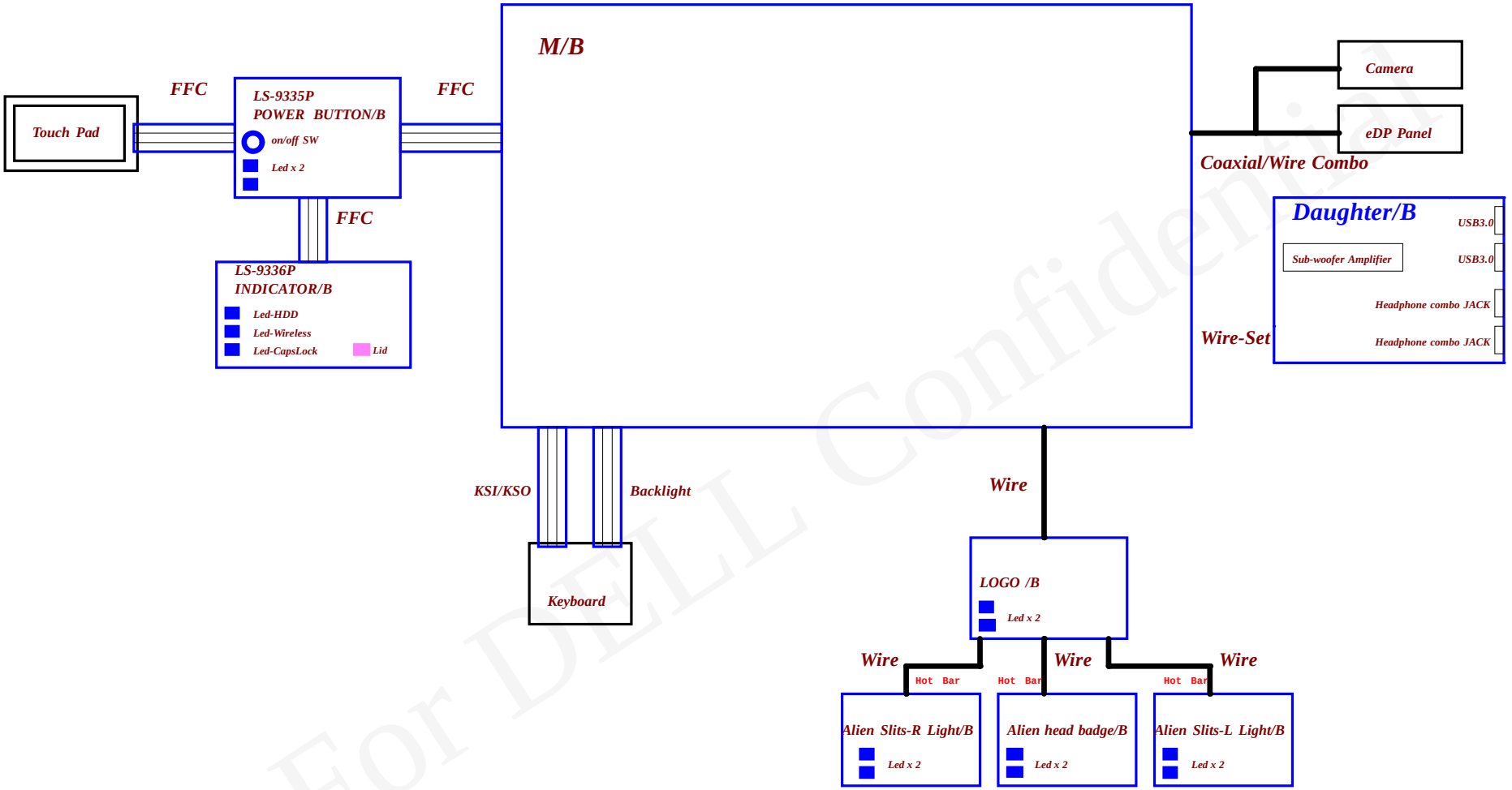

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Wednesday, July 22, 2015 | Sheet 3 of 78

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	NVIDIA Graphic
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	AMD Graphic
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

Board ID TABLE

ID		PCB Revision
NV	AMD	
0	10	EVT
1	11	DVT-1
2	12	DVT-1.1
3	13	DVT-2
4	14	DVT-3
5	15	Pilot build

TBT connector change to SMD type.

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N16)
CLKOUT_PCIE5	DGPU (Caldera)

BDW	USB3.0	
	Port1	Right side1
	Port2	Right side2
	Port3	Left side 1
	Port4	
	Port5	Caldera
	Port6	Left side 2
	USB2.0	
	Port0	Right side1
	Port1	Left side 1 (PowerShare)
	Port2	Caldera
	Port3	ELC
	Port4	BT
	Port5	Touch screen
	Port6	Camera
	Port7 / 8	Right side 2 Left side 2
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100/1000 LAN
	Lane 4	M.2 Card WLAN
	Lane 5	PCIE 4x MUX
	Lane 6	
	SATA	
	SATA0	HDD
	SATA1	NGFF SSD
	SATA2	NGFF SSD
	SATA3	

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes list			
Size	Document Number: LA-C912P		Rev: 0.1
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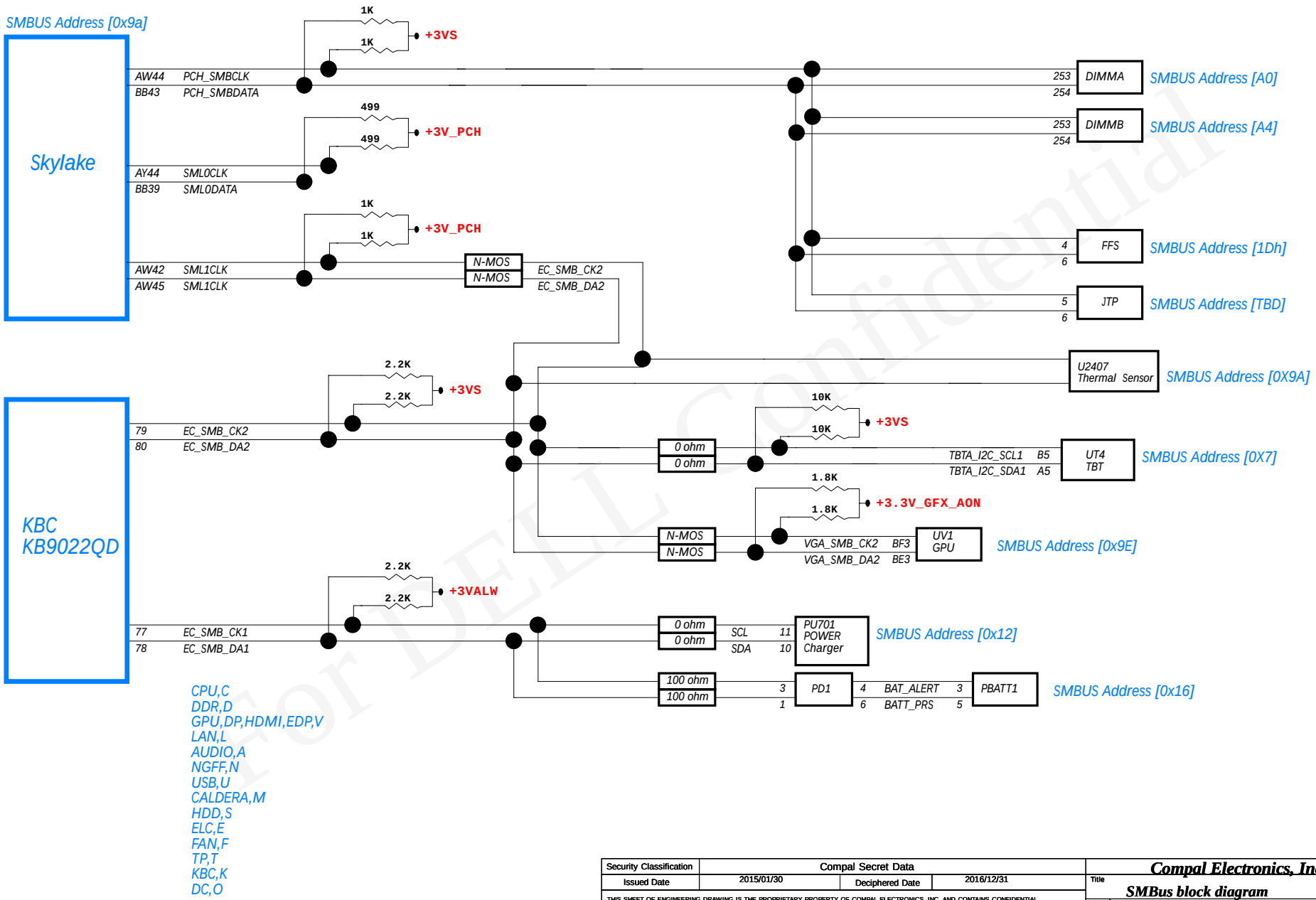

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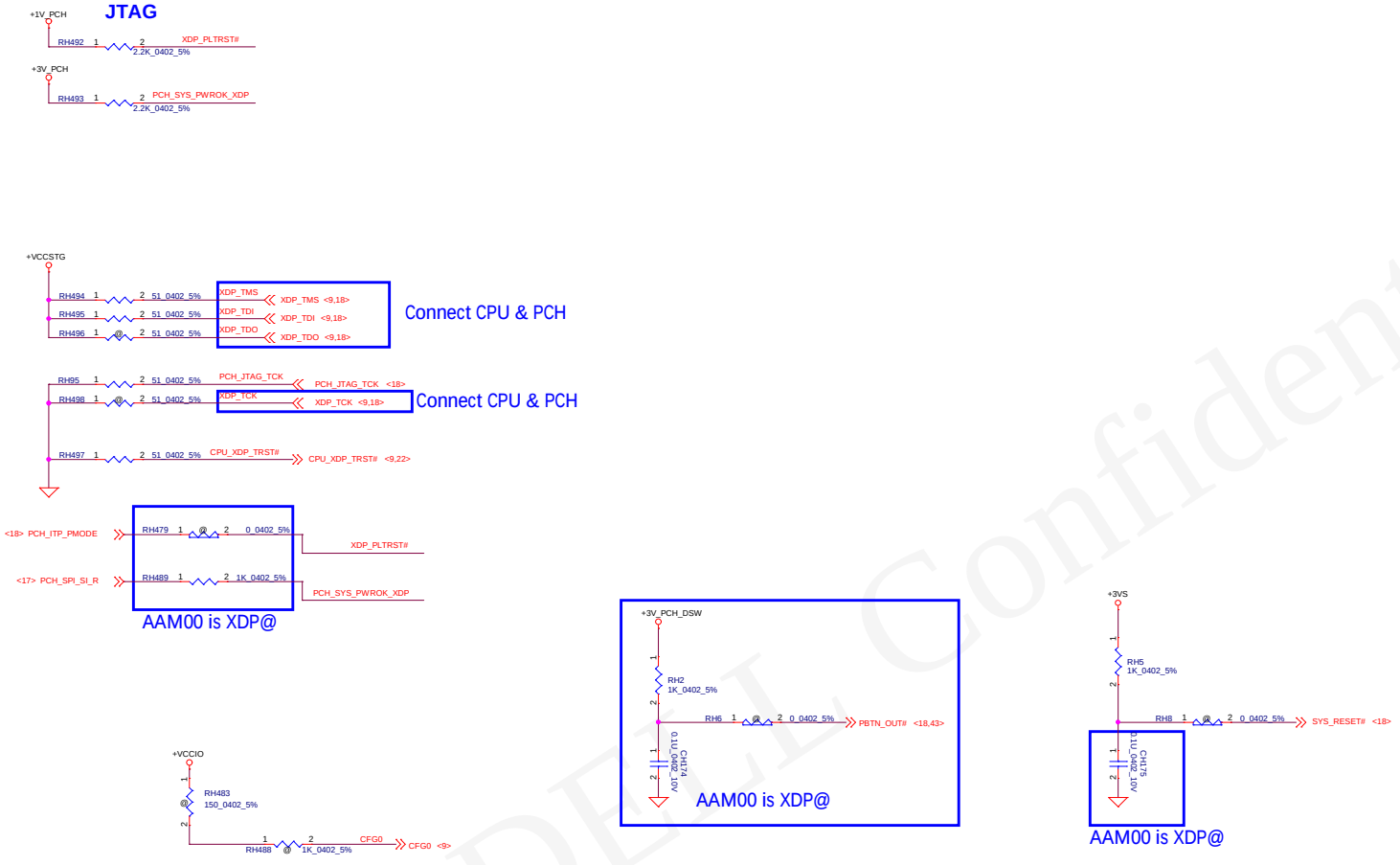
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **SMBus block diagram**

Size	Document Number	Rev
	LA-C912P	0.1

Date: Wednesday, July 22, 2015 Sheet 5 of 78



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

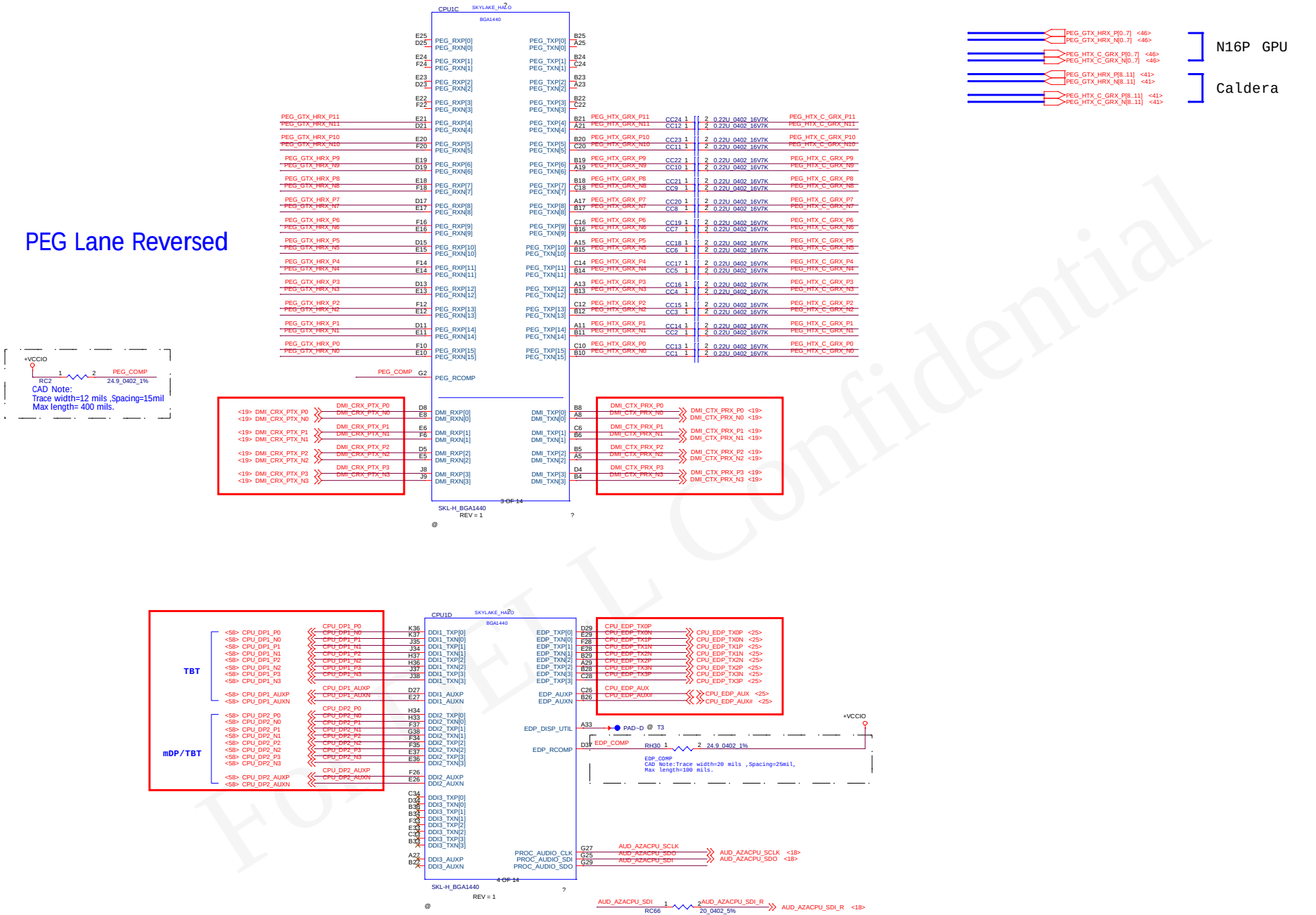
Compal Electronics, Inc.

Title: **XDP CONN**

Size	Document Number	Rev
		0.1

Date: Wednesday, July 22, 2015 Sheet 6 of 78

PEG Lane Reversed



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

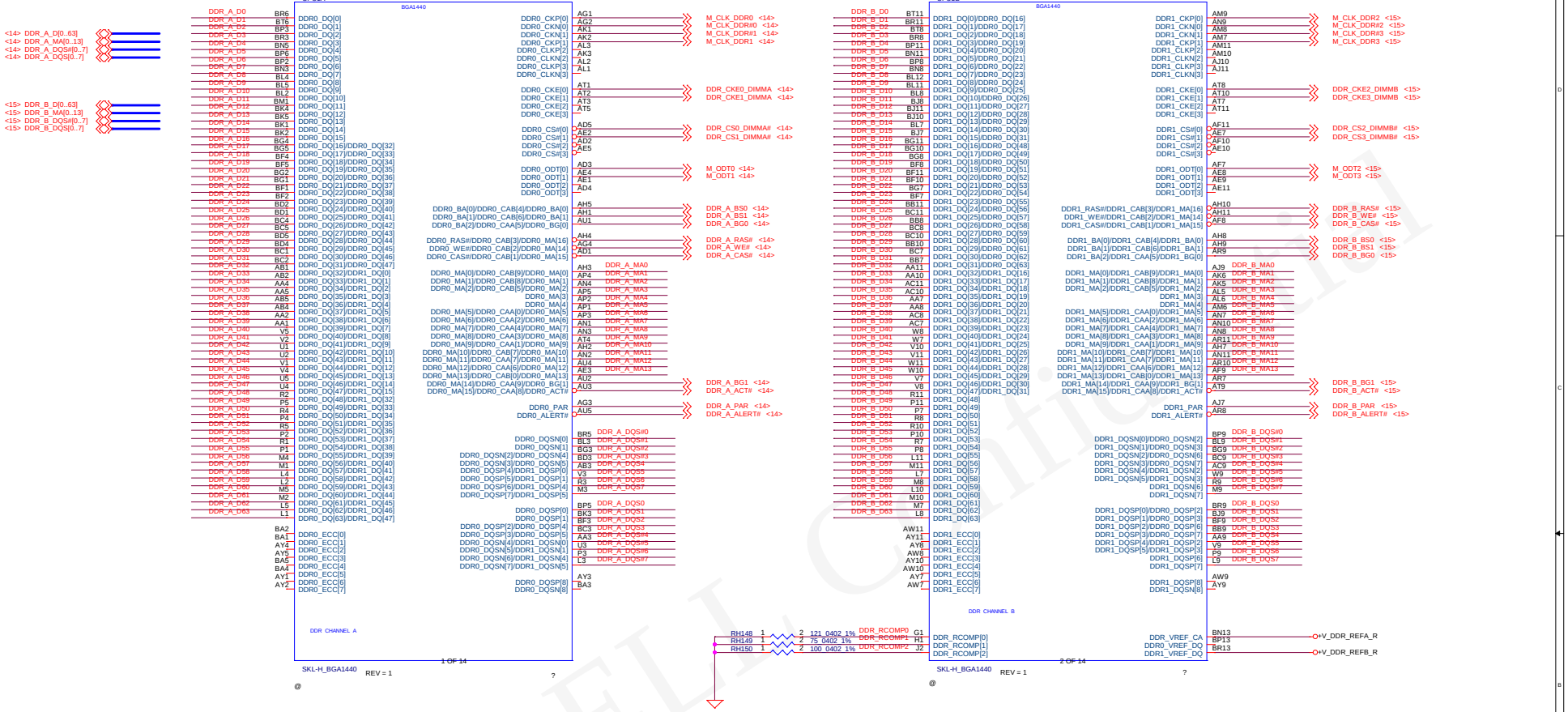
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
C		0.1

Date: Wednesday, July 22, 2015 Sheet 7 of 78

Interleave



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: ***PROCESSOR(2/7) DDRIII***

Size	Document Number	Rev
C		0.1

Date: Wednesday, July 22, 2015 Sheet 8 of 78

CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) * 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

4/13 UC1 SA00005U600 is X1 code.
Change PN SA00005U600 to SA00007WE00.

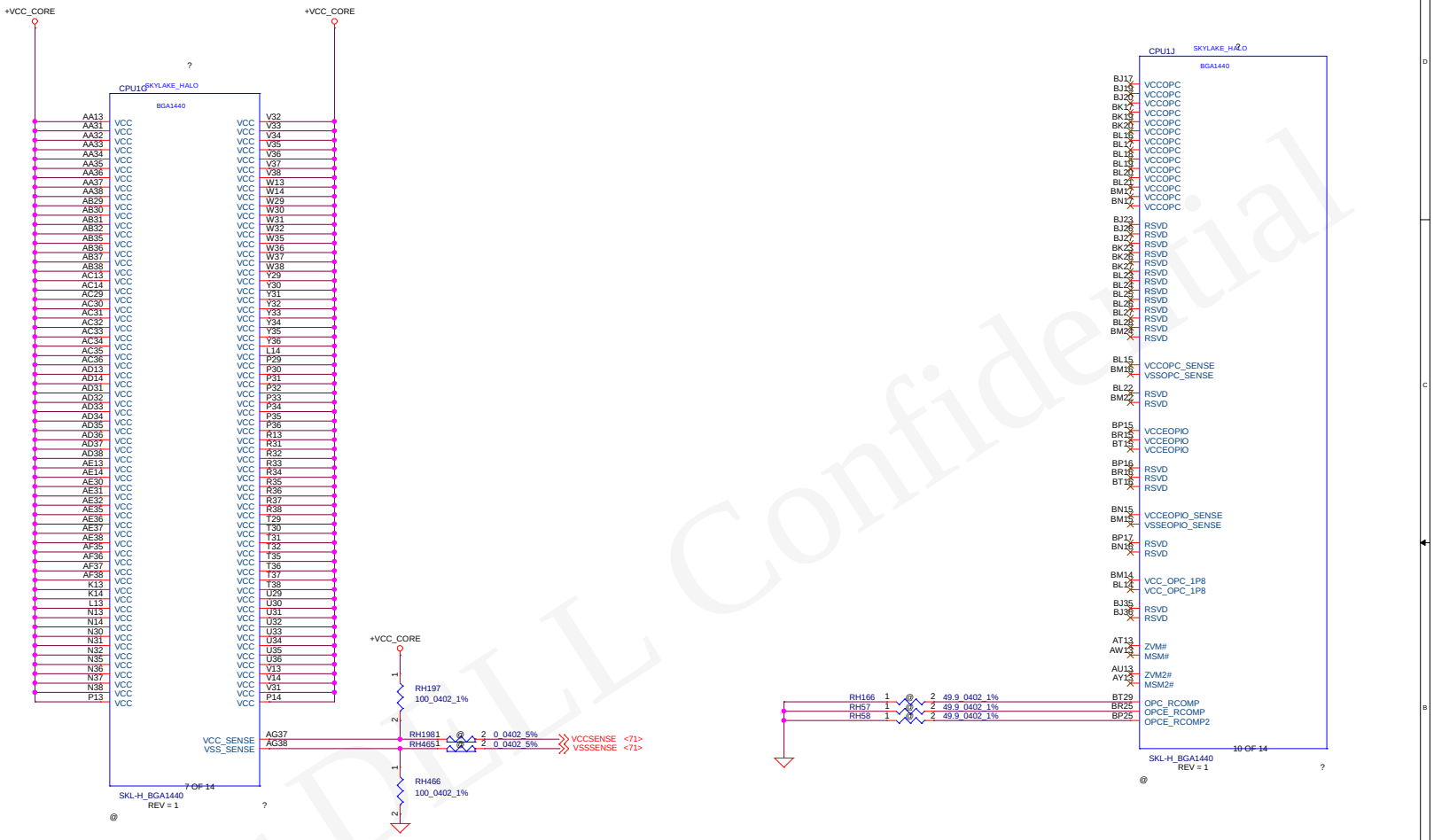
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(3/7) RSVD,CFG

Size: C | Document Number | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 9 of 78

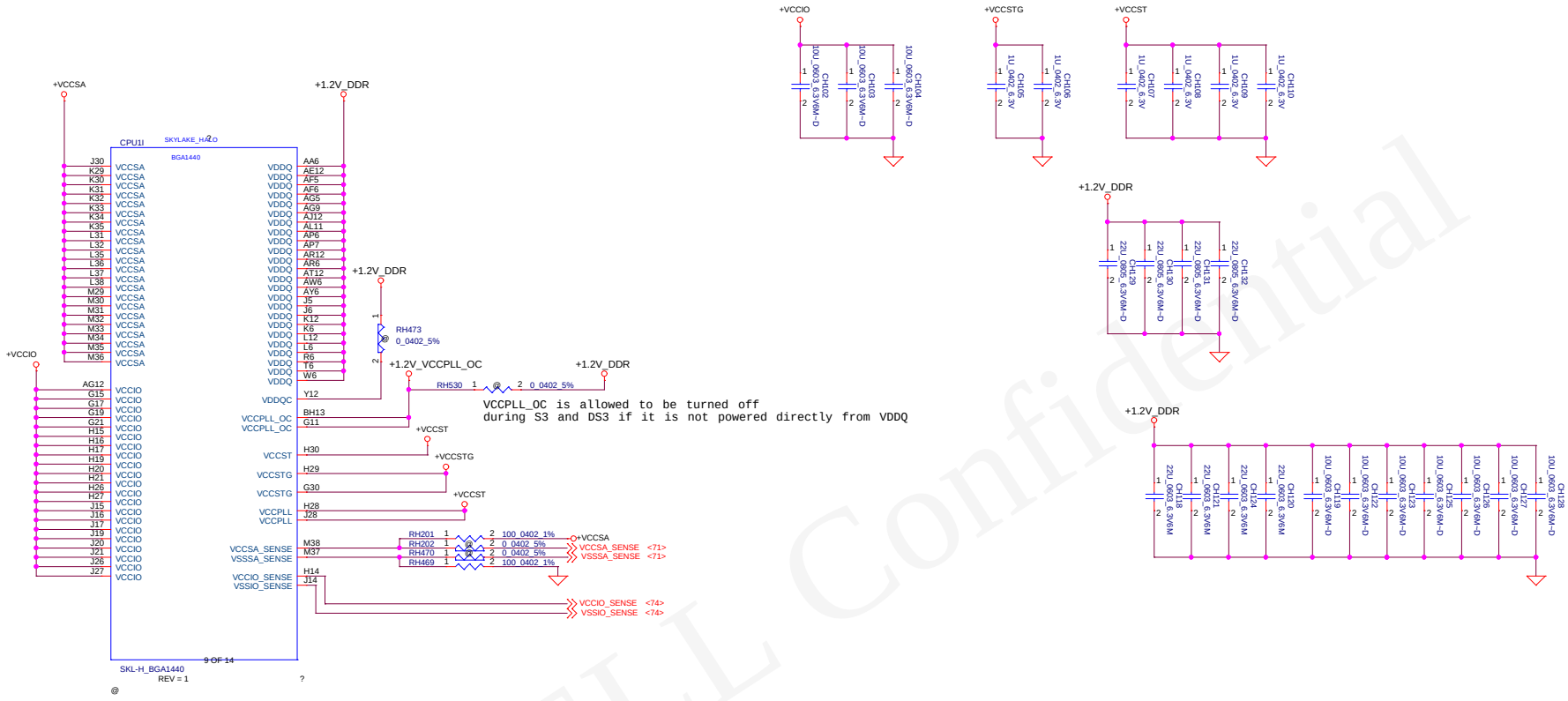


Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Title: ***PROCESSOR(4/7) PWR,BYPASS***

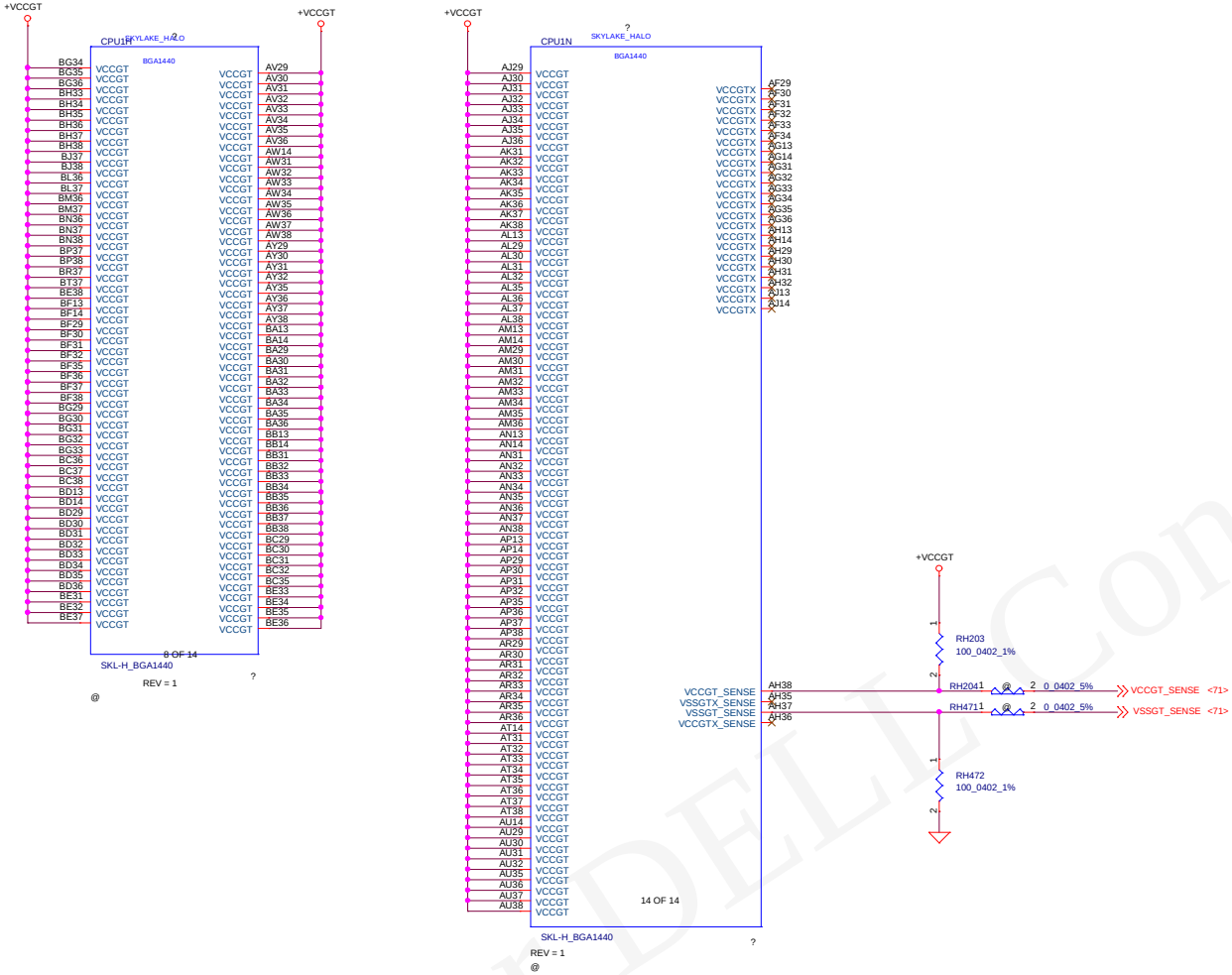
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, July 22, 2015 Sheet 10 of 78



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	PROCESSOR(5/7) PWR
Size: Custom	Document Number: Rev 0.1
Date: Wednesday, July 22, 2015	Sheet 11 of 78

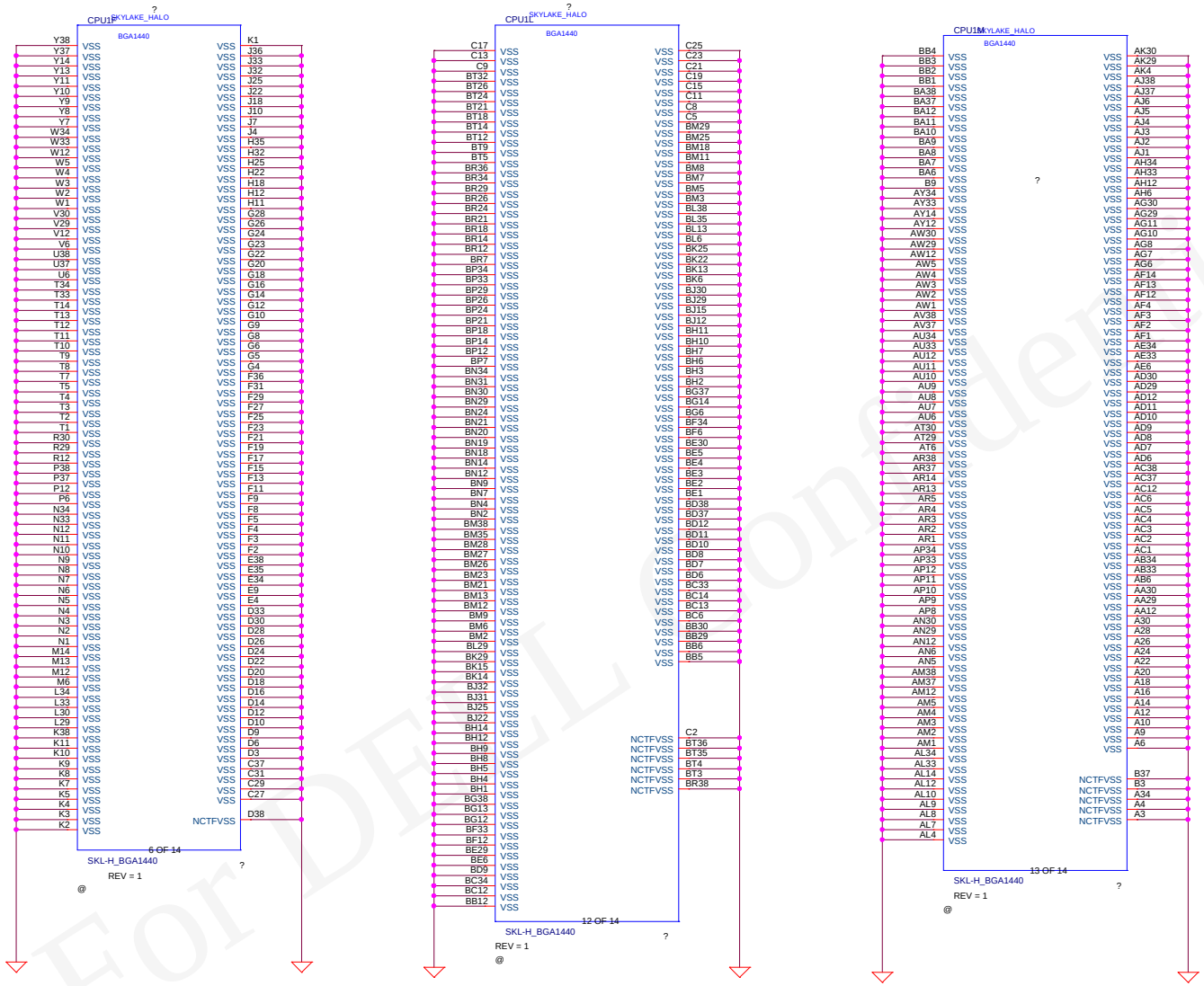


Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Title: PROCESSOR(6/7) PM,XDP,CLK

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 12 of 78



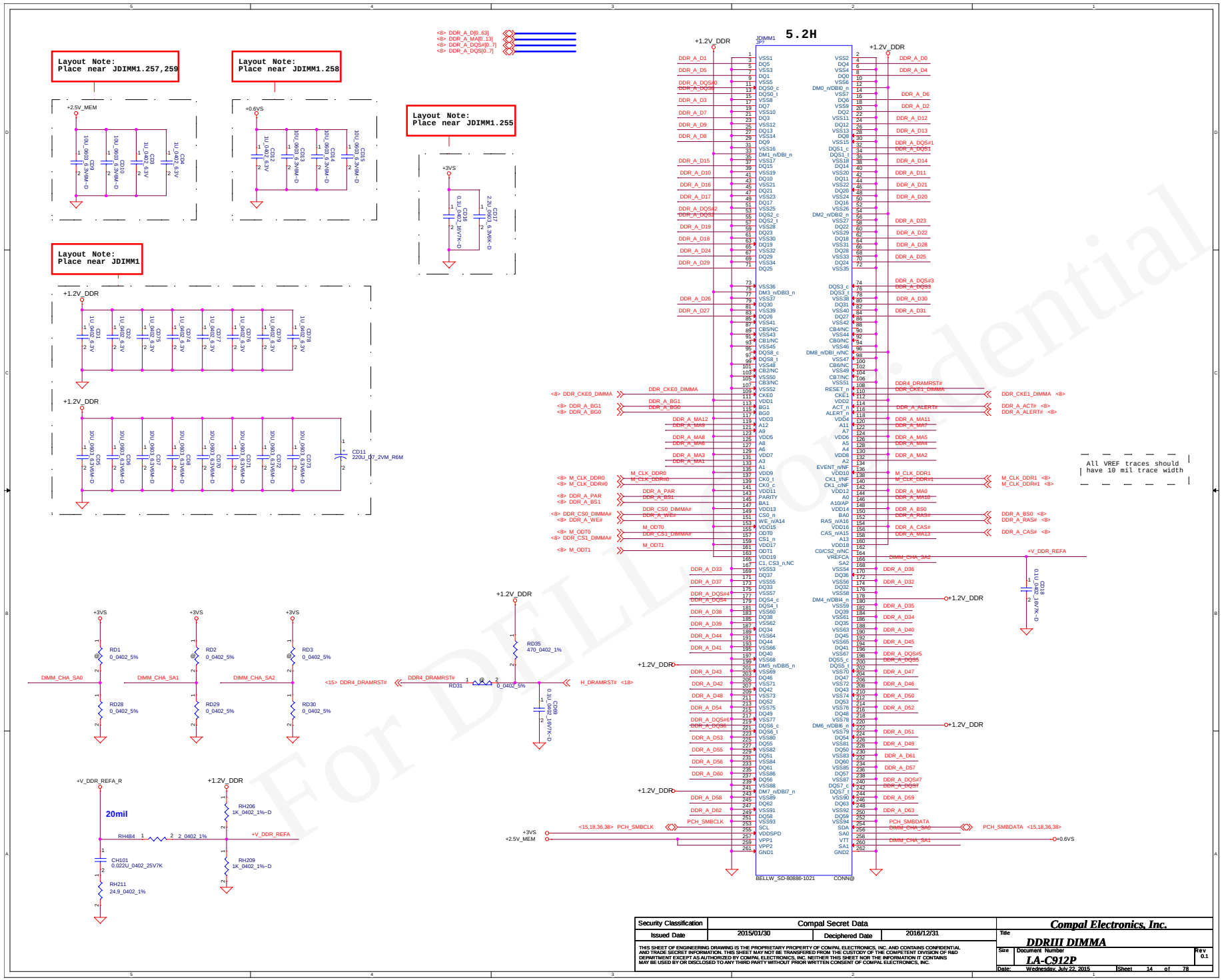
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PROCESSOR(7/7) VSS**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, July 22, 2015 | Sheet 13 of 78



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Issued Date	2015/01/30	Deciphered Date 2016/12/31	Title: DDRIII DIMMA
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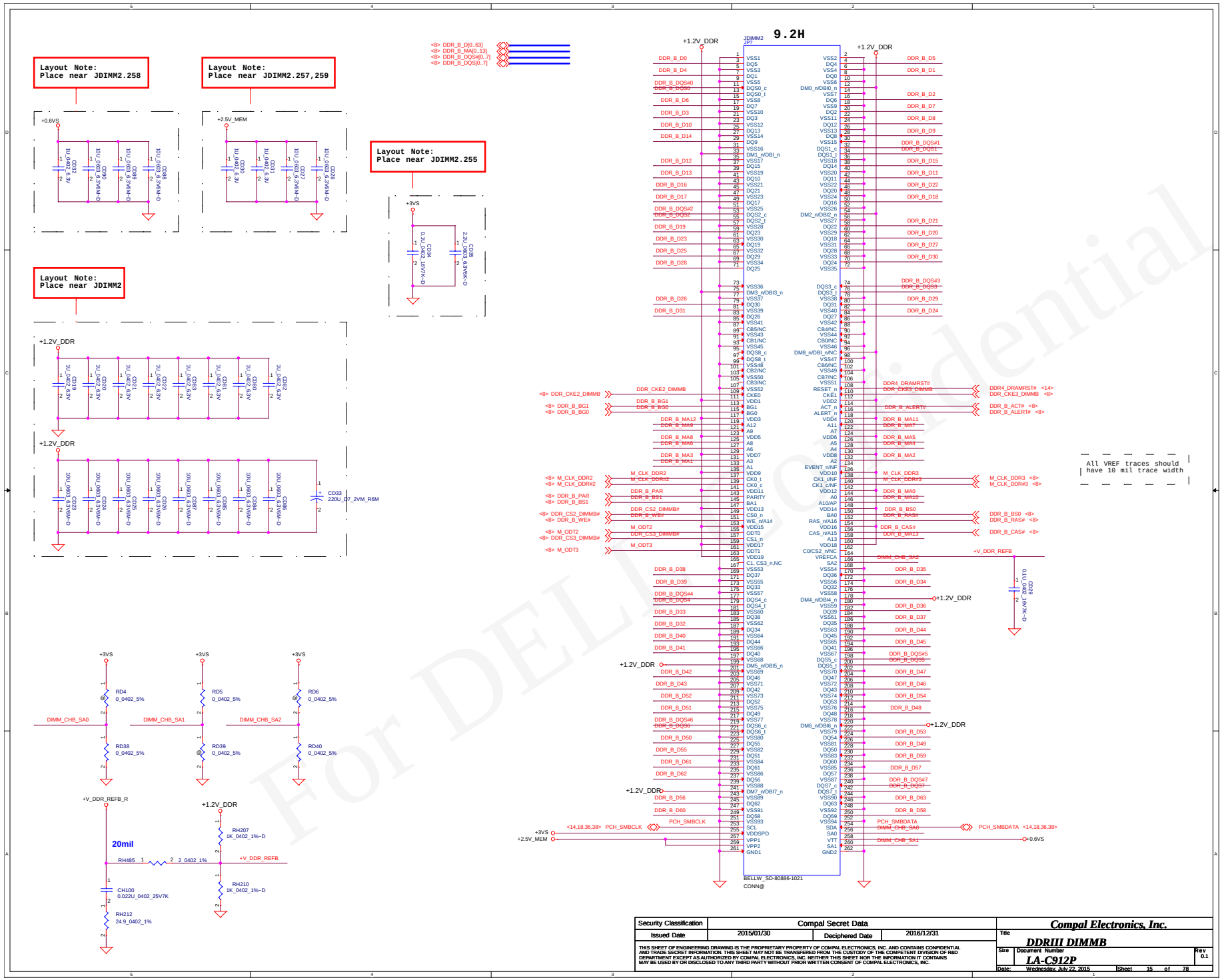

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Title	DDRIII DIMMB		
Size	Document Number		Rev
	LA-C912P		0.1
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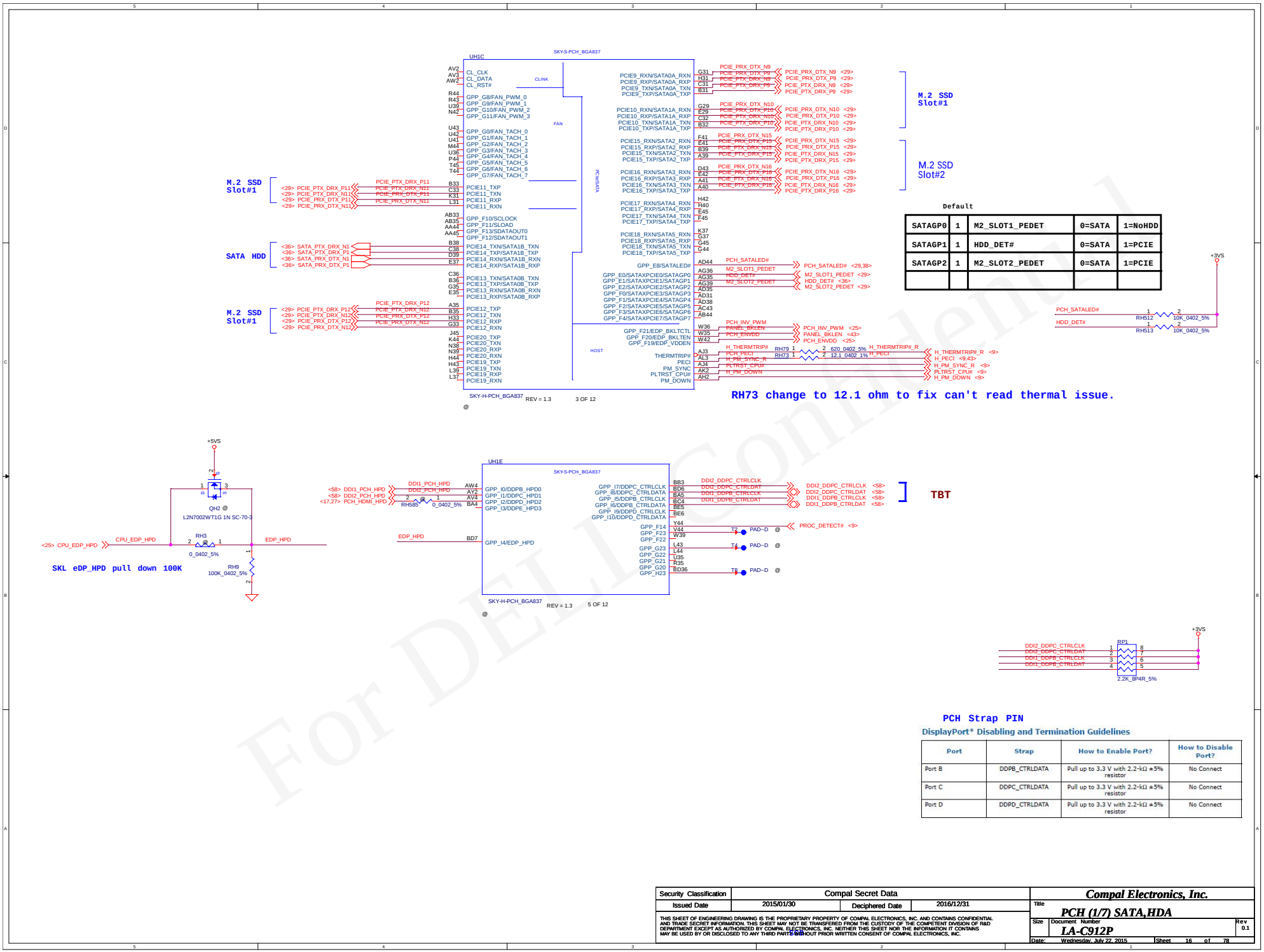

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	PCH (1/7) SATA,HDA
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RTC CRYSTAL

PCH_RTCX1 — RH70 1 — 2 10M_0402_5% — PCH_RTCX2
YH1 32.768KHZ_X1A000141000300
Max Crystal ESR = 50k Ohm.
CH45 8.2P_0402_50V
CH46 8.2P_0402_50V

XTAL24_IN — RH72 1 — 2 1M_0402_5%~D — XTAL24_OUT
YH2 24MHZ_12PF_X3G024000DC1H
CH47 15P_0402_50V
CH48 15P_0402_50V

+3VS
UH3 TC7SH08FU_SSOP5
PCH_PLTRST# — PLT_RST# <28,29,30,31,43,58>
RH199 100K_0402_5%

+3VS — EC_SMI# — 10K_0402_5% — RH110

+RTC_CELL — RH531 1M_0402_5% — INTRUDER#

UH1G (SKY-S-PCH_BGA837)

PEG	<46> CLKREQ#_GPU	CLK_PEG_GPU# <46> / CLK_PEG_GPU <46>
NGFF1	<29> CLKREQ_PCIE#1	CLK_PCIE_N1 <29> / CLK_PCIE_P1 <29>
NGFF2	<29> CLKREQ_PCIE#2	CLK_PCIE_N2 <29> / CLK_PCIE_P2 <29>
TBT	<58> CLKREQ_PCIE#3	CLK_PCIE_N3 <58> / CLK_PCIE_P3 <58>
LAN	<30> CLKREQ_PCIE#4	CLK_PCIE_N4 <30> / CLK_PCIE_P4 <30>
WLAN	<28> CLKREQ_PCIE#5	CLK_PCIE_N5 <28> / CLK_PCIE_P5 <28>
Card Reader	<31> CLKREQ_PCIE#6	CLK_PCIE_N6 <31> / CLK_PCIE_P6 <31>
Caldera	<41,43> CLKREQ#_DGPU	CLK_PCIE_N7 <41> / CLK_PCIE_P7 <41>

	PCIE Diff	CLK Req
TBT	1~4	3
LAN	5	4
WLAN	6	5
CR	7	6
NGFF1	9~12	1
NGFF2	15~16	2

+1V_PCH — RH71 1 — 2 2.7K_0402_1% — XCLK_BIASREF

RP3 10K_0804_8P4R_5% — RP5 10K_0804_8P4R_5%

REV = 1.3 7 OF 12

UH1A (SKY-S-PCH_BGA837)

PCH_PLTRST# <41,46>
TBT_FORCE_PWR <58>
EC_SMI# <43>
INTRUDER#

PCH_SPI_SI_R — RH583 1 — 2 0_0402_5% — <36> FFS_INT1 / <16,27> PCH_HDMI_HPD / <36> FFS_INT2

+3VS — RH584 1 — 2 10K_0402_5%

NV PULL High, AMD PULL Low.

1 OF 12 REV = 1.3

+3V_PCH — RH74 1 — 2 3.3K_0402_5% — PCH_SPI_CS# — RH75 1 — 2 1K_0402_5% — PCH_SPI_WP#_R — RH78 1 — 2 1K_0402_5% — PCH_SPI_HOLD#_R — RH4551 — 2 1K_0402_5% — PCH_SPI_HOLD#_R

9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

RPH5 15_0804_8P4R_5%
PCH_SPI_HOLD# — PCH_SPI_HOLD#_R
PCH_SPI_SO — PCH_SPI_SO_R
PCH_SPI_SI — PCH_SPI_SI_R
PCH_SPI_WP# — PCH_SPI_WP#_R
PCH_SPI_SI_R <6>
PCH_SPI_CLK — RH104 EMI@ — PCH_SPI_CLK_R 15_0402_1%

SPI ROM FOR ME (16MByte)
PN: SA00005VV10

+3V_PCH — CH49 0.1U_0402_16V7K~D
UH4 W25Q128FVSIQ_SO8
/CS — PCH_SPI_CS#
DO(IO1) — PCH_SPI_SO
/WP(IO2) — PCH_SPI_WP#
GND
VCC
/HOLD(IO3) — PCH_SPI_HOLD#
CLK — PCH_SPI_CLK
DI(IO0) — PCH_SPI_SI

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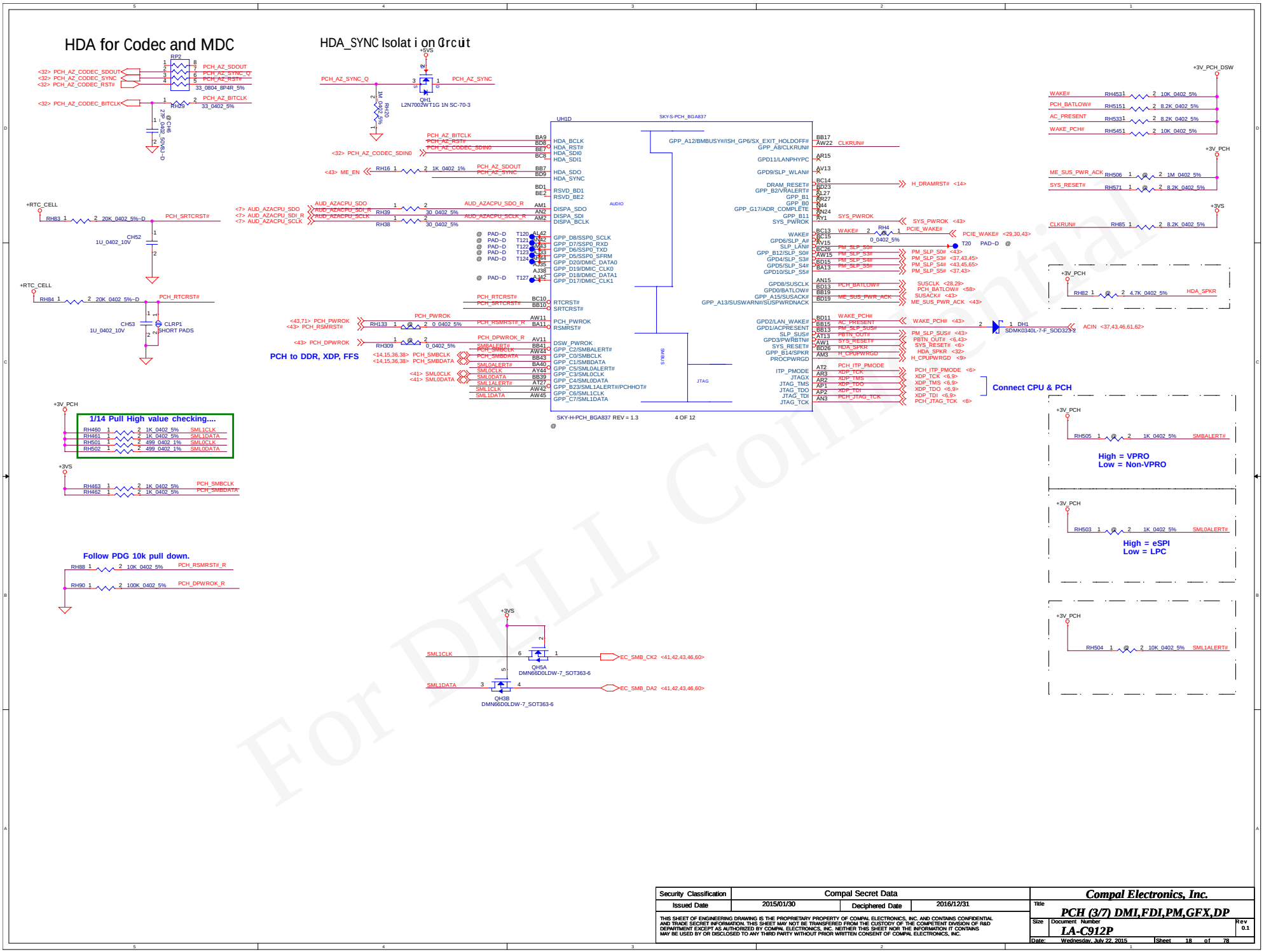
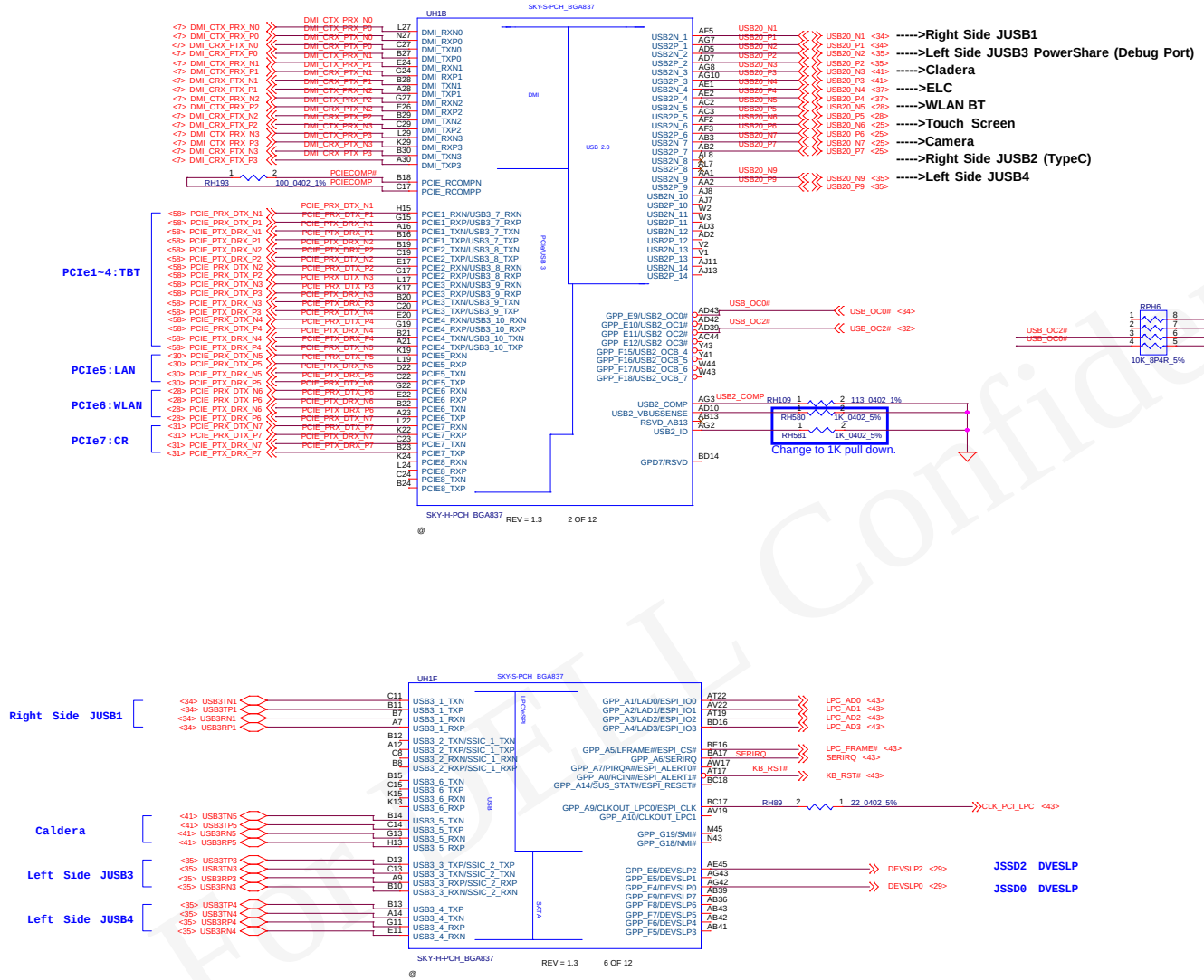
Compal Electronics, Inc.

Title: **PCH (2/7) SMBUS, CLK, SPI, LPC**

Size: — Document Number: **LA-C912P** — Rev: 0.1

Date: Wednesday, July 22, 2015 — Sheet 17 of 78





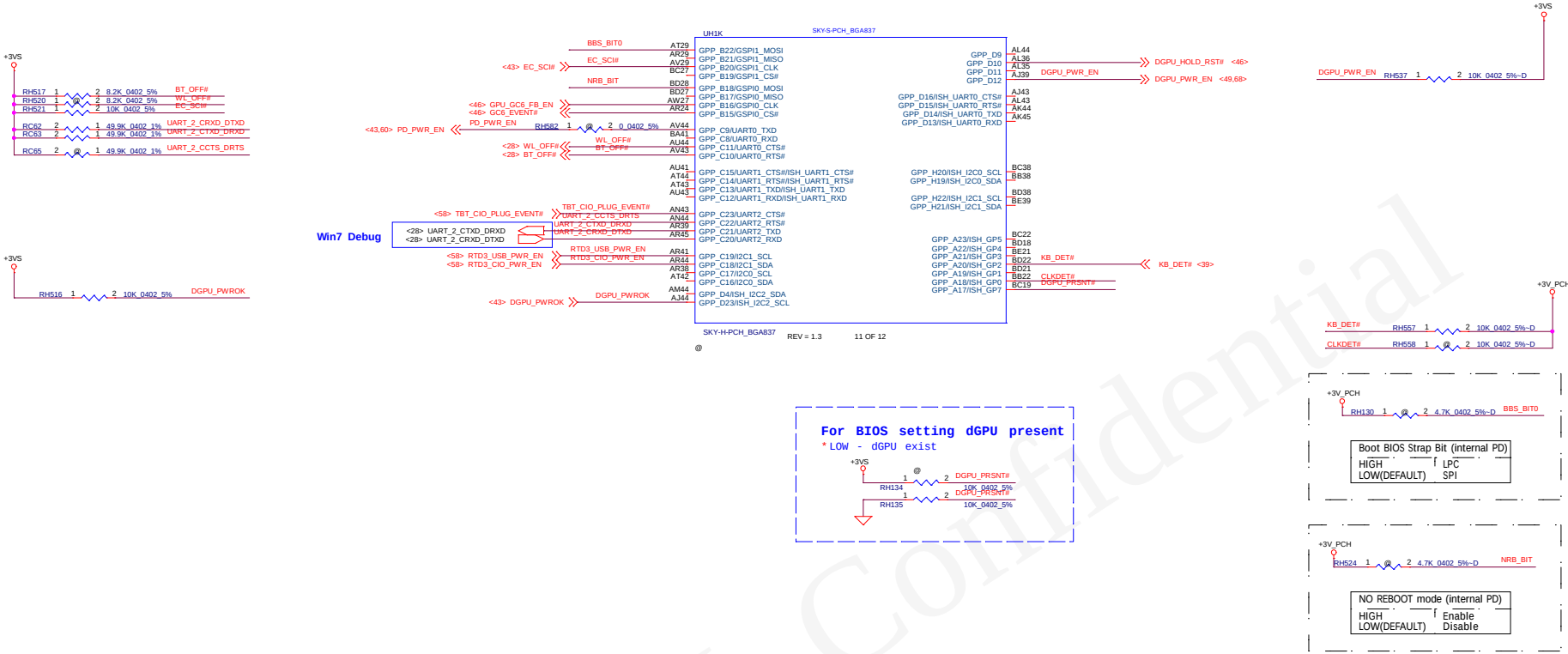
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PCH (4/7) PCI, USB**

Size	Document Number	Rev
	LA-C912P	0.1

Date: Wednesday, July 22, 2015 Sheet 19 of 78



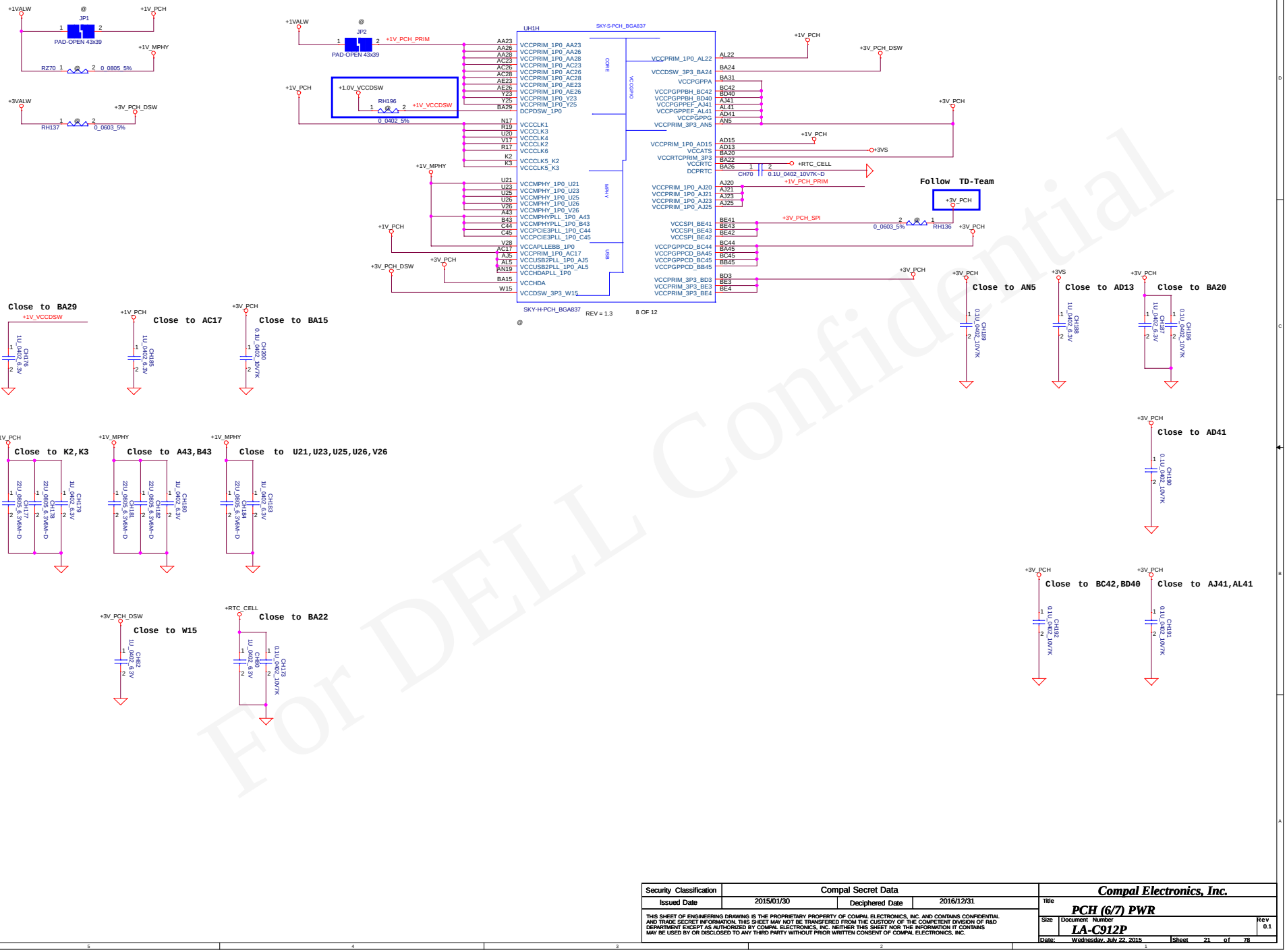
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PCH (5/7) GPIO, CPU, MISC**

Size	Document Number	Rev
	LA-C912P	0.1

Date: Wednesday, July 22, 2015 Sheet 20 of 78



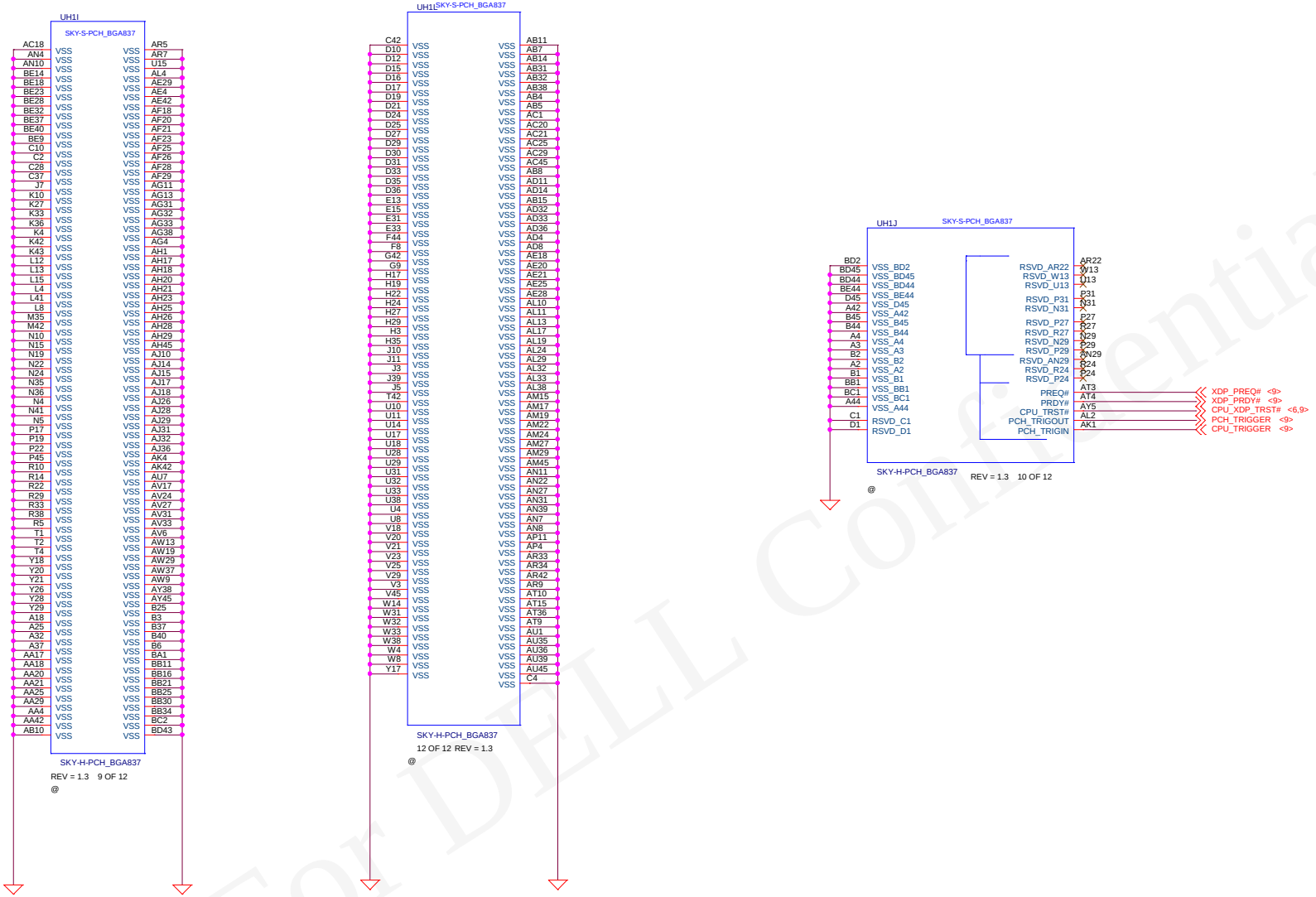
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PCH (6/7) PWR**

Size	Document Number	Rev
	LA-C912P	0.1

Date: Wednesday, July 22, 2015 Sheet 21 of 78



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PCH (7/7) VSS**

Size	Document Number	Rev
	LA-C912P	0.1

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Security Classification	Compal Secret Data		
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Title: Reserved Page		
Size	Document Number: LA-C912P	Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 23 of 78	

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Title: Reserved Page		
Size	Document Number: LA-C912P	Rev: 0.1
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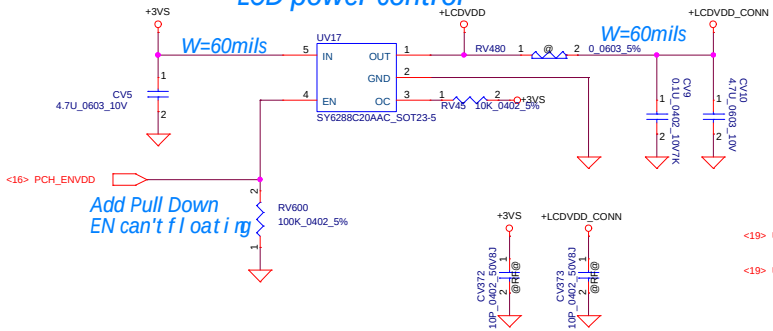
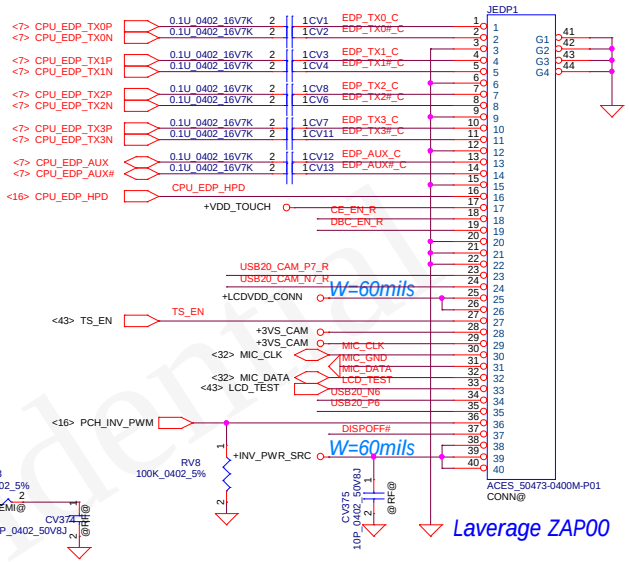
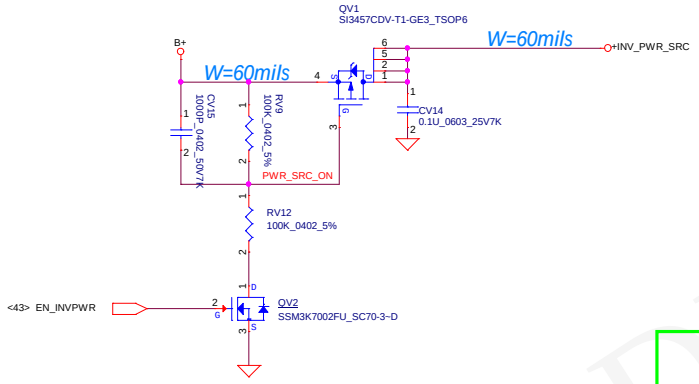
LCD power control



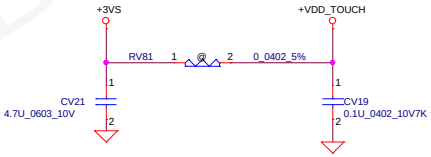
eDP connector



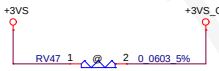
LCD backlight power control

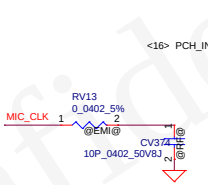


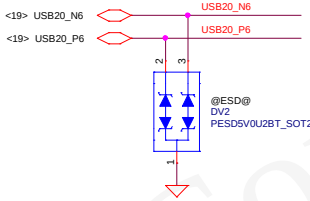
Touch screen panel power control

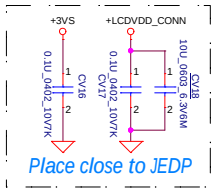


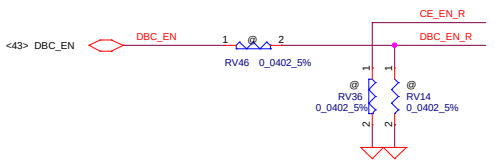
Webcam power control











Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **LCD Conn/Cam, Touch**

Size	Document Number	Rev
Custom	LA-C912P	0.1

Date: Wednesday, July 22, 2015 | Sheet 25 of 78

Empty page

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **3D Camera**

Size	Document Number	Rev
Custom	LA-C912P	0.1

Date: Wednesday, July 22, 2015 | Sheet 26 of 78

4/16 Change to 0201

4/21 Change to 0ohm.
NV suggest.

W=60mils

+HDMI_5V_OUT

HDMI_HPLUG

JHDMI1

FUTUR_061-HA18-0001

CONN@

W=60mils

+5VS

UV3

AP2330W-7_SC59-3

+HDMI_5V_OUT

W=60mils

4/16 Change to 0201 resistor.

HDMI_Down

+3VS_VGA

QX1

BSS138-G_SOT23-3

RX1

100K_0402_5%

ROYALTY HDMI W/LOGO
CPN:RO0000002HM

46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

To GPU

+HDMI_5V_OUT

+3VS_VGA

DV3

DV5

SDM10U45-7_SOD523-2

TMDS_TRLCLK

TMDS_CTRLDAT

QV92A

QV92B

DMN66D0LDW-7_SOT363-6

HDMI_SCLF

HDMI_SDAF

HDMI_SCLR

HDMI_SDAR

27NH_LQG15HS27NJ02D_300MA_5%

TMDS_CTRLCLK_R

TMDS_CTRLDAT_R

Place closed to JHDMI1

To PCH

PCH_HDMI_HPD

QX2

MMST3904-7-F_SOT323-3

RX2

150K_0402_5%

RX4

100K_0402_5%

CX1

0.1U_0402_16V7K

To GPU

TMDS_HPD

TC7SH08FU_SSOP5-D

DGPU_PEX_RST#

RX5

100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

Title: **HDMI LS & Conn.**

Size	Document Number	Rev
Custom	LA-C912P	0.1

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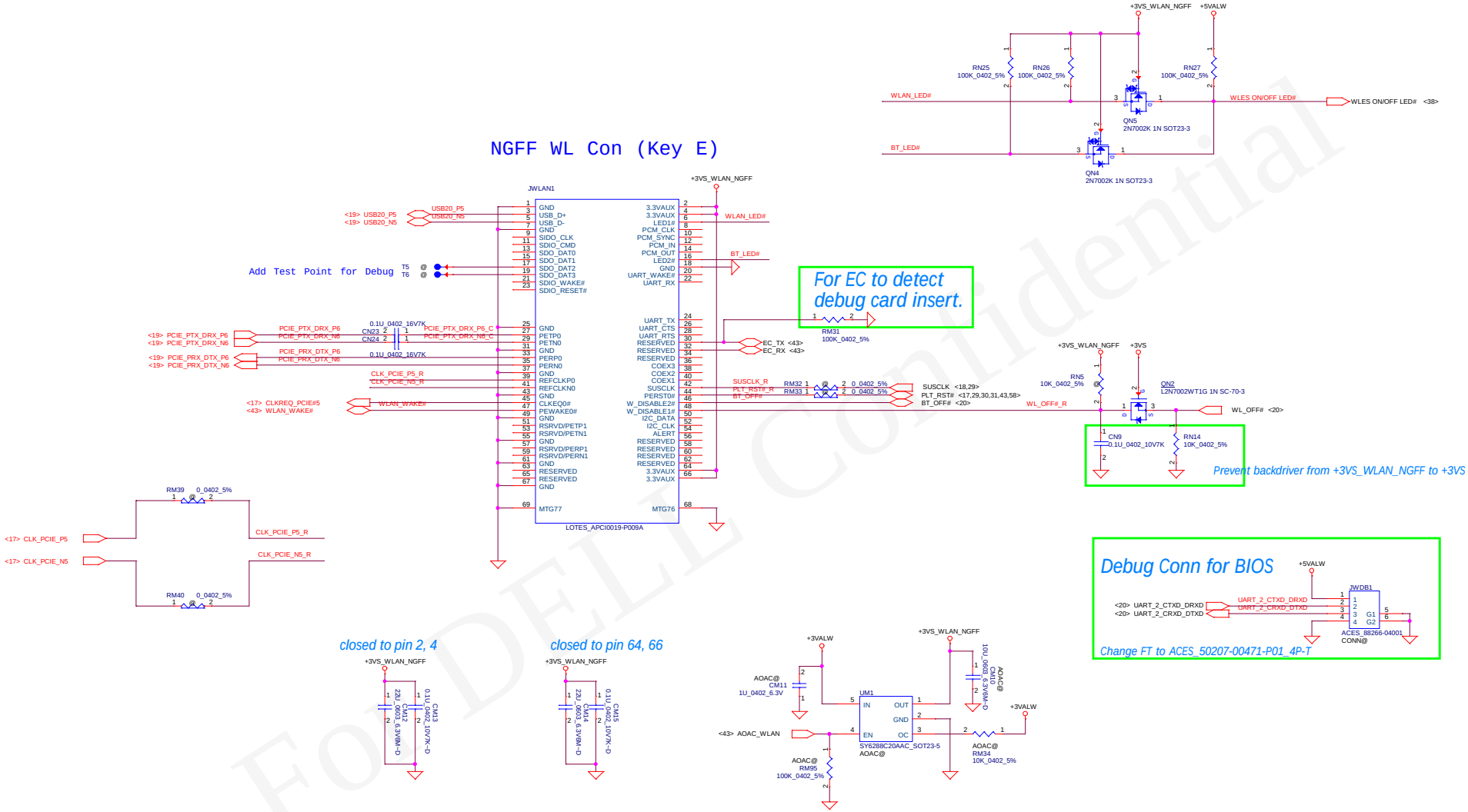
NGFF WL Con (Key E)



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Issued Date	2015/01/30	Deciphered Date 2016/12/31	Title: WLAN
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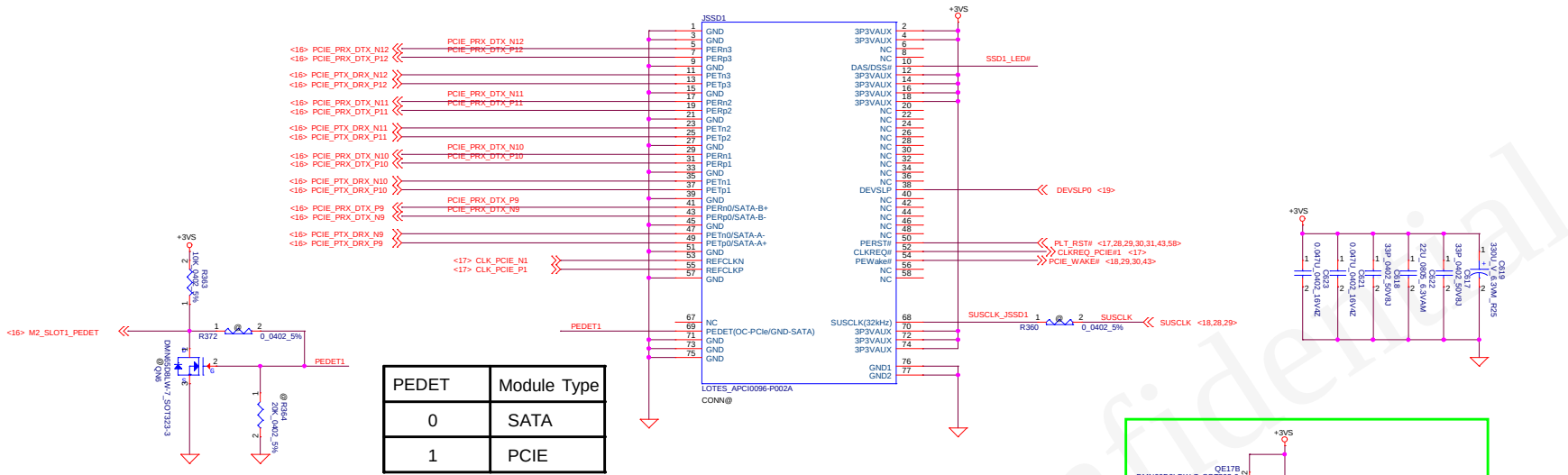
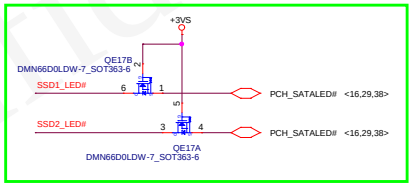
			Date: Wednesday, July 22, 2015; Sheet 28 of 78

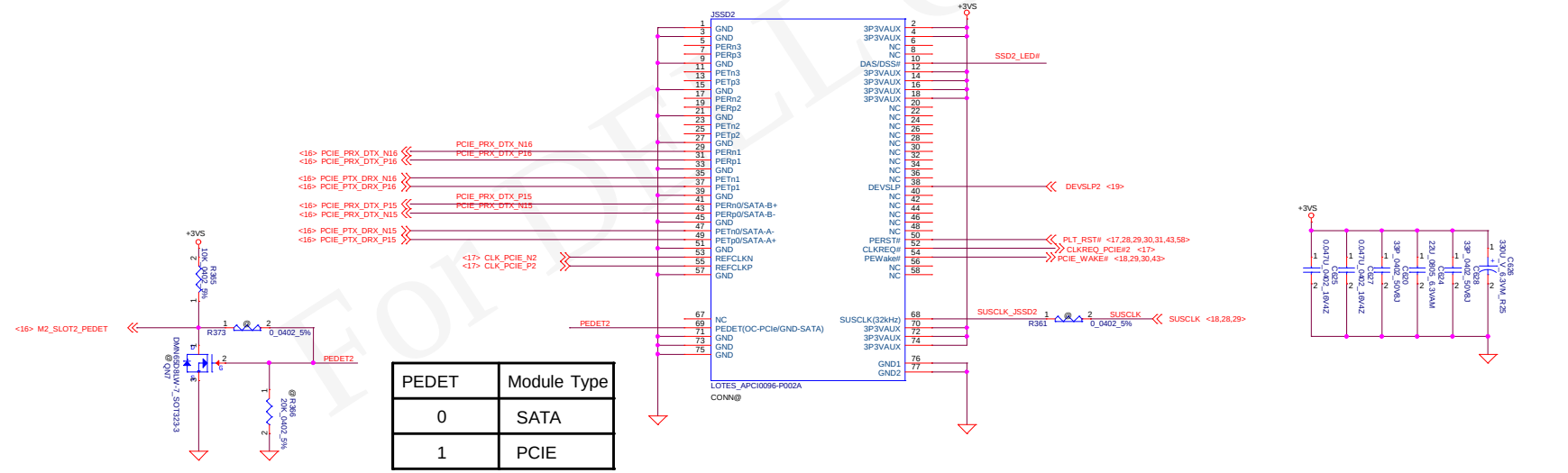
SSD
NGFF Slot_1 Key M



PEDET	Module Type
0	SATA
1	PCIE



SSD
NGFF Slot_2 Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/30	Deciphered Date 2016/12/31	Title: Mini Card/LED
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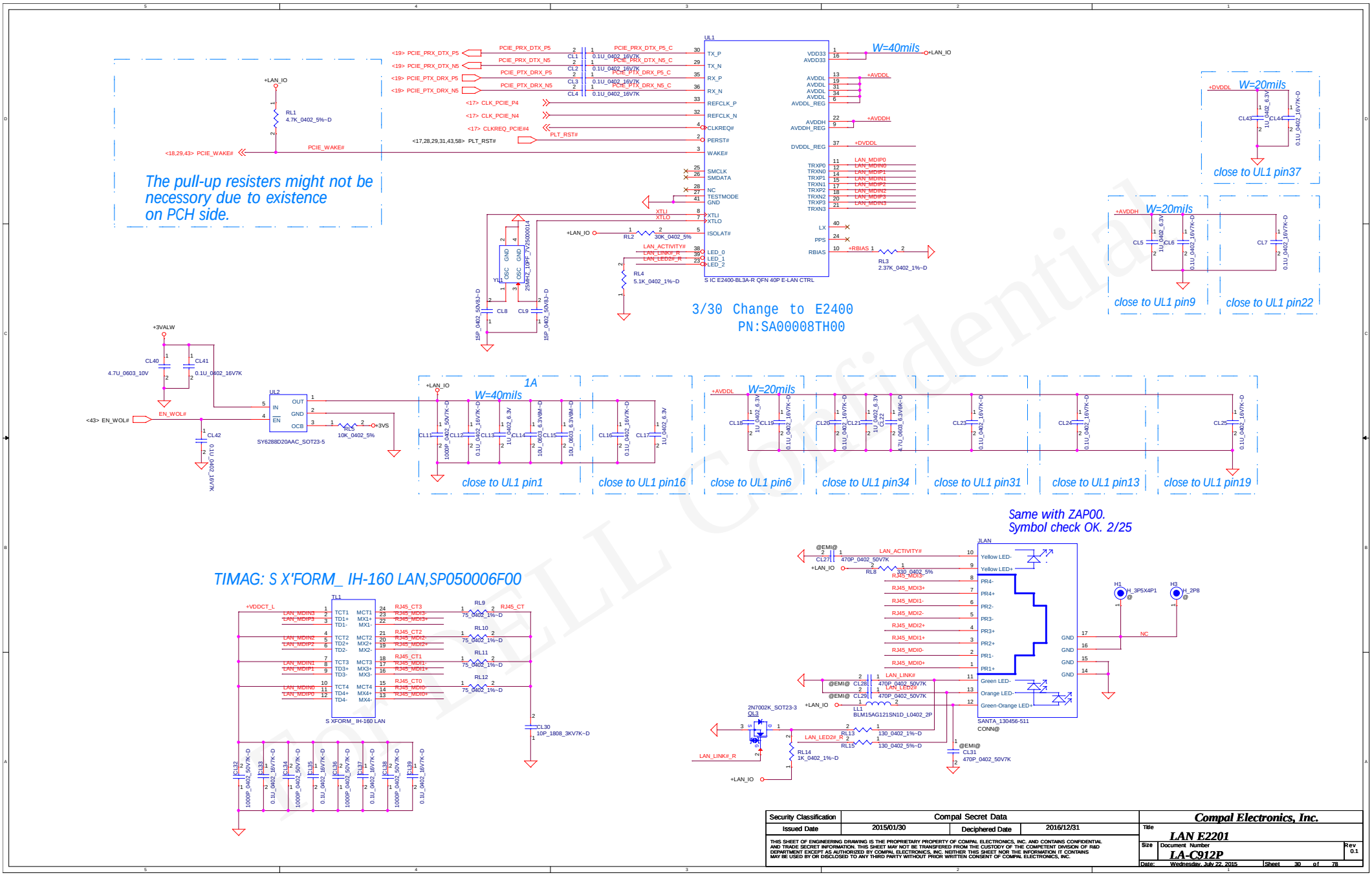
			Date: Wednesday, July 22, 2015 Sheet 29 of 78



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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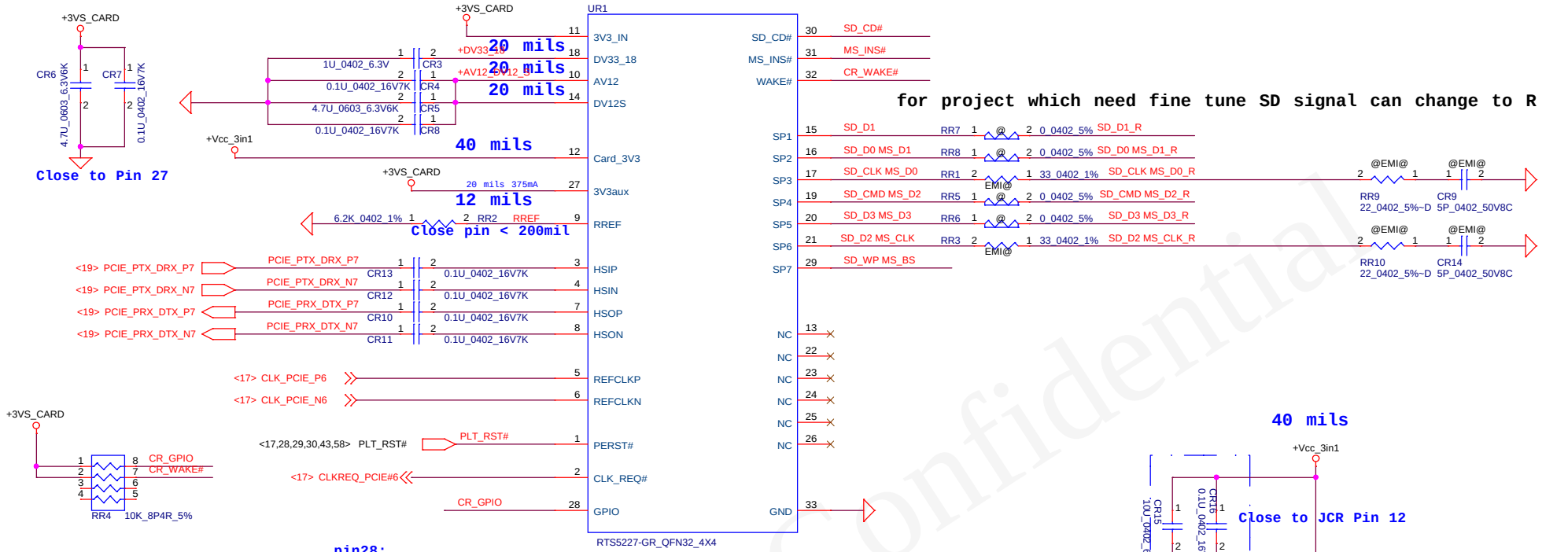
Compal Electronics, Inc.

Title: **LAN E2201**

Size: | Document Number: **LA-C912P** | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 30 of 78



	NO Card	SD Insert	MS Insert
15_SP1	PD80	SD_D1_PU80	PD80
16_SP2	PD80	SD_D0_PU80	MS_D1_PD80
17_SP3	PD80	SD_CLK_PD80	MS_D0_PD80
19_SP4	PD80	SD_CMD_PU80	MS_D2_PD80
20_SP5	PD80	SD_D3_PU80	MS_D3_PD80
21_SP6	PD80	SD_D2_PU80	MS_CLK_PD80
29_SP7	PD200	SD_WP_PD200	MS_BS_PD200
30_SD_CD#	PU200	PU200	PU200
31_MS_CD#	PU200	PU200	PU200

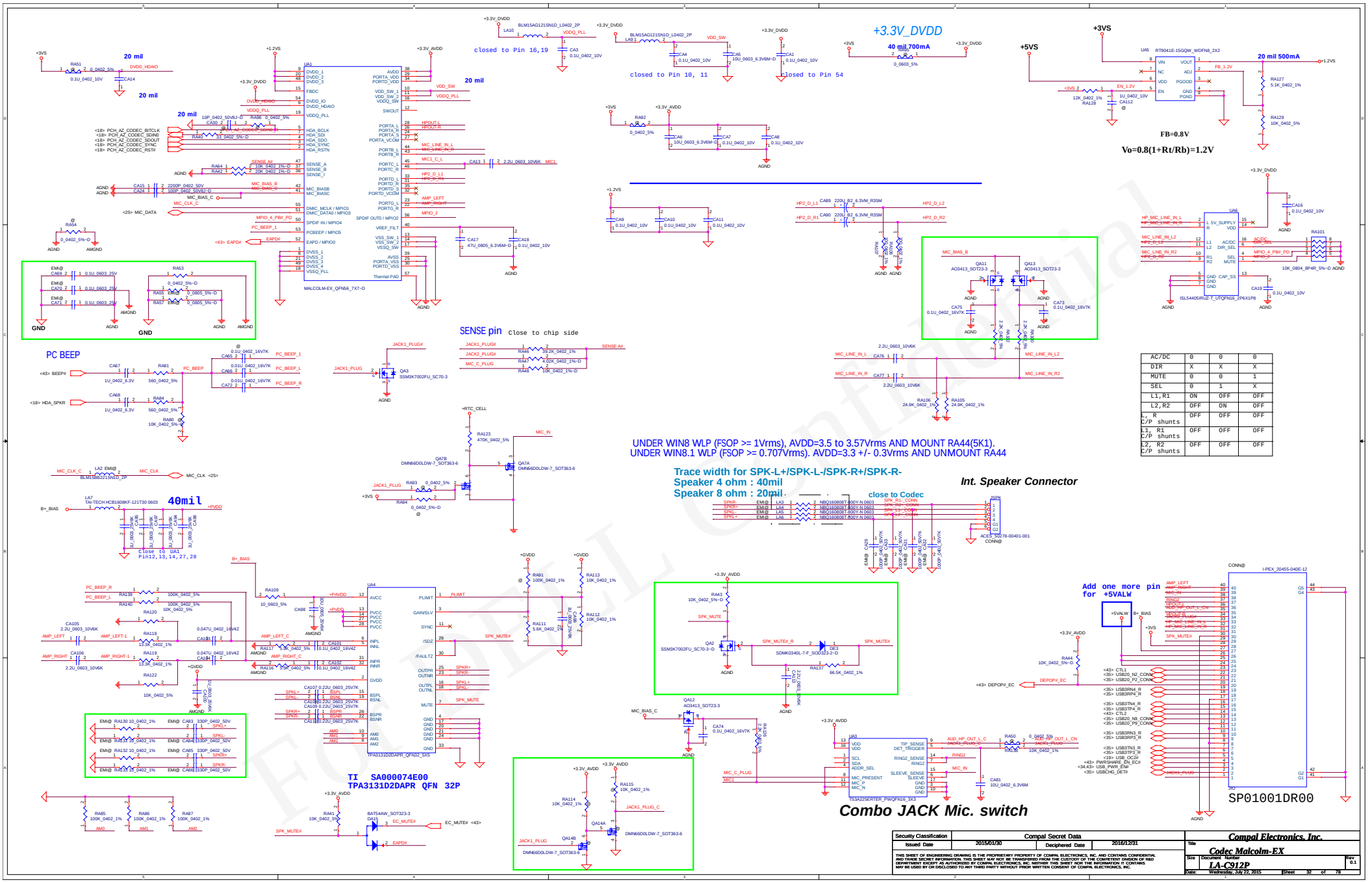
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **Card Reader RTS5179**

Size | Document Number: **LA-C912P** | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 31 of 78



AC/DC	0	0	0
DIR	X	X	X
MUTE	0	0	1
SEL	0	1	X
L1,R1	ON	OFF	OFF
L2,R2	OFF	ON	OFF
L, R C/P shunts	OFF	OFF	OFF
L1, R1 C/P shunts	OFF	OFF	OFF
L2, R2 C/P shunts	OFF	OFF	OFF

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: Codec Malcolm-EX

Size: Document Number: LA-C912P Rev: 0.1

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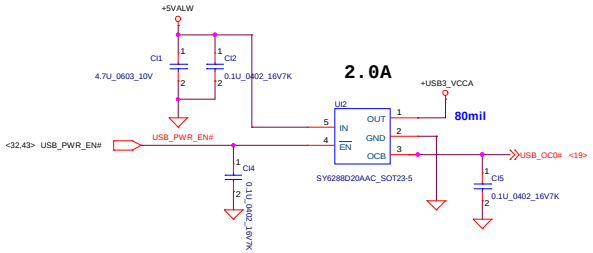
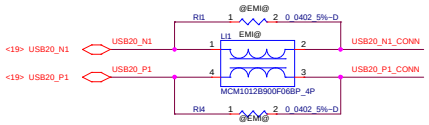
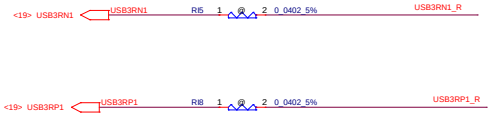
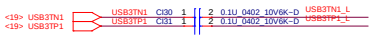
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.		
Title: Reserved Page		
Size	Document Number: LA-C912P	Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 33 of 78	



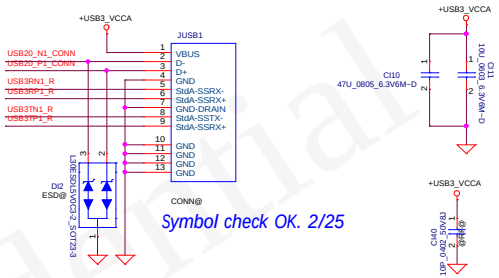


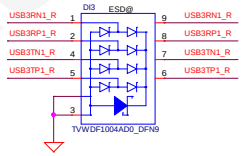




JUSB1

On MB (Right Side)

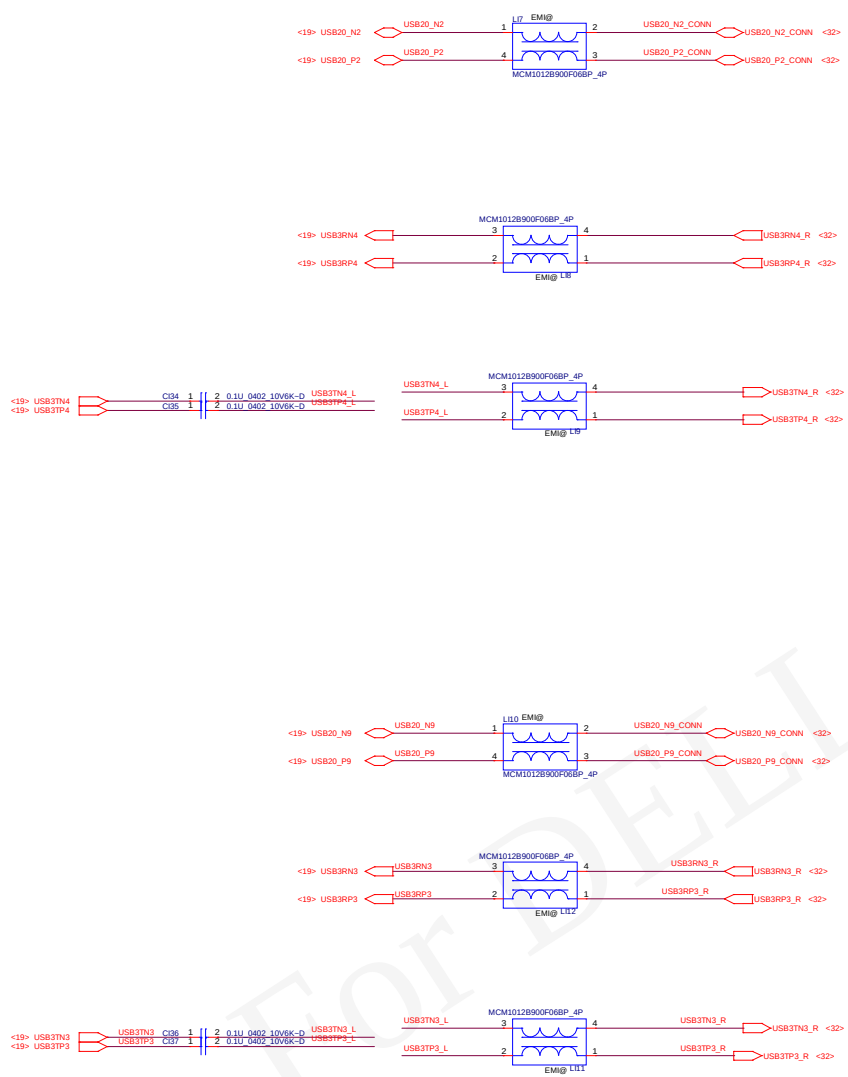


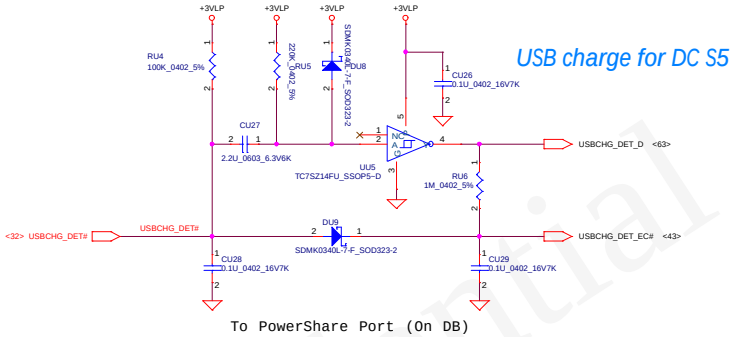


JUSB2 change to TypeC

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	USB 3.0/2.0 x2 (left side)
Size: Custom	Document Number: LA-C912P
Rev	0.1
Date: Wednesday, July 22, 2015	Sheet 34 of 78

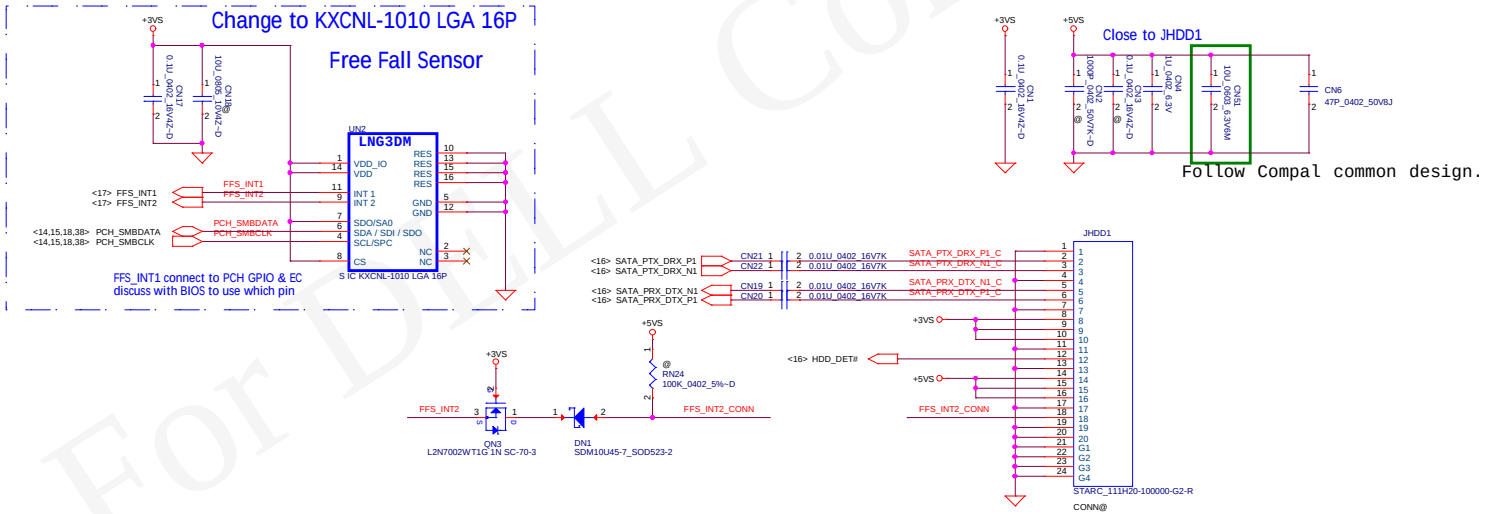




USB charge for DC S5

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: USB 3.0/2.0 x2 (left side)			
Size: Custom	Document Number: LA-C912P		Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet: 35 of 78		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/01/30	Deciphered Date 2016/12/31	Title: HDD/ODD
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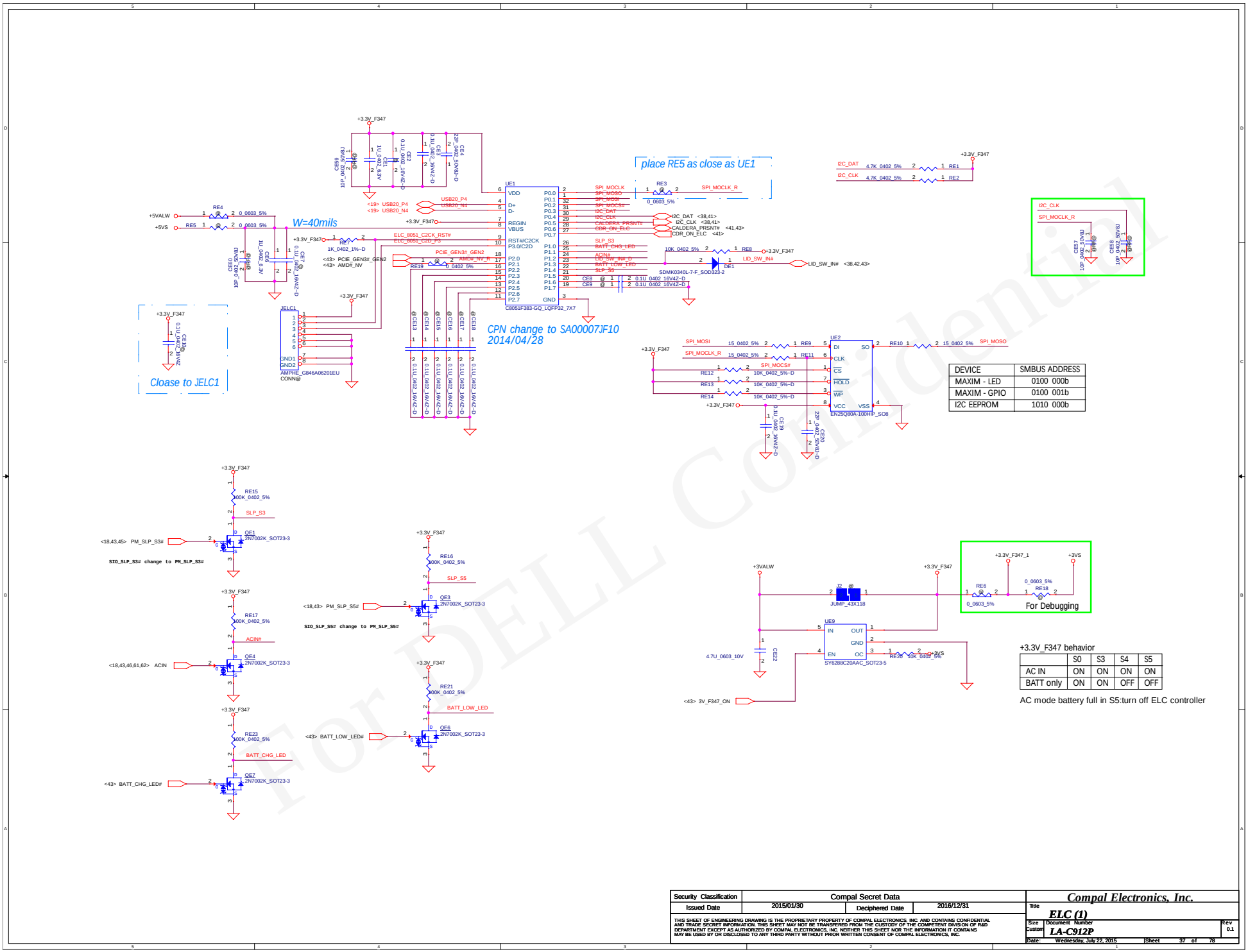
			Date: Wednesday, July 22, 2015; Sheet 36 of 78



DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

+3.3V_F347 behavior

	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BATT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

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Issued Date	2015/01/30	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

Title: ELC (1)

Size: Custom | Document Number: LA-C912P | Rev: 0.1

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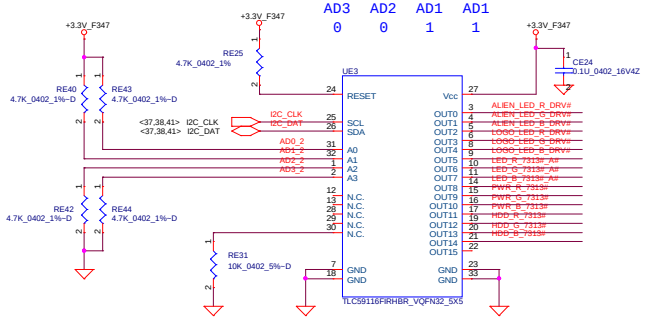
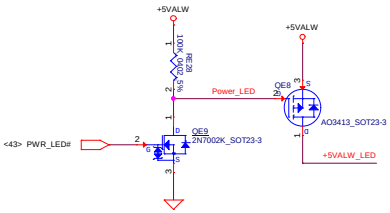
MAX7313 change to TI TLC59116F PWM expander

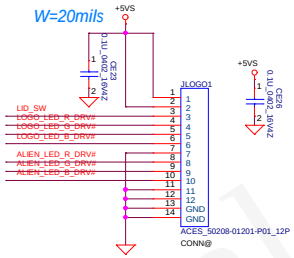
AD3 AD2 AD1 AD1
0 0 1 1



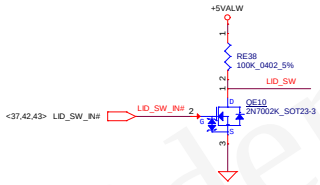
Power LED



W=20mils

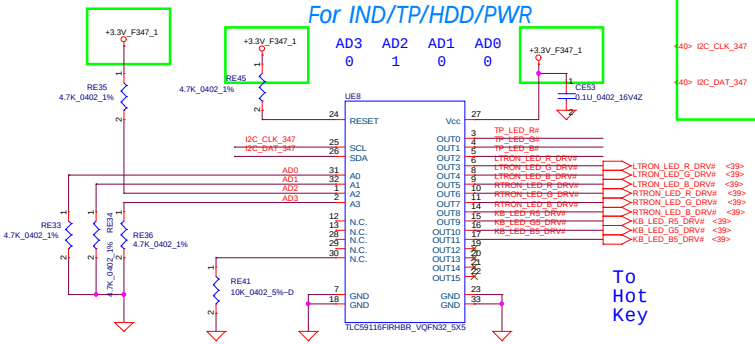


Logic up LED board

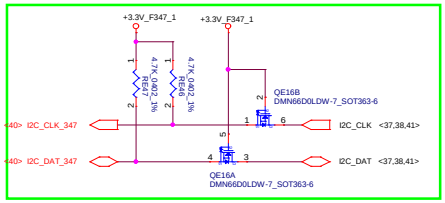


For IND/TP/HDD/PWR

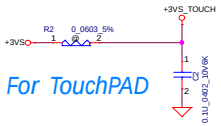
AD3 AD2 AD1 AD0
0 1 0 0



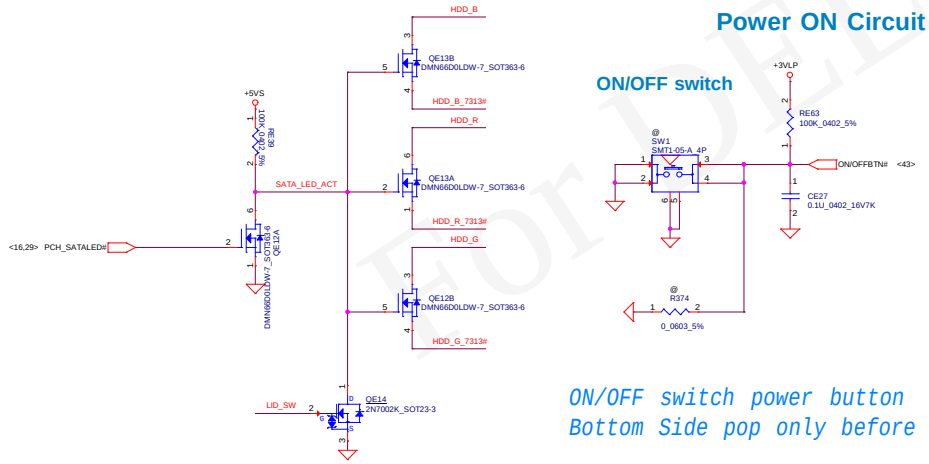
To Hot Key



For TouchPAD



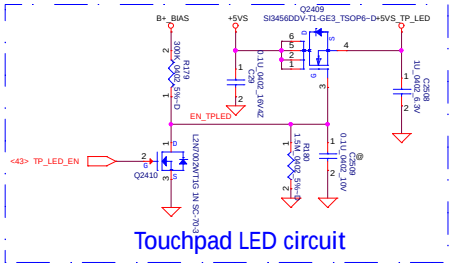
Power ON Circuit

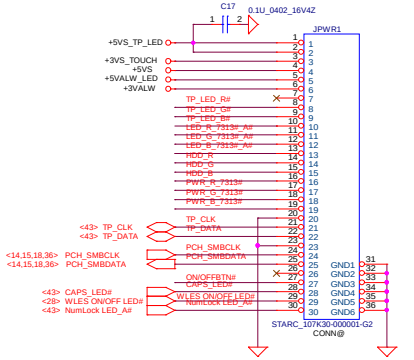


ON/OFF switch

ON/OFF switch power button
Bottom Side pop only before MP

Touchpad LED circuit





Change Symbol OK
2/18 -Tarry

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Issued Date	2015/01/30	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

Title: ELC (2)/TP/PWR SW

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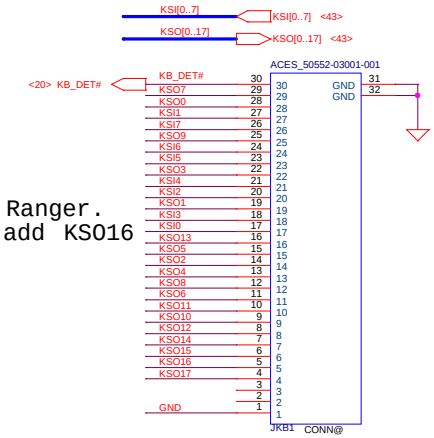
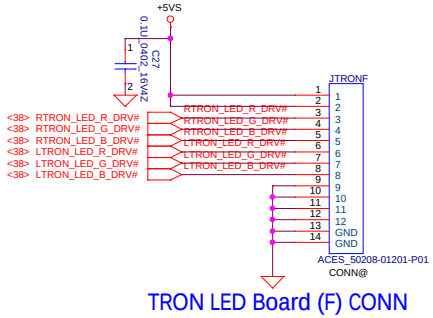
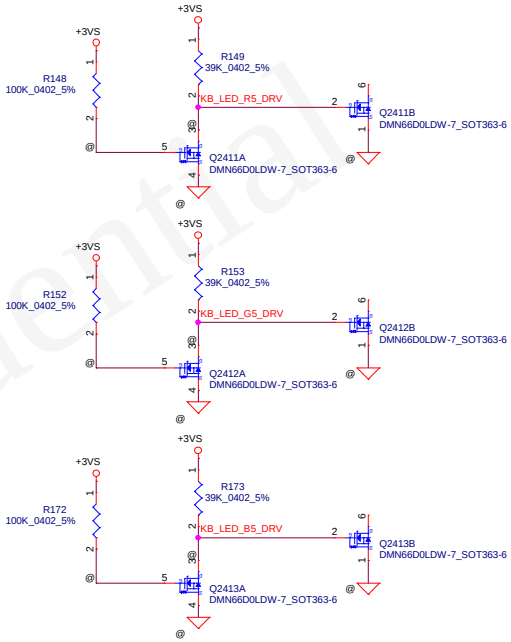
INT_KBD Conn.



Net follow Ranger.
Only Pin26 add KSO16

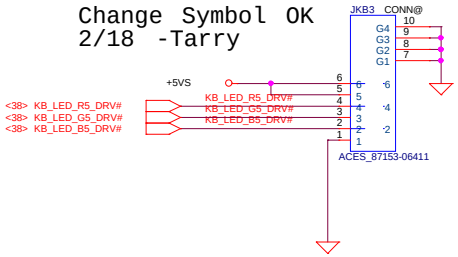


TRON LED Board (F) CONN

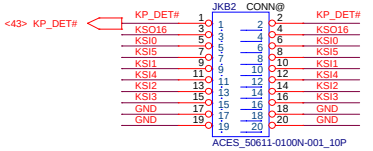


Hot Key Conn.
PWM

Change Symbol OK
2/18 -Tarry



Hot Key Conn.
Key Pad



Compal Electronics, Inc.		
Title: KB/HotKey conn		
Size	Document Number: LA-C912P	Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 39 of 78	

1/28 ADD

+5VS RE104 1 @ 2 0_0603_5% +5V_LED

+3VS RE105 1 @ 2 0_0603_5%

K/B Backlight

AD3	AD2	AD1	AD0
0	0	1	0

+3.3V_F347_1

RE32 4.7K_0402_1%

RE26 4.7K_0402_1%~D

RE29 4.7K_0402_1%~D

RE30 4.7K_0402_1%

RE27 4.7K_0402_1%

RE37 10K_0402_5%

CE25 0.1U_0402_16V4Z

UE4 TLC59116FIRHBR_VQFN32_5X5

RESET, Vcc, SCL, SDA, A0, A1, A2, A3, N.C., GND, OUT0–OUT15

I2C_CLK_347, I2C_DAT_347, AD0_1, AD1_1, AD2_1, AD3_1

KB_LED_R1_DRV#, KB_LED_G1_DRV#, KB_LED_B1_DRV#, KB_LED_R2_DRV#, KB_LED_G2_DRV#, KB_LED_B2_DRV#, KB_LED_R3_DRV#, KB_LED_G3_DRV#, KB_LED_B3_DRV#, KB_LED_R4_DRV#, KB_LED_G4_DRV#, KB_LED_B4_DRV#

JKBBL1 ACES_50552-02001-001 CONN@

+5VS

KB BL LED

+5V_LED, +3VS

R144 39K_0402_5% KB_LED_R1_DRV
R146 100K_0402_5% KB_LED_R1_DRV#
Q28A DMN66D0LDW-7_SOT363-6
Q28B DMN66D0LDW-7_SOT363-6

R145 39K_0402_5% KB_LED_R3_DRV
R147 100K_0402_5% KB_LED_R3_DRV#
Q34A DMN66D0LDW-7_SOT363-6
Q34B DMN66D0LDW-7_SOT363-6

R150 39K_0402_5% KB_LED_G1_DRV
R154 100K_0402_5% KB_LED_G1_DRV#
Q29A DMN66D0LDW-7_SOT363-6
Q29B DMN66D0LDW-7_SOT363-6

R151 39K_0402_5% KB_LED_G3_DRV
R155 100K_0402_5% KB_LED_G3_DRV#
Q35A DMN66D0LDW-7_SOT363-6
Q35B DMN66D0LDW-7_SOT363-6

R156 39K_0402_5% KB_LED_B1_DRV
R158 100K_0402_5% KB_LED_B1_DRV#
Q30A DMN66D0LDW-7_SOT363-6
Q30B DMN66D0LDW-7_SOT363-6

R157 39K_0402_5% KB_LED_B3_DRV
R159 100K_0402_5% KB_LED_B3_DRV#
Q36A DMN66D0LDW-7_SOT363-6
Q36B DMN66D0LDW-7_SOT363-6

R160 39K_0402_5% KB_LED_R2_DRV
R162 100K_0402_5% KB_LED_R2_DRV#
Q31A DMN66D0LDW-7_SOT363-6
Q31B DMN66D0LDW-7_SOT363-6

R161 39K_0402_5% KB_LED_R4_DRV
R163 100K_0402_5% KB_LED_R4_DRV#
Q37A DMN66D0LDW-7_SOT363-6
Q37B DMN66D0LDW-7_SOT363-6

R164 39K_0402_5% KB_LED_G2_DRV
R166 100K_0402_5% KB_LED_G2_DRV#
Q32A DMN66D0LDW-7_SOT363-6
Q32B DMN66D0LDW-7_SOT363-6

R165 39K_0402_5% KB_LED_G4_DRV
R167 100K_0402_5% KB_LED_G4_DRV#
Q38A DMN66D0LDW-7_SOT363-6
Q38B DMN66D0LDW-7_SOT363-6

R168 39K_0402_5% KB_LED_B2_DRV
R170 100K_0402_5% KB_LED_B2_DRV#
Q33A DMN66D0LDW-7_SOT363-6
Q33B DMN66D0LDW-7_SOT363-6

R169 39K_0402_5% KB_LED_B4_DRV
R171 100K_0402_5% KB_LED_B4_DRV#
Q39A DMN66D0LDW-7_SOT363-6
Q39B DMN66D0LDW-7_SOT363-6

Compal Electronics, Inc.	
Title	ELC(3)
Size	Document Number: LA-C912P
Rev	0.1
Date:	Wednesday, July 22, 2015
Sheet	40 of 78

EC 控制 P_IN
PCI_SMCLK
PCI_SMDAT
USB_PWR_EN#
DOCKING_LED ON#
DOCKING_LED OFF#
DOCK_PSID
DOCK_ACIN
DOCK_EN
PRSNT#_R

PCIE_CLK_BUFFER

Caldera connector

Follow ZAP00 design.

CDRA_LED WHITE 20mil
CDRA_LED WHITE_R_R 20mil

CDRA_LED RED 20mil
CDRA_LED RED_R_R 20mil

221 ohm for white LED
316 ohm for red LED
on dock cable side

To PCH

Form Caldera

Tie 1kΩ to VDD = Register Access SMBus Slave mode
FLOAT = Read External EEPROM (Master SMBUS Mode)
Tie 1kΩ to GND = Pin Mode

Tie 1kΩ to GND = Root Complex Loopback (INA_n to OUTA_n
Float = Normal Operation
Tie 1kΩ to VDD = End-point Loopback (INB_n to OUTA_n)

Tie 1kΩ to GND = GEN 1,2
Float = Auto Rate select
Tie 20kΩ to GND = GEN 3 without De-emphasis
Tie 1kΩ to VDD = GEN 3 with De-emphasis

Auto RX-Detect

EQ Set ting

Level	EQ(A) TYPE	EQ(A) DC	db at 2.5G	db at 4G	Suggested Use
1	0	0	3.7	4.9	< 5 inch trace
2	0	R	5.8	7.9	5 inch 5- 6 trace
3	0	F	7.7	9.9	5 inch 6- 8 trace
4	R	1	9.9	11	10 inch 5- 6 trace
5	R	0	11.2	14.3	10 inch 6- 8 trace
6	R	R	11.4	14.6	15 inch 6- 8 trace
7	R	F	13.5	17	20 inch 6- 8 trace
8	R	1	15	18.5	25 to 30 inch 6- 8 trace
9	F	0	12.8	18	30 inch 6- 8 trace
10	F	R	17.4	22	35 inch 6- 8 trace
11	F	F	19.7	24.4	10m, 30awg cable
12	F	1	21.1	25.8	10m- 12 meable
13	1	0	21.7	27.4	
14	1	R	23.5	29.9	
15	1	F	25.8	31.4	
16	1	1	27.3	32.7	

DEMA Set ting

Level	DEMA(A) DEMB(A)	DEMA(B) DEMB(B)	DEM dB	Suggested Use
1	0	0	0	<5 inch 4- 8 trace
2	0	R	0	<5 inch 4- 8 trace
3	0	F	-2.5	10 inch 4- 8 trace
4	R	0	0	<5 inch 4- 8 trace
5	R	0	-2.5	10 inch 4- 8 trace
6	R	R	-0	15 inch 4- 8 trace
7	R	F	0	<5 inch 4- 8 trace
8	R	1	-3.5	10 inch 4- 8 trace
9	F	0	-0	15 inch 4- 8 trace
10	F	R	0	<5 inch 4- 8 trace
11	F	F	-3.5	10 inch 4- 8 trace
12	F	1	-0	15 inch 4- 8 trace
13	1	0	0	<5 inch 4- 8 trace
14	1	R	-3.5	10 inch 4- 8 trace
15	1	F	-0	15 inch 4- 8 trace
16	1	1	-0	20 inch 4- 8 trace

Level control Set ting

Level	Pin Set ting	Description
1	0	1kΩ to GND
2	R	20kΩ to GND
3	F	Float
4	1	1kΩ to VDD

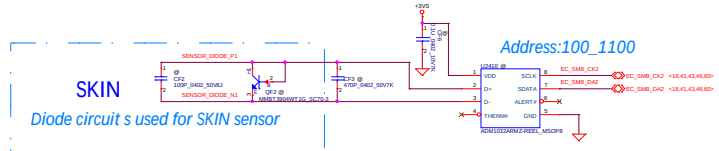
EQ*MB

DEM*EGPU

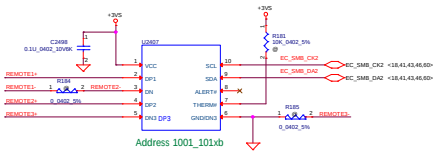
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/01/30	Deciphered Date	2014/12/30	Title: USB3.0
			Size: Document Number: LA-C912P	Rev: 0.1
			Date: Wednesday, April 09, 2014	Sheet 45 of 56

SKIN

Diode circuit s used for SKIN sensor

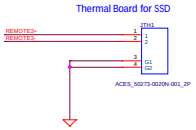


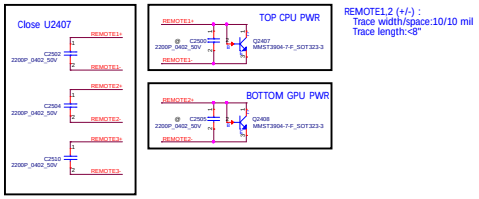
Fintek thermal sensor-> CPU core, DIMM



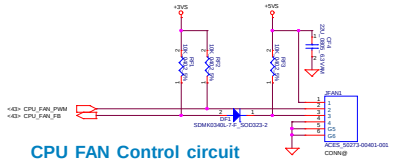
2nd source
SA000029210-->EMC1403-2-AIZL-TR

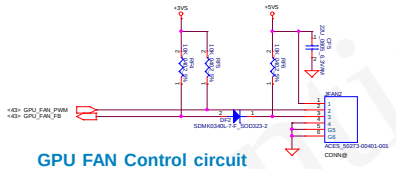
Thermal Board for SSD





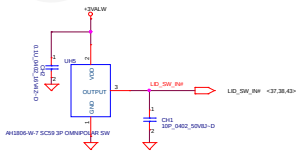
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"





Lid Switch

(Hall Effect Switch)



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Issued Date	2015/01/30	Deciphered Date	2016/12/31
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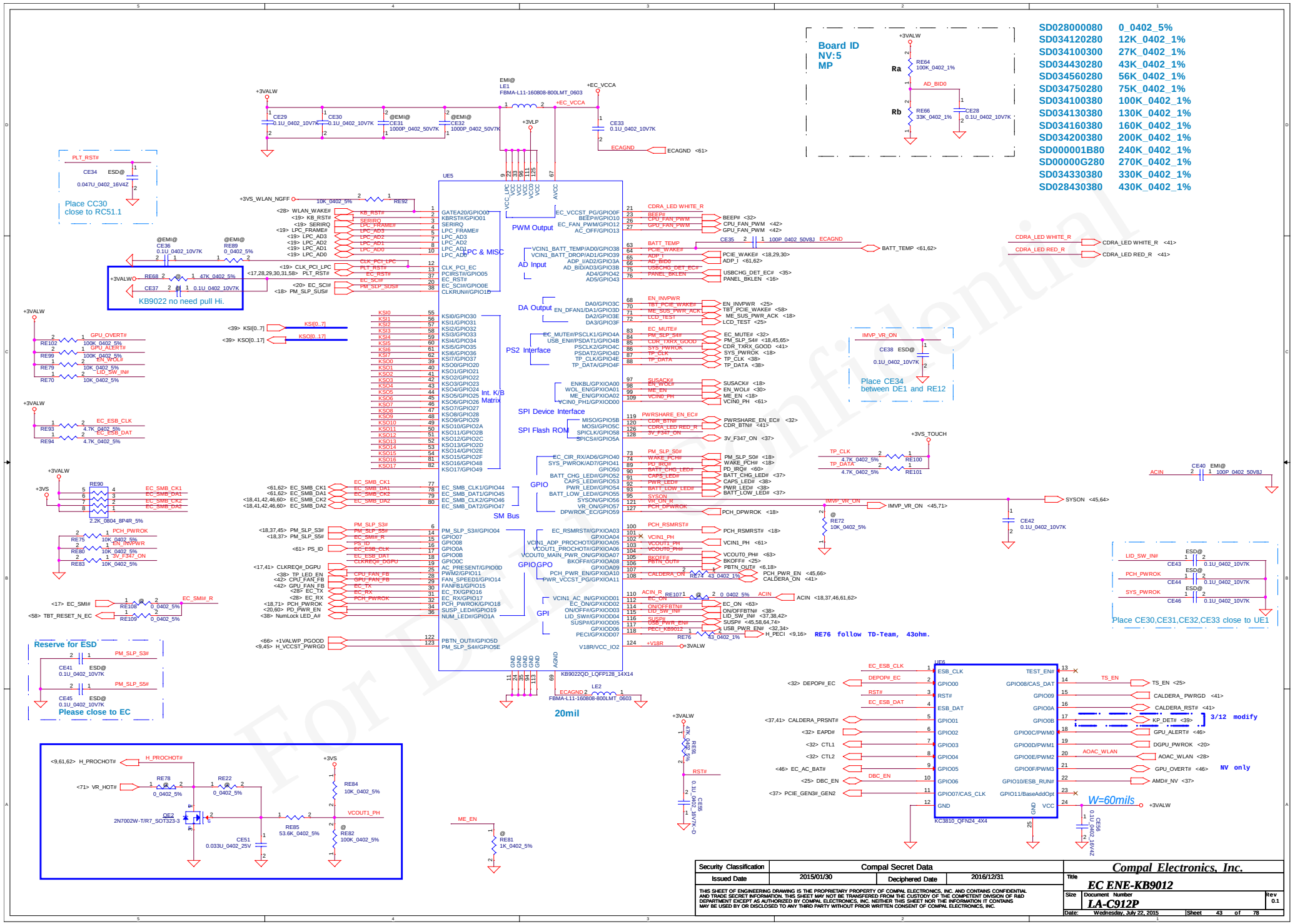
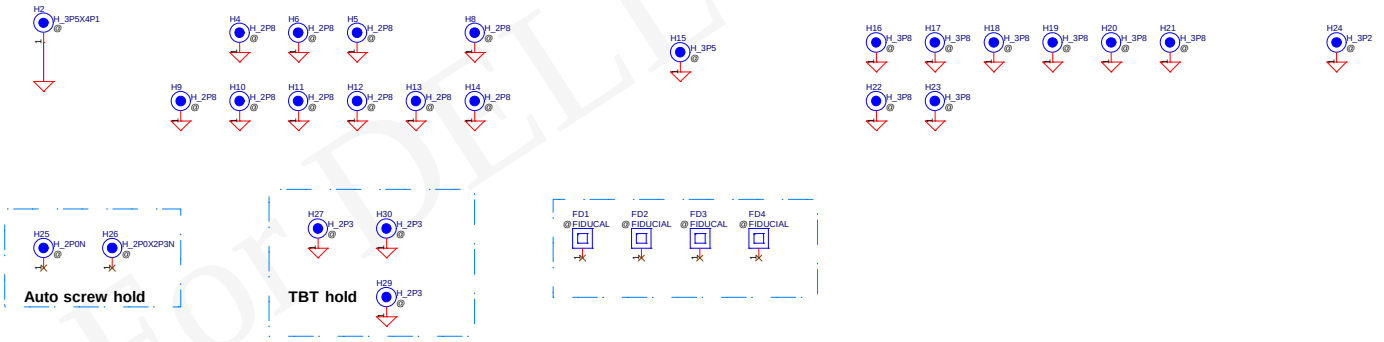
			Size: Document Number: LA-C912P Rev: 0.1
			Date: Wednesday, July 22, 2015 Sheet 42 of 78



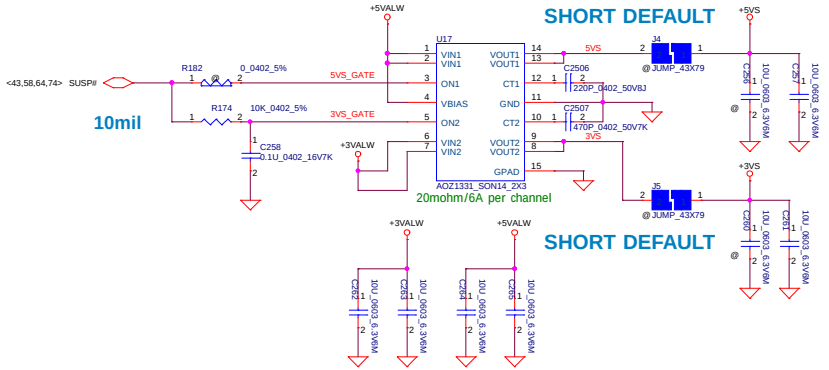
Screw Hole



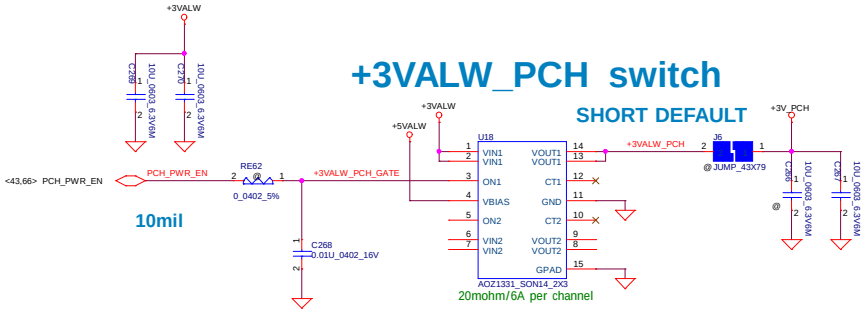
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.		
Title: Screw Hole		
Size	Document Number: LA-C912P	Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 44 of 78	

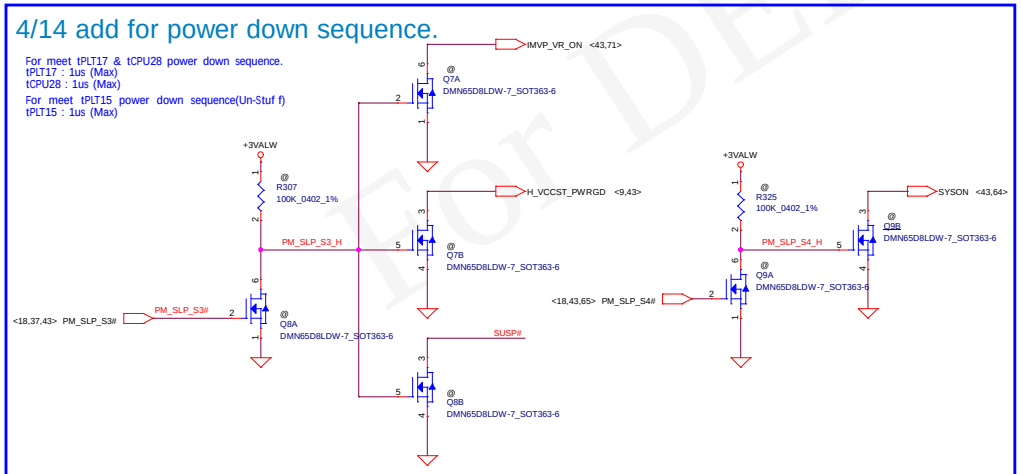
+5VS and +3VS switch



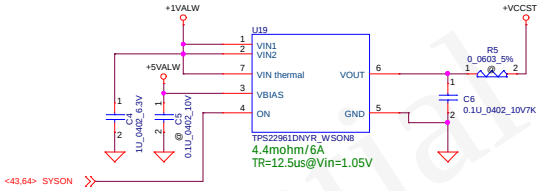
+3VALW_PCH switch



4/14 add for power down sequence.

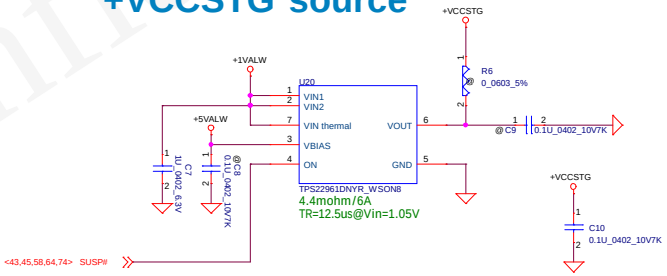


+VCCST Load Switch



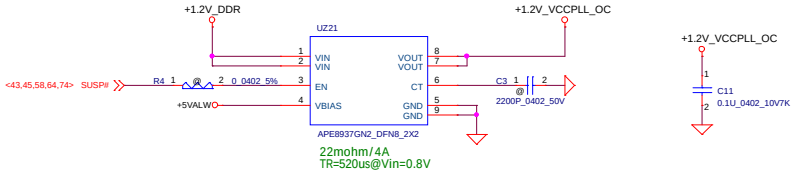
Main source ☐TI SA00007XR00 (S IC TPS22961DNYR WSON 8P LOAD SWITCH)
2nd source ☐AOS SA00008A800 (S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW)
3rd source ☐EMC SA00008R600 (S IC EM5201V DFN3X3 8P LOAD SWITCH)
4st source ☐APEC SA00006V300 (S IC APE8939GN3 DFN 8P LOAD SWITCH)

+VCCSTG source



Main source ☐TI SA00007XR00 (S IC TPS22961DNYR WSON 8P LOAD SWITCH)
2nd source ☐AOS SA00008A800 (S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW)
3rd source ☐EMC SA00008R600 (S IC EM5201V DFN3X3 8P LOAD SWITCH)
4st source ☐APEC SA00006V300 (S IC APE8939GN3 DFN 8P LOAD SWITCH)

+1.2V_VCCPLL_OC



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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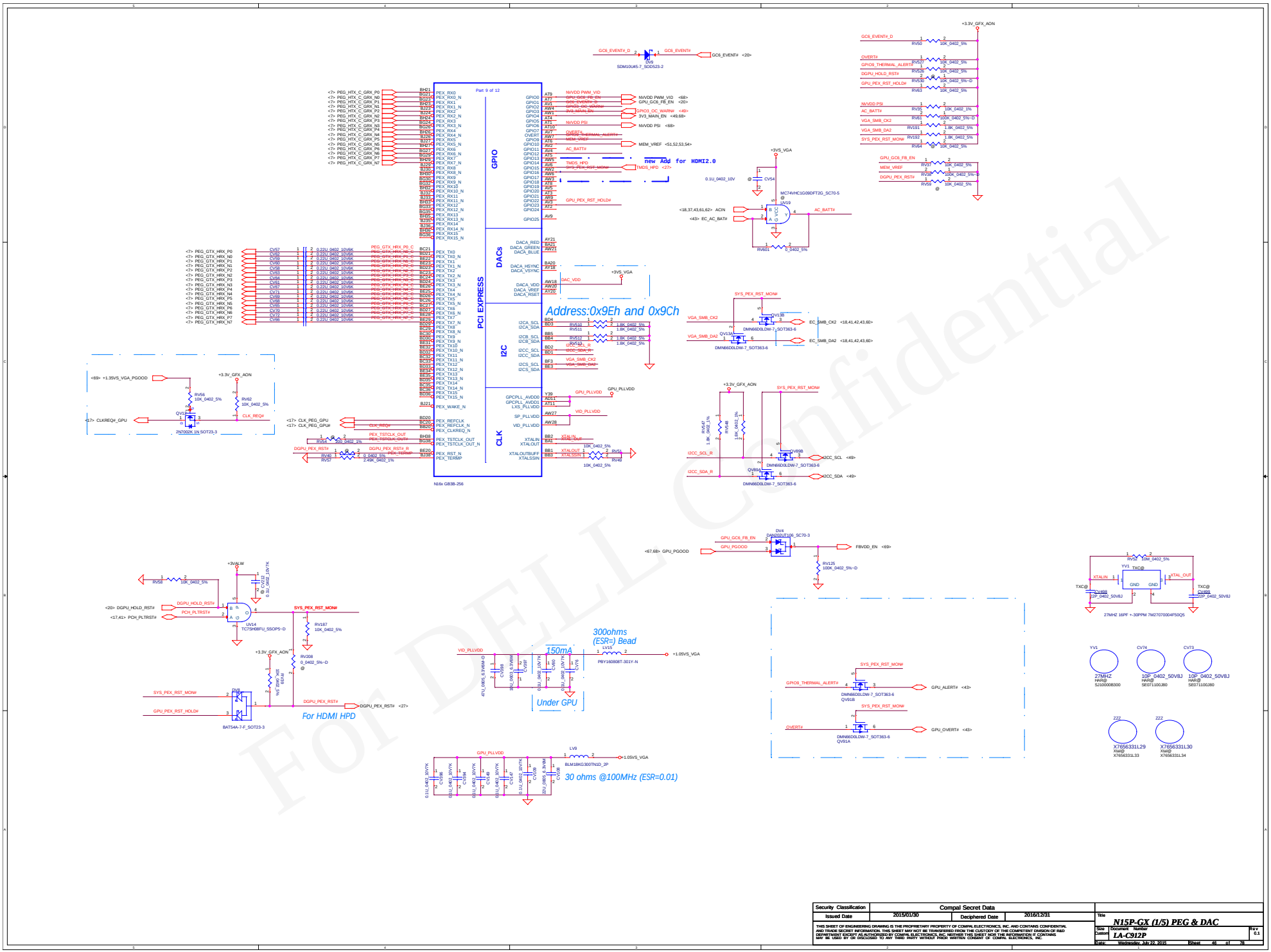
Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: LA-C912P		Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 45 of 78		



Security Classification	Compal Secret Data	
Issued Date	2015/01/30	Deciphered Date 2016/12/31

Title: N15P-GX (1/5) PEG & DAC

Size: Document Number: LA-C912P Rev: 0.1

Date: Wednesday, July 22, 2015 Sheet 46 of 78

Part 10 of 12

LVDS/TMDS

NC

TEST

SERIAL

GENERAL

new Add for HDMI2.0

trace width: 16mils
differential voltage sensing.
differential 50ohm signal routing.

Part 12 of 12

N16x GB3B-256

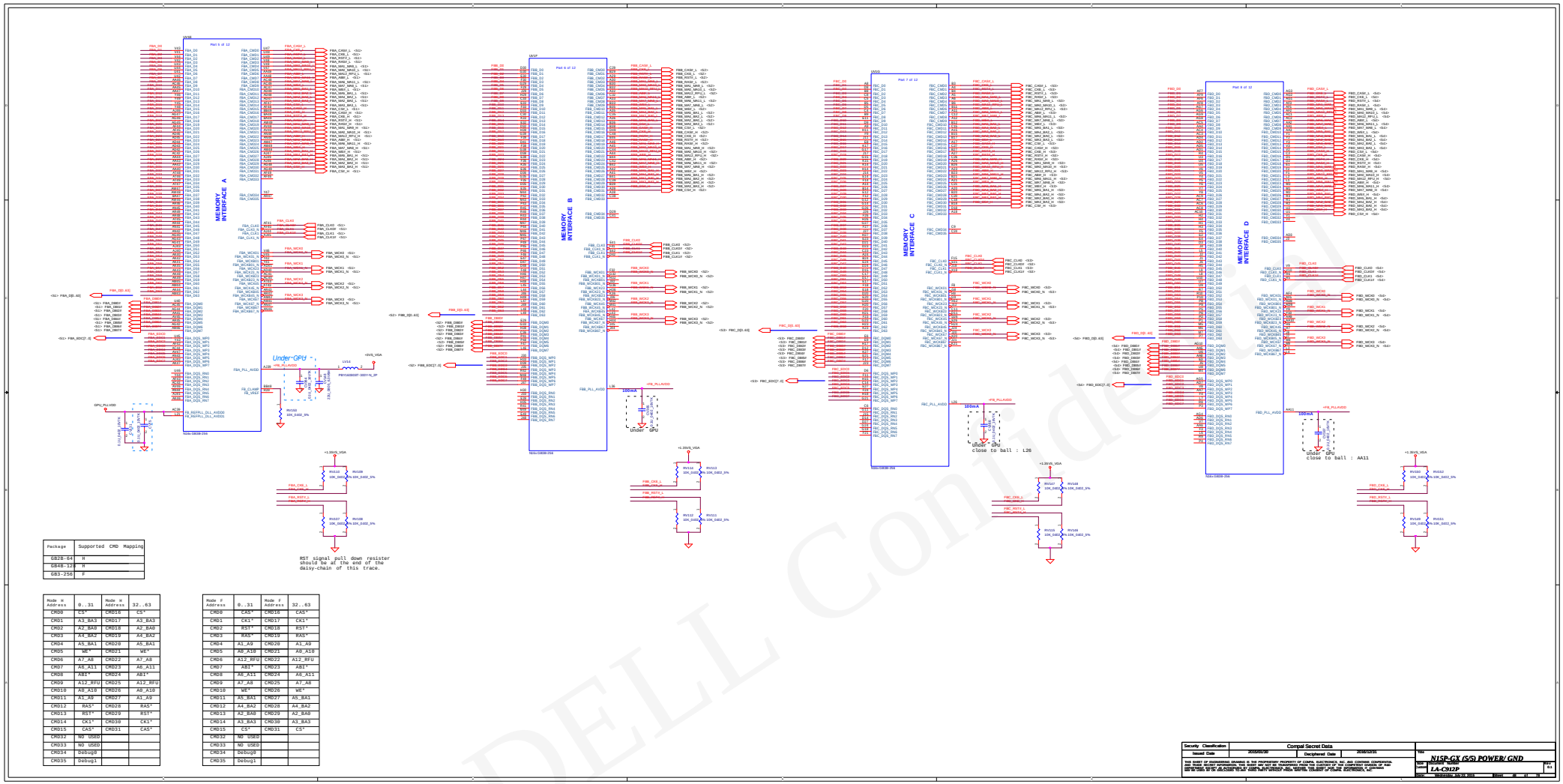
W25X20CL 2M-Bit/256K-byte
SA00003GM30

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Title: N15P-GX (1/5) PEG & DAC

Size: B | Document Number: LA-C912P | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 47 of 78

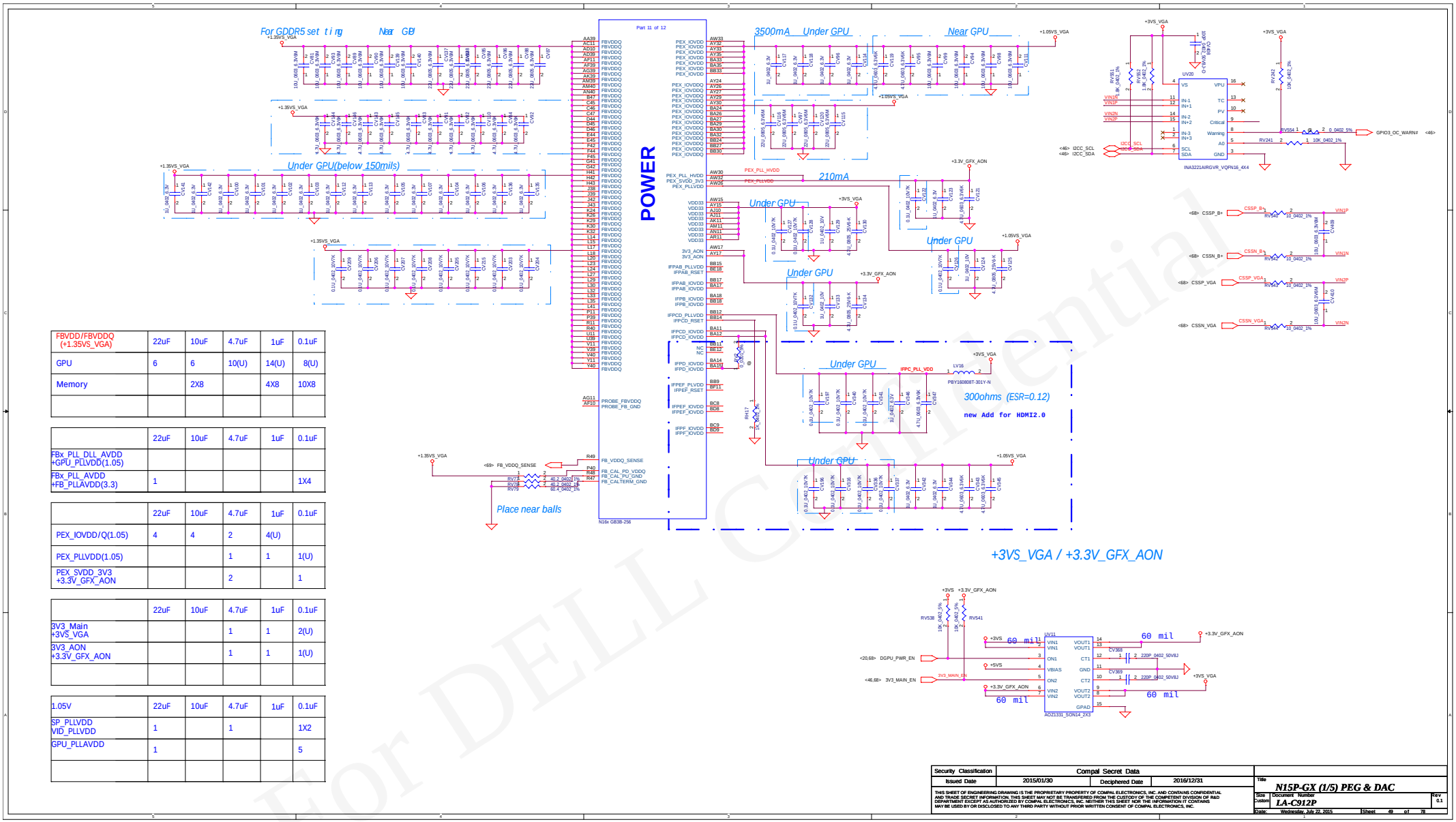


Package	Supported CMD Mapping
GB2B-64	H
GB4B-128	H
GB3-256	F

Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A8_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A9_A10	CMD26	A9_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Mode F Address	0..31	Mode F Address	32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CK1*	CMD17	CK1*
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A9_A10	CMD21	A9_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	AB1*	CMD23	AB1*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		Title
Issued Date	2015/01/20	Deciphered Date	2015/12/31	N15P-GX (GS) POWER/ GND
			Size: C	Document Number: LA-C912P	Rev: 0.1
			Date: Wednesday, July 29, 2015	Sheet 48 of 51



FBVDD/FBVDDQ (+1.35VS_VGA)	22uF	10uF	4.7uF	1uF	0.1uF
GPU	6	6	10(U)	14(U)	8(U)
Memory		2X8		4X8	10X8

	22uF	10uF	4.7uF	1uF	0.1uF
FBx_PLL_DLL_AVDD +GPU_PLLVDD(1.05)					
FBx_PLL_AVDD +FB_PLLAVDD(3.3)	1				1X4

	22uF	10uF	4.7uF	1uF	0.1uF
PEX_IOVDD/Q(1.05)	4	4	2	4(U)	
PEX_PLLVDD(1.05)			1	1	1(U)
PEX_SVDD_3V3 +3.3V_GFX_AON			2		1

	22uF	10uF	4.7uF	1uF	0.1uF
3V3_Main +3VS_VGA			1	1	2(U)
3V3_AON +3.3V_GFX_AON			1	1	1(U)

1.05V	22uF	10uF	4.7uF	1uF	0.1uF
SP_PLLVDD VID_PLLVDD	1		1		1X2
GPU_PLLAVDD	1				5

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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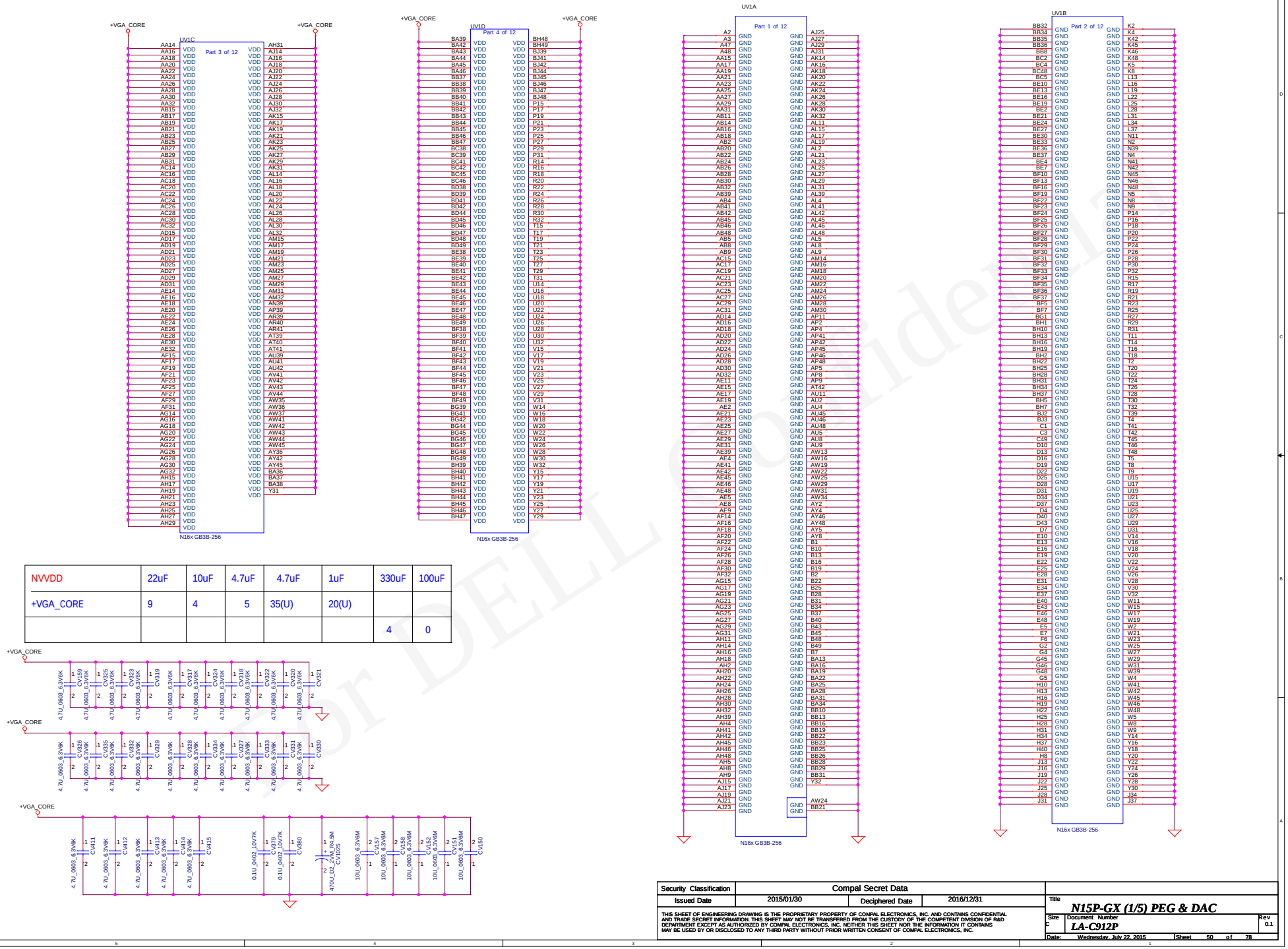
Title: *N15P-GX (1/5) PEG & DAC*

Size: C-custom | Document Number: *LA-C912P* | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 49 of 78



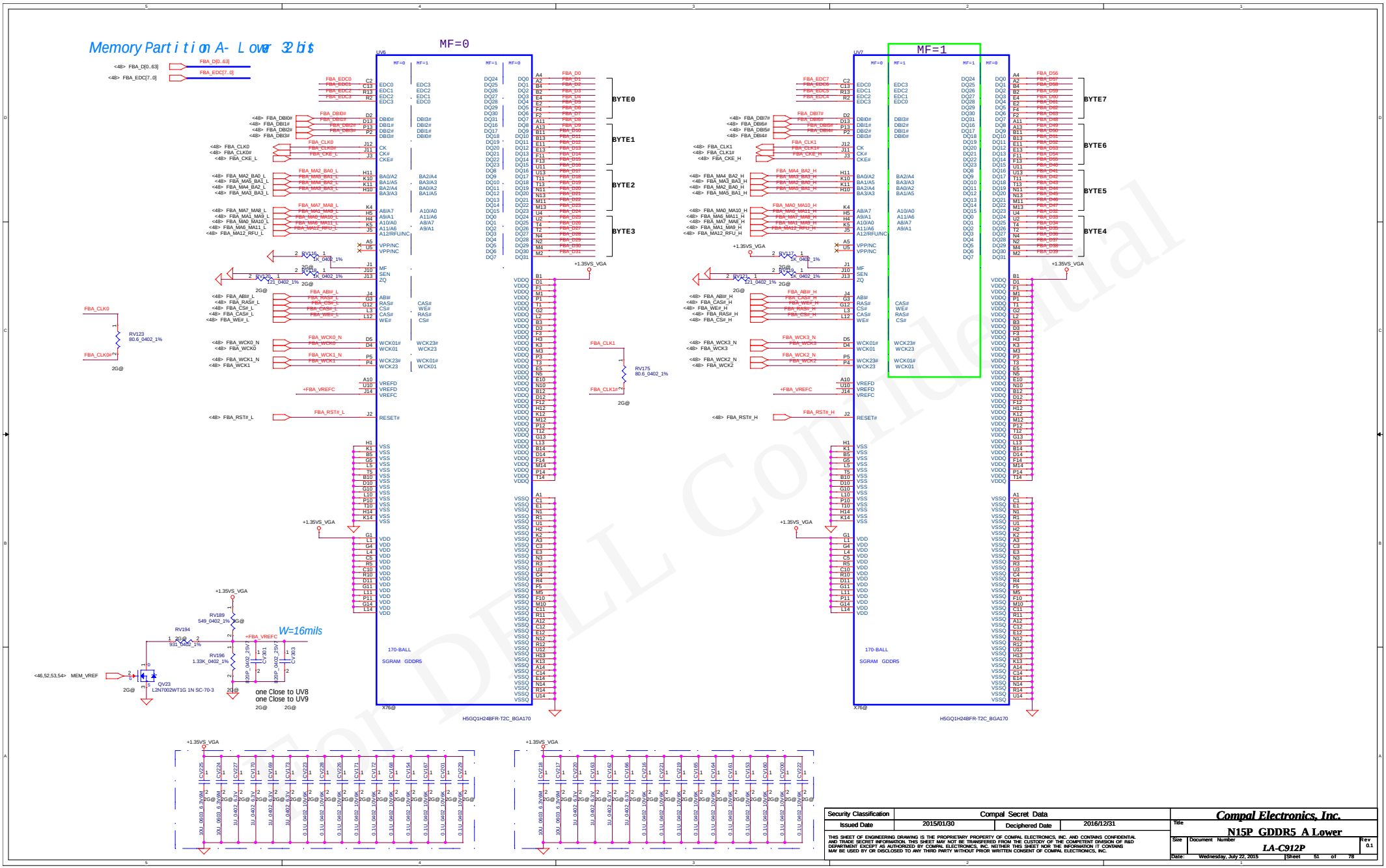
NVVDD	22uF	10uF	4.7uF	4.7uF	1uF	330uF	100uF
+VGA_CORE	9	4	5	35(U)	20(U)		
						4	0

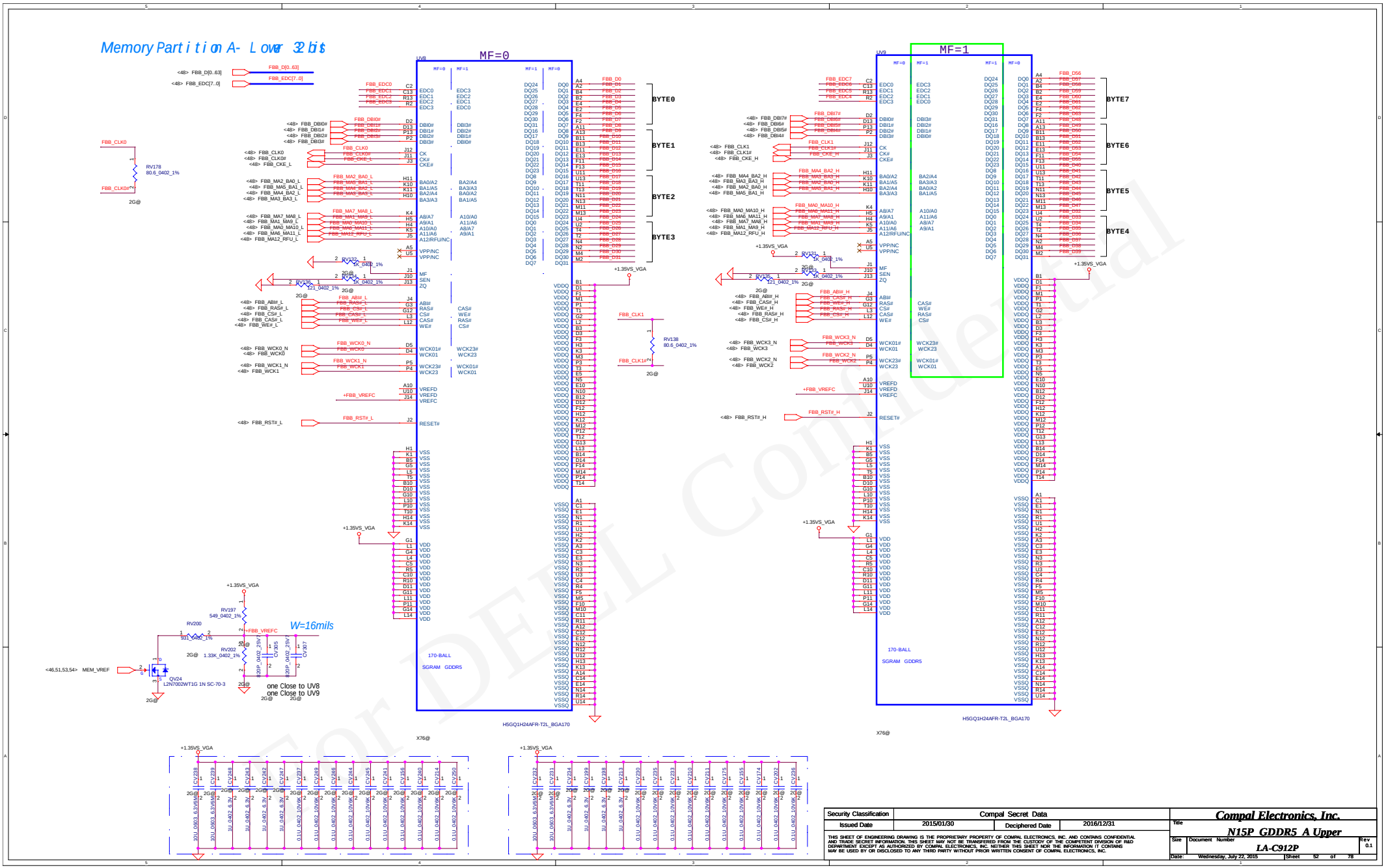
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Title: *N15P-GX (1/5) PEG & DAC*

Size	Document Number	Rev
C	LA-C912P	0.1

Date: Wednesday, July 22, 2015 Sheet 50 of 78





Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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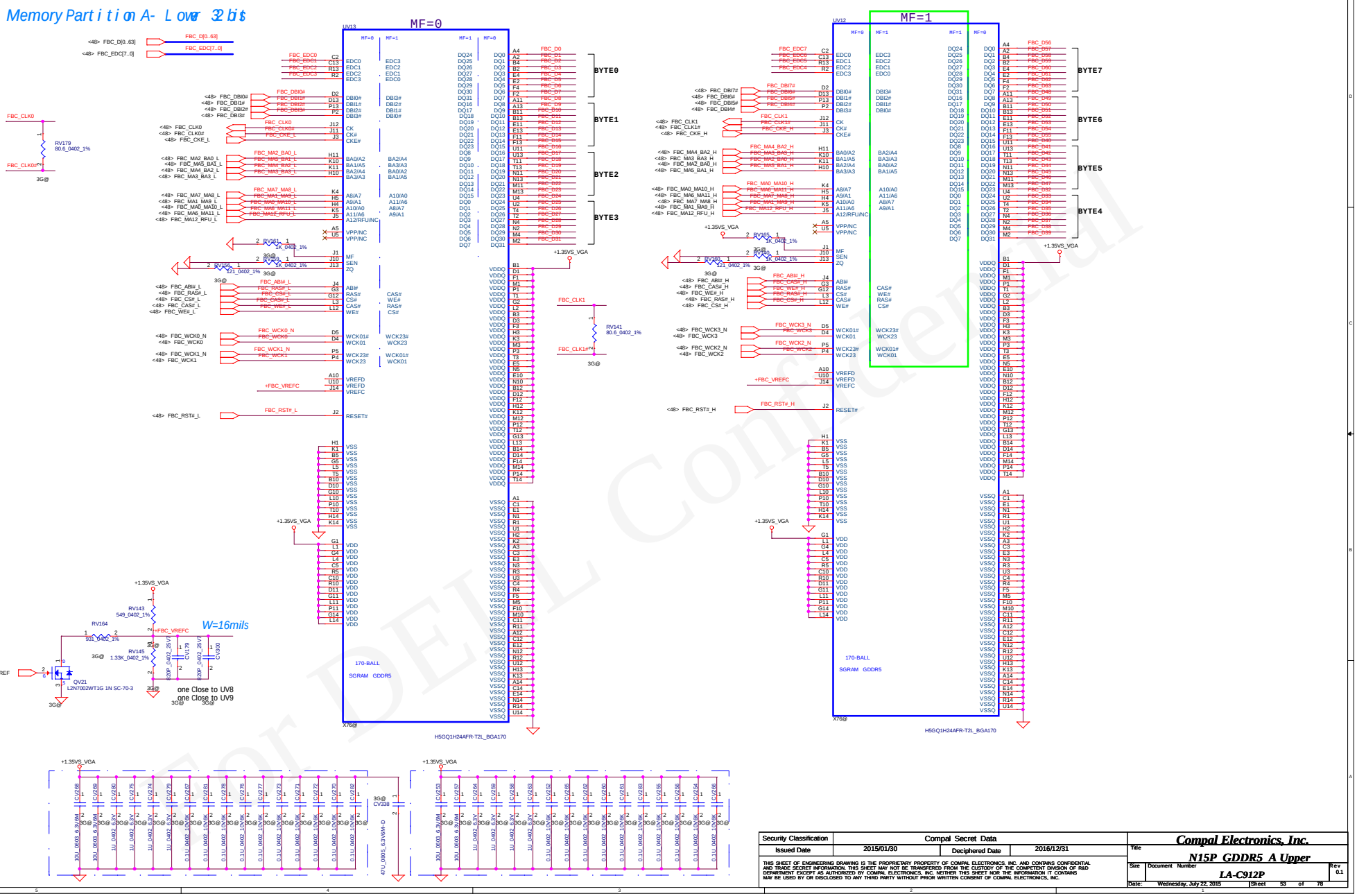
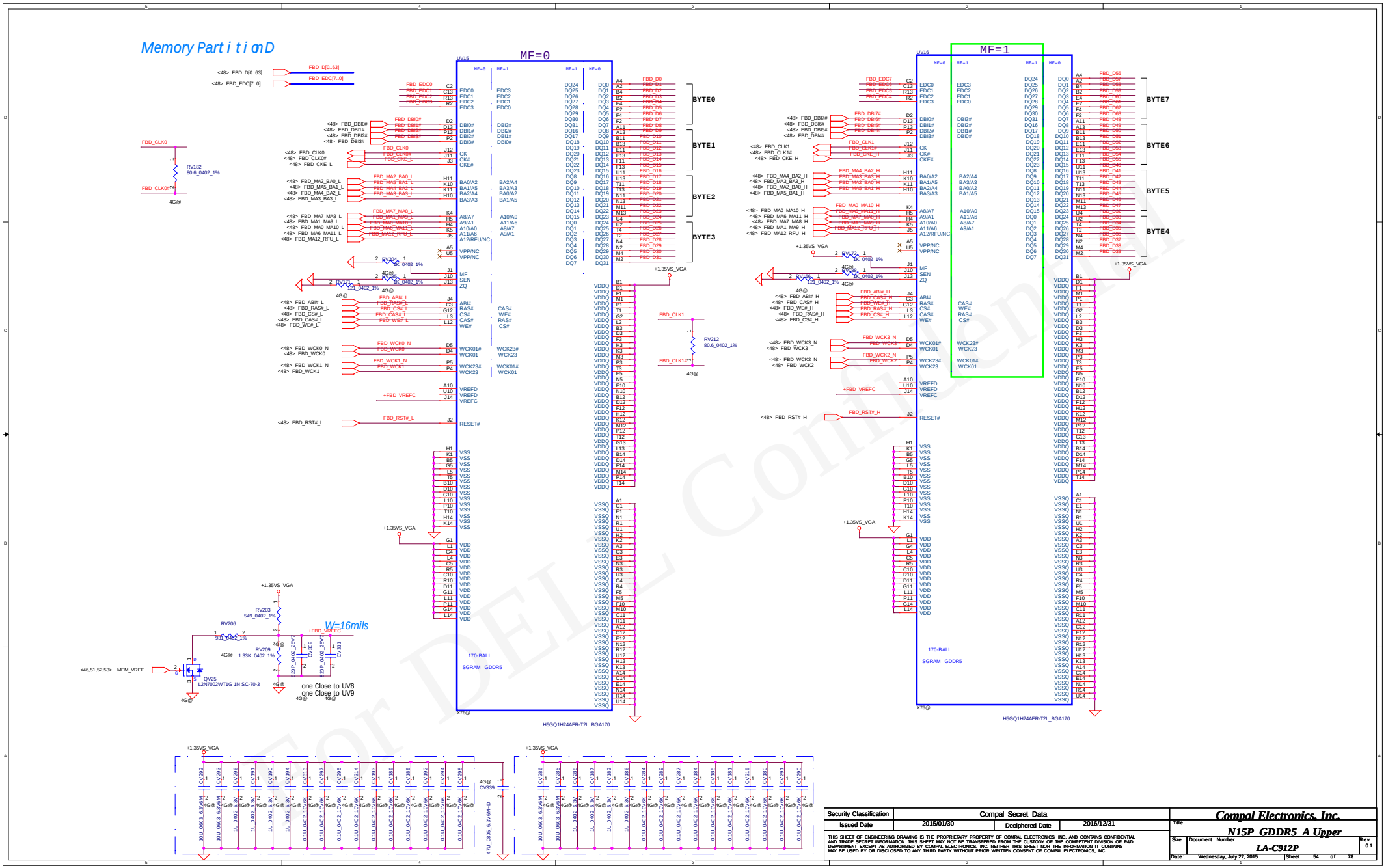
Compal Electronics, Inc.			
Title: N15P_GDDR5_A Upper			
Size	Document Number: LA-C912P		Rev: 0.1
Date: Wednesday, July 22, 2015		Sheet 52 of 78	





Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

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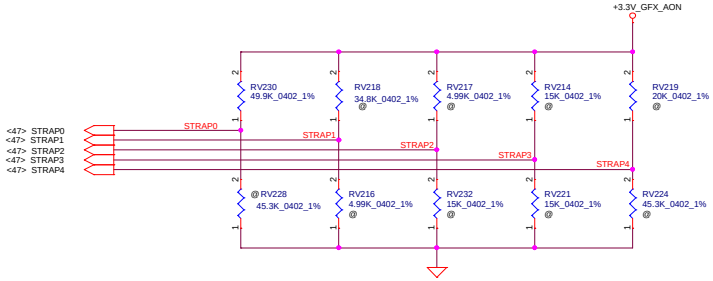
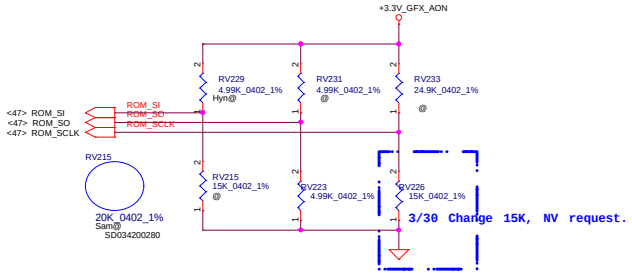
Compal Electronics, Inc.			
Title: N15P_GDDR5_A Upper			
Size	Document Number: LA-C912P		Rev: 0.1
Date: Wednesday, July 22, 2015		Sheet 54 of 78	





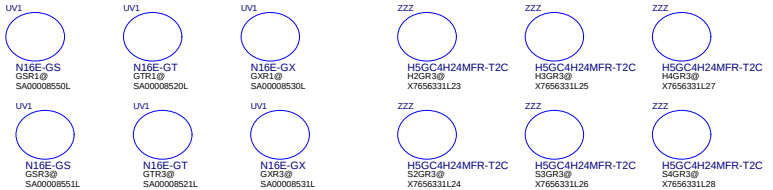
3/30 Change 15K, NV request.

R_pu

VRAM	Strap	ROM-SI
Hynix H5GC4H24MFR-T2C	0x2	PL 15K
Samsung K4G41325FC-HC03	0x3	PL 20K
Hynix H5GC4H24AJR-R0C	0x8	PH 5K

Set as Hynix H5GC4H24AJR-T2C @5G

	PU to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



PCI_DEVID

SUB_VENDER
0- w/o dGPU ROM
1-w/ dGPU ROM

FB[1:0]
0-Reserved
1-Reserved
2-256M
3-Reserved

VGA_DEVICE
0- Non-permary 3D
1-

SMB_ALT_ADDR
0-0x9E
1-0x9C(Multi-GPU)

PEX_PLL_EN_TERM
0-Disable
1-Enable

3GIO_PADCFG
0110-GEN1/GEN2
0000-GEN3

PCIE_MAX_SPEED
0-booting to PCIE Gen1
1-booting to PCIE Gen2/Gen3

PCIE_SPEED_CHNAGE_GEN3
0-Disable PCIE Gen3
1-Enable PCIE Gen3

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHNAGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Title: N15P-GX (1/5) PEG & DAC

Size	Document Number	Rev
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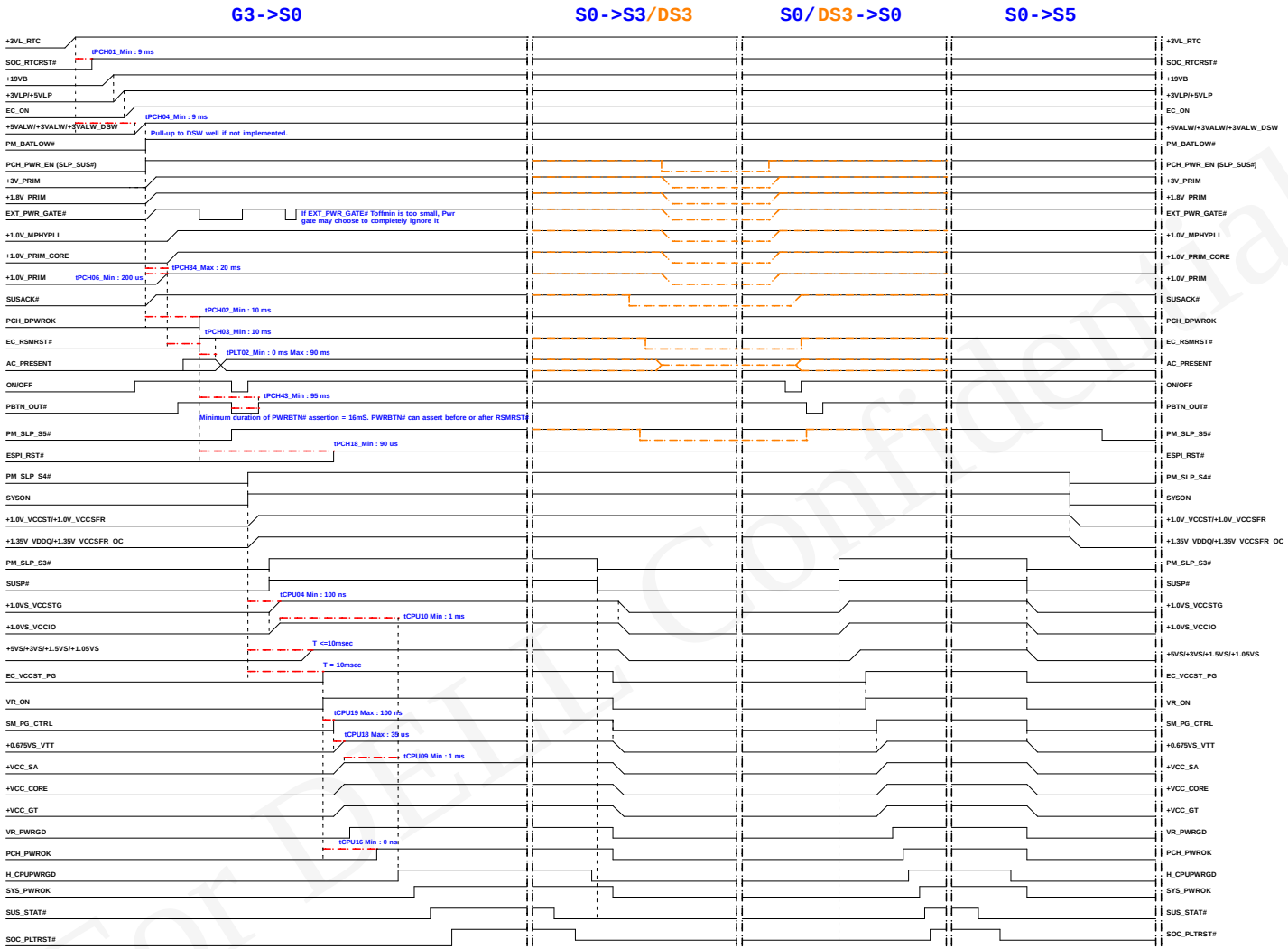
Date: Wednesday, July 22, 2015 Sheet 55 of 78

[AAX06-PWR Sequence_SKL-H 4+4_DDR4_Volume_NON CS]



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Issued Date	2015/01/30	Deciphered Date	2016/12/31
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			Size: LA-C912P Rev: 0.1
			Date: Wednesday, July 23, 2015 Sheet 66 of 79

Empty page

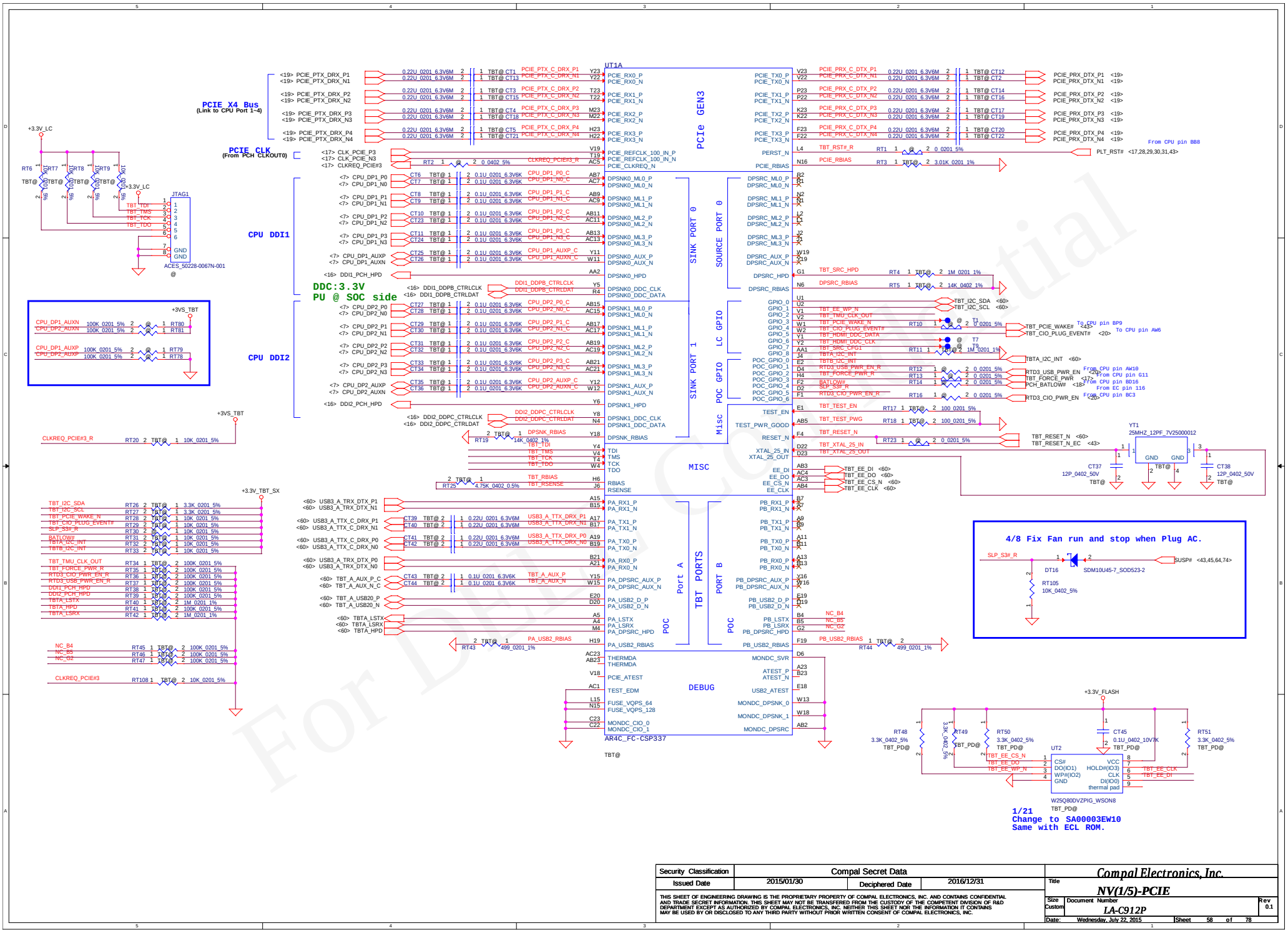
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: ***Mini DP/Thunder Bolt power***

Size	Document Number	Rev
Custom	*LA-C912P*	0.1

Date: Wednesday, July 22, 2015 Sheet 57 of 78



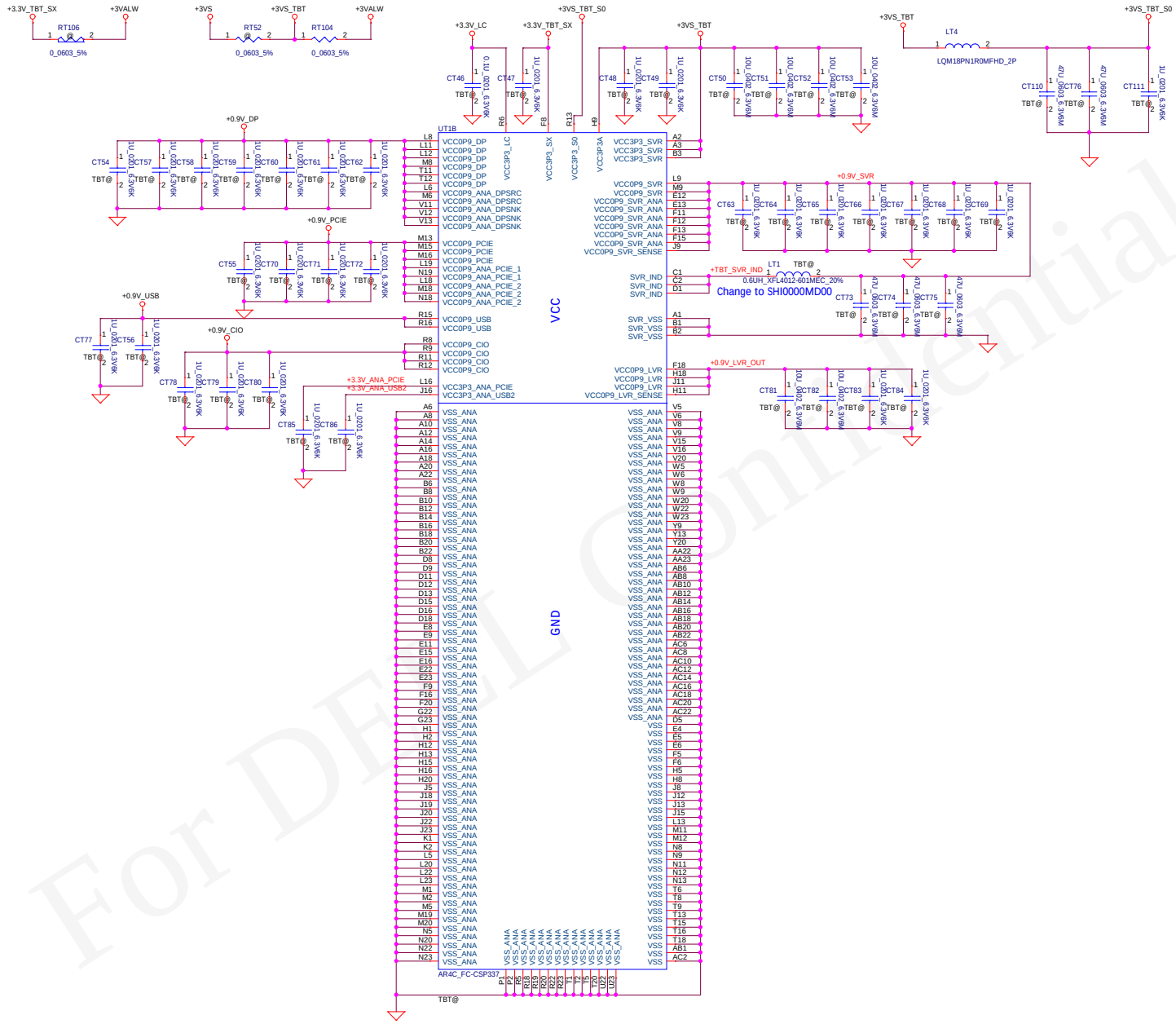
Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: NV(1/5)-PCIE

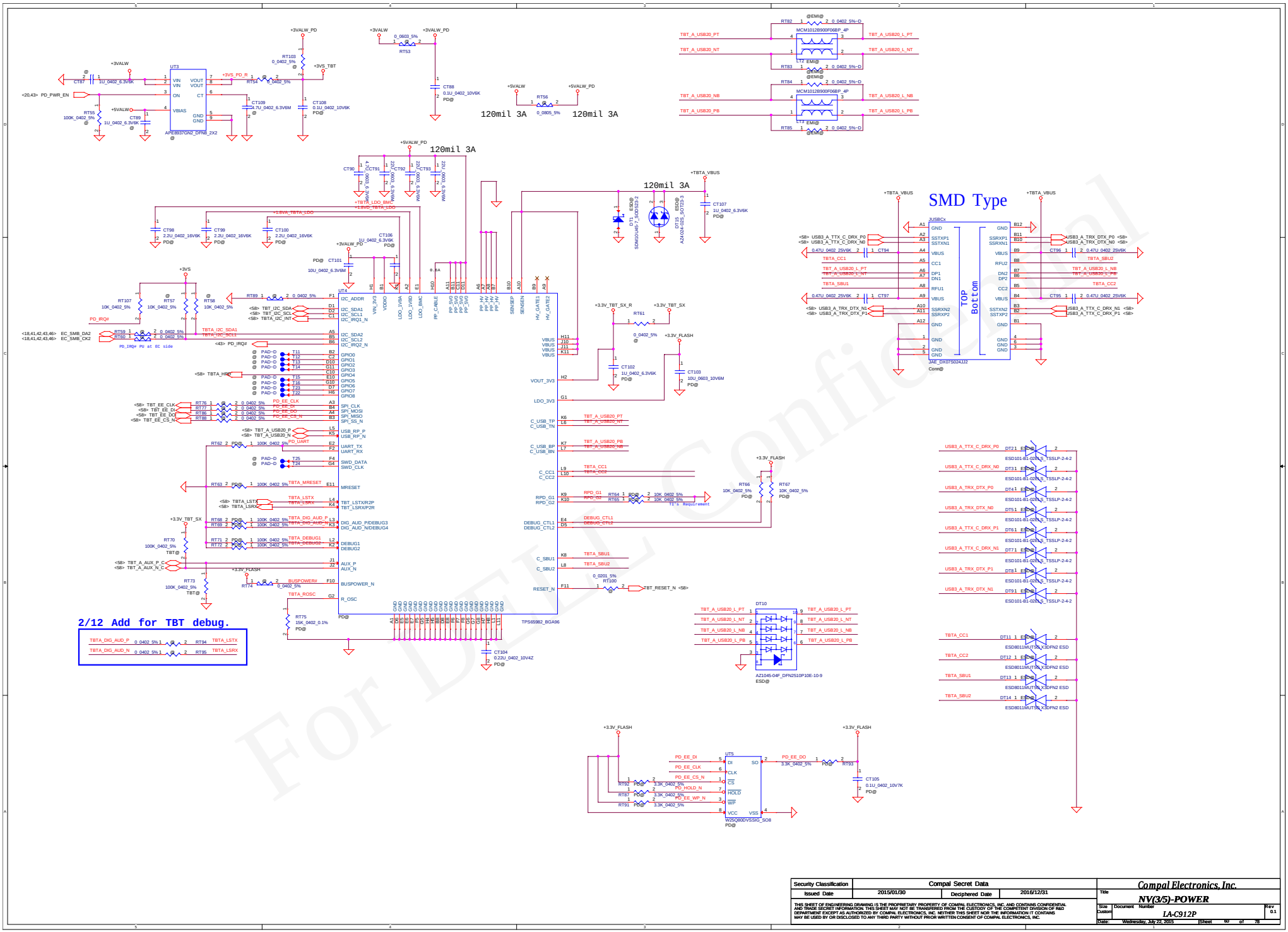
Size: Custom | Document Number: LA-C912P | Rev: 0.1

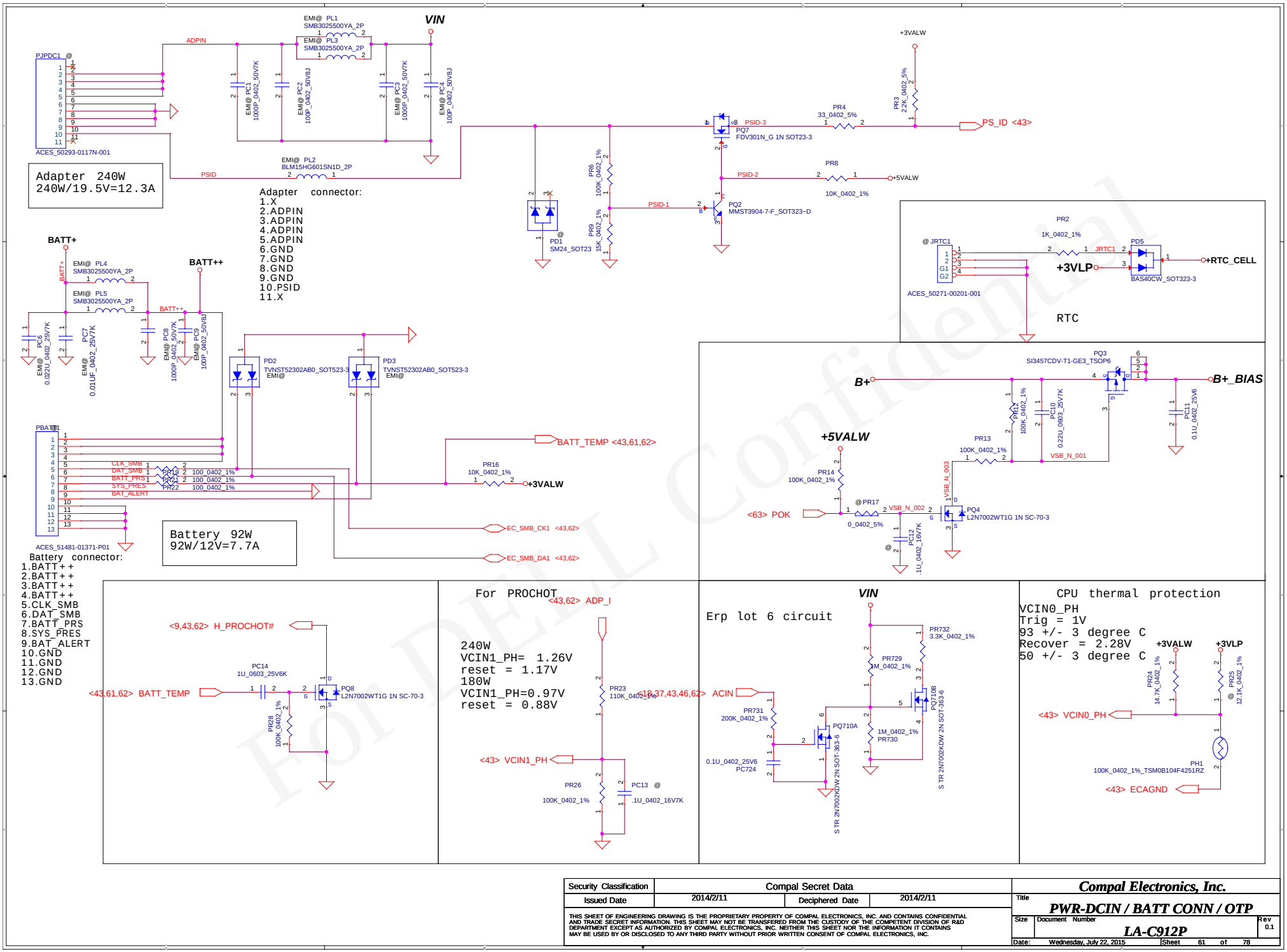
Date: Wednesday, July 22, 2015 | Sheet 58 of 78



Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

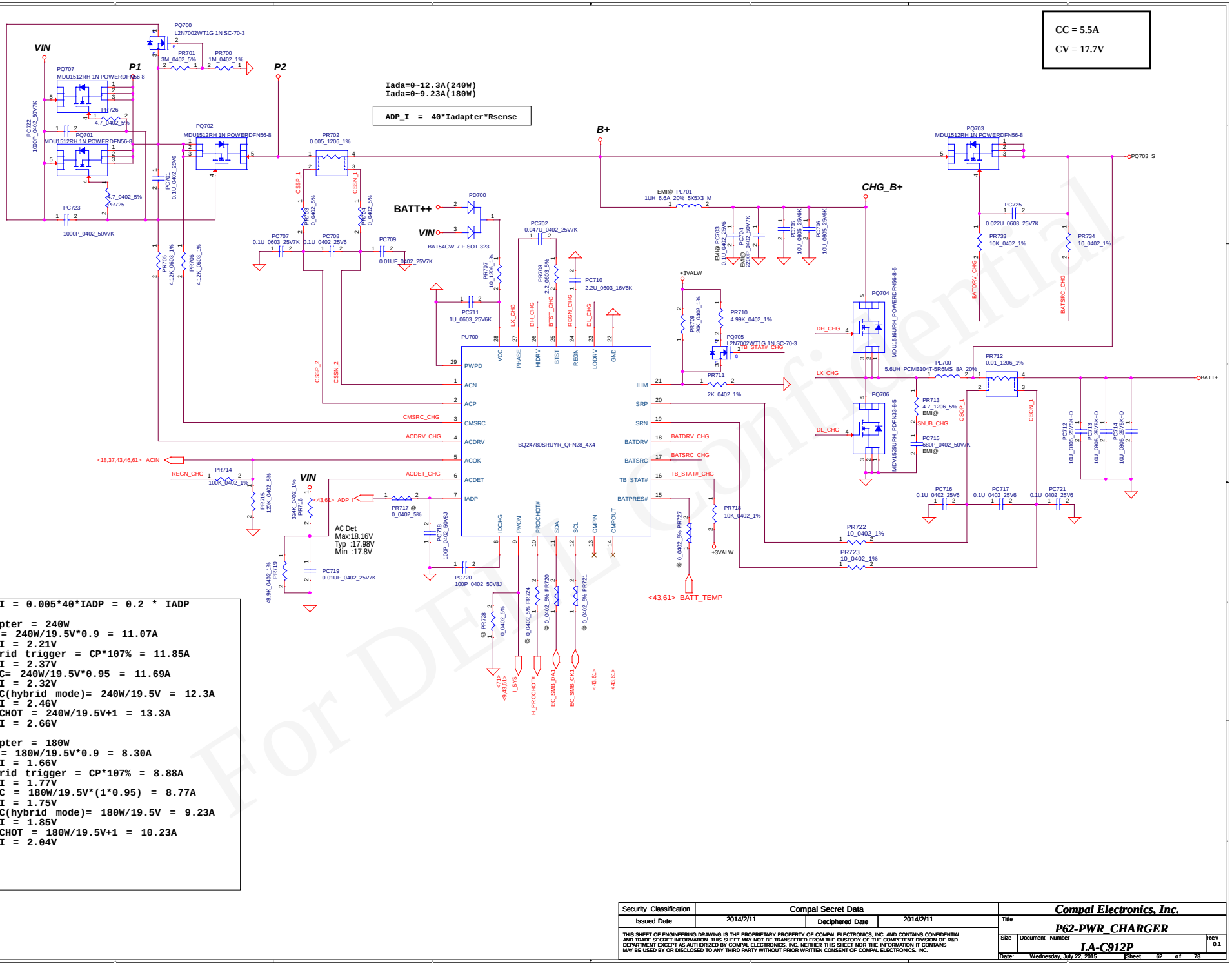
Compal Electronics, Inc.			
Title	NV(2/5)-IFP ABCDEF DAC XTAL		
Size: Custom	Document Number: LA-C912P		Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 59 of 78		





Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.	
Title	PWR-DCIN / BATT CONN / OTP
Size	Document Number: LA-C912P
Rev	0.1
Date:	Wednesday, July 22, 2015
Sheet	61 of 78




```
ADPI = 0.005*40*IADP = 0.2 * IADP

Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 2.21V
Hybrid trigger = CP*107% = 11.85A
ADPI = 2.37V
IPCC= 240W/19.5V*0.95 = 11.69A
ADPI = 2.32V
IPCC(hybrid mode)= 240W/19.5V = 12.3A
ADPI = 2.46V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 2.66V

Adapter = 180W
CP = 180W/19.5V*0.9 = 8.30A
APDI = 1.66V
Hybrid trigger = CP*107% = 8.88A
ADPI = 1.77V
IPCC = 180W/19.5V*(1*0.95) = 8.77A
ADPI = 1.75V
IPCC(hybrid mode)= 180W/19.5V = 9.23A
ADPI = 1.85V
PROCHOT = 180W/19.5V+1 = 10.23A
ADPI = 2.04V
```

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/2/11	Deciphered Date	2014/2/11
Title	P62-PWR_CHARGER		
Size	Document Number	LA-C912P	Rev 0.1
Date: Wednesday, July 22, 2015	Sheet 62 of 78		

Input Current: 7.5A
3.3V*10A/0.85/12V=2.23
5V*10A/0.85/12V=5.27

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit

<61> POK

DCR = 18mohm

ESR = 18mohm

DCR = 6mohm

ESR = 15mohm

3.3VALWP
TDC=10.01A
Peak Current 14.31A
OCP current 17.17A
FSW=355kHz

	TYP	MAX
H/S Rds(on) :	11.5mohm	14mohm
L/S Rds(on) :	2.7mohm	3.3mohm

5VALWP
TDC=10.77A (8.77A+2A)
Peak Current 15.38A
OCP current 18.45A
FSW=300kHz

	TYP	MAX
H/S Rds(on) :	11.5mohm	14mohm
L/S Rds(on) :	2.7mohm	3.3mohm

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

EN
Rising=1.6~0.3V

Security Classification	Compal Secret Data	
Issued Date	2014/2/11	Deciphered Date 2014/2/11

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size | Document Number: LA-C912P | Rev: 0.1

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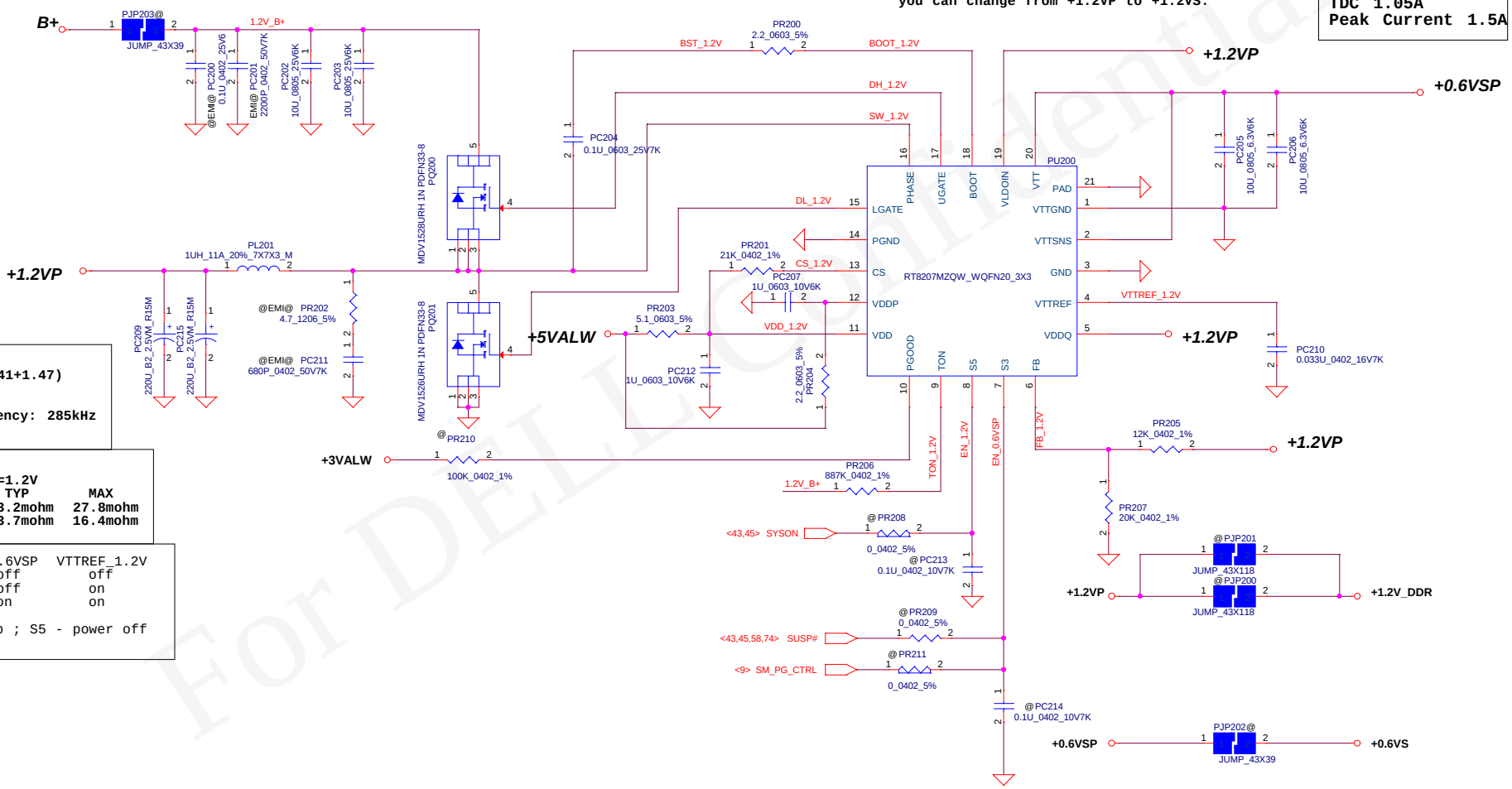
Input Current: 1A
1.2V*8.88A/0.85/12V=1

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

0.6VSP
TDC 1.05A
Peak Current 1.5A



1.2VP
TDC=8.88A (7.41+1.47)
Ipeak=12.68A
OCP=15.21A
Switching Frequency: 285kHz

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

	TYP	MAX
H/S Rds(on) :	23.2mohm	27.8mohm
L/S Rds(on) :	13.7mohm	16.4mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

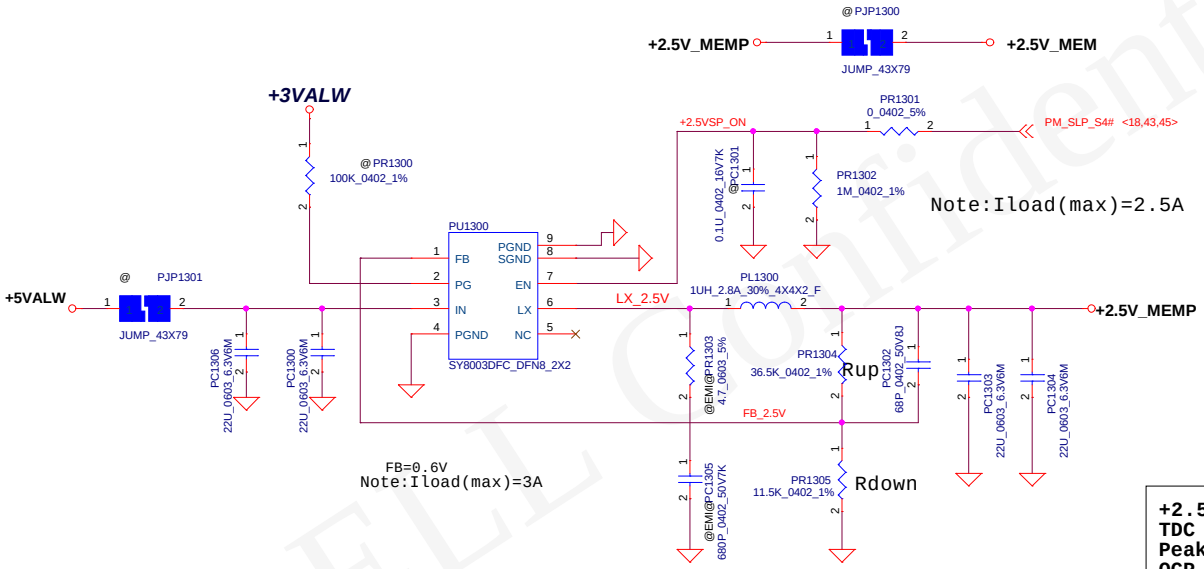
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: PWR-1.2VP/0.6VSP

Size | Document Number: LA-C912P | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 64 of 78



+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

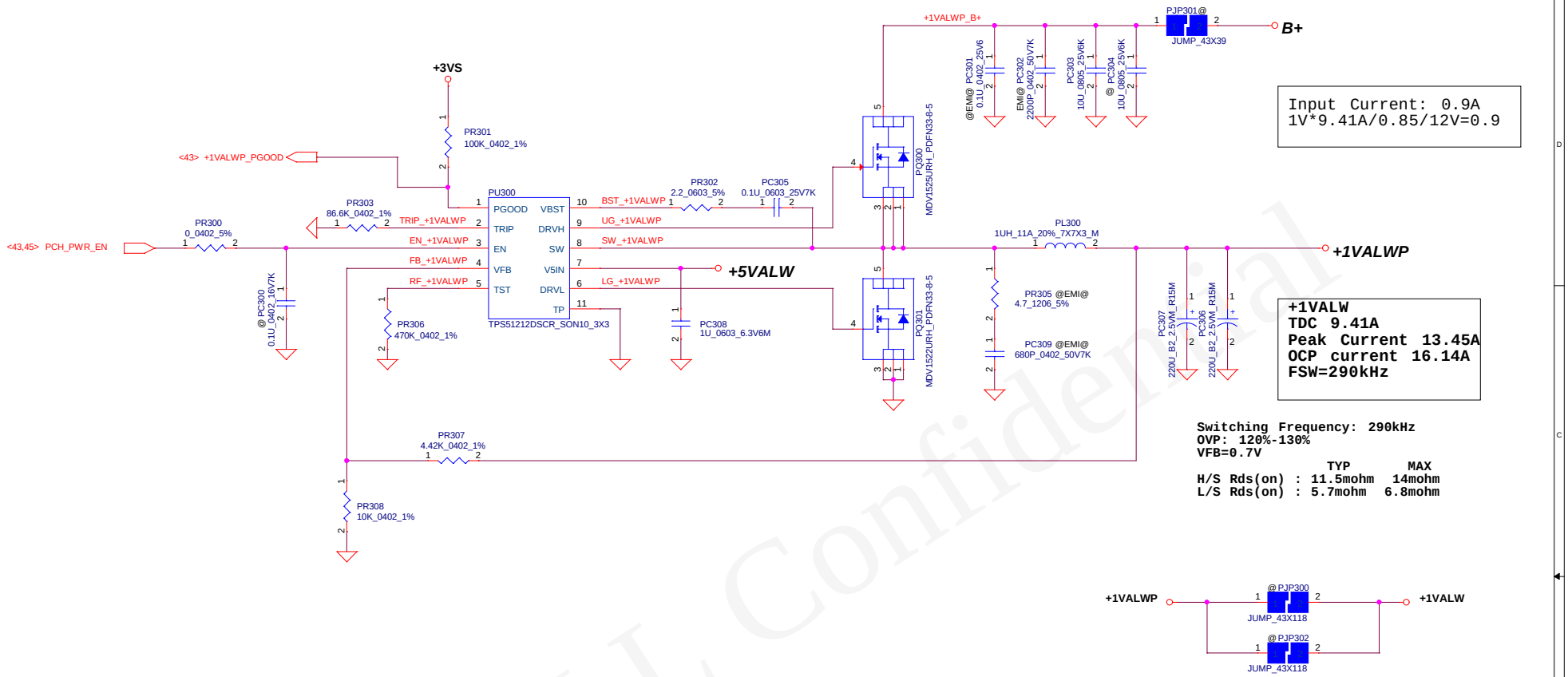
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.

Title: **PWR_+2.5V_MEM**

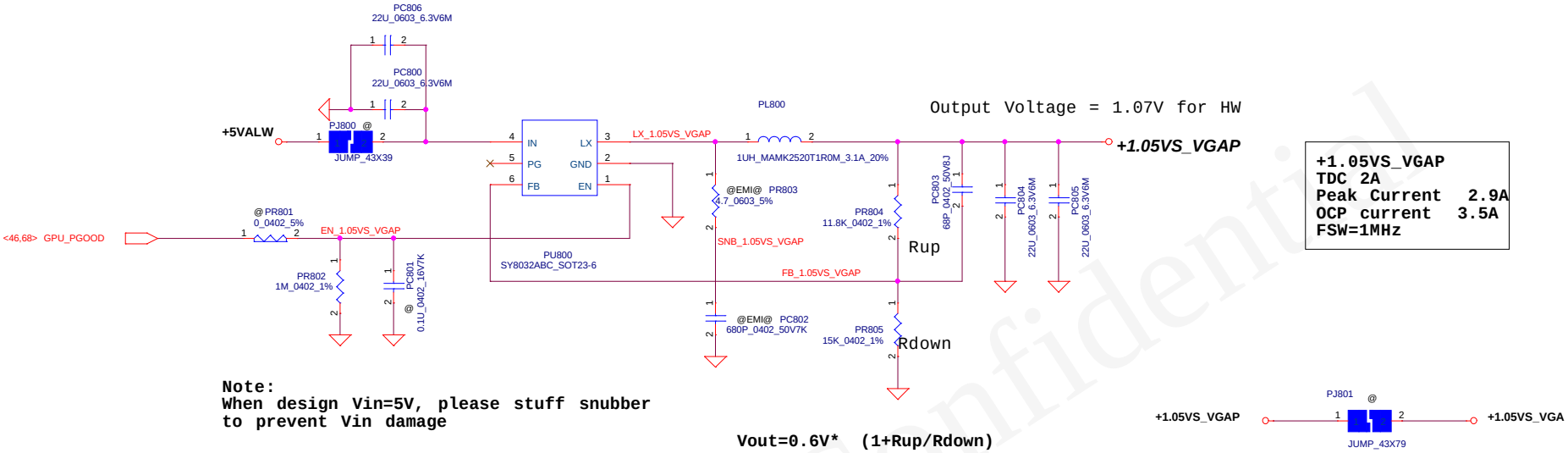
Size | Document Number: **LA-C912P** | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 65 of 78



Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.			
Title	PWR-1.05VSP		
Size	Document Number		Rev
	LA-C912P		0.1
Date:	Wednesday, July 22, 2015	Sheet	66 of 78



Output Voltage = 1.07V for HW

+1.05VS_VGAP
TDC 2A
Peak Current 2.9A
OCP current 3.5A
FSW=1MHz

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

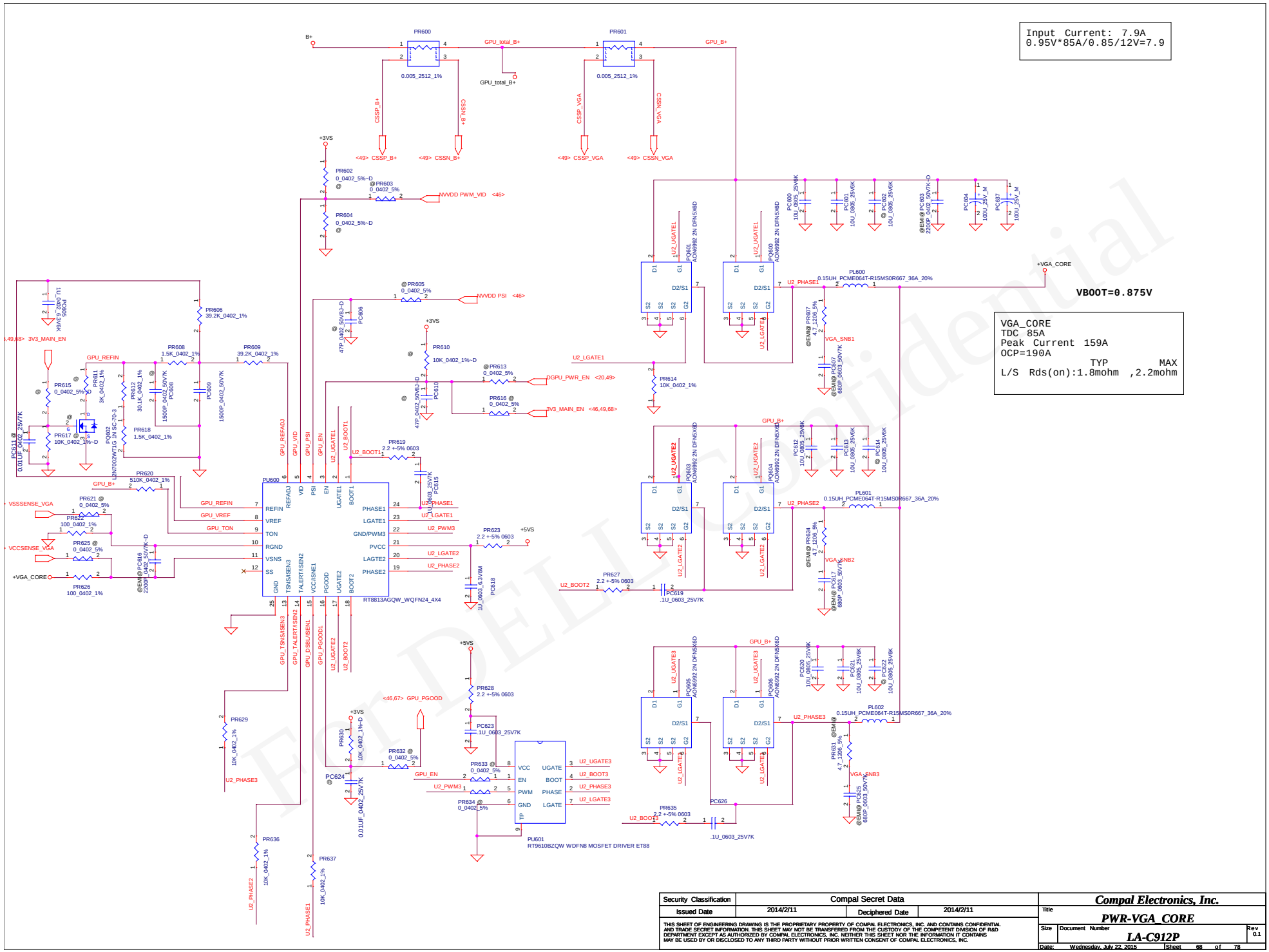
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

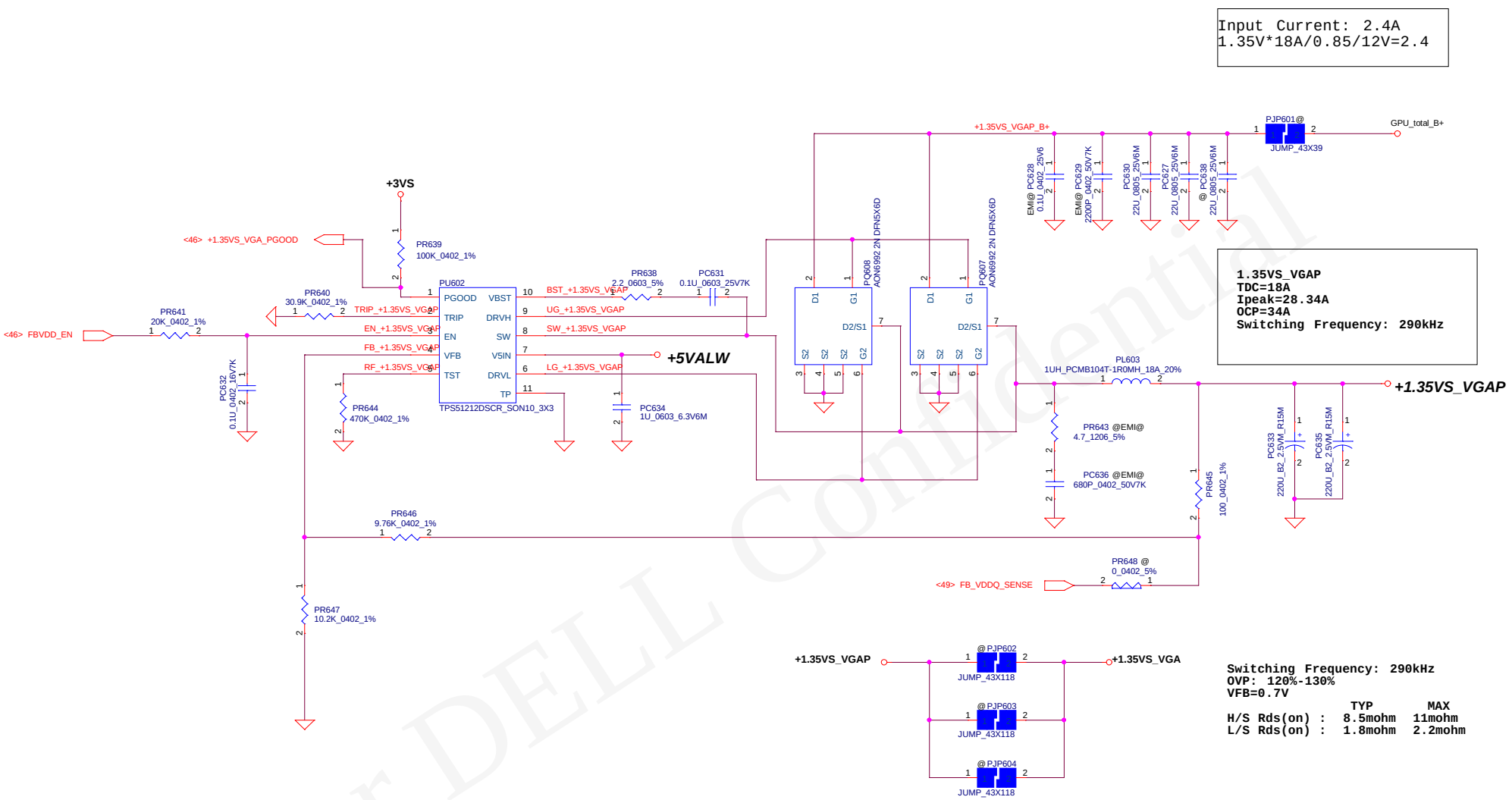
Compal Electronics, Inc.

Title: **PWR-1.05VS_VGA**

Size	Document Number	Rev
	LA-C912P	0.1

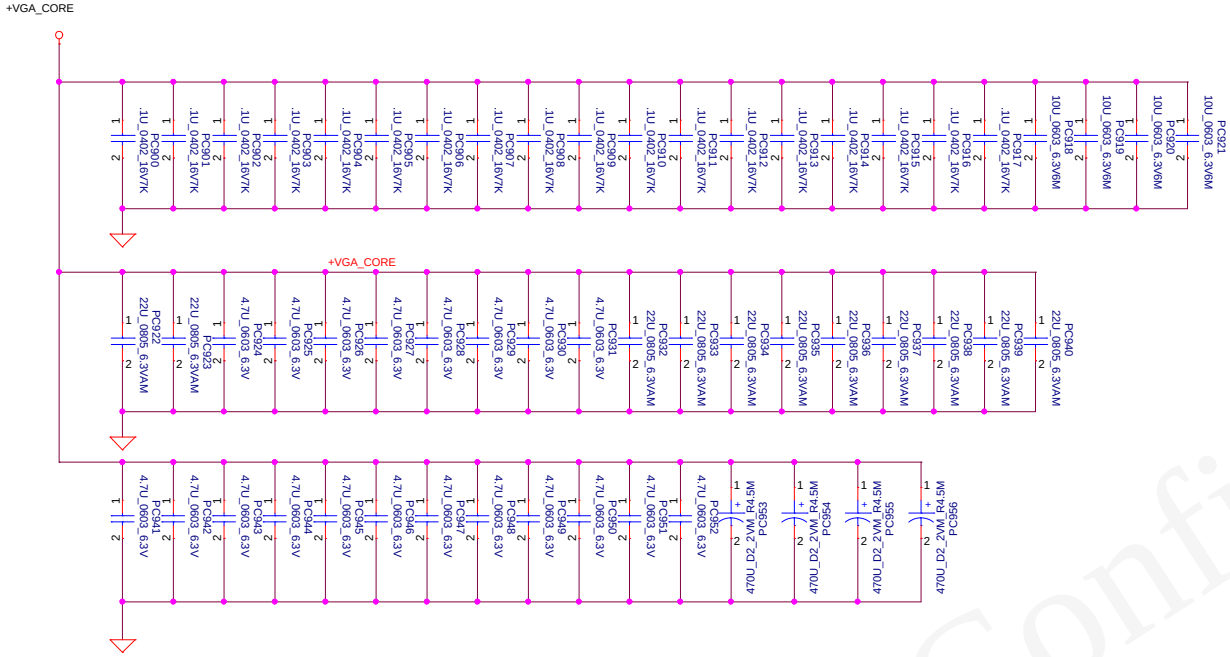
Date: Wednesday, July 22, 2015 Sheet 67 of 78





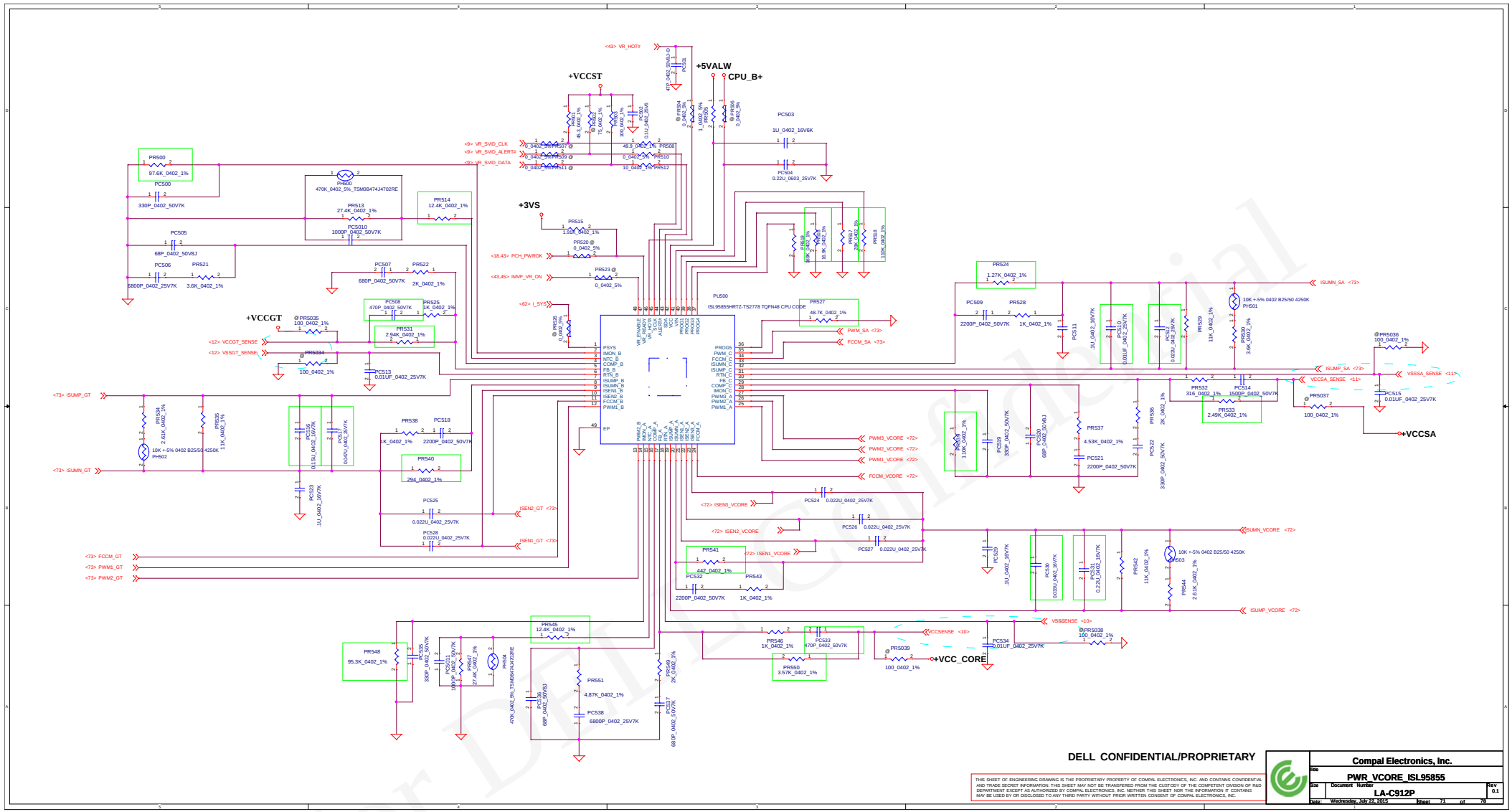
Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

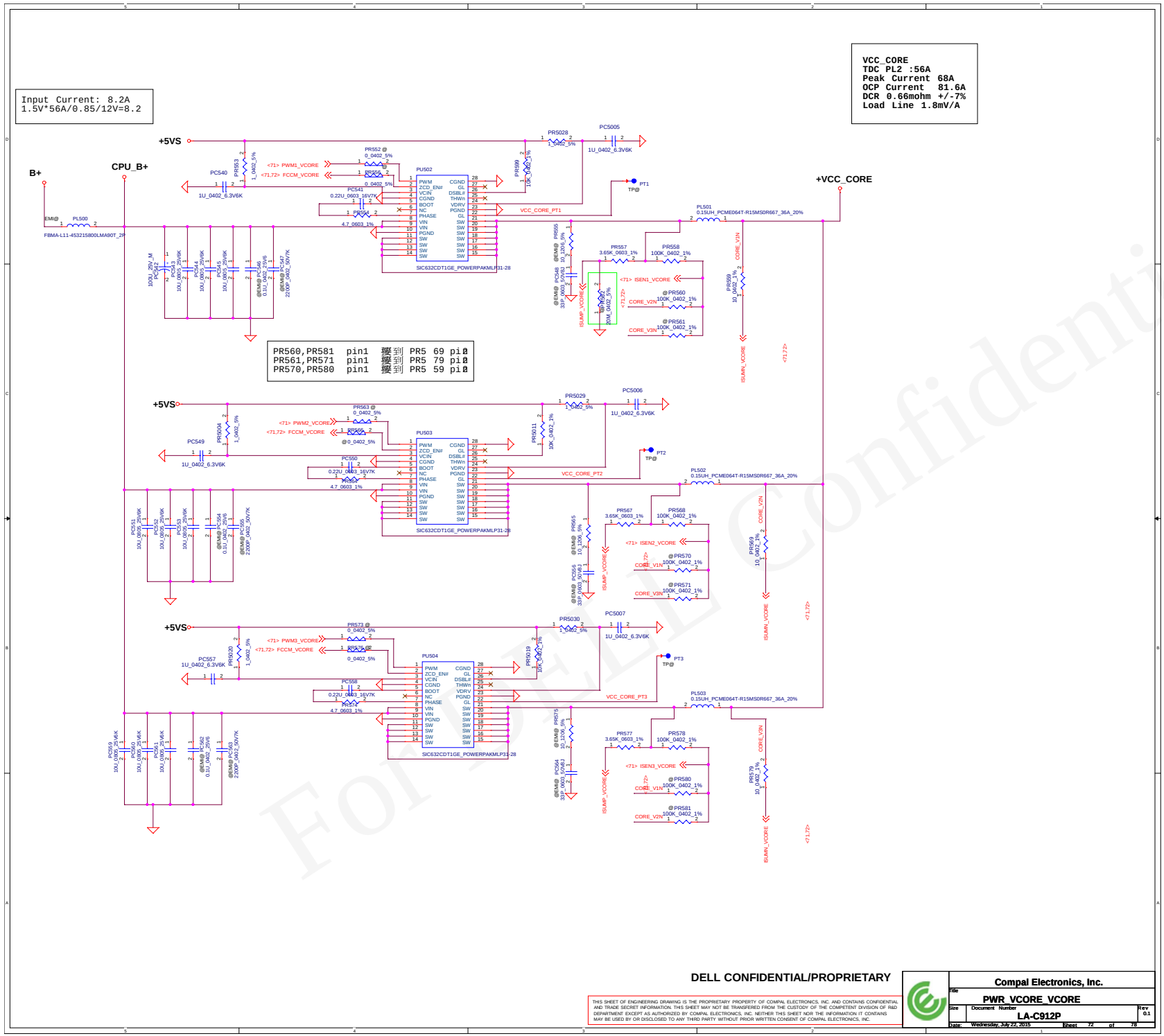
Compal Electronics, Inc.		
Title	PWR-1.35VRAM	
Size	Document Number LA-C912P	Rev 0.1
Date: Wednesday, July 22, 2015	Sheet 69 of 78	

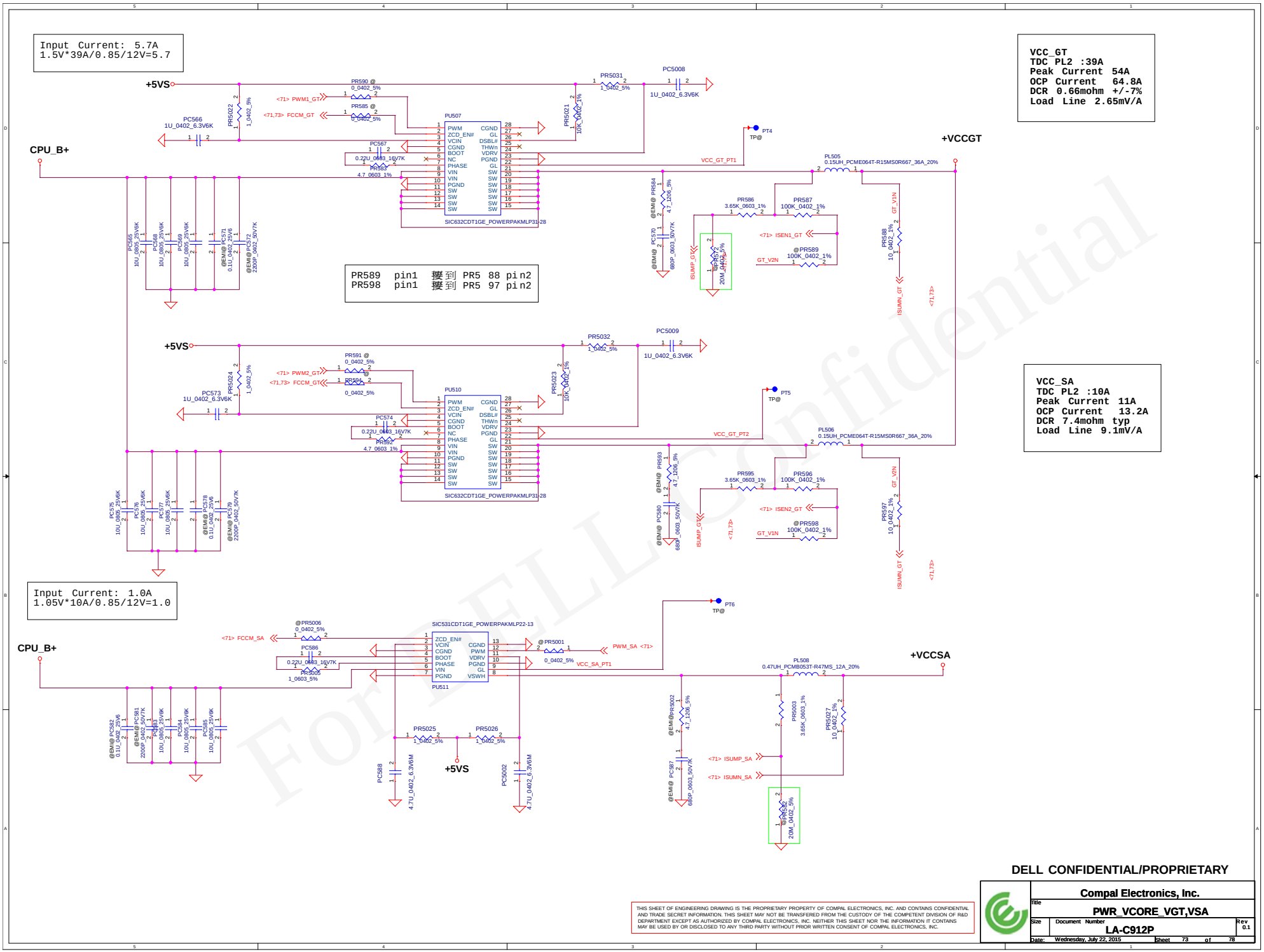


Security Classification	Compal Secret Data		
Issued Date	2014/2/11	Deciphered Date	2014/2/11

Compal Electronics, Inc.		
Title: PWR-PROCESSOR DECOUPLING		
Size	Document Number: LA-C912P	Rev: 0.1
Date: Wednesday, July 22, 2015	Sheet 70 of 78	





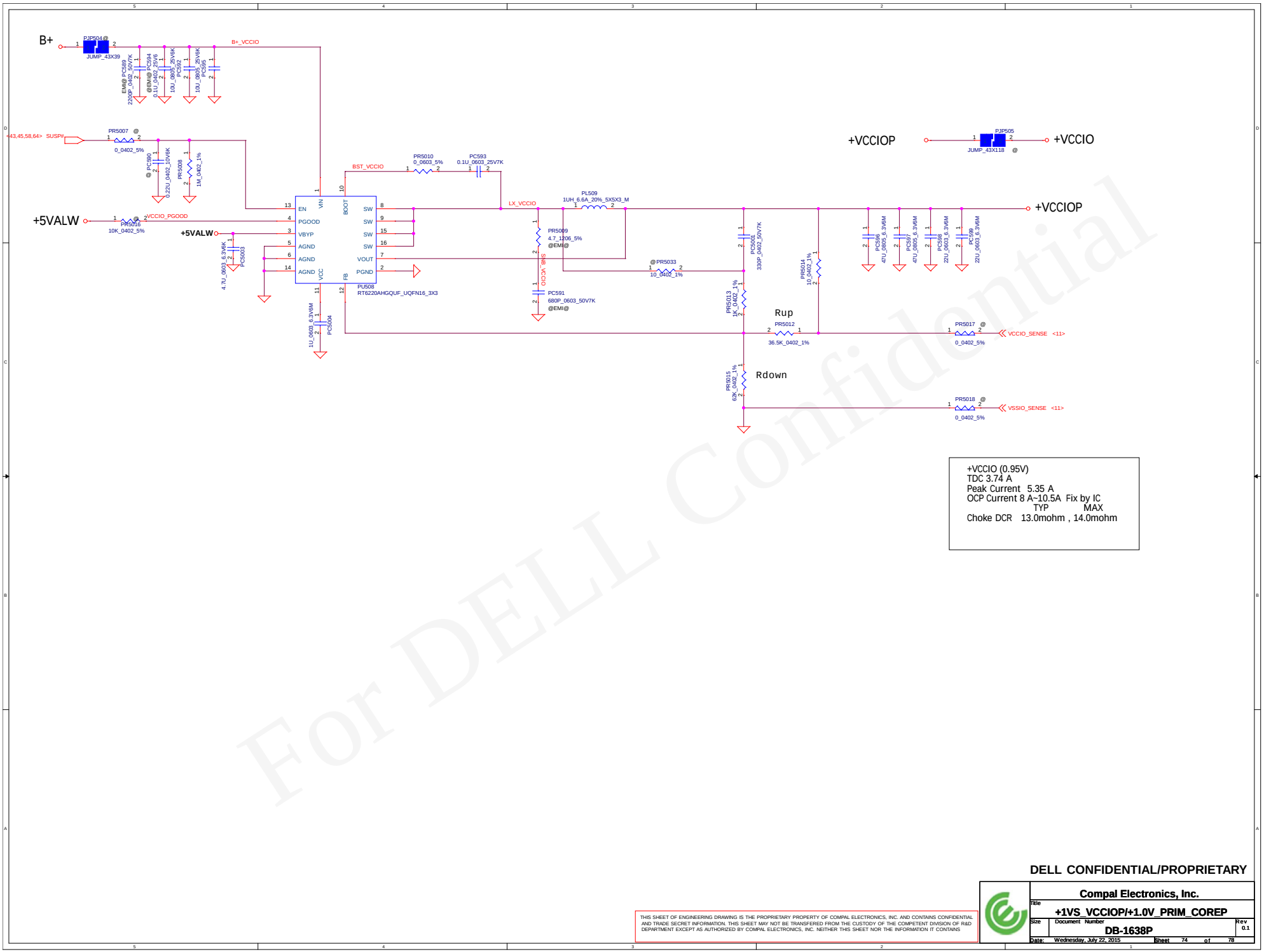


Compal Electronics, Inc.

Title: PWR_VCORE_VGT,VSA

Size: | Document Number: LA-C912P | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 73 of 78



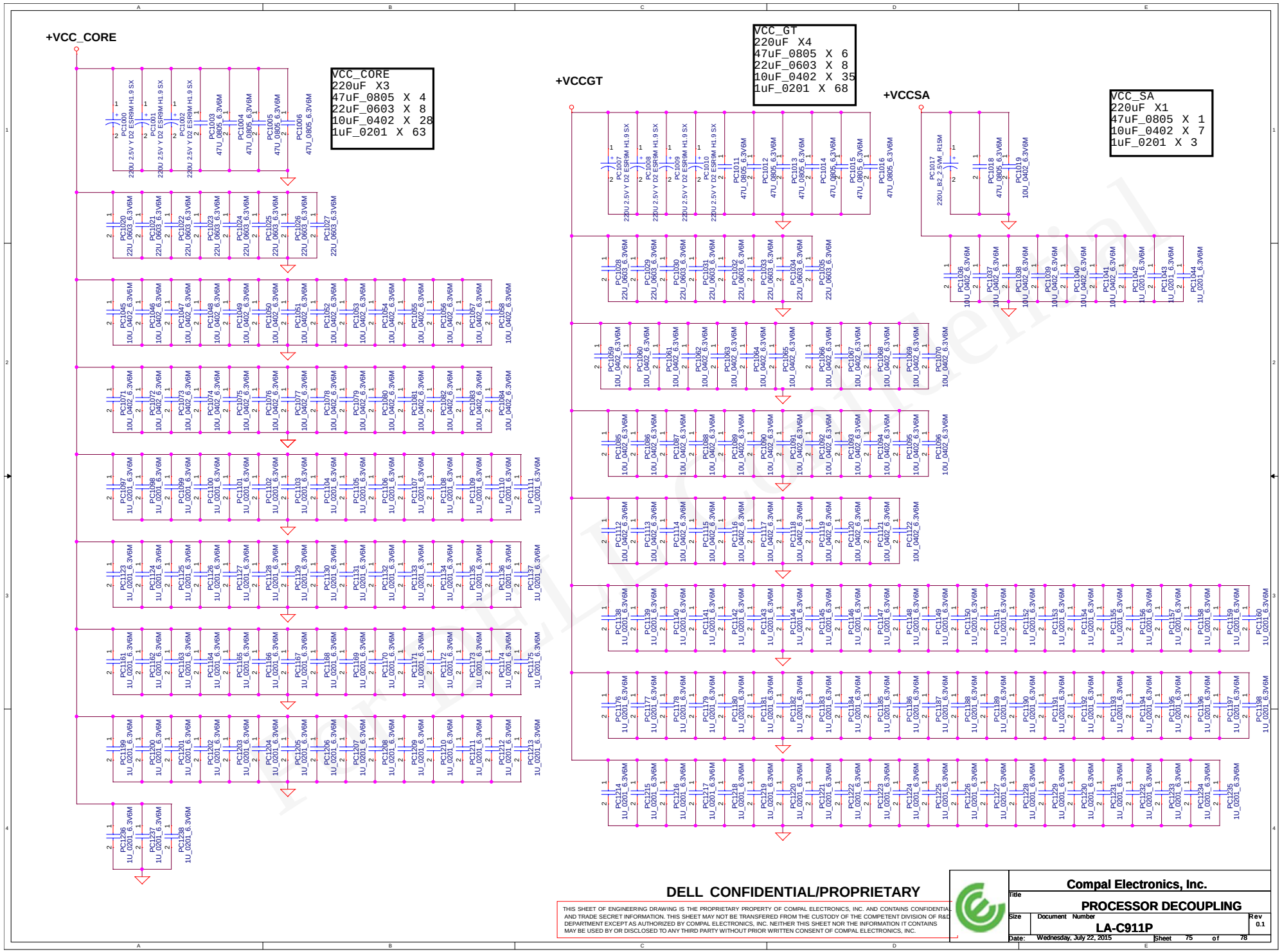
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

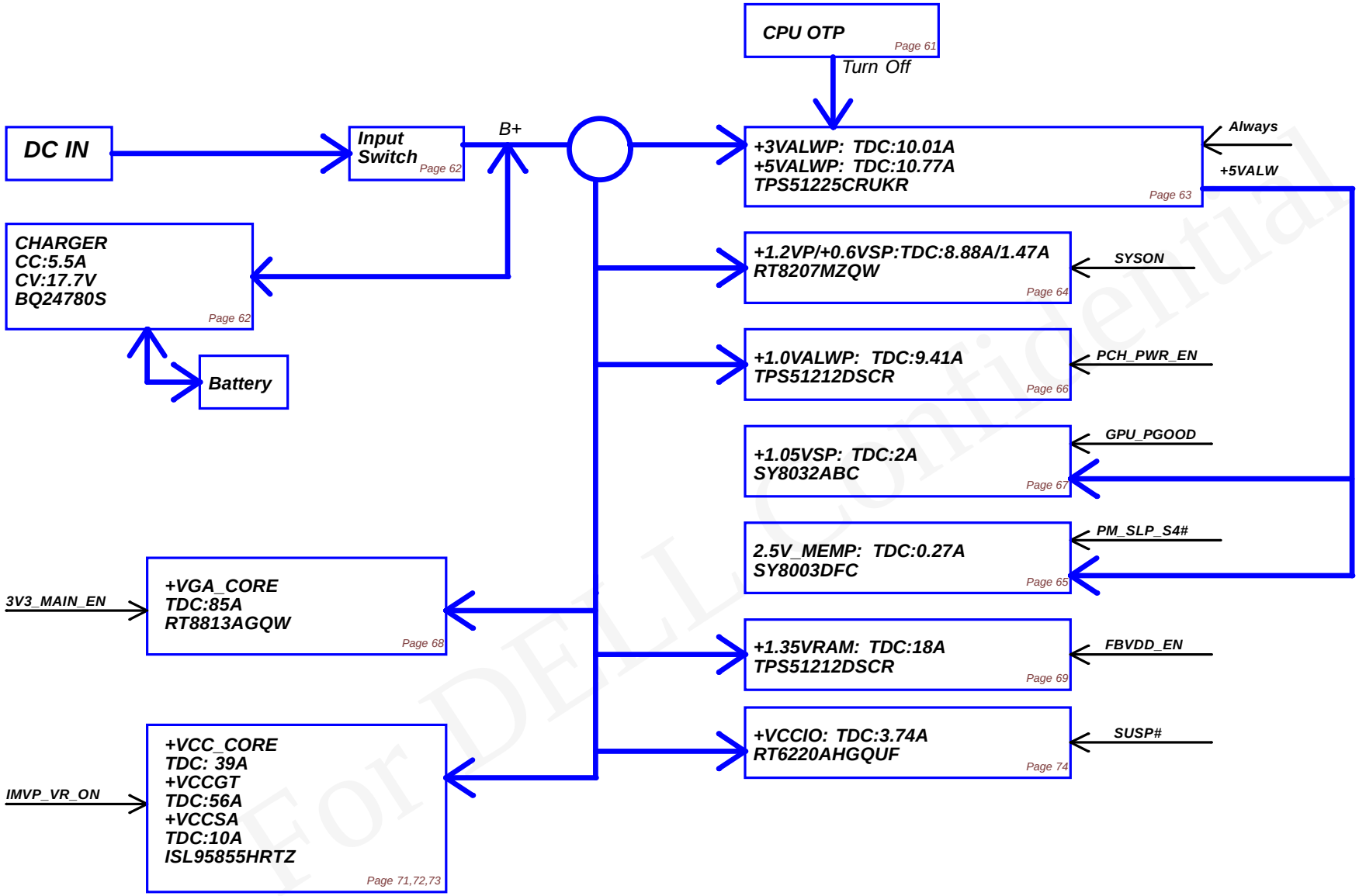
Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

Size | Document Number: DB-1638P | Rev: 0.1

Date: Wednesday, July 22, 2015 | Sheet 74 of 78



Power block



Security Classification	Compal Secret Data		
Issued Date	2015/01/06	Deciphered Date	2016/01/06

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number	LA-C912P	Rev 0.1
Date: Wednesday, July 22, 2015	Sheet 76 of 78		

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	68	PWR_+VGA_CORE	2015.4.1	Nick_Lin	Change VGA_CORE Choke	Change from S COIL .12UH 20% PCME063T-R12MS0R625 41A ($H00000QR00) to 0.15UH_PCME064T-R15MS0R667_36A_20% (SH00000U300) Location:PL600,PL601,PL602	
2	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	Change net from +1.0V_VCCST to +VCCST		
3	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	umount PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	Change from100_0402_1% (SD034100080) to @ Location:PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	
4	66	PWR_+1VALWP	2015.4.11	Nick_Lin	Change OCP setting	Change from 210K_0402_1%_0402_1% (SD034210380) to 86.6K_0402_1% (SD034866280) Location:PR303	
5	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Mount PC627 for Acoustic	Change from 10U_0805_25V (SE00000QK00) to 22U_0805_25V (SE00000XH80) Location:PC638	
6	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Change PC630 for Acoustic	Add 22U_0805_25V (SE00000XH80) Location:PC627,PC630	
7	62	PWR_CHARGER	2015.4.11	Nick_Lin	Change PR702 for PMON function	Change from 0.004_1206_1% (SD000017Q00) to 0.005_1206_1%(SD000017R00) Location:PR303	
8	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD000009480 (S RES 1/16W 1.47K +-1% 0402) to SD034127180 (S RES 1/16W 1.27K +-1% 0402) Location PR524 Change form SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR530 Change form SE068221J80 (S CER CAP 220P 25V J NPO 0402) to SE074152K80 (S CER CAP 1500P 50V K X7R 0402) Location PC514 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD000003480 (S RES 1/16W 316 +-1% 0402) Location PR532 Change form SE074681K80 (S CER CAP 680P 50V K X7R 0402) to SE074331K80 (S CER CAP 330P 50V K X7R 0402) Location PC522 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034453180 (S RES 1/16W 4.53K +-1% 0402) Location PR537 Change form SD034113380 (S RES 1/16W 113K +-1% 0402) to SD034110380 (S RES 1/16W 110K +-1% 0402) Location PR539 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE076333K80 (S CER CAP .033U 16V K X7R 0402) Location PC530 Change form SD034267080 (S RES 1/16W 267 +-1% 0402) to SD034301080 (S RES 1/16W 301 +1% 0402) Location PR541 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC533	

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
9	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034487100 (S RES 1/16W 4.87K +-1% 0402) Location PR511 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402) Location PC517 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC508 Change form SD034182180 (S RES 1/16W 1.82K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR521 Change form SD034953280 (S RES 1/16W 95.3K +-1% 0402) to SD034976280 (S RES 1/16W 97.6K +-1% 0402) Location PR500	
10	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VCC_CORE VR_IMAX	Change form SD034301080 (S RES 1/16W 301 +1% 0402) to SD034442080 (S RES 1/16W 442 +1% 0402) Location PR541 Change form SD034243180 (S RES 1/16W 2.43K +-1% 0402) to SD034357180 (S RES 1/16W 3.57K +-1% 0402) Location PR550 Change form SD034562180 (S RES 1/16W 5.62K +-1% 0402) to SD034280280 (S RES 1/16W 28K +-1% 0402) Location PR517 Change form SD034931280 (S RES 1/16W 93.1K +-1% 0402) to SD034953280 (S RES 1/16W 95.3K +-1% 0402) Location PR548	
11	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VR_ProcHOt Trig point	Change form SD034105280 (S RES 1/16W 10.5K +-1% 0402) to SD00000AJ80 (S RES 1/16W 12.4K +-1% 0402) Location PR545,PR514	
12	61	PWR_DCIN / BATT CONN / OTP	2015.6.24	Nick_Lin	fine tune OTP setting	Change form SD034162280 (S RES 1/16W 16.2K +1% 0402) to SD034147280 (S RES 1/16W 14.7K +1% 0402) Location PR24	

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