MS-7507

Version 0A

CPU:

- Intel Prescott (L2=2MB) - 3.4G & Above
- Intel Cendar Mill (65nm) - 3.73G & Above
- Intel Smithfield (90nm Dual core)
- Intel Conroe (65W Dual core)

System Chipset:

- Intel Lakeport - MCH (North Bridge)
- Intel ICH7R (South Bridge)

On Board Chipset:

- BIOS -- SPI
- HD -- ALC888
- LPC Super I/O -- F71882FG
- LAN-- REALTEK RTL8111C Co-lay RTL8101E
- CLOCK -- RTM876-660

Main Memory:

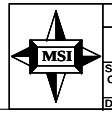
- DDR II *2 (Max 2GB)

Expansion Slots:

- PCI2.3 SLOT * 2
- PCI EXPRESS X1 SLOT
- PCI EXPRESS X16 SLOT

ST PWM:

- Controller: 3 PHASES



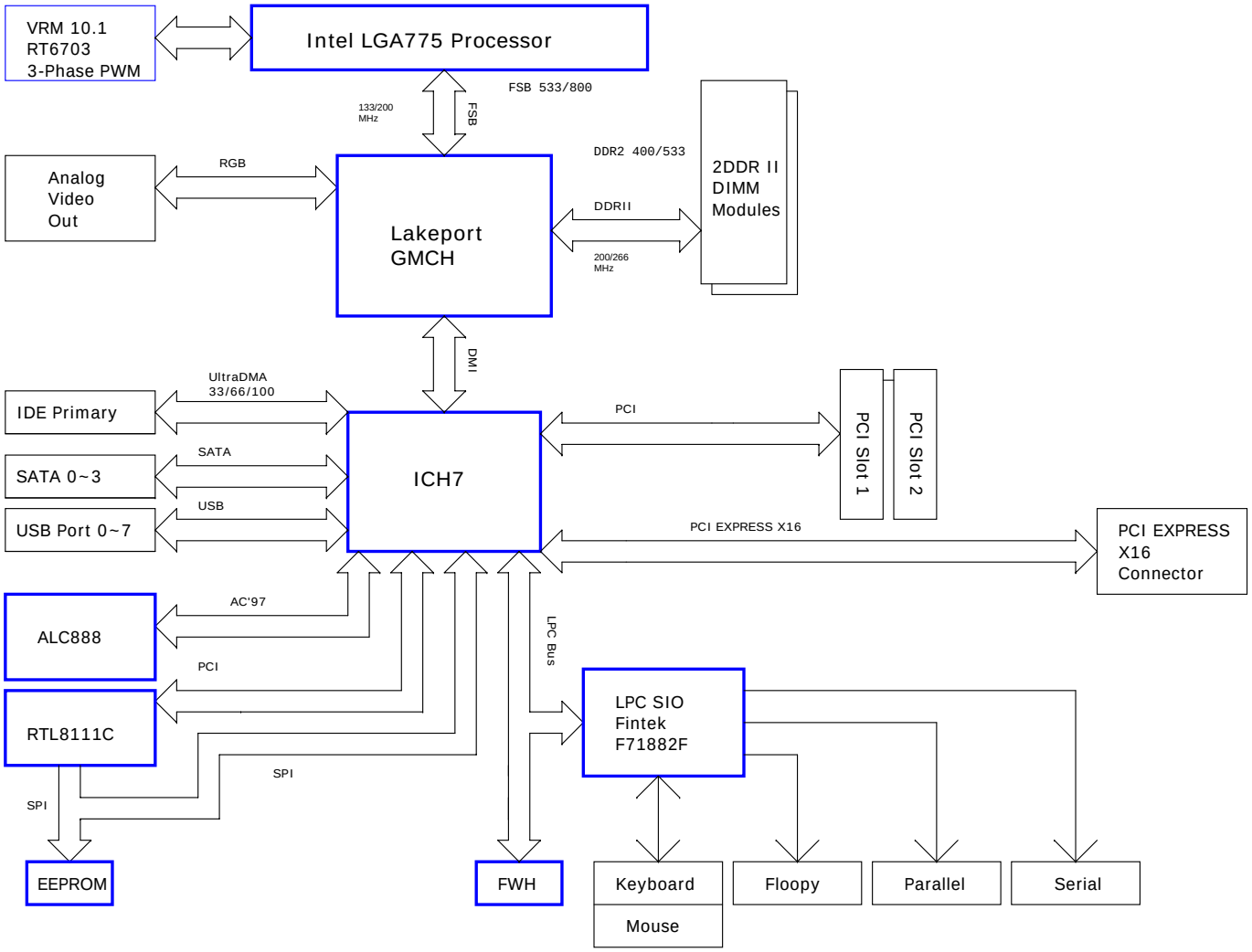
MICRO-STAR INT'L CO.,LTD

MS-7507

Size	Document Description	Rev
Custom	Cover Sheet	0A

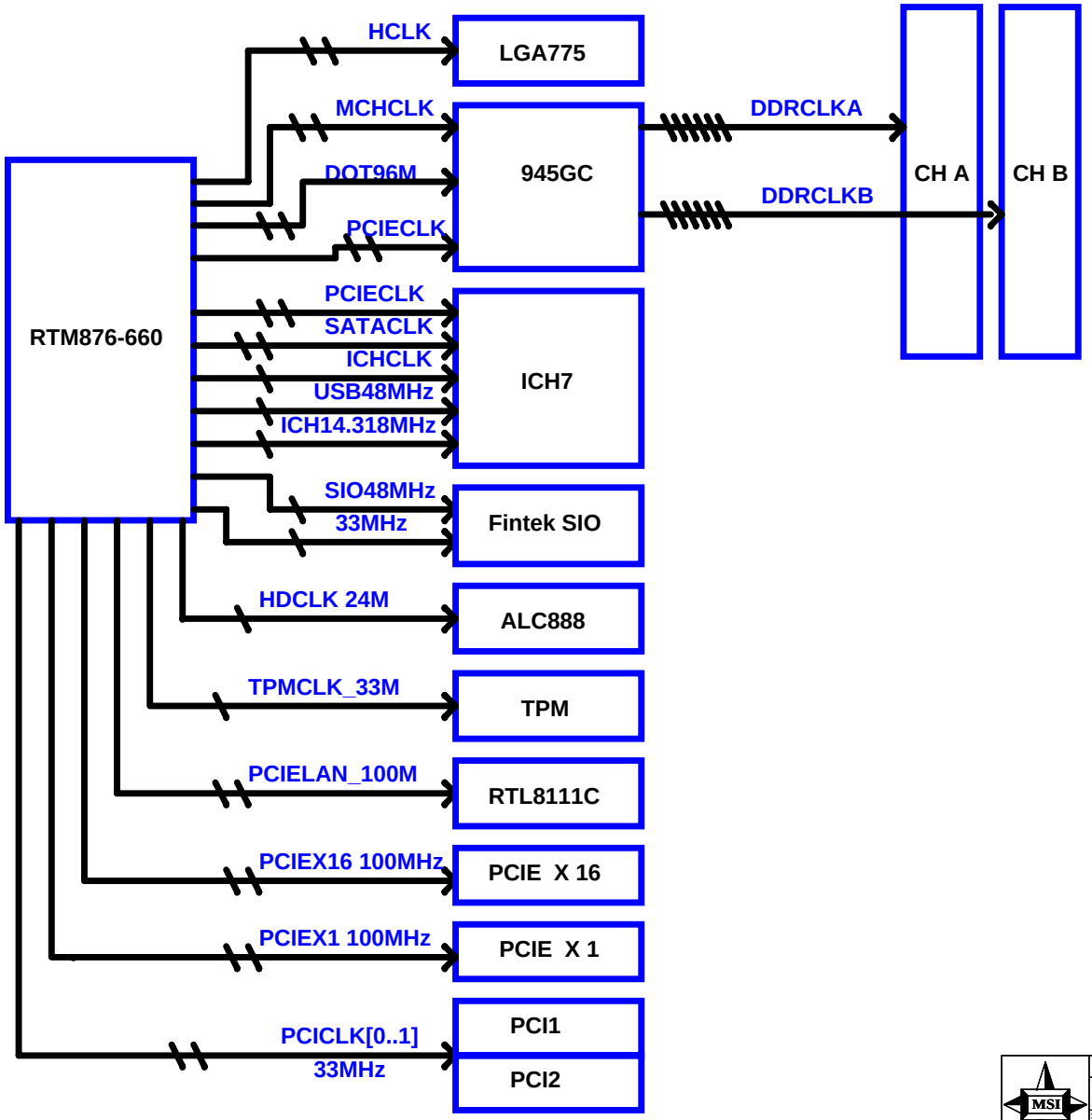
Date: Wednesday, August 29, 2007 Sheet 1 of 34

Block Diagram

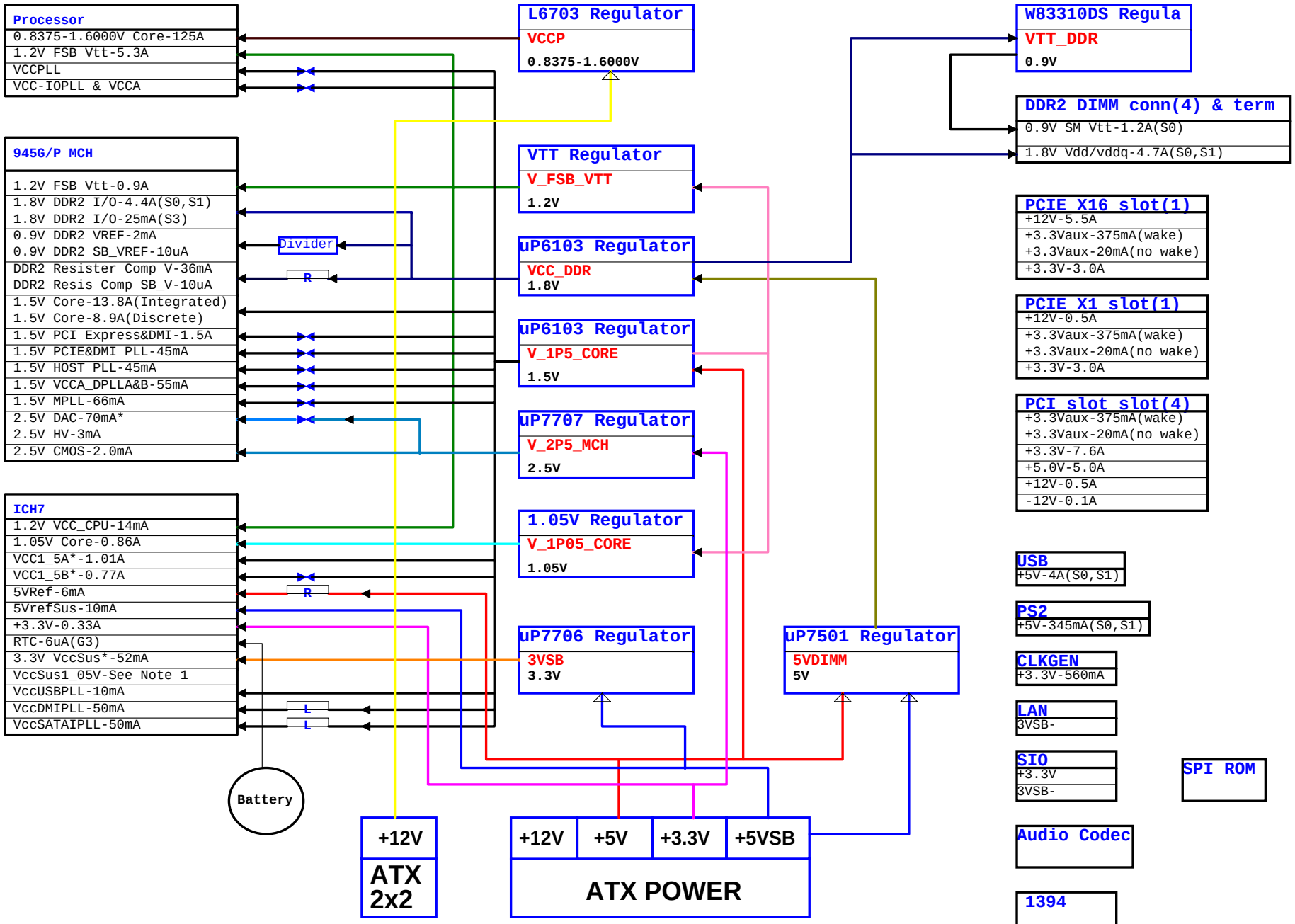


MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 2 of 34	

CLOCK MAP



MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: CLOCK MAP	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 3 of 34	

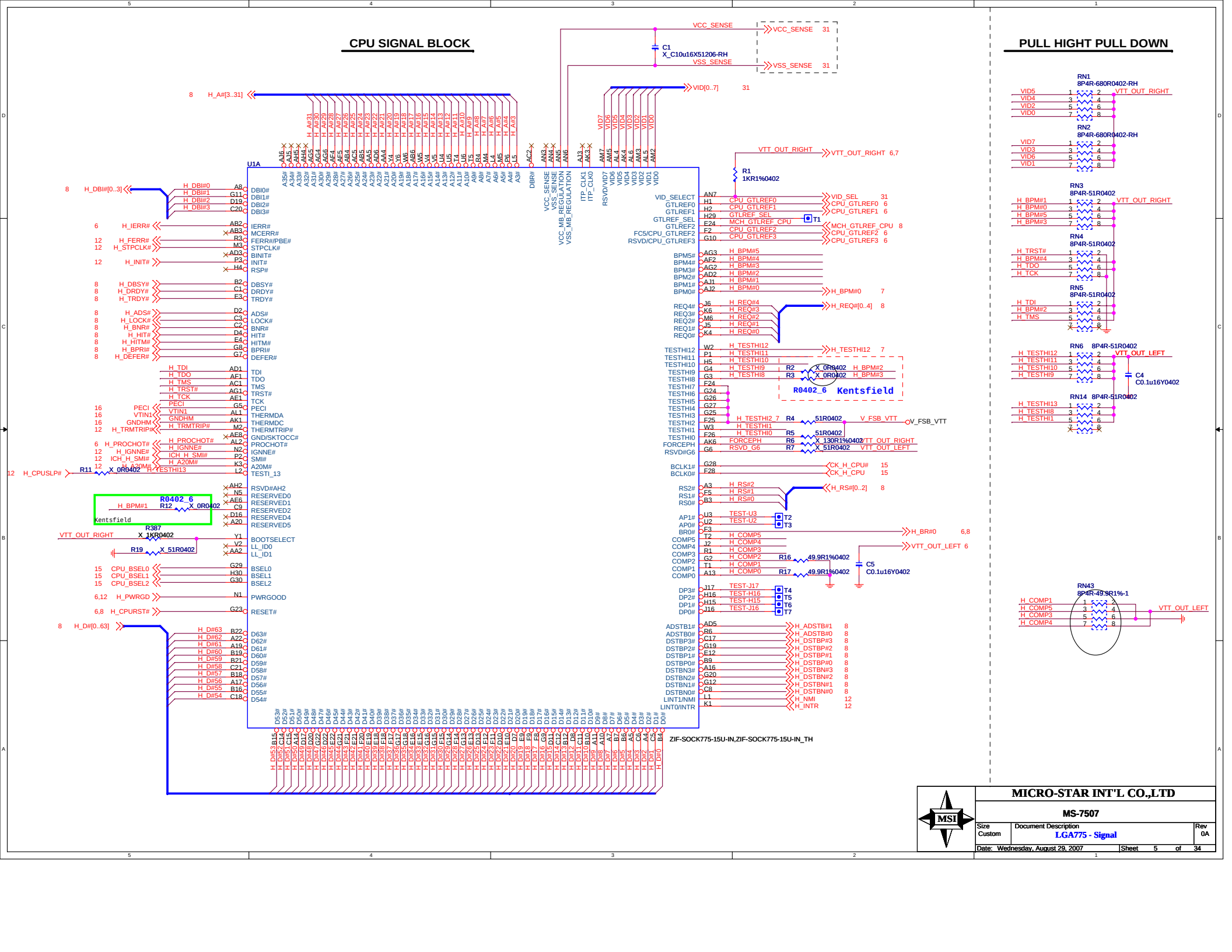


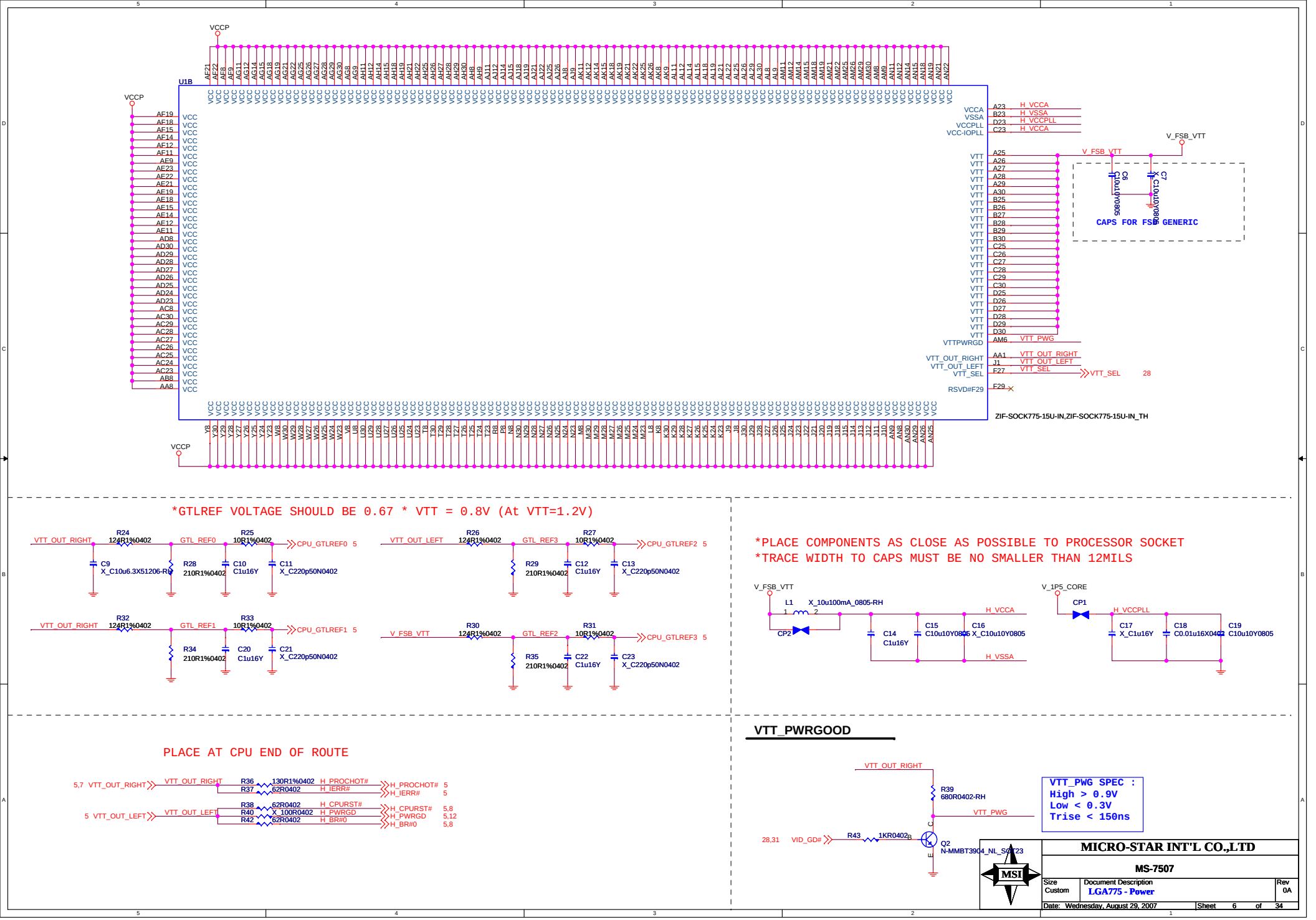
MICRO-STAR INT'L CO.,LTD

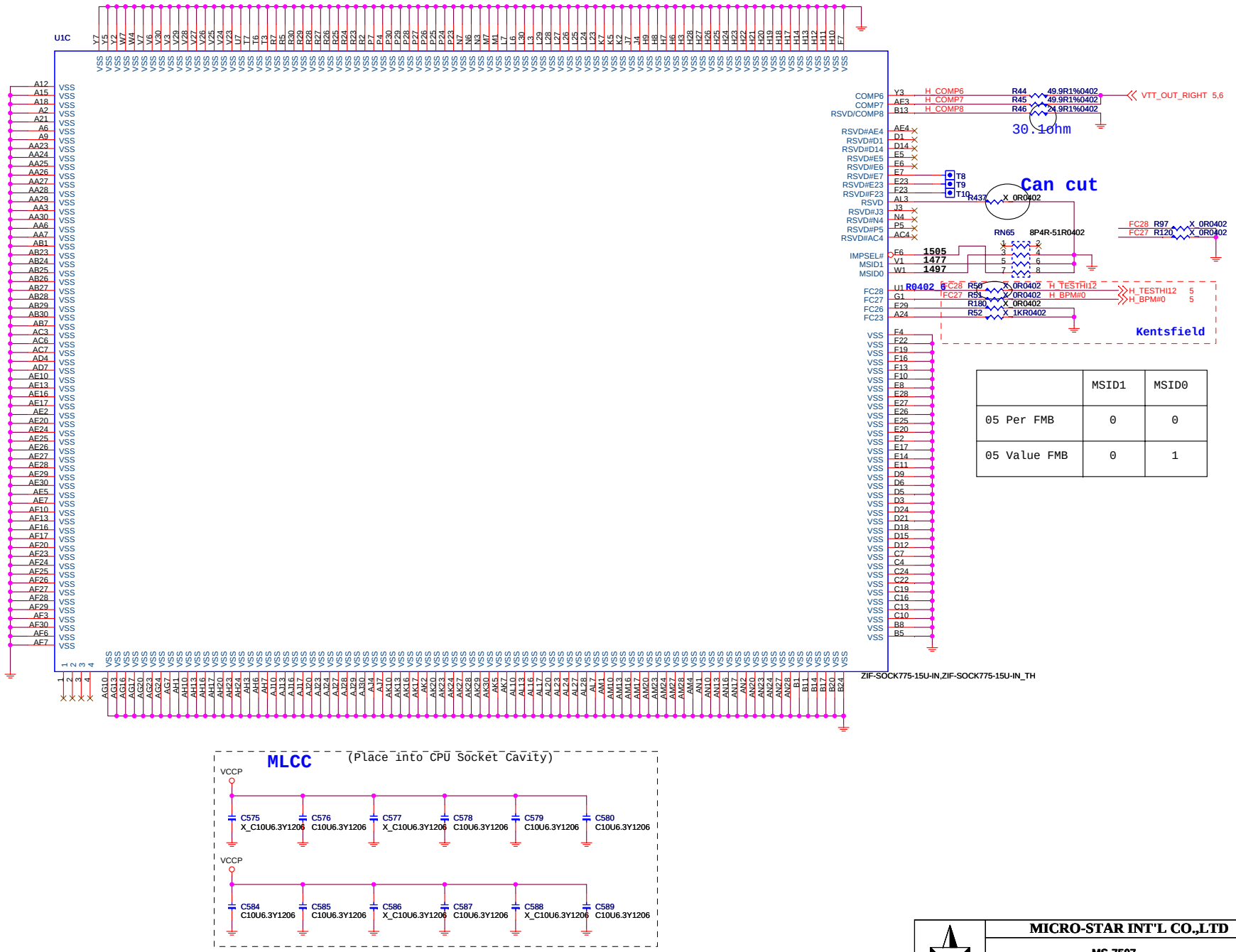
MS-7507

Size	Document Description	Rev
Custom	LGA775 - Signal	0A

Date: Wednesday, August 29, 2007 Sheet 4 of 34


CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
U1A
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
R0402_6 Kentsfield
MICRO-STAR INT'L CO.,LTD
MS-7507
LGA775 - Signal
Date: Wednesday, August 29, 2007
Sheet 5 of 34


U1B
VCCP
VCC
VCCA
VSSA
VCCPLL
VCC-IOPLL
VTT
VTTPWRGD
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
RSVD#F29
H_VCCA
H_VSSA
H_VCCPLL
VTT_PWG
V_FSB_VTT
C6 C10u10Y0805
C7 X_C10u10Y0805
CAPS FOR FSB GENERIC
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)
R24 124R1%0402
R25 100R1%0402
R26 124R1%0402
R27 100R1%0402
R28 210R1%0402
R29 210R1%0402
R32 124R1%0402
R33 100R1%0402
R34 210R1%0402
R30 124R1%0402
R31 100R1%0402
R35 210R1%0402
C9 X_C10u6.3X51206-RH
C10 C1u16Y
C11 X_C220p50N0402
C12 C1u16Y
C13 X_C220p50N0402
C20 C1u16Y
C21 X_C220p50N0402
C22 C1u16Y
C23 X_C220p50N0402
GTL_REF0
GTL_REF3
GTL_REF1
GTL_REF2
CPU_GTLREF0
CPU_GTLREF2
CPU_GTLREF1
CPU_GTLREF3
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
V_FSB_VTT
V_1P5_CORE
L1 X_10u100mA_0805-RH
CP1
CP2
C14 C1u16Y
C15 C10u10Y0805
C16 X_C10u10Y0805
C17 X_C1u16Y
C18 C0.01u16X0402
C19 C10u10Y0805
PLACE AT CPU END OF ROUTE
5,7 VTT_OUT_RIGHT
5 VTT_OUT_LEFT
R36 130R1%0402
R37 62R0402
R38 62R0402
R40 X_100R0402
R42 62R0402
H_PROCHOT#
H_IERR#
H_CPURST#
H_PWRGD
H_BR#0
VTT_PWRGOOD
R39 680R0402-RH
R43 1KR0402
28,31 VID_GD#
Q2 N-MMBT3904_NL_SOT23
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
MICRO-STAR INT'L CO.,LTD
MS-7507
Size Custom
Document Description LGA775 - Power
Rev 0A
Date: Wednesday, August 29, 2007
Sheet 6 of 34



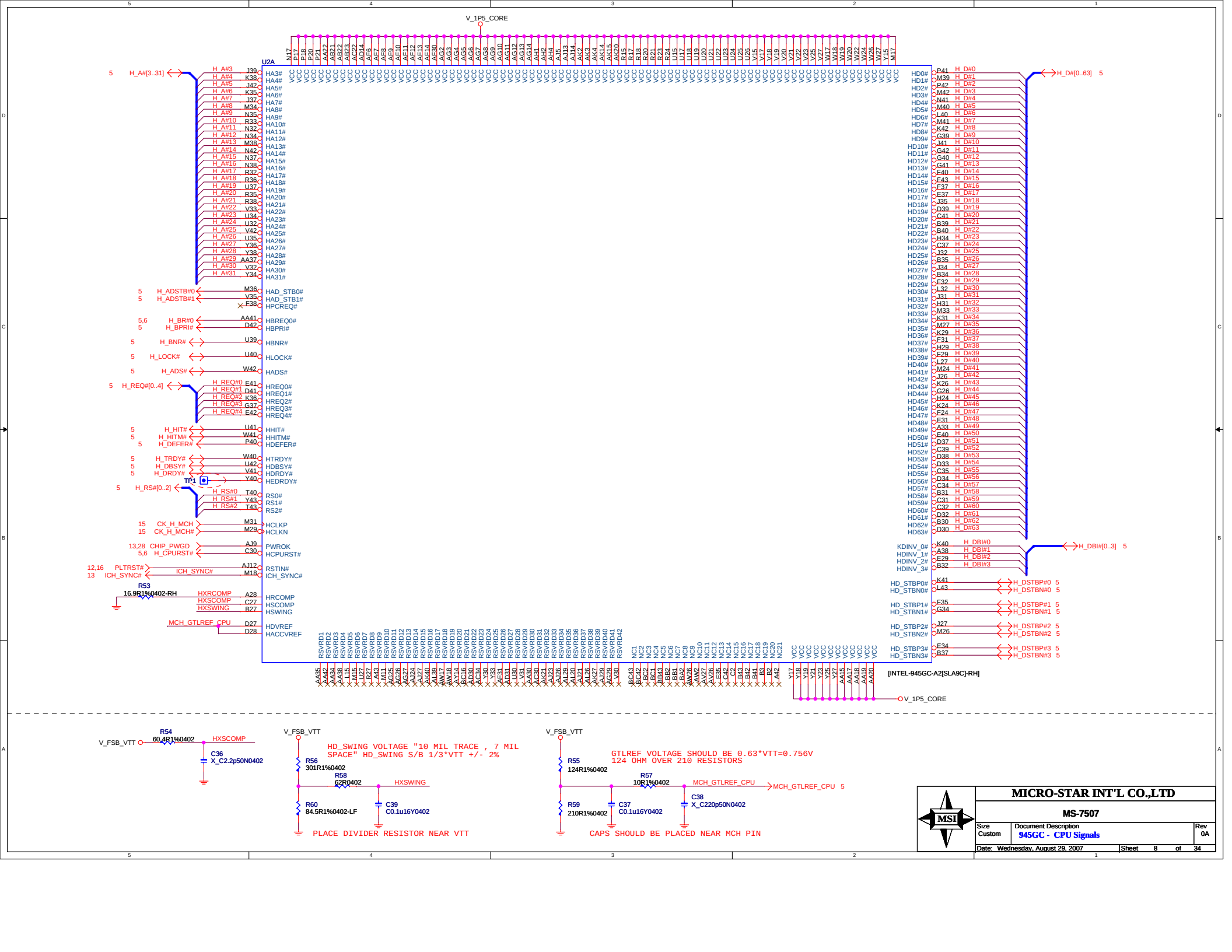
	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

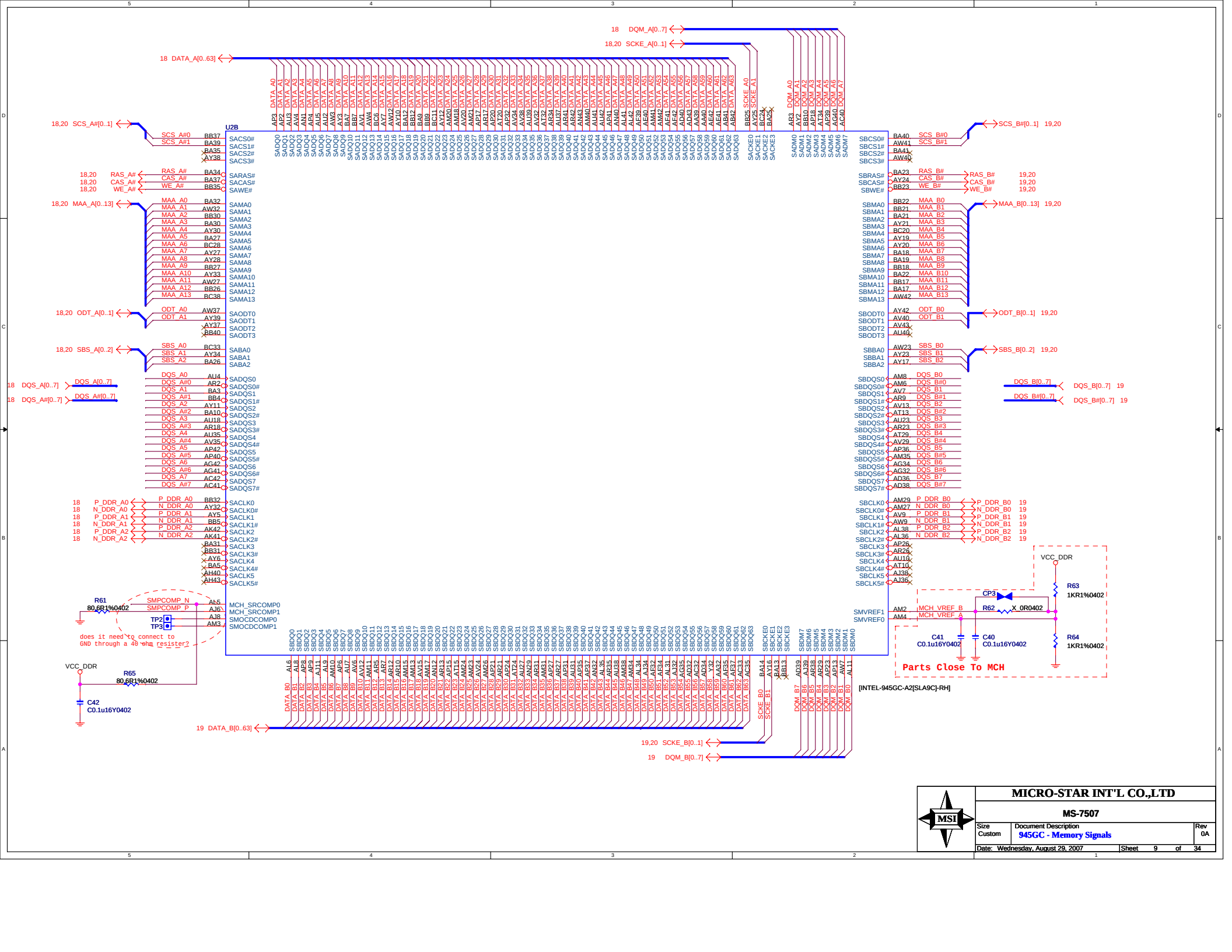
MICRO-STAR INT'L CO.,LTD

MS-7507

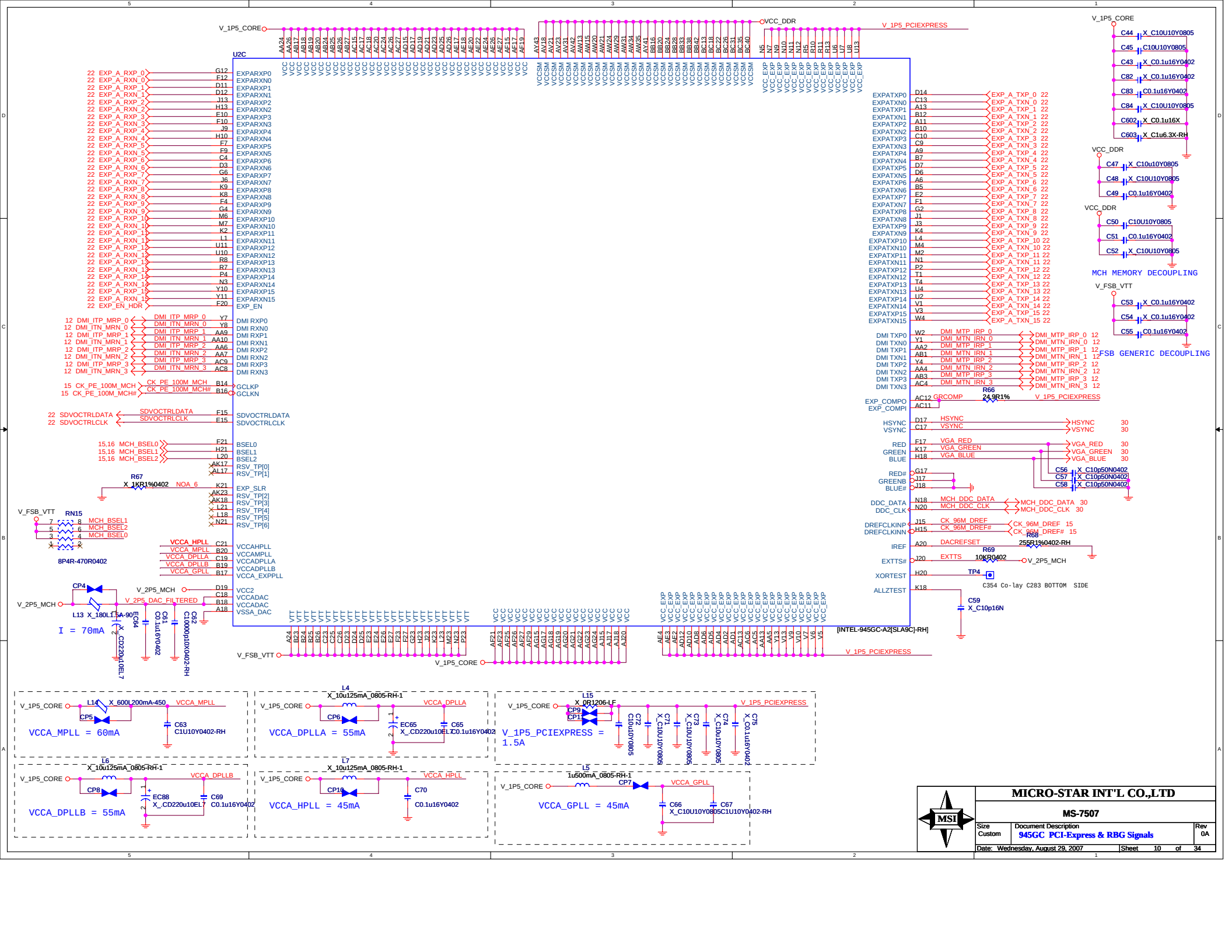
Size	Document Description	Rev
Custom	LGA775 - GND	0A

Date: Monday, September 10, 2007 Sheet 7 of 34


V_1P5_CORE
U2A
H_A#[3..31]
H_ADSTB#0
H_ADSTB#1
H_BR#0
H_BPRI#
H_BNR#
H_LOCK#
H_ADS#
H_REQ#[0..4]
H_HIT#
H_HITM#
H_DEFER#
H_TRDY#
H_DBSY#
H_DRDY#
TP1
H_RS#[0..2]
CK_H_MCH
CK_H_MCH#
CHIP_PWGD
H_CPURST#
PLTRST#
ICH_SYNC#
R53
16.9R1%0402-RH
HXRCOMP
HXSCOMP
HXSWING
MCH_GTLREF_CPU
H_D#[0..63]
H_DBI#[0..3]
H_DSTBP#0
H_DSTBN#0
H_DSTBP#1
H_DSTBN#1
H_DSTBP#2
H_DSTBN#2
H_DSTBP#3
H_DSTBN#3
[INTEL-945GC-A2[SLA9C]-RH]
V_1P5_CORE
R54
60.4R1%0402
V_FSB_VTT
HXSCOMP
C36
X_C2.2p50N0402
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/3*VTT +/- 2%
R56
301R1%0402
R58
62R0402
HXSWING
R60
84.5R1%0402-LF
C39
C0.1u16Y0402
PLACE DIVIDER RESISTOR NEAR VTT
GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
124 OHM OVER 210 RESISTORS
R55
124R1%0402
R57
10R1%0402
MCH_GTLREF_CPU
R59
210R1%0402
C37
C0.1u16Y0402
C38
X_C220p50N0402
CAPS SHOULD BE PLACED NEAR MCH PIN
MICRO-STAR INT'L CO.,LTD
MS-7507
Size
Custom
Document Description
945GC - CPU Signals
Rev
0A
Date: Wednesday, August 29, 2007
Sheet 8 of 34



MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: 945GC - Memory Signals
Rev: 0A	
Date: Wednesday, August 29, 2007	Sheet 9 of 34


U2C
[INTEL-945GC-A2[SLA9C]-RH]
V_1P5_CORE
VCC_DDR
V_1P5_PCIEXPRESS
V_FSB_VTT
V_2P5_MCH
MCH MEMORY DECOUPLING
FSB GENERIC DECOUPLING
VCCA_MPLL = 60mA
VCCA_DPLLA = 55mA
V_1P5_PCIEXPRESS = 1.5A
VCCA_DPLLB = 55mA
VCCA_HPLL = 45mA
VCCA_GPLL = 45mA
I = 70mA
MICRO-STAR INT'L CO.,LTD
MS-7507
945GC PCI-Express & RBG Signals
Size Custom
Rev 0A
Date: Wednesday, August 29, 2007
Sheet 10 of 34

MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: Intel .945GC - GND	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 11 of 34	

ICH 7 PART 1/3

PCI INTERFACE | INTERRUPT | SPI | DIRECT MEDIA | PCI EXPRESS | CPU | LAN

U3A

GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

SPI FLASH ROM

SPI FLASH

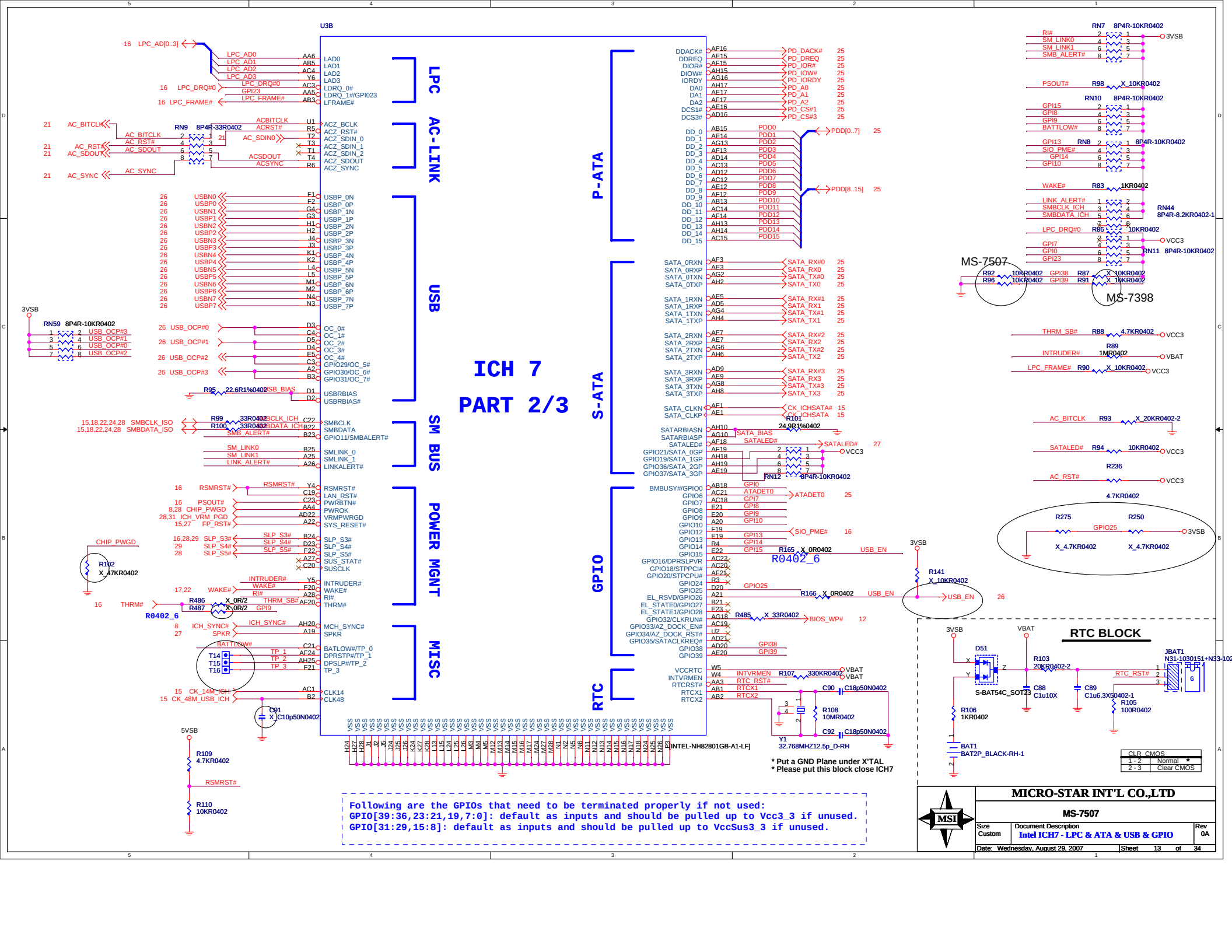
SPI DEBUG PROT

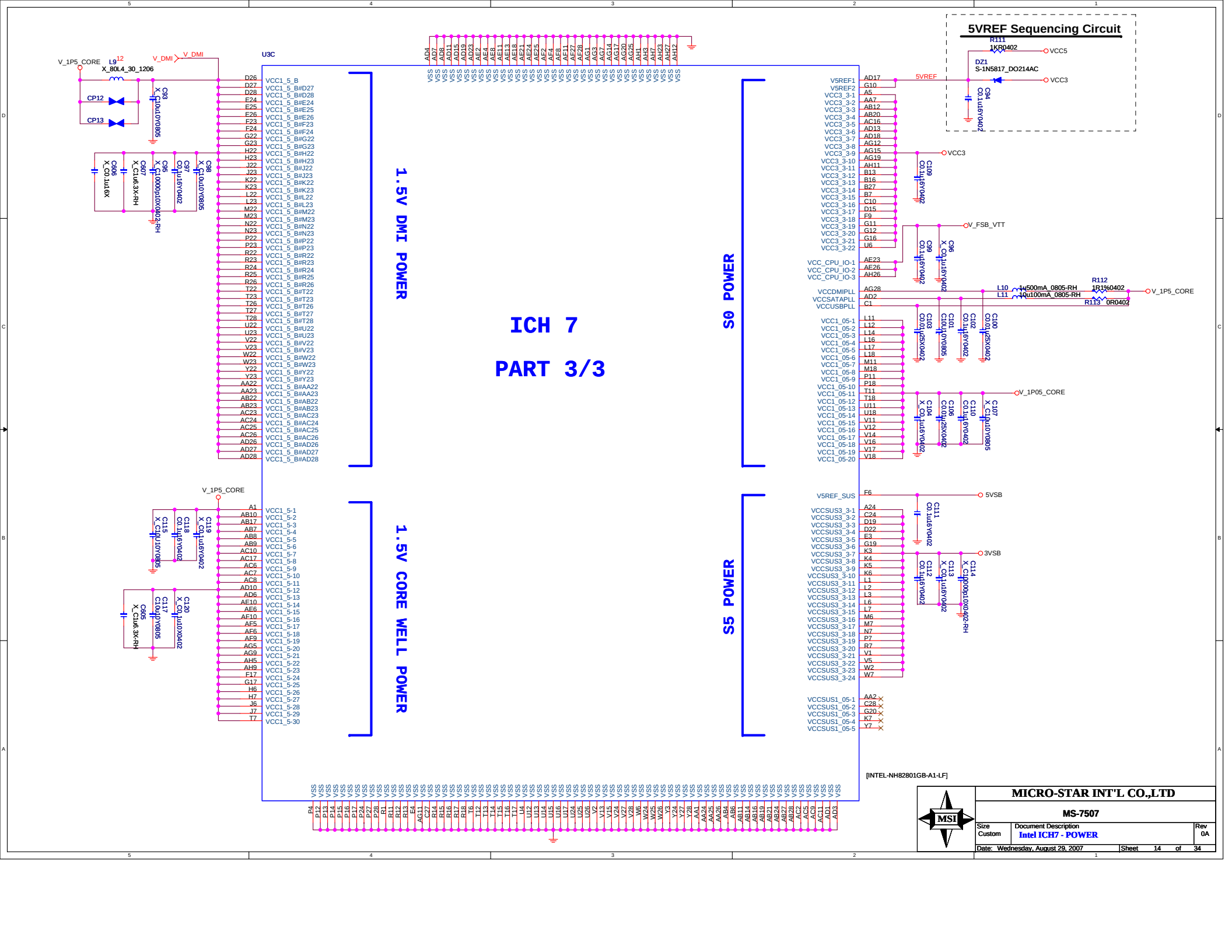
Close to SPI ROM

Closer to SB.

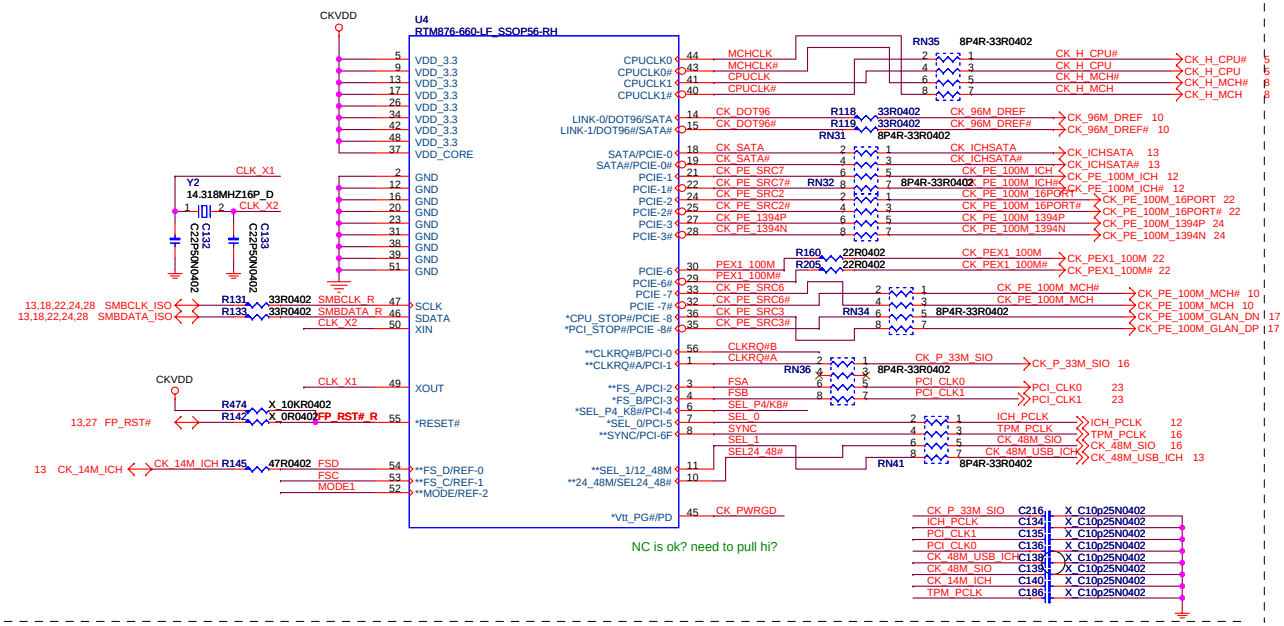
[INTEL-NH82801GB-A1-LF]

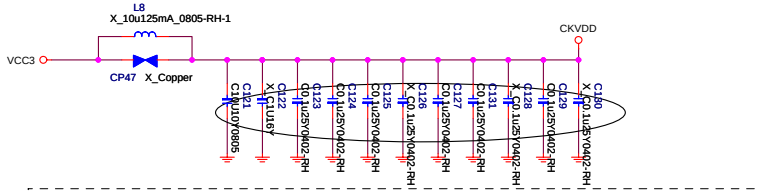
Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7507
Size	Custom
Document Description	Intel ICH7 - PCI & DMI & CPU & IRQ
Rev	0A
Date	Wednesday, August 29, 2007
Sheet	12 of 34


ICH 7
PART 2/3
U3B
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
[INTEL-NH82801GB-A1-LF]
RTC BLOCK
MICRO-STAR INT'L CO.,LTD
MS-7507
Intel ICH7 - LPC & ATA & USB & GPIO
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
* Put a GND Plane under X'TAL
* Please put this block close ICH7

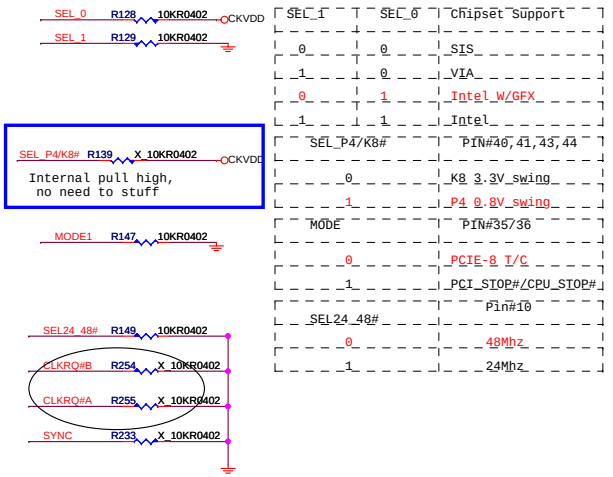

ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
U3C
5VREF Sequencing Circuit
R111 1KR0402
VCC5
DZ1 S-1N5817_DO214AC
VCC3
C94 C0.1u16Y0402
5VREF
V_1P5_CORE
L9 X_80L4_30_1206
V_DMI
CP12
CP13
C93 X_C10u10Y0805
C606 X_C0.1u16X
C607 X_C1u6.3X-RH
C95 X_C10000p10X0402-RH
C97 C0.1u16Y0402
C98 X_C10u10Y0805
VCC1_5_B
VCC1_5_B#D27
VCC1_5_B#D28
VCC1_5_B#E24
VCC1_5_B#E25
VCC1_5_B#E26
VCC1_5_B#F23
VCC1_5_B#F24
VCC1_5_B#G22
VCC1_5_B#G23
VCC1_5_B#H22
VCC1_5_B#H23
VCC1_5_B#J22
VCC1_5_B#J23
VCC1_5_B#K22
VCC1_5_B#K23
VCC1_5_B#L22
VCC1_5_B#L23
VCC1_5_B#M22
VCC1_5_B#M23
VCC1_5_B#N22
VCC1_5_B#N23
VCC1_5_B#P22
VCC1_5_B#P23
VCC1_5_B#R22
VCC1_5_B#R23
VCC1_5_B#R24
VCC1_5_B#R25
VCC1_5_B#R26
VCC1_5_B#T22
VCC1_5_B#T23
VCC1_5_B#T26
VCC1_5_B#T27
VCC1_5_B#T28
VCC1_5_B#U22
VCC1_5_B#U23
VCC1_5_B#V22
VCC1_5_B#V23
VCC1_5_B#W22
VCC1_5_B#W23
VCC1_5_B#Y22
VCC1_5_B#Y23
VCC1_5_B#AA22
VCC1_5_B#AA23
VCC1_5_B#AB22
VCC1_5_B#AB23
VCC1_5_B#AC23
VCC1_5_B#AC24
VCC1_5_B#AC25
VCC1_5_B#AC26
VCC1_5_B#AD26
VCC1_5_B#AD27
VCC1_5_B#AD28
V_1P5_CORE
C115 X_C10u10Y0805
C118 C0.1u16Y0402
C119 X_C1u16Y0402
C805 X_C1u6.3X-RH
C117 C10u10Y0805
C120 X_C1u10X0402
VCC1_5-1
VCC1_5-2
VCC1_5-3
VCC1_5-4
VCC1_5-5
VCC1_5-6
VCC1_5-7
VCC1_5-8
VCC1_5-9
VCC1_5-10
VCC1_5-11
VCC1_5-12
VCC1_5-13
VCC1_5-14
VCC1_5-15
VCC1_5-16
VCC1_5-17
VCC1_5-18
VCC1_5-19
VCC1_5-20
VCC1_5-21
VCC1_5-22
VCC1_5-23
VCC1_5-24
VCC1_5-25
VCC1_5-26
VCC1_5-27
VCC1_5-28
VCC1_5-29
VCC1_5-30
V5REF1
V5REF2
VCC3_3-1
VCC3_3-2
VCC3_3-3
VCC3_3-4
VCC3_3-5
VCC3_3-6
VCC3_3-7
VCC3_3-8
VCC3_3-9
VCC3_3-10
VCC3_3-11
VCC3_3-12
VCC3_3-13
VCC3_3-14
VCC3_3-15
VCC3_3-16
VCC3_3-17
VCC3_3-18
VCC3_3-19
VCC3_3-20
VCC3_3-21
VCC3_3-22
VCC3
C109 C0.1u16Y0402
V_FSB_VTT
C99 C0.1u16Y0402
C96 X_C1u16Y0402
VCC_CPU_IO-1
VCC_CPU_IO-2
VCC_CPU_IO-3
VCCDMIPLL
VCCSATAPLL
VCCUSBPLL
L10 1u500mA_0805-RH
L11 10u100mA_0805-RH
R112 1R1%0402
R113 0R0402
V_1P5_CORE
C103 C0.01u25X0402
C101 C10u10Y0805
C102 C0.1u16Y0402
C100 C0.01u25X0402
VCC1_05-1
VCC1_05-2
VCC1_05-3
VCC1_05-4
VCC1_05-5
VCC1_05-6
VCC1_05-7
VCC1_05-8
VCC1_05-9
VCC1_05-10
VCC1_05-11
VCC1_05-12
VCC1_05-13
VCC1_05-14
VCC1_05-15
VCC1_05-16
VCC1_05-17
VCC1_05-18
VCC1_05-19
VCC1_05-20
V_1P05_CORE
C104 X_C1u16Y0402
C106 C0.01u25X0402
C110 C0.1u16Y0402
C107 X_C10u10Y0805
V5REF_SUS
VCCSUS3_3-1
VCCSUS3_3-2
VCCSUS3_3-3
VCCSUS3_3-4
VCCSUS3_3-5
VCCSUS3_3-6
VCCSUS3_3-7
VCCSUS3_3-8
VCCSUS3_3-9
VCCSUS3_3-10
VCCSUS3_3-11
VCCSUS3_3-12
VCCSUS3_3-13
VCCSUS3_3-14
VCCSUS3_3-15
VCCSUS3_3-16
VCCSUS3_3-17
VCCSUS3_3-18
VCCSUS3_3-19
VCCSUS3_3-20
VCCSUS3_3-21
VCCSUS3_3-22
VCCSUS3_3-23
VCCSUS3_3-24
5VSB
C111 C0.1u16Y0402
3VSB
C112 C0.1u16Y0402
C113 X_C1u16Y0402
C114 X_C10000p10X0402-RH
VCCSUS1_05-1
VCCSUS1_05-2
VCCSUS1_05-3
VCCSUS1_05-4
VCCSUS1_05-5
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INT'L CO.,LTD
MS-7507
Size Custom
Document Description Intel ICH7 - POWER
Rev 0A
Date: Wednesday, August 29, 2007
Sheet 14 of 34

Clock Generator - RTM876-660

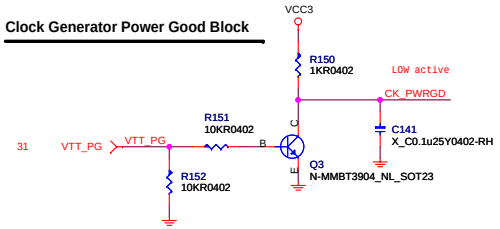


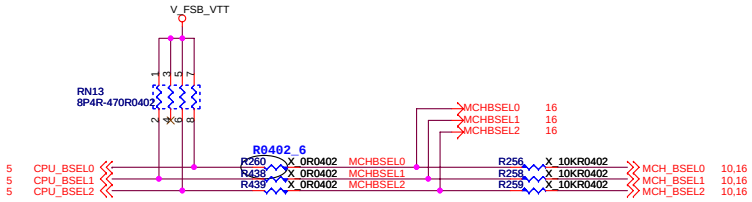


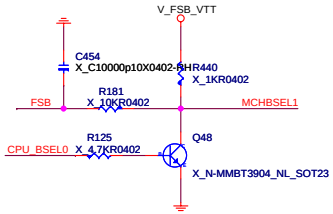
STRAPPING RESISTOR



Clock Generator Power Good Block



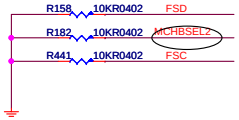




CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid

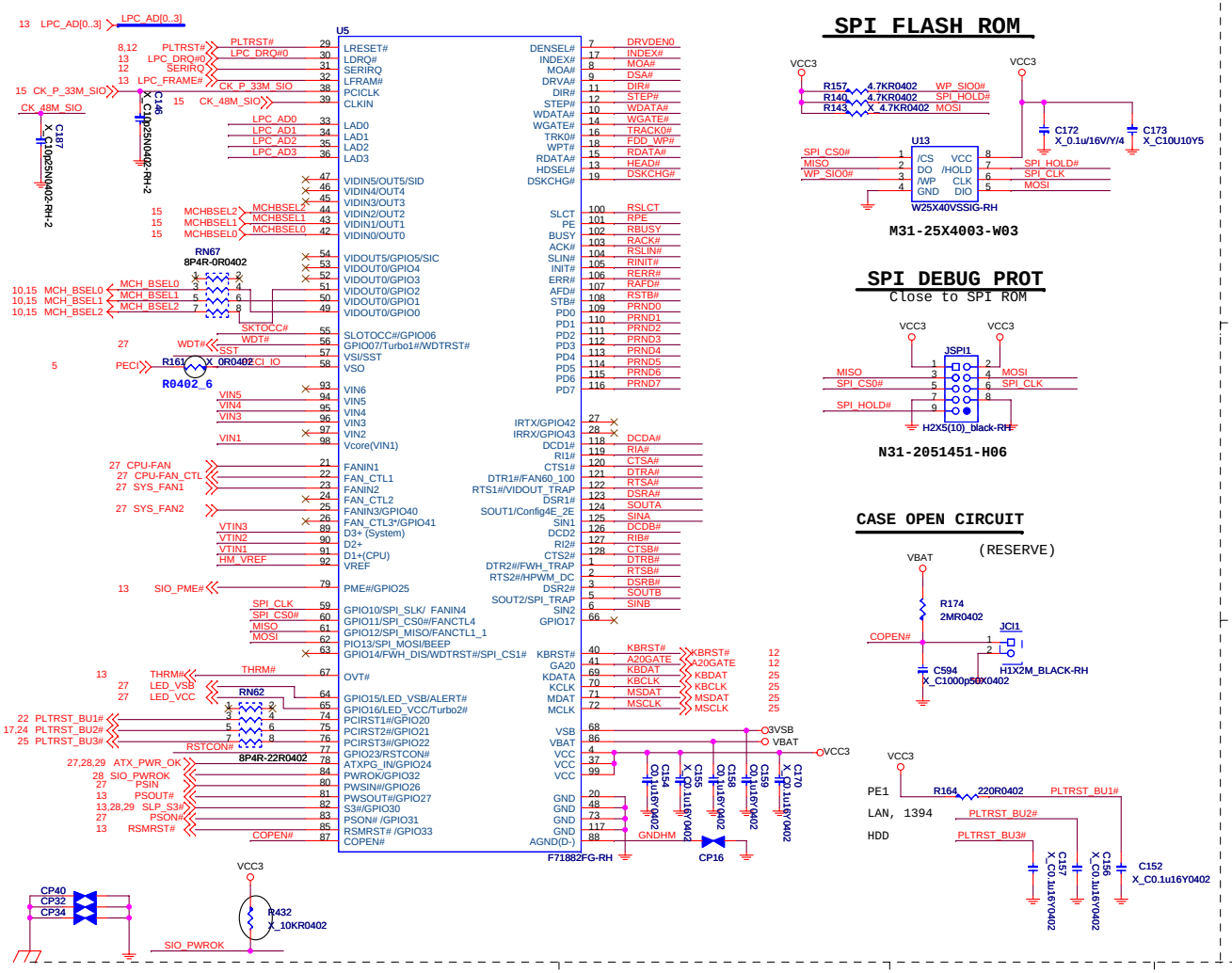


MICRO-STAR INT'L CO.,LTD

MS-7507

Size	Document Description	Rev
Custom	CLK-RTM 876-660	0A

Date: Wednesday, August 29, 2007 Sheet 15 of 34



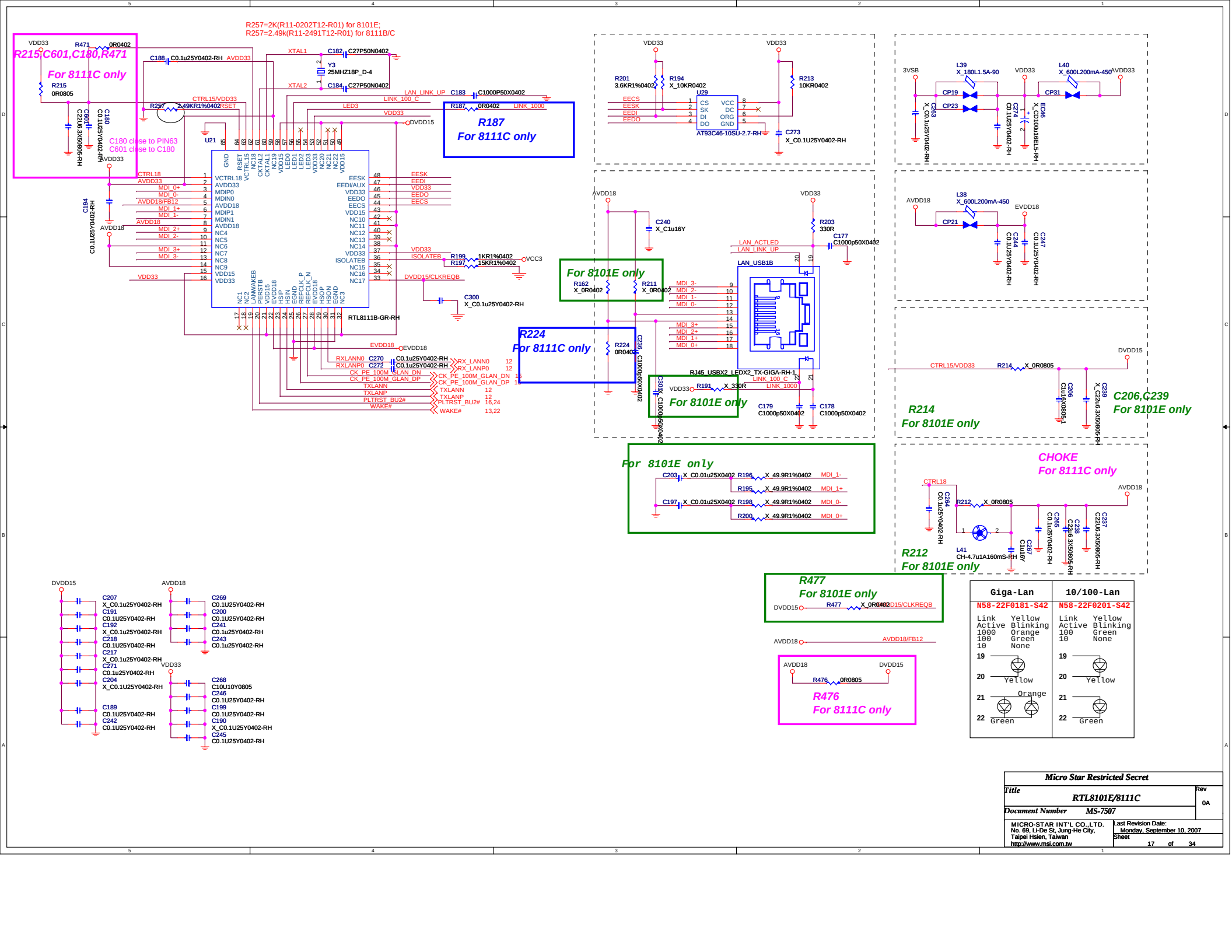
	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#, SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

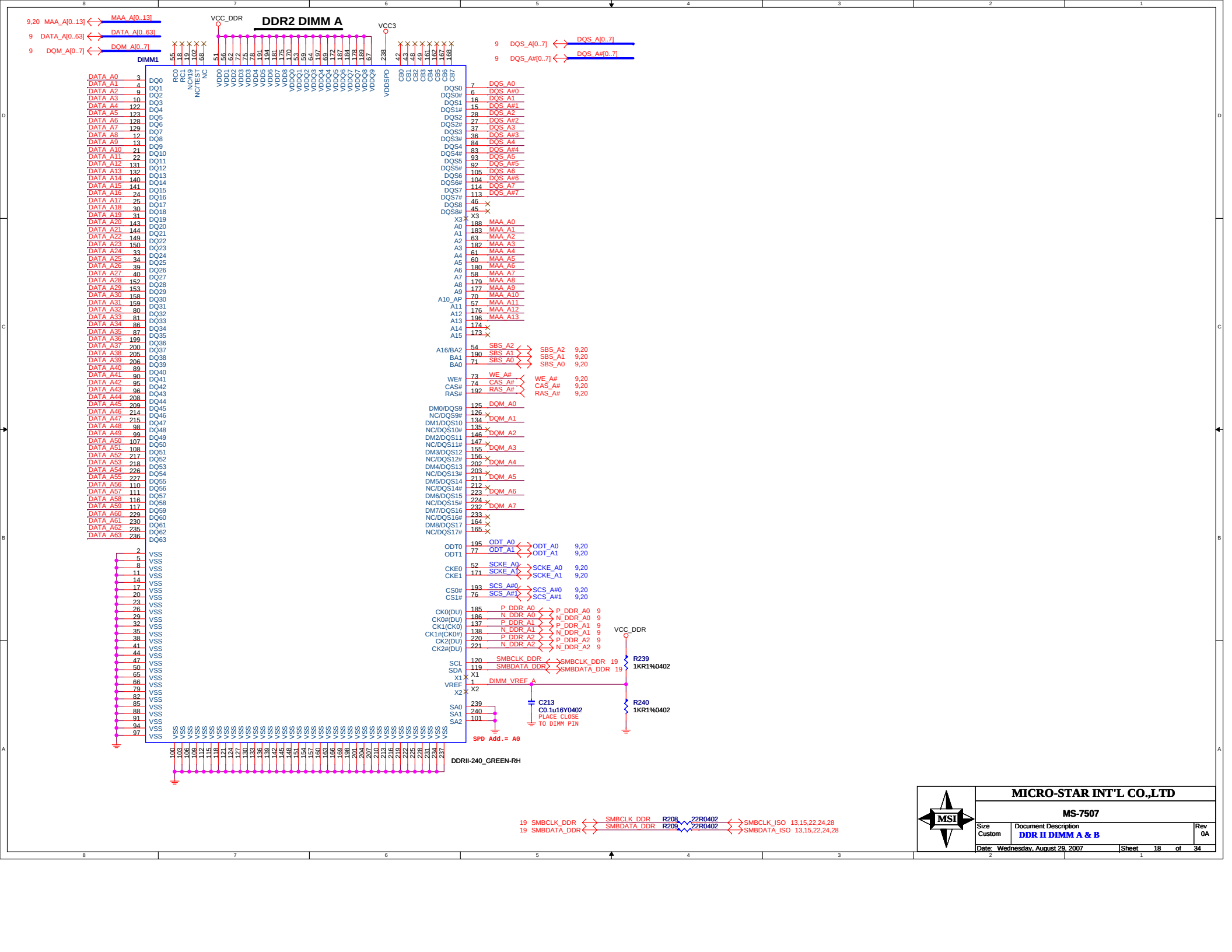
MICRO-STAR INT'L CO.,LTD

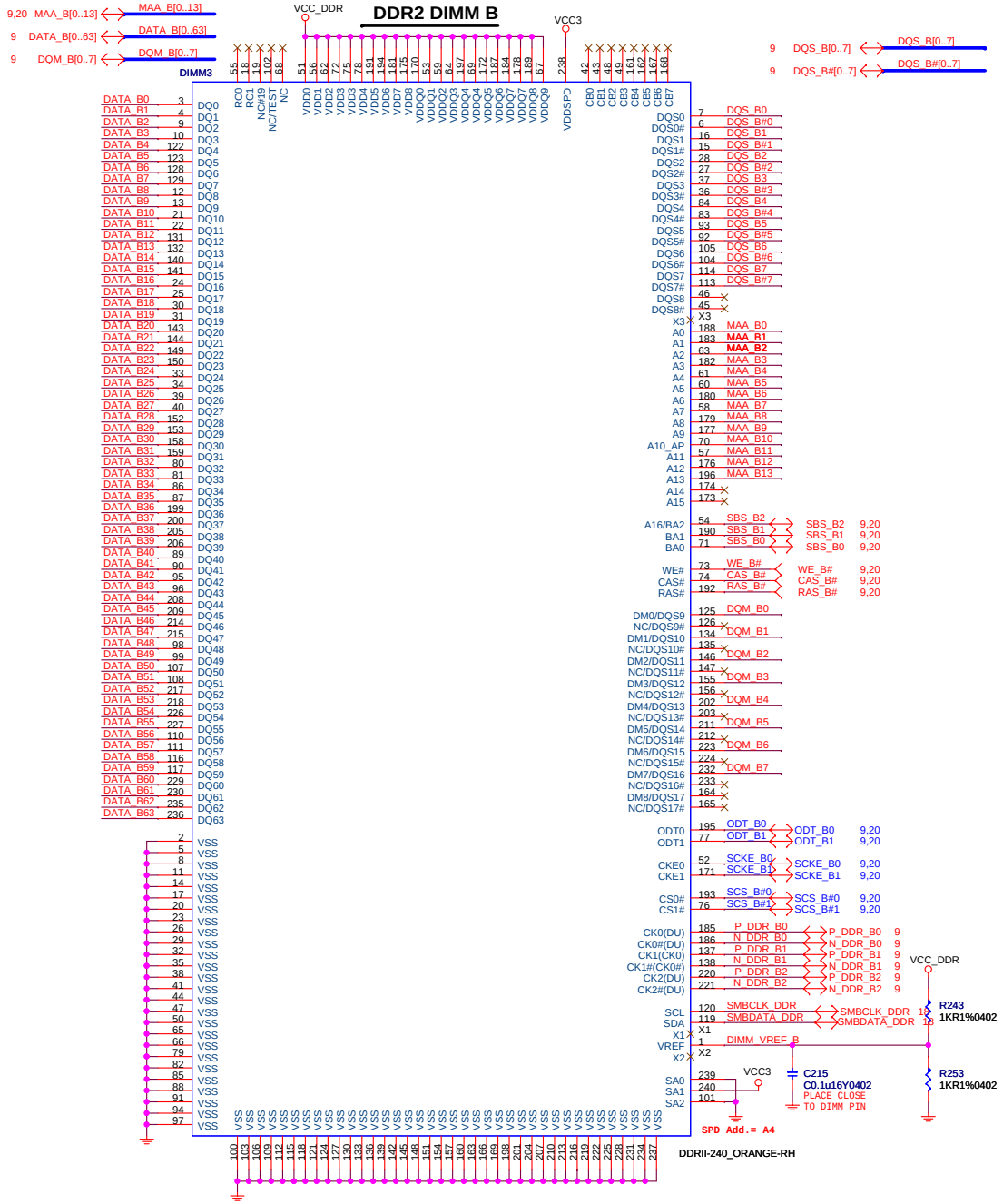
MS-7507

Size: Custom | Document Description: SIO-Fintek F71882F & IO-Port | Rev: 0A

Date: Monday, September 10, 2007 | Sheet 16 of 34


R257=2K(R11-0202T12-R01) for 8101E;
R257=2.49k(R11-2491T12-R01) for 8111B/C
R215,C601,C180,R471
For 8111C only
C180 close to PIN63
C601 close to C180
R187
For 8111C only
For 8101E only
R224
For 8111C only
For 8101E only
For 8101E only
For 8101E only
R214
For 8101E only
C206,C239
For 8101E only
CHOKE
For 8111C only
R212
For 8101E only
R477
For 8101E only
R476
For 8111C only
RTL8111B-GR-RH
Giga-Lan
N58-22F0181-S42
10/100-Lan
N58-22F0201-S42
Micro Star Restricted Secret
RTL8101E/8111C
MS-7507
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Monday, September 10, 2007
17 of 34


DDR2 DIMM A
DIMM1
VCC_DDR
VCC3
MAA_A[0..13]
DATA_A[0..63]
DQM_A[0..7]
DQS_A[0..7]
DQS_A#[0..7]
SPD Add.= A0
DDRII-240_GREEN-RH
C213
C0.1u16Y0402
PLACE CLOSE TO DIMM PIN
R239
1KR1%0402
R240
1KR1%0402
R208 22R0402
R209 22R0402
SMBCLK_ISO 13,15,22,24,28
SMBDATA_ISO 13,15,22,24,28
MICRO-STAR INT'L CO.,LTD
MS-7507
Size Custom
Document Description
DDR II DIMM A & B
Rev 0A
Date: Wednesday, August 29, 2007
Sheet 18 of 34



MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: DDR II DIMM A & B
Rev: 0A	
Date: Wednesday, August 29, 2007	Sheet 19 of 34

CHANNEL A V_SM_VTT DECOUPLING CAPS

VTT_DDR

C224 C4.7u6.3X5
C226 X_C4.7u6.3X5

VTT_DDR

C229 C0.1u16Y0402
C231 C0.1u16Y0402
C233 X_C0.1u16Y0402
C234 X_C0.1u16Y0402

CHANNEL B V_SM_VTT DECOULPING CAPS

VTT_DDR

C220 X_C4.7u6.3X5
C222 C4.7u6.3X5

VTT_DDR

C223 X_C0.1u16Y0402
C225 X_C0.1u16Y0402
C227 X_C0.1u16Y0402
C228 C0.1u16Y0402

VCC_DDR

C248 C1U10Y0402-RH
C249 C1U10Y0402-RH
C250 C1U10Y0402-RH
C251 X_C1U10Y0402-RH
C252 X_C1U10Y0402-RH
C253 C1U10Y0402-RH
C254 C1U10Y0402-RH
C255 X_C1U10Y0402-RH

VCC_DDR

C256 C1U10Y0402-RH
C257 X_C1U10Y0402-RH
C258 X_C1U10Y0402-RH
C259 X_C1U10Y0402-RH
C260 X_C1U10Y0402-RH
C261 C1U10Y0402-RH
C266 X_C1U10Y0402-RH
C262 X_C1U10Y0402-RH

VTT_DDR

RN23 8P4R-33R0402
MAA_A4 MAA_A3 MAA_A2 MAA_A1 MAA_A9 MAA_A5 MAA_A8 MAA_A6 SBS_A2 MAA_A12 MAA_A11 MAA_A7

RN25 8P4R-33R0402
RN27 8P4R-33R0402

9,18 RAS_A#
9,18 WE_A#
9,18 CAS_A#

RN46 8P4R-33R0402
RAS_A# WE_A# CAS_A# MAA_A13

RN47 8P4R-33R0402
MAA_A0 MAA_A10 SBS_A0 SBS_A1

RN60 8P4R-43R0402
ODT_A1 SCS_A#1 ODT_A0 SCS_A#0

change RN

SCKE_A0 R227 43R0402
SCKE_A1 R228 43R0402

9,18 MAA_A[0..13]
9,18 SBS_A[0..2]
9,18 SCS_A#[0..1]
9,18 SCKE_A[0..1]
9,18 ODT_A[0..1]

VTT_DDR

RN24 8P4R-33R0402
MAA_B4 MAA_B3 MAA_B2 MAA_B1 SBS_B2 MAA_B12 MAA_B11 MAA_B7 MAA_B9 MAA_B5 MAA_B8 MAA_B6

RN26 8P4R-33R0402
RN28 8P4R-33R0402

9,19 WE_B#
9,19 RAS_B#
9,19 CAS_B#

RN29 8P4R-33R0402
WE_B# RAS_B# CAS_B# MAA_B13

RN30 8P4R-33R0402
MAA_B10 MAA_B0 SBS_B0 SBS_B1

RN61 8P4R-43R0402
ODT_B1 SCS_B#1 ODT_B0 SCS_B#0

change RN

SCKE_B0 R231 43R0402
SCKE_B1 R232 43R0402

9,19 MAA_B[0..13]
9,19 SBS_B[0..2]
9,19 SCS_B#[0..1]
9,19 SCKE_B[0..1]
9,19 ODT_B[0..1]

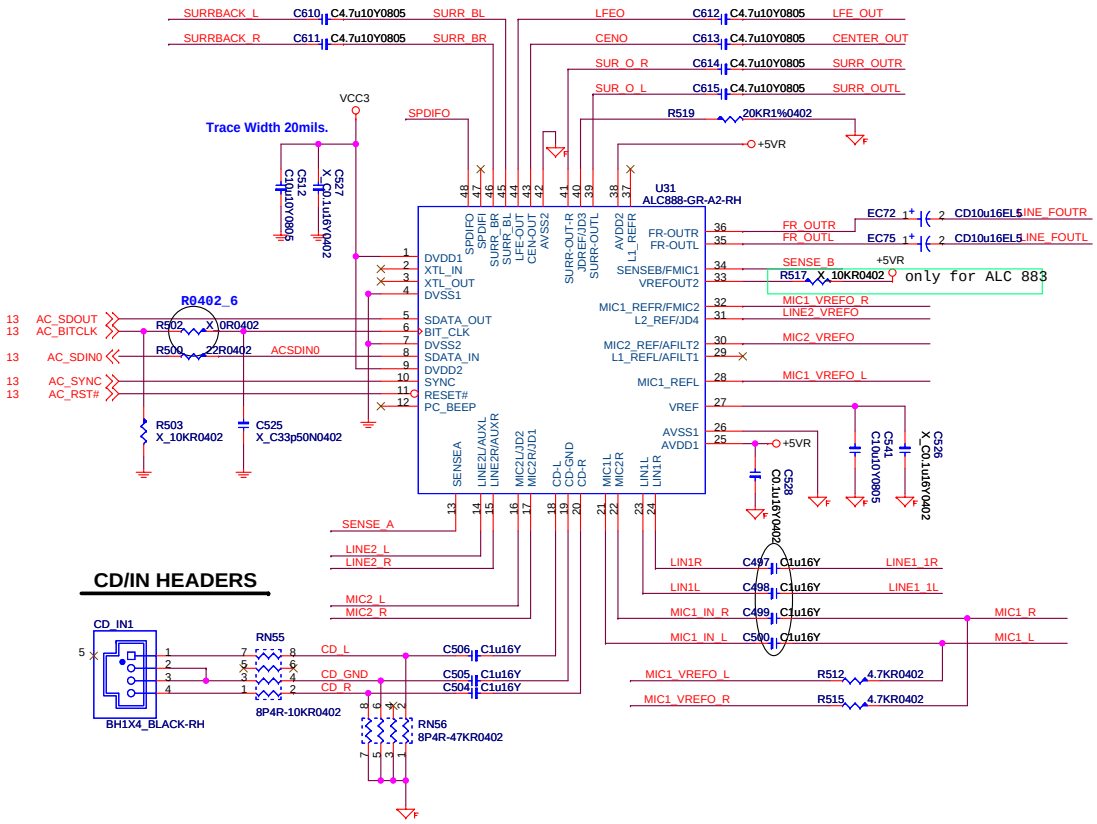
MICRO-STAR INT'L CO.,LTD

MS-7507

Size	Document Description	Rev
Custom	DDR II VTT DECOUPLING	0A

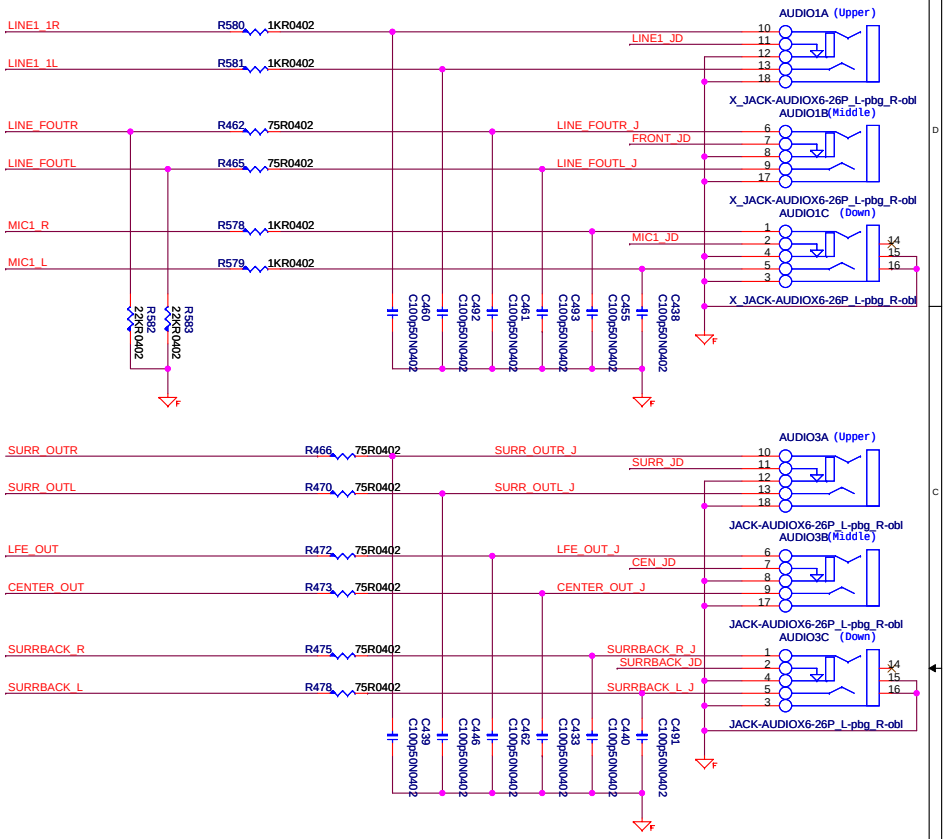
Date: Wednesday, August 29, 2007 Sheet 20 of 34

ALC888 CODEC

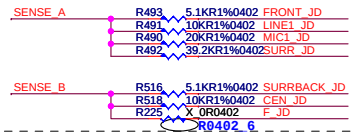


CD/IN HEADERS

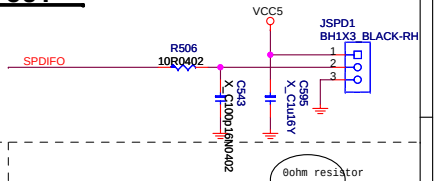
ALC888 JACK



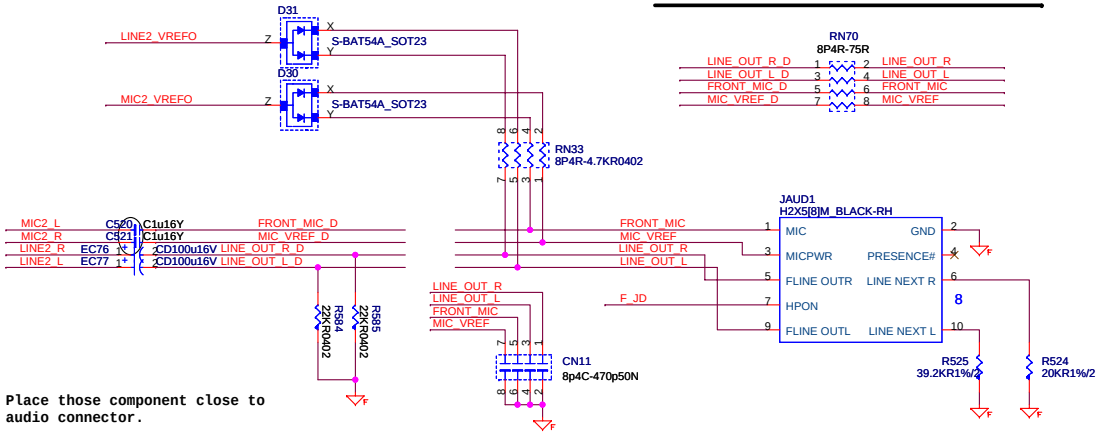
ALC883 JACK DETECT



SPDIF OUT

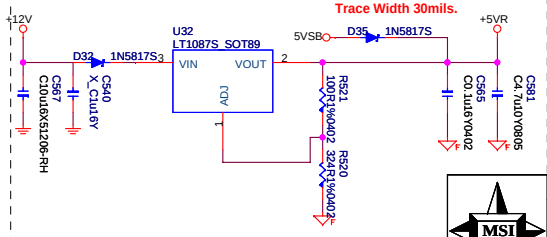


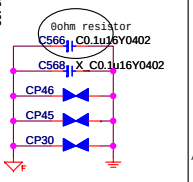
Azalia Front Audio Connector



Place those component close to audio connector.

AUDIO CODE REGULATORS

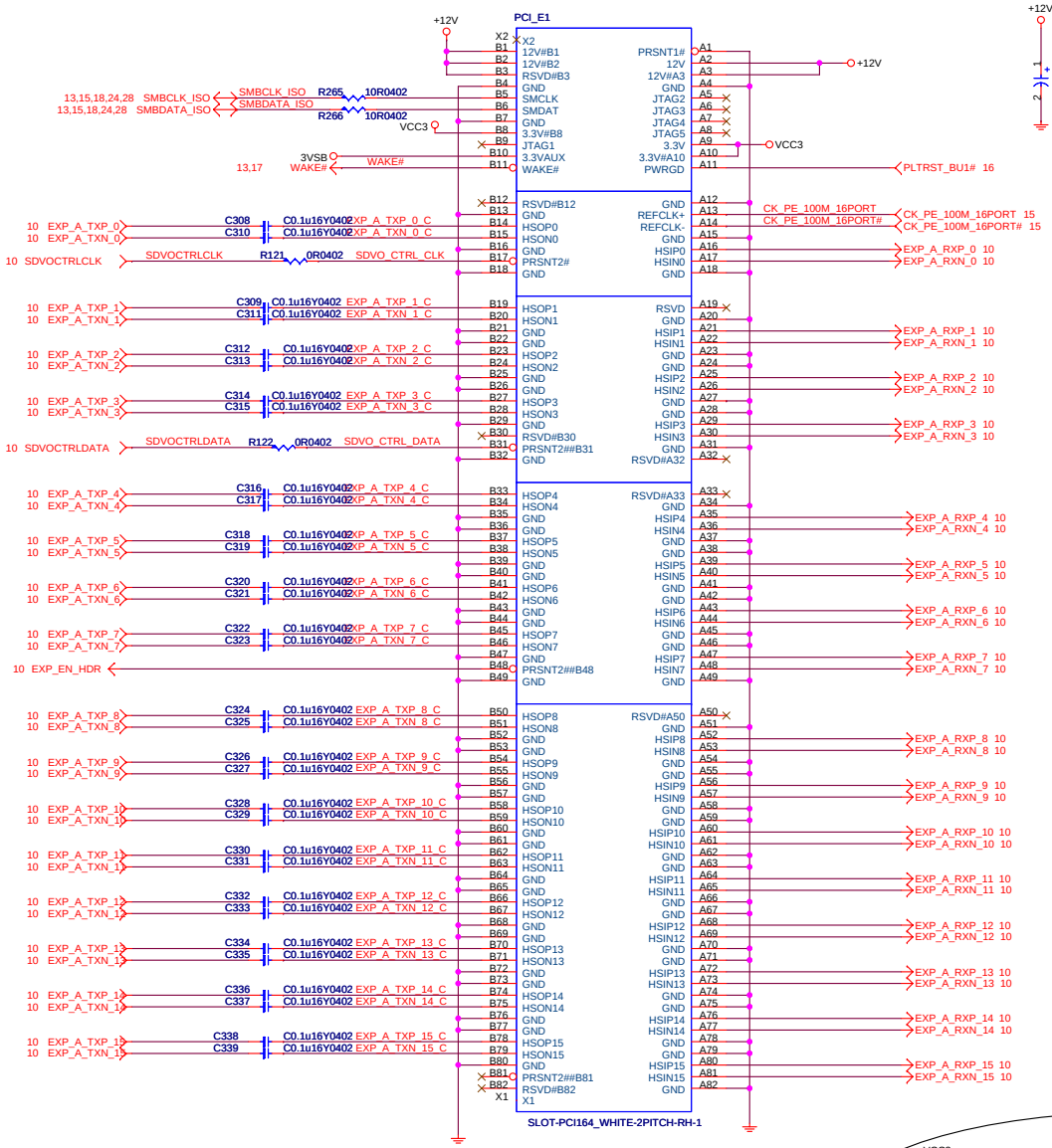




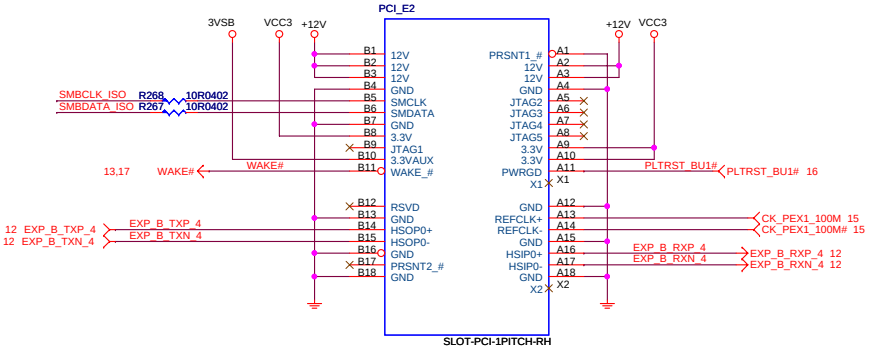
For EMI

MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: 21 HD ALC888	Rev: 0A
Date: Monday, September 10, 2007	Sheet 21 of 34	

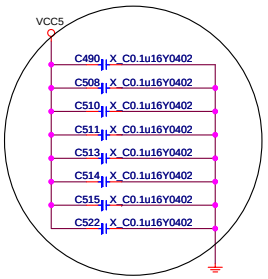
PCIE X16 PORT

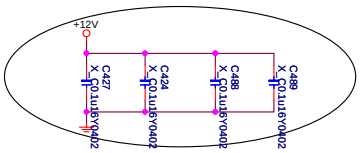


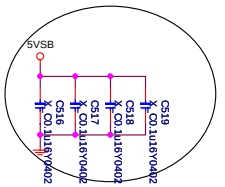
PCIE X1 PORT

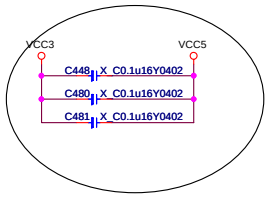


EMI

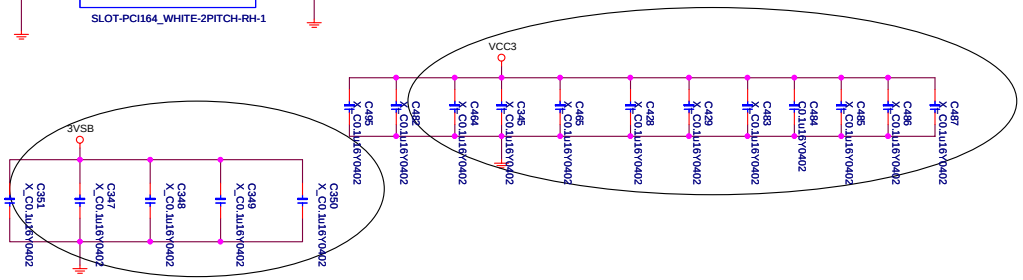


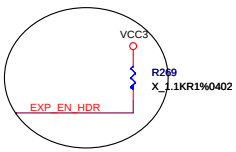


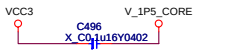




EMI

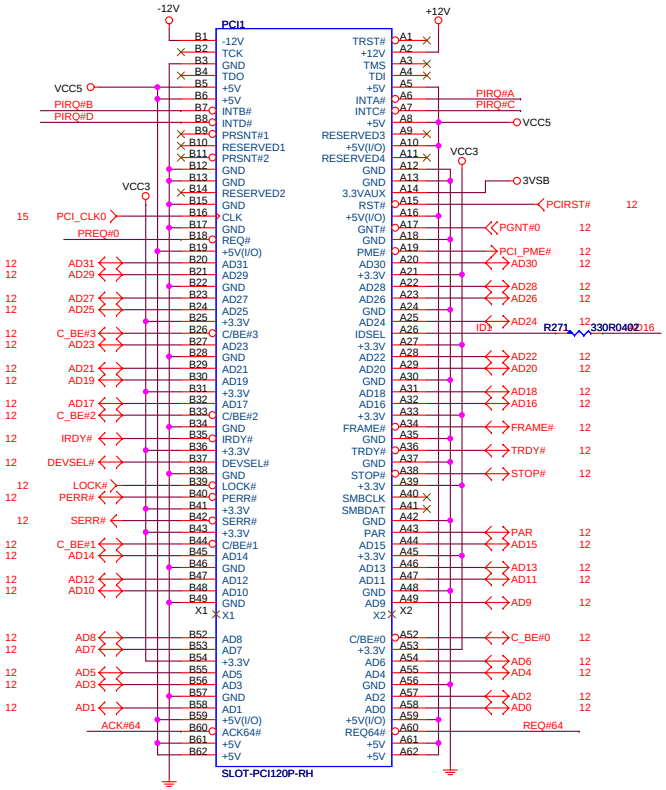






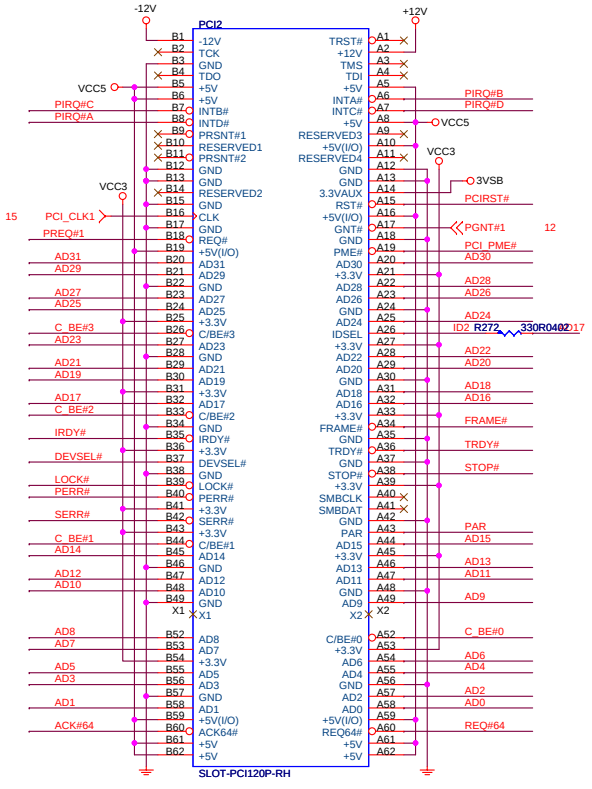
MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: PCI EXPRESSX16&X1	Rev: 0A
Date: Monday, September 10, 2007	Sheet 22 of 34	

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



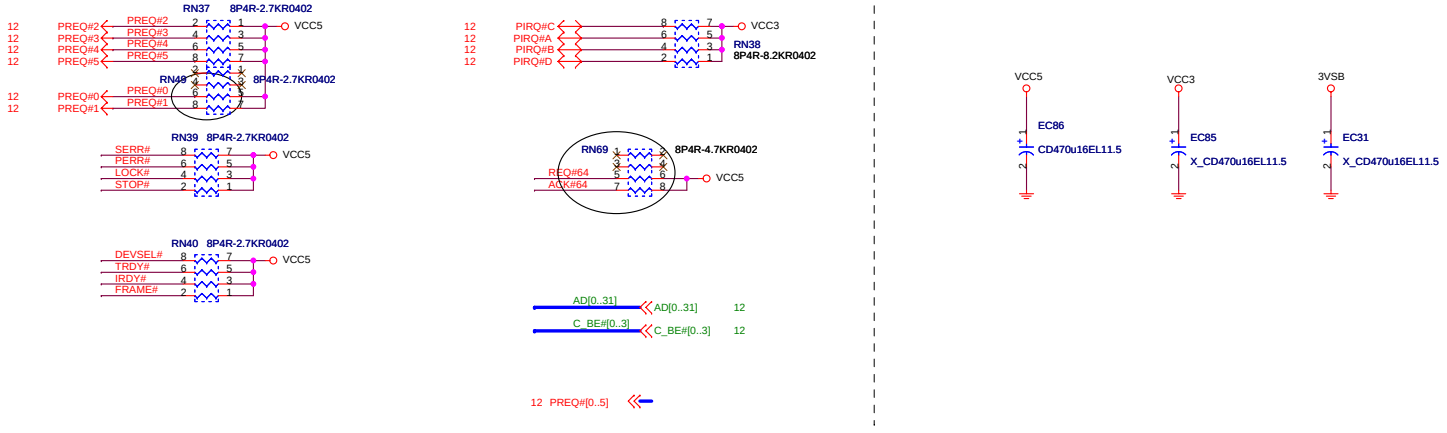
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

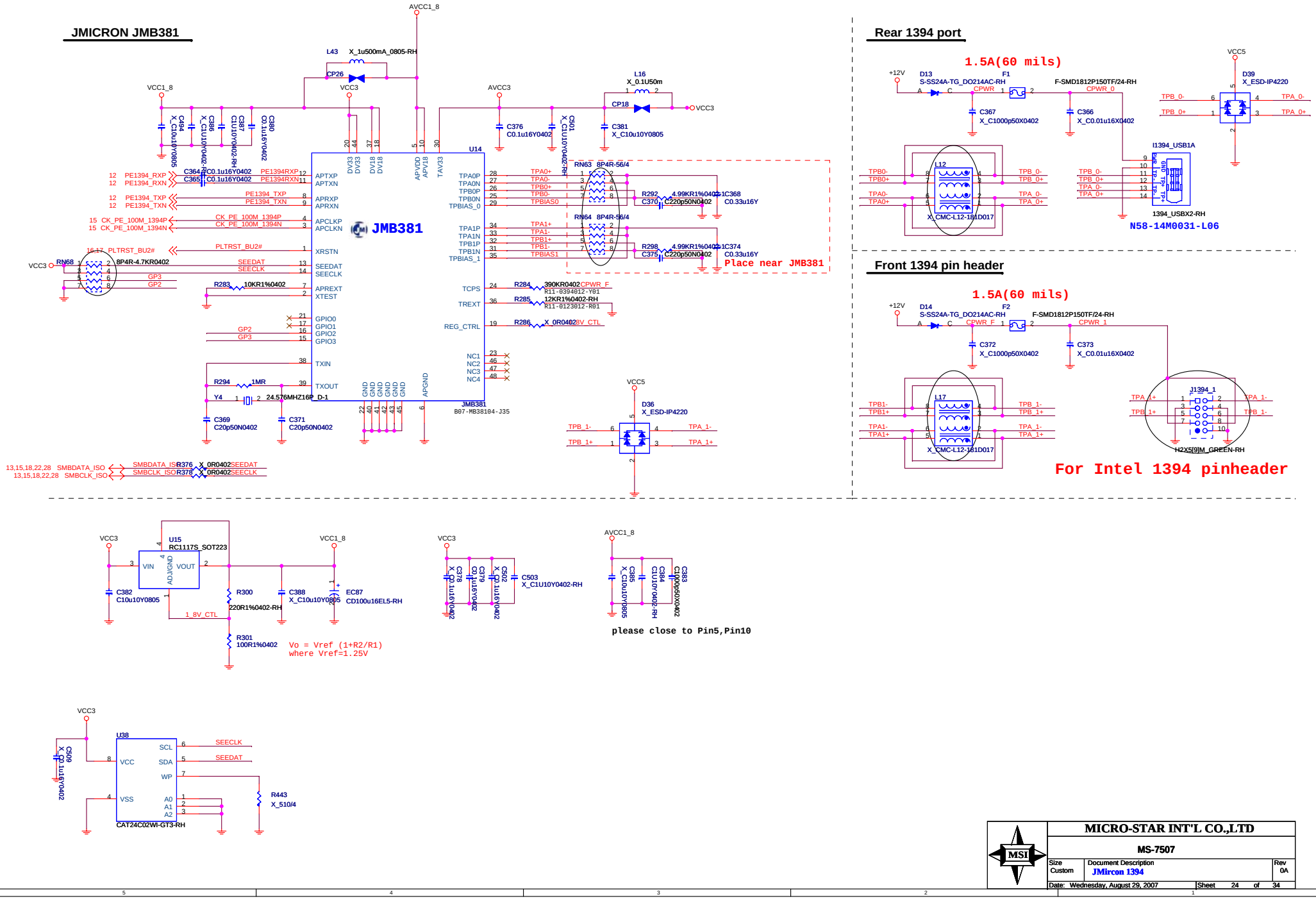


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

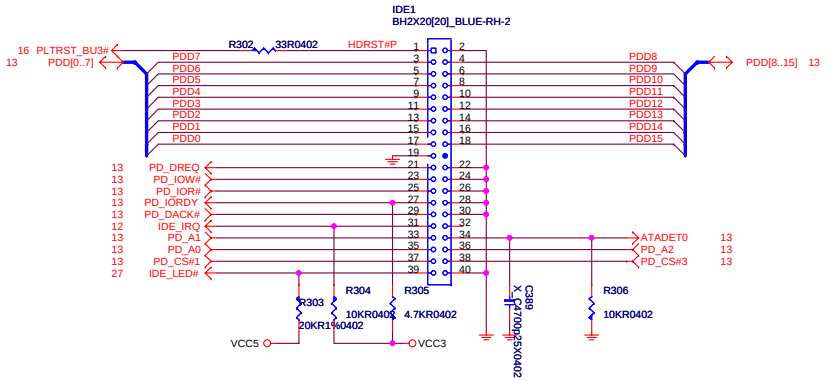
PCI PULL-UP / DOWN RESISTORS



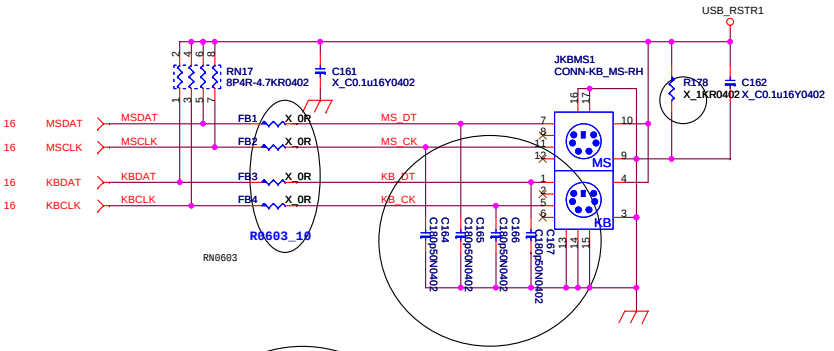
MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: PCI Slot 1 &2	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 23 of 34	

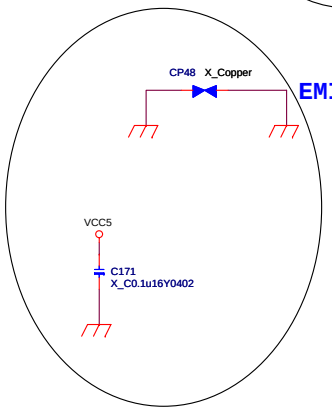

JMICRON JMB381
JMB381
Place near JMB381
Rear 1394 port
1.5A(60 mils)
N58-14M0031-L06
Front 1394 pin header
1.5A(60 mils)
For Intel 1394 pinheader
please close to Pin5,Pin10
Vo = Vref (1+R2/R1)
where Vref=1.25V
MICRO-STAR INT'L CO.,LTD
MS-7507
Document Description
JMircon 1394
Rev 0A
Date: Wednesday, August 29, 2007
Sheet 24 of 34

ATA 33/66/100 IDE Connectors

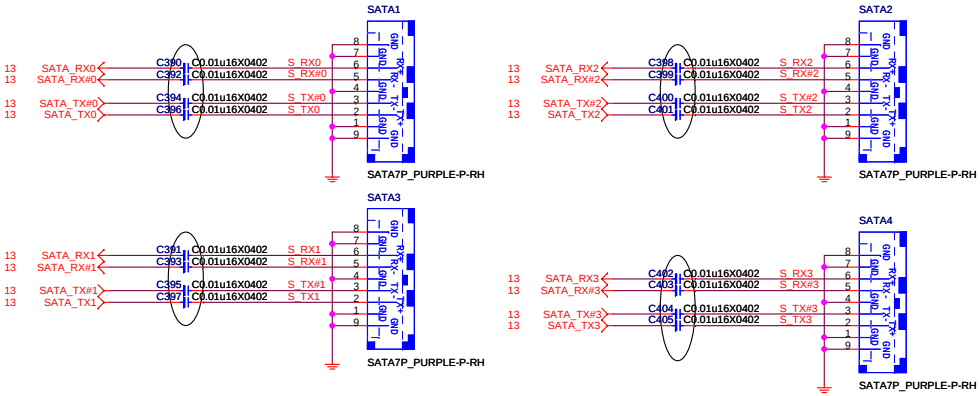


PS2 KEYBOARD & MOUSE CONNECTOR





SERIAL ATA CONNECTOR BLOCK



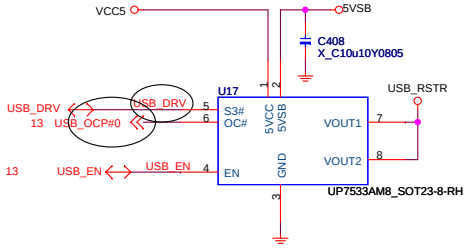
MICRO-STAR INT'L CO.,LTD

MS-7507

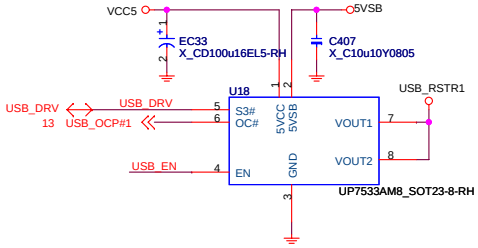
Size	Document Description	Rev
Custom	IDE & SATA Connectors	0A

Date: Monday, September 10, 2007 Sheet 25 of 34

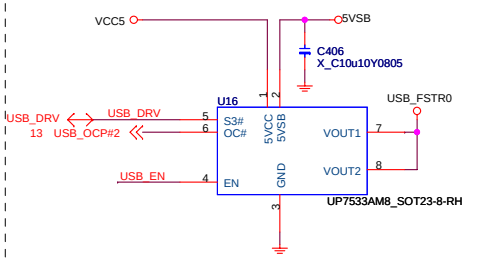
POWER CIRCUIT FOR USB PORT 0,1



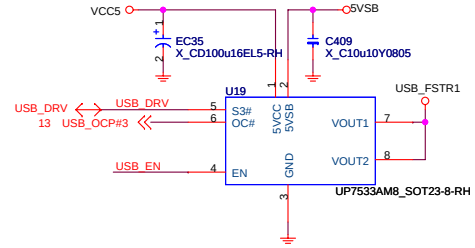
POWER CIRCUIT FOR USB PORT 2,3



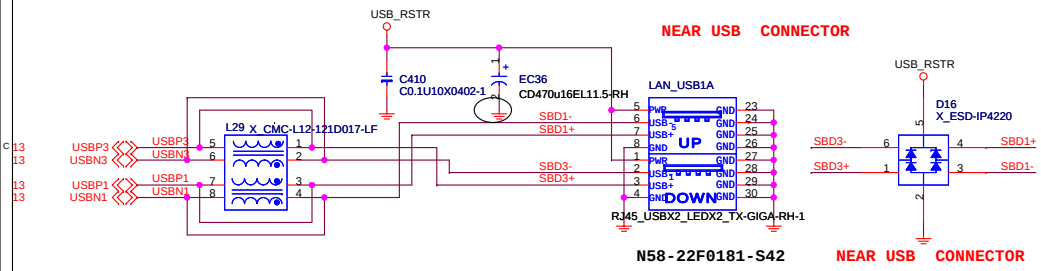
POWER CIRCUIT FOR USB PORT 4,5



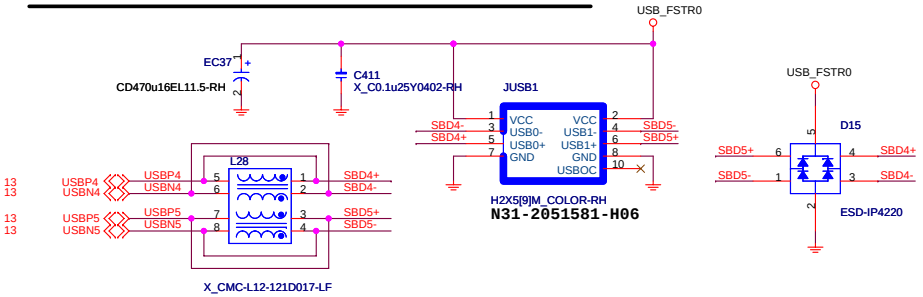
POWER CIRCUIT FOR USB PORT 6,7



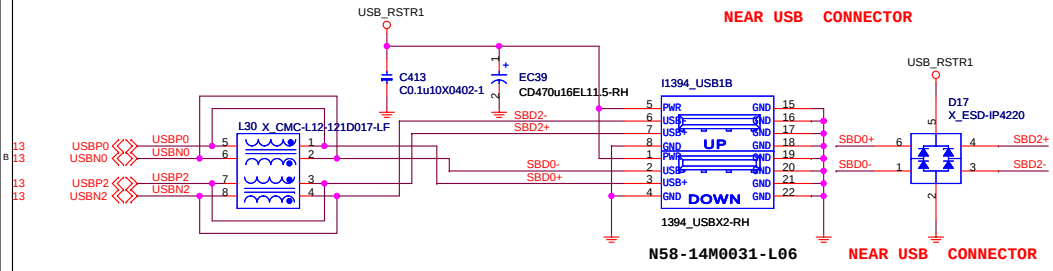
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



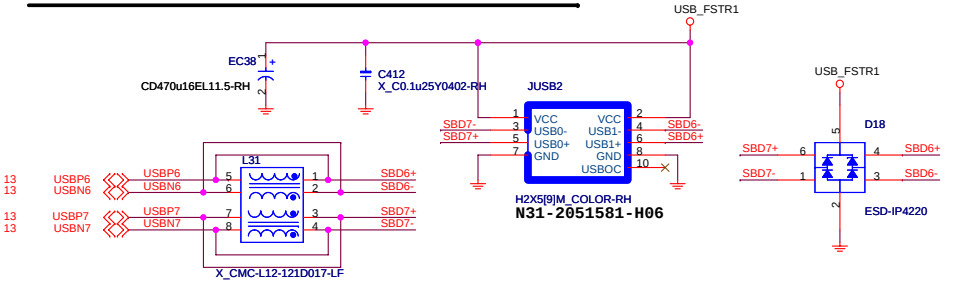
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

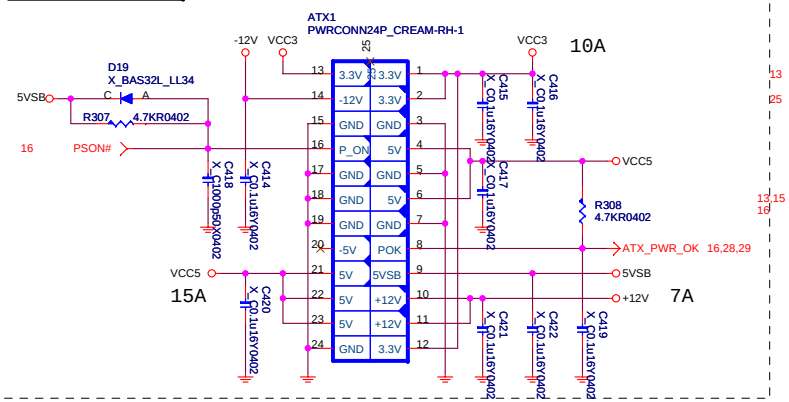


CP27

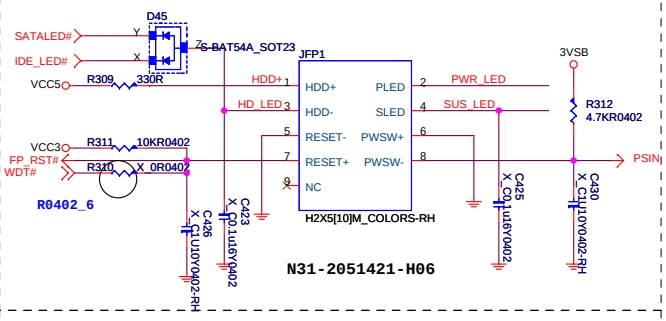
CP28

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7507	
Size: Custom	Document Description: USB CONNECTORS	Rev: 0A
Date: Monday, September 10, 2007	Sheet 26 of 34	

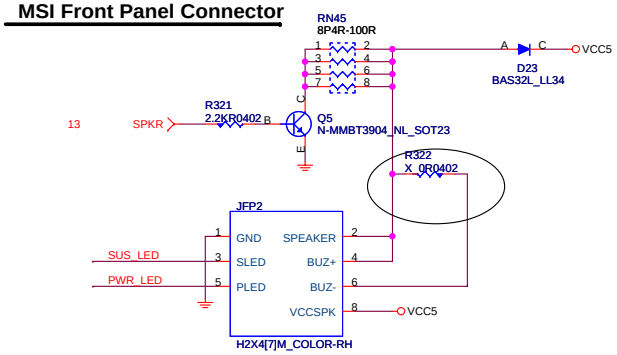
ATX Connector



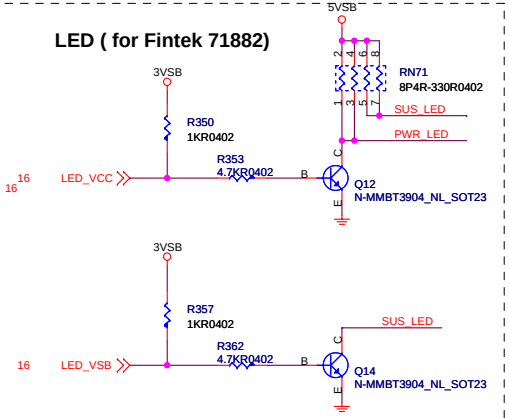
INTEL/PB Front Panel Connector



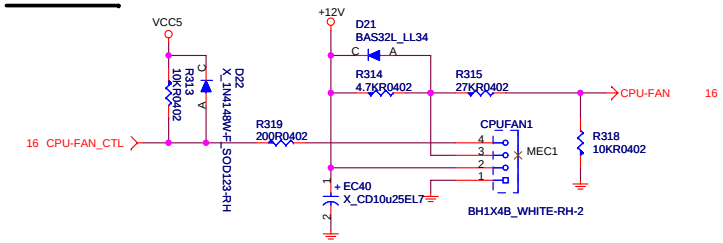
MSI Front Panel Connector



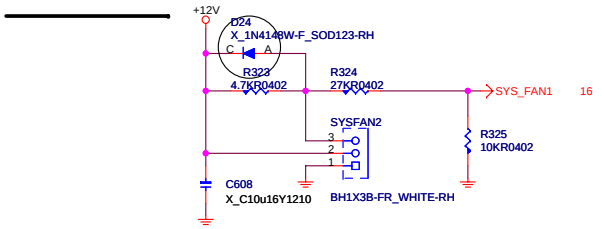
LED (for Fintek 71882)



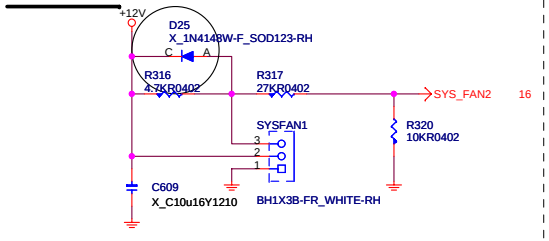
CPU FAN



SYSTEM FAN

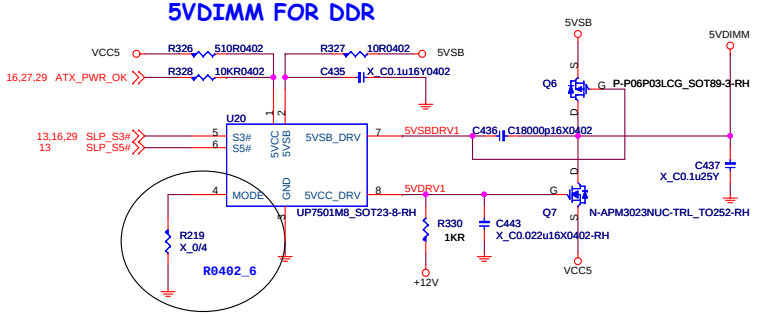


PWR FAN

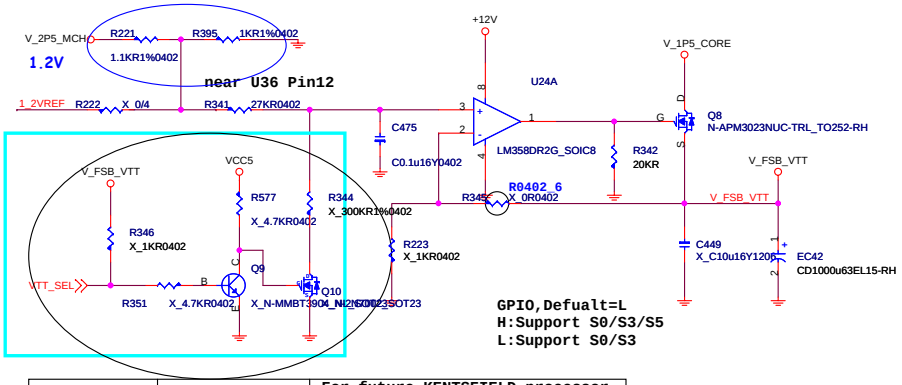


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7507	
Size: Custom	Document Description: ATX & Front Panel & FAN	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 27 of 34	

5VDIMM FOR DDR

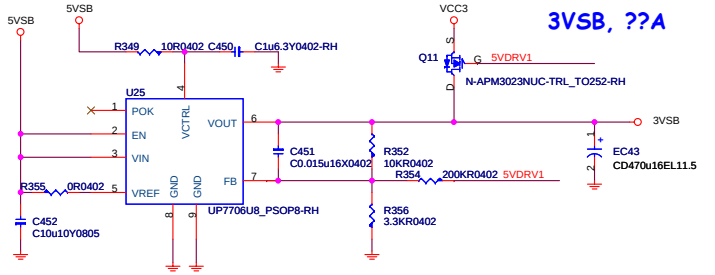


1.2V

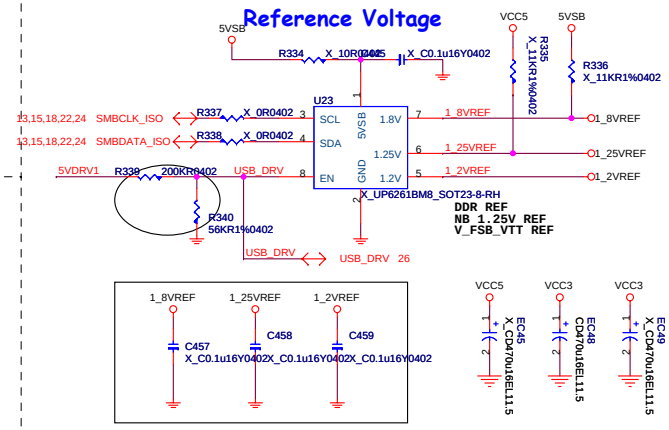


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

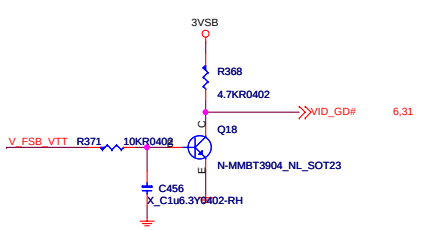
3VSB, ??A



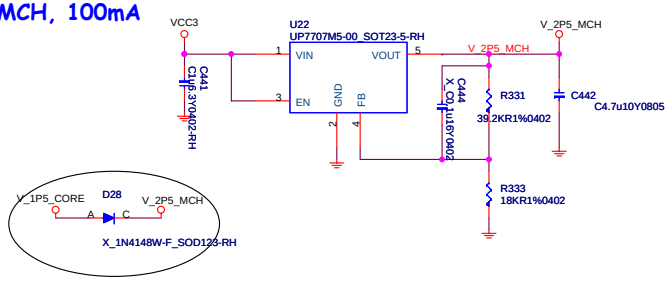
Reference Voltage



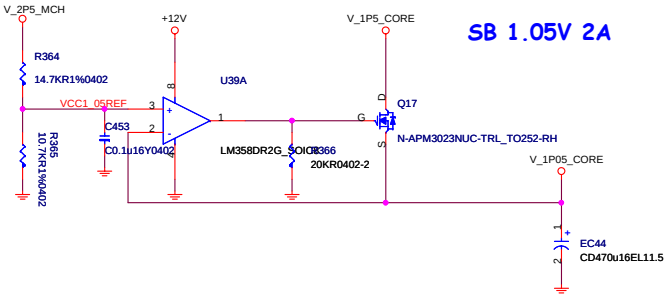
PLACE NEAR PIN OUT

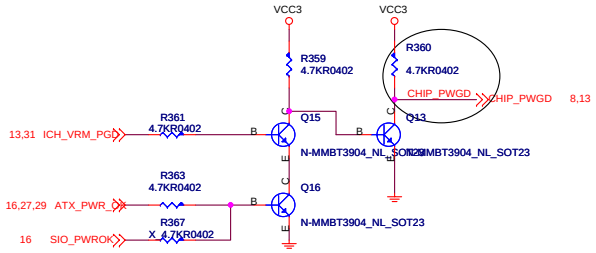


V_2P5_MCH, 100mA



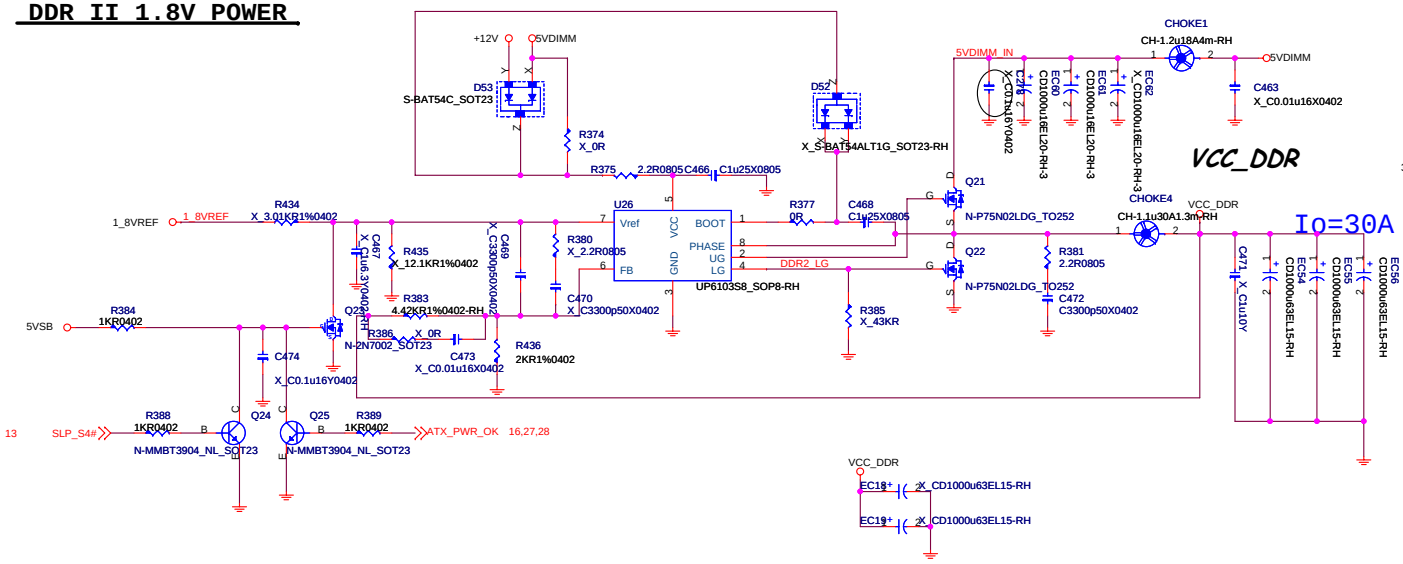
SB 1.05V 2A



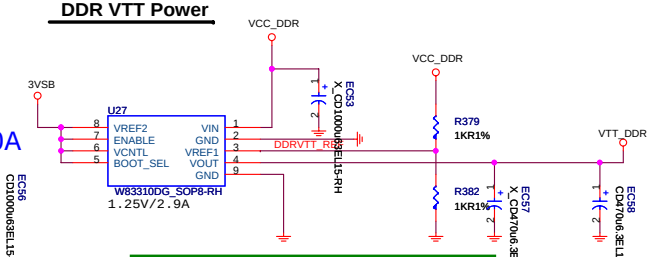


MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: ACPI controller UPI
Rev: 0A	
Date: Wednesday, August 29, 2007	Sheet 28 of 34

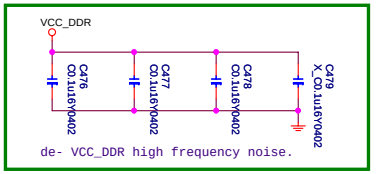
DDR II 1.8V POWER



DDR VTT Power



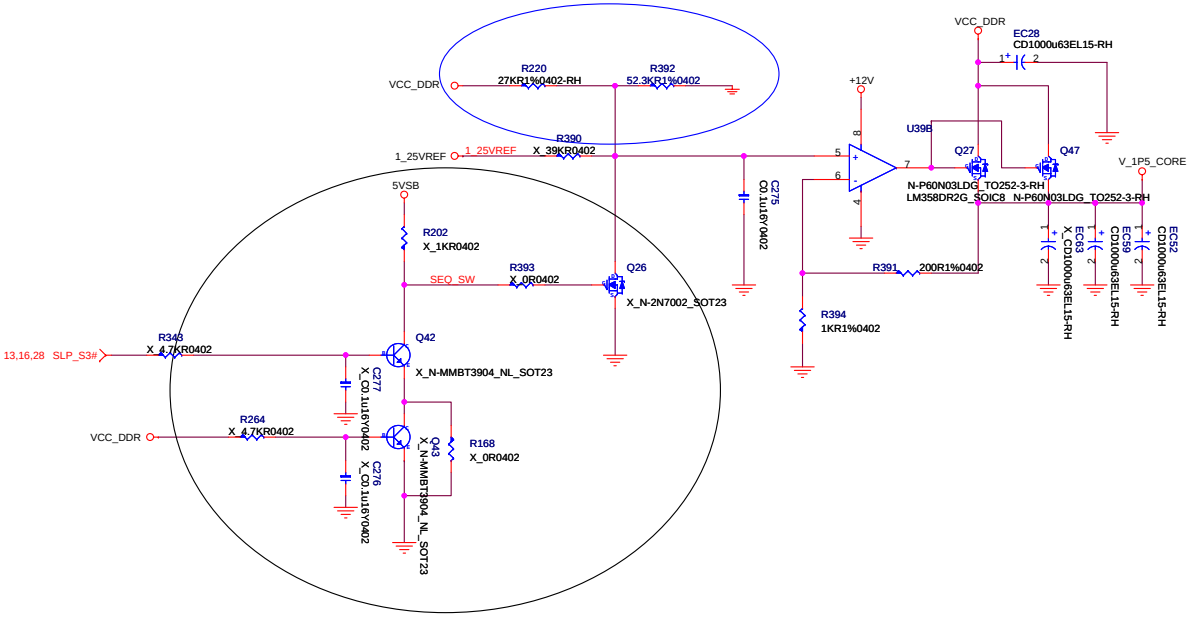
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



Do it need so many?

1.5V Core

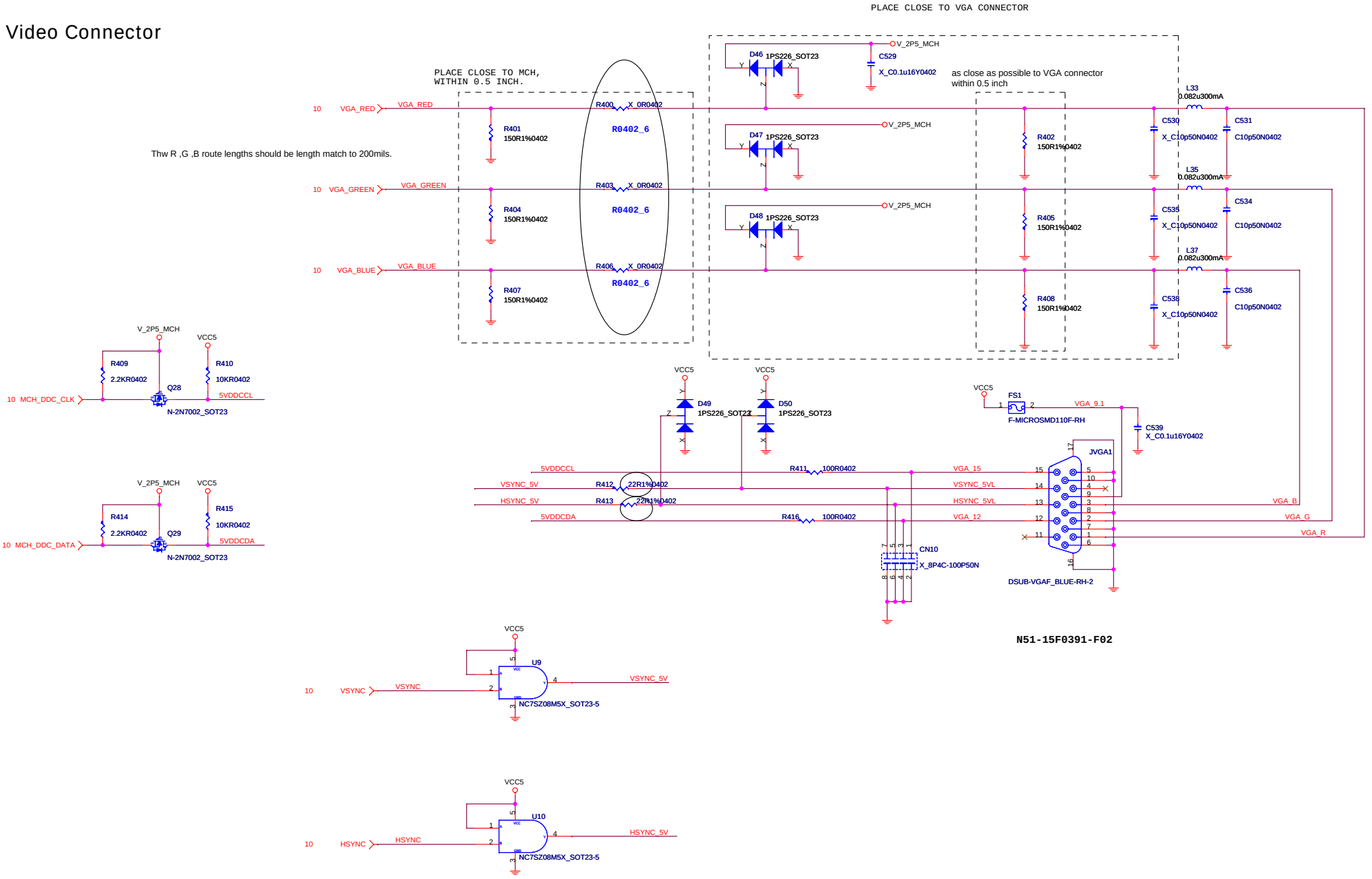
For cost down



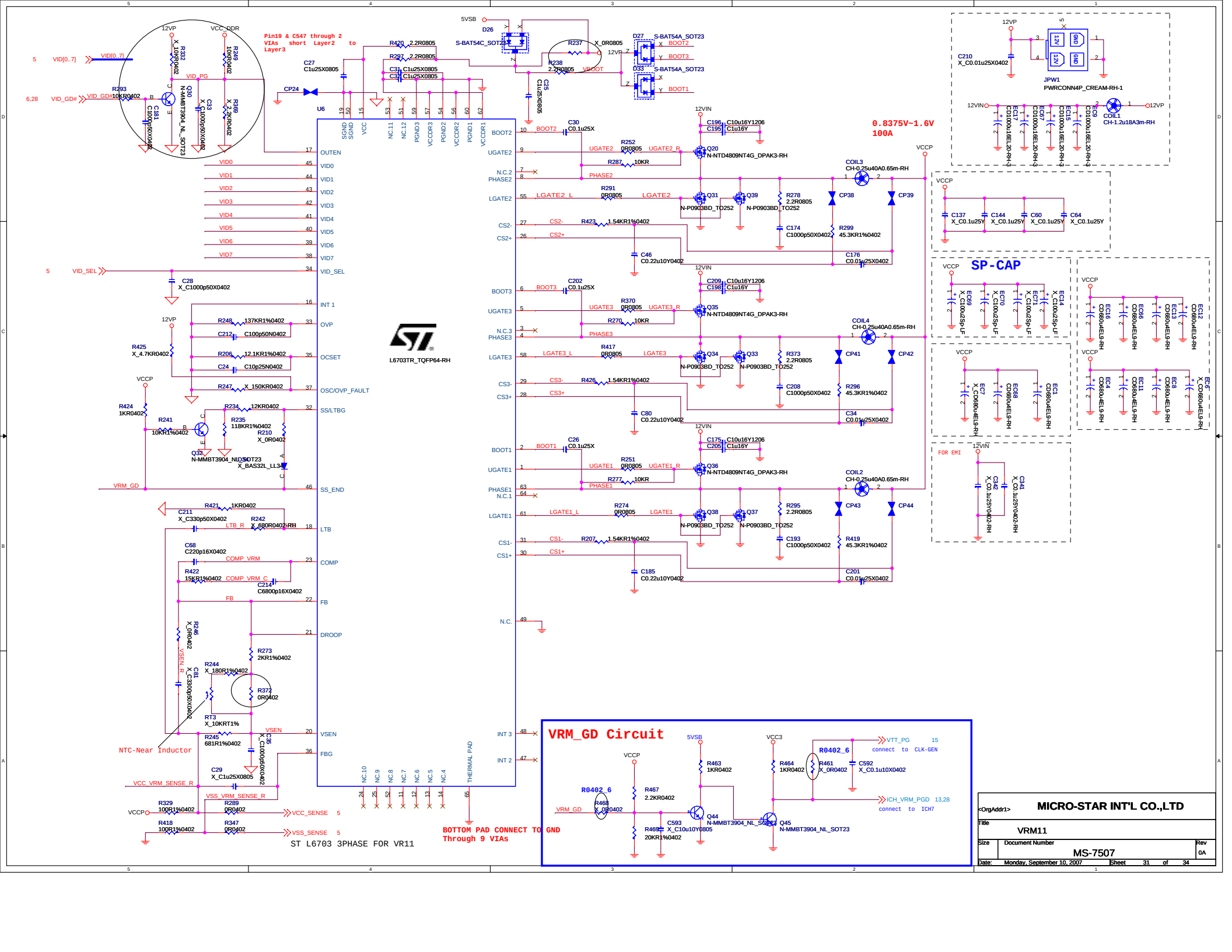
Io=22.8A

MICRO-STAR INT'L CO.,LTD	
MS-7507	
Size: Custom	Document Description: NB Core Power & DDR Power
Rev: 0A	
Date: Wednesday, August 29, 2007	Sheet 29 of 34

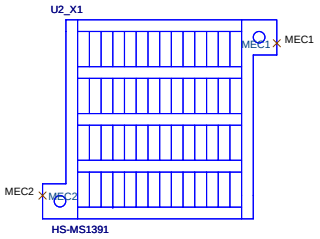
Video Connector



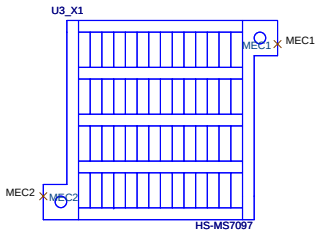
MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: VGA Connector	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 30 of 34	

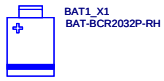

Pin19 & C547 through 2 VIAs short Layer2 to Layer3
L6703TR_TQFP64-RH
0.8375V~1.6V 100A
VRM_GD Circuit
NTC-Near Inductor
BOTTOM PAD CONNECT TO GND Through 9 VIAs
ST L6703 3PHASE FOR VR11
SP-CAP
FOR EMI
MICRO-STAR INT'L CO.,LTD
VRM11
MS-7507
Monday, September 10, 2007

ICH7 HEATSINK

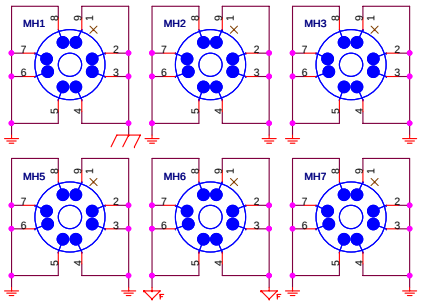


MCH HEATSINK

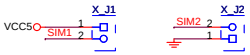




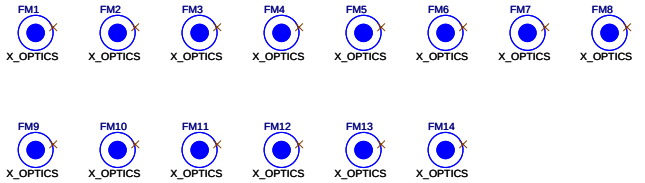
Mounting Holes



Simulation



Optics Orientation Holes



MICRO-STAR INT'L CO.,LTD		
MS-7507		
Size: Custom	Document Description: MANUAL PARTS	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 32 of 34	

1.link CIS library
2.change lan whole page circuit
3.move SPI rom and header connector to SB
4.modify SMB on CLKGEN
5.change R363 to 4.7K
6.add SIO_PWROK to circuit
7.SIO 57pin(SST) pull-low use 100K
8.add VCC3 sense on SIO
9.reserve Q19 for VTIN3
10.change com port,KBMS and parallel port ground(GND) to PGND
11.delete Mounting Holes pin4 and pin5 connecting
12.delete two Mounting Holes
13.Change two Mounting Holes ground(GNDF) to AGND
14.change SIO and Chassis intrusion power VBAT0 to VBAT
15.add beep function for SIO
16.Pull-high SIO 77pin to 3VSB
17.modify PSOUT# pull-high to 3VSB
18.reserve R223 for V_FSB_VTT FB
19.Change KB&MS 0ohm series resistor to L
20.delete OC# signal on JUSB1&2
21.reserve C30 for LAN connector
22.Delete DDR2 two DIMMs
23.delete PCI SLOT3
24.fang sir help to adjust 1394 and USB page
25.add PCIE X1 Connector
26.change VRM circuit
27.modify VCC5_SB to 5VSB in VRM page
28.add GND_USB,add coppers connect to GND_VGA and to GND
29.change audio whole page circuit
30.change AGND to GNDF
31.modify 1394 circuit using EMI solution
32.modify diode footprint for layout
33.change CPU footprint
34.add reserved D52,D54 for uPI power solution
35.delete CPU three Address traces
36.add some reserve pull-low resistors at CLKGEN page
37.modify frequence latch circuit
38.modify audio 6 of DIP caps to SMT cap
39.add GPI9 for throttle function
40.modify 1394 circuit
41.modify USB power circuit
42.modify frequence latch circuit
43.remove GPIO24 pull-low/pull-high
44.modify VGA circuit follow EMI solution
45.delete 2.5V control circuit
46.change 1.5V_Core ragulator
47.change front audio detect mode
48.Change ACPI circuit for cost down

Title: History		
Size: Custom	Document Number: MS-7507	Rev: 0A
Date: Wednesday, August 29, 2007	Sheet 33 of 34	

ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

Title	BIOS Request Form	
Size C	Document Number MS-7507	Rev 0A
Date: Wednesday, August 29, 2007	Sheet 34 of 34	