MS-7501 VER:0A

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882
LAN -- RTL8111C(B)/RTL8101E
HD Codec -- ALC888
BIOS -- SPI ROM 8M
1394 -- JMB381

Main Memory:

DDR II X 4 (Max 8GB)

Expansion Slots:

PCI-E X 16 *1
PCI-E X 1 *1

PCI 2.2 Slot X 2

Clock Generator:

Controller--ICS9LPRS477

PWM:

Controller -- ST6740L + UP6262 3+1 Phase

Title	Cover Sheet
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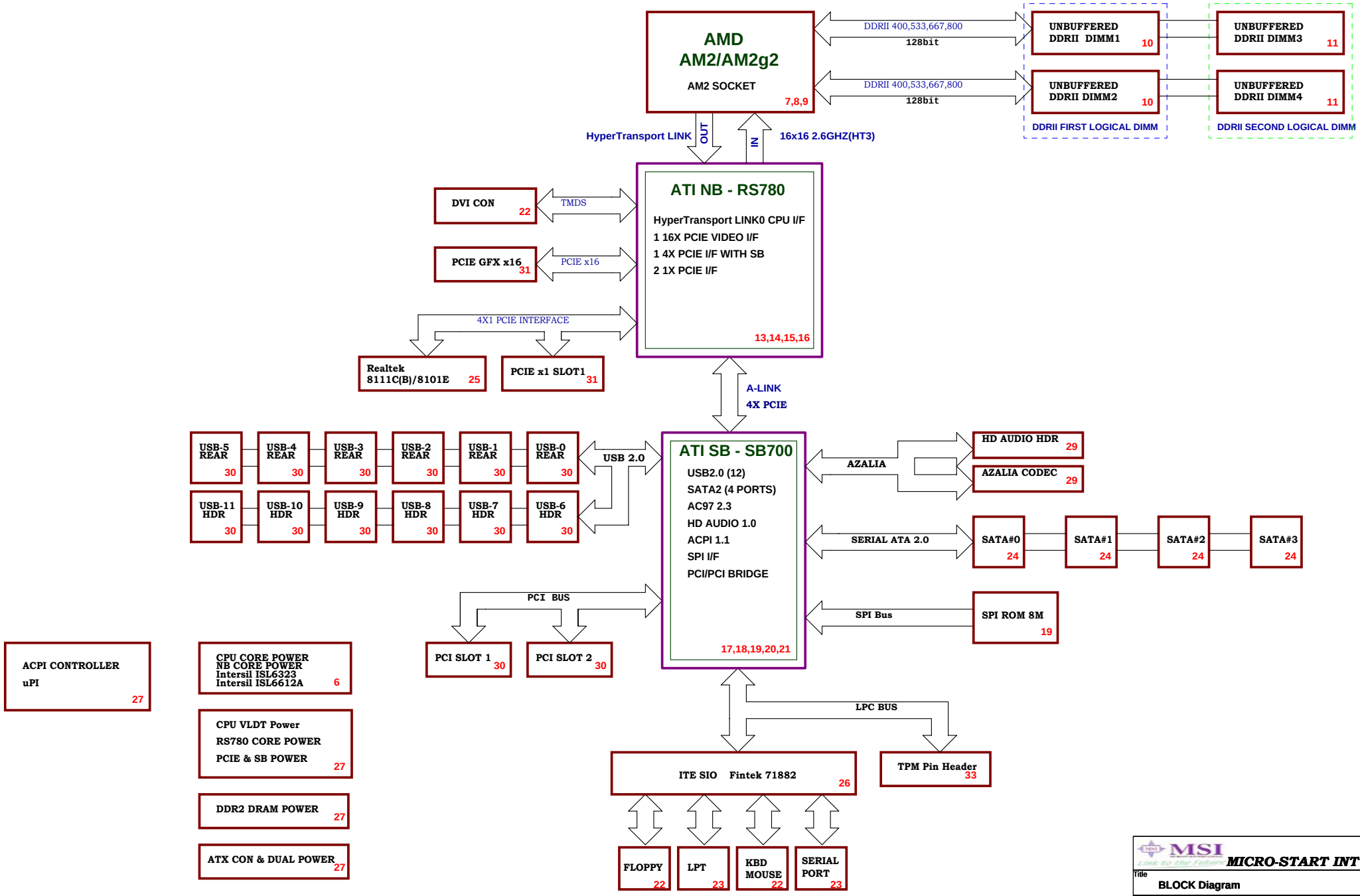
Project RS-780 BLOCK DIAGRAM



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Title: BLOCK Diagram		
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SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTEVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTEVNT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VID05/GP27		LEO_GPIO2	20	26
VID04/GP26		LEO_GPIO1	21	26
VID01/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SMI#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	PREQ#0 PGNT#0	AD16	PCICLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	PREQ#1 PGNT#1	AD17	PCICLK1

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Title: GPIO Configuration

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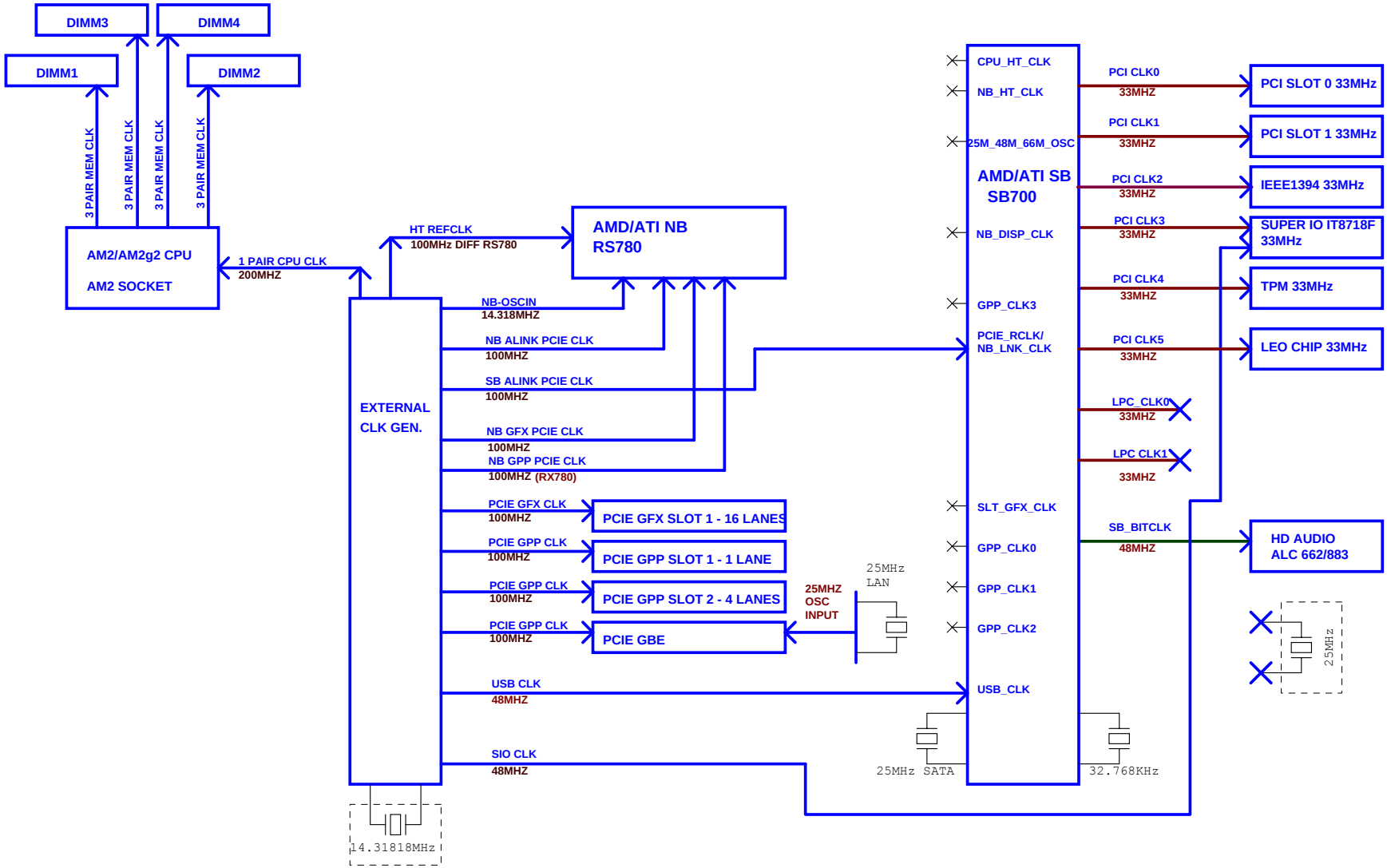

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Title: Clock Distribution		
Size: Custom	Document Number: MS-7501	Rev: 0A
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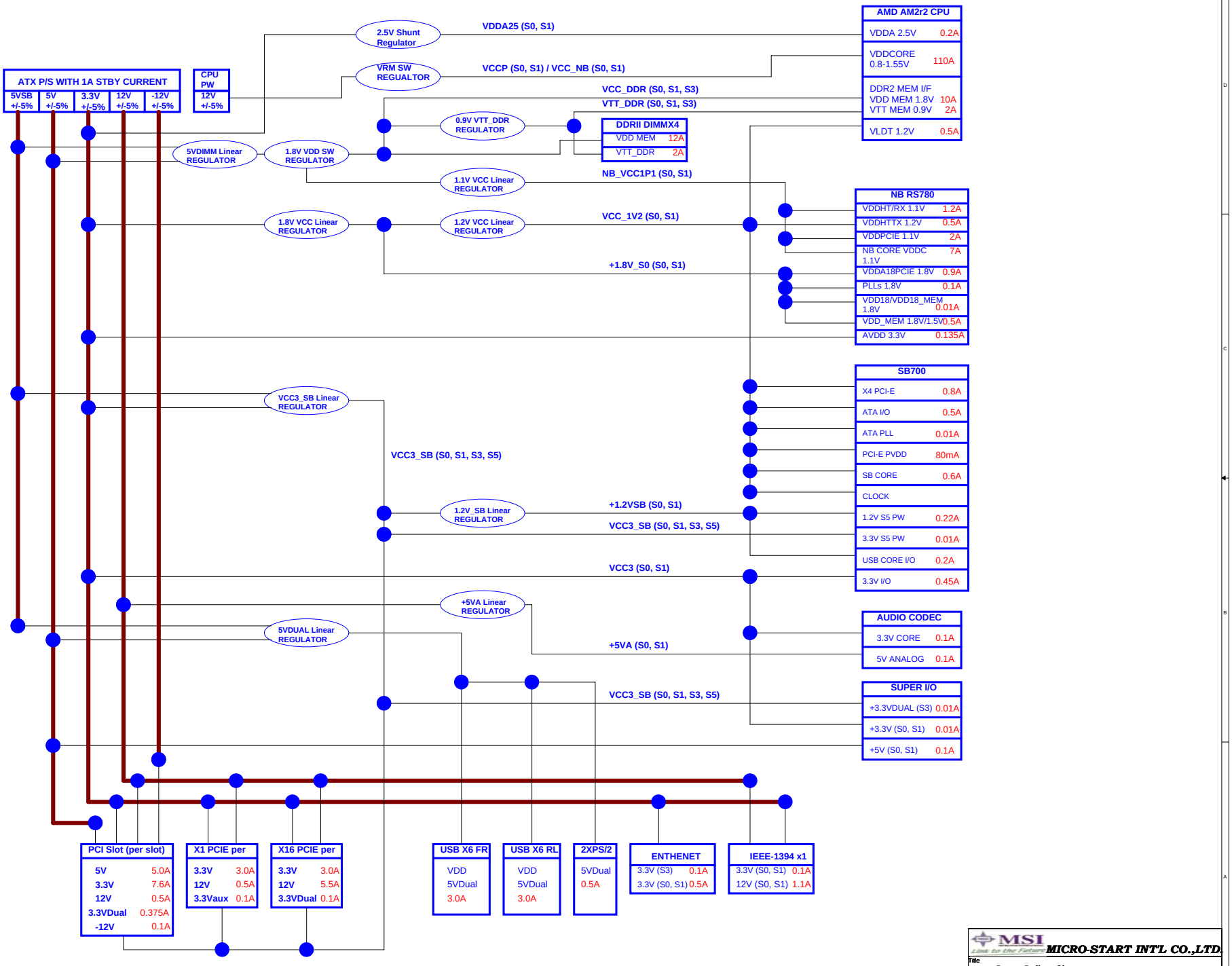
Power Deliver Chart



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Title: Power Deliver Chart		
Size: C	Document Number: MS-7501	Rev: 0A
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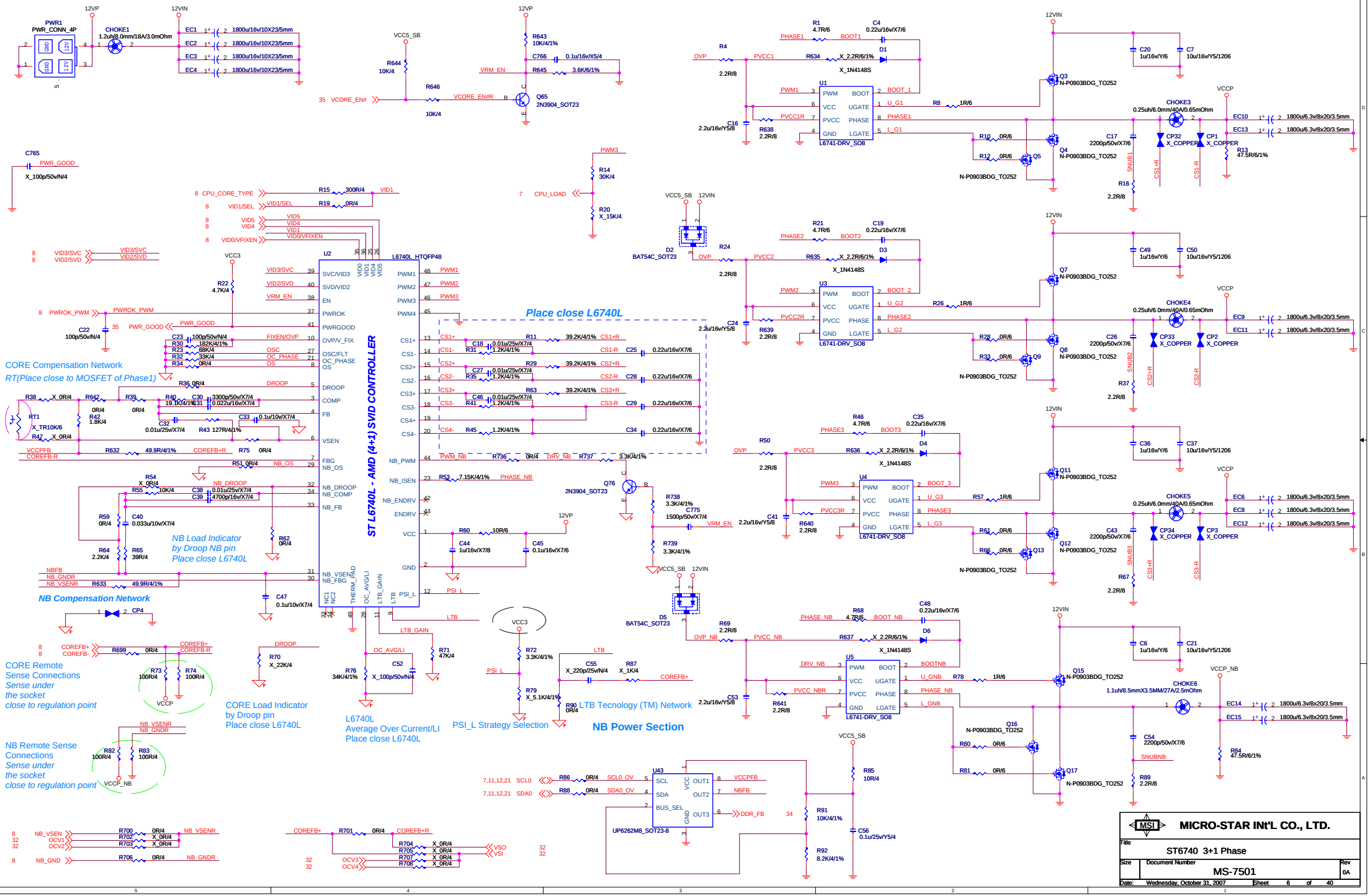
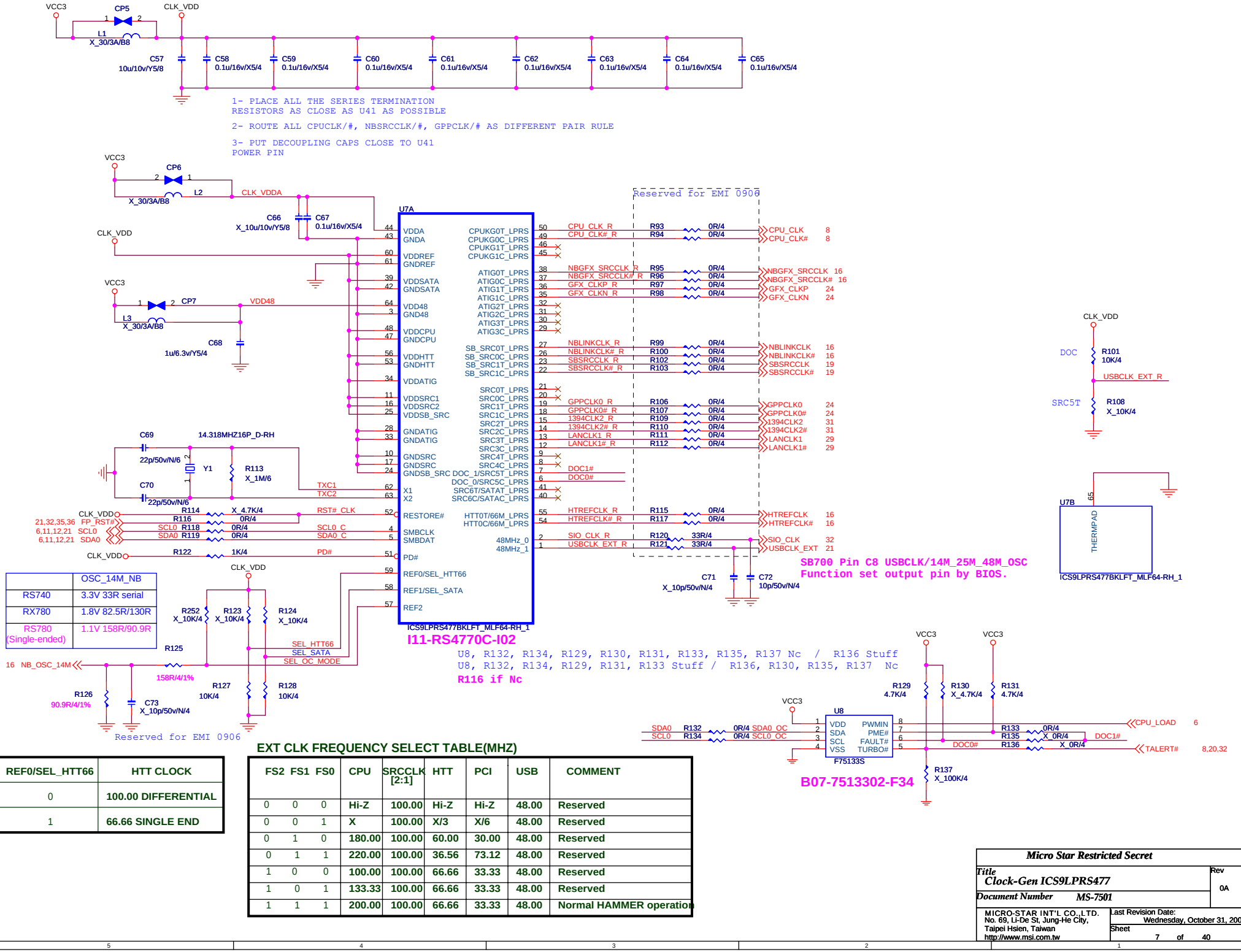

ST L6740L - AMD (4+1) SVID CONTROLLER
L6740L_HTQFP48
Place close L6740L
CORE Compensation Network
RT(Place close to MOSFET of Phase1)
NB Load Indicator
by Droop NB pin
Place close L6740L
NB Compensation Network
CORE Remote
Sense Connections
Sense under
the socket
close to regulation point
NB Remote Sense
Connections
Sense under
the socket
close to regulation point
CORE Load Indicator
by Droop pin
Place close L6740L
L6740L
Average Over Current/LI
Place close L6740L
PSI_L Strategy Selection
LTB Tecnology (TM) Network
NB Power Section
L6741-DRV_SO8
UP6262M8_SOT23-8
MICRO-STAR INt'L CO., LTD.
ST6740 3+1 Phase
MS-7501
Wednesday, October 31, 2007



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Title: Clock-Gen ICS9LPRS477

Rev: 0A

Document Number: MS-7501

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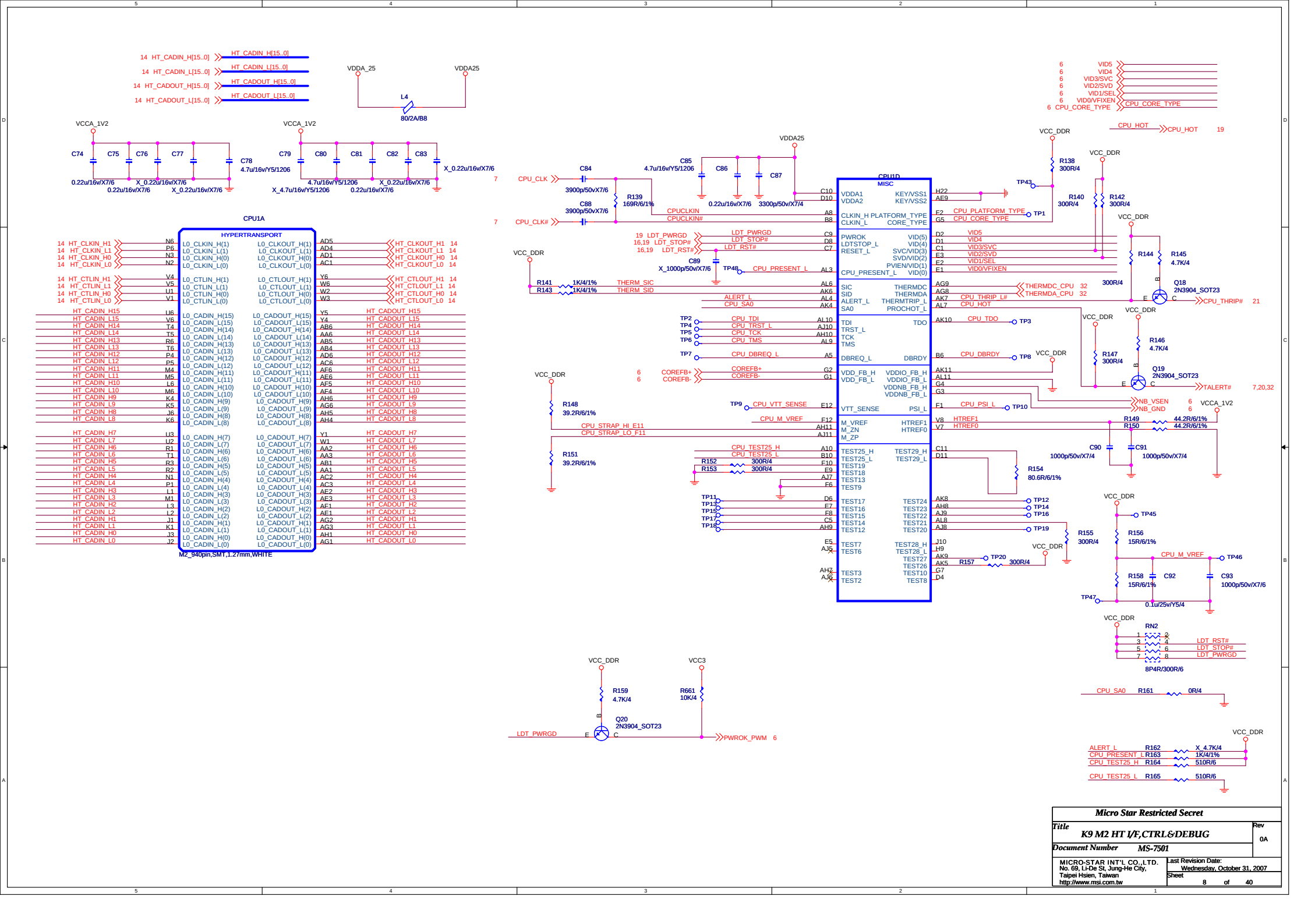

Micro Star Restricted Secret	
Title: K9 M2 HT I/F,CTRL&DEBUG	Rev: 0A
Document Number: MS-7501	
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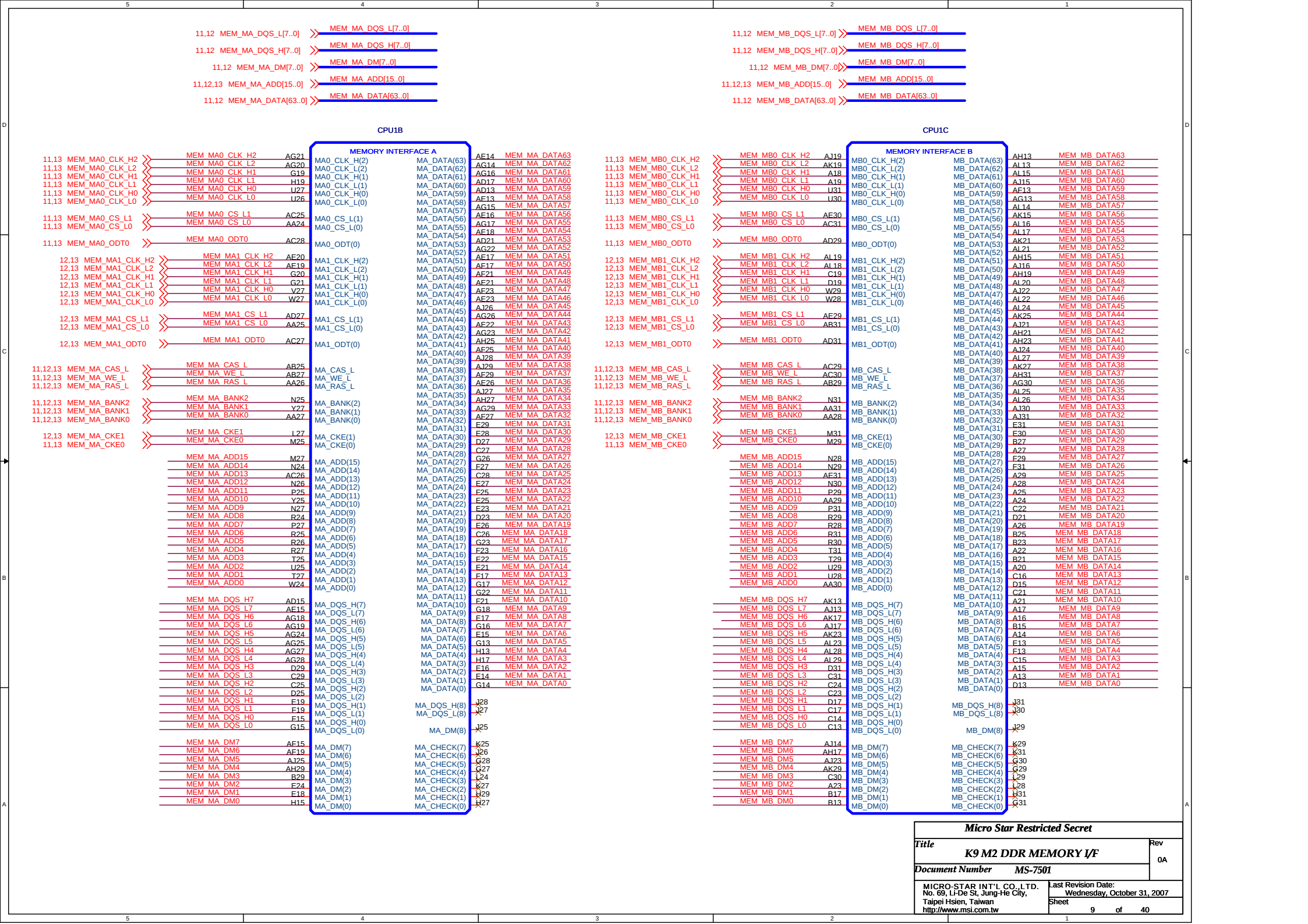
11,12 MEM_MA_DQS_L[7..0] MEM_MA_DQS_L[7..0]
11,12 MEM_MA_DQS_H[7..0] MEM_MA_DQS_H[7..0]
11,12 MEM_MA_DM[7..0] MEM_MA_DM[7..0]
11,12,13 MEM_MA_ADD[15..0] MEM_MA_ADD[15..0]
11,12 MEM_MA_DATA[63..0] MEM_MA_DATA[63..0]
11,12 MEM_MB_DQS_L[7..0] MEM_MB_DQS_L[7..0]
11,12 MEM_MB_DQS_H[7..0] MEM_MB_DQS_H[7..0]
11,12 MEM_MB_DM[7..0] MEM_MB_DM[7..0]
11,12,13 MEM_MB_ADD[15..0] MEM_MB_ADD[15..0]
11,12 MEM_MB_DATA[63..0] MEM_MB_DATA[63..0]
CPU1B
MEMORY INTERFACE A
CPU1C
MEMORY INTERFACE B
Micro Star Restricted Secret
Title
K9 M2 DDR MEMORY I/F
Rev
0A
Document Number
MS-7501
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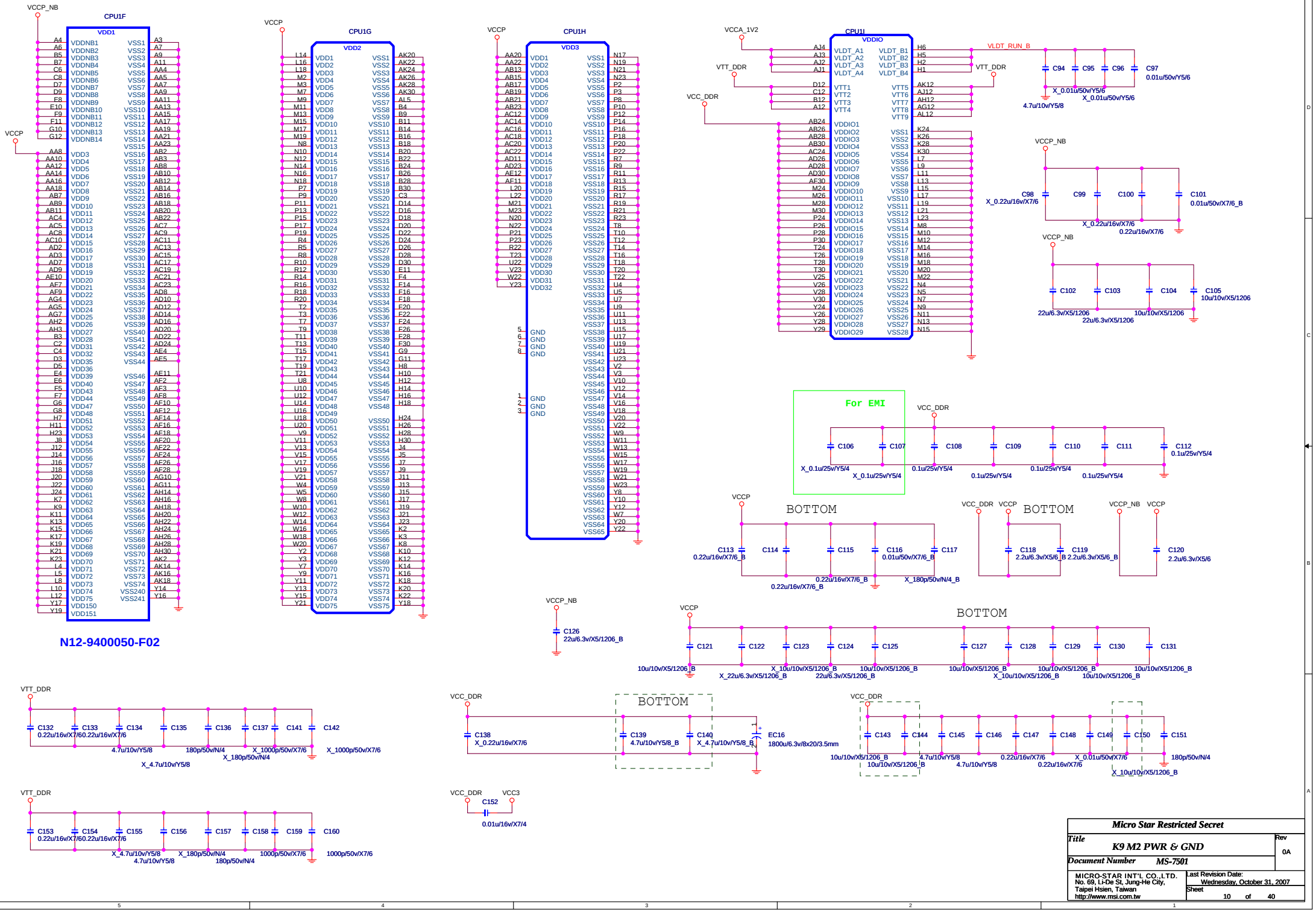
CPU1F
VDD1
VCCP_NB
VCCP
N12-9400050-F02
CPU1G
VDD2
CPU1H
VDD3
CPU1I
VDDIO
VCCA_1V2
VTT_DDR
VCC_DDR
VLDT_RUN_B
For EMI
BOTTOM
VCC3
Micro Star Restricted Secret
Title
K9 M2 PWR & GND
Rev
0A
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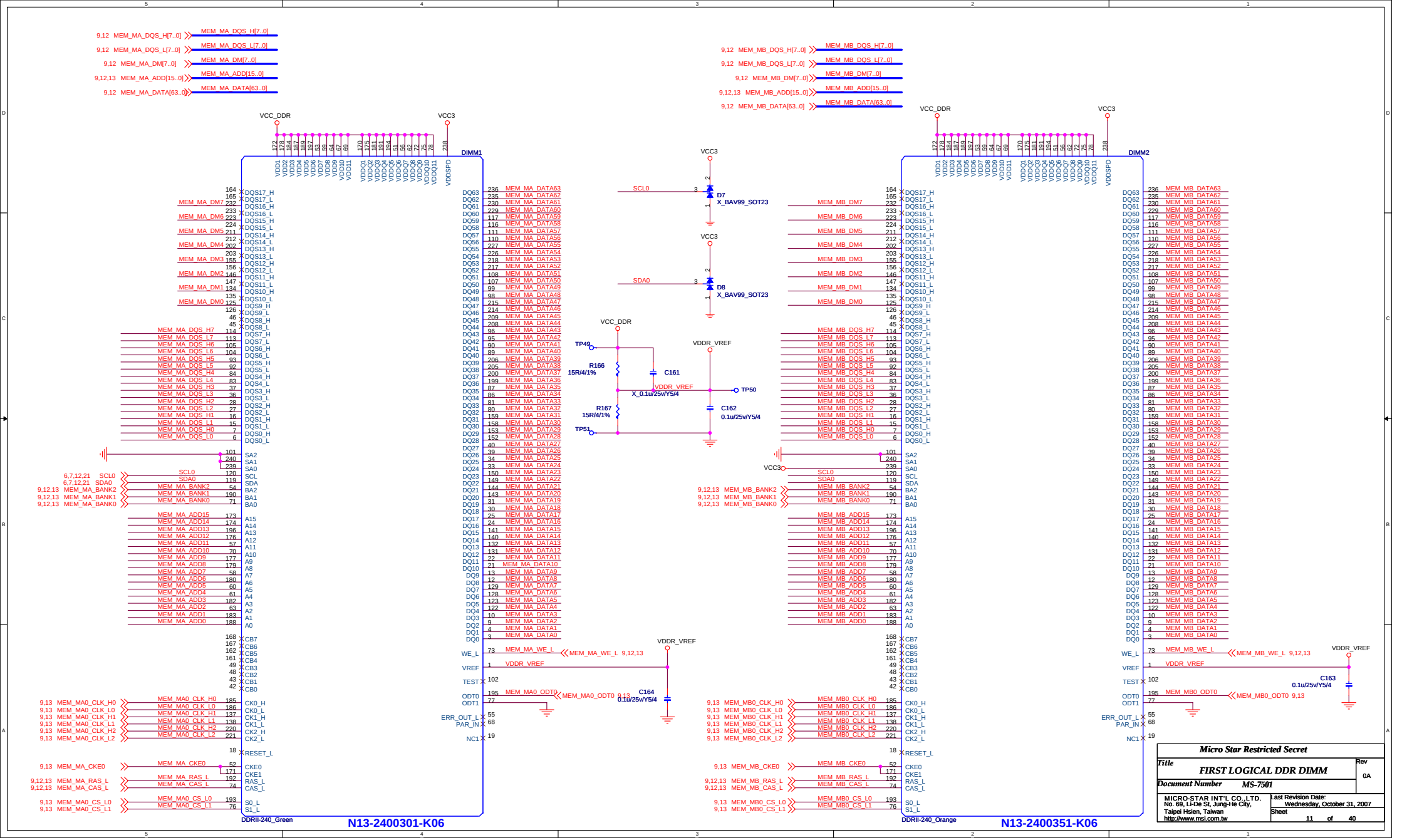
MEM_MA_DQS_H[7..0]
MEM_MA_DQS_L[7..0]
MEM_MA_DM[7..0]
MEM_MA_ADD[15..0]
MEM_MA_DATA[63..0]
MEM_MB_DQS_H[7..0]
MEM_MB_DQS_L[7..0]
MEM_MB_DM[7..0]
MEM_MB_ADD[15..0]
MEM_MB_DATA[63..0]
VCC_DDR
VCC3
VDDR_VREF
DIMM1
DIMM2
D7
X_BAV99_SOT23
D8
X_BAV99_SOT23
R166
15R/4/1%
R167
15R/4/1%
C161
X_0.1u/25v/Y5/4
C162
0.1u/25v/Y5/4
C163
0.1u/25v/Y5/4
C164
0.1u/25v/Y5/4
TP49
TP50
TP51
DDRII-240_Green
DDRII-240_Orange
N13-2400301-K06
N13-2400351-K06
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Title
FIRST LOGICAL DDR DIMM
Rev
0A
Document Number
MS-7501
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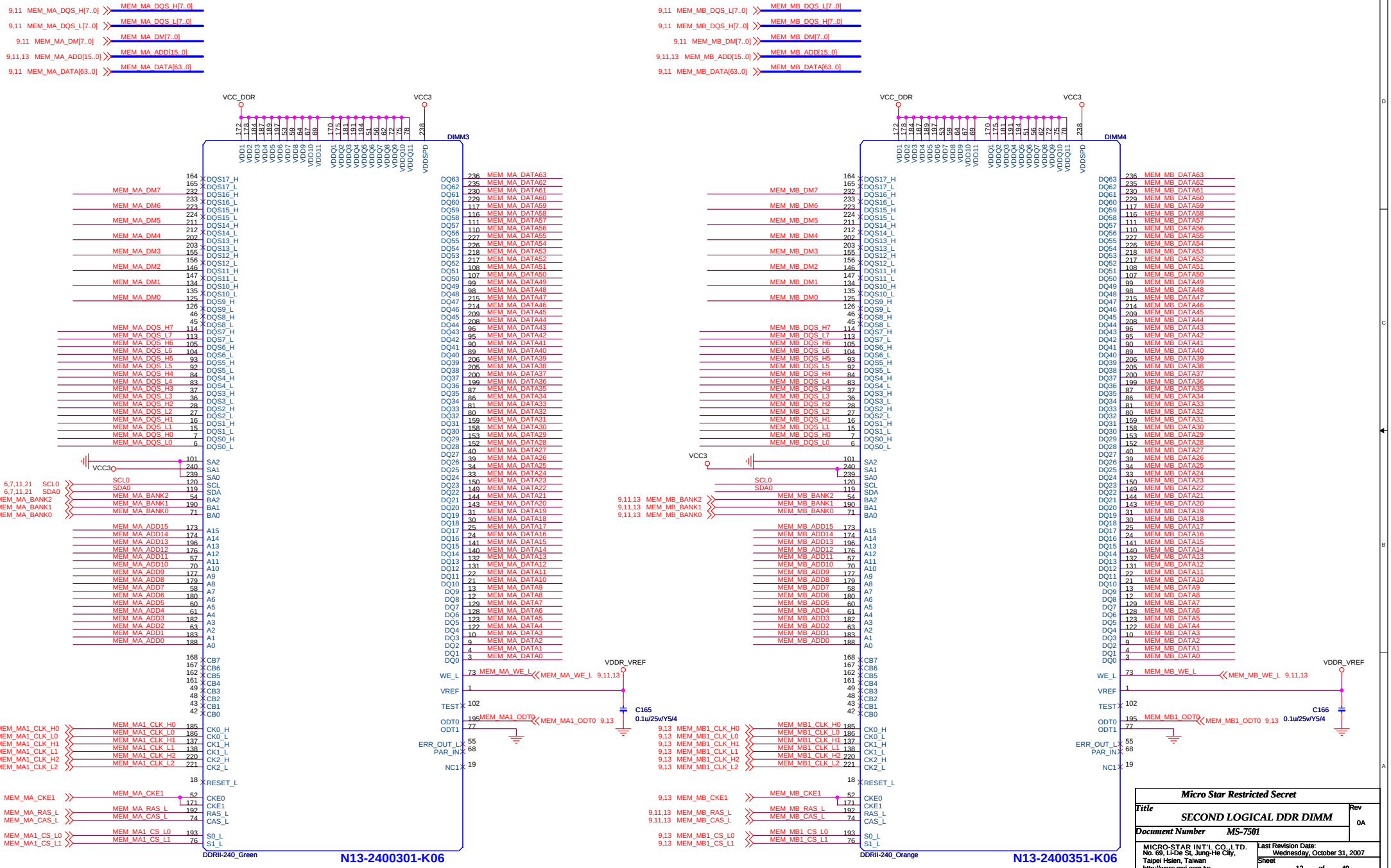

Micro Star Restricted Secret

Title	SECOND LOGICAL DDR DIMM
Rev	0A
Document Number	MS-7501

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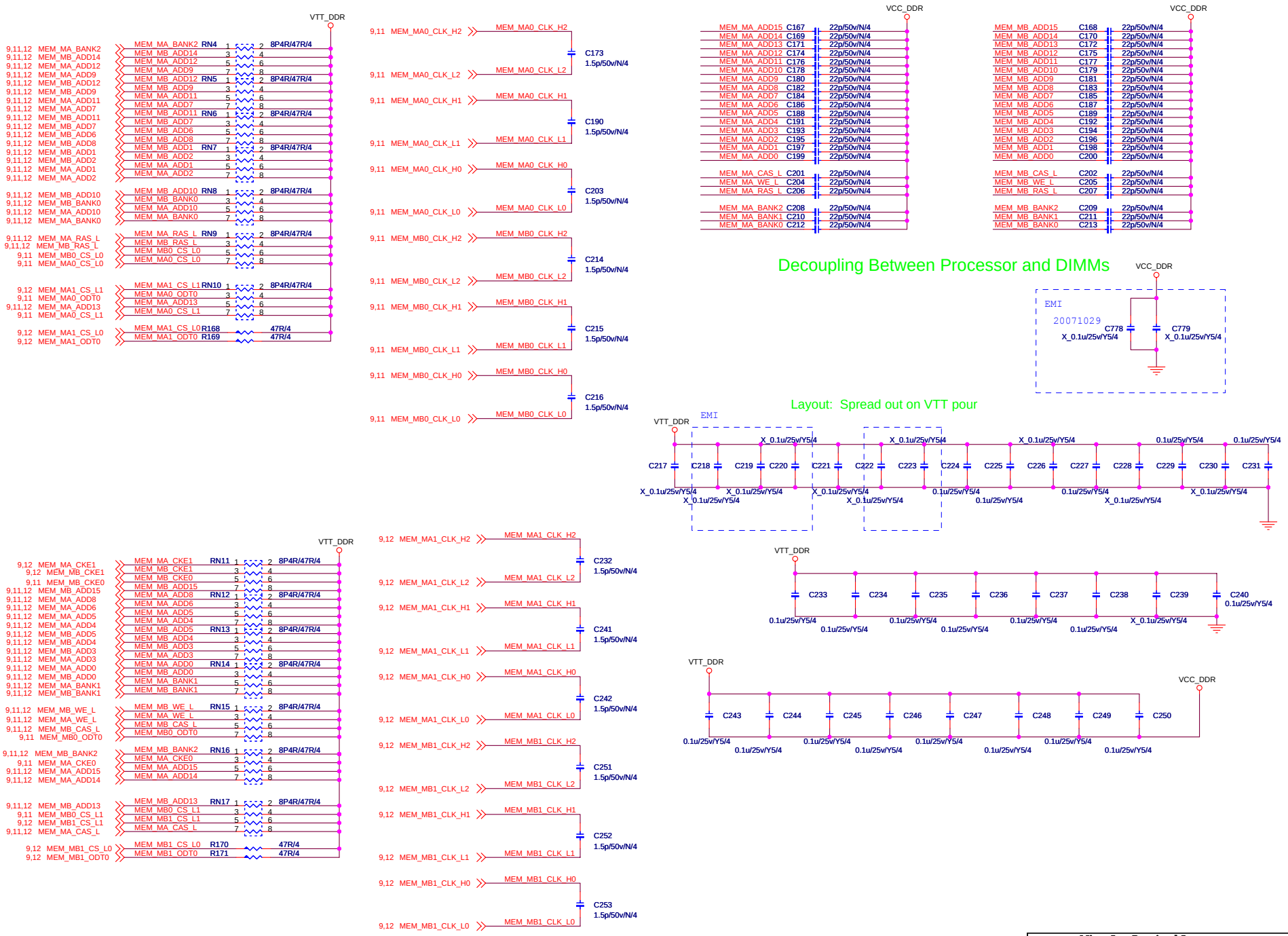

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Document Number	*MS-7501*	
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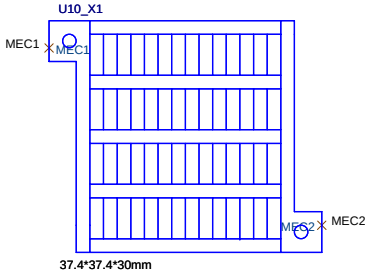
NB HEAT-SINK



7383
E31-0401580-K08
E31-0401580-E25

8 HT_CADOUT_H[15..0] HT_CADOUT_H[15..0]
8 HT_CADOUT_L[15..0] HT_CADOUT_L[15..0]

8 HT_CADIN_H[15..0] HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] HT_CADIN_L[15..0]

20 / 5 / 5 / 5 / 20

20 / 5 / 5 / 5 / 20

U10A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CADOUT_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_CADIN_H0
HT_CADOUT_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_CADIN_L0
HT_CADOUT_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_CADIN_H1
HT_CADOUT_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_CADIN_L1
HT_CADOUT_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_CADIN_H2
HT_CADOUT_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_CADIN_L2
HT_CADOUT_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_CADIN_H3
HT_CADOUT_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_CADIN_L3
HT_CADOUT_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_CADIN_H4
HT_CADOUT_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_CADIN_L4
HT_CADOUT_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_CADIN_H5
HT_CADOUT_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_CADIN_L5
HT_CADOUT_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_CADIN_H6
HT_CADOUT_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_CADIN_L6
HT_CADOUT_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_CADIN_H7
HT_CADOUT_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_CADIN_L7
HT_CADOUT_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_CADIN_H8
HT_CADOUT_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_CADIN_L8
HT_CADOUT_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_CADIN_H9
HT_CADOUT_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_CADIN_L9
HT_CADOUT_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_CADIN_H10
HT_CADOUT_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_CADIN_L10
HT_CADOUT_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_CADIN_H11
HT_CADOUT_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_CADIN_L11
HT_CADOUT_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_CADIN_H12
HT_CADOUT_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_CADIN_L12
HT_CADOUT_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_CADIN_H13
HT_CADOUT_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_CADIN_L13
HT_CADOUT_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_CADIN_H14
HT_CADOUT_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_CADIN_L14
HT_CADOUT_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_CADIN_H15
HT_CADOUT_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_CADIN_L15
8 HT_CLKOUT_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_CLKIN_H0 8
8 HT_CLKOUT_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_CLKIN_L0 8
8 HT_CLKOUT_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_CLKIN_H1 8
8 HT_CLKOUT_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_CLKIN_L1 8
8 HT_CTLOUT_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_CTLIN_H0 8
8 HT_CTLOUT_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_CTLIN_L0 8
8 HT_CTLOUT_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_CTLIN_H1 8
8 HT_CTLOUT_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_CTLIN_L1 8
301R/4/1% R172 HT_RXCALP	C23	HT_RXCALP	HT_TXCALP	B24	HT_TXCALP 301R/4/1% R173
HT_RXCALN	A24	HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

5 / 10

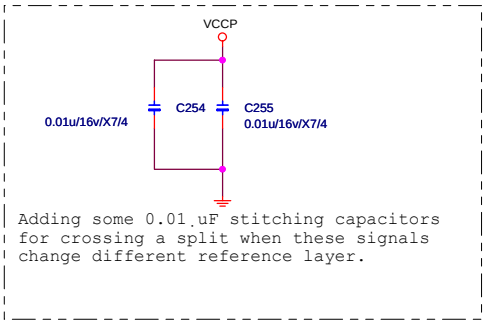
5 / 10

NB,RS780,A01,FCBGA-528pin

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R



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Title: RS780-HT L		
Size	Document Number: MS-7501	Rev: 0A
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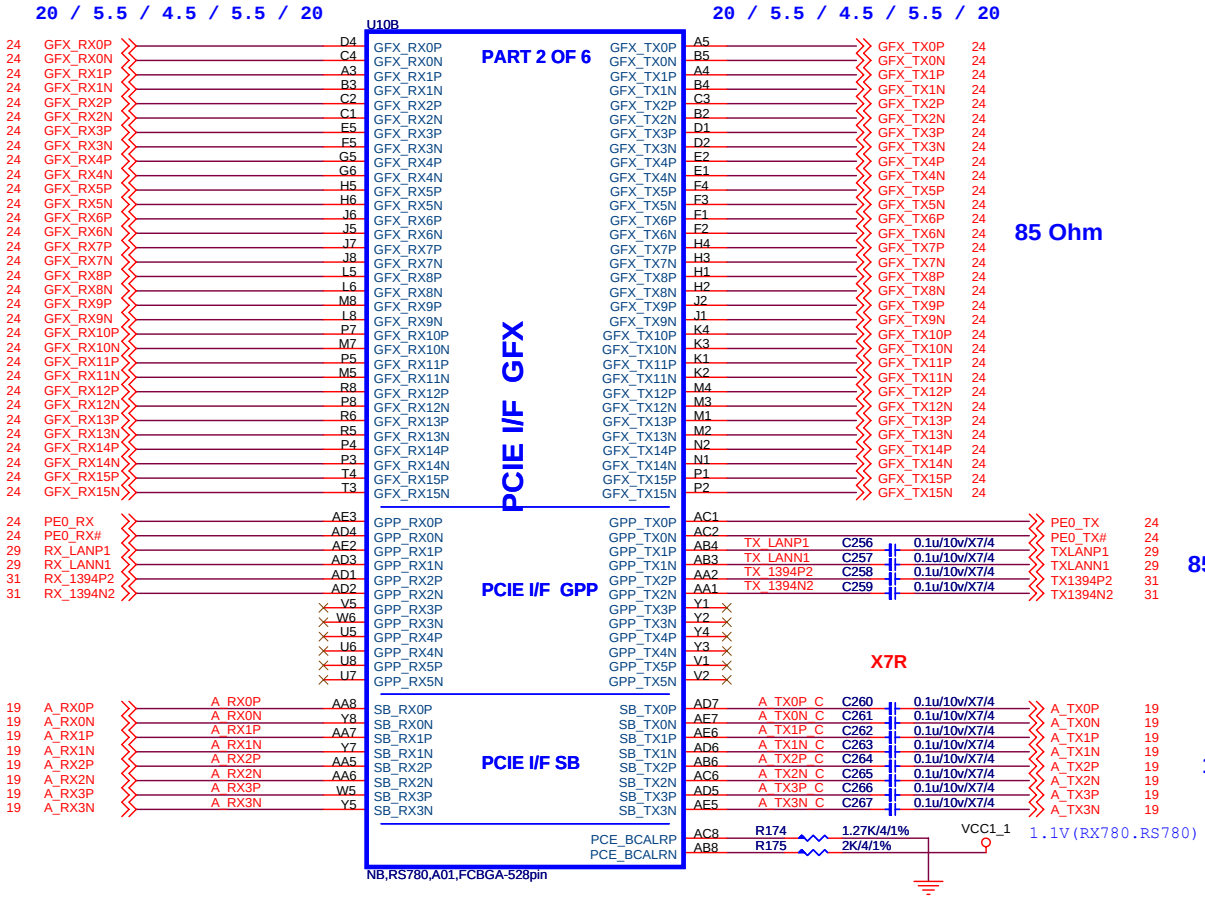

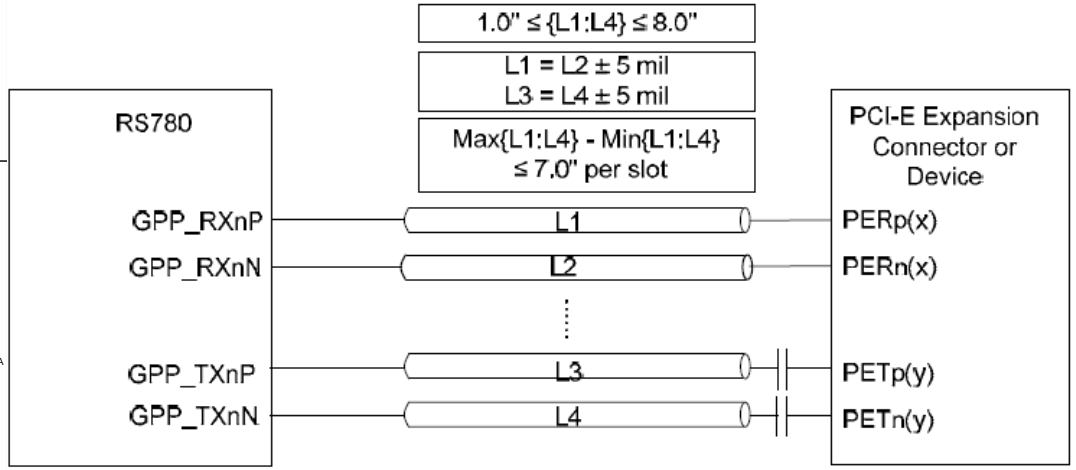

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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NC : U11 , R182 , R290
Stuff : R742 and R743
for RS780 A12 spec
Remind BIOS

ANALOG POWER X5R

PLL X5R

CRB Shiner_Rev2.1 DNI

ANALOG POWER X5R

RX740/RS740/RS780 difference table

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

NC : Q22, R219, R220, Q23, R226, R227
Stuff : R225, R228
for RS780 A12 spec

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)

RX780: pin DFT_GPIO5
RS780: pin VSYNC

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Appicable

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RX780/RS740/RS780 JTAG PIN MAPPING

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

JTAG interface	RS780 Ball Name	Ball #
TEST_EN	TESTMODE	D13
TCK	I2C_CLK	B9
TDI	I2C_DATA	A9
TDO	TMDS_HPD	D9
TMS	DDC_DATA0/AUX0N	B8

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Title: RS780-SYSTEM I/F

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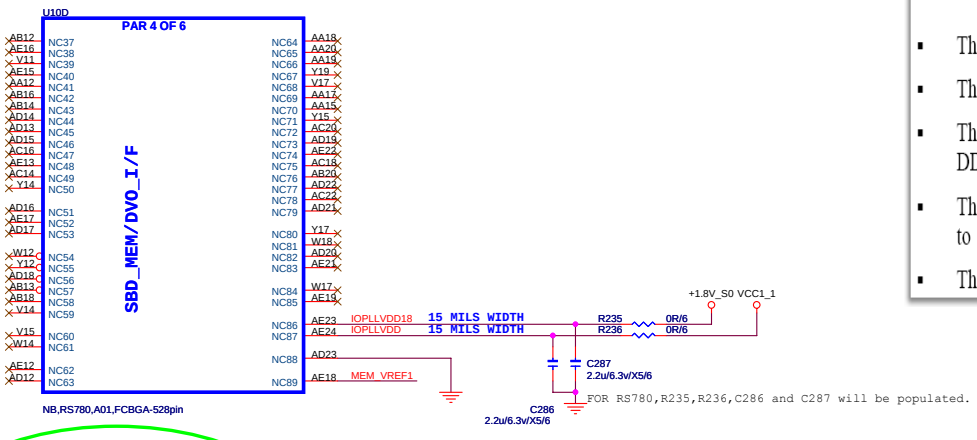
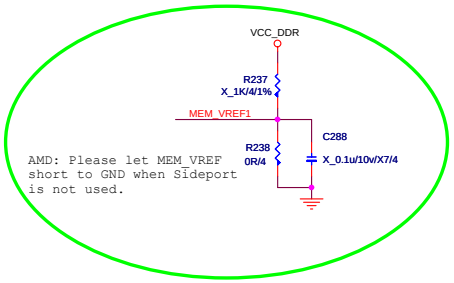




Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

Max Power Estimates for RS780 and SB700

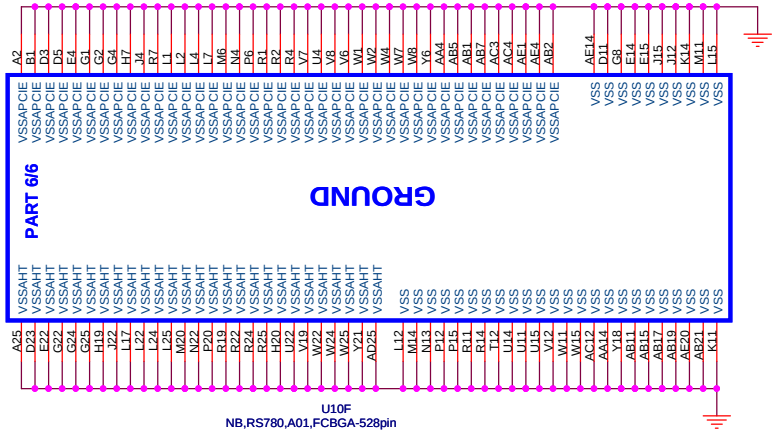
(Preliminary Data w/ Internal Clock Generator and IMC disabled) April 2007

Voltage	Usage	Domain	Max(Spec)
1.0-1.1V	RS780	S0/S1	10A
1.1V	RS780	S0/S1	3-4A
1.2V	RS780 & SB700	S0/S1	2.4A (1A-NB / 1.4A-SB)
1.8V	RS780& SB700	S0/S1	0.8A (0.75A-NB / 50mA-SB)

Max Power Estimates for RS780 and SB700 (continued)

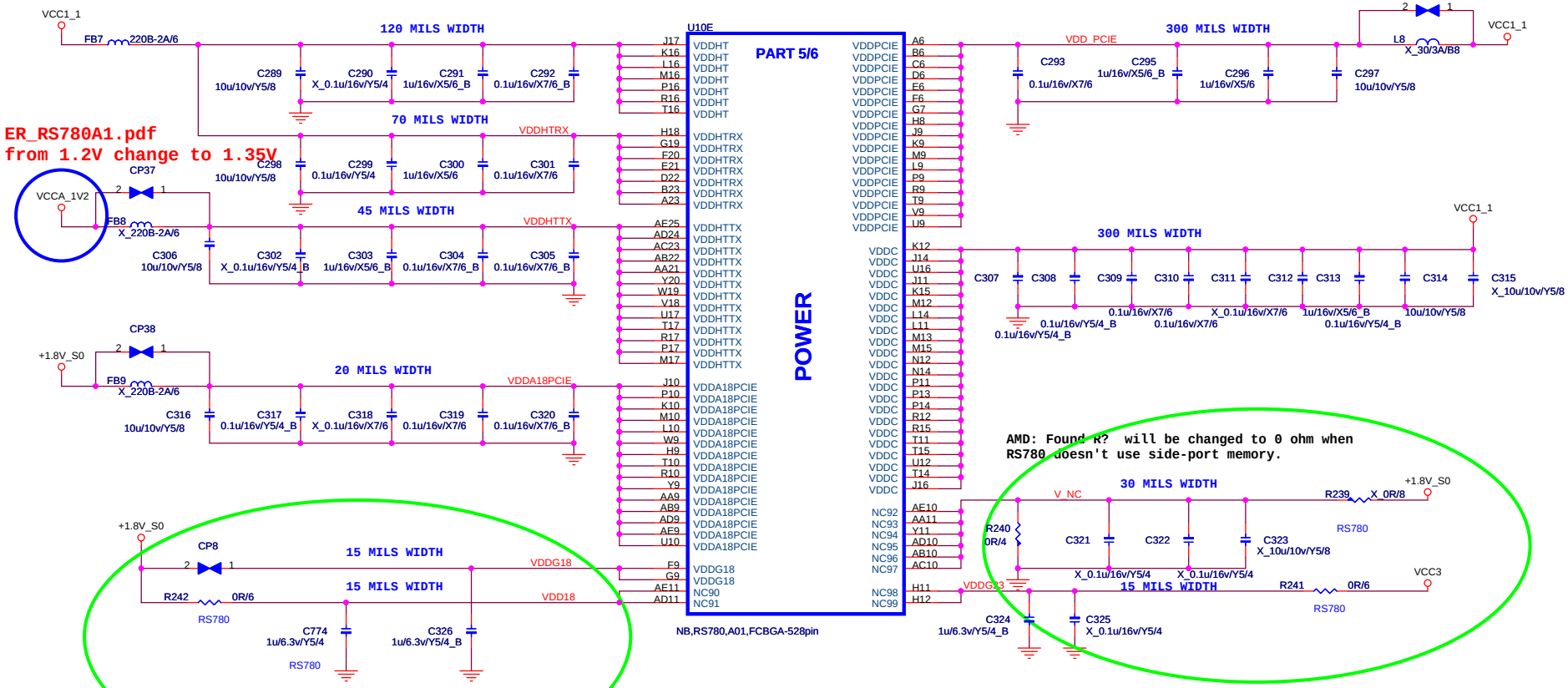
April 2007

Voltage	Usage	Domain	Max(Spec)
3.3V	RS780& SB700	S0/S1	428mA (0.3A-NB / 128mA-SB)
1.2VDual	SB700	S0/S1/S2/S3/S4/S5	217mA
3.3VDual	SB700	S0/S1/S2/S3/S4/S5	495mA
5V	SB700 V5_VREF	S0/S1	0.21mA



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



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Title: RS780-POWER

Size | Document Number: MS-7501 | Rev: 0A

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SB HEAT-SINK

U13_X1

MSI DDR

SB_HEATSINK

7388

SIO PCICLK has beaneged PCICLK5 to PCICLK4 for AMD recommand

For EMI

PCICLK0_SLOT1 — C327 15p/50v/N/4

PCICLK4_SIO — C329 15p/50v/N/4

PCICLK1_SLOT2 — C334 15p/50v/N/4

TPM_PCLK — C330 15p/50v/N/4

U13A

SB700

Part 1 of 5

PLACE PCIE CAPS CLOSE TO U13

100 Ohm

A_RST# — R247 33R/4 — N2

A_RX0P — C335 0.1u/10v/X7/4 — A_RX0P_C — V23

A_RX0N — C336 0.1u/10v/X7/4 — A_RX0N_C — V22

A_RX1P — C337 0.1u/10v/X7/4 — A_RX1P_C — V24

A_RX1N — C338 0.1u/10v/X7/4 — A_RX1N_C — V25

A_RX2P — C331 0.1u/10v/X7/4 — A_RX2P_C — U25

A_RX2N — C340 0.1u/10v/X7/4 — A_RX2N_C — U24

A_RX3P — C332 0.1u/10v/X7/4 — A_RX3P_C — T23

A_RX3N — C341 0.1u/10v/X7/4 — A_RX3N_C — T22

PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N

A_TX0P U22 PCIE_RX0P

A_TX0N U21 PCIE_RX0N

A_TX1P U19 PCIE_RX1P

A_TX1N V19 PCIE_RX1N

A_TX2P R20 PCIE_RX2P

A_TX2N R21 PCIE_RX2N

A_TX3P R18 PCIE_RX3P

A_TX3N R17 PCIE_RX3N

VCC_SB — L9 30/3A/B8 — PCIE_VDDR — R246 562R/4/1% — R253 2.05K/4/1 — T25 PCIE_CALRP — T24 PCIE_CALRN

PCIE_PVDD — P24

P25 PCIE_PVSS

C343 10u/6.3V/X5/8 — C344 1u/6.3v/Y5/4

PCI EXPRESS INTERFACE

PCI CLKS

PCICLK0 P4 — PCI_CLK0 — R244 33R/4 — PCICLK0_SLOT1 — PCICLK0_SLOT1 25

PCICLK1 P3 — PCI_CLK1 — R248 33R/4 — PCICLK1_SLOT2 — PCICLK1_SLOT2 25

PCICLK2 P1 — PCI_CLK2 — R249 33R/4 — TPM_PCLK — TPM_PCLK 23,32

PCICLK3 P2 — PCICLK3 — PCICLK3 23

PCICLK4 T4 — PCI_CLK4 — R251 33R/4 — PCICLK4_SIO — PCICLK4_SIO 23,32

PCICLK5/GPIO41 T3 — PCICLK5 — PCICLK5 23

PCIRST# N1 — PCI_RST# — R245 33R/4 — PCIRST# 25

10 pf For SA

VCC3 — C342 0.1u/16v/Y5/4_B

Adding some 0.1 uF stitching capacitors for crossing a split when these signals change different reference layer.

AD[31..0] — AD[31..0] 25

AD0 U2 — AD0

AD1 P7 — AD1

AD2 V4 — AD2

AD3 T1 — AD3

AD4 V3 — AD4

AD5 U1 — AD5

AD6 V1 — AD6

AD7 V2 — AD7

AD8 T2 — AD8

AD9 W1 — AD9

AD10 T9 — AD10

AD11 R6 — AD11

AD12 R7 — AD12

AD13 R5 — AD13

AD14 U8 — AD14

AD15 U5 — AD15

AD16 Y7 — AD16

AD17 W8 — AD17

AD18 V9 — AD18

AD19 Y8 — AD19

AD20 AA8 — AD20

AD21 Y4 — AD21

AD22 Y3 — AD22

AD23 Y2 — AD23

AD24 AA2 — AD24

AD25 AB4 — AD25

AD26 AA1 — AD26

AD27 AB3 — AD27

AD28 AB2 — AD28

AD29 AC1 — AD29

AD30 AC2 — AD30

AD31 AD1 — AD31

PCI_CBE#[3..0] — PCI_CBE#[3..0] 25

CBE0# W2 — PCI_CBE#0

CBE1# U7 — PCI_CBE#1

CBE2# AA7 — PCI_CBE#2

CBE3# Y1 — PCI_CBE#3

FRAME# AA6 — PCI_FRAME# 25

DEVSEL# W5 — PCI_DEVSEL# 25

IRDY# AA5 — PCI_IRDY# 25

TRDY# Y5 — PCI_TRDY# 25

PAR U6 — PCI_PAR 25

STOP# W6 — PCI_STOP# 25

PERR# W4 — PCI_PERR# 25

SERR# V7 — PCI_SERR# 25

REQ0# AC3 — PCI_REQ#0 25

REQ1# AD4 — PCI_REQ#1 25

REQ2# AB7 — PCI_REQ#2 25

REQ3#/GPIO70 AE6 — PCI_REQ#3 — PCI_REQ#3 25

REQ4#/GPIO71 AB6 — PCI_REQ#4 — PCI_REQ#4 25

GNT0# AD2 — PCI_GNT#0 25

GNT1# AE4 — PCI_GNT#1 25

GNT2# AD5 — PCI_GNT#2 — TP25

GNT3#/GPIO72 AC6 — PCI_GNT#3 — TP41

GNT4#/GPIO73 AE5 — PCI_GNT#4 — TP27

CLKRUN# AD6 — PCI_CLKRUN#

LOCK# V5 — PCI_LOCK# 25

INTE#/GPIO33 AD3 — PCI_INTE# 25

INTF#/GPIO34 AC4 — PCI_INTF# 25

INTG#/GPIO35 AE2 — PCI_INTG# 25

INTH#/GPIO36 AE3 — PCI_INTH# 25

PCI INTERFACE

PCI_CLKRUN# — R256 10K/4 — VCC3

LPC_AD[3..0] — LPC_AD[3..0] 32

7 SBSRCCLK — N25 PCIE_RCLKP/NB_LNK_CLKP

7 SBSRCCLK# — N24 PCIE_RCLKN/NB_LNK_CLKN

100 Ohm

K23 NB_DISP_CLKP

K22 NB_DISP_CLKN

M24 NB_HT_CLKP

M25 NB_HT_CLKN

P17 CPU_HT_CLKP

M18 CPU_HT_CLKN

M23 SLT_GFX_CLKP

M22 SLT_GFX_CLKN

J19 GPP_CLK0P

J18 GPP_CLK0N

L20 GPP_CLK1P

L19 GPP_CLK1N

M19 GPP_CLK2P

M20 GPP_CLK2N

N22 GPP_CLK3P

P22 GPP_CLK3N

TP26 — 25M_48M_66M_OSC — L18 25M_48M_66M_OSC

25M_X1 — J21 25M_X1

R257 0R/4_B

J20 25M_X2

CLOCK GENERATOR

LPCCLK0 G22 — LPC_CLK0 — R258 22R/4 — LPCCLK0 23

LPCCLK1 F22 — LPC_CLK1 — R259 22R/4 — LPCCLK1 23

LAD0 H24 — LPC_AD0

LAD1 H23 — LPC_AD1

LAD2 J25 — LPC_AD2

LAD3 J24 — LPC_AD3

LFRAME# H25 — LPC_FRAME# 32

LDRQ0# H22 — LPC_DRQ#0 32

LDRQ1#/GNT5#/GPIO68 AB8 — SB600_PCI_GNT5# — TP28

BMREQ#/REQ5#/GPIO65 AD7 — SB600_PCI_REQ5# — R262 10K/4 — VCC3

SERIRQ V15 — SERIRQ 32

LPC

3VDUAL — D9 BAT54C_SOT23 — VBAT

16mil

R265 1K/4 — VBATIN_R — BAT1 — BAT2P/Holder

VBATIN — JBAT1 CNT N31+N33_BG

16mil

32K_X1 — A3 X1

Y2 32.768KHZ/12.5p

32K_X2 — B3 X2

R260 X_20M/6

R266 20M/6

C346 18p/50v/N/6

C347 18p/50v/N/6

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

RTC XTAL

VCC_DDR — R261 300R/4

+1.8V_S0 — R263 1K/4

16 ALLOW_LDTSTOP — R267 X_0R/4 — F23 ALLOW_LDTSTP

8 CPU_HOT — E24 PROCHOT#

8 LDT_PWRGD — LDT_PWRGD — F22 LDT_PG

8,16 LDT_STOP# — LDT_STOP# — G25 LDT_STP#

8,16 LDT_RST# — LDT_RST# — G24 LDT_RST#

CPU

RTCCLK C3 — INTR_ALERT# — TP40

INTRUDER_ALERT# C2

VBAT B2 — VBAT_IN — R269 X_100K/4 — 3VDUAL

C348

C349 0.1u/16v/Y5/4

1u/6.3v/Y5/4

RTC

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

SB,SB700,A11,FCBGA-528pin

Check U13 New Version : Port Number

MICRO-STAR INt'L CO., LTD.

Title: SB700-PCIE/PCI/CPU/LPC

Size: — Document Number: MS-7501 — Rev: 0A

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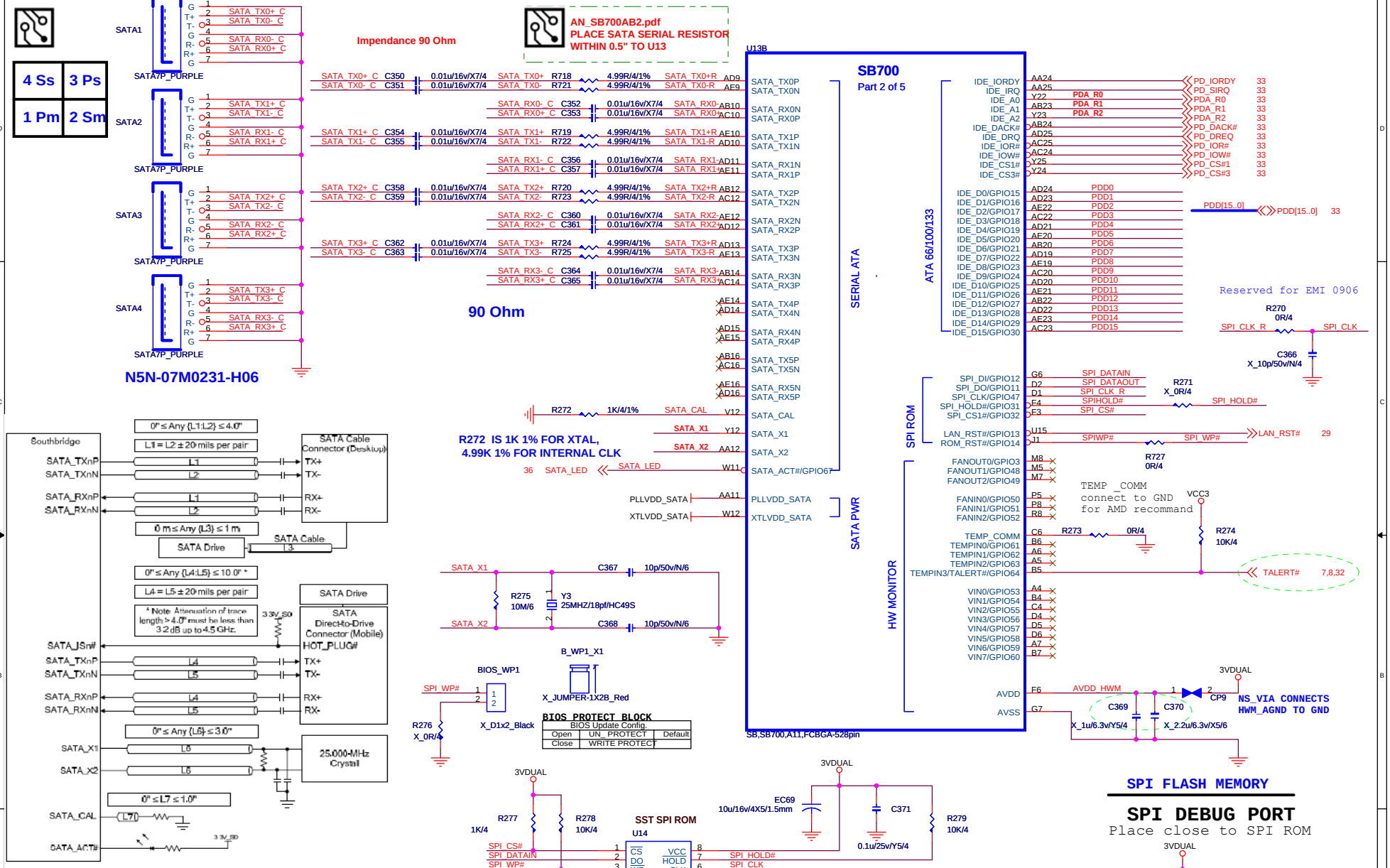


Figure 29: Layout Guidelines the Serial ATA Signals

Trace spacing:

- ASIC breakout (first 0.5") ≥ 1:1
- After the breakout region ≥ 5:1 on both sides of pair.

Impedance:

- 100 Ω ± 15% differential.
- Reference to a solid GND (not PWR) plane.

SB700 Pin C8 USBCLK/14M_25M_48M_OSC
Function set output pin by BIOS.

Cap have been unpopulate for meet power sequence

Added Cap 0.1 uF stitching capacitors for crossing a split

90 Ohm

Trace spacing:

- ASIC breakout (first 0.5") ≥ 1:1
- After the breakout region ≥ 4:1 on both sides of pair.
- Serpentine spacing ≥ 4:1 on both sides of pair.
- ≥ 5:1 from reference plane anti-etch (copper void) or edges.
- ≥ 0.5" from clock chips, oscillators, crystals, core logic or CPU devices.

Impedance:

- 90 Ω ± 15% differential
- Reference to a solid GND (not PWR) plane.

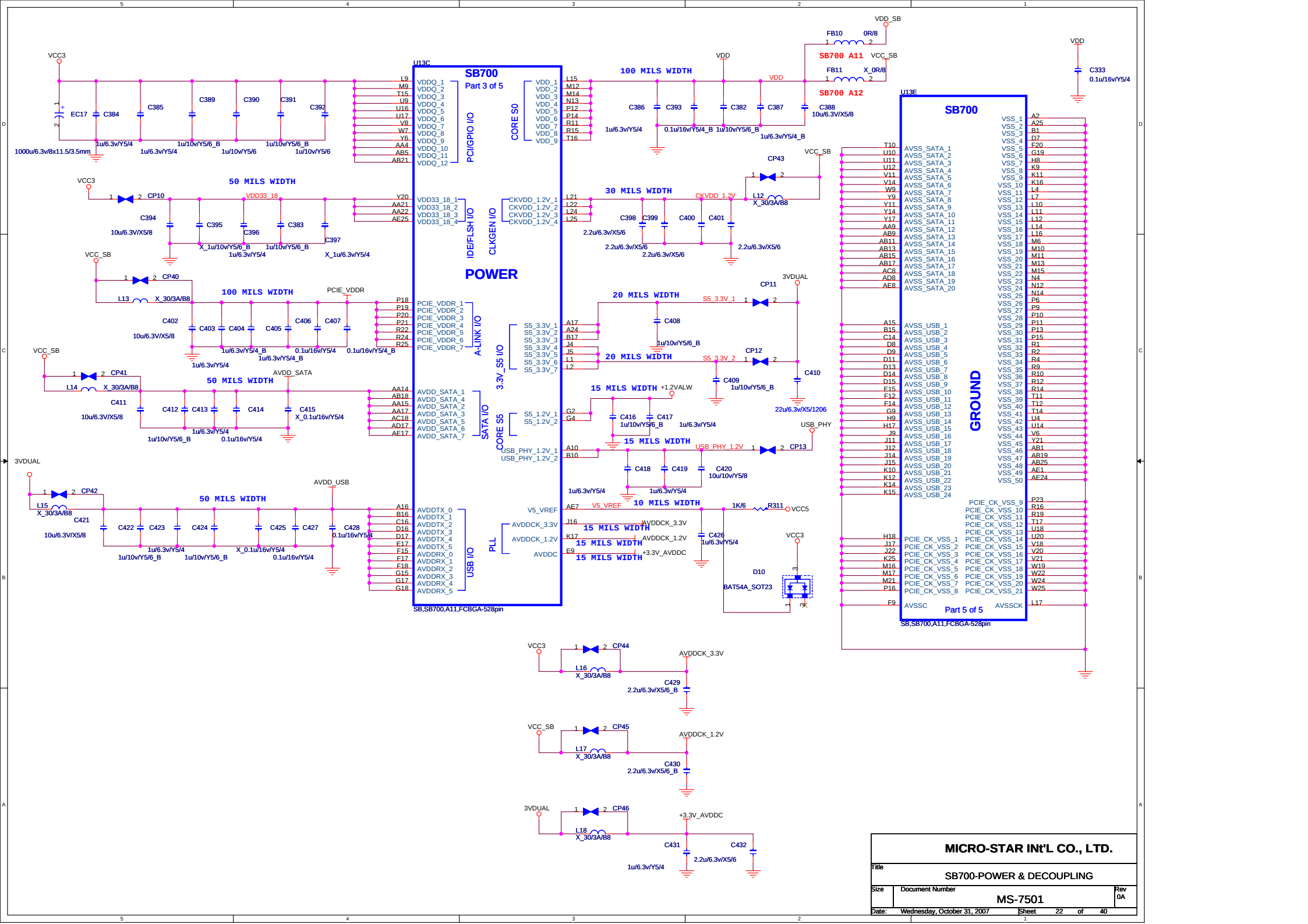
Reserved for EMI 0906

For EMI(closed SB)

Figure 26 Layout Guidelines for the Universal Serial Bus Signals

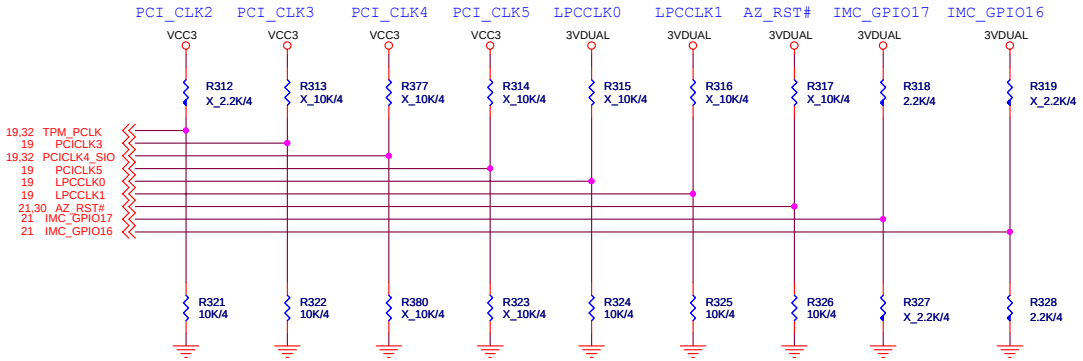
Title	SB700-ACPI/GPIO/USB/AUDIO
Size	Document Number: MS-7501
Rev	0A
Date:	Wednesday, October 31, 2007
Sheet	21 of 40

MICRO-STAR INt'L CO., LTD.


SB700
Part 3 of 5
U13C
POWER
SB700
Part 5 of 5
U13E
GROUND
SB700 A11
SB700 A12
100 MILS WIDTH
50 MILS WIDTH
30 MILS WIDTH
20 MILS WIDTH
15 MILS WIDTH
10 MILS WIDTH
SB,SB700,A11,FCBGA-528pin
MICRO-STAR INt'L CO., LTD.
SB700-POWER & DECOUPLING
MS-7501
Rev 0A
Wednesday, October 31, 2007
Sheet 22 of 40

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

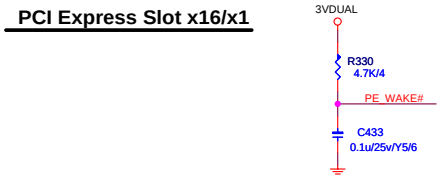
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

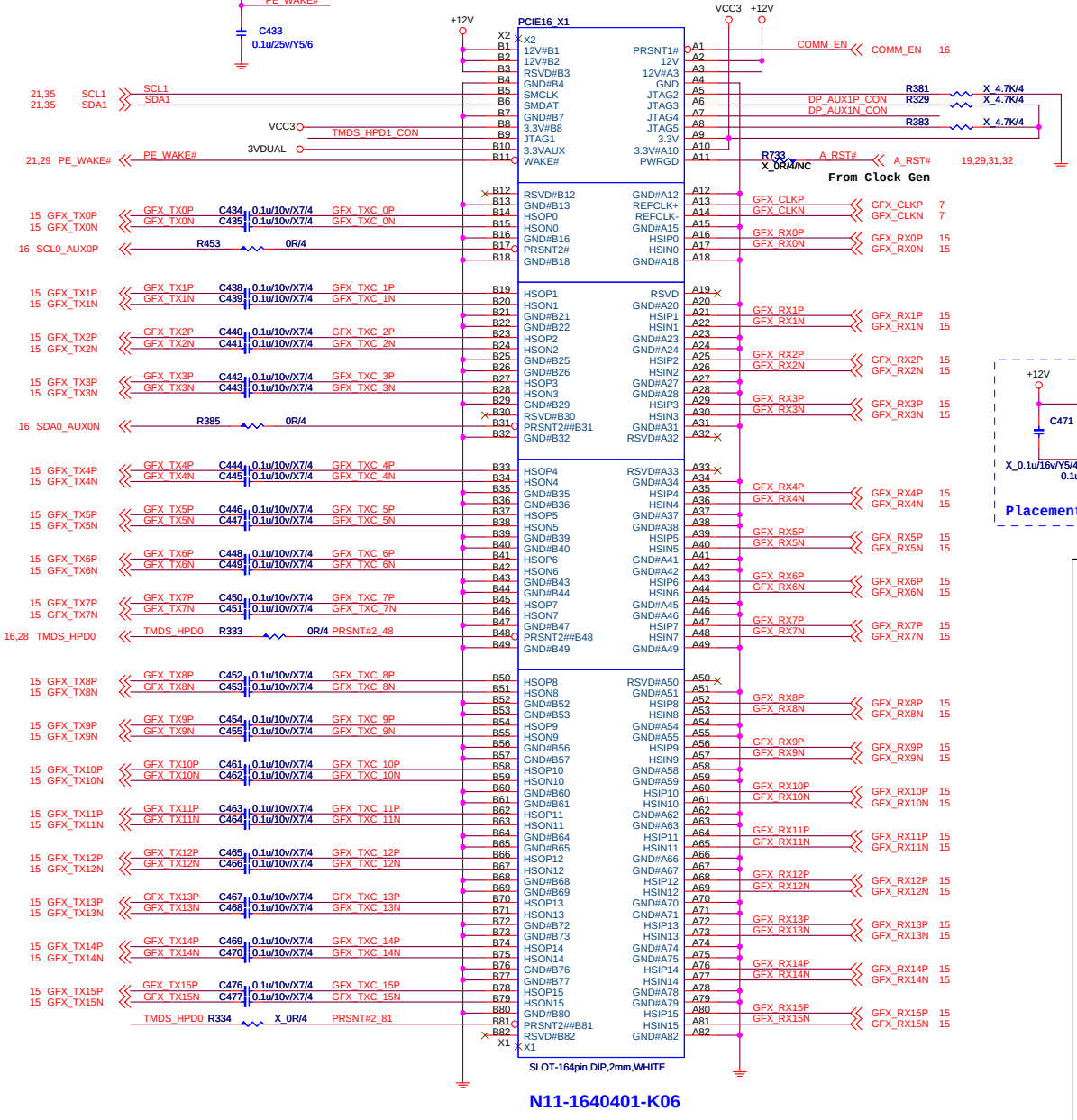
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INt'L CO., LTD.			
Title: SB700-STRAPS			
Size	Document Number: MS-7501		Rev: 0A
Date: Wednesday, October 31, 2007	Sheet 23 of 40		

PCI Express Slot x16/x1

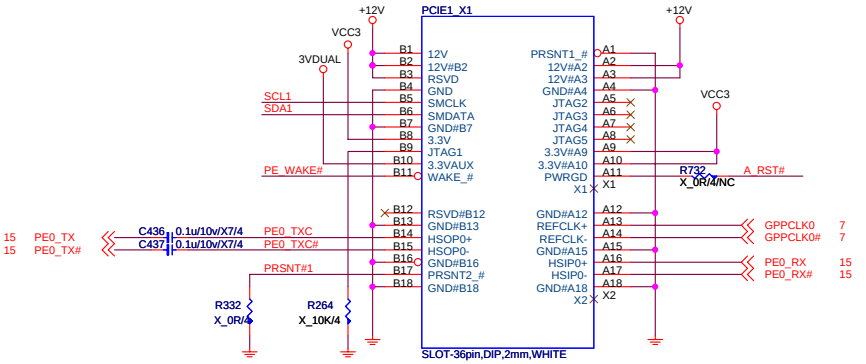


PCI EXPRESS x16 Slot

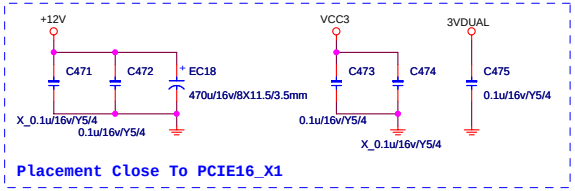


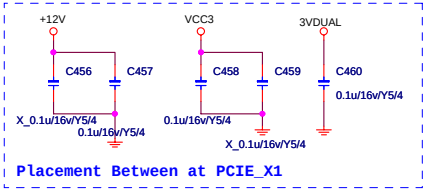
N11-1640401-K06

PCI EXPRESS 1 Slot-1



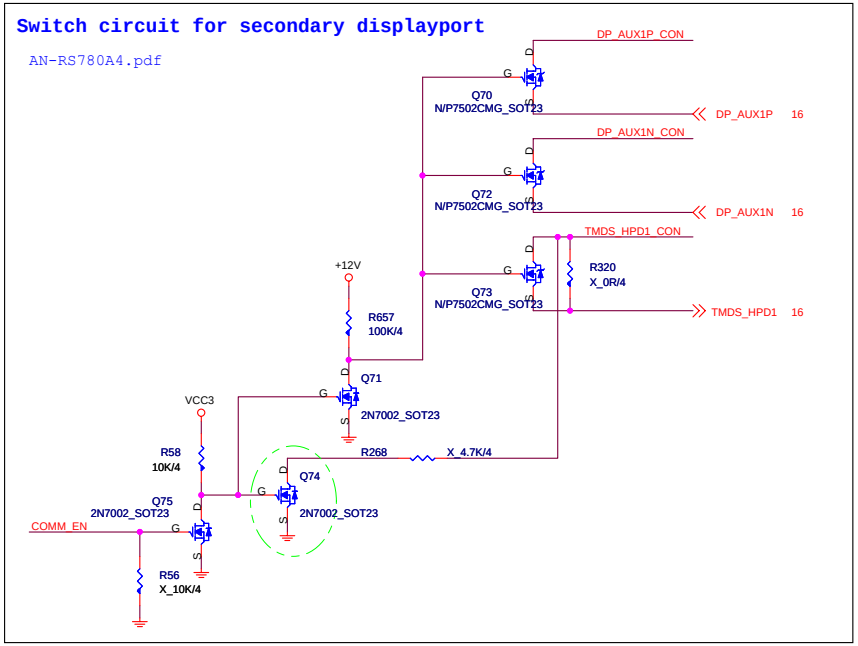
N11-0360091-F02





Switch circuit for secondary displayport

AN-RS780A4.pdf



MICRO-START INT'L CO.,LTD.

Title	PCI EXPRESS X16 & X1 SLOT	
Size: Custom	Document Number: MS-7501	Rev: 0A
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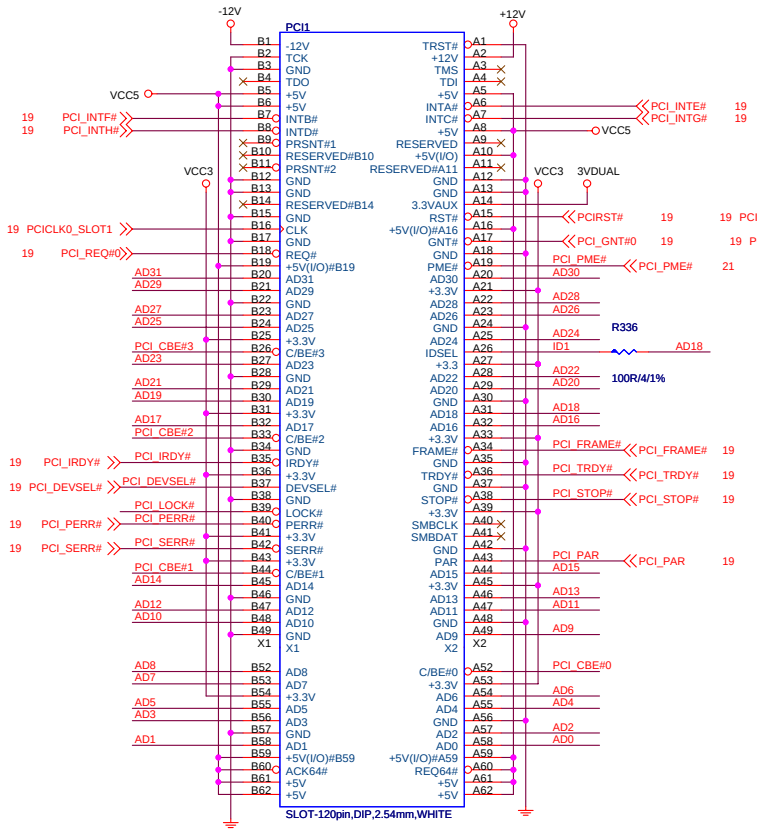
19 AD[31..0] AD[31..0]

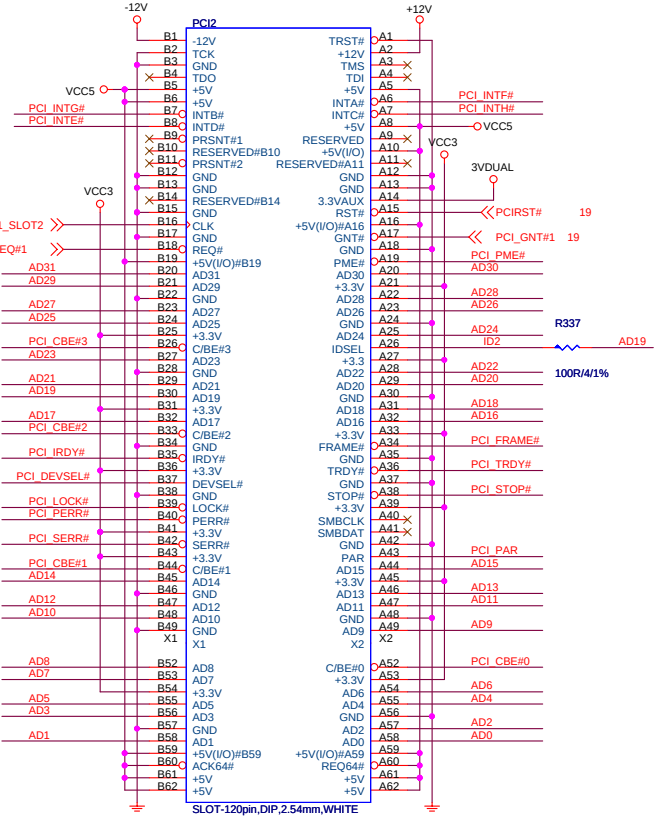
19 PCI_CBE#[3..0] PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

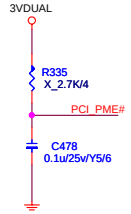


IDSEL = AD18
MASTER = PCI_REQ#0
PCI_GNT#0

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

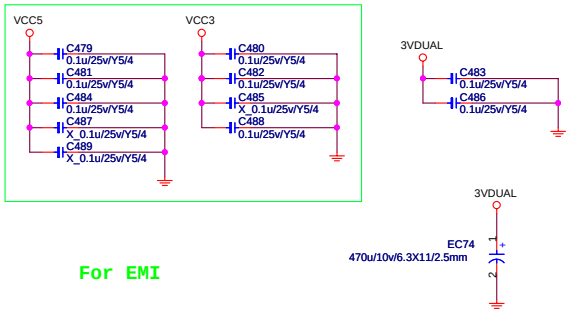


IDSEL = AD19
MASTER = PCI_REQ#1
PCI_GNT#1



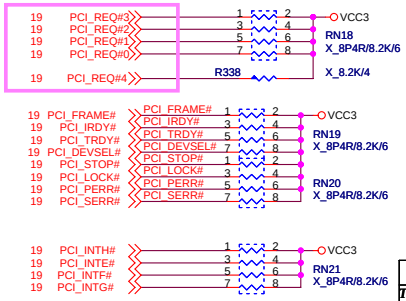
N11-1200271-F02

PCI SLOT DECOUPLING CAPACITORS



For EMI

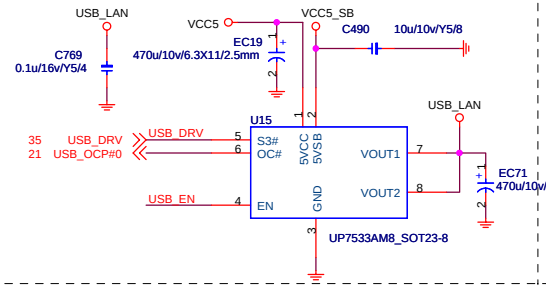
PCI PULL-UP / DOWN RESISTORS



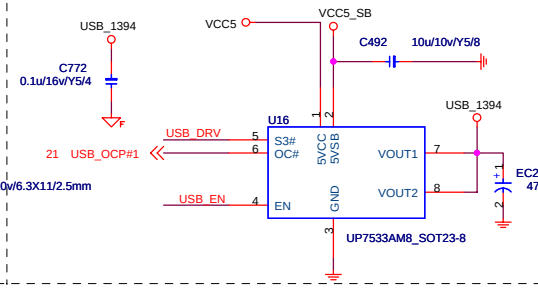
Micro Star Restricted Secret

Title: PCI Slot 1 2	Rev: 0A
Document Number: MS-7501	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, October 31, 2007
	Sheet 25 of 40

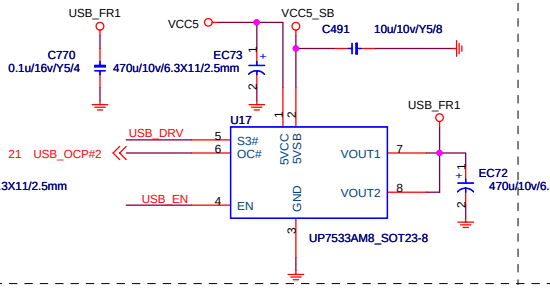
POWER CIRCUIT FOR USB PORT 4,5



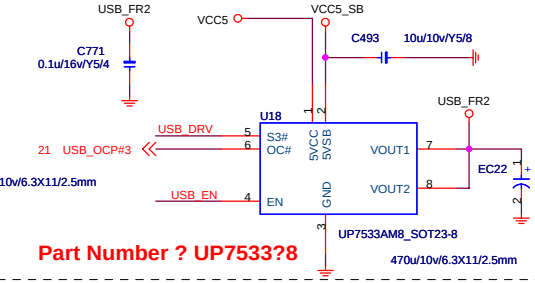
POWER CIRCUIT FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



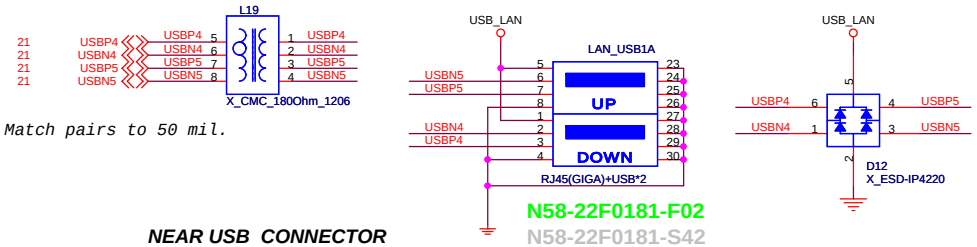
POWER CIRCUIT FOR USB PORT 6,7



Part Number ? UP7533?8

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



Match pairs to 50 mil.

N58-22F0181-F02

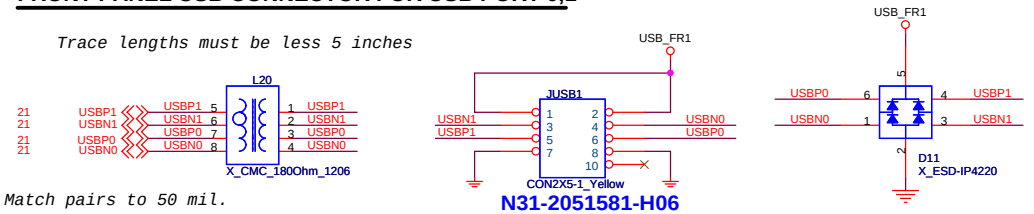
N58-22F0181-S42

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches



Match pairs to 50 mil.

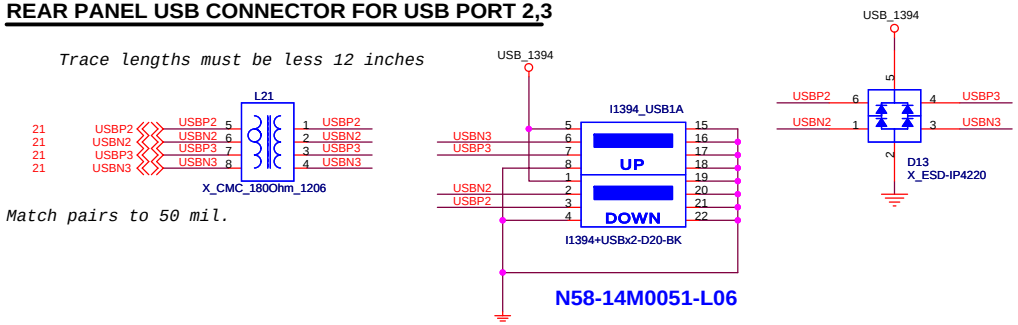
N31-2051581-H06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



Match pairs to 50 mil.

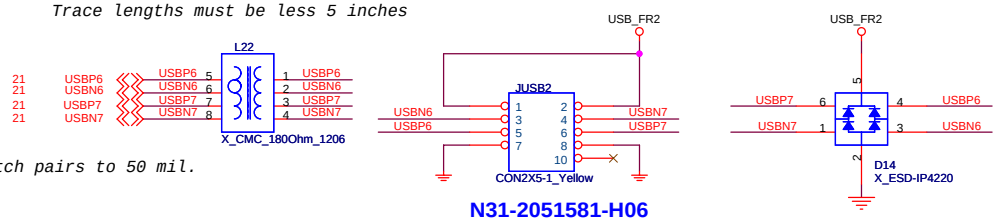
N58-14M0051-L06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



Match pairs to 50 mil.

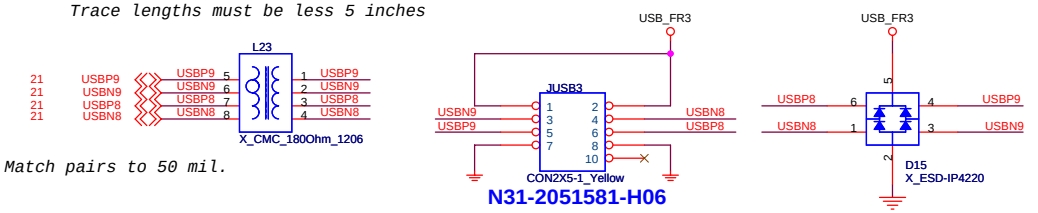
N31-2051581-H06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



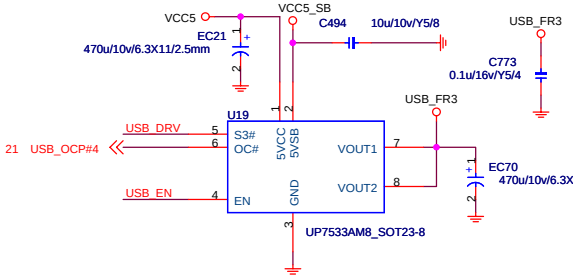
Match pairs to 50 mil.

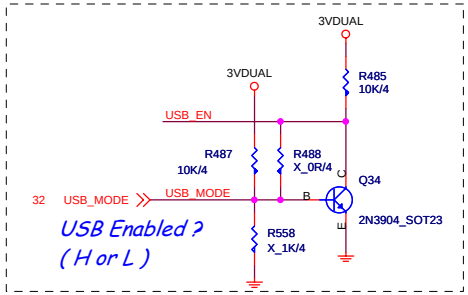
N31-2051581-H06

NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

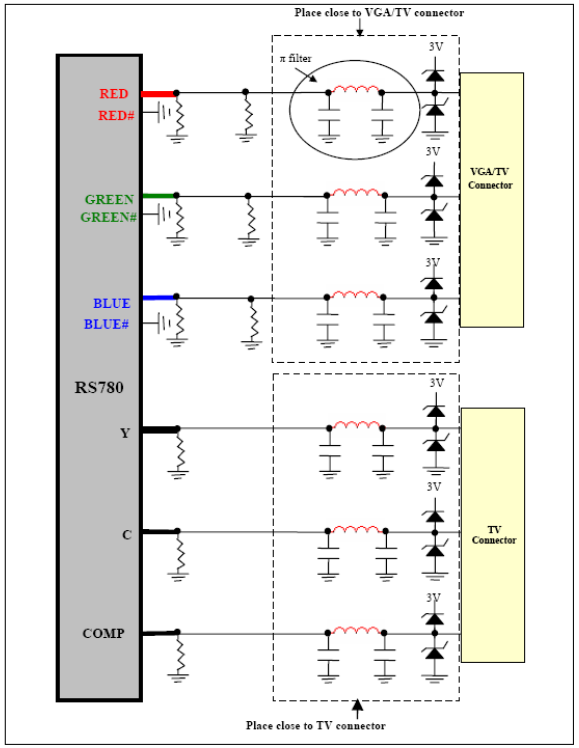
POWER CIRCUIT FOR USB PORT 8,9



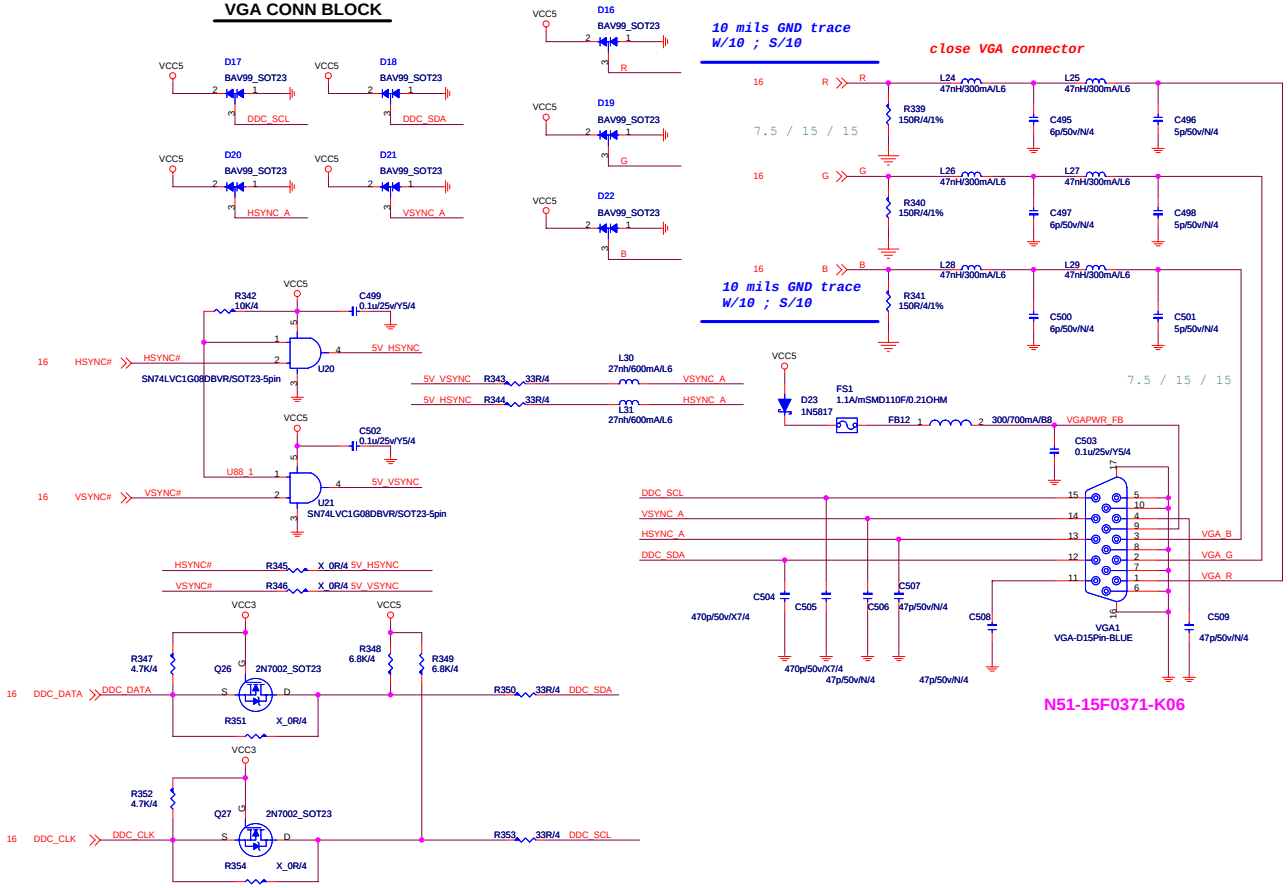


MICRO-STAR INt'L CO., LTD.		
Title: USB Conn.		
Size	Document Number: MS-7501	Rev: 0A
Date: Wednesday, October 31, 2007	Sheet 26 of 40	

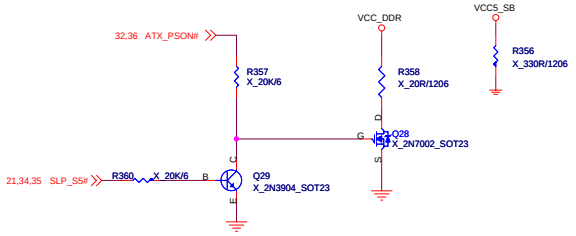
Figure 29: Placement of VGA and TV-Out Connectors



VGA CONN BLOCK



MEMORY VOLTAGE BLEED-OFF CIRCUIT



MICRO-STAR INt'L CO., LTD.	
Title	VGA CONN
Size	Document Number: MS-7501
Rev	0A
Date:	Wednesday, October 31, 2007
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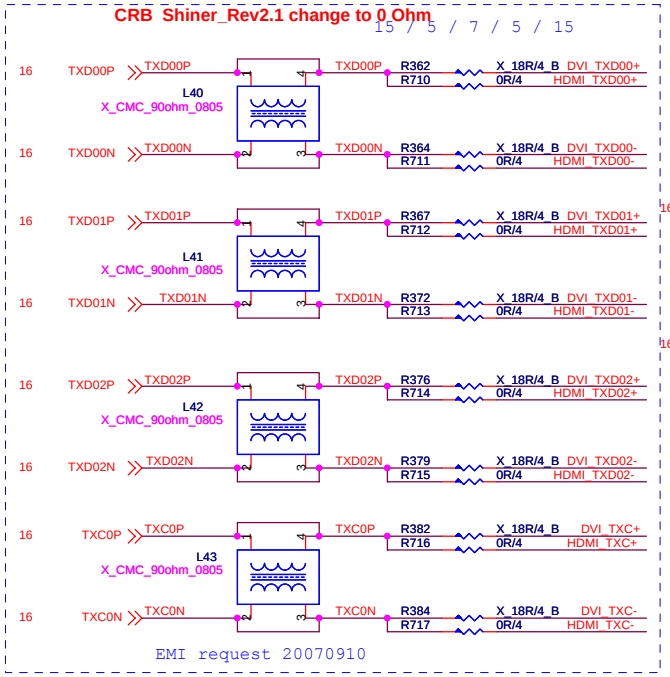
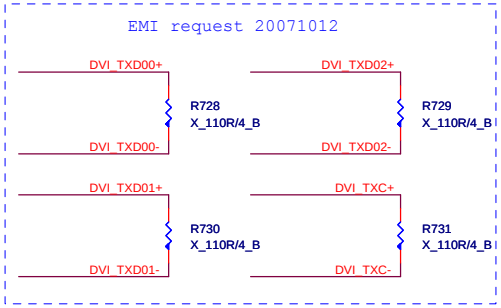
T:2 , H:4.5 ,W:5 ,S:7,Er:4.2 ,Zo=104.8 Ohm

CRB Shiner_Rev2.1 change to 0 Ohm

15 / 5 / 7 / 5 / 15





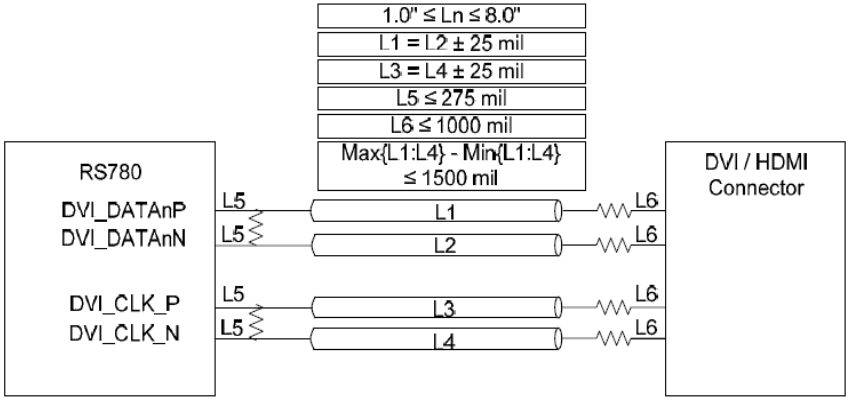
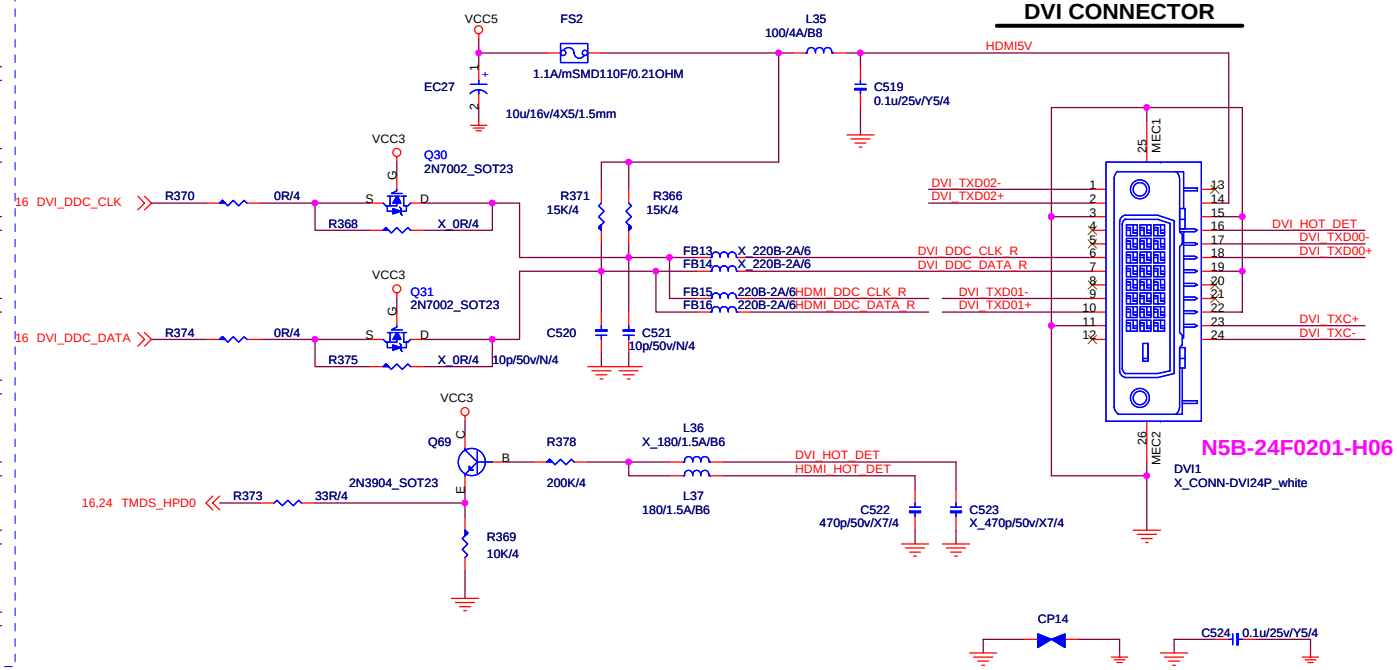
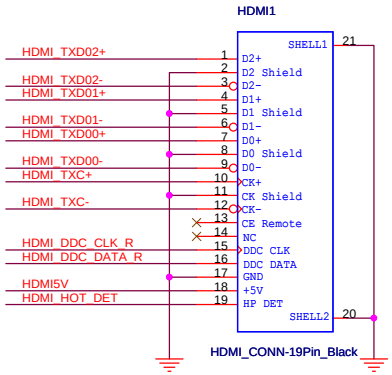


Figure 32: Layout Guidelines for the DVI/HDMI Signals

DVI CONNECTOR



HDMI CONNECTOR



MICRO-STAR INt'L CO., LTD.		
Title: HDMI / DVI CONNECTOR		
Size	Document Number: MS-7501	Rev: 0A
Date: Wednesday, October 31, 2007	Sheet 28 of 40	

1. Pin 64:RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.

2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.

3. RTL8111B/C/8101E, Pin 1~16 forward to transformer, this will made the trace more short.

4. As the Layout Guide, the output pin of Transistor trace please layout it more widely.

5. Make nine through holes at the center of IC board. The back side of IC is GND. Please be aware to connect this GND to the GND of outside of LAN chip.

6. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.

7. The Spec of transistor suggest use the current least 1.2A.

8. 1.5V請留 power plane並且盡量大一點.

9. 1.5V Bypass 電容不能省. Add 0.1u cap. for each power pin of LAN.

10. For RTL8111B, Pin62 有外接兩顆電容絕對不能省.

0 : DISABLE SWITCH REGULATOR 8111C
1 : ENABLE

R395 Place near Pin64

2K for 8101E;
2.49k for 8111B/8111C

MDIx+/- Reference to GND plan.

Cap Place near U22

1 for disable on board
ROM ONLY 81111C

RTL8111C-GR

B06-8111C0C-R09

CHOKE7 close to U22 Pin 1 within 0.5cm

C532 , C533 CLOSE TO CHOKE7

C551 , C529 CLOSE TO Q32

C560 , C561 close to U22 Pin 63 within 0.5cm

For RTL8101E stuff R410 , C563 NC

8111B/8111C TO 0 ohm
8101E TO 0.01uf

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q32	Q33
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A

Power comsuption

	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

N58-16F0031-F02

Giga-Lan	10/100-Lan
N58-22F0081-S42	N58-22F0061-S42 N58-22F0061-F02
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None

N58-22F0181-F02
N58-22F0181-S42

Micro Star Restricted Secret	
Title	LAN - Realtek 8111C(B)/8101E
Rev	0A
Document Number	MS-7501
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, October 31, 2007
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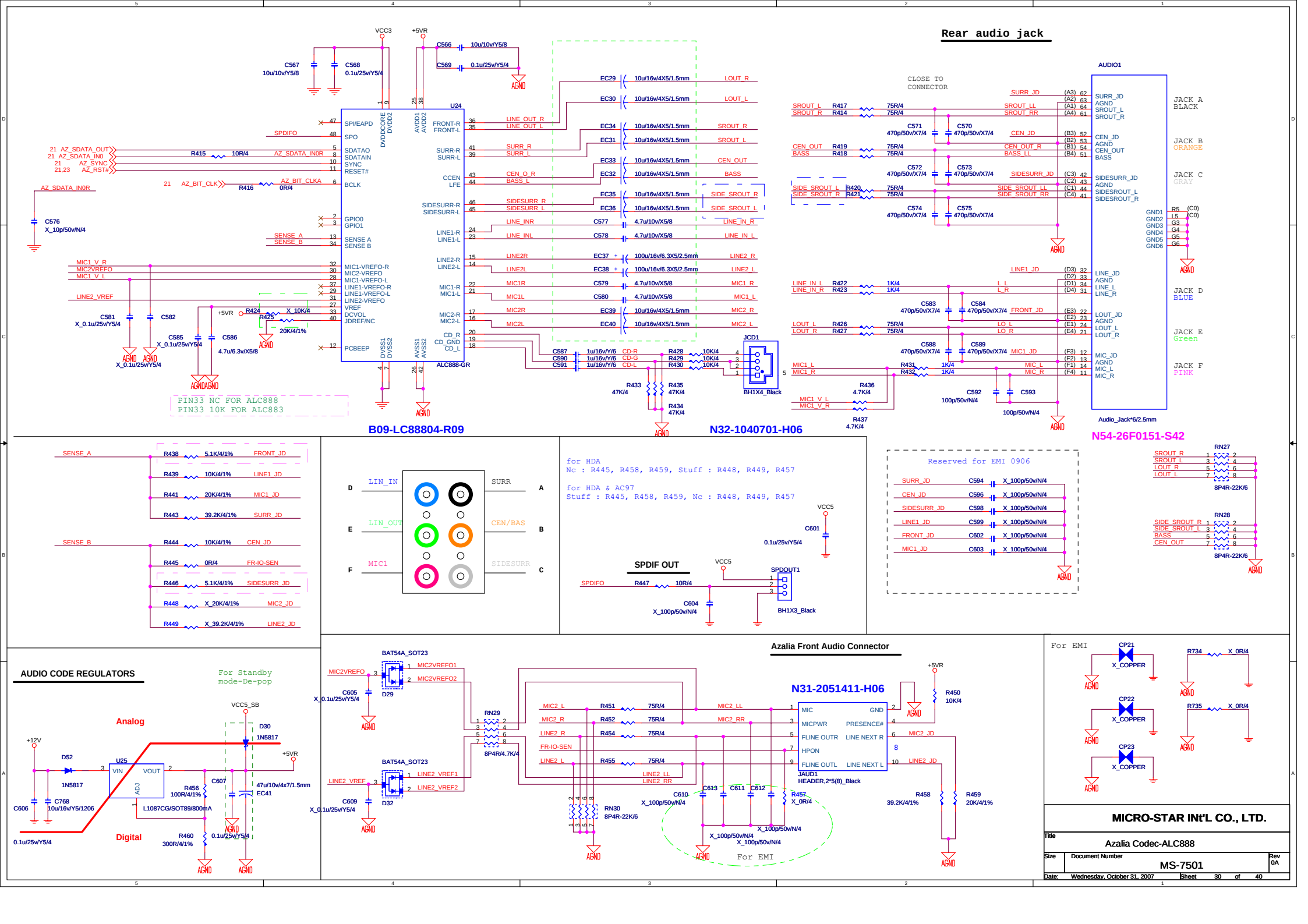
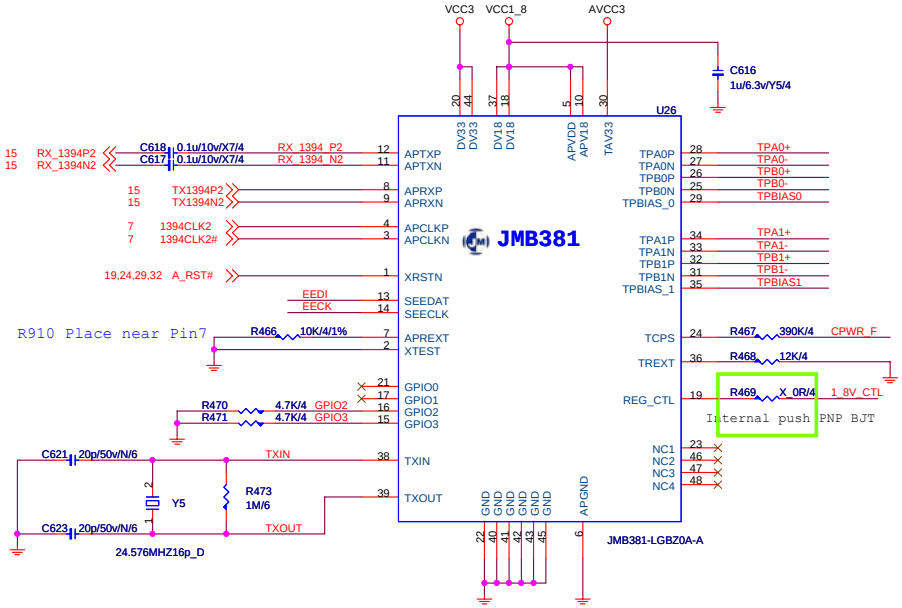
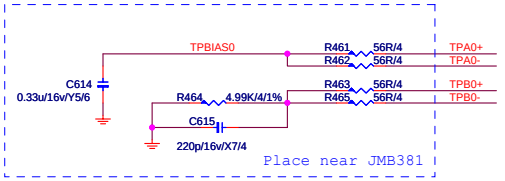
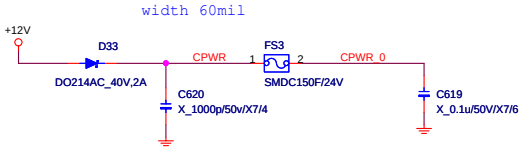

Rear audio jack
U24
ALC888-GR
B09-LC88804-R09
N32-1040701-H06
N54-26F0151-S42
AUDIO1
JACK A BLACK
JACK B ORANGE
JACK C GRAY
JACK D BLUE
JACK E Green
JACK F PINK
CLOSE TO CONNECTOR
PIN33 NC FOR ALC888
PIN33 10K FOR ALC883
Reserved for EMI 0906
for HDA
Nc : R445, R458, R459, Stuff : R448, R449, R457
for HDA & AC97
Stuff : R445, R458, R459, Nc : R448, R449, R457
SPDIF OUT
AUDIO CODE REGULATORS
For Standby mode-De-pop
Analog
Digital
Azalia Front Audio Connector
N31-2051411-H06
For EMI
MICRO-STAR INt'L CO., LTD.
Azalia Codec-ALC888
MS-7501
Wednesday, October 31, 2007

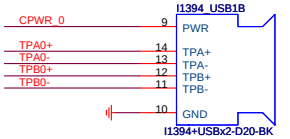
1394 CONTROLLER



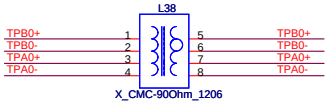
Rear 1394 port



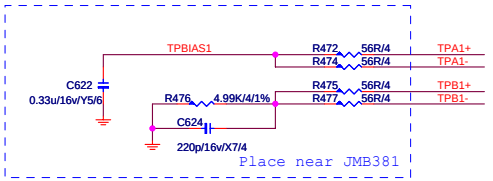


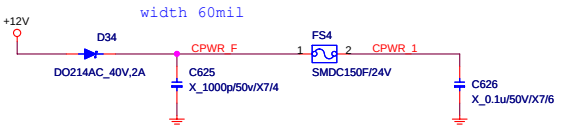


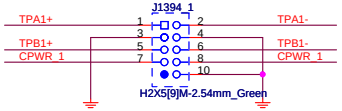
N58-14M0051-L06



Front 1394 pin header

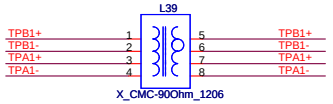






N31-2051551-H06

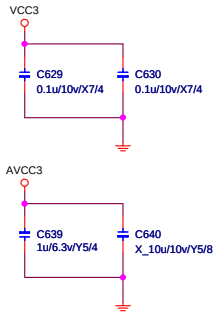
For Intel 1394 pinheader

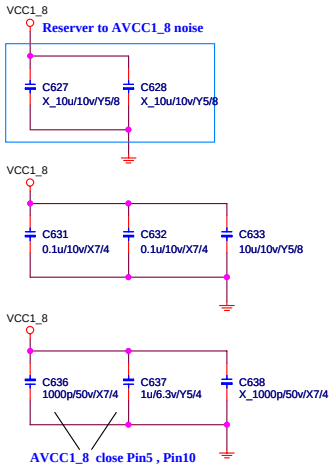


EMI request 11/28

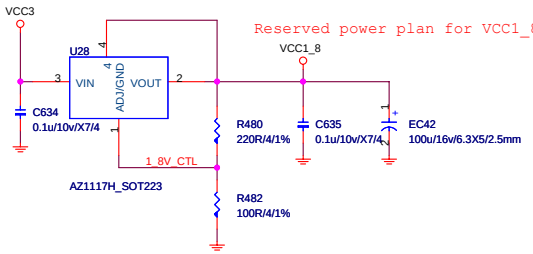
Table 5.1 JMB381 Operating Modes

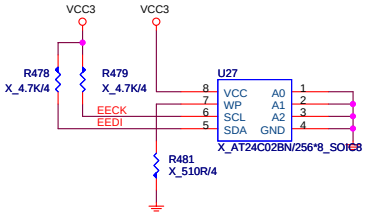
	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1





A1117 CO-LAY SOT223 (TO_261) PNP BJT





S3 Resume time

Title	1394 Controller - JMB381	
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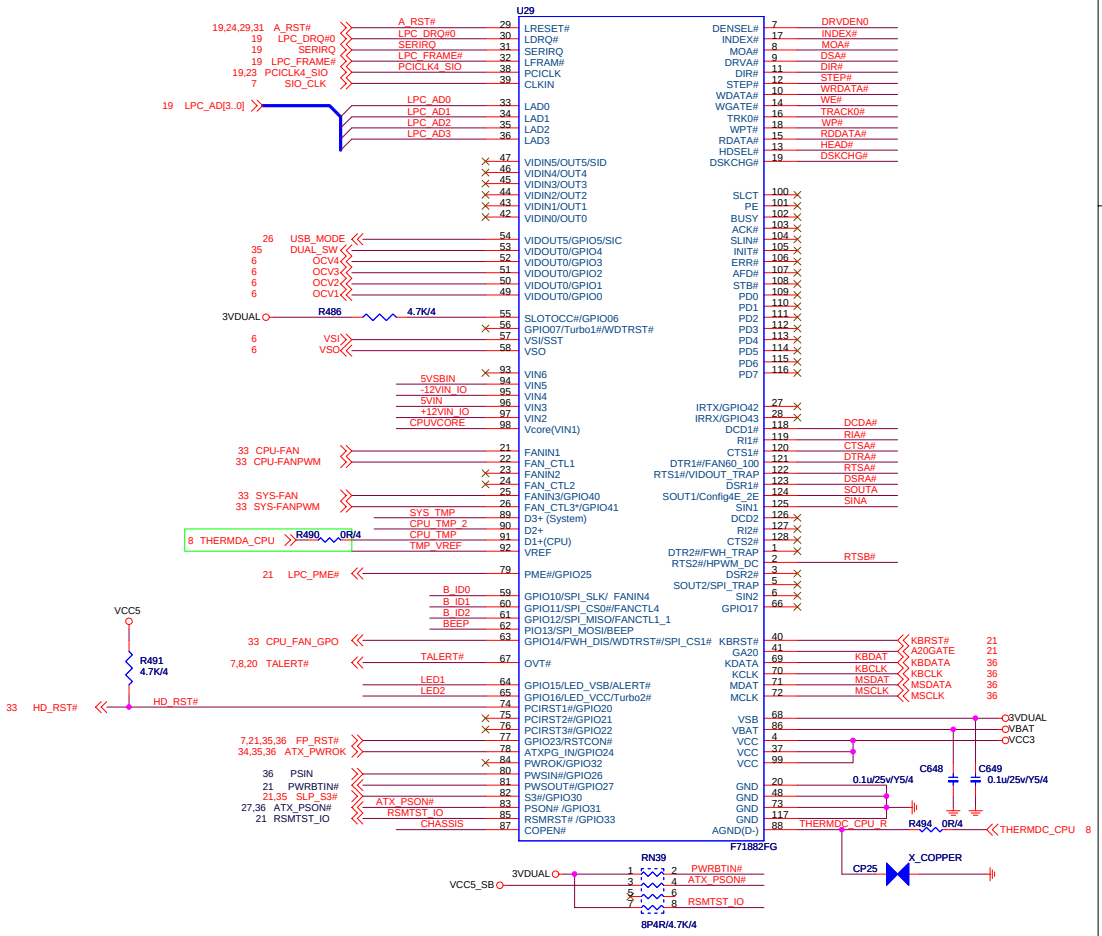
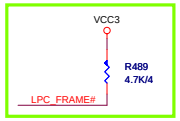
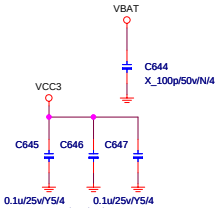
Super I/O

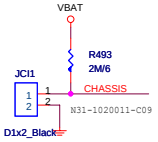
LPC SUPER I/O F71882



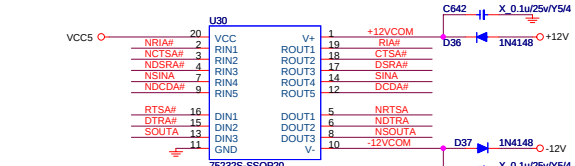




Chasiss Intrusion

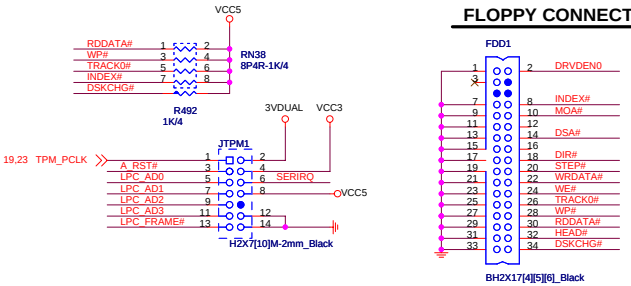


SERIAL PORT 1

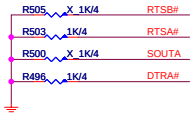


N31-2051331-H06

FLOPPY CONNECTOR

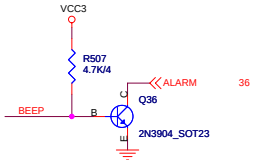


LPC I/O STRAPPING RESISTOR

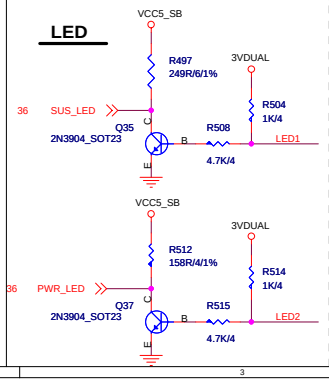


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

BEEP

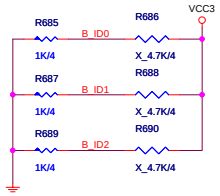


LED

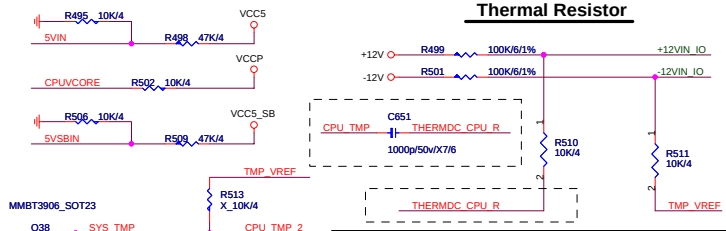


Board ID

Board ID [2:0]	Function
0 0 0	Normal
1 0 0	DOT?



Thermal Resistor



NOTE: LOCATE CLOSE STATUS PANEL

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Title: LPC-F71882 / FDD / COM

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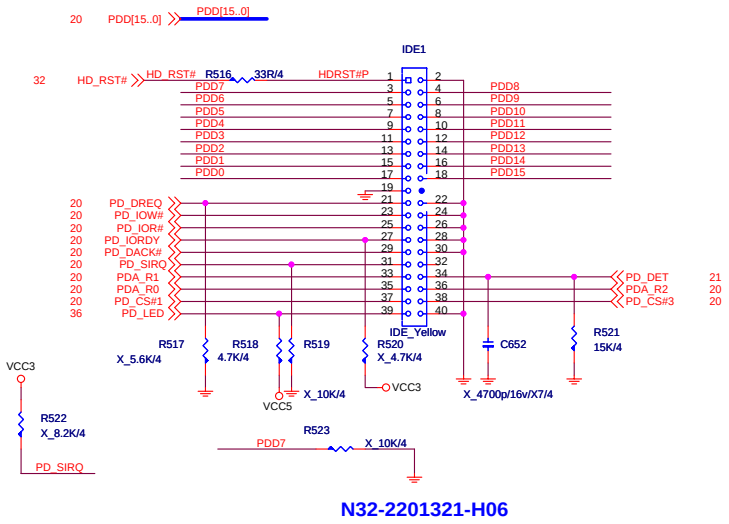
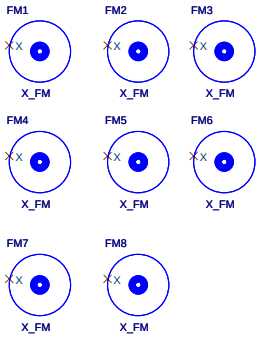
IDE 1

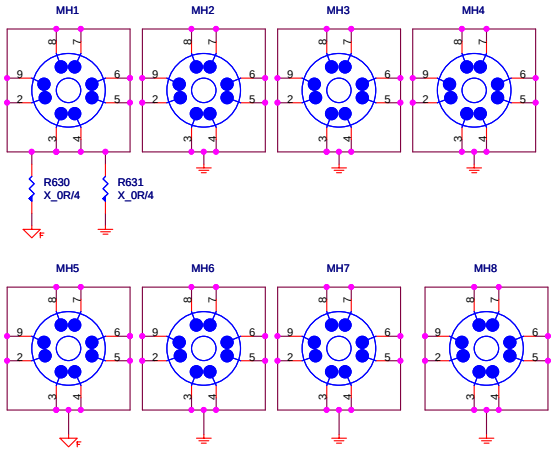


N32-2201321-H06

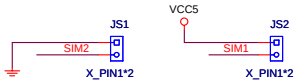
Optics Orientation Holes



Mounting Holes



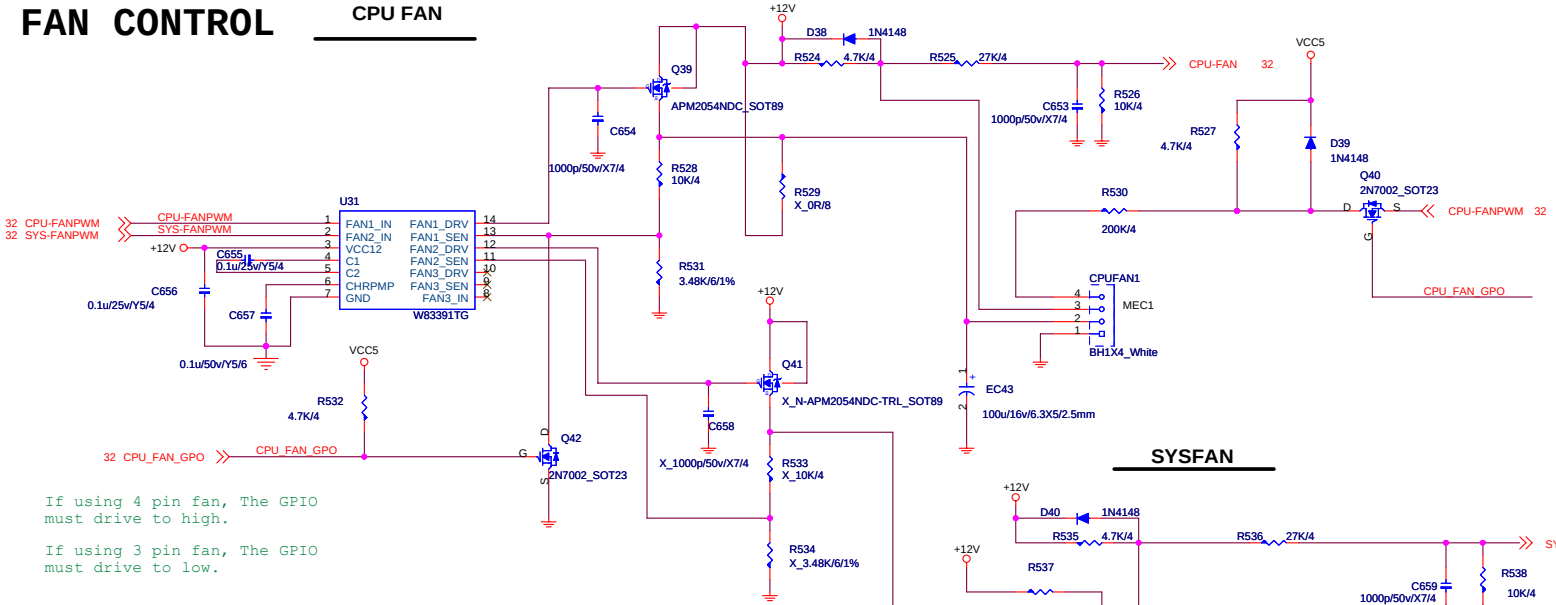
Simulation



FAN CONTROL

CPU FAN

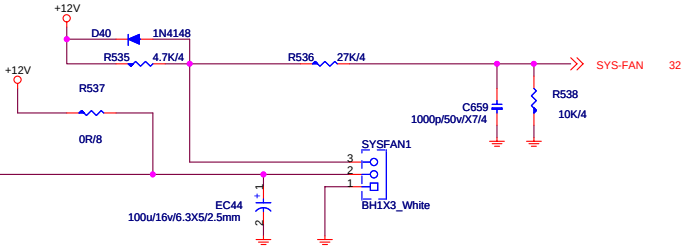
If using 3 pin fan, The Q40 will turn off to avoid the VCC5(R527) bias to CPU-FANPWM.



If using 4 pin fan, The GPIO must drive to high.

If using 3 pin fan, The GPIO must drive to low.

SYSFAN



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Document Number: MS-7501		
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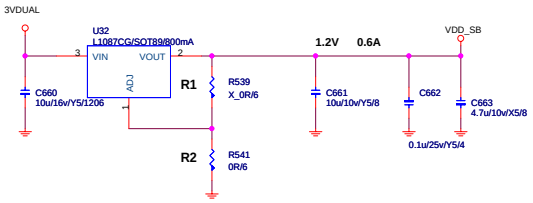
Page 22 : FB10 (A11) , FB11 (A12)

1.25V reference voltage

A11 : Stuff
A12 : Nc

Vo = Vref (1+R2/R1) + ladj x R2

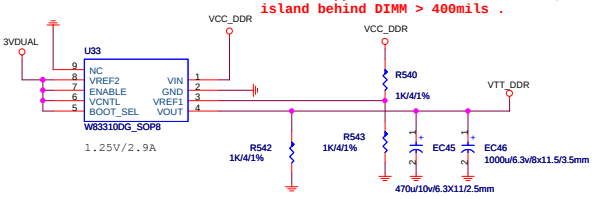


PA_SB700AA1

R539 has been un-populated and R541 has been populated for U32 heat.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



Power Rail Sequence

AMD

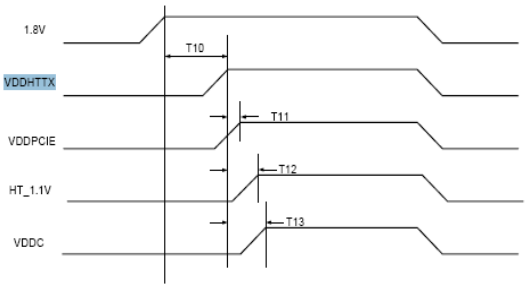
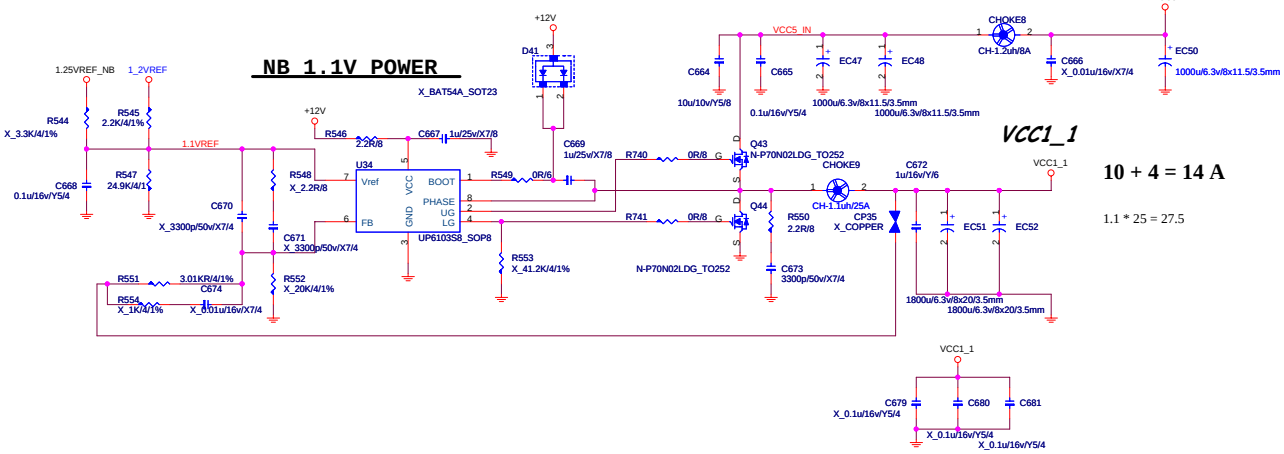


Figure 4-1 RD790 Power Rail Power Up Sequence

NB 1.1V POWER

[(((14 * 1.1)/5)*40)/0.8] = 154

5 * 8 * 0.8 = 32



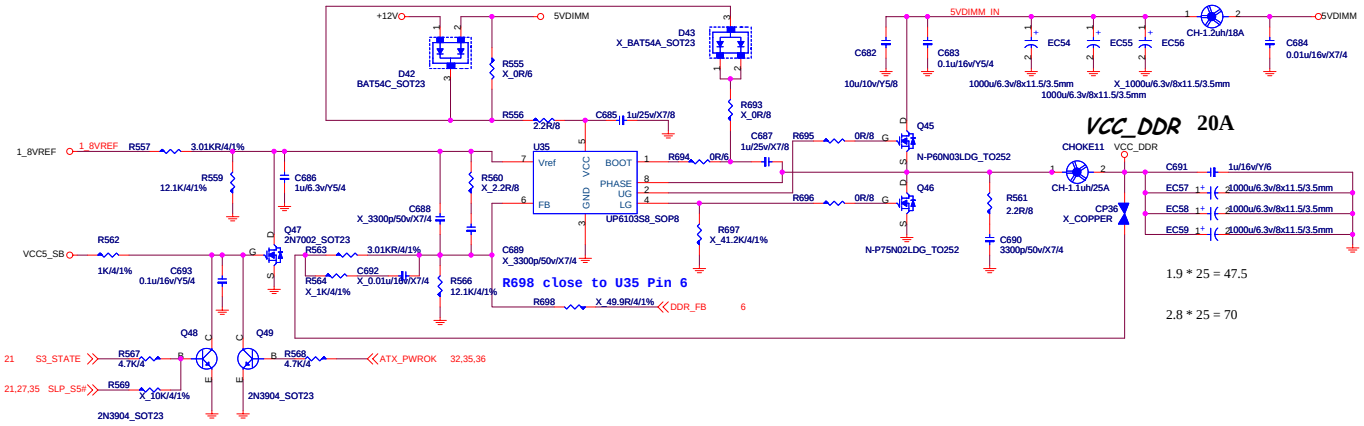
VCC1_1

10 + 4 = 14 A

1.1 * 25 = 27.5

DDR II 1.8V POWER

5 * 18 * 0.8 = 72



VCC_DDR 20A

1.9 * 25 = 47.5

2.8 * 25 = 70

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Document Number: MS-7501	
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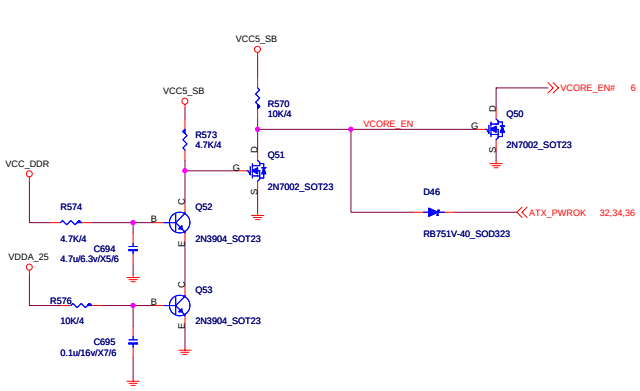
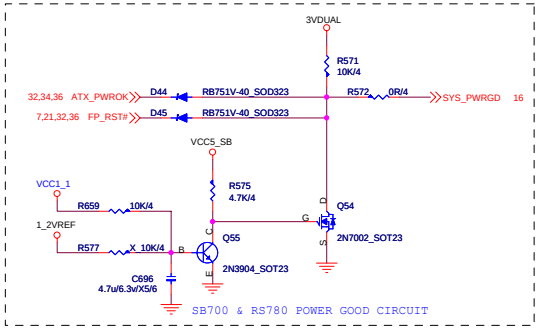




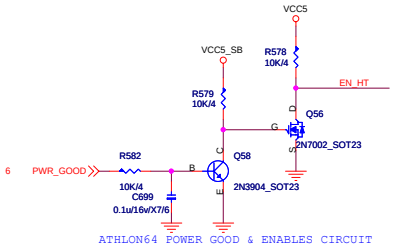


Table 15. Power Sequencing Group Definitions

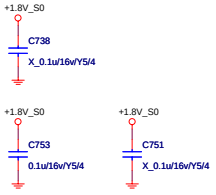
Power Group A		Power Group B	
VDDIO[1, 2]	Vcc_DDR	VDD[1:0][3]	Vcore
VTT[1, 2]	VTT	VDDNB	Vcore_NB
VDDA	VDDA25	VLDT	HT

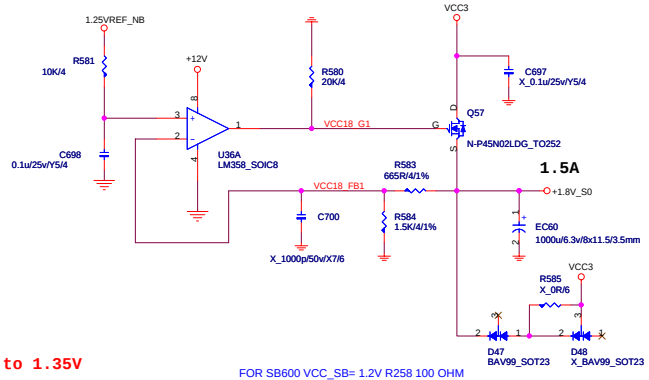
Notes:

1) *VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.*

2) *VDDIO and VTT only apply to DDR2 compatible processors.*

3) *VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.*

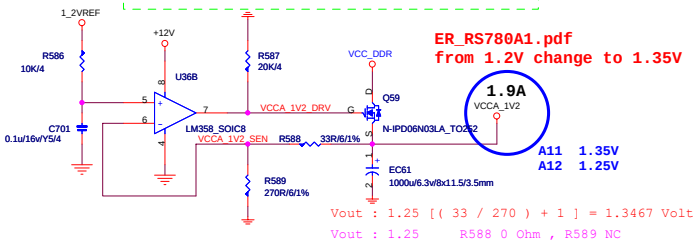


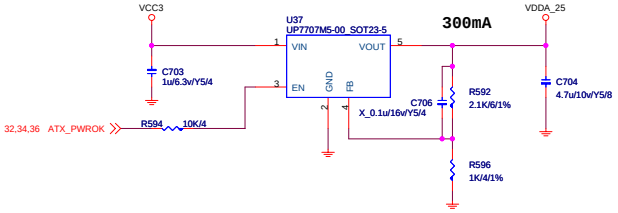


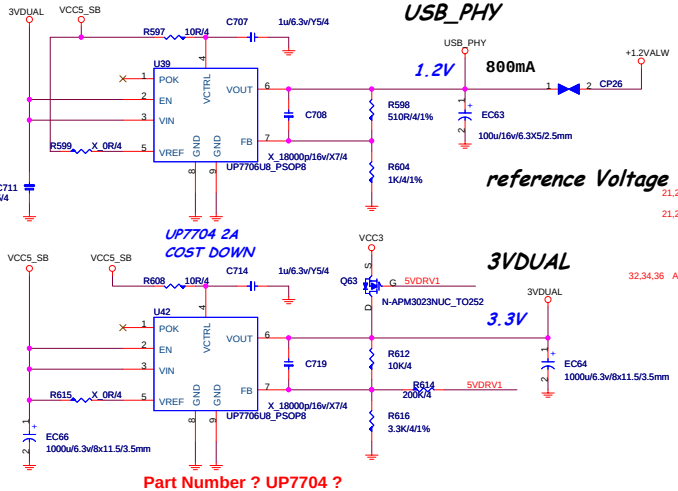
FOR SB600 VCC_SB= 1.2V R258 100 OHM

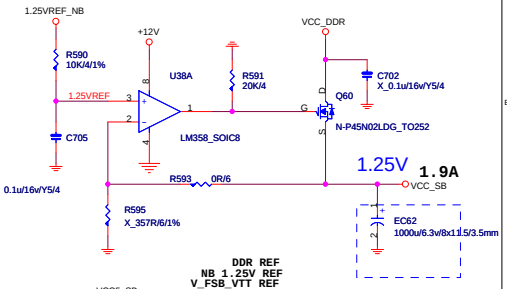
According to ER_RS780A1,increasing the north bridge VDDHTTX voltage from 1.2V to 1.35V helps to reduce the susceptibility and exposure to this problem.(This issue will be resolved in the A12 silicon revision.)

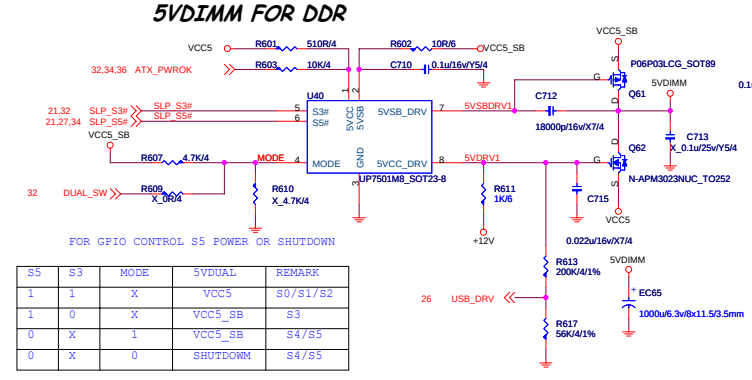
ER_RS780A1.pdf
from 1.2V change to 1.35V



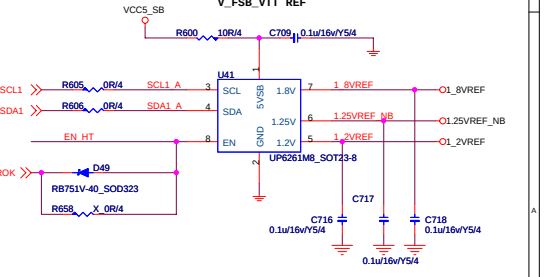








S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWM	S4/S5



ATX connector / Front Panel

Intel Front Panel

ESD Protect

R618 330R/4 3VDUAL
SATA_LED 20
PD_LED 33
D50 BAT54A_SOT23
C720 X_180p/50v/N/4
SUS_LED
PWR_LED
EMI
For MSI / Intel Front Panel
3VDUAL
C722 X_0.1u/25v/Y5/4
R621 33R/4
HDD+
HDD-
JFP1
HDD+ PLED
HDD- SLED
RESET- PWSW+
RESET+ PWSW-
NC
HEADER,2*5(10)_Yellow
PWR_LED
SUS_LED
PWSW-
PWSW+
R620 X_1K/4
R622 0R/4
R623 4.7K/4
C723 C724 X_0.1u/25v/Y5/4
EMI
Near Super I/O
PSIN
7,21,32,35 FP_RST#
R624 33R/4
RESET-
RESET+
R625 100R/4/1%
R650 100R/4
C729 0.1u/25v/Y5/4
C730 X_0.1u/25v/Y5/4
R626 X_10K/4
C731 X_0.1u/25v/Y5/4
EMI

PS2 KEYBOARD & MOUSE CONNECTOR

USB_1394
RN40 8P4R/4.7K/4
EC67 X_100u/16v/6.3X5/2.5mm
C721 X_0.1u/25v/Y5/4
R619 X_1K/4
JKBMS1
MSDATA FB17 300/600mA/B6
MSCLK FB18 300/600mA/B6
KBDATA FB19 300/600mA/B6
KBCLK FB20 300/600mA/B6
MS
KB
CONN-KB
C725 180p/50v/N/4
C728 180p/50v/N/4
C726 180p/50v/N/4
C727 180p/50v/N/4
CP29

BUZZER

VCC5
D51 X_1N4148S
BZ1 BUZZER
32 ALARM
R627 100R/8
SPK
21 SPKR
R628 2.2K/4
Q64 2N3904_SOT23
C736 0.1u/25v/Y5/4

ATX Connector

ATXPWR1
VCC3 C737 X_0.1u/25v/Y5/4
-12V C748 1000p/50v/X7/4
27,32 ATX_PSON# C750 1000p/50v/X7/4
C749 0.1u/25v/Y5/4
C752 0.1u/25v/Y5/4
EC68 1000u/6.3v/8x11.5/3.5mm
R629 10K/4
ATX_PWROK 32,34,35
VCC5_SB
C761 0.1u/25v/Y5/4
+12V
C762 X_0.1u/25v/Y5/4
C763 0.1u/25v/Y5/4
C764 0.1u/25v/Y5/4
PWRCONN24P_CREAM
3VDUAL C739 X_0.1u/16v/Y5/4

EMI solution

CP27
CP28
CP30
VCC3 C733 X_0.1u/16v/Y5/4
VCC5 C734 X_0.1u/25v/Y5/4
VCC5 C735 X_0.1u/25v/Y5/4
VCCP C740 X_0.1u/16v/Y5/4
VCC5 C741 C742 C743 C744 C745 C746 C747 X_0.1u/16v/Y5/4
VCC3 C756 C757 C758 C759 C760 X_0.1u/16v/Y5/4
VCC3 C754 VCC5 C755 X_0.1u/25v/Y5/4

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Title: ATX/Front Panel/KB/EMI	Rev: 0A
Document Number: MS-7501	
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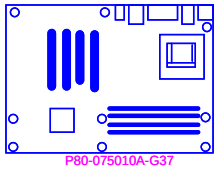
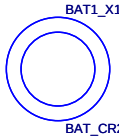
PCB

PCB1

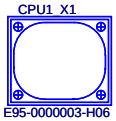


P80-075010A-G37

BATTERY



CPU RM



PCB : 2116

P80-075010A-G37
P80-075010A-E55

U10 & U13 new version (Part number) ?

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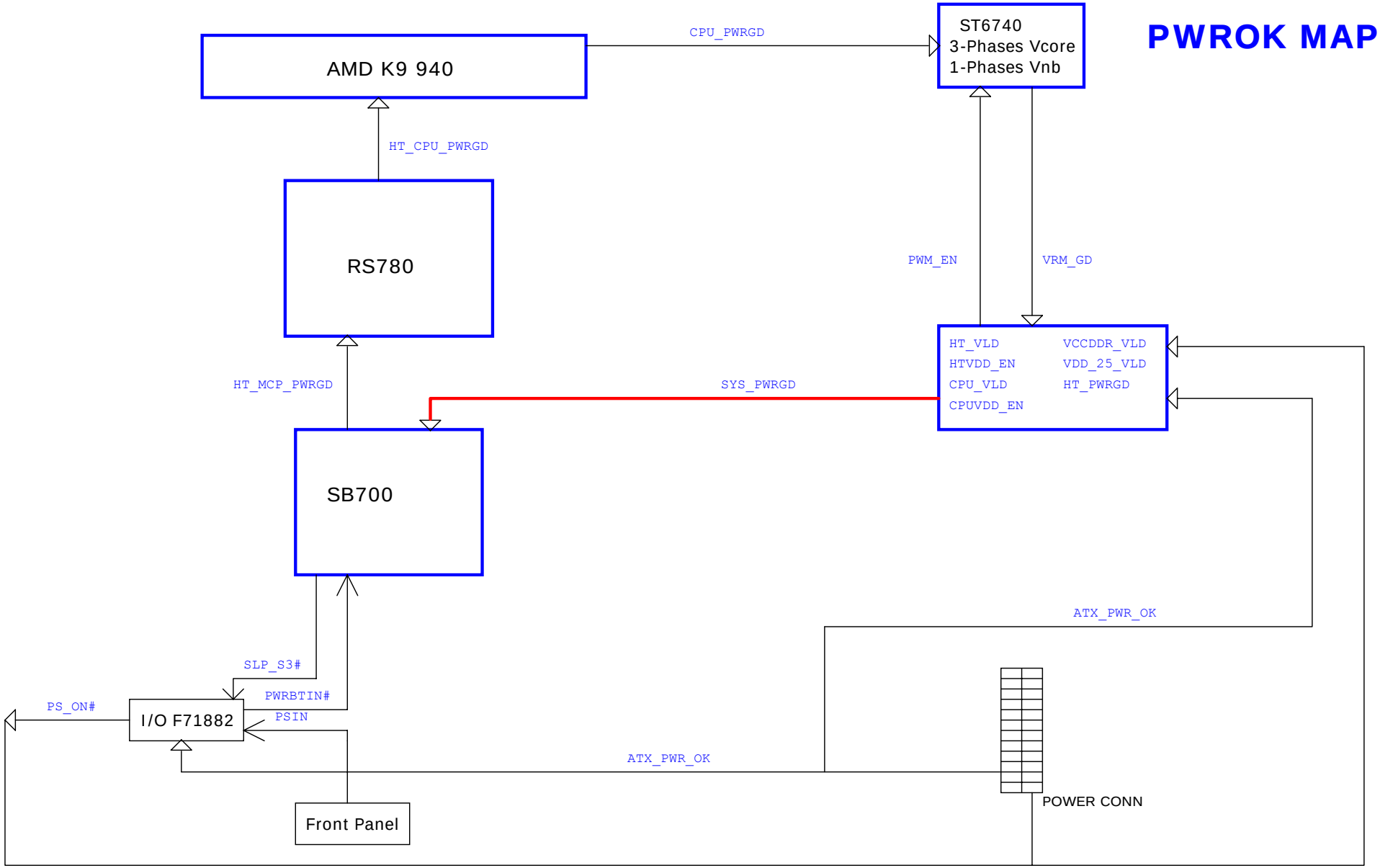
PWROK MAP



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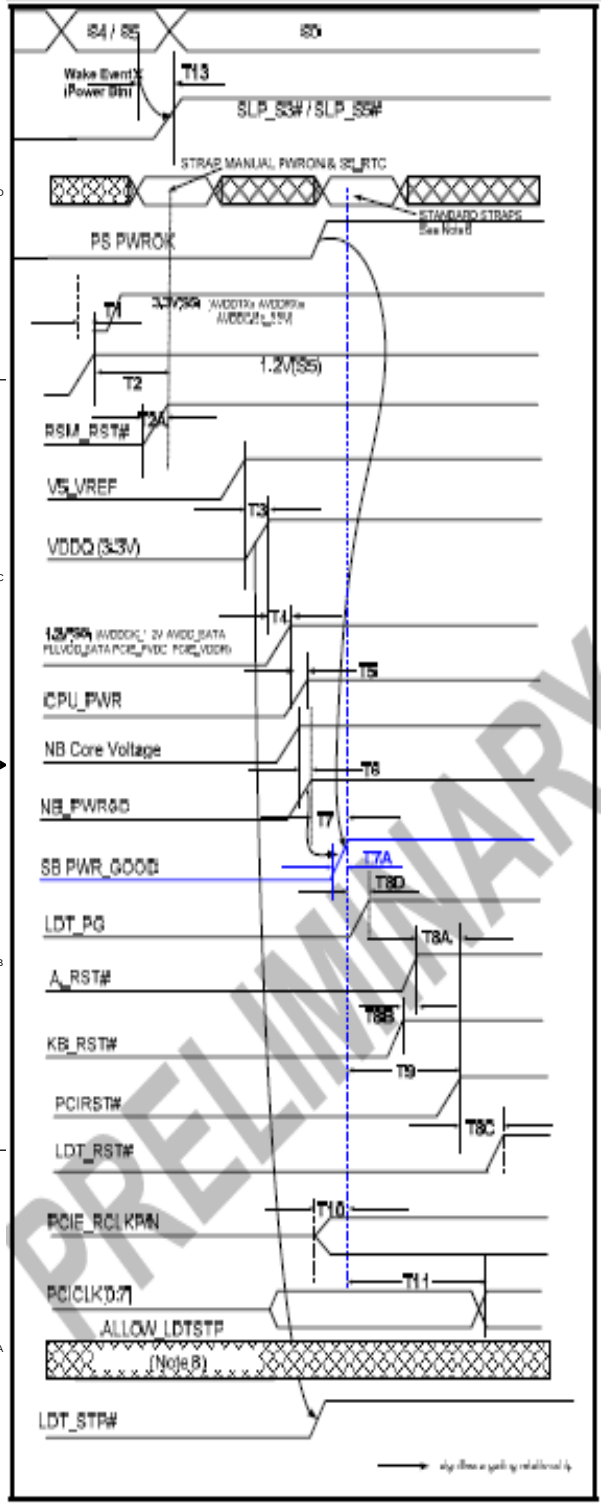

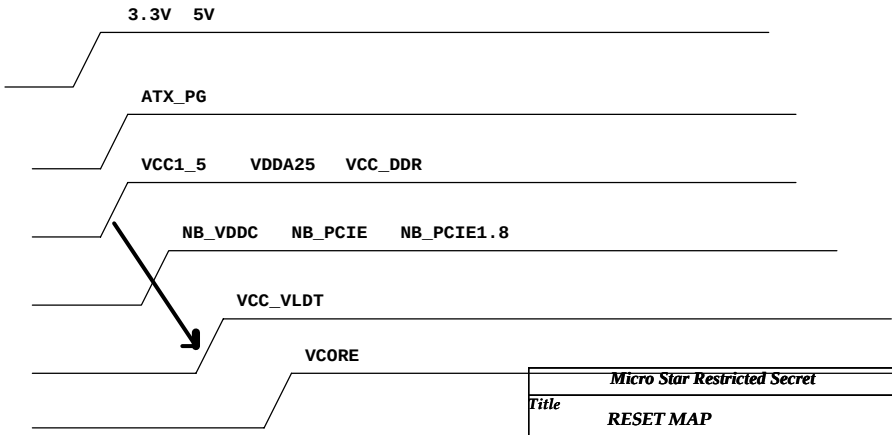

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Title RESET MAP	Rev 0A
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