MS-7500 0C BTX(264.16mm X 266.4mm)

CPU:

AMD AM2R2+ Socket940

System Chipset:

North Bridge --- AMD-ATI RX780/RS780

South Bridge --- AMD-ATI SB700

OnBoard Chipset:

Clock Gen:Seligo P625

AZALIA Codec:ADI1884

LAN(PHY):BOARDCOM 5754 (5764)

SIO:SMSC 5327

Flash ROM: 32 MB SPI (CHIP)

Main Memory:

DDRII (667/800MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 1

PWM:

Controller:ISL6323 (4-Phase 89W)

ACPI:

INTERSIL 6545

Other:

FDD *1
SATA(SATA2-300MB/s) *4
USB2.0 *10 (Rear*6 Front*4)
DVI*1
VGA PORT *1
PRINT Header *1
TPM *1
COM PORT *1
COM Header *1

<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	Cover Sheet	
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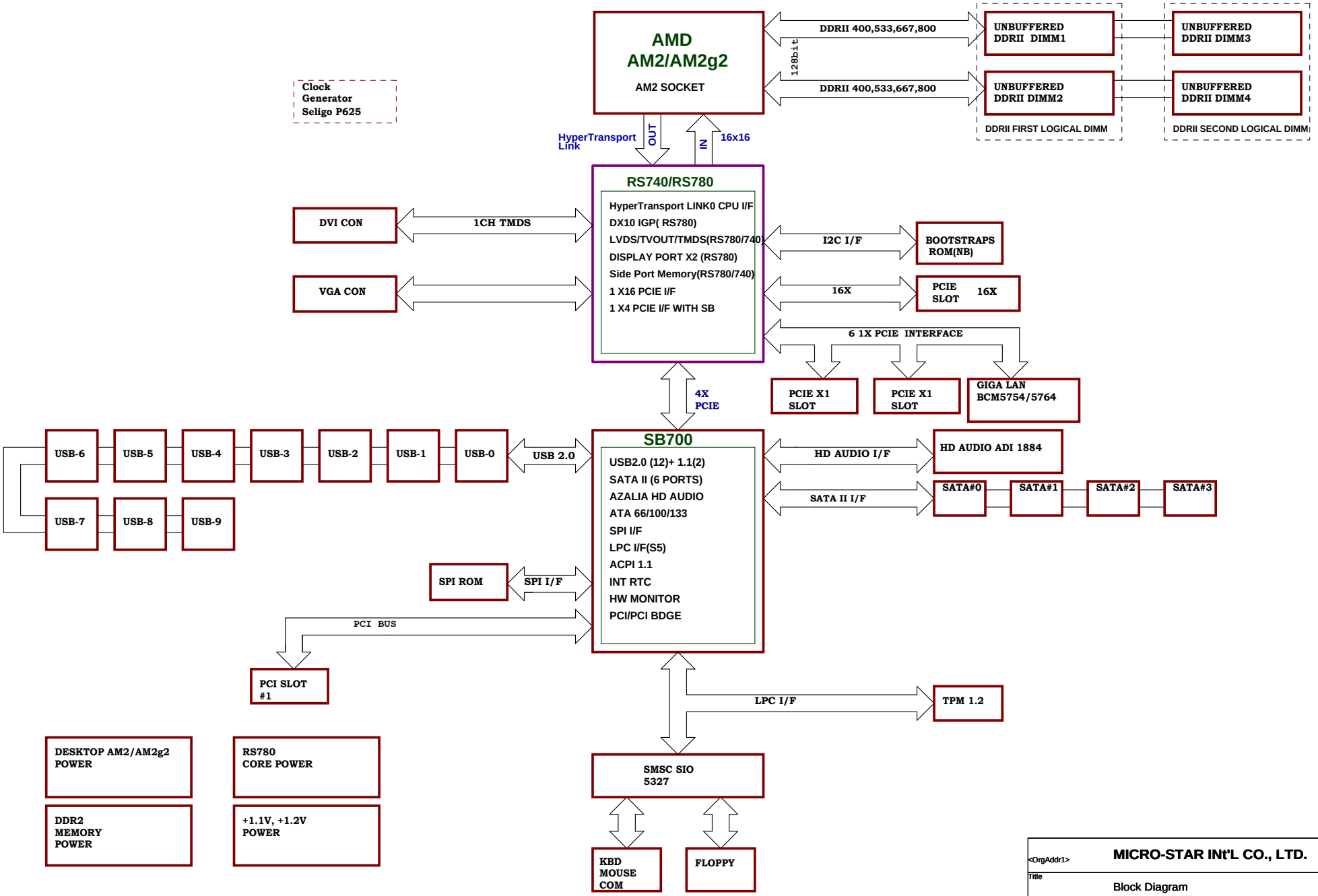
RX780/RS780 + SB700 CUSTOMER DESKTOP REFERENCE DESIGN



<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	Block Diagram	
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MA0_CLK_H0/L0 MEM_MA0_CLK_H1/L1 MEM_MA0_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MB0_CLK_H0/L0 MEM_MB0_CLK_H1/L1 MEM_MB0_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	QUAD STACK	USB0- USB0+ USB1- USB1+ USB2- USB2+ USB3- USB3+	USB_OC#0 (OC#0~1)
	LAN_USB1	USB4- USB4+ USB5- USB5+	USB_OC#1 (OC#2)
Front	FRONT USB	USB6- USB6+ USB7- USB7+	USB_OC#2 (OC#3)
	MEDIA CARD READER	USB8- USB8+ USB9- USB9+	USB_OC#3 (OC#4)

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD20	PCICLK2_SLOT1 (PCICLK2)
TPM				LPCCLK0
SIO				LPCCLK1

PCI RESET DEVICE

SB 700	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

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TABLE 37
SIO8 GPIO ASSIGNMENTS

SIO GPIO	Function	Comment
GP 11	CHAFAN_PWM	Chassis Fan PWM command input, install 1K PU to +3.3 V
GP 12	RC_ID	Multi-state GPIO
GP 13	PME#	PME# from PCI slots.
GP 14	SMB Data Main	
GP 15	3V_SW_AUX	3V DUAL control
GP 16	WAKE#	PCI Express WAKE#, 1K PU to +3.3 V SB
GP 17	SMB_CLK_M	SMBus clock main
GP 21	DIAG_BEEP	Diagnostic beep signal; route to internal speaker amplifier
GP 22	CPUFAN_PWM	CPU Fan PWM command input, install 1K PU to +3.3 V
GP 23	**AUDIO_AMP_DIS#**	**To disable internal speaker.**

SIO GPIO	Function	Comment
GP 24	~~HOOD_SW_DET~~	~~Intrusion Switch Dotect. Route to P125.1. Add 8.2K pullup to +3.3 V.~~
GP 25	~~HOOD_SENSE#~~	~~1M PU to SIO_BAT.~~
GP 26	SKTOCC#	Route to SKTOCC# on CPU, install 10M PU to BATT, CPU occupied signal
GP 27	WAKE_OUT#	Wake Disable Output.
GP 30	LED_COLOR	Route to P5.4, front LED/button header, power LED driver
GP 31	LED_BLINK	Route to P5.2, front LED/button header, power LED driver
GP 32	TRMTRIP#	Route to Thermtrip# voltage translation, 8.2K PU to +3.3 V, CPU shutdown
GP 33	HD_LED_IN#	Route to Hard Drive LED control circuilt.
GP 36	SMBCLK_THERM	SMB clock for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 37	SMBDATA_THERM	SMB data for sensor bus for fan sense chip; 4.7K PU to + 3.3 V SB
GP 40	DENSEL#	Route to P10.2, floppy connector
GP 41	HD_LED_OUT#	Hard drive LED output
GP 42	RING#	Power management output to Southbridge RI# input, 8.2K PU to +3.3 V SB
GP 43	SMB_CLK_R	SMBus clock resume
GP 44	~~HOOD_LOCK#~~	~~Route to R124.1, install 2.2K pullup to +5 V~~
GP 45	~~HOOD_UNLOCK#~~	~~Route to R124.6, install 2.2K pullup to +5 V~~
GP 46	LPC_SMI#	LPC SMI output to Southbridge, install 8.2K pull up to +3.3 V SB
GP 50	RI2#	Route to 2nd serial port RI# pin.
GP 51	DCD2#	Route to 2nd serial port DCD# pin.
GP 52	RXD2	Route to 2nd serial port RxDAT pin.
GP 53	TXD2	Route to 2nd serial port TxDAT pin.
GP 54	DSR2#	Route to 2nd serial port DSR# pin.
GP 55	RTS2#	Route to 2nd serial port RTS# pin.
GP 56	CTS2#	Route to 2nd serial port CTS# pin.
GP 57	DTR2#	Route to 2nd serial port DTR# pin.
GP 60	CLAMP_CTRL	Clamp Control Signal. Route to power bleed off transistors.
GP 61	SIO_PCIE_RST#	Reset; route to PCI Express X1 and x16 slots
GP 62	PWRBTN_IN#	Front panel power button input
GP 63	SLP_S3#	Connected to S3 sleep input from Southbridge
GP 64	SLP_S4#	Connected to SLP_S4# (not S5) sleep input from Southbridge
GP 66	PWRBTN_OUT#	Route to Southbridge PWRBTN# input
GP 67	PSON#	Power supply main voltage control; route to P1. 16, install 2.2K PU to +5 VAUX
GP 70	USB_PWR#	Connected to SLP_S5#
GP 71	SMB DATA Resume	
GP 72	5V_DUAL_Control	Controls aux voltage FET on 5V_DUAL circuit
GP 73	CHAFAN2_TACH	Power supply tach input; 4.7K PU to +3.3 V
GP 74	CHAFAN2_PWM	Power supply PWM command input; 1K PU to +3.3 V
GP 75	PWRGD_30MS	Power Good delayed 30 ms. 1K PU to + 3 V SB
GP 76	PWRGD_50MS#	Inverted Power Good delayed 50 ms. 1K PU to + 3 V SB
GP 85	CPUFAN_TACH	Tach input from CPU fan connector, 4.7K PU to +3.3 V

ATI SB700 GPIO Matrix

		Pin Capabilities					Pin Defaults			BIOS Assignments				
Pin	GPIO	Alternate Functions	Strapping Funtion / Internal PU or PD	Input/ Output	Power Well	Voltage Tolerance	Default Signal Definition	Default Buffer Type	Default Output Level	Function	Input/ Output	Output Level	Motherboard Function	Implementaion Notes
A27	GPIO 0	#		I/O/D	Vcc3_3	5		I		GPIO 0	I		BRD_ID0	
A25	~~GPIO 1~~	~~ROM_CS#~~		I/O	Vcc3_3	5		I		GPIO 1	I			
B26	GPIO 2	SPKR		I/O	Vcc3_3	5		I		SPKR	O		SB600 SPKR OUT	
M4	GPIO 3	FANOUT0		I/O	Vcc3_3	5		I		GPIO 3	I		PROCHOT2_SB	
B27	GPIO 4	SMARTVOLT/SATA_IS2#		I/O	Vcc3_3	5		TRI-STATE		GPIO 4	I		BRD_REV0	
D23	GPIO 5	SHUTDOWN#		I/O	Vcc3_3	5		TRI-STATE		GPIO 5	I		BRD_REV1	
B29	GPIO 6	GHI#/SATA_IS1#		I/OD	Vcc3_3	5		TRI-STATE		GPIO 6	I		CHASSIS_ID0	
A23	GPIO 7	~~WD_PWRGD~~		I/O	Vcc3_3	5		TRI-STATE		GPIO 7	I			
C26	GPIO 8	DDC1_SDA		I/O	Vcc3_3	5		TRI-STATE		GPIO 8	I		CHASSIS_ID2	
D26	GPIO 9	DDC1_SCL		I/O	Vcc3_3	5		TRI-STATE		GPIO 9	1		BRD_ID1	
C28	GPIO 10	SATA_IS0#		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 10	I		CHASSIS_ID1	
J6	GPIO 11	SPI_DO		I/O	VccSUS3	3.3		TRI-STATE		SPI_DO	O		SPI DATA-OUT	
J3	GPIO 12	SPI_DI		I/O	VccSUS3	3.3		TRI-STATE		SPI_DI	I		SPI DATA-IN	
C23	GPIO 13	LAN_RST#		OD	Vcc3_3	5		O						
05	GPIO 14	ROM_RST#		I/O	Vcc3_3	5		O		ROM_RST#	O		LPC ROM RST#	
AD28	GPIO 15	IDE_D0		I/O	Vcc3_3	5		TRI-STATE		IDE_D0	I/O		IDE_D0	
AD26	GPIO 16	IDE_D1		I/O	Vcc3_3	5		TRI-STATE		IDE_D1	I/O		IDE_D1	
AE29	GPIO 17	IDE_D2		I/O	Vcc3_3	5		TRI-STATE		IDE_D2	I/O		IDE_D2	
AF27	GPIO 18	IDE_D3		I/O	Vcc3_3	5		TRI-STATE		IDE_D3	I/O		IDE_D3	
AG29	GPIO 19	IDE_D4		I/O	Vcc3_3	5		TRI-STATE		IDE_D4	I/O		IDE_D4	
AH28	GPIO 20	IDE_D5		I/O	Vcc3_3	5		TRI-STATE		IDE_D5	I/O		IDE_D5	
AJ28	GPIO 21	IDE_D6		I/O	Vcc3_3	5		TRI-STATE		IDE_D6	I/O		IDE_D6	
AJ27	GPIO 22	IDE_D7		I/O	Vcc3_3	5		TRI-STATE		IDE_D7	I/O		IDE_D7	
AH27	GPO 23	IDE_D8		I/O	Vcc3_3	5		TRI-STATE		IDE_D8	I/O		IDE_D8	
AG27	GPIO 24	IDE_D9		I/O	Vcc3_3	5		TRI-STATE		IDE_D9	I/O		IDE_D9	
AG28	GPIO 25	IDE_D10		I/O	Vcc3_3	5		TRI-STATE		IDE_D10	I/O		IDE_D10	
AF28	GPIO 26	IDE_D11		I/O	Vcc3_3	5		TRI-STATE		IDE_D11	I/O		IDE_D11	
AG29	GPIO 27	IDE_D12		I/O	Vcc3_3	5		TRI-STATE		IDE_D12	I/O		IDE_D12	
AE28	GPIO 28	IDE_D13		I/O	Vcc3_3	5		TRI-STATE		IDE_D13	I/O		IDE_D13	
AD25	GPIO 29	IDE_D14		I/O	Vcc3_3	5		TRI-STATE		IDE_D14	I/O		IDE_D14	
AD29	GPIO 30	IDE_D15		I/O	Vcc3_3	5		TRI-STATE		IDE_D15	I/O		IDE_D15	
G2	GPIO 31	SPI_HOLD#		I/O	VccSUS3	3.3		TRI-STATE		SPI_HOLD#	O		SPI HOLD#	
G6	GPIO 32	SPI_CS#		I/O	VccSUS3	3.3		TRI-STATE		SPI_CS#	O		SPI CHIP SELECT#	
AD3	GPIO 33	INTE#		I/O	Vcc3_3	5		TRI-STATE		INTE#			PCI INTE#	To PCI slots J21 & J22.
AF1	GPIO 34	INTF#		I/O	Vcc3_3	5		TRI-STATE		INTF#			PCI INTF#	To PCI slots J21 & J22.
AF4	GPIO35	INTG#		I/O	Vcc3_3	5		TRI-STATE		INTG#			PCI INTG#	To PCI slots J21 & J22.
AF3	GPIO36	INTH#		I/O	Vcc3_3	5		TRI-STATE		INTH#			PCI INTH#	To PCI slots J21 & J22.
B24	~~GPIO37~~	~~DPSLP_OD#~~	Open drain. Requires external pullup to Vcc3_3.	I/O	Vcc3_3	5		TRI-STATE						
L1	~~GPIO38~~	~~AC_BITCLK~~		I/O	Vcc3_3	5		I						
L2	GPIO39	AC_SDOUT	STRAP: High=enable debug straps, low=use hardcoded defaults.	I/O	Vcc3_3	5		O						
M3	GPIO40	CLK_REQ2#/SATA_IS5		I/O	Vcc3_3	5		I		GPIO 40	I		PRT_DET#	
T1	GPIO41	PCICLK5		I/O	Vcc3_3	5		O						
L4	GPIO42	AZ_SDIN0		I/O	VccSUS3	3.3		I						
J2	GPIO43	AZ_SDIN1		I/O	VccSUS3	3.3		I						
J4	GPIO44	AZ_SDIN2		I/O	VccSUS3	3.3		I						
L5	~~GPIO45~~	~~AC_RST#~~		I/O	VccSUS3	3.3		O		GPIO 45	O			
K2	GPIO46	AZ_SDIN3		I/O	Vcc3_3	5		I		ACZ_SDIN3	I		AZALIA AUDIO IN	
G3	GPIO47	SPI_CLK		I/O	VccSUS3	3.3		O		SPI_CLK	O		SPI CLOCK	
T3	GPIO 48	FANOUT1		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 48	I		COMM_B_DET#	
V4	GPIO 49	FANOUT2		I/O	Vcc3_3	3.3		TRI-STATE		GPIO 49	I		FRONT_AUD_DET#	
N3	GPIO 50	FANIN0		I/O	Vcc3_3	3.3		TRISTATE		GPIO 50	I		FRONT_USB_DET#	
P2	GPIO 51	FANIN1		I/O	Vcc3_3	3.3		TRISTATE		GPIO 51	I		FLASH_SEC_OVERRIDE	
W4	GPIO 52	FANIN2		I/O	Vcc3_3	3.3		TRISTATE		GPIO 52	I		PASSWORD_ENABLE	
V5	GPIO 53	VIN0		I/O	Vcc3_3	3.3		TRISTATE		GPIO 53	I		BOOT_BLOCK_ENAB	
L7	GPIO 54	VIN1		I/O	Vcc3_3	3.3		TRISTATE		GPIO 54	I		BOOT_BLOCK_RECOVERY#	
M8	GPIO 55	VIN2		I/O	Vcc3_3	3.3		TRISTATE		GPIO 55			BRD_ID2	
V6	GPIO 56	VIN3		I/O	Vcc3_3	3.3		TRISTATE						
M6	GPIO 57	VIN4		I/O	Vcc3_3	3.3		TRISTATE						
P4	GPIO 58	VIN5		I/O	Vcc3_3	3.3		TRISTATE						
M7	GPIO 59	VIN6		I/O	Vcc3_3	3.3		TRISTATE						
V7	GPIO 60	VIN7		I/O	Vcc3_3	3.3		TRISTATE						
P7	GPIO 61	TEMPIN0		I/O	Vcc3_3	3.3		TRISTATE						
P8	GPIO 62	TEMPIN1		I/O	Vcc3_3	3.3		TRISTATE						
T8	GPIO 63	TEMPIN2		I/O	Vcc3_3	3.3		TRISTATE						
T7	GPIO 64	TEMPIN3/TALERT#		I/O	Vcc3_3	3.3		TRISTATE						
W22	GPIO 65	BMREQ#/REQ5#		I/O	Vcc3_3	3.3		TRISTATE		BMREQ#	I			
A4	GPIO 66	LLB#		I/O	VccSUS3	3.3		TRISTATE						
AC12	GPIO 67	SATA_ACT#		I/O	Vcc3_3	3.3		TRISTATE		SATA_ACT	O		SATA LED	
AH26	GPIO 68	LDRQ1#/GNT5#		I/O	Vcc3_3	5		TRISTATE		LDRQ1#	I			
F5	GPIO 69	RTC_IRQ#		I/O	VccSUS3_3VBAT	3.3		O						
AH8	GPIO 70	REQ3#		I/O	Vcc3_3	5		TRISTATE						
AH5	GPIO 71	REQ4#		I/O	Vcc3_3	5		TRISTATE						
AB12	GPIO 72	GNT3#		I/O	Vcc3_3	5		O						
AG4	GPIO 73	GNT4#		I/O	Vcc3_3	5		O						

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Title: GPIO Table

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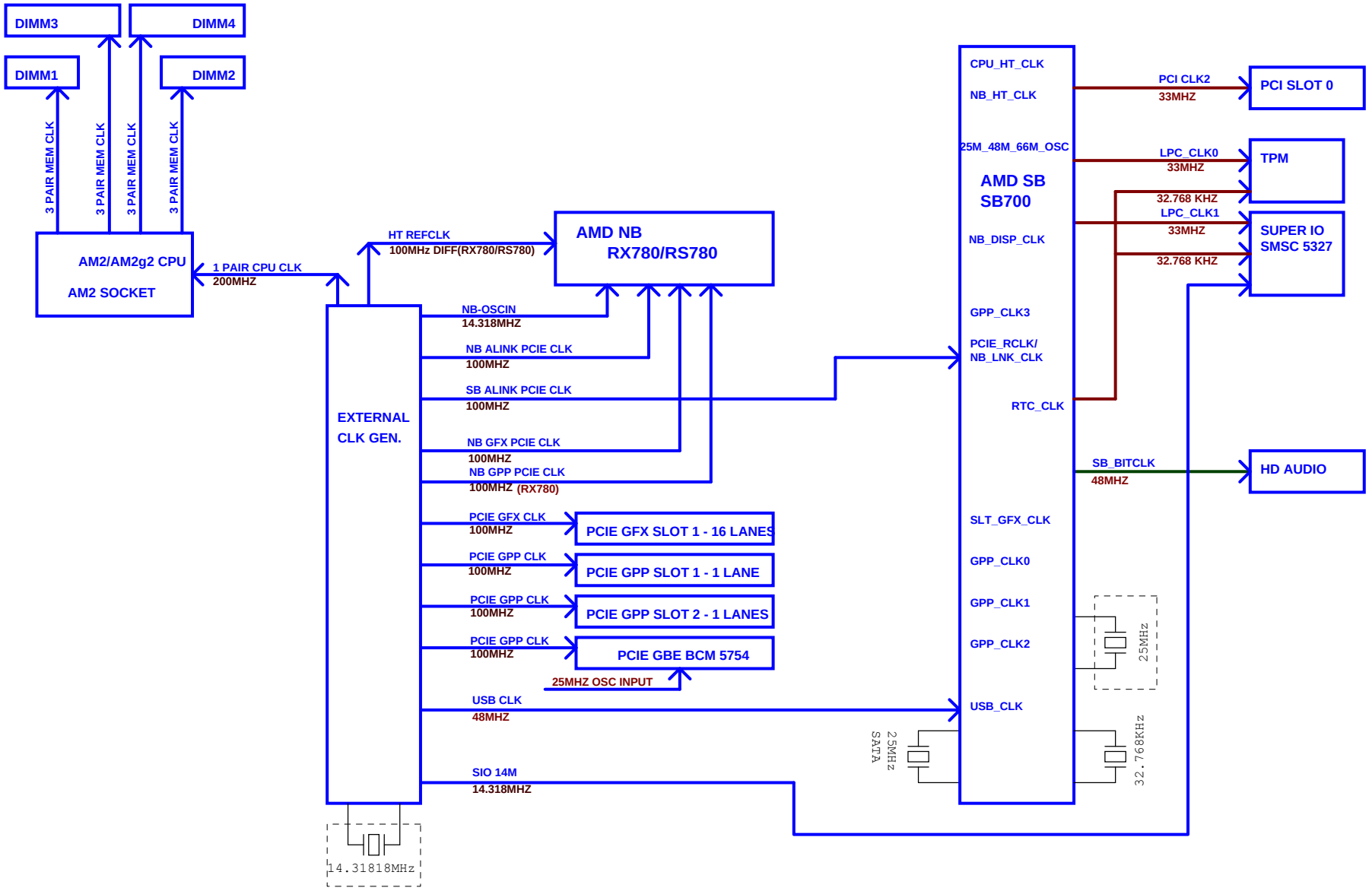

External clock mode

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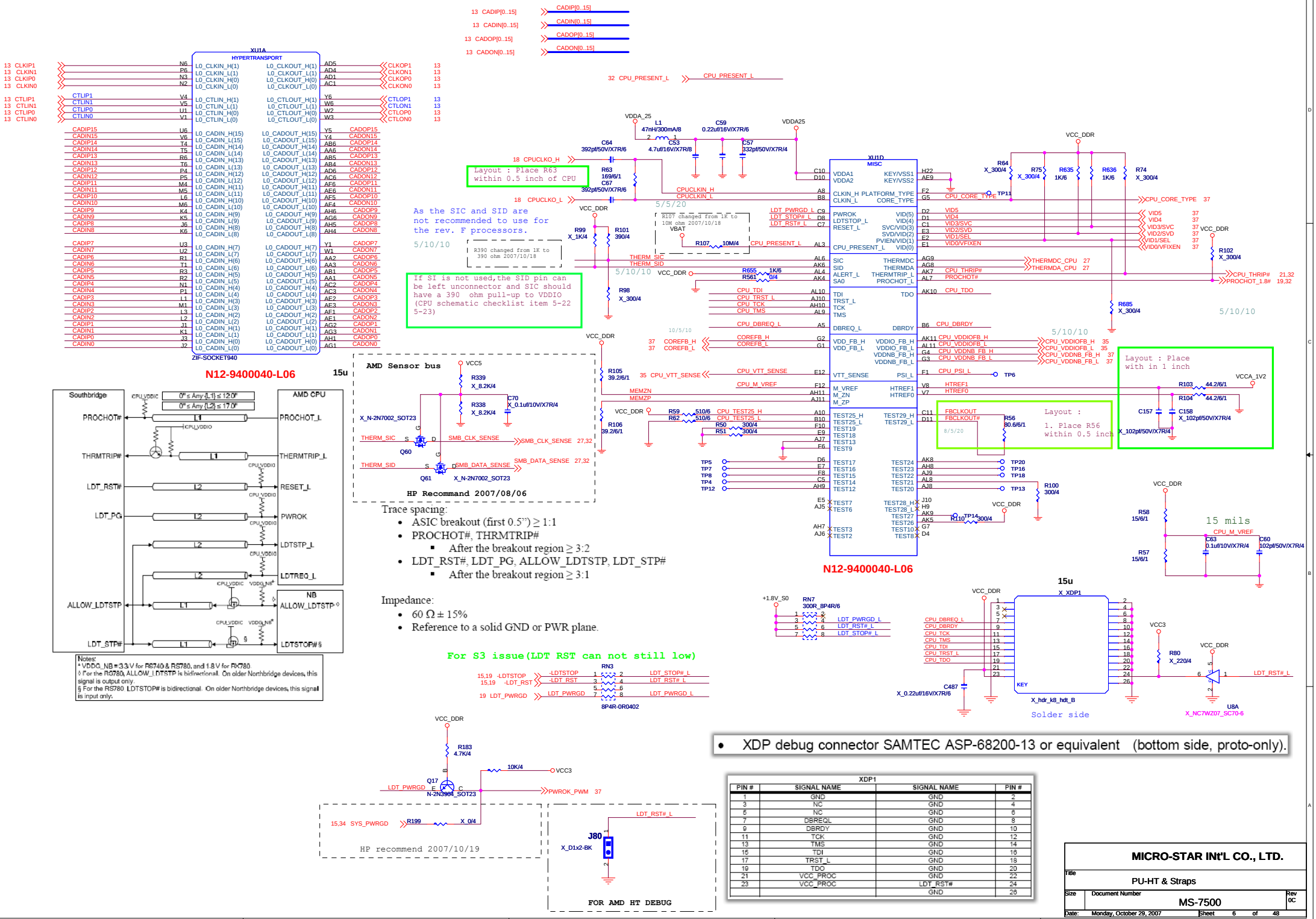
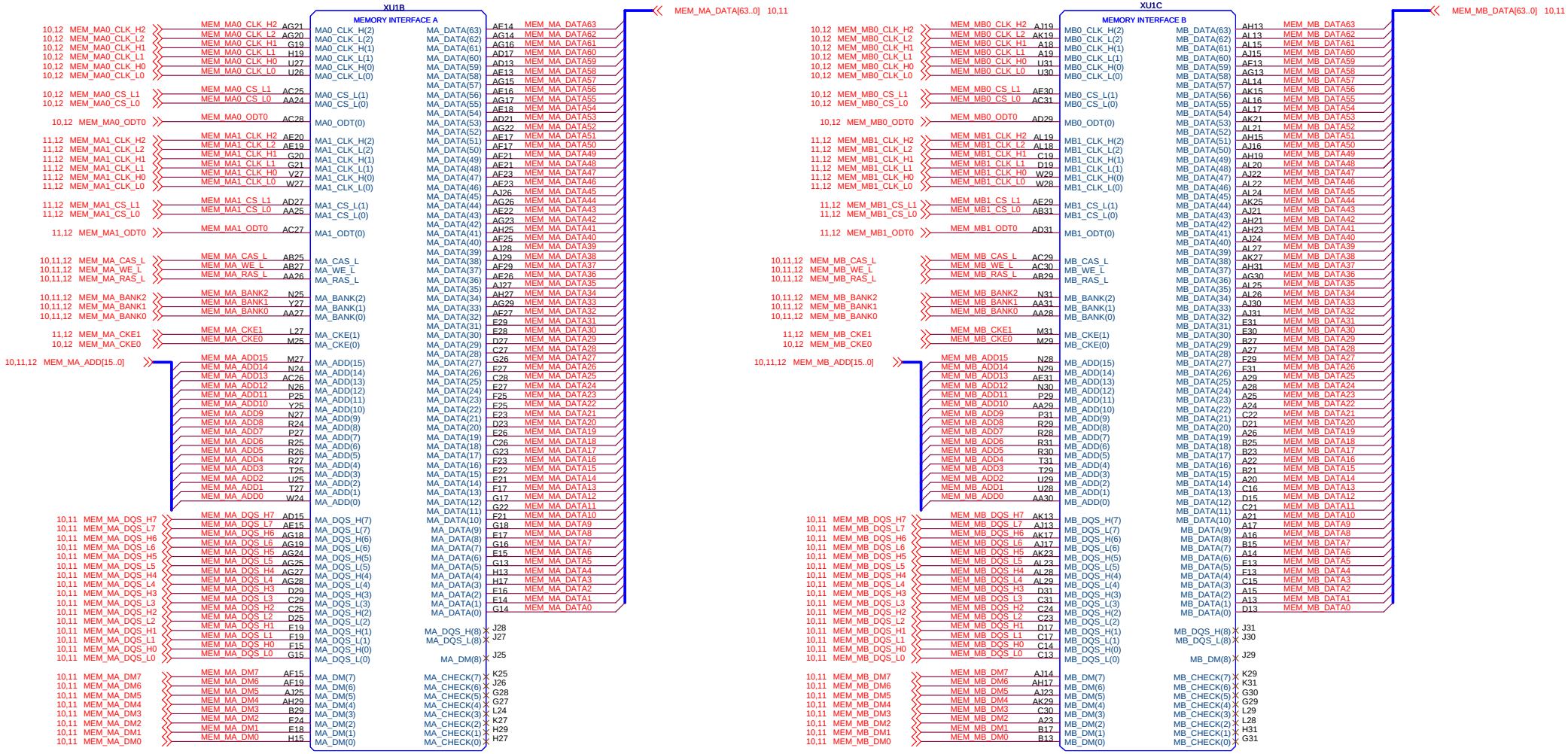


XDP1			
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	GND	GND	2
3	NC	GND	4
5	NC	GND	6
7	DBREQL	GND	8
9	DBRDY	GND	10
11	TCK	GND	12
13	TMS	GND	14
15	TDI	GND	16
17	TRST_L	GND	18
19	TDO	GND	20
21	VCC_PROC	GND	22
23	VCC_PROC	LDT_RST#	24
		GND	26



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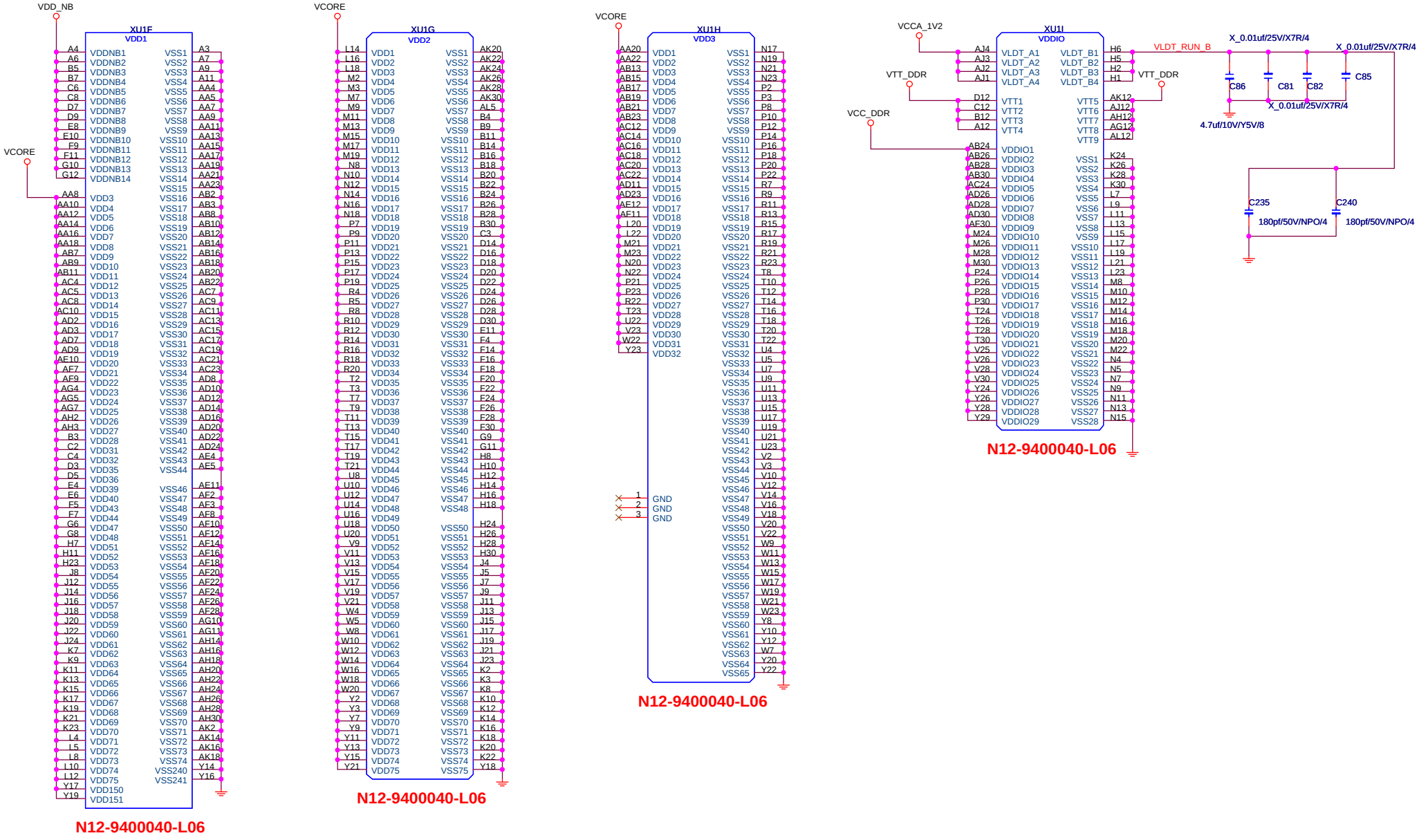

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Title: CPU-Power & GND		
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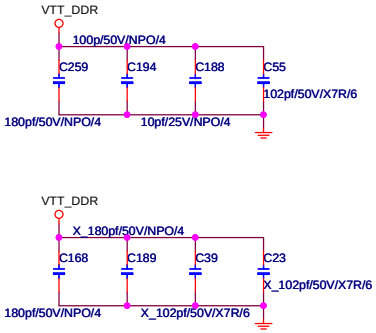
VTT_DDR-Decoupling



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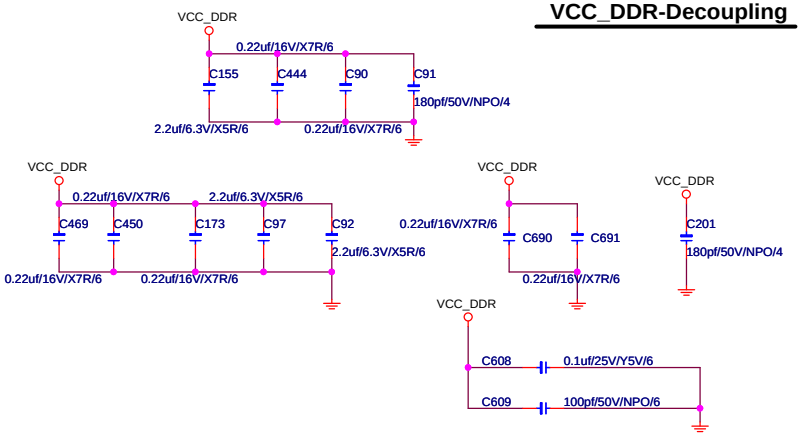
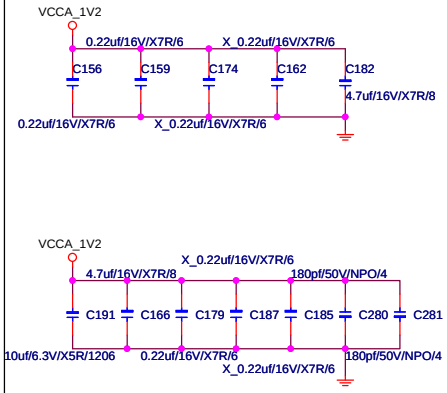
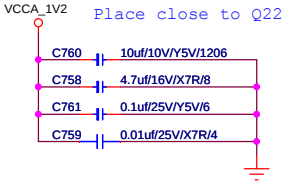
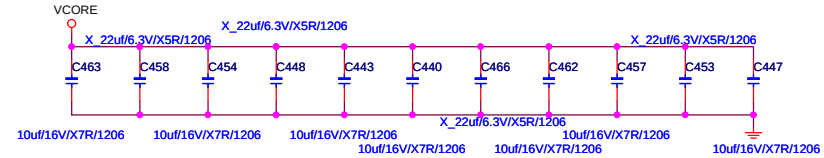


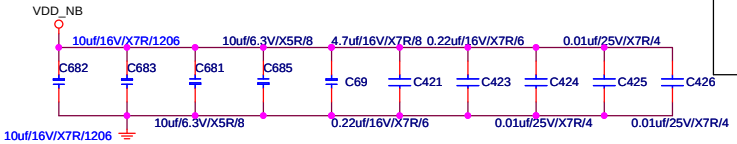
VCCA_1V2-Decoupling

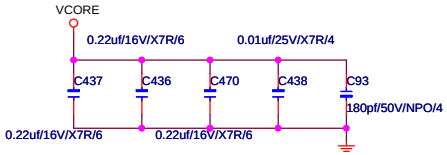


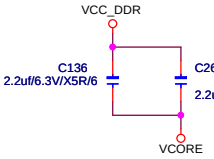


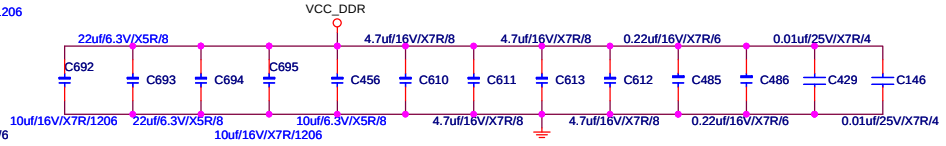
VCORE-Decoupling

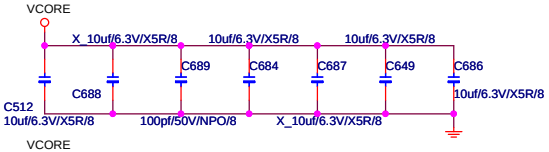


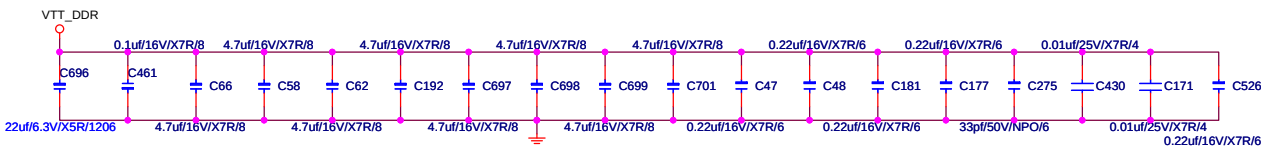


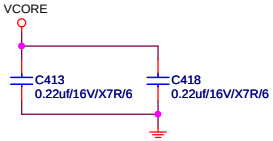


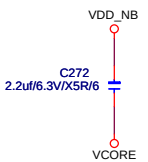


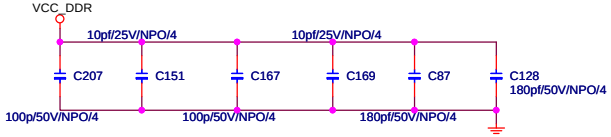


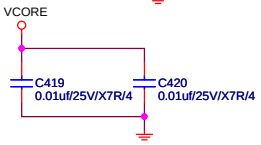


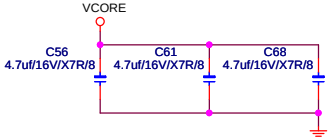






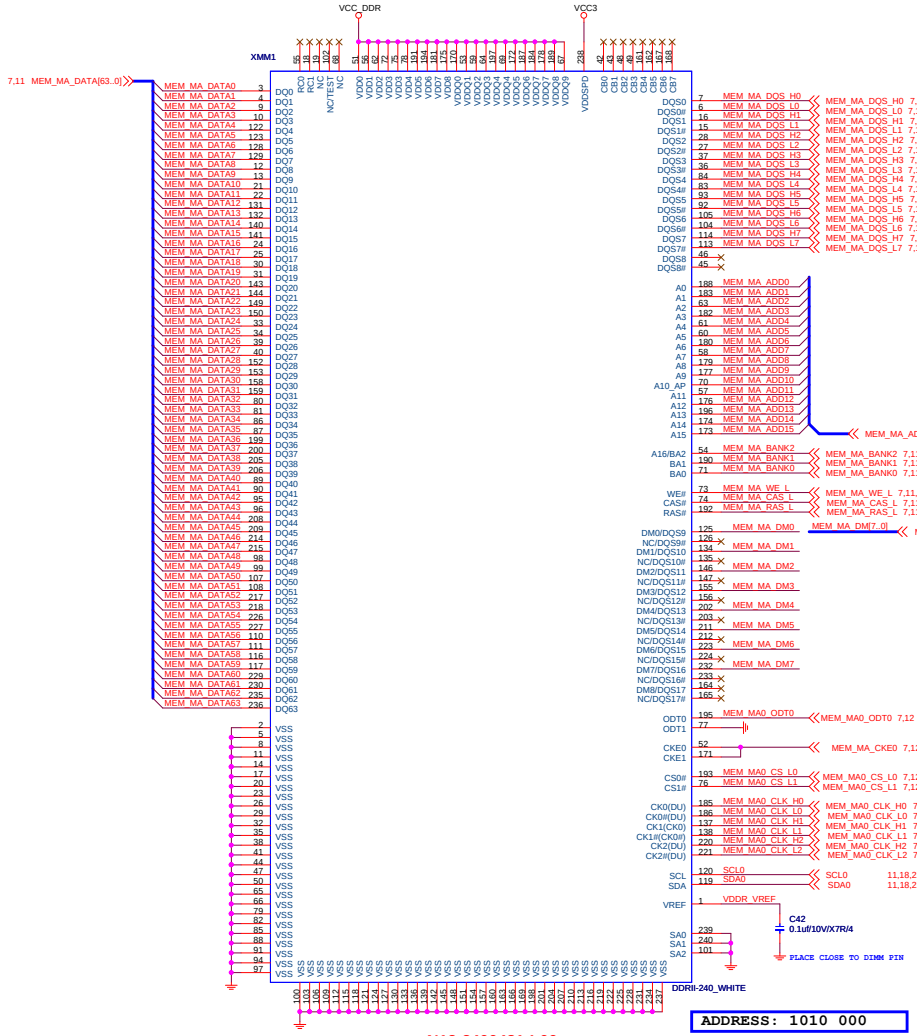






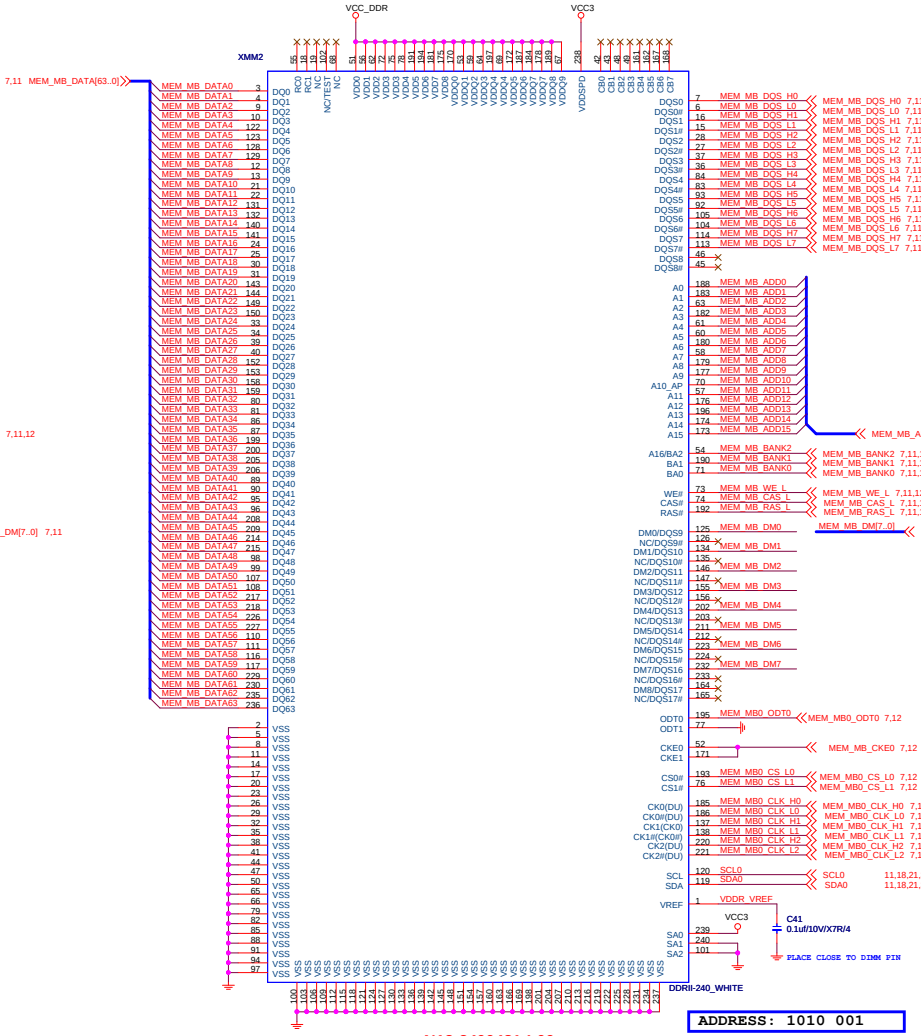
MICRO-STAR INt'L CO., LTD.

Title	CPU-Decoupling	
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 9 of 48	



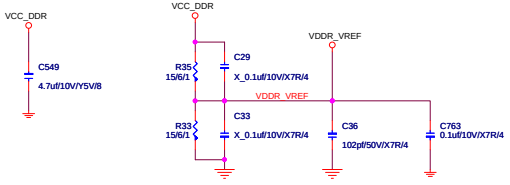
N13-2400481-L06

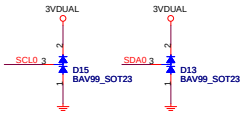
WHITE COLOR



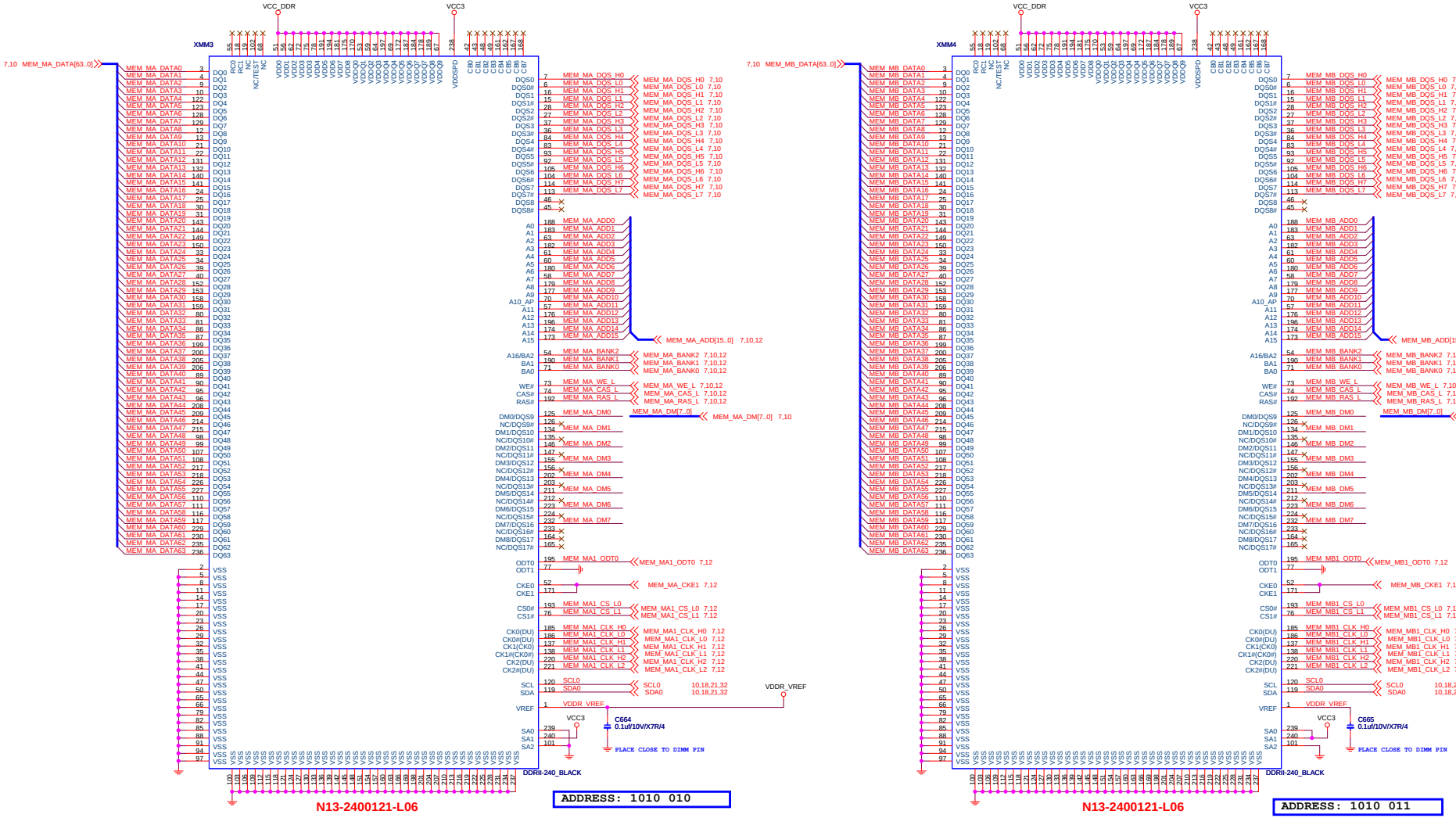
N13-2400481-L06

WHITE COLOR

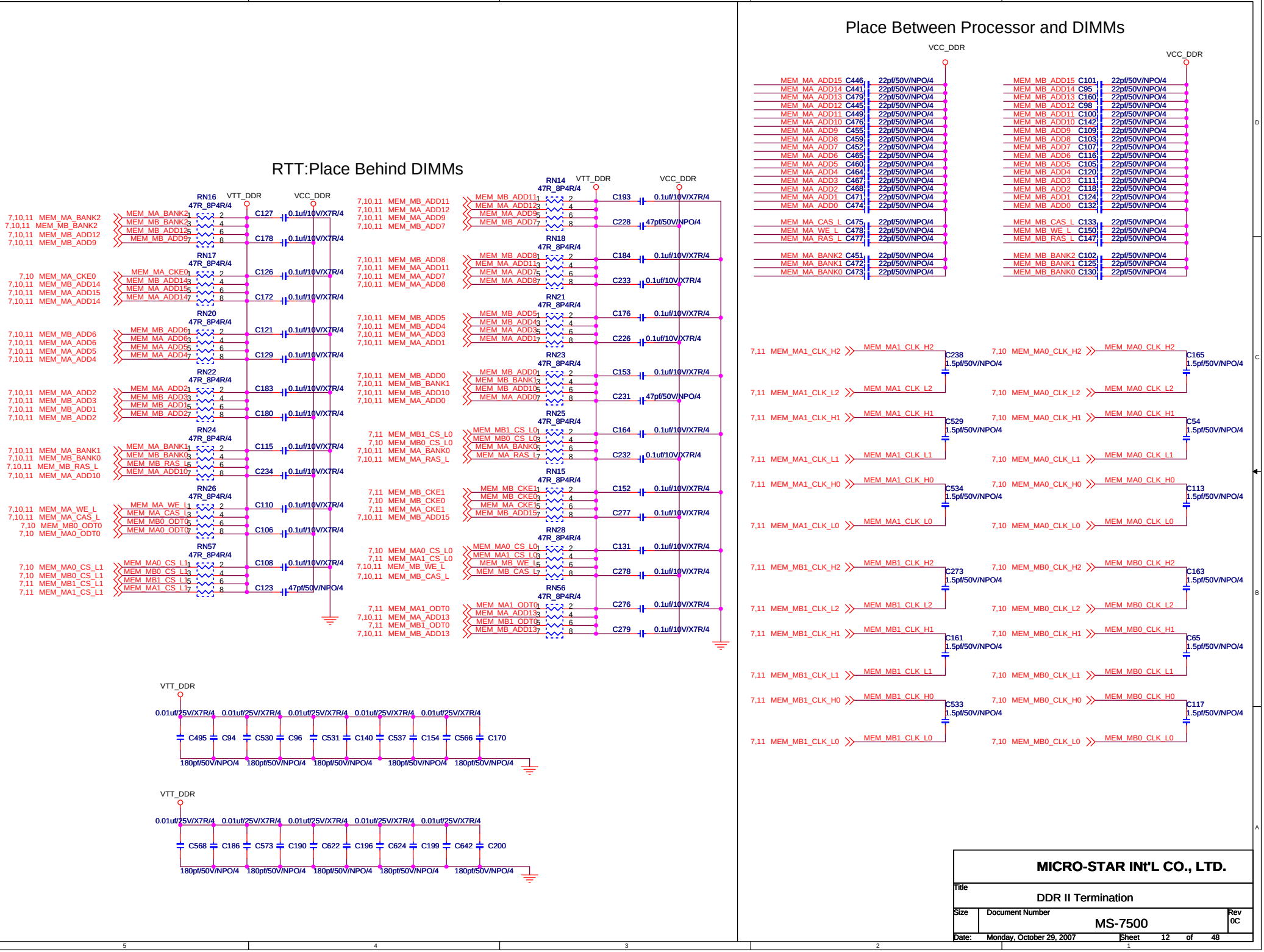




MICRO-STAR INt'L CO., LTD.		
Title: FIRST LOGICAL DDR DIMM		
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 10 of 48	



MICRO-STAR INt'L CO., LTD.			
Title: SECOND LOGICAL DDR DIMM			
Size	Document Number: MS-7500		Rev: 0C
Date: Monday, October 29, 2007	Sheet 11 of 48		


RTT:Place Behind DIMMs
Place Between Processor and DIMMs
VTT_DDR
VCC_DDR
RN16
RN17
RN20
RN22
RN24
RN26
RN57
RN14
RN18
RN21
RN23
RN25
RN15
RN28
RN56
47R_8P4R/4
0.1uf/10V/X7R/4
47pf/50V/NPO/4
22pf/50V/NPO/4
1.5pf/50V/NPO/4
0.01uf/25V/X7R/4
180pf/50V/NPO/4
MICRO-STAR INt'L CO., LTD.
DDR II Termination
MS-7500
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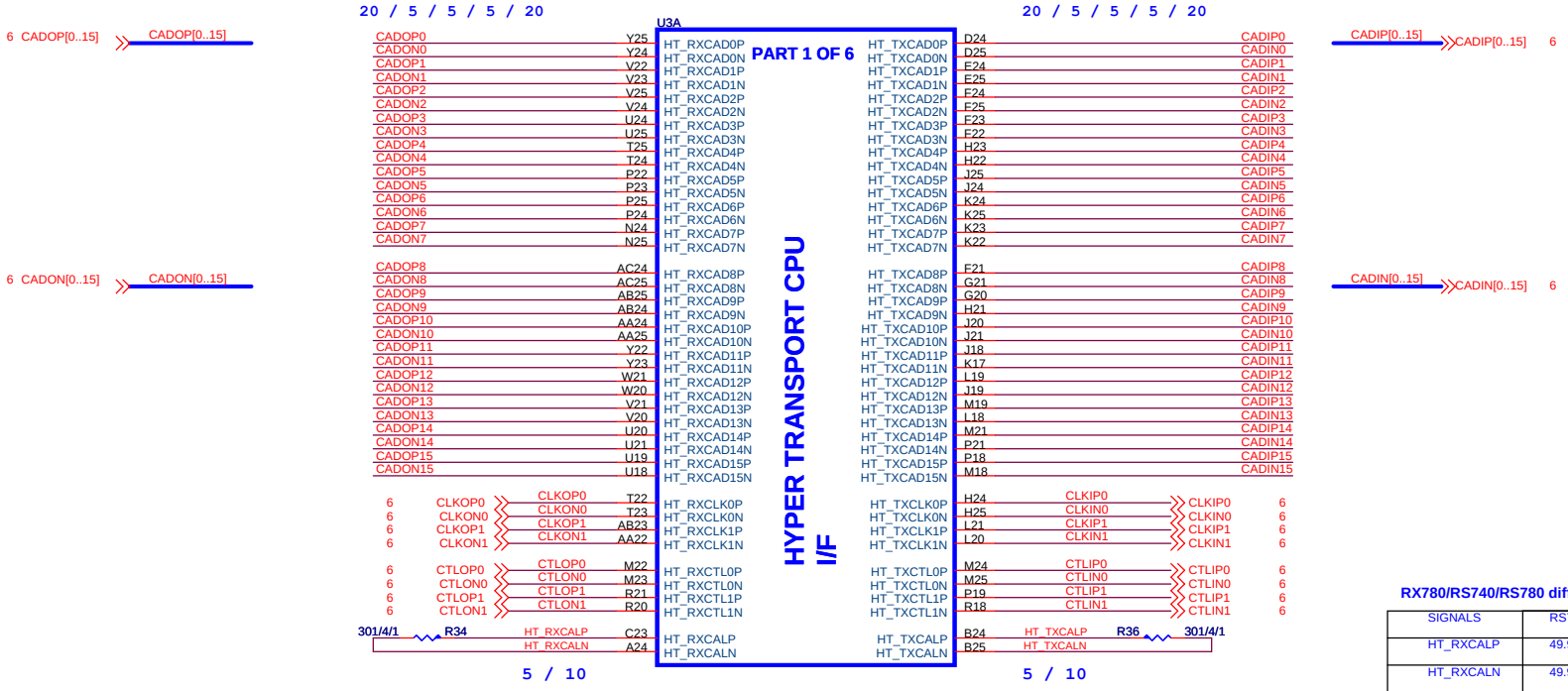
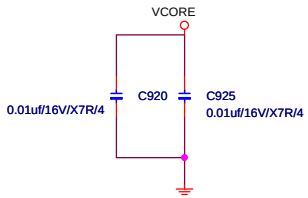


RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

08/10/07 AMD: Please note that R34 and R36 are 301 1% resistor when using RS780.
R34 and R36 are 1.21K 1% resistor when using RX780.

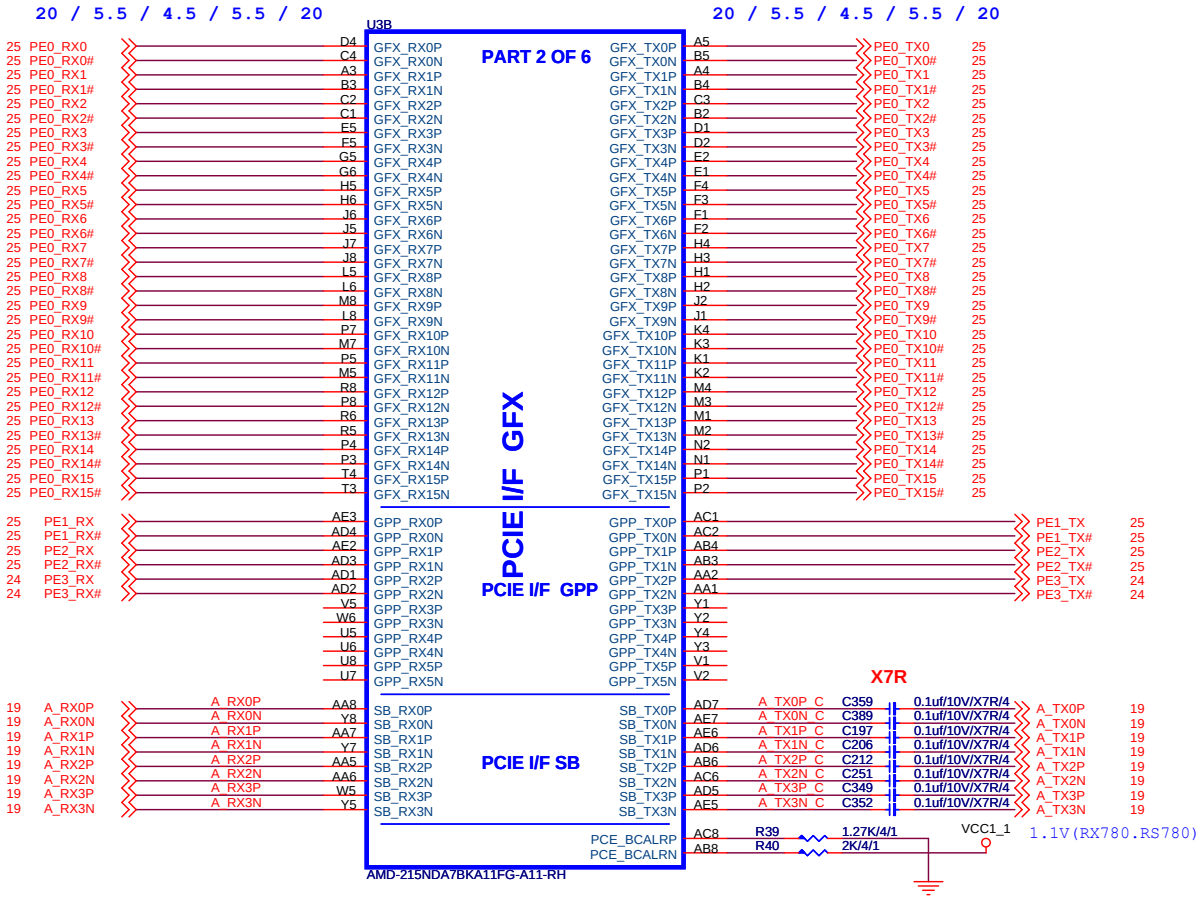


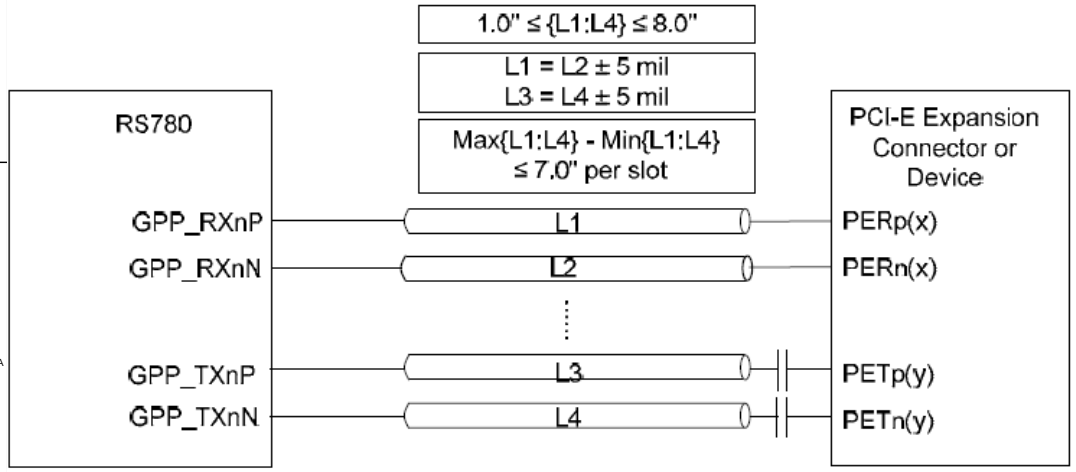
Adding some 0.01 uF stitching capacitors for crossing a split when these signals change different reference layer.

For 07/09/07

AMD-215NDA7BKA11FG-A11-RH

MICRO-STAR INt'L CO., LTD.			
Title: RS780/RX780-HT LINK I/F			
Size	Document Number: MS-7500		Rev: 0C
Date: Monday, October 29, 2007	Sheet 13 of 48		



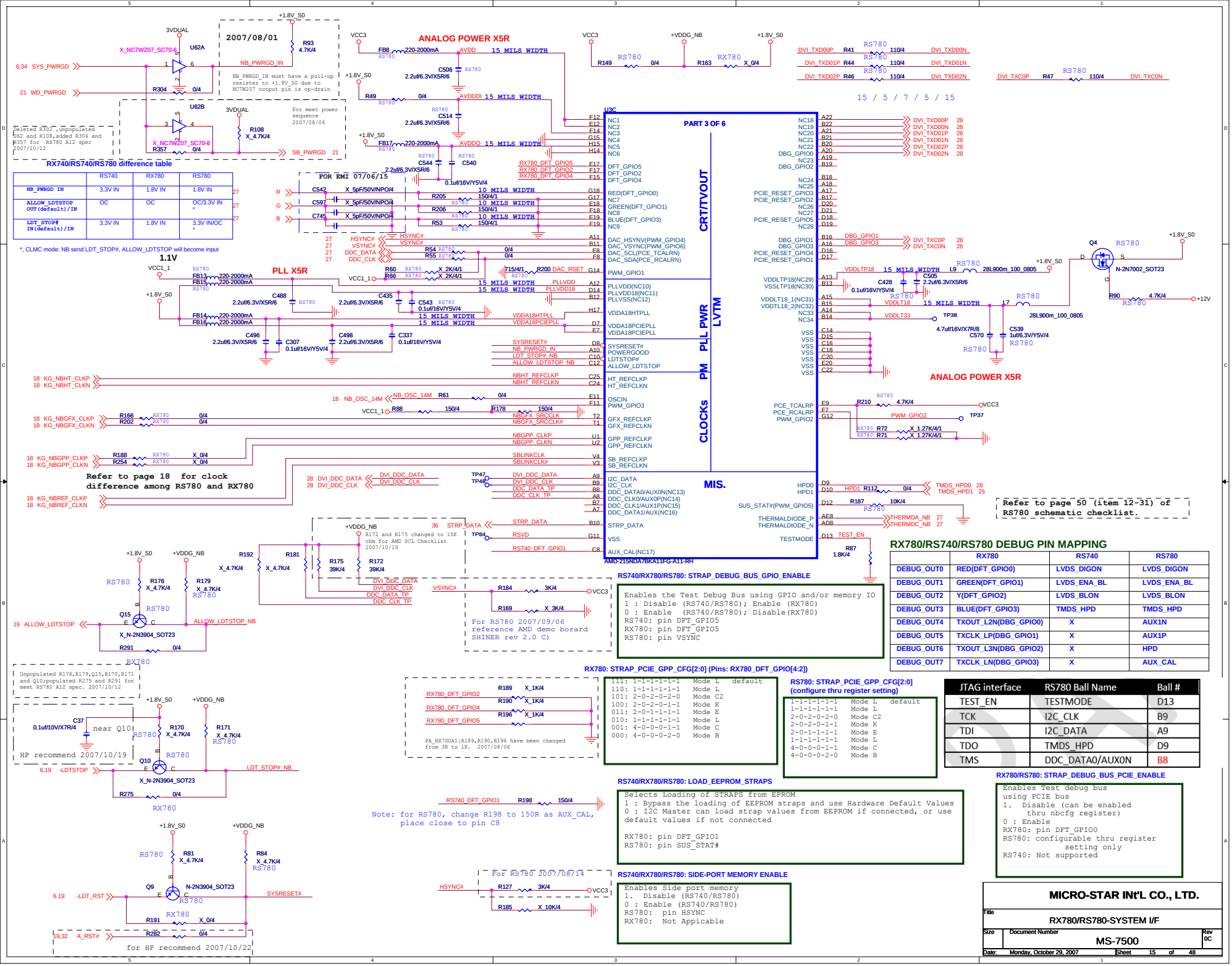


RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

MICRO-STAR INt'L CO., LTD.		
Title: RX780/RS780-PCIE I/F		
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 14 of 48	



	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

DEBUG PIN MAPPING	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

JTAG interface	RS780 Ball Name	Ball #
TEST_EN	TESTMODE	D13
TCK	I2C_CLK	B9
TDI	I2C_DATA	A9
TDO	TMDS_HPD	D9
TMS	DDC_DATA0/AUX0N	B8

Title	RX780/RS780-SYSTEM I/F
Size	Document Number: MS-7500
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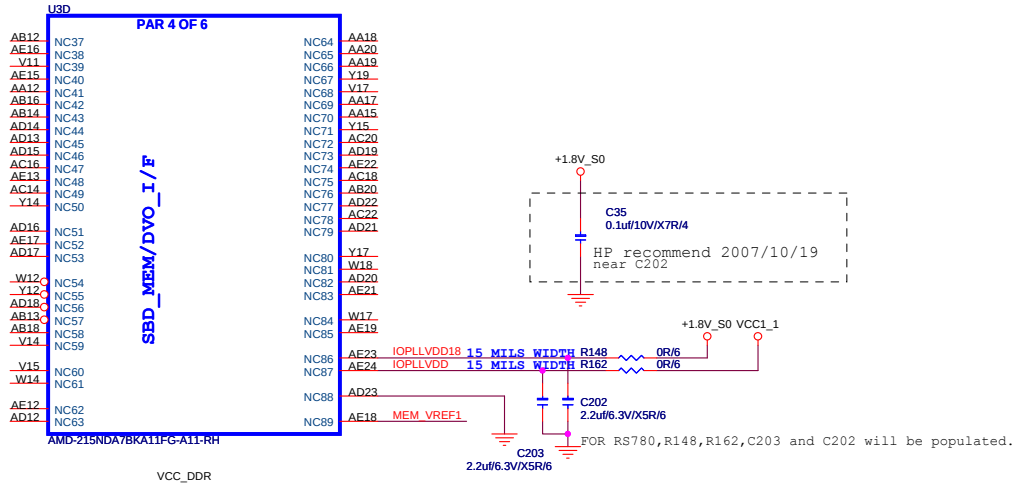

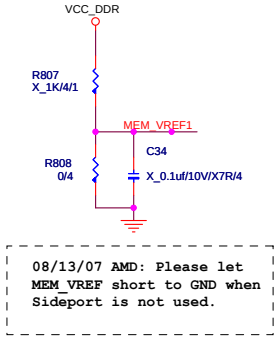

Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

MICRO-STAR INt'L CO., LTD.		
Title: SPMEM/STRAPS		
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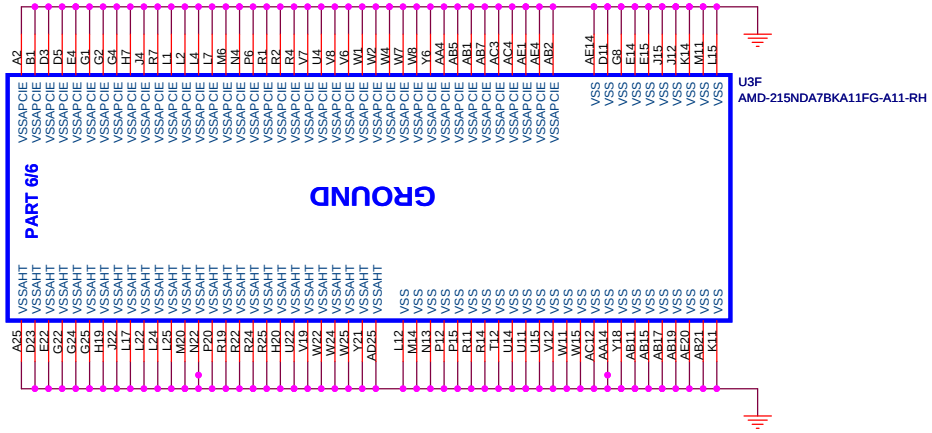
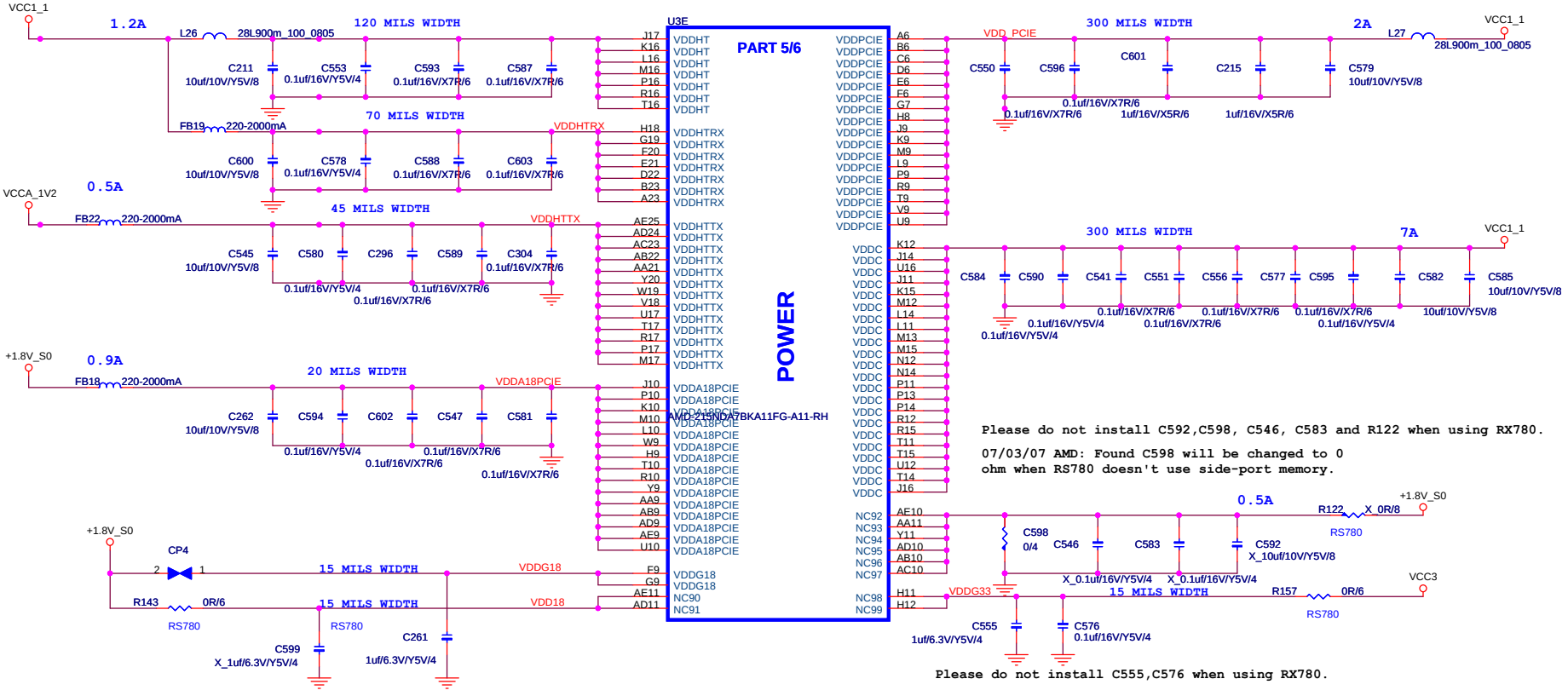


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



Please do not install C592,C598, C546, C583 and R122 when using RX780.

07/03/07 AMD: Found C598 will be changed to 0 ohm when RS780 doesn't use side-port memory.

Please do not install C555,C576 when using RX780.

07/03/07 AMD: Found C599 will be changed to 0 ohm when RS780 doesn't use side-port memory.

08/26/07 AMD: recommend R143 install 0 ohm and C599 install 1uf.

MICRO-STAR INt'L CO., LTD.		
Title: RX780/RS780-POWER		
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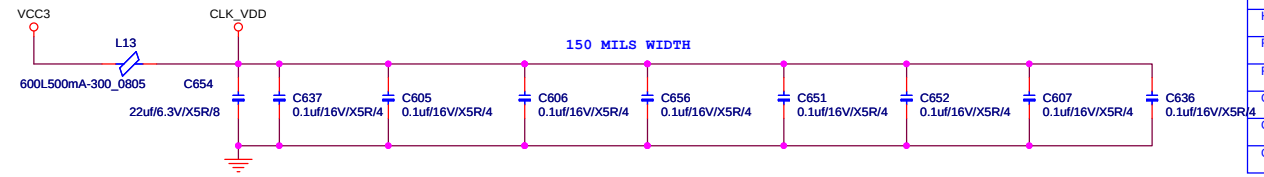
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

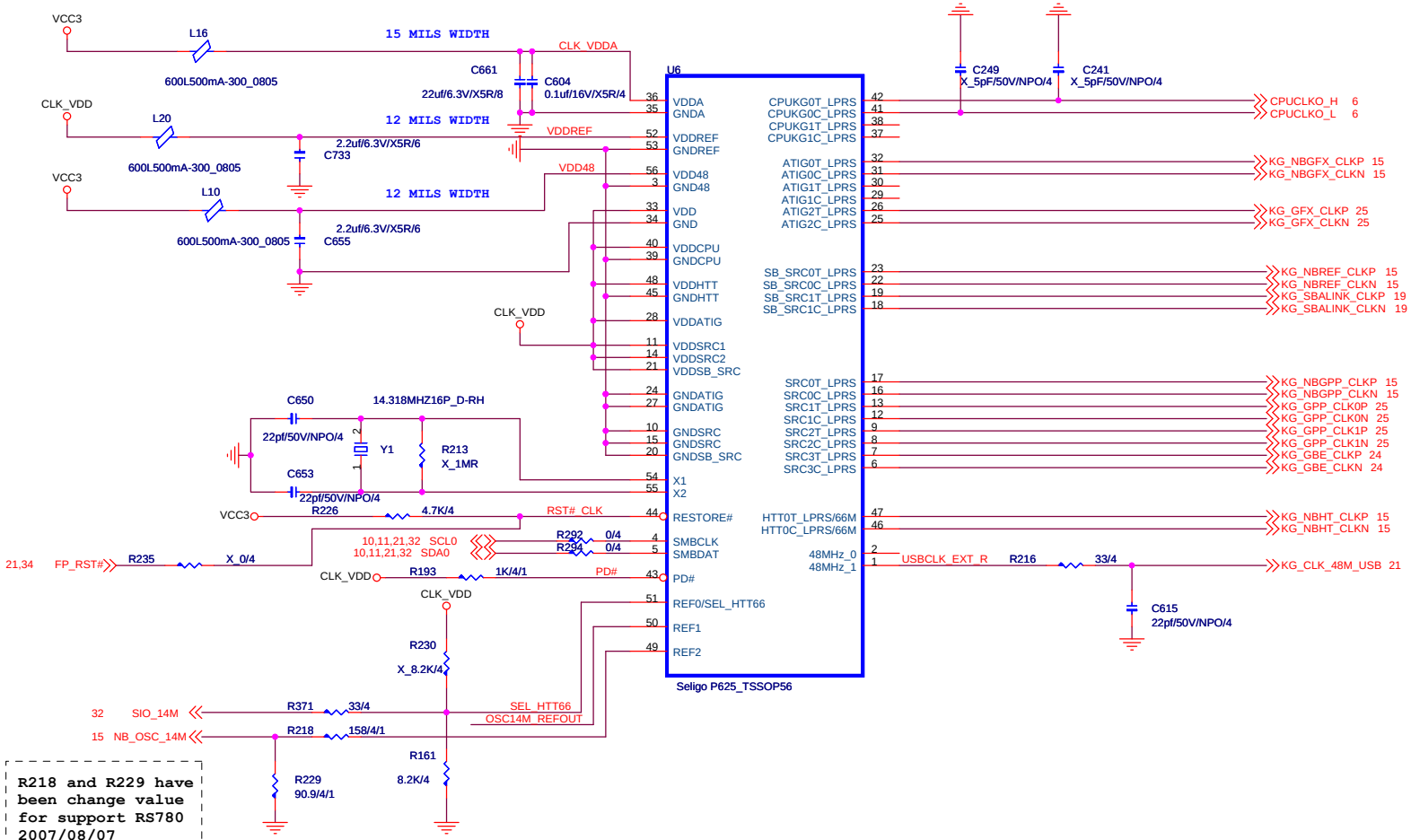
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U6 AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U6 POWER PIN



R218 and R229 have been change value for support RS780 2007/08/07

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

	NB_OSC_14M
RS740	3.3V IN
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

MICRO-STAR INt'L CO., LTD.

Title: Clock-Gen Seligo P625

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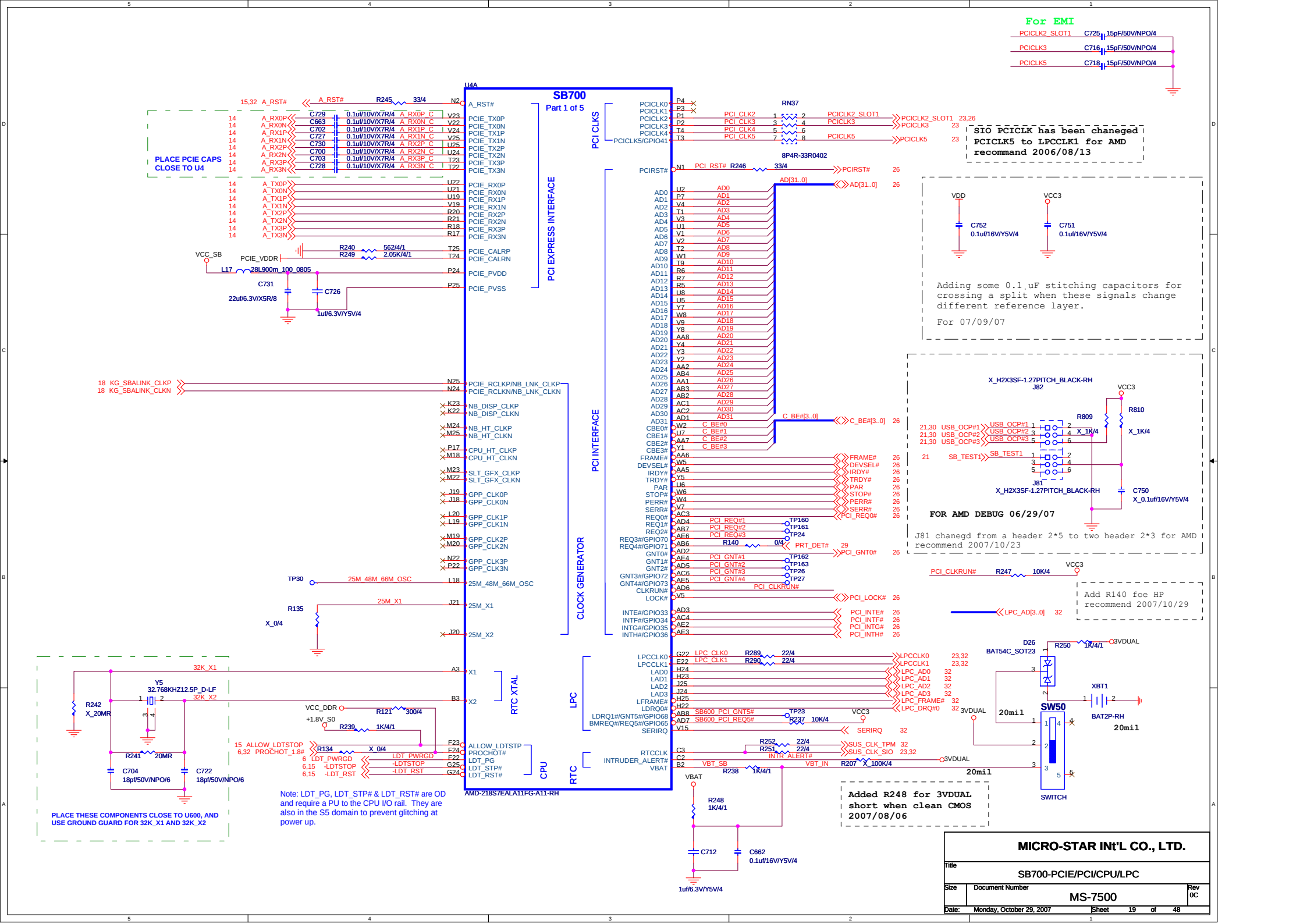
For EMI
PCICLK2_SLOT1 C725 15pF/50V/NPO/4
PCICLK3 C716 15pF/50V/NPO/4
PCICLK5 C718 15pF/50V/NPO/4
U4A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
PLACE PCIE CAPS CLOSE TO U4
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
AMD-218S7EALA11FG-A11-RH
SIO PCICLK has beneged PCICLK5 to LPCCLK1 for AMD recommand 2006/08/13
8P4R-33R0402
Adding some 0.1 uF stitching capacitors for crossing a split when these signals change different reference layer.
For 07/09/07
FOR AMD DEBUG 06/29/07
J81 chanegd from a header 2*5 to two header 2*3 for AMD recommend 2007/10/23
Add R140 foe HP recommend 2007/10/29
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
Added R248 for 3VDUAL short when clean CMOS 2007/08/06
MICRO-STAR INt'L CO., LTD.
SB700-PCIE/PCI/CPU/LPC
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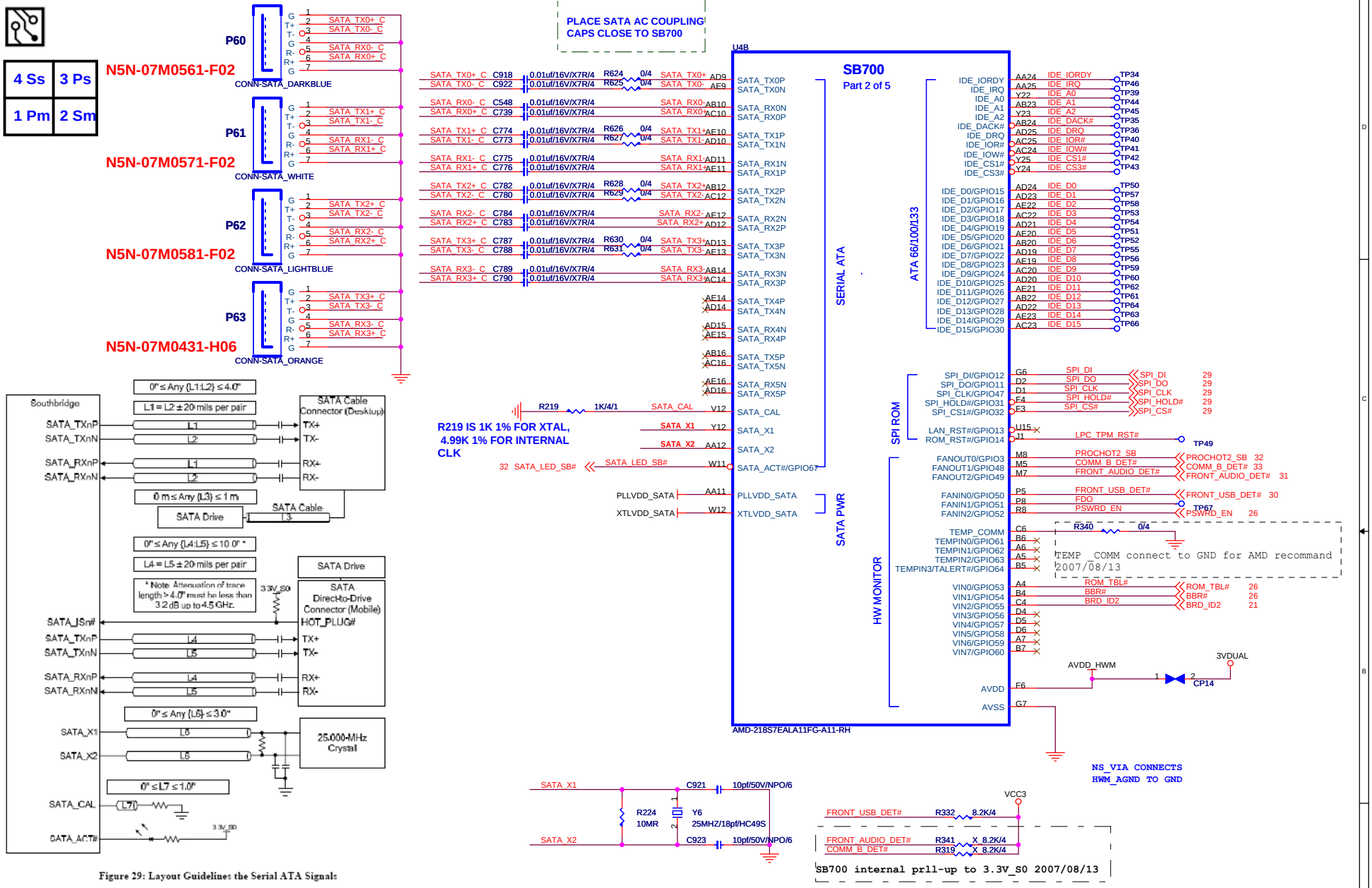

Figure 29: Layout Guidelines the Serial ATA Signals

Trace spacing:

- ASIC breakout (first 0.5") ≥ 1:1
- After the breakout region ≥ 5:1 on both sides of pair.

Impedance:

- 100 Ω ± 15% differential.
- Reference to a solid GND (not PWR) plane.

MICRO-STAR INt'L CO., LTD.	
Title	SB700-SATA/IDE/HWM/SPI
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The pull-up on the SB700 side of the transistor is not needed. The SB700 has a default internal 10k pull-up. (See attached pic for reference) MSI can NI R352 for HP recommand 2007/08/19

C377 has been unpopulate for meet power sequence 2007/08/13

Modify PRT_DET# circuit 2006/08/06

For EMI(closed SB)

AMD recommend 2007/10/19

BOARD ID[2:0]	PHASE
001	USDT
010	CMT
011	SFF

BOARD_REV[1:0]	PHASE
00	All Proto
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN

Trace spacing:
- ASIC breakout (first 0.5") ≥ 1:1
- After the breakout region ≥ 4:1 on both sides of pair.
- Serpentine spacing ≥ 4:1 on both sides of pair.
- ≥ 5:1 from reference plane anti-etch (copper void) or edges.
- ≥ 0.5" from clock chips, oscillators, crystals, core logic or CPU devices.

Impedance:
- 90 Ω ± 15% differential
- Reference to a solid GND (not PWR) plane.

Figure 26 Layout Guidelines for the Universal Serial Bus Signals

MICRO-STAR INt'L CO., LTD.	
Title	SB700-ACPI/GPIO/USB/AUDIO
Size	Document Number: MS-7500 Rev 0C
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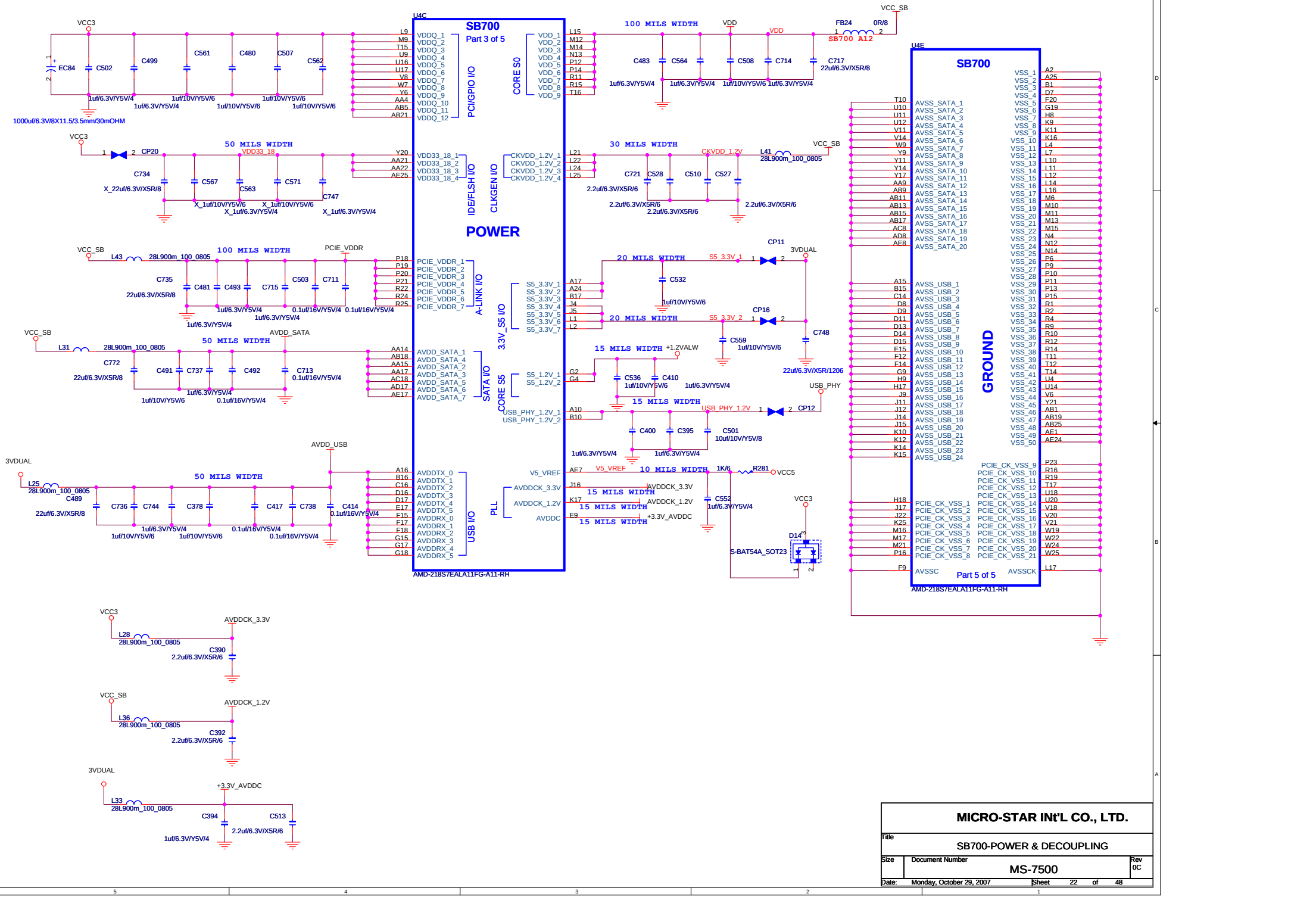
U4C
SB700
Part 3 of 5
POWER
AMD-218S7EALA11FG-A11-RH
U4E
SB700
GROUND
Part 5 of 5
AMD-218S7EALA11FG-A11-RH
VCC3
VCC_SB
3VDUAL
VDD
VDD33_18
PCIE_VDDR
AVDD_SATA
AVDD_USB
AVDDCK_3.3V
AVDDCK_1.2V
+3.3V_AVDDC
CKVDD_1.2V
USB_PHY
V5_VREF
+1.2VALW
+3.3V_AVDDC
1000uf/6.3V/8X11.5/3.5mm/30mOHM
100 MILS WIDTH
50 MILS WIDTH
30 MILS WIDTH
20 MILS WIDTH
15 MILS WIDTH
10 MILS WIDTH
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
SB700 A12
S-BAT54A_SOT23
MICRO-STAR INt'L CO., LTD.
SB700-POWER & DECOUPLING
MS-7500
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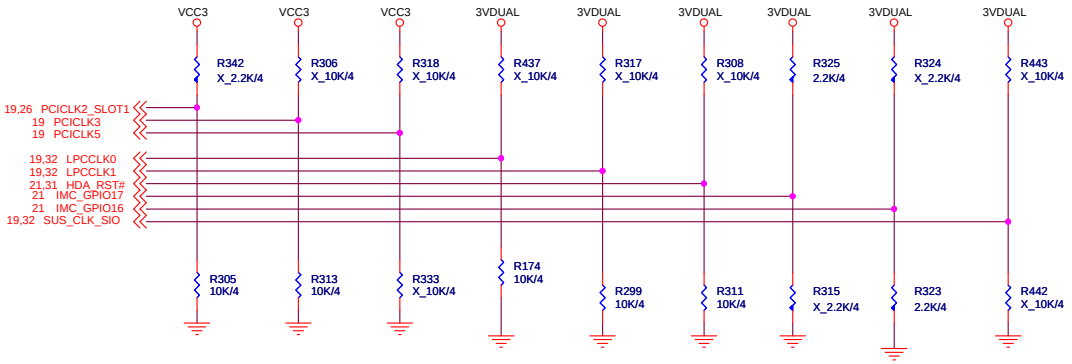
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	RESERVED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM

R325 and R323 have been changed from 10K ohm to 2.2K ohm 2007/08/01(AMD demo schematic update)

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

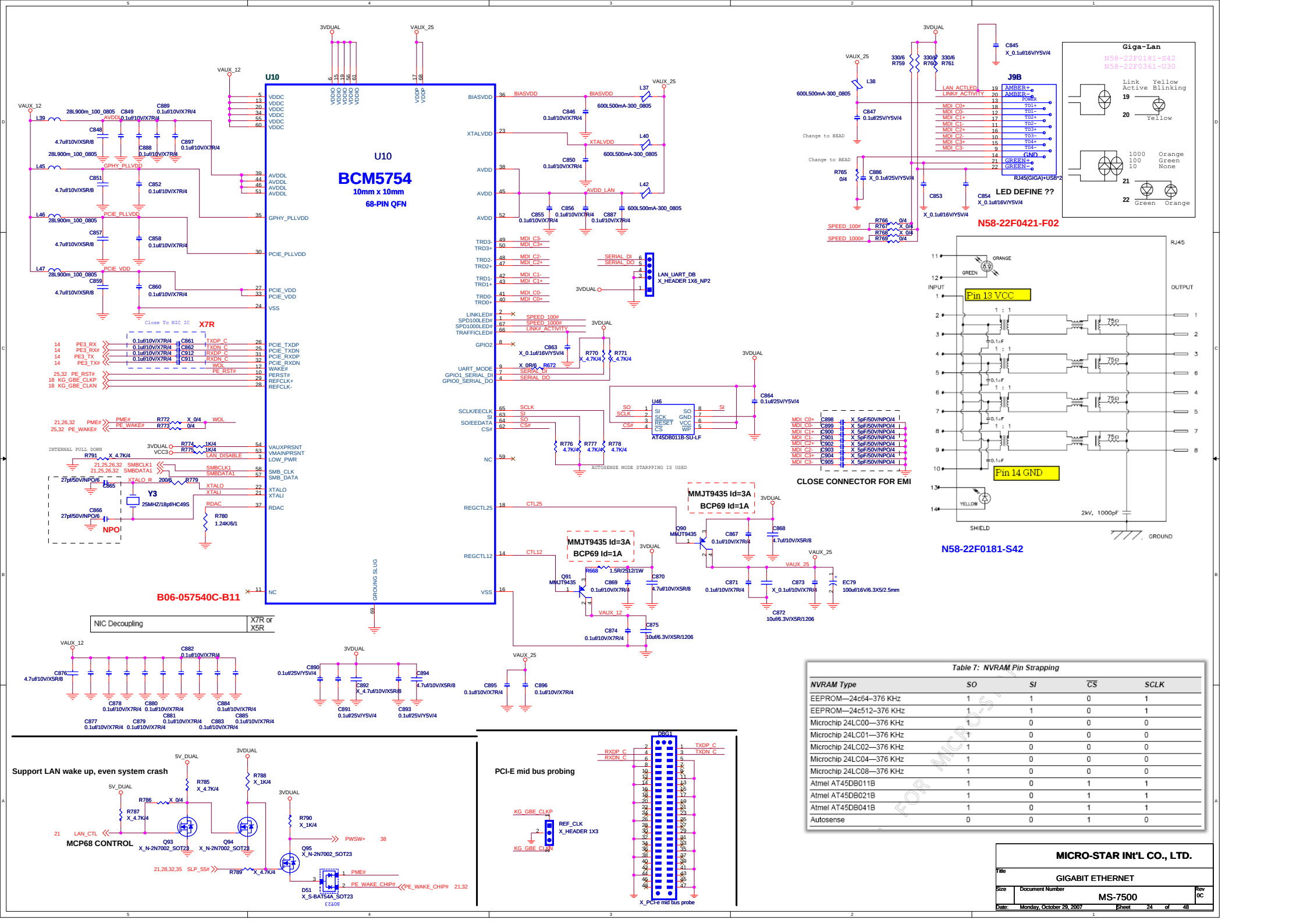
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INt'L CO., LTD.

Title: SB700-STRAPS

Size | Document Number: MS-7500 | Rev: 0C

Date: Monday, October 29, 2007 | Sheet 23 of 48


U10
BCM5754
10mm x 10mm
68-PIN QFN
B06-057540C-B11
X7R
NPO
Close To NIC IC
INTERNAL PULL DOWN
Y3
25MHZ/18pf/HC49S
NIC Decoupling
X7R or X5R
MMJT9435 Id=3A
BCP69 Id=1A
CLOSE CONNECTOR FOR EMI
AUTOSENSE MODE STARPPING IS USED
AT45DB011B-SU-LF
LAN_UART_DB
X_HEADER 1X6_NP2
Support LAN wake up, even system crash
MCP68 CONTROL
PCI-E mid bus probing
REF_CLK
X_HEADER 1X3
X_PCI-e mid bus probe
Giga-Lan
N58-22F0181-S42
N58-22F0361-U30
J9B
RJ45(GIGA)+USB*2
LED DEFINE ??
N58-22F0421-F02
Pin 13 VCC
Pin 14 GND
N58-22F0181-S42
Table 7: NVRAM Pin Strapping
NVRAM Type | SO | SI | CS | SCLK
EEPROM—24c64–376 KHz | 1 | 1 | 0 | 1
EEPROM—24c512–376 KHz | 1 | 1 | 0 | 1
Microchip 24LC00—376 KHz | 1 | 0 | 0 | 0
Microchip 24LC01—376 KHz | 1 | 0 | 0 | 0
Microchip 24LC02—376 KHz | 1 | 0 | 0 | 0
Microchip 24LC04—376 KHz | 1 | 0 | 0 | 0
Microchip 24LC08—376 KHz | 1 | 0 | 0 | 0
Atmel AT45DB011B | 1 | 0 | 1 | 1
Atmel AT45DB021B | 1 | 0 | 1 | 1
Atmel AT45DB041B | 1 | 0 | 1 | 1
Autosense | 0 | 0 | 1 | 0
MICRO-STAR INT'L CO., LTD.
Title
GIGABIT ETHERNET
Size
Document Number
MS-7500
Rev
0C
Date: Monday, October 29, 2007
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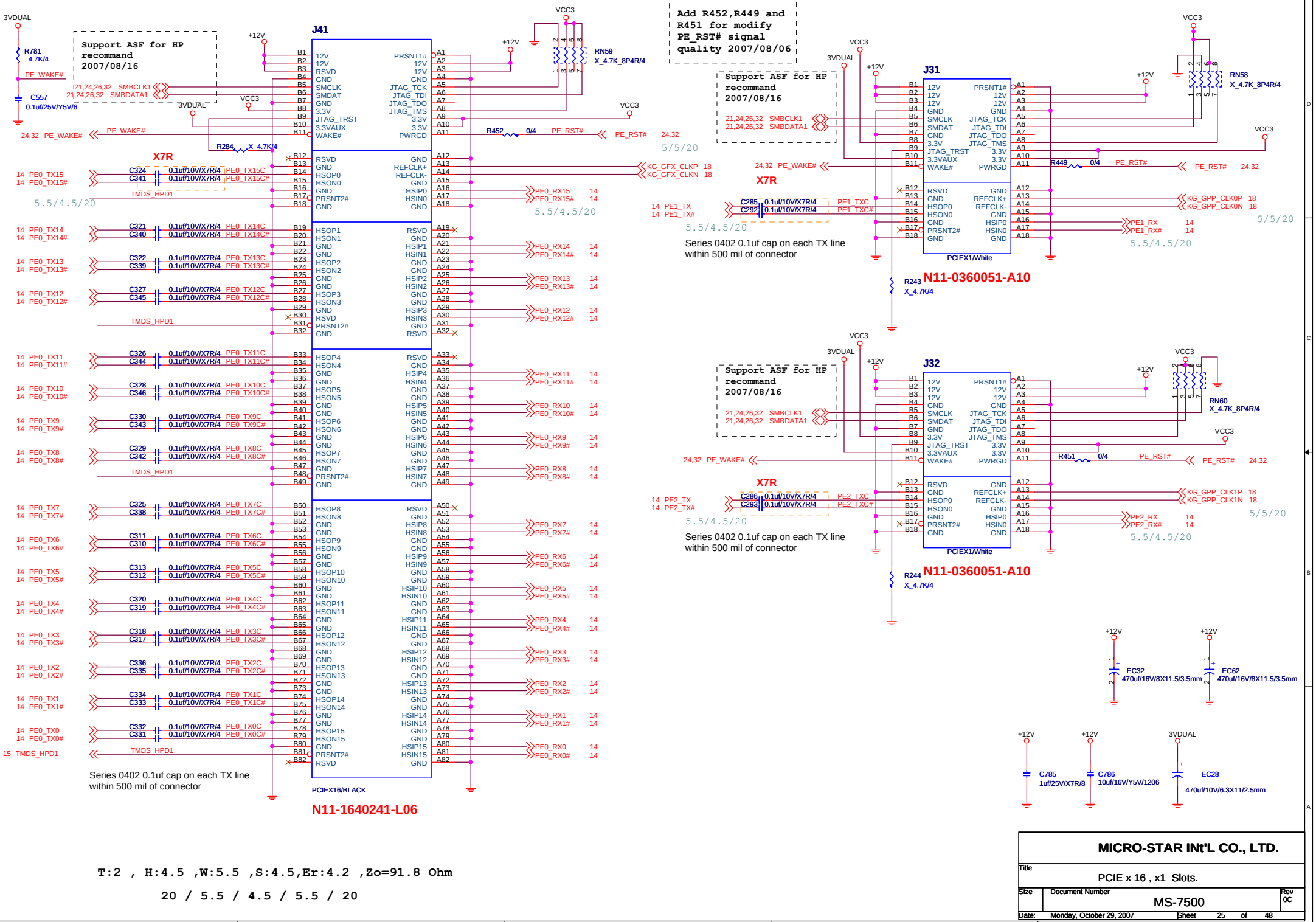
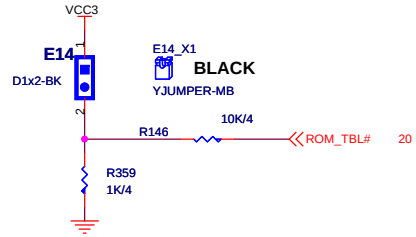
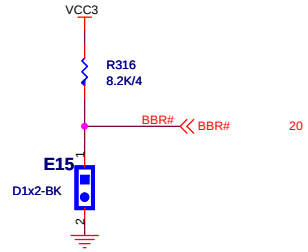

Support ASF for HP recommand 2007/08/16
J41
PCIEX16/BLACK
N11-1640241-L06
Series 0402 0.1uf cap on each TX line within 500 mil of connector
Add R452,R449 and R451 for modify PE_RST# signal quality 2007/08/06
J31
PCIEX1/White
N11-0360051-A10
Series 0402 0.1uf cap on each TX line within 500 mil of connector
J32
PCIEX1/White
N11-0360051-A10
Series 0402 0.1uf cap on each TX line within 500 mil of connector
T:2 , H:4.5 ,W:5.5 ,S:4.5,Er:4.2 ,Zo=91.8 Ohm
20 / 5.5 / 4.5 / 5.5 / 20
MICRO-STAR INt'L CO., LTD.
PCIE x 16 , x1 Slots.
MS-7500
Monday, October 29, 2007

BOOT BLOCK WRITE JUMPER



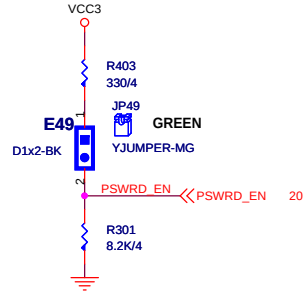
N31-1020211-P05

BOOT BLOCK RECOVERY HEADER



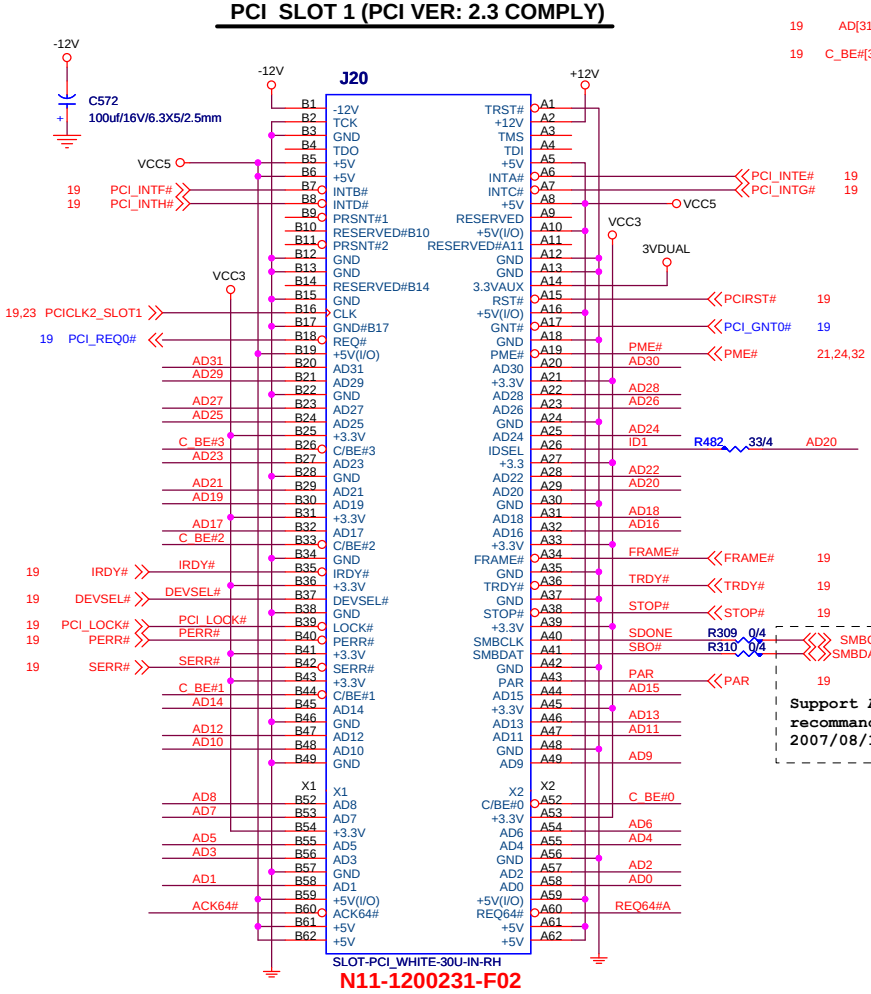
N31-1020211-P05

PASSWORD JUMPER



N31-1020211-P05

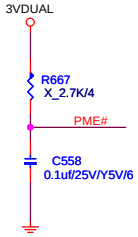
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



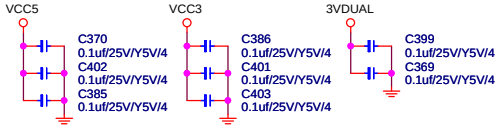
N11-1200231-F02

Support ASF for HP recommand 2007/08/16

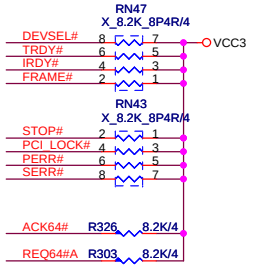
19 AD[31..0] AD[31..0]
19 C_BE#[3..0] C_BE#[3..0]



PCI SLOT DECOUPLING CAPACITORS

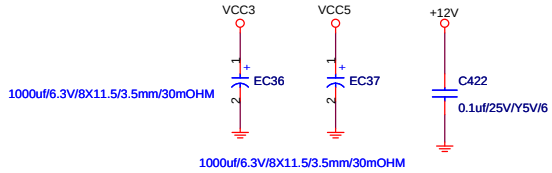


PCI PULL-UP / DOWN RESISTORS



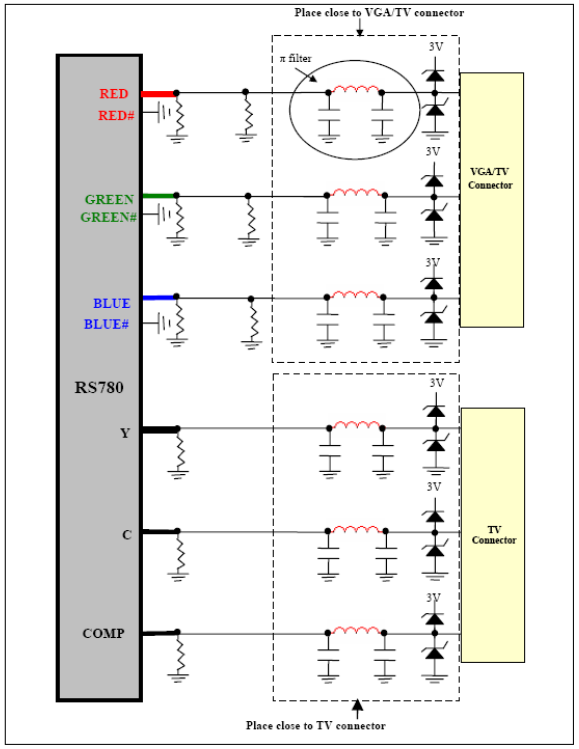
SB700
PCI SLOT1
IDSEL = AD20
PCI_REQ0#
PCI_GNT0#
PCI_INTE#

PCIRST#
PCICLK2_SLOT1



MICRO-STAR INt'L CO., LTD.	
Title	PCI Slot1
Size	Document Number: MS-7500 — Rev: 0C
Date: Monday, October 29, 2007	Sheet 26 of 48

Figure 29: Placement of VGA and TV-Out Connectors



VGA CONN BLOCK

Add L6,L21 and L22 for EMI solution 2007/08/20

close VGA connector

D44 BAV99_SOT23 VGA_R
D45 BAV99_SOT23 VGA_G
D46 BAV99_SOT23 VGA_B
D47 BAV99_SOT23 DDC_SCL
D48 BAV99_SOT23 DDC_SDA
D49 BAV99_SOT23 HSYNC_A
D50 BAV99_SOT23 VSYNC_A

7.5 / 15 / 15

R95 150/4/1 L6 0R/6 L4 47nH/300mA/0.7/6 C149 3.3pF/50V/NPO/4 C148 2.2pF/25V/NPO/4
R94 150/4/1 L21 0R/6 L3 47nH/300mA/0.7/6 C144 3.3pF/50V/NPO/4 C143 2.2pF/25V/NPO/4
R92 150/4/1 L22 0R/6 L2 47nH/300mA/0.7/6 C139 3.3pF/50V/NPO/4 C175 2.2pF/25V/NPO/4

R86 10K/4 C112 0.1uf/25V/Y5V/4 U11 NC7WZ08 5V_HSYNC
C138 0.1uf/25V/Y5V/4 U49 NC7WZ08 5V_VSYNC
5V_VSYNC R686 33/4 L34 27nh/600mA/L6 VSYNC_A
5V_HSYNC R687 33/4 L35 27nh/600mA/L6 HSYNC_A

D5 1N5817
FS1 1.1A/mSMD110F/0.21OHM FB12 301S/0805 VGAPWR_FB
C104 0.1uf/25V/Y5V/4

R300 4.7K/4 Q19 N-2N7002_SOT23 R617 X_0/4 DDC_DATA R688 33/4 DDC_SDA
R91 6.8K/4 R89 6.8K/4
R180 4.7K/4 Q20 N-2N7002_SOT23 R618 X_0/4 DDC_CLK R689 33/4 DDC_SCL

DDC_SCL VSYNC_A HSYNC_A DDC_SDA VGA_B VGA_G VGA_R

C122 470pf/50V/X7R/4 C135 470pf/50V/X7R/4 C114 47pf/50V/NPO/4 C134 47pf/50V/NPO/4 C792 47pf/50V/NPO/4 C793 47pf/50V/NPO/4

J69 DSUB-VGAF_BLUE-RH
N51-15F0521-F02

Temperature Sensing

R592 has been populated and R615 has been un-populated for HP recommand 2007/08/09
R615 has been deleted for HP recommand 2007/10/22

3VDUAL R592 0/4
C765 100p/50V/NPO/4 C24 0.1uf/10V/X7R/4 C404 10uf/10V/Y5V/8
U24 SMSC VDD DP1 DN1 DP2 DN2 GND SMCLK SMDATA
C673 100p/50V/NPO/4 C676 100p/50V/NPO/4
THERMDA_CPU THERMDC_CPU
6,32 SMB_CLK_SENSE SMB_DATA_SENSE
EMC1043 MSOP8_T
CPU & NB temperature sensor
D0F-0104302-S32

C677 X_100p/50V/NPO/4 Q69 X_N-2N3904_SOT23
COLSE CHIPSET
R622 0/4 THERMDA_NB R623 0/4 THERMDC_NB
Add NB therm-circuit For HP recommand 2007/08/06

FRONT PANEL USB CONNECTOR FOR USB PORT 10

Trace lengths must be less 5 inches
Match pairs to 50 mil.
L15 X_Common Chock
RN55 0R_8P4R/6
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 10

5V_DUAL_USB
22uf/6.3V/X5R/1206 C397 C442 C490 22uf/6.3V/X5R/1206
0.1uf/25V/Y5V/4
P25 CON2X5-1_Black
N32-2051671-H06

5V_DUAL_USB
D39 IP4220/SOT457

MICRO-STAR INT'L CO., LTD.		
Title: VGA CONNECTOR		
Size	Document Number: MS-7500	Rev: 0C
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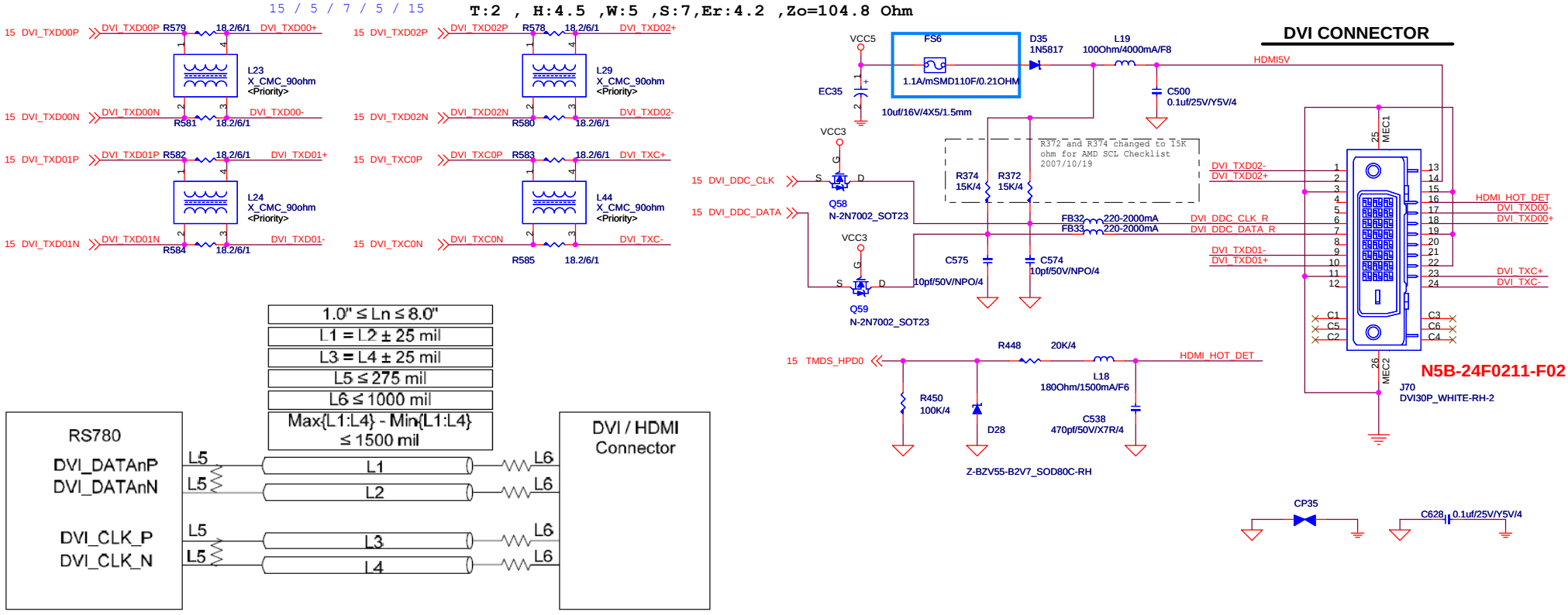
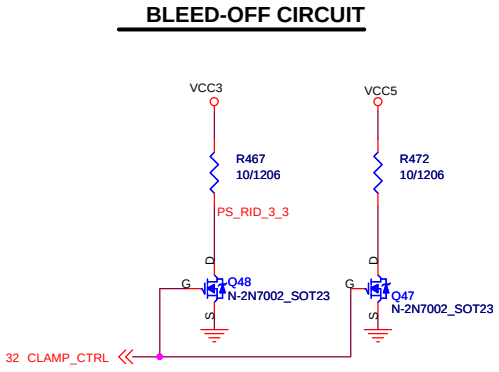


Figure 32: Layout Guidelines for the DVI/HDMI Signals

7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.



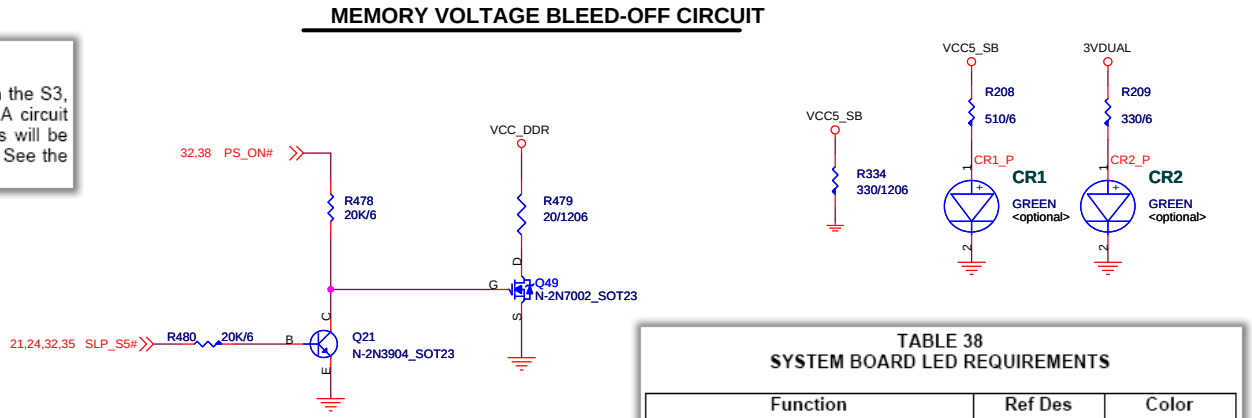
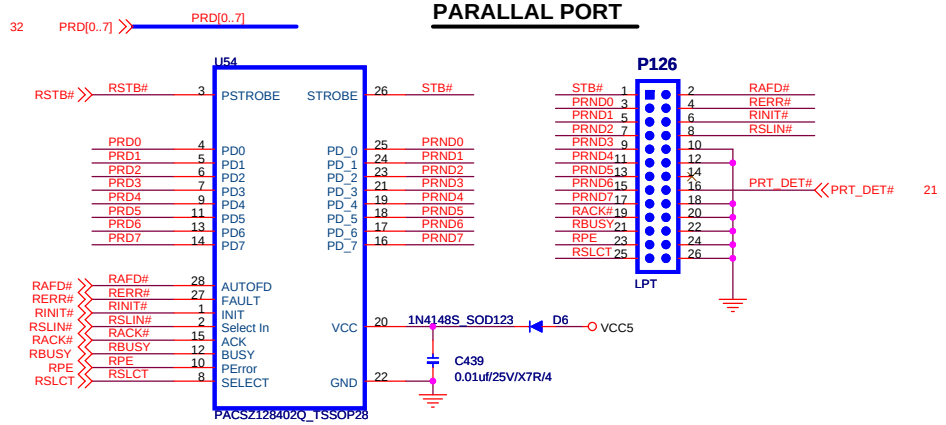


TABLE 38
SYSTEM BOARD LED REQUIREMENTS

Function	Ref Des	Color
+5 V AUX	CR1	Green
+3 V AUX	CR2	Green

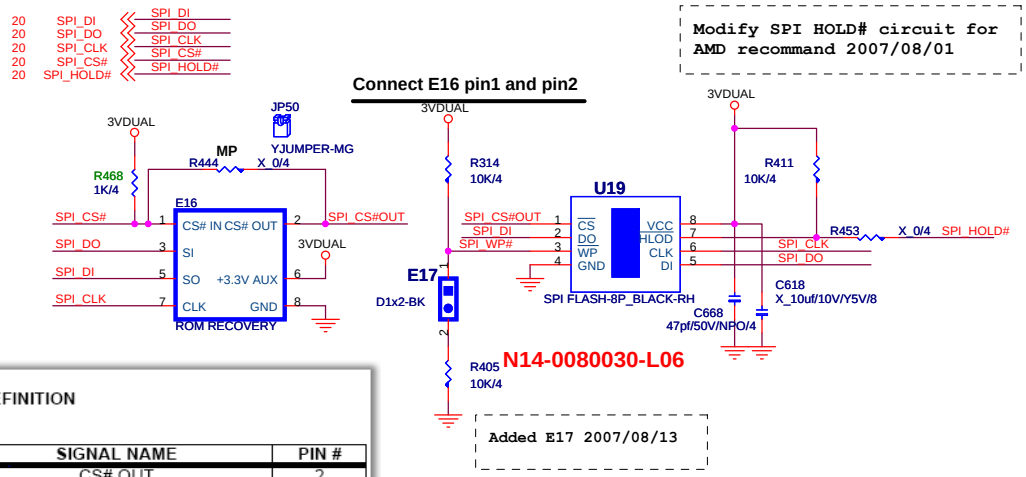
MICRO-STAR INt'L CO., LTD.		
Title: DVI CONNECTOR / BLEED OFF		
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 28 of 48	

PARALLAL PORT



Modify Parallal port circuit 2007/08/13 (Added U54)

SPI ROM



Modify SPI HOLD# circuit for AMD recommand 2007/08/01

Added E17 2007/08/13

TABLE 22
ROM RECOVERY HEADER DEFINITION

E16

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	CS# IN	CS# OUT	2
3	SI	KEY (no pin)	4
5	SO	VCC (+3.3V AUX)	6
7	CLK	GND	8

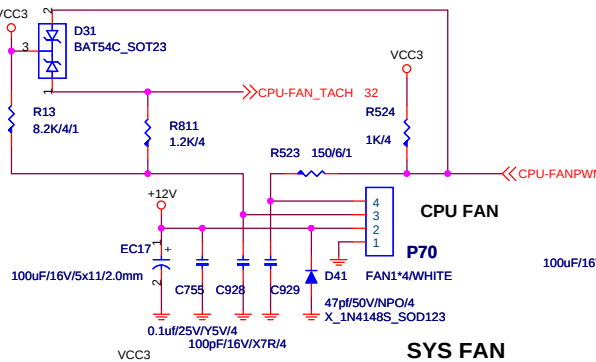
Parallel Port 2 x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

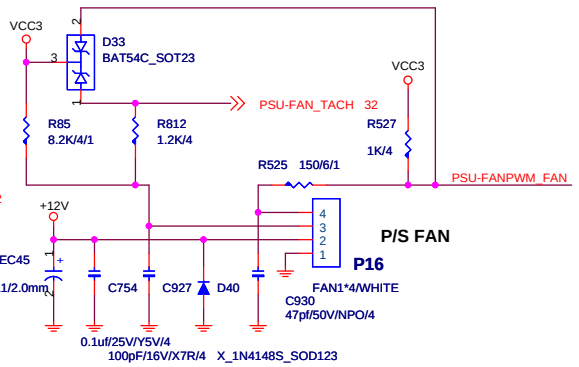
FAN BOLCK

Modify Fan-circuit for HP recommend 2007/08/06

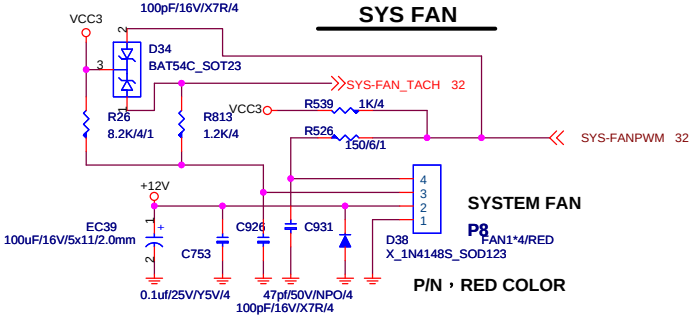
CPU FAN

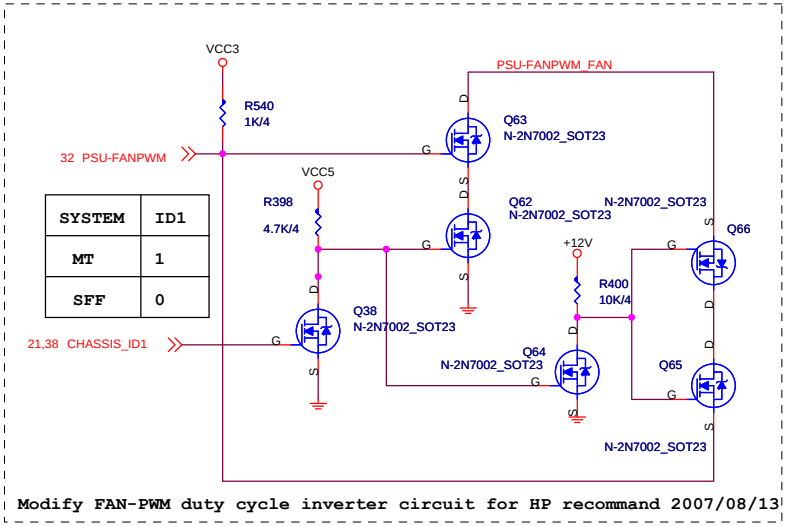


PSU FAN



SYS FAN





Modify FAN-PWM duty cycle inverter circuit for HP recommand 2007/08/13

P70 – CPU P8 – Chassis P16 – Power Supply

Pin #	Signal Name
1	GND
2	+12 V
3	FAN TACH
4	FAN PWM INPUT

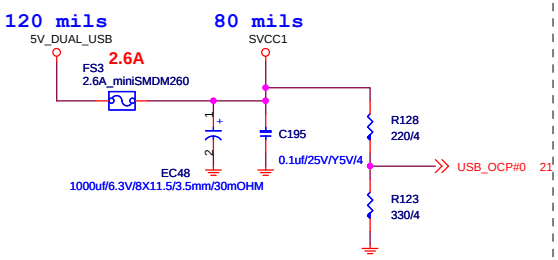
MICRO-STAR INt'L CO., LTD.

Title: SPI ROM / FAN / LPT

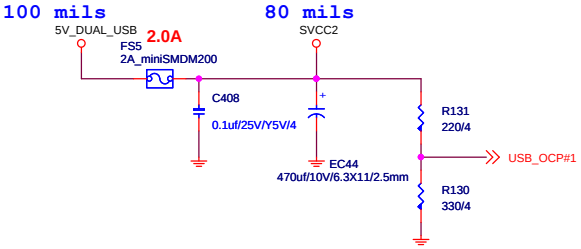
Size | Document Number: MS-7500 | Rev: 0C

Date: Monday, October 29, 2007 | Sheet 29 of 48

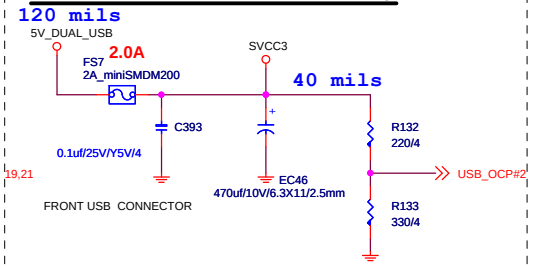
POWER CIRCUIT FOR USB PORT 0,1,2,3



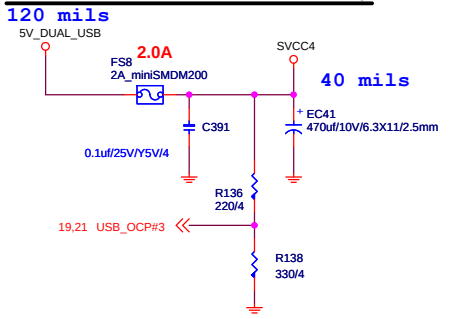
POWER CIRCUIT FOR USB PORT 4,5



POWER CIRCUIT FOR USB PORT 6,7

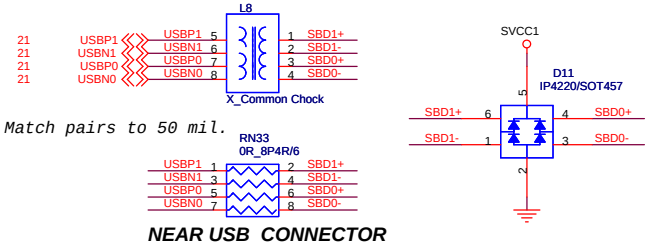


POWER CIRCUIT FOR USB PORT 8,9



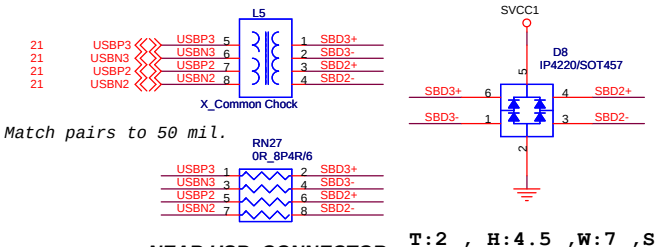
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3

Trace lengths must be less 12 inches

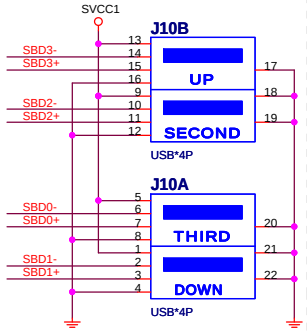


Match pairs to 50 mil.

Trace lengths must be less 12 inches



Match pairs to 50 mil.



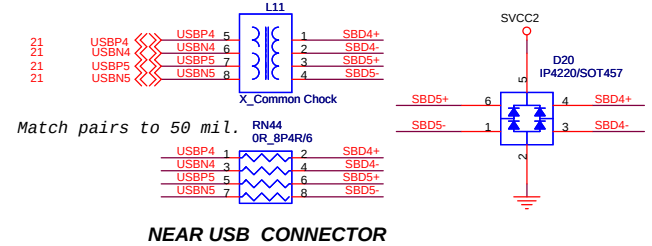
N53-16M0051-S42

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

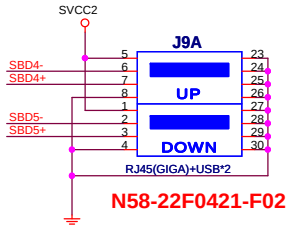
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

REAL USB CONNECTOR WITH RJ45 FOR USB PORT 4,5

Trace lengths must be less 5 inches



Match pairs to 50 mil.



N58-22F0421-F02

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

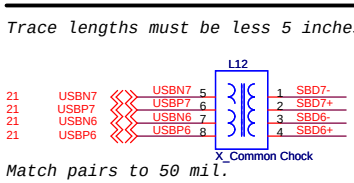
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

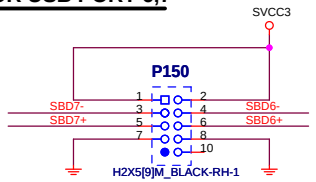
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



Match pairs to 50 mil.



N31-2051391-H06

COLOR BLACK

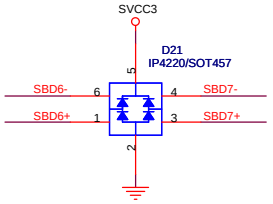


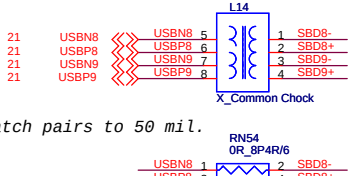
TABLE 10
MEDIA CARD READER USB HEADER DEFINITION (TOP VIEW)

P150

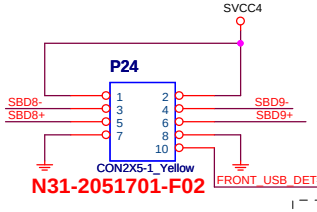
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 4 (-)	USB Port 5 (-)	4
5	USB Port 4 (+)	USB Port 5 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	No Connect	10

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



Match pairs to 50 mil.



N31-2051701-F02

FRONT USE DETECT

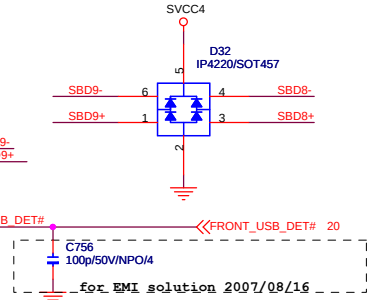


TABLE 9
FRONT I/O USB HEADER DEFINITION (TOP VIEW)

P24

Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 8 (-)	USB Port 9 (-)	4
5	USB Port 8 (+)	USB Port 9 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	FRONT USB DETECT#	10

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

MICRO-STAR INt'L CO., LTD.

Title: USB Conn.

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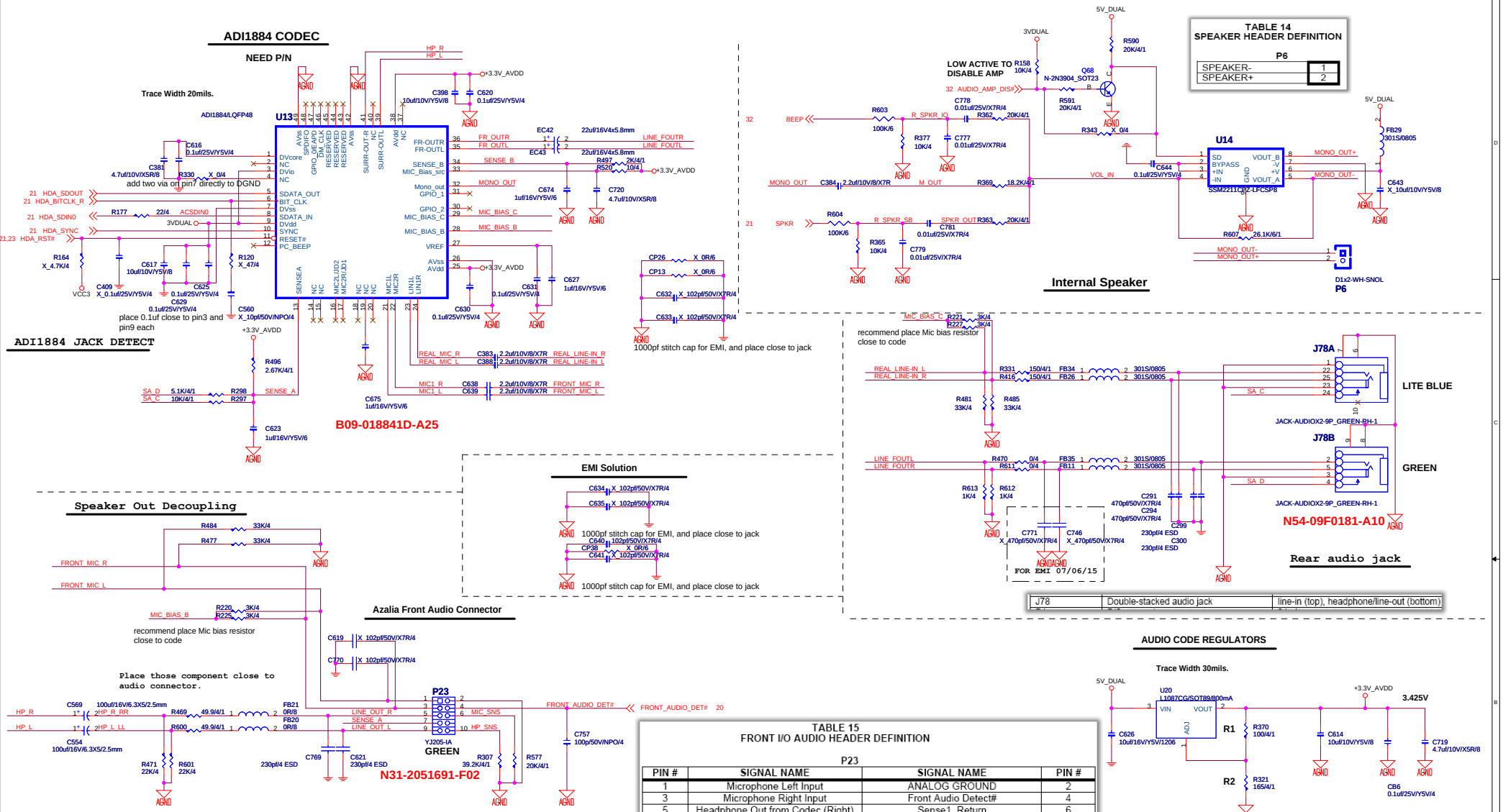

TABLE 15
FRONT I/O AUDIO HEADER DEFINITION

P23

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	Microphone Left Input	ANALOG GROUND	2
3	Microphone Right Input	Front Audio Detect#	4
5	Headphone Out from Codec (Right)	Sense1_Return	6
7	Sense Send	KEY (no pin)	8
9	Headphone Out from Codec (Left)	Sense2_Return	10

ANALOG I/O

Pin Name	Pin Number	I/O	Description	Capabilities * Input	Capabilities * Output
PCBEEP	12	I	Monaural Input from system for Analog PCBeep	LI	
PORT-F_L	16	I/O	Auxillary Input / Output	LI	LO
PORT-F_R	17				
PORT-B_L	21	I	Front Panel stereo MIC / Line-In	LI / MIC	
PORT-B_R	22				
PORT-C_L	23	I	Rear Panel stereo MIC / Line-In	LI / MIC	
PORT-C_R	24				
MONO_OUT	32	O	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone		LO
PORT-D_L	35	O	Rear Panel Headphone / Line-Out		HP / LO
PORT-D_R	36				
PORT-A_L	39	O	Front Panel Headphone / Line-Out		HP / LO
PORT-A_R	41				

* LI – Line Level Input
LO – Line Level Output
HP – Output capable of driving headphone load & power
MIC – Input supports Microphones with MIC Bias & boost amplifier.

POWER and GROUND

Pin Name	Pin Number	I/O	Description
DV_{CORE} 1.4V to 1.9V	1	I/O	*CAUTION: DO NOT APPLY 3.3V TO THIS PIN!* Filter connection for internal core voltage regulator. If pin 9 is connected to 3.3V DV_{DD}, this pin must be connected to filter caps: 10uf, 1.0uf & 0.1uf connected in parallel between pin 1 and DV_{SS} (pin 4). *Direct, filtered 1.4V to 1.9V DV_{DD} may be applied to pin 1 to lower the Digital power requirements. Pin 9 MUST be connected to pin 1 in this case.*

MICRO-STAR INT'L CO., LTD.

Title	Azalia Codec-ADI 1884		
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LPC length should be less than 18 inches.

LPC SUPER I/O SMSC 5327

U5 — SCH5327

Floppy Interface | Parallel Port | COM1 | COM2 | KBD & Mouse | LPC Interface | Miscellaneous | SMBus | Power Mangement | RST Gen. | LEDs | Digital Sensor

SCH5327 Delta PAS Rev 0.28

B02-0532704-S32

for EMI solution 2007/08/16

DEFAULT USE CHIP RST

HP RECOMMAND 2007/08/06

SB700 Internal Pull-High

installed R2 for AMD recommend 2007/10/19

TPM 1.2

U40 — SLB9635TT1.2/TSSOP28

TPM_ADDR :
0x02E (Low)
0x04E *(High) Default

TPMPP1 Default 1-2 (GND)
PP : Physical presence
standard connect to GND.

Reserved

SB700 Internal Pull-High

(Place capacitor close to IC)

SYSOPT Strap (RTS1~):
R124 - 0x2E* DEFAULT
R144 - 0x4E

R147 changed pull up to VCC_DDR 2007/10/18

ICH, CNR, DIMMS, CLK GEN — SMB_CLK_M, SMB_DAT_M, PWRGD_SD — SCH5317 (SEE NOTE) — SMB_CLK_R, SMB_DAT_R — ICH, PCI

Add the detection circuit for 4-pin 12V connector from the power supply. 2007/08/13

MICRO-STAR INT'L CO., LTD.	
Title	SIO-SMSC5327 / TPM
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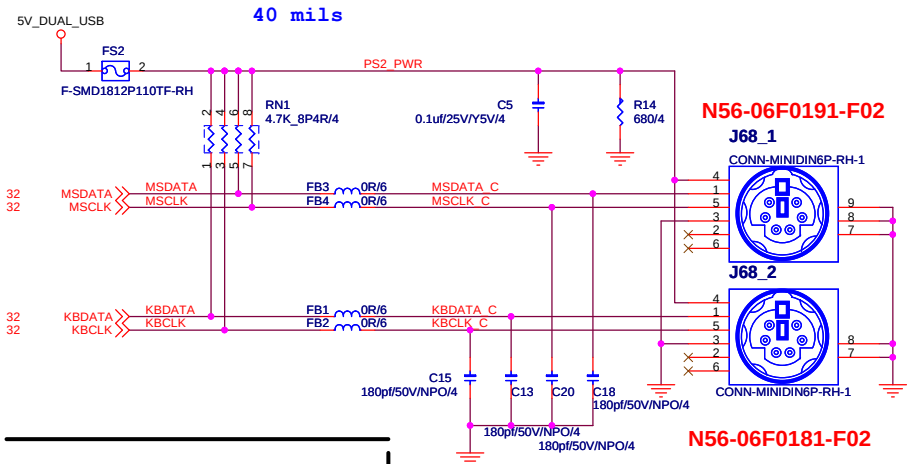
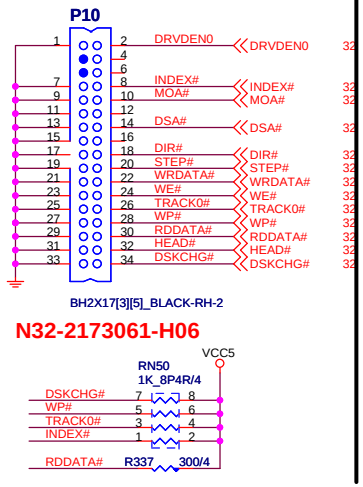
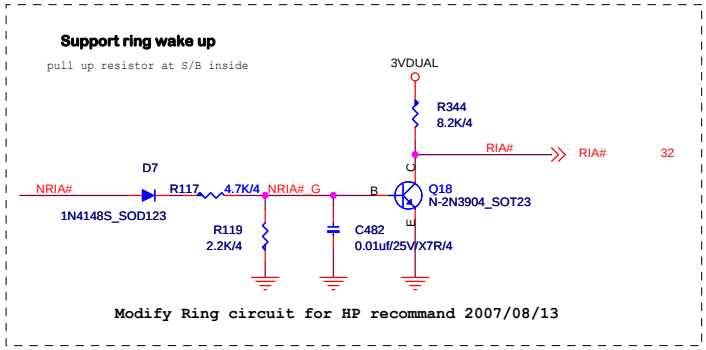
PS2 KEYBOARD & MOUSE CONNECTOR

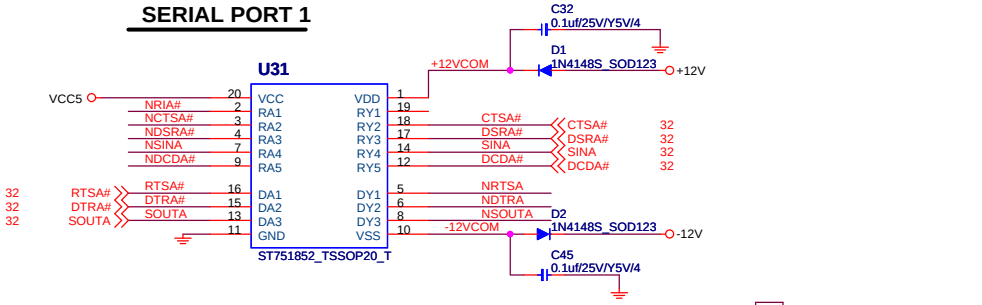


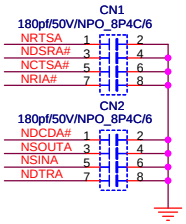
FLOPPY CONN BOLCK

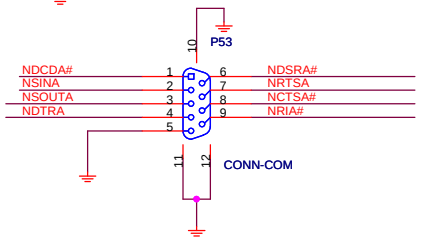




SERIAL PORT 1







SERIAL PORT 2

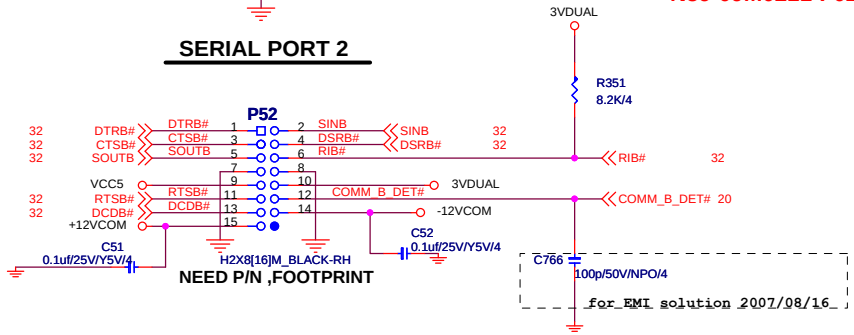


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

MICRO-STAR INt'L CO., LTD.

Title	KB/MS&COM1&Floppy Conn.	
Size	Document Number: MS-7500	Rev: 0C
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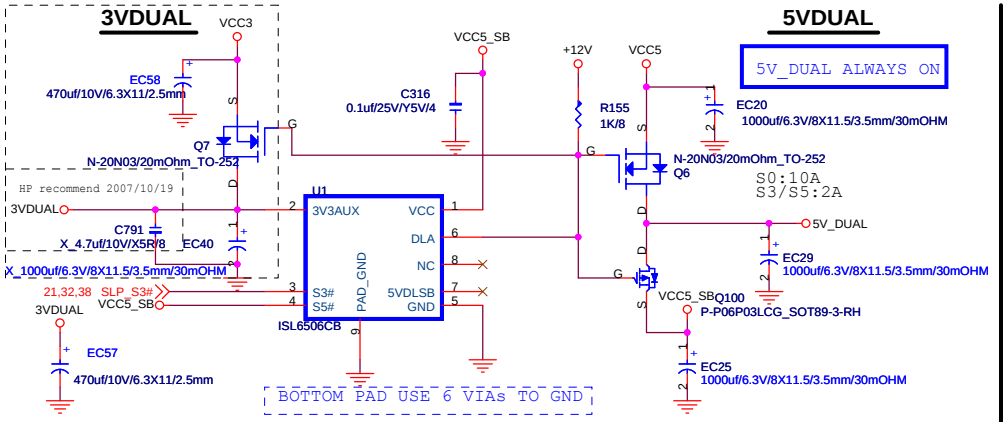
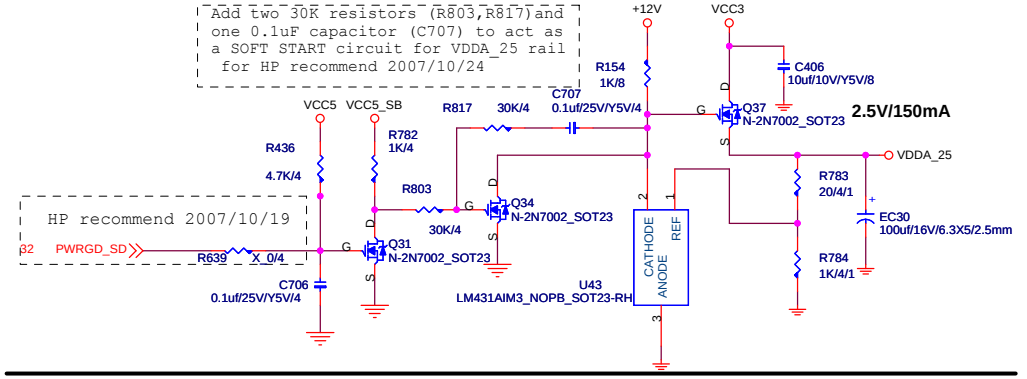
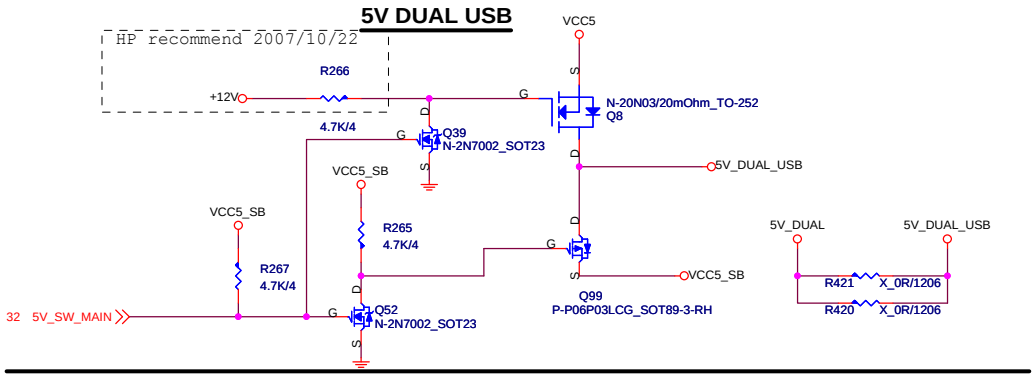
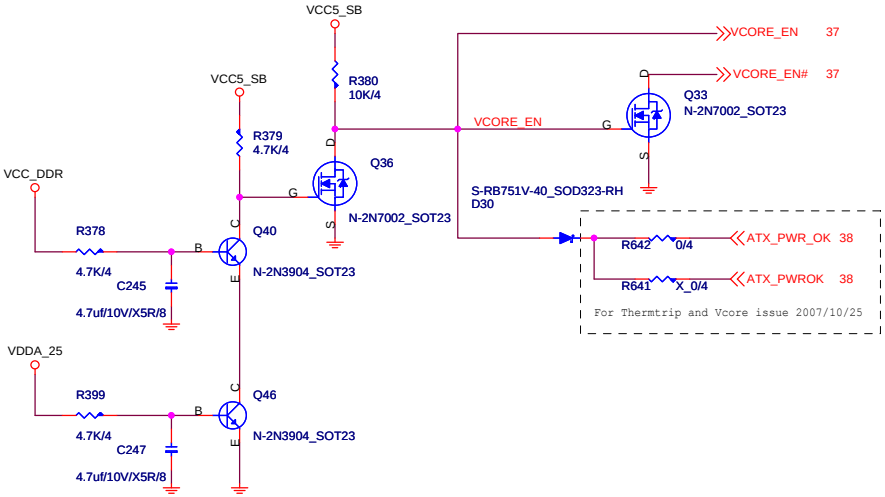


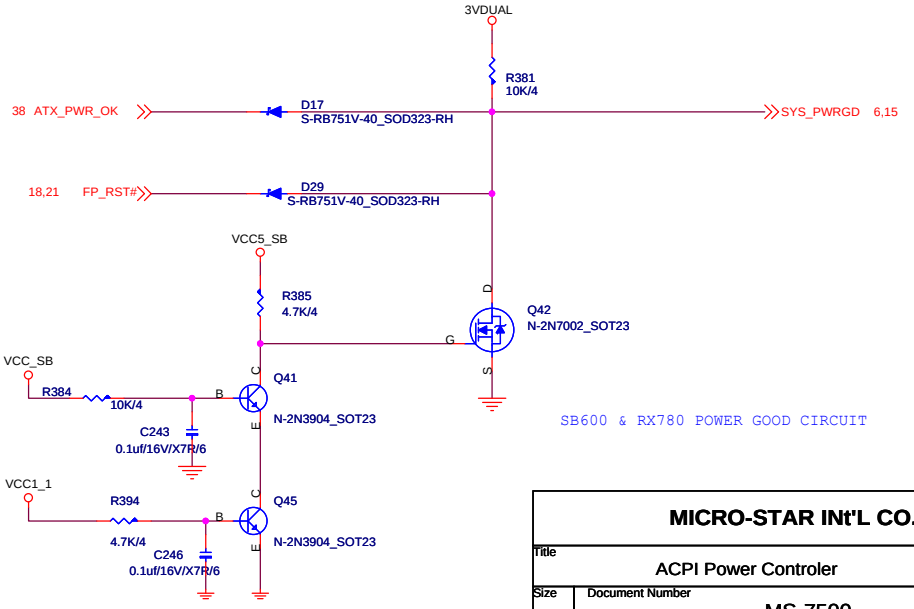
ACPI POWER STATE SUPPORT

Voltage	S0/S1	S3	S4/S5	S5	No AC
3.3 V Main	On	Off	Off	Off	Off
5 V Main	On	Off	Off	Off	Off
12 V	On	Off	Off	Off	Off
-12 V	On	Off	Off	Off	Off
CPU Core Voltage	On	Off	Off	Off	Off
RS780 core/SB600	On	Off	Off	Off	Off
1.8 V DDR2_VDDQ	On	On	On	Off	Off
0.9 V DDR2_VTT	On	On	On	Off	Off
5 V Standby	On	On	On	On	Off
3.3 V Standby	On	On	On	On	Off
5 V Dual (USB-PS/2)	On – main	On – aux	Off	Off	Off
5 V Dual (Memory)	On – main	On – aux	On – aux	Off	Off
3.3 V Dual (PCI)	On – main	On – aux	On – aux	On – aux	Off
3.3 V LAN (EPW)	On	On	On	On	Off
3.3 V Digital Audio	On	On	Off	Off	Off
5 V Analog Audio	On	Off	Off	Off	Off
Battery/RTC Voltage	On	On	On	On	On









MICRO-STAR INt'L CO., LTD.

Title	ACPI Power Controler	
Size	Document Number: MS-7500	Rev: 0C
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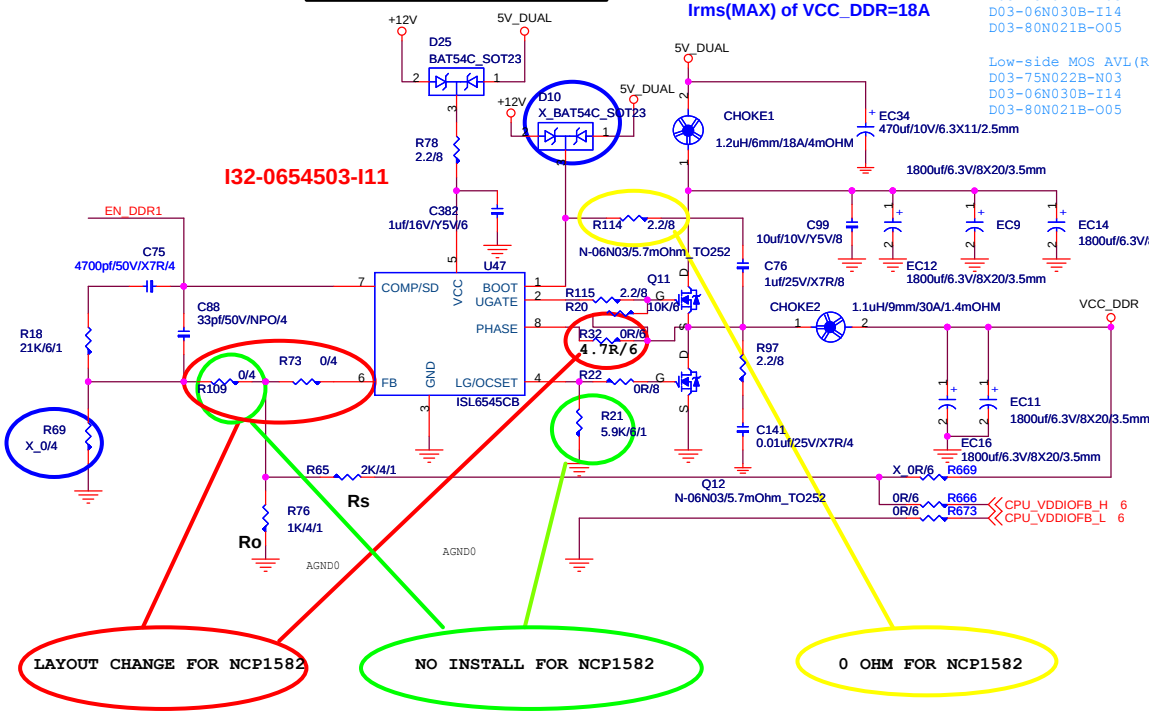
DDR II 1.8V POWER

Irms(MAX) of VCC_DDR=18A

High-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

Low-side MOS AVL(RoHS):
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

I32-0654503-I11



LAYOUT CHANGE FOR NCP1582

NO INSTALL FOR NCP1582

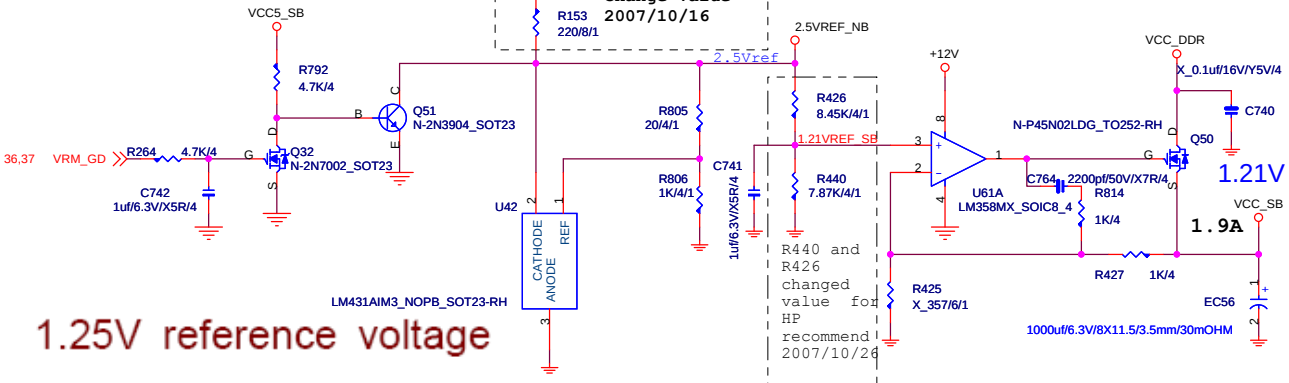
0 OHM FOR NCP1582

for Intersil
D10, R69 not install R109 0 ohm R32 0 ohm R114 2.2 ohm R21 5.9K ohm
for ON-semi
D10 BAT54C R109 not install R32 4.7 ohm R114 0 ohm R21 not install R69 0 ohm

$$I_{PEAK} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (21.5μA

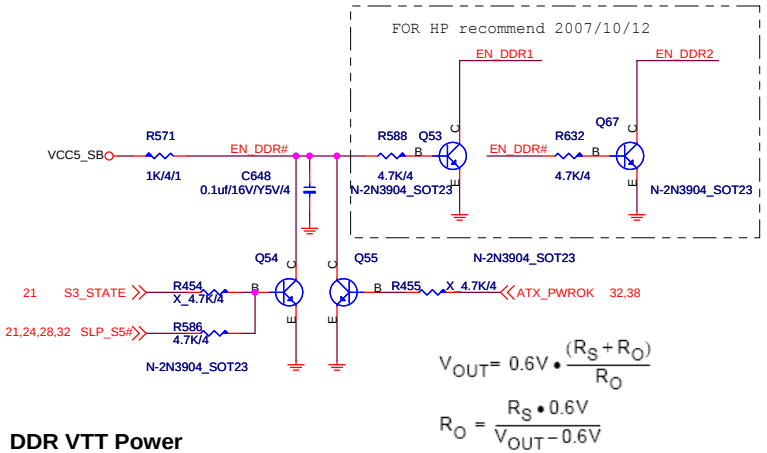
SHUTDOWN CONTROL						
Shutdown Pin Enable Threshold	–	VSD	1.14	1.24	1.34	V



1.25V reference voltage

Co-lay ISL6545 and NCP1582A

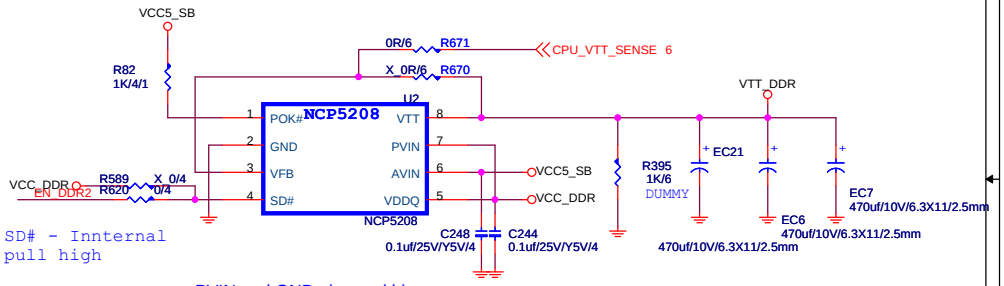
reserved for NCP1582A



$$V_{OUT} = 0.6V \bullet \frac{(R_S + R_O)}{R_O}$$

$$R_O = \frac{R_S \bullet 0.6V}{V_{OUT} - 0.6V}$$

DDR VTT Power



SD# - Innternal pull high

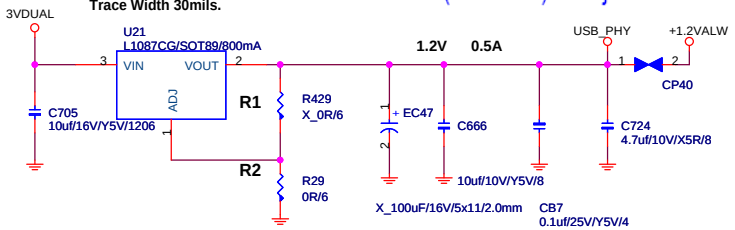
PVIN and GND pin need big power plane

at least 3 vias to inner power plane

I31-0520803-O05

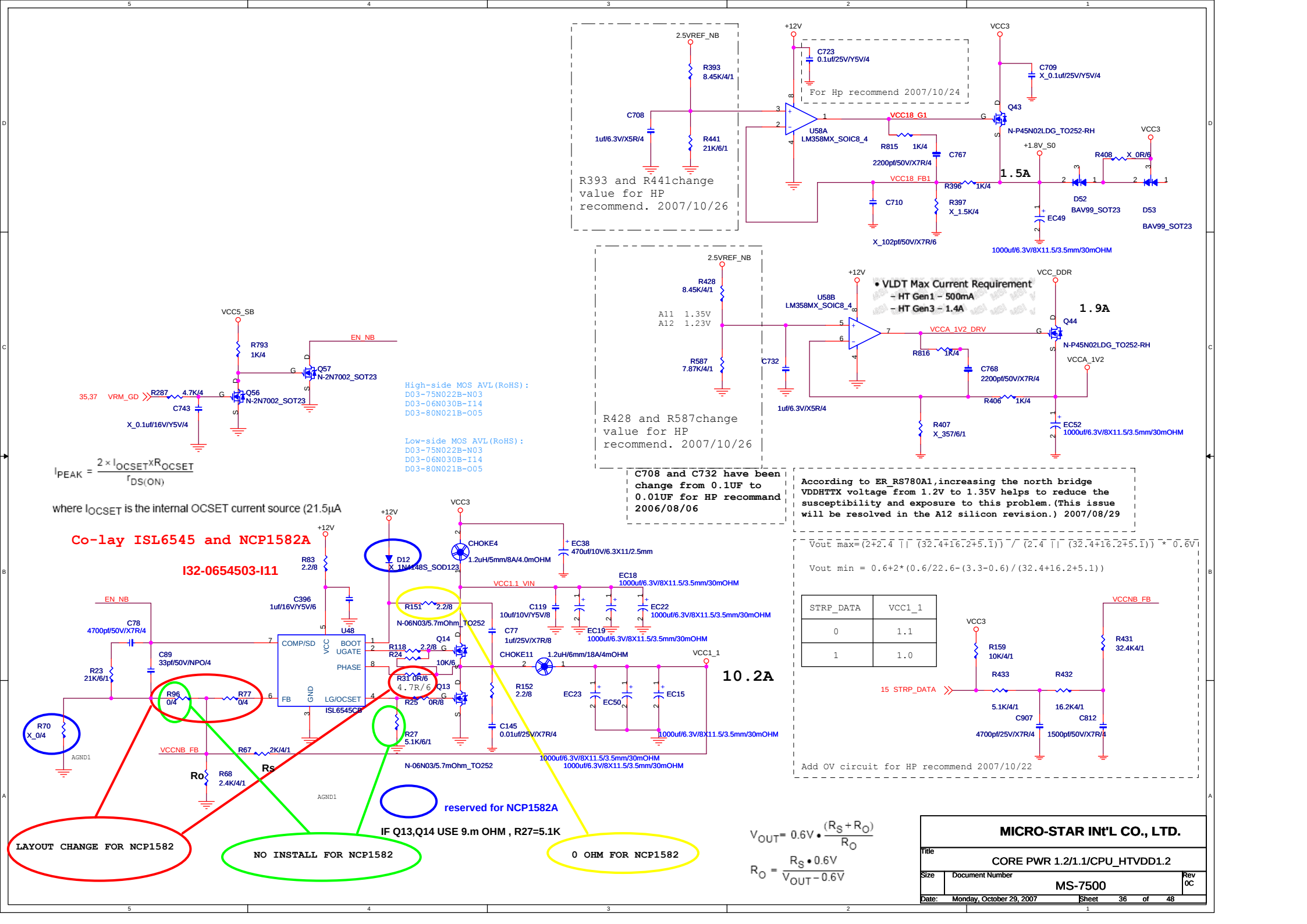
I31-0520803-O05

Vo = Vref (1+R2/R1) + ladj x R2



R429 has been un-populated and R29 has been populated for U21 heat 2007/08/01

MICRO-STAR INt'L CO., LTD.		
Title: Sys. Regulators / DDR		
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 35 of 48	



Title	CORE PWR 1.2/1.1/CPU_HTVDD1.2
Size	Document Number: MS-7500
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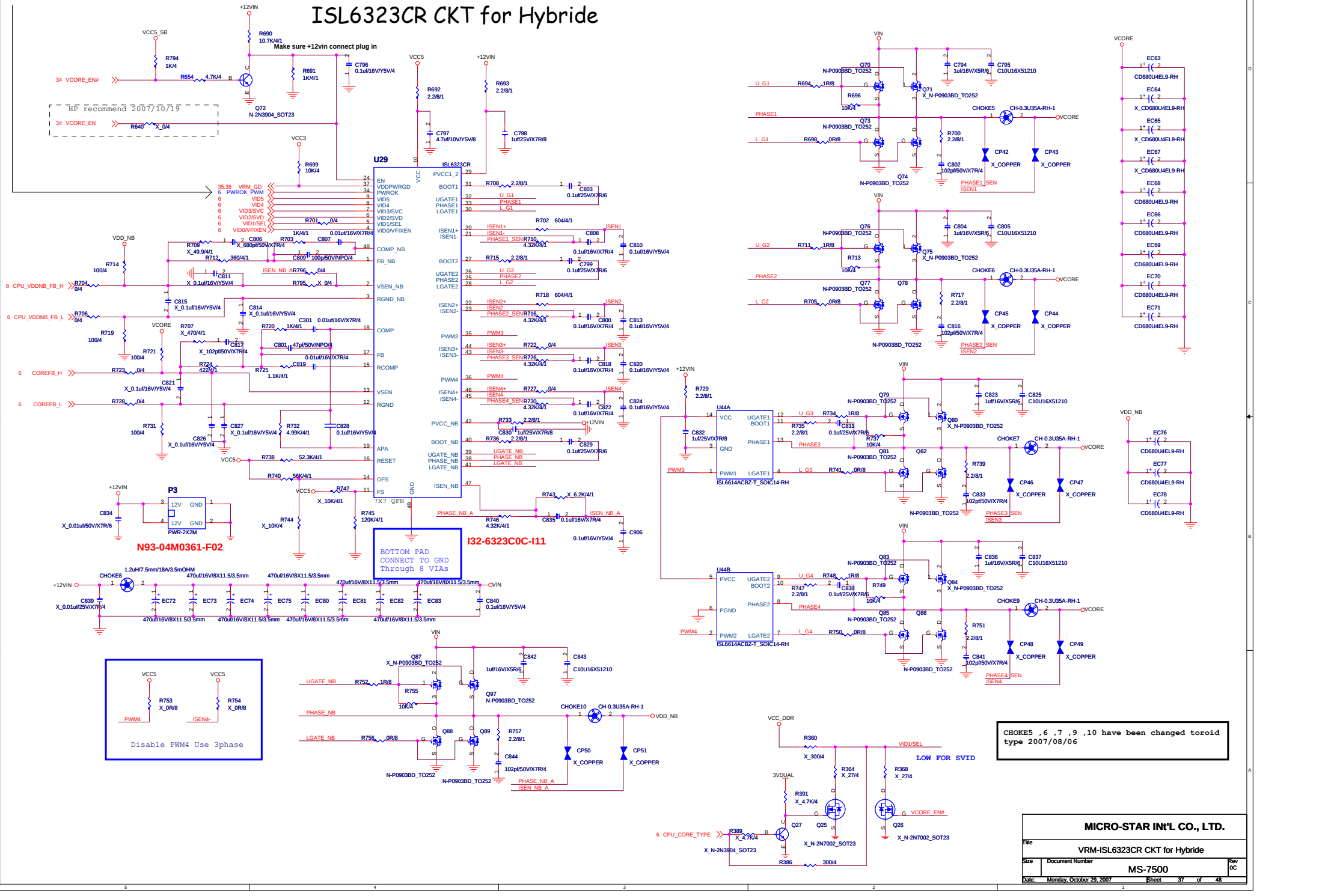
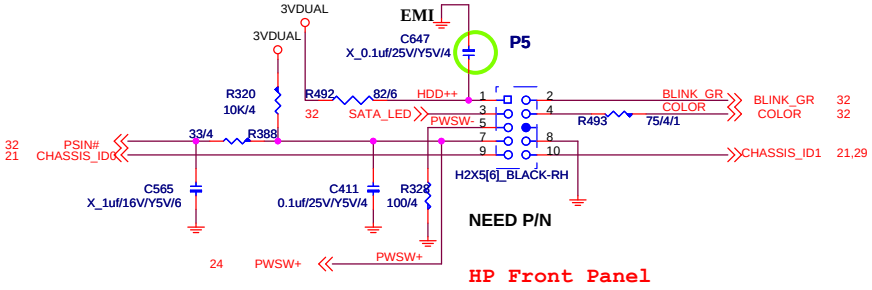
MICRO-STAR INt'L CO., LTD.

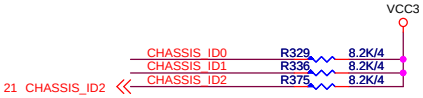
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWROK Input HIGH Threshold		2	-	-	V
PWROK Input LOW Threshold		-	-	0.8	V

ISL6323CR CKT for Hybride



Front Panel





HD_LED +	1	2	PWR_LED + (BLINK)
HD_LED -	3	4	PWR_LED – (COLOR)
GND	5	6	(key)
POWER_BUTTON#	7	8	GND
CHASSIS_ID0	9	10	CHASSIS_ID1

ATX Connector

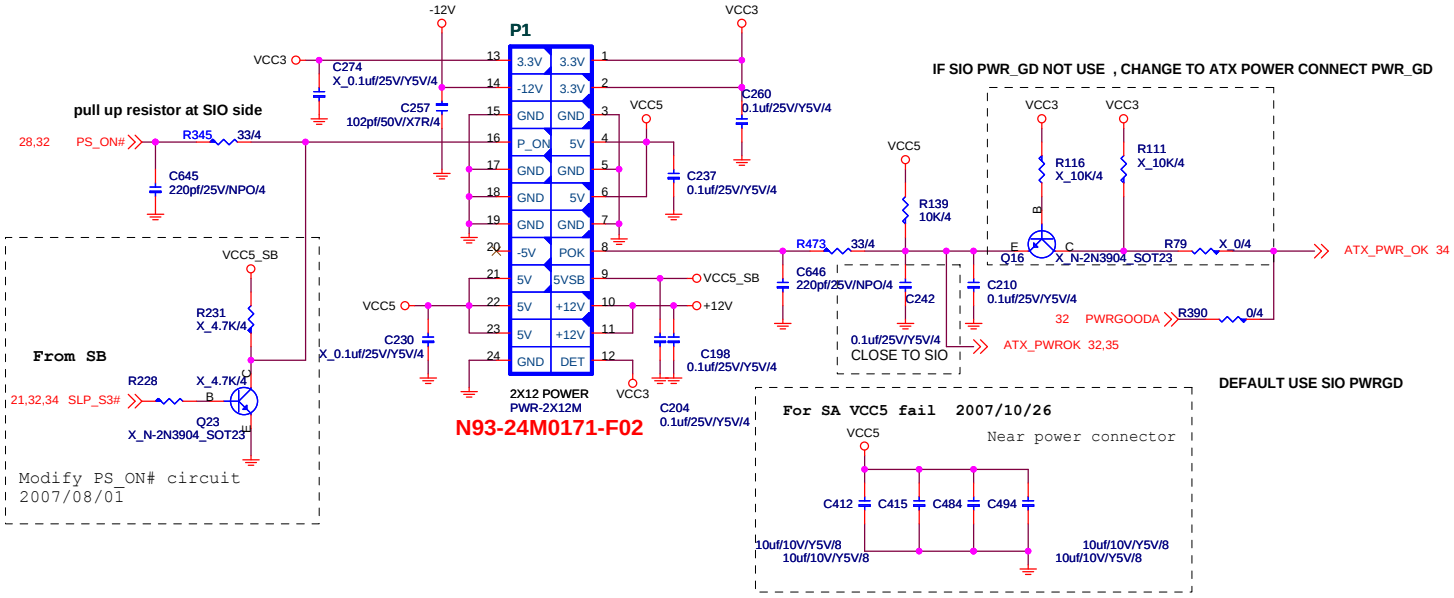


TABLE 5
POWER SUPPLY CONNECTOR PINOUT

	P1		
+3.3 V	13	1	+3.3 V
-12 V	14	2	+3.3 V
GND	15	3	GND
PSON#	16	4	+5 V
GND	17	5	GND
GND	18	6	+5 V
GND	19	7	GND
NOT USED	20	8	POWER OK
+5 V	21	9	+5 V STANDBY
+5 V	22	10	+12 V
+5 V	23	11	+12 V
GND	24	12	+3.3 V

MICRO-STAR INt'L CO., LTD.

Title	Front Panel	
Size	Document Number: MS-7500	Rev: 0C
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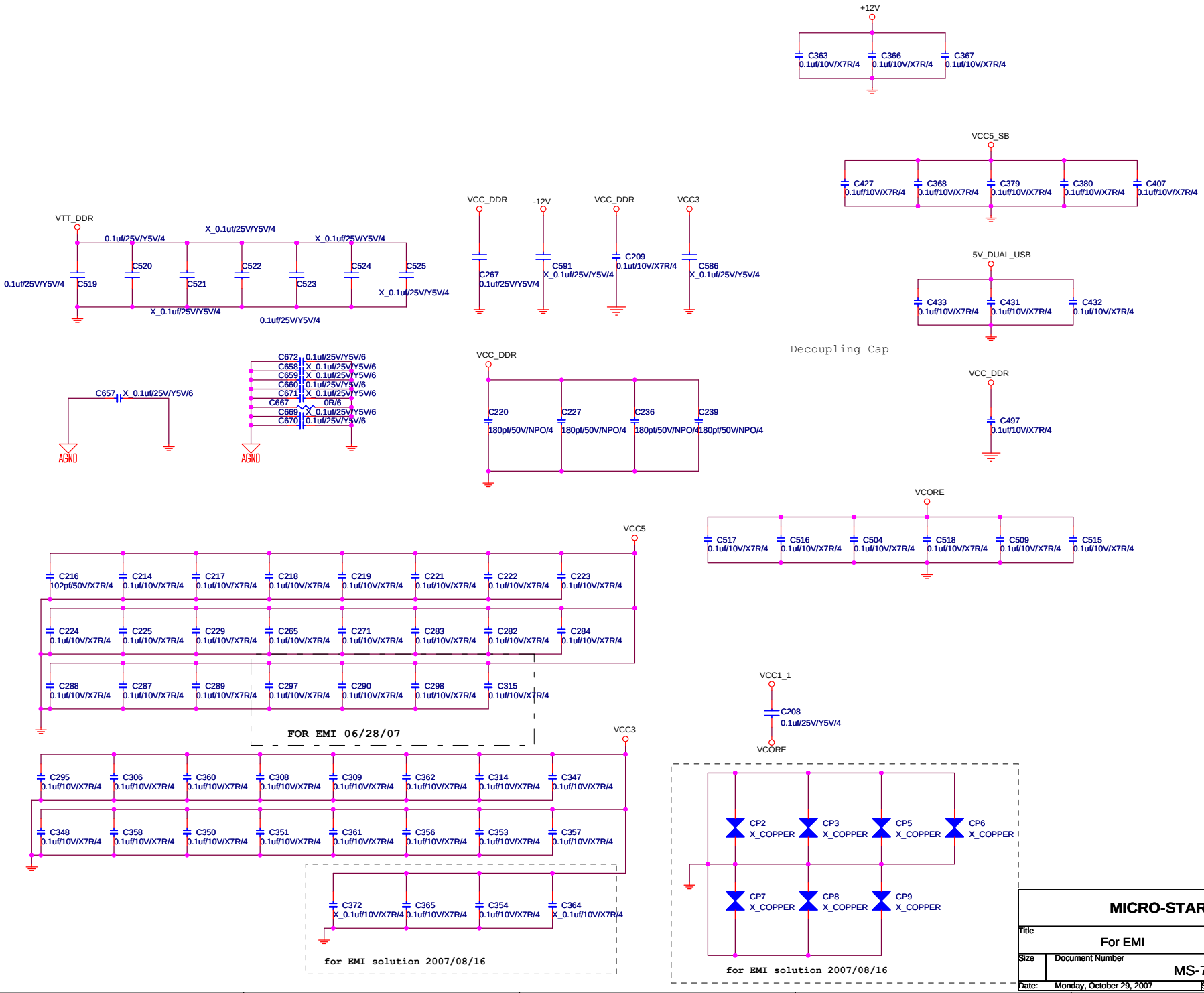

MICRO-STAR INt'L CO., LTD.		
Title: For EMI		
Size	Document Number: MS-7500	Rev: 0C
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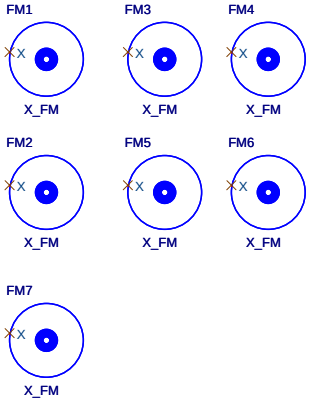
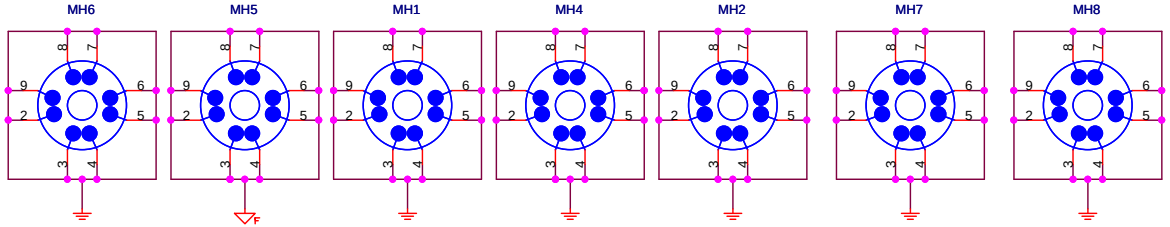
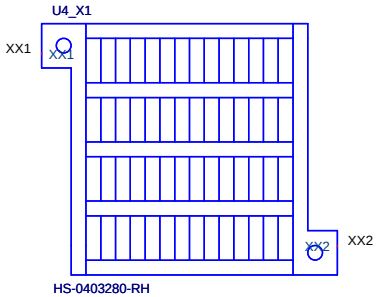
Optics Orientation Holes

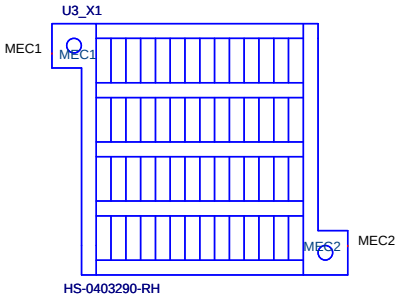


Mounting Holes

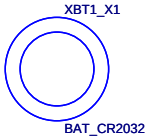


NB/SB FAN/HEAT-SINK



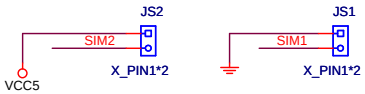


BATTERY

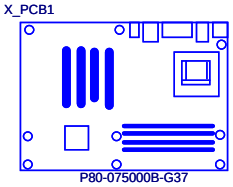


BIOS

Simulation



PCB



MICRO-STAR INt'L CO., LTD.		
Title: BOM - Option Parts		
Size	Document Number: MS-7500	Rev: 0C
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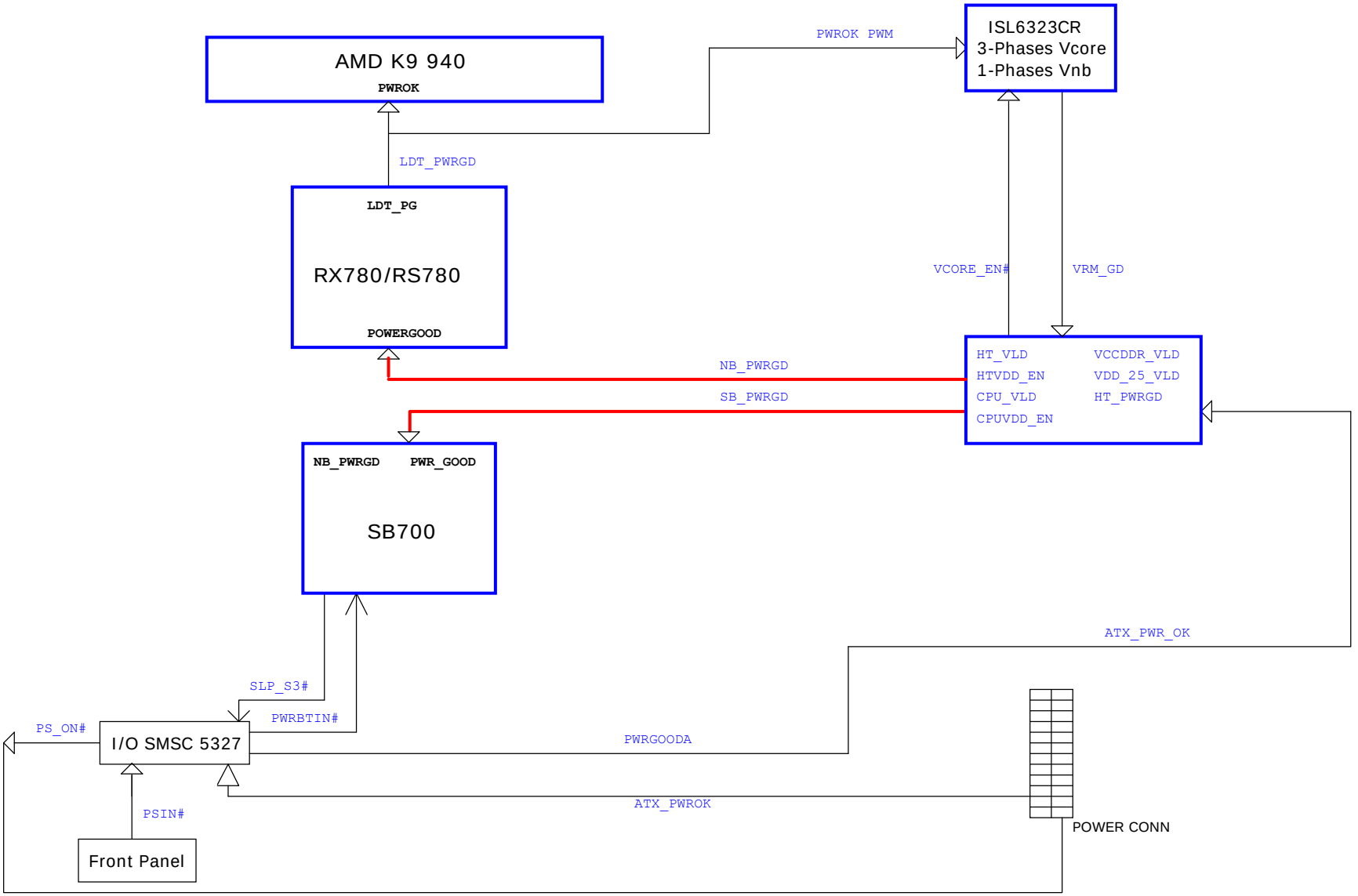
PWROK MAP



MICRO-STAR INt'L CO., LTD.		
Title: PWROK MAP		
Size	Document Number: MS-7500	Rev: 0C
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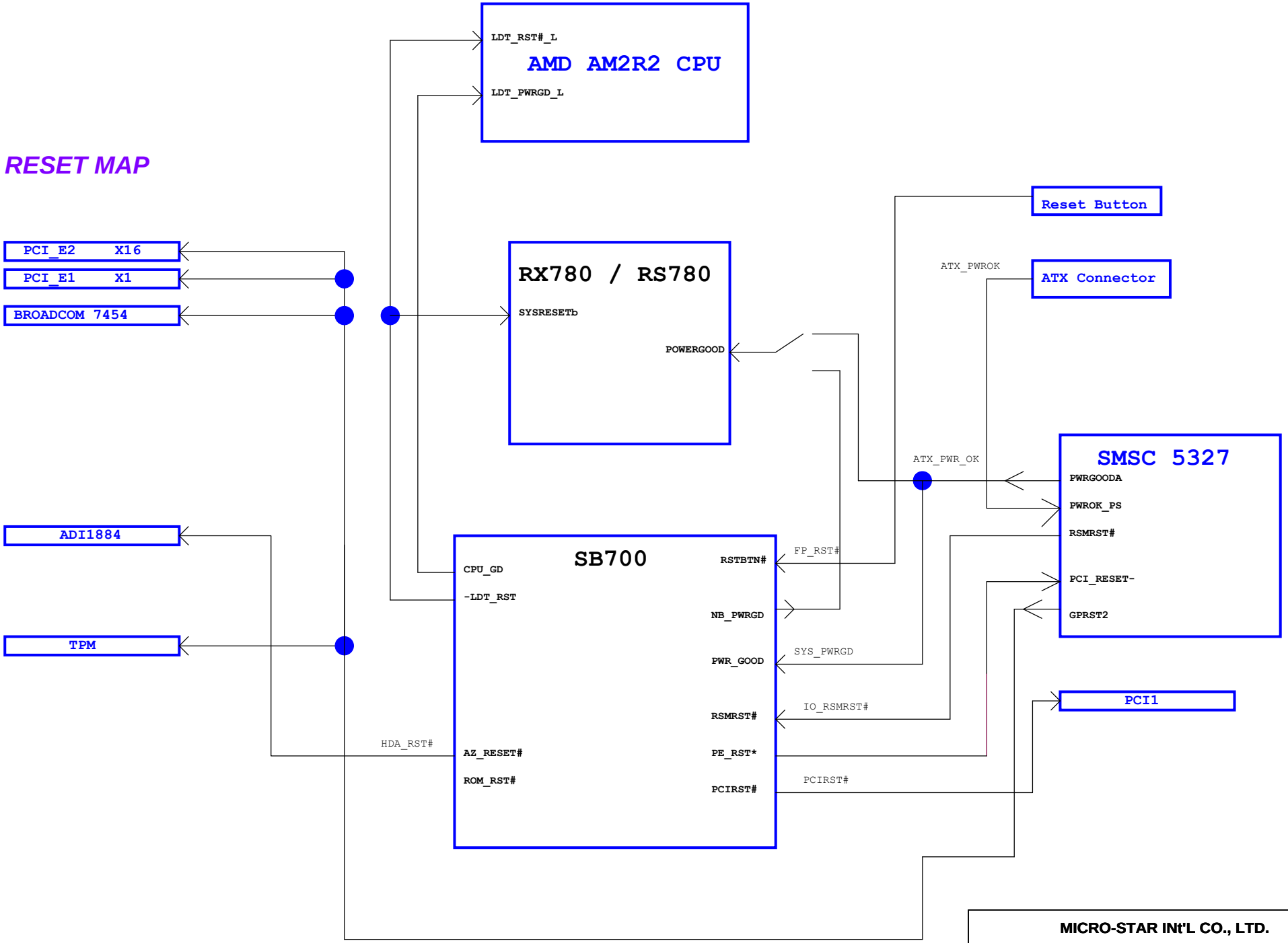

MICRO-STAR INt'L CO., LTD.		
Title: RESET MAP		
Size	Document Number: MS-7500	Rev: 0C
Date: Monday, October 29, 2007	Sheet 42 of 48	

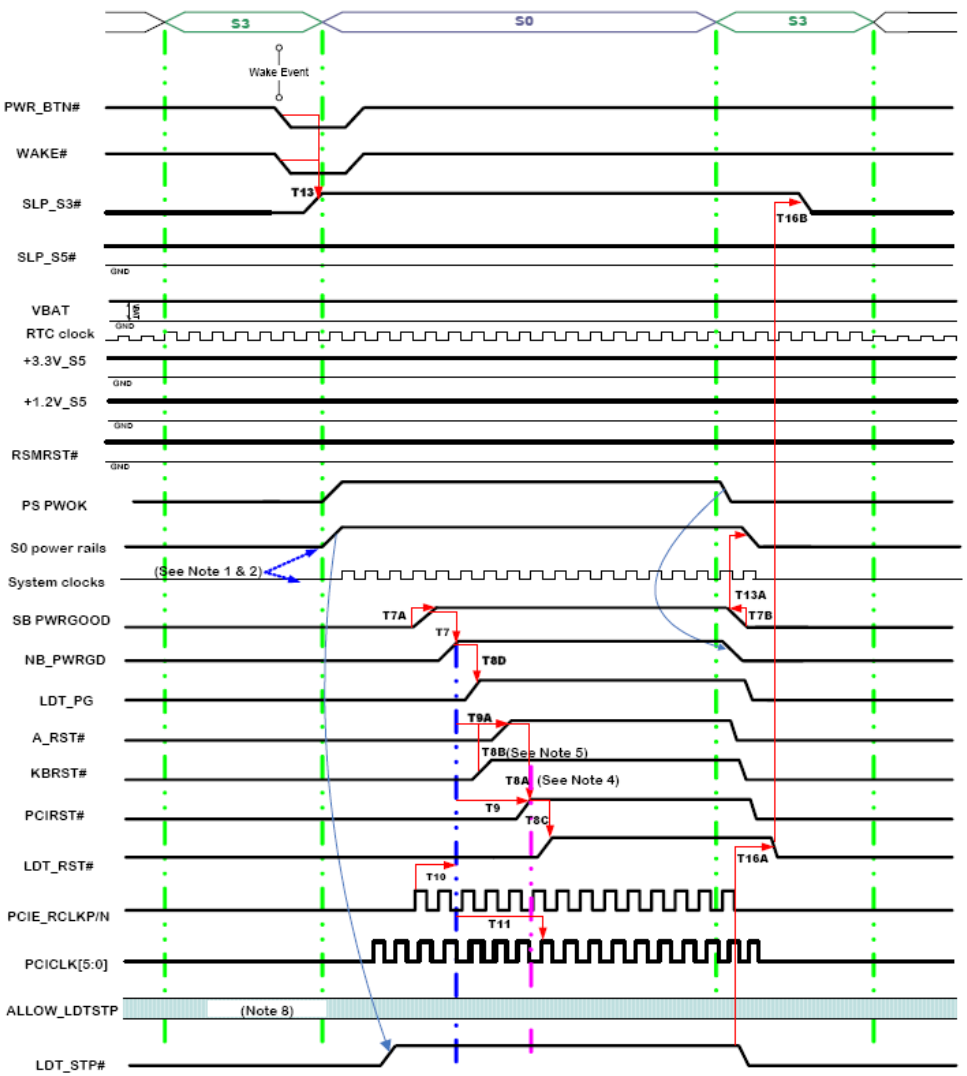

Figure 4-1: SB700 Power Up/Down Sequence

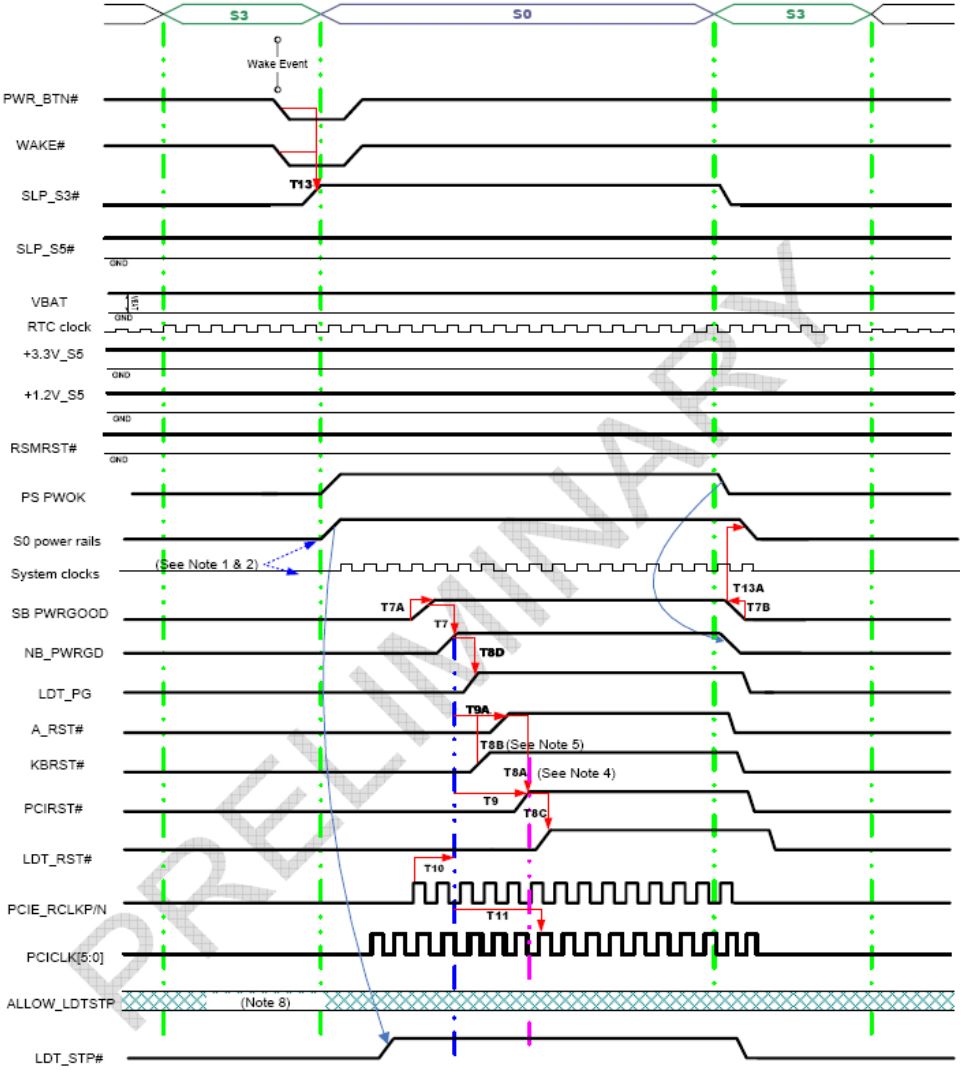

Figure 4-2: SB700 S3/S0 Power Up/Down Sequence

MICRO-STAR INt'L CO., LTD.		
Title: Power Sequence		
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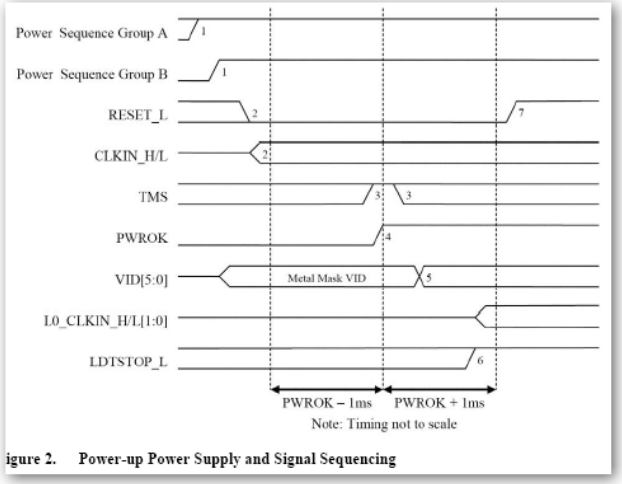

igure 2. **Power-up Power Supply and Signal Sequencing**

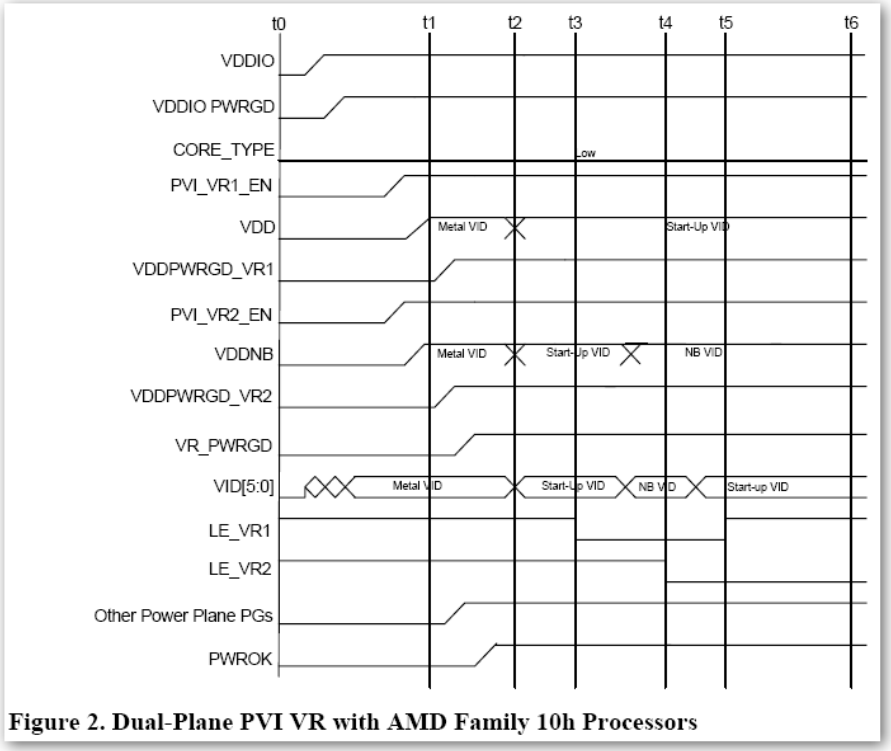

Figure 2. Dual-Plane PVI VR with AMD Family 10h Processors

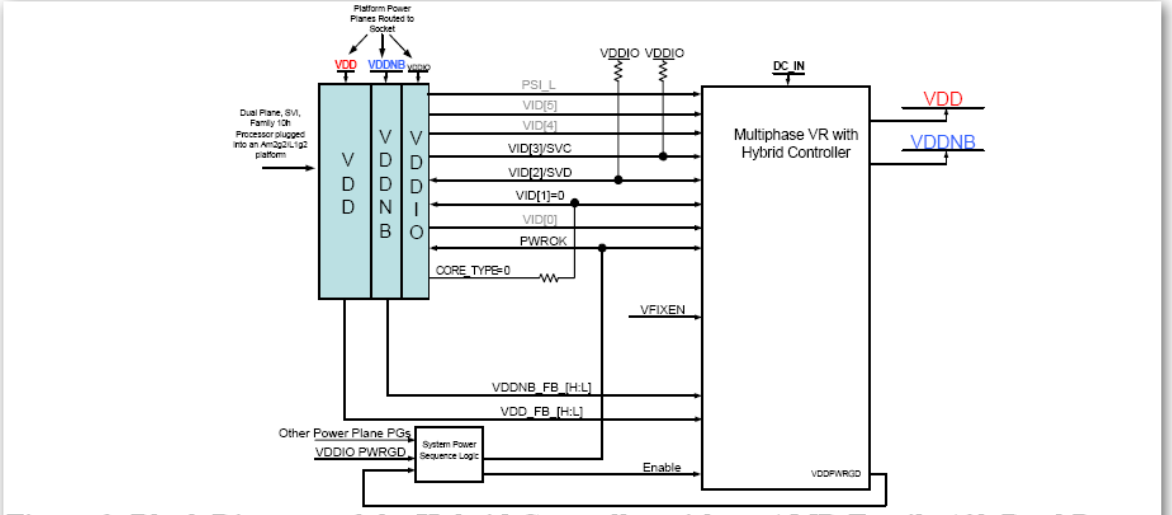

Figure 9. Block Diagram of the Hybrid Controller with an AMD Family 10h Dual Power Plane Processor (or Later) Operating in SVI Mode

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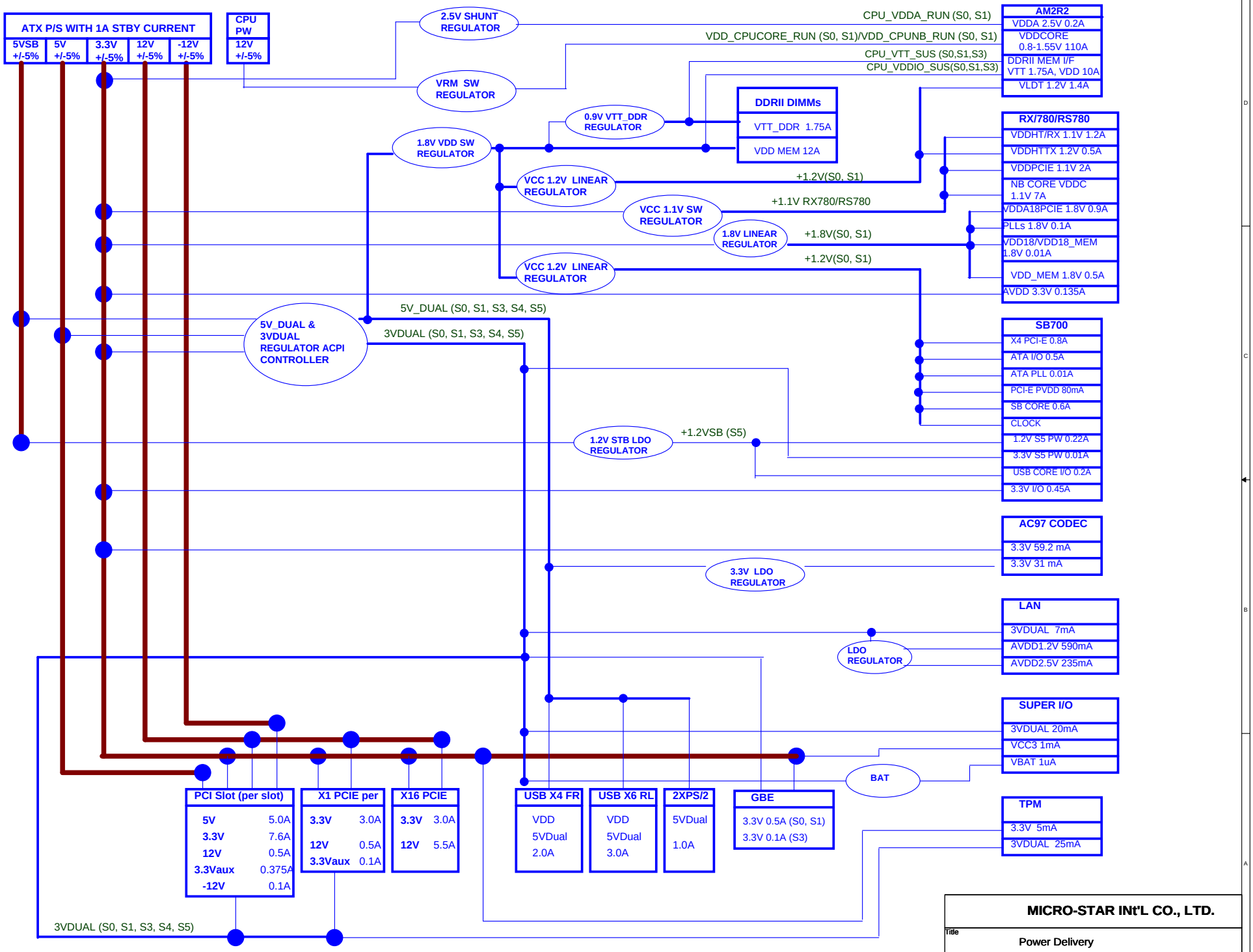

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06/05/07 Preliminary release

06/15/07

Page 06:R108,R109,R657 AND R658 have been deleted.

Page 15:C542,C597 AND C745 have been added(FOR EMI).

Page 15:R93,R126,R165,R190,R199 R201,R167,R204,R270,R255,R179,R222,R236 and R248 have been deleted(using external CLK-GEN)

Page 15:R175,R179,Q15 and R291 have been added(level-shift for ALLOW_LDTSTOP).

Page 15:R197,R45 and R47 have been deleted(DVI single channel).

Page 18:R338,R339,R340 AND R361 have been deleted(using external CLK-GEN)

Page 19:R176,R211,R214 AND R215 have been deleted(using external CLK-GEN)

Page 19:R242 AND R250 have been deleted.

Page 19:R125 PULLUP 3VDUAL.

Page 19:Add R276.

Page 23:R285,R183,R212,R186,R288,R203R,R189,R366,R357,R352,R351and R344 have been deleted(SB700 HAS 15K INTERNAL PULLUP FOR PCI_AD[30:23)

Page 24:R187,R431,R433 AND R432 have been deleted(using external CLK-GEN)

Page 25:R408,R409,R394,R402,R414,R415,R410,R424,R430,R422 and R423 have been deleted(using external CLK-GEN)

Page 28:R625,R626,R627,R628,R629,R630 have been deleted(using DVI single channel)

Page 31:C771 and C746 have been added(FOR EMI).

06/22/07

Page 06:C157,C158,R99 have been unpopulated,RN3 and R102 have been populated.

Page 06:U51,RN2 have been deleted(for AMD recommand),R74 and J80 have been added.

Page 06:Add R183 and Q17(level-shift).

Page 15:R42,RN43 and Q104 have been deleted,U62 has been added.

Page 15:R172,R175,R181,R192 and R187 have been changed from 3Kohm to 4.7Kohm.

Page 15:R182 has been changed from 2Kohm to 10Kohm.

Page 15:C570 has been changed from 2.2uF to 4.7uF.

Page 17:Add ferrite bead L18,L26,L27,FB19,FB22.

Page 18:L10,L13,L16 and L20 have been populated.

Page 18:C654 and C661have been changed from 10uF to 22uF.

Page 18:C655 and C733 have been changed from 1uF to 2.2uF.

Page 15:R161,R223,R230 and R231 been changed from 10Kohm to 8.2Kohm.

Page 19:R241 has been changed from 5.1Mohm to 20Mohm,R242 has been added.

Page 19: C323,C354,Y4,R168 have been deleted.U4.J21 connected to GND(25M_X1).

Page 20:L29,C412,C924 have been unpopulated.

Page 21:RN36,RN38,Rn35,RN39,Rn40,C372,C511,C535 and C707 have been deleted,R278,R279 and R280 have been added.

Page 21:Add R186 and Q22 (level-shift).

Page 21:SMBDATA1 and SMBCLK1 have been connected U10.

Page 22:Add C394,C513,C748,L22,L36,L41 and EC84,delete C484,C527,C723.

Page 22:C489,C717,C734,C735 and C772 have been changed from 10uF to 22uF.

Page 22:C378,C390,C480,C507,C508,C561,C563,C564,C567,C571,C714,C736,C744 and C747 have been changed from 0.1uF to 1uF.

Page 22:C392,C510,C527,C528 and C721 have been changed from 1uF to 2.2uF.

Page 23:R308,R318 and R333 have been unpopulated,R311 have been populated.

Page 25:Add RN 58,RN59,RN60.

Page 26:RN43,RN47 have been unpopulated.

Page 27:R180,R300 have been changed from 3Kohm to 4.7Kohm,and R89,R91 have been changed from 2.2Kohm to 6.8Kohm.

Page 28:R581~R585,R578~R580 have been changed from 18ohm to 18.2ohm,and R372,R374 have been changed from 2.2Kohm to 6.8Kohm.

Page 28:L21~L24 have been deleted.

Page 31:R177 has been changed from 10ohm to 22ohm.

Page 34:Add R394,C246 and Q45 (AMD recommand).

Page 35:Add R673 (CPU_VDDIOFB_L).

Page 35:Add C723,U22,R430,R30,C707,cb8 and C749 (for PA_SB700AA1).

Page 40:Add U4_X1 (SB HEATSINK).

06/26/07

Page 16:Add R807,R808,C34(for NB MEM_VREF).

Page 18:U6 has been changed from ICS9LPRS472 (MLF 64pin) to ICS9LPRS475 (TSSOP 56pin).

Page 18:R231and R223 have been deleted.

Page 20:L29 has been deleted and CP14 has been added.

06/27/07

Page 34:C245 has been changed from 0.1uF to 4.7uF.(power sequence)

06/28/07

Page 39:Add C290,C297,C298,C315 for EMI.

06/29/07

Page 15:R173,R135,R574,R196 have been deleted and R189,R190,R196 have been added.

Page 16:R148,R162,C202 and C203 have been unpopulated.

Page 19:Add R809,R810,C750,J81 FOR AMD debug.

Page 21:R125 has been deleted.

Page 22:C414 has been populated.

Page 24:R766 and R769 have been populated,R767 and R768 unpopulated.(for HP LAN LED spec)

Page 27:D44,D45 and D46 pin2 connect to VCC3.

Page 36:Add D52,D53.

07/04/07

Page 6:R64 has been unpopulated.

07/05/07

Page 34:Add R399,C247,Q46 for S3 function.

07/09/07

Page 13:Adding C920,C925 0.01uF stitching capacitors for crossing a split when these signals change different reference layer.

Page 19:Adding C751,C752 0.1uF stitching capacitors for crossing a split when these signals change different reference layer.

07/11/07

Page 21:Added C387 0.1uF stitching capacitors for crossing a split when these signals change different reference layer.

Page 32: R575 has been deleted.

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08/01/07

Page 15:Added R93 duo to NC7W207 output pin is op-drain .

Page 23:R325 and R323 have been changed from 10Kohm to 2.2Kohm.(AMD demo schematic update)

Page 29:Add R453 because modify SPI_HOLD# circuit for AMD recommend.

Page 32 :Modify PS_IN# circuit for can't boot issue.

Page 35 :R429 unpopulated and R29 populated for U21 too hot issue.

Page 36 :R430 unpopulated and R30 populated for U22 too hot issue.

Page 38 :Modify PS_ON# and ATX_PWR_GD circuit for can't boot issue.

08/07/07

Page 06:Added AMD Sensor Bus for HP recommend.

Page 15:Added U62.B and R108 for meet powr sequence.

Page 19:Added R248 for 3VDUAL short issue when clean CMOS.

Page 21:C377 and C373 have been unpopulate for meet power sequence.

Page 21:Added PRT_DET# circuit..

Page 25:Added R452,R449 and R451 for modify PE_RST# signal quality.

Page 27:Added NB THERM circuit for HP recommend.

Page 29:Modify Fan-circuit for HP recommend.

Page 32:R335 has been populated for SATA LED.

Page 32:Modify PE_RST# circuit for HP recommend.

Page 34:5V DUAL USB circuit have been populated.

Page 35:R153 has been changed from 220 ohm to 110 ohm for 2.5VREF_NB voltage isn't stable.

Page 37:CPU PWM circuit follow HOUNDS Ver 0B modified.

08/08/07

Page 29:Added FAN-PWM duty cycle inverter circuit for HP recommend.

08/09/07

Page 6:Added C70 for the voltage divider for the gates of the AMD SB-TSI translation circuit needs a decoupling cap.

Page 27: R592 has been populated and R615 has been un-populated for HP recommend .

08/13/07

Page 13: R34 and R36 have changed to 301 ohm 1% resistor when using RS780 for AMD recommend.

Page 14 and 19:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

Page 15: U62 pin5 and R108 pin1 have been connected to 3VDUAL for AMD recommend.

Page 15:Deleted R296. WD_PWRGD signal only connect to R439.

Page 16: C808 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.

Page 17: C598 and C599 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.

Page 19:SIO PCICLK has been Changed from PCICLK5 to LPCCLK1 for AMD recommend.

Page 20: Add R340 .(TEMP _COMM connect to GND for AMD recommend)

Page 21: Deleted R186 and Q22.(SB THRMTRIP# not Implemented)

Page 22: C734,C567,C563,C571,C747 have been un-populated when IDE or flash not using for AMD recommend.

Page 25:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

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08/13/07

Page 20:R341 and R319 have been un-populated.(SB700 internal pull-up).

Page 20:Deleted C412 and C924.(SB HW Monitor).

Page 29:Modify Parall port circuit for HP recommend.

Page 29:Added E17(SPI Write Protection) for HP recommend.

Page 29:Modify FAN-PWM duty cycle inverter circuit for HP recommend.

Page 32:Add the detection circuit for 4-pin 12V connector from the power supply for HP recommend.

Page 33:Modify RING Wake Up circuit for HP recommend.

08/14/07

Page 15:R169 has been changed to 3K ohm and populated for RS780.

Page 15:R88 and R178 have been populated for RS780.

Page 15:R198 has been changed to 150 ohm and populated for RS780.

Page 15:R127 has been populated for RS780.

Page 21:Add R186,Q22 ,R199 level shift circuit to U4 THERMTRIP# for HP recommend.

Page 27:D39 has been populated for USB ESB protection.

Page 30:D8,D11,D20,D21,D32,D39 have been populated for USB ESB protection.

Page 31:Add C554 and C569 decouple cap for HP recommend.

Page 32:R335 has been un-populated for HP recommend.

Page 32:R144 has been changed to 470 ohm.

Page 32:U31 has been changed from 75232 to 75185.

Page 33:Net "RDDATA#"pull up resistance value change to 300 ohm.

Page 35:R454 and R455 have been un-populated.R586 has been changed to 4.7K ohm and populated.

Page 35:R21 has been changed to 5.9K ohm for MSI POWER TEAM recommend.

Page 36:R27 has been changed to 5.1K ohm for MSI POWER TEAM recommend.

Page 38:R228,Q23 and R231 have been un-populated.R345 and C645 populated.

08/16/07

Page 39:Added C372,C365,C354 and C364 for EMI.

Page 39:Added CP2,CP3,CP5,CP6,CP7,CP8 and CP9 for EMI.

08/20/07

Page 15:R188 and R254 have been uninstalled for RS780.

Page 21:R217 , R260 and C371 have been deleted.(for I2C signal)

Page 27:Add L6,L21 and L22 for EMI solution.

09/27/07

Page 15:R169 have been uninstalled for RS780.R184 installed 3K

For RS780 2007/09/06
reference AMD demo borard
SHINER rev 2.0 C)

Page 35:Changed EC9,EC12,EC14 from 1000uf to 1800uf that MSI POWER TEAM recommend.

Page 36:Changed R25 from 0ohm to 5.1k for MSI POWER TEAM recommend.

Page 37:Changed C807,C301,C819 to 10nf and R702,R718 to 604ohm for MSI POWER TEAM recommend.

10/03/07

Page 35, 36: Change C741, 708 and C732 from 0.01uF to 1uF for DDR power drop issue.

Page 18: Remove R235 for S3 issue.

10/09/07

Page 6: Uninstall R102 and R74 for HP recommended.

10/11/07

Page 12: Change C228, C123 and C231 from 0.1uF to 47pF for EMI.

Page 29: Change C668 from 0.1uF to 47pF for EMI.

Page 9: Install 100pF cap in C609, C194 and C689 for EMI.

Page 9: Change C169 from 180pF to 100pF for EMI.

Page 9: Change C207 from 0.1uF to 100pF for EMI.

Page 9: Install 10pF cap in C188 for EMI.

Page 9: Change C151 from 0.1uF to 10pF for EMI.

Page 9: Change C169 from 180pF to 10pF for EMI.

Page 9: Change C461 from 10uF to 0.1uF for EMI.

Page 9: Change C275 from 0.22uF to 33pF for EMI.

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10/05/07

Page 39: Added C220, C227, C236, C239 and C216 for EMI.

Page 18: Reserved C249 and C241 for EMI.

Page 20: Following AN_SB700AB2.pdf to added 0 ohm series resistor on SATA_TX [5:0]P/N.
R624, R625, R626, R627, R628, R629, R630 and R631

Page 31: Conneted C291, C294, C299, C300, C619, C621, C769 and 770 to GND for Huston EMC lab recommend.

10/08/07

Page 35, 36: Reserved R814, R815, R816, C764, C767 and C768 for Houston lab recommened.

Page 6: Change R107 connected power from VCC_DDR to VBAT.

Page 15: Change the name of a net from SYRESTE# to SYRESET#.

10/12/07

Page 35: Added R588,R632 and Q67 for EN_DDR2 circuit.

Page 35: Added EC47 for USB_PHY POWER.(HP recommend)

Page 15: Deleted R302 ,unpopulated U62 and R108,added R304 and R357 for meet RS780 A12 spec. (AMD recommend)

Page 15: Unpopulated R176,R179,Q15,R170,R171 and Q10;populated R275 and R291 for meet RS780 A12 spec.(AMD recommend)

Page 28: Added L23,L24,L29 and L44 for EMI.

10/16/07

Page 34: Unpopulated EC40 for 3VDUAL issue.(prevent ISL6506CB into OCP state)

Page 35: Populated C742 for meet CPU power sequence.(AMD recommend)

Page 35: Changed R153 from 110 ohm to 220ohm.

10/18/07

Page 6: R107 changed to 10M ohm and R101 changed to 390 ohm for HP recommend.

Page 32: R147 changed pull up to VCC_DDR for HP recommend.

Page 32: Added R633,R634,R637 and R638 (0 ohm) for HP recommecd.

10/19/07

Page 6: Added 0 ohm R199(unpopulated) for HP recommend.(SYS_PWRGD connected to PWROK_PWM)

Page 15 16 : Added two 0.1uF cap (C35,C37) for HP recommend.

Page 34: Added 0 ohm R639(unpopulated) for HP recommend.(PWRGD_SD connected to Q31 pin G)

Page 37: Added 0 ohm R640(unpopulated) for HP recommend.(VCORE_EN connected to U29 pin 24)

Page 34: Added a 4.7uF cap (C791) for HP recommend.

Page 15: Changed R172 and R175 from 4.7K ohm to 39K ohm for AMD RS780 SCL.

Page 18: Changed R218 from 150 ohm to 158 ohm and and changed R229 from 75 ohm to 90.9 ohm for AMD RS780 SCL.

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10/19/07

Page 19: Uninstall R135 for AMD SB700 SCL.

Page 21: Added R268 and R270 for AMD SB700 SCL.

Page 21: Added R268 and R270 for AMD SB700 SCL.

Page 28: Changed R372 and R374 from 6.8K ohm to 15K ohm for AMD RS780 SCL.

Page 32: Install R2 for AMD SB700 SCL.

10/22/07

Page 15: Add R112 and connect U3C.D10 to PCI-E X16 SLOT(B17 B31 B48 B81) for HP recommend.

Page 15: NO_STUFF R81,R84 and R191 and connect A_RST# to SYSRESET# via 0 ohm (R282) for HP recommend.

Page 22: Deleted FB23.

Page 25: STUFF EC28 for HP recommend.

Page 26: Deleted R803,E1 and R438 for HP recommend.

Page 26: CP13,CP26,CP38 changed to 0ohm for HP recomemd (uninstalled).

Page 27: Deleted R615 R593 and R594 for HP recommend.

Page 27: Deleted R599,R602, R597, R598, R595, R596, R609, R608, R605, R606, C680, C679, C678, Q102, Q101 and P12 for HP recommend.

Page 27: Changed R159 from 10K ohm to 280 ohm and Changed R160 from 5K ohm to 330 ohmfor HP recommend.

Page 27: Deleted FS9,R159 and R160 for HP recommend.

Page 30: Changed R128,R131,R132 and R136 from 10K ohm to 280 ohm and Changed R123,R130,R133 and R138 from 5K ohm to 330 ohmfor HP recommend.

Page 34: NO STUFF EC40 and STUFF EC57 for HP recommend.

Page 34: Deleted D27 for HP recommend.(5VDUAL).

Page 35: C742 changed from 0.1uF to 1uF.

Page 36: Deleted U22,C723,R430,R30,C707,C749,CB8.

Page 36: Add OV circuit for HP recommend.

10/23/07

Page 15: R304 pin 1 connect to WD_PWRGD for HP recommend.

Page 20: CP14 pin 2 connect to 3VDUAL for HP recommend.

Page 39: J81 chanegd from a header 2*5 to two header 2*3 for AMD recommend .

10/24/07

Page 34: Add two 30K resistors (R803,R817)and one 0.1uF capacitor (C707) to act as a SOFT START circuit for VDDA_25 for HP recommend.

Page 35: R440 change from 1.5Kohm to 1.37K ohm for HP recommend .

Page 36: Add C723 for HP recommend .

Page 21: Add R445 pull up +3VDAUL to USB_OCP#4 for HP recommend .

Page 36: Changed R159 from 10K ohm %5 to 10 ohm 1%and Deleted R182 (same pull up VCC3 to STRP_DATA)

Page 19: Modify battery circuit for HP recommend .

10/25/07

Page 21: Deleted R445 and uninstall R439 for HP recommend.

Page 31: Changed EC42,EC43 from 10uF to 22 uF for HP recommend.

Page 34: Add R641,642 for thermtrip and Vcore issue .

10/26/07

Page 21: R129 changed from 11.8K 1% ohm to 11.3K 1% ohm for SA USB fail.

Page 27: C148,C143,C175 changed from 6pf to 2.2pf and C149,C144,C139 changed from 6pf to 3.3pf and L6,L21,L22 changed from 47nH to 0 ohm for SA VGA signals fail.

Page 35 R440 changed from 1.5K 1% ohm to 7.87K 1% ohm and R426 changed from 1.5k 1% ohm to 8.45K 1% ohm.

Page 36 : R393 , R428 changed from 1.5K 1% ohm to 8.45K 1% ohm and R587 changed from 1.74K 1% ohm to 7.87K 1% ohm and R441 changed from 4.21K 1% ohm to 21K 1% ohm for HP recommend.

Page 38: Add C412,C415,C484 and C494 for SA VCC5 fail.

10/29/07

Page 19: Add Add R144 foe HP recommend.

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