MS-6637 AIO 21.5" LCD PC

MS-7441 Version 0A

CPU:
Intel Yorkfield, Wolfdale,
Conroe, Conroe-1M, Conroe-L - 65W CPU
(FSB1333/1066/800)

System Chipset:
Intel EaglelakeG4X - GMCH (North Bridge)
Intel ICH10/ICH10R (South Bridge)

On Board Chipset:
I82567PHY Gb LAN
HD Audio Codec - Realtek ALC885
LPC Super I/O : Fintek F71882F
Clock GEN - IDTCV184-2
TPM - SLB 9635 TT1.2

Main Memory:
Dual Channel SODIMM DDR II-800*4 (Up to 4GByte)

Intersil PWM:
VRD11 Intersil 6326 (4phase)

Expansion Slots:
PCI-E[X1] Slot *2
MXM 3.0 Socket x 1

MS-6637N1	ERP Number	Functiom
MS-7441-XX	601-7441-XXX	Mainboard
MS-4180-020	604-4182-020	Side USB/ PWR BTN/OSD
MS-4181-010	604-4181-010	RT DP to LVDS
MS-4182-	604-4182-	MSt DP to LVDS

MS-XXXXN1	ERP Number	Functiom
MS-7441-XX	601-7441-XXX	Mainboard

Model type	Function	BOM Config	ERP BOM No	BOM Opt.
MS-7441N1-xx	Eaglelake G45+ICH10+TPM.	CFG-MA	601-7441-01	
MS-7441N1-xx	Eaglelake G45+ICH10+TPM+MXM3.0-A	CFG-MA-MX	601-7441-02	

CONTENT	SHEET

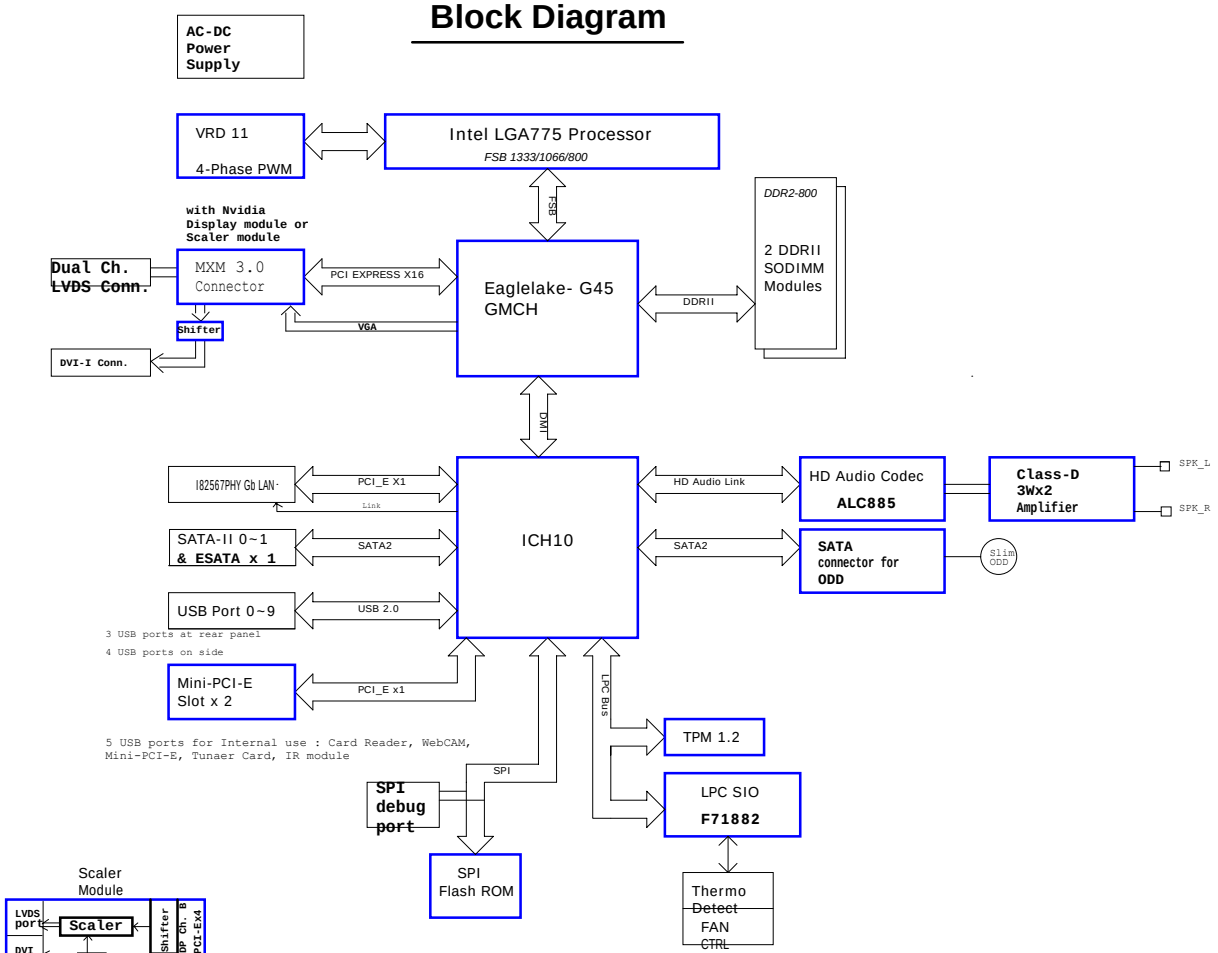
MICRO-STAR INT'L CO.,LTD

MS-7441N1

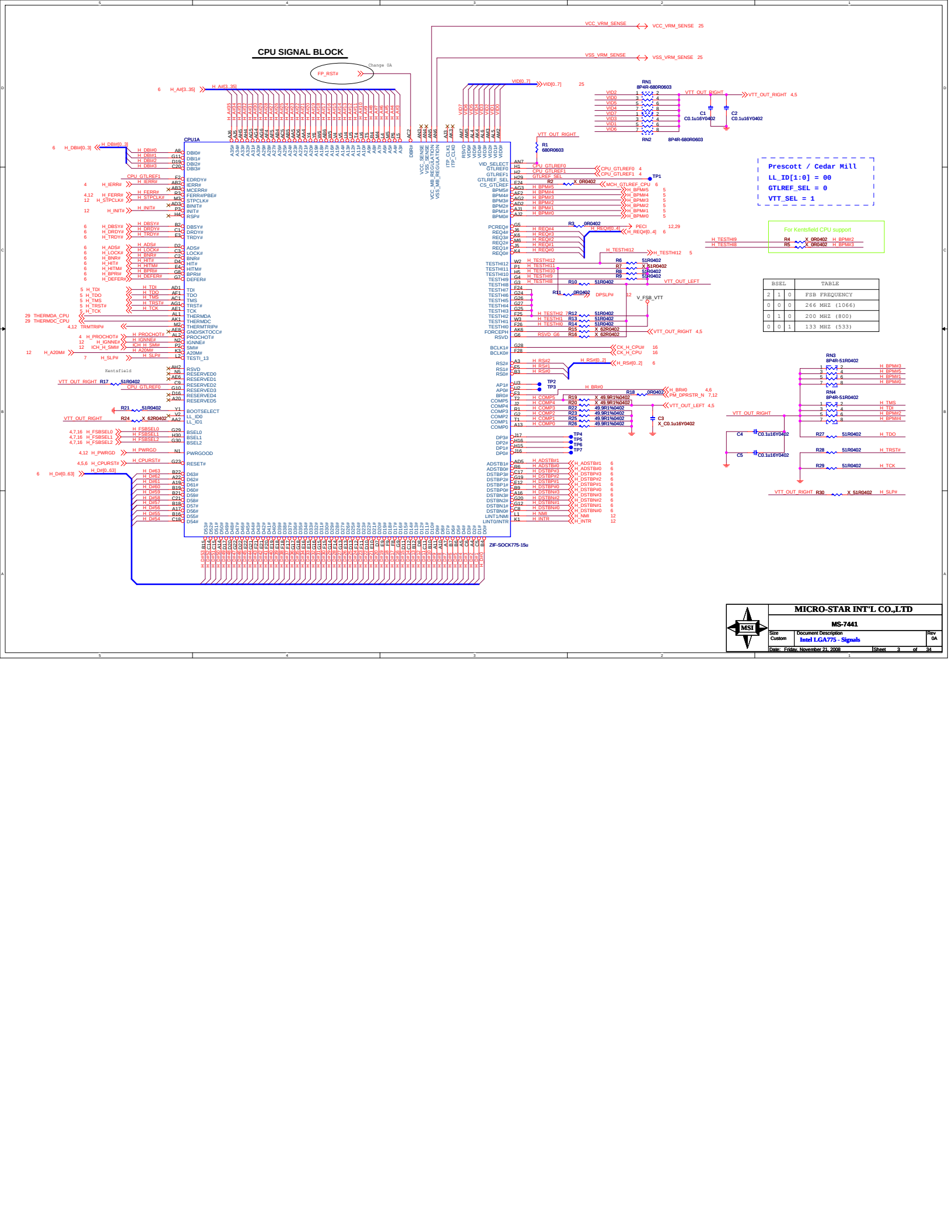
Size: Custom | Document Description: COVER SHEET | Rev: 0A

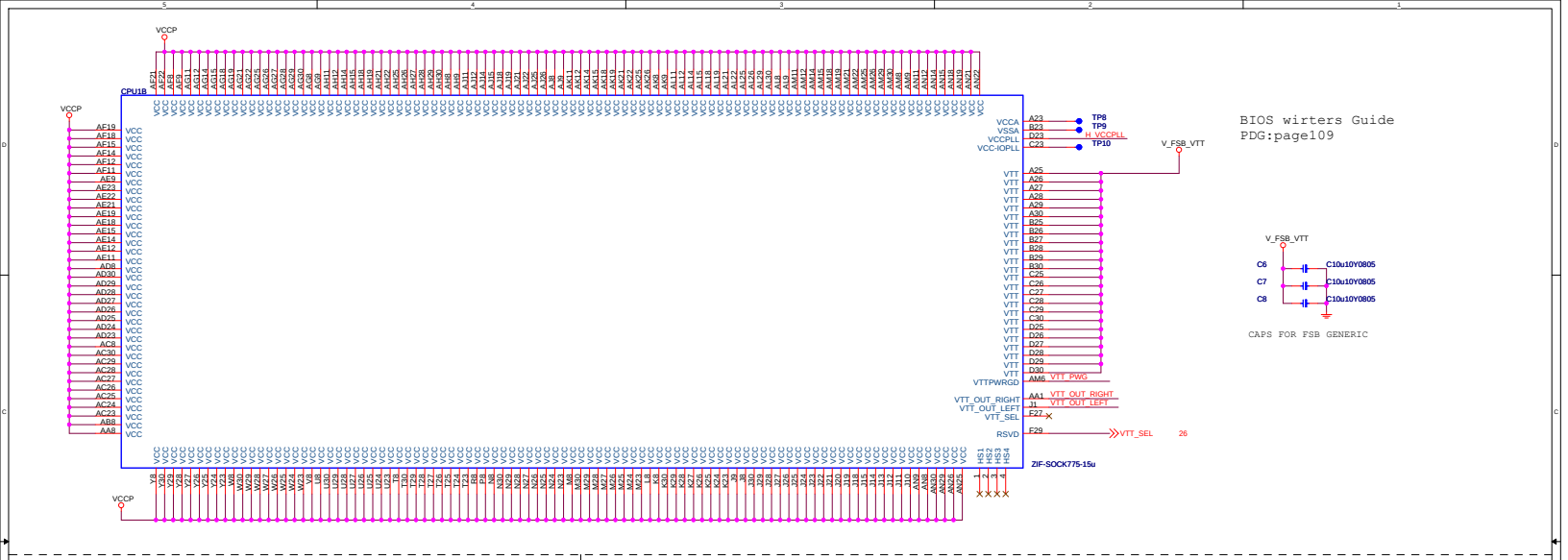
Date: Friday, November 21, 2008 | Sheet 1 of 34

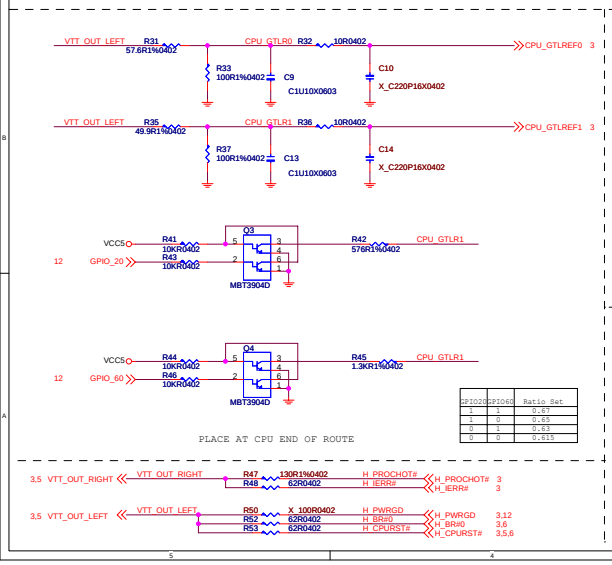
Block Diagram

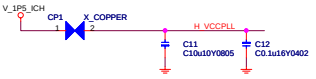


MICRO-STAR INT'L CO.,LTD		
MS-7441 G45 AIO LCD PC		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Friday, November 21, 2008	Sheet 2 of 34	

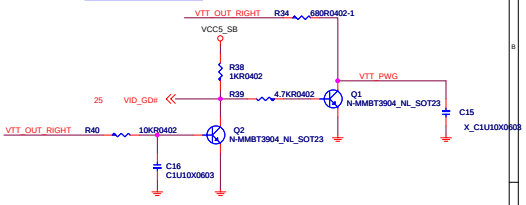

CPU SIGNAL BLOCK
Change 0A
FP_RST#
VCC_VRM_SENSE
VCC_VRM_SENSE 25
VSS_VRM_SENSE
VSS_VRM_SENSE 25
VID[0..7]
VID[0..7] 25
RN1
8P4R-680R0603
VID2
VID0
VID5
VID4
VID7
VID3
VID1
VID6
RN2
8P4R-680R0603
VTT_OUT_RIGHT
VTT_OUT_RIGHT 4,5
C1
C0.1u16Y0402
C2
C0.1u16Y0402
H_A#[3..35]
CPU1A
H_DBI#[0..3]
H_DBI#0
H_DBI#1
H_DBI#2
H_DBI#3
CPU_GTLREF1
H_IERR#
H_FERR#
H_STPCLK#
H_INIT#
H_DBSY#
H_DRDY#
H_TRDY#
H_ADS#
H_LOCK#
H_BNR#
H_HIT#
H_HITM#
H_BPRI#
H_DEFER#
H_TDI
H_TDO
H_TMS
H_TRST#
H_TCK
THERMDA_CPU
THERMDC_CPU
TRMTRIP#
H_PROCHOT#
H_IGNNE#
ICH_H_SMI#
H_A20M#
H_SLP#
Kentsfield
VTT_OUT_RIGHT R17 51R0402
CPU_GTLREF0
R21 51R0402
VTT_OUT_RIGHT R24 X_62R0402
H_FSBSEL0
H_FSBSEL1
H_FSBSEL2
H_PWRGD
H_CPURST#
H_D#[0..63]
H_D#63
H_D#62
H_D#61
H_D#60
H_D#59
H_D#58
H_D#57
H_D#56
H_D#55
H_D#54
ZIF-SOCK775-15u
R1
680R0603
VTT_OUT_RIGHT
VID_SELECT
CPU_GTLREF0
CPU_GTLREF1
GTLREF_SEL
R2 X 0R0402
MCH_GTLREF_CPU 6
TP1
H_BPM#5
H_BPM#4
H_BPM#3
H_BPM#2
H_BPM#1
H_BPM#0
R3 0R0402
H_REQ#[0..4]
PECI 12,29
H_REQ#[0..4] 6
H_TESTHI12 5
R6 51R0402
R7 X 51R0402
R8 51R0402
R9 51R0402
VTT_OUT_LEFT
R10 51R0402
R11 0R0402
DPSLP# 12
V_FSB_VTT
R12 51R0402
R13 51R0402
R14 51R0402
R15 X 62R0402
R16 X 62R0402
VTT_OUT_RIGHT 4,5
CK_H_CPU#
CK_H_CPU
H_RS#[0..2]
H_RS#[0..2] 6
H_BR#0
R18 0R0402
H_BR#0 4,6
PM_DPRSTR_N 7,12
VTT_OUT_LEFT 4,5
C3
X_C0.1u16Y0402
R19 X 49.9R1%0402
R20 X 49.9R1%0402
R22 49.9R1%0402
R23 49.9R1%0402
R25 49.9R1%0402
R26 49.9R1%0402
TP2
TP3
TP4
TP5
TP6
TP7
H_ADSTB#1
H_ADSTB#0
H_DSTBP#3
H_DSTBP#2
H_DSTBP#1
H_DSTBP#0
H_DSTBN#3
H_DSTBN#2
H_DSTBN#1
H_DSTBN#0
H_NMI
H_INTR
Prescott / Cedar Mill
LL_ID[1:0] = 00
GTLREF_SEL = 0
VTT_SEL = 1
For Kentsfield CPU support
H_TESTHI9
H_TESTHI8
R4 X 0R0402 H_BPM#2
R5 X 0R0402 H_BPM#3
BSEL TABLE
2 1 0 FSB FREQUENCY
0 0 0 266 MHZ (1066)
0 1 0 200 MHZ (800)
0 0 1 133 MHZ (533)
RN3
8P4R-51R0402
H_BPM#3
H_BPM#5
H_BPM#1
H_BPM#0
RN4
8P4R-51R0402
H_TMS
H_TDI
H_BPM#2
H_BPM#4
C4 C0.1u16Y0402
C5 C0.1u16Y0402
R27 51R0402 H_TDO
R28 51R0402 H_TRST#
R29 51R0402 H_TCK
VTT_OUT_RIGHT R30 X 51R0402 H_SLP#
MICRO-STAR INT'L CO.,LTD
MS-7441
Size Custom
Document Description
Intel LGA775 - Signals
Rev 0A
Date: Friday, November 21, 2008
Sheet 3 of 34



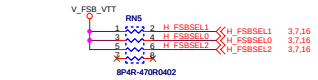




VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns



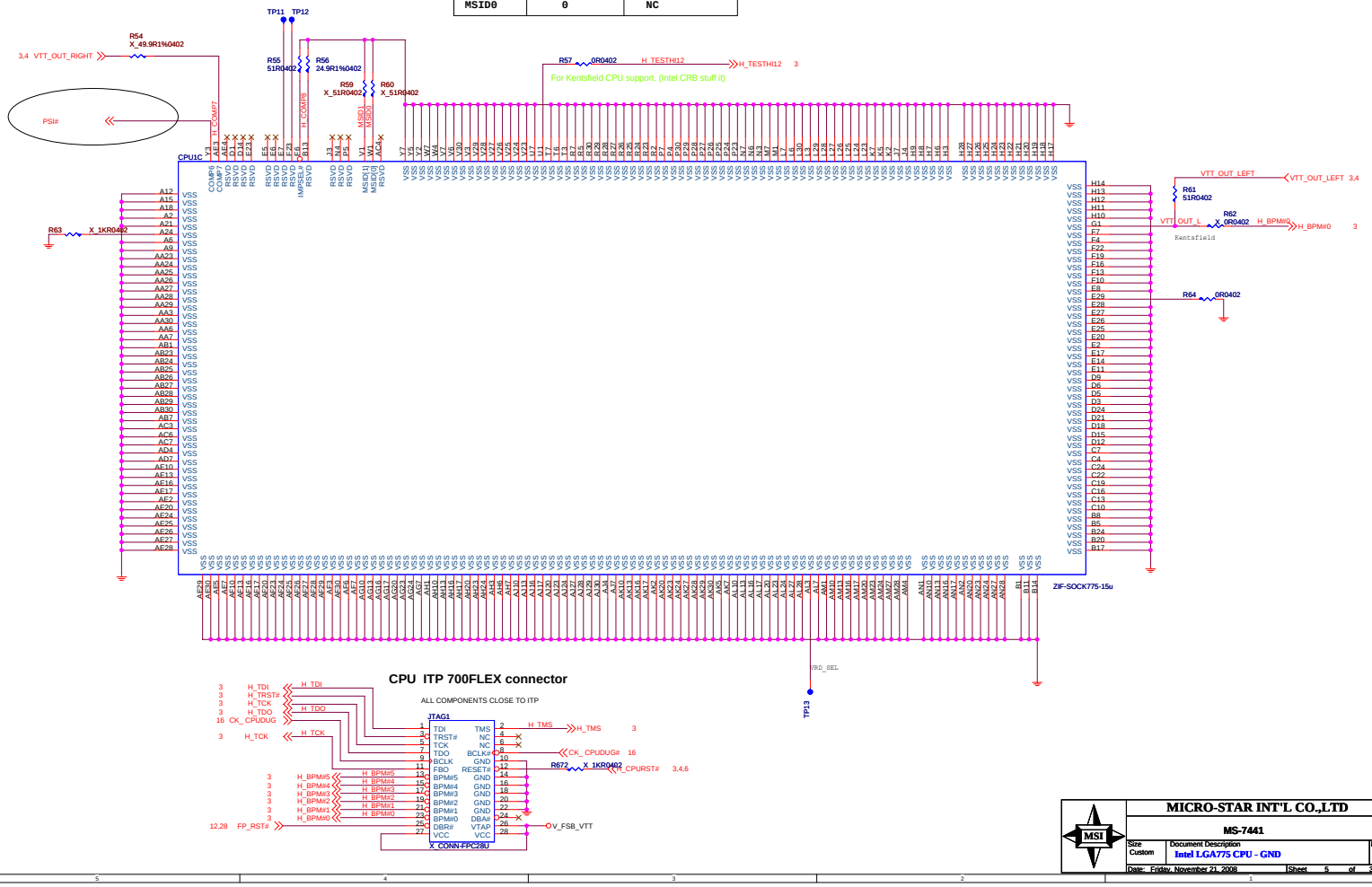
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED



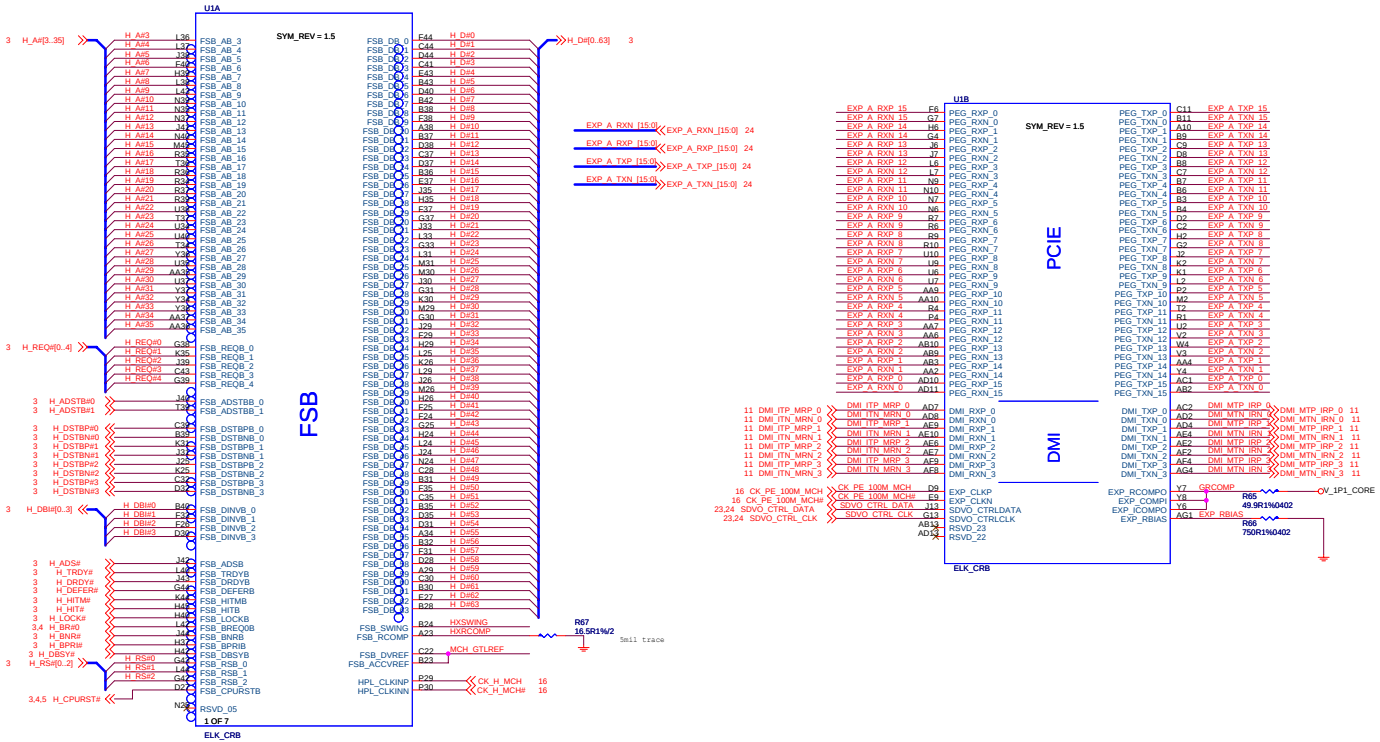
PLACE AT ICH END OF ROUTE

MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: Intel LGA775 - Power	Rev: 0A
Date: Friday, November 21, 2008	Sheet 4 of 34	

	Intel Core 2 Due or Wolfdale processor	Intel Core 2 Quad or Yorkfield Processer
MSID1	0	NC
MSID0	0	NC



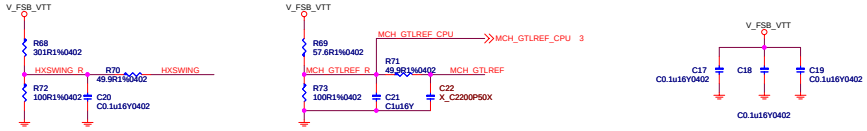
MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: Intel LGA775 CPU - GND	Rev: 0A
Date: Friday, November 21, 2008	Sheet 5 of 34	



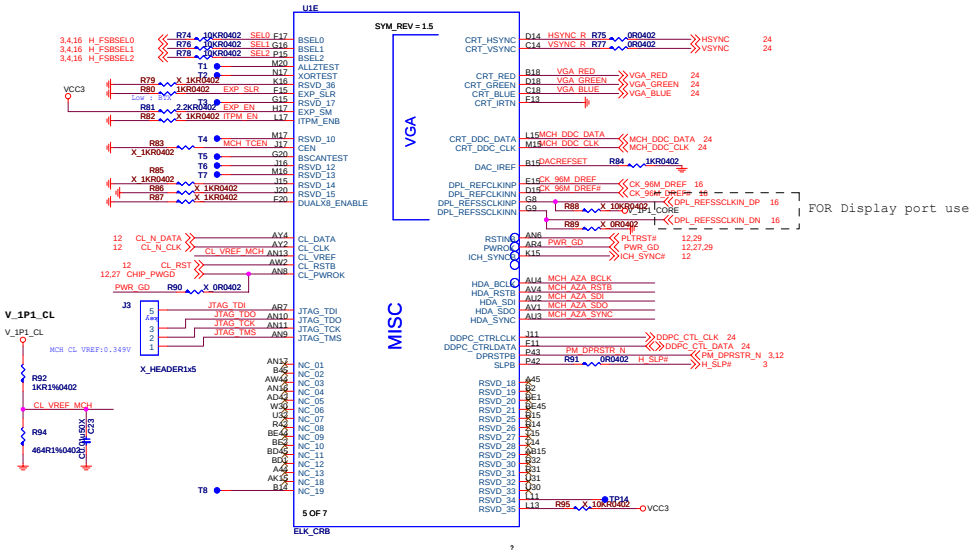
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/4*VTT +/- 2%

PLACE DIVIDER RESISTOR NEAR VTT

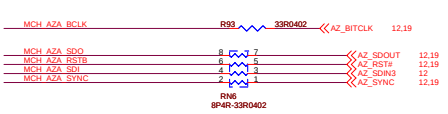
GTLREF VOLTAGE SHOULD BE 0.63S*VTT=0.7V 100 OHM OVER 200 RESISTORS



MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: Eaglelake FSB/PCIE	Rev: 0A
Date: Friday, November 21, 2008	Sheet 6 of 34	



HDMI Support



ITPM_ENB
Itegrated TPM Enable:
0=Enable iTPM
1=Disable iTPM

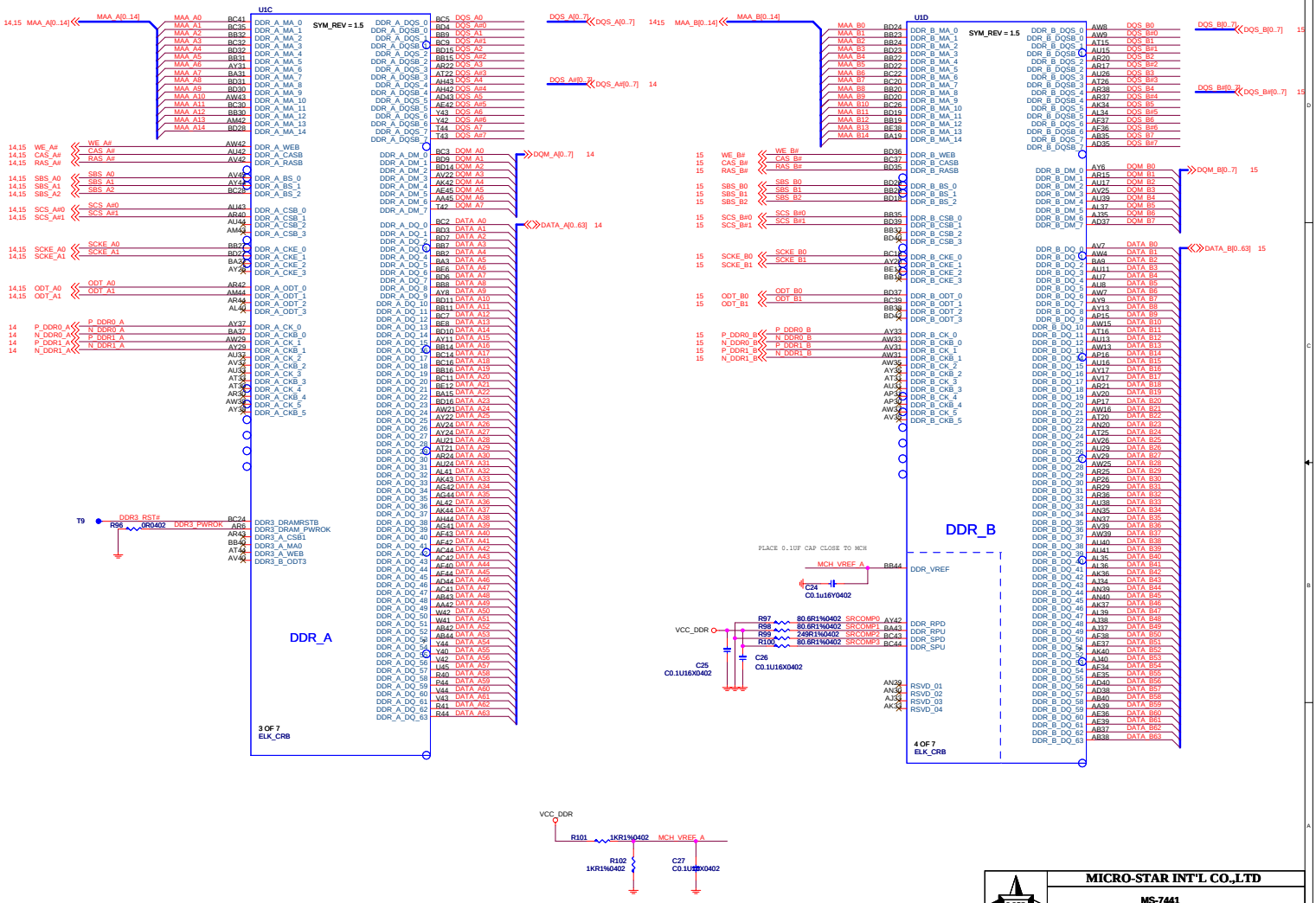
DualX8_Enable
0=2X8 PCIe Ports Enable
1=1X16 PCIe Port Enable

DEMO BOARD CHANGE

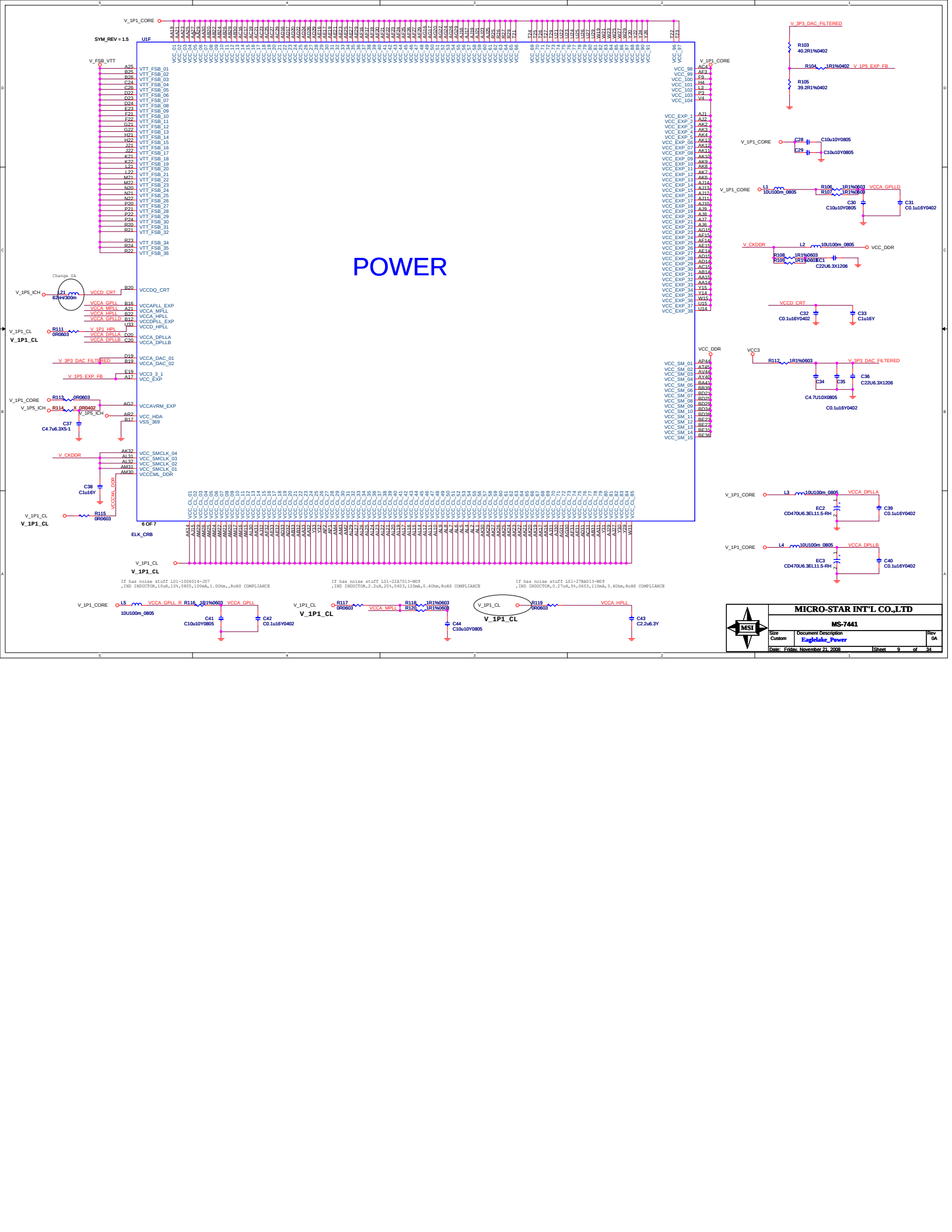
Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot

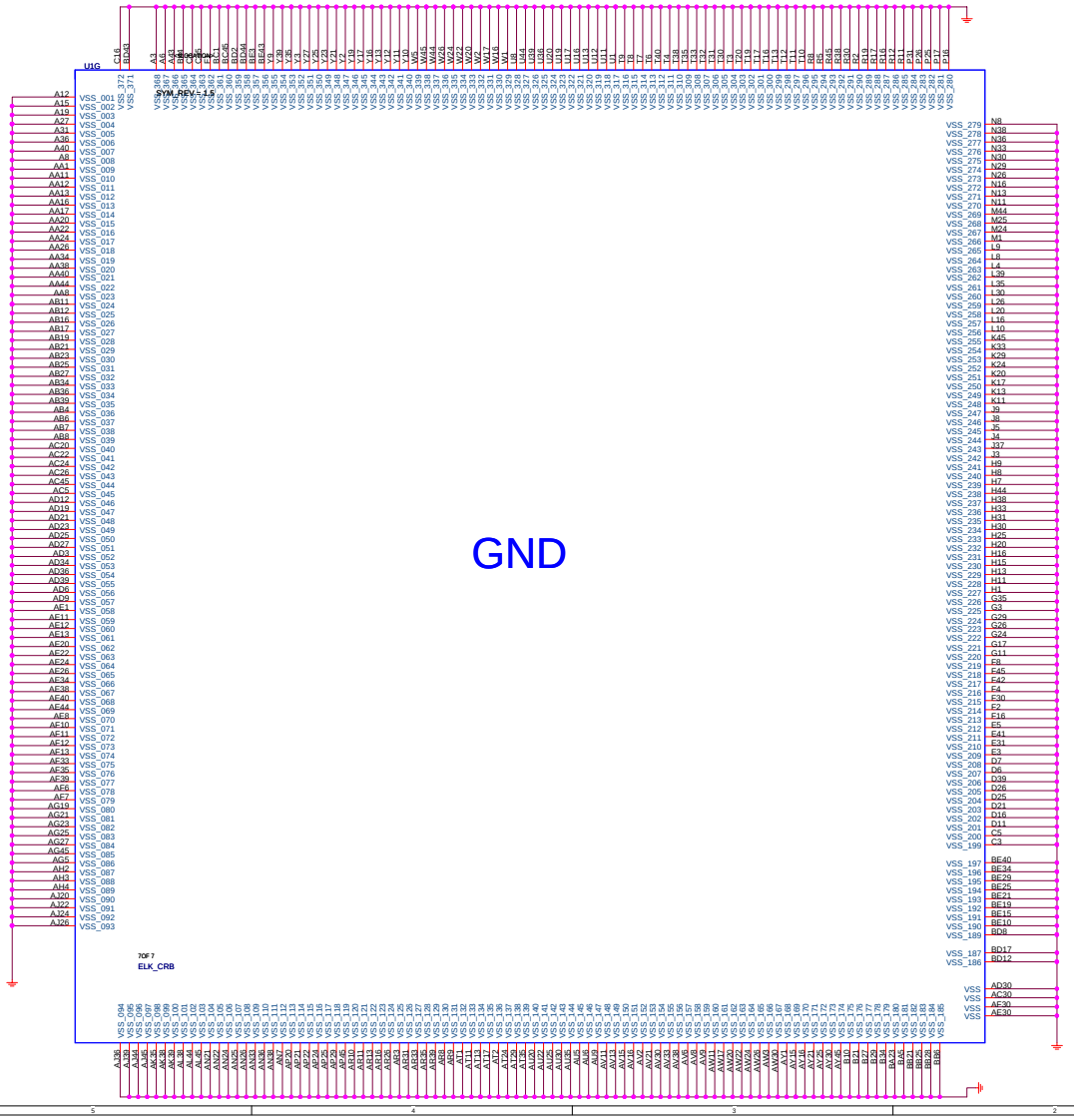
PIN	H	L	Description
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7441		
Size: Custom	Document Description: Eaglelake VGA/MISC		Rev: 0A
Date: Friday, November 21, 2008	Sheet 7 of 34		



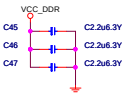
MICRO-STAR INT'L CO.,LTD	
MS-7441	
Size: Custom	Document Description: Eaglelake_Memory DDR2
Rev: 0A	
Date: Friday, November 21, 2008	Sheet 8 of 34


POWER
SYM_REV = 1.5
U1F
6 OF 7
ELK_CRB
V_1P1_CORE
V_FSB_VTT
V_1P1_CL
V_1P1_ICH
V_3P3_DAC_FILTERED
V_1P5_EXP_FB
V_CKDDR
VCCD_CRT
VCCA_GPLL
VCCA_MPLL
VCCA_HPLL
VCCA_GPLLD
VCCDPLL_EXP
VCCD_HPLL
VCCA_DPLLA
VCCA_DPLLB
VCCA_DAC_01
VCCA_DAC_02
VCC3_3_1
VCC_EXP
VCCAVRM_EXP
VCC_HDA
VSS_369
VCC_SMCLK_04
VCC_SMCLK_03
VCC_SMCLK_02
VCC_SMCLK_01
VCCCML_DDR
VCC_DDR
VCC3
VCCA_DPLLA
VCCA_DPLLB
VCCA_GPLL_R
VCCA_MPLL
VCCA_HPLL
If has noise stuff L01-1006014-J07 ,IND INDUCTOR,10uH,10%,0805,100mA,1.00hm,,RoHS COMPLIANCE
If has noise stuff L01-22A7013-M09 ,IND INDUCTOR,2.2uH,20%,0603,120mA,0.40hm,RoHS COMPLIANCE
If has noise stuff L01-27BA013-M09 ,IND INDUCTOR,0.27uH,5%,0603,110mA,3.40hm,RoHS COMPLIANCE
MICRO-STAR INT'L CO.,LTD
MS-7441
Size Custom
Document Description Eaglelake_Power
Rev 0A
Date: Friday, November 21, 2008
Sheet 9 of 34

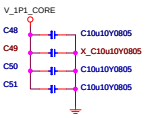


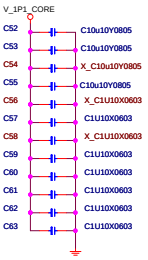
All cap place close to GMCH

MCH memory decouping cap

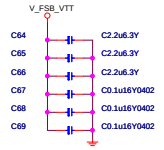


V_1P1_Core decouping cap

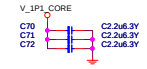




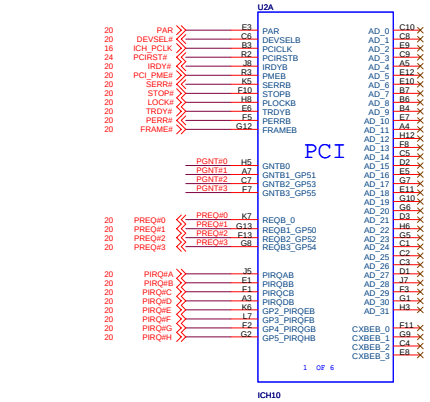
V_FSB_VTT decouping cap(FSB)

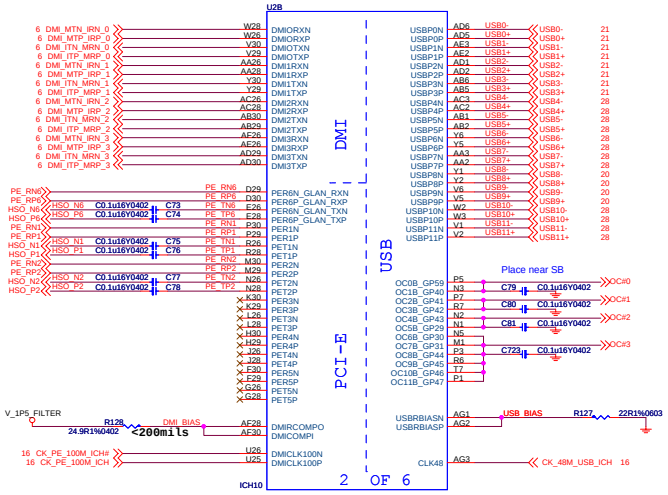


V_1P1_Core decouping cap(PCIE)



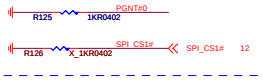
MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: Eaglelake - GND	Rev: 0A
Date: Friday, November 21, 2008	Sheet 10 of 34	



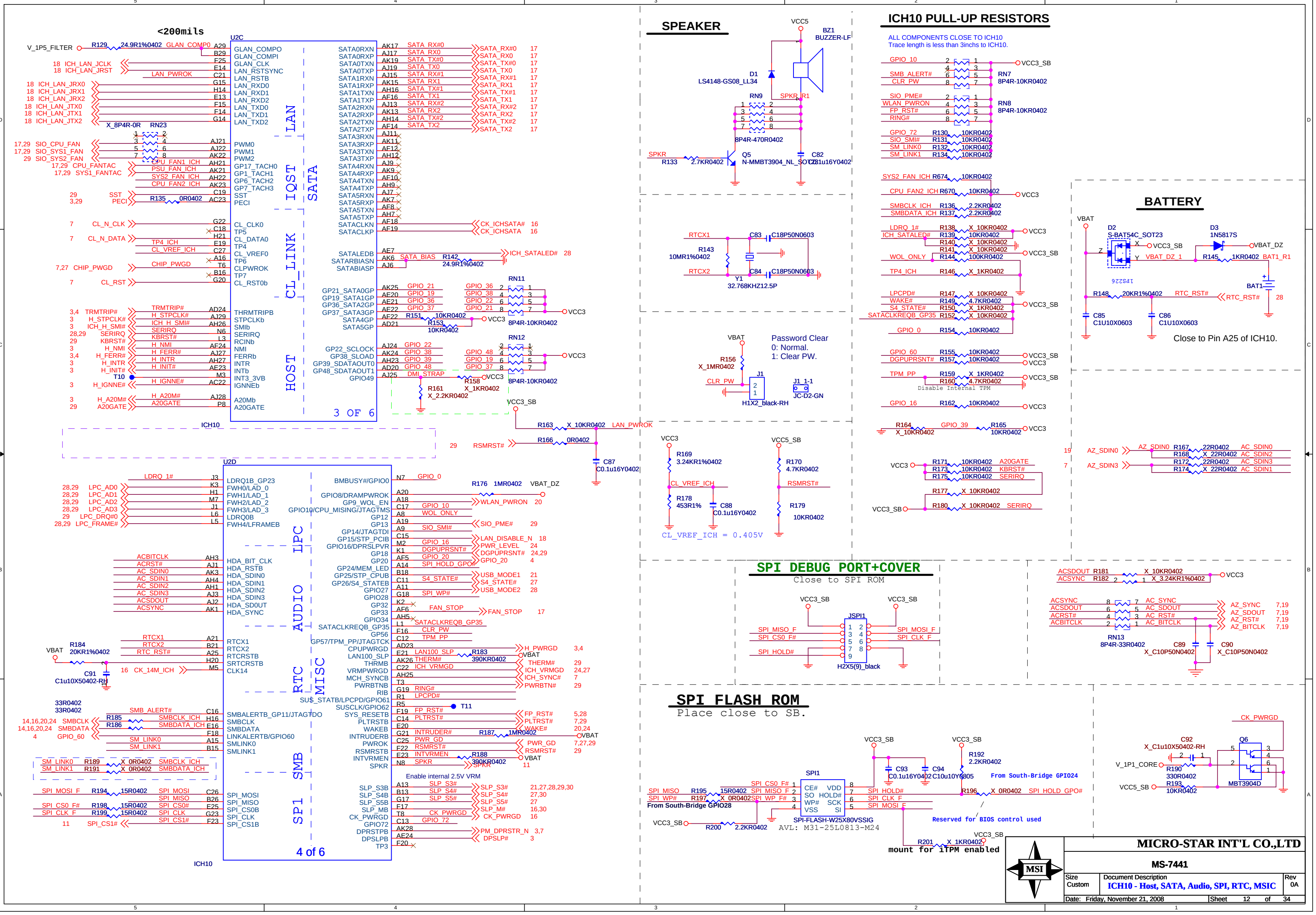


ICH10 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	EN	DIS	Danbury Tec.
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



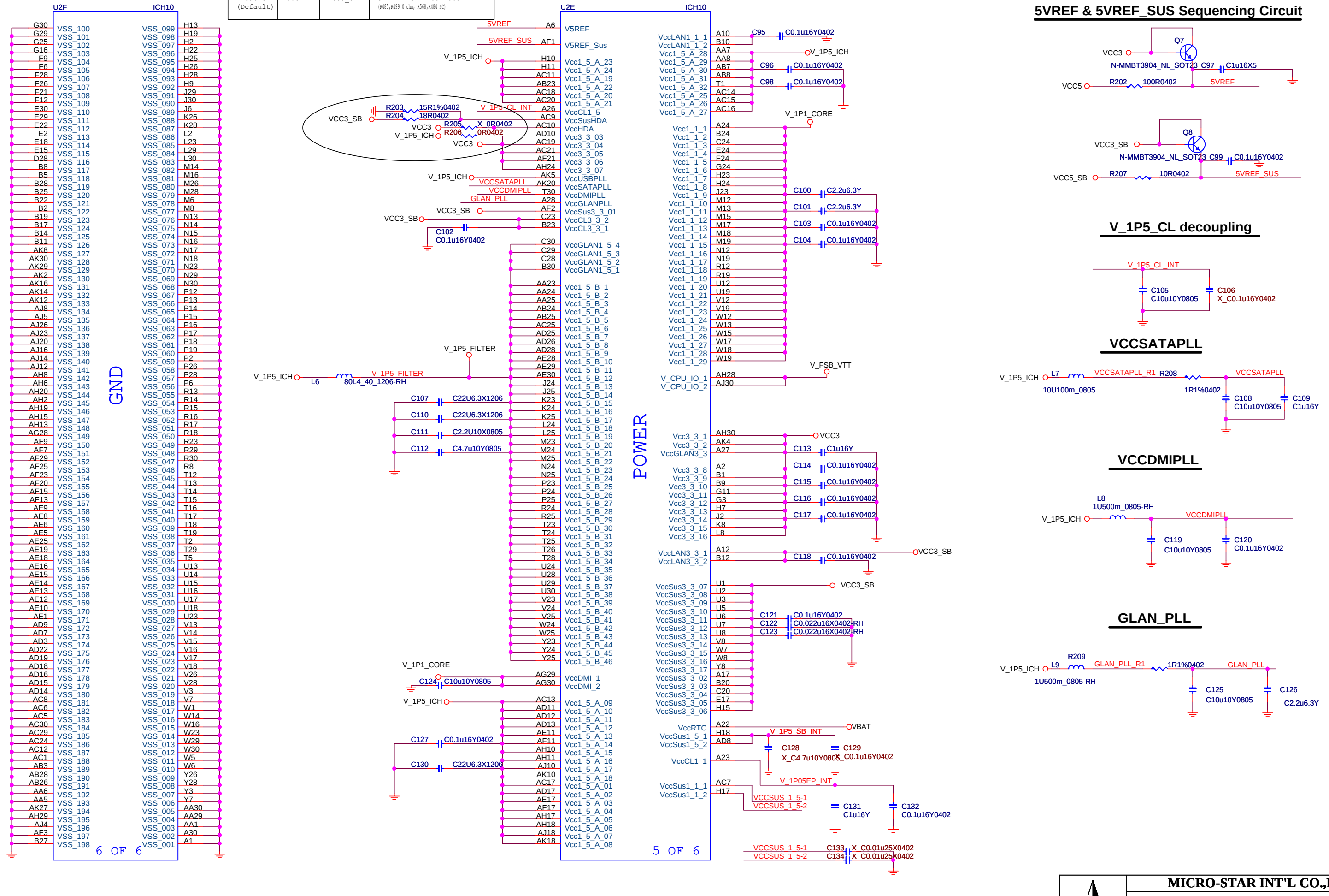
MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: ICH10 - PCI, DMI, USB, PCIE & Slots	Rev: 0A
Date: Friday, November 21, 2008	Sheet 11 of 34	



<200mils
SPEAKER
ICH10 PULL-UP RESISTORS
ALL COMPONENTS CLOSE TO ICH10
Trace length is less than 3inchs to ICH10.
BATTERY
Close to Pin A25 of ICH10.
Password Clear
0: Normal.
1: Clear PW.
CL_VREF_ICH = 0.405V
SPI DEBUG PORT+COVER
Close to SPI ROM
SPI FLASH ROM
Place close to SB.
From South-Bridge GPIO24
From South-Bridge GPIO28
Reserved for BIOS control used
AVL: M31-25L0813-M24
mount for iTPM enabled
Enable internal 2.5V VRM
Disable Internal TPM
3 OF 6
4 of 6
MICRO-STAR INT'L CO.,LTD
MS-7441
Size
Custom
Document Description
ICH10 - Host, SATA, Audio, SPI, RTC, MSIC
Rev
0A
Date: Friday, November 21, 2008
Sheet 12 of 34

Support HDMI Function need change VccHDA and VccSusHDA from 3.3V to 1.5V

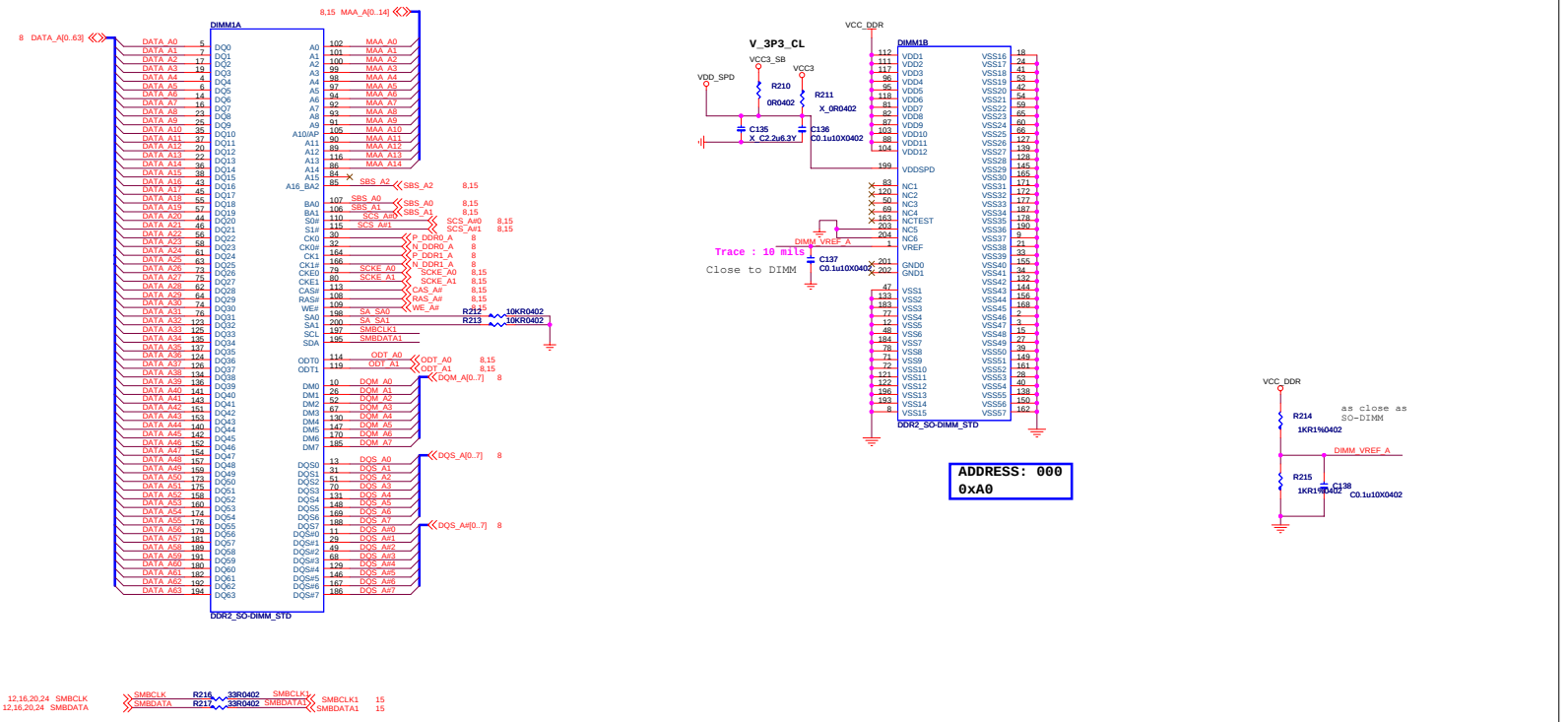
HDMI	VccHDA	VccSusHDA	Description
Enable	1.5V	1.5V_SB	STAFF R484, R499, R568 (R499=18 ohm,R568=15ohm, R484=0 ohm)
Disable (Default)	3.3V	VCC3_SB	STAFF R484 R499 R568 (R485,R499=0 ohm, R568,R484 NC)



MICRO-STAR INT'L CO.,LTD			
MS-7441			
Size: Custom	Document Description: ICH10 - Power, GND		Rev: 0A
Date: Friday, November 21, 2008	Sheet 13 of 34		

DDRII SODIMM A0

ADDR=1010000B

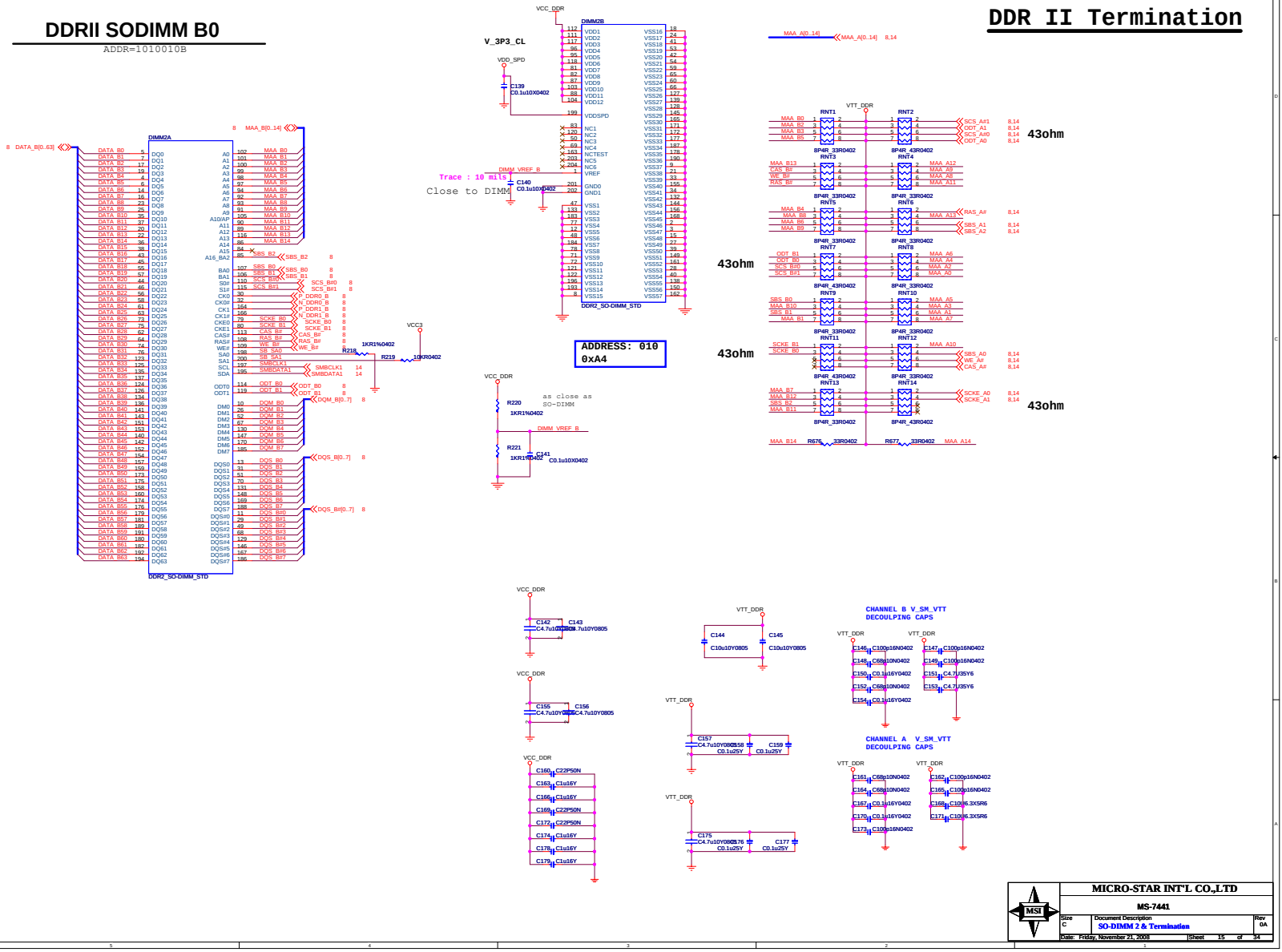


MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: SO-DIMM 1	Rev: 0A
Date: Friday, November 21, 2008	Sheet 14 of 34	

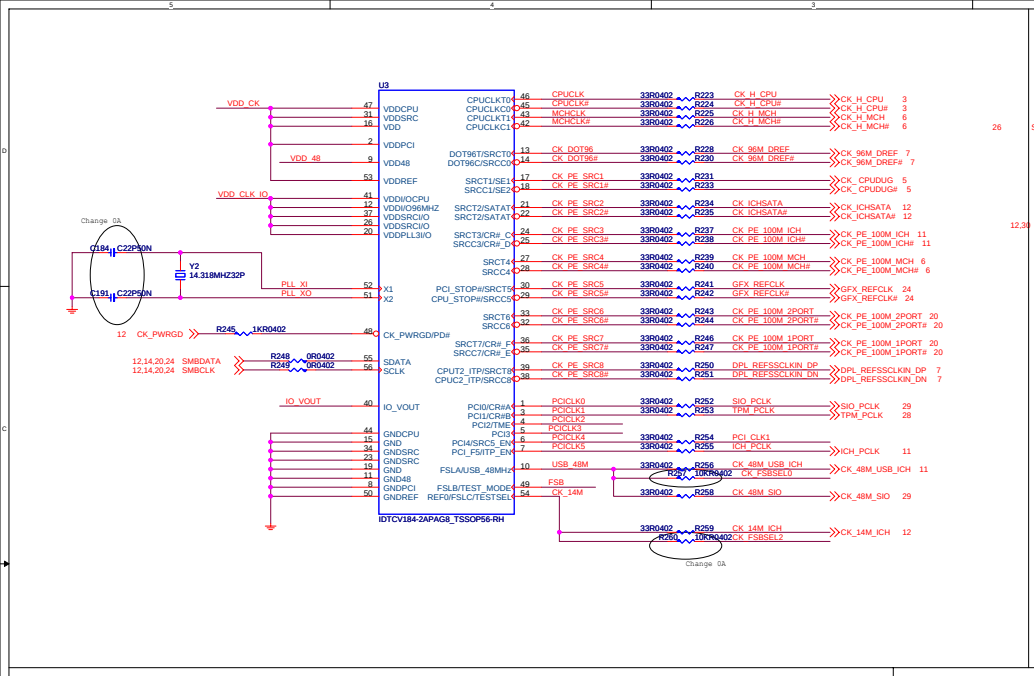
DDRII SODIMM B0

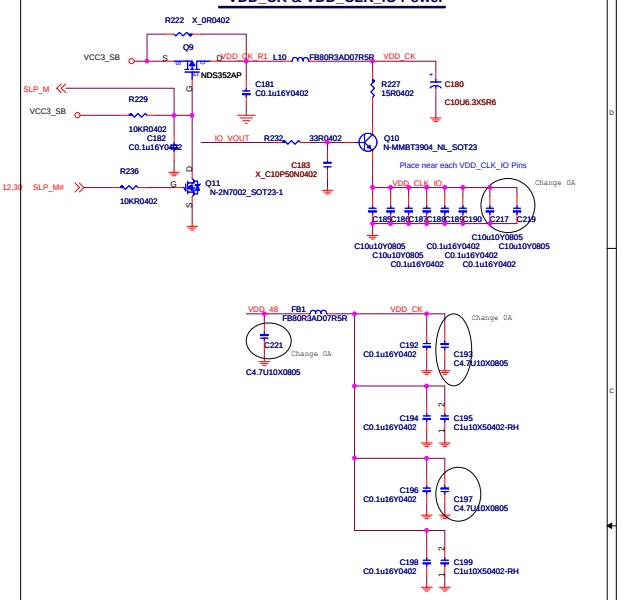
ADDR=1010010B

DDR II Termination

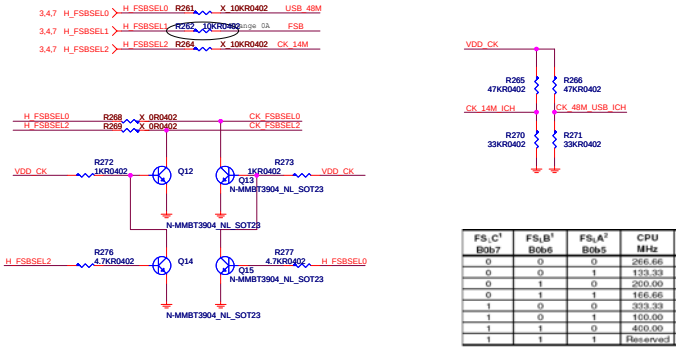


MICRO-STAR INT'L CO.,LTD			
MS-7441			
Size: C	Document Description: SO-DIMM 2 & Termination		Rev: 0A
Date: Friday, November 21, 2008	Sheet 15 of 34		





CPU Frequency select



FS_C¹ B0b7	FS_B¹ B0b6	FS_A¹ B0b5	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Reserved

Strapping risistor

H=Overclocking disable

PCICLK2 R263 10KR0402 VCC3

Clock CFG bit, combined with pin 4.
Voltage decoding : L=0.55V.

PCICLK3 R267 10KR0402

H=SRC5 ; L=CPU/PCI stop

PCICLK4 R274 10KR0402 VCC3

H=CPU_ITP ; L=SRC8

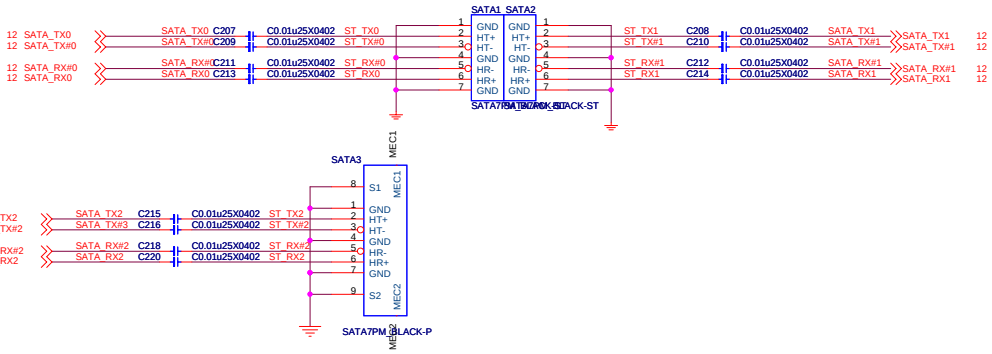
PCICLK5 R275 10KR0402

For EMI Reserve

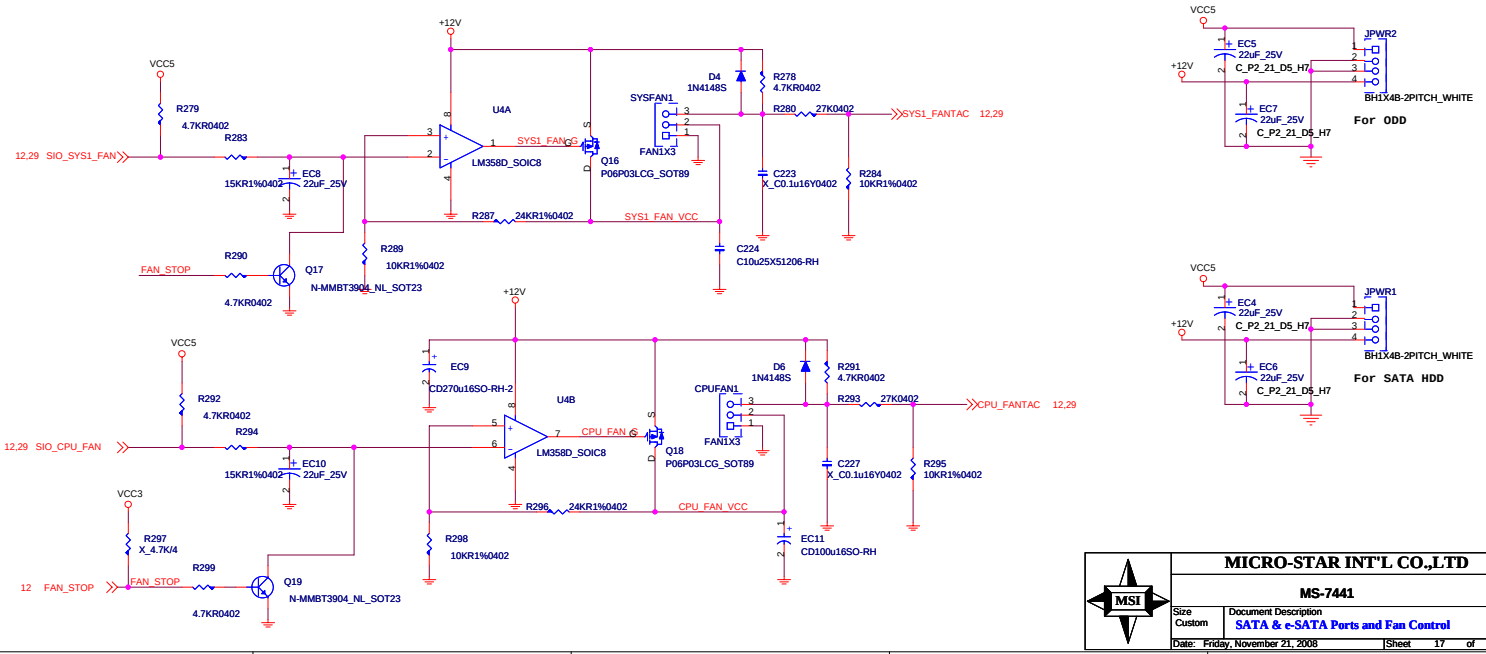
SIO_PCLK C200 X_C22P50N0402
PCI_CLK1 C201 X_C10P50N0402
ICH_PCLK C202 X_C10P50N0402
TPM_PCLK C203 X_C10P50N0402
CK_48M_USB_ICH C204 X_C10P50N0402
CK_48M_SIO C205 X_C10P50N0402
CK_14M_ICH C206 X_C10P50N0402

MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: CLOCK Generator-IDTCV184-2	Rev: 0A
Date: Friday, November 21, 2008	Sheet 16 of 34	

SATA PORT



FAN-COUNTROL CIRCUIT



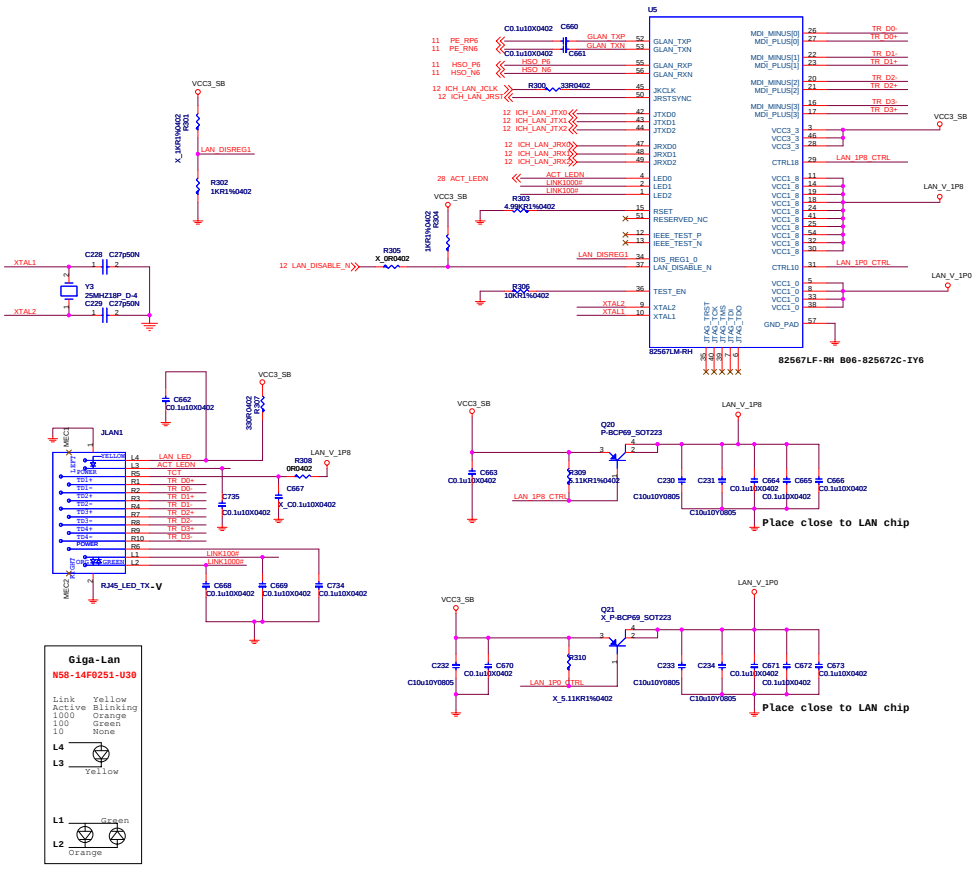
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7441	
Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control	Rev: 0A
Date: Friday, November 21, 2008	Sheet 17 of 34	

Maximum current of 1.8 V is less then 270mA, Maximum current of 1.0 V is less then 139mA.

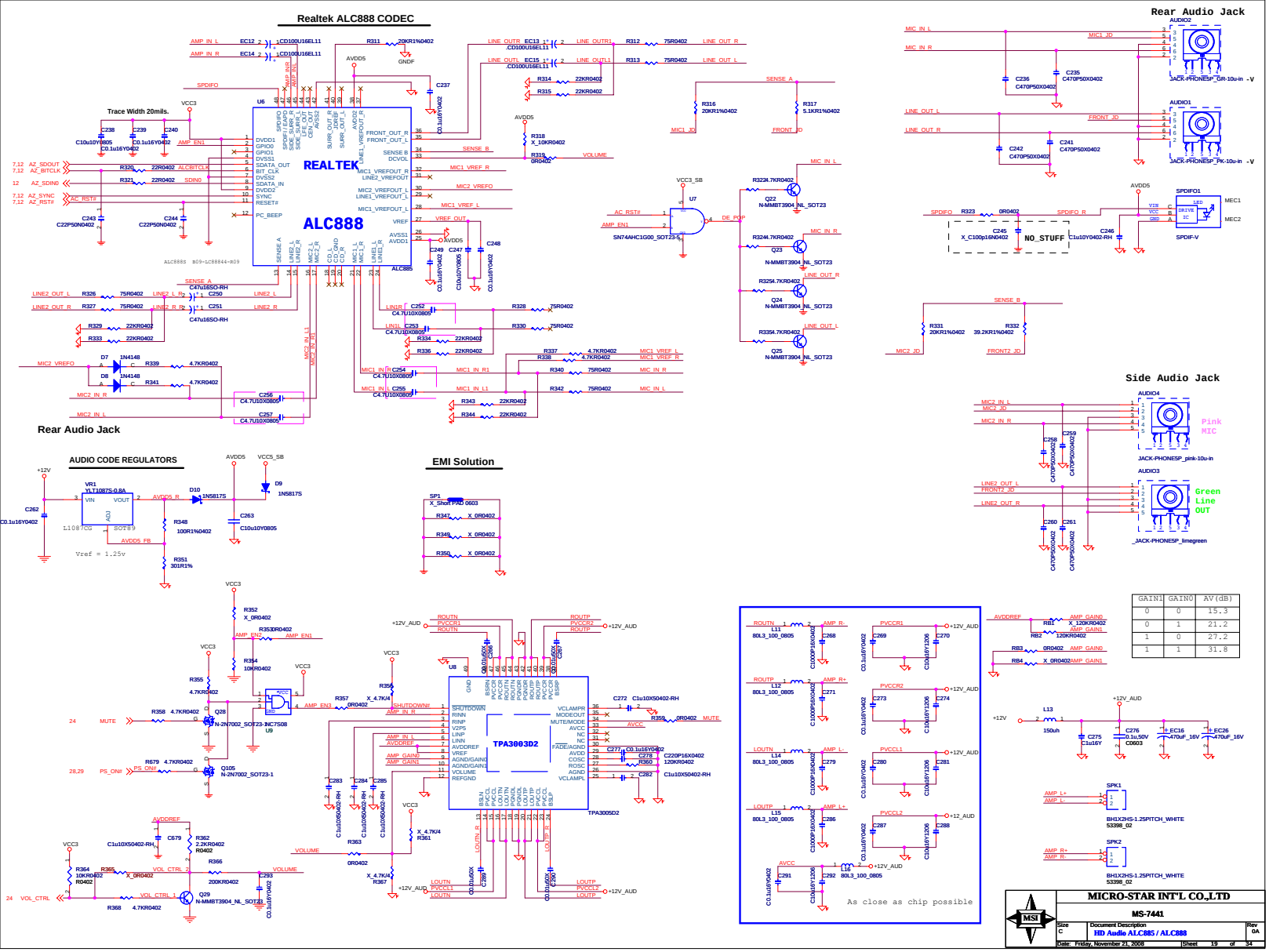
For proper and safe operation, the power supplies must follow the following rule:

VDDO (3.3V) ≥ AVDD (1.8) ≥ DVDD (1.05V)

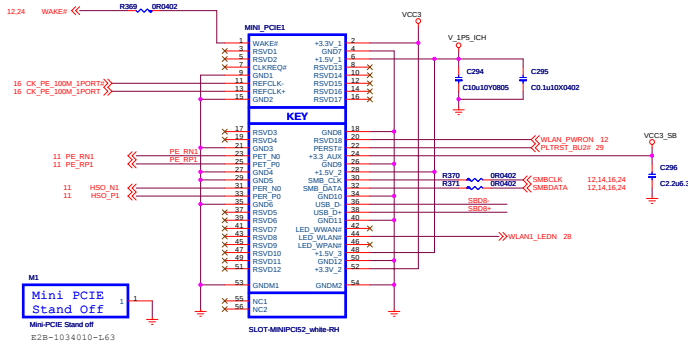
This means that VDDO must start ramping before AVDD and DVDD, but DVDD may reach its nominal operating range before AVDD and VDDO.

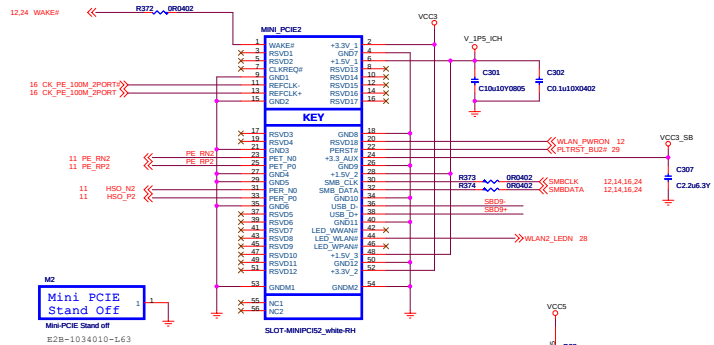


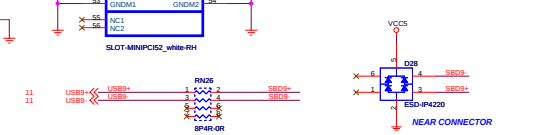
MICRO-STAR INT'L CO.,LTD	
MS-7441	
Size: C	Document Description: I82567PHY Gb LAN
Rev: 0A	
Date: Friday, November 21, 2008	Sheet 18 of 34

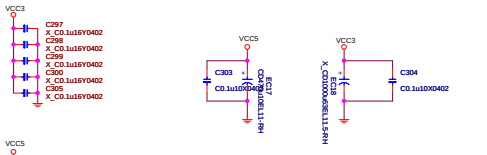


GAIN1	GAIN0	AV(dB)
0	0	15.3
0	1	21.2
1	0	27.2
1	1	31.8

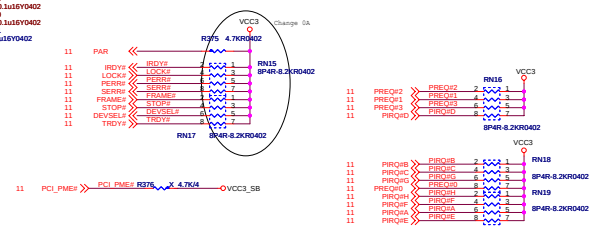








PCI PULL-UP / DOWN RESISTORS



MICRO-STAR INT'L CO.,LTD	
MS-7441	
Size: C	Document Description: Mini-PCIE Slots
Rev: 0A	
Date: Friday, November 21, 2008	Sheet 20 of 34

Vertical Connectors

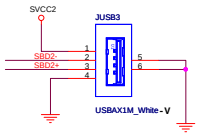
USB : N53-04M0361-K06

LAN : N58-14F0251-U30

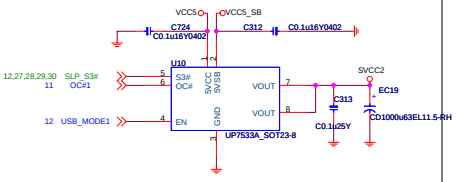
Audio : N54-05F0751-H06

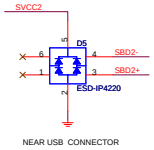
N54-05F0761-H06

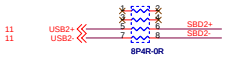
REAR USB PORT 2



RUSB POWER FOR PORT 2







NEAR USB CONNECTOR

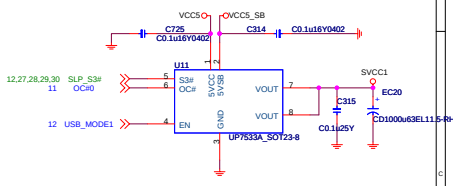
USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

S0, S1, S2 USB_MODE = high --> USB power = VCC5

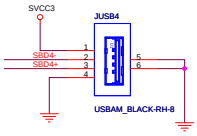
S3, S4, S5 USB_MODE = high --> USB power = VCC5_SB

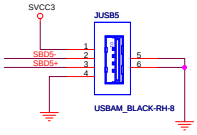
USB_MODE = low --> USB power = 0

RUSB POWER FOR PORT 0,1

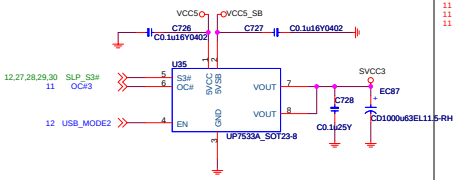


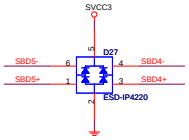
SIDE USB PORT 0 , 1





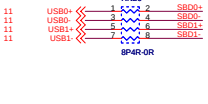
SIDE POWER FOR PORT 0,1

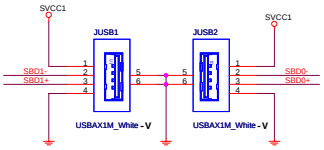


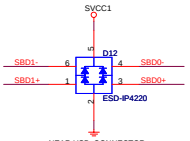


NEAR USB CONNECTOR

REAR USB PORT 0,1

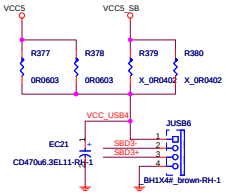


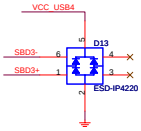




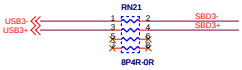
NEAR USB CONNECTOR

WebCAM





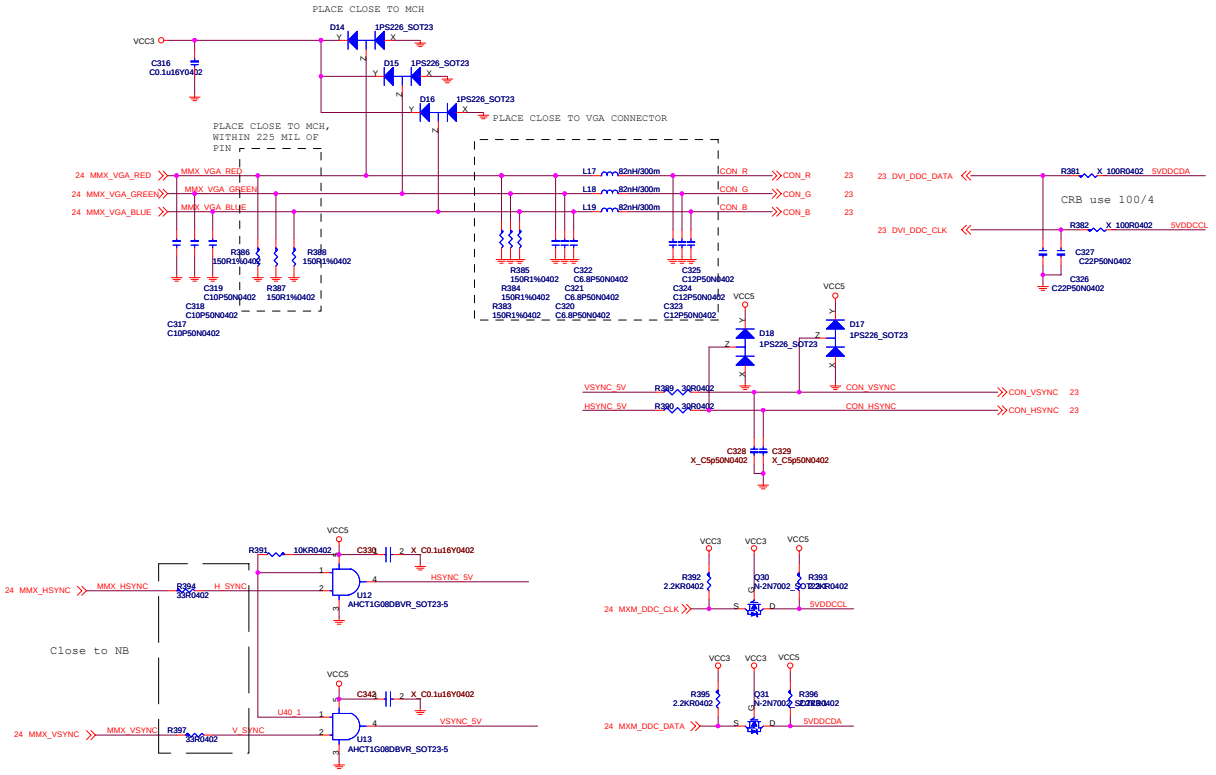
NEAR USB CONNECTOR



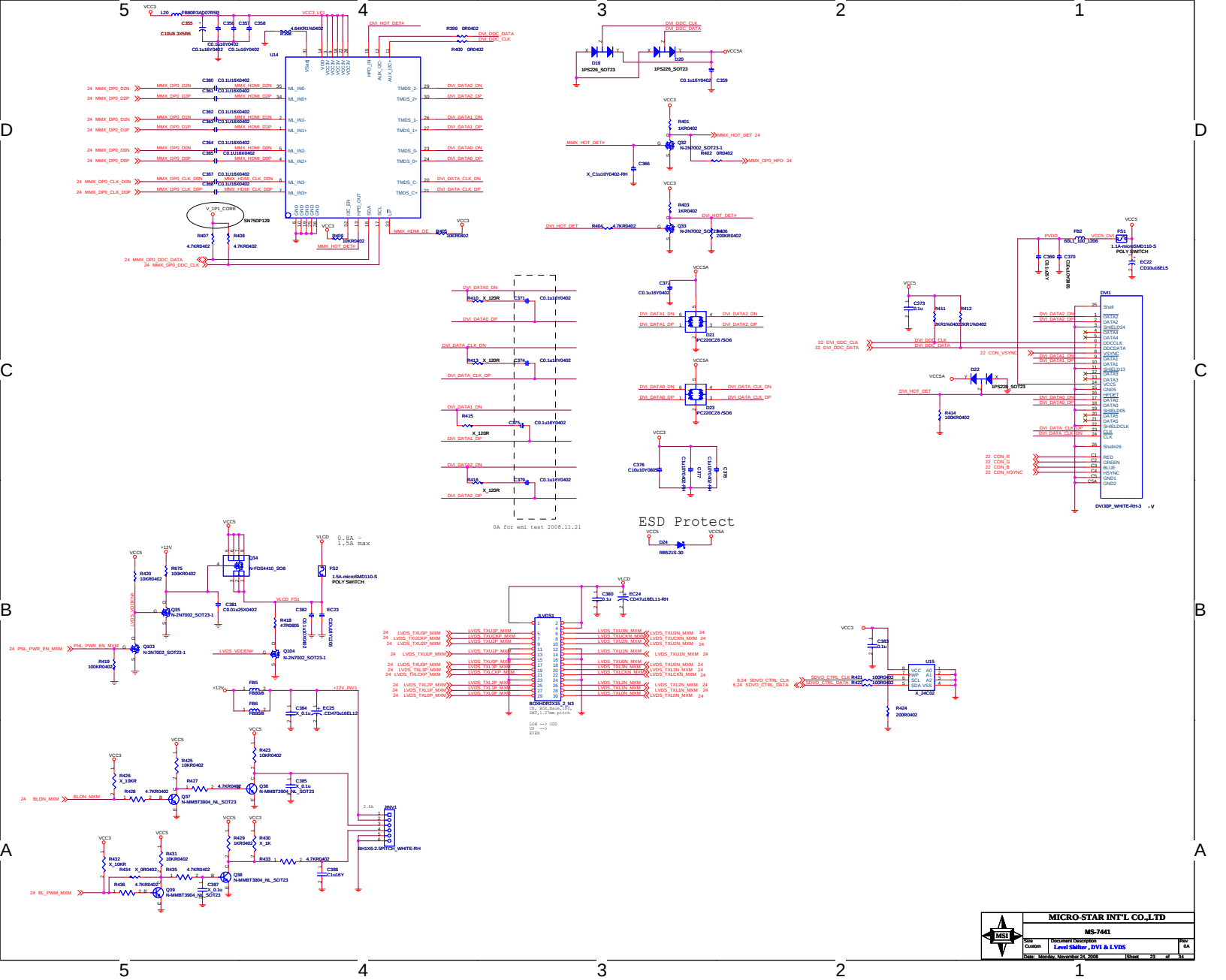
port 8, 9 for Mini-PCI-E

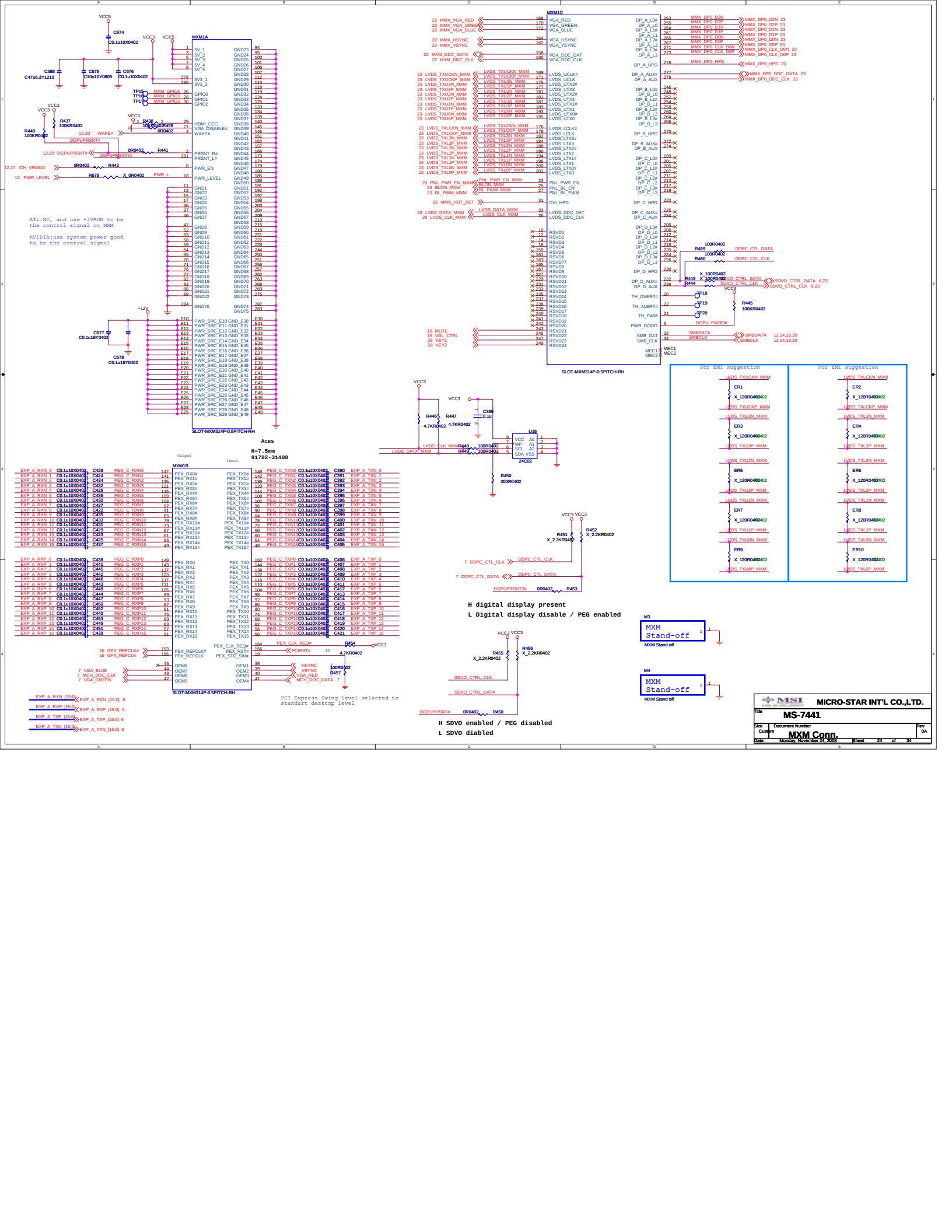
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7441	
Size: Custom	Document Description: USB Connectors	Rev: 0A
Date: Friday, November 21, 2008	Sheet 21 of 34	

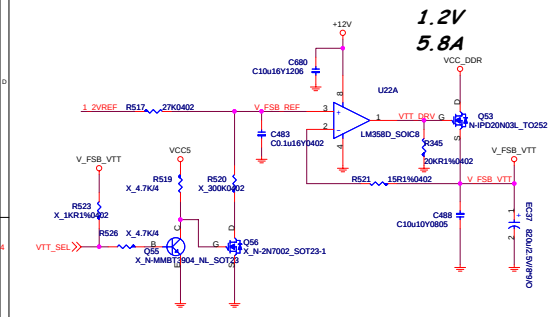
Video Connector

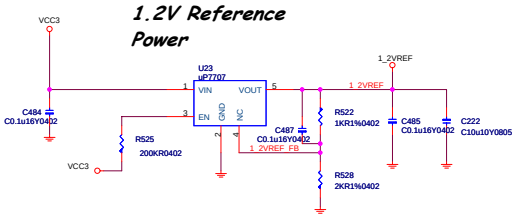


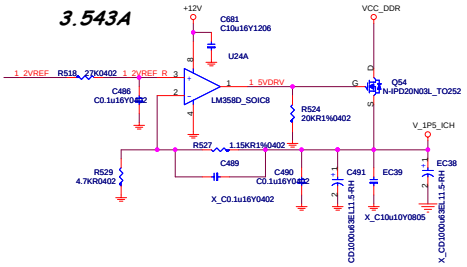
MICRO-STAR INT'L CO.,LTD		
MS-7441		
Size: Custom	Document Description: VGA Circuit	Rev: 0A
Date: Friday, November 21, 2008	Sheet 22 of 34	

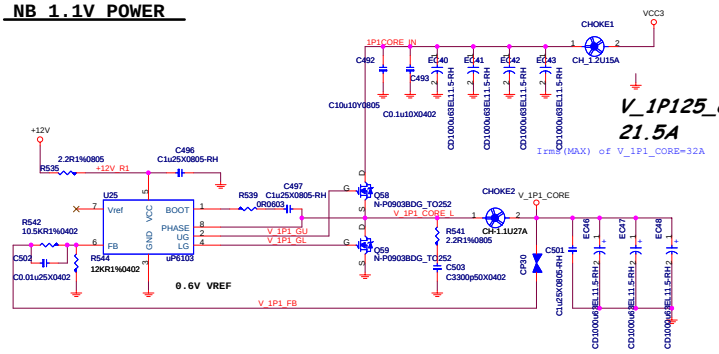

ESD Protect
0A for emi test 2008.11.21
MICRO-STAR INT'L CO.,LTD
MS-7441
Level Shifter , DVI & LVDS
Monday, November 24, 2008
23
34

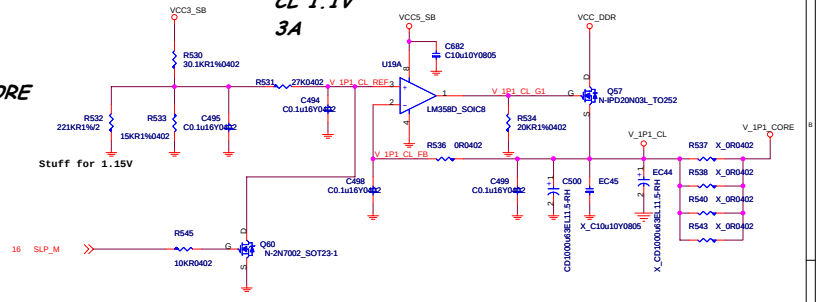

MXM1A
MXM1B
MXM1C
SLOT-MXM314P-0.5PITCH-RH
ATi:NC, and use +3VRUN to be the control signal on MXM
nVIDIA:use system power good to be the control signal
Aces
H=7.5mm
91782-31408
H digital display present
L Digital display disable / PEG enabled
H SDVO enabled / PEG disabled
L SDVO diabled
PCI Express Swing level selected to standart desktop level
For EMI suggestion
MXM Stand-off
MICRO-STAR INT'L CO.,LTD.
MS-7441
MXM Conn.



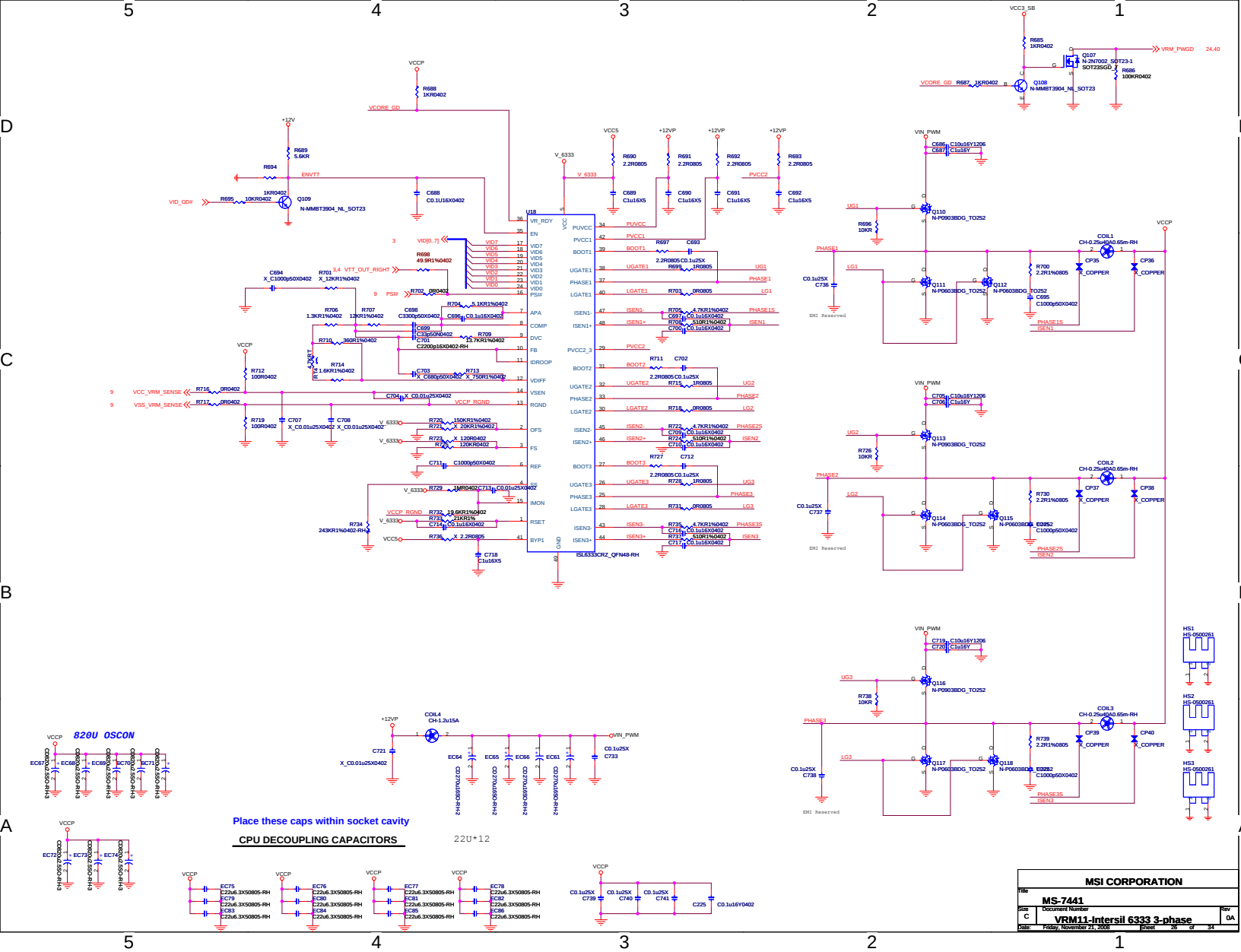








MSI CORPORATION			
Title	MS-7441		
Size: Custom	Document Number: V_1P5_ICH ,V_1P1_CORE,5VDIMM		Rev: 0A
Date: Friday, November 21, 2008	Sheet 26 of 34		


820U OSCON
Place these caps within socket cavity
CPU DECOUPLING CAPACITORS
22U*12
ISL6333CRZ_QFN48-RH
MSI CORPORATION
MS-7441
VRM11-Intersil 6333 3-phase
Friday, November 21, 2008
Sheet 26 of 34

DDR II 1.8V POWER

Iripple=24.127*0.8*=(1.8/5)*=(1-1.8/5)/1=9.264768A
2.35*3*1.7=11.985A>9.264768A

Iinput x 5V = 1.8V x12.17A /0.8
Iinput = 5.48A

D=1.8/5=0.36

Iripple=12*0.6*0.8/1=5.76A

5.76/1.7=3.38A

SODIMMx2	Vterm	NB	+1_5VRUN
5.52A	1A	3A	2.65A = 12.17A

VCC_DDR 6.5A

VTT_DDR 1.5A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

Irms(MAX) of VCC_DDR=24.4A

To meet Intel power down sequence.

de- VCC_DDR high frequency noise.

5VDIMM FOR DDR/AMT

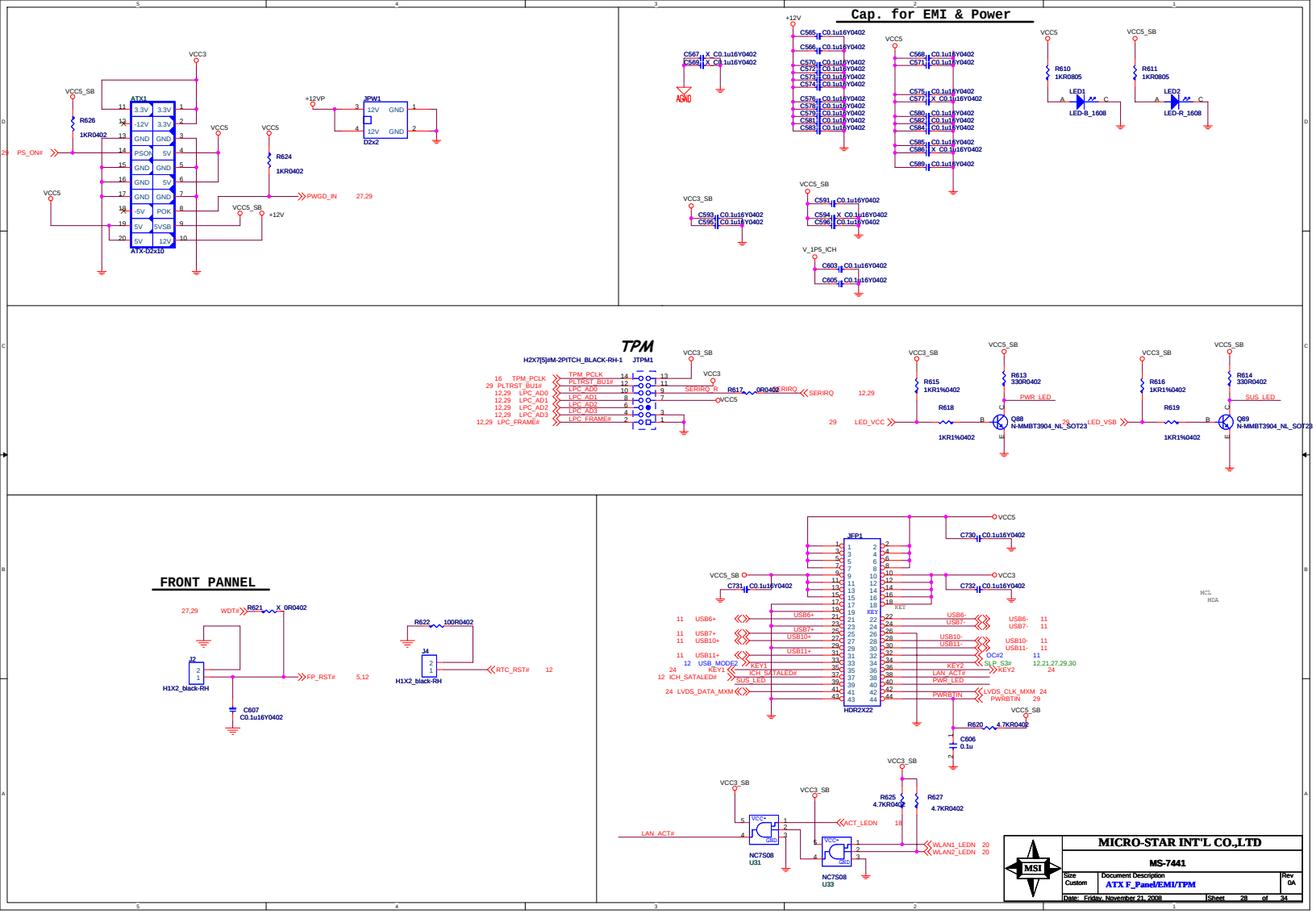
H:Support S0/S3/S5
L:Support S0/S3

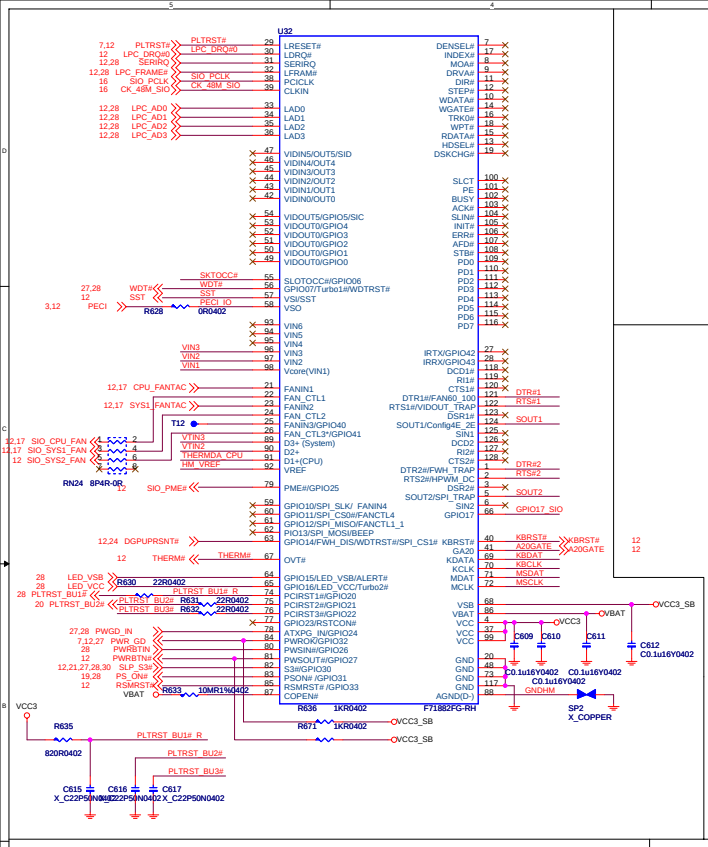
5VDIMM at S0/M0:
+1.8VIMM +1_05VM
5.48A + 1.7A = 7.18A

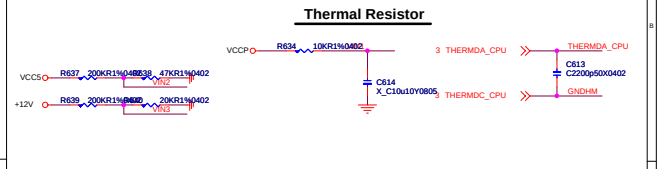
VCC3_SB

0A to 10 Modify Glitch issue

MICRO-STAR INT'L CO.,LTD
MS-7441
Size C | Document Description: VCC_DDR / VTT_DDR/VCC3_SB | Rev 0A
Date: Friday, November 21, 2008 | Sheet 27 of 34

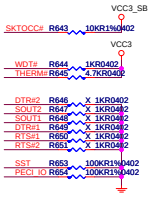

Cap. for EMI & Power
TPM
FRONT PANNEL
MICRO-STAR INT'L CO.,LTD
MS-7441
ATX F_Panel/EMI/TPM
Date: Friday, November 21, 2008
Sheet 28 of 34

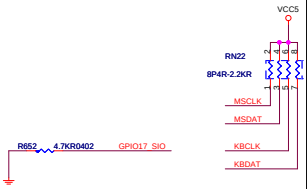


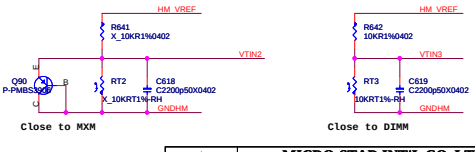


LPC I/O STRAPPING RESISTOR

STRAP	Don't STUFF	STUFF
SOUT1	4E (default)	2E
DTR1#	FAN START DUTY 60%	FAN START DUTY 100%
RTS1#	PIN49-54 = VID_OUT PIN42~47 = VID_IN	PIN49-54 = GPIO PIN42~47 = VIDIN/OUT
SOUT2	SPI_DISABLE	SPI_ENABLE
DTR2#	SPI_Backup	SPI_Primary
RTS2#	PWM FAN	LINEAR FAN





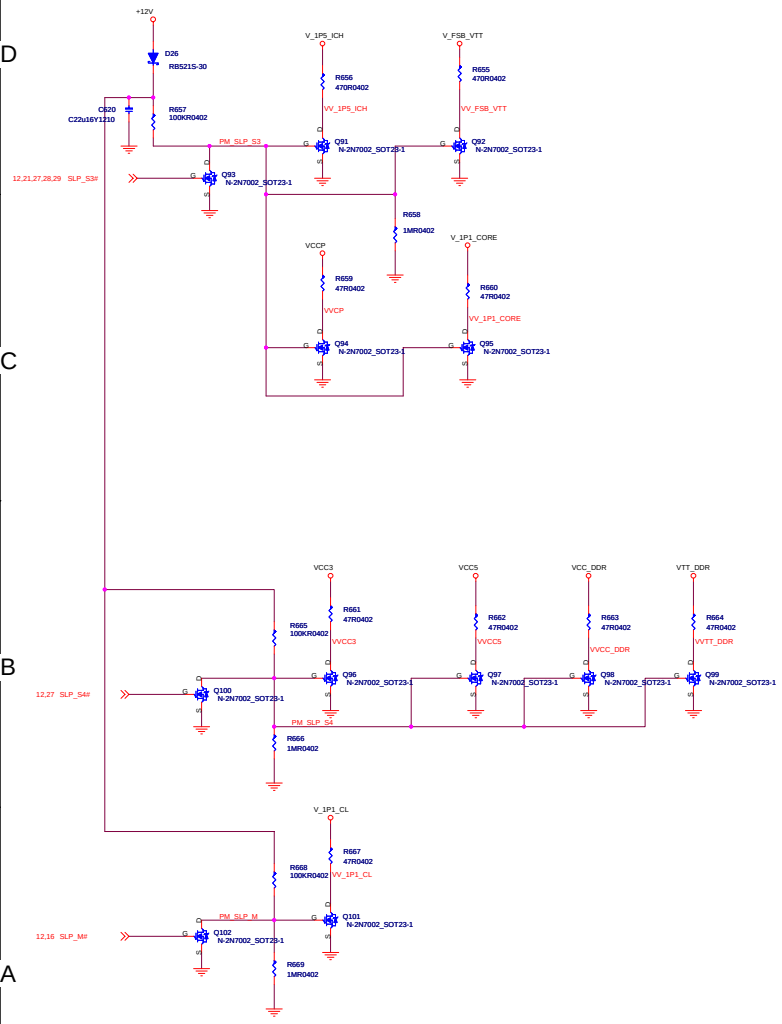


MICRO-STAR INT'L CO.,LTD

MS-7441

Size: Custom | Document Description: SIO-Fintek F71882F | Rev: 0A

Date: Friday, November 21, 2008 | Sheet 29 of 34



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7441	
Size: C	Document Description: Discharge circuit	Rev: 0A
Date: Friday, November 21, 2008	Sheet 30 of 34	

PCB

PCB1

MS-7441 0A,Red

Battery

BAT1_1

BAT-BCR2032P-RH

U2_PSD1

Intel ICH10R

X_ICH10R_A1

Heatsink

U2_X1

ICH10_Heatsink

U2_X2 HK1*3(-2)

U2_X3 HK1*3(-2)

U1_X1

X_EagleLake_HS

MH7

MH8

BIOS Label

B_LABEL1

BIOS_LABEL1

Optical Fiducial Marks

FM1 FM2 FM3 FM4 FM5

FM6 FM7 FM8 FM9

FM10 FM11 FM12 FM13

FM14 FM15 FM16 FM17

Innl

X_J1

SIM1

X_PIN1*2

Single-ended 50ohm W=5 mil

X_J3

SIM3N

X_PIN1*2

differential 95ohm W=4 S=8

X_J4

SIM3P

X_PIN1*2

differential 95ohm W=4 S=8

Top OR bottom

X_J2

SIM2

X_PIN1*2

Single-ended 50ohm W=4 mil

X_J6

SIM4P

X_PIN1*2

differential 90ohm W=4.5 S=7.5

X_J7

SIM4N

X_PIN1*2

differential 90ohm W=4.5 S=7.5

X_J5

SIM5

X_PIN1*2

Single-ended 40ohm W=8

Mounting Holes

MH1 MH2 MH3 MH4

MH5 MH6

R612 0R0402

AGND

VCC3 VCC5 VCC5_SB +12V

For EMI

C331 C332 C333 C334 C335 C336 C337 C338 C339 C340

C343 C344 C345 C346 C347 C348 C349 C350

C254 X_C0.1u16Y0402

C351 X_C0.1u16Y0402

C352 X_C0.1u16Y0402

X_C0.1u16Y0402

EMI SUGGESTION

VCC3 VCC5

C622 C624 C626 C628 X C0.1u16Y0402

VCC3_SB

C633 C635 C637 C0.1u16Y0402

VCC5_SB

C639 C640 C642 X C0.1u16Y0402

+12V

C648 C650 C652 C654 C655 X C0.1u16Y0402

VTT_DDR

C659 X C0.1u16Y0402

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7441	
Size: Custom	Document Description: MANUAL PARTS	Rev: 0A
Date: Friday, November 21, 2008	Sheet 31 of 34	

ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull up to VCC3_SB	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	Battery low detection	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	PCI-E WLAN card power on / Enable	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	pull-down with 100K	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	High to Inhibit FANs power on noise	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	DPRSLPVR / PWR_LEVEL for MXM	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	pull_up VCC3 with 10K.	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	SPI_HOLD_GPO#,not use	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505 iAMT,not use	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	USB power mode control,(Hi) S3 support,(Lo) USB PWR off	3.3V_SB		A11
GPIO 28	I/O	GPO	SPI_WP#	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#2 connect to USB connector (Port6,7)	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		M1
GPIO 32	I/O	GPO	NC	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	NC	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	SATACLKREQB_GP35,not use	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC0#	OC#0 connect to USB connector (Port0,1,2,3)	3.3V_SB		N3
GPIO 41	I/O	OC1#	OC#1 connect to USB connector (Port4,5)	3.3V_SB		P7
GPIO 42	I/O	OC1#	OC#1 connect to USB connector (Port4,5)	3.3V_SB		R7
GPIO 43	I/O	OC2#	OC#2 connect to USB connector (Port6,7)	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping ,not use	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use) , SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector (Port0,1,2,3)	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	GTLREF GPO	3.3V_SB		F18
GPIO 61	I/O	GPO	LPCPD#,connect to SIO and TPM	3.3V_SB	MUXED	R1
GPIO 62	I/O	GPO	(Not Use)	3.3V_SB	MUXED	R5
GPIO 63	I/O	GPO	(Not Use)	3.3V_SB		G17
GPIO 72	I/O	GPO	pull-up to VCC3_SB with 10K	3.3V_SB		C13

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#

SIO - F71882FG Configuration

PIN NAME	PIN#	USAGE	Input/Output
GPIO7	56	WDT#	OUTPUT
GPIO14	**63**	**DGPUPRSNT#**	**INPUT**
GPIO15	64	LED_VSB	OUTPUT
GPIO16	65	LED_VCC	OUTPUT
GPIO20,21	74,75	PLT_RST#	OUTPUT
GPIO32	84	PWR_OK	OUTPUT
GPIO26	80	PWRBTIN	INPUT
GPIO27	81	PWRBTN#	OUTPUT
GPIO30	82	SLP_S3#	INPUT
GPIO31	83	PS_ON#	OUTPUT
GPIO33	85	RSMRST#	OUTPUT
VSO	58	PECI	INPUT
VSI/SST	57	**SST**	OUTPUT
FAN_CTL1	**22**	CPU_FAN	OUTPUT
FAN_CTL2	**24**	**SYS1_FAN**	OUTPUT

Jumper Setting

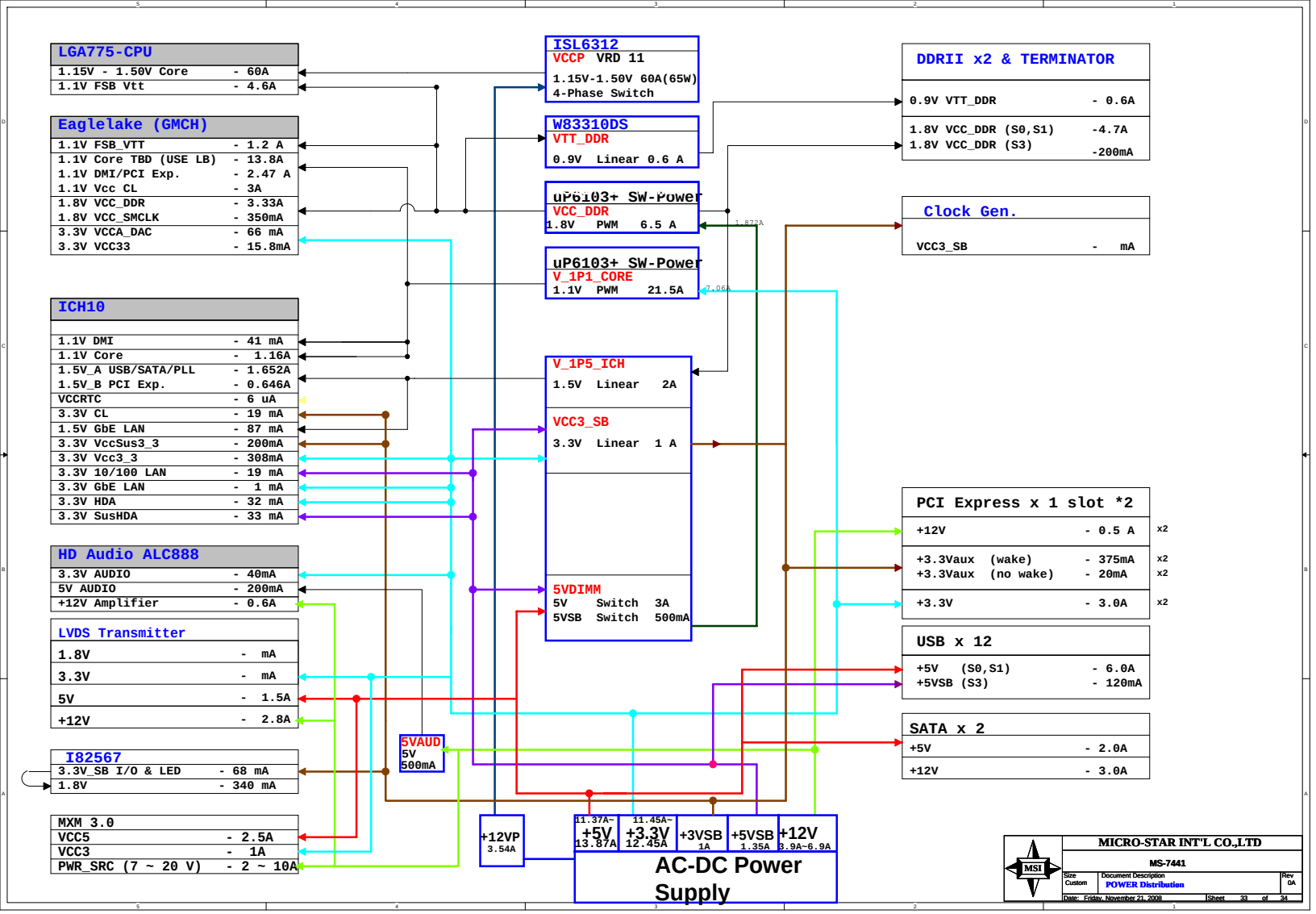
SW_CMOS1	(OFF)Normal	(ON)Clear CMOS
J1	(1-2)short: Normal	(1-2)Open: Clear PW
SW_RST1	(OFF) Normal	(ON)Restart System

MICRO-STAR INT'L CO.,LTD

MS-7441

Size: Custom | Document Description: GPIO & Jumper setting | Rev: 0A

Date: Friday, November 21, 2008 | Sheet 32 of 34


LGA775-CPU
1.15V - 1.50V Core - 60A
1.1V FSB Vtt - 4.6A
Eaglelake (GMCH)
1.1V FSB_VTT - 1.2 A
1.1V Core TBD (USE LB) - 13.8A
1.1V DMI/PCI Exp. - 2.47 A
1.1V Vcc CL - 3A
1.8V VCC_DDR - 3.33A
1.8V VCC_SMCLK - 350mA
3.3V VCCA_DAC - 66 mA
3.3V VCC33 - 15.8mA
ICH10
1.1V DMI - 41 mA
1.1V Core - 1.16A
1.5V_A USB/SATA/PLL - 1.652A
1.5V_B PCI Exp. - 0.646A
VCCRTC - 6 uA
3.3V CL - 19 mA
1.5V GbE LAN - 87 mA
3.3V VccSus3_3 - 200mA
3.3V Vcc3_3 - 308mA
3.3V 10/100 LAN - 19 mA
3.3V GbE LAN - 1 mA
3.3V HDA - 32 mA
3.3V SusHDA - 33 mA
HD Audio ALC888
3.3V AUDIO - 40mA
5V AUDIO - 200mA
+12V Amplifier - 0.6A
LVDS Transmitter
1.8V - mA
3.3V - mA
5V - 1.5A
+12V - 2.8A
I82567
3.3V_SB I/O & LED - 68 mA
1.8V - 340 mA
MXM 3.0
VCC5 - 2.5A
VCC3 - 1A
PWR_SRC (7 ~ 20 V) - 2 ~ 10A
ISL6312
VCCP VRD 11
1.15V-1.50V 60A(65W)
4-Phase Switch
W83310DS
VTT_DDR
0.9V Linear 0.6 A
uP6103+ SW-Power
VCC_DDR
1.8V PWM 6.5 A
uP6103+ SW-Power
V_1P1_CORE
1.1V PWM 21.5A
V_1P5_ICH
1.5V Linear 2A
VCC3_SB
3.3V Linear 1 A
5VDIMM
5V Switch 3A
5VSB Switch 500mA
5VAUD
5V
500mA
DDRII x2 & TERMINATOR
0.9V VTT_DDR - 0.6A
1.8V VCC_DDR (S0,S1) -4.7A
1.8V VCC_DDR (S3) -200mA
Clock Gen.
VCC3_SB - mA
PCI Express x 1 slot *2
+12V - 0.5 A x2
+3.3Vaux (wake) - 375mA x2
+3.3Vaux (no wake) - 20mA x2
+3.3V - 3.0A x2
USB x 12
+5V (S0,S1) - 6.0A
+5VSB (S3) - 120mA
SATA x 2
+5V - 2.0A
+12V - 3.0A
+12VP
3.54A
11.37A~
+5V
13.87A
11.45A~
+3.3V
12.45A
+3VSB
1A
+5VSB
1.35A
+12V
3.9A~6.9A
AC-DC Power Supply
MICRO-STAR INT'L CO.,LTD
MS-7441
Size Custom
Document Description
POWER Distribution
Rev 0A
Date: Friday, November 21, 2008
Sheet 33 of 34

MICRO-STAR INT'L CO.,LTD

MS-7441

Size: Custom

Document Description: History

Rev: 0A

Date: Friday, November 21, 2008

Sheet 34 of 34