MS-7440

Version 0A

CPU:

Intel Dimondville

System Chipset:

Intel 945GSE (North Bridge)
Intel ICH7M(South Bridge)

On Board Chipset:

Clock Generator - ICS9LPRS113

HD AUDIO CODEC(ALC888)

Giga LAN -- Realtek RTL8111C

LVDS CHRONTEL - CH7308B(option)

SIO-Fintek F71882F

Card Reader RTS5158E

AMP - (TBD)

BIOS -- SPI

Main Memory:

DDR II SO-DIMM x 1 (Max 1GB)

Expansion Slots:

Internal Mini PCIE x1

Intersil PWM:

Controller: ISL6261CRZ-T

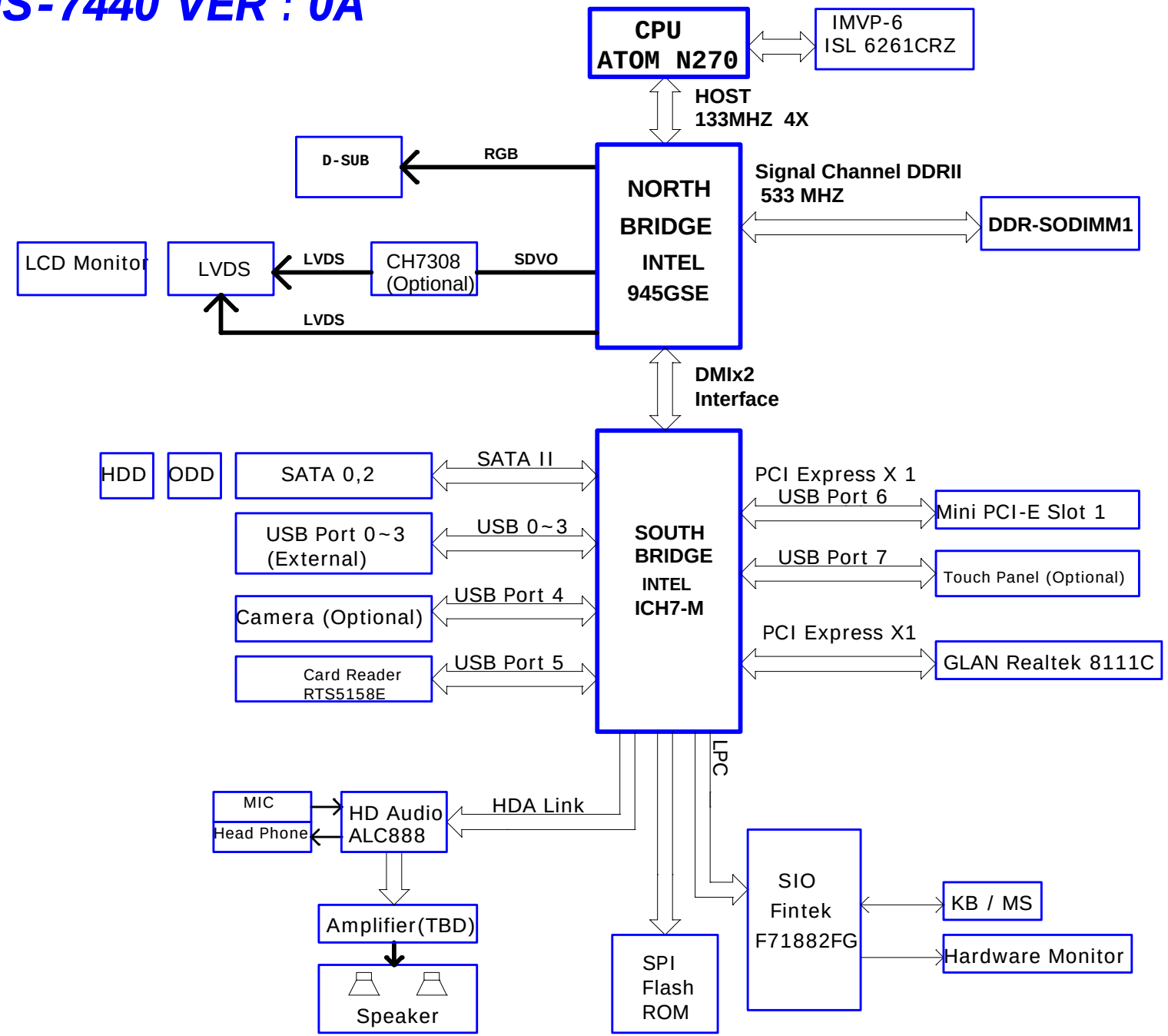
MICRO-STAR INT'L CO.,LTD

MS-7440

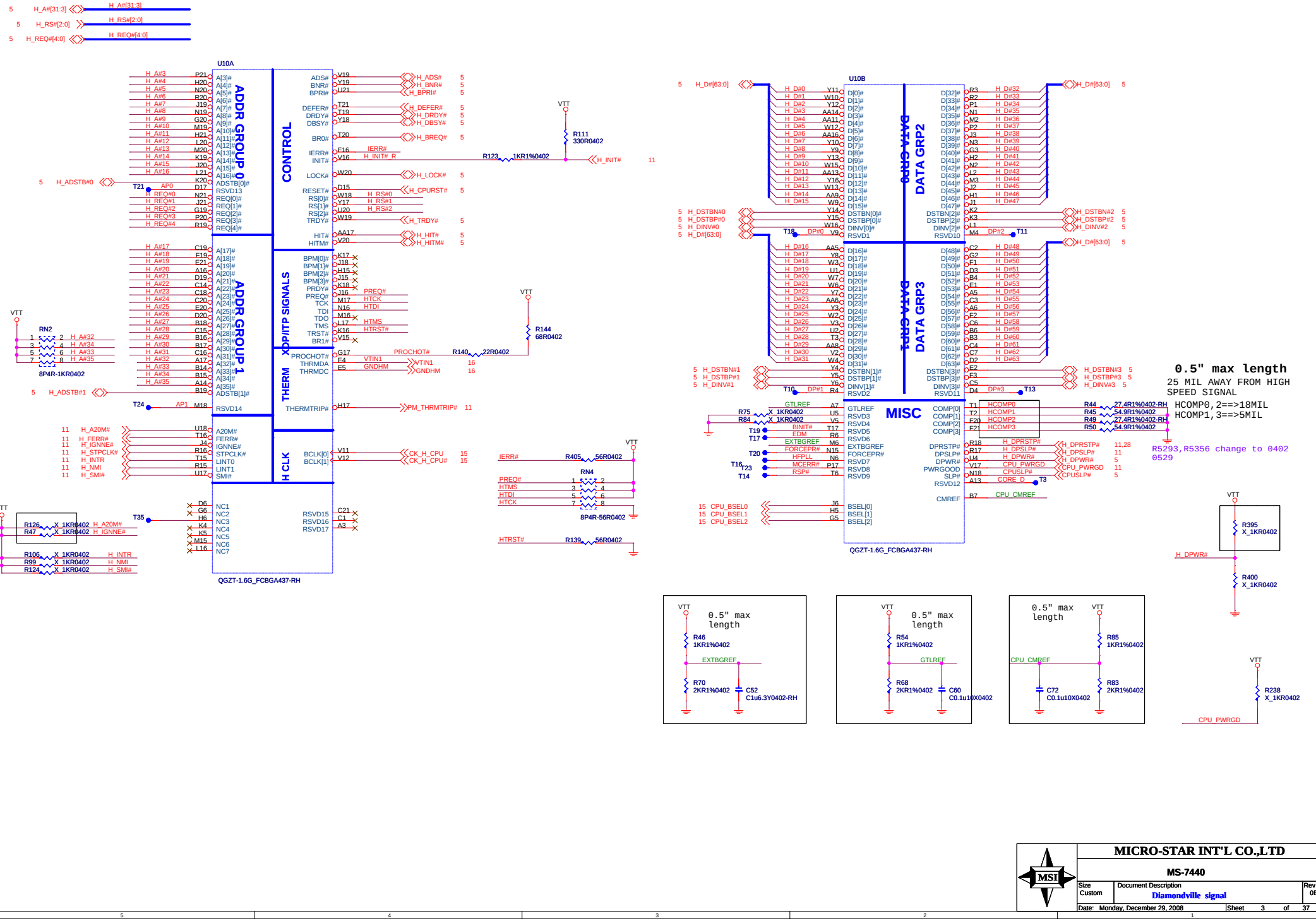
Size: Custom | Document Description: COVER SHEET | Rev: 0B

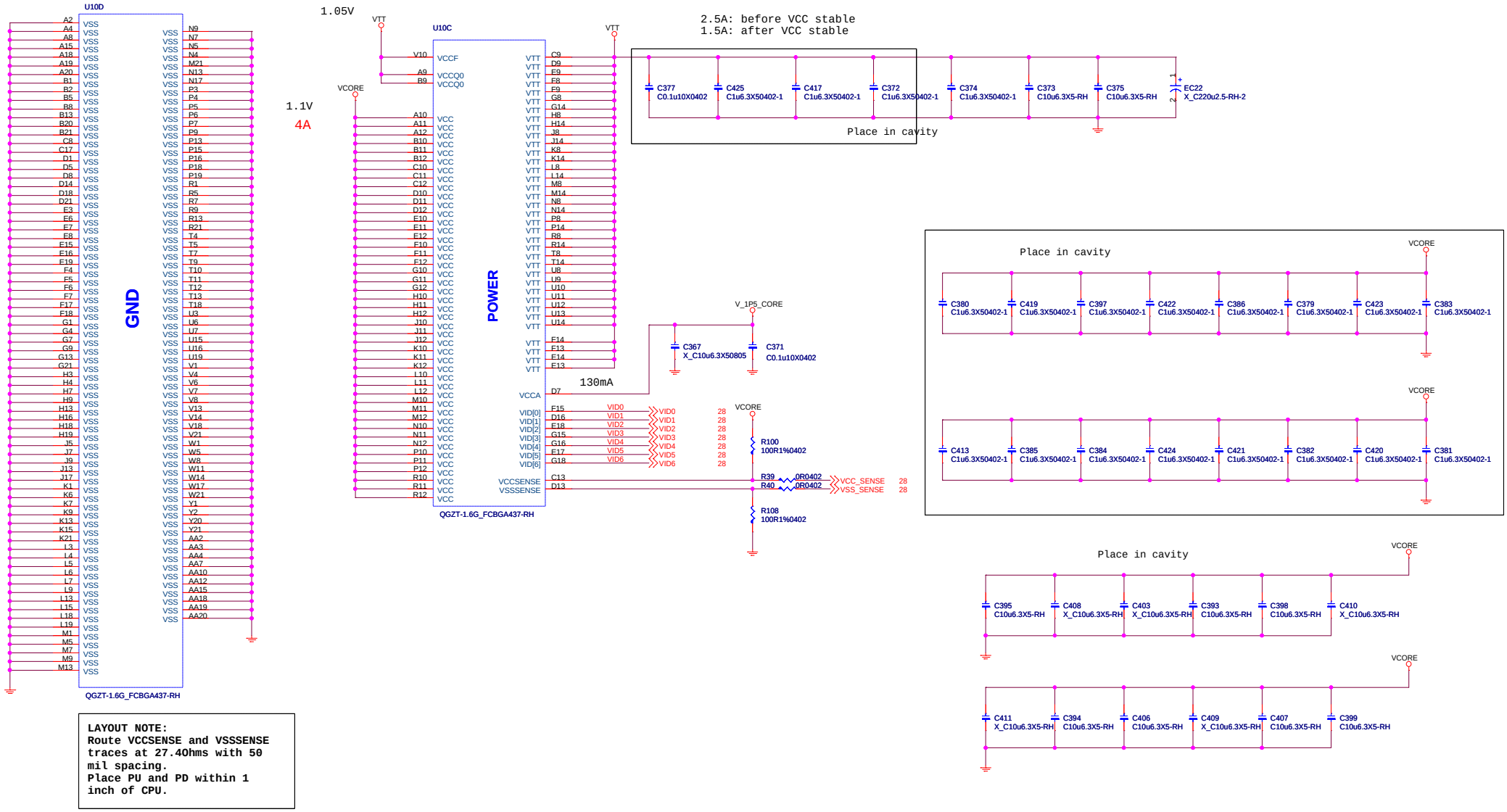
Date: Monday, December 29, 2008 | Sheet 1 of 37

MS-7440 VER : 0A



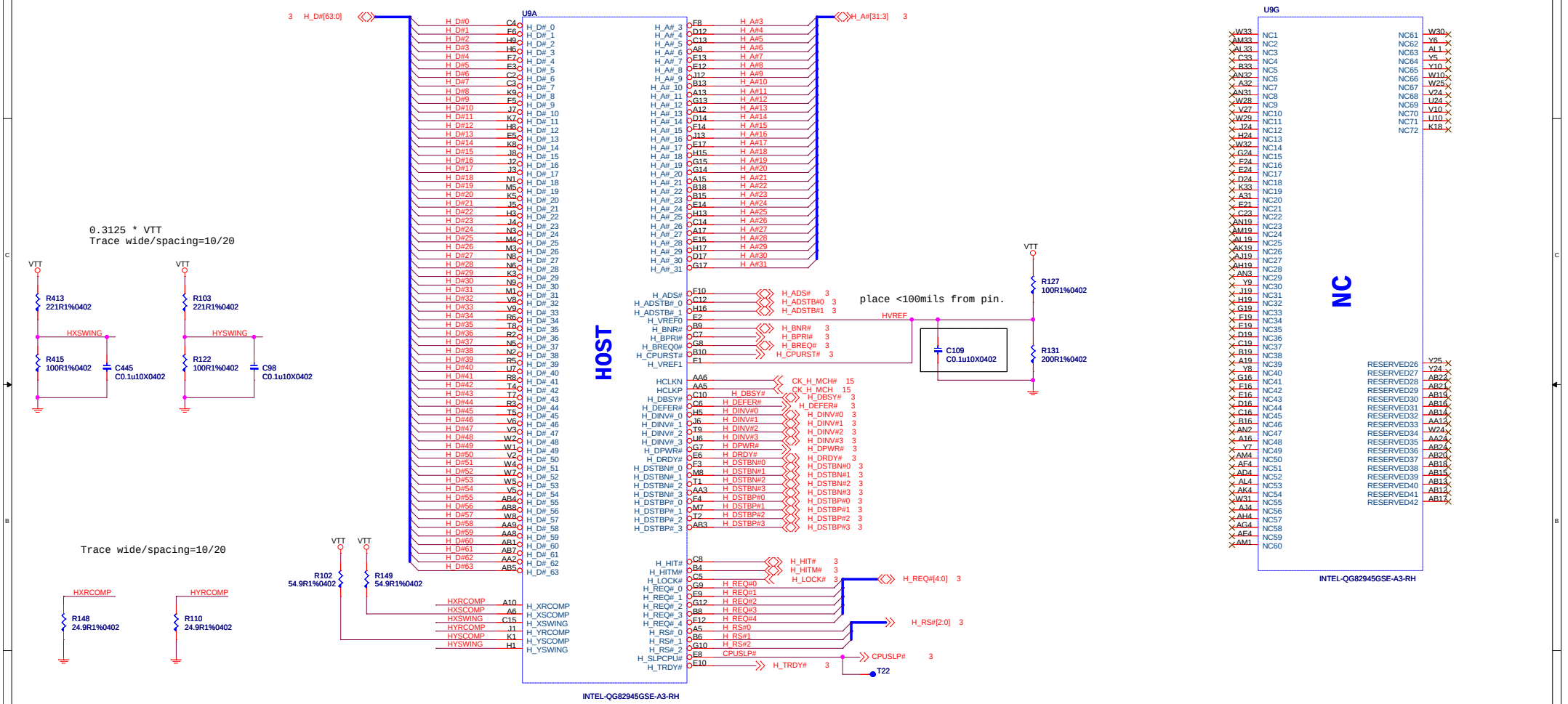
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7440	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0B
Date: Monday, December 29, 2008	Sheet 2 of 37	


U10A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
DP/ITP SIGNALS
THERM
H CLK
QGZT-1.6G_FCBGA437-RH
U10B
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
QGZT-1.6G_FCBGA437-RH
0.5" max length
25 MIL AWAY FROM HIGH SPEED SIGNAL
HCOMP0,2==>18MIL
HCOMP1,3==>5MIL
R5293,R5356 change to 0402
0529
MICRO-STAR INT'L CO.,LTD
MS-7440
Diamondville signal
Date: Monday, December 29, 2008
Sheet 3 of 37

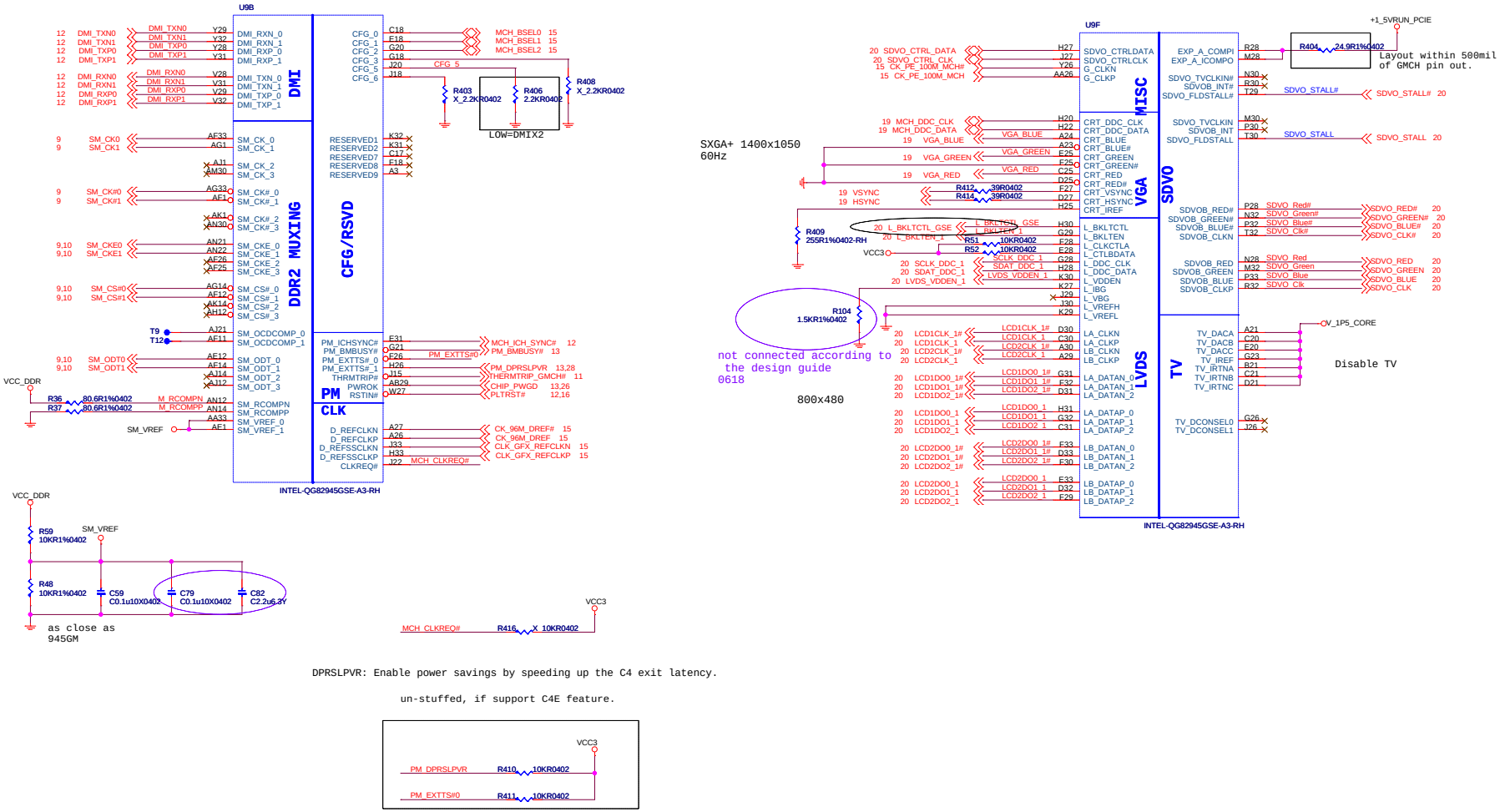


LAYOUT NOTE:
Route VCCSENSE and VSSSENSE traces at 27.4Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

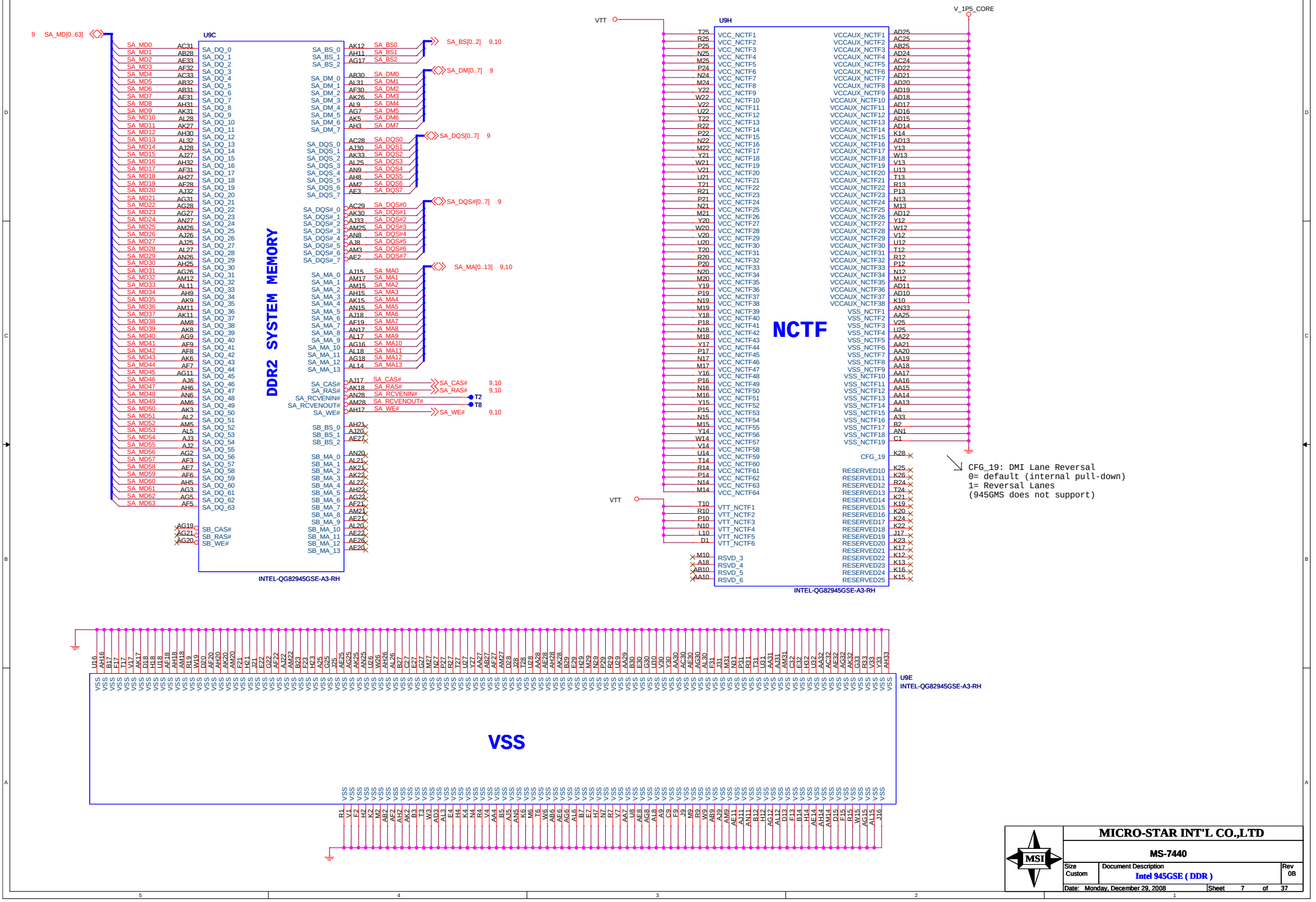
MICRO-STAR INT'L CO.,LTD	
MS-7440	
Size: Custom	Document Description: Diamondville_Power/GND
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 4 of 37



MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: Intel 945GSE (HOST)	Rev: 0B
Date: Monday, December 29, 2008	Sheet 5 of 37	



MICRO-STAR INT'L CO.,LTD	
MS-7440	
Size: Custom	Document Description: Intel 945GSE (DMI / VGA)
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 6 of 37



MICRO-STAR INT'L CO.,LTD	
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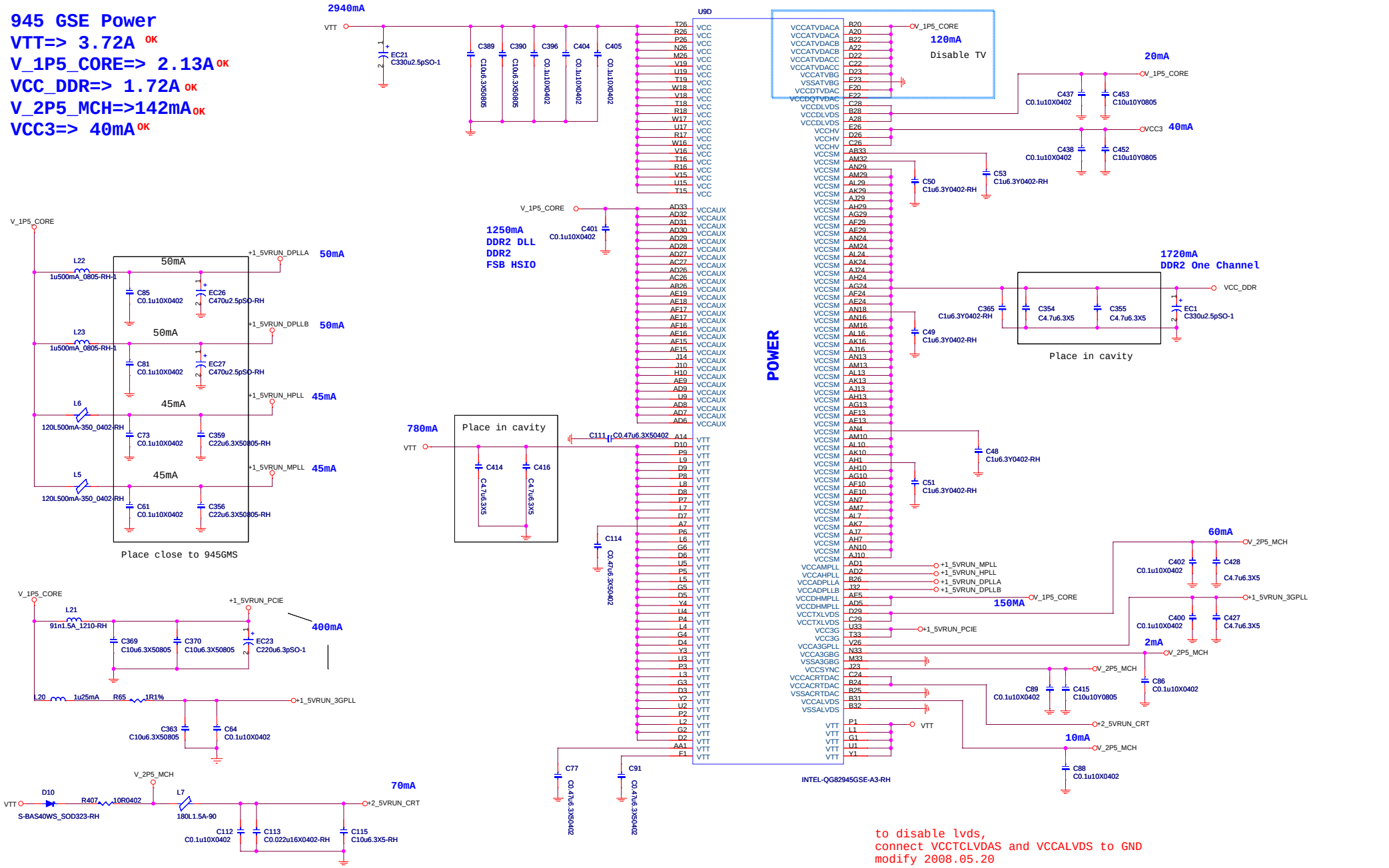
Size: Custom	Document Description: Intel 945GSE (DDR)
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 7 of 37

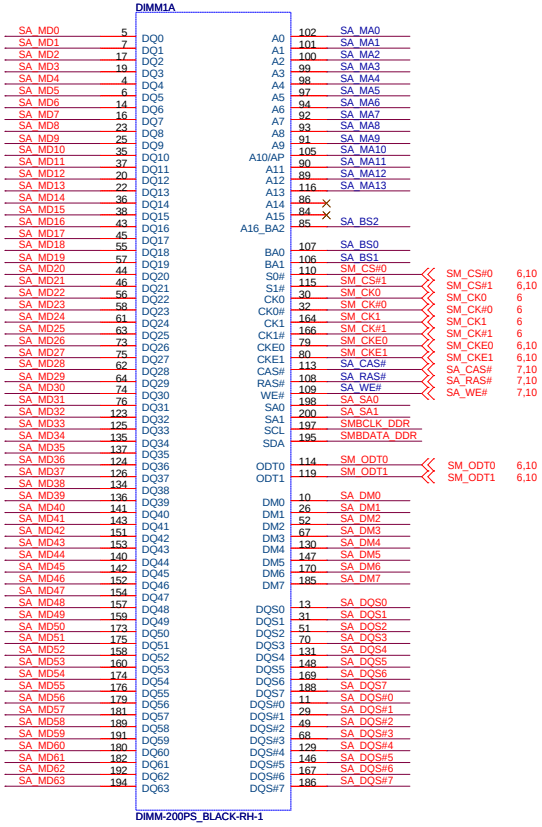
945 GSE Power

- VTT=> 3.72A OK
- V_1P5_CORE=> 2.13A OK
- VCC_DDR=> 1.72A OK
- V_2P5_MCH=>142mA OK
- VCC3=> 40mA OK

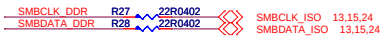


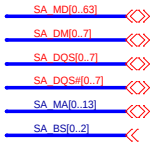
to disable lvds,
connect VCCTCLVDAS and VCCALVDS to GND
modify 2008.05.20

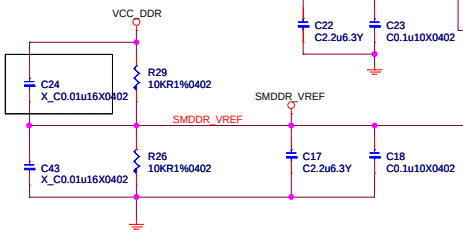
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: Intel 945GSE (Power)	Rev: 0B
Date: Monday, December 29, 2008	Sheet 8 of 37	

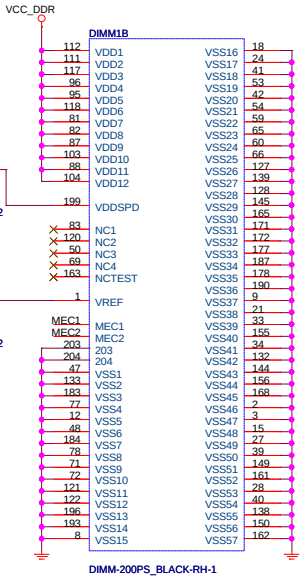


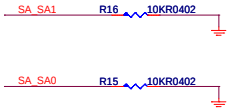
N13-2000220-A10
Bottom



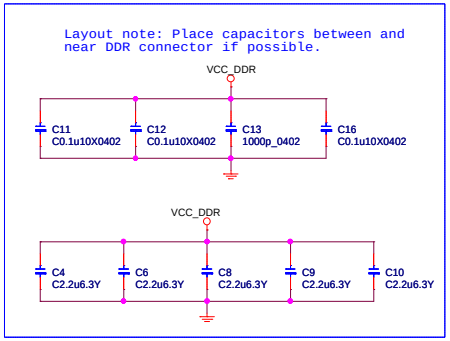




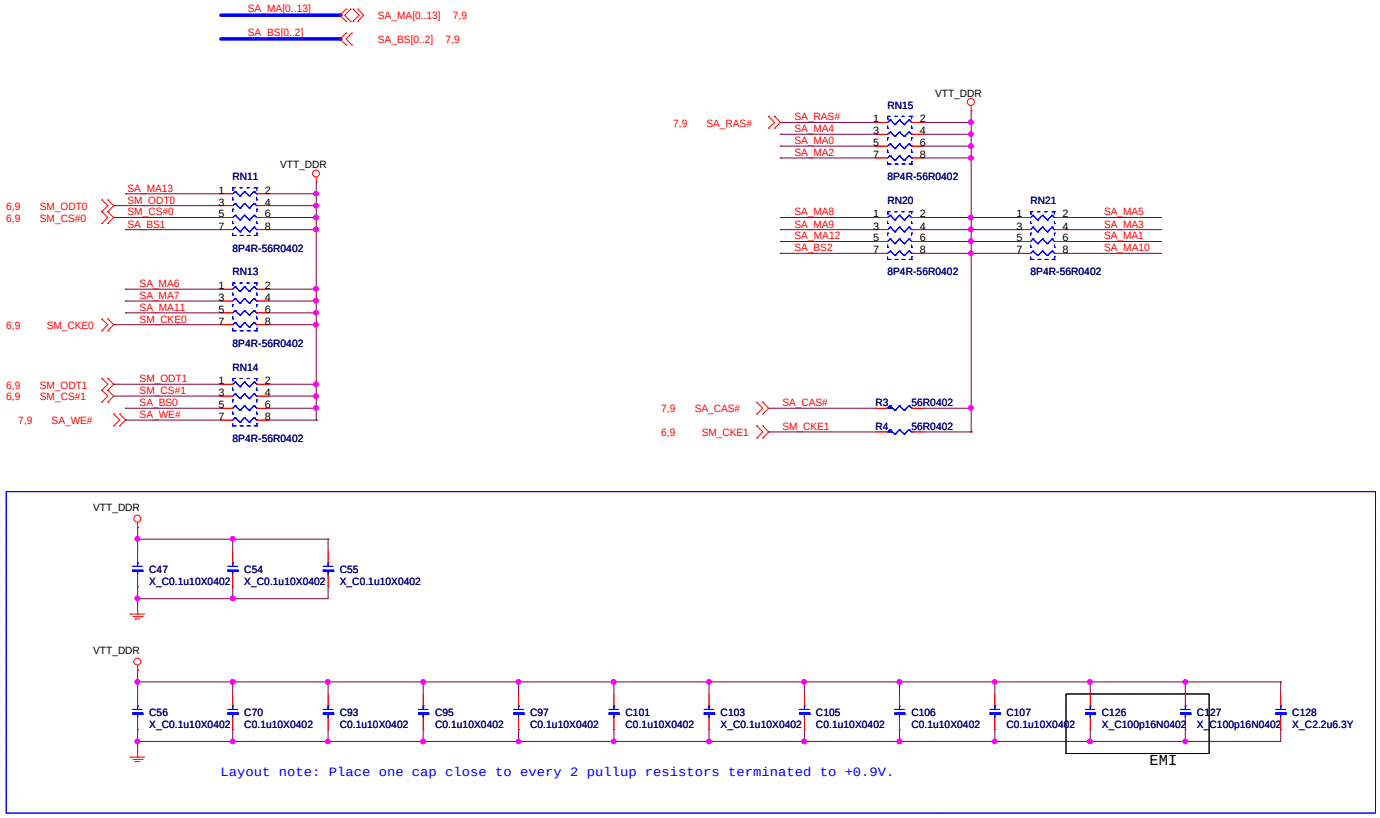




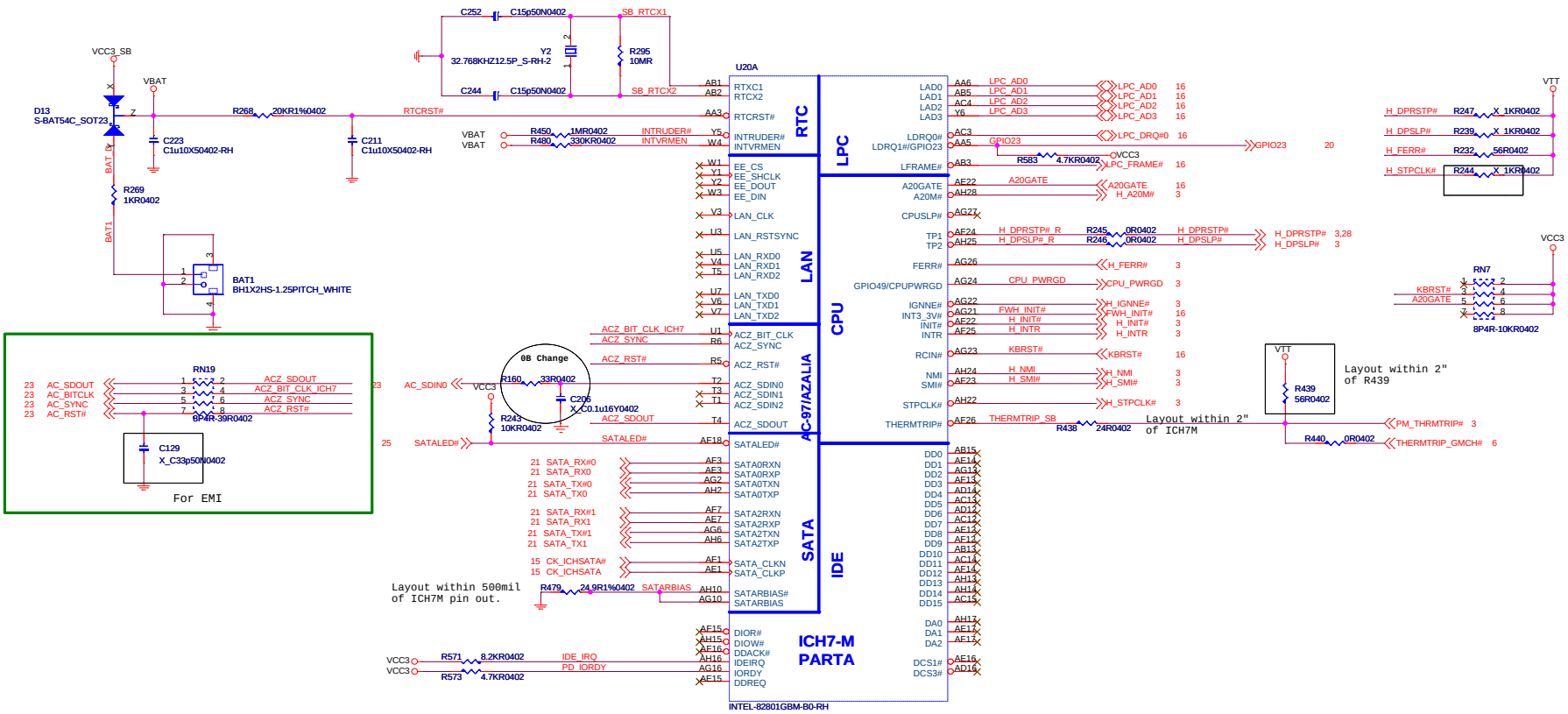
ADDRESS: 000
0xA0



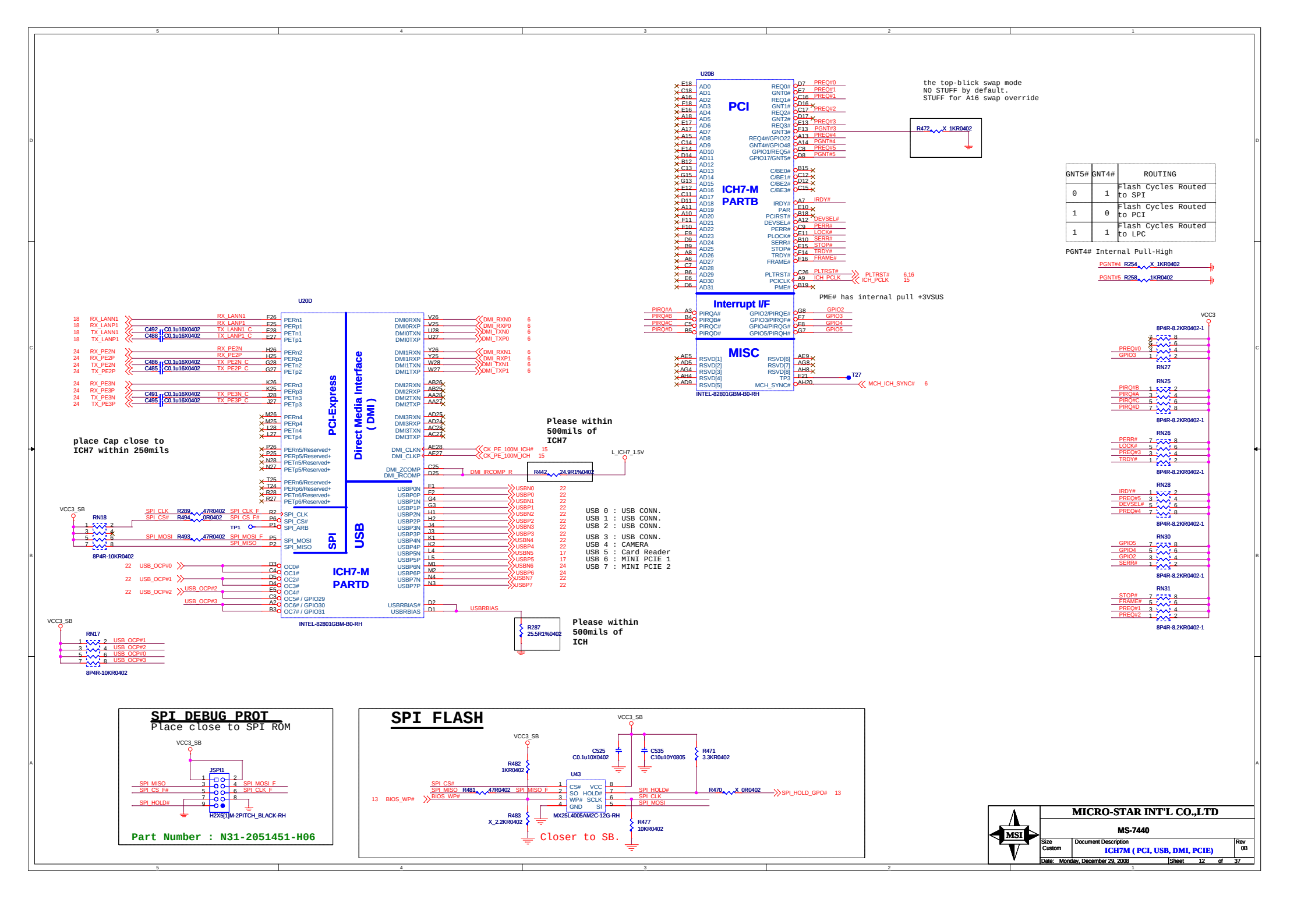
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: DDR2 SO-DIMM1 Slot	Rev: 0B
Date: Monday, December 29, 2008	Sheet 9 of 37	

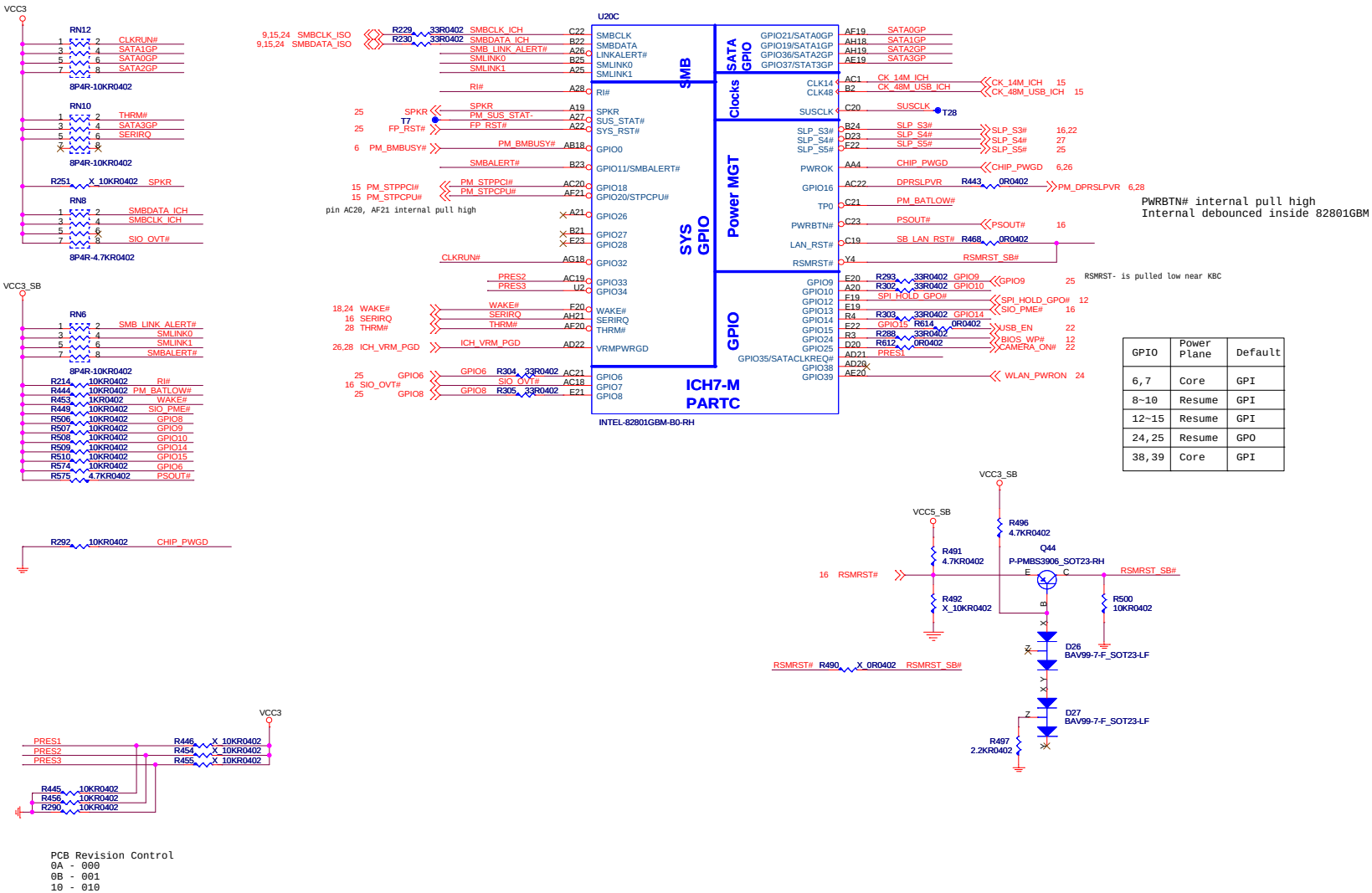


MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: DDR2 Termination	Rev: 0B
Date: Monday, December 29, 2008	Sheet 10 of 37	



MICRO-STAR INT'L CO.,LTD	
MS-7440	
Size: Custom	Document Description: ICH7M (CPU,LPC,SATA,HDA)
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 11 of 37


U20B
PCI
ICH7-M
PARTB
Interrupt I/F
MISC
INTEL-82801GBM-B0-RH
the top-blick swap mode
NO STUFF by default.
STUFF for A16 swap override
R472 X_1KR0402
PME# has internal pull +3VSUS
GNT5# GNT4# ROUTING
0 1 Flash Cycles Routed to SPI
1 0 Flash Cycles Routed to PCI
1 1 Flash Cycles Routed to LPC
PGNT4# Internal Pull-High
PGNT#4 R254 X_1KR0402
PGNT#5 R258 1KR0402
U20D
PCI-Express
Direct Media Interface (DMI)
USB
SPI
ICH7-M
PARTD
INTEL-82801GBM-B0-RH
place Cap close to ICH7 within 250mils
Please within 500mils of ICH7
R442 24.9R1%0402
L_ICH7_1.5V
R287 25.5R1%0402
Please within 500mils of ICH
USB 0 : USB CONN.
USB 1 : USB CONN.
USB 2 : USB CONN.
USB 3 : USB CONN.
USB 4 : CAMERA
USB 5 : Card Reader
USB 6 : MINI PCIE 1
USB 7 : MINI PCIE 2
RN18
8P4R-10KR0402
RN17
8P4R-10KR0402
RN27
RN25
RN26
RN28
RN30
RN31
8P4R-8.2KR0402-1
SPI DEBUG PROT
Place close to SPI ROM
JSPI1
H2X5[1]M-2PITCH_BLACK-RH
Part Number : N31-2051451-H06
SPI FLASH
U43
MX25L4005AM2C-12G-RH
R482 1KR0402
R483 X_2.2KR0402
R471 3.3KR0402
R477 10KR0402
R470 X_0R0402
C525 C0.1u10X0402
C535 C10u10Y0805
Closer to SB.
MICRO-STAR INT'L CO.,LTD
MS-7440
ICH7M (PCI, USB, DMI, PCIE)
Date: Monday, December 29, 2008
Sheet 12 of 37



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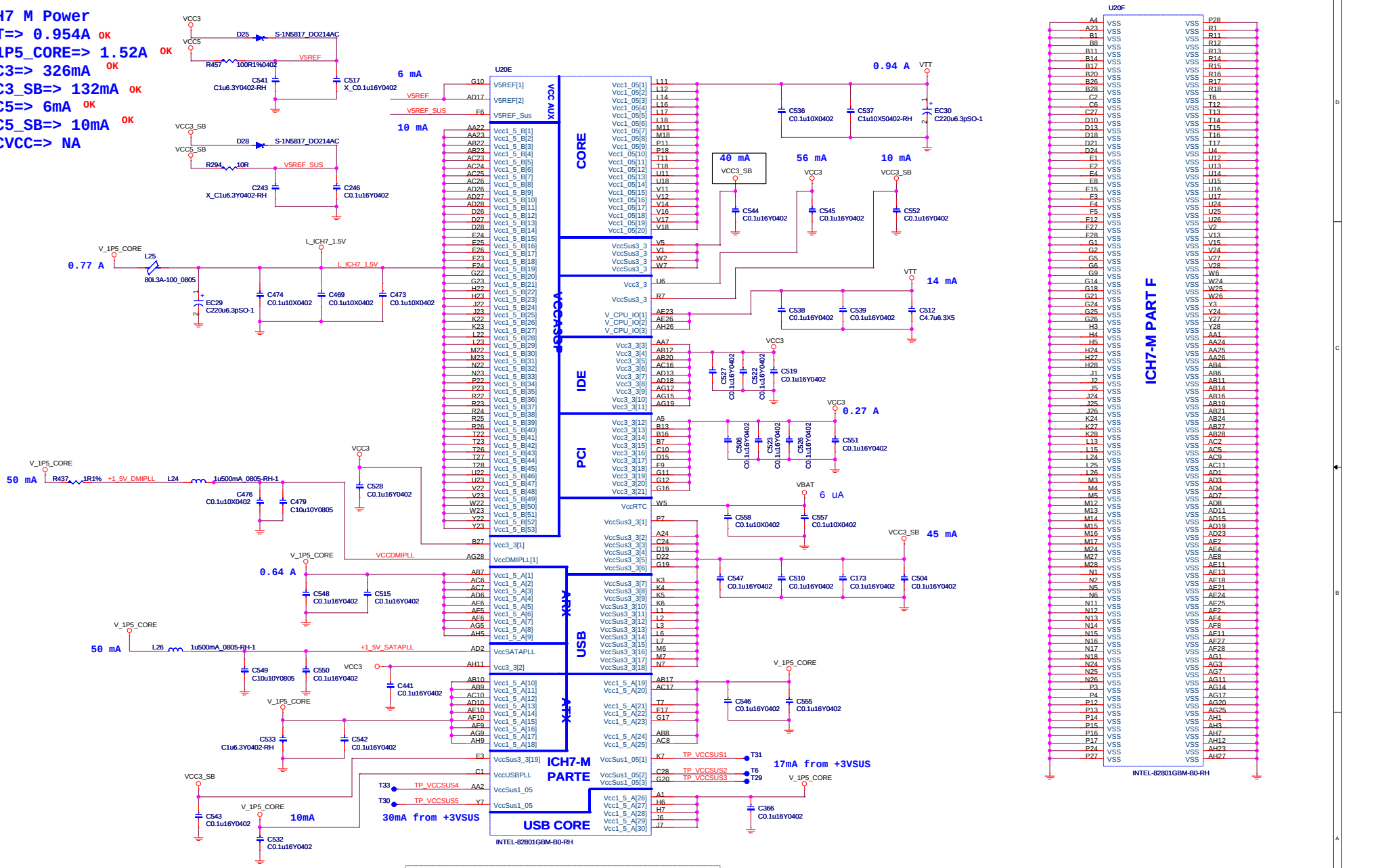
MS-7440		
Size: Custom	Document Description: ICH7M (GPIO,CLK,SM)	Rev: 0B
Date: Monday, December 29, 2008	Sheet 13 of 37	

ICH7 M Power
VTT=> 0.954A OK
V_1P5_CORE=> 1.52A OK
VCC3=> 326mA OK
VCC3_SB=> 132mA OK
VCC5=> 6mA OK
VCC5_SB=> 10mA OK
RTCVCC=> NA



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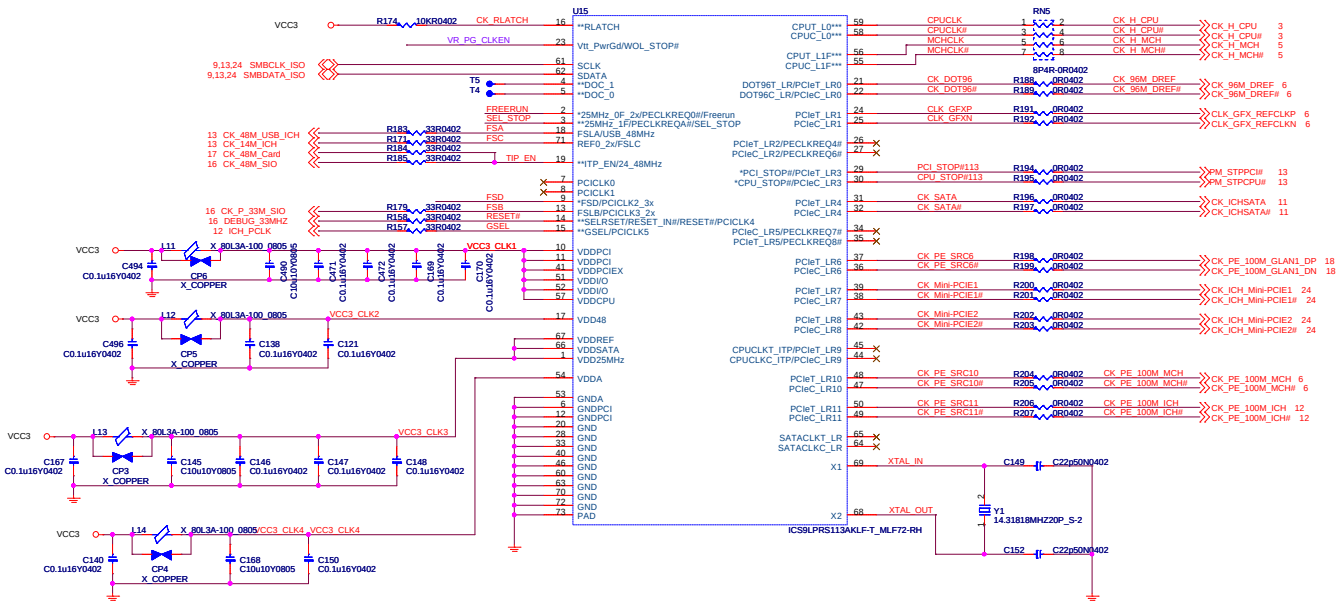
MS-7440	
Size: Custom	Document Description: ICH7M (Power)
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 14 of 37

CLK Gen ICS9LPRS113



CLOCK GEN STRAPING

1 => Pin21/22 96MHz
0 => Pin21/22 100MHz

GSEL — R175 4.7KR0402 — VCC3
R176 X 4.7KR0402

L-PCICLK4
H:RESET*
to be WDT rest=> HI

RESET# — R177 4.7KR0402

113
TIP_EN=0 => PCIEX9,
TIP_EN=1 => CPU_ITP

TIP_EN — R186 X 4.7KR0402

FREERUN — R156 X 4.7KR0402 — VCC3
R173 X 4.7KR0402

Selects pin 29/830
1 = PCI_STOP#/CPU_STOP#
0 =PCIEX CLK output

SEL_STOP — R155 4.7KR0402 — VCC3
R172 X 4.7KR0402

FSD — R180 10KR0402

pull high to VTT
modify 0530

VTT — R154 1KR0402, R153 1KR0402, R152 1KR0402

CPU_BSEL0	R164 1KR0402	MCH_BSEL0 6
CPU_BSEL1	R159 1KR0402	MCH_BSEL1 6
CPU_BSEL2	R161 1KR0402	MCH_BSEL2 6

R181 10KR0402 FSA
R178 10KR0402 FSB
R170 10KR0402 FSC

VCC3 — R193 1KR0402 — VR_PWRGD_CLKEN

28 VR_PWRGD_CLKEN# — Q17 N-2N7002_SOT23-1

CK_P_33M_SIO	C124	X_C10p25N0402
ICH_PCLK	C122	X_C10p25N0402
CK_48M_Card	C139	X_C10p25N0402
DEBUG_33MHZ	C123	X_C10p25N0402
CK_48M_USB_ICH	C137	X_C10p25N0402
CK_48M_SIO	C141	X_C10p25N0402
CK_14M_ICH	C125	X_C10p25N0402

CPU Table

BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	100MHZ
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

CLK Gen 113

BSEL[2]	BSEL[1]	BSEL[0]	BCLK
H	L	H	100MHZ
L	L	H	133MHZ
L	H	L	200MHz
L	H	H	166MHZ

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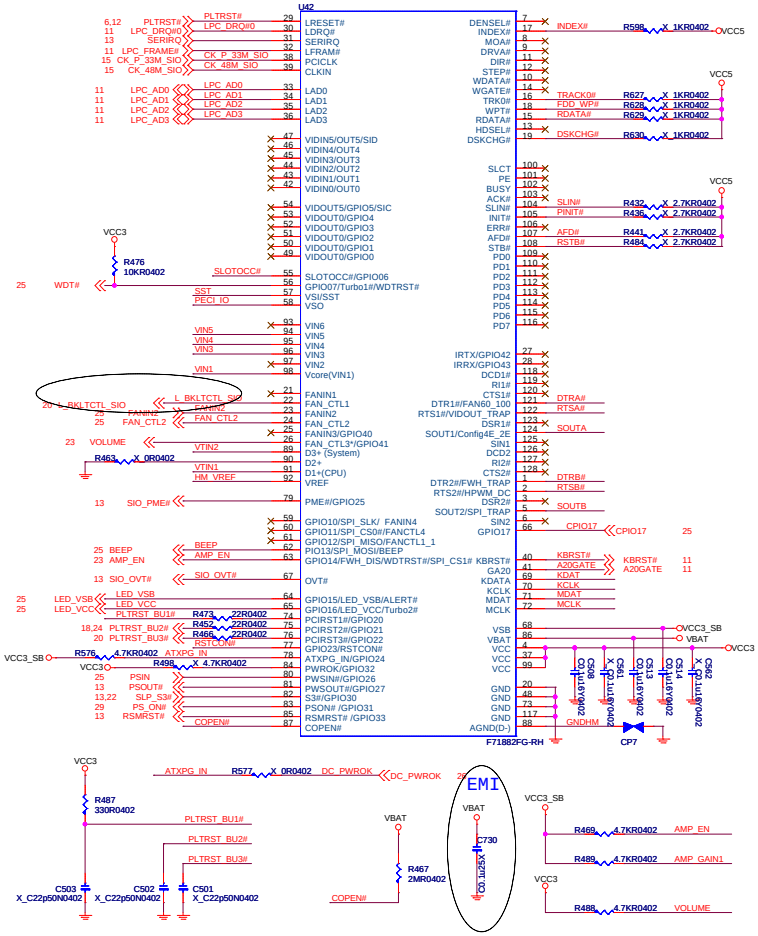
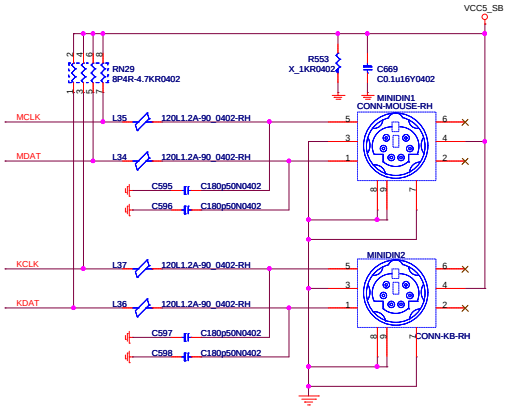
MS-7440

Size: Custom | Document Description: CLK GEN [ICS9LPRS113] | Rev: 0B

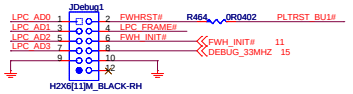
Date: Monday, December 29, 2008 | Sheet 15 of 37



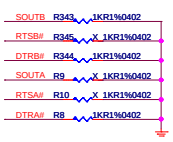
PS2 KEYBOARD & MOUSE CONNECTOR

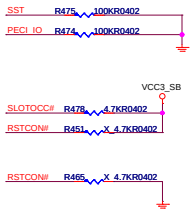


LPC Debug Port

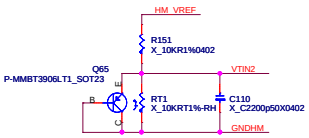


STRAPPING RESISTOR

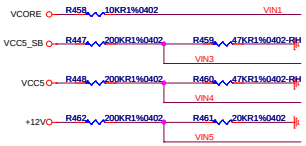


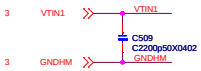


Thermal Resistor



Hardware monitor





Pin	Function	Net name	HI	LO
1	FWH_TRAP	DTRB#	SPI as a backup BIOS	SPI as a primary BIOS
2	HPWM_DC	RTSB#	PWM Fan	LINEAR FAN
5	SPI_TRAP	SOUTB	SPI function disable	SPI function enable
121	FAN60_100	DTRA#	Power on FAN speed DUTY : 60%	Power on FAN speed DUTY : 100%
122	VIDOUT	RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
124	Config4E_2E	SOUTA	4E	2E

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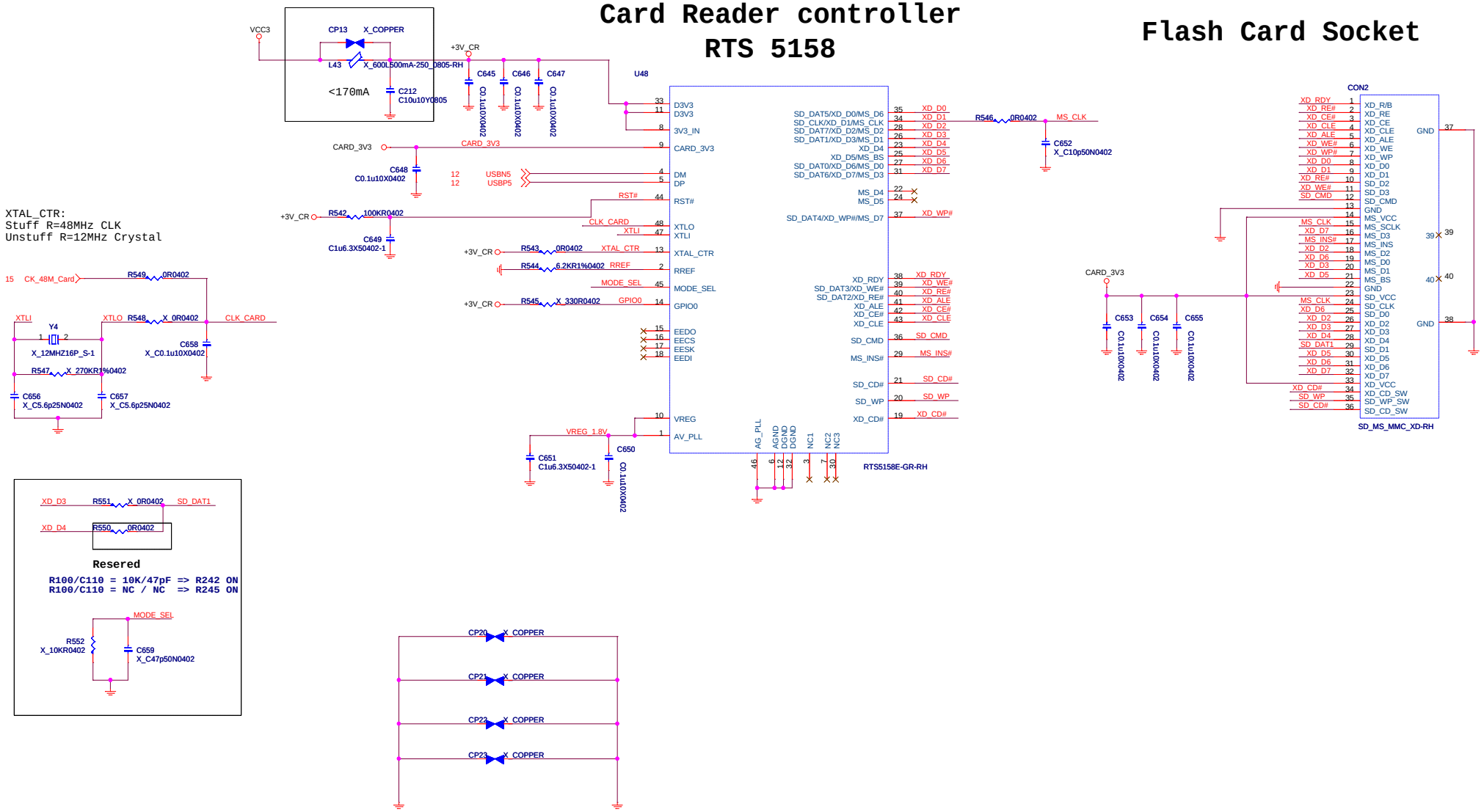
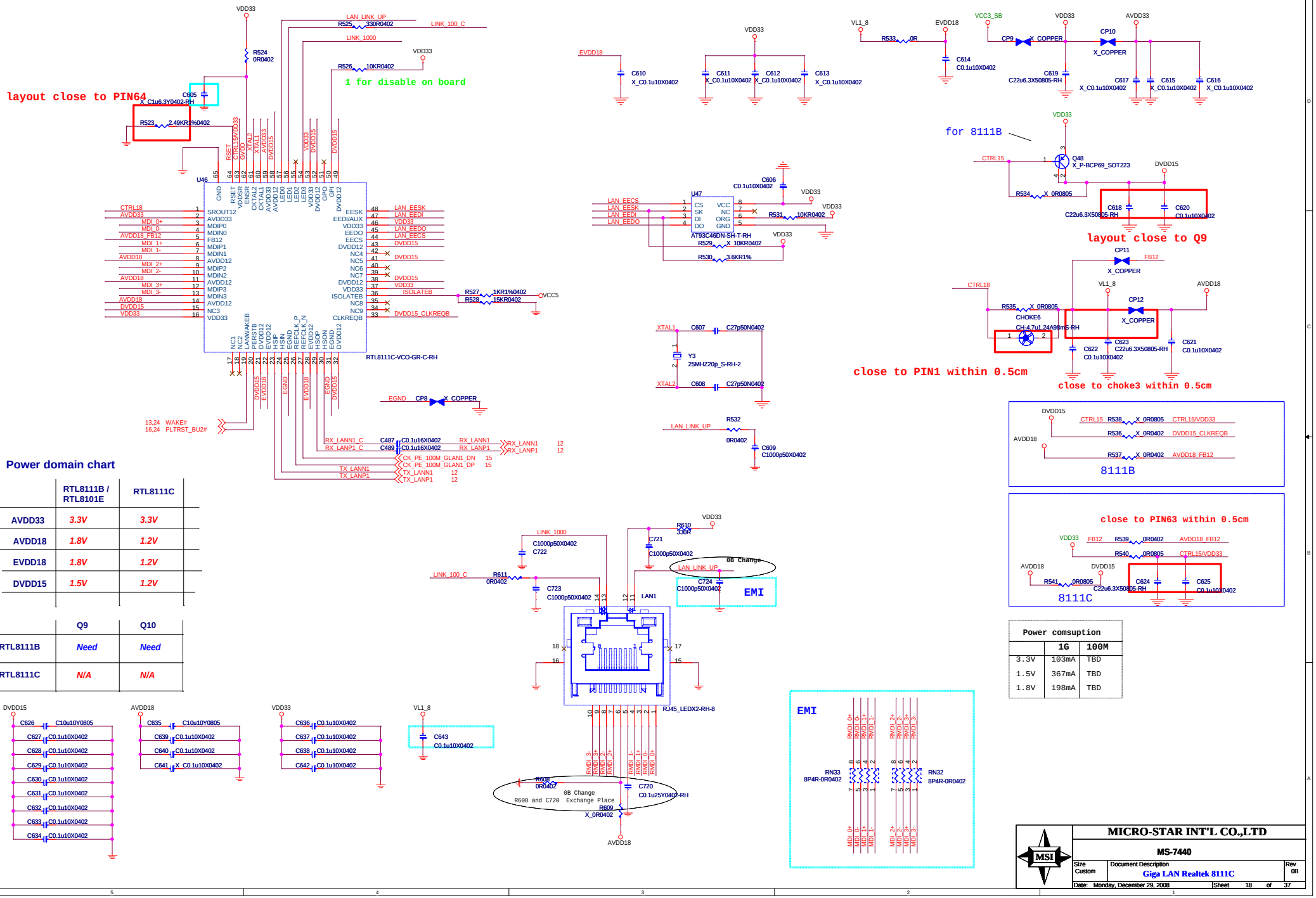
	MS-7440		
Size: Custom	Document Description: SIO-Fintek F71882F		Rev: 0B
Date: Monday, December 29, 2008	Sheet 16 of 37		

Card Reader controller
RTS 5158

Flash Card Socket



MICRO-STAR INT'L CO.,LTD	
MS-7440	
Size: Custom	Document Description: Card Reader RTS5158E
Rev: 0B	
Date: Monday, December 29, 2008	Sheet 17 of 37



Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q9	Q10
RTL8111B	Need	Need
RTL8111C	N/A	N/A

Power comsuption

	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

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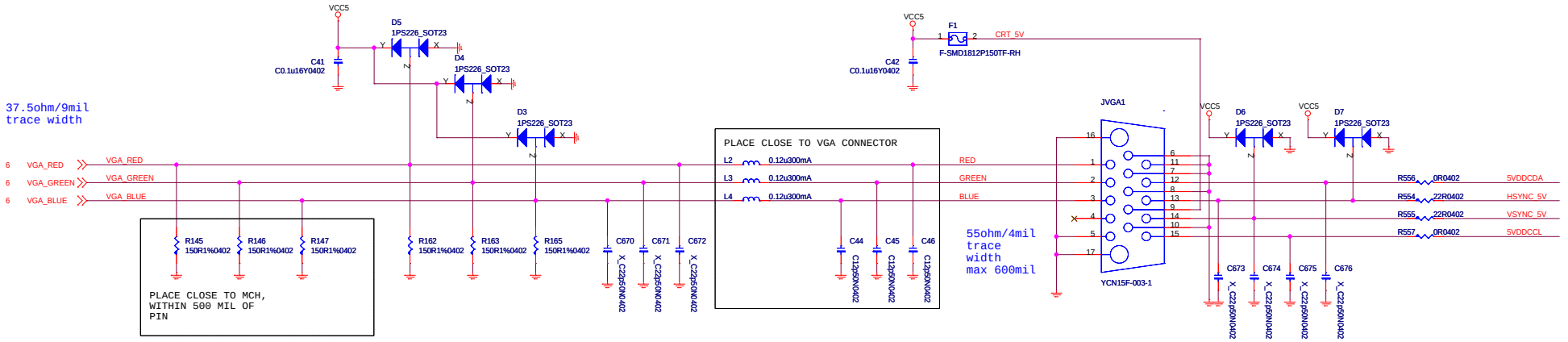
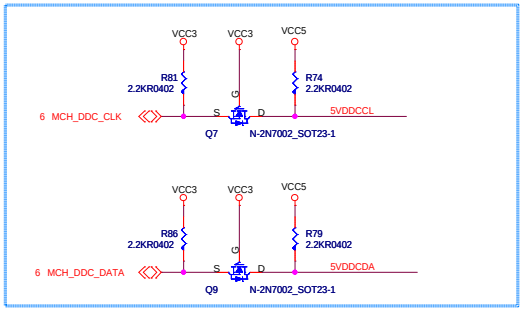
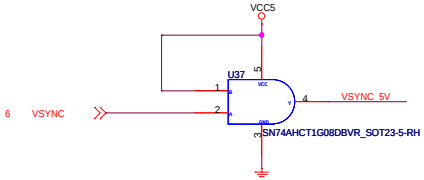
MS-7440		
Size: Custom	Document Description: Giga LAN Realtek 8111C	Rev: 0B
Date: Monday, December 29, 2008	Sheet 18 of 37	

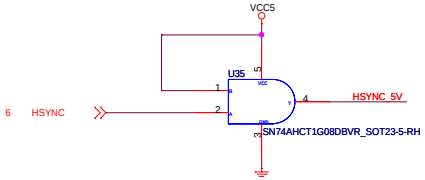
Video Connector

change ESD diode
modify 0609



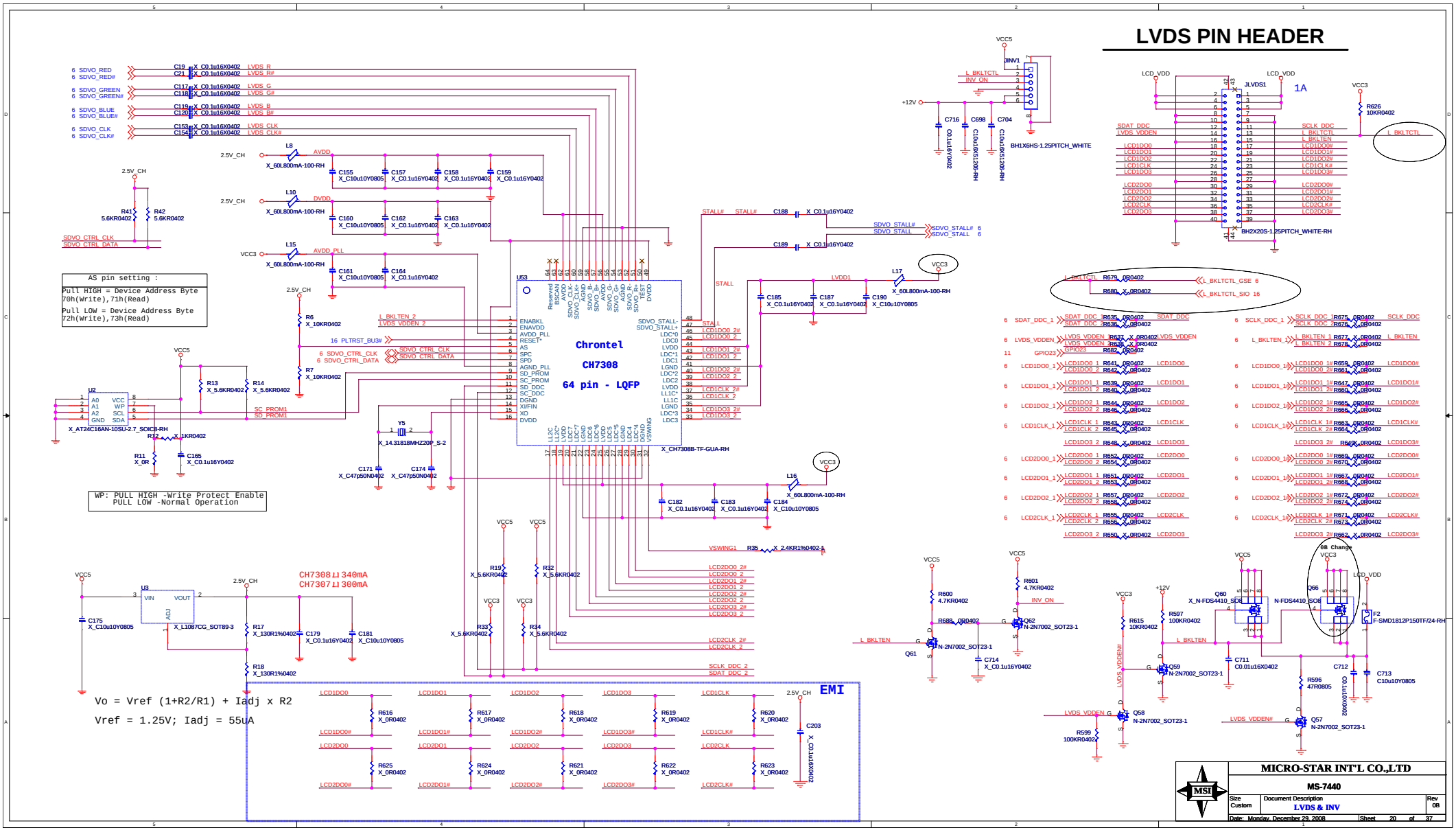




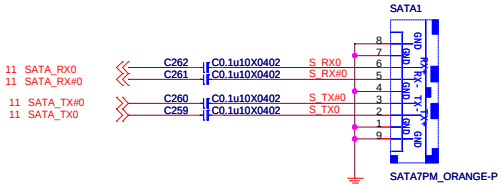


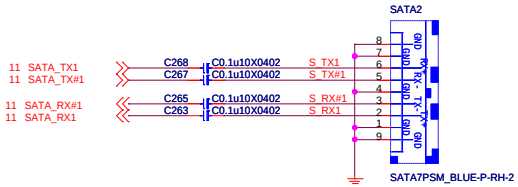
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: CRT	Rev: 0B
Date: Monday, December 29, 2008	Sheet 19 of 37	

LVDS PIN HEADER

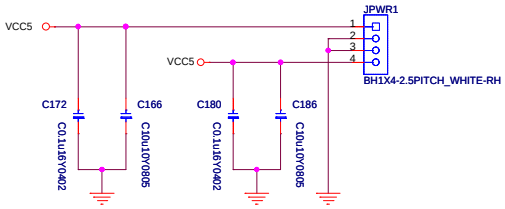


SERIAL ATA CONNECTOR BLOCK



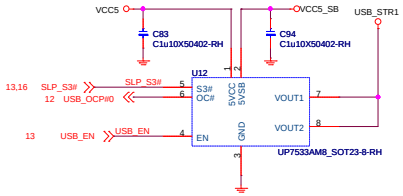


HDD Power For 2.5"

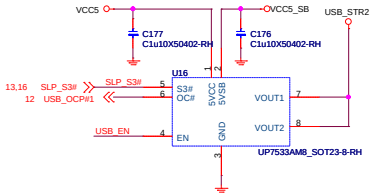


MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: SATA & CF Card	Rev: 0B
Date: Monday, December 29, 2008	Sheet 21 of 37	

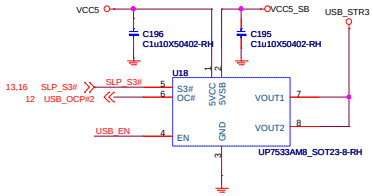
POWER CIRCUIT FOR USB PORT 0,1



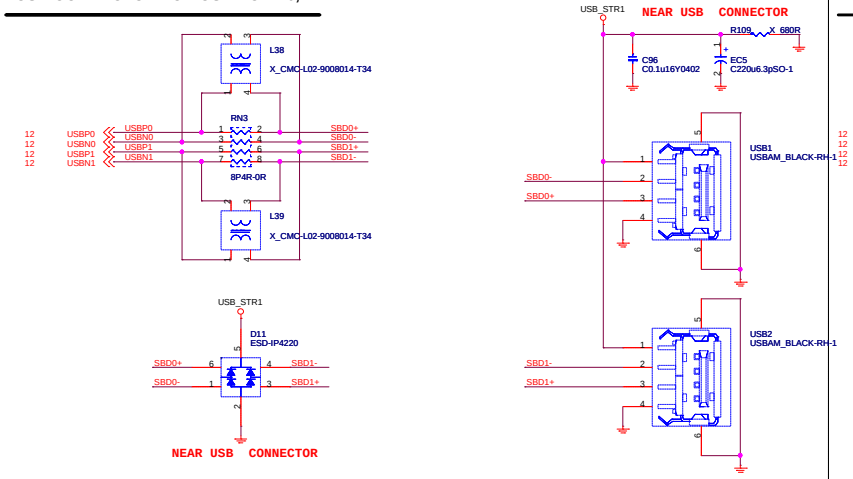
POWER CIRCUIT FOR USB PORT 2,3



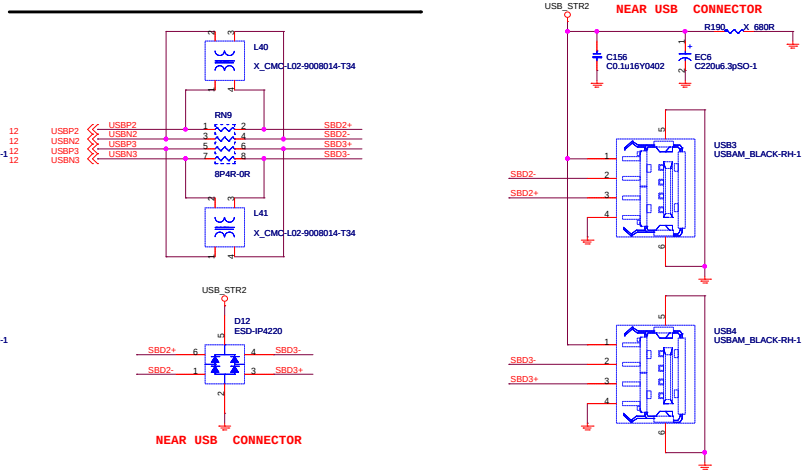
POWER CIRCUIT FOR USB PORT 4



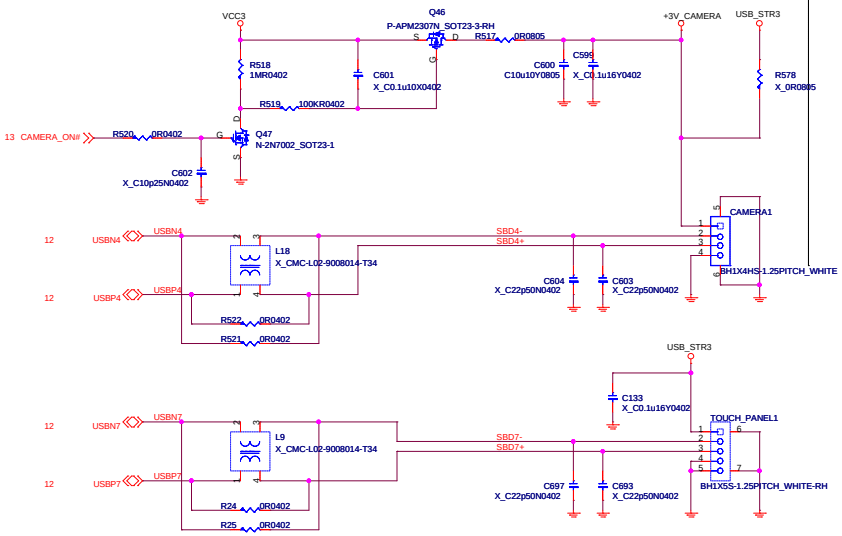
USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



CAMERA



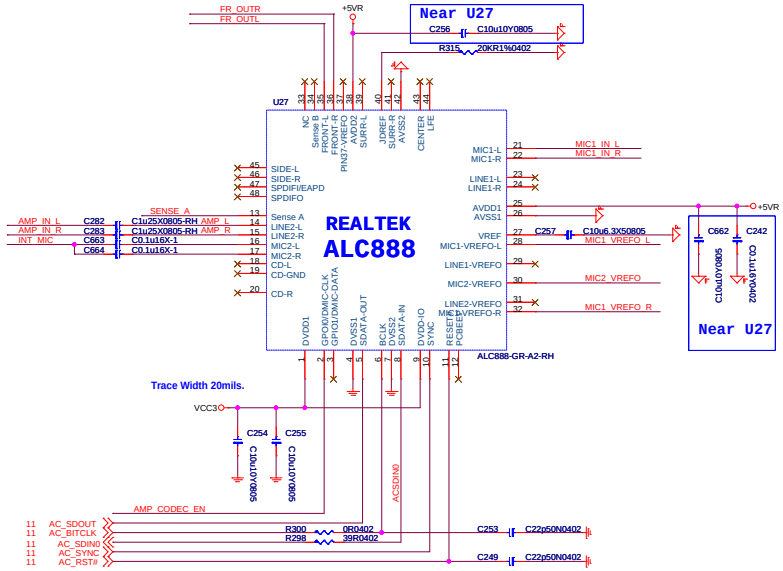
MICRO-STAR INT'L CO.,LTD

MS-7440

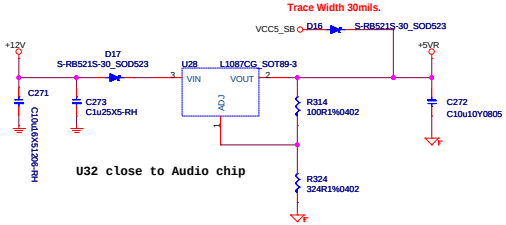
Size	Document Description	Rev
Custom	USB 0~4 CONNECTORS	0B

Date: Monday, December 29, 2008 Sheet 22 of 37

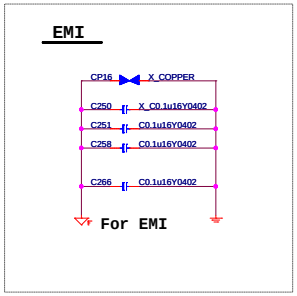
ALC888 CODEC



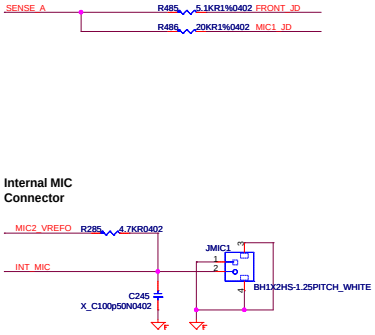
AUDIO CODE REGULATORS



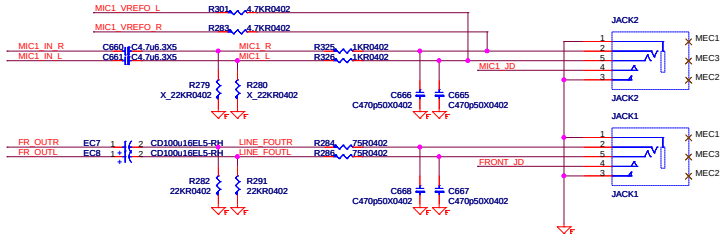
EMI

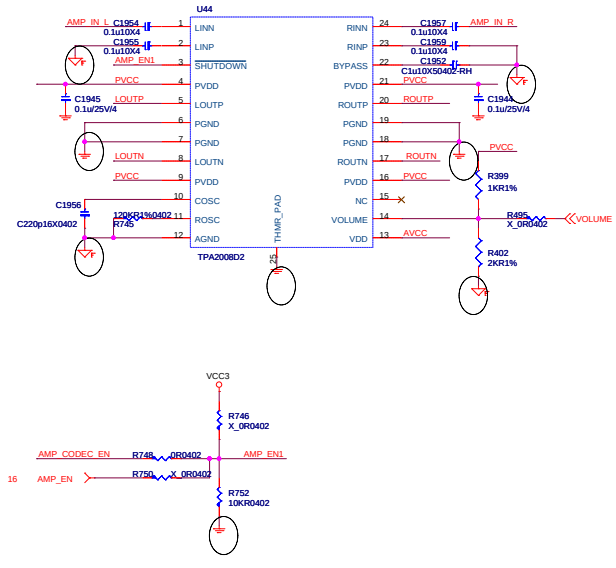


ALC888_JACK_DETECT



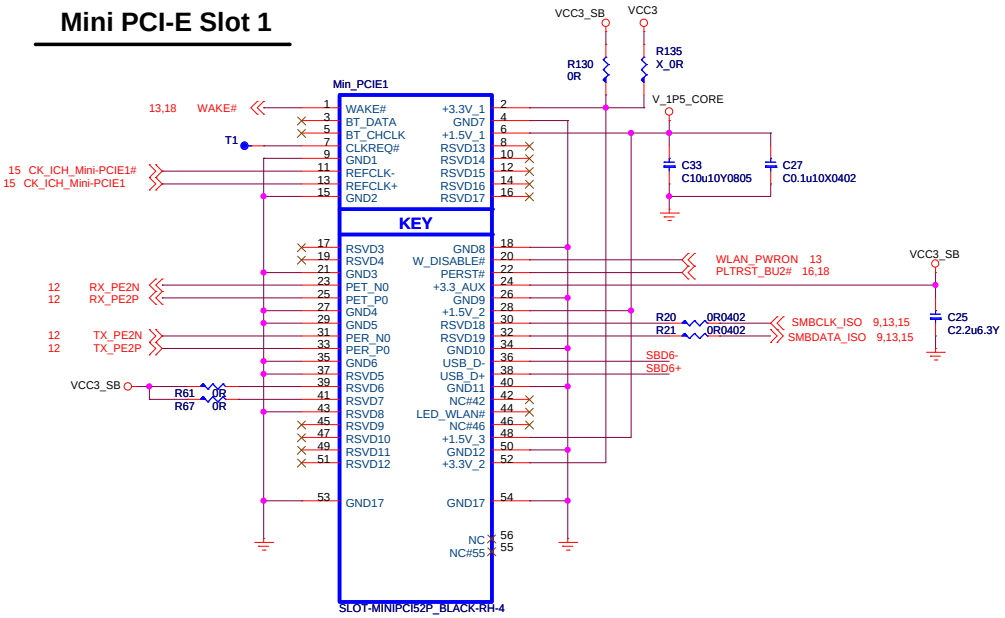
ALC888_JACK



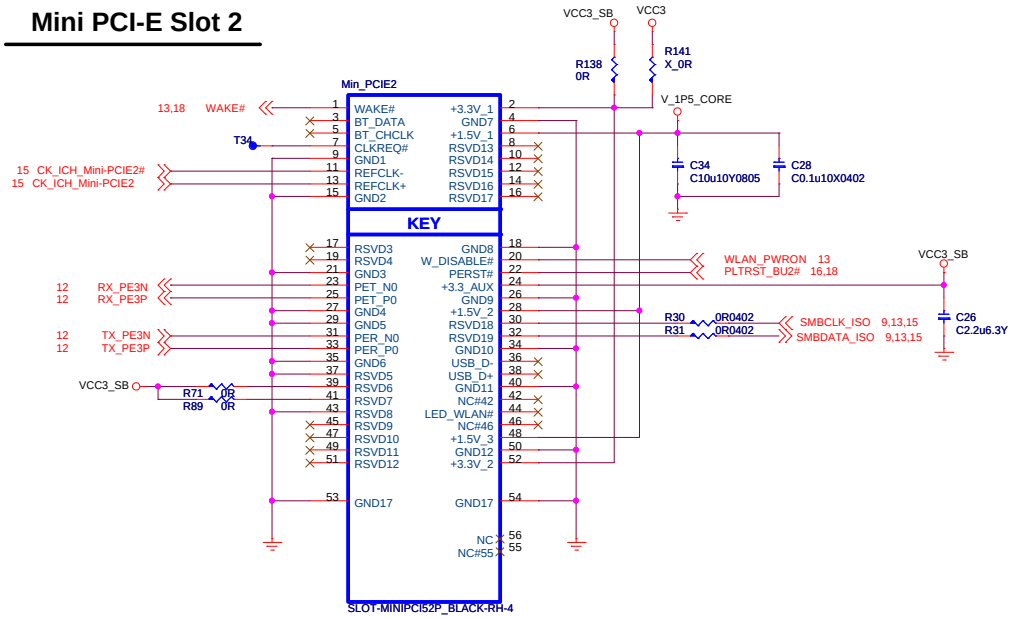


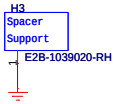
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7440	
Size: Custom	Document Description: Azalia - ALC888 & AMP	Rev: 0B
Date: Monday, December 29, 2008	Sheet 23 of 37	

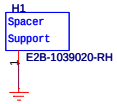
Mini PCI-E Slot 1

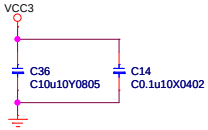


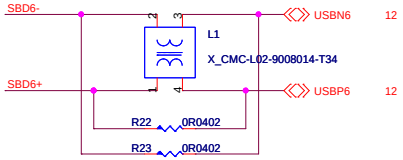
Mini PCI-E Slot 2

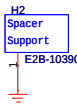


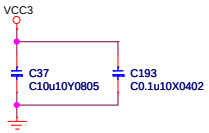






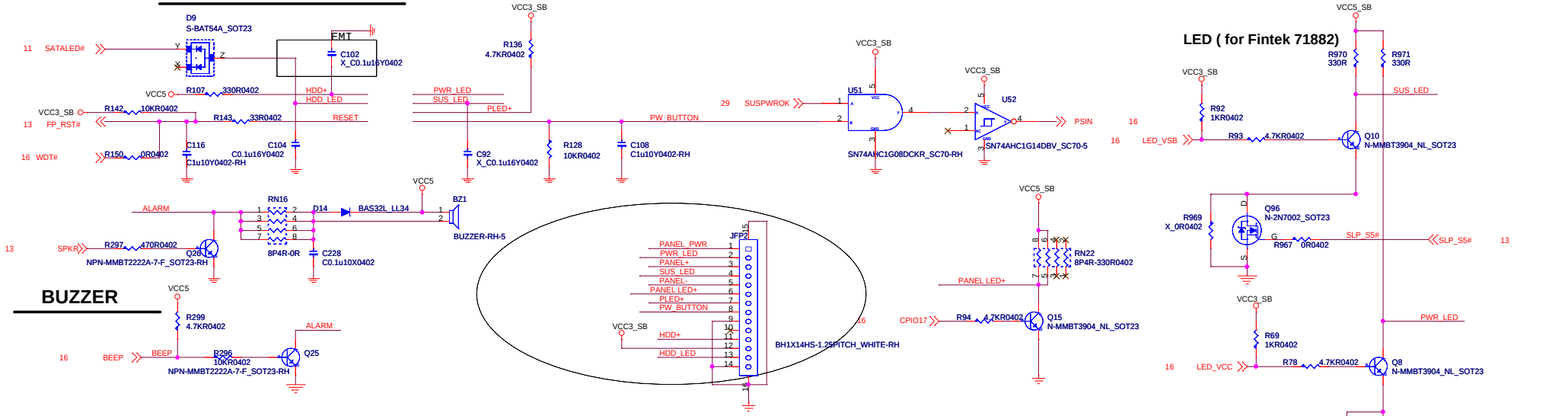




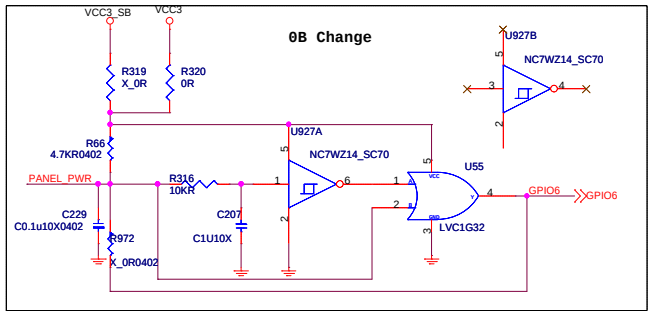


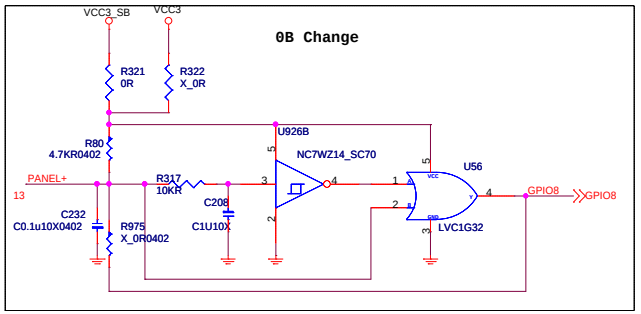
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: Mini PCI-E Slot	Rev: 0B
Date: Monday, December 29, 2008	Sheet 24 of 37	

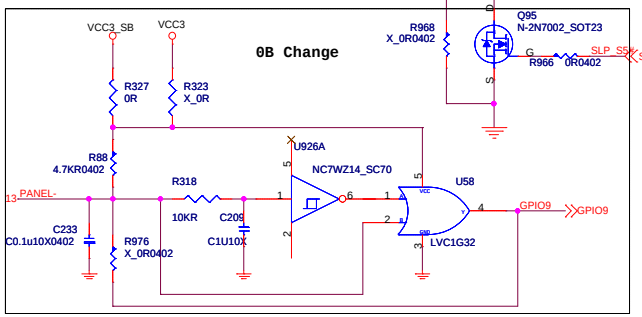
INTEL/PB Front Panel Connector



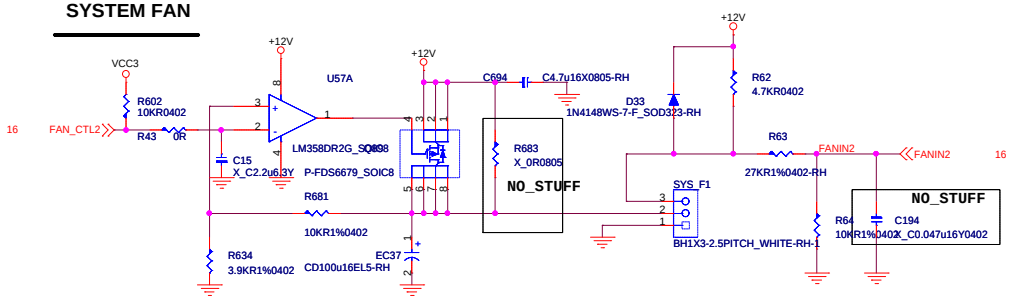
BUZZER

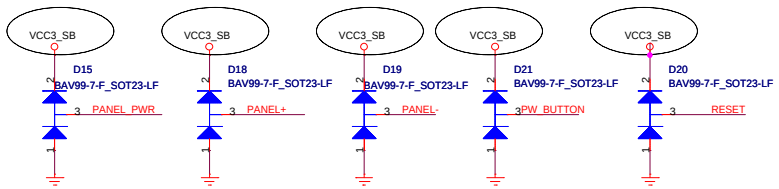


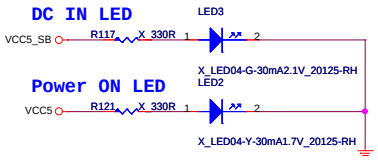


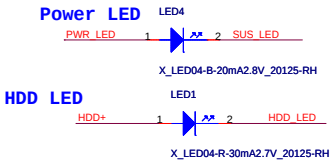


SYSTEM FAN







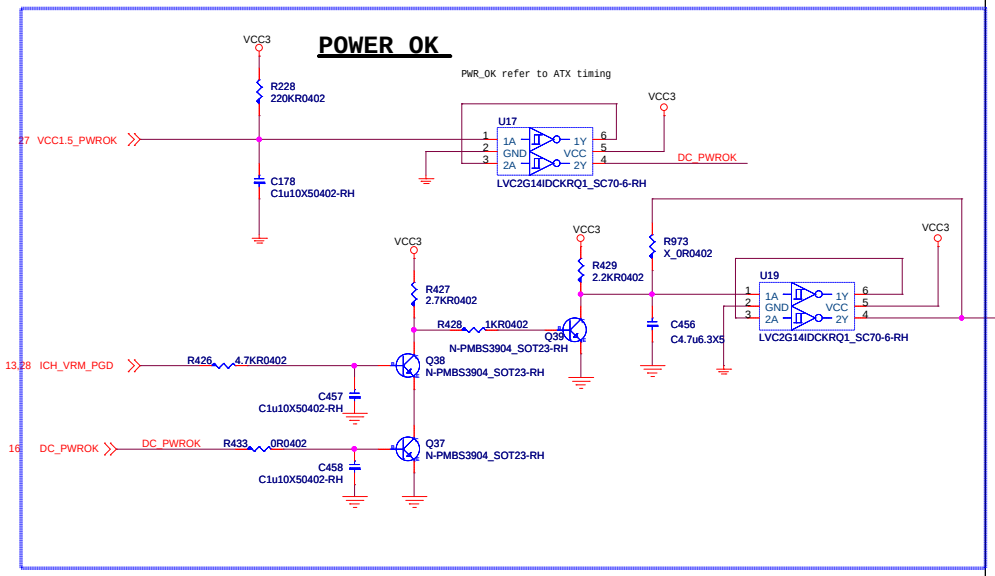


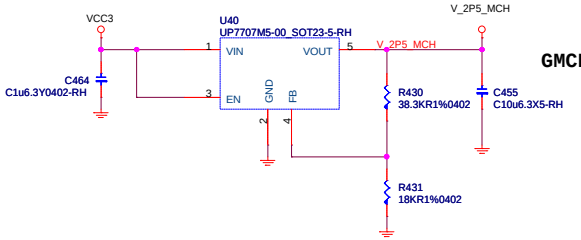
MICRO-STAR INT'L CO.,LTD

MS-7440

Size: Custom | Document Description: Front Panel&FAN Control | Rev: 0B

Date: Monday, December 29, 2008 | Sheet 25 of 37





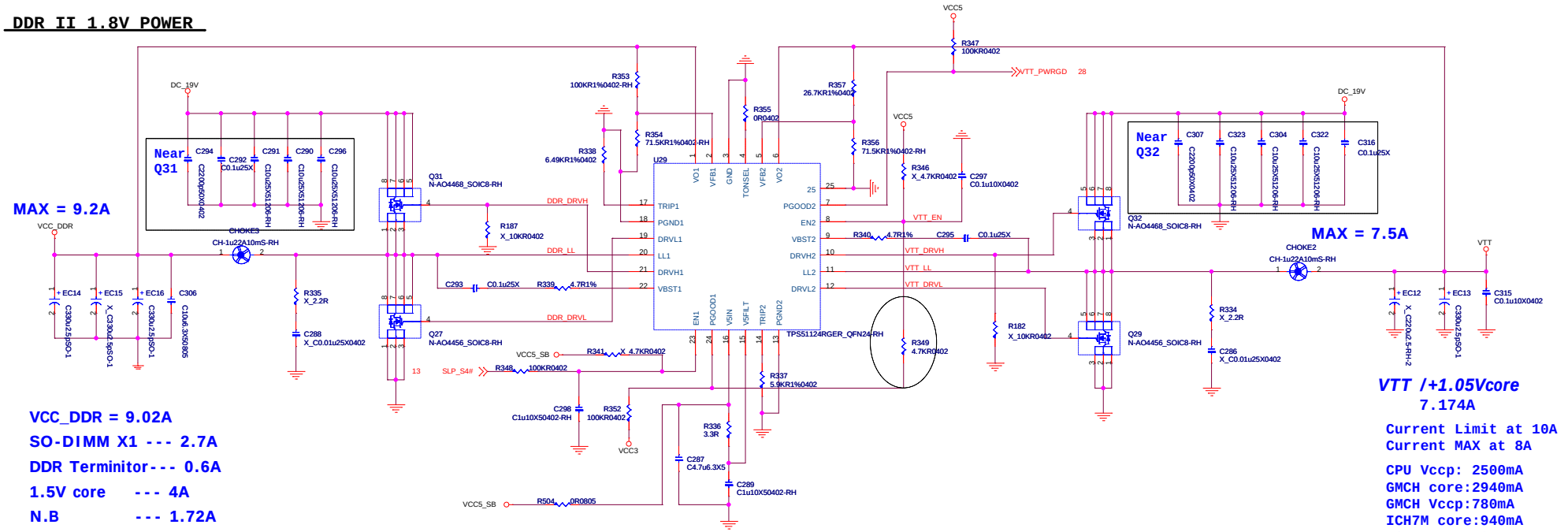
V_2P5_MCH 142mA

GMCH:70mA+2mA+10mA+60mA=142mA

UP7707 Spec 600mA

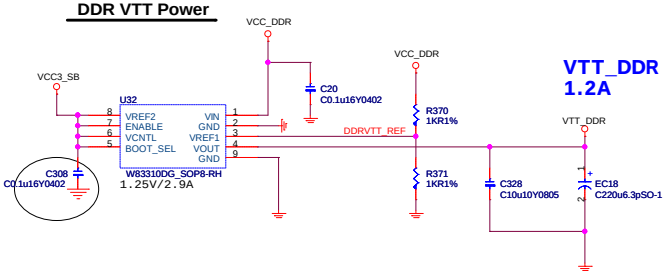
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: ACPI CONTROLLER	Rev: 0B
Date: Monday, December 29, 2008	Sheet 26 of 37	

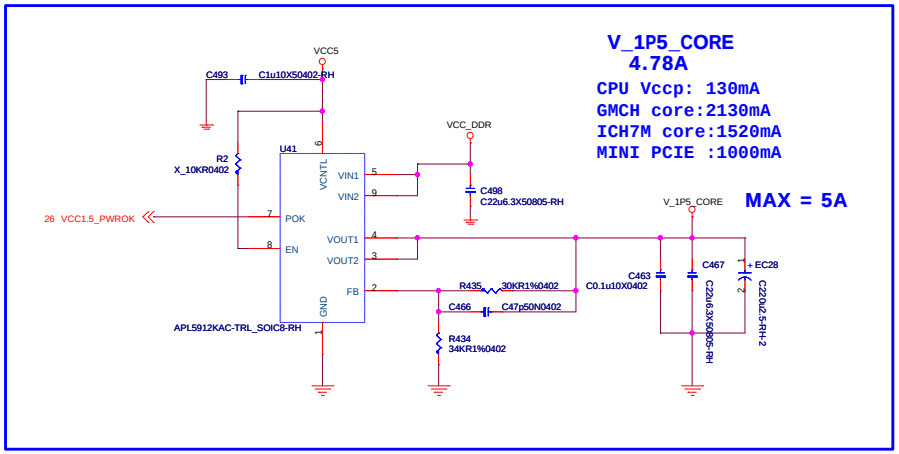
DDR II 1.8V POWER

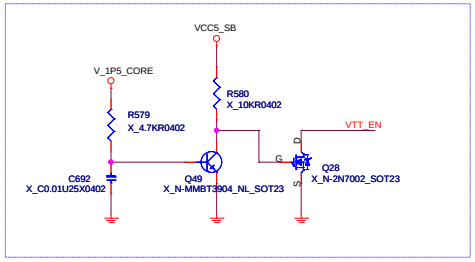


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .







MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: GMCH VCORE	Rev: 0B
Date: Monday, December 29, 2008	Sheet 27 of 37	

Modify from Intersil suggestion
0515'06

Throttling temp.
105 degree C

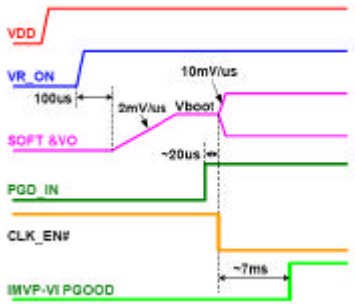
500 ohm?

Recommend 0.45uH

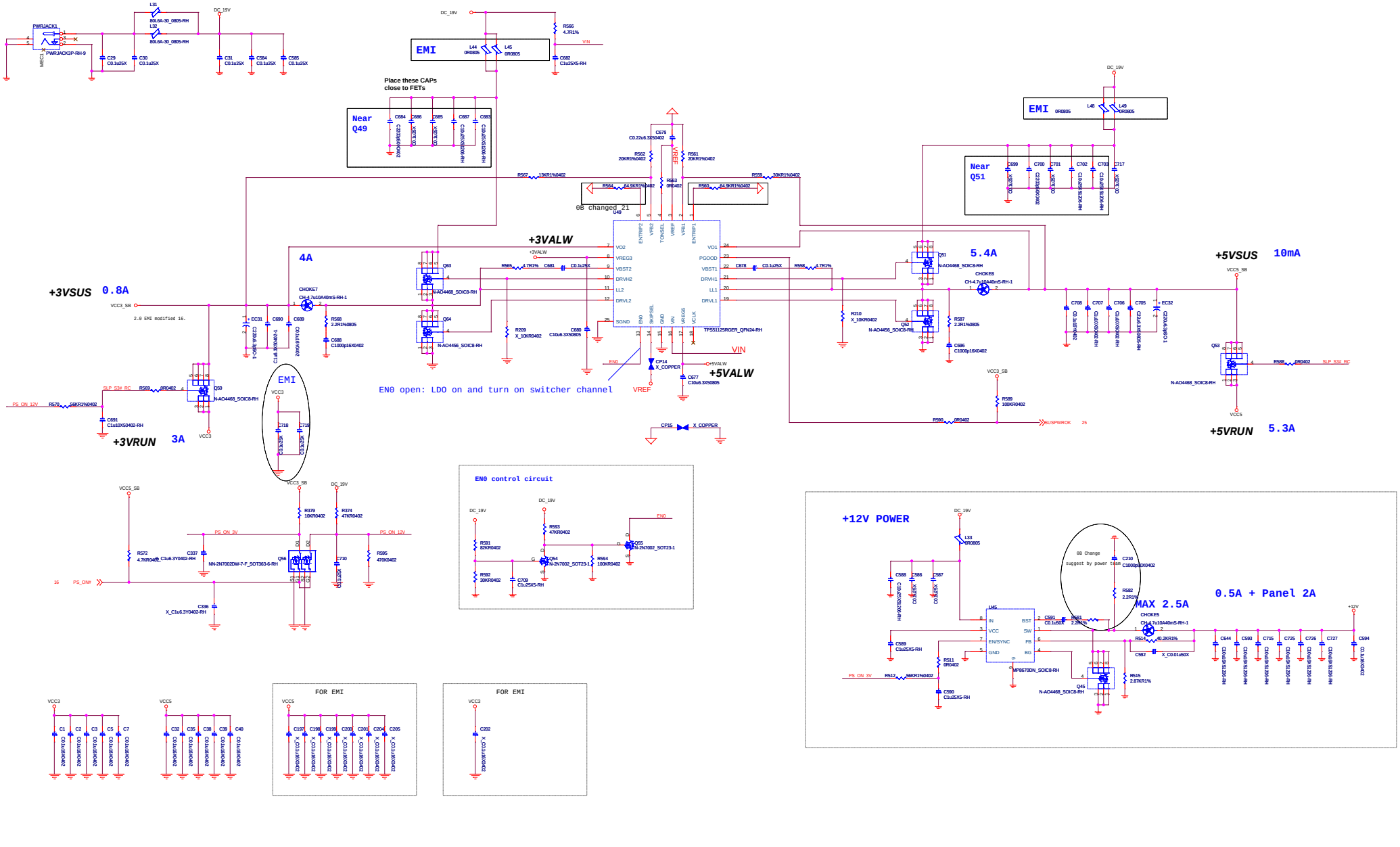
VCORE 4A

Parallel

modify 0610



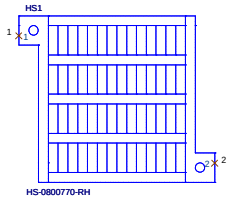
MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: CPU POWER	Rev: 0B
Date: Monday, December 29, 2008	Sheet 28 of 37	


+3VSUS 0.8A
+3VRUN 3A
+3VALW
4A
+5VALW
+5VSUS 10mA
+5VRUN 5.3A
5.4A
EMI
Near Q49
Near Q51
Place these CAPs close to FETs
08 changed 21
EN0 open: LDO on and turn on switcher channel
EN0 control circuit
+12V POWER
MAX 2.5A
0.5A + Panel 2A
FOR EMI
FOR EMI
TPS51125RGER_QFN24-RH
MP8670DN_SOIC8-RH
MICRO-STAR INT'L CO.,LTD
MS-7440
DC-IN POWER

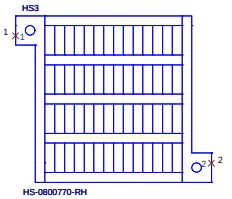
PCB1
PCB-7440-0B

BAT1_X1
BAT-BT-CR2032-RH

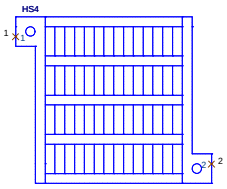
CPU HEATSINK



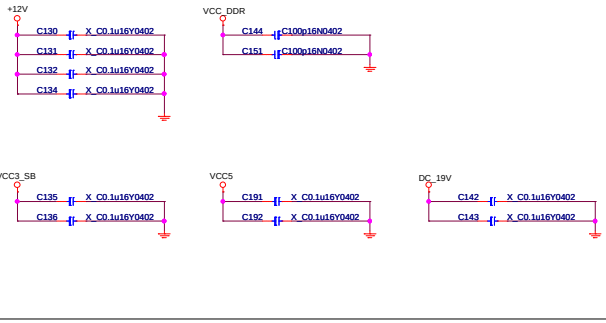
SB HEATSINK



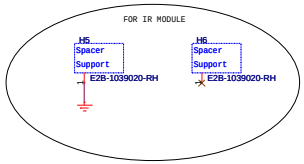
NB HEATSINK



EMI

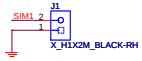


FOR IR MODULE

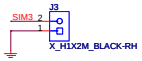


Simulation

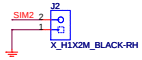
Layer1 / 5mil / 55ohm



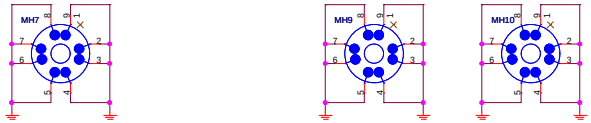
Layer6 / 5mil / 55ohm



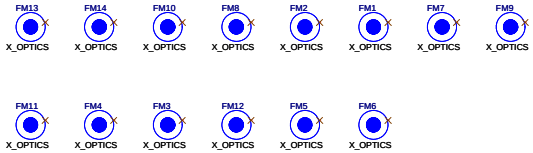
Layer4 / 4.5mil / 55ohm



Mounting Holes



Optics Orientation Holes



MICRO-STAR INT'L CO.,LTD

MS-7440

Size	Document Description	Rev
Custom	MANUAL PARTS	0B

Date: Monday, December 29, 2008 Sheet 30 of 37

ICH7M

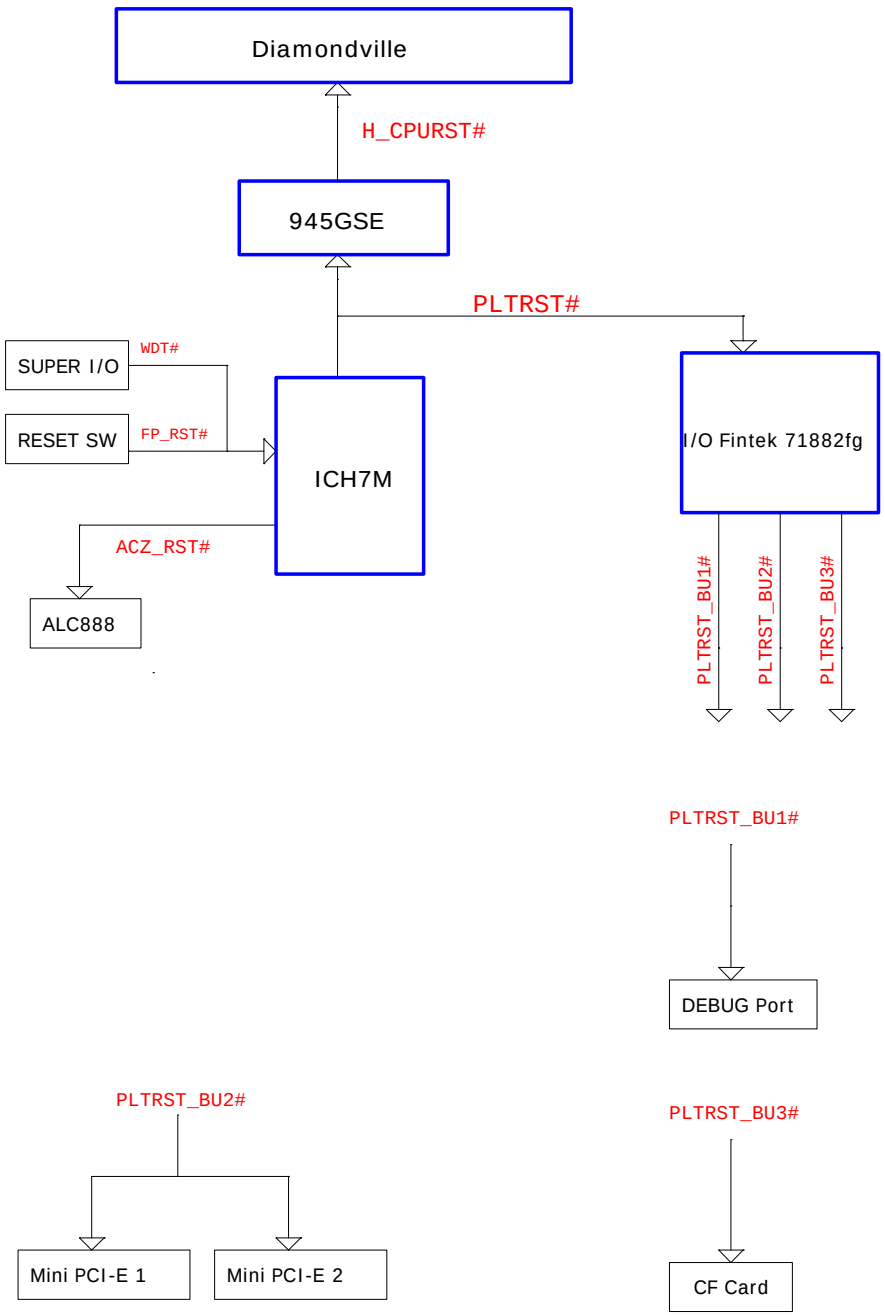
GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Rickles Signal Name
GPIO[0]	BM_BUSY#	AB18	I	VCC3p3	N	Y	3.3	N/A	PM_BMBUSY#
GPIO[1]	REQ[5]#	C8	I	V5REF	Y	N	5	N/A	PREQ#5
GPIO[2]	PIRQE#	G8	I	V5REF	Y	N	5	N/A	GPIO2
GPIO[3]	PIRQF#	F7	I	V5REF	Y	N	5	N/A	GPIO3
GPIO[4]	PIRQG#	F8	I	V5REF	Y	N	5	N/A	GPIO4
GPIO[5]	PIRQH#	G7	I	V5REF	Y	N	5	N/A	GPIO5
GPIO[6]	unmuxed	AC21	I	Vcc3p3	Y	Y	3.3	N/A	ATADET0
GPIO[7]	unmuxed	AC18	I	Vcc3p3	Y	N	3.3	N/A	SIO_OVT#
GPIO[8]	unmuxed	E21	I	VccSus3p3	Y	Y	3.3	N/A	NC
GPIO[9]	unmuxed	E20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[10]	unmuxed	A20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[11]	SMBALERT#	B23	I	VccSus3p3	Y	Y	3.3	N/A	SMBALERT#
GPIO[12]	unmuxed	F19	I	VccSus3p3	Y	N	3.3	N/A	SPI_HOLD_GPO#
GPIO[13]	unmuxed	E19	I	VccSus3p3	Y	Y	3.3	N/A	SIO_PME#
GPIO[14]	unmuxed	R4	I	VccSus3p3	Y	Y	3.3		NC
GPIO[15]	unmuxed	E22	I	VccSus3p3	N	N	3.3	1	NC
GPIO[16]	DPRSLPVR	AC22	O	Vcc3p3	N	N	3.3	1	DPRSLPVR
GPIO[17]	GNT[5]#	D8	O	Vcc3p3	N	N	3.3	1	PGNT#5
GPIO[18]	STPPCI#	AC20	O	Vcc3p3	N	N	3.3	1	PM_STPPCI#
GPIO[19]	SATA1GP	AH18	I	Vcc3p3	D	N	3.3	1	SATA1GP
GPIO[20]	STPCPU#	AF21	O	Vcc3p3	N	N	3.3	O	PM_STPCPU#
GPIO[21]	SATA0GP	AF19	I	Vcc3p3	N	N	3.3	0	SATA0GP
GPIO[22]	REQ4#	A13	I	Vcc3p3	N	N	3.3	0	PREQ#4
GPIO[23]	LDRQ1#	AA5	O	Vcc3p3	N	N	3.3		NC
GPIO[24]	unmuxed	B3	O	VccSus3p3	Y	N	3.3	1	BIOS_WP#
GPIO[25]	unmuxed	D20	O	VccSus3p3	N	N	3.3	N/A	CAMERA_ON#
GPIO[26]	unmuxed	A21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#5	C3	I	VccsUS3p3	Y	N	3.3		USB_OCP#2
GPIO[30]	OC#6	A2	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[31]	OC#7	B3	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[32]	CLKRUN#	AG18	O	Vcc3p3	N	N	3.3	1	CLKRUN#
GPIO[33]	AZ_DOCK_EN#	AC19	O	Vcc3p3	N	N	3.3	1	PRES2
GPIO[34]	AZ_DOCK_RST#	U2	O	Vcc3p3	N	N	3.3	0	PRES3
GPIO[35]	SATACLKREQ#	AD21	O	Vcc3p3	N	N	3.3	0	PRES1
GPIO[36]	SATA2GP	AH19	I	Vcc3p3	N	N	3.3	0	SATA2GP
GPIO[37]	SATA3GP	AE19	I	Vcc3p3	N	N	3.3	0	SATA3GP
GPIO[38]	unmuxed	AD20	I	Vcc3p3	Y	N	3.3	1	NC
GPIO[39]	unmuxed	AE20	I	Vcc3p3	Y	N	3.3	1	WLAN_PWRON
GPIO[48]	GNT4#	A14	O	Vcc3p3	N	N	3.3	1	PGNT#4
GPIO[49]	CPUPWRGD	AG24	OD	V_FSB_VTT	Y	N	3.3	1	CPU_PWRGD

SIO(F71882)

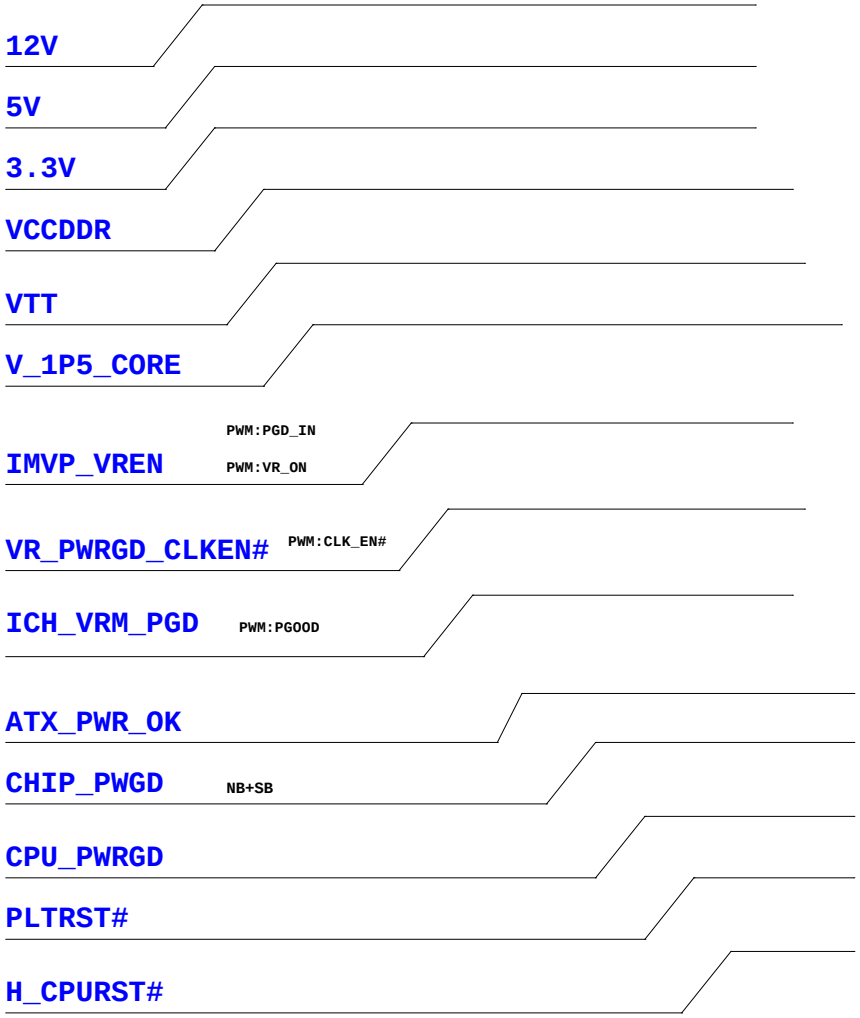
PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	UNUSED		
GPIO3	UNUSED		
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	UNUSED		
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	AMP_EN	OUTPUT	RESERVED TO ENABLE THE AMPLIFIER
GPIO15	LED_VSB	OUTPUT	OUTPUT FOR PWR LED
GPIO16	LED_VCC	OUTPUT	OUTPUT FOR PWR LED
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESET BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESET BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESET BUFFER3
GPIO23	UNUSED		
GPIO24	UNUSED		
GPIO26	PSIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PSOUT#	OUTPUT	POWER BUTTON BUFFER OUT TO SB
GPIO30	SLP_S3#	INPUT	FROME SOUTHBRIDGE S3#
GPIO31	PS_ON#	OUTPUT	OUTPUT FOR POWER ON
GPIO32	UNUSED		
GPIO33	RSMRST#	OUTPUT	OUTPUT FOR SOUTRHBRIDGE RSMRST#
GPIO40	AMP_GAIN0	OUTPUT	SET AMPLIFIER GAIN
GPIO41	UNUSED		
GPIO42	UNUSED		
GPIO43	AMP_GAIN1	OUTPUT	SET AMPLIFIER GAIN

DDR-II DIMM Config.

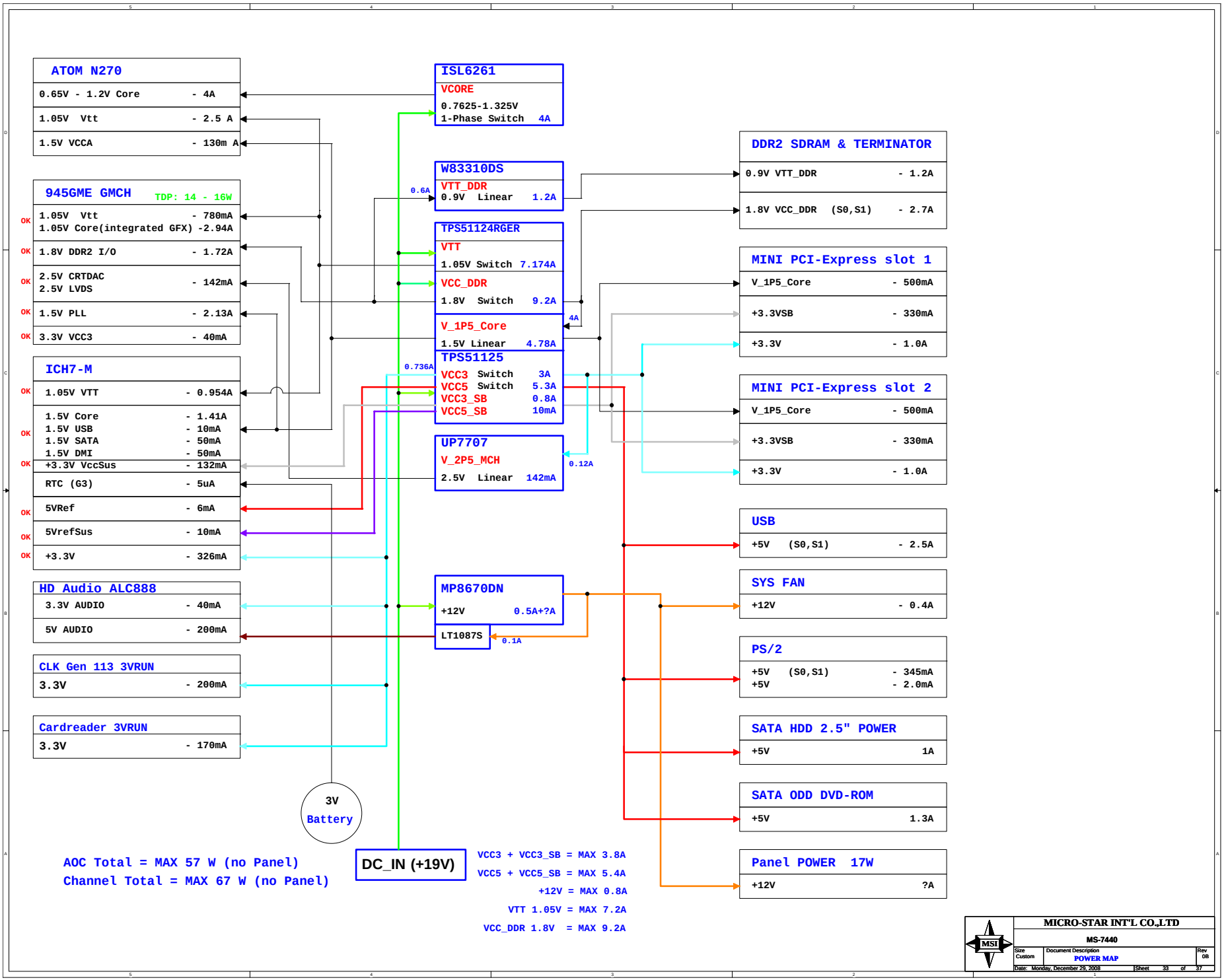
DEVICE	ADDRESS	CLOCK	
DIMM 1	00	SM_CK0/#0	SM_CK1/#1



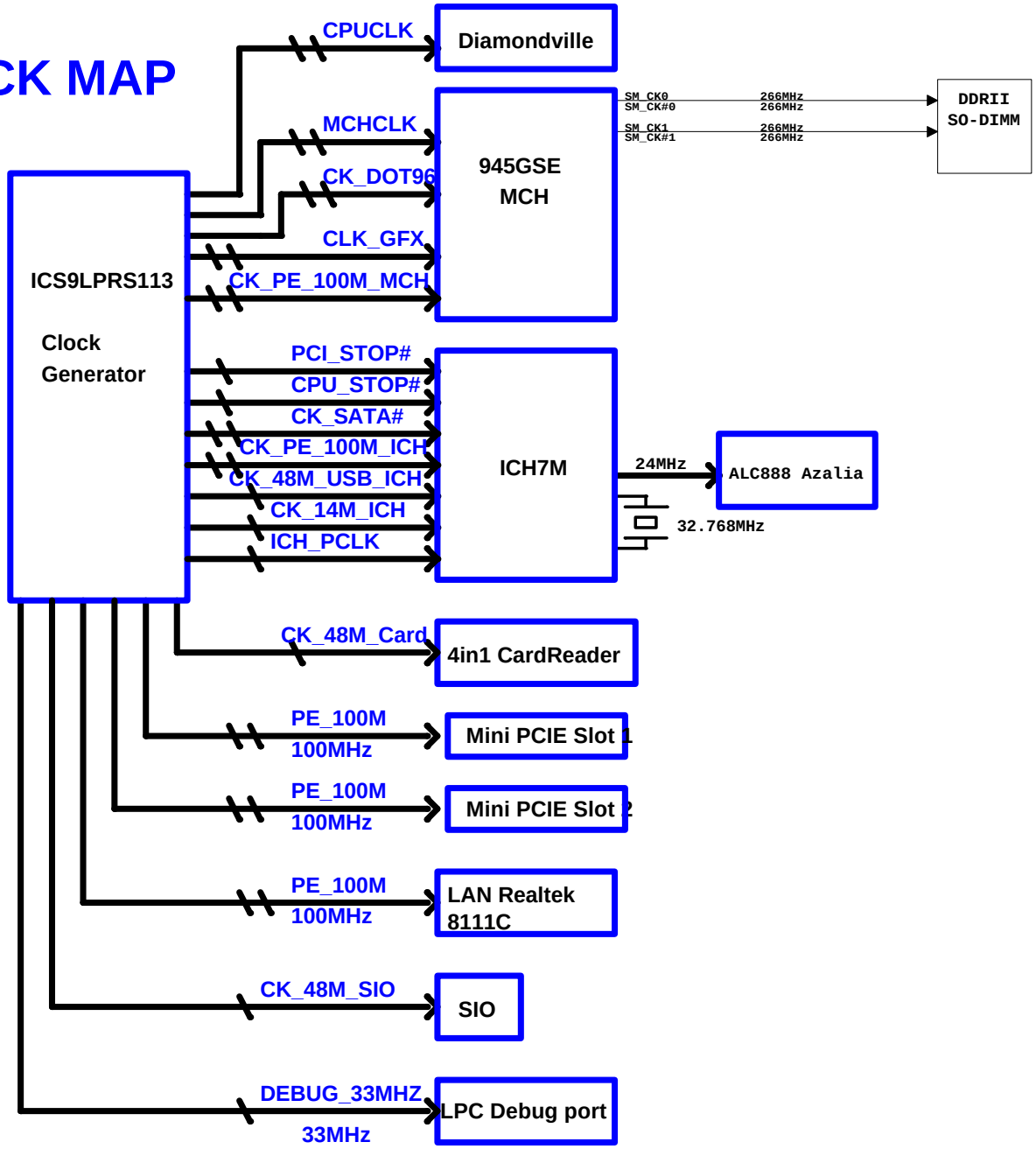
Power Sequence



MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: Power sequence & RST	Rev: 0B
Date: Monday, December 29, 2008	Sheet 32 of 37	


ATOM N270
0.65V - 1.2V Core - 4A
1.05V Vtt - 2.5 A
1.5V VCCA - 130m A
945GME GMCH TDP: 14 - 16W
OK 1.05V Vtt - 780mA
1.05V Core(integrated GFX) -2.94A
OK 1.8V DDR2 I/O - 1.72A
OK 2.5V CRTDAC - 142mA
2.5V LVDS
OK 1.5V PLL - 2.13A
OK 3.3V VCC3 - 40mA
ICH7-M
OK 1.05V VTT - 0.954A
1.5V Core - 1.41A
OK 1.5V USB - 10mA
1.5V SATA - 50mA
1.5V DMI - 50mA
OK +3.3V VccSus - 132mA
RTC (G3) - 5uA
OK 5VRef - 6mA
OK 5VrefSus - 10mA
OK +3.3V - 326mA
HD Audio ALC888
3.3V AUDIO - 40mA
5V AUDIO - 200mA
CLK Gen 113 3VRUN
3.3V - 200mA
Cardreader 3VRUN
3.3V - 170mA
3V Battery
ISL6261
VCORE
0.7625-1.325V
1-Phase Switch 4A
W83310DS
VTT_DDR
0.6A
0.9V Linear 1.2A
TPS51124RGER
VTT
1.05V Switch 7.174A
VCC_DDR
1.8V Switch 9.2A
V_1P5_Core
4A
1.5V Linear 4.78A
TPS51125
0.736A
VCC3 Switch 3A
VCC5 Switch 5.3A
VCC3_SB 0.8A
VCC5_SB 10mA
UP7707
V_2P5_MCH
0.12A
2.5V Linear 142mA
MP8670DN
+12V 0.5A+?A
LT1087S
0.1A
DC_IN (+19V)
DDR2 SDRAM & TERMINATOR
0.9V VTT_DDR - 1.2A
1.8V VCC_DDR (S0,S1) - 2.7A
MINI PCI-Express slot 1
V_1P5_Core - 500mA
+3.3VSB - 330mA
+3.3V - 1.0A
MINI PCI-Express slot 2
V_1P5_Core - 500mA
+3.3VSB - 330mA
+3.3V - 1.0A
USB
+5V (S0,S1) - 2.5A
SYS FAN
+12V - 0.4A
PS/2
+5V (S0,S1) - 345mA
+5V - 2.0mA
SATA HDD 2.5" POWER
+5V 1A
SATA ODD DVD-ROM
+5V 1.3A
Panel POWER 17W
+12V ?A
AOC Total = MAX 57 W (no Panel)
Channel Total = MAX 67 W (no Panel)
VCC3 + VCC3_SB = MAX 3.8A
VCC5 + VCC5_SB = MAX 5.4A
+12V = MAX 0.8A
VTT 1.05V = MAX 7.2A
VCC_DDR 1.8V = MAX 9.2A
MICRO-STAR INT'L CO.,LTD
MS-7440
Size Custom
Document Description POWER MAP
Rev 0B
Date: Monday, December 29, 2008
Sheet 33 of 37

CLOCK MAP



MICRO-STAR INT'L CO.,LTD		
MS-7440		
Size: Custom	Document Description: CLK MAP	Rev: 0B
Date: Monday, December 29, 2008	Sheet 34 of 37	

MS-7440 0A Change List

1	Remove mini pci-e 2	
2	Remove CF Care	
3	Change System Fan	
4	LED1,LED2,LED3,LED4 NO STUFF	
5	Remove 7308 function (NO STUFF)	
6	Add Touch Panel Connector (USB)	P.22
7	Change JVGA1 and SO-DIMM Footprint	P.19 P.9
8	Change Min_PCIE1 and Min_PCIE1 and H1 and H2 Footprint	P.24
9	LCTLA_CLK and LCTLB_DATA pull-up to3.3 V (LVDS)	P.06
10	LIBG pulled-down to GND (LVDS)	P.06
11	PS_ON# Pull-up VCC5_SB	P.25
12	PSOUT# and ATXPG_IN Pull-up VCC3_SB	P.13 P.16
13	C90 Change to C11-2257013-W08 (X5R)	P.28
14	L1/L9/RN33 SWAP (layout require)	P.24 P.18
15	PWR_LED and SUS_LED Add control singal SLP_S5#	P.25 09/23
16	RN16 change to 220 ohm	P.25 09/23
17	add test point (T25,T26,T35,T38~T316)	09/23
18	7308 NO STUFF	P.20 09/24
19	RN30/RN27/RN19/RN18/RN32 SWAP (layout require)	P.20 09/24
20	Remove Q49 And Change to Q63,Q64 For VCC3_SB	P.29 09/24
21	Remove Q35 And Change to Q97,Q98 For VCORE	P.28 09/24
22	RN31/RN26/RN8 SWAP (layout require)	09/25
23	Keyboard/mouse power change to VCC5_SB	P.16 09/25
24	C236,C565,C237,C234,C574,C553,C554,C582,C583,C567,C576,C575, C563,C559,C556,C577,C581 changr rating to 25V and add CP19	P.23 09/25
25	Remove RN1 and add R970/R971	P.25 09/25
26	Add buffer circuit for GPIO6/GPIO8/GPIO9	P.25 09/25
27	Remove R346 and U29 PIN 8 through 4.7K connect to U29 PIN 24, Delay Time (Let VTT slower than VCC_DDR)	P.27 09/25
28	SB heatsink change to E31-0800771-K08	P.30 09/26
29	JFP2 change to N31-2071101-H06 (add HDD_LED)	P.25 09/26
30	Add stand off H5/H6 (IR module)	P.30 09/26

31	L_BKLTEN connect to GPIO10 (R682 NO STUFF)	09/30
32	Camara change to IR module (camara power no stuff)	09/30
33	Add Cap C197~C205 and add CP20~CP23and remove C133/C264 for EMI (unstuff)	10/03
34	Add VTT_EN singal circuit (reserved for power sequence error)	P.27 10/03
35	Remove MH1,MH2,MH3,H3,H4,FM15,FM16 (layout require)	P.30 10/06
36	L1/L9 SWAP (layout require)	10/06
37	P4.C408,C403,C410,C411,C409 P10.C47,C54,C55,C56,C103,C126,C127,C128 P18.C611,C612,C613,C641 P27.EC15,EC12 P28.EC24 (change to unstuff)	10/07
38	Add R182,R187,R209,R210,R208 (unstuff) Add R208	10/07
39	JFP2 7pin connect to PLED+ , JFP2 12pin connect to VCC3_SB	10/07
40	R296 change to 10 kohm (for BZ1 no voice)	P25 10/07
41	C492,C488,C486,C485,C491,C495,C487,C489,C19,C21,C117,C118,C119,C120,C153,C154 change to X7R	10/07
42	remove test point (T25,T26,T35,T38~T316)	10/08
43		
44		
45		

MICRO-STAR INT'L CO.,LTD

MS-7440

Size	Document Description	Rev
Custom	Revision History	0B

Date: Monday, December 29, 2008 Sheet 35 of 37

MS-7440 0B Change List

1	Change GPIO6 GPIO8 GPIO9 Circuit for buttom turn low with SMI signal keep low	P.25 12/05
2	Add brightness DC Control Circuit (Unstuff)	P.25 12/05
3	RN16 change to 0 ohm for BZ1 no sound	P.25 12/05
4	Add Q66 (supply 3V power for LCD panel)	P.20 12/05
5	R532 connect to C724 (for LAN ative LED)	P.18 12/05
6	R608 and C720 Exchange Place	P.18 12/05
7	C282 and C283 Change to 1uF for Prevent Internal Amp Output 爆破聲	P.23 12/05
8	RN5 Change to 0 ohm for CPU Clock Fail by SA Signal Measure	P.15 12/05
9	R677 Unstuff and R682 Mounting for Penal on/off Control From GPIO23	P.20 12/05
10	Add R160 and C206 for AC_SDIN0 RC Delate (SA fail)	P.11 12/05
11	R287 Change to 25.5 ohm (SA USB signal fail)	P.12 12/05
12	Add C210,R581,R582 for 12V (suggest by STEVEN)	P.29 12/05
	power team suggestion	
	The tests If DC Power & Transient are finished and please see below the modified values.	
	Vcore	
13	R73: 976 ohm 1% (Droop)	P.28 12/05
	Q98: D03-0445603-A68 (L_Side MOS)	
	VTT	
14	Q29: D03-0445603-A68 (L_Side MOS)	P.27 12/05
	R337: 5.9k ohm 1% (OCP: 12A)	
	R357: 26.7k ohm 1% (Offset)	
	EC13: 330uF 2.5V	
	VCC_DDR	
15	Q27: D03-0445603-A68 (L_Side MOS)	P.27 12/05
	R338: 6.49k ohm 1% (OCP: 13.3A)	
	VCC5_SB	
16	Q52: D03-0445603-A68 (L_Side MOS)	P.29 12/05
	C705: 22uF X5R (Vout)	
	R560: 64.9k ohm 1% (OCP: 11A)	

	VCC3_SB	
17	Q64: D03-0445603-A68 (L_Side MOS)	P.29 12/05
	R564: 64.9k ohm (OCP: 9A)	
18	Change AMP Circuit	P.23 12/05
19	Remove USB Function Of Min_PCIE2 Slot (for touch panel)	P.22 12/05
20	Change GPIO6 GPIO8 GPIO9 Circuit for buttom turn low with SMI signal keep low	P.25 12/08
21	L_BKLTEN Control Change to GPIO23 from GPIO10 (for close LVDS signal)	P.20 12/09
22	L_BKLTEN and LVDS_VDDEN control from GPIO23	P.20 12/11
23	RT1and R151 Unstuff and Q65 Mounting (for system thermal sensor)	P.16 12/15
24	Change PCI ExpressR Mini Card Electromechanical Specification Revision 1.2	P.24 12/16
25	Change part number of SATA2 connector to N5N-07M0750-H06	P.21 12/16
26	CHIP_PWGD add Schmitt Trigger for power sequence	P.26 12/16
27	+3V_CR power add C212 for sometime OS can't detect card deader device	P.17 12/24
28	JINV1/JFP2/JPWR1/SYS_F1 change part number for ME request	12/24
29	Add stand off H3 and H4 for MINI PCI-E half card	P.24 12/24
30	Remove JFP1 and R125	P.25 12/26
31	Change CAMERA1 part number(4pin)	P.22 12/26

MICRO-STAR INT'L CO.,LTD

MS-7440

Size C | Document Description: Revision History | Rev 0B

Date: Monday, December 29, 2008 | Sheet 36 of 37

Table 5: Differential Impedance Targets for Recommended Routing

Signal Type	Routing Geometry	Impedance
PCI-E Gen4	4 mil trace / 6 mil space / 7 mil pitch	85Ω ± 10%
DMI	4 mil trace / 6 mil space / 7 mil pitch	85Ω ± 10%
SATA	4 mil trace / 6 mil space / 7 mil pitch	85Ω ± 10%
USB	4 mil trace / 6 mil space / 7 mil pitch	90Ω ± 10%
USB (Option # 1)	4 mil trace / 6 mil space / 7 mil pitch	85Ω ± 10%
USB (Option # 2)	4 mil trace / 6 mil space / 7 mil pitch	100Ω ± 10%
LAN	4 mil trace / 6 mil space / 7 mil pitch	100Ω ± 10%
CLK	4 mil trace / 6 mil space / 7 mil pitch	100Ω ± 10%
Serial Port	4 mil trace / 6 mil space / 7 mil pitch	100Ω ± 10%
Parallel Port	4 mil trace / 6 mil space / 7 mil pitch	100Ω ± 10%

Note: It is recommended to apply 4 mil / 7 mil trace spacing to the critical signals to minimize EMI. It is also recommended to apply equivalent length routing rule when it does not affect the routing topology.

Table 6: Differential Impedance Targets for Graphics Routing (Sheet 1 of 2)

Signal Type	Routing Geometry	Impedance
Main Link	4 mil trace / 7 mil space	100 Ω ±10%
DMI	4 mil trace / 7 mil space	100 Ω ±10%
SDVO	4 mil trace / 7 mil space	100 Ω ±10%
LVDS	4 mil trace / 7 mil space	100 Ω ±10%
LVDS (Option # 1)	5 mil trace / 7 mil space	90Ω ±10%
LVDS (Option # 2)	5 mil trace / 7 mil space	85Ω ±10%
LVDS (Option # 3)	5 mil trace / 7 mil space	100 Ω ±10%

Table 6: Differential/Capacitance Targets for Graphics Routing (Sheet 1 of 2)

Signal Type	Routing Geometry	Impedance
USB	4 mil trace / 7 mil space	90Ω ± 10%
PCI-E Gen3	4 mil trace / 7 mil spacing	85Ω ± 10%
USB (Option)	5 mil trace / 7 mil space	90Ω ± 10%
USB (Option)	4 mil trace / 7 mil spacing	85Ω ± 10%

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MS-7440

Document Description

Layout Rule

Rev: 0

File: ms

Date: Monday, December 31, 2012 Sheet 37 of 37