MS-7437 (MS-6632)

Version 0A

CPU:

Intel Dimondville

System Chipset:

Intel 945GSE (North Bridge)
Intel ICH7M(South Bridge)

On Board Chipset:

Clock Generator - ICS9LPRS113
HD AUDIO CODEC(ALC888)
Giga LAN -- Realtek RTL8111C
LVDS CHRONTEL - CH7308B
SIO-Fintek F71882F
Card Reader RTS5158E
AMP - TPA3005D2
BIOS -- SPI

Main Memory:

DDR II SO-DIMM x 1 (Max 1GB)

Expansion Slots:

Internal Mini PCIE x1
Internal Mini PCIE x2 (Option)
CF Card Connector

Intersil PWM:

Controller: ISL6261CRZ-T

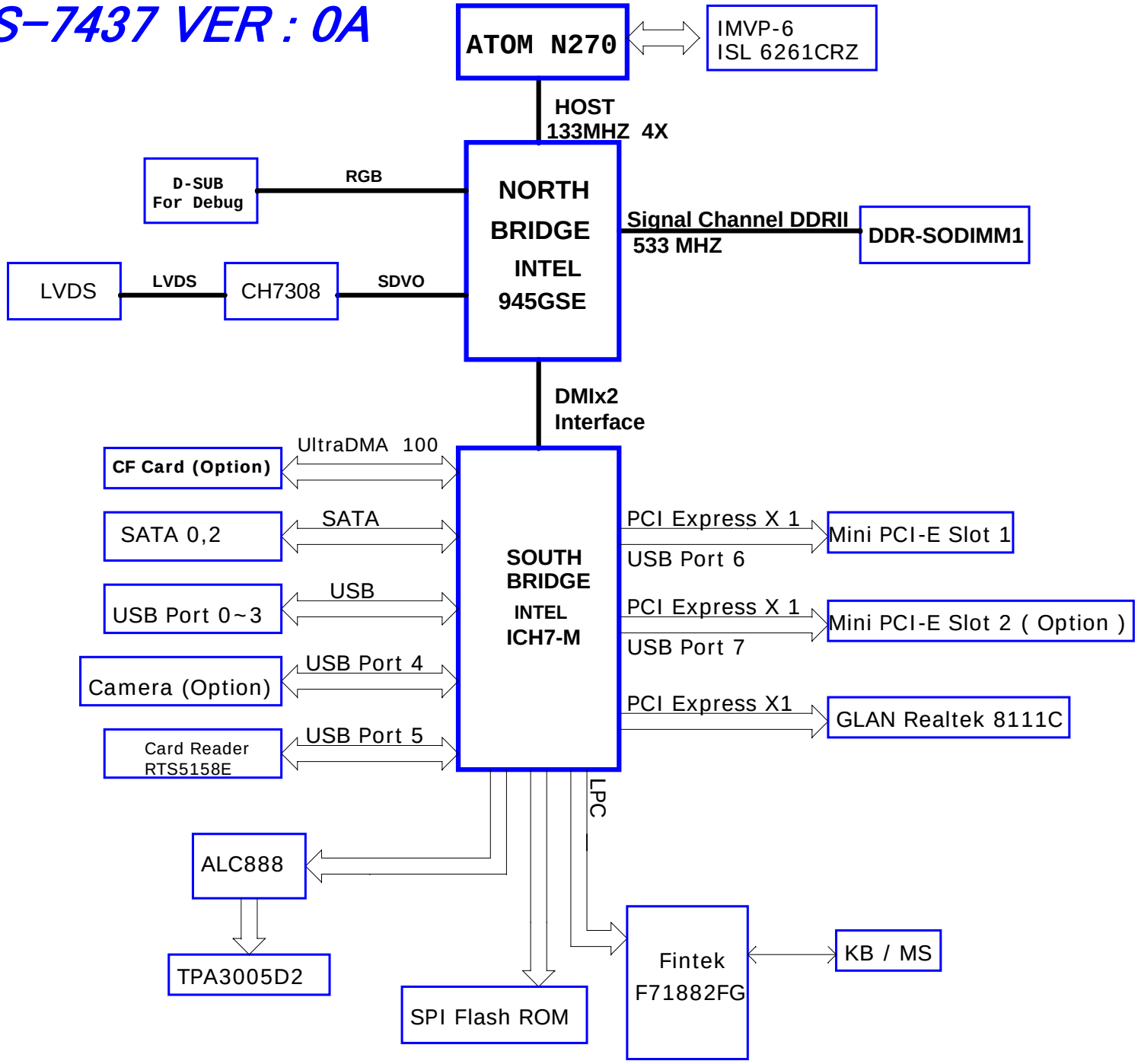
MICRO-STAR INT'L CO.,LTD

MS-7437

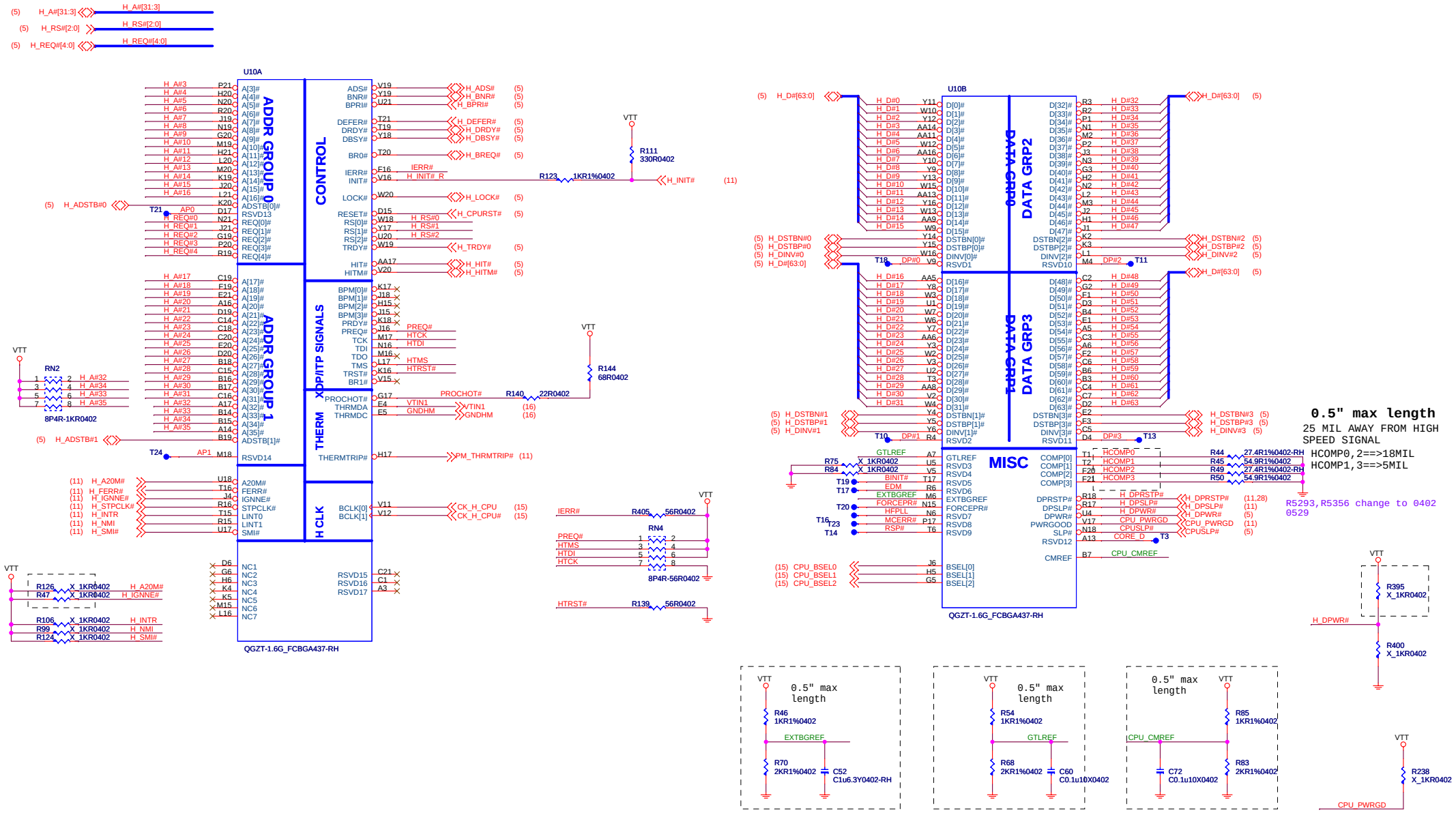
Size: Custom | Document Description: COVER SHEET | Rev: 0A

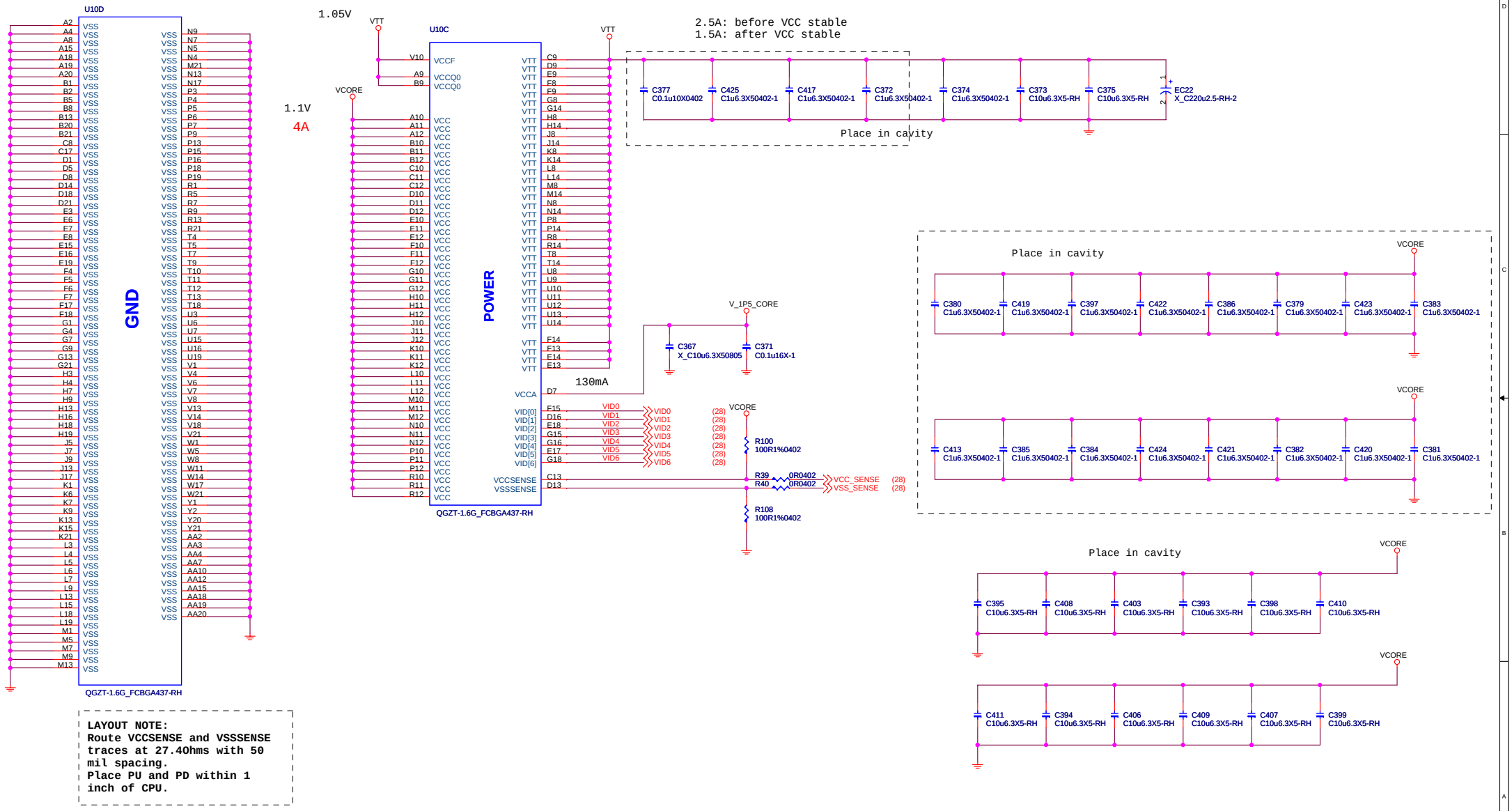
Date: Friday, September 05, 2008 | Sheet 1 of 35

MS-7437 VER : 0A



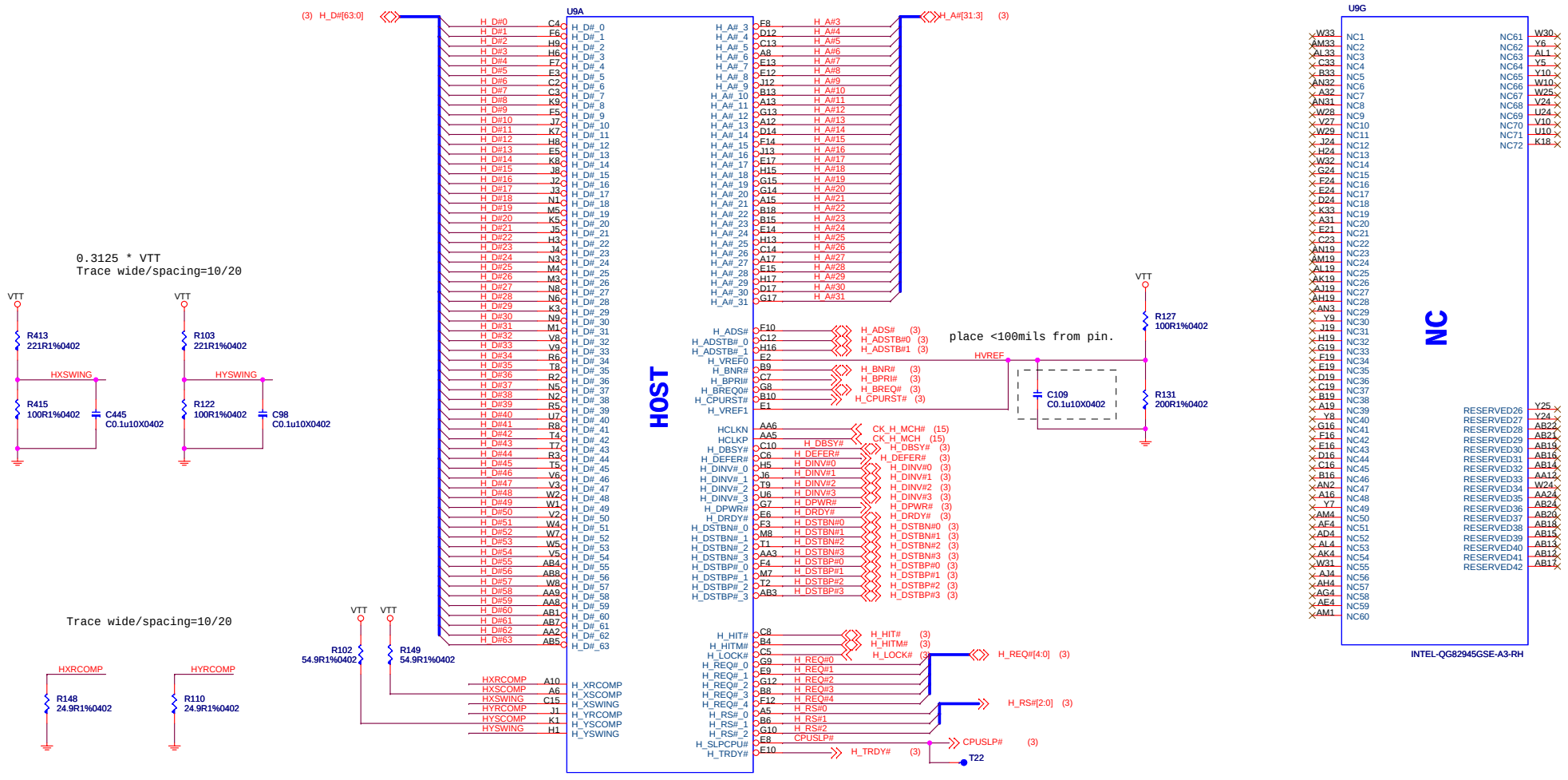
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7437	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 0A
Date: Friday, September 05, 2008	Sheet 2 of 35	


U10A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
QGZT-1.6G_FCBGA437-RH
U10B
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
QGZT-1.6G_FCBGA437-RH
0.5" max length
25 MIL AWAY FROM HIGH SPEED SIGNAL
HCOMP0,2==>18MIL
HCOMP1,3==>5MIL
R5293,R5356 change to 0402
0529
8P4R-1KR0402
8P4R-56R0402
MICRO-STAR INT'L CO.,LTD
MS-7437
Diamondville signal
Rev 0A
Date: Friday, September 05, 2008
Sheet 3 of 35



LAYOUT NOTE:
Route VCCSENSE and VSSSENSE traces at 27.4Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: Diamondville_Power/GND
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 4 of 35

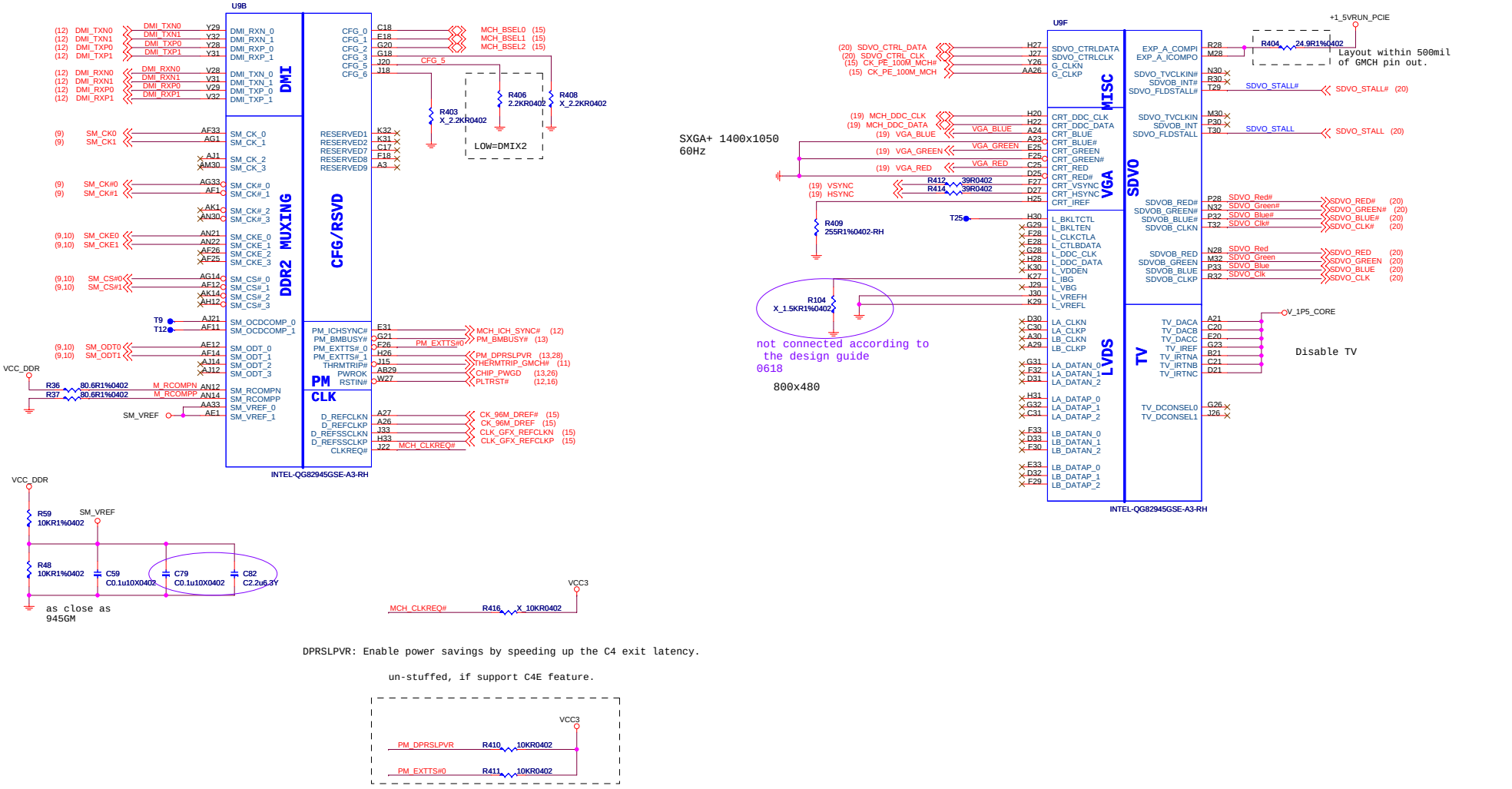


MICRO-STAR INT'L CO.,LTD

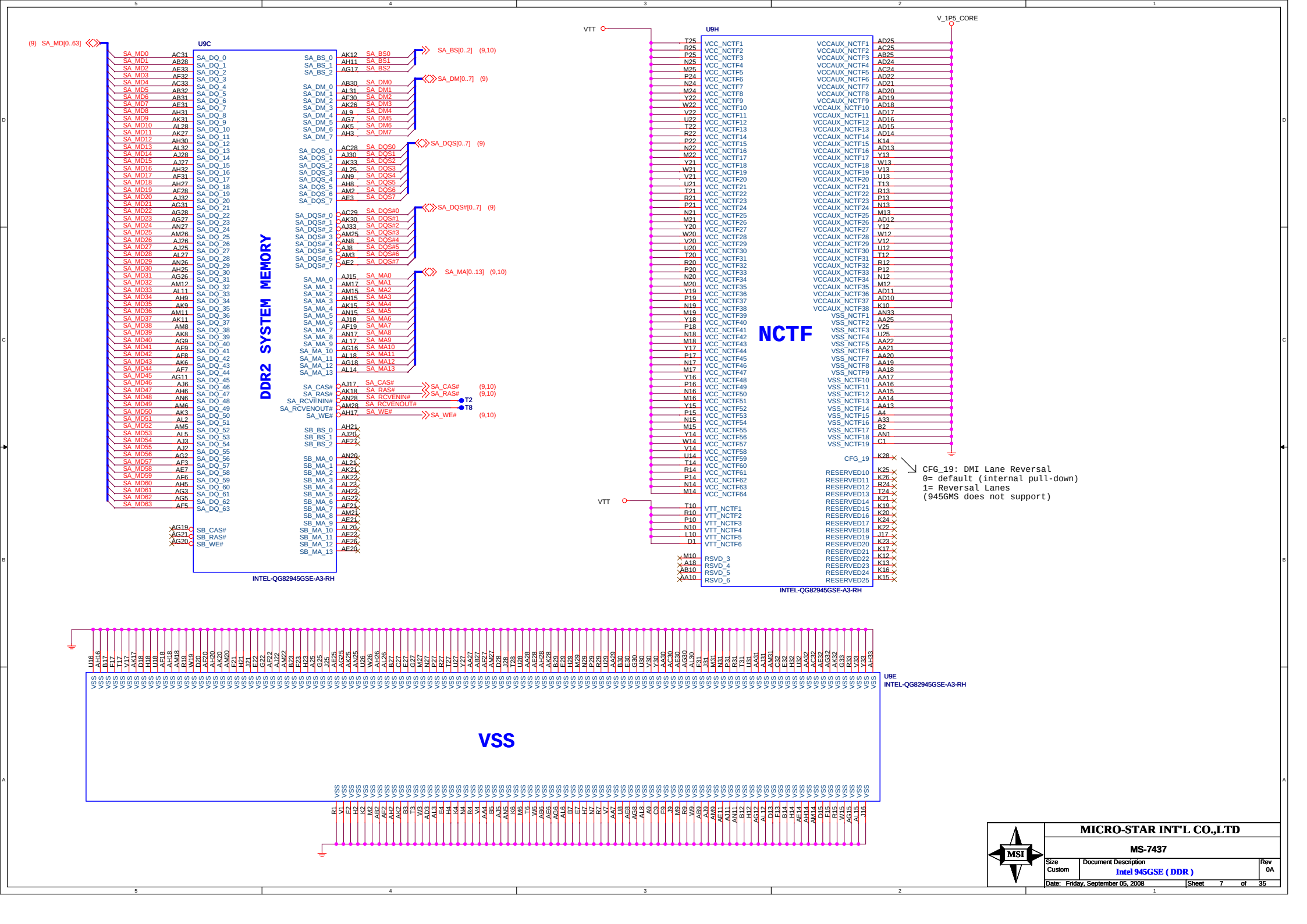
MS-7437

Size	Document Description	Rev
Custom	Intel 945GSE (HOST)	0A

Date: Friday, September 05, 2008 | Sheet 5 of 35



MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: Intel 945GSE (DMI / VGA)
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 6 of 35


(9) SA_MD[0..63]
U9C
DDR2 SYSTEM MEMORY
SA_MD0 AC31
SA_MD1 AB28
SA_MD2 AE33
SA_MD3 AF32
SA_MD4 AC33
SA_MD5 AB32
SA_MD6 AB31
SA_MD7 AE31
SA_MD8 AH31
SA_MD9 AK31
SA_MD10 AL28
SA_MD11 AK27
SA_MD12 AH30
SA_MD13 AL32
SA_MD14 AJ28
SA_MD15 AJ27
SA_MD16 AH32
SA_MD17 AF31
SA_MD18 AH27
SA_MD19 AF28
SA_MD20 AJ32
SA_MD21 AG31
SA_MD22 AG28
SA_MD23 AG27
SA_MD24 AN27
SA_MD25 AM26
SA_MD26 AJ26
SA_MD27 AJ25
SA_MD28 AL27
SA_MD29 AN26
SA_MD30 AH25
SA_MD31 AG26
SA_MD32 AM12
SA_MD33 AL11
SA_MD34 AH9
SA_MD35 AK9
SA_MD36 AM11
SA_MD37 AK11
SA_MD38 AM8
SA_MD39 AK8
SA_MD40 AG9
SA_MD41 AF9
SA_MD42 AF8
SA_MD43 AK6
SA_MD44 AF7
SA_MD45 AG11
SA_MD46 AJ6
SA_MD47 AH6
SA_MD48 AN6
SA_MD49 AM6
SA_MD50 AK3
SA_MD51 AL2
SA_MD52 AM5
SA_MD53 AL5
SA_MD54 AJ3
SA_MD55 AJ2
SA_MD56 AG2
SA_MD57 AF3
SA_MD58 AE7
SA_MD59 AF6
SA_MD60 AH5
SA_MD61 AG3
SA_MD62 AG5
SA_MD63 AF5
SA_DQ_0 SA_DQ_1 SA_DQ_2 SA_DQ_3 SA_DQ_4 SA_DQ_5 SA_DQ_6 SA_DQ_7 SA_DQ_8 SA_DQ_9 SA_DQ_10 SA_DQ_11 SA_DQ_12 SA_DQ_13 SA_DQ_14 SA_DQ_15 SA_DQ_16 SA_DQ_17 SA_DQ_18 SA_DQ_19 SA_DQ_20 SA_DQ_21 SA_DQ_22 SA_DQ_23 SA_DQ_24 SA_DQ_25 SA_DQ_26 SA_DQ_27 SA_DQ_28 SA_DQ_29 SA_DQ_30 SA_DQ_31 SA_DQ_32 SA_DQ_33 SA_DQ_34 SA_DQ_35 SA_DQ_36 SA_DQ_37 SA_DQ_38 SA_DQ_39 SA_DQ_40 SA_DQ_41 SA_DQ_42 SA_DQ_43 SA_DQ_44 SA_DQ_45 SA_DQ_46 SA_DQ_47 SA_DQ_48 SA_DQ_49 SA_DQ_50 SA_DQ_51 SA_DQ_52 SA_DQ_53 SA_DQ_54 SA_DQ_55 SA_DQ_56 SA_DQ_57 SA_DQ_58 SA_DQ_59 SA_DQ_60 SA_DQ_61 SA_DQ_62 SA_DQ_63
AG19 SB_CAS#
AG21 SB_RAS#
AG20 SB_WE#
INTEL-QG82945GSE-A3-RH
SA_BS_0 AK12 SA_BS0
SA_BS_1 AH11 SA_BS1
SA_BS_2 AG17 SA_BS2
SA_BS[0..2] (9,10)
SA_DM_0 AB30 SA_DM0
SA_DM_1 AL31 SA_DM1
SA_DM_2 AF30 SA_DM2
SA_DM_3 AK26 SA_DM3
SA_DM_4 AL9 SA_DM4
SA_DM_5 AG7 SA_DM5
SA_DM_6 AK5 SA_DM6
SA_DM_7 AH3 SA_DM7
SA_DM[0..7] (9)
SA_DQS_0 AC28 SA_DQS0
SA_DQS_1 AJ30 SA_DQS1
SA_DQS_2 AK33 SA_DQS2
SA_DQS_3 AL25 SA_DQS3
SA_DQS_4 AN9 SA_DQS4
SA_DQS_5 AH8 SA_DQS5
SA_DQS_6 AM2 SA_DQS6
SA_DQS_7 AE3 SA_DQS7
SA_DQS[0..7] (9)
SA_DQS#_0 AC29 SA_DQS#0
SA_DQS#_1 AK30 SA_DQS#1
SA_DQS#_2 AJ33 SA_DQS#2
SA_DQS#_3 AM25 SA_DQS#3
SA_DQS#_4 AN8 SA_DQS#4
SA_DQS#_5 AJ8 SA_DQS#5
SA_DQS#_6 AM3 SA_DQS#6
SA_DQS#_7 AE2 SA_DQS#7
SA_DQS#[0..7] (9)
SA_MA_0 AJ15 SA_MA0
SA_MA_1 AM17 SA_MA1
SA_MA_2 AM15 SA_MA2
SA_MA_3 AH15 SA_MA3
SA_MA_4 AK15 SA_MA4
SA_MA_5 AN15 SA_MA5
SA_MA_6 AJ18 SA_MA6
SA_MA_7 AF19 SA_MA7
SA_MA_8 AN17 SA_MA8
SA_MA_9 AL17 SA_MA9
SA_MA_10 AG16 SA_MA10
SA_MA_11 AL18 SA_MA11
SA_MA_12 AG18 SA_MA12
SA_MA_13 AL14 SA_MA13
SA_MA[0..13] (9,10)
SA_CAS# AJ17 SA_CAS#
SA_RAS# AK18 SA_RAS#
SA_RCVENIN# AN28 SA_RCVENIN#
SA_RCVENOUT# AM28 SA_RCVENOUT#
SA_WE# AH17 SA_WE#
SA_CAS# (9,10)
SA_RAS# (9,10)
T2
T8
SA_WE# (9,10)
SB_BS_0 AH21
SB_BS_1 AJ20
SB_BS_2 AE27
SB_MA_0 AN20
SB_MA_1 AL21
SB_MA_2 AK21
SB_MA_3 AK22
SB_MA_4 AL22
SB_MA_5 AH22
SB_MA_6 AG22
SB_MA_7 AF21
SB_MA_8 AM21
SB_MA_9 AE21
SB_MA_10 AL20
SB_MA_11 AE22
SB_MA_12 AE26
SB_MA_13 AE20
VTT
U9H
NCTF
VCC_NCTF1 T25
VCC_NCTF2 R25
VCC_NCTF3 P25
VCC_NCTF4 N25
VCC_NCTF5 M25
VCC_NCTF6 P24
VCC_NCTF7 N24
VCC_NCTF8 M24
VCC_NCTF9 Y22
VCC_NCTF10 W22
VCC_NCTF11 V22
VCC_NCTF12 U22
VCC_NCTF13 T22
VCC_NCTF14 R22
VCC_NCTF15 P22
VCC_NCTF16 N22
VCC_NCTF17 M22
VCC_NCTF18 Y21
VCC_NCTF19 W21
VCC_NCTF20 V21
VCC_NCTF21 U21
VCC_NCTF22 T21
VCC_NCTF23 R21
VCC_NCTF24 P21
VCC_NCTF25 N21
VCC_NCTF26 M21
VCC_NCTF27 Y20
VCC_NCTF28 W20
VCC_NCTF29 V20
VCC_NCTF30 U20
VCC_NCTF31 T20
VCC_NCTF32 R20
VCC_NCTF33 P20
VCC_NCTF34 N20
VCC_NCTF35 M20
VCC_NCTF36 Y19
VCC_NCTF37 P19
VCC_NCTF38 N19
VCC_NCTF39 M19
VCC_NCTF40 Y18
VCC_NCTF41 P18
VCC_NCTF42 N18
VCC_NCTF43 M18
VCC_NCTF44 Y17
VCC_NCTF45 P17
VCC_NCTF46 N17
VCC_NCTF47 M17
VCC_NCTF48 Y16
VCC_NCTF49 P16
VCC_NCTF50 N16
VCC_NCTF51 M16
VCC_NCTF52 Y15
VCC_NCTF53 P15
VCC_NCTF54 N15
VCC_NCTF55 M15
VCC_NCTF56 Y14
VCC_NCTF57 W14
VCC_NCTF58 V14
VCC_NCTF59 U14
VCC_NCTF60 T14
VCC_NCTF61 R14
VCC_NCTF62 P14
VCC_NCTF63 N14
VCC_NCTF64 M14
VTT_NCTF1 T10
VTT_NCTF2 R10
VTT_NCTF3 P10
VTT_NCTF4 N10
VTT_NCTF5 L10
VTT_NCTF6 D1
RSVD_3 M10
RSVD_4 A18
RSVD_5 AB10
RSVD_6 AA10
VCCAUX_NCTF1 AD25
VCCAUX_NCTF2 AC25
VCCAUX_NCTF3 AB25
VCCAUX_NCTF4 AD24
VCCAUX_NCTF5 AC24
VCCAUX_NCTF6 AD22
VCCAUX_NCTF7 AD21
VCCAUX_NCTF8 AD20
VCCAUX_NCTF9 AD19
VCCAUX_NCTF10 AD18
VCCAUX_NCTF11 AD17
VCCAUX_NCTF12 AD16
VCCAUX_NCTF13 AD15
VCCAUX_NCTF14 AD14
VCCAUX_NCTF15 K14
VCCAUX_NCTF16 AD13
VCCAUX_NCTF17 Y13
VCCAUX_NCTF18 W13
VCCAUX_NCTF19 V13
VCCAUX_NCTF20 U13
VCCAUX_NCTF21 T13
VCCAUX_NCTF22 R13
VCCAUX_NCTF23 P13
VCCAUX_NCTF24 N13
VCCAUX_NCTF25 M13
VCCAUX_NCTF26 AD12
VCCAUX_NCTF27 Y12
VCCAUX_NCTF28 W12
VCCAUX_NCTF29 V12
VCCAUX_NCTF30 U12
VCCAUX_NCTF31 T12
VCCAUX_NCTF32 R12
VCCAUX_NCTF33 P12
VCCAUX_NCTF34 N12
VCCAUX_NCTF35 M12
VCCAUX_NCTF36 AD11
VCCAUX_NCTF37 AD10
VCCAUX_NCTF38 K10
VSS_NCTF1 AN33
VSS_NCTF2 AA25
VSS_NCTF3 V25
VSS_NCTF4 U25
VSS_NCTF5 AA22
VSS_NCTF6 AA21
VSS_NCTF7 AA20
VSS_NCTF8 AA19
VSS_NCTF9 AA18
VSS_NCTF10 AA17
VSS_NCTF11 AA16
VSS_NCTF12 AA15
VSS_NCTF13 AA14
VSS_NCTF14 AA13
VSS_NCTF15 A4
VSS_NCTF16 A33
VSS_NCTF17 B2
VSS_NCTF18 AN1
VSS_NCTF19 C1
CFG_19 K28
RESERVED10 K25
RESERVED11 K26
RESERVED12 R24
RESERVED13 T24
RESERVED14 K21
RESERVED15 K19
RESERVED16 K20
RESERVED17 K24
RESERVED18 K22
RESERVED19 J17
RESERVED20 K23
RESERVED21 K17
RESERVED22 K12
RESERVED23 K13
RESERVED24 K16
RESERVED25 K15
INTEL-QG82945GSE-A3-RH
V_1P5_CORE
CFG_19: DMI Lane Reversal
0= default (internal pull-down)
1= Reversal Lanes
(945GMS does not support)
U16 AH16 B17 E17 T17 V17 AK17 D18 H18 U18 AE18 AH18 AM18 R19 W19 D20 AF20 AH20 AK20 AM20 F21 H21 J21 E22 G22 AE22 AJ22 AM22 B23 F23 H23 A25 G25 J25 AC25 AK25 AN25 U26 W26 AH26 AL26 B27 E27 G27 M27 N27 P27 R27 U27 V27 Y27 AA27 AB27 AF27 AM27 D28 J28 L28 U28 AA28 AE28 AH28 AK28 B29 E29 H29 M29 N29 P29 R29 U29 AA29 B30 E30 G30 U30 V30 AA30 AC30 AE30 AG30 E31 J31 M31 N31 P31 R31 U31 H32 U32 AA31 AJ31 AM31 C32 E32 H32 U32 AC32 AE32 AG32 G33 R33 V33 Y33 AH33
VSS
U9E
INTEL-QG82945GSE-A3-RH
R1 V1 F2 H2 K2 M2 AB2 AE2 AH2 A2 B3 T3 W3 AD3 AL3 E4 H4 M4 N4 R4 V4 AA4 B5 AJ5 AN5 L6 M6 T6 W6 AB6 AE6 AG6 A6 E7 H7 N7 R7 V7 AA7 U8 AB8 AG8 AL8 A9 C9 F9 J9 M9 W9 AB9 AJ9 AM9 AE11 AJ11 AN11 B12 H12 AG12 AL12 D13 F13 B14 H14 AE14 AJ14 AM14 D15 F15 R15 W15 AG15 AL15 J16
MICRO-STAR INT'L CO.,LTD
MS-7437
Size Custom
Document Description
Intel 945GSE (DDR)
Rev 0A
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945 GSE Power

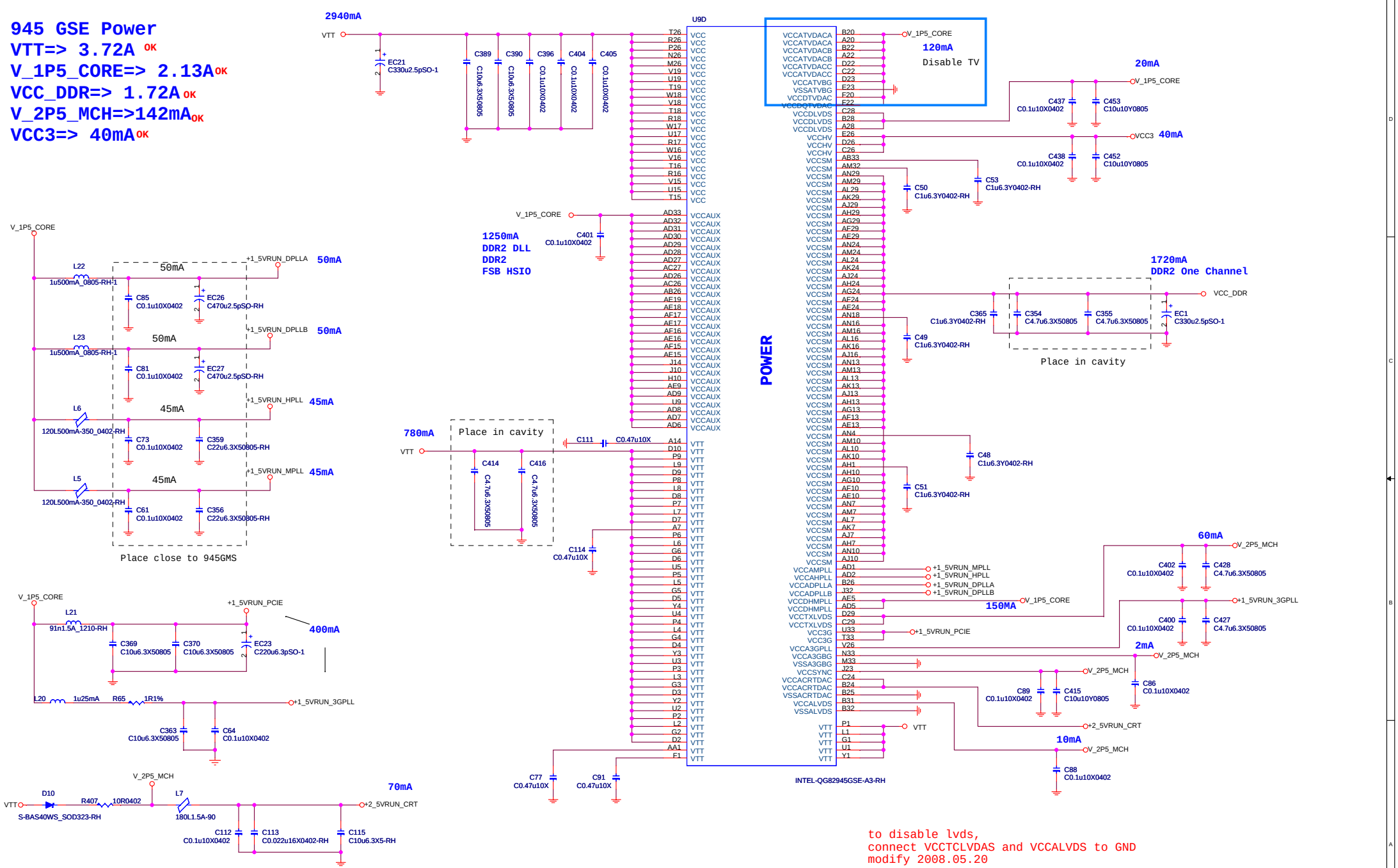
VTT=> 3.72A OK

V_1P5_CORE=> 2.13A OK

VCC_DDR=> 1.72A OK

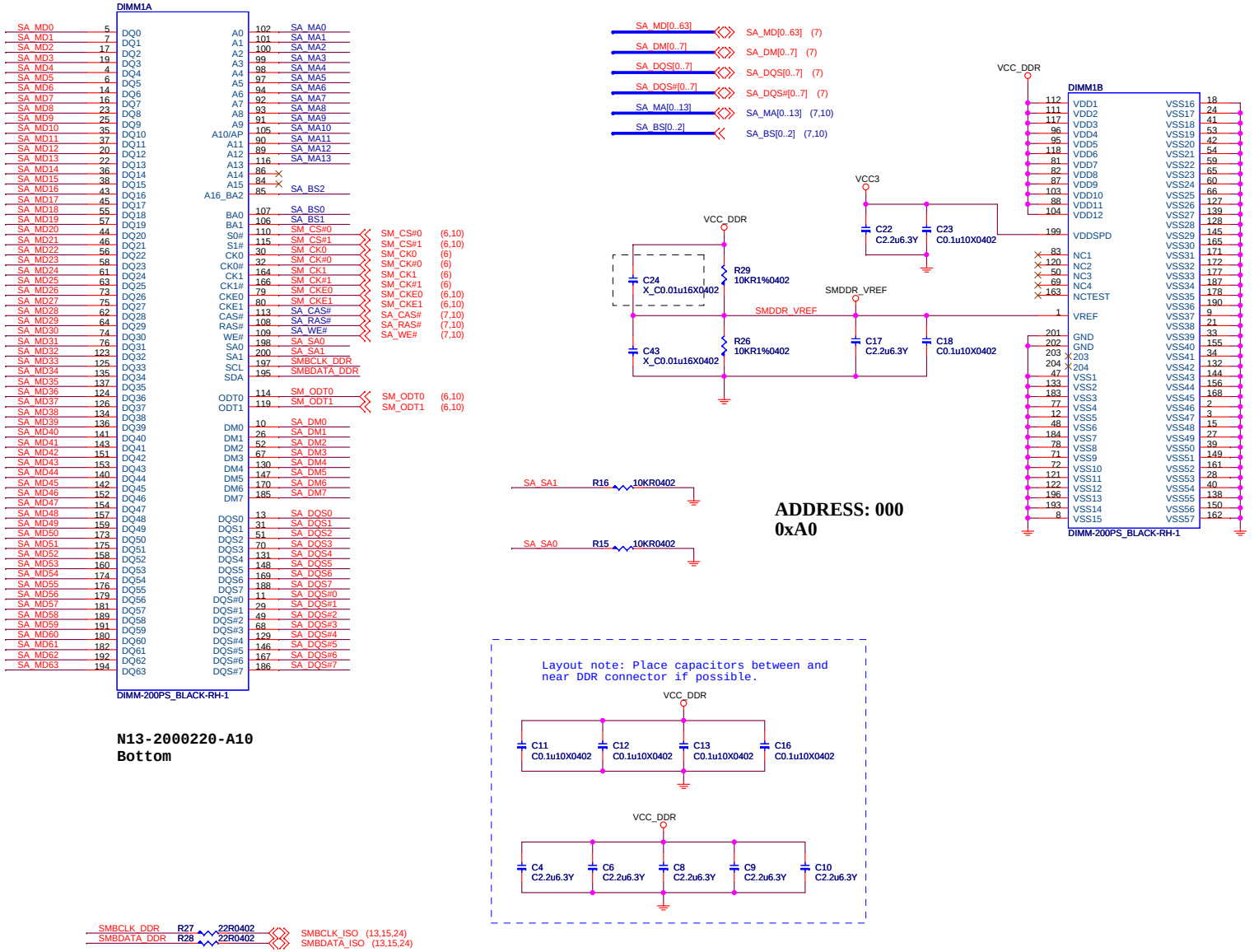
V_2P5_MCH=>142mA OK

VCC3=> 40mA OK



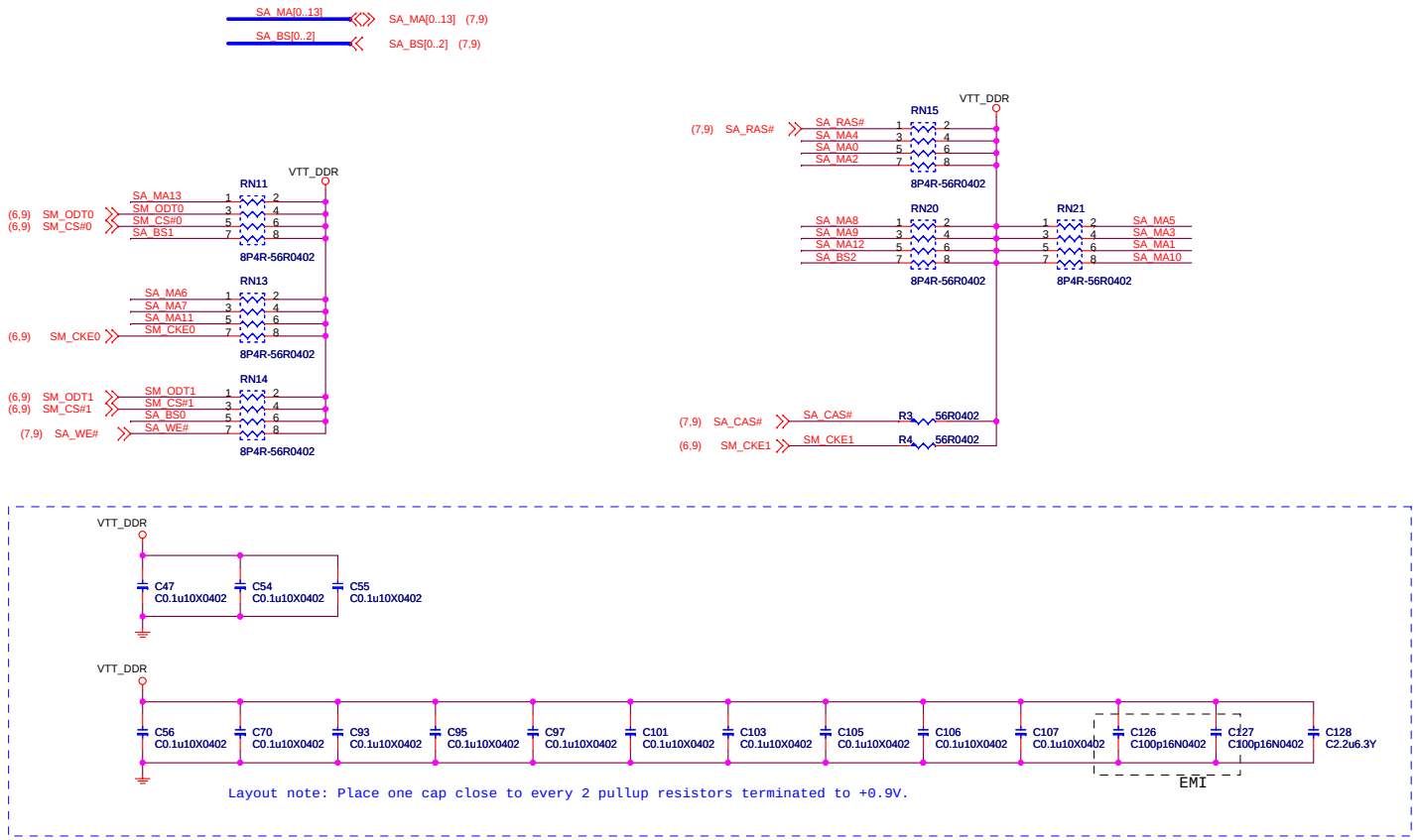
to disable lvds,
connect VCCTCLVDAS and VCCALVDS to GND
modify 2008.05.20

MICRO-STAR INT'L CO.,LTD		
MS-7437		
Size: Custom	Document Description: Intel 945GSE (Power)	Rev: 0A
Date: Friday, September 05, 2008	Sheet 8 of 35	

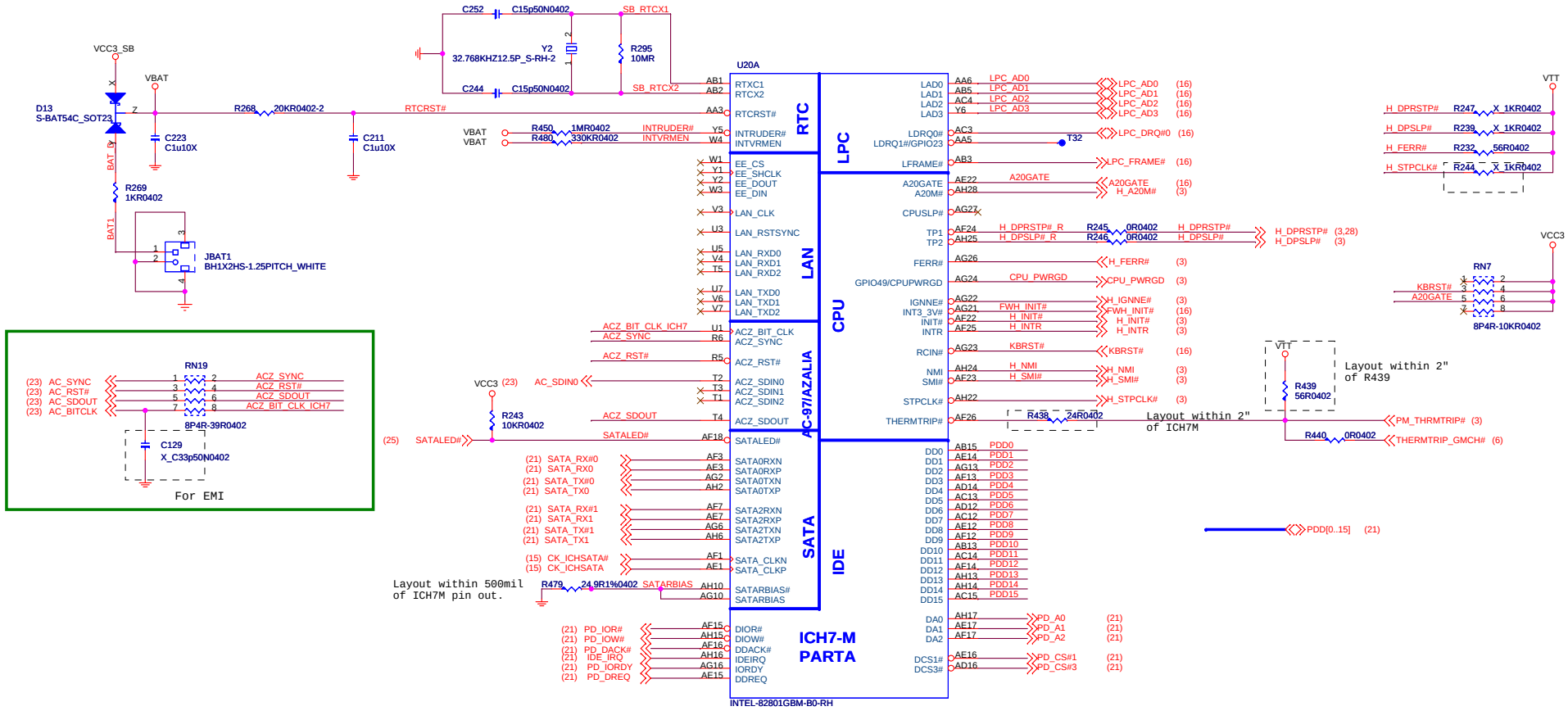


N13-2000220-A10
Bottom

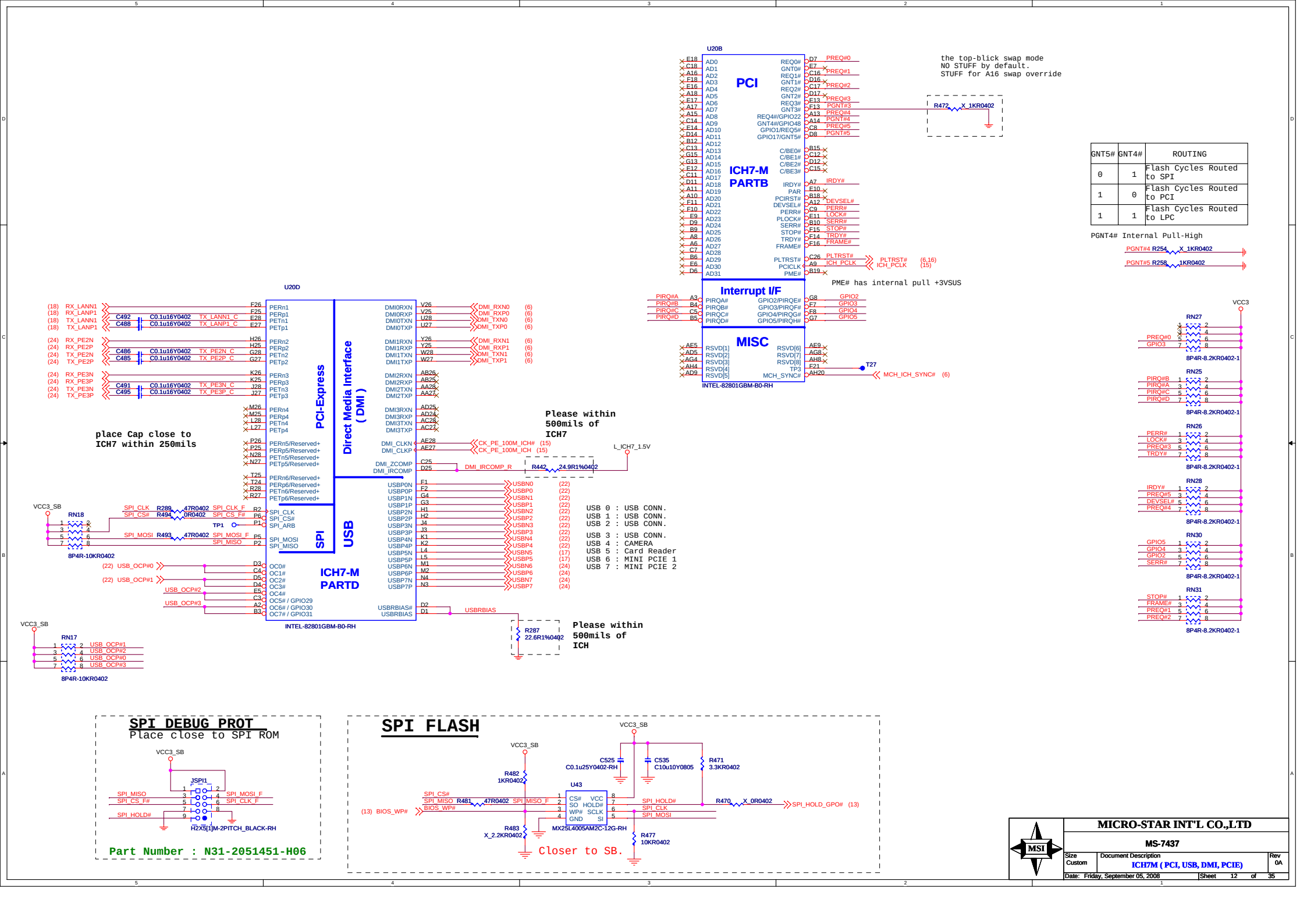
MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: DDR2 SO-DIMM1 Slot
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 9 of 35



MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: DDR2 Termination
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 10 of 35



MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: ICH7M (CPU,LPC,SATA,HDA)
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 11 of 35


U20B
PCI
ICH7-M
PARTB
Interrupt I/F
MISC
INTEL-82801GBM-B0-RH
the top-blick swap mode
NO STUFF by default.
STUFF for A16 swap override
R472 X_1KR0402
PME# has internal pull +3VSUS
PGNT4# Internal Pull-High
PGNT#4 R254 X_1KR0402
PGNT#5 R258 1KR0402
U20D
PCI-Express
Direct Media Interface (DMI)
SPI
USB
ICH7-M
PARTD
INTEL-82801GBM-B0-RH
place Cap close to
ICH7 within 250mils
Please within
500mils of
ICH7
R442 24.9R1%0402
L_ICH7_1.5V
R287 22.6R1%0402
Please within
500mils of
ICH
USB 0 : USB CONN.
USB 1 : USB CONN.
USB 2 : USB CONN.
USB 3 : USB CONN.
USB 4 : CAMERA
USB 5 : Card Reader
USB 6 : MINI PCIE 1
USB 7 : MINI PCIE 2
RN18
RN17
RN27
RN25
RN26
RN28
RN30
RN31
8P4R-10KR0402
8P4R-8.2KR0402-1
GNT5# GNT4# ROUTING
0 1 Flash Cycles Routed to SPI
1 0 Flash Cycles Routed to PCI
1 1 Flash Cycles Routed to LPC
SPI DEBUG PROT
Place close to SPI ROM
JSPI1
H2X5[1]M-2PITCH_BLACK-RH
Part Number : N31-2051451-H06
SPI FLASH
U43
MX25L4005AM2C-12G-RH
Closer to SB.
MICRO-STAR INT'L CO.,LTD
MS-7437
ICH7M (PCI, USB, DMI, PCIE)
Date: Friday, September 05, 2008
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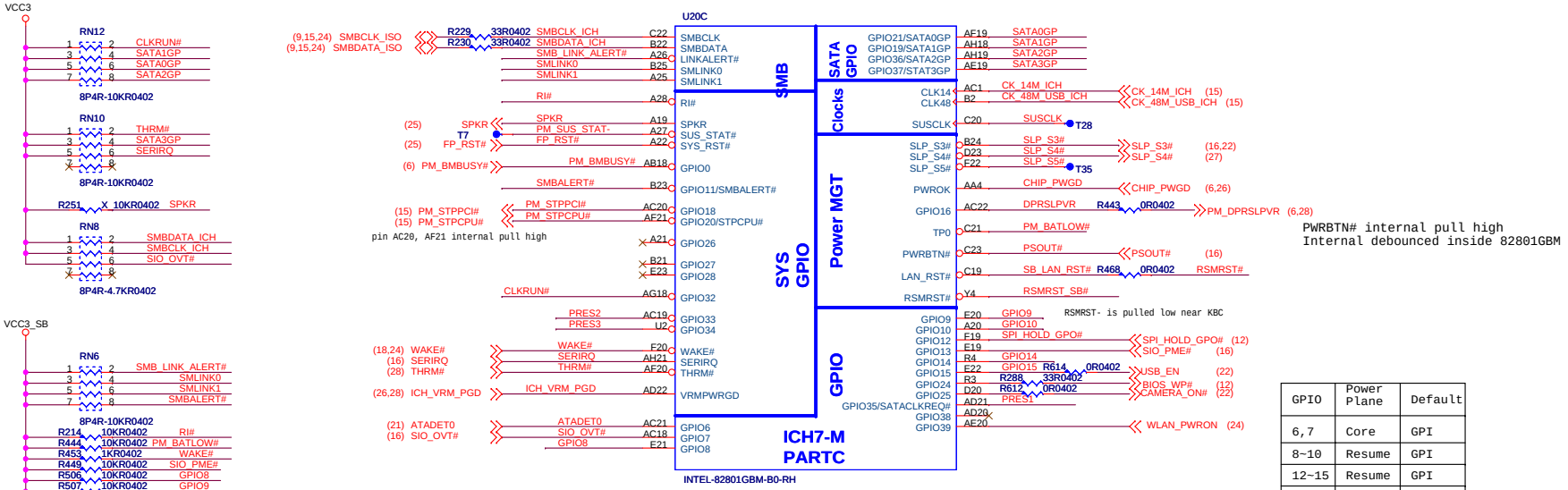

GPIO	Power Plane	Default
6,7	Core	GPI
8~10	Resume	GPI
12~15	Resume	GPI
24,25	Resume	GPO
38,39	Core	GPI

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ICH7M (GPIO,CLK,SM)	0A

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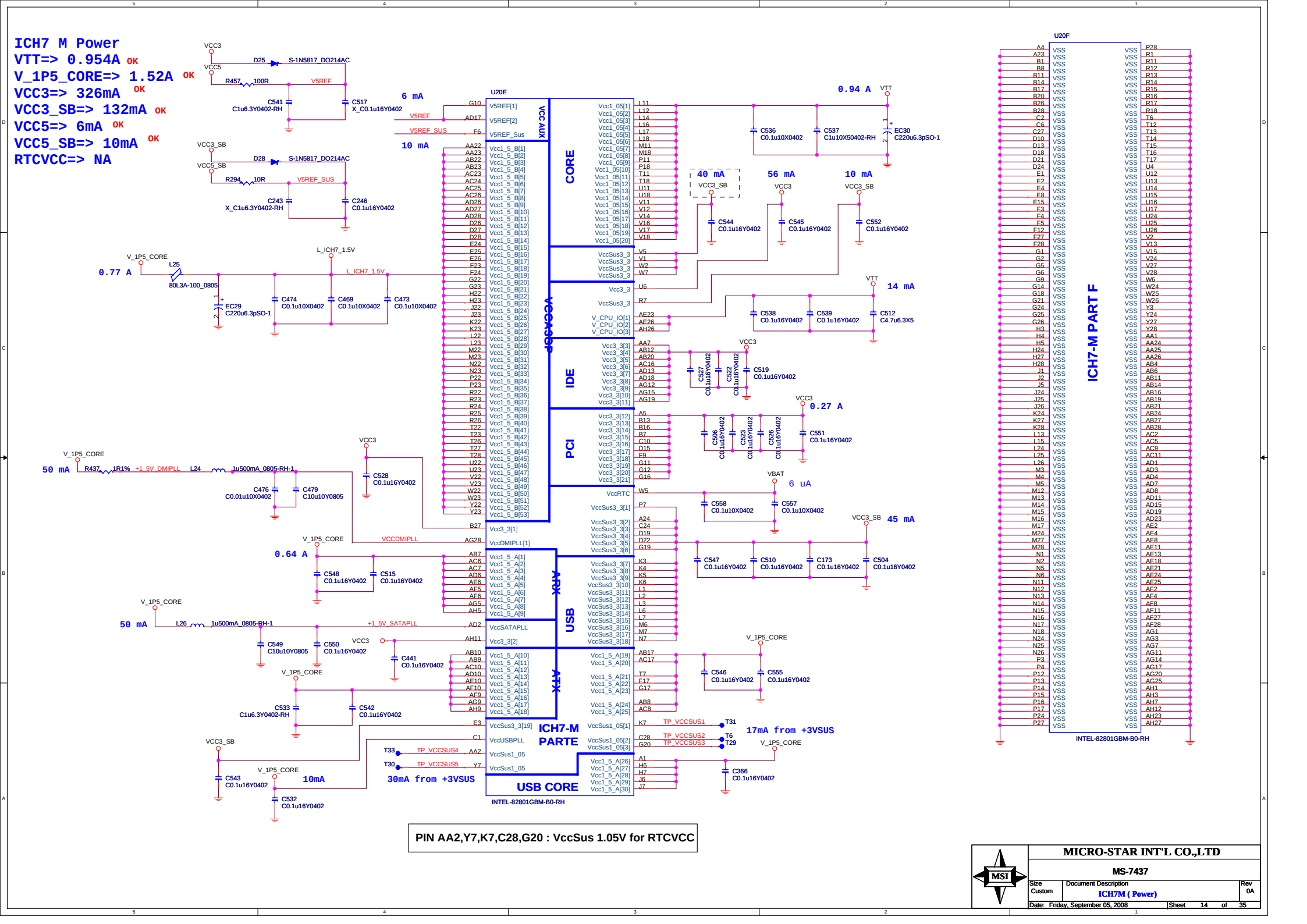
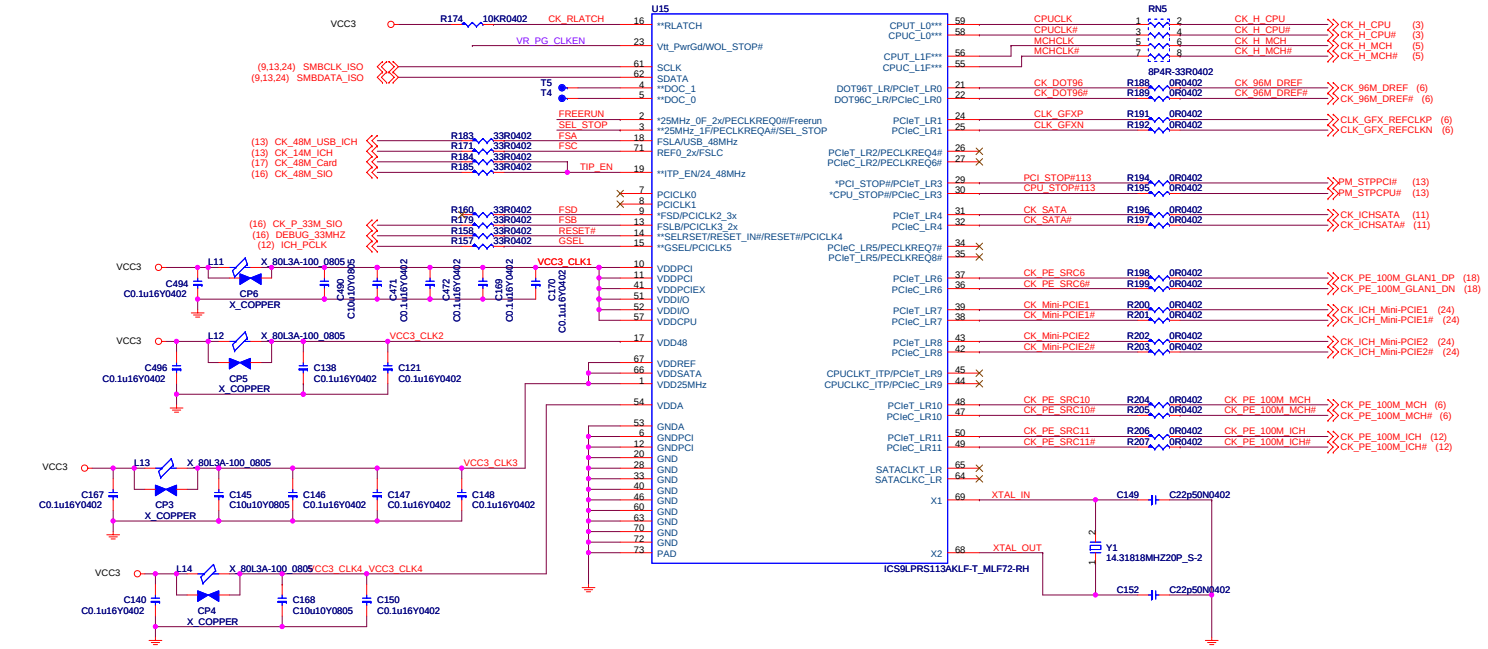
ICH7 M Power

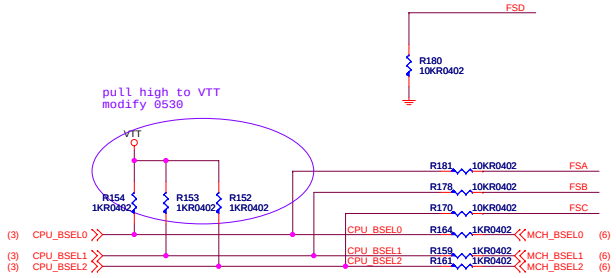
VTT=> 0.954A OK
V_1P5_CORE=> 1.52A OK
VCC3=> 326mA OK
VCC3_SB=> 132mA OK
VCC5=> 6mA OK
VCC5_SB=> 10mA OK
RTCVCC=> NA

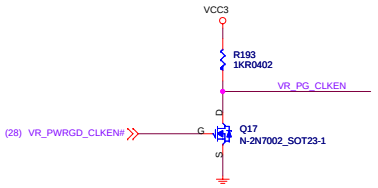


MICRO-STAR INT'L CO.,LTD	
MS-7437	
Size: Custom	Document Description: ICH7M (Power)
Rev: 0A	
Date: Friday, September 05, 2008	Sheet 14 of 35

CLK Gen ICS9LPRS113







CLOCK GEN STRAPING

1 => Pin21/22 96MHz
0 => Pin21/22 100MHz

GSEL R175 4.7KR0402 VCC3
R176 X_4.7KR0402

L:PCICLK4
H:RESET*
to be WDT rest=> HI

RESET# R177 4.7KR0402

113
TIP_EN=0 => PCIEX9.
TIP_EN=1 => CPU_ITP

TIP_EN R186 X_4.7KR0402

FREERUN R156 X_4.7KR0402 VCC3
R173 X_4.7KR0402

Selects pin 29/830
1 = PCI_STOP#/CPU_STOP#
0 =PCIEX CLK output

SEL_STOP R155 4.7KR0402 VCC3
R172 X_4.7KR0402

CK_P_33M_SIO C124 X_C10p25N0402
ICH_PCLK C122 X_C10p25N0402
CK_48M_Card C139 X_C10p25N0402
DEBUG_33MHZ C123 X_C10p25N0402
CK_48M_USB_ICH C137 X_C10p25N0402
CK_48M_SIO C141 X_C10p25N0402
CK_14M_ICH C125 X_C10p25N0402

CPU Table

BSEL[2]	BSEL[1]	BSEL[0]	BCLK
L	L	L	100MHZ
L	L	H	133MHZ
L	H	L	RESERVED
L	H	H	166MHZ

CLK Gen 113

BSEL[2]	BSEL[1]	BSEL[0]	BCLK
H	L	H	100MHZ
L	L	H	133MHZ
L	H	L	200MHz
L	H	H	166MHZ

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Size: Custom | Document Description: CLK GEN [ICS9LPRS113] | Rev: 0A

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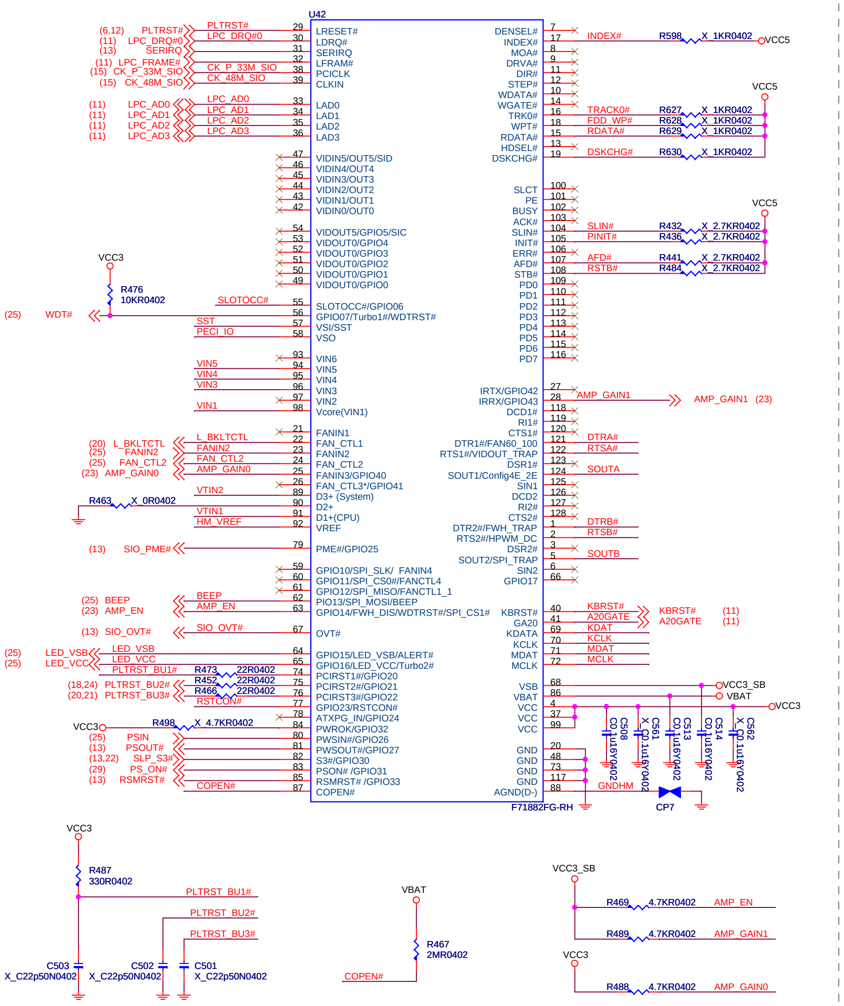
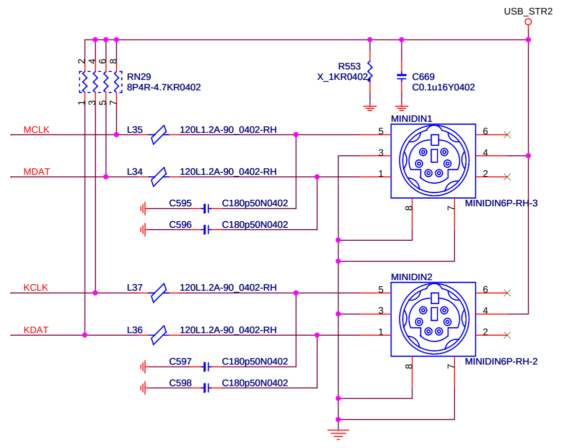
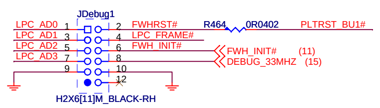


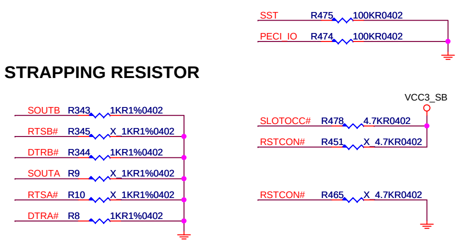
PS2 KEYBOARD & MOUSE CONNECTOR



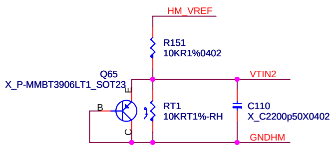
LPC Debug Port



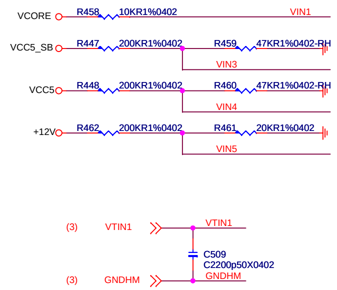
STRAPPING RESISTOR



Thermal Resistor



Hardware monitor



Pin	Function	Net name	HI	LO
1	FWH_TRAP	DTRB#	SPI as a backup BIOS	SPI as a primary BIOS
2	HPWM_DC	RTSB#	PWM Fan	LINEAR FAN
5	SPI_TRAP	SOUTB	SPI function disable	SPI function enable
121	FAN60_100	DTRA#	Power on FAN speed DUTY : 60%	Power on FAN speed DUTY : 100%
122	VIDOUT	RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
124	Config4E_2E	SOUTA	4E	2E

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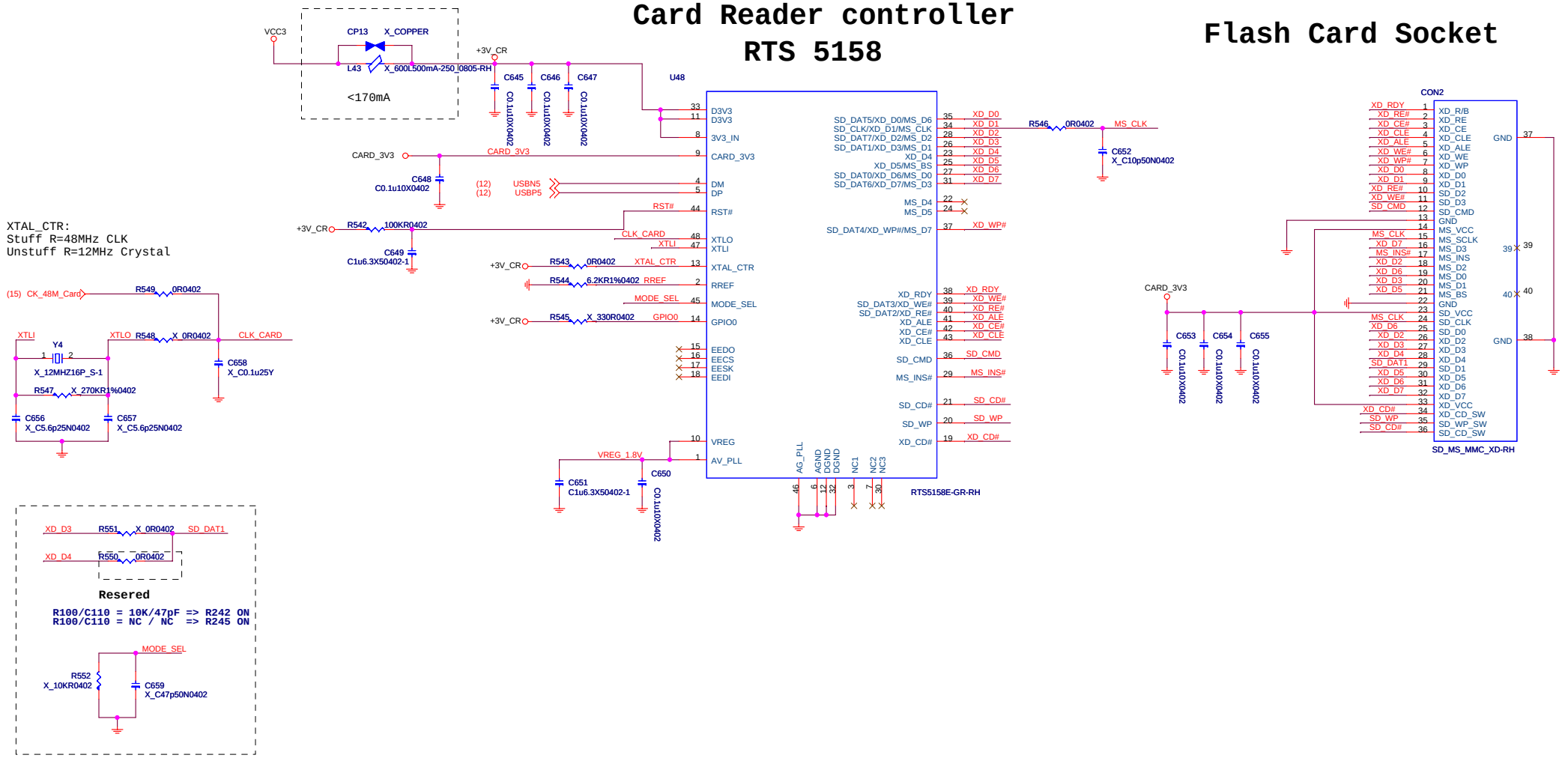
Card Reader controller
RTS 5158

Flash Card Socket



XTAL_CTR:
Stuff R=48MHz CLK
Unstuff R=12MHz Crystal

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MS-7437		
Size: Custom	Document Description: Card Reader RTS5158E	Rev: 0A
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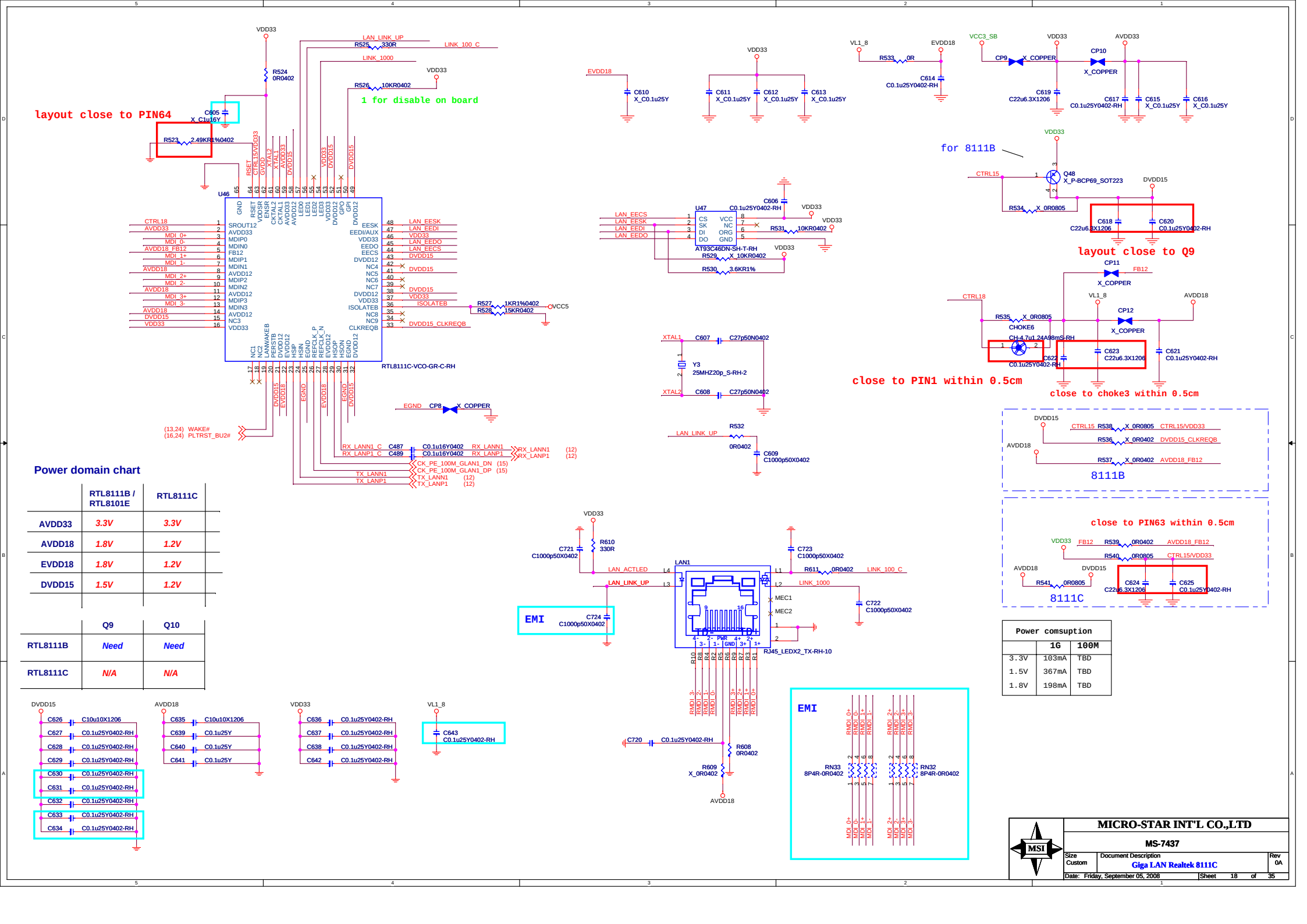

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q9	Q10
RTL8111B	Need	Need
RTL8111C	N/A	N/A

Power comsuption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

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Size: Custom	Document Description: Giga LAN Realtek 8111C
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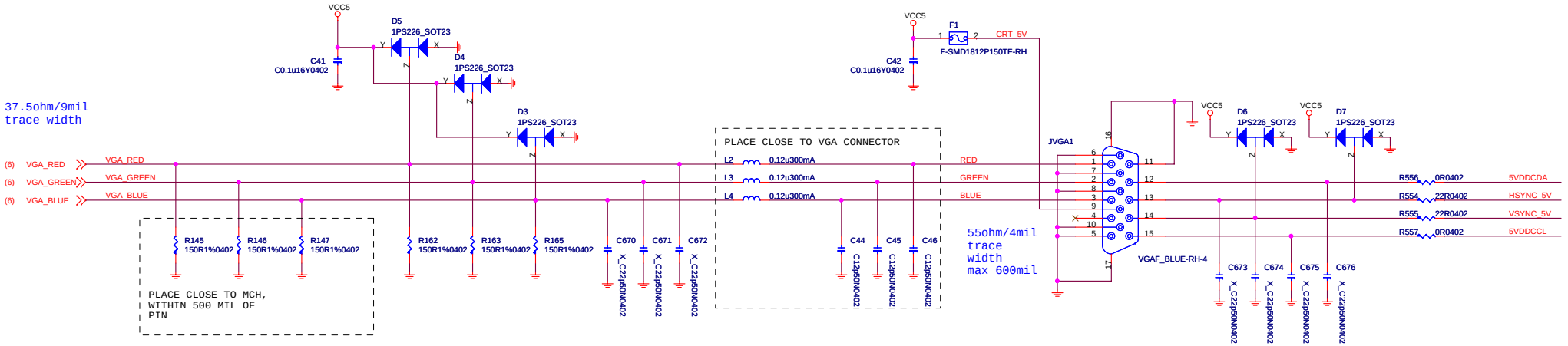
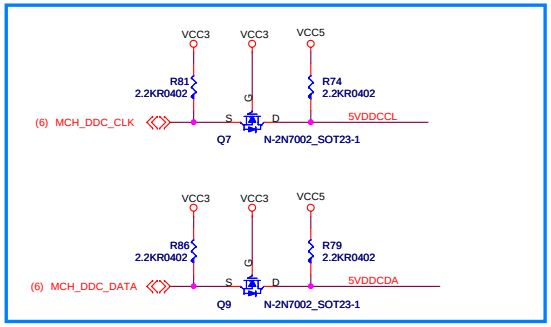
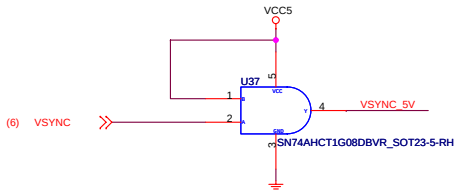
Video Connector

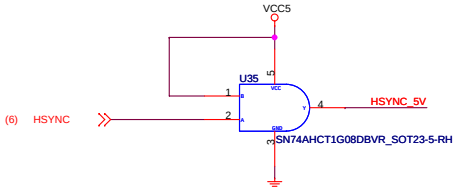
change ESD diode
modify 0609

37.5ohm/9mil
trace width









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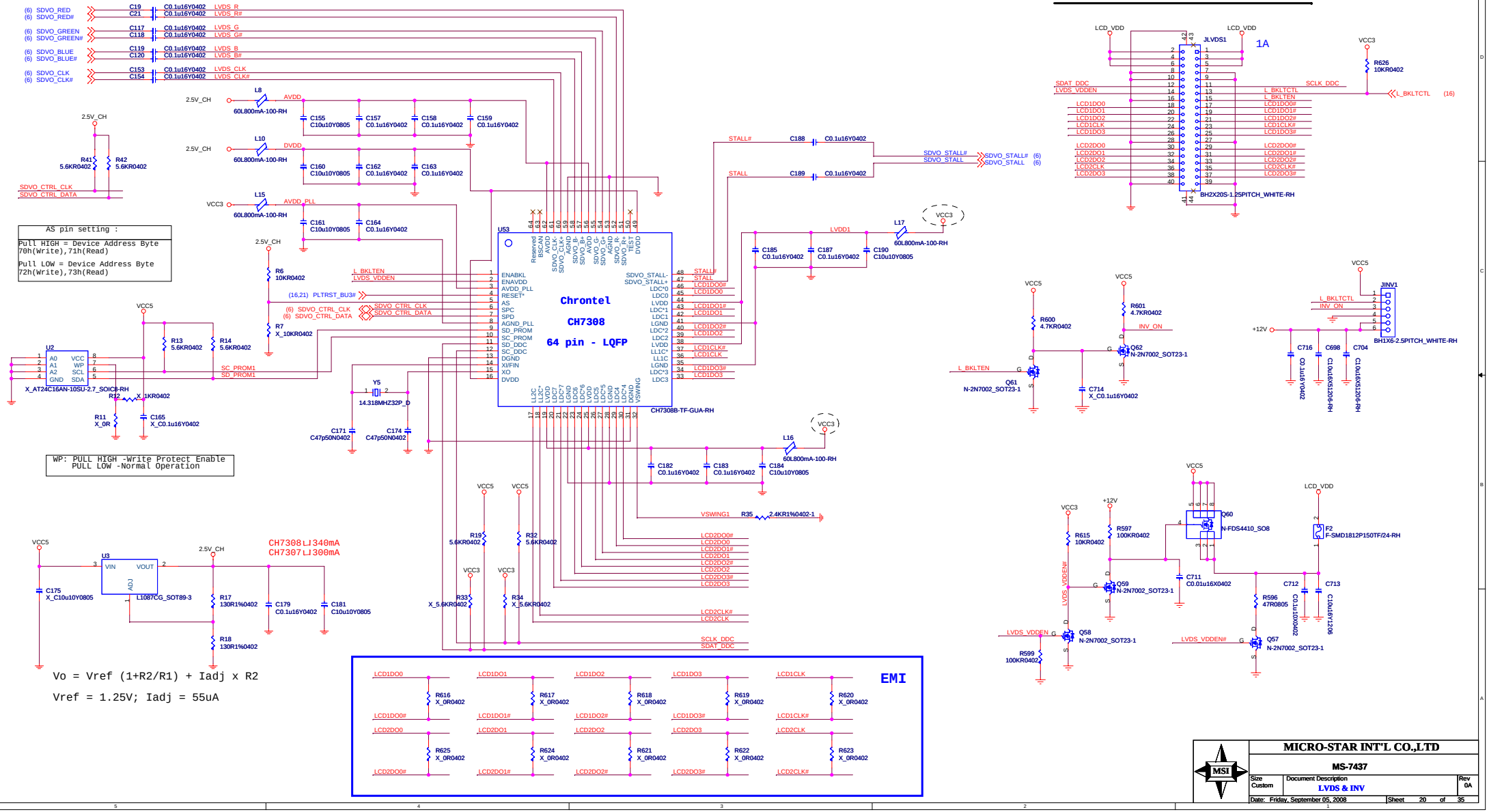
LVDS PIN HEADER



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Size: Custom	Document Description: LVDS & INV
Rev: 0A	
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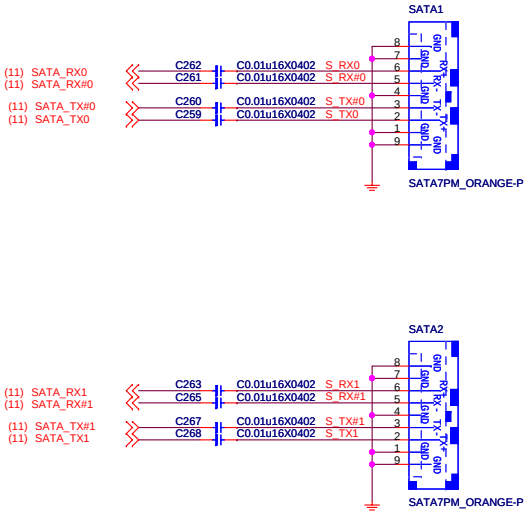
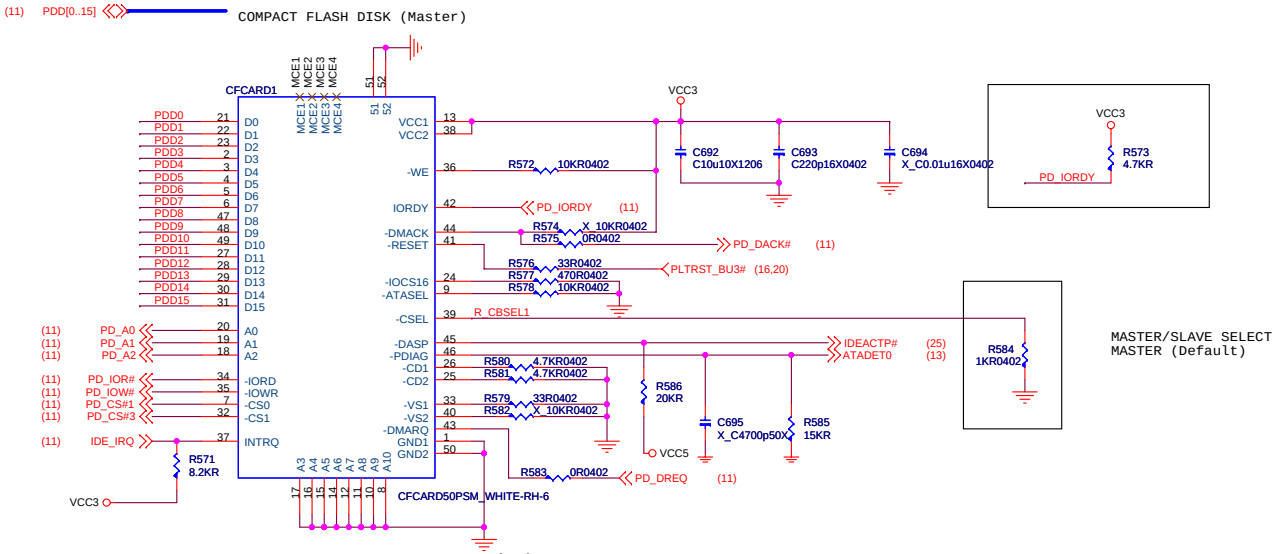
SERIAL ATA CONNECTOR BLOCK

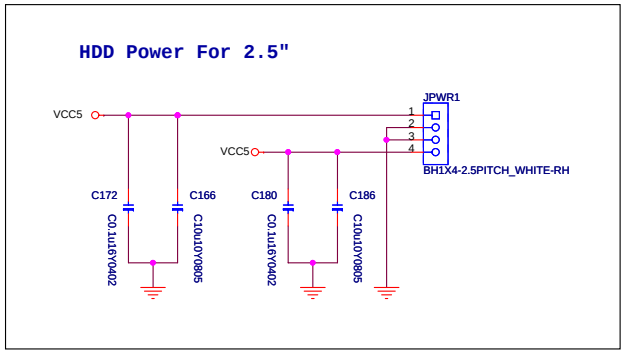


CF Card BLOCK



PDIAG# & DASP# are output during reset for SLAVE detection.

HDD Power For 2.5"



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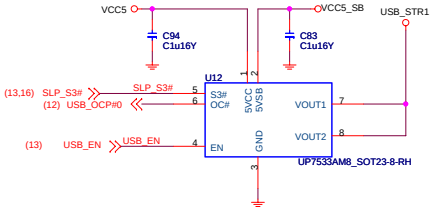
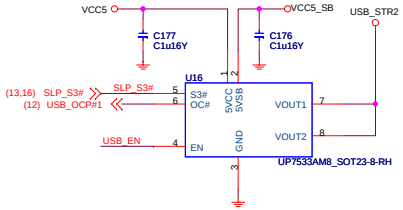
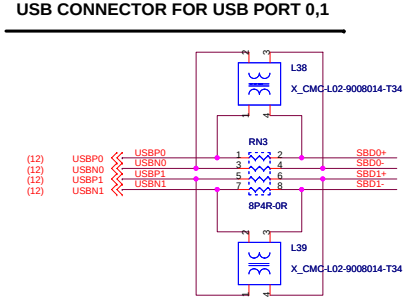
POWER CIRCUIT FOR USB PORT 0,1

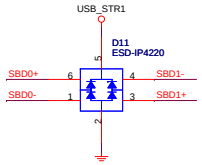


POWER CIRCUIT FOR USB PORT 2,3

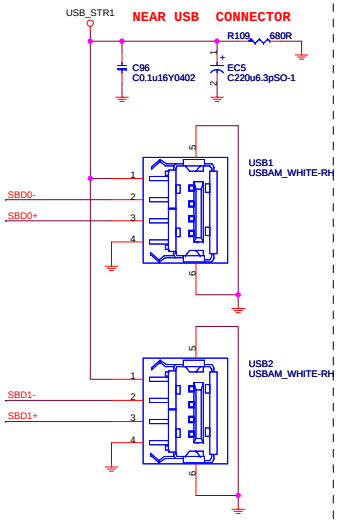


USB CONNECTOR FOR USB PORT 0,1

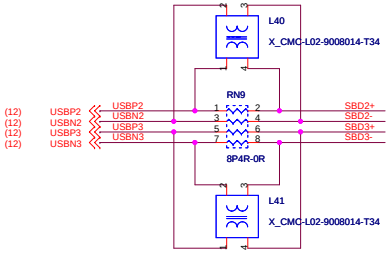


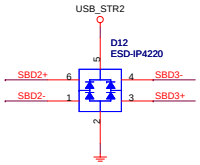


NEAR USB CONNECTOR

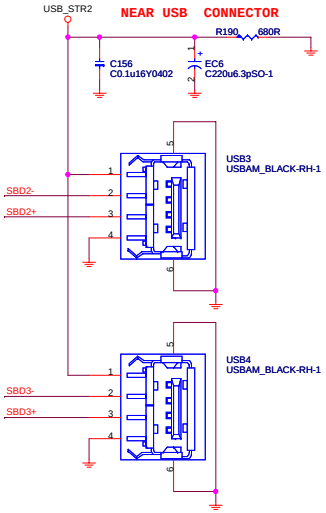


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

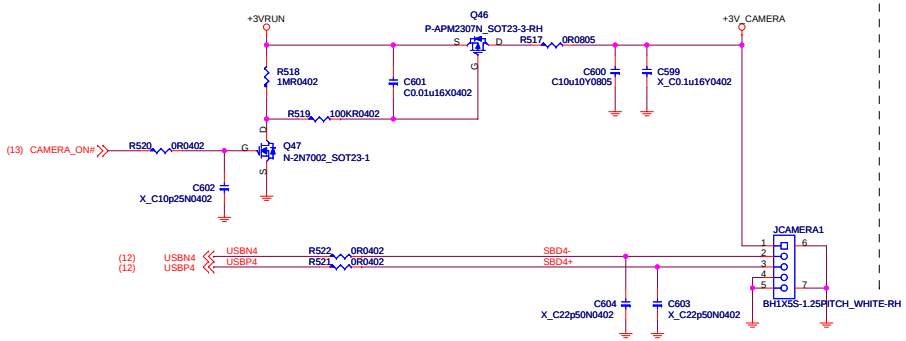




NEAR USB CONNECTOR



CAMERA



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Size: Custom	Document Description: USB 0~4 CONNECTORS	Rev: 0A
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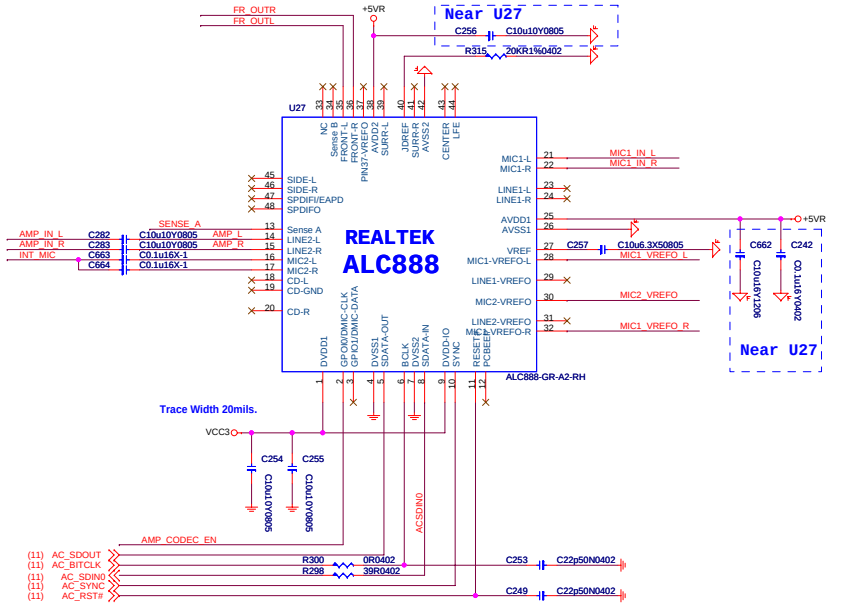
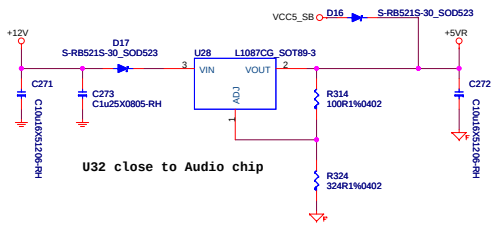
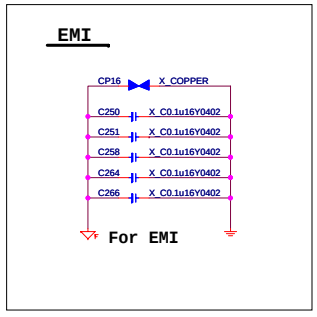
ALC888 CODEC



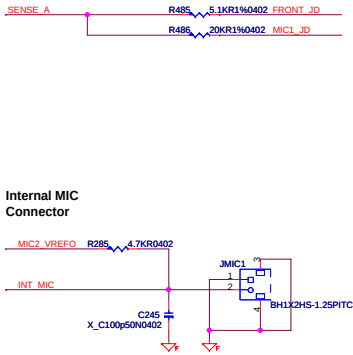
AUDIO CODE REGULATORS



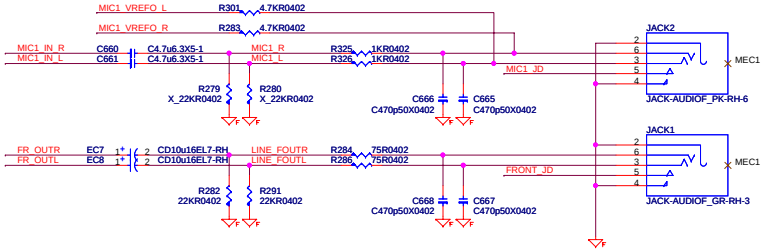
EMI

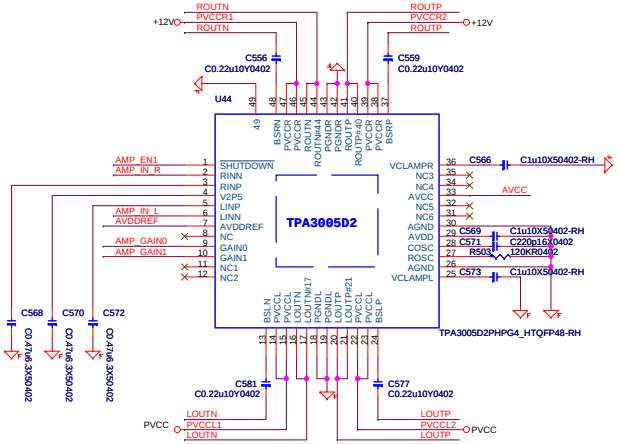


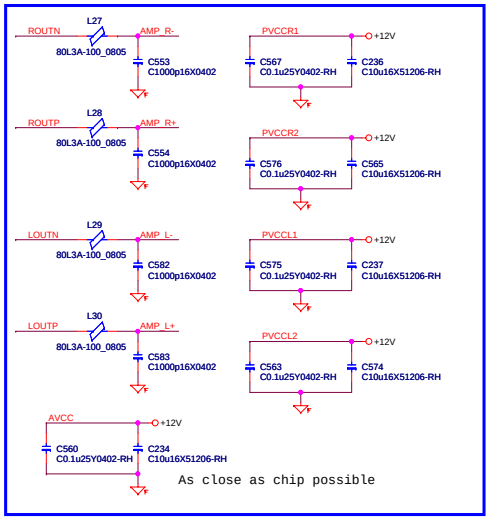
ALC888 JACK DETECT

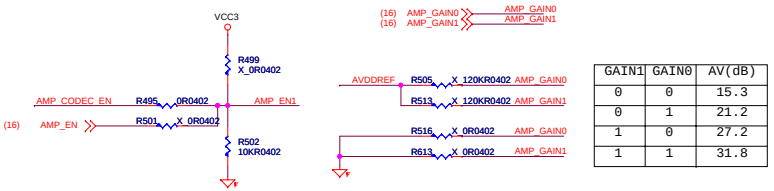


ALC888 JACK

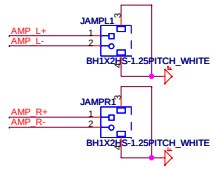








GAIN1	GAIN0	AV(dB)
0	0	15.3
0	1	21.2
1	0	27.2
1	1	31.8



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Size: Custom	Document Description: Azalia - ALC888 & AMP
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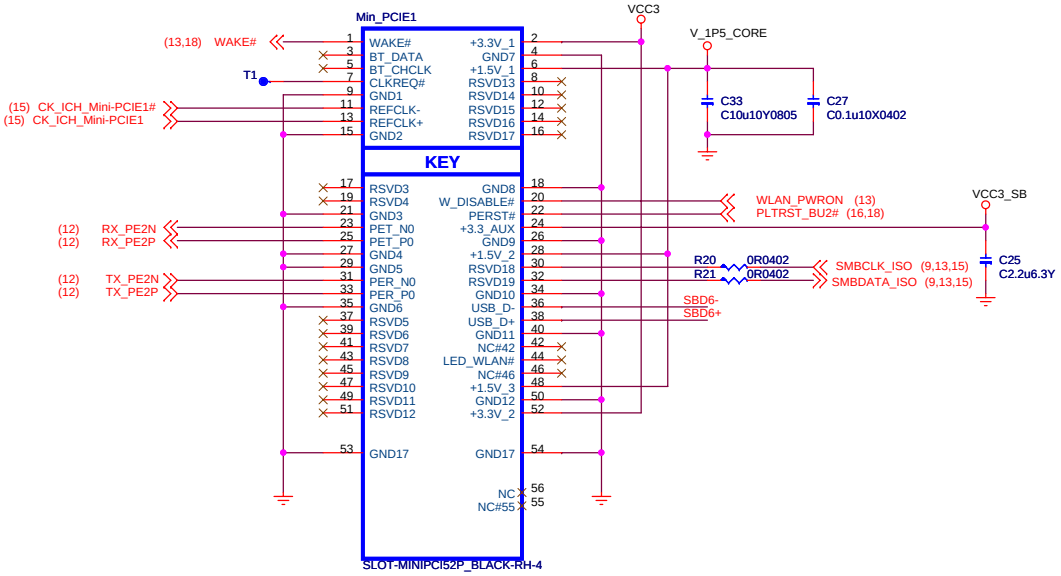
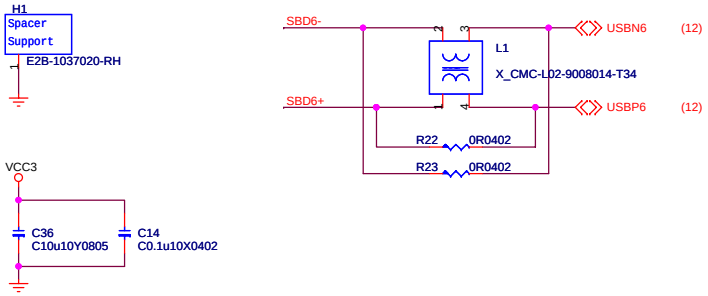
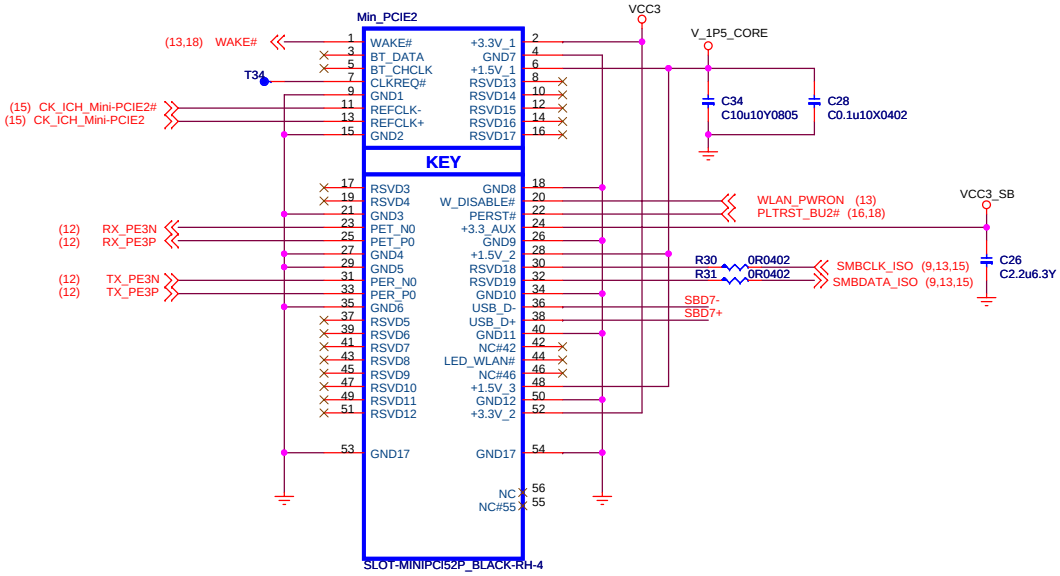
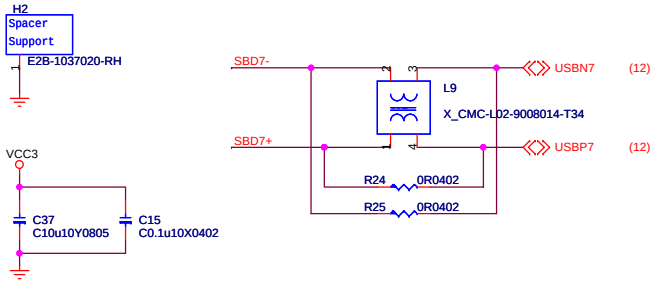
Mini PCI-E Slot 1





Mini PCI-E Slot 2





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Size: Custom	Document Description: Mini PCI-E Slot	Rev: 0A
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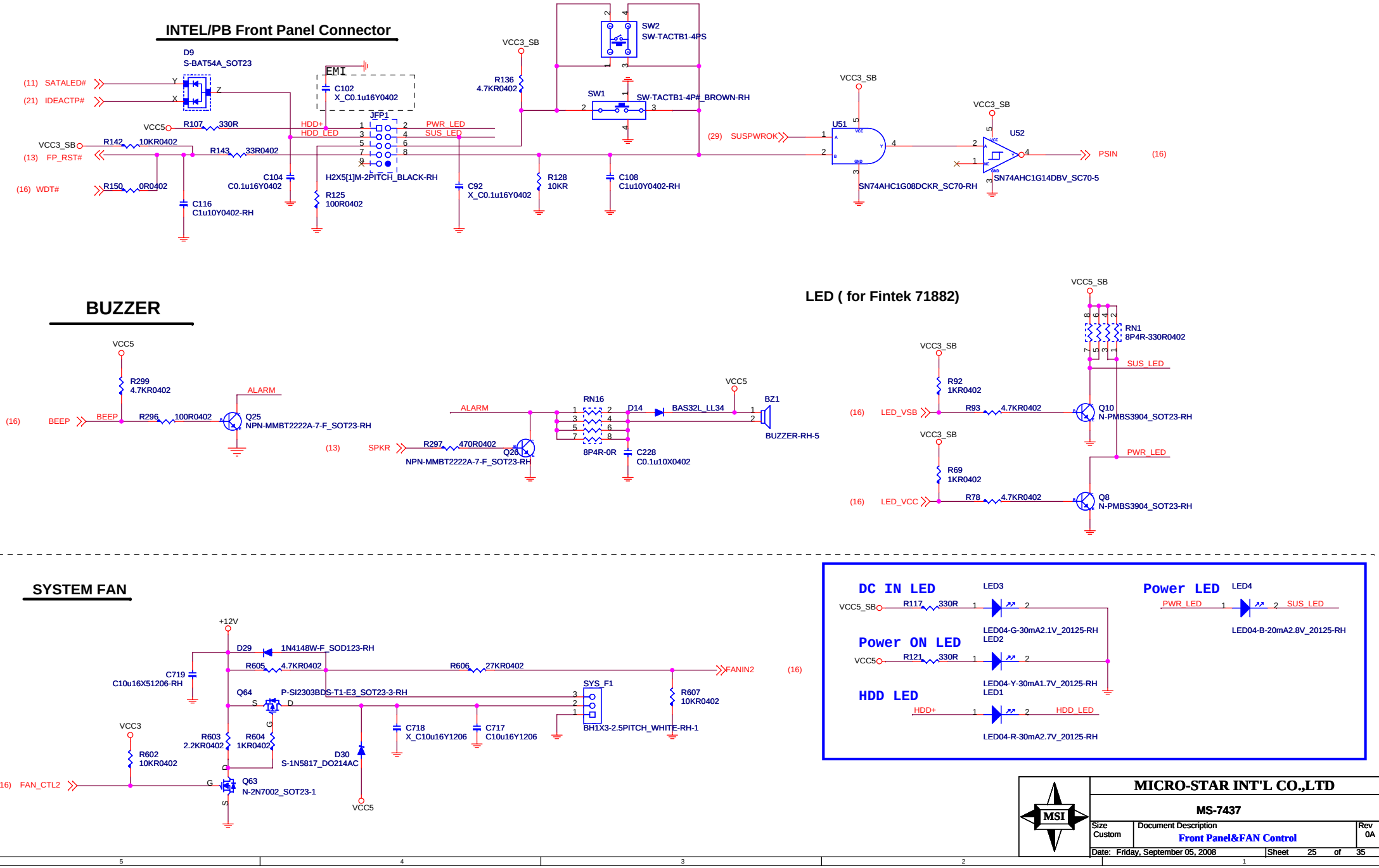
INTEL/PB Front Panel Connector
D9
S-BAT54A_SOT23
(11) SATALED#
(21) IDEACTP#
EMI
C102
X_C0.1u16Y0402
VCC5
R107 330R
HDD+
HDD_LED
JFP1
PWR_LED
SUS_LED
VCC3_SB
R142 10KR0402
(13) FP_RST#
R143 33R0402
(16) WDT#
R150 0R0402
C104
C0.1u16Y0402
C116
C1u10Y0402-RH
H2X5[1]M-2PITCH_BLACK-RH
R125
100R0402
C92
X_C0.1u16Y0402
R136
4.7KR0402
SW2
SW-TACTB1-4PS
SW1
SW-TACTB1-4P#_BROWN-RH
R128
10KR
C108
C1u10Y0402-RH
(29) SUSPWROK
U51
SN74AHC1G08DCKR_SC70-RH
U52
SN74AHC1G14DBV_SC70-5
PSIN
(16)
BUZZER
VCC5
R299
4.7KR0402
(16) BEEP
R296 100R0402
ALARM
Q25
NPN-MMBT2222A-7-F_SOT23-RH
(13) SPKR
R297 470R0402
Q26
RN16
8P4R-0R
D14
BAS32L_LL34
C228
C0.1u10X0402
BZ1
BUZZER-RH-5
LED (for Fintek 71882)
VCC5_SB
RN1
8P4R-330R0402
SUS_LED
R92
1KR0402
(16) LED_VSB
R93 4.7KR0402
Q10
N-PMBS3904_SOT23-RH
PWR_LED
R69
1KR0402
(16) LED_VCC
R78 4.7KR0402
Q8
N-PMBS3904_SOT23-RH
SYSTEM FAN
+12V
D29
1N4148W-F_SOD123-RH
C719
C10u16X51206-RH
R605 4.7KR0402
R606 27KR0402
FANIN2
(16)
Q64
P-SI2303BDS-T1-E3_SOT23-3-RH
SYS_F1
R607
10KR0402
C718
X_C10u16Y1206
C717
C10u16Y1206
BH1X3-2.5PITCH_WHITE-RH-1
R603
2.2KR0402
R604
1KR0402
D30
S-1N5817_DO214AC
R602
10KR0402
(16) FAN_CTL2
Q63
N-2N7002_SOT23-1
DC IN LED
LED3
R117 330R
LED04-G-30mA2.1V_20125-RH
Power ON LED
LED2
R121 330R
LED04-Y-30mA1.7V_20125-RH
HDD LED
LED1
LED04-R-30mA2.7V_20125-RH
Power LED
LED4
LED04-B-20mA2.8V_20125-RH
MICRO-STAR INT'L CO.,LTD
MS-7437
Size
Custom
Document Description
Front Panel&FAN Control
Rev
0A
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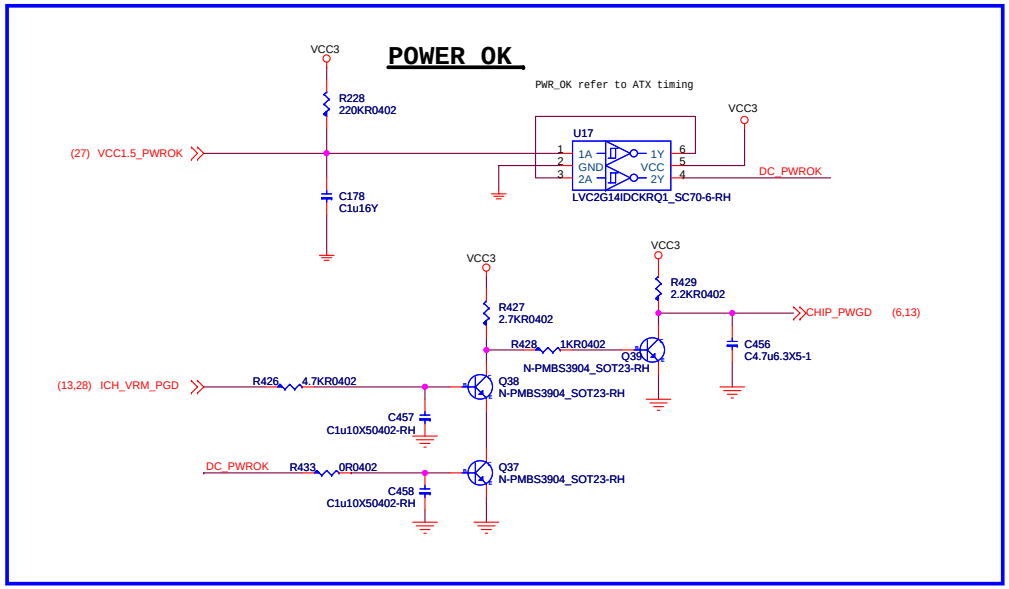

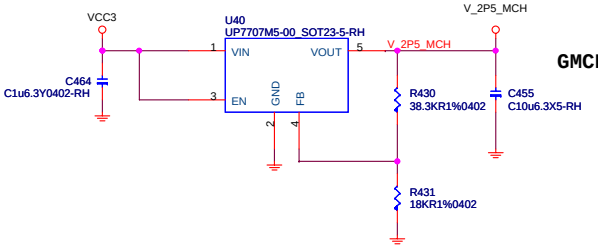

V_2P5_MCH 142mA

GMCH:70mA+2mA+10mA+60mA=142mA

UP7707 Spec 600mA

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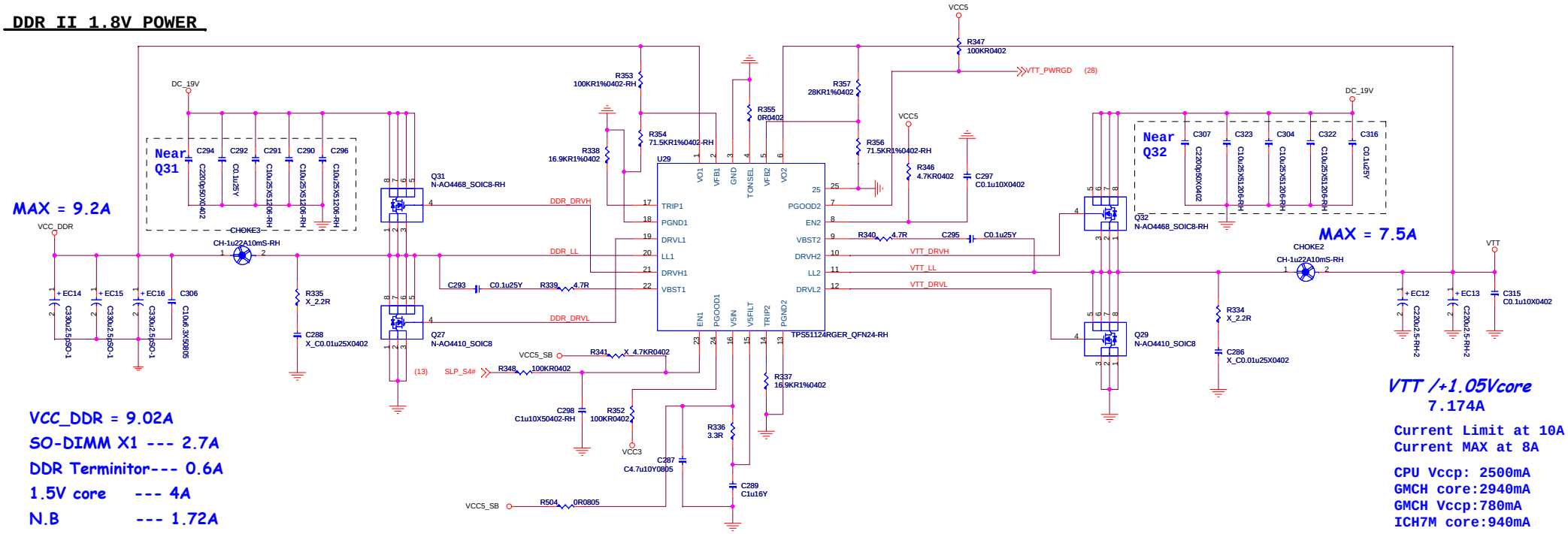
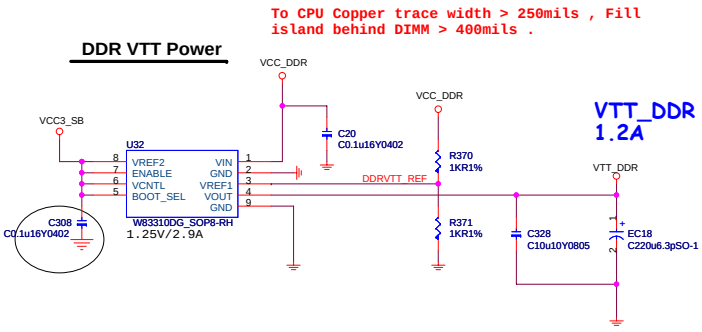
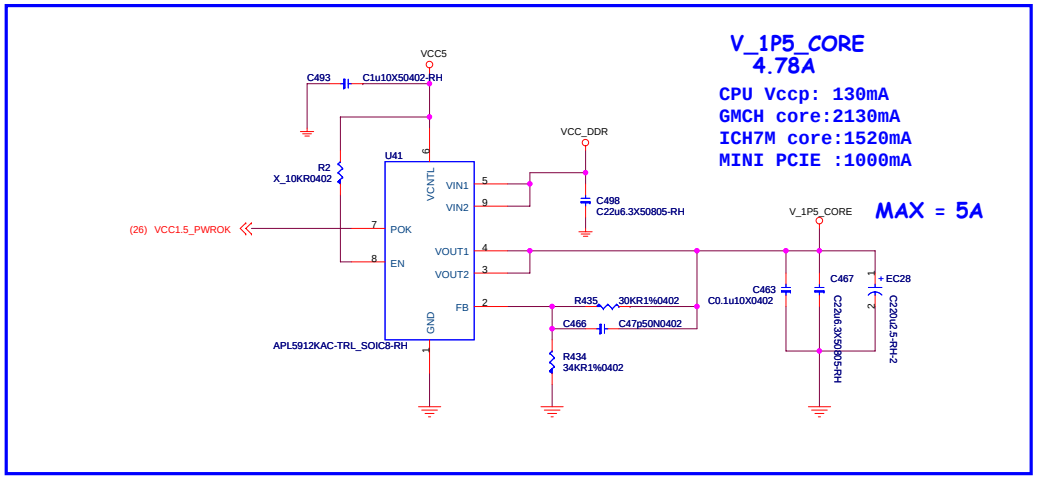
DDR II 1.8V POWER







MICRO-STAR INT'L CO.,LTD	
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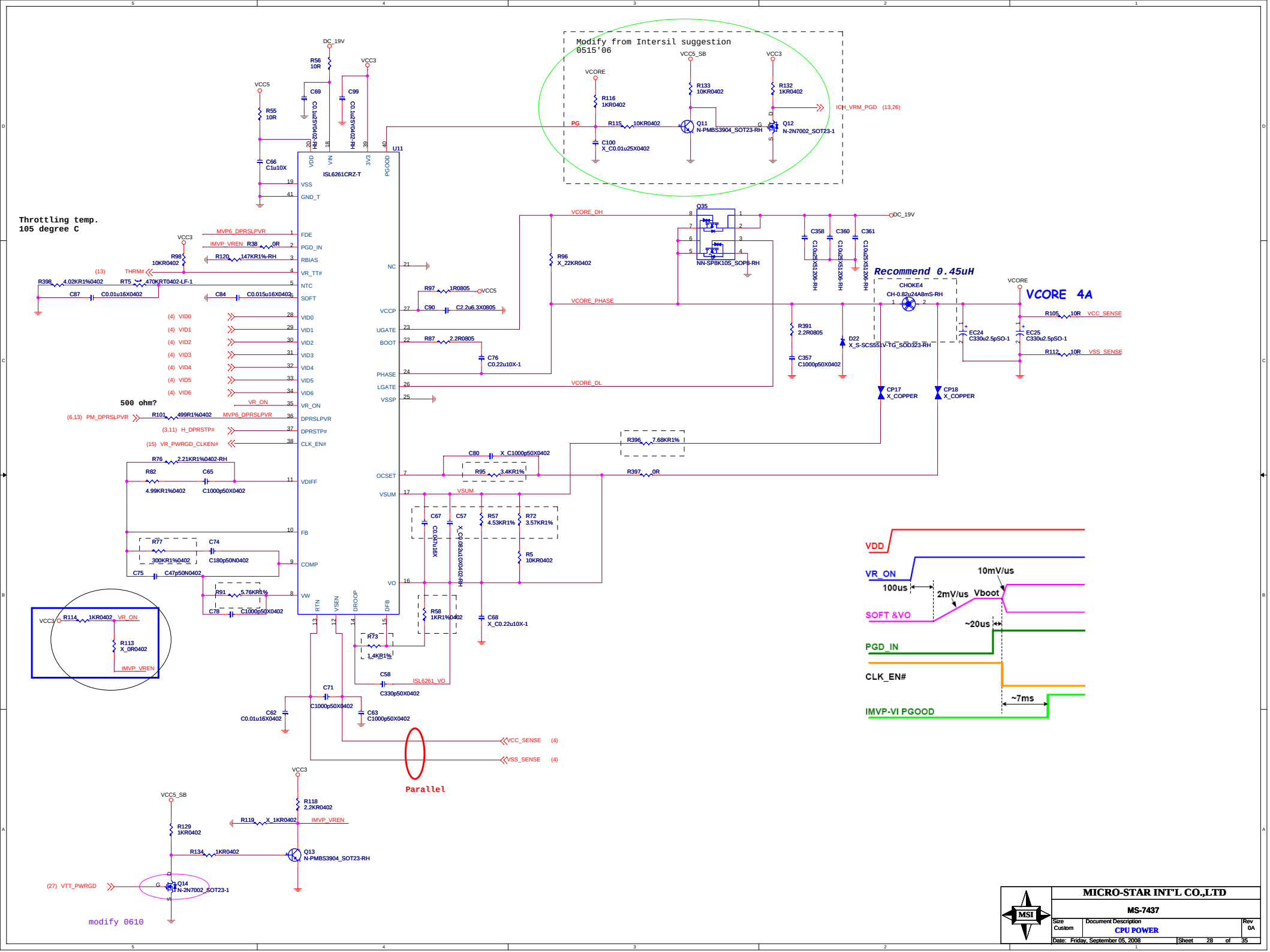
Modify from Intersil suggestion
0515'06
Throttling temp.
105 degree C
500 ohm?
Recommend 0.45uH
VCORE 4A
ISL6261CRZ-T
U11
Q35
NN-SP8K10S_SOP8-RH
CHOKE4
CH-0.82u24A8mS-RH
D22
X_S-SCS551V-TG_SOD323-RH
Q11
N-PMBS3904_SOT23-RH
Q12
N-2N7002_SOT23-1
Q13
N-PMBS3904_SOT23-RH
Q14
N-2N7002_SOT23-1
Parallel
modify 0610
VDD
VR_ON
100us
2mV/us
Vboot
10mV/us
SOFT &VO
~20us
PGD_IN
CLK_EN#
~7ms
IMVP-VI PGOOD
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CPU POWER
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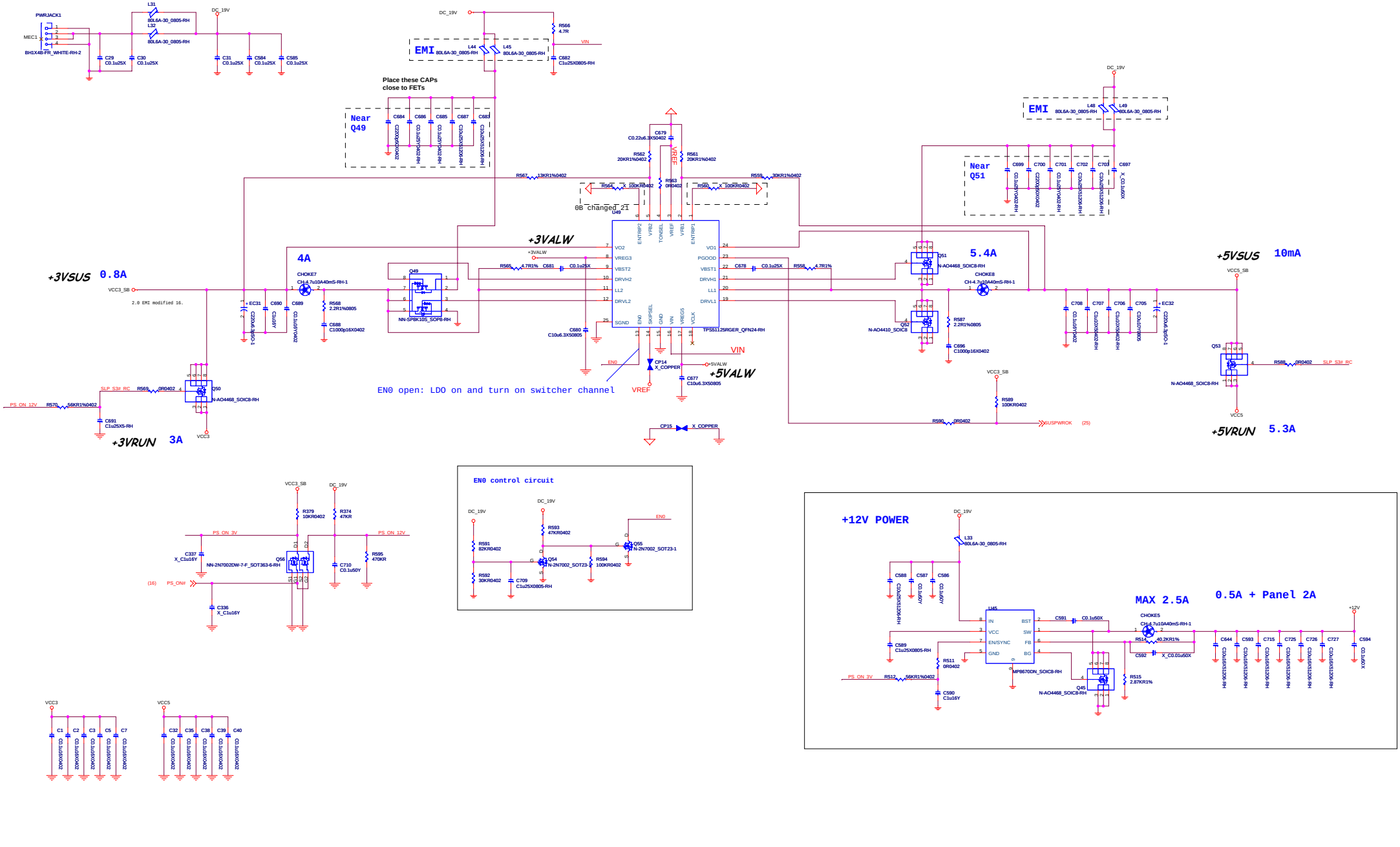

PWRJACK1
DC_19V
EMI
Place these CAPs close to FETs
Near Q49
Near Q51
0B changed 21
+3VALW
+3VSUS 0.8A
4A
+3VRUN 3A
5.4A
+5VSUS 10mA
+5VRUN 5.3A
+5VALW
VIN
VREF
EN0 open: LDO on and turn on switcher channel
TPS51125RGER_QFN24-RH
EN0 control circuit
+12V POWER
MAX 2.5A
0.5A + Panel 2A
MICRO-STAR INT'L CO.,LTD
MS-7437
DC-IN POWER

PCB1
PCB-7437-0A

BAT1
BAT-BT-CR2032-RH
RTC Battery

NB HEATSINK

H3 H4

CPU HEATSINK

HS2
HS-0800770-RH

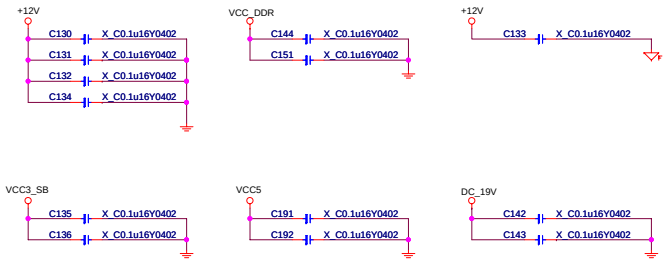
CPU HEATSINK

HS1
HS-0800770-RH

SB HEATSINK

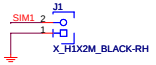
HS3
HS-0800770-RH

EMI

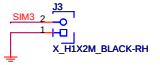


Simulation

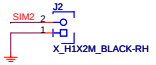
Layer1 / 5mil / 55ohm



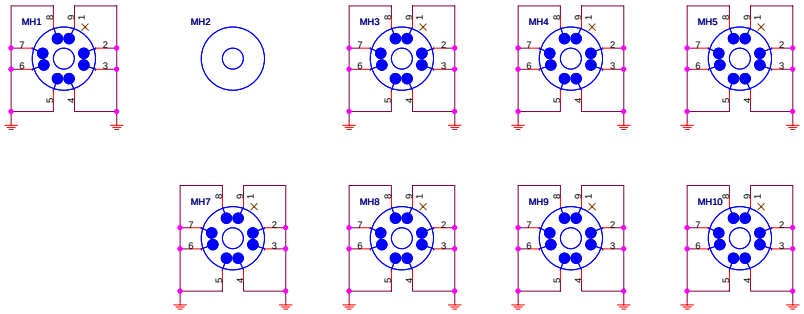
Layer6 / 5mil / 55ohm



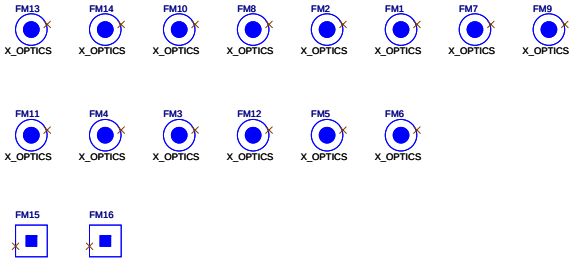
Layer4 / 4.5mil / 55ohm



Mounting Holes



Optics Orientation Holes



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ICH7M

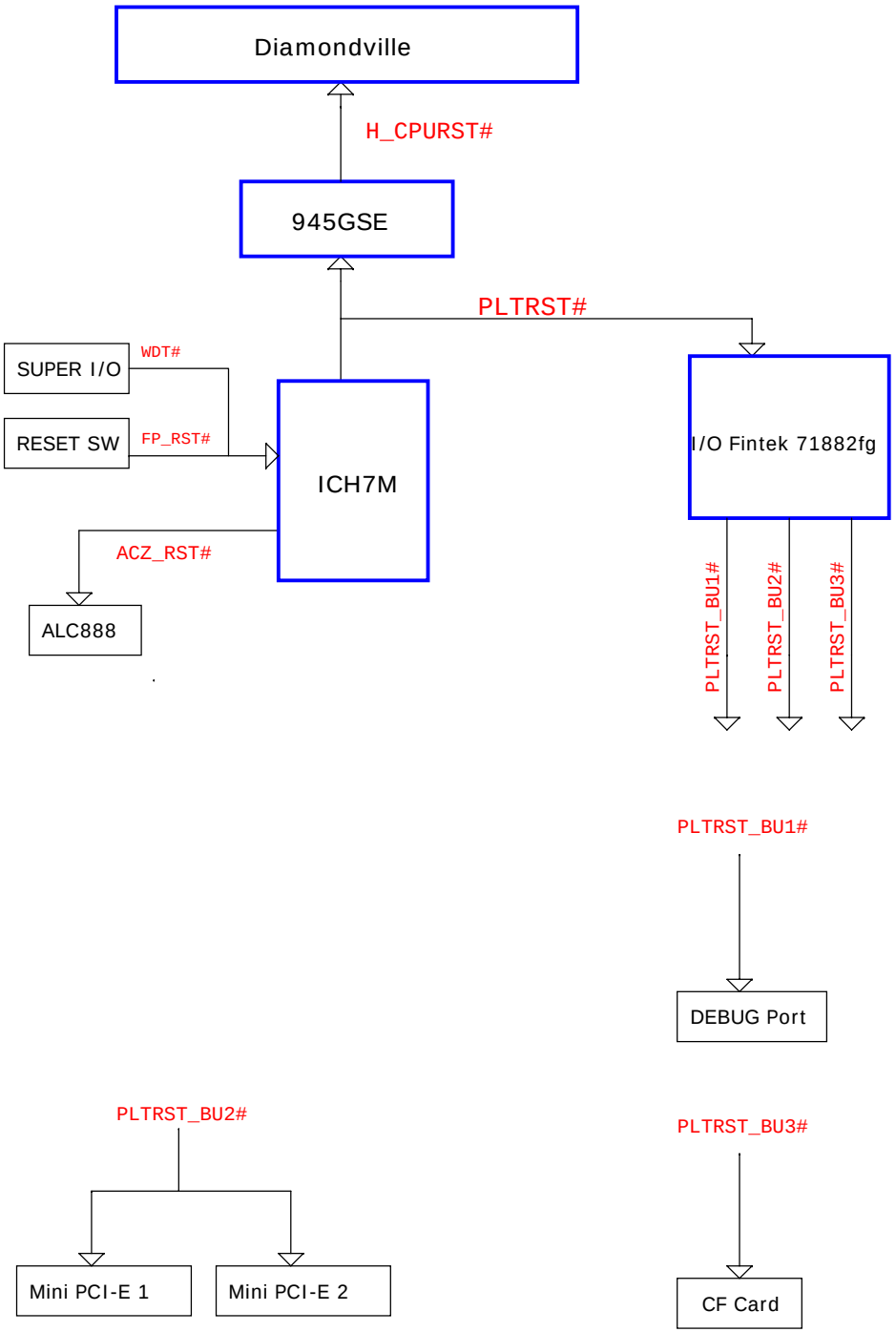
GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Rickles Signal Name
GPIO[0]	BM_BUSY#	AB18	I	VCC3p3	N	Y	3.3	N/A	PM_BMBUSY#
GPIO[1]	REQ[5]#	C8	I	V5REF	Y	N	5	N/A	PREQ#5
GPIO[2]	PIRQE#	G8	I	V5REF	Y	N	5	N/A	GPIO2
GPIO[3]	PIRQF#	F7	I	V5REF	Y	N	5	N/A	GPIO3
GPIO[4]	PIRQG#	F8	I	V5REF	Y	N	5	N/A	GPIO4
GPIO[5]	PIRQH#	G7	I	V5REF	Y	N	5	N/A	GPIO5
GPIO[6]	unmuxed	AC21	I	Vcc3p3	Y	Y	3.3	N/A	ATADET0
GPIO[7]	unmuxed	AC18	I	Vcc3p3	Y	N	3.3	N/A	SIO_OVT#
GPIO[8]	unmuxed	E21	I	VccSus3p3	Y	Y	3.3	N/A	NC
GPIO[9]	unmuxed	E20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[10]	unmuxed	A20	I	VccSus3p3	Y	N	3.3	N/A	NC
GPIO[11]	SMBALERT#	B23	I	VccSus3p3	Y	Y	3.3	N/A	SMBALERT#
GPIO[12]	unmuxed	F19	I	VccSus3p3	Y	N	3.3	N/A	SPI_HOLD_GPO#
GPIO[13]	unmuxed	E19	I	VccSus3p3	Y	Y	3.3	N/A	SIO_PME#
GPIO[14]	unmuxed	R4	I	VccSus3p3	Y	Y	3.3		NC
GPIO[15]	unmuxed	E22	I	VccSus3p3	N	N	3.3	1	NC
GPIO[16]	DPRSLPVR	AC22	O	Vcc3p3	N	N	3.3	1	DPRSLPVR
GPIO[17]	GNT[5]#	D8	O	Vcc3p3	N	N	3.3	1	PGNT#5
GPIO[18]	STPPCI#	AC20	O	Vcc3p3	N	N	3.3	1	PM_STPPCI#
GPIO[19]	SATA1GP	AH18	I	Vcc3p3	D	N	3.3	1	SATA1GP
GPIO[20]	STPCPU#	AF21	O	Vcc3p3	N	N	3.3	O	PM_STPCPU#
GPIO[21]	SATA0GP	AF19	I	Vcc3p3	N	N	3.3	0	SATA0GP
GPIO[22]	REQ4#	A13	I	Vcc3p3	N	N	3.3	0	PREQ#4
GPIO[23]	LDRQ1#	AA5	O	Vcc3p3	N	N	3.3		NC
GPIO[24]	unmuxed	B3	O	VccSus3p3	Y	N	3.3	1	BIOS_WP#
GPIO[25]	unmuxed	D20	O	VccSus3p3	N	N	3.3	N/A	CAMERA_ON#
GPIO[26]	unmuxed	A21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#5	C3	I	VccsUS3p3	Y	N	3.3		USB_OCP#2
GPIO[30]	OC#6	A2	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[31]	OC#7	B3	I	VccsUS3p3	Y	N	3.3		USB_OCP#3
GPIO[32]	CLKRUN#	AG18	O	Vcc3p3	N	N	3.3	1	CLKRUN#
GPIO[33]	AZ_DOCK_EN#	AC19	O	Vcc3p3	N	N	3.3	1	PRES2
GPIO[34]	AZ_DOCK_RST#	U2	O	Vcc3p3	N	N	3.3	0	PRES3
GPIO[35]	SATACLKREQ#	AD21	O	Vcc3p3	N	N	3.3	0	PRES1
GPIO[36]	SATA2GP	AH19	I	Vcc3p3	N	N	3.3	0	SATA2GP
GPIO[37]	SATA3GP	AE19	I	Vcc3p3	N	N	3.3	0	SATA3GP
GPIO[38]	unmuxed	AD20	I	Vcc3p3	Y	N	3.3	1	NC
GPIO[39]	unmuxed	AE20	I	Vcc3p3	Y	N	3.3	1	WLAN_PWRON
GPIO[48]	GNT4#	A14	O	Vcc3p3	N	N	3.3	1	PGNT#4
GPIO[49]	CPUPWRGD	AG24	OD	V_FSB_VTT	Y	N	3.3	1	CPU_PWRGD

SIO(F71882)

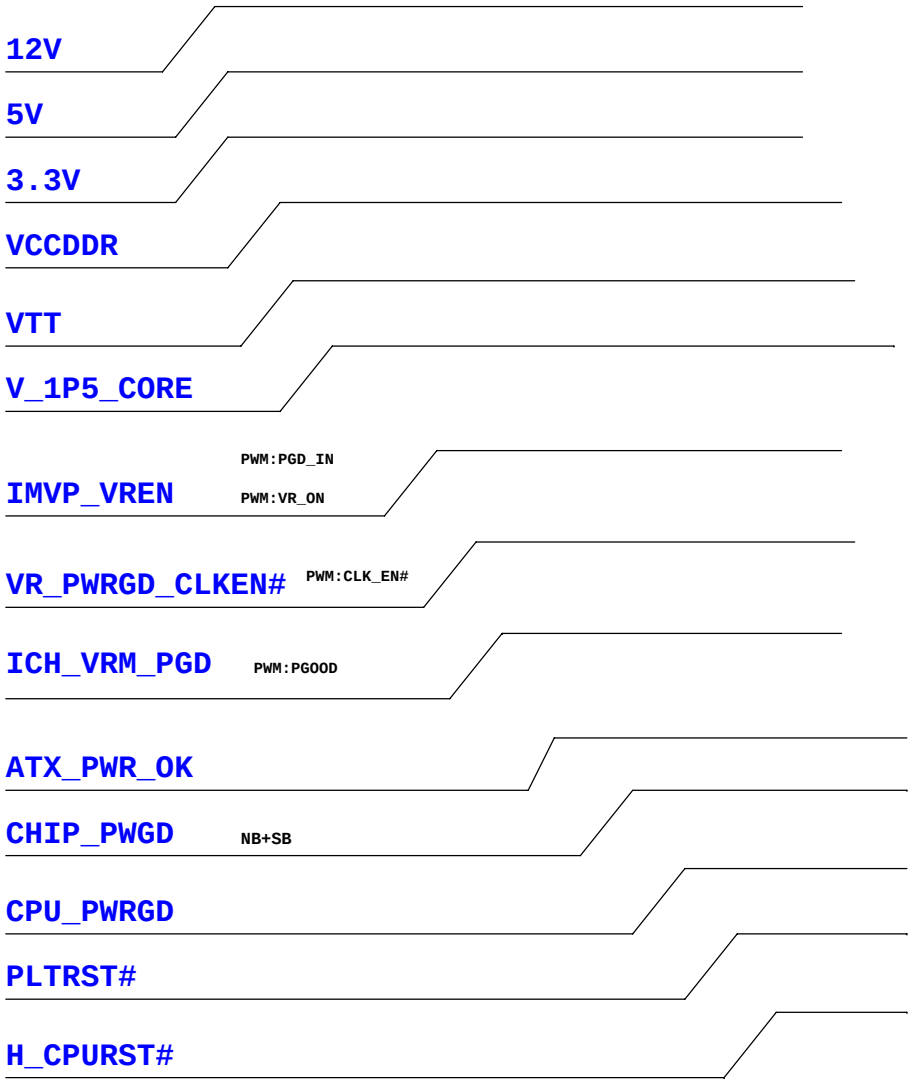
PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	UNUSED		
GPIO3	UNUSED		
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	UNUSED		
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	AMP_EN	OUTPUT	RESERVED TO ENABLE THE AMPLIFIER
GPIO15	LED_VSB	OUTPUT	OUTPUT FOR PWR LED
GPIO16	LED_VCC	OUTPUT	OUTPUT FOR PWR LED
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESET BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESET BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESET BUFFER3
GPIO23	UNUSED		
GPIO24	UNUSED		
GPIO26	PSIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PSOUT#	OUTPUT	POWER BUTTON BUFFER OUT TO SB
GPIO30	SLP_S3#	INPUT	FROME SOUTHBRIDGE S3#
GPIO31	PS_ON#	OUTPUT	OUTPUT FOR POWER ON
GPIO32	UNUSED		
GPIO33	RSMRST#	OUTPUT	OUTPUT FOR SOUTRHBRIDGE RSMRST#
GPIO40	AMP_GAIN0	OUTPUT	SET AMPLIFIER GAIN
GPIO41	UNUSED		
GPIO42	UNUSED		
GPIO43	AMP_GAIN1	OUTPUT	SET AMPLIFIER GAIN

DDR-II DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	SM_CK0/#0	SM_CK1/#1



Power Sequence



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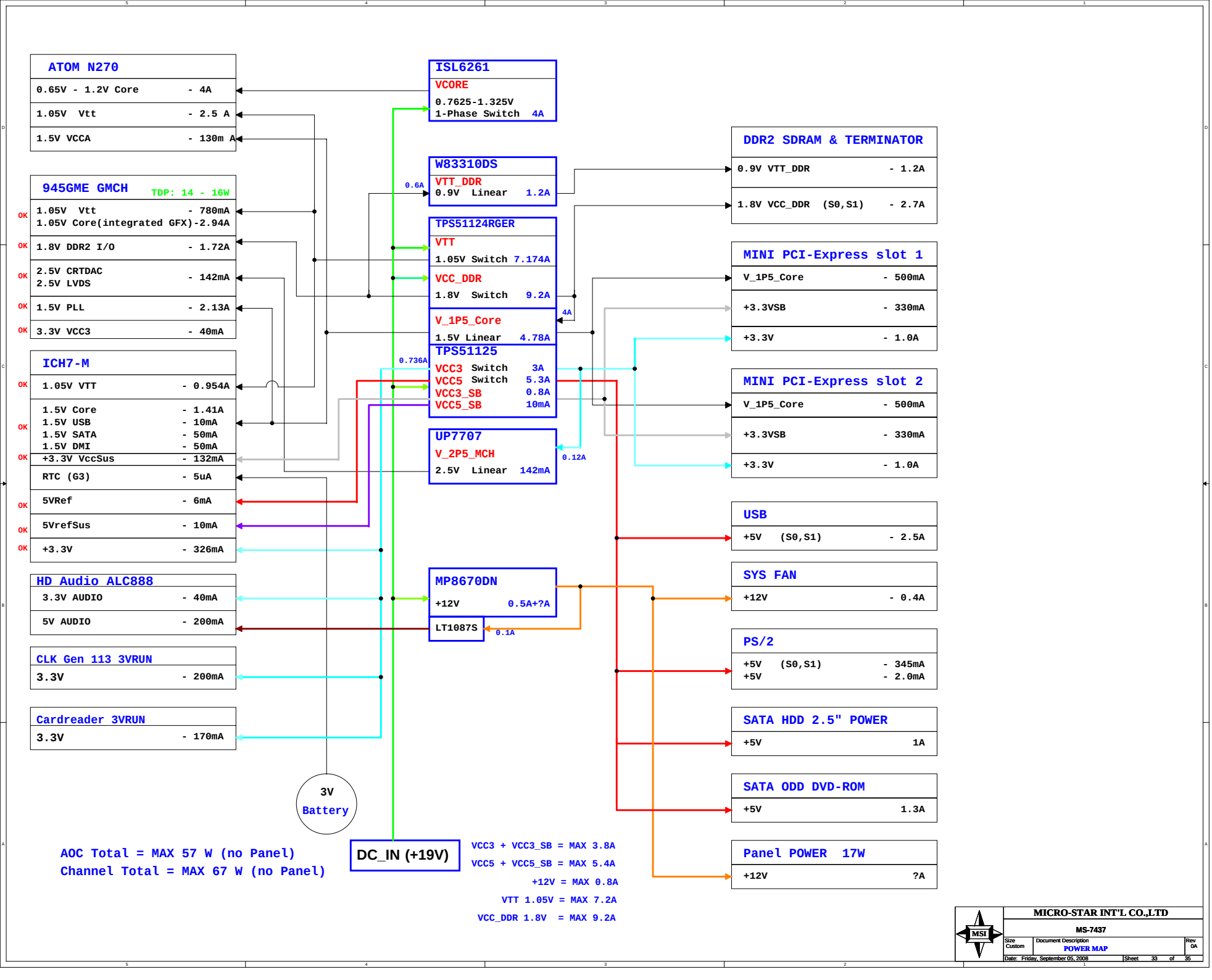

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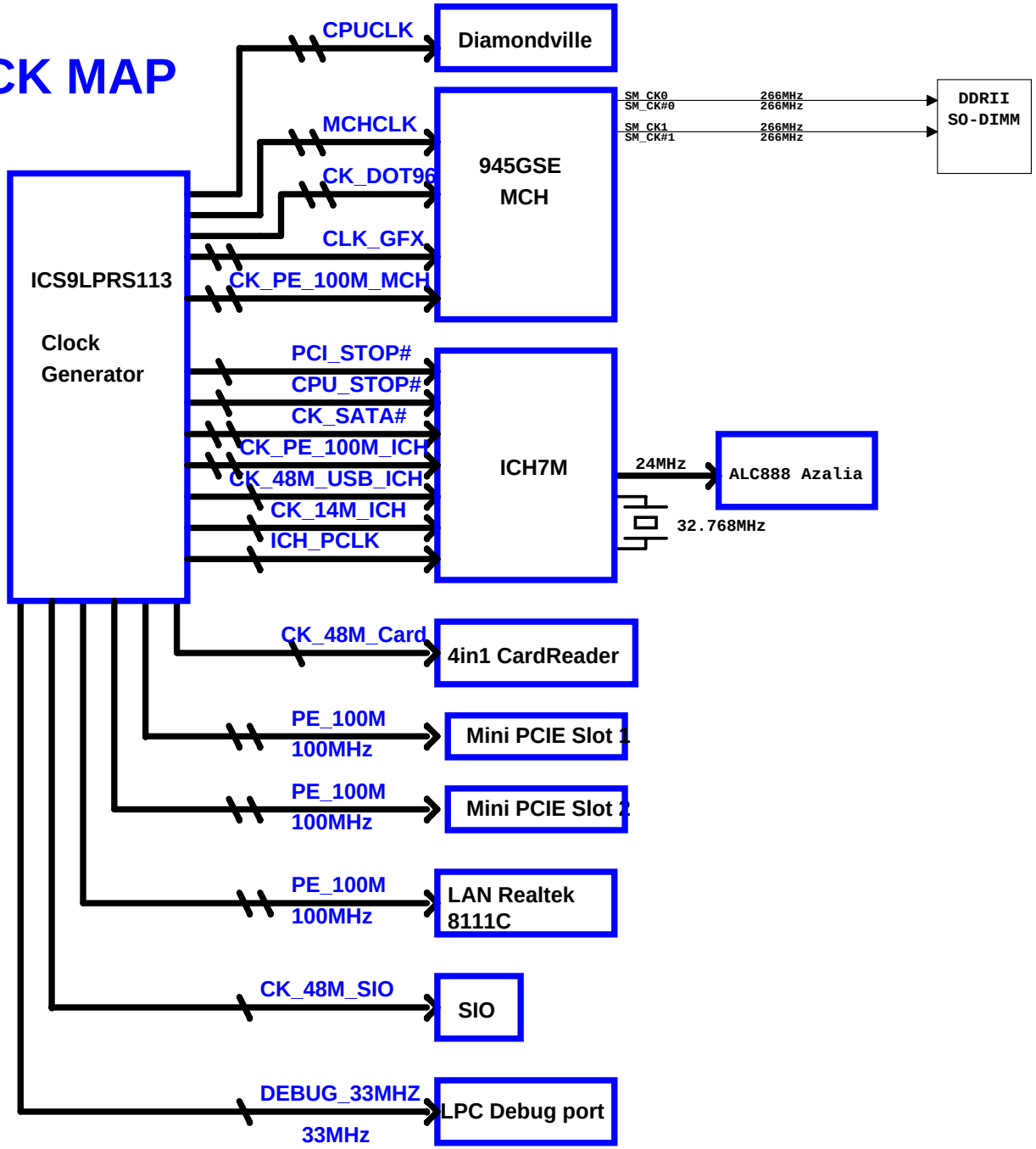
CLOCK MAP



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