MS-7436 (MS-6631)

Version 0A

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)
Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- SPI
LAN -- Realtek RTL8111C
Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)
CF Card Connector for flash Memory

Expansion Slots:

Internal Mini PCIE x1

Intersil PWM:

Controller: 6314

MSI

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Title	COVER SHEET	
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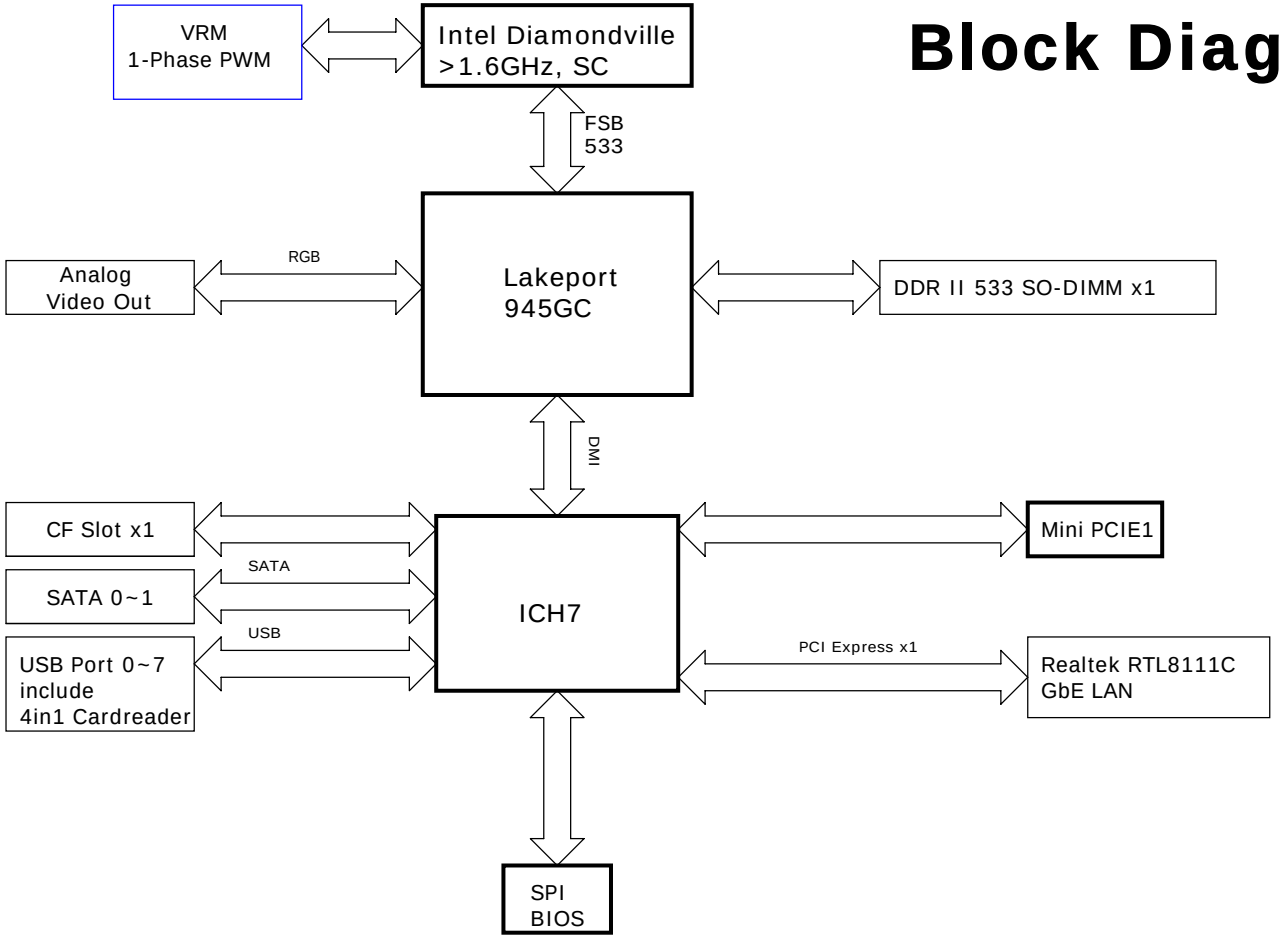
Block Diagram



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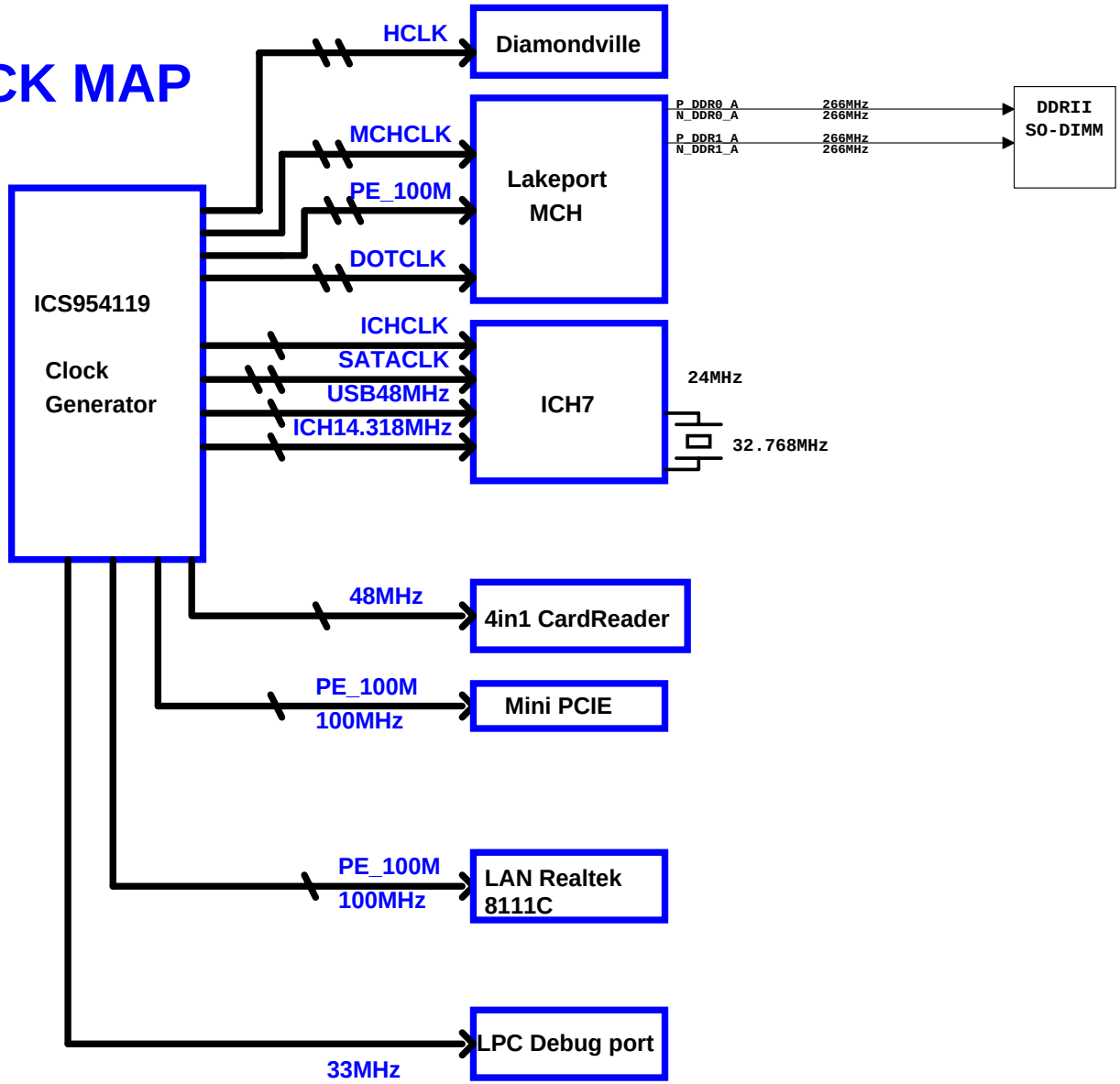
Title: BLOCK DIAGRAM		
Size: A3	Document Number: MS-7436	Rev: 0A
Date: Thursday, August 14, 2008	Sheet 2 of 31	

CLOCK MAP



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Title: CLOCK MAP		
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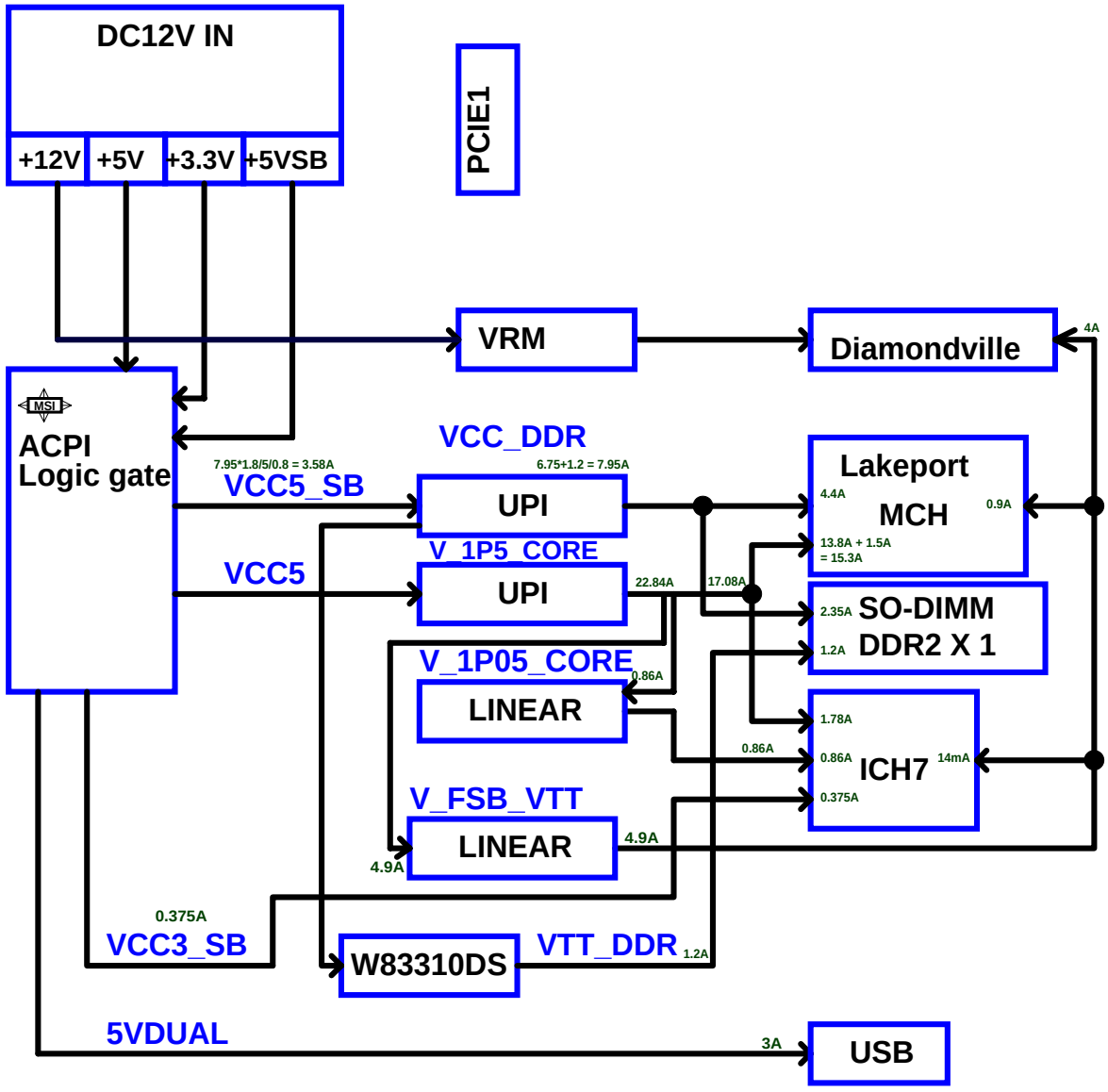
POWER MAP



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ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	ATADET0	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	GPI7	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	NC
GPIO[25]	S1_3_LED	D20	I/O	VccSus3p3	Y	N	3.3	1	pull high VCC3 SB
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

SIGNAL	DEVICE
MiniPCIeRST#	MINI PCIE SLOT
TPMRST#	TPM
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
CF_RST#	CF_CARD
H_CPURST#	CPU
FWHRST#	LPT Debug port
MCHRST#	MCH

SMBCLK, SMBDATA	DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR

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Title: GPIO MAP

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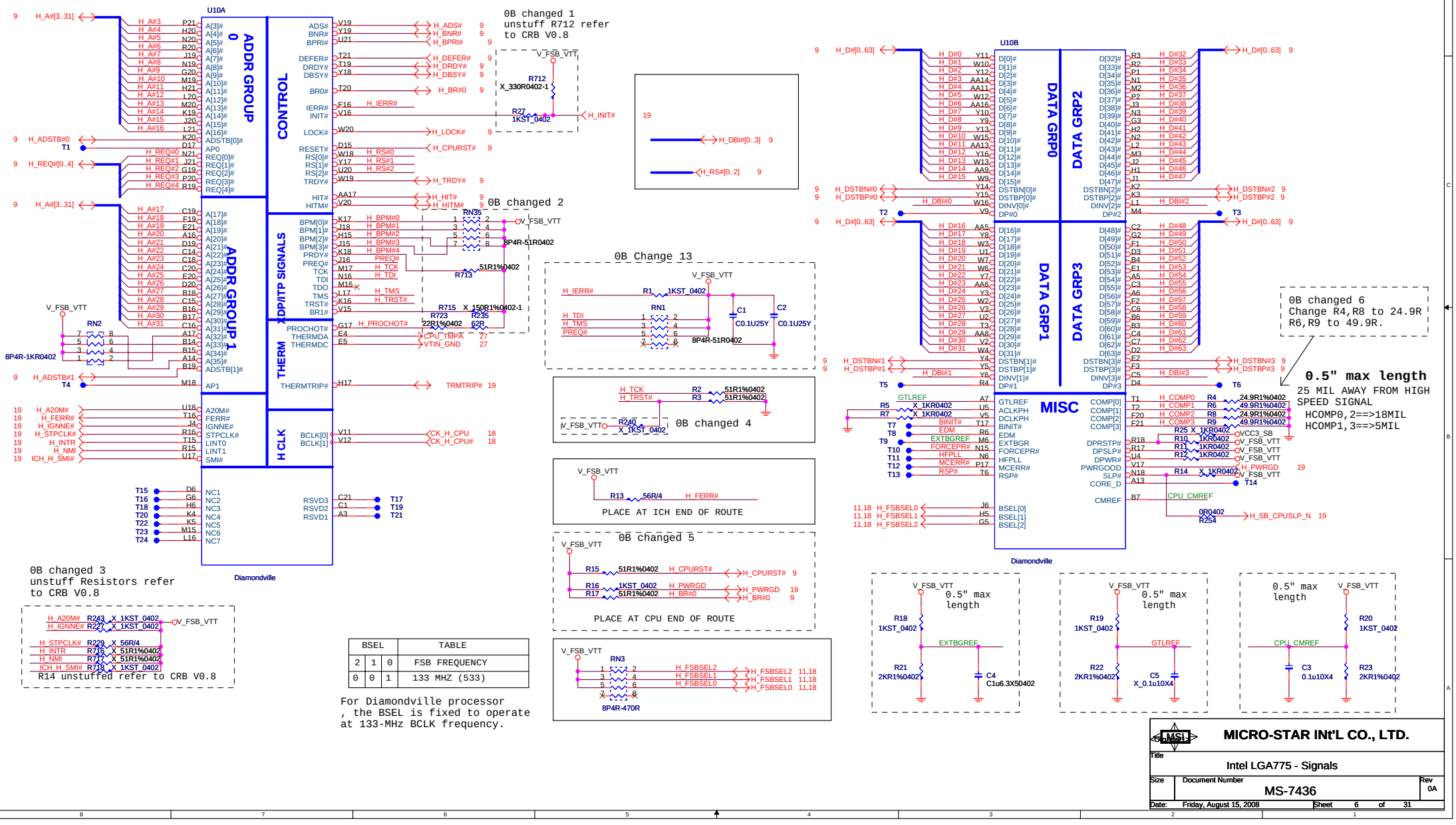
CPU SIGNAL BLOCK



BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	1	133 MHZ (533)

Title	Intel LGA775 - Signals
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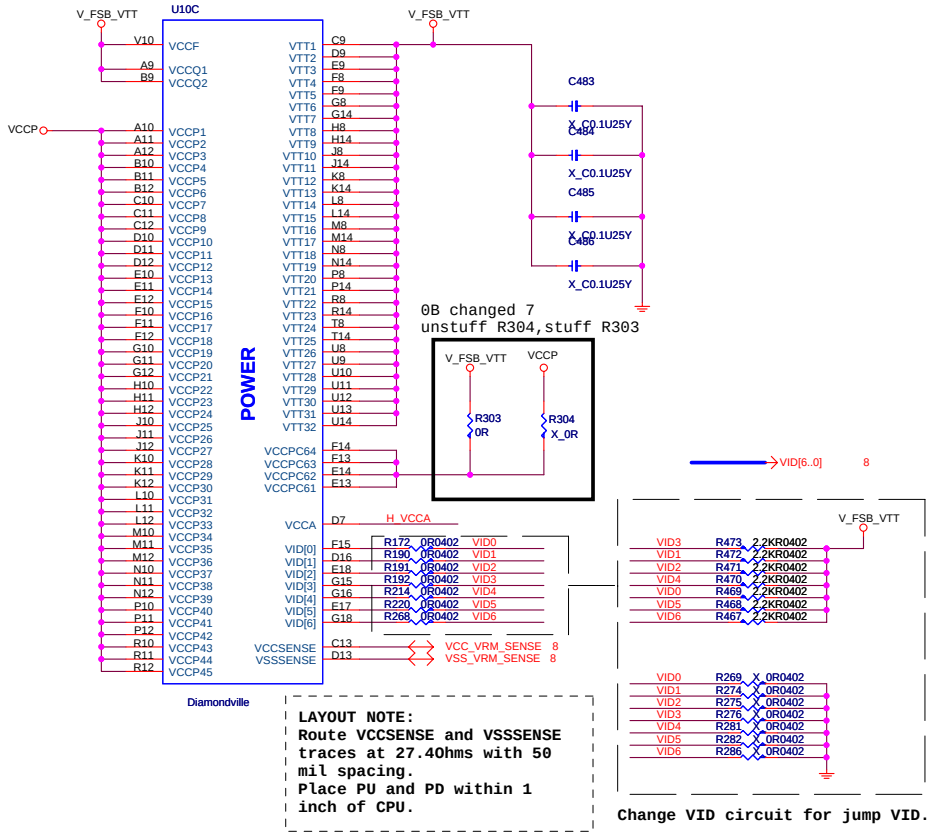
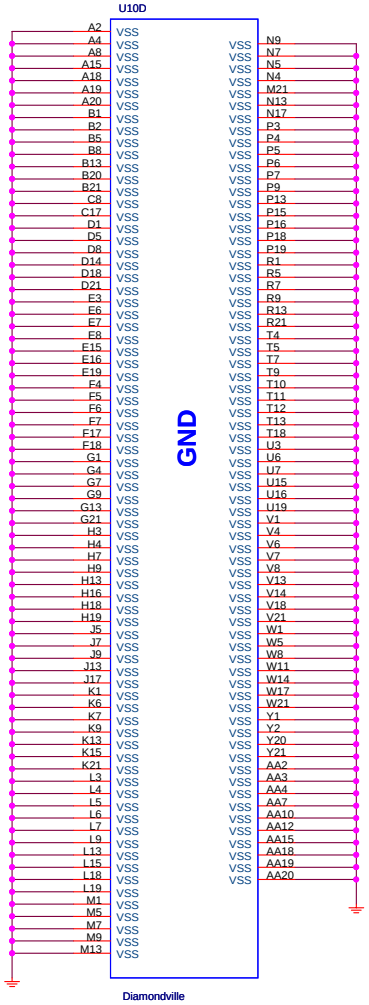
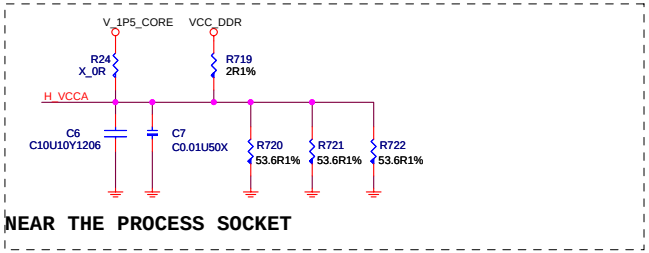
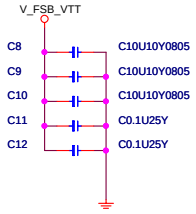




0B changed 8-->change pull up circuit follow CRB V0.7.





CAPS FOR FSB GENERIC

2.5A: before VCC stable
1.5A: after VCC stable

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Title: Intel LGA775 - Power

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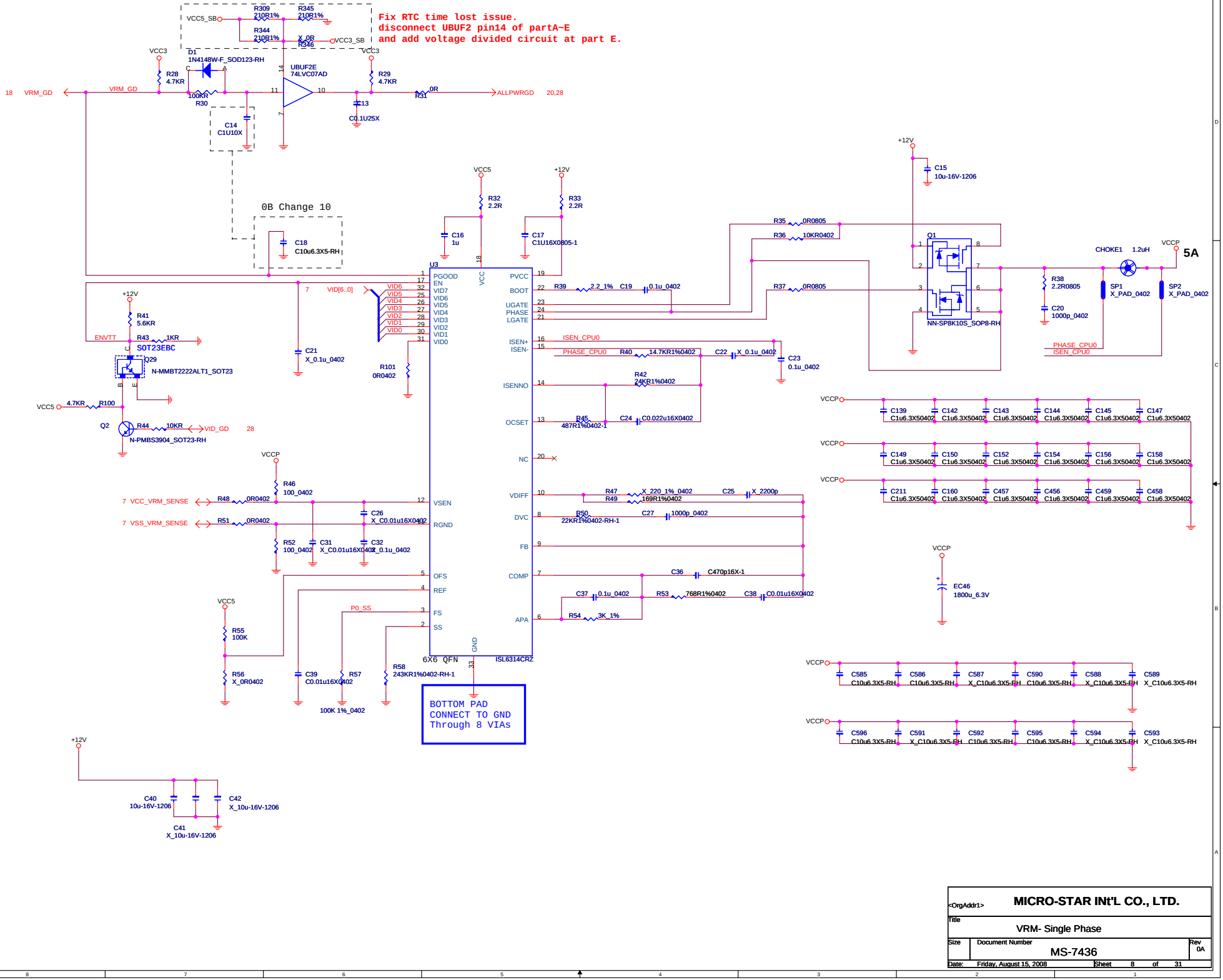
Fix RTC time lost issue.
disconnect UBUF2 pin14 of partA~E
and add voltage divided circuit at part E.
0B Change 10
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
U3
ISL6314CR2
6X6 QFN
NN-SP8K10S_SOP8-RH
N-MMBT2222ALT1_SOT23
N-PMBS3904_SOT23-RH
UBUF2E
74LVC07AD
1N4148W-F_SOD123-RH
SOT23EBC
MICRO-STAR INt'L CO., LTD.
<OrgAddr1>
VRM- Single Phase
MS-7436
Rev 0A
Friday, August 15, 2008
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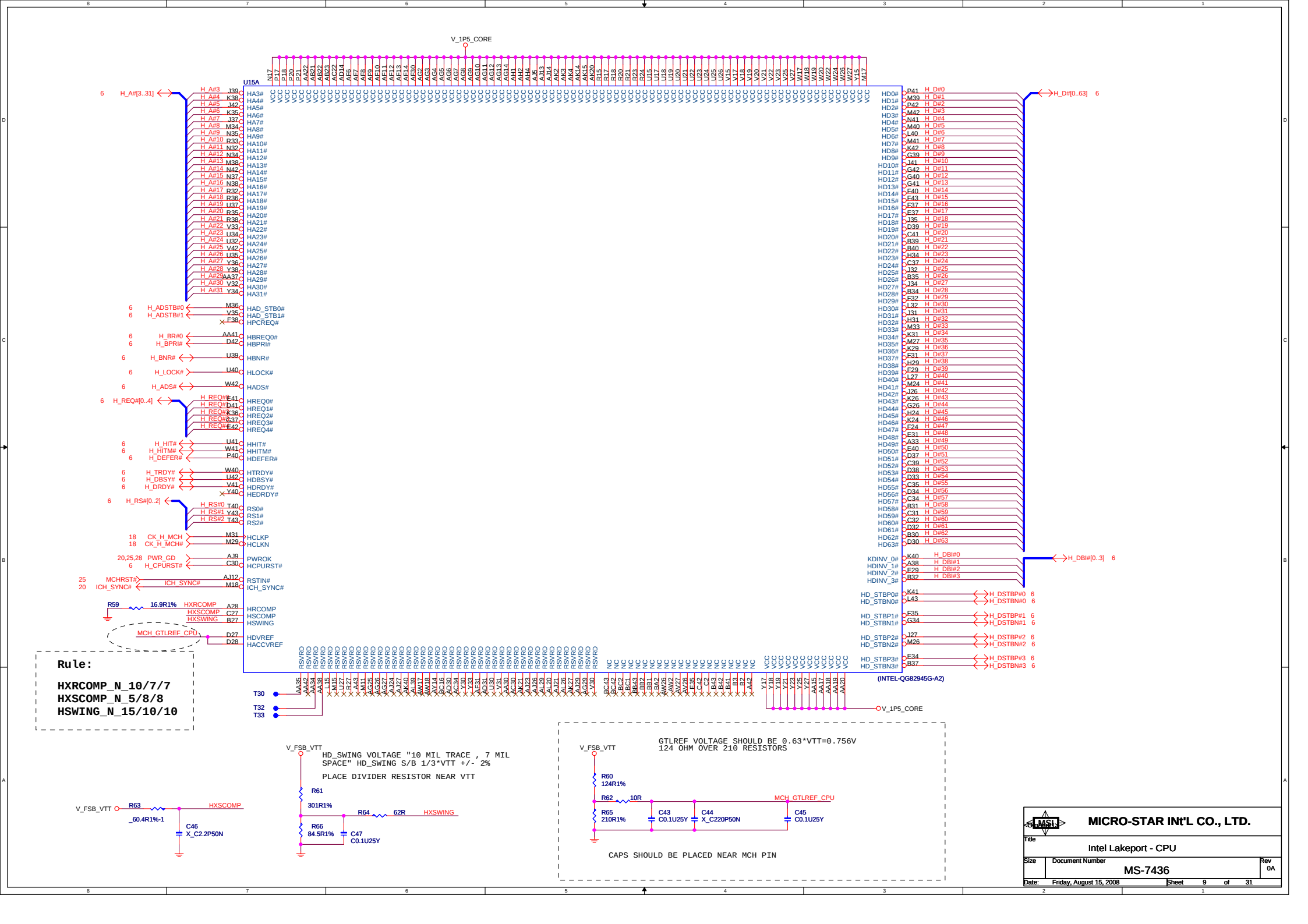
V_1P5_CORE
U15A
H_A#[3..31]
H_D#[0..63]
H_DBI#[0..3]
H_ADSTB#0
H_ADSTB#1
H_BR#0
H_BPRI#
H_BNR#
H_LOCK#
H_ADS#
H_REQ#[0..4]
H_HIT#
H_HITM#
H_DEFER#
H_TRDY#
H_DBSY#
H_DRDY#
H_RS#[0..2]
CK_H_MCH
CK_H_MCH#
PWR_GD
H_CPURST#
MCHRST#
ICH_SYNC#
R59
16.9R1%
HXRCOMP
HXSCOMP
HXSWING
MCH_GTLREF_CPU
(INTEL-QG82945G-A2)
Rule:
HXRCOMP_N_10/7/7
HXSCOMP_N_5/8/8
HSWING_N_15/10/10
V_FSB_VTT
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/3*VTT +/- 2%
PLACE DIVIDER RESISTOR NEAR VTT
R61
301R1%
R64
62R
R66
84.5R1%
C47
C0.1U25Y
R63
_60.4R1%-1
C46
X_C2.2P50N
GTLREF VOLTAGE SHOULD BE 0.63*VTT=0.756V
124 OHM OVER 210 RESISTORS
R60
124R1%
R62
10R
R65
210R1%
C43
C0.1U25Y
C44
X_C220P50N
C45
C0.1U25Y
CAPS SHOULD BE PLACED NEAR MCH PIN
MICRO-STAR INt'L CO., LTD.
Intel Lakeport - CPU
MS-7436
Friday, August 15, 2008
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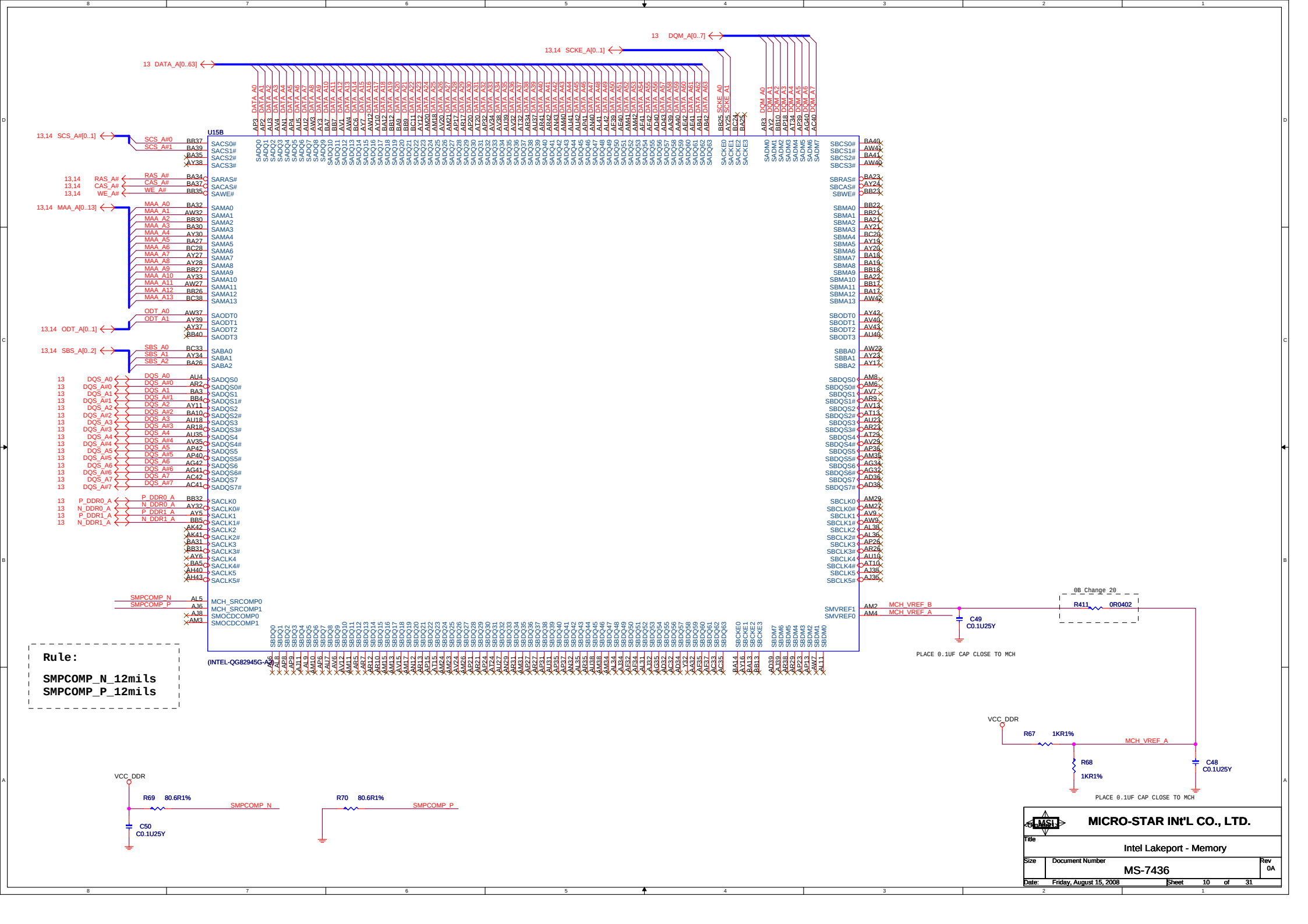

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Title	Intel Lakeport - Memory	
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EXP_EN: PCI Express* SDVO Concurrent Select

0: Only SDVO or PCI-E Operational

1: SDVO and PCI-E operating simultaneously via PCI Express-G port

EXP_SLR: PCI Express Static Lane Reversal

0: BTX 1: ATX

MCH MEMORY DECOUPLING

CLOSE TO GMCH

Rule:15-mil

FSB GENERIC DECOUPLING

I = 70mA

I = 60mA

I = 55mA

I = 45mA

I = 55mA

I = 45mA

I = 1.5A

Title	Intel Lakeport - PCI EXPRESS
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MSI	MICRO-STAR INt'L CO., LTD.		
Title	Intel Lakeport - GND		
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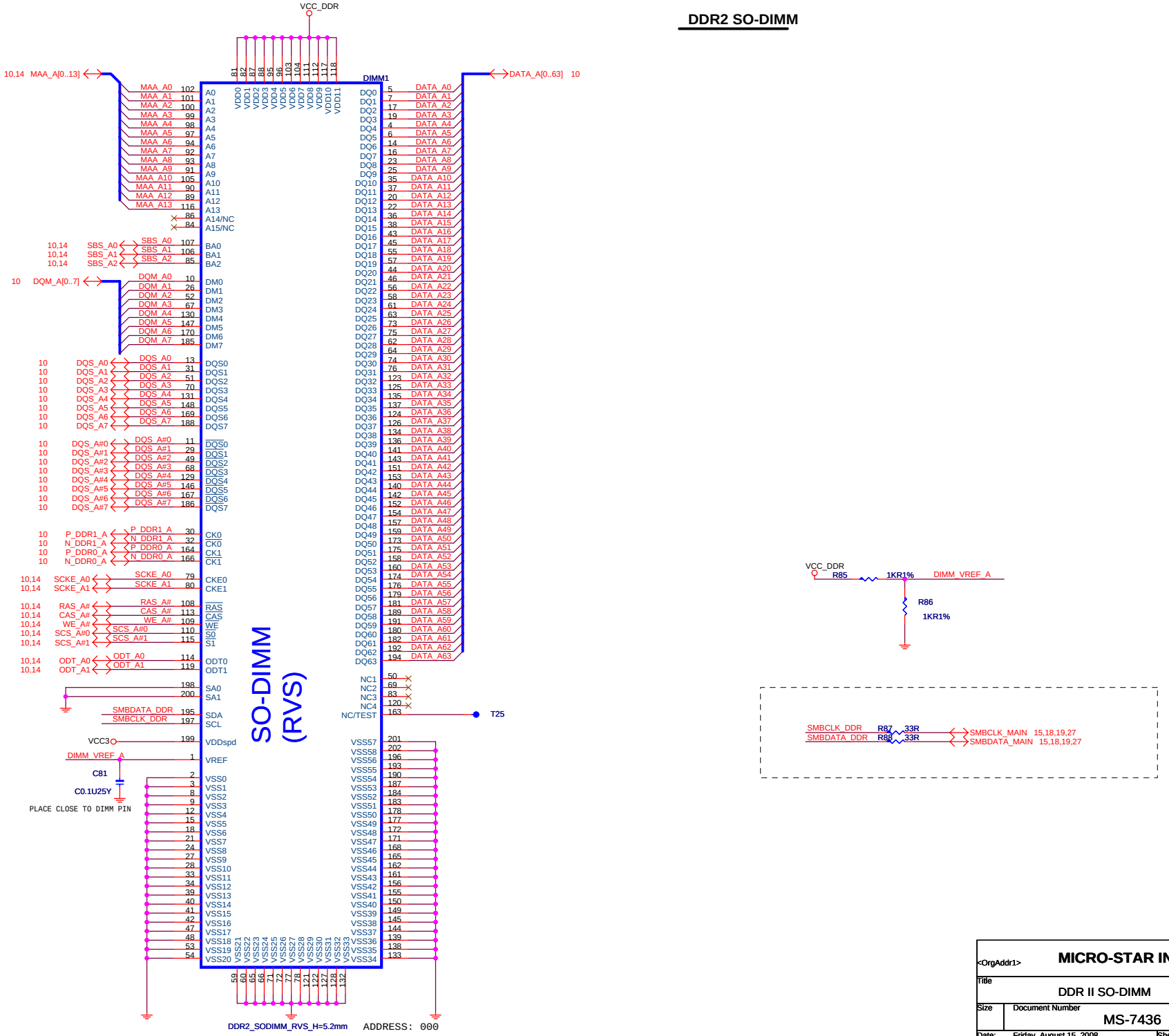
DDR2 SO-DIMM



<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	DDR II SO-DIMM	
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CHANNEL A V_SM_VTT
DECOULPING CAPS

CHANNEL B V_SM_VTT
DECOULPING CAPS

SCS_A#0 change 43 ohm

Grantsdale GMCH Power Sequencing
Requirement Between 1.5V Core and 2.5V DAC

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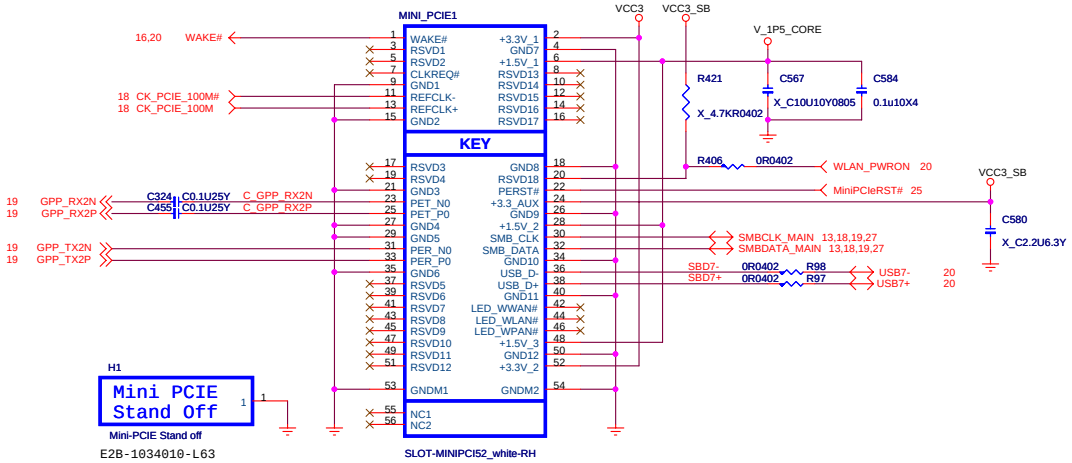
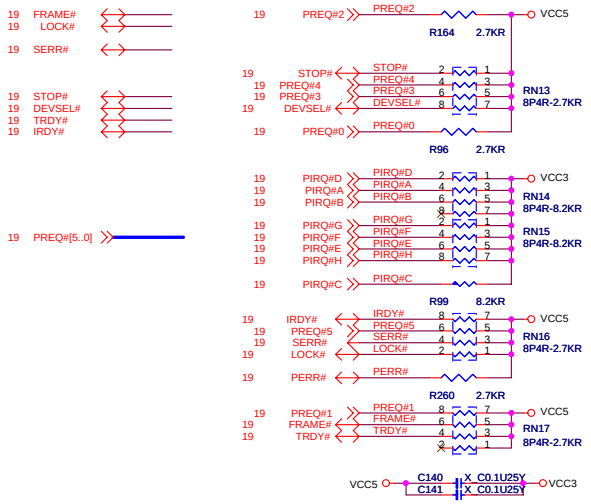
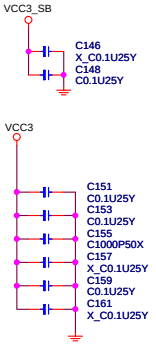


PCI PULL-UP / DOWN RESISTORS



DECOUPLING CAPACITORS



MICRO-START INT'L CO.,LTD.		
Title: Mini PCI Slot		
Size: Custom	Document Number: MS-7436	Rev: 0A
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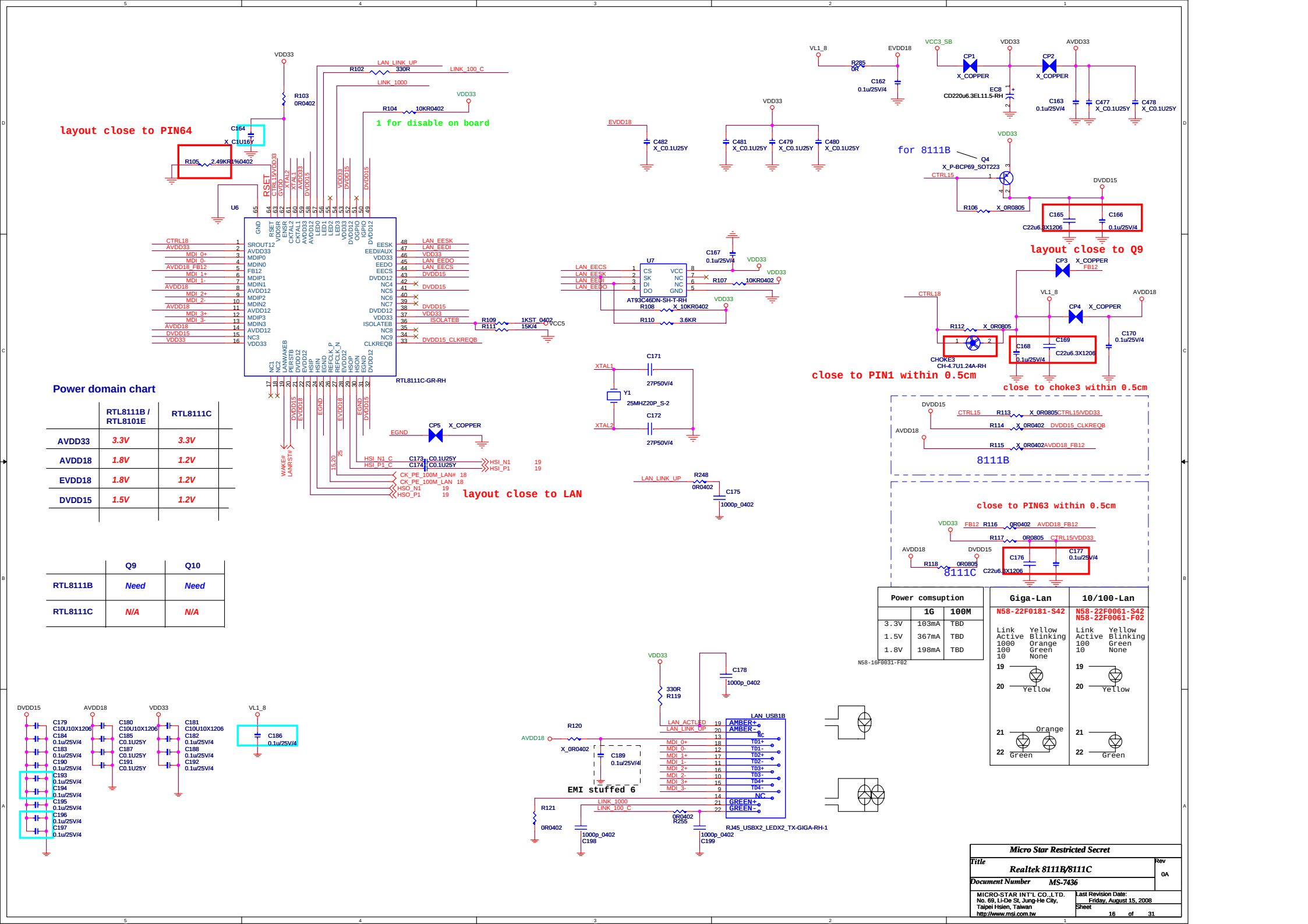
layout close to PIN64
1 for disable on board
RTL8111C-GR-RH
layout close to LAN
for 8111B
layout close to Q9
close to PIN1 within 0.5cm
close to choke3 within 0.5cm
8111B
close to PIN63 within 0.5cm
8111C
EMI stuffed 6
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
Power domain chart
RTL8111B / RTL8101E
RTL8111C
AVDD33 3.3V 3.3V
AVDD18 1.8V 1.2V
EVDD18 1.8V 1.2V
DVDD15 1.5V 1.2V
Q9
Q10
RTL8111B Need Need
RTL8111C N/A N/A
Power comsuption
1G
100M
3.3V 103mA TBD
1.5V 367mA TBD
1.8V 198mA TBD
N58-16F0031-F02
Giga-Lan
N58-22F0181-S42
10/100-Lan
N58-22F0061-S42
N58-22F0061-F02
Link Active 1000 100 10
Yellow Blinking Orange Green None
Yellow
Orange
Green
Micro Star Restricted Secret
Realtek 8111B/8111C
0A
MS-7436
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
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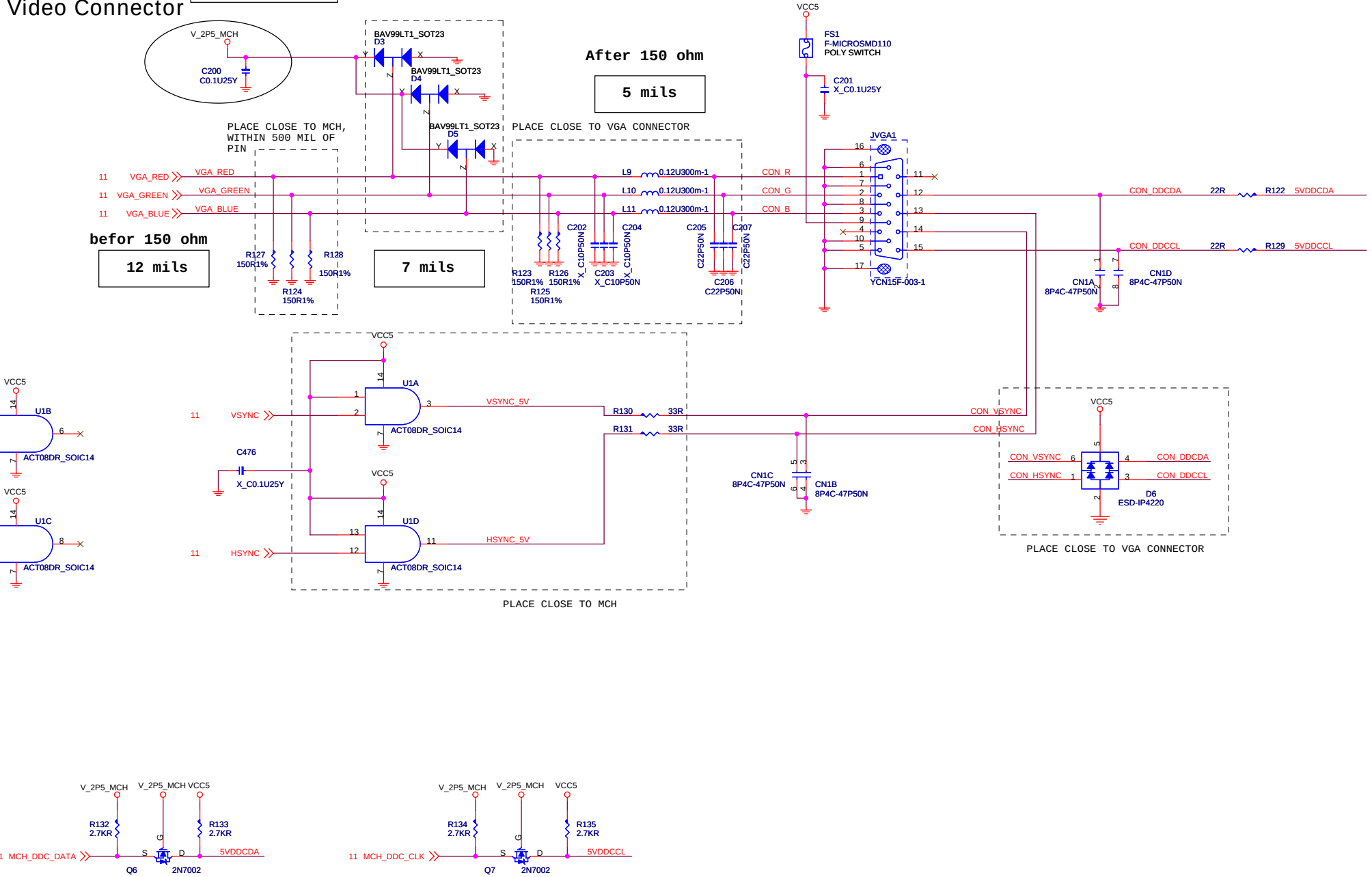
Video Connector

Power 20 mils



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Title: VGA Connector		
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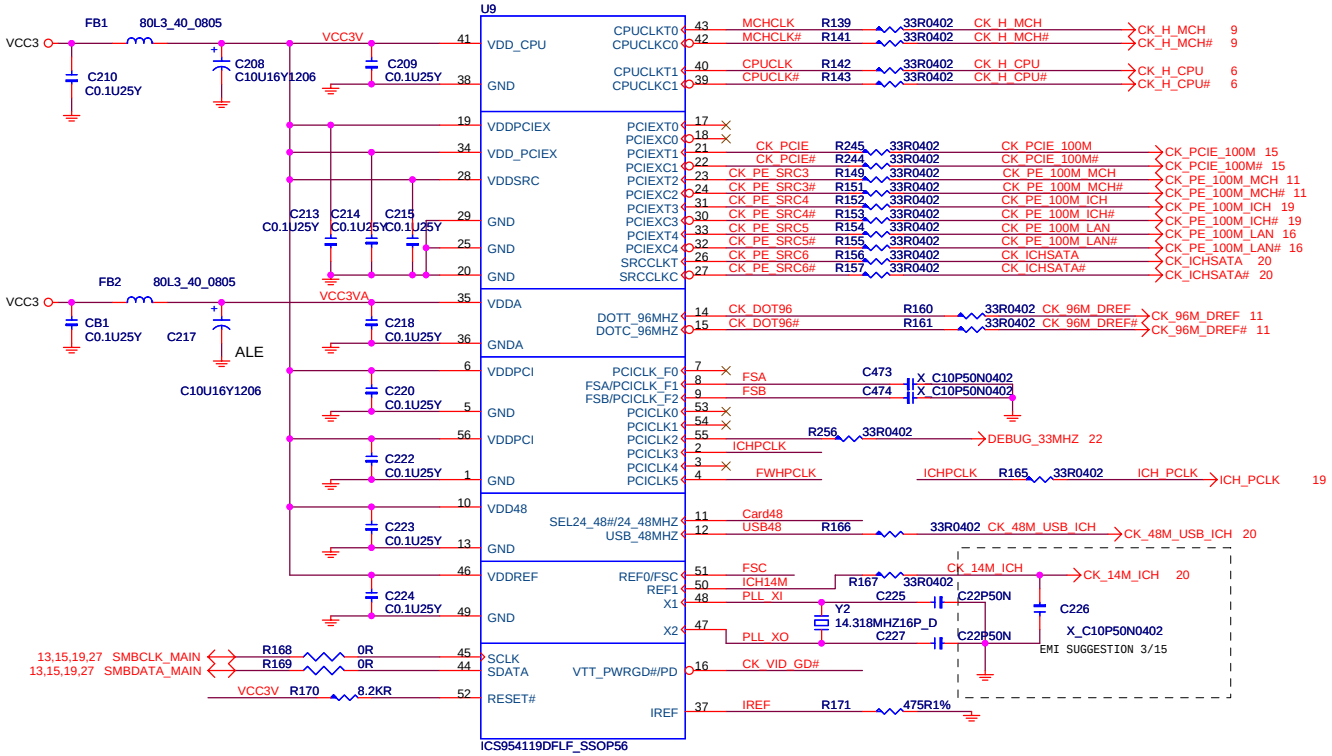
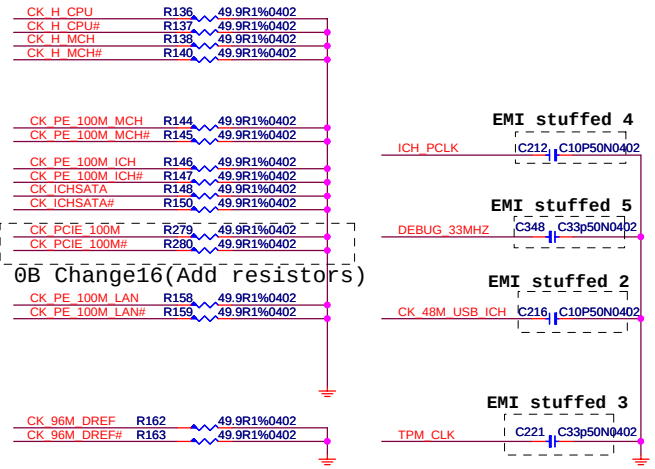
Clock Generator - ICS954119

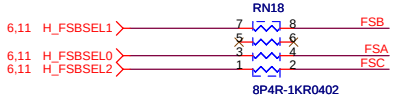
Trace length less than 0.5inchs

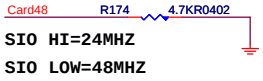


EMC HF filter capacitors, located close to PLL

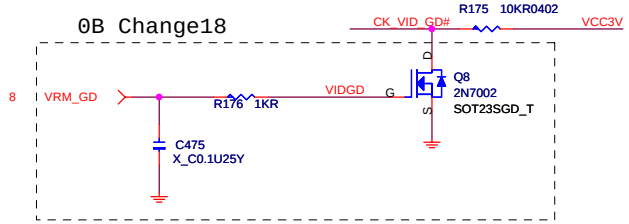


BSEL[0..2] Level Shift





Clock Generator VTT Power Down Block



<Org Address> MSI	MICRO-STAR INt'L CO., LTD.	
Title	Clock Generator - ICS954101	
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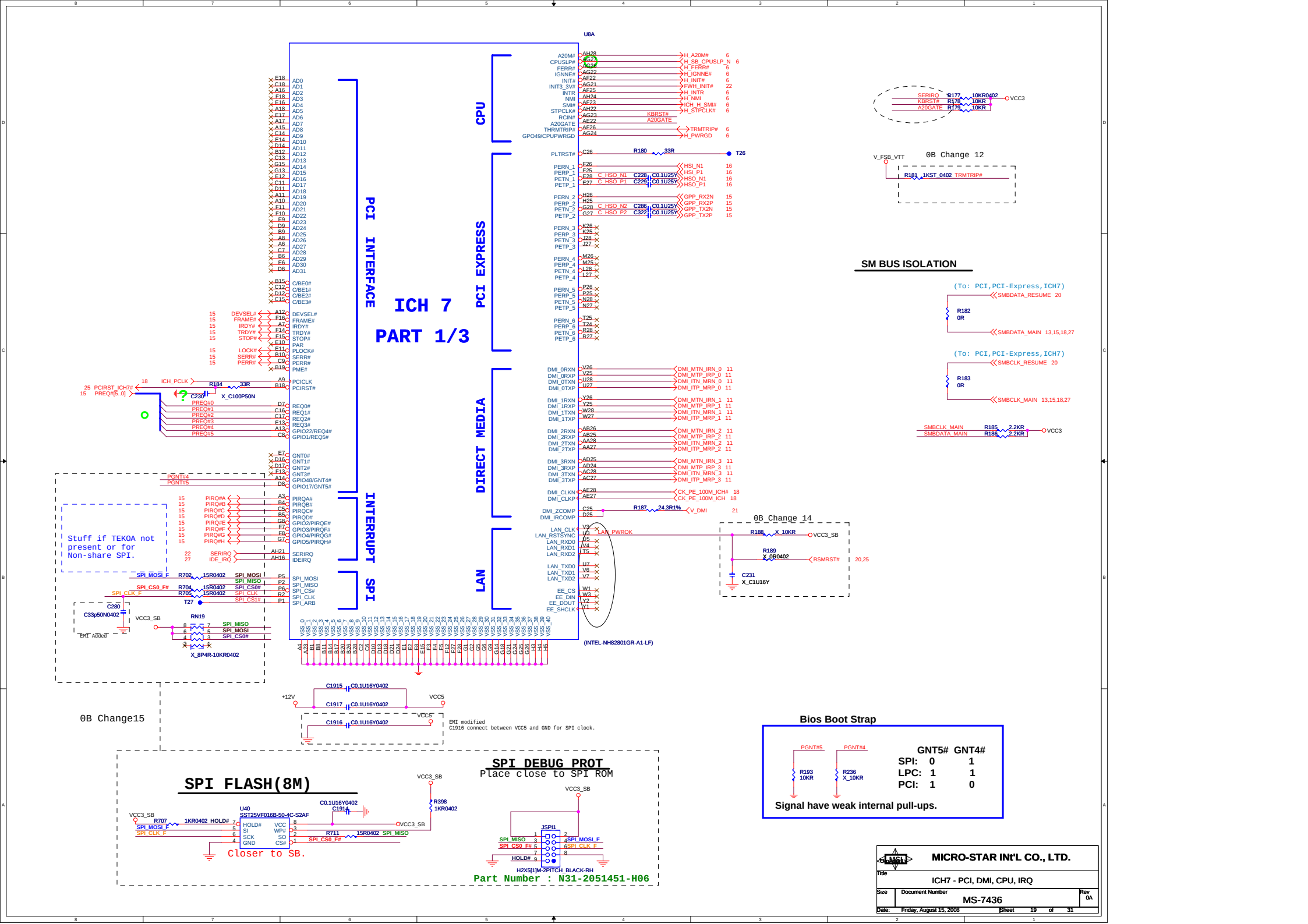
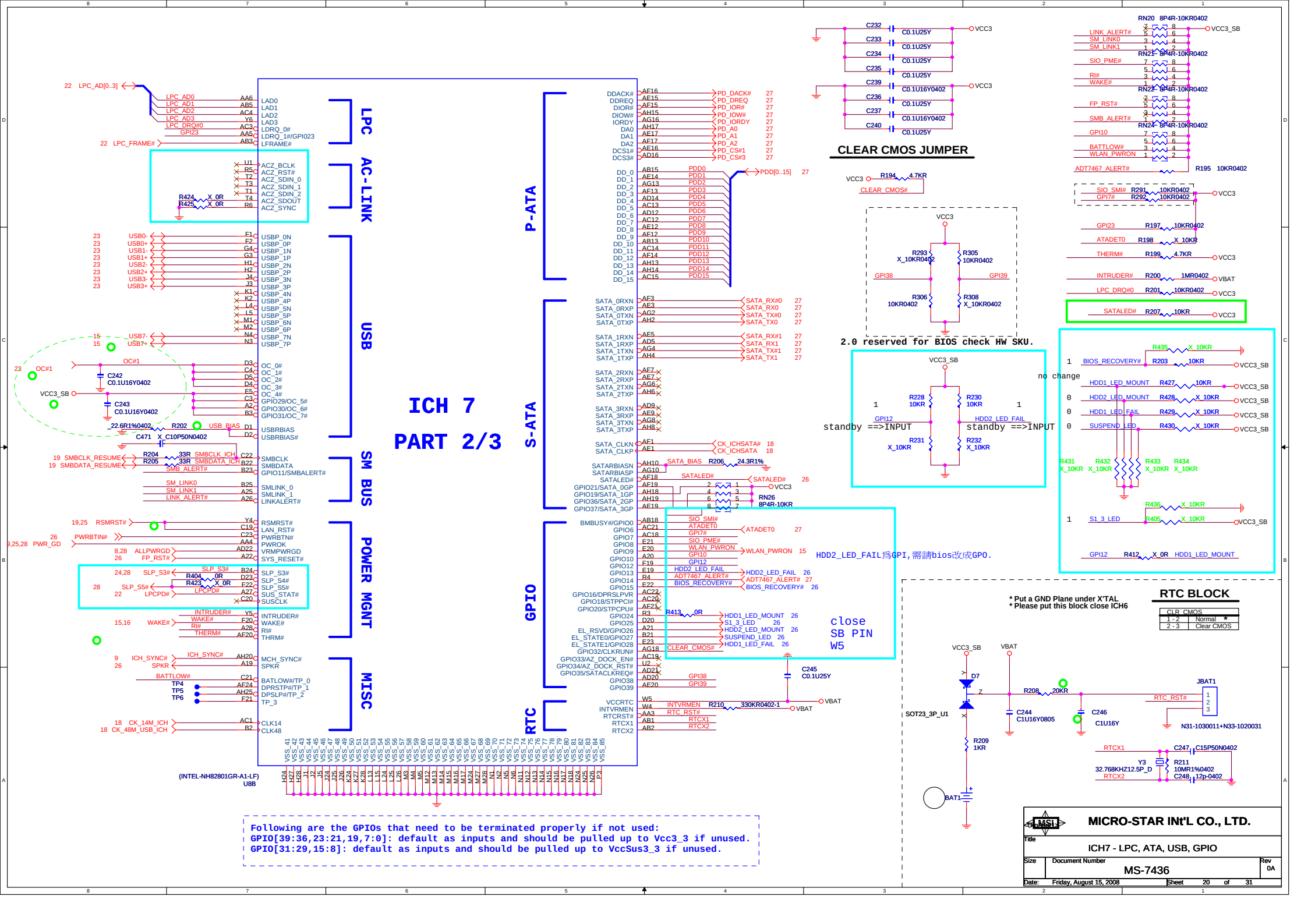
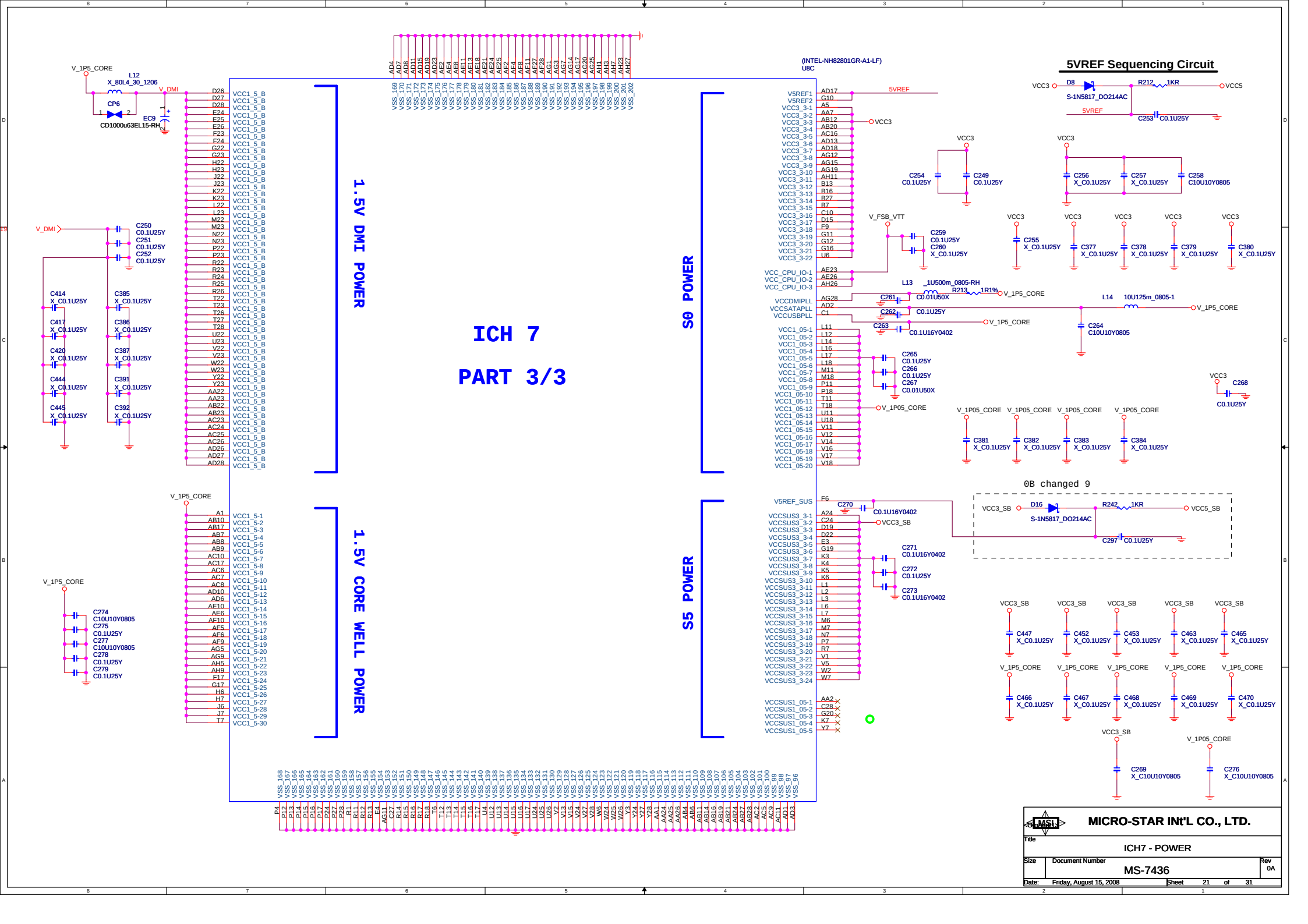
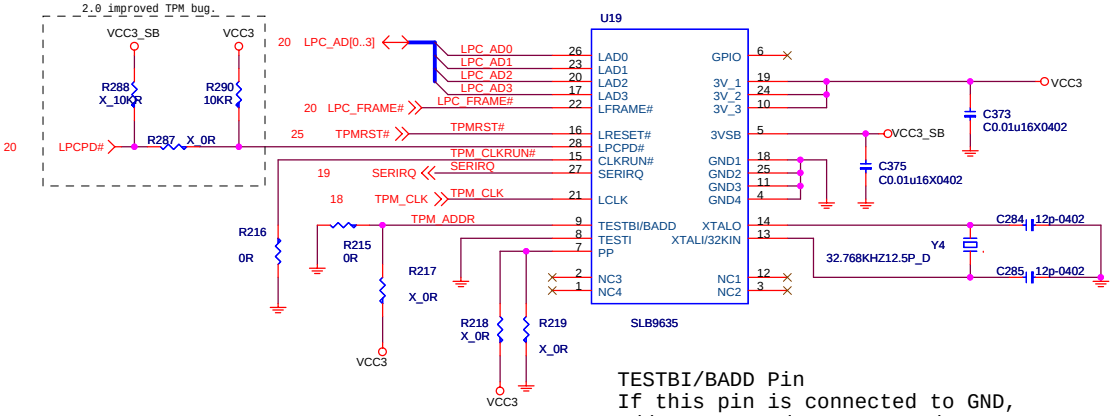

U8A
ICH 7
PART 1/3
CPU
PCI EXPRESS
DIRECT MEDIA
PCI INTERFACE
INTERRUPT
SPI
LAN
(INTEL-NH82801GR-A1-LF)
SM BUS ISOLATION
(To: PCI,PCI-Express,ICH7)
SMBDATA_RESUME 20
R182 0R
SMBDATA_MAIN 13,15,18,27
(To: PCI,PCI-Express,ICH7)
SMBCLK_RESUME 20
R183 0R
SMBCLK_MAIN 13,15,18,27
SMBCLK_MAIN R185 2.2KR
SMBDATA_MAIN R186 2.2KR
VCC3
SERIRQ R177 10KR0402
KBRST# R178 10KR
A20GATE R179 10KR
VCC3
V_FSB_VTT
0B Change 12
R181 1KST_0402 TRMTRIP#
0B Change 14
R188 X_10KR
VCC3_SB
R189 X_0R0402
RSMRST# 20,25
C231 X_C1U16Y
LAN_PWROK
Stuff if TEKOA not present or for Non-share SPI.
SPI_MOSI_F R702 15R0402 SPI_MOSI
SPI_MISO
SPI_CS0_F# R704 15R0402 SPI_CS0#
SPI_CLK_F R705 15R0402 SPI_CLK
SPI_CS1#
C280 C33p50N0402
EMI Added
VCC3_SB
RN19
SPI_MISO
SPI_MOSI
SPI_CS0#
X_8P4R-10KR0402
0B Change15
C1915 C0.1U16Y0402
C1917 C0.1U16Y0402
C1916 C0.1U16Y0402
+12V
VCC5
EMI modified
C1916 connect between VCC5 and GND for SPI clock.
SPI FLASH(8M)
U40
SST25VF016B-50-4C-S2AF
R707 1KR0402 HOLD#
SPI_MOSI_F
SPI_CLK_F
C0.1U16Y0402 C1914
R711 15R0402 SPI_MISO
SPI_CS0_F#
R398 1KR0402
Closer to SB.
SPI DEBUG PROT
Place close to SPI ROM
JSPI1
H2X5[1]M-2PITCH_BLACK-RH
Part Number : N31-2051451-H06
Bios Boot Strap
PGNT#5 R193 10KR
PGNT#4 R236 X_10KR
GNT5# GNT4#
SPI: 0 1
LPC: 1 1
PCI: 1 0
Signal have weak internal pull-ups.
MICRO-STAR INt'L CO., LTD.
Title
ICH7 - PCI, DMI, CPU, IRQ
Size
Document Number
MS-7436
Rev 0A
Date: Friday, August 15, 2008
Sheet 19 of 31


ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
(INTEL-NH82801GR-A1-LF)
U8B
CLEAR CMOS JUMPER
2.0 reserved for BIOS check HW SKU.
HDD2_LED_FAIL為GPI,需請bios改成GPO.
close
SB PIN
W5
RTC BLOCK
* Put a GND Plane under X'TAL
* Please put this block close ICH6
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MICRO-STAR INt'L CO., LTD.
ICH7 - LPC, ATA, USB, GPIO
MS-7436
Friday, August 15, 2008
Sheet 20 of 31

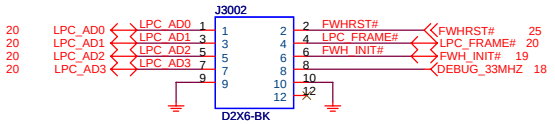

ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
(INTEL-NH82801GR-A1-LF)
U8C
5VREF Sequencing Circuit
0B changed 9
MICRO-STAR INt'L CO., LTD.
ICH7 - POWER
MS-7436
Friday, August 15, 2008

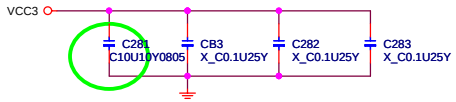
IO Address:0x02E

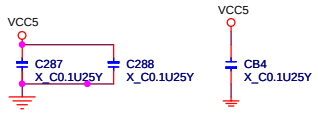


TESTBI/BADD Pin
If this pin is connected to GND,
addresses 2EH/2FH are used.
If it is strapped to VCC,
addresses 4EH/4FH are used.

LPC Debug Port

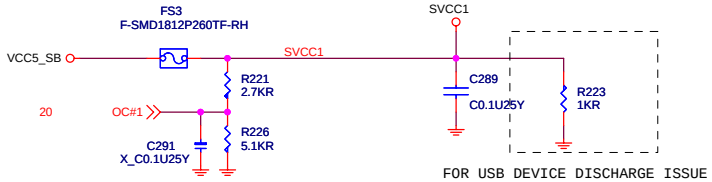






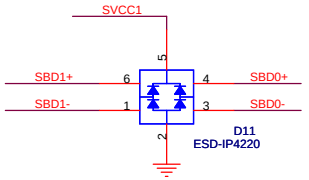
<OrgAddr1>	MICRO-STAR INt'L CO., LTD.	
Title	FWH	
Size	Document Number MS-7436	Rev 0A
Date: Friday, August 15, 2008	Sheet 22 of 31	

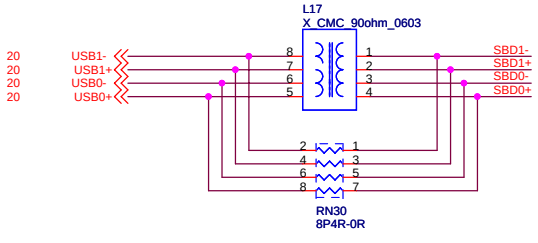
POWER CIRCUIT FOR USB PORT 0,1 (REAR)

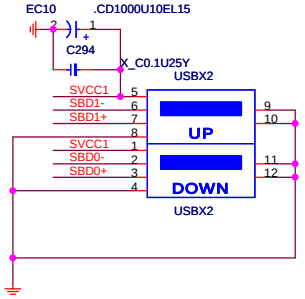


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

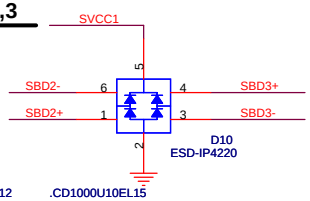


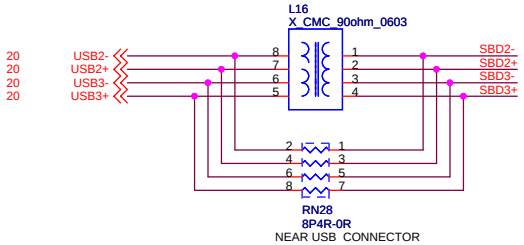


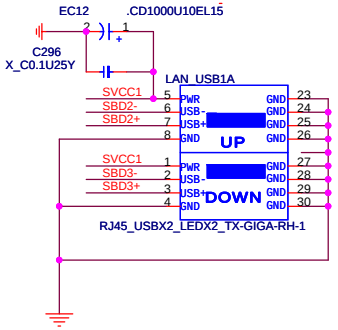


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"







MSI MICRO-STAR INT'L CO.,LTD.

Title: USB CONNECTORS		
Size: A3	Document Number: MS-7436	Rev: 0A
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DC Voltage IN

Place these CAPs close to FETs

+3VSUS

+3VALW

+5VSUS

+3VRUN

+5VALW

+5VRUN

3.33A

18.11A

EN0 open: LDO on and turn on switcher channel

DC Voltage OUT1

19V TO 12V

/6A

2.0 EMI modified 7~11.

Title	DC-IN POWER		
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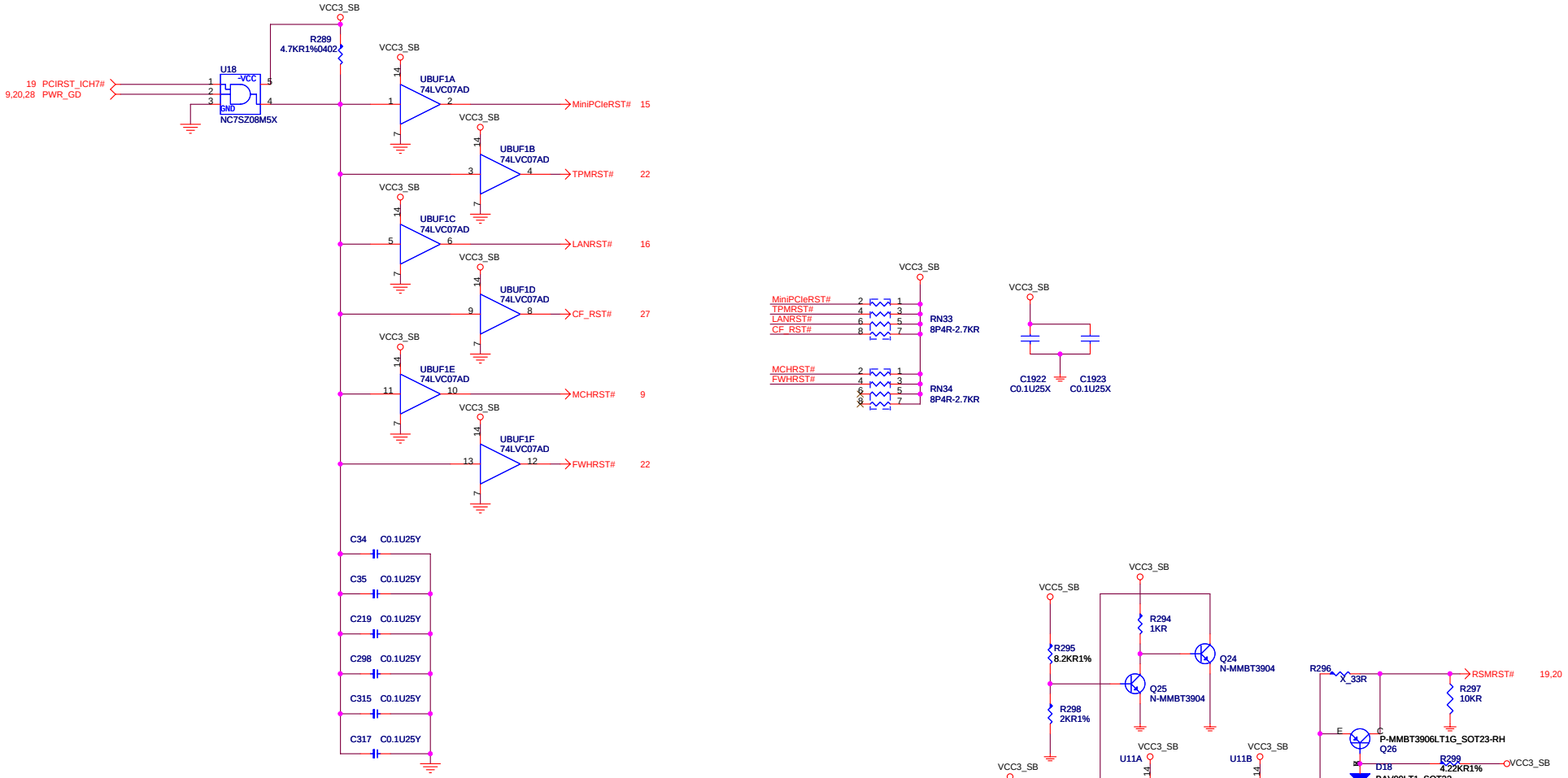
MICRO-START INT'L CO.,LTD.



MICRO-STAR INt'L CO. , LTD.		
Title: **5VSB POWER**		
Size: Custom	Document Number: MS-7436	Rev: 0A
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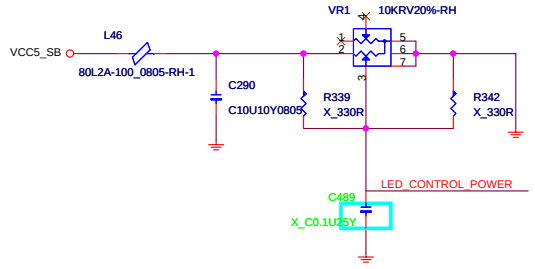
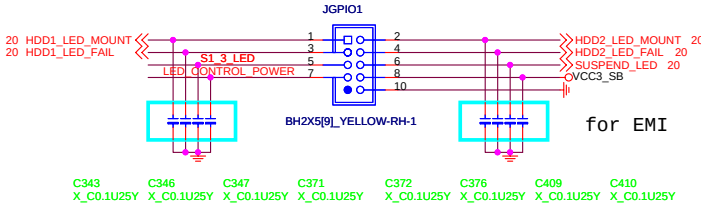
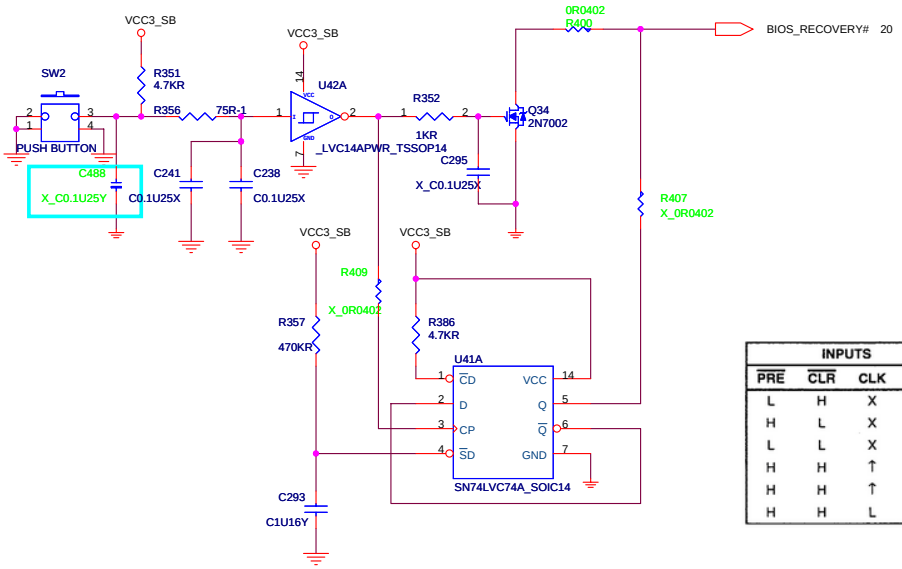
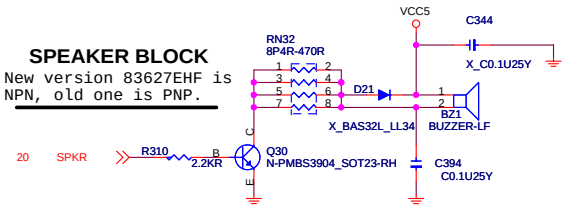
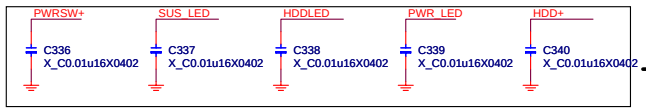




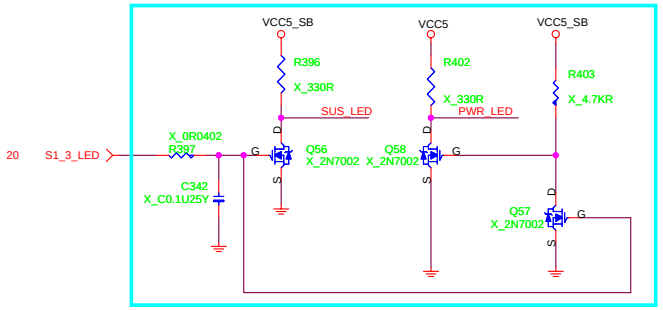


INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

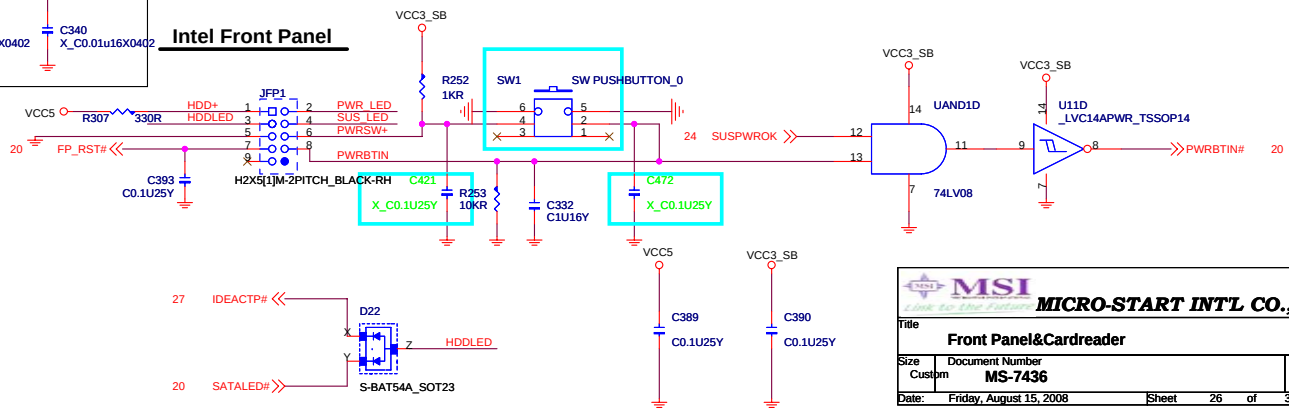




Reserve For EMI



Intel Front Panel



MICRO-START INT'L CO.,LTD.

Title	Front Panel&Cardreader	
Size: Custom	Document Number: MS-7436	Rev: 0A
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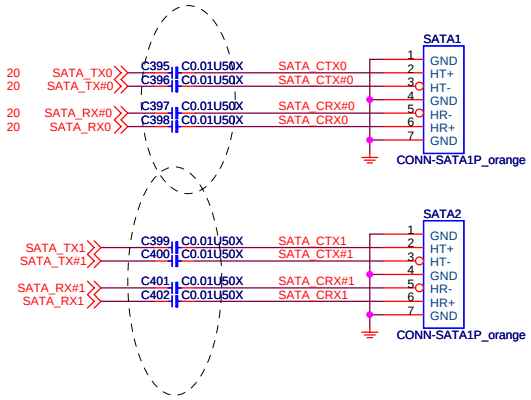
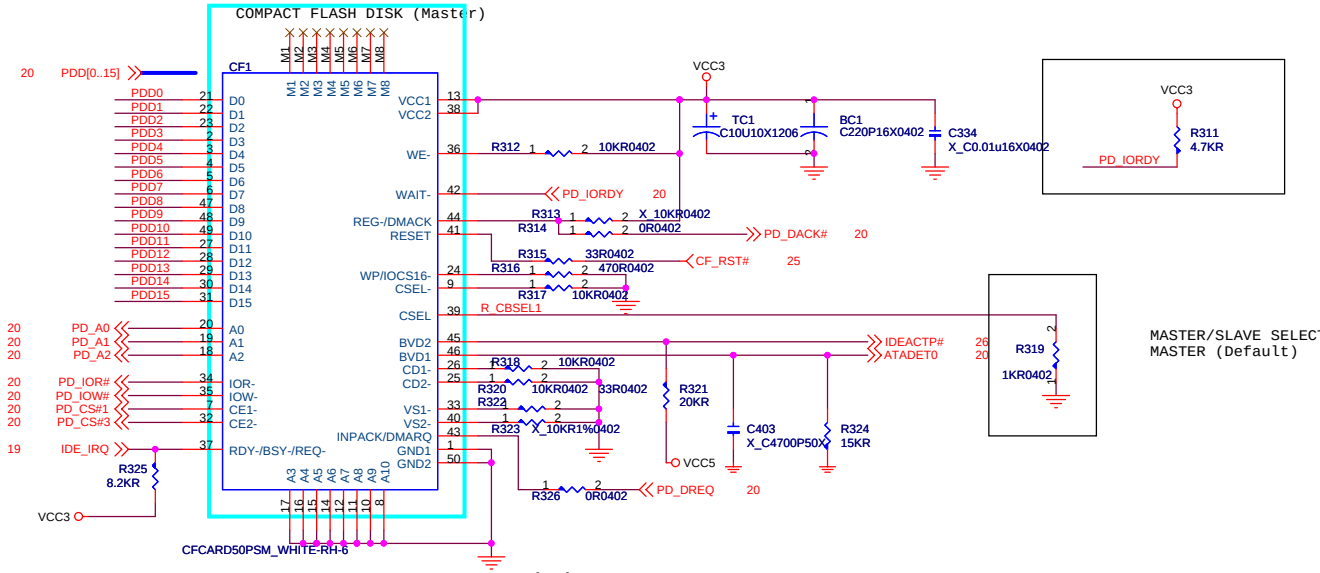
SERIAL ATA CONNECTOR BLOCK



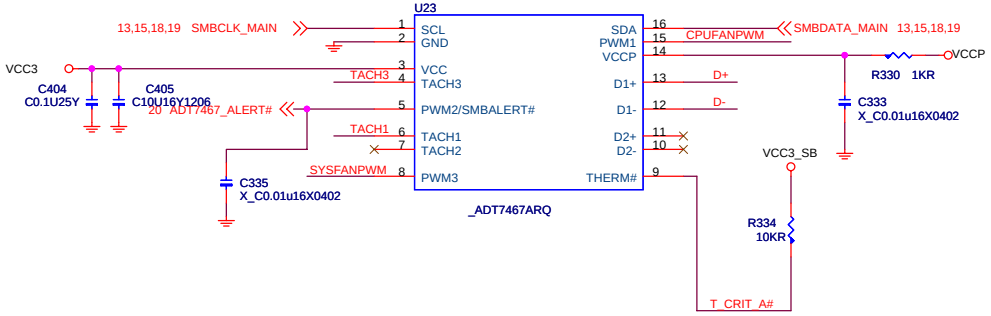
COMPACT FLASH CONNECTOR

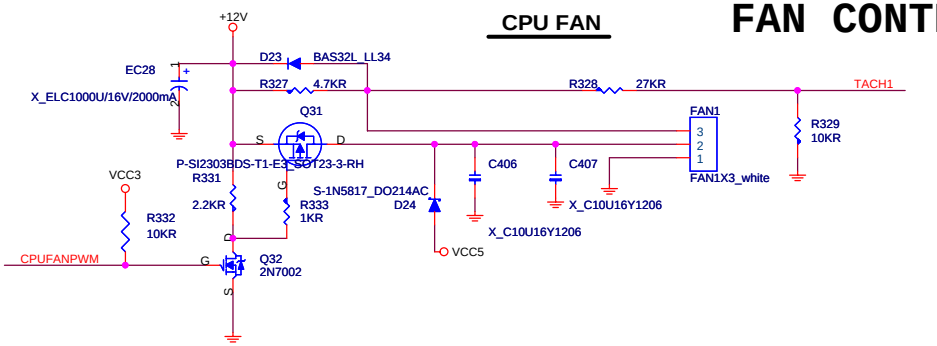


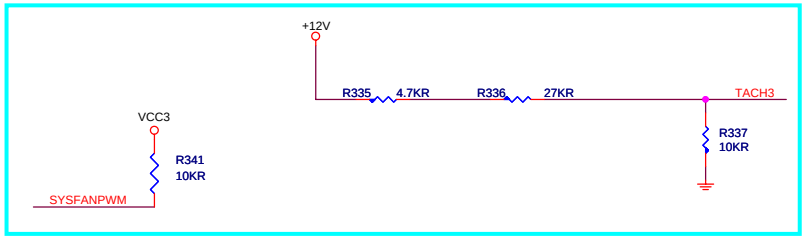
PDIAG# & DASP# are output during reset for SLAVE detection.

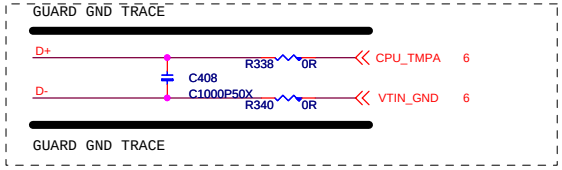
CPU FAN

FAN CONTROL









PLACE ADT7467 AS CLOSE AS POSSIBLE TO CPU

GUARD TRACE & D+/D- WIDTH:SPACE= 10:10 MIL(MIN)

MICRO-START INT'L CO.,LTD.

Title: SATA1,2 , CF_Card& Fan control		
Size: A3	Document Number: MS-7436	Rev: 0A
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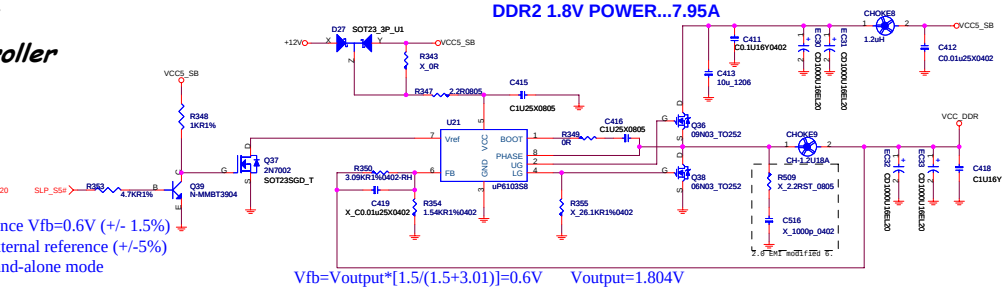
ACPI Controller

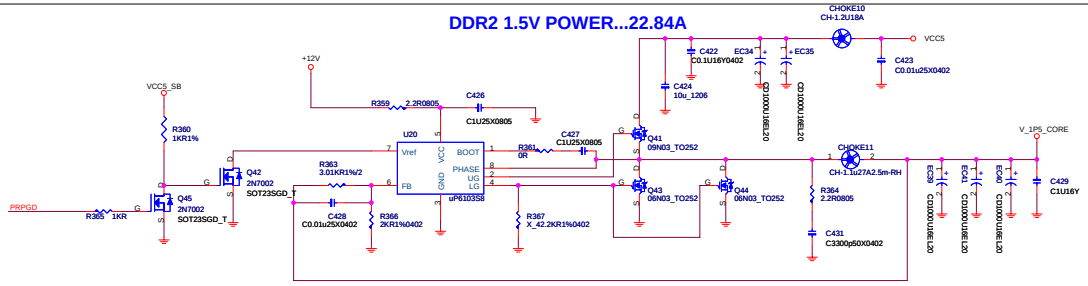
DDR2 1.8V POWER...7.95A



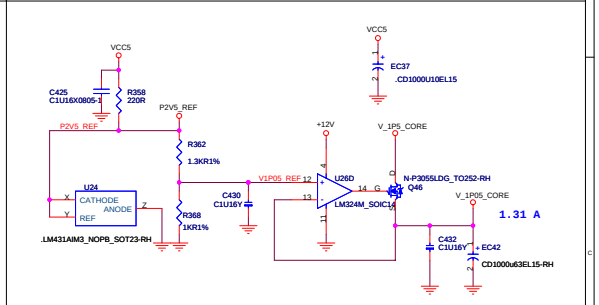
Internal reference Vfb=0.6V (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

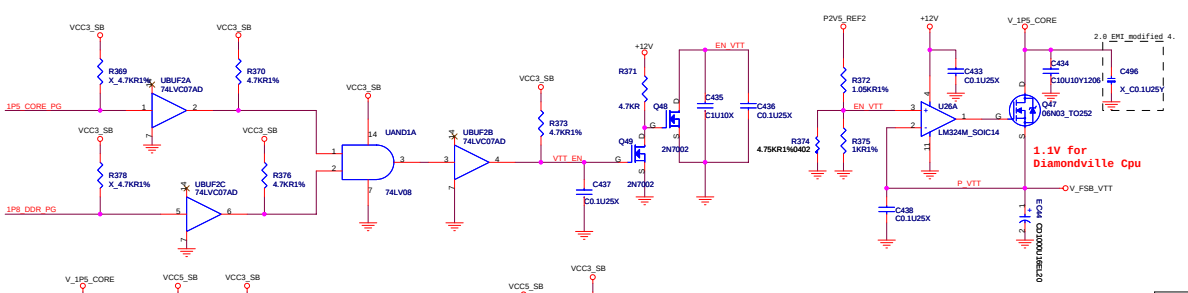
Vfb=Voutput*[1.5/(1.5+3.01)]=0.6V Voutput=1.804V

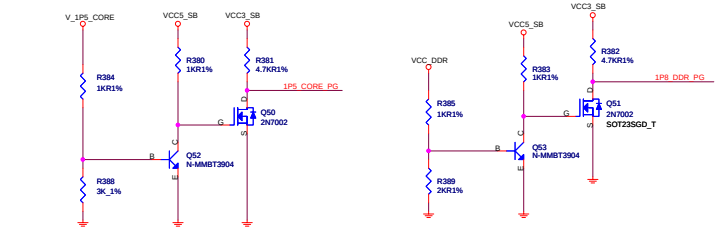
DDR2 1.5V POWER...22.84A

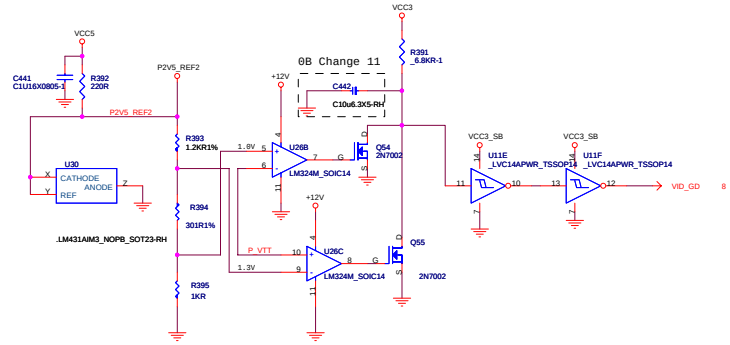


Vfb=Voutput*[2/(2+3.01)]=0.6V Voutput=1.503V

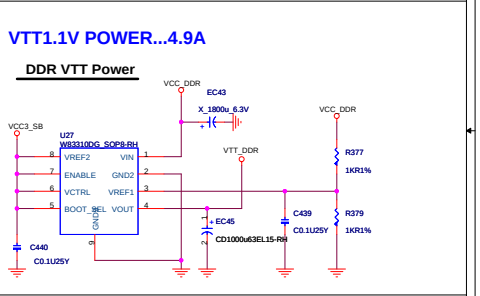


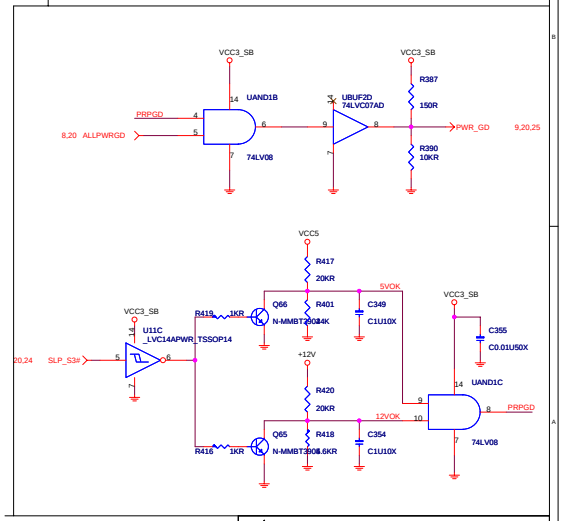






VTT1.1V POWER...4.9A





MICRO-STAR INt'L CO., LTD.			
Title: MS7 ACPI CONTROLLER			
Size	Document Number: MS-7436		Rev: 0A
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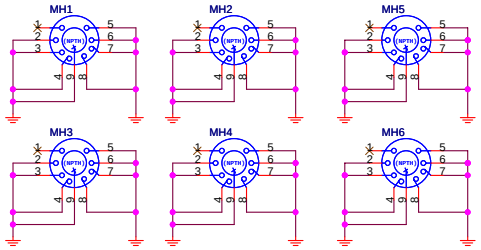
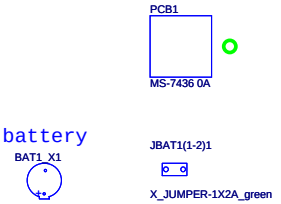
Auto-BOM Manual Parts

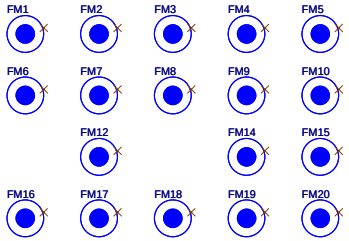
Mounting Holes



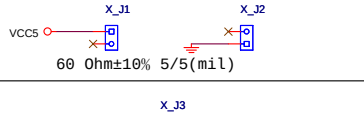
MANUAL PART



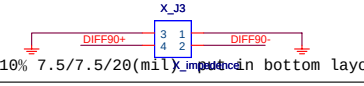
Optics Orientation Holes



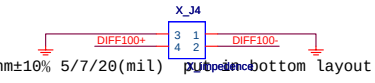
Simulation



60 Ohm±10% 5/5(mil)

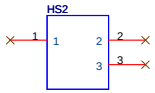


90 Ohm±10% 7.5/7.5/20(mil) pair in bottom layout

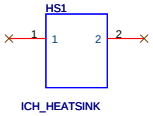


100 Ohm±10% 5/7/20(mil) pair in bottom layout

CPU HEAT SINK NB HEAT SINK



SB HEAT SINK



MICRO-STAR INt'L CO., LTD.		
Title: Auto BOM manual		
Size	Document Number: MS-7436	Rev: 0A
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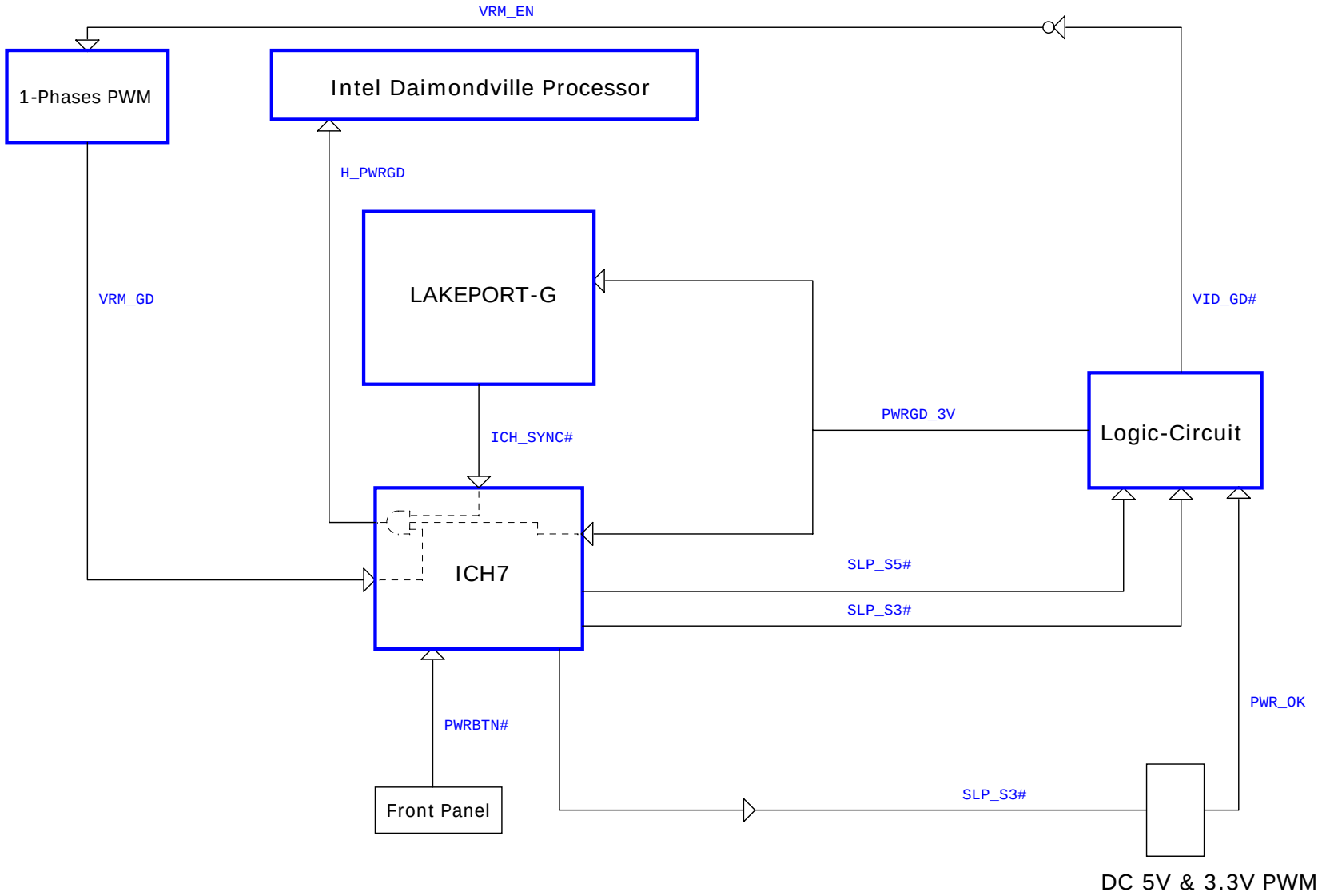
PWROK MAP



MSI	MICRO-STAR INt'L CO., LTD.	
Title	PWOK MAP	
Size	Document Number MS-7436	Rev 0A
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MSI	MICRO-STAR INt'L CO., LTD.
Title	History
Size	Document Number: MS-7436
Rev	0A
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