MS-7411 Ver:0A

CPU:

AMD AM2+
AMD AMD Athlon 64 X2
AMD Athlon 64 FX
AMD Athlon 64
AMD Sempron CPUs

System Chipset:

AMD - RS780 (North Bridge)
- RX780 (North Bridge)
AMD - SB700 (South Bridge)

On Board Chipset:

BIOS - SPI
Azalia CODEC - Realtek ALC662(Default)/888
LPC Super I/O -- ITE IT8718F(GX)
LAN - Marvell 8039/8056/8071/8075/8070(Default)
IEEE1394 - VIA VT6308P
TMP - WPCT200(Default)/ST19WP18
Asset ID - PCA24S08
HWM W83201G

Main Memory:

DDR II * 4 (Max 4GB)

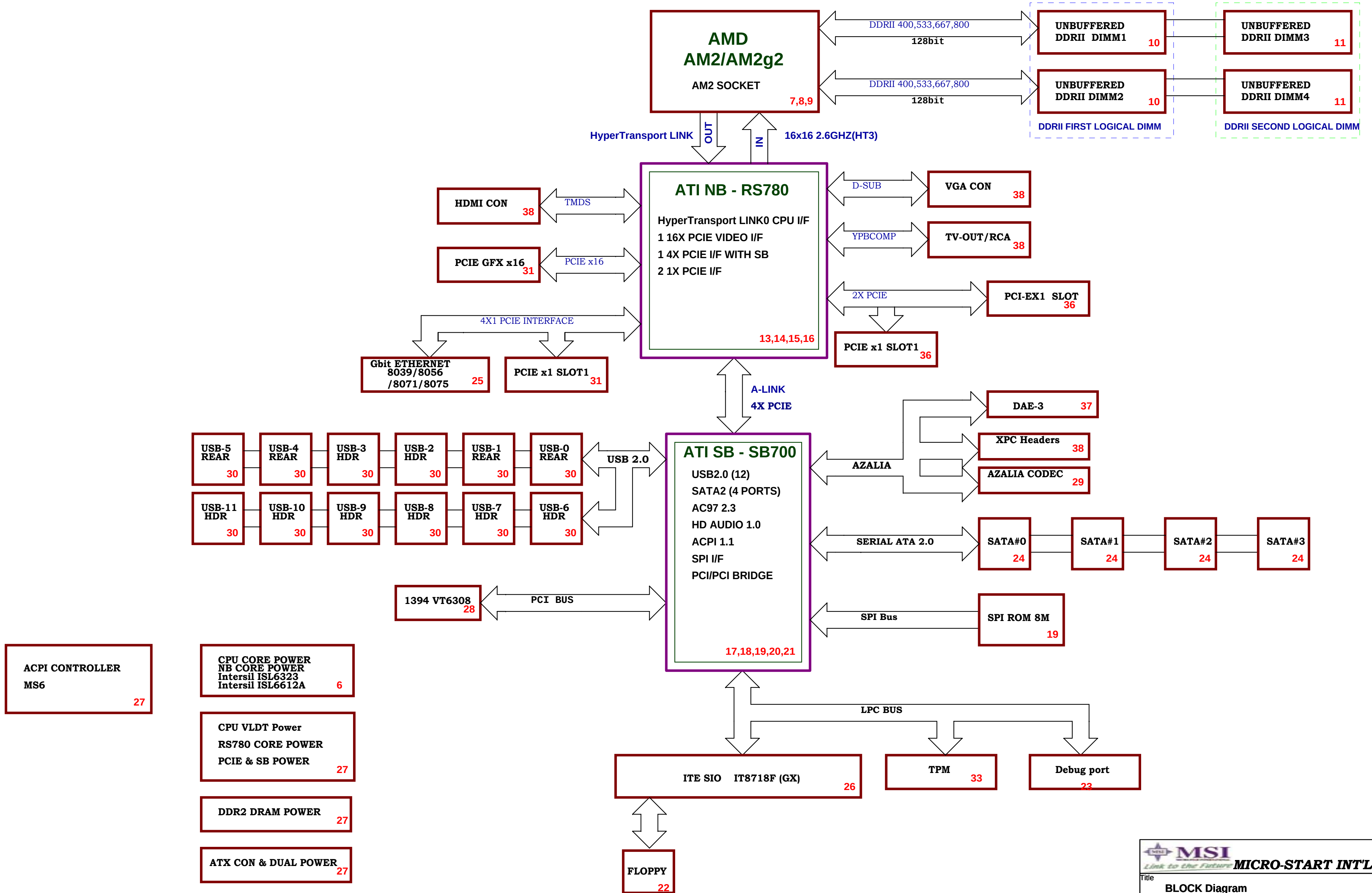
Expansion Slots:

PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI 2.3 Slot * 2

Intersil PWM:

Controller - Intersil 6323 3 Phase

Project RS-780 BLOCK DIAGRAM



MSI MICRO-START INT'L CO.,LTD.

Title	BLOCK Diagram	
Size: Custom	Document Number: MS-7411	Rev: 0A
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SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTEVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTEVNT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SMI#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	PREQ#0 PGNT#0	AD16	PCICLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	PREQ#1 PGNT#1	AD17	PCICLK1
IEEE-1394	PCI_INTC#	PREQ#2 PGNT#2	AD18	PCICLK2

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	GPIO Configuration	
Size C	Document Number MS-7411	Rev 0A
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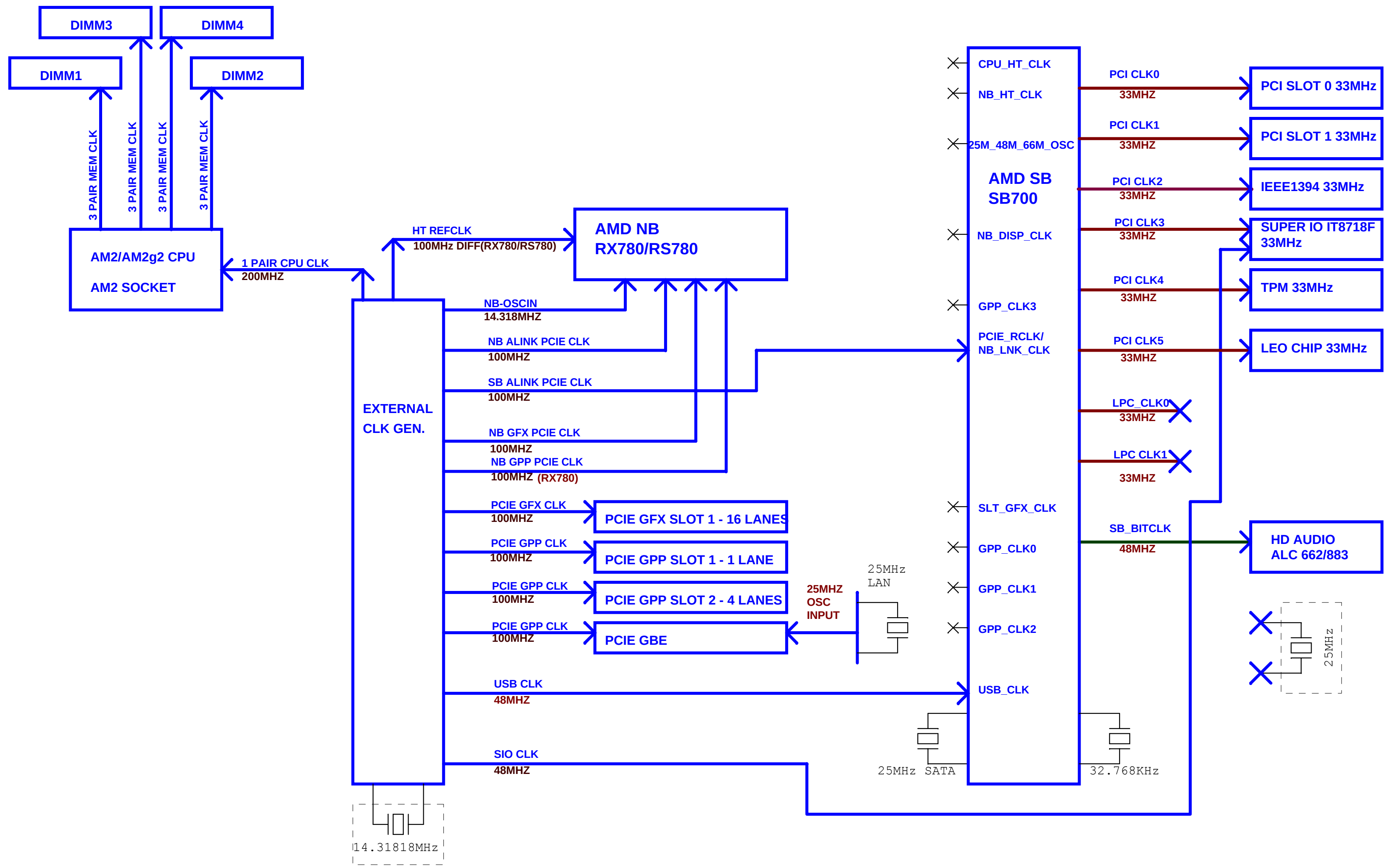

External clock mode

Internal clock mode

MICRO-START INT'L CO.,LTD.

Title: Clock Distribution Chart		
Size: Custom	Document Number: MS-7411	Rev: 0A
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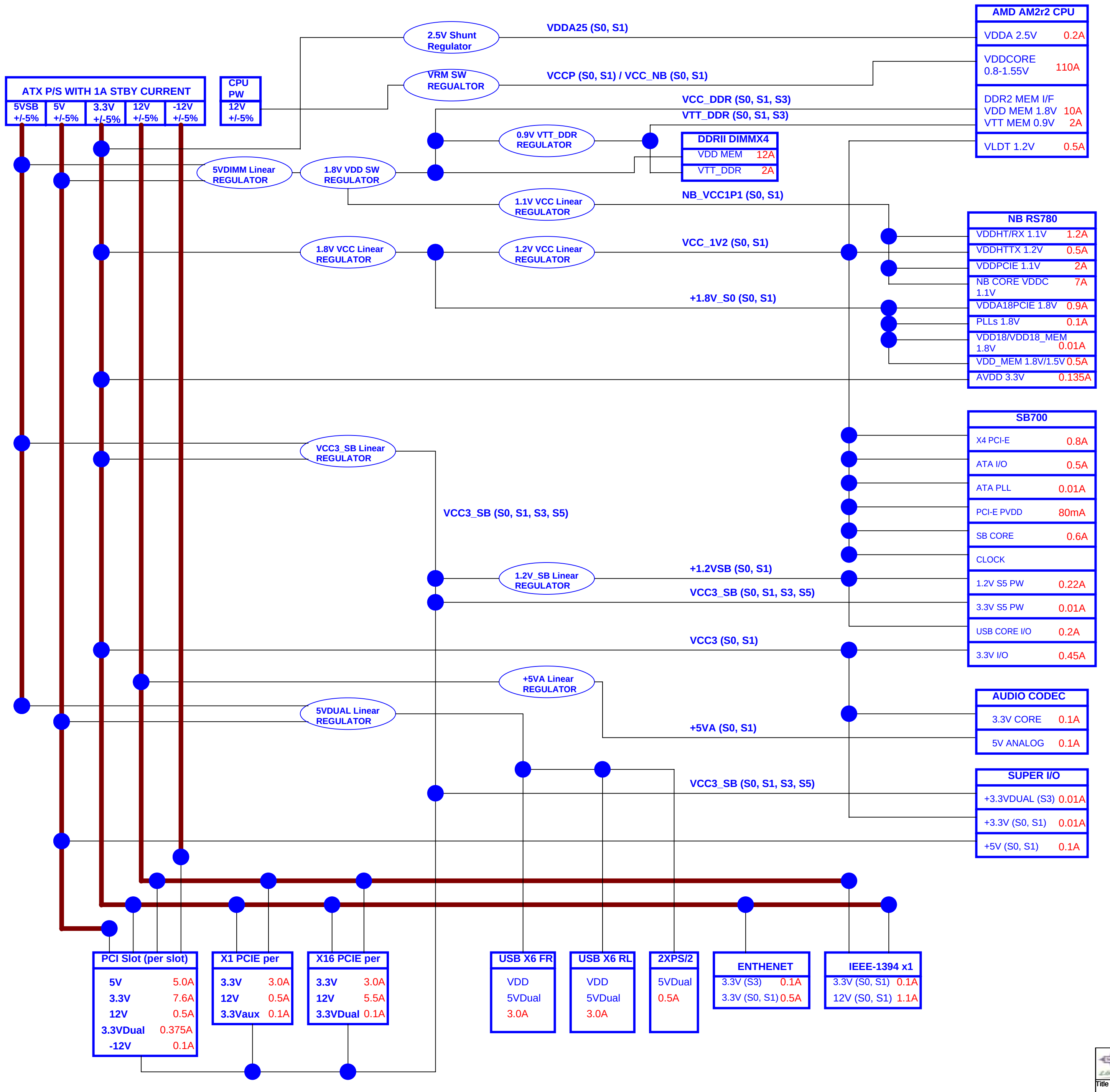
Power Deliver Chart



MICRO-START INT'L CO.,LTD.

Title	Power Deliver Chart	
Size C	Document Number MS-7411	Rev 0A
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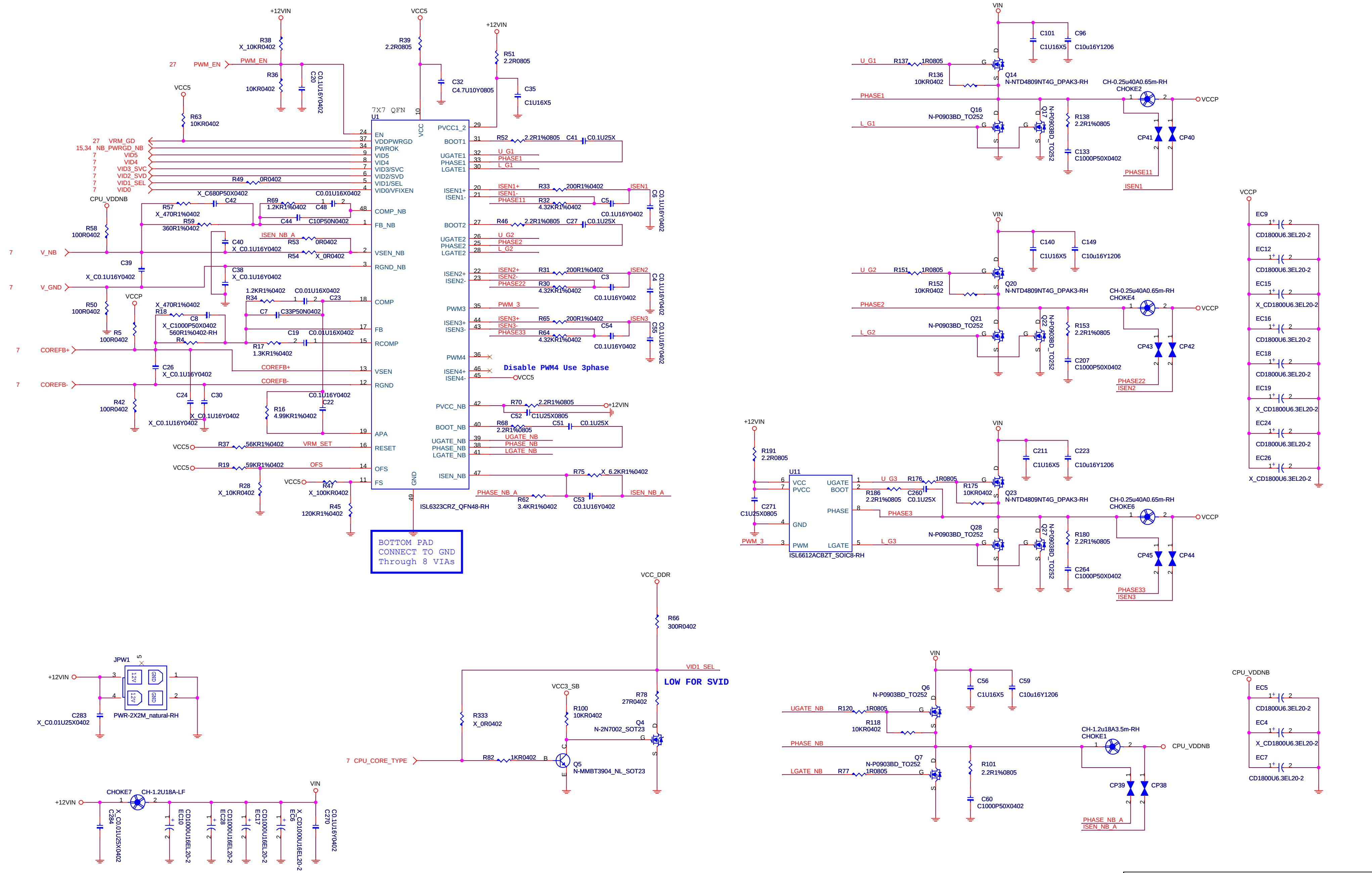
Intersil 6323 3 Phase



MICRO-START INT'L CO.,LTD.		
Title	Intersil 6323 3 Phase	
Size: C	Document Number: MS-7411	Rev: 0A
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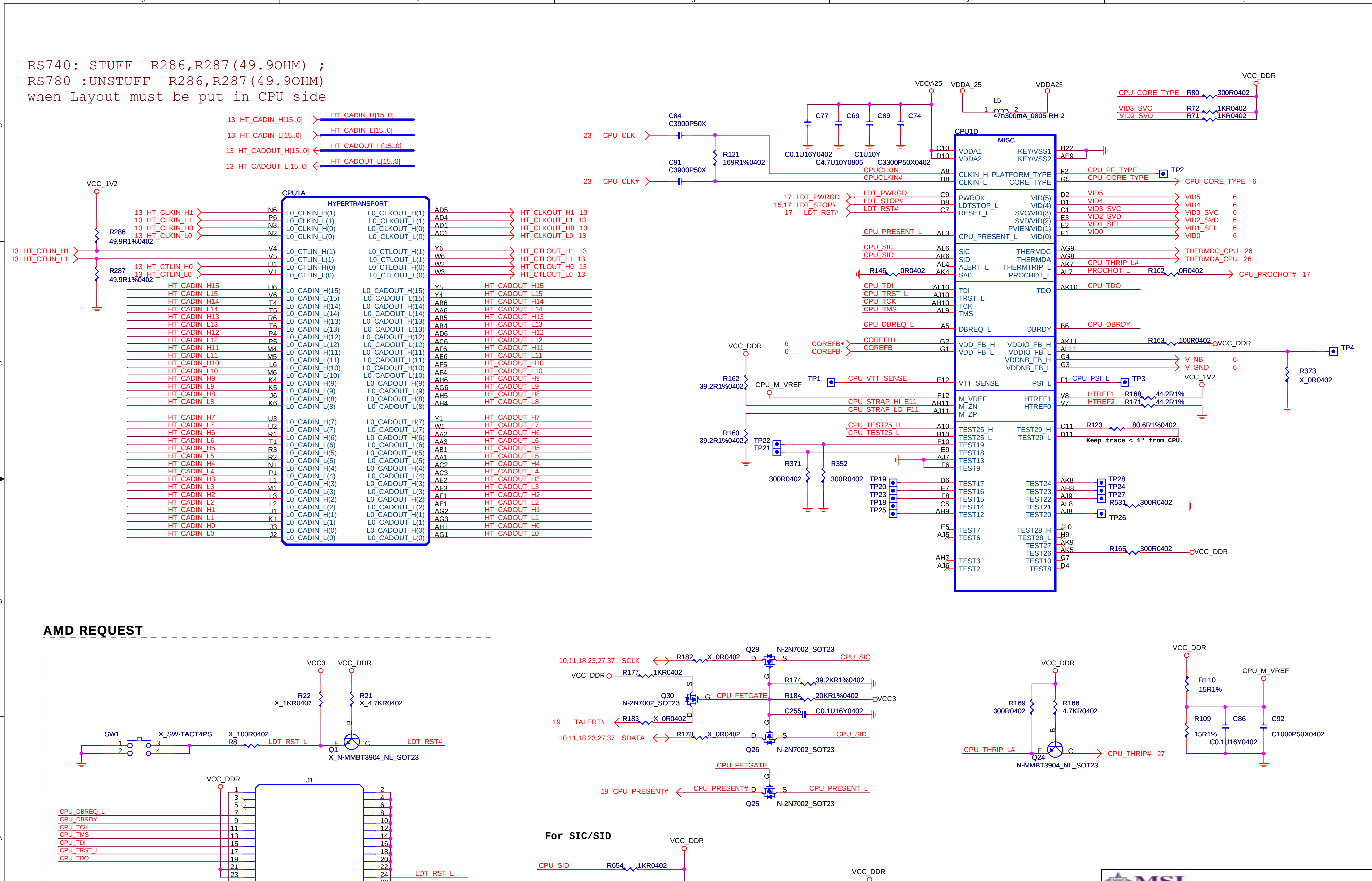
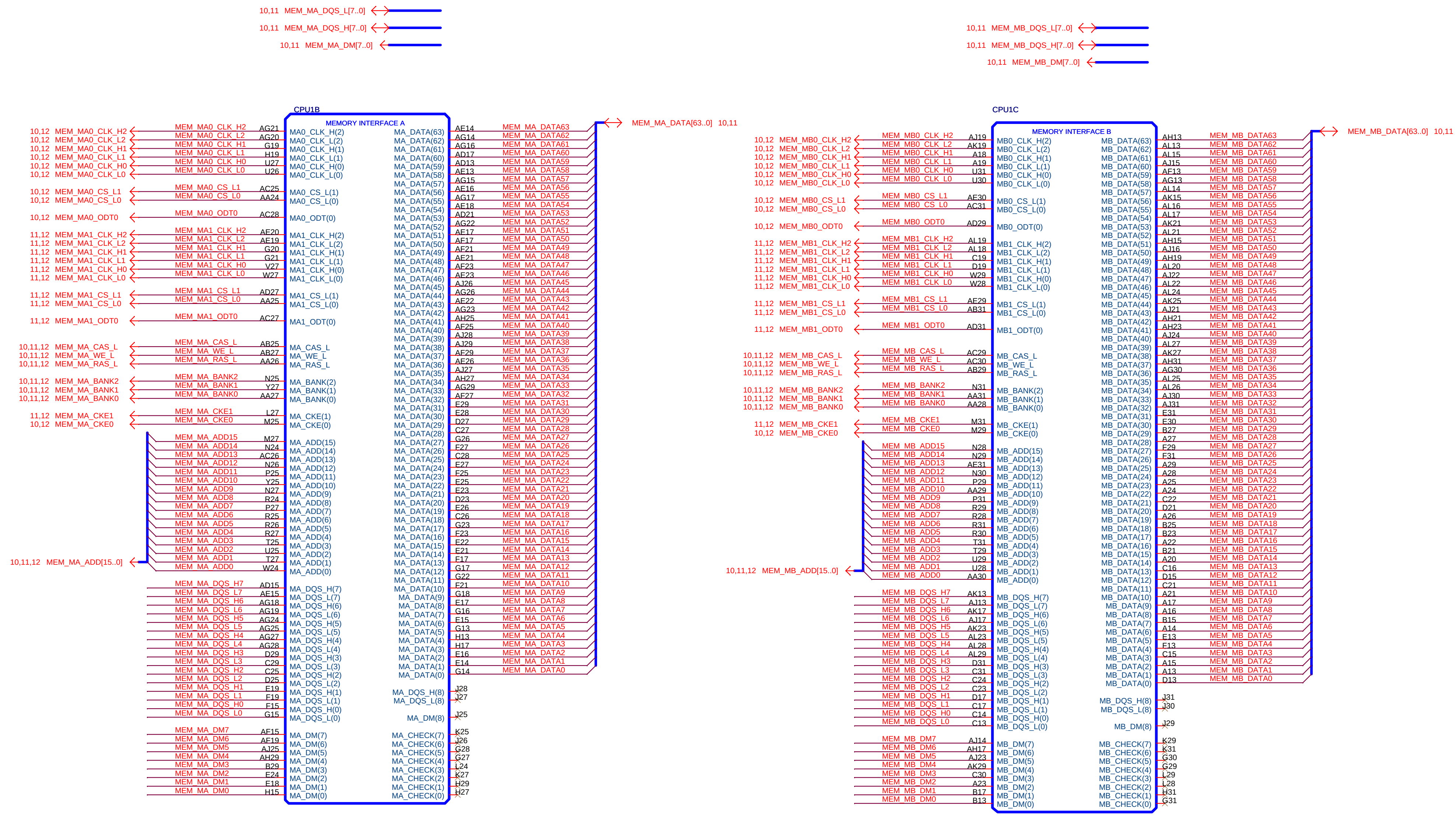


Title	CPU AM2 HT I/F,CTRL&DEBUG	
Size: Custom	Document Number: MS-7411	Rev: 0A
Date: Thursday, October 11, 2007	Sheet 7 of 39	



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Title: CPU AM2 DDR MEMORY I/F

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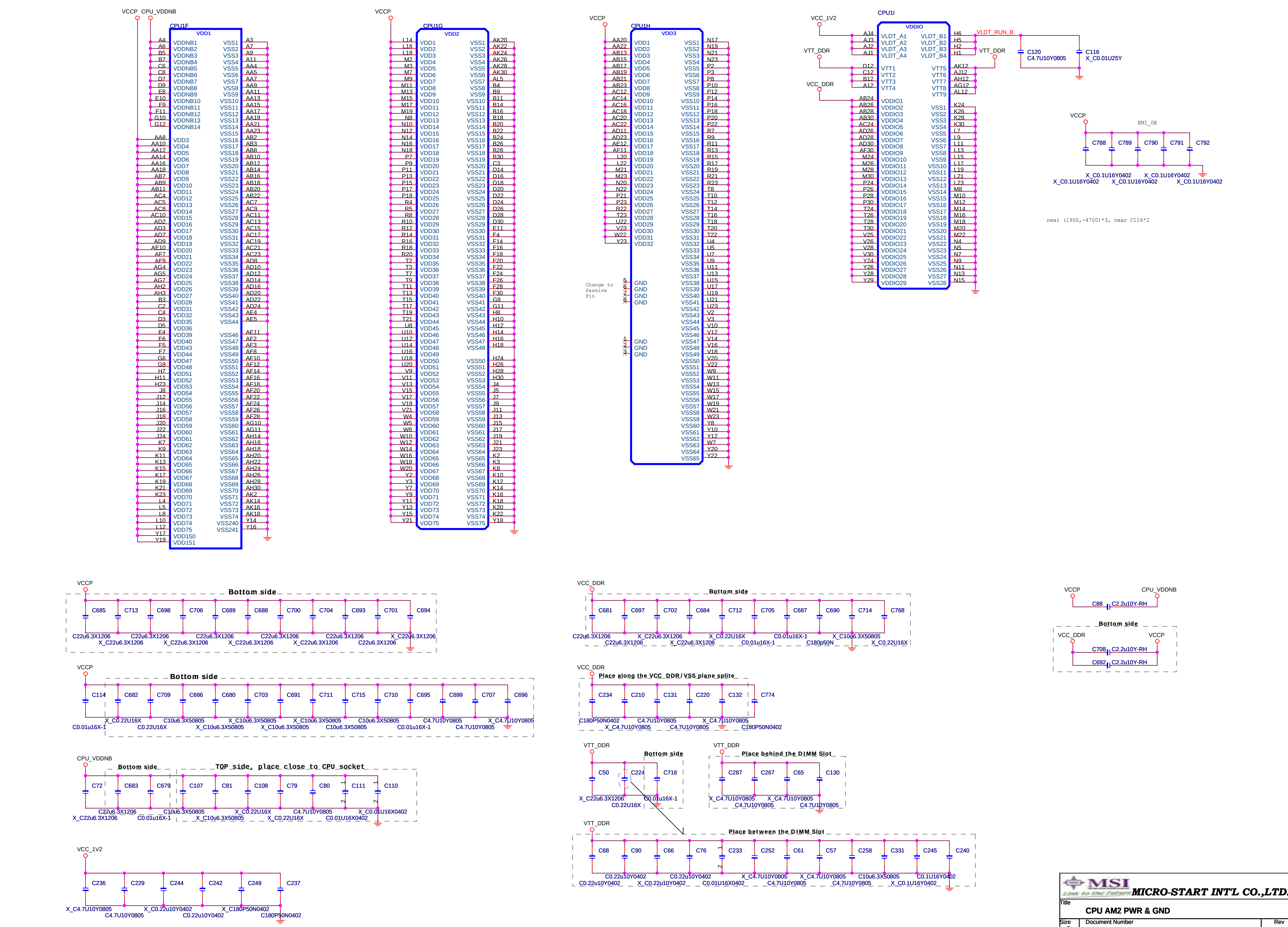
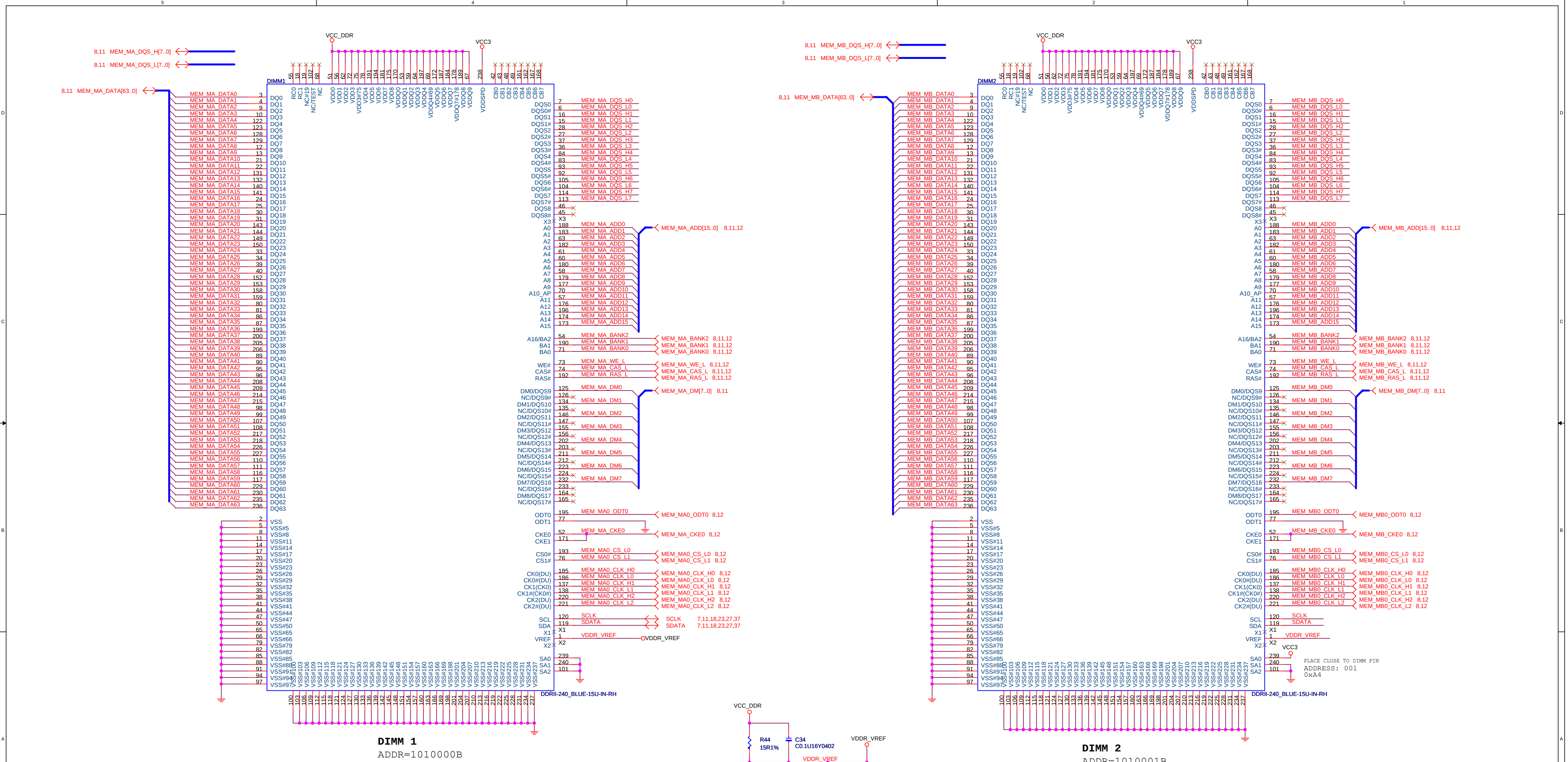
CPU AM2 PWR & GND



MICRO-START INT'L CO.,LTD.

Title	CPU AM2 PWR & GND	
Size C	Document Number MS-7411	Rev 0A
Date: Thursday, October 11, 2007	Sheet 9 of 39	



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Title	FIRST LOGICAL DDR DIMM	
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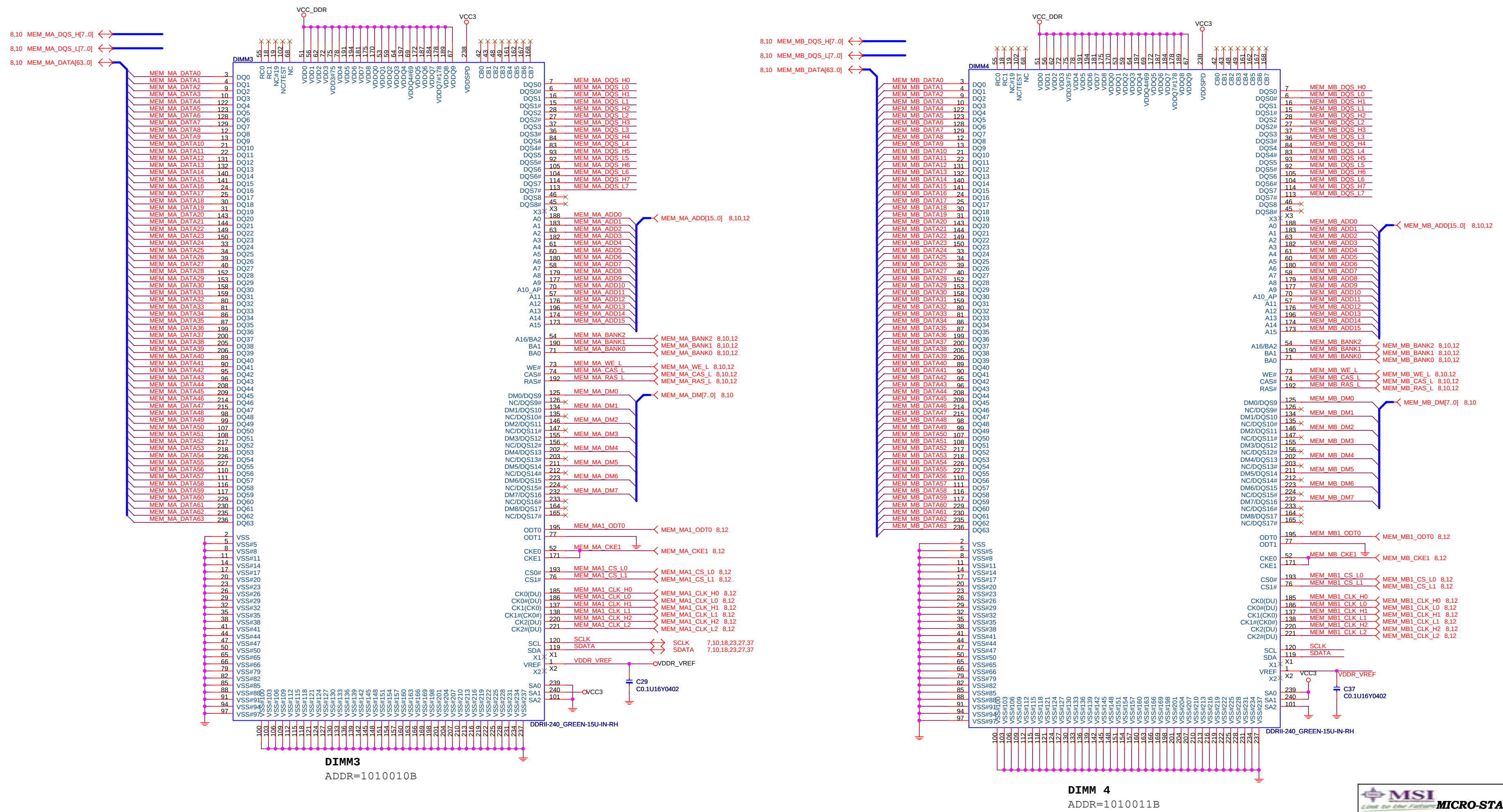

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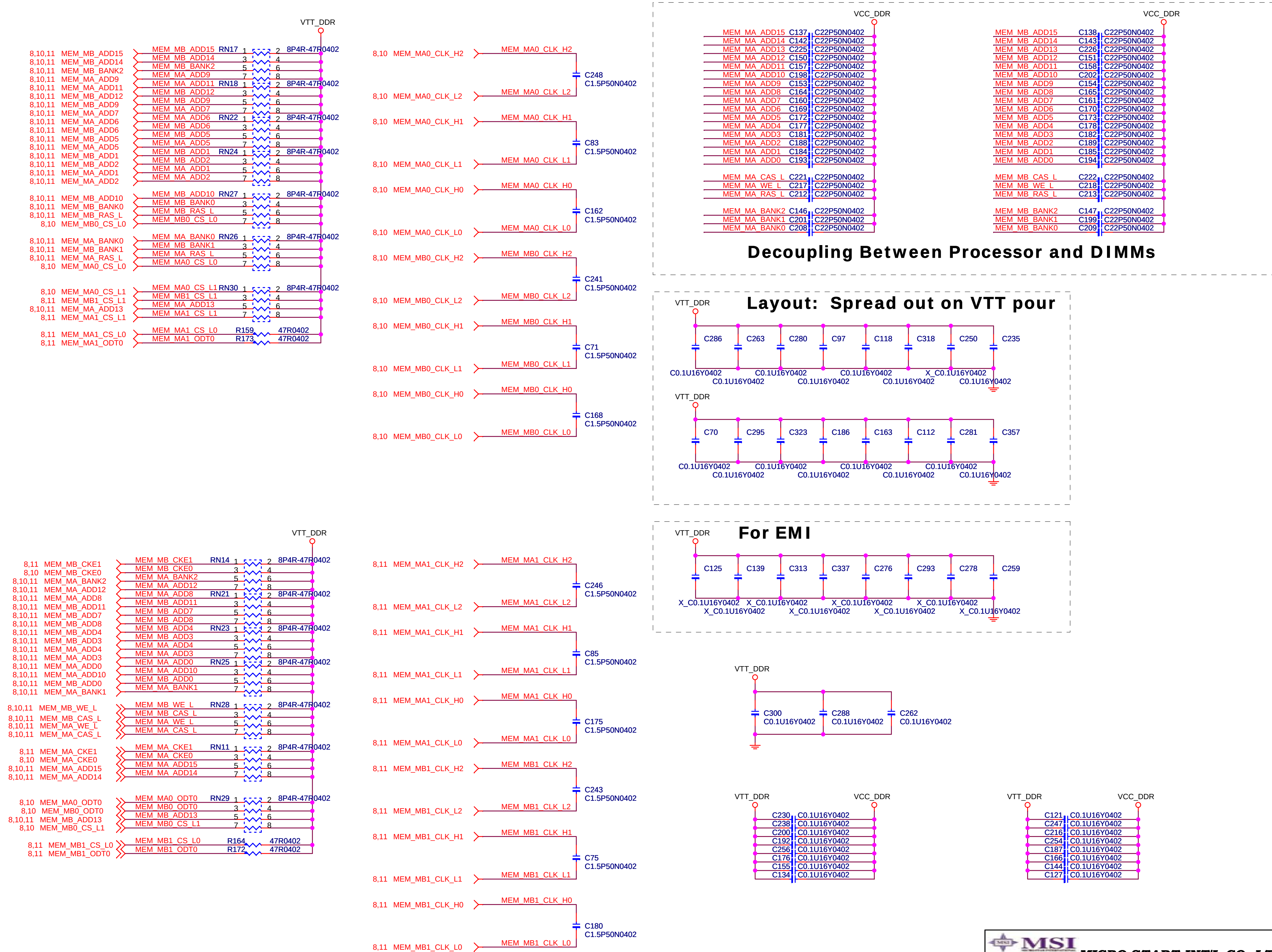
Title	SECOND LOGICAL DDR DIMM	
Size: Custom	Document Number: MS-7411	Rev: 0A
Date: Thursday, October 11, 2007	Sheet 11 of 39	



MICRO-START INT'L CO.,LTD.

Title	DDR TERMINATOR	
Size: Custom	Document Number: MS-7411	Rev: 0A
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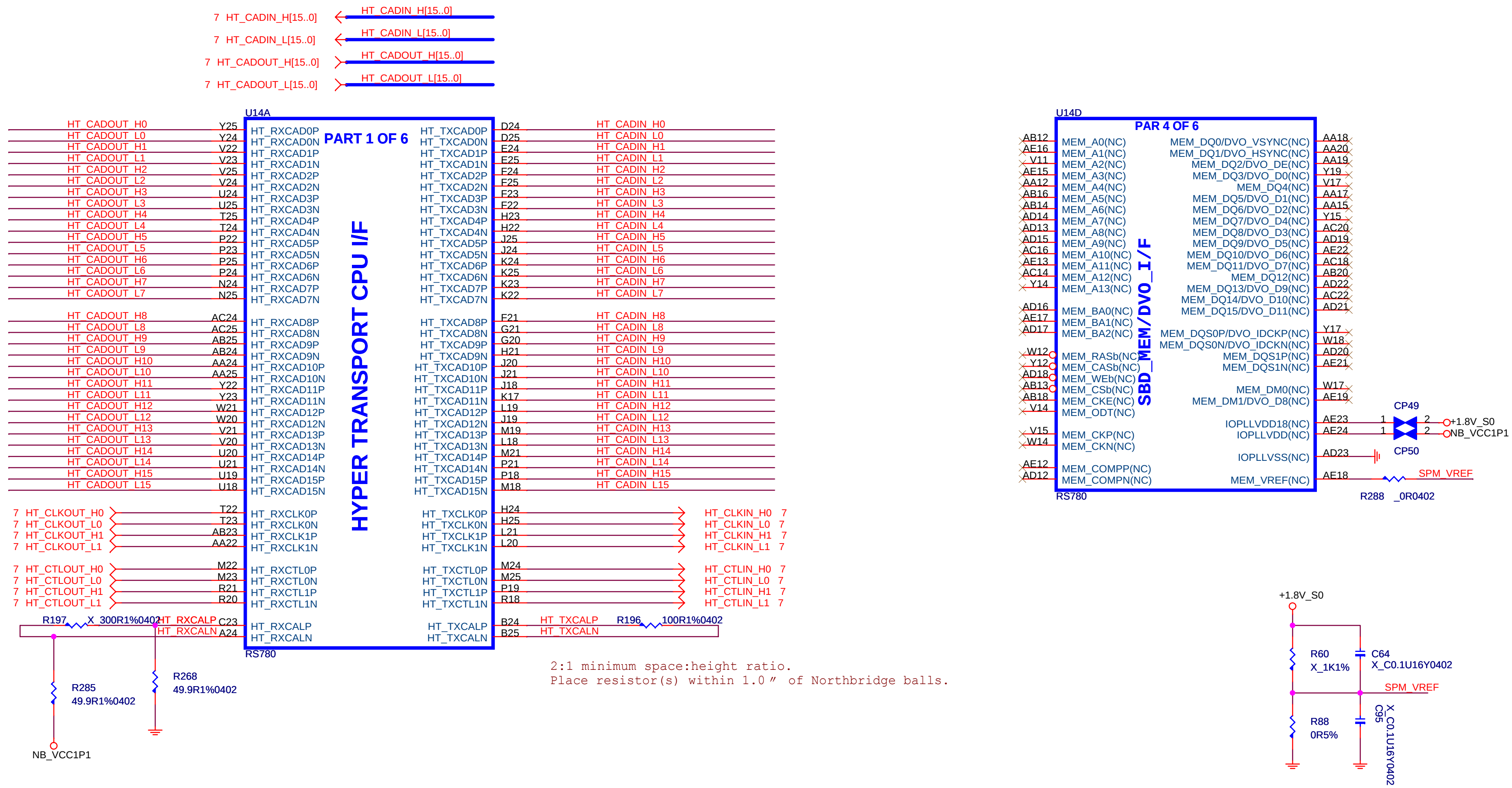
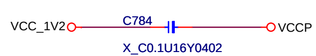
RS780-HT LINK I/F



RS740: STUFF R268,R285(49.9OHM) ;R196 100R ; UNSTUFF R197
RS780 STUFF R197,R196(1.21K) ;UNSTUFF R268,R285

2:1 minimum space:height ratio.
Place resistor(s) within 1.0″ of Northbridge balls.

Decoupling Cap for HT.



MSI MICRO-START INT'L CO.,LTD.		
Title: RS780-HT LINK I/F		
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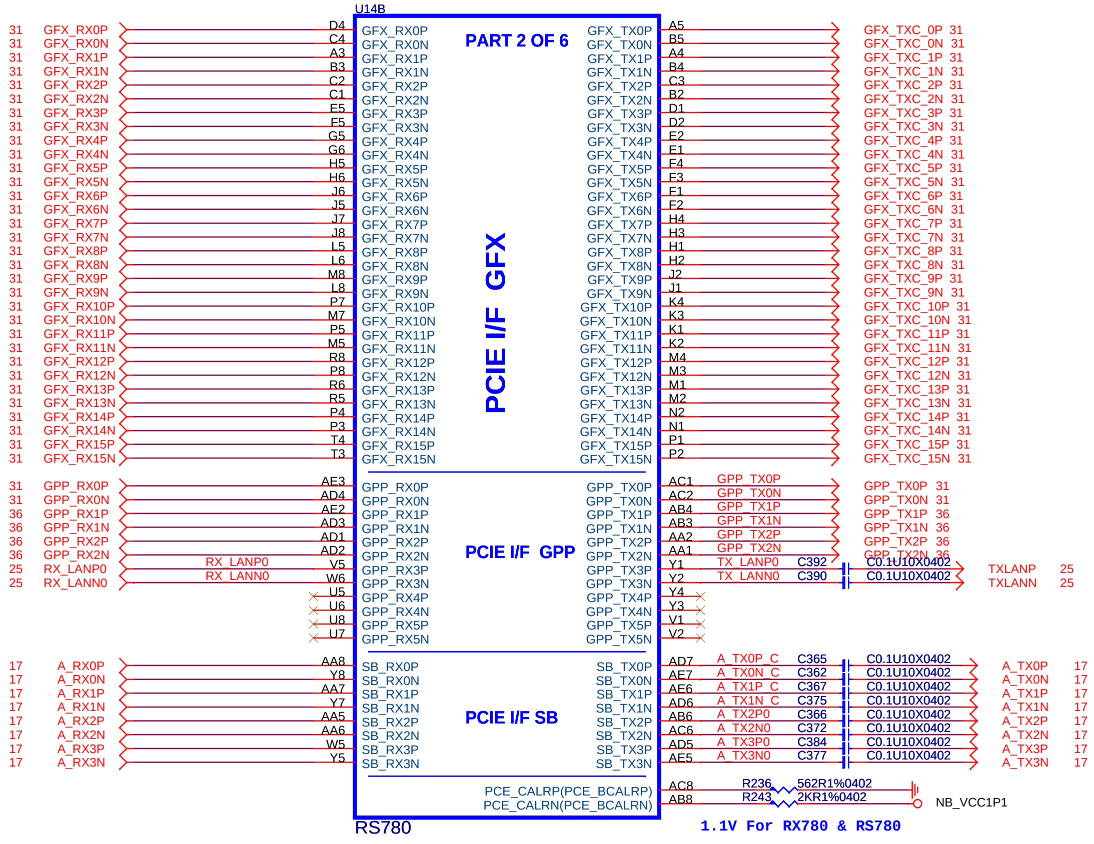
RS780-PCIE I/F



RS740: R236   562 ohm
RS780 :R236 1.27 K OHM

MSI	MICRO-START INT'L CO.,LTD.	
Title: RS780-PCIE I/F		
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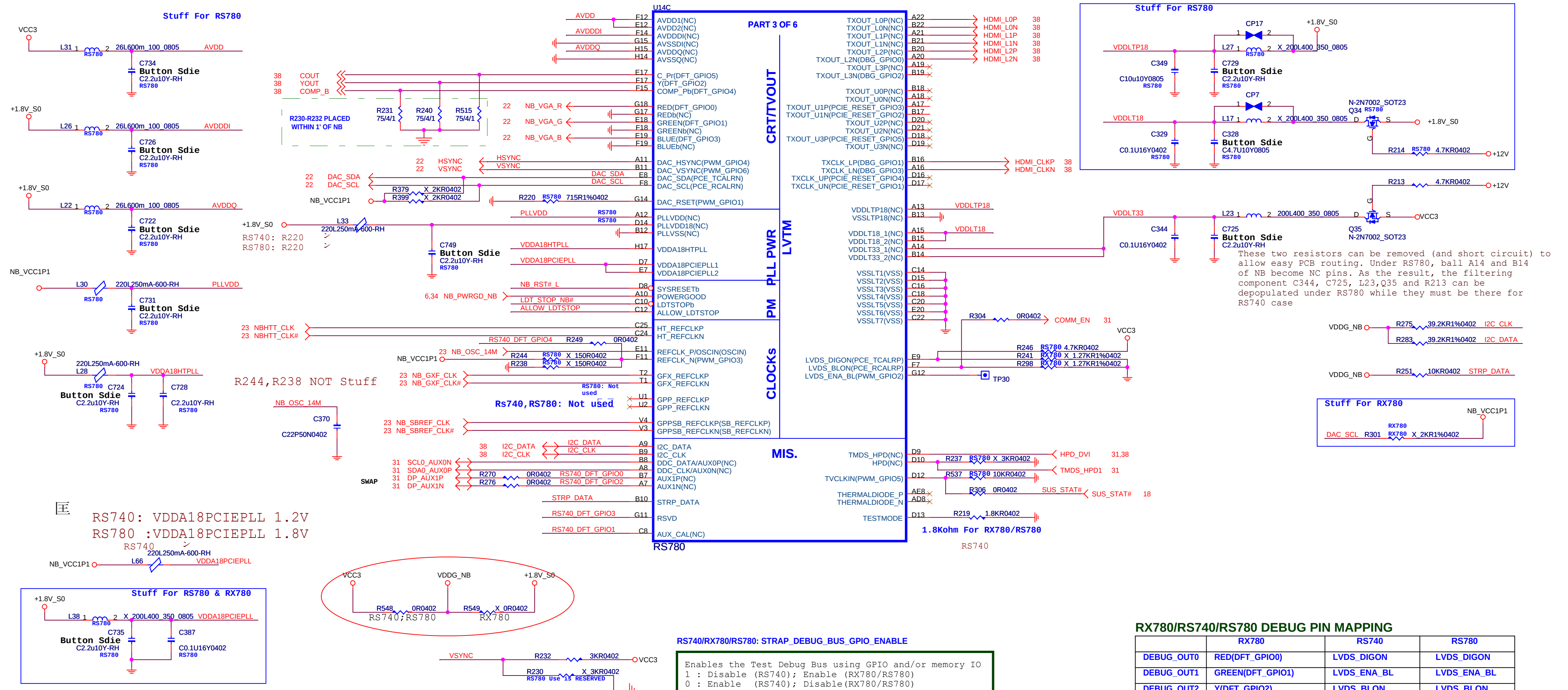
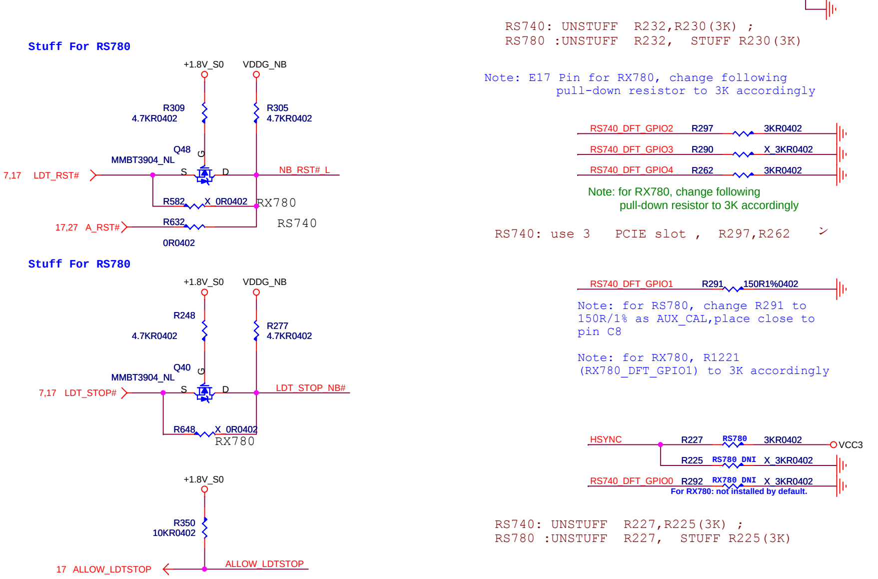
RS780-SYSTEM I/F





RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RX780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Appicable

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

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Title	RS780-SYSTEM I/F	
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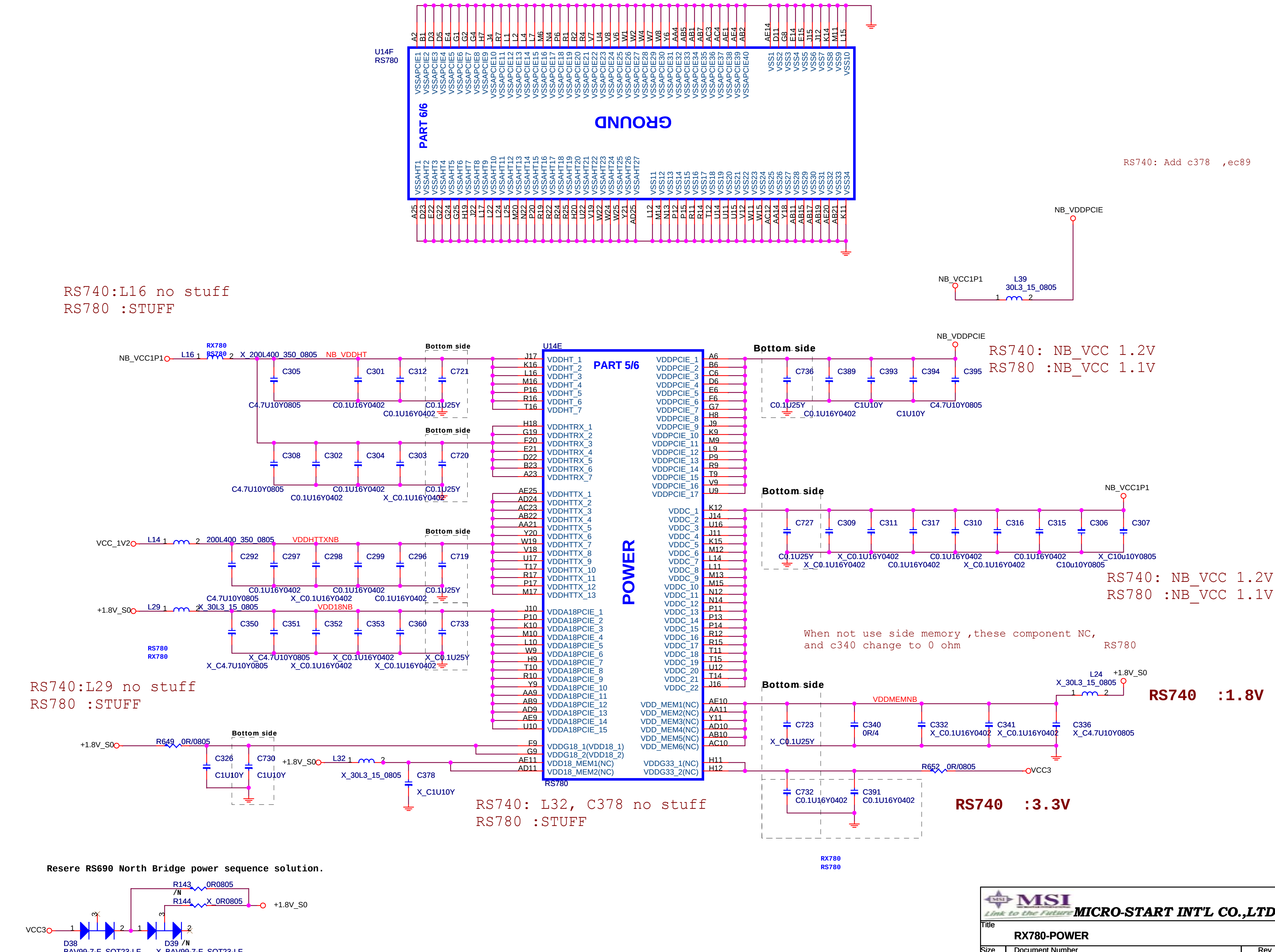

MICRO-START INT'L CO.,LTD.

Title	RX780-POWER	
Size Custom	Document Number MS-7411	Rev 0A
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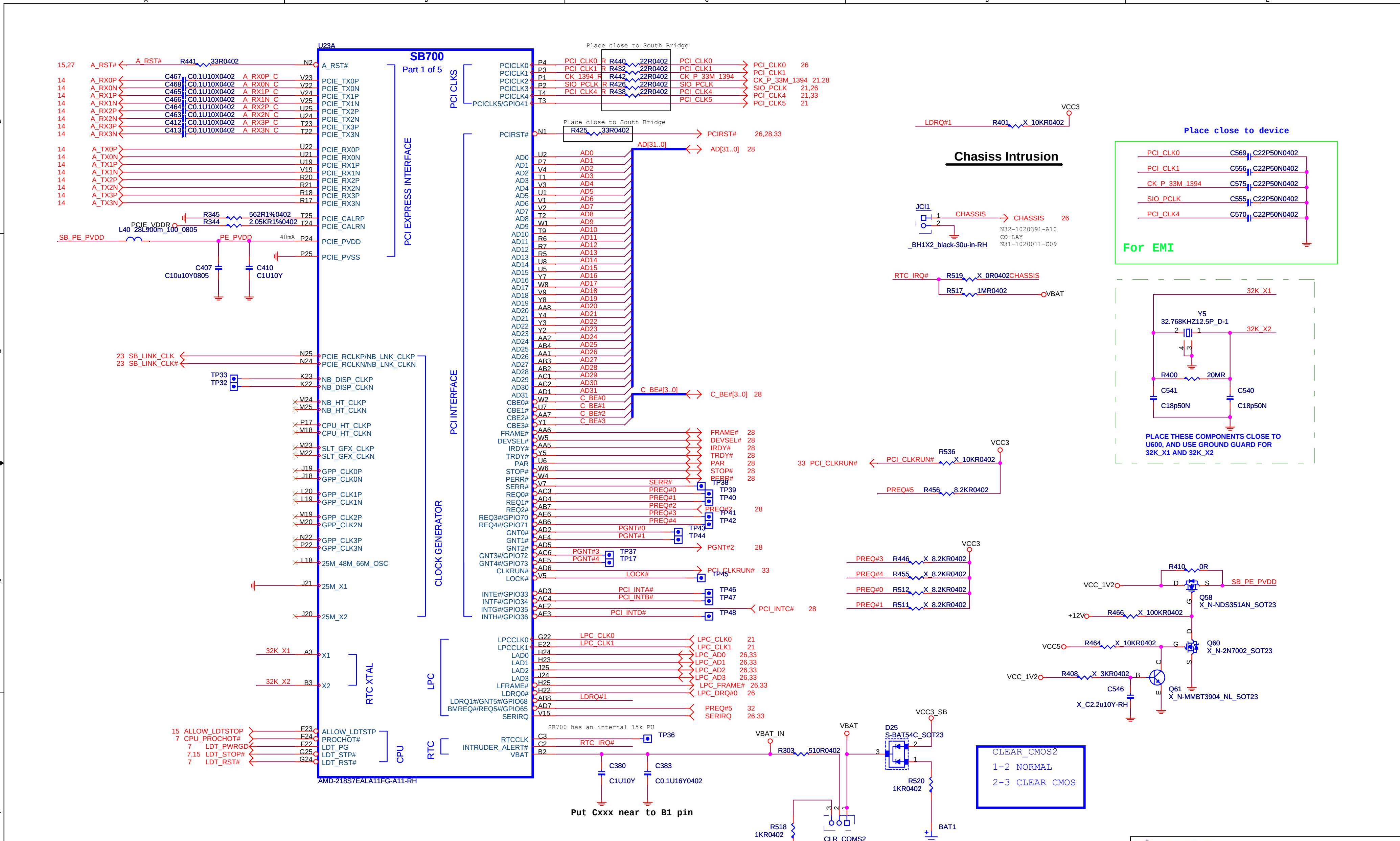
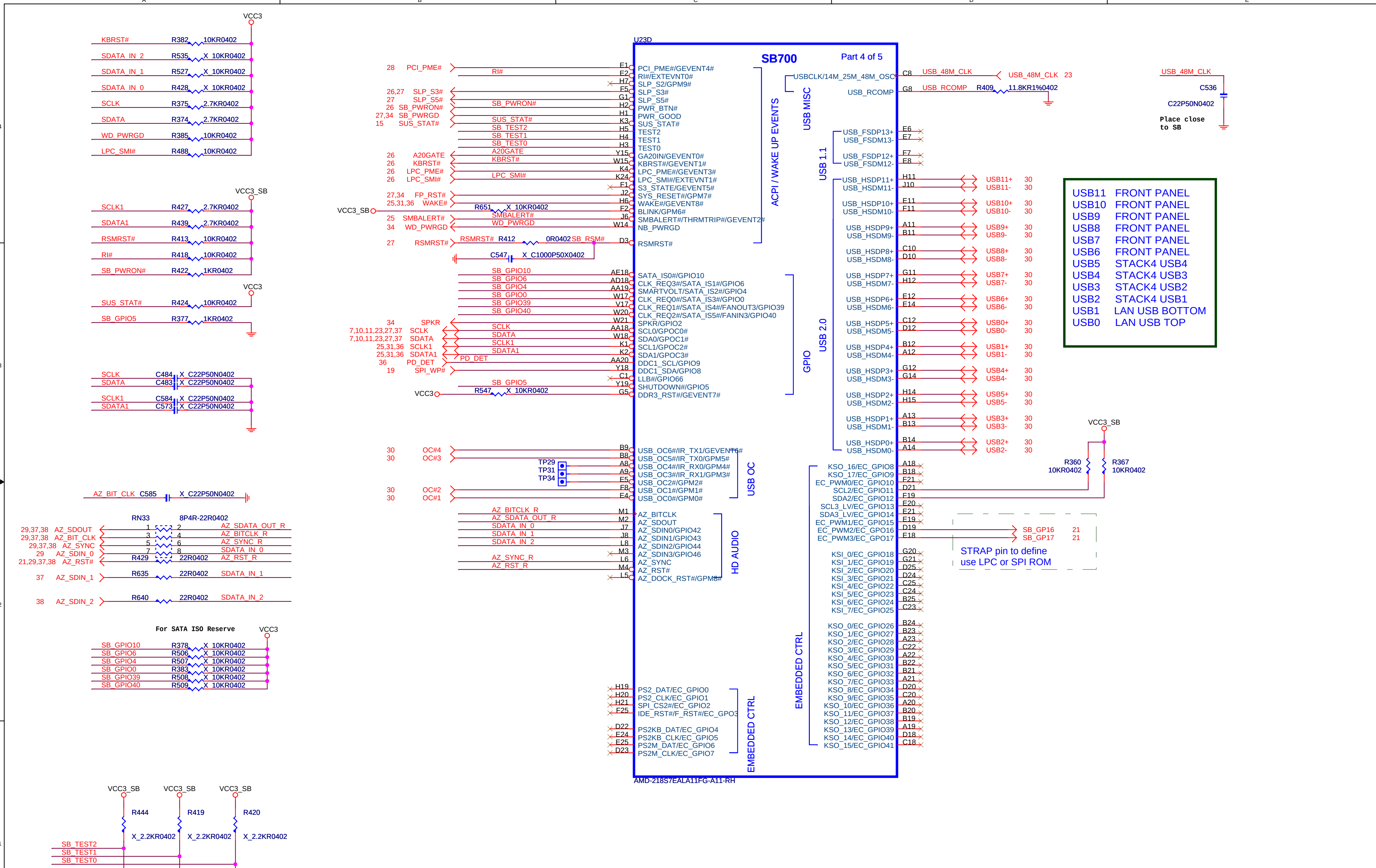


MSI MICRO-START INT'L CO.,LTD.

Title	SB700 PCIE/PCI/CPU/LPC	
Size: Custom	Document Number: MS-7411	Rev: 0A
Date: Thursday, October 11, 2007	Sheet 17 of 39	



MICRO-START INT'L CO.,LTD.

Title: SB700 ACPI/GPIO/USB/AUDIO

Size	Document Number	Rev
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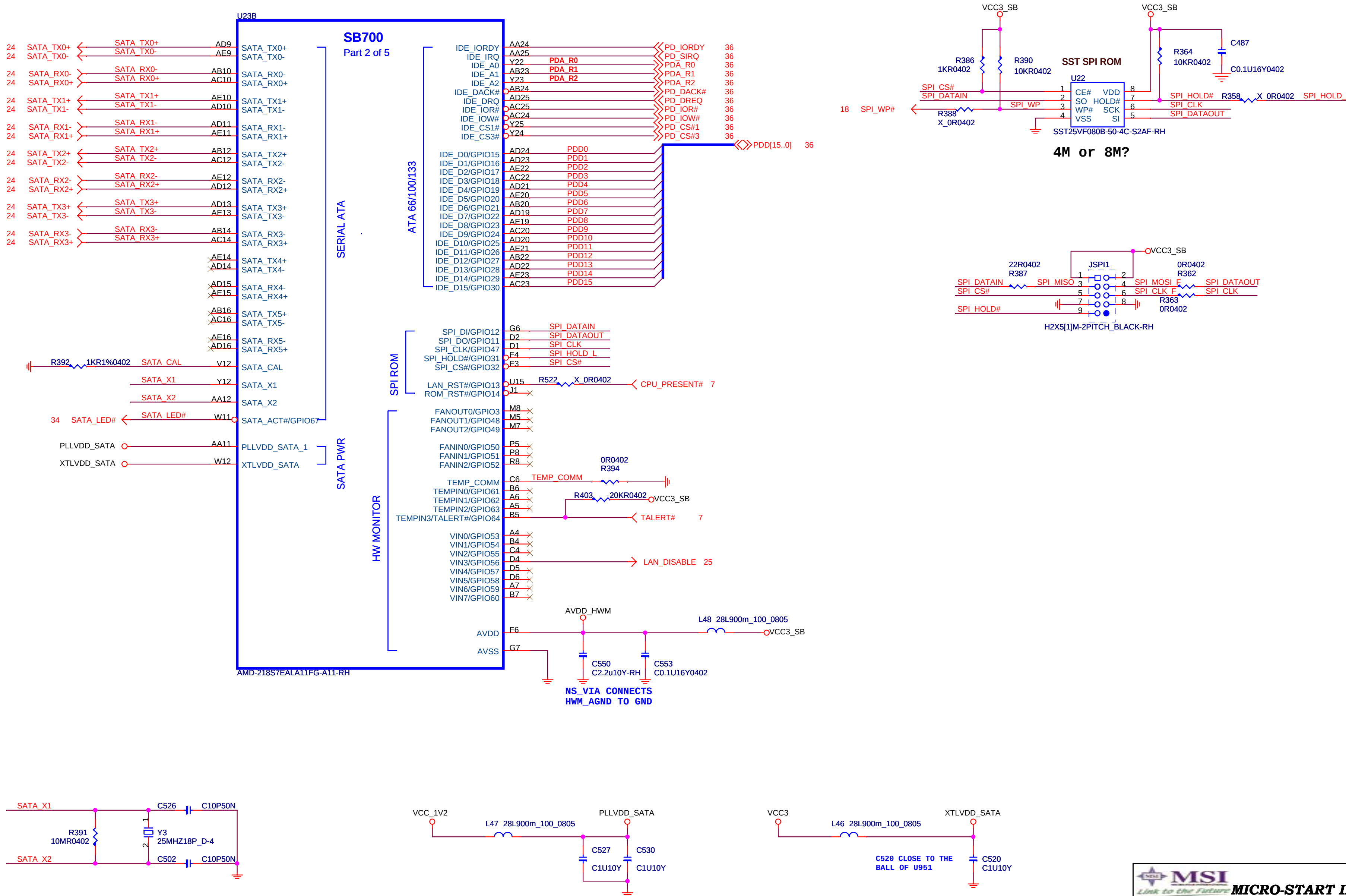

MSI MICRO-START INT'L CO.,LTD.

Title	SB600 SATA/IDE/HWM/SPI		
Size: Custom	Document Number: MS-7411		Rev: 0A
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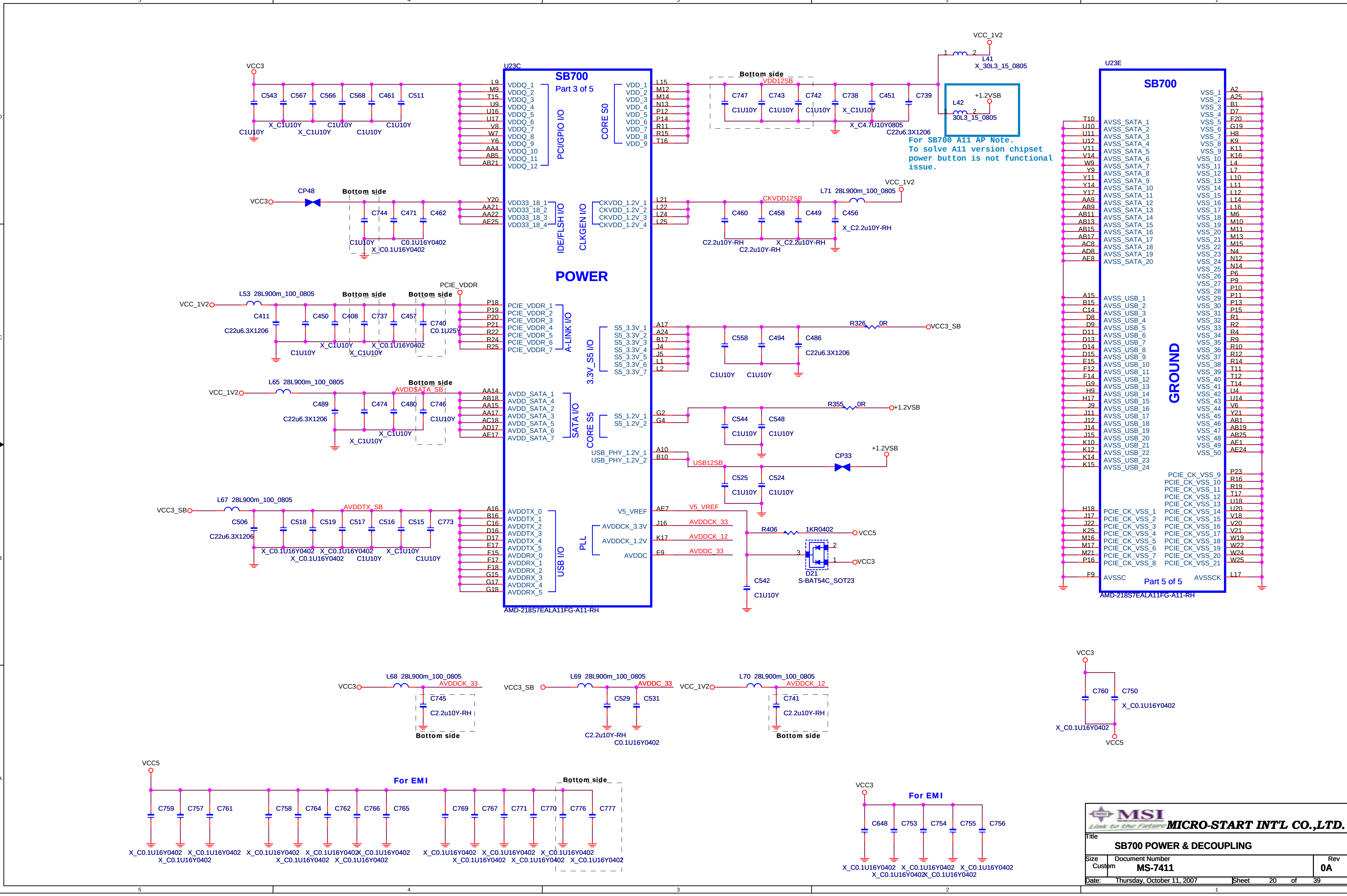

U23C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
VDDQ_1 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12
L9 M9 T15 U9 U16 U17 V8 W7 Y6 AA4 AB5 AB21
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9
L15 M12 M14 N13 P12 P14 R11 R15 T16
VDD33_18_1 VDD33_18_2 VDD33_18_3 VDD33_18_4
Y20 AA21 AA22 AE25
CKVDD_1.2V_1 CKVDD_1.2V_2 CKVDD_1.2V_3 CKVDD_1.2V_4
L21 L22 L24 L25
PCIE_VDDR_1 PCIE_VDDR_2 PCIE_VDDR_3 PCIE_VDDR_4 PCIE_VDDR_5 PCIE_VDDR_6 PCIE_VDDR_7
P18 P19 P20 P21 R22 R24 R25
S5_3.3V_1 S5_3.3V_2 S5_3.3V_3 S5_3.3V_4 S5_3.3V_5 S5_3.3V_6 S5_3.3V_7
A17 A24 B17 J4 J5 L1 L2
AVDD_SATA_1 AVDD_SATA_4 AVDD_SATA_2 AVDD_SATA_3 AVDD_SATA_5 AVDD_SATA_6 AVDD_SATA_7
AA14 AB18 AA15 AA17 AC18 AD17 AE17
S5_1.2V_1 S5_1.2V_2
G2 G4
USB_PHY_1.2V_1 USB_PHY_1.2V_2
A10 B10
AVDDTX_0 AVDDTX_1 AVDDTX_2 AVDDTX_3 AVDDTX_4 AVDDTX_5 AVDDRX_0 AVDDRX_1 AVDDRX_2 AVDDRX_3 AVDDRX_4 AVDDRX_5
A16 B16 C16 D16 D17 E17 F15 F17 F18 G15 G17 G18
V5_VREF AVDDCK_3.3V AVDDCK_1.2V AVDDC
AE7 J16 K17 F9
AMD-218S7EALA11FG-A11-RH
VCC3
C543 C567 C566 C568 C461 C511
C1U10Y X_C1U10Y X_C1U10Y C1U10Y C1U10Y C1U10Y
Bottom side
VDD12SB
C747 C743 C742 C738 C451 C739
C1U10Y C1U10Y C1U10Y X_C1U10Y X_C4.7U10Y0805 C22u6.3X1206
VCC_1V2
L41
X_30L3_15_0805
+1.2VSB
L42
30L3_15_0805
For SB700 A11 AP Note.
To solve A11 version chipset
power button is not functional
issue.
CP48
C744 C471 C462
C1U10Y C0.1U16Y0402 X_C0.1U16Y0402
CKVDD12SB
L71 28L900m_100_0805
C460 C458 C449 C456
C2.2u10Y-RH C2.2u10Y-RH X_C2.2u10Y-RH X_C2.2u10Y-RH
PCIE_VDDR
L53 28L900m_100_0805
VCC_1V2
C411 C450 C408 C737 C457 C740
C22u6.3X1206 C1U10Y X_C1U10Y X_C1U10Y X_C0.1U16Y0402 C0.1U25Y
C558 C494 C486
C1U10Y C1U10Y C22u6.3X1206
R326 0R
VCC3_SB
L65 28L900m_100_0805
AVDDSATA_SB
C489 C474 C480 C746
C22u6.3X1206 X_C1U10Y X_C1U10Y C1U10Y
R355 0R
+1.2VSB
C544 C548
C1U10Y C1U10Y
CP33
USB12SB
C525 C524
C1U10Y C1U10Y
L67 28L900m_100_0805
VCC3_SB
AVDDTX_SB
C506 C518 C519 C517 C516 C515 C773
C22u6.3X1206 X_C0.1U16Y0402 X_C0.1U16Y0402 X_C0.1U16Y0402 C1U10Y X_C1U10Y C1U10Y
V5_VREF
AVDDCK_33
AVDDCK_12
AVDDC_33
R406 1KR0402
VCC5
D21
S-BAT54C_SOT23
VCC3
C542
C1U10Y
U23E
SB700
GROUND
Part 5 of 5
AVSS_SATA_1 … AVSS_SATA_20
T10 U10 U11 U12 V11 V14 W9 Y9 Y11 Y14 Y17 AA9 AB9 AB11 AB13 AB15 AB17 AC8 AD8 AE8
AVSS_USB_1 … AVSS_USB_24
A15 B15 C14 D8 D9 D11 D13 D14 D15 E15 F12 F14 G9 H9 H17 J9 J11 J12 J14 J15 K10 K12 K14 K15
PCIE_CK_VSS_1 … PCIE_CK_VSS_21
H18 J17 J22 K25 M16 M17 M21 P16
AVSSC AVSSCK
F9 L17
VSS_1 … VSS_50
A2 A25 B1 D7 F20 G19 H8 K9 K11 K16 L4 L7 L10 L11 L12 L14 L16 M6 M10 M11 M13 M15 N4 N12 N14 P6 P9 P10 P11 P13 P15 R1 R2 R4 R9 R10 R12 R14 T11 T12 T14 U4 U14 V6 Y21 AB1 AB19 AB25 AE1 AE24
P23 R16 R19 T17 U18 U20 V18 V20 V21 W19 W22 W24 W25
AMD-218S7EALA11FG-A11-RH
L68 28L900m_100_0805
VCC3
AVDDCK_33
C745
C2.2u10Y-RH
Bottom side
L69 28L900m_100_0805
VCC3_SB
AVDDC_33
C529 C531
C2.2u10Y-RH C0.1U16Y0402
L70 28L900m_100_0805
VCC_1V2
AVDDCK_12
C741
C2.2u10Y-RH
Bottom side
VCC3
C760 C750
X_C0.1U16Y0402 X_C0.1U16Y0402
VCC5
VCC5
For EMI
Bottom side
C759 C757 C761 C758 C764 C762 C766 C765 C769 C767 C771 C770 C776 C777
X_C0.1U16Y0402
VCC3
For EMI
C648 C753 C754 C755 C756
X_C0.1U16Y0402
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
SB700 POWER & DECOUPLING
Size Custom
Document Number
MS-7411
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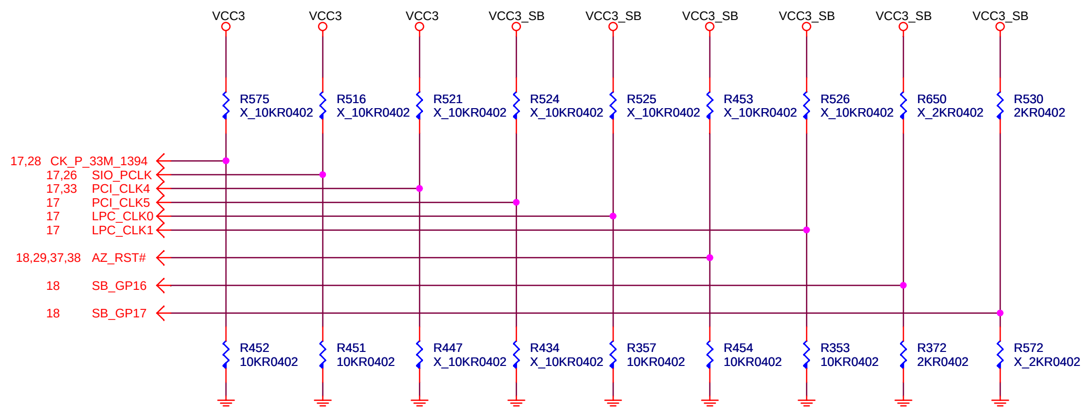
REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	PCI_CLK2 CK_P_33M_1394	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	Booting from PCI Memory	Internal Clock Generator	INTERNAL RTC	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED	L, H = LPC ROM L, L = FWH ROM
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT	Note: NC represents internal 10-k? 5% pull-up

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: SB700 STRAPS

Size: B | Document Number: MS-7411 | Rev: 0A

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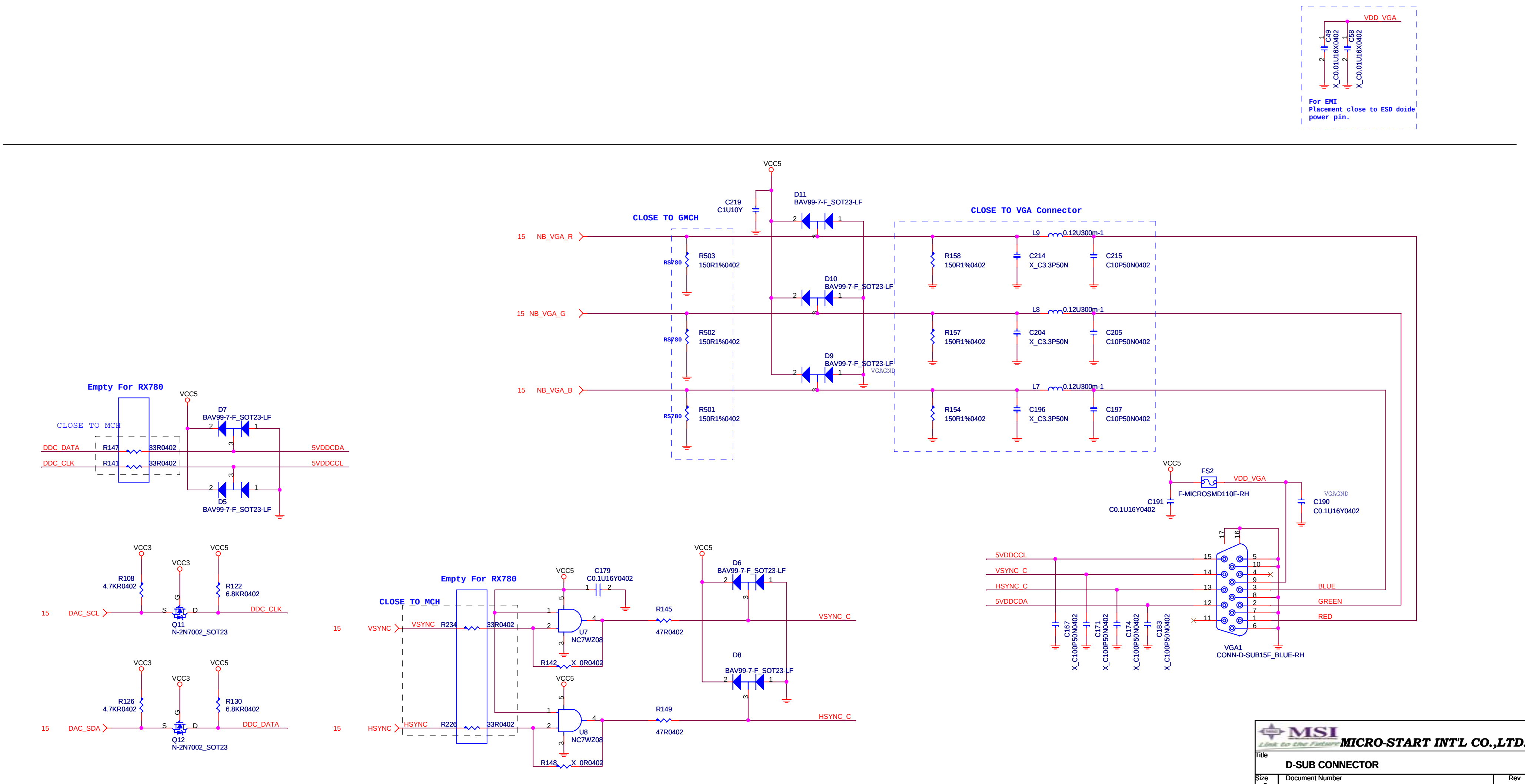
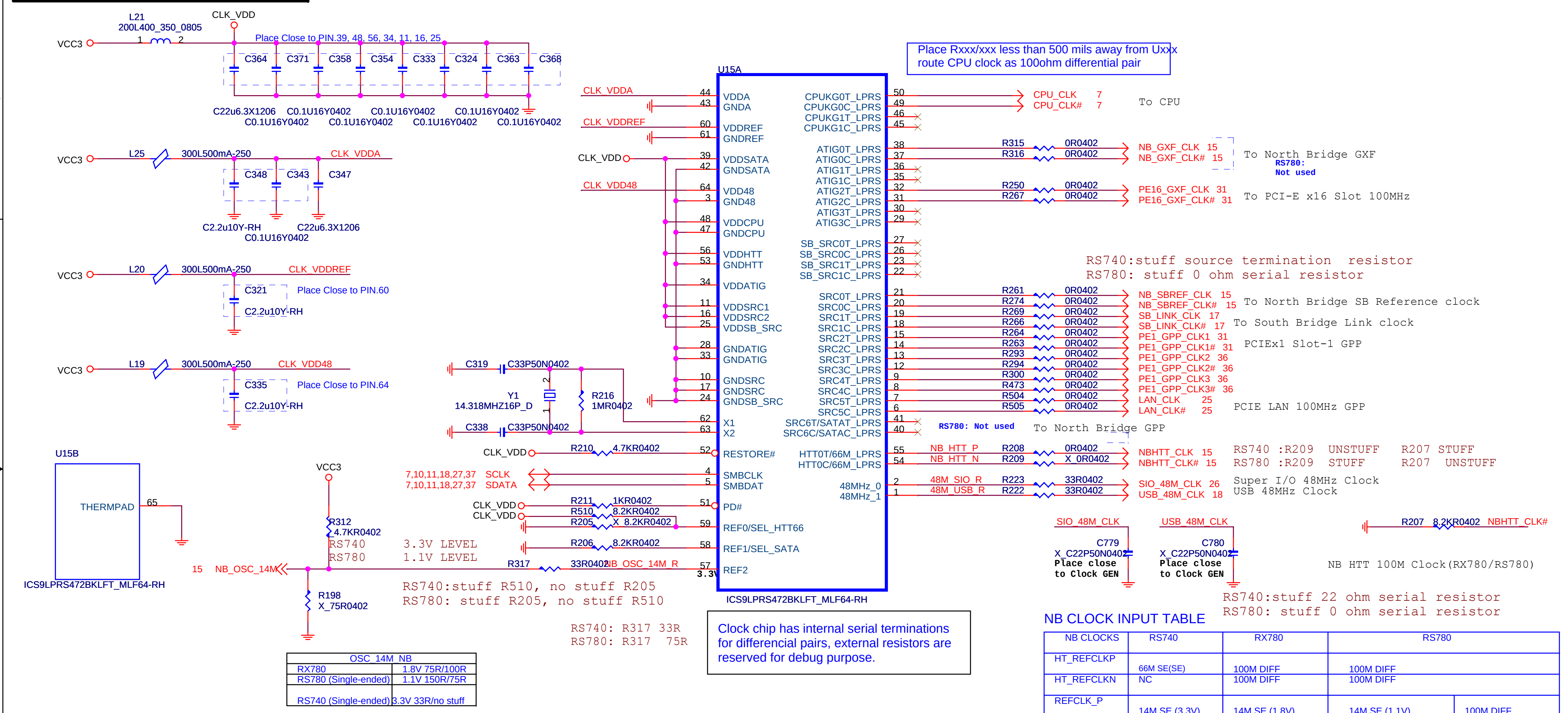
DVI CONNECTOR



MSI	MICRO-START INT'L CO.,LTD.	
Title	D-SUB CONNECTOR	
Size C	Document Number MS-7411	Rev 0A
Date: Thursday, October 11, 2007	Sheet 22 of 39	

Clock Gen ICS9LPR472



OSC_14M_NB	
RX780	1.8V 75R/100R
RS780 (Single-ended)	1.1V 150R/75R
RS740 (Single-ended)	3.3V 33R/no stuff

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

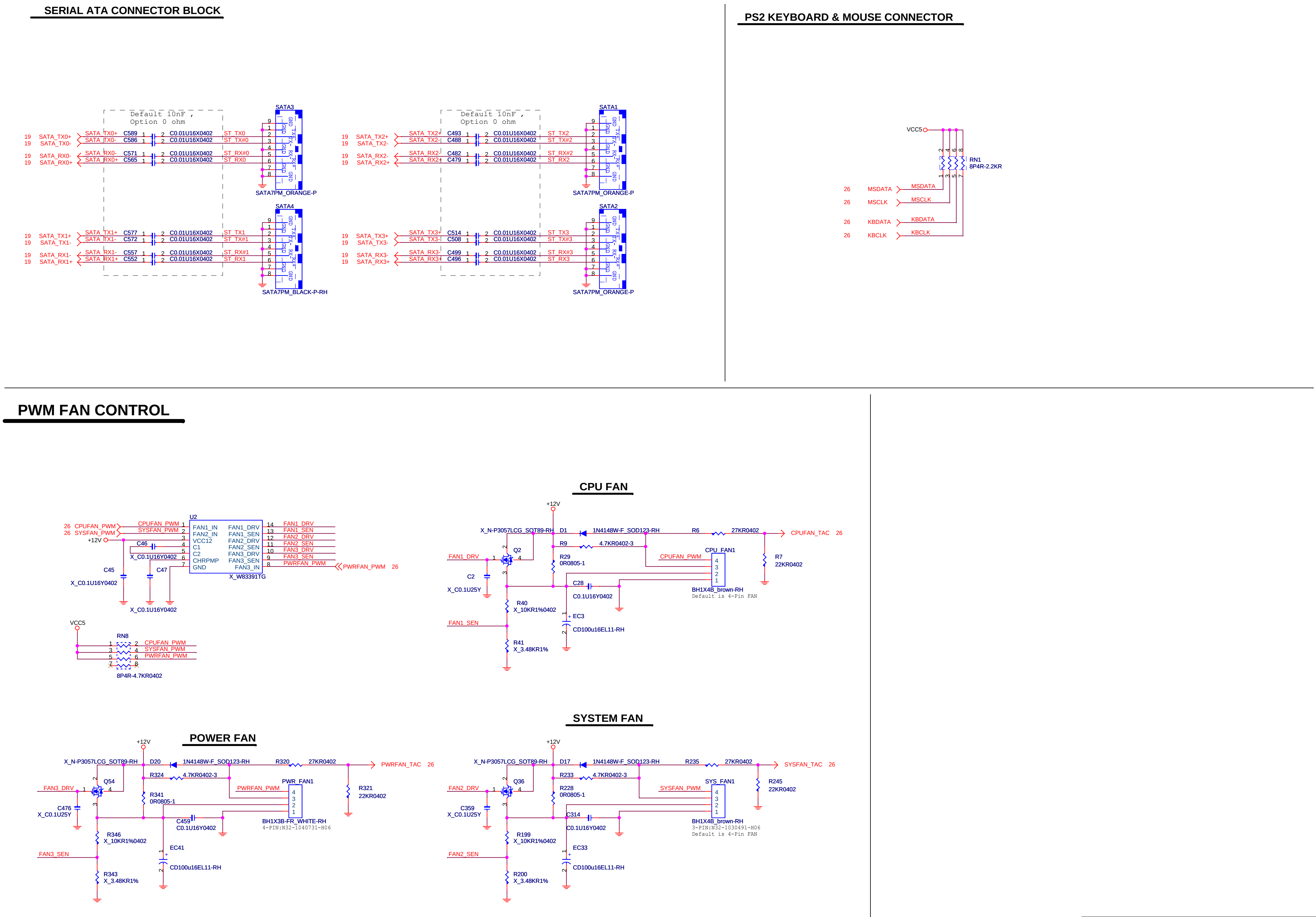
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

MICRO-START INT'L CO.,LTD.

Title	Clock Gen ICS9LPR472	
Size B	Document Number MS-7411	Rev 0A
Date: Thursday, October 11, 2007	Sheet 23 of 39	



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Link to the Future
MICRO-START INT'L CO.,LTD.

Title	SATA & COM1	
Size C	Document Number MS-7411	Rev 0A
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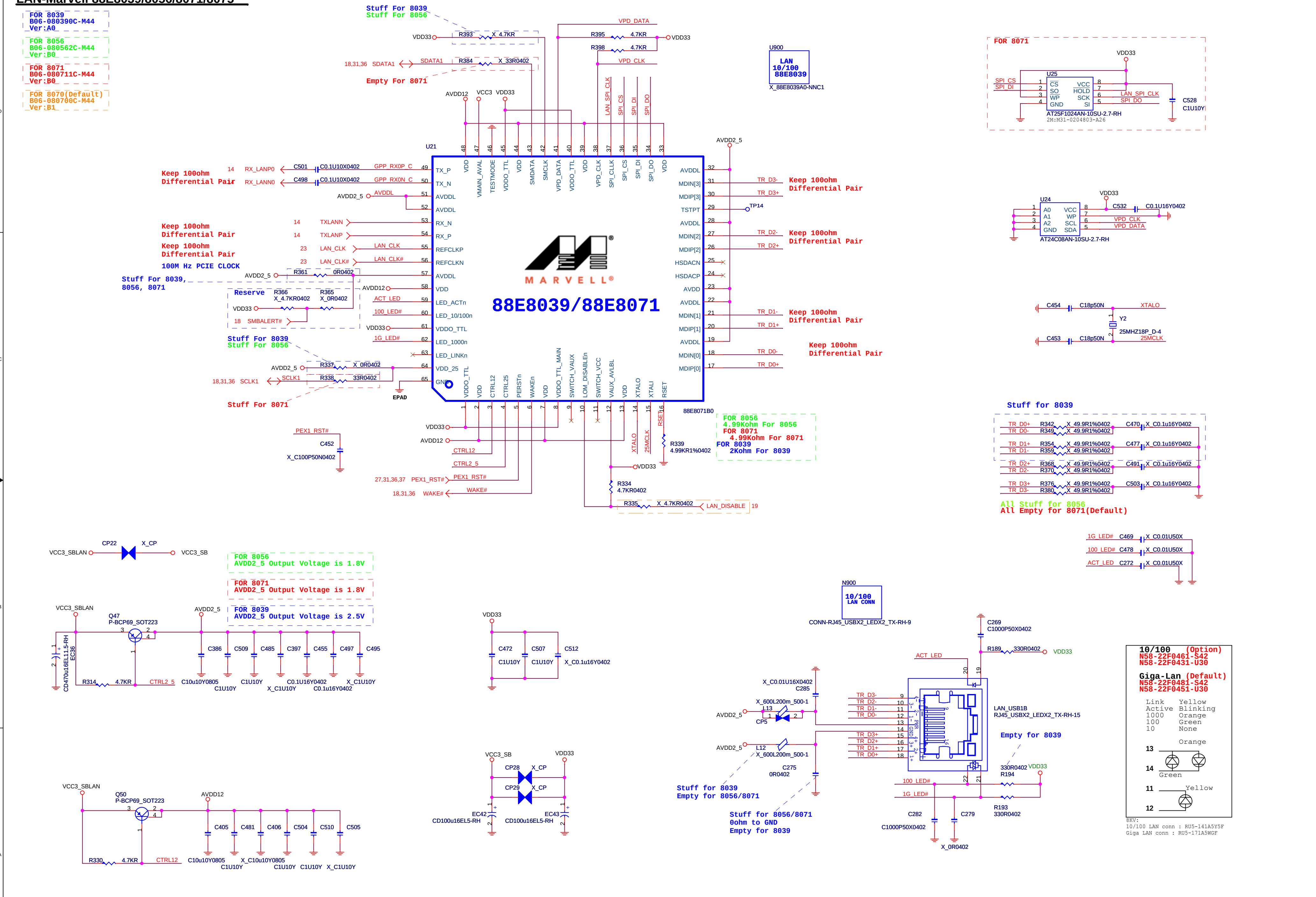
LAN-Marvell 88E8039/8056/8071/8075



MSI MICRO-START INT'L CO.,LTD.

Title	LAN-Marvell 88E8039/8056/8071		
Size: C	Document Number: MS-7411		Rev: 0A
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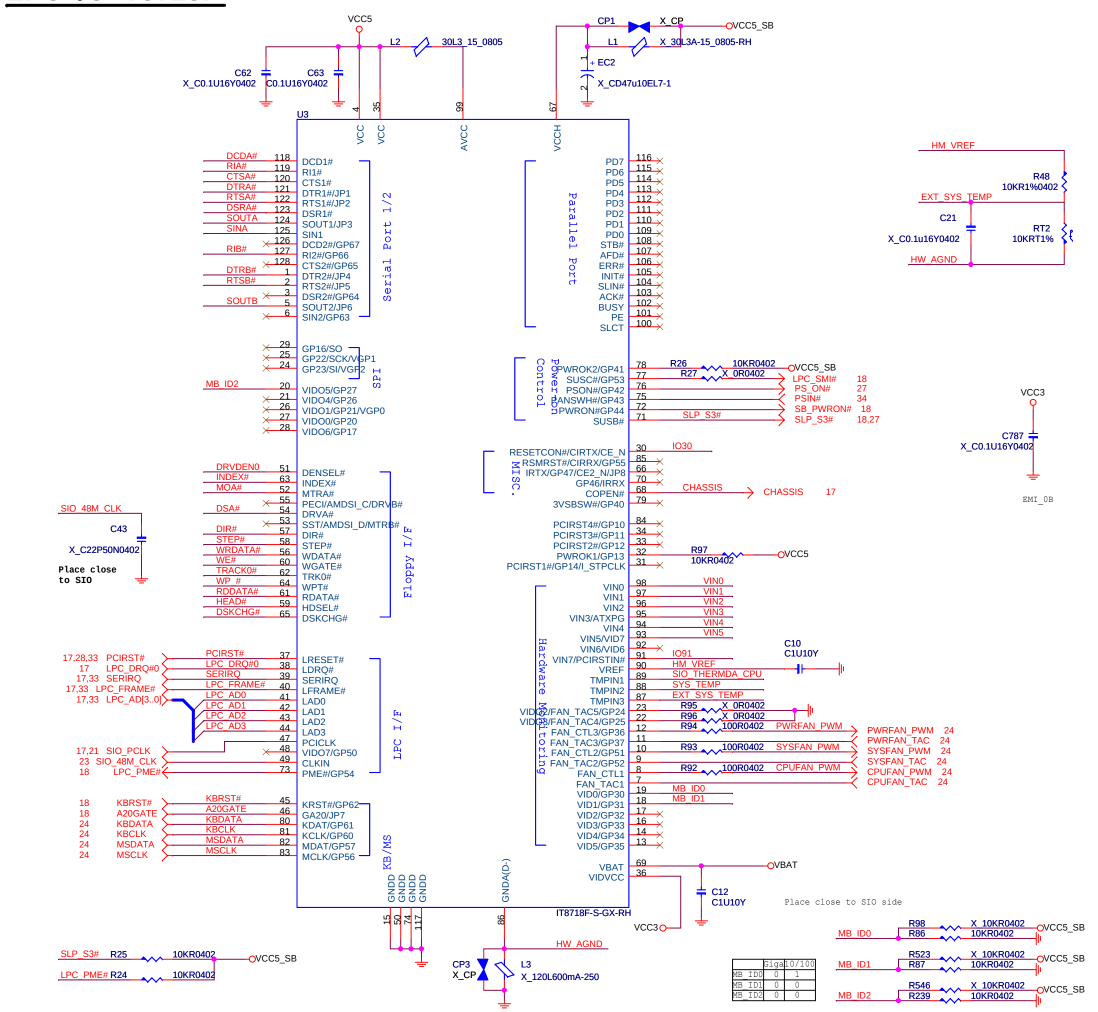
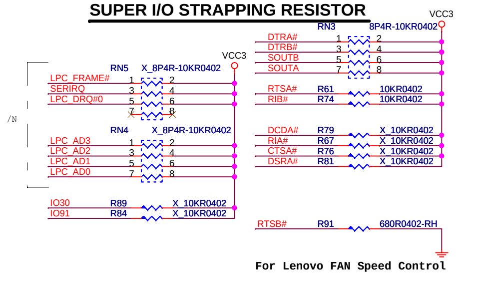
LPC I/O IT8718F



SUPER I/O STRAPPING RESISTOR



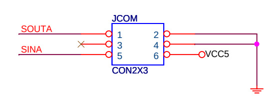
Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
	0	Flash I/F Address Segment 1 (FFFE_0000h~FFFF_FFFFh, 000F_0000h~000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
	0	Enable VIDOUT pins
CHIP_SEL	--	Chip selection in configuration.
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
	0	The output buffers are push-pull.
FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
	0	The default value of EC Index 15h / 16h / 17h is 40h
VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
	0	The threshold voltage of VID is 0.8 / 0.4V

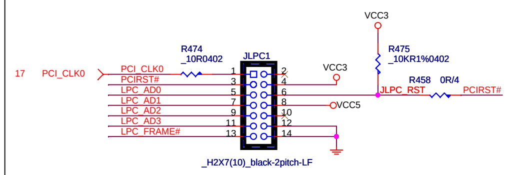
BIOS WRITE PROTECT

Super I/O Chassis

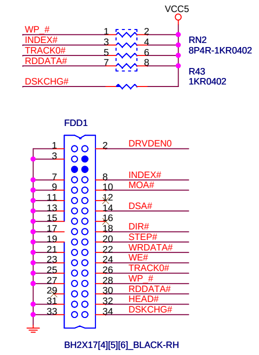
SERIAL PORT 1



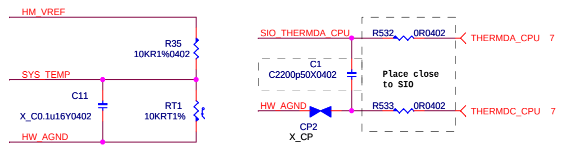
LPC DEBUG PORT



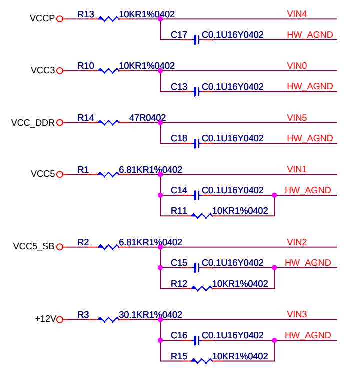
FLOPPY CONNECTOR



PARALLEL PORT



Thermal Resistor



MSI MICRO-START INT'L CO.,LTD.

Title	LPC I/O IT8718F	
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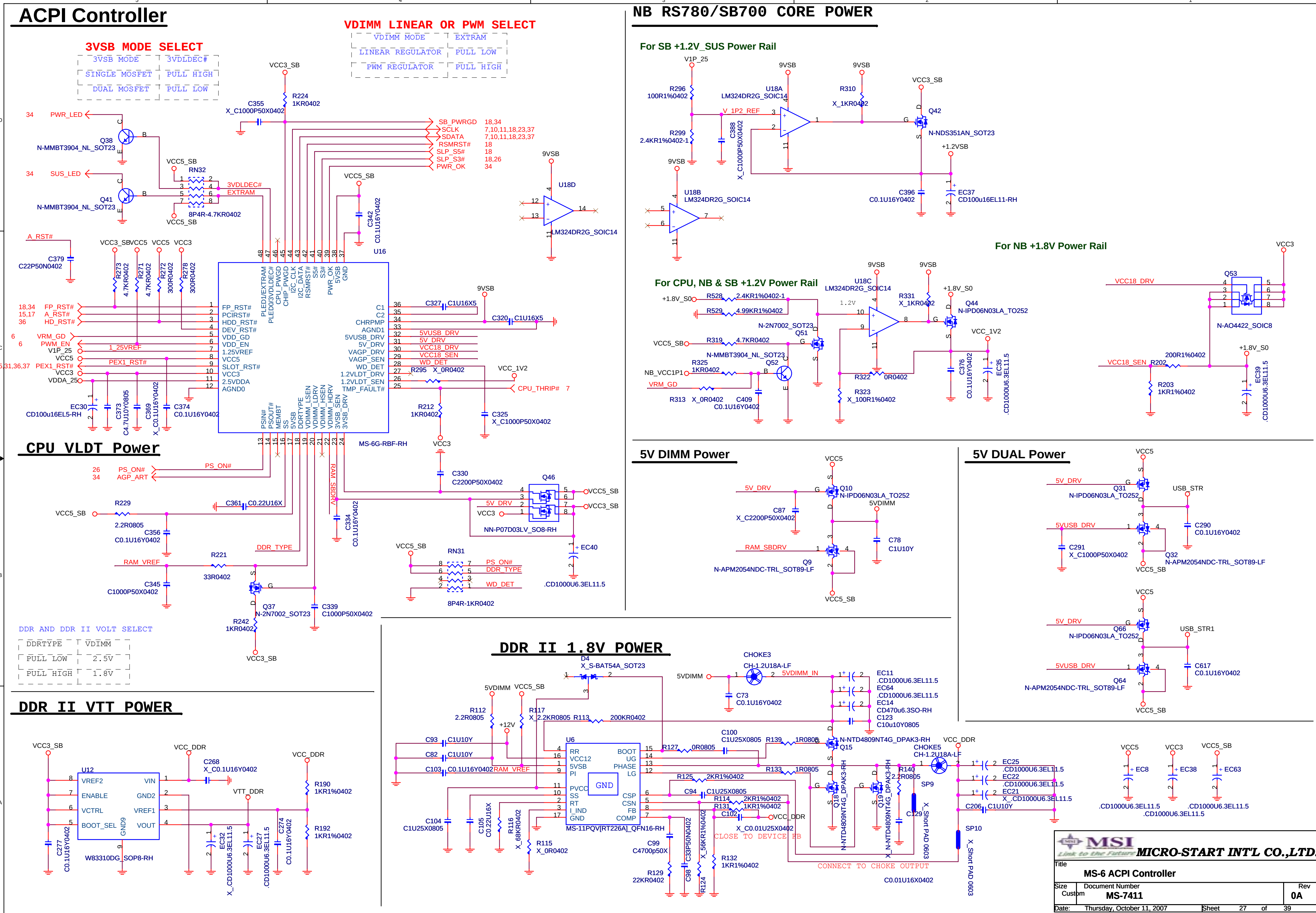
ACPI Controller
3VSB MODE SELECT
3VSB MODE | 3VDLDEC#
SINGLE MOSFET | PULL HIGH
DUAL MOSFET | PULL LOW
VDIMM LINEAR OR PWM SELECT
VDIMM MODE | EXTRAM
LINEAR REGULATOR | PULL LOW
PWM REGULATOR | PULL HIGH
NB RS780/SB700 CORE POWER
For SB +1.2V_SUS Power Rail
For NB +1.8V Power Rail
For CPU, NB & SB +1.2V Power Rail
U16
MS-6G-RBF-RH
PWR_LED
SUS_LED
Q38 N-MMBT3904_NL_SOT23
Q41 N-MMBT3904_NL_SOT23
RN32 8P4R-4.7KR0402
SB_PWRGD
SCLK
SDATA
RSMRST#
SLP_S5#
SLP_S3#
PWR_OK
U18A LM324DR2G_SOIC14
U18B LM324DR2G_SOIC14
U18C LM324DR2G_SOIC14
U18D LM324DR2G_SOIC14
Q42 N-NDS351AN_SOT23
Q44 N-IPD06N03LA_TO252
Q53 N-AO4422_SOIC8
CPU VLDT Power
Q46 NN-P07D03LV_SO8-RH
Q37 N-2N7002_SOT23
RN31 8P4R-1KR0402
DDR AND DDR II VOLT SELECT
DDRTYPE | VDIMM
PULL LOW | 2.5V
PULL HIGH | 1.8V
5V DIMM Power
Q10 N-IPD06N03LA_TO252
Q9 N-APM2054NDC-TRL_SOT89-LF
5V DUAL Power
Q31 N-IPD06N03LA_TO252
Q32 N-APM2054NDC-TRL_SOT89-LF
Q66 N-IPD06N03LA_TO252
Q64 N-APM2054NDC-TRL_SOT89-LF
DDR II 1.8V POWER
D4 X_S-BAT54A_SOT23
CHOKE3 CH-1.2U18A-LF
CHOKE5 CH-1.2U18A-LF
U6 MS-11PQV[RT226A]_QFN16-RH
Q15 N-NTD4809NT4G_DPAK3-RH
CLOSE TO DEVICE PB
CONNECT TO CHOKE OUTPUT
DDR II VTT POWER
U12 W83310DG_SOP8-RH
MICRO-START INT'L CO.,LTD.
Title
MS-6 ACPI Controller
Size Custom
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Rev 0A
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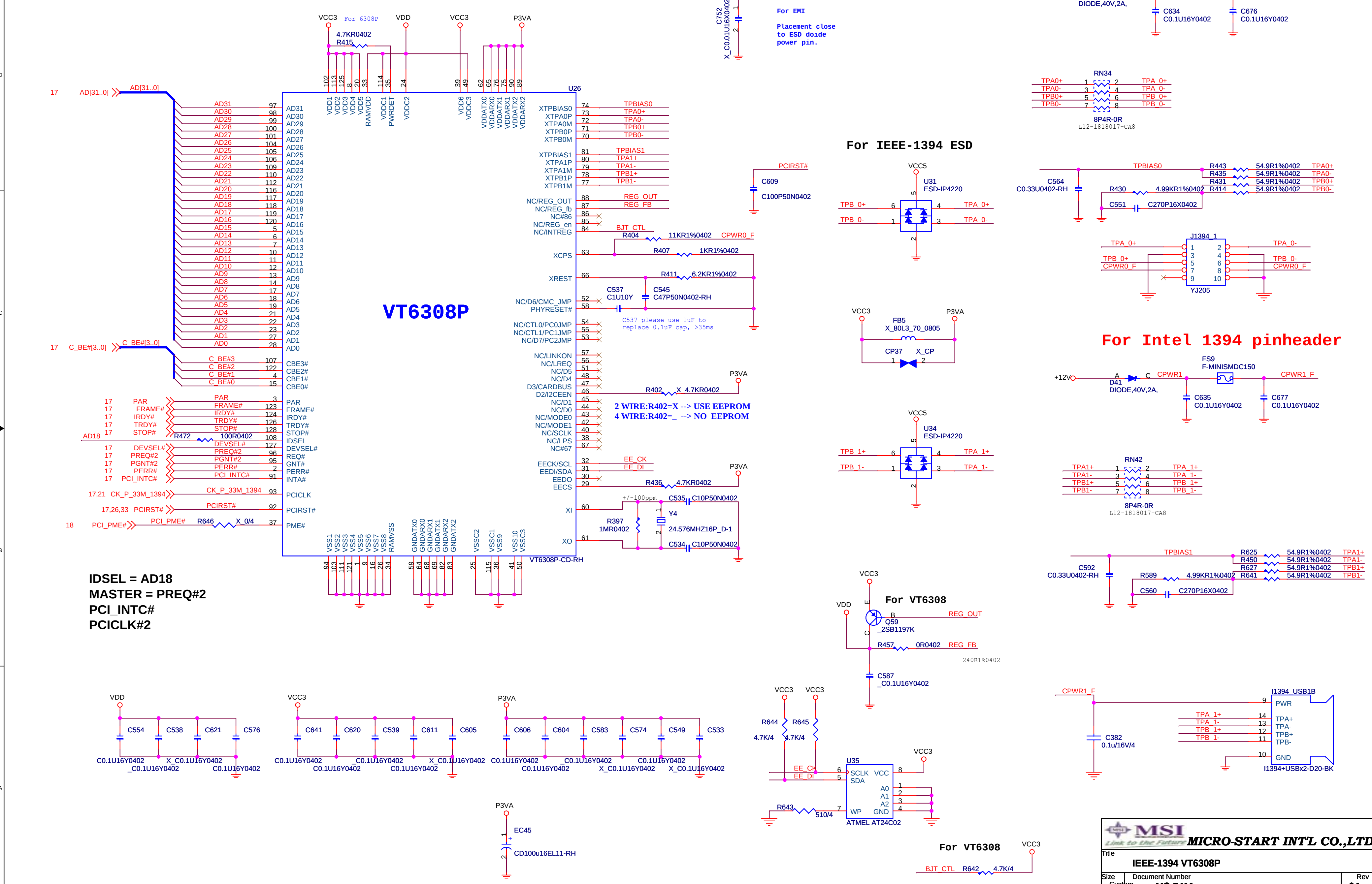
IEEE-1394 VT6308P



IDSEL = AD18
MASTER = PREQ#2
PCI_INTC#
PCICLK#2

MICRO-START INT'L CO.,LTD.

Title	IEEE-1394 VT6308P
Size	Custom
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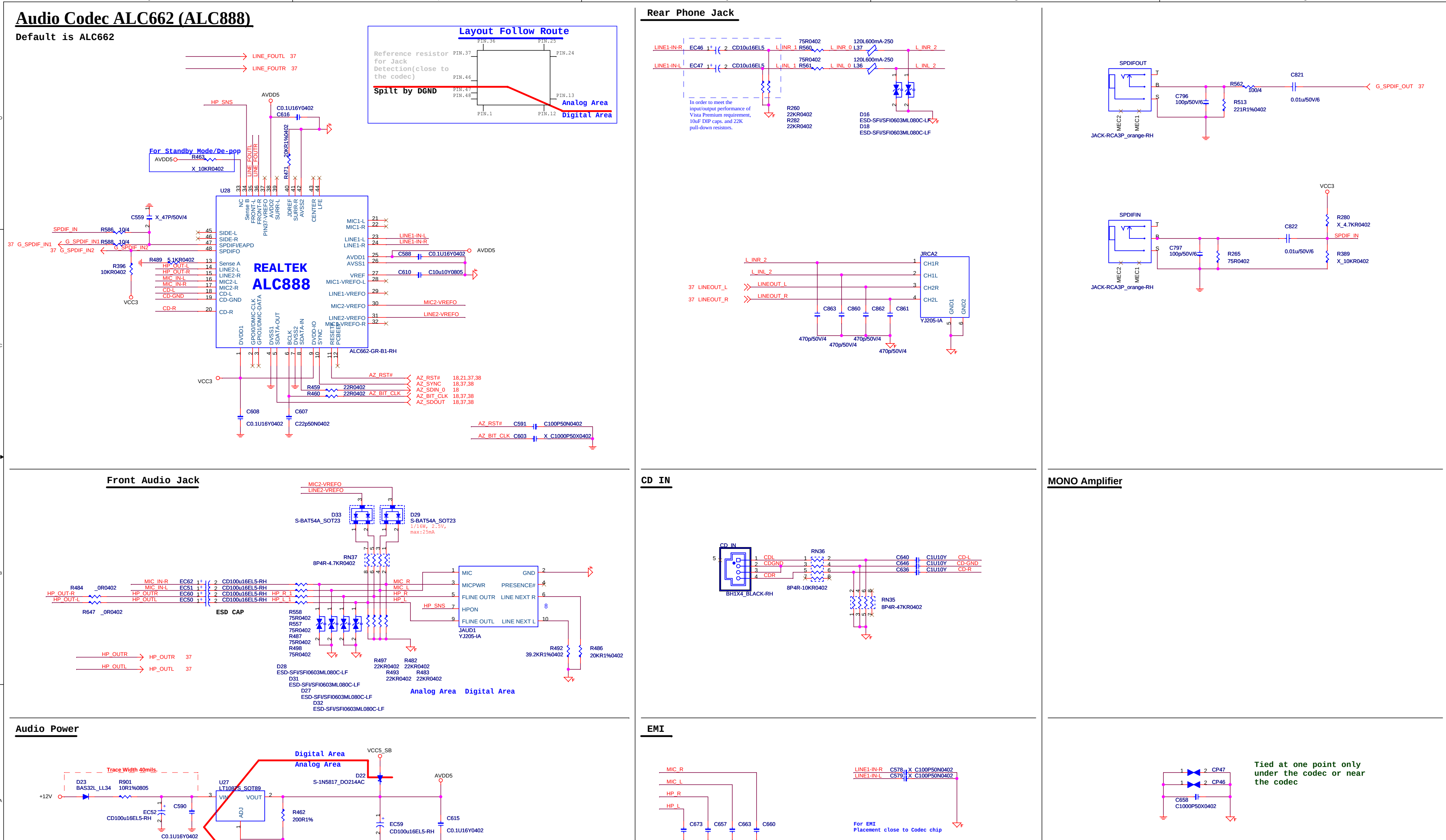

MICRO-START INT'L CO.,LTD.

Title	ALC888	
Size: Custom	Document Number: MS-7411	Rev: 0A
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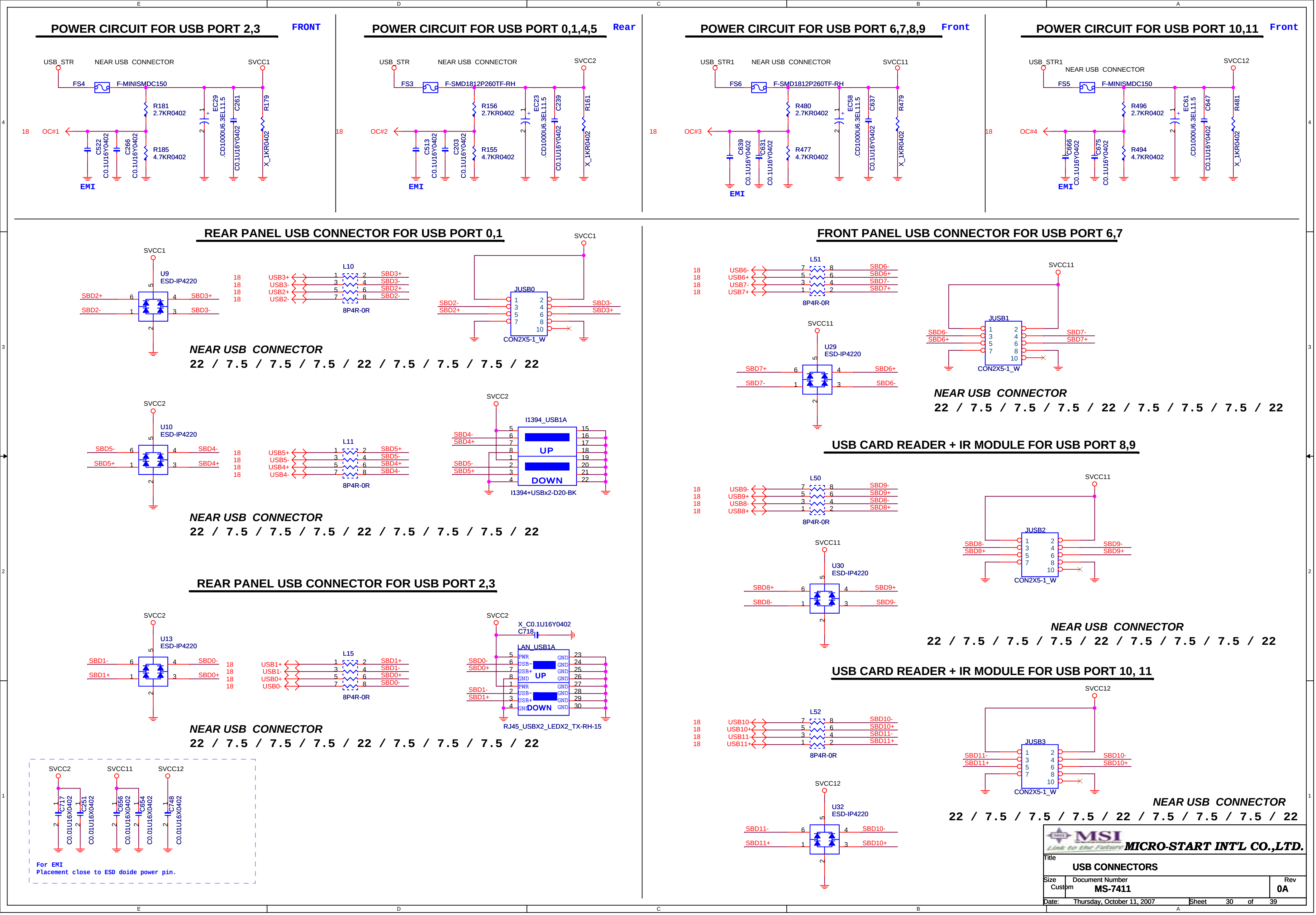

POWER CIRCUIT FOR USB PORT 2,3
FRONT
POWER CIRCUIT FOR USB PORT 0,1,4,5
Rear
POWER CIRCUIT FOR USB PORT 6,7,8,9
Front
POWER CIRCUIT FOR USB PORT 10,11
Front
NEAR USB CONNECTOR
EMI
REAR PANEL USB CONNECTOR FOR USB PORT 0,1
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7
NEAR USB CONNECTOR
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22
USB CARD READER + IR MODULE FOR USB PORT 8,9
REAR PANEL USB CONNECTOR FOR USB PORT 2,3
USB CARD READER + IR MODULE FOR USB PORT 10, 11
For EMI
Placement close to ESD doide power pin.
MICRO-START INT'L CO.,LTD.
Title
USB CONNECTORS
Size
Custom
Document Number
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Rev
0A
Date: Thursday, October 11, 2007
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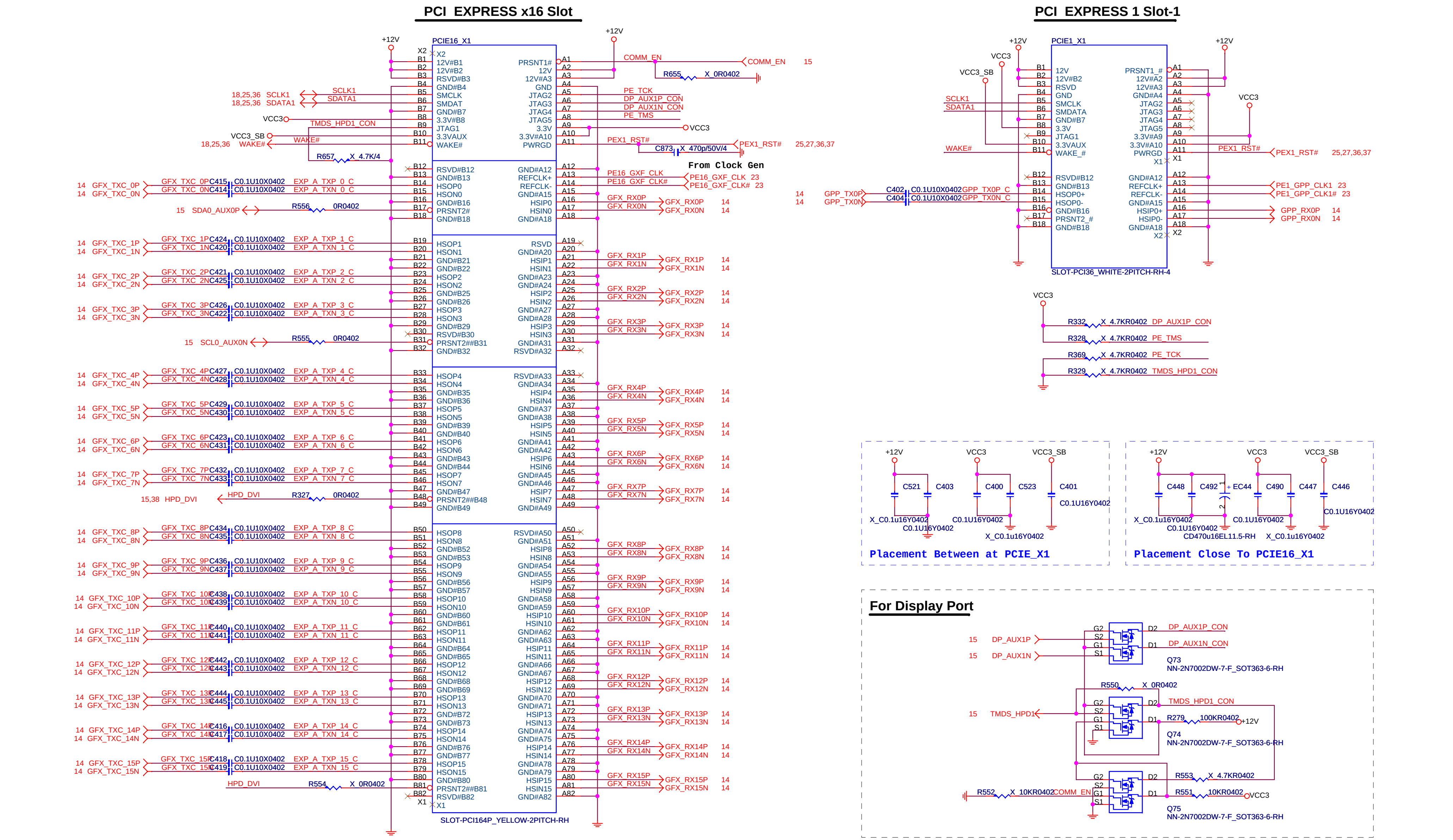
PCI Express Slot x16/x1



MSI MICRO-START INT'L CO.,LTD.

Title: PCI EXPRESS X16 & X1 SLOT		
Size: Custom	Document Number: MS-7411	Rev: 0A
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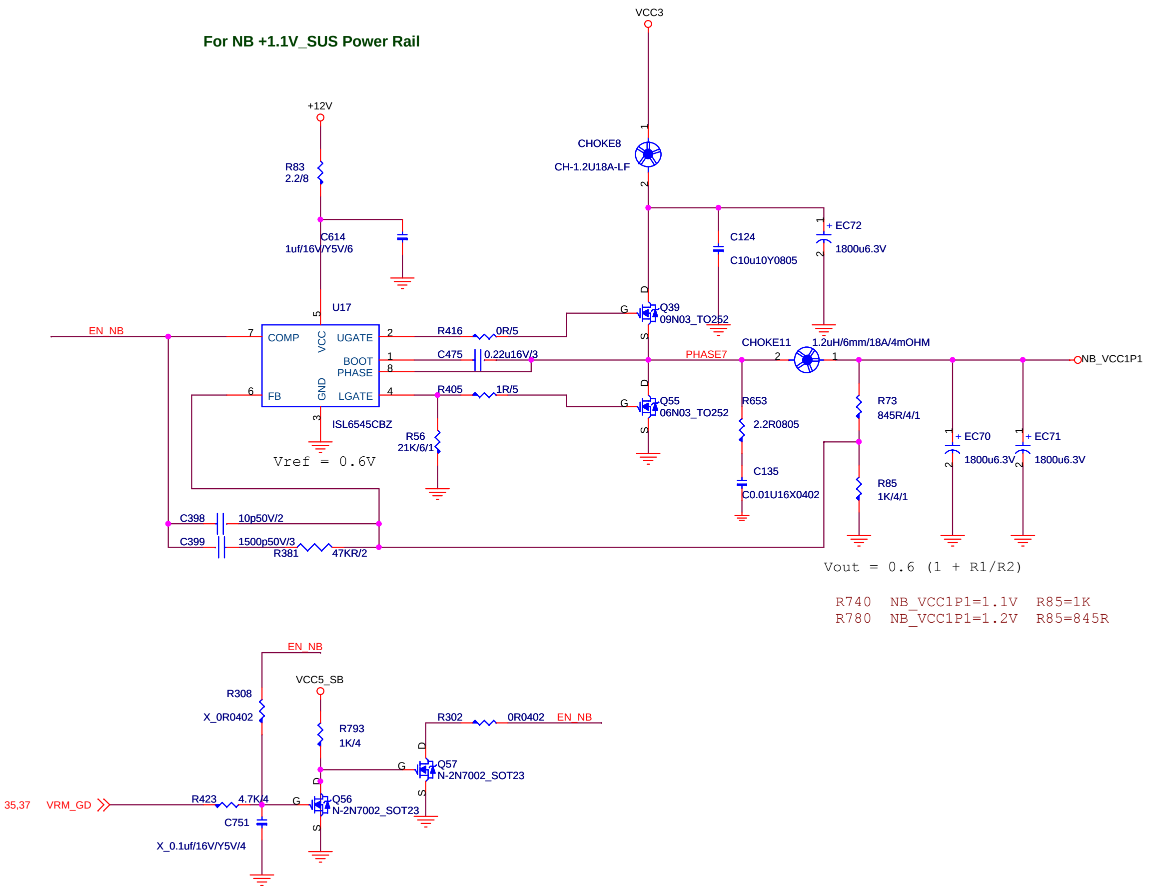
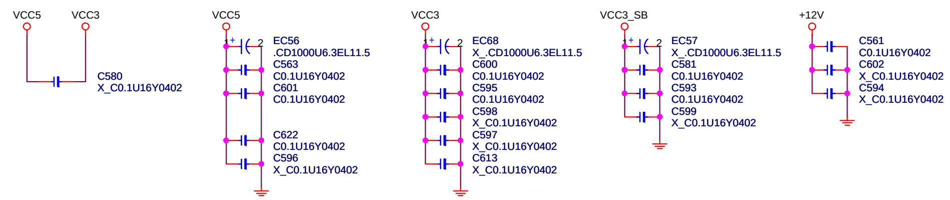
For NB +1.1V_SUS Power Rail



PCI PULL-UP / DOWN RESISTORS



MSI MICRO-START INT'L CO.,LTD.

Title	NB Power core & PCI resistor	
Size: Custom	Document Number: MS-7411	Rev: 0A
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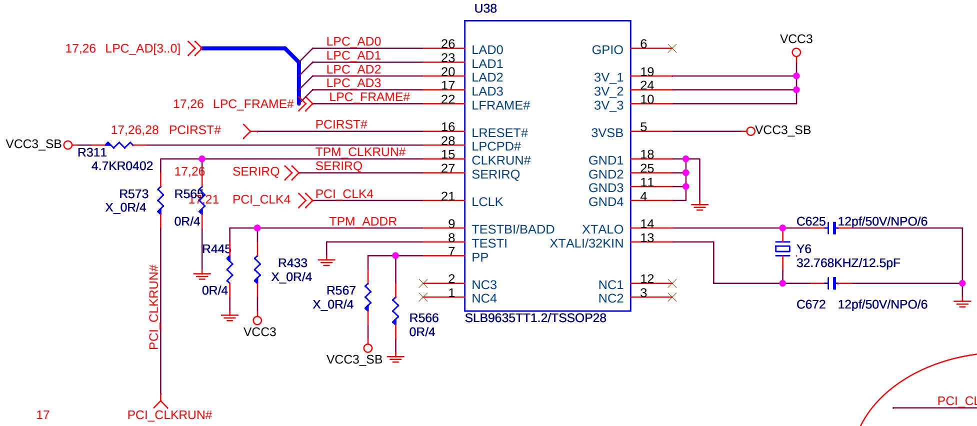
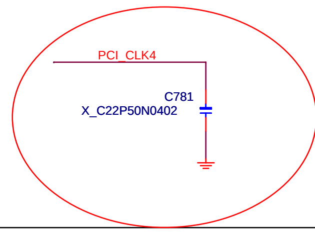
TPM Chipset

IO Address:0x02E



PP : Physical presence
standard connect to GND.



ASSET ID Chipset

ASF2.0 Hard Ware Monitor

CPU Thermo Sense

MICRO-START INT'L CO.,LTD.		
Title: TMP/Asset ID/HWM W83201G		
Size: B	Document Number: MS-7411	Rev: 0A
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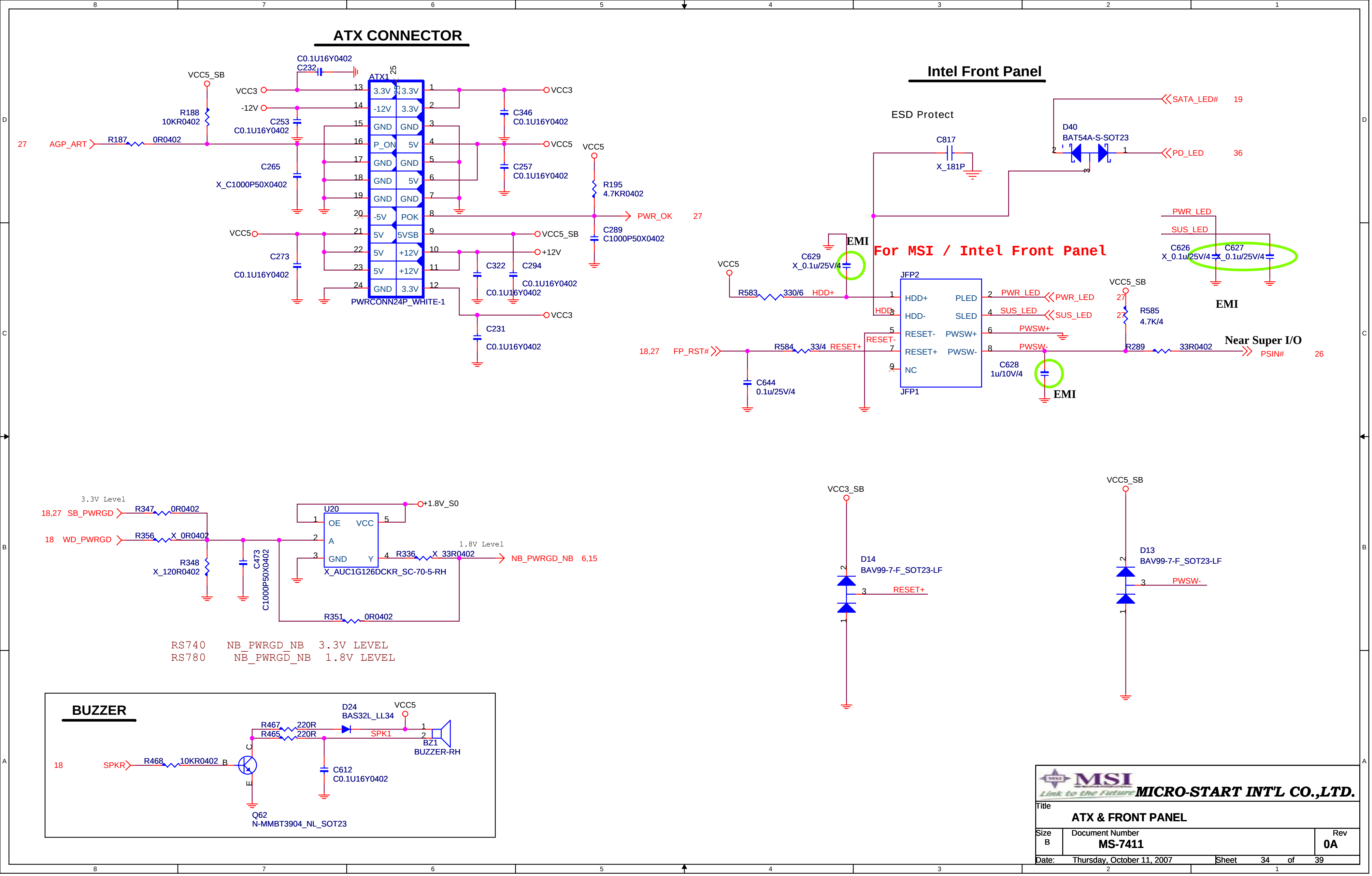
ATX CONNECTOR
ATX1
PWRCONN24P_WHITE-1
3.3V
-12V
GND
P_ON
-5V
5V
5VSB
+12V
POK
VCC5_SB
VCC3
-12V
R188
10KR0402
C232
C0.1U16Y0402
C253
C0.1U16Y0402
27
AGP_ART
R187
0R0402
C265
X_C1000P50X0402
C346
C0.1U16Y0402
C257
C0.1U16Y0402
VCC5
R195
4.7KR0402
PWR_OK
C289
C1000P50X0402
C273
C0.1U16Y0402
+12V
C322
C294
C0.1U16Y0402
C231
Intel Front Panel
ESD Protect
C817
X_181P
D40
BAT54A-S-SOT23
SATA_LED#
19
PD_LED
36
EMI
For MSI / Intel Front Panel
C629
X_0.1u/25V/4
R583
330/6
HDD+
HDD-
JFP2
JFP1
PLED
SLED
RESET-
RESET+
PWSW+
PWSW-
NC
PWR_LED
SUS_LED
C626
X_0.1u/25V/4
C627
X_0.1u/25V/4
VCC5_SB
R585
4.7K/4
Near Super I/O
R289
33R0402
PSIN#
26
18,27
FP_RST#
R584
33/4
C644
0.1u/25V/4
C628
1u/10V/4
3.3V Level
18,27
SB_PWRGD
R347
0R0402
18
WD_PWRGD
R356
X_0R0402
R348
X_120R0402
C473
C1000P50X0402
U20
OE
VCC
A
GND
Y
X_AUC1G126DCKR_SC-70-5-RH
+1.8V_S0
1.8V Level
R336
X_33R0402
NB_PWRGD_NB
6,15
R351
0R0402
RS740 NB_PWRGD_NB 3.3V LEVEL
RS780 NB_PWRGD_NB 1.8V LEVEL
VCC3_SB
D14
BAV99-7-F_SOT23-LF
D13
BAV99-7-F_SOT23-LF
BUZZER
D24
BAS32L_LL34
R467
220R
R465
220R
SPK1
BZ1
BUZZER-RH
SPKR
R468
10KR0402
C612
C0.1U16Y0402
Q62
N-MMBT3904_NL_SOT23
MSI
MICRO-START INT'L CO.,LTD.
Title
ATX & FRONT PANEL
Size
B
Document Number
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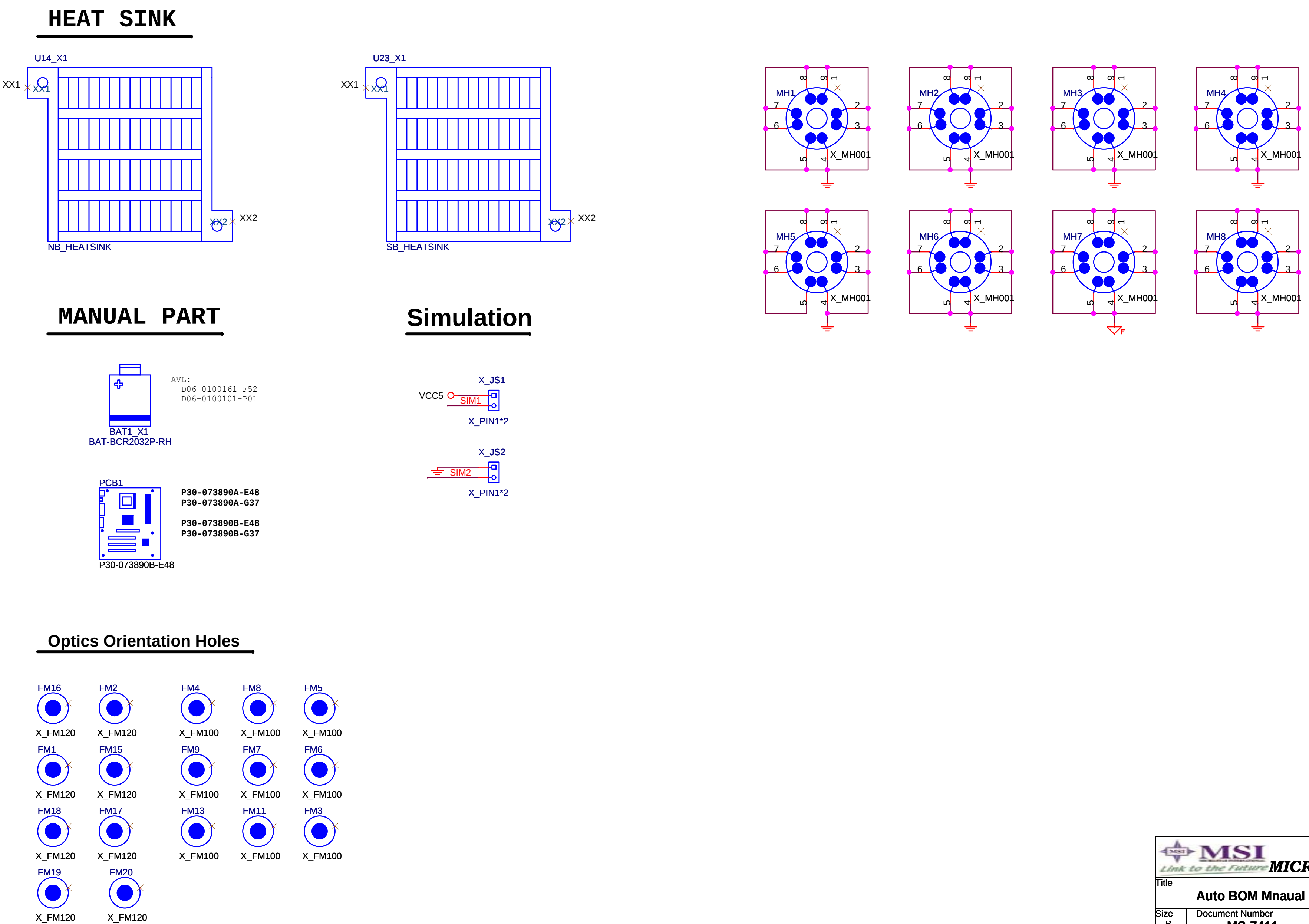

MICRO-START INT'L CO.,LTD.

Title	Auto BOM Mnaual	
Size B	Document Number MS-7411	Rev 0A
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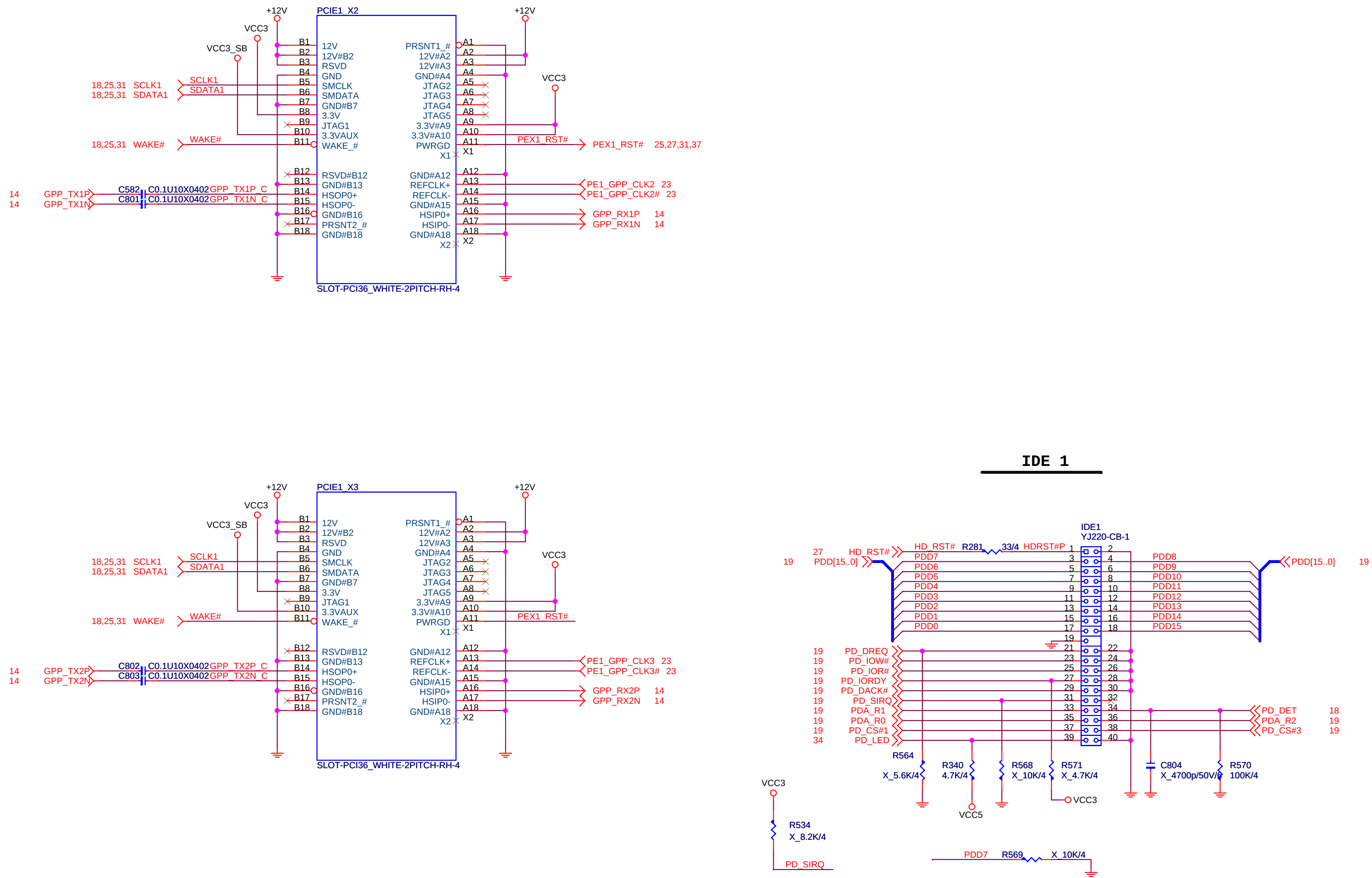

MICRO-STAR INT'L CO.,LTD.

Title: PCI EXPRESS X1 SLOT& IDE

Size	Document Number	Rev
Custom	MS-7411	0A

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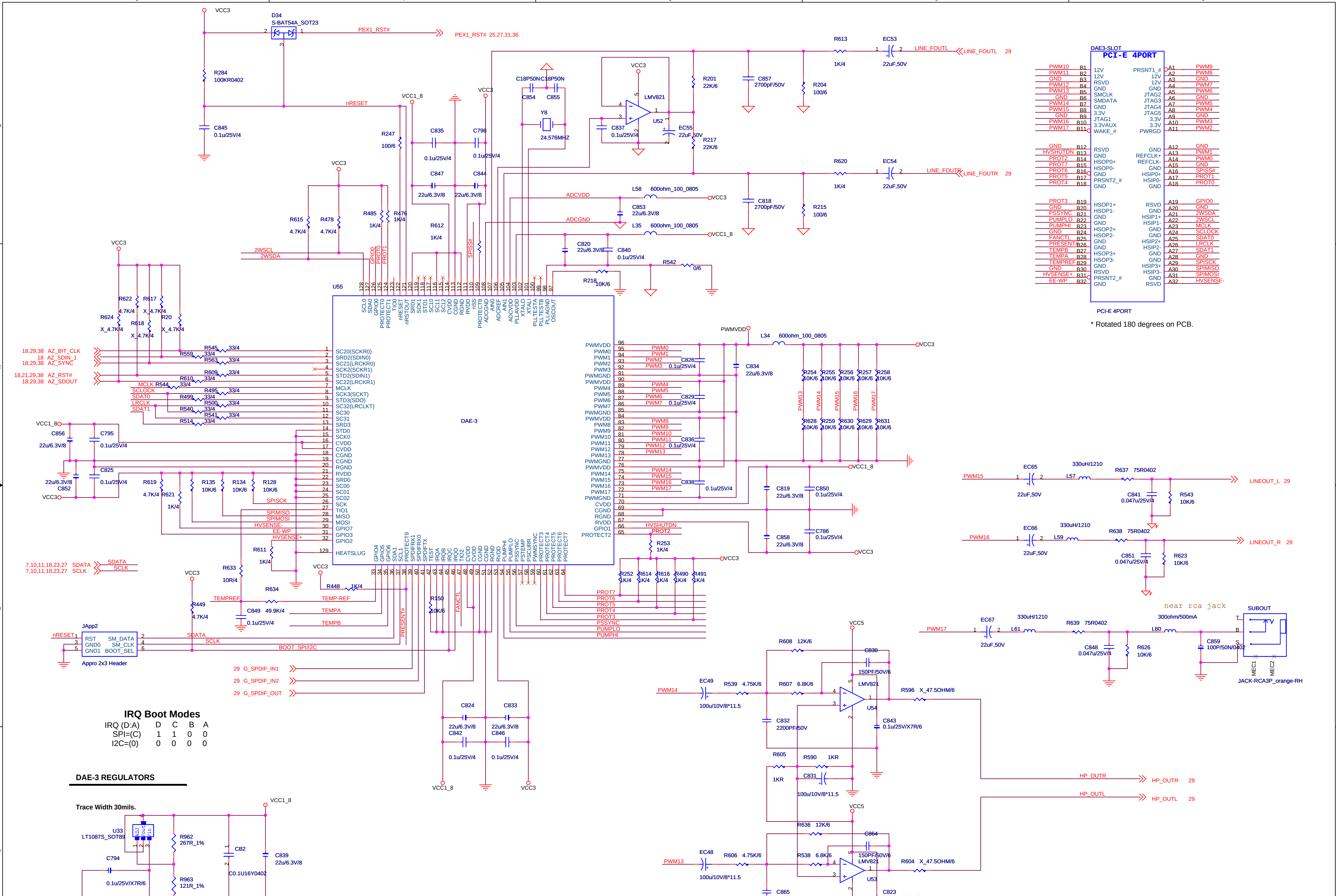

IRQ Boot Modes

IRQ (D:A)	D	C	B	A
SPI=(C)	1	1	0	0
I2C=(0)	0	0	0	0

DAE-3 REGULATORS

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Title	DAE-3	
Size: Custom	Document Number: MS-7411	Rev: 0A
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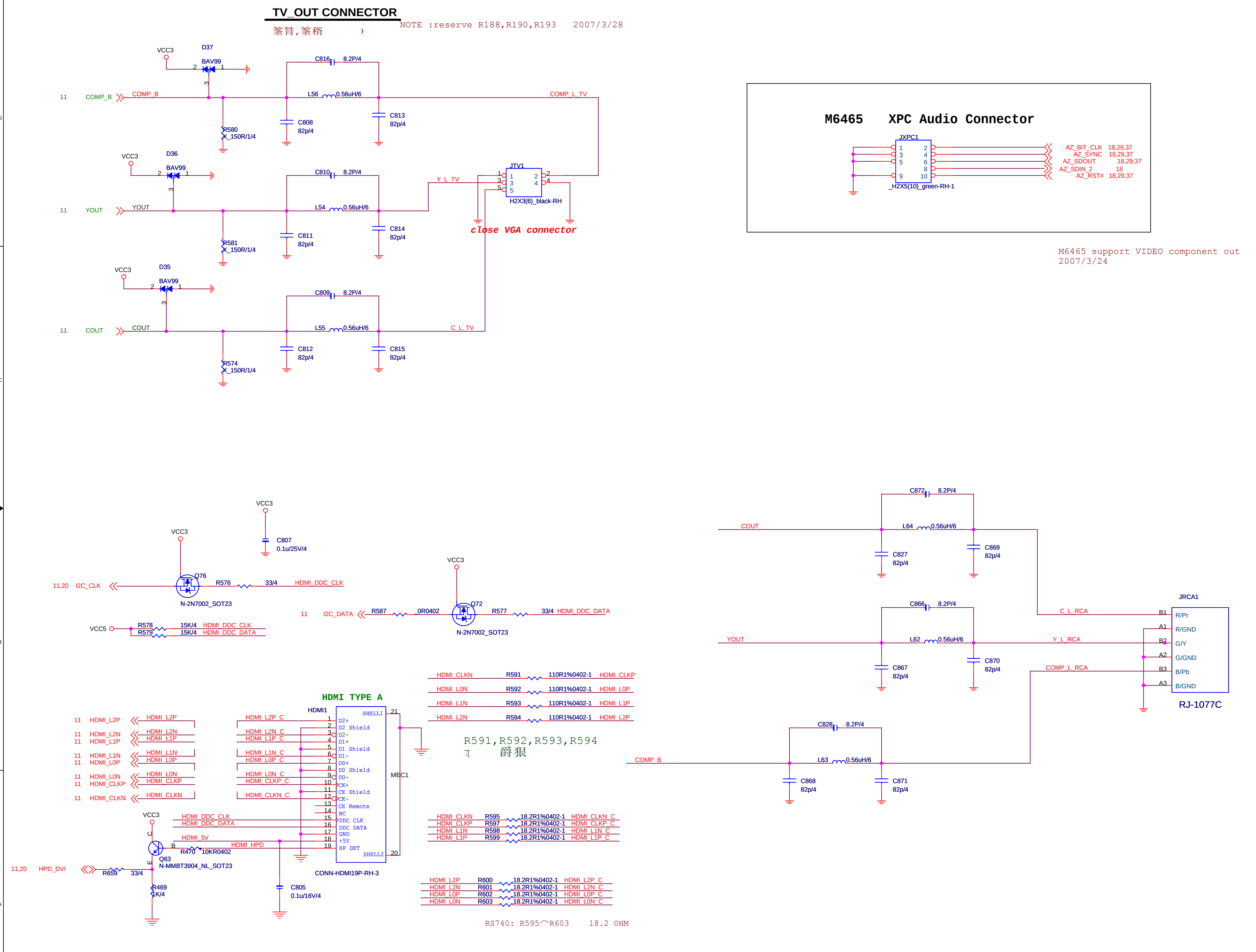

MSI MICRO-START INT'L CO.,LTD.

Title	HDMI/TV-OUT/RCA	
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1. Remove PCI slot   page 32

2. Add two PCIEX1 slot   page 36

3.change to INTEL front panel   page 34

4. remove LPT port   page 24 , add IDE port   page 36

5. remove DVI port   page 22, add HDMI Interface   page 38

6. Add TV-OUT RCA interface, change RS780 interface circuit   page 38 and page 15

7.AUDIO, add DAE-3 circuit ,change ALC888 i/o port, page29
as SKIP request ,change some resistors ,caps   page 37

8.after AMD request ,add serial port ,and LPC debug port   Page 26

9. Remove KB/MS   page 24

10. add 1394 eeprom, and connector and usb connector   page 28

11.change USB pin header and 1394 pin header   , page 28 &30

12. TPM Change to SLB9635TT1.2, page 33

13. DEL wake on lan & wake on modem circuit, page 18

14. DEL JTEMP , page 26

15. DEL BIOS write protect   Circuit , and pull high LPC_SMI#   page 26

16. DEL ASP2.0 hardware monitor,CPU thermo ,asset ID chipset circuit ,   page 33

17.before RV-OUT CON add CLC filter , page 38

18.Add PCI bus pull high resistors, page 17