BAD40_HC
DIS/UMA Schematics Document
Sandy&Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

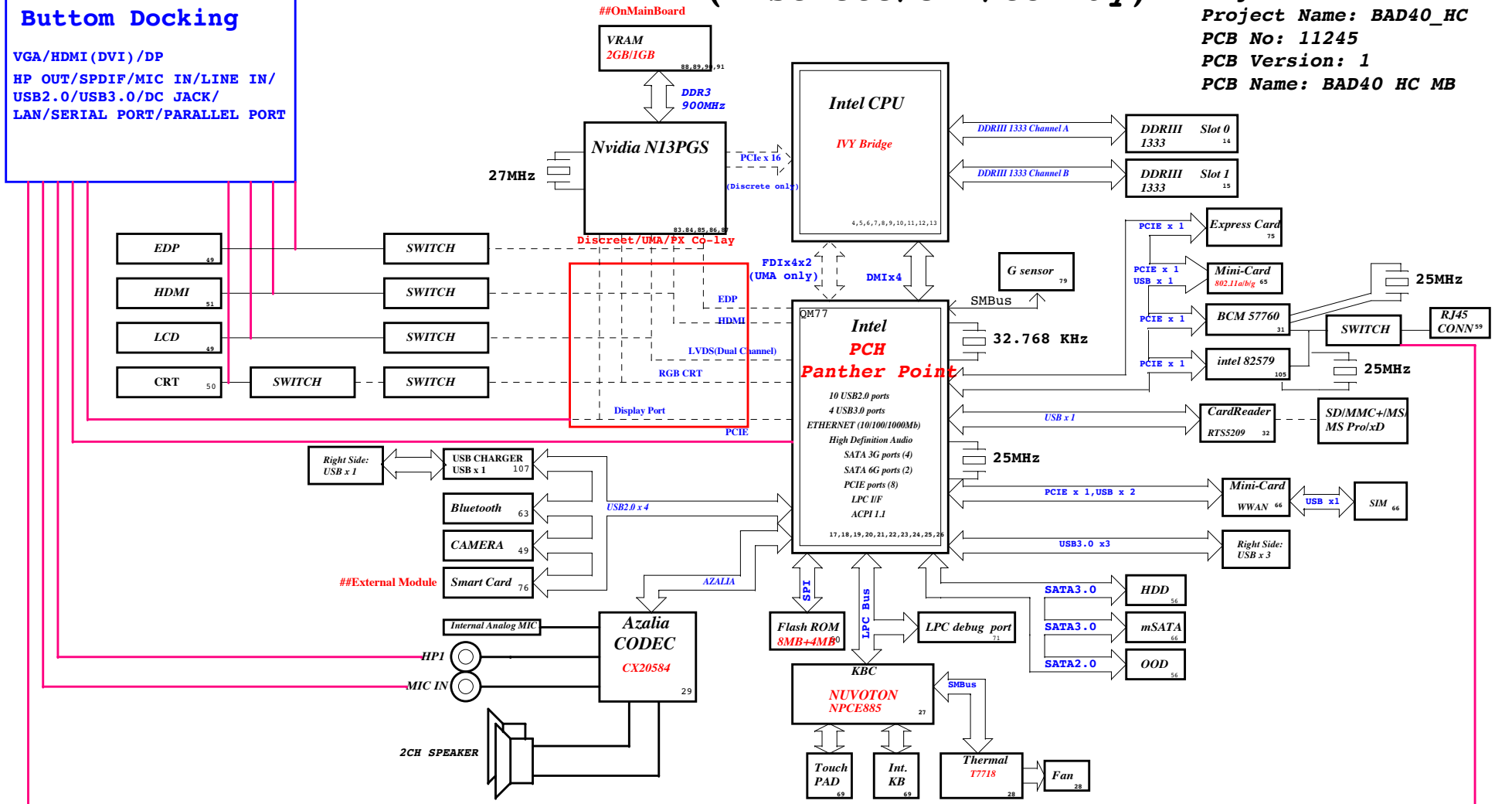
Title: Cover Page		
Size: A3	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 1 of 108	

BAD40 HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4SA01.001
Project Name: BAD40_HC
PCB No: 11245
PCB Version: 1
PCB Name: BAD40 HC MB

Buttom Docking

VGA/HDMI(DVI)/DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



SYSTEM DC/DC TPS5146 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

CPU DC/DC VT1317SFCX 42-43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8237AGQW 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8239CGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT1317SFCX 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208AGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8015AGQW 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC	
INPUTS	OUTPUTS

Switches

INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 2 of 108

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	N/A
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel /BCM LAN
LANE7	New Card
LANE8	N/A

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	USB. port 1
1	USB. port 2
2	USB. port 3
3	Dock
4	X
5	Fingerprint
6	X
7	X
8	Mini Card2 (WWAN) &BT
9	X
10	3G SIM
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: BAD40 HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 3 of 108

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

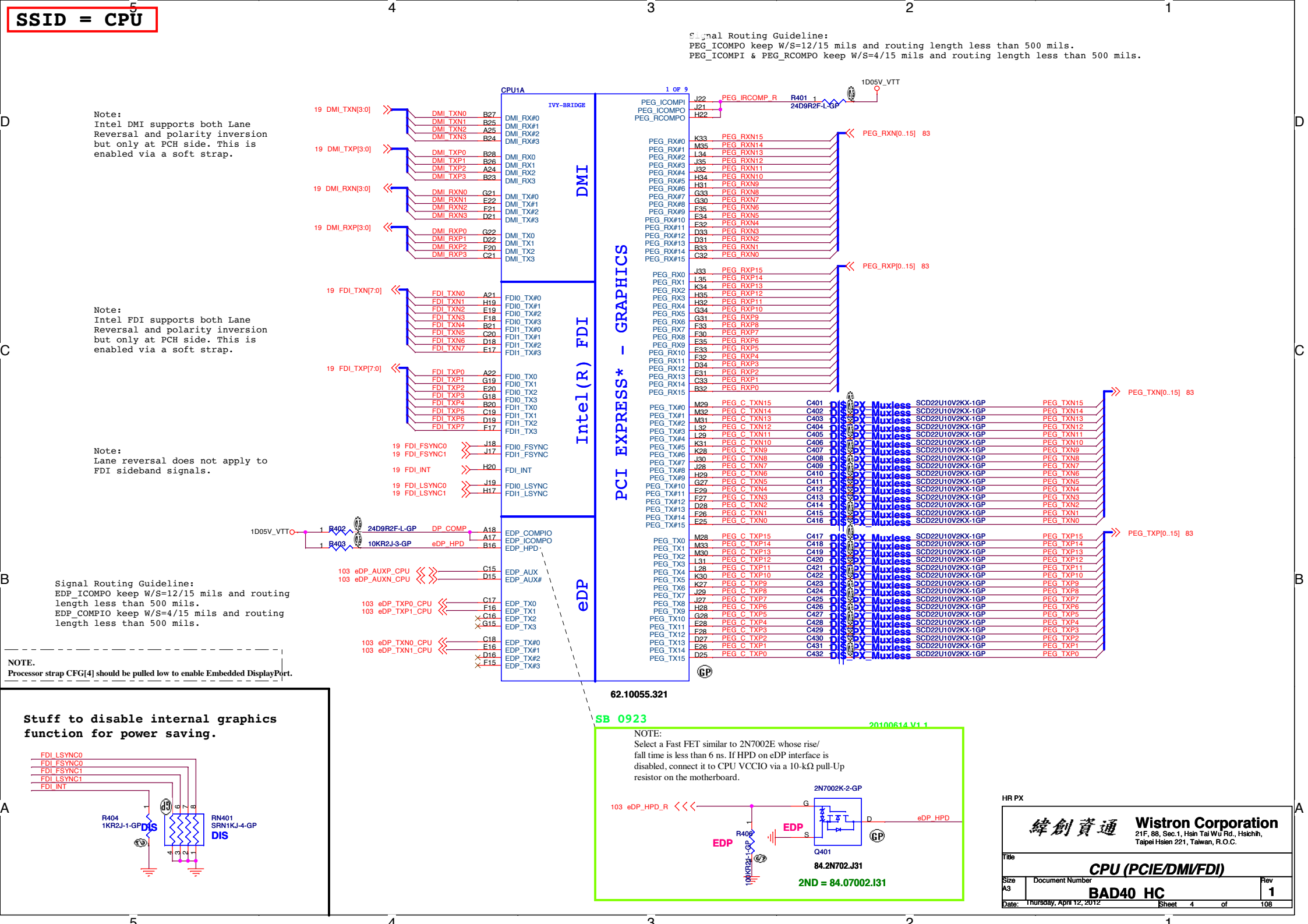
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



Stuff to disable internal graphics function for power saving.

SB 0923

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

HR PX

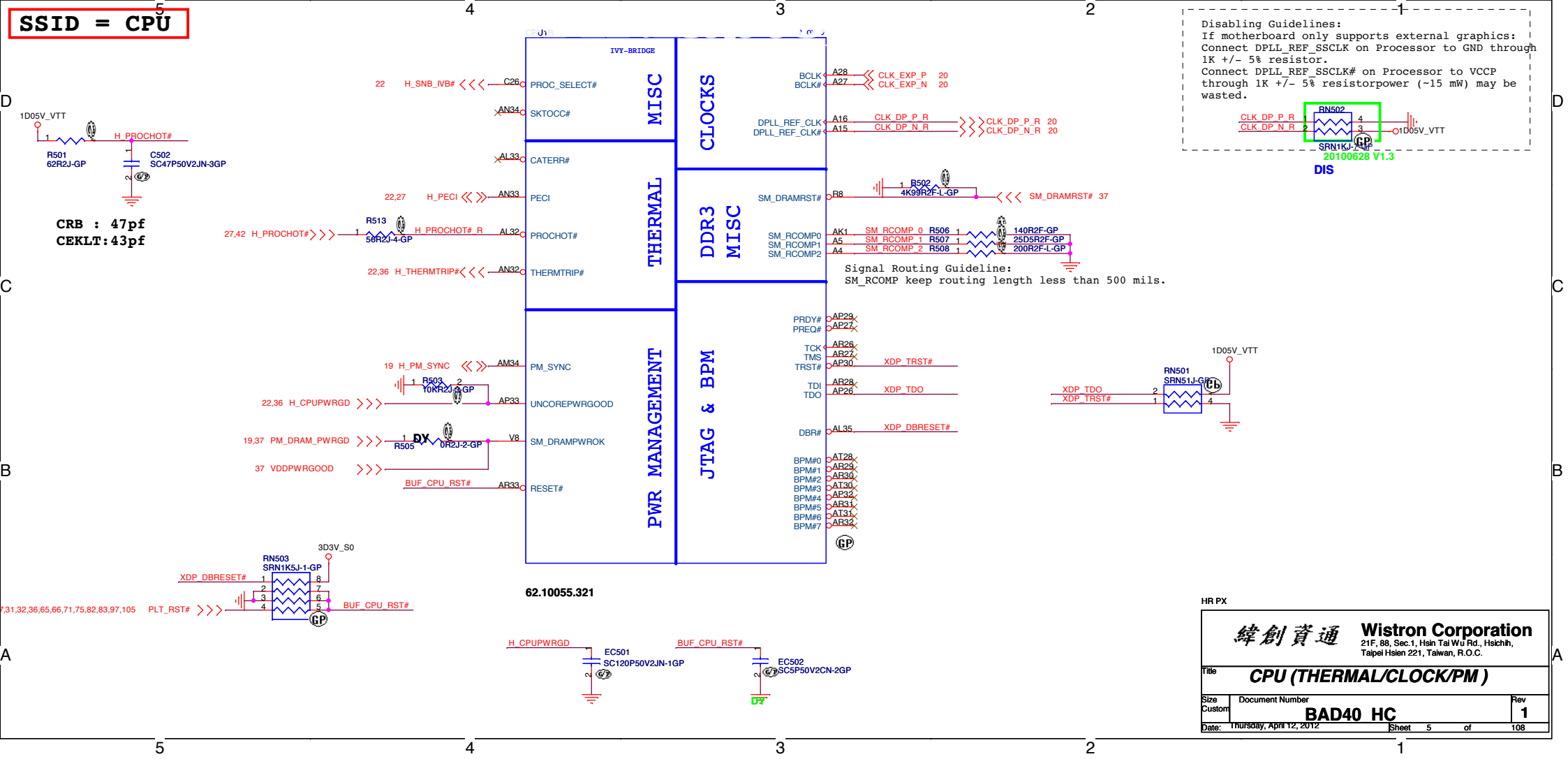
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 4 of 108

SSID = CPU



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

CRB : 47pf
CEKLT:43pf

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

20100628 V1.3

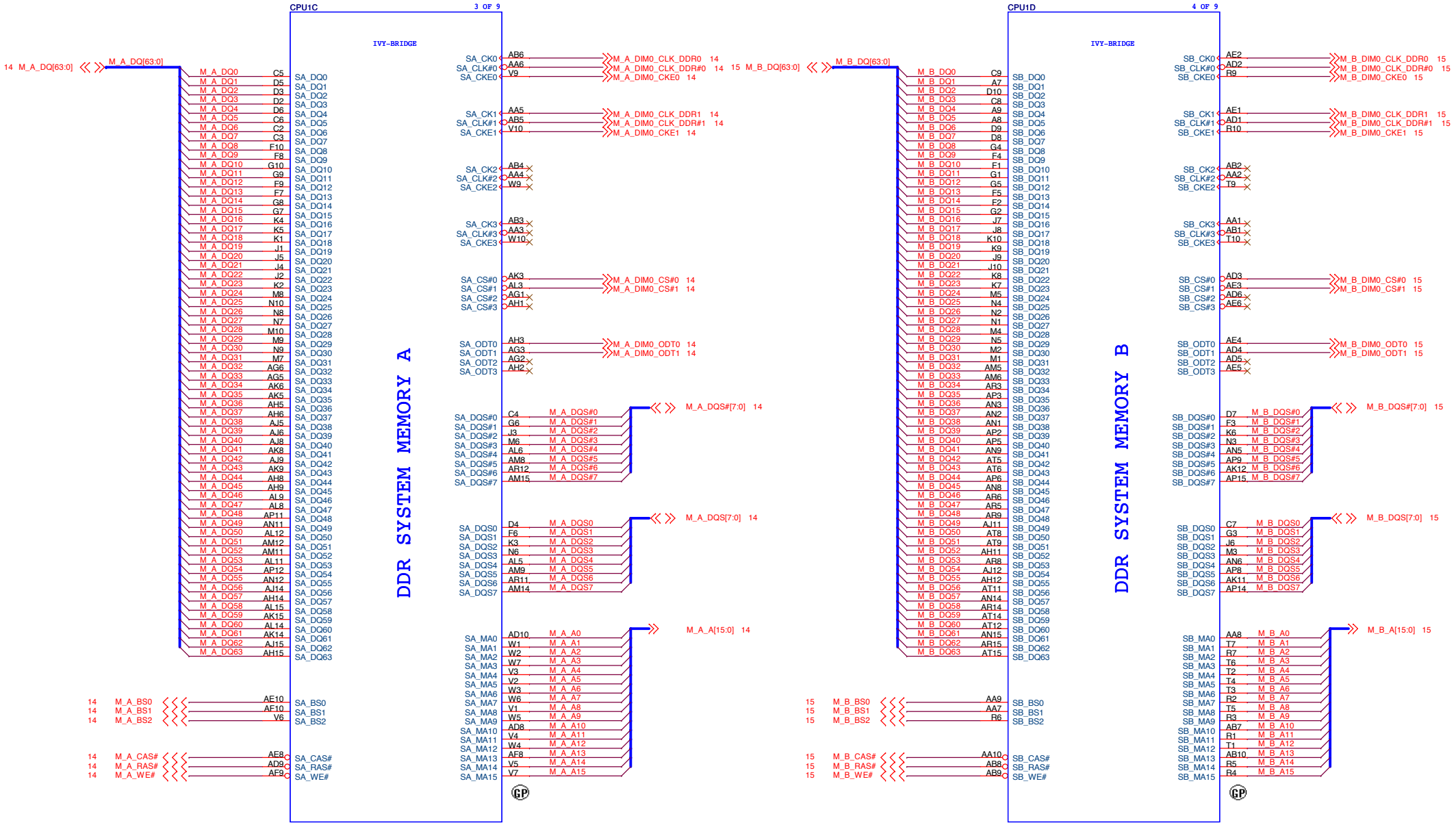
DIS

62.10055.321

HR PX

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (THERMAL/CLOCK/PM)	
Size: Custom	Document Number: BAD40 HC
Rev: 1	
Date: Thursday, April 12, 2012	Sheet 5 of 108

SSID = CPU



62.10055.321

62.10055.321

<Variant Name>

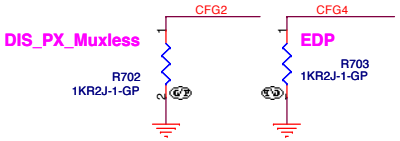
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 6 of 108

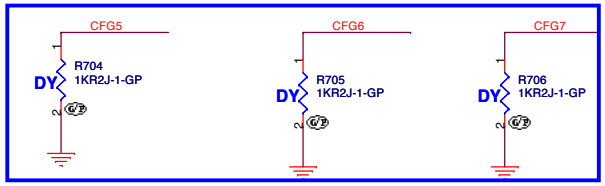
SSID = CPU



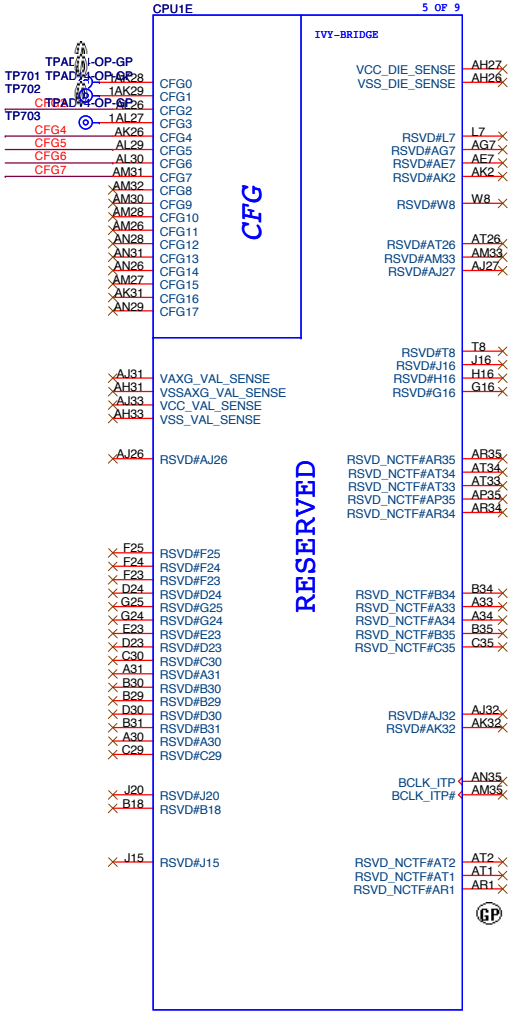
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

SA



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



62.10055.321

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 7 of 108

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

0308 -1
change to 78.2261T.5BL for acousit noice

0308 -1

0308 -1
change to 78.2261T.5BL for acousit noice

0312 -1

0308 -1

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F

6 OF 9

IVY-BRIDGE

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP

VR_SVID_ALERT# R805 75R2F-2-GP

0412 -1M

R801,R802 close to CPU

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

1215 SC

TP801 TPAD14-OP-GP

TP802 TPAD14-OP-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 8 of 108

62.10055.321

SSID = CPU

VAXG Output Decoupling Recommendation
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906, R907 close to CPU

POWER

CPU1G — 7 OF 9 — IVY-BRIDGE

GRAPHICS

SENSE LINES

VAXG_SENSE (AK35) / VSSAXG_SENSE (AK34) → VCC_AXG_SENSE 42 / VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF (AL1) → +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ (B4) / SB_DIMM_VREFDQ (D1) → M_VREF_DQ_DIMM0_C 37 / M_VREF_DQ_DIMM1_C 37

Chief River

SNB 上件，1010 back IVB

M_VREF_DQ_DIMM0_C / M_VREF_DQ_DIMM1_C → RN902 SRN1KJ-7-GP (DY) → 1D5V_S0

DDR3 -1.5V RAILS

VDDQ1–VDDQ15 (AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1)

PROCESSOR VDDQ: 10A

C909 (DY), C910, C911, C912, C913, C914 (DY) — SC10U6D3V5KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

SA RAIL

VCCSA1–VCCSA8 (M27, M26, L26, J26, J25, J24, H26, H25)

PROCESSOR VCCSA: 6A

C916 (DY), C915 — SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

R902 100R2F-L1-GP-U — R902 need be close to pin H23.

VCCSA_SENSE (H23) → VCCSA_SENSE 48

1.8V RAIL

VCCPLL1–VCCPLL3 (B6, A6, A2)

1D8V_S0

PROCESSOR VCCPLL: 1.8A

C922 — SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

VCCSA_VID0 (C22) / VCCSA_VID1 (C24)

VCCIO_SEL (A19) ← H_SNB_IVB#_PWRCTRL

SB 1020 change to DY for co-lay

3D3V_S5 → R911 (DY) 100KR2J-1-GP → H_SNB_IVB#_PWRCTRL

PIn A19	
1.05V	H
1V	L

1D05V_VTT

R908 (DY) 10KR2J-3-GP — VCCSA_VID0 / VCCSA_VID1

R912 (DY) 10KR2J-3-GP

R913 10KR2J-3-GP

R914 10KR2J-3-GP

VCCSA_VID0 48 / VCCSA_VID1 48

VCCSA Voltage Select		
VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

VCC_GFXCORE

R903 0R3J-0-U-GP DIS
R904 0R3J-0-U-GP DIS
R905 0R3J-0-U-GP DIS
R901 0R3J-0-U-GP DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

62.10055.321

VCC_GFXCORE

R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U

VCC_AXG_SENSE
VSS_AXG_SENSE

UMA_PX_Muxless

1201 SC

PROCESSOR VAXG: 38A

C901–C906 SC10U6D3V5KX-1GP (C905, C906 DY)

C907–C921 SC10U6D3V5KX-1GP (C907 DY)

C923–C930 SC22U6D3V5MX-2GP (C926, C928 DY)

C931, C932 SC22U6D3V5MX-2GP (C931 DY)

<Variant Name>

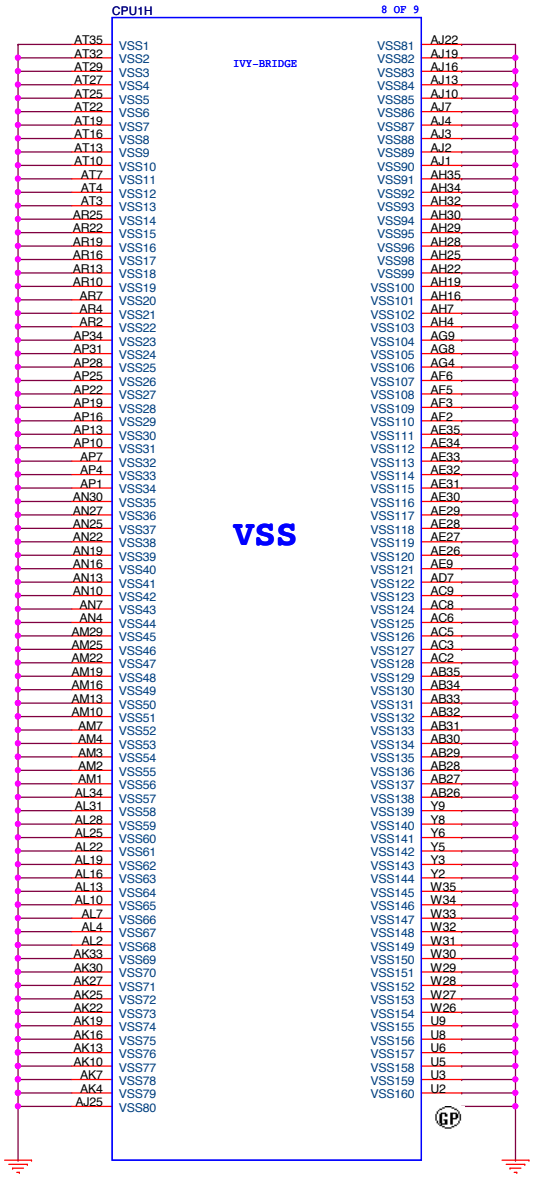
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

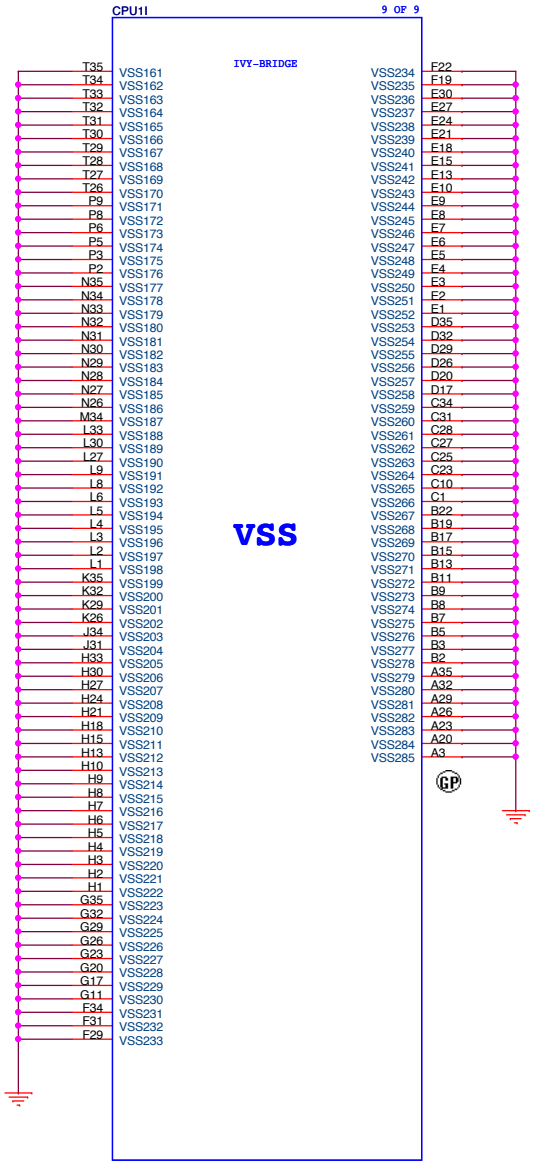
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 9 of 108

SSID = CPU



62.10055.321



62.10055.321

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 10 of 108

reserve

JE40 delete XDP function

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***XDP***	
Size: A4	Document Number: **BAD40_HC**	Rev: 1
Date: Thursday, April 12, 2012	Sheet 11 of 108	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 12 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 13 of 108

SSID = MEMORY

M_A_A[15:0] 6

M_A_BS2 6

M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6

DDR_VREF_S3

M_VREF_DQ_DIMM0

0308 -1
R1404 2
0R0603-FAD
M1

1228 SC
R1405 0R3J-0-U-GP
DY

DDR_WR_VREF01_B4 37

Tracew should be at least 20 mils wide

C1411 SCD1U10V2KX-5GP
C1413 SCD1U10V2KX-5GP

0D75V_S0

Place these caps close to VTT1 and VTT2.

1125 SC for RF

C1419 SC1U6D3V2KX-GP DY
C1420 SC1U6D3V2KX-GP
C1421 SC1U6D3V2KX-GP
C1422 SC2200P50V2KX-2GP
C1418 SCD1U10V2KX-5GP

15,37 DDR3_DRAMRST#

0D75V_S0

H =4mm

DDR3-204P-122-GP

62.10017.Z51
2nd = 62.10017.V51

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
	79	A16/BA2	
	109	BA0	
	108	BA1	
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
	116	ODT0	
	120	ODT1	
	126	VREF_CA	
M_VREF_DQ_DIMM0	1	VREF_DQ	
	30	RESET#	
	203	VTT1	
	204	VTT2	

NP1	NP1	
NP2	NP2	
RAS#	110	M_A_RAS# 6
WE#	113	M_A_WE# 6
CAS#	115	M_A_CAS# 6
CS0#	114	M_A_DIM0_CS#0 6
CS1#	121	M_A_DIM0_CS#1 6
CKE0	73	M_A_DIM0_CKE0 6
CKE1	74	M_A_DIM0_CKE1 6
CK0	101	M_A_DIM0_CLK_DDR0 6
CK0#	103	M_A_DIM0_CLK_DDR#0 6
CK1	102	M_A_DIM0_CLK_DDR1 6
CK1#	104	M_A_DIM0_CLK_DDR#1 6
DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	
SDA	200	PCH_SMBDATA 15,20,66,79
SCL	202	PCH_SMBCLK 15,20,66,79
EVENT#	198	TS#_DIMM0_1 15
VDDSPD	199	3D3V_S0
SA0	197	
SA1	201	
NC#1	77	
NC#2	122	
NC#/TEST	125	
VDD1	75	1D5V_S3
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
VSS	20	
VSS	25	
VSS	26	
VSS	31	
VSS	32	
VSS	37	
VSS	38	
VSS	43	
VSS	44	
VSS	48	
VSS	49	
VSS	54	
VSS	55	
VSS	60	
VSS	61	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	127	
VSS	128	
VSS	133	
VSS	134	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	150	
VSS	151	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	178	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

C1401 SCD1U10V2KX-5GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS#_DIMM0_1 R1403 10KR2J-3-GP 3D3V_S0

SODIMM A DECOUPLING

1D5V_S3

C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 SC10U10V5ZY-1GP DY
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP DY
C1408 SC10U10V5ZY-1GP DY
C1409 SC10U6D3V5KX-1GP DY
C1410 SC10U6D3V5KX-1GP
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

HR PX

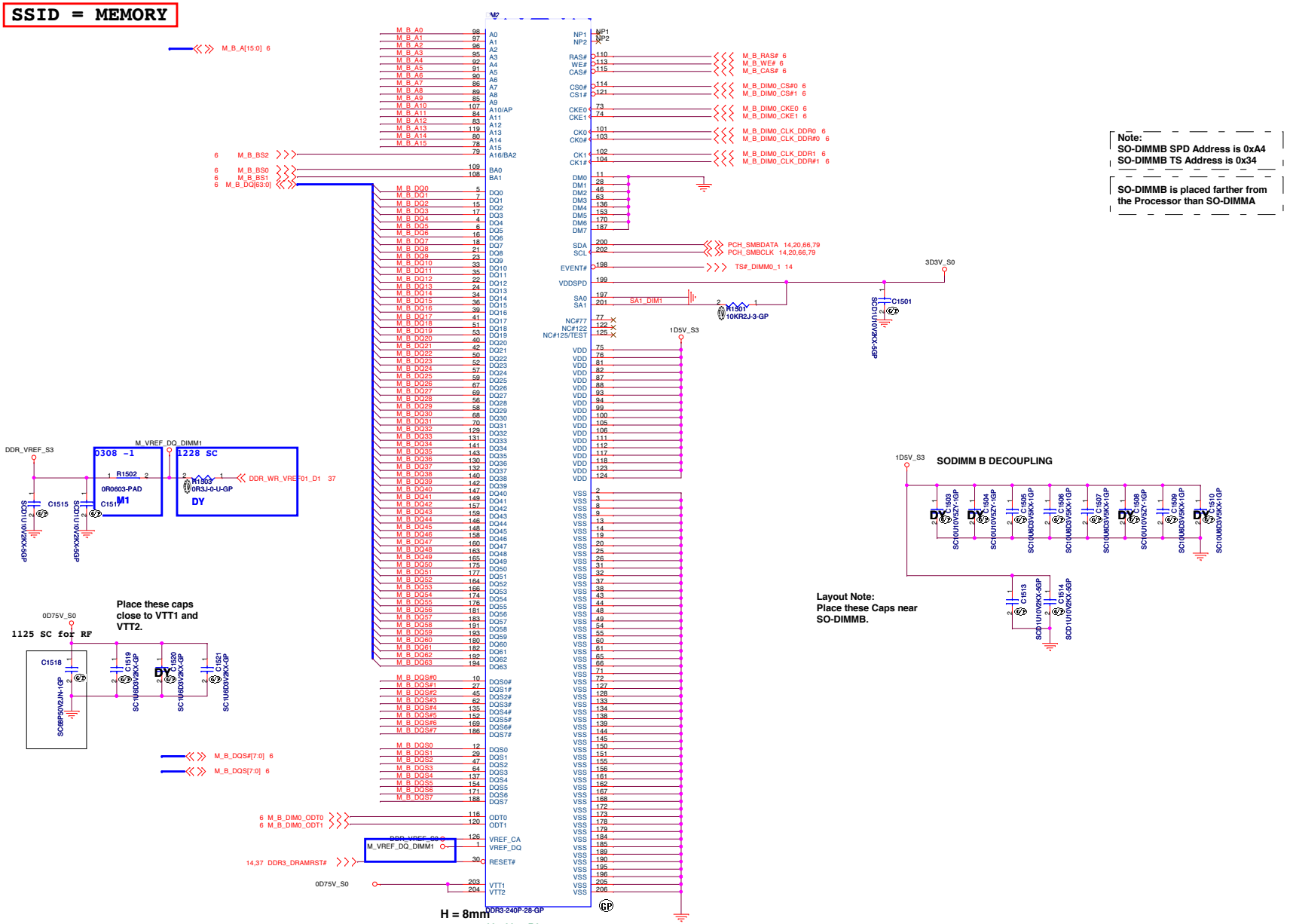
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 14 of 108

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 15 of 108

(Blanking)

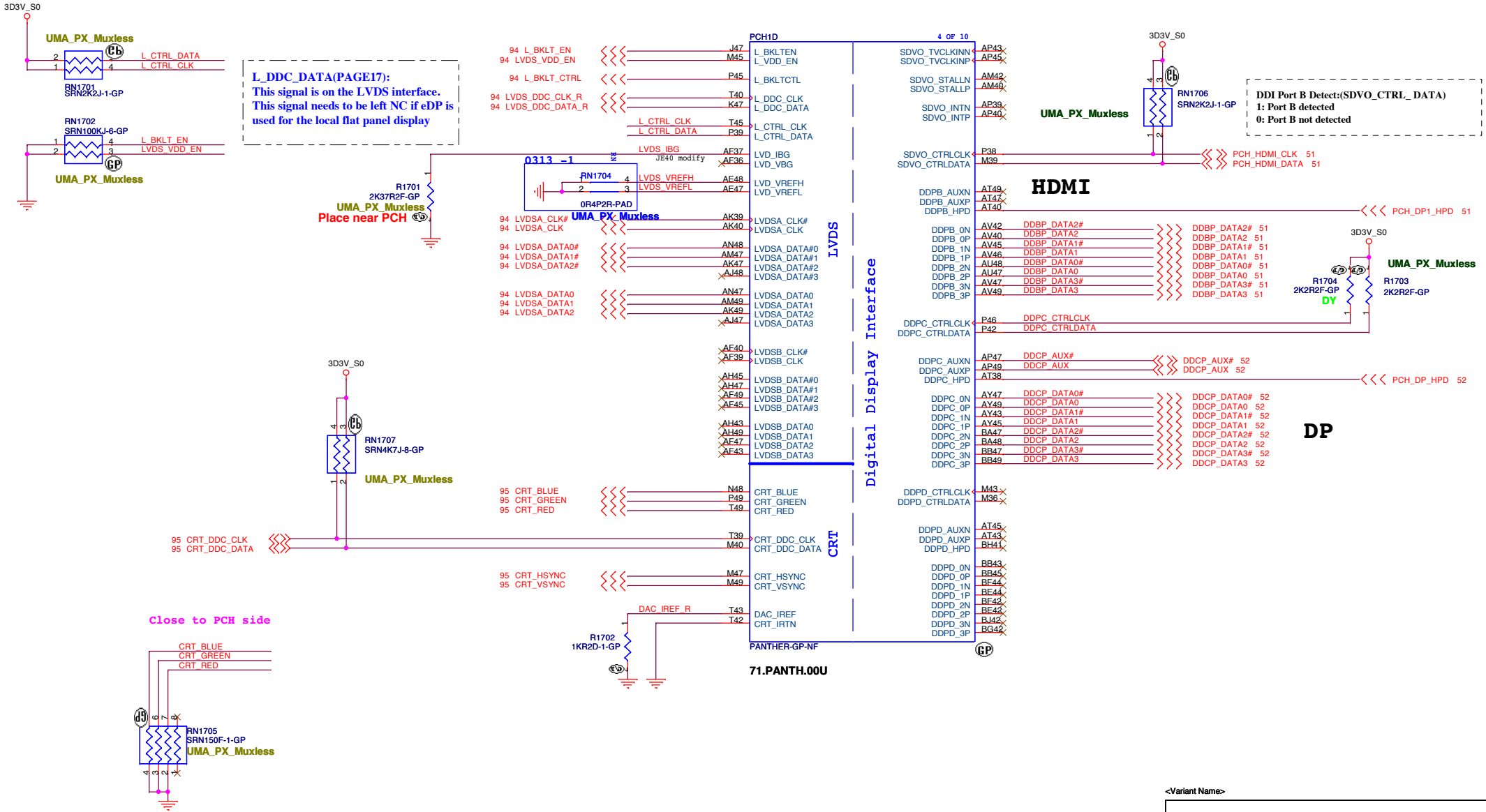
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR3-SODIMM2*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 16 of 108



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

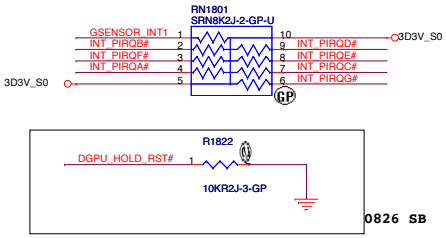
Title: PCH (LVDS/CRT/DDI)

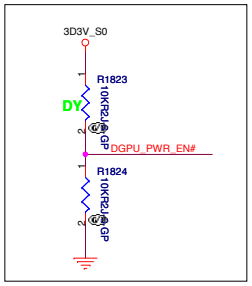
Size	Document Number	Rev
A3	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 17 of 108

SSID = PCH

0826 SB



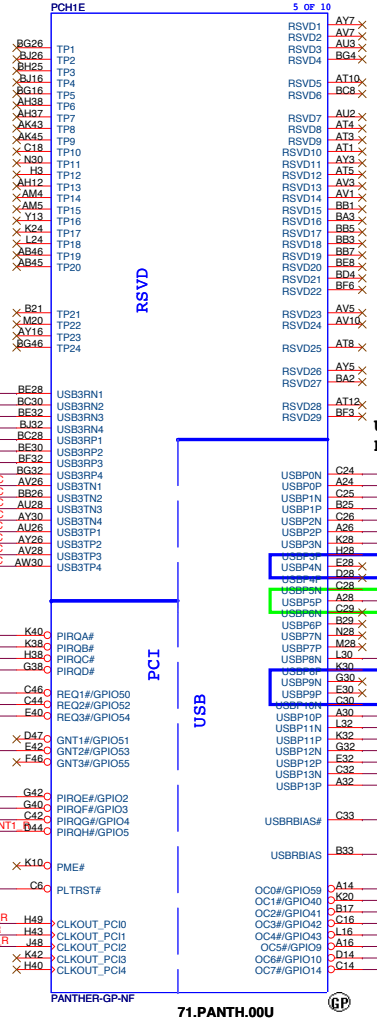


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

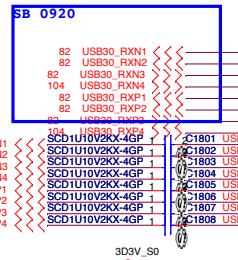
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

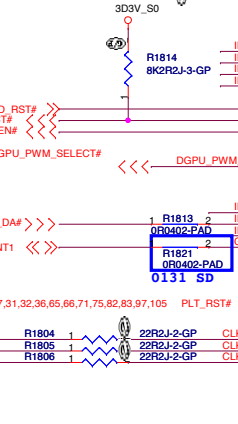
PCH1E

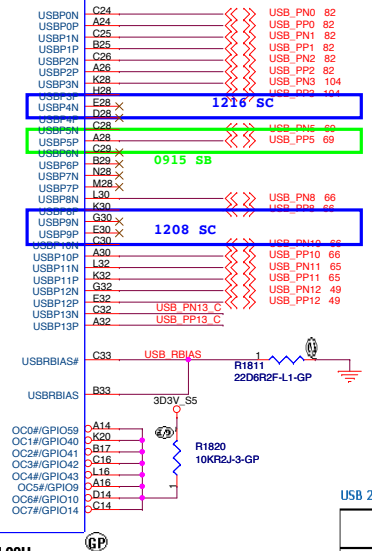
5 OF 10



SB 0920







USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

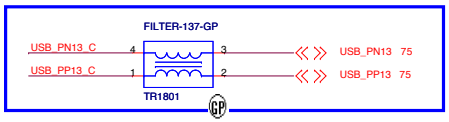
Pair	Device
0	USB port 2 on S/B
1	USB port 3 on S/B
2	USB port 4 on S/B(usb charger)
3	DOCK
4	BLUETOOTH(from port3)
5	Fingerprint(from port2)(NO USE)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB port1(SATA Combo),on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

USB 2.0 Overcurrent Pin Default Usage

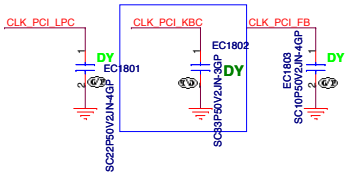
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

0314 -1 for EMI



1125 SC for RF



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 18 of 108

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_TXN0–7, FDI_TXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#, DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

PANTHER-GP-NF

71.PANTH.00U

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.

JE40 modify

0302 -1 for SBA

1222 SC

Non_iAMT_SBA

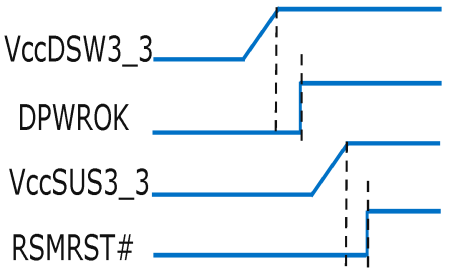
iAMT_SBA

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

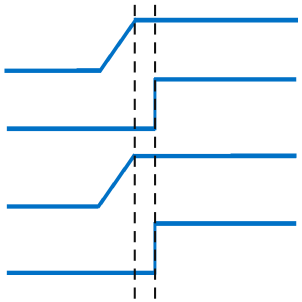
PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

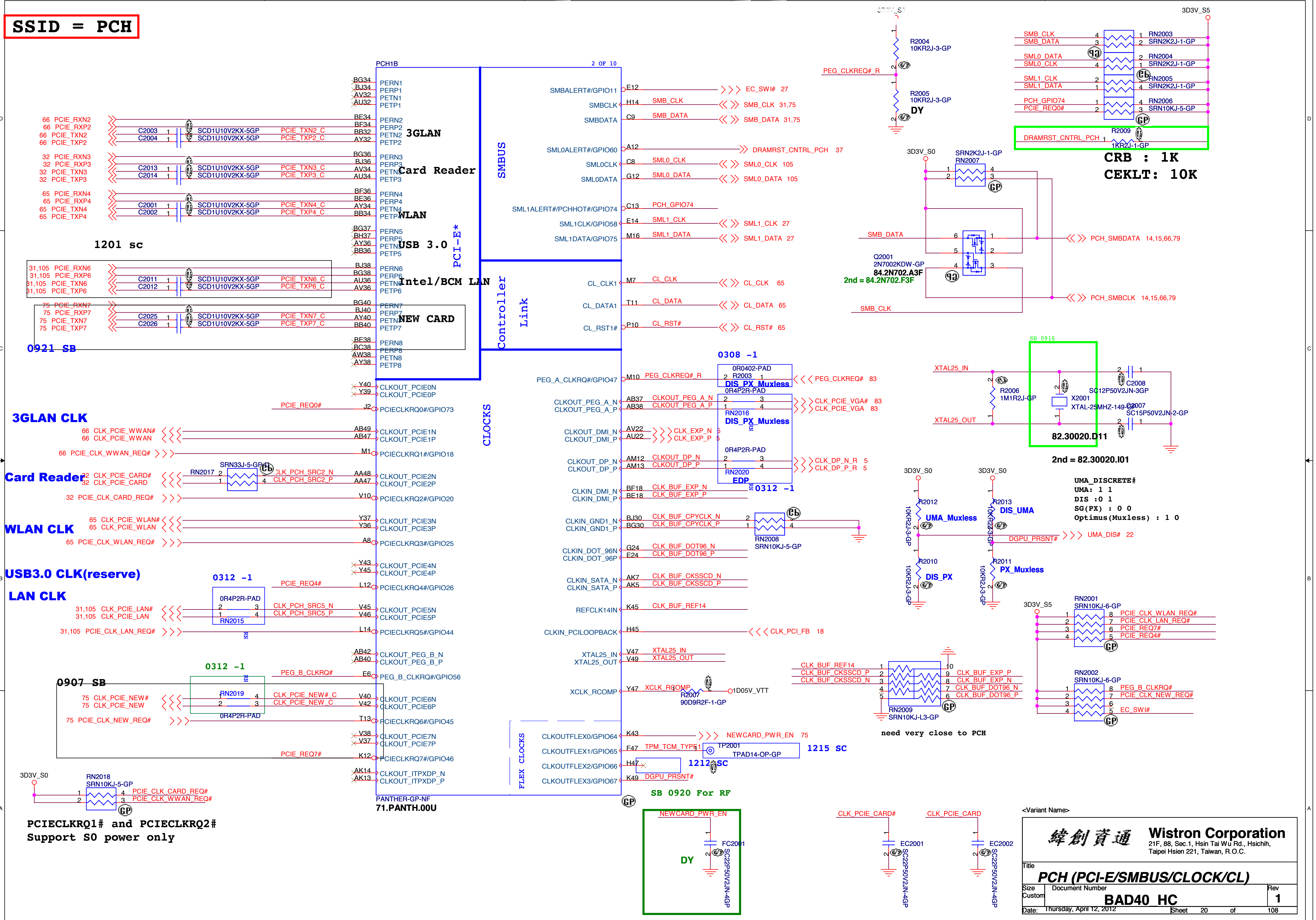
DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DMI/FDI/PM)**

Size: A3 | Document Number: **BAD40_HC** | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 19 of 108



SSID = PCH
PCH1B
2 OF 10
3GLAN
Card Reader
WLAN
USB 3.0
Intel/BCM LAN
NEW CARD
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
1201 sc
0921 SB
0907 SB
0312 -1
0308 -1
1215 SC
1212 SC
SB 0920 For RF
SB 0916
3GLAN CLK
Card Reader
WLAN CLK
USB3.0 CLK(reserve)
LAN CLK
CRB : 1K
CEKLT: 10K
PEG_CLKREQ#_R
DRAMRST_CNTRL_PCH
EC_SWI# 27
SMB_CLK 31,75
SMB_DATA 31,75
DRAMRST_CNTRL_PCH 37
SML0_CLK 105
SML0_DATA 105
SML1_CLK 27
SML1_DATA 27
CL_CLK 65
CL_DATA 65
CL_RST# 65
PCH_SMBDATA 14,15,66,79
PCH_SMBCLK 14,15,66,79
Q2001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F
PEG_CLKREQ# 83
CLK_PCIE_VGA# 83
CLK_PCIE_VGA 83
DIS_PX_Muxless
EDP
X2001
XTAL-25MHZ-149-GP
82.30020.D11
2nd = 82.30020.l01
UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0
UMA_Muxless
DIS_UMA
DIS_PX
PX_Muxless
UMA_DIS# 22
CLK_PCI_FB 18
NEWCARD_PWR_EN 75
need very close to PCH
TPAD14-OP-GP
PANTHER-GP-NF
71.PANTH.00U
PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only
DY

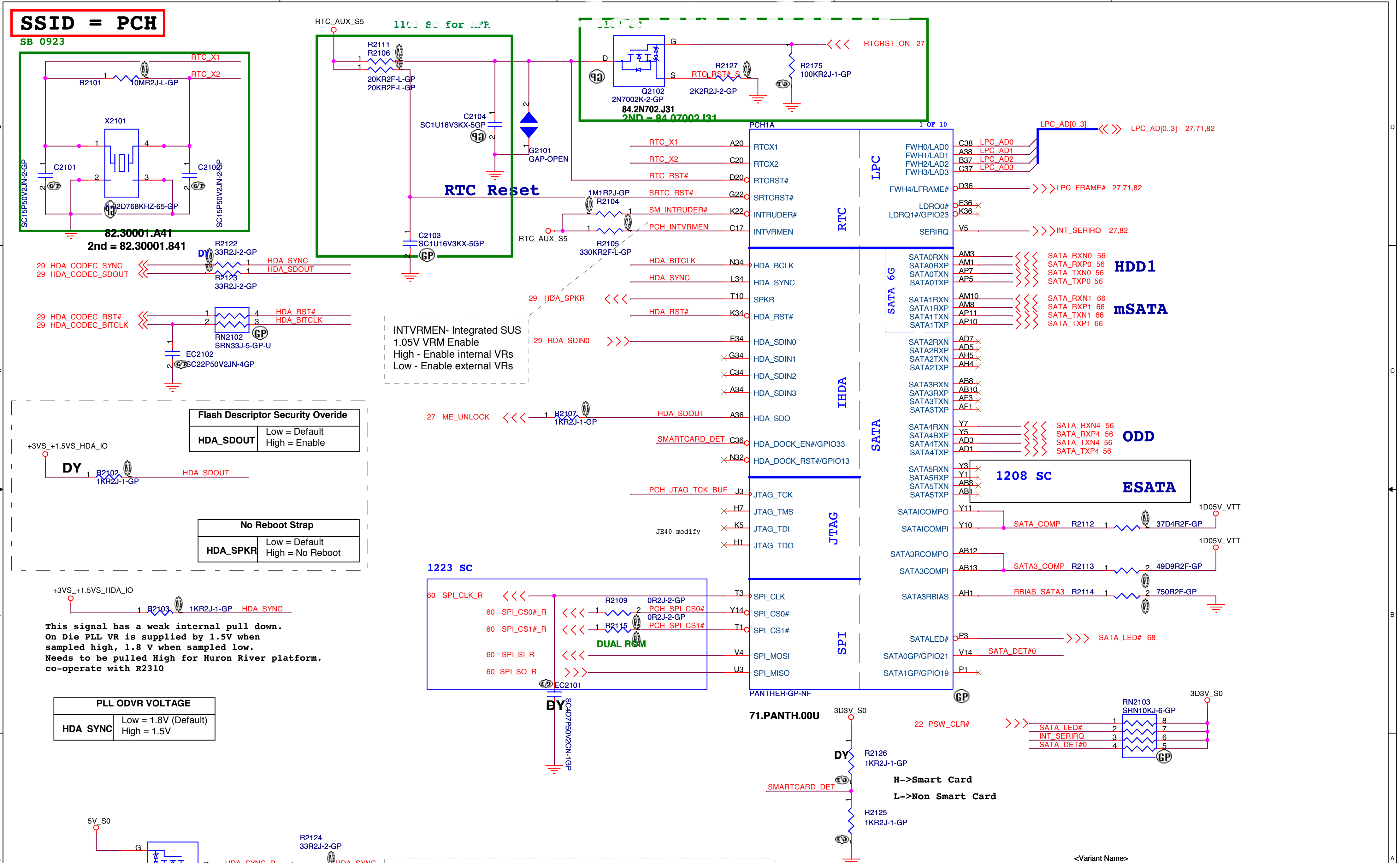
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**PCH (PCI-E/SMBUS/CLOCK/CL)**	
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 20 of 108	

SSID = PCH

SB 0923



INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (SPI/RTC/LPC/SATA/IHDA)	
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 21 of 108	

S3D = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# / H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S5 — **0908 SB**
DY — R2220 10KR2J-3-GP — PCH_GPIO24 — R2207 100KR2J-1-GP

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

	LVDS	eDP
EDP#_LVDS	H	L

PassWord Clear
G2201 GAP-OPEN

1124 SC
del R2206

1208 SC for Del e-SATA

3D3V_S0 — R2224 10KR2J-3-GP — eSATA_DET# — R2209 10KR2J-3-GP DY

3D3V_S0 — RN2201 SRN10KJ-5-GP — DGPU_HPD_INTR# / EC_SCI#
RN2202 SRN10KJ-8-GP — MFG_MODE / S_GPIO / PCH_TEMP_ALERT#
3D3V_S5 — RN2204 SRN10KJ-6-GP — USB3_PWR_ON / LAN_DIS#
PCH_GPIO15 — R2201 1KR2J-1-GP

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — UMA_VRAM800MHZ — PCH_GPIO22 — R2219 10KR2J-3-GP — VRAM900MHZ

VRAM Size

3D3V_S0 — R2214 10KR2J-3-GP — 2G — R2216 10KR2J-3-GP — 1G
VRAM_SIZE1 / VRAM_SIZE2
R2215 10KR2J-3-GP — 1G_512M — R2217 10KR2J-3-GP — 512M_2G

PCH1F — 6 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

GPIO:
S_GPIO T7 — EC_VPS_SMI# A42 (27 EC_VPS_SMI#) — DGPU_HPD_INTR# H36 — EC_SCI# E38 (27) — ICC_EN# C10 — LAN_DIS# C4 (105 LAN_DIS#) — PCH_GPIO15 G2 — SATA_ODD_PRSNT# U2 (56 SATA_ODD_PRSNT#) — DGPU_PWROK D40 (92,93) — PCH_GPIO22 T5 — PCH_GPIO24 E8 — PCH_GPIO27 E16 (TP2203) — PLL_ODVR_EN P8 — PSW_CLR# K1 (21) — eSATA_DET# K4 — DMI_OVRVLTG V8 — FDI_OVRVLTG M5 — MFG_MODE N2 — EDP#_LVDS M3 (49) — TPM_TCM_TYPE2 V13 — PCH_TEMP_ALERT# V3 — USB3_PWR_ON D6 — PCH_NCTF_1 A4 — PCH_NCTF_3 A46 — PCH_NCTF_2 BF1 — PCH_NCTF_4 BF49
BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49/TEMP_ALERT#, GPIO57

CPU/MISC:
TACH4/GPIO68 C40 — SATA_ODD_PWRGT 56
TACH5/GPIO69 B41 — UMA_DIS# 20
TACH6/GPIO70 C41 — VRAM_SIZE1
TACH7/GPIO71 A40 — VRAM_SIZE2
A20GATE P4 — H_A20GATE 27
PECI AU16 — H_PECI_R — DY R2203 0R2J-2-GP — H_PECI 5,27
RCIN# P5 — H_RCIN# 27
PROCPWRGD AY11 — H_CPUPWRGD 5,36
THRMTRIP# AY10 — PCH_THERMTRIP_R
INIT3_3V# T14
DF_TVS AY1 — NV_CLE
TS_VSS1 AH8, TS_VSS2 AK11, TS_VSS3 AH10, TS_VSS4 AK10
NC_1 P37

NCTF:
VSS_NCTF_15#BG2, VSS_NCTF_16#BG48, VSS_NCTF_17#BH3, VSS_NCTF_18#BH47, VSS_NCTF_19#BJ4, VSS_NCTF_20#BJ44, VSS_NCTF_21#BJ45, VSS_NCTF_22#BJ46, VSS_NCTF_23#BJ5, VSS_NCTF_24#BJ6, VSS_NCTF_25#C2, VSS_NCTF_26#C48, VSS_NCTF_27#D1, VSS_NCTF_28#D49, VSS_NCTF_29#E1, VSS_NCTF_30#E49, VSS_NCTF_31#F1, VSS_NCTF_32#F49
VSS_NCTF_1#A4, VSS_NCTF_2#A44, VSS_NCTF_3#A45, VSS_NCTF_4#A46, VSS_NCTF_5#A5, VSS_NCTF_6#A6, VSS_NCTF_7#B3, VSS_NCTF_8#B47, VSS_NCTF_9#BD1, VSS_NCTF_10#BD49, VSS_NCTF_11#BE1, VSS_NCTF_12#BE49, VSS_NCTF_13#BF1, VSS_NCTF_14#BF49
NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47, BD1,BD49,BE1,BE49,BF1,BF49, BG2,BG48,BH3,BH47,BJ4,BJ44, BJ45,BJ46,BJ5,BJ6,C2,C48,D1, D49,E1,E49,F1,F49

1D8V_S0 — R2221 2K2R2J-2-GP — NV_CLE — R2222 1KR2J-1-GP — H_SNB_IVB# 5

-1. 4/11
RN2205 SRN56J-4-GP — DY — 1D05V_VTT
PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

0908 SB
3D3V_S5 — R2223 10KR2J-3-GP — ICC_EN# — R2211 1KR2J-1-GP DY

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

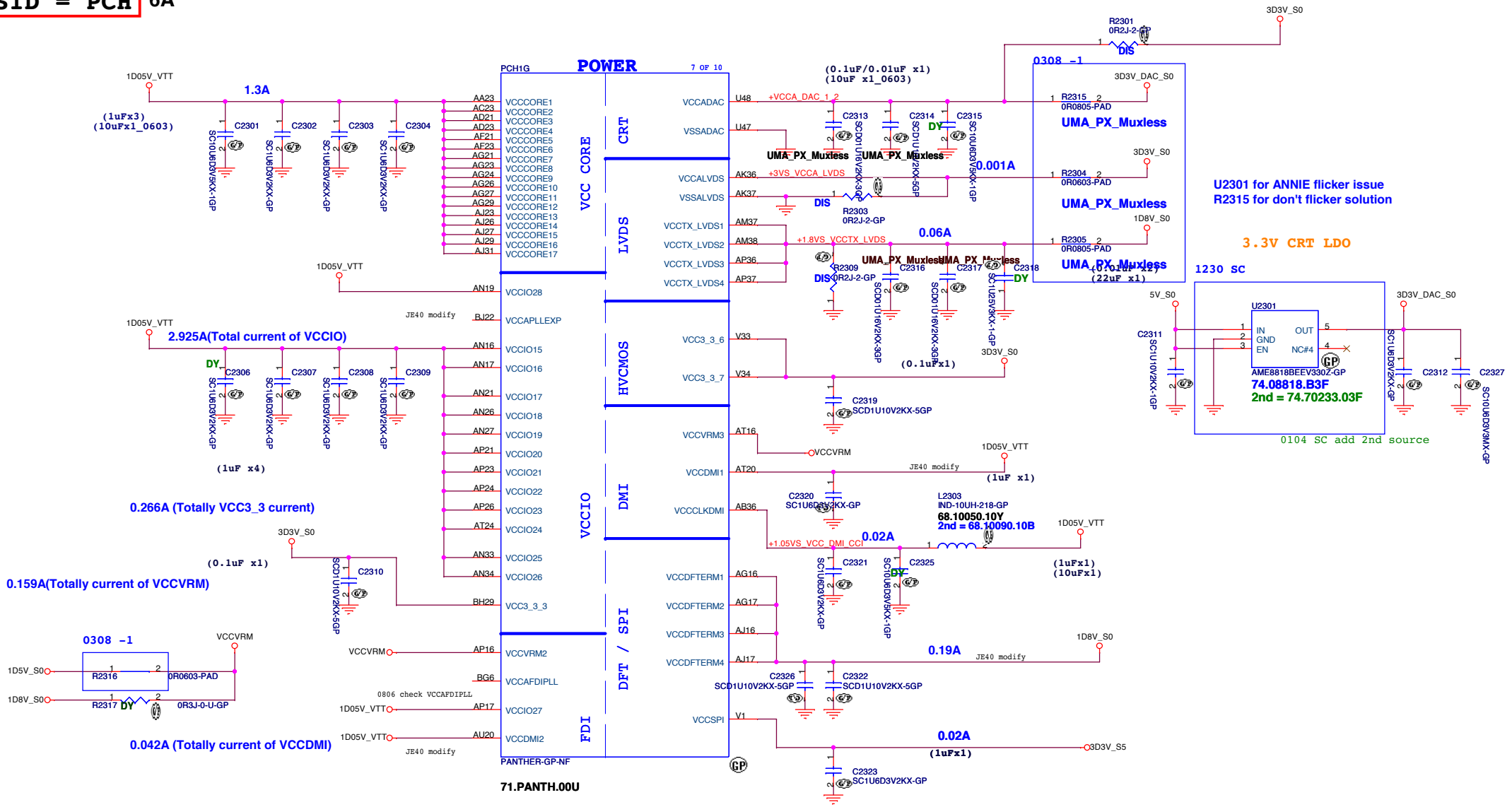
PLL_ODVR_EN — DY 1 R2212 1KR2J-1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 22 of 108

SSID = PCH 6A



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 23 of 108

SSID = PCH

POWER

PCH1J

PANTHER-GP-NF

71.PANTH.00U

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

CPU

MISC

RTC

HDA

10 OF 10

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.08A

0.01A

6uA

JE40 modify 07/16

83.R0304.D8F

74.09090.A3F

<Variant Name>

0308 -1

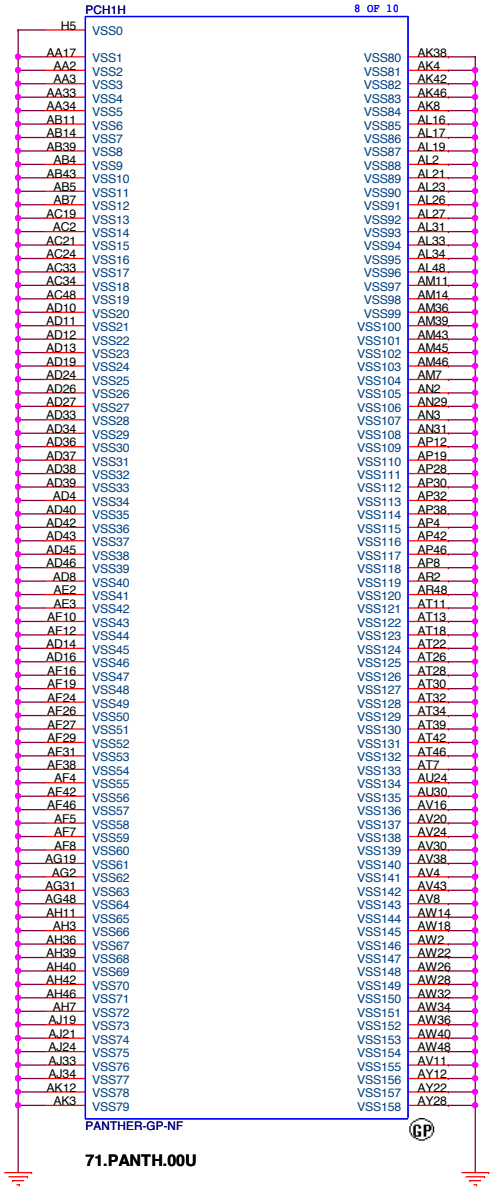
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)

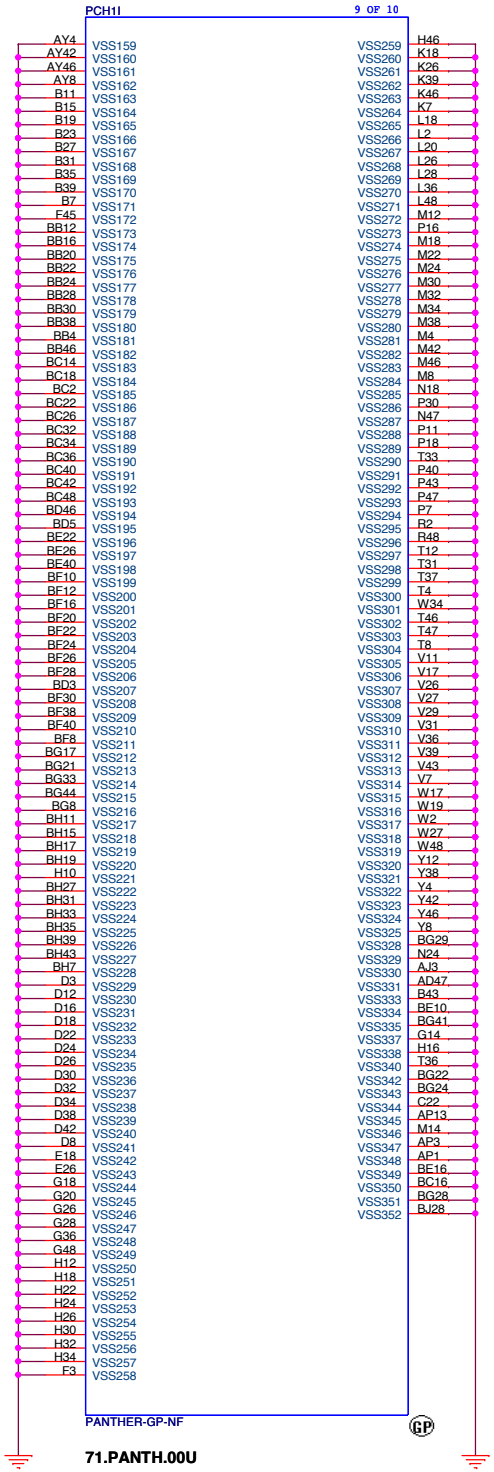
Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 24 of 108

SSID = PCH



71.PANTH.00U



71.PANTH.00U

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 25 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Clock(colay)

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 26 of 108

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100.0K	1.65V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

MODEL_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
BAD50-HC	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
BAD40-HC	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V < 2.875 V
BAD30-HC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V < 2.616 V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

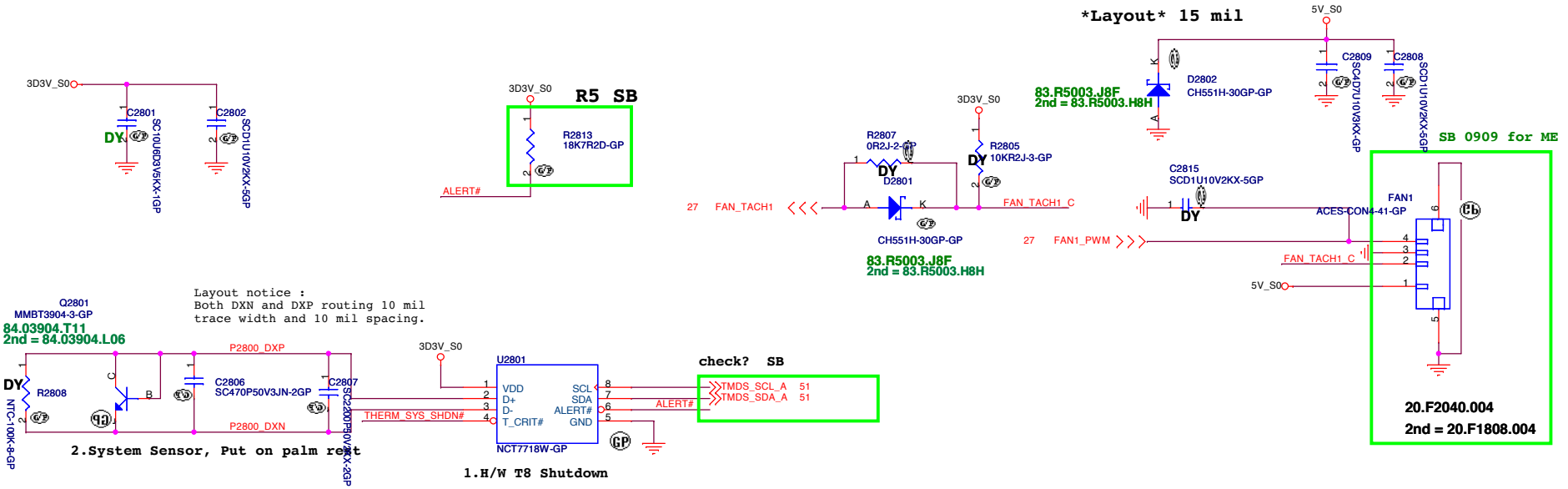
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 27 of 105

SSID = Thermal

Fan controller P2793

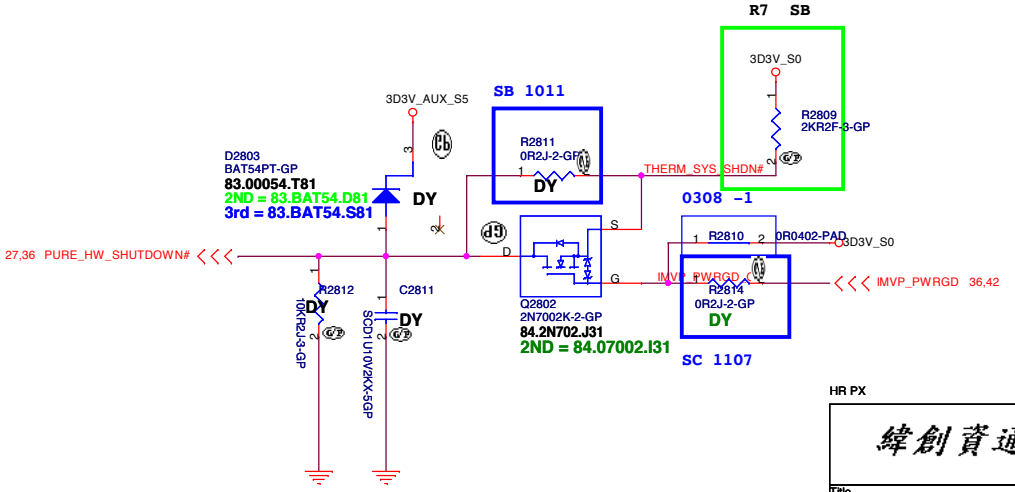
Layout 15 mil



ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point



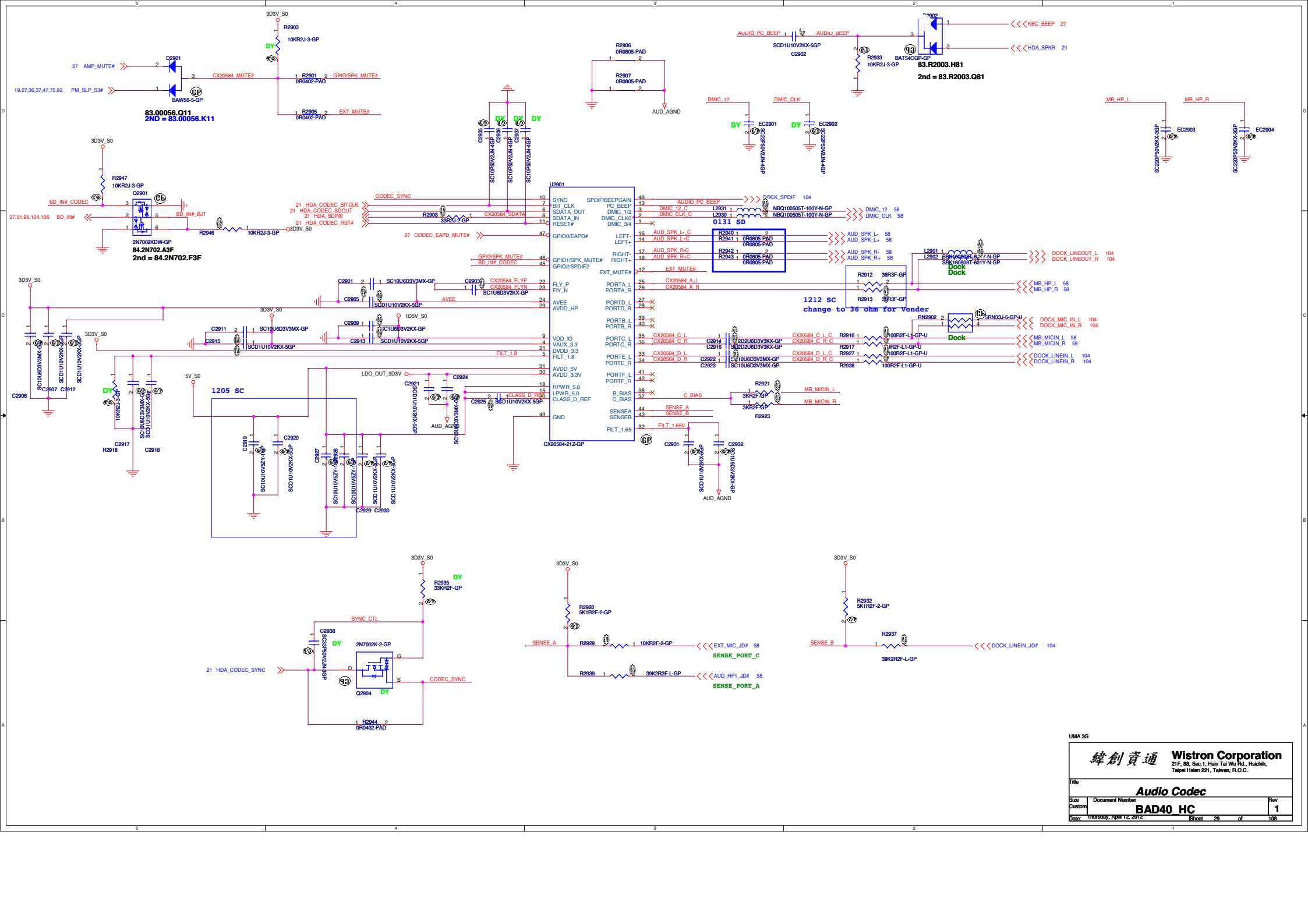
HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal T7718/Fan Controllor P2793

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 28 of 108


U2901
CX20584-21Z-GP
83.00056.Q11
2ND = 83.00056.K11
2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F
0131 SD
1205 SC
1212 SC
change to 36 ohm for Vender
83.R2003.H81
2nd = 83.R2003.Q81
2N7002K-2-GP
Dock
UMA 3G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
BAD40_HC
Rev 1
Thursday, April 12, 2012
Sheet 29 of 106

AUDIO OP AMPLIFIER

<Variant Name>

緯創資通

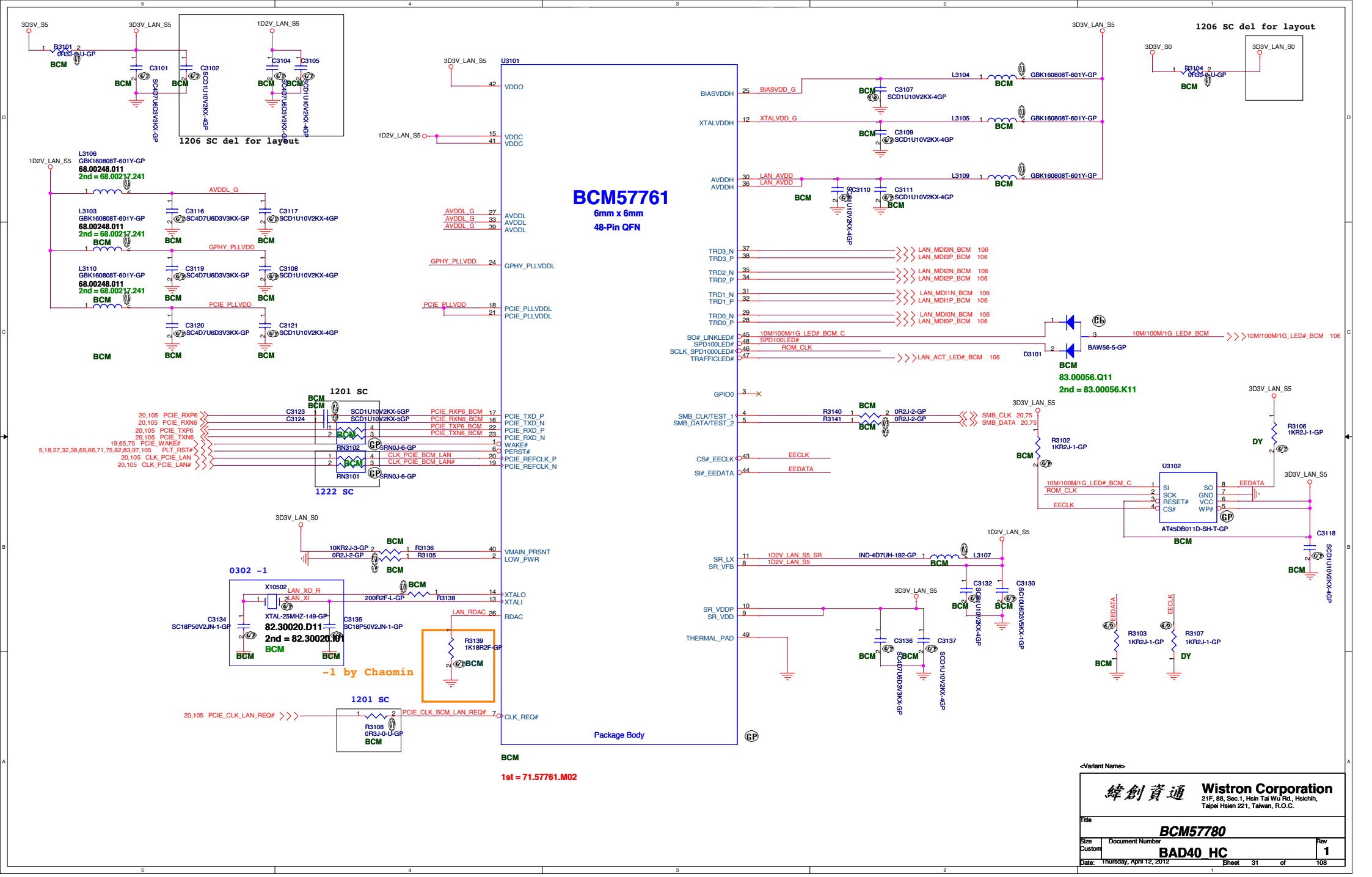
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

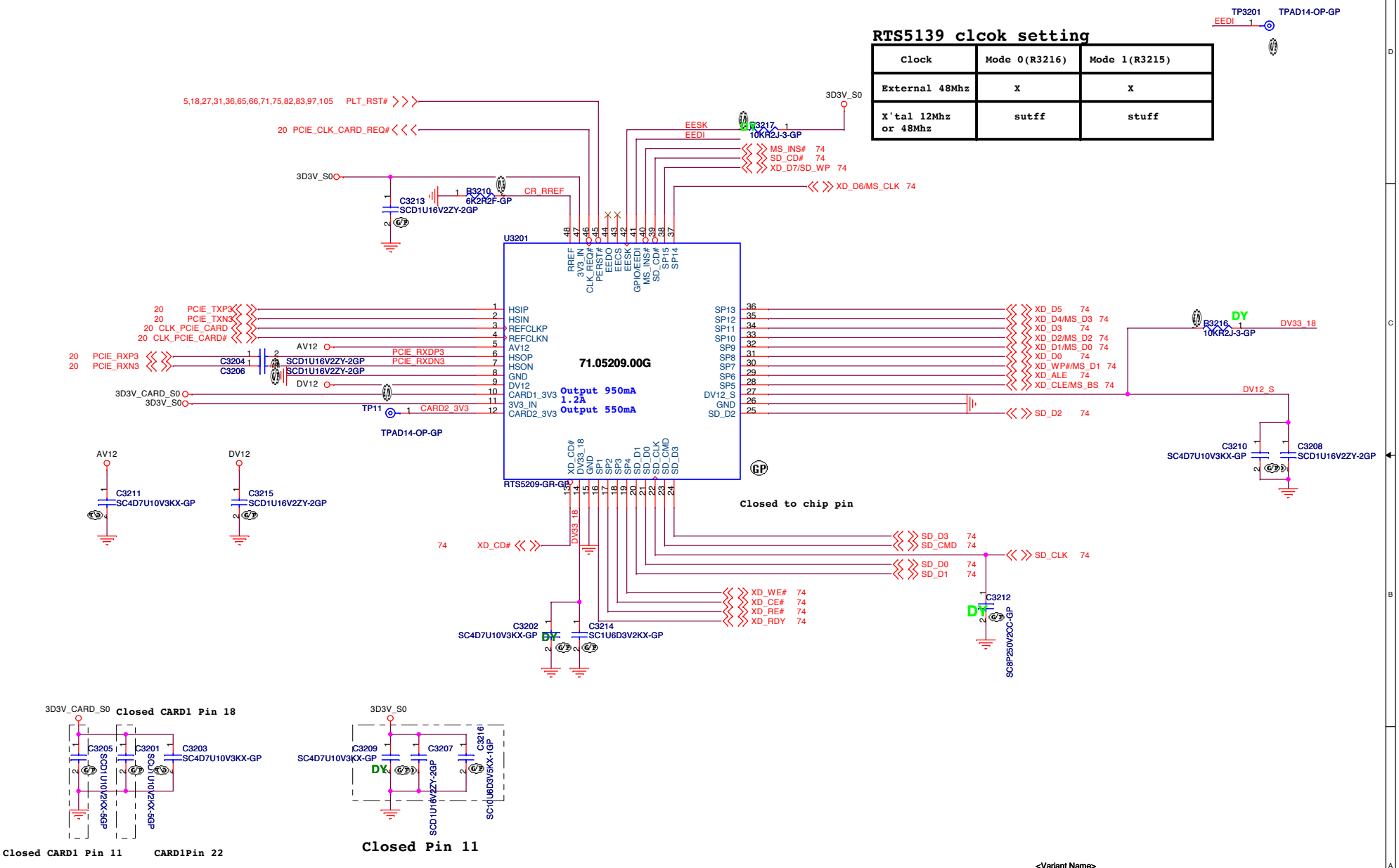
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 30 of 108


BCM57761
6mm x 6mm
48-Pin QFN
Package Body
1206 SC del for layout
1201 SC
1222 SC
0302 -1
-1 by Chaomin
83.00056.Q11
2nd = 83.00056.K11
82.30020.D11
2nd = 82.30020.K01
1st = 71.57761.M02
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM57780
BAD40_HC
Thursday, April 12, 2012
Sheet 31 of 108

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	sutff	stuff



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5209(CARD READER)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 32 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 33 of 108

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 34 of 108

reserve

HR

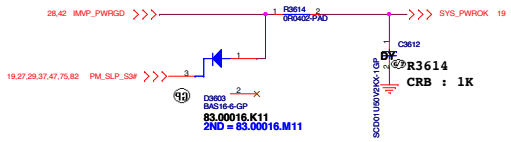
緯創資通 **Wistron Corporation**
21F, 68, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

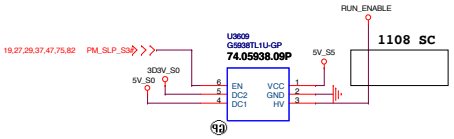
Size	Document Number	Rev
Custom	BAD40_HC	1

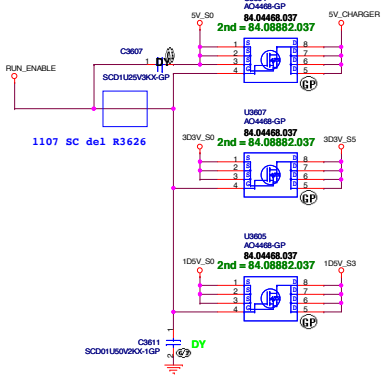
Date: Thursday, April 12, 2012 Sheet 35 of 108

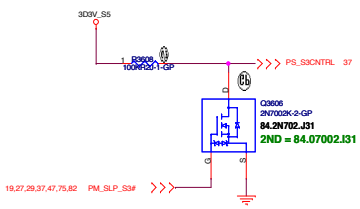
Power Sequence

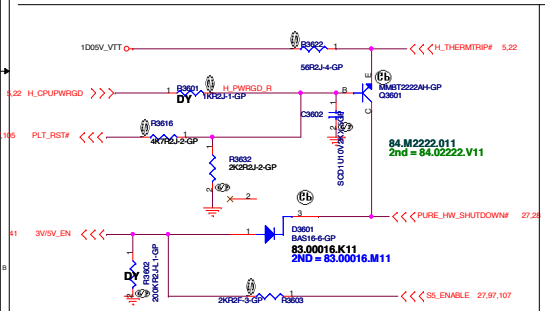


ANNIE Run Power

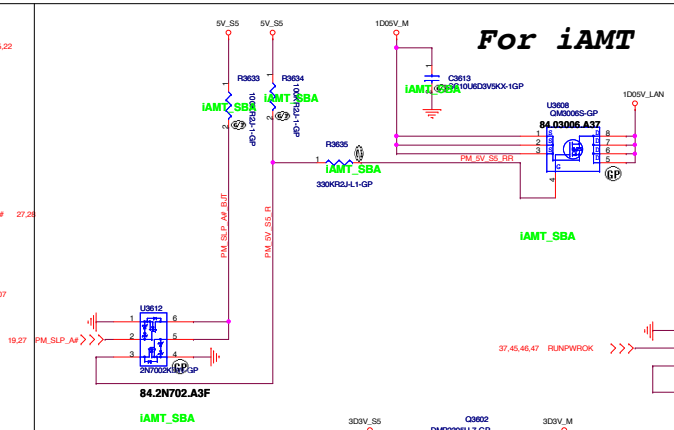


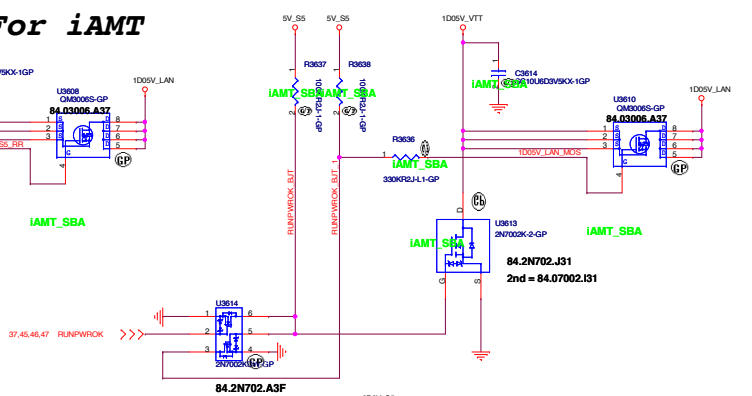






For iAMT

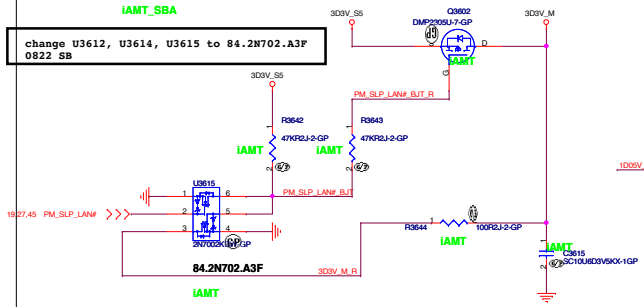


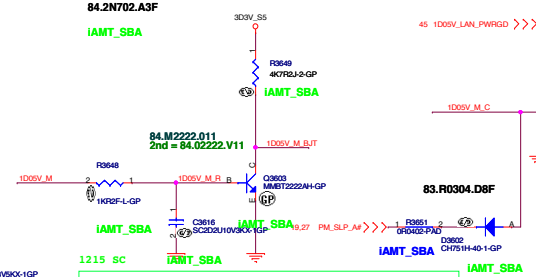


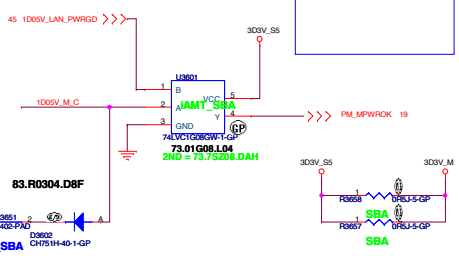
0312 -1 del for layout

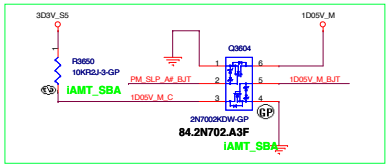
0412 -1M del for layout

change U3612, U3614, U3615 to 84.2N702.A3F
0822 SB









HR PX

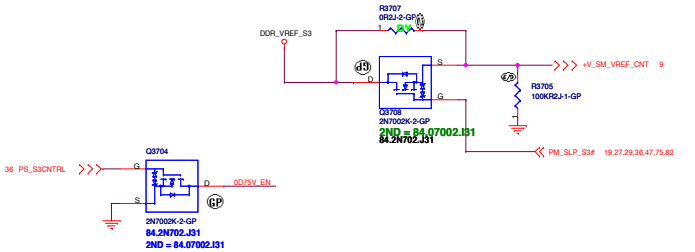
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

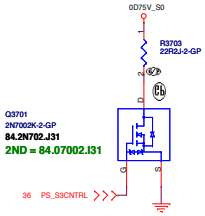
Size	Document Number	Rev
Custom	BAD40 HC	1

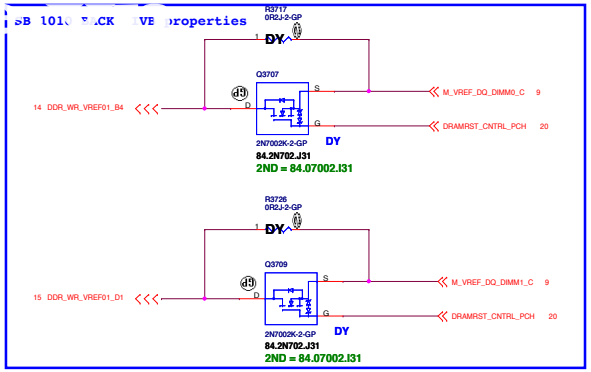
Date: Thursday, April 12, 2012 Sheet 36 of 108

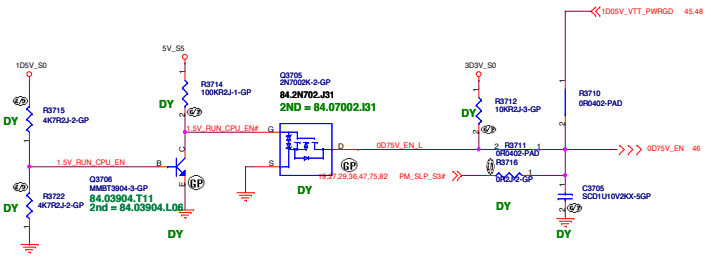
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



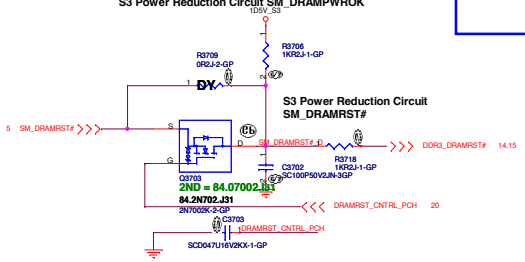
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



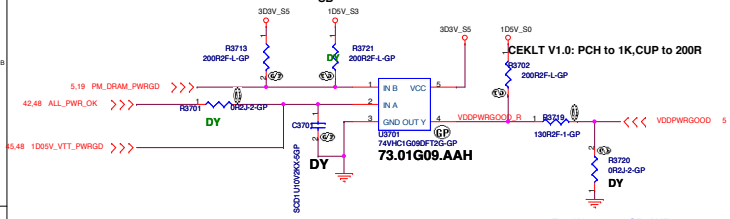




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

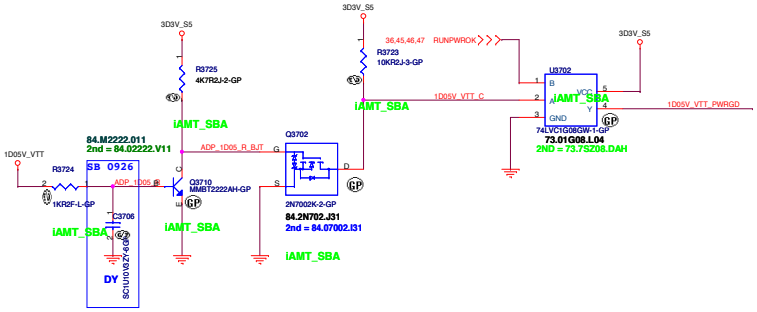


SB
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



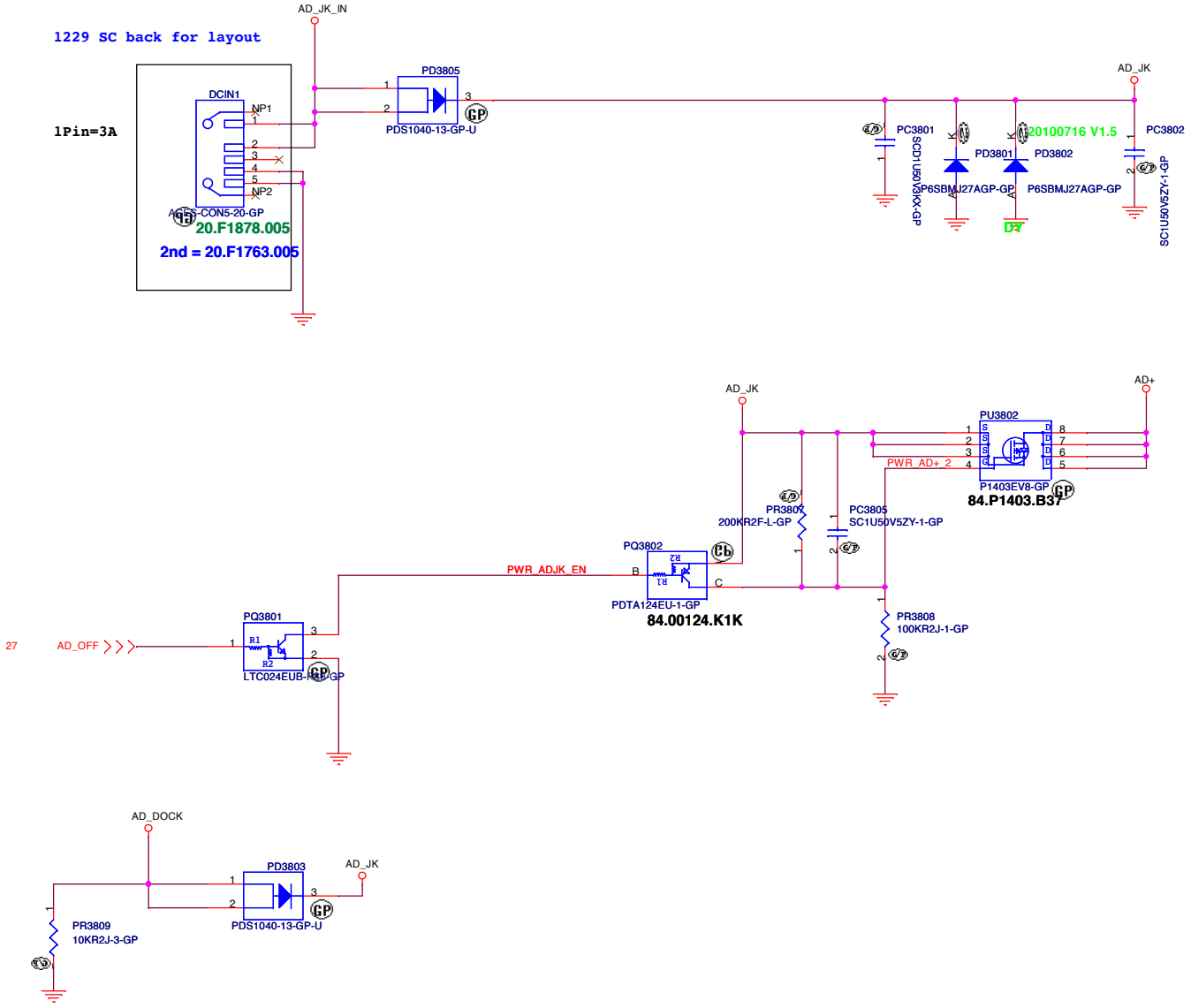
CEKLT V1.0: PCH to 1K,CUP to 200R

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY



HR PX
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 37 of 108

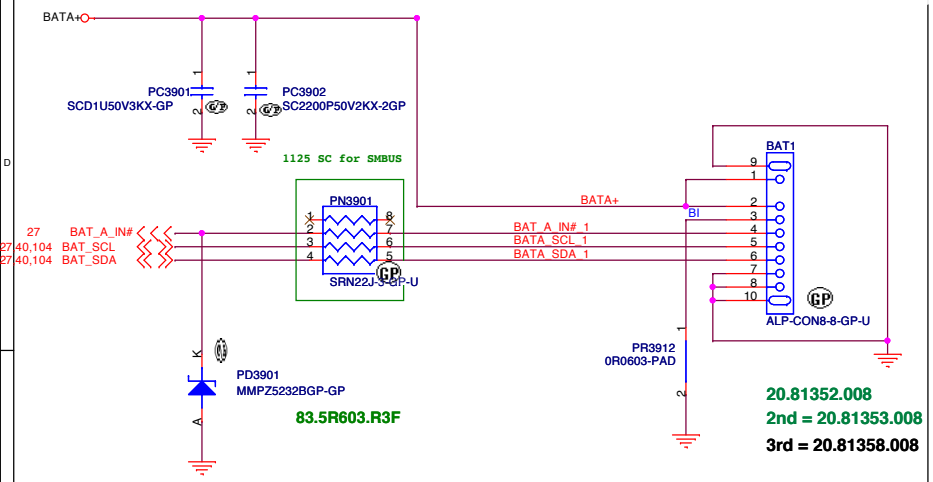


<Variant Name>

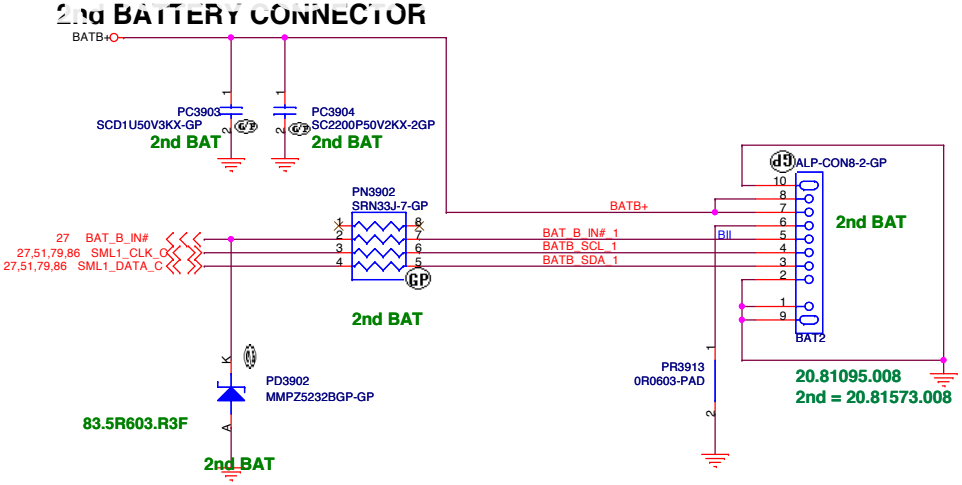
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DCIN JACK***	
Size A3	Document Number **BAD40_HC**	Rev **1**
Date: Thursday, April 12, 2012	Sheet 38 of 108	

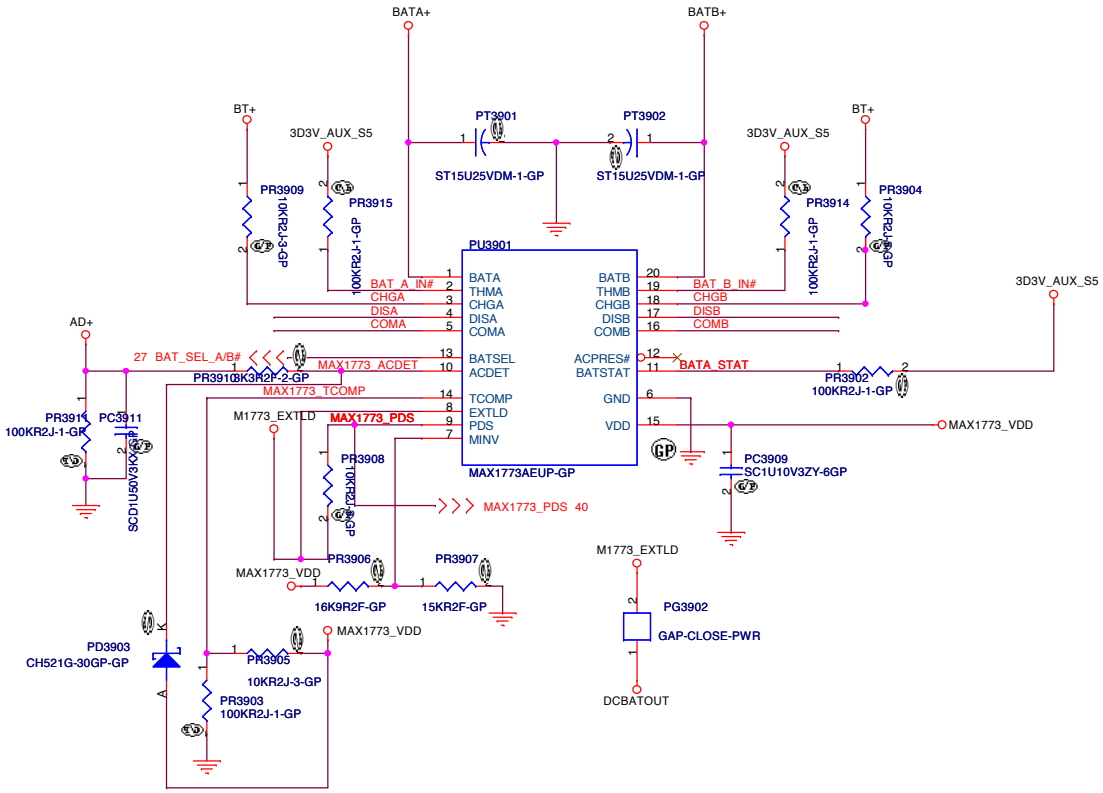
MAIN BATTERY CONNECTOR



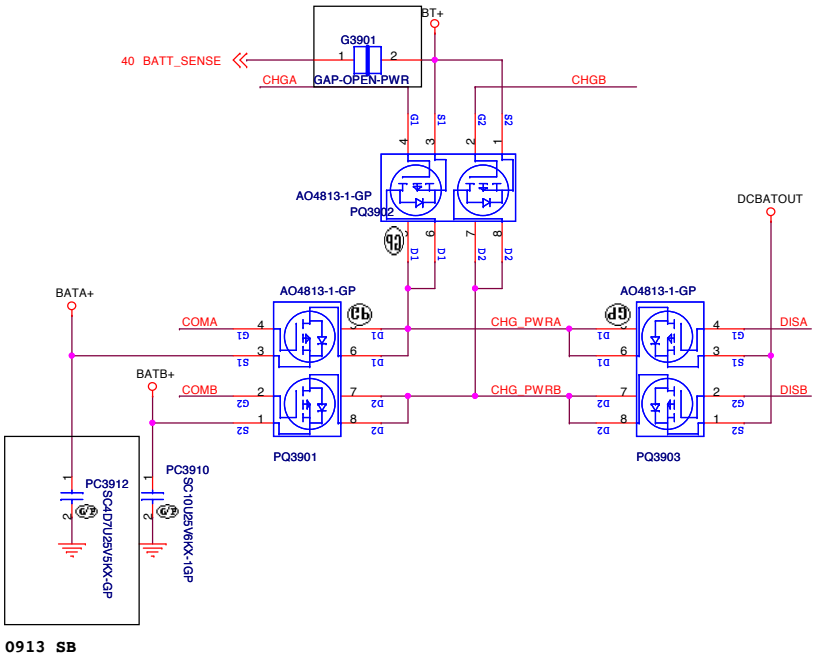
2nd BATTERY CONNECTOR



BATTERY SWITCH



1108 SC



0913 SB

HR PX

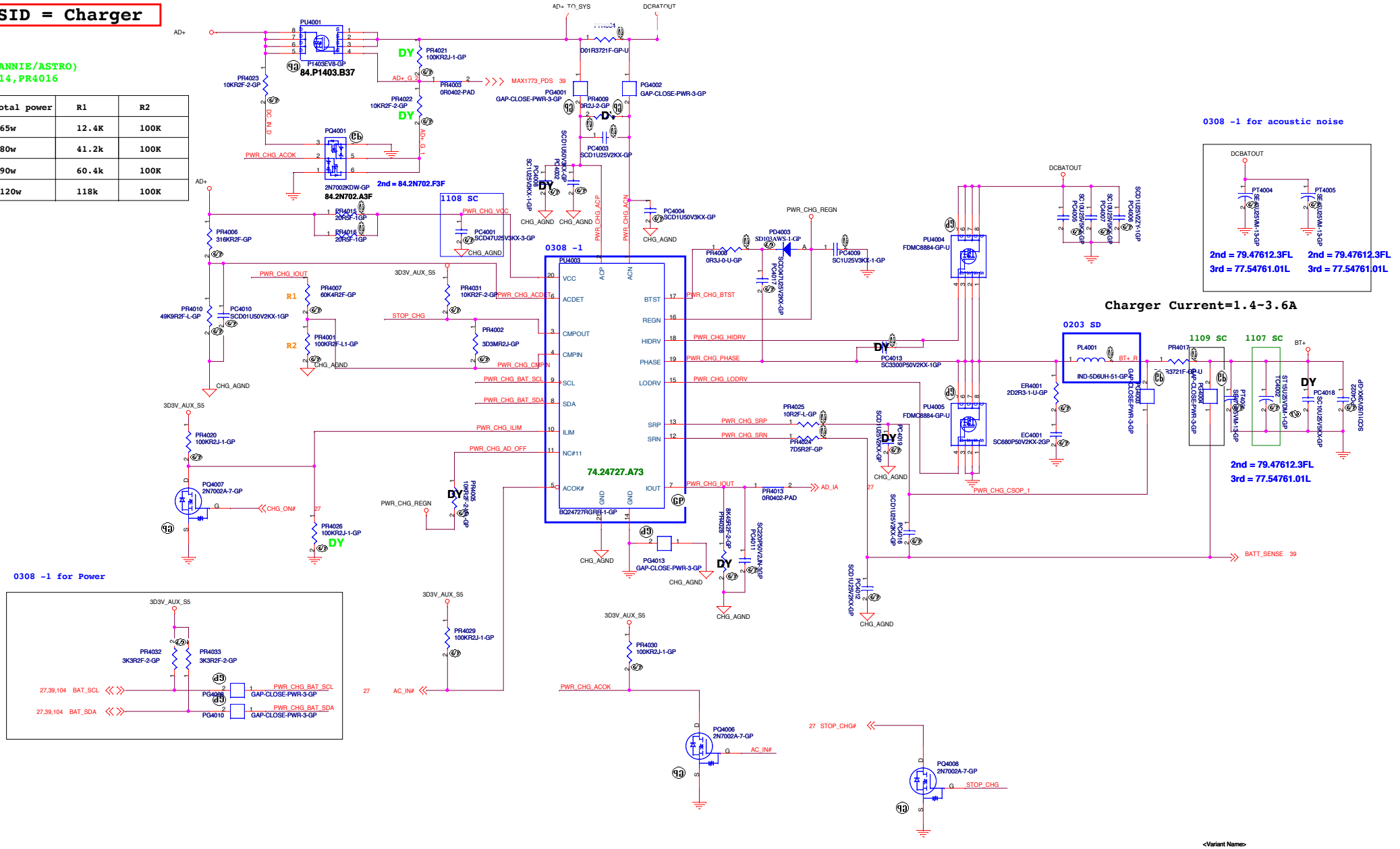
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size A3	Document Number BAD40 HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 39 of 108	

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 40 of 108

0315 -1
del close gap for Layout

1205 SC for Power

PR 04 change to 1K

1222 SC del GAP for layout

1125 SC for RF

1212 SC change to 84.03664.037 for Power

1125 SC for RF

0308 -1
change to 47U
for acoustic noise

2nd = 79.47612.3FL
3rd = 77.54761.01L

Iomax=30A
OCP>40A

SB 0923

1114 SC For EMI

1107 SC

2nd = 79.22710.20L

Iomax=6A
OCP>10A

Vz=3.9V
UVP Function
DCBATOUT<7.5V 3/5V disable

0118 SD for Power

1114 SC for EMI

0308 -1
for acoustic noise

0308 -1

74.08239.B73

<Variant Name>

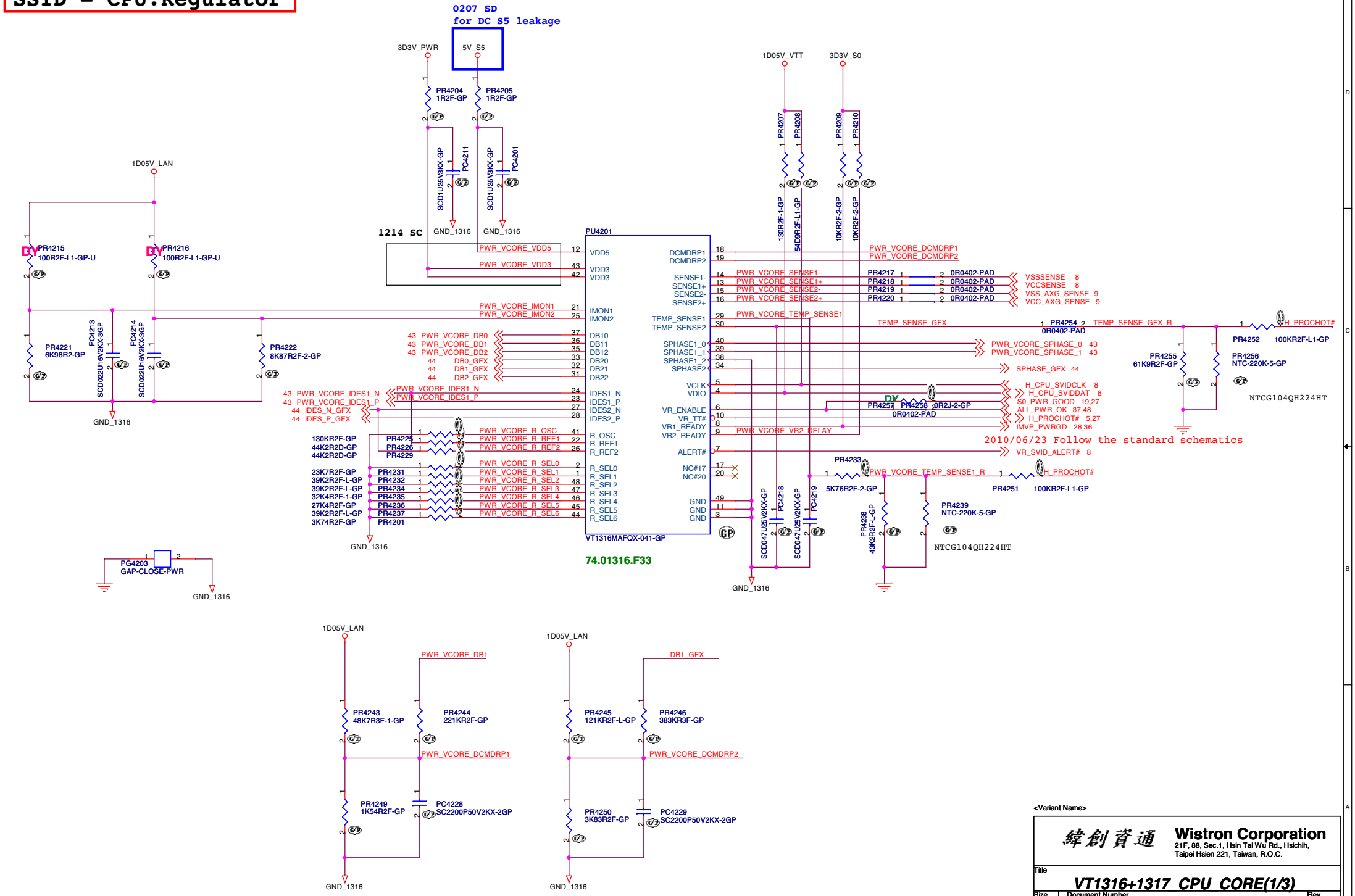
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8329 5V/3D3V

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 41 of 108

SSID = CPU.Regulator



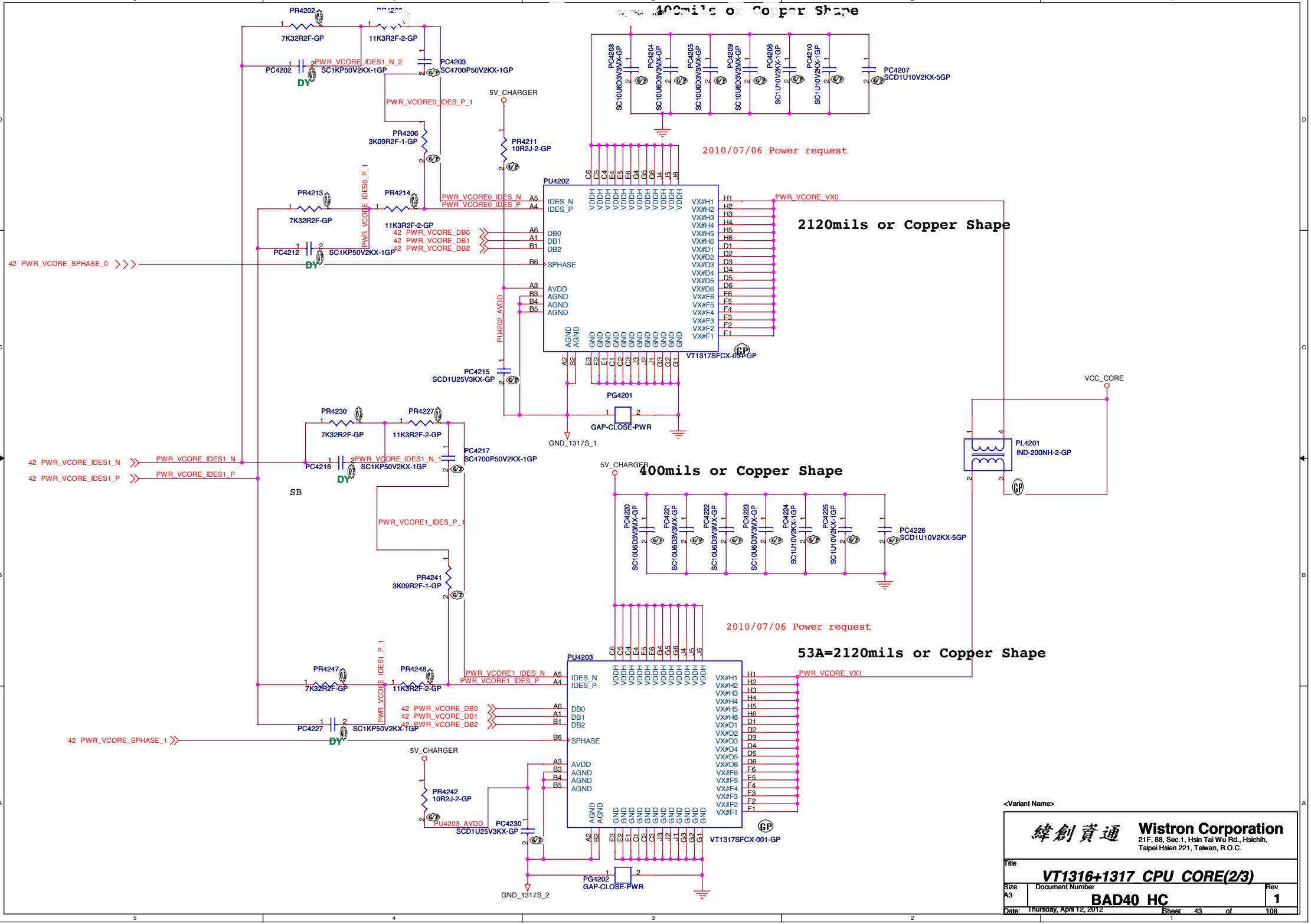
<Variant Name>

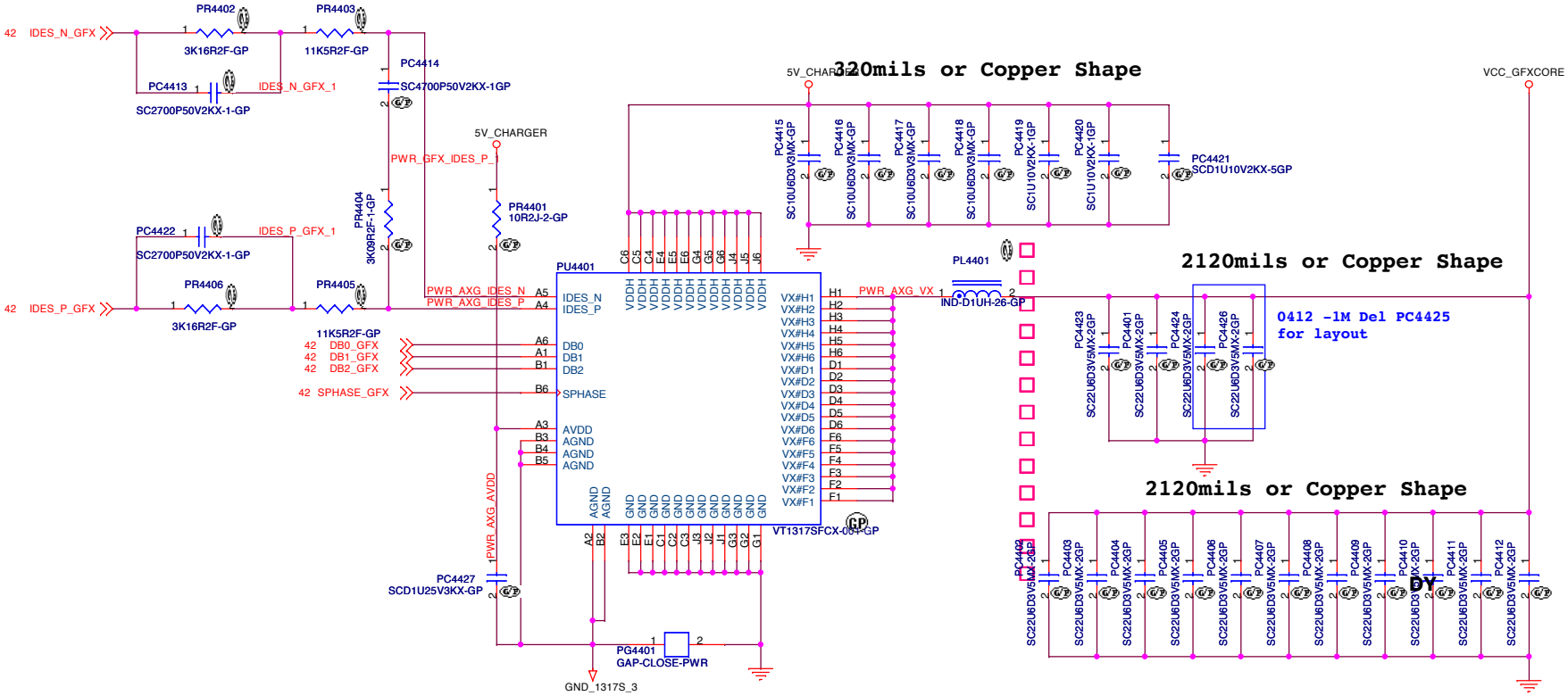
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VT1316+1317 CPU CORE(1/3)*

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 42 of 108


400mils or Copper Shape
2010/07/06 Power request
2120mils or Copper Shape
400mils or Copper Shape
2010/07/06 Power request
53A=2120mils or Copper Shape
SB
PU4202
PU4203
VT1317SFCX-001-GP
PG4201
PG4202
GAP-CLOSE-PWR
PL4201
IND-200NH-2-GP
5V_CHARGER
VCC_CORE
GND_1317S_1
GND_1317S_2
PWR_VCORE_VX0
PWR_VCORE_VX1
PWR_VCORE0_IDES_P_1
PWR_VCORE1_IDES_P_1
PU4202_AVDD
PU4203_AVDD
42 PWR_VCORE_SPHASE_0
42 PWR_VCORE_SPHASE_1
42 PWR_VCORE_IDES1_N
42 PWR_VCORE_IDES1_P
PWR_VCORE_IDES1_N_2
PWR_VCORE_IDES1_N_1
PWR_VCORE0_IDES_N
PWR_VCORE0_IDES_P
PWR_VCORE1_IDES_N
PWR_VCORE1_IDES_P
42 PWR_VCORE_DB0
42 PWR_VCORE_DB1
42 PWR_VCORE_DB2
PWR_VCORE_IDES0_P_1
PWR_VCORE_IDES1_P_1
7K32R2F-GP
11K3R2F-2-GP
3K09R2F-1-GP
10R2J-2-GP
SC1KP50V2KX-1GP
SC4700P50V2KX-1GP
SCD1U25V3KX-GP
SC10U6D3V3MX-GP
SC1U10V2KX-1GP
SCD1U10V2KX-5GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT1316+1317 CPU CORE(2/3)
Size A3
Document Number
BAD40 HC
Rev 1
Date: Thursday, April 12, 2012
Sheet 43 of 108



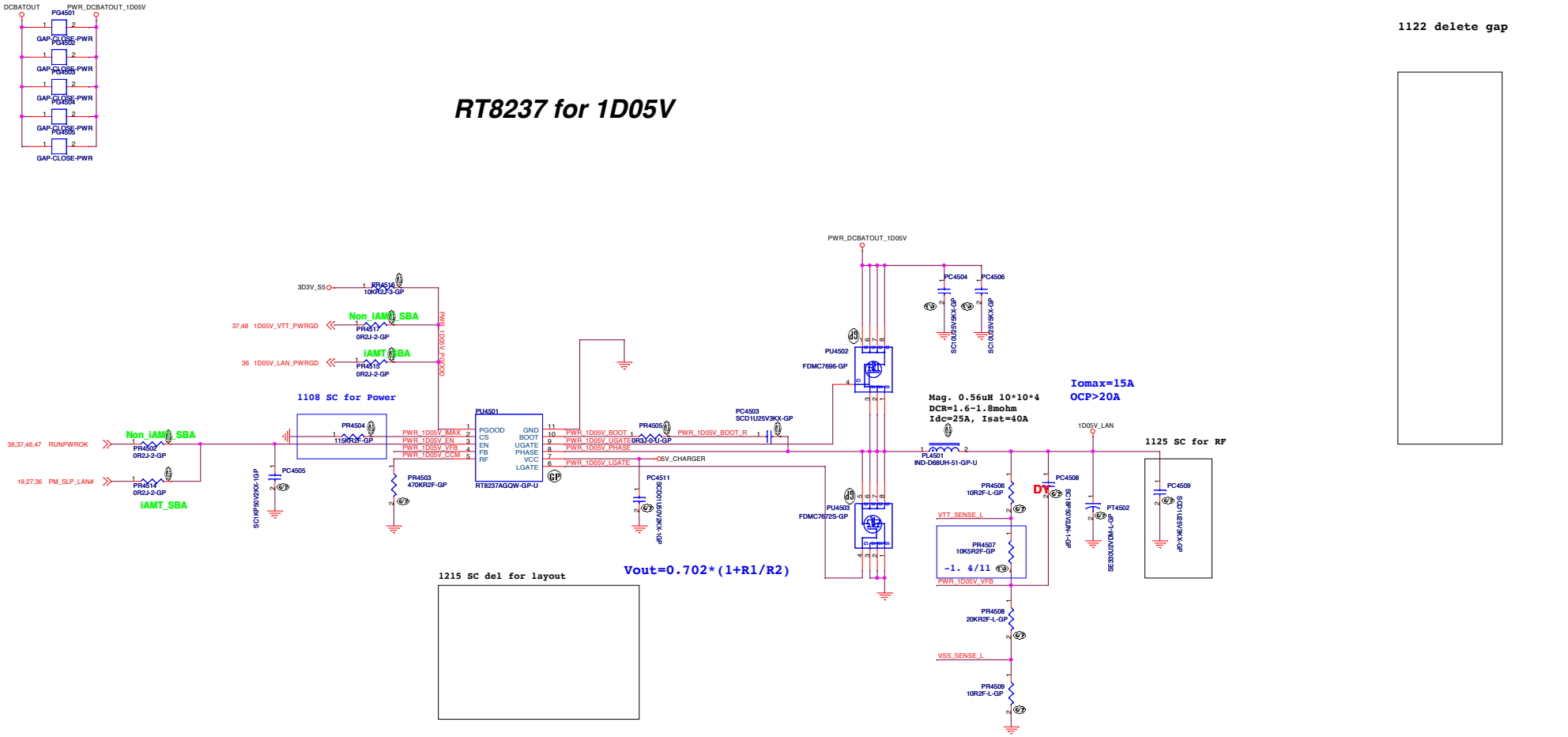
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 CPU CORE(3/3)

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 44 of 108



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

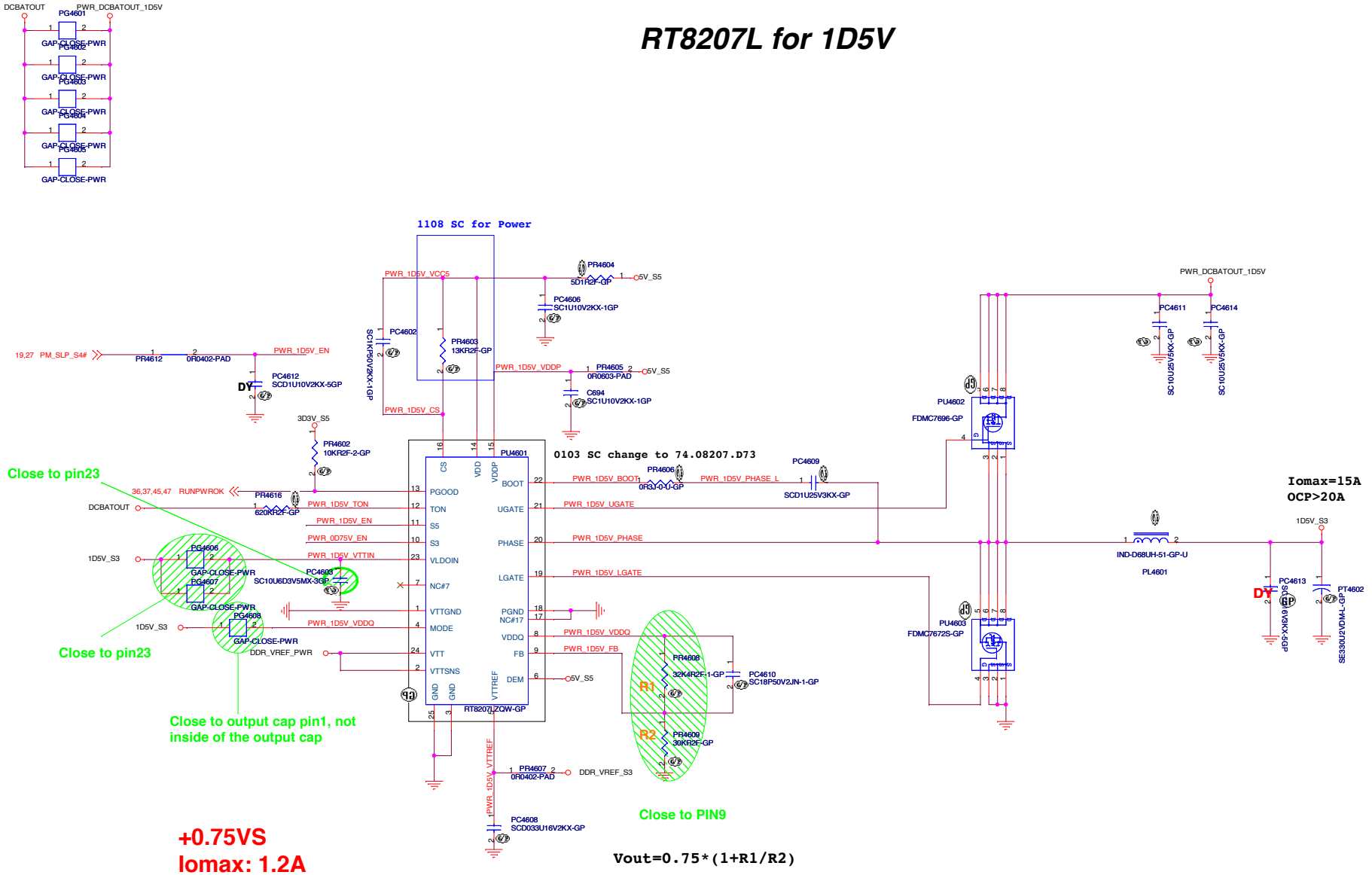
Title: DC to DC 1D05V(RT8237)

Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 45 of 108

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

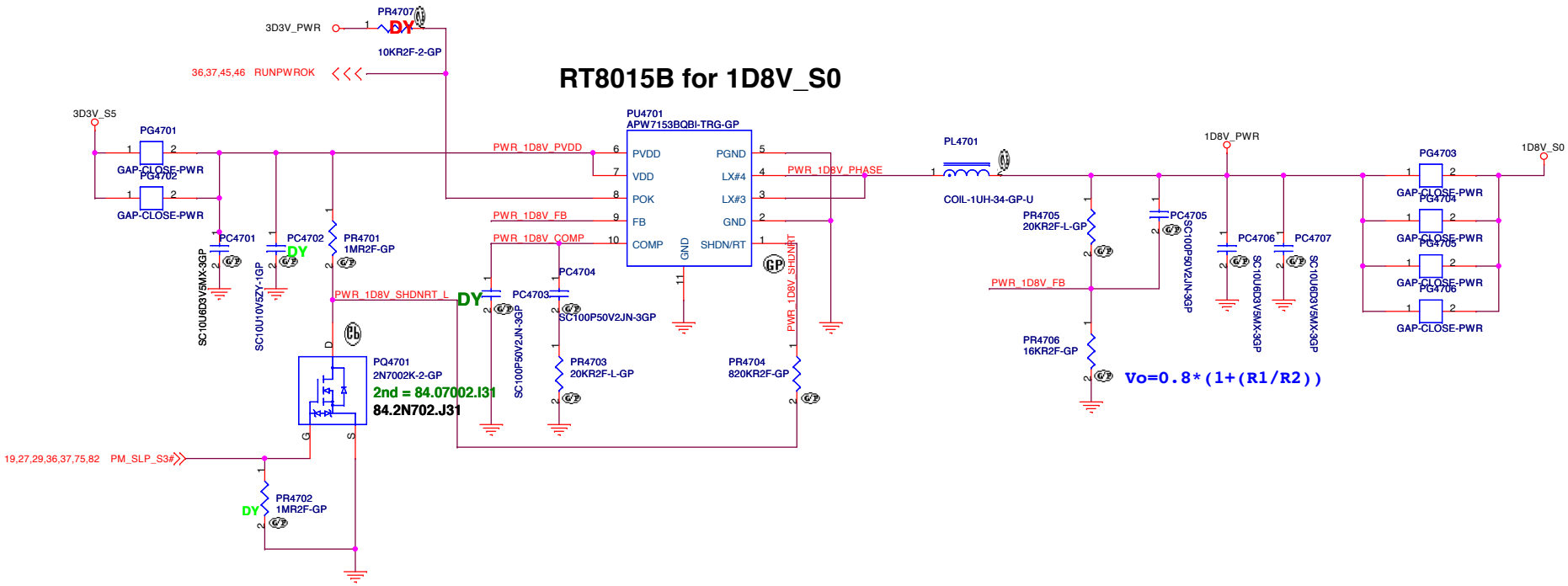
<Variant Name>

Title: RT8207L_+1.5V_SUS

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 46 of 108

SSID = PWR.Plane.Regulator_1p8v



<Variant Name>

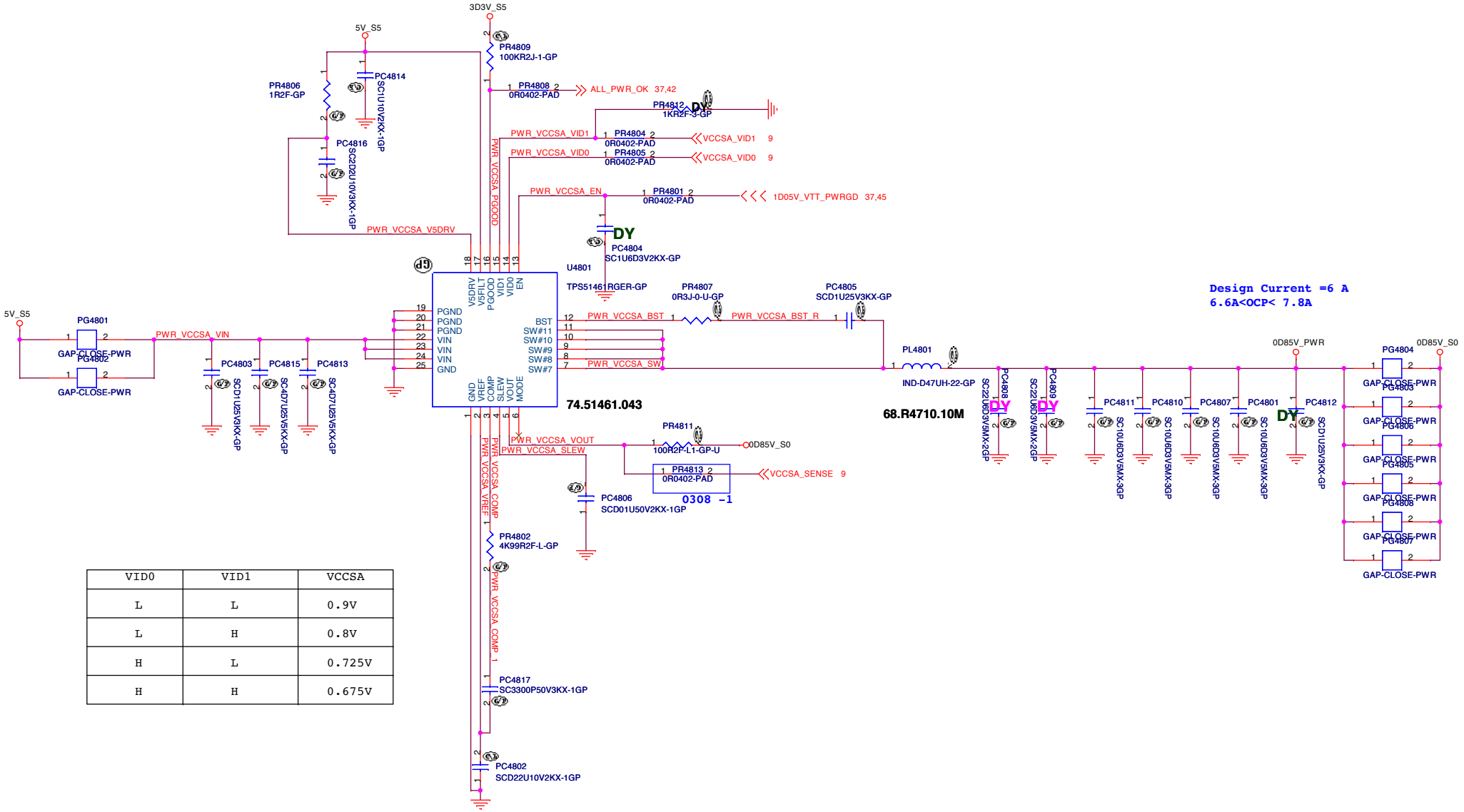
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DC CONVERTER_1D8V(RT8015A)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 47 of 108

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC CONVERTER VCCSA(TPS51461)

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 48 of 108

SSID = VIDEO

INVERTER POWER

F4901
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.A41

DCBATOUT_LCD → C4906 SC470U25V5KX-GP, C4904 SC150U50V2KX-1GP, C4905 SCD1U50V3KX-GP → DCBATOUT

1122 SC del EDP&LVDS colay

LVDS CONNECTOR

DCBATOUT_LCD

LCD1 PS-CON40-GP 20.F1816.040

1206 SC del for layout

BLON_OUT_C
LCD_BRIGHTNESS
33R2J-2-GP R4902
3D3V_CAMERA_S0

DBC_EN_C 103
LBKLT_CTL 94
USB_PN12 18
USB_PP12 18
For Camera, GND
LVDSA_CLK_R 94
LVDSA_CLK_R# 94
LVDSA_DATA2_R 94
LVDSA_DATA2_R# 94
LVDSA_DATA1_R 94
LVDSA_DATA1_R# 94
LVDSA_DATA0_R 94
LVDSA_DATA0_R# 94
DP_DATA1_R 103
DP_DATA1_R# 103
DP_AUX 103
DP_AUX# 103
DP_DATA0_R 103
DP_DATA0_R# 103
EDP#_LVDS_R
LVDS_DDC_DATA 94
LVDS_DDC_CLK 94
3D3V_S0
LCDVDD

C4901 SCD1U10V2KX-L1-GP
C4902 SC1U6D3V2KX-L-1-GP

Camera Power

F4902
FUSE-1D1A6V-4GP-U
69.50007.691
2ND = 69.50007.771

3D3V_S0 → 3D3V_CAMERA_S0
C4903 SC10U6D3V5MX-3GP

R4915 100KR2J-1-GP DY LVDSA_DATA2# DP_AUX#
R4916 100KR2J-1-GP DY LVDSA_DATA2_DP_AUX
R4917 100KR2J-1-GP DY LVDSA_DATA2# DP_AUX#
R4918 100KR2J-1-GP DY LVDSA_DATA2_DP_AUX

1121 SC

3D3V_S0 → R4919 10KR2J-L-GP
3D3V_S0 → R4933 10KR2J-L-GP
0131 SD
EDP#_LVDS_D → R4929 0R0402-PAD → EDP#_LVDS 22
Q4904 MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
EDP#_LVDS_R → R4923 150KR2J-L1-GP → EDP#_LVDS_B

SSID = VIDEO

LCD POWER for ANNIE

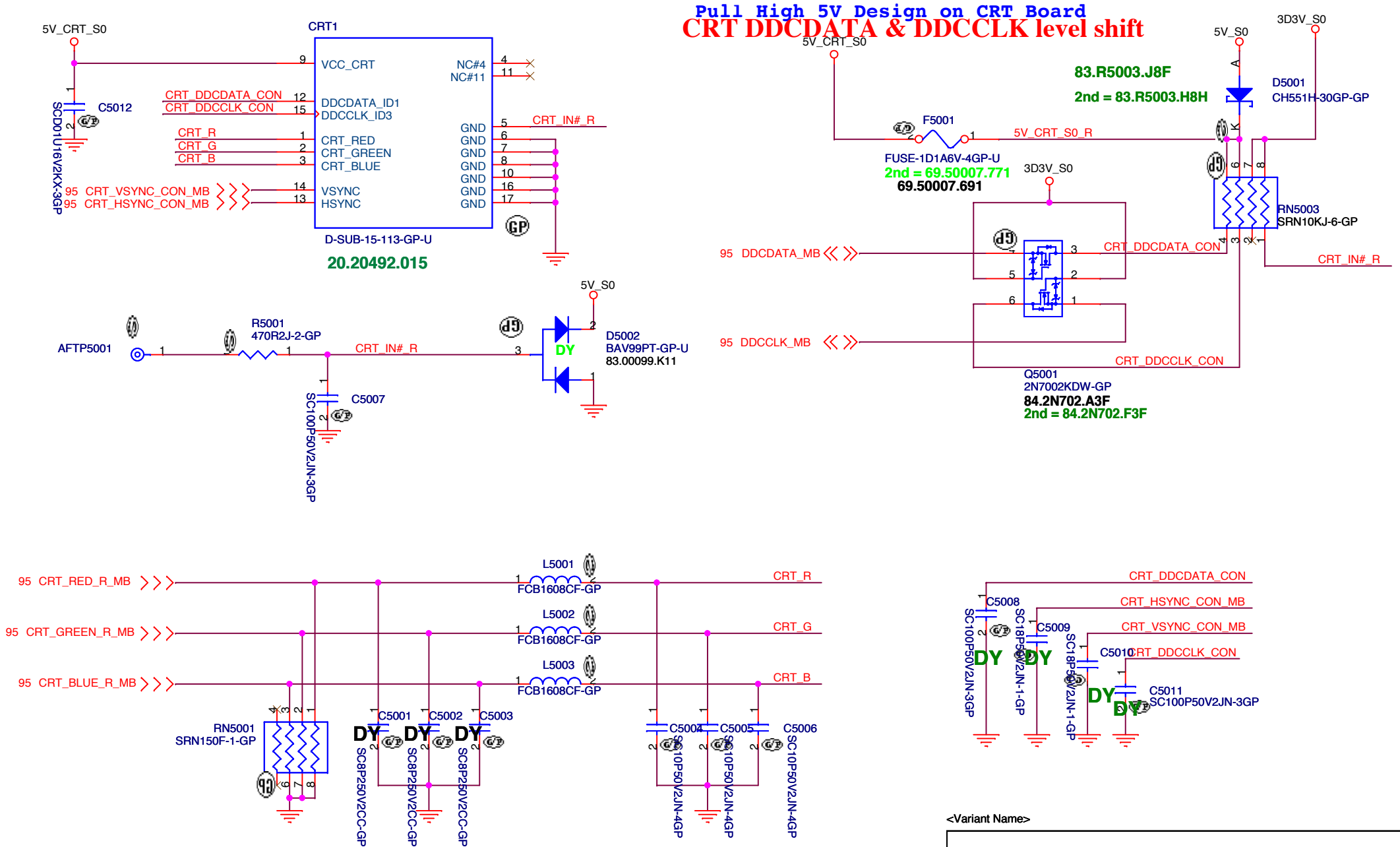
LCDVDD
94 LCDVDD_EN
Layout 40 mil
U4901 RT9724GB-GP
EN, GND, VOUT, VIN#5, VIN#4
3D3V_S0
R4914 100KR2J-1-GP
C4909 SCD1U16V2KX-3GP DY
C4908 SC4D7U6D3V3KX-GP
C4907 SC4D7U6D3V3KX-GP
74.09724.09F

R4904 10KR2J-3-GP DY → 3D3V_S0
DBC_EN_C → R4901 33R2J-2-GP → DBC_EN → TP4901
R4906 DY 10KR2J-3-GP DY
27 BLON_OUT → R4903 1KR2J-1-GP → BLON_OUT_C
R4911 100KR2J-1-GP
C4910 SC100P50V2JN-3GP

<Variant Name>

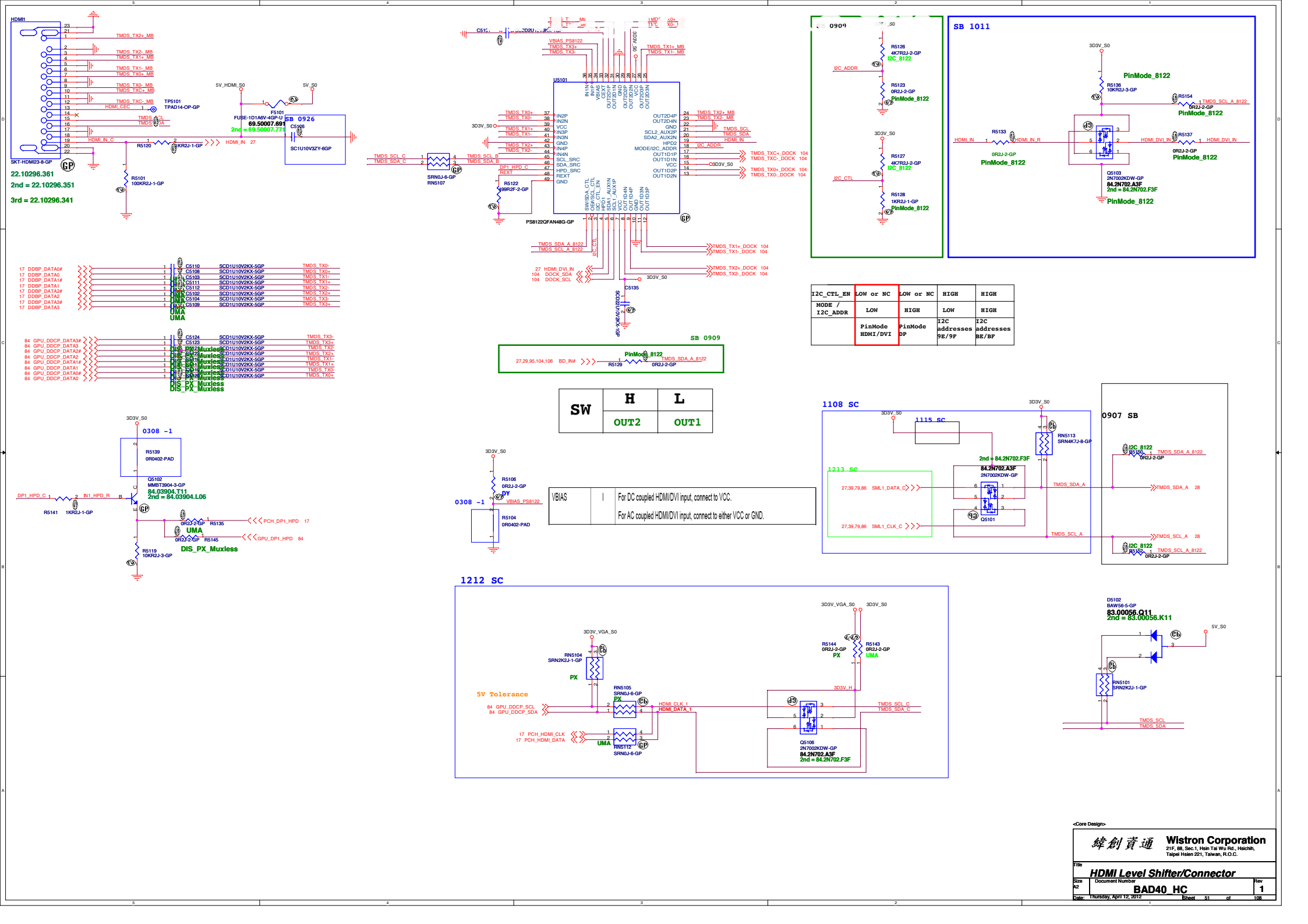
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A3
Document Number: BAD40_HC
Rev: 1
Date: Thursday, April 12, 2012
Sheet 49 of 108



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CRT Connector***
Size: A4	Document Number: **BAD40_HC**
Rev: 1	
Date: Thursday, April 12, 2012	Sheet 50 of 108



<Core Design>

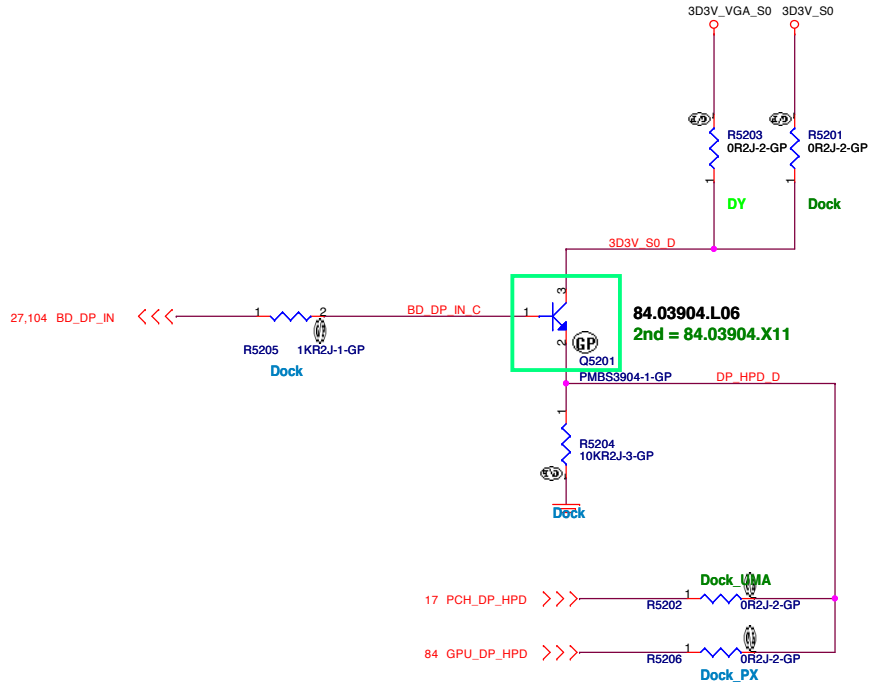
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

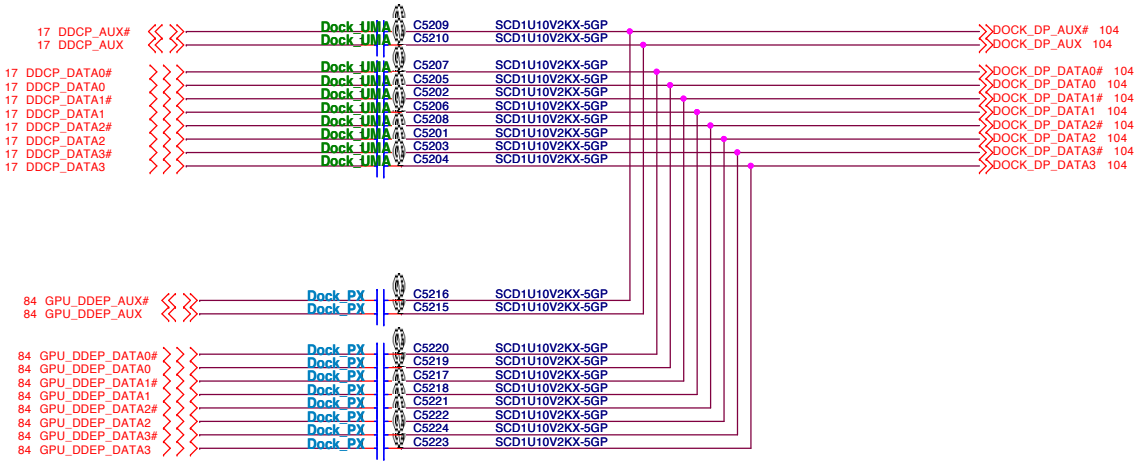
Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 51 of 108

DP





HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display Port***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 52 of 108

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 53 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

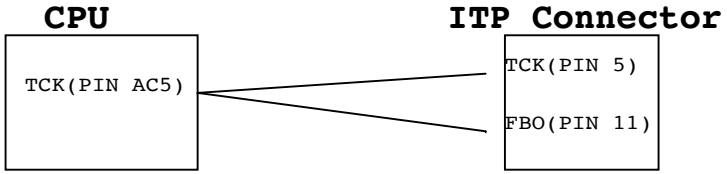
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 54 of 108

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



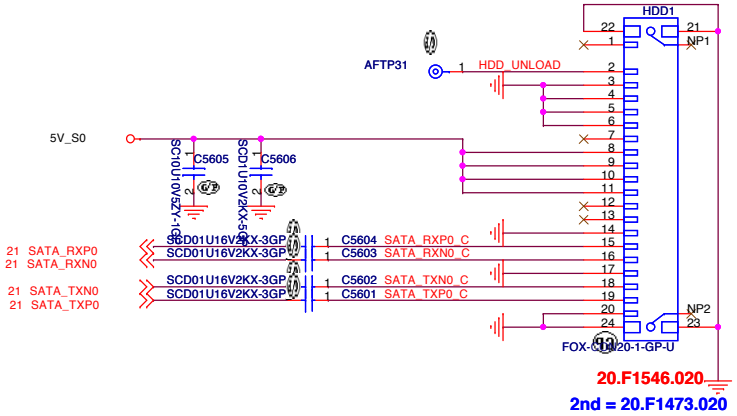
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

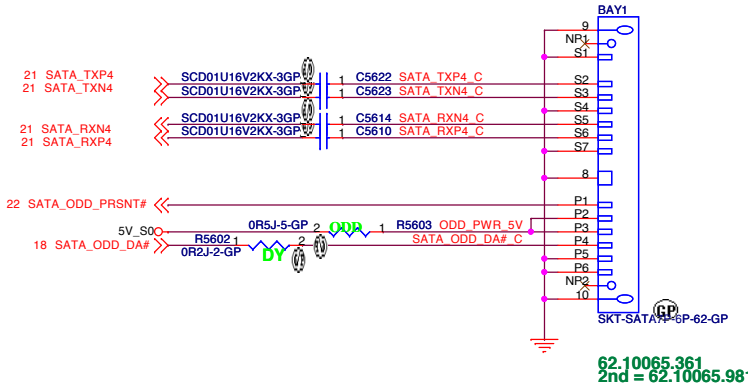
Title: ITP		
Size: A4	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 55 of 108	

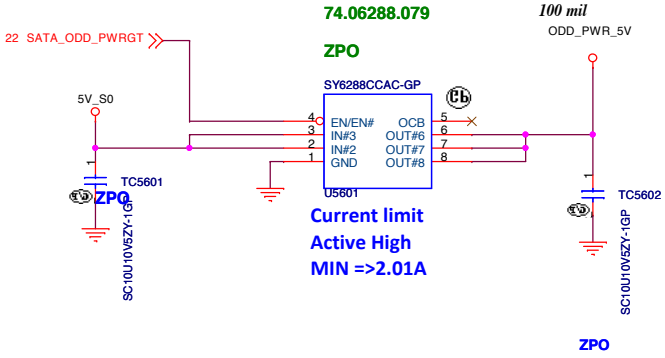
SSID = SATA

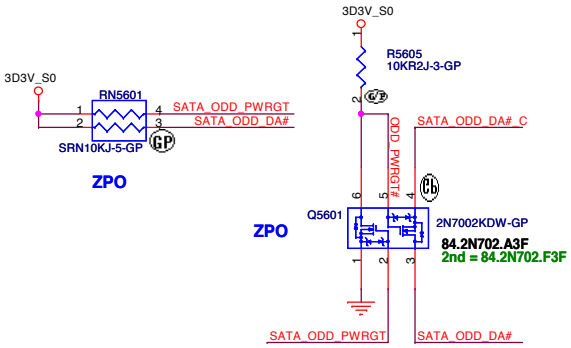
SATA HDD Connector



ODD Connector







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: BAD40 HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 56 of 108

reserved

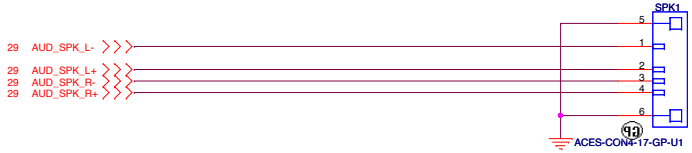
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***E-SATA/USB CHARGER***	
Size: Custom	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 57 of 108	

SSID = AUDIO

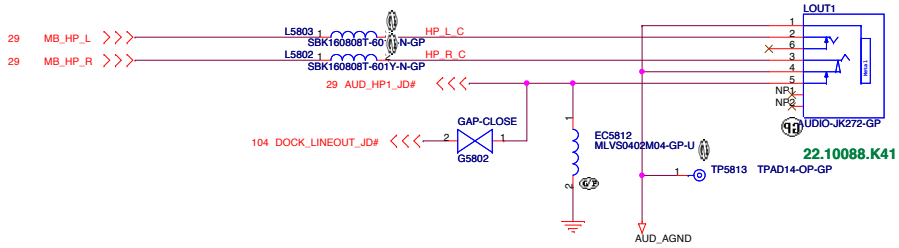
Speaker Connector



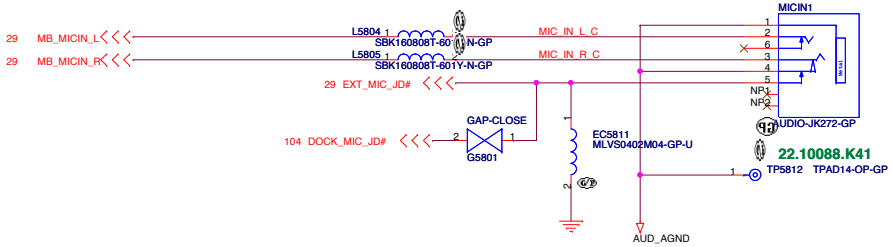
20.F1621.004

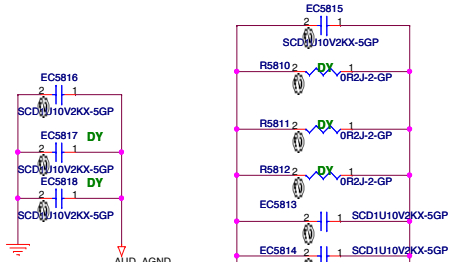
2nd = 20.F1937.004

LINE OUT

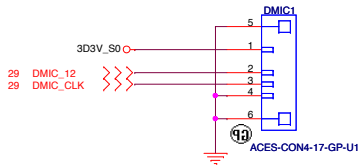


MIC IN





Internal Microphone

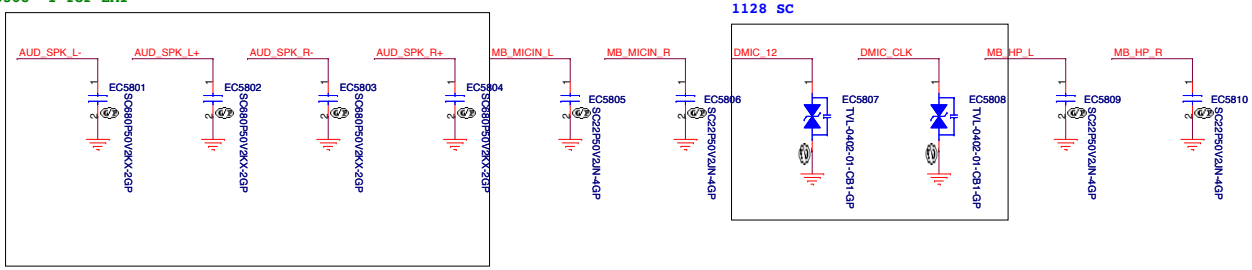


20.F1621.004

2nd = 20.F1937.004

0308 -1 for EMI

1128 SC



<Variant Name>

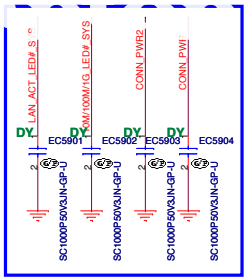
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

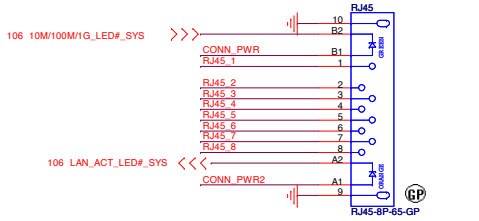
Title: Audio Jack

Size: Custom | Document Number: BAD40_HC | Rev: 1

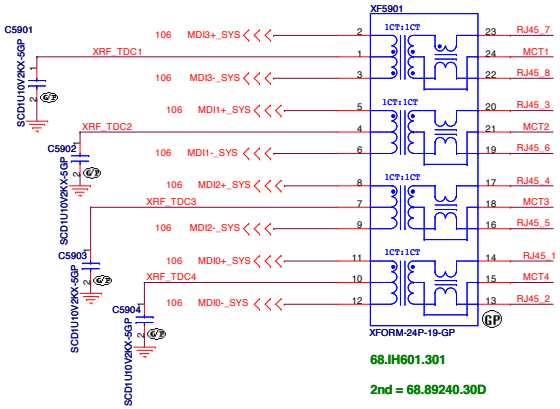
Date: Thursday, April 12, 2012 | Sheet 58 of 108

SSID = LOM

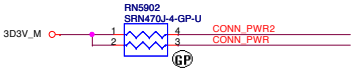


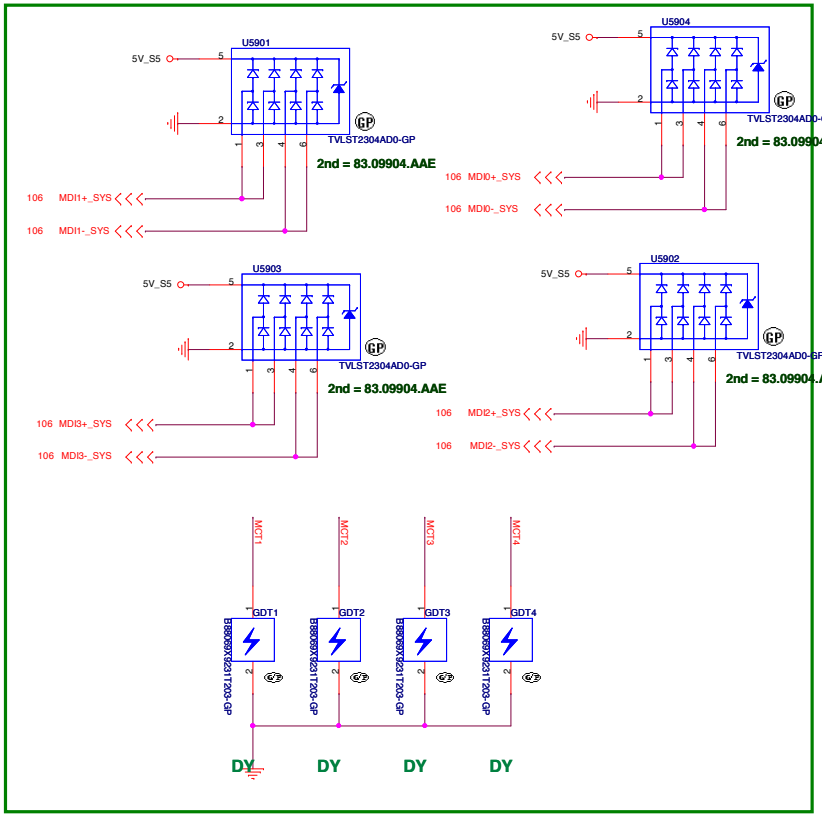


22.10177.J21
2nd = 22.10177.J51

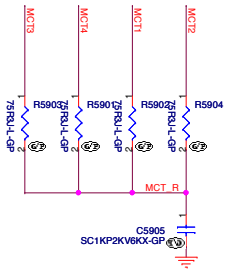


68.IH601.301
2nd = 68.89240.30D





2nd = 83.09904.AAE



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

Size	Document Number	Rev
Custom	BAD40_HC	1

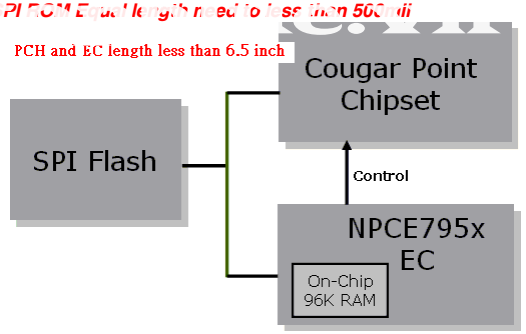
Date: Thursday, April 12, 2012 Sheet 59 of 108

SPI FLASH ROM (8M byte) for PCH

SSID = Flash.ROM

SPI ROM Trace length need to less than 500 mil

PCH and EC length less than 6.5 inch



1212 SC

64MB:72.25640.D01,72.25Q64.B01
32MB:72.25Q32.A01, 72.25320.C01

SYSTEM SPI ROM

1216 SC

3D3V_S5

R6011 4K7R2J-2-GP
R6016 4K7R2J-2-GP
R6017 4K7R2J-2-GP

SPI_HOLD_0#

C6002 SCD1U10V2KX-3GP
C6003 SCD1U10V2KX-3GP

21 SPI_CS0#_R
21 SPI_SO_R

R6001 33R2J-2-GP

SPI_SO_0
SPI_WP#_0

U6001
CE# VDD
SO HOLD#
WP# SCK
VSS SI

SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_CLK_R_0
SPI_SI_R_0

R6012 33R2J-2-GP
R6013 33R2J-2-GP

SPI_CLK_R_21
SPI_SI_R_21

R6008 4K7R2J-2-GP
R6009 4K7R2J-2-GP
R6010 4K7R2J-2-GP

DUAL ROM

21 SPI_CS1#_R
21 SPI_SO_R

R6007 33R2J-2-GP

SPI_SO_1
SPI_WP#_1

U6003
SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_HOLD_1#
SPI_CLK_R_1
SPI_SI_R_1

R6014 33R2J-2-GP
R6015 33R2J-2-GP

SPI_CLK_R_C
SPI_SI_R_C

1230 SC

RN6001 4RN0J-6-GP

SPI_CLK_R_21
SPI_SI_R_21

SSID = RBATT

3D3V_AUX_S5

D6001 BAS16-6-GP

83.00016.K11
2nd = 83.00016.M11

DY

+RTC_PWR_R

R6002 1KR2J-1-GP

20.F1639.002
2nd = 20.F1804.002

RTC_AUX_S5

Q6001 CH715FGP-GP-U

RTC_PWR1

R6006 510R2J-1-GP

+RTC_PWR

RTC1

ACES-CON2-20-GP

Width=20mils

83.R0304.D81
2nd = 83.R2004.G81

EC BIOS Flash ROM

256KB

3D3V_AUX_S5

for ENE FAE suggest,SPICS# is push-pull pin,
don't need to pull high

R6003 10KR2J-3-GP
R6004 10KR2J-3-GP

SPI_HOLD#

27 SPICS#
27 SPIDI
27 SPI_WP2#

150R2F-1-GP

ER6001

SPI_DI
SPI_WP2#

R6003 10KR2J-3-GP

U6002
CE# VCC
SO HOLD#
WP# SCK
GND SIO

PM25LD020C-SCE-GP
72.25020.E01
2nd = 72.25020.00D

SPI_3D3V_VCC
SPI_HOLD#
SPICLK_1
SPI_DO

150R2F-1-GP
150R2F-1-GP

ER6004 0R0603-PAD
C6004 SCD22U16V3KX-2-GP
ER6003
ER6002

SPICLK 27
SPIDO 27

SPICLK_1
SPI_DO
SPIDI

EC6004 SC4D7P50V2CN-1GP
EC6005 SC4D7P50V2CN-1GP
EC6006 SC4D7P50V2CN-1GP

DY DY DY

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Flash/RTC*

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 60 of 108

SSID = USB

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 61 of 108

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Port

Size	Document Number	Rev
A3	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 62 of 108

SSID = User.Interface

Bluetooth Module conn.

reserved 1216

<Variant Name>

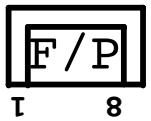
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 63 of 108

Finger printer



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

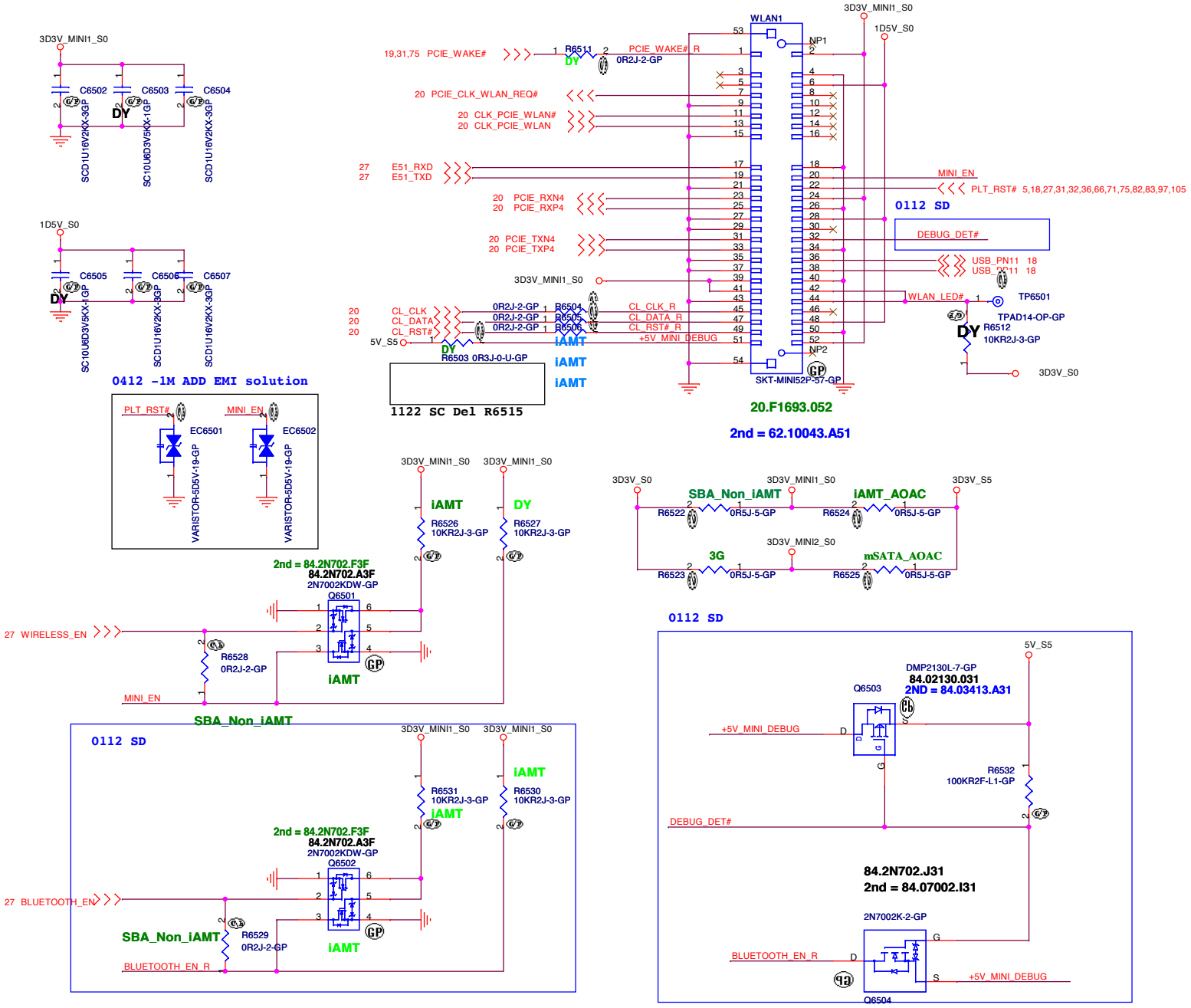
Title
RESERVED

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 64 of 108

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/TP CONN***

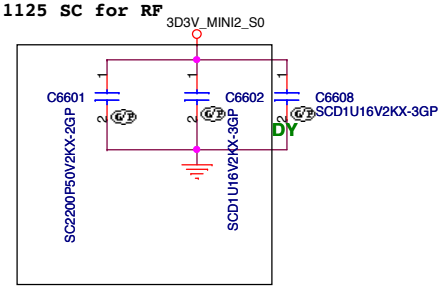
Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 65 of 108

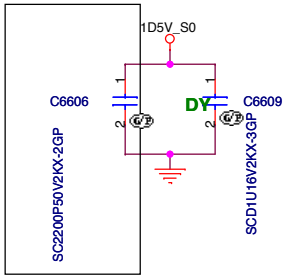
SSID = Wireless

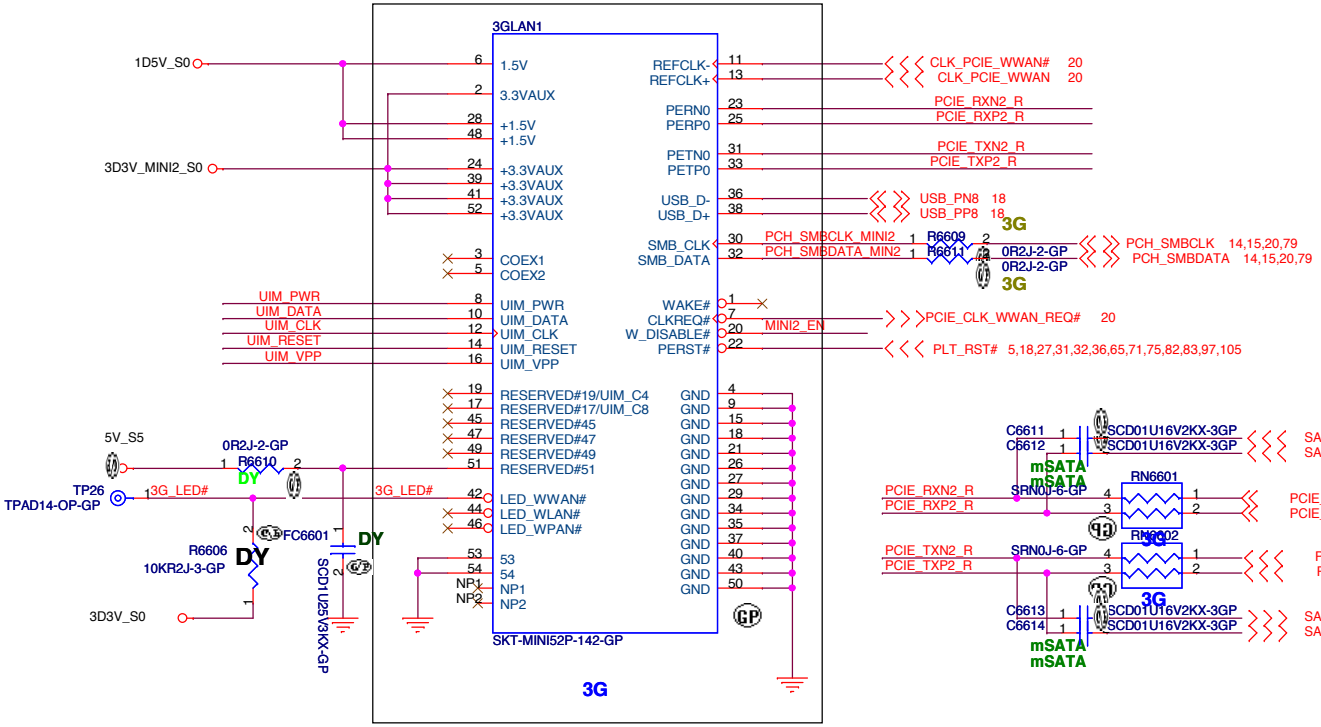
Mini Card Connector(3GLAN)

1125 SC for RF

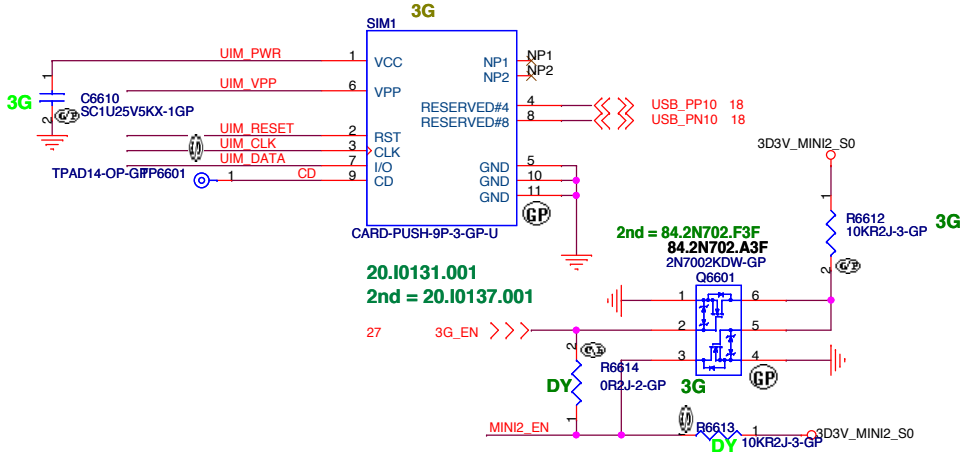


1125 SC for RF





0103 SC change to 62.10043.H61



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*3G*
Size: Custom	Document Number: BAD40_HC
Rev	1
Date: Thursday, April 12, 2012	Sheet 66 of 108

reserved

<Variant Name>

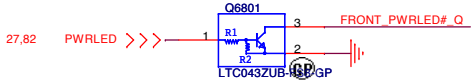
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***mSATA***

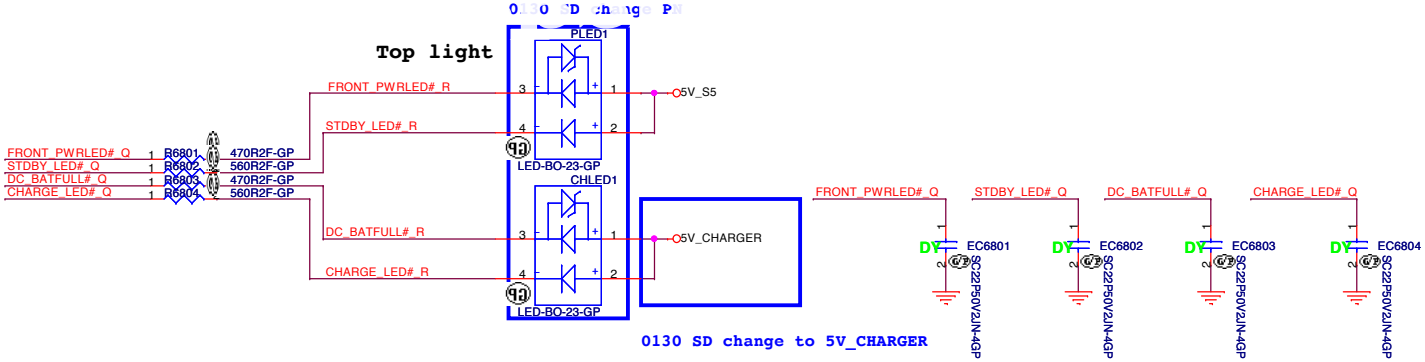
Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 67 of 108

Power button LED

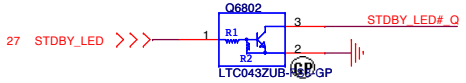


84.00043.011
2nd = 84.05143.011



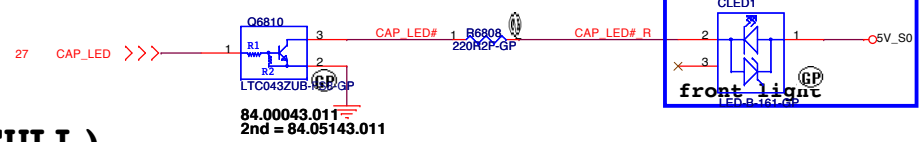
0130 SD change to 5V_CHARGER

Power STDBY_LED



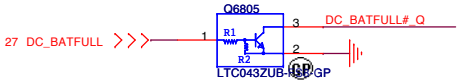
84.00043.011
2nd = 84.05143.011

Caps Lock LED



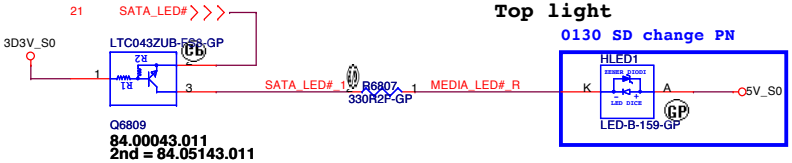
84.00043.011
2nd = 84.05143.011

Battery LED2(DC_BATFULL)



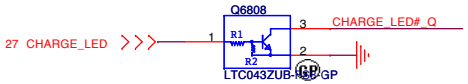
84.00043.011
2nd = 84.05143.011

SATA HDD LED



84.00043.011
2nd = 84.05143.011

Battery LED1(CHARGE)



84.00043.011
2nd = 84.05143.011

0302 -1 Del PWR BTN

1107 SC Del BXD PWR LED

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

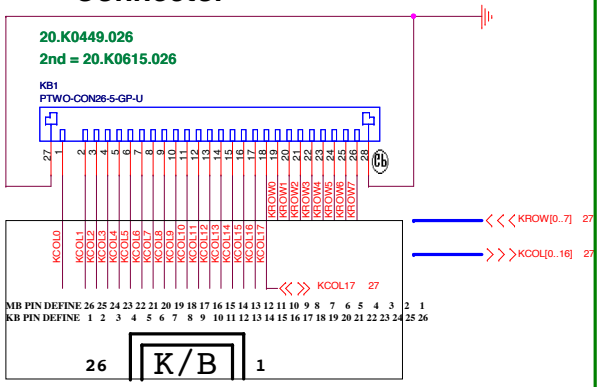
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 68 of 108

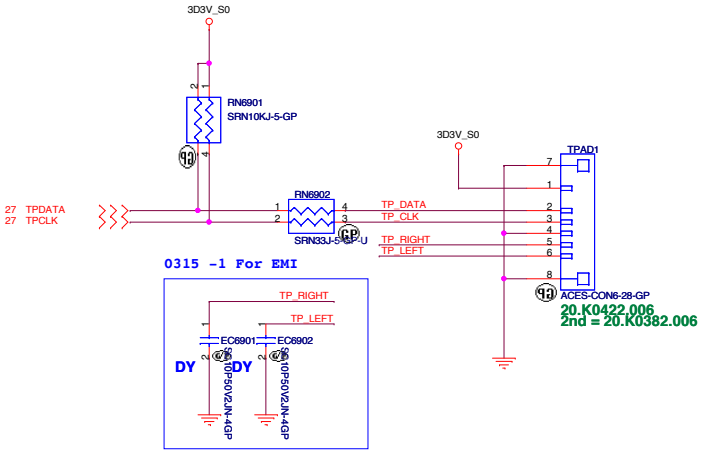
SSID = KBC

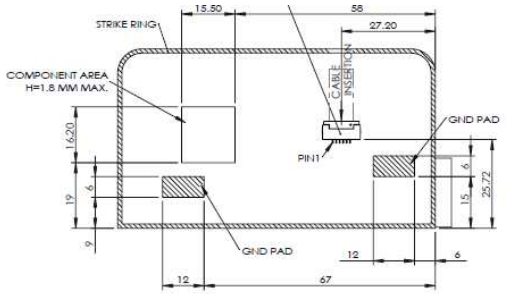
SB 0919 change PN for Layout

Internal KeyBoard Connector



TOUCH PAD 1.0 pitch



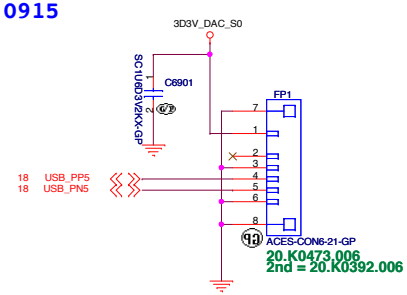


COMPONENT - BOTTOM VIEW

J1 PIN ASSIGNMENT:
PIN1 : TP_L
PIN2 : TP_R
PIN3 : GND
PIN4 : PS2_CLK
PIN5 : PS2_DAT
PIN6 : VDD

Finger Printer 0.5 pitch

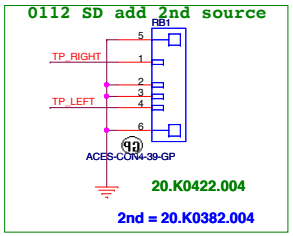
SB 0915



Pin No.	Define
1	ESD ground
2	USB D- Signal
3	USB D+ Signal
4	GND
5	NC
6	3.3V Power pin

Rubber Dome 1.0 pitch

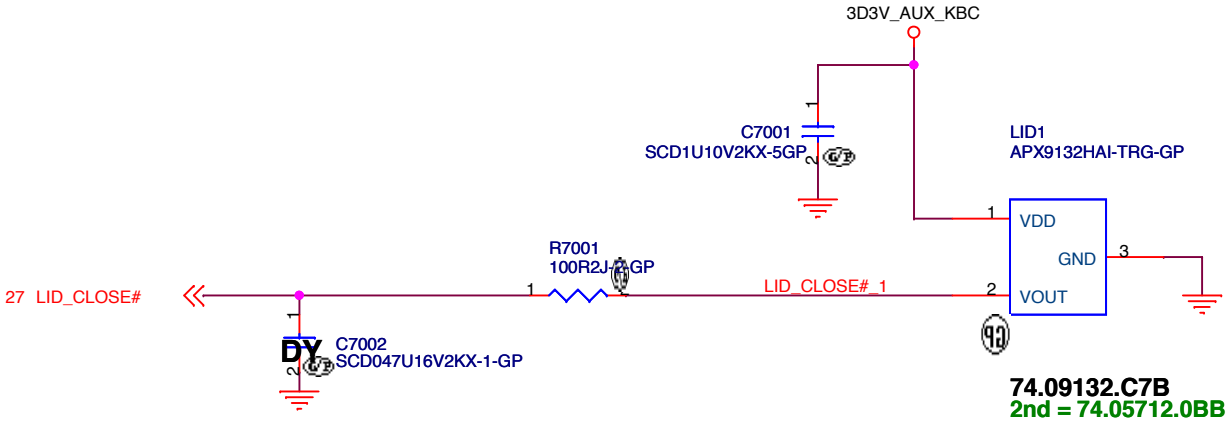
0909 SB
0112 SD add 2nd source



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 69 of 108



<Variant Name>

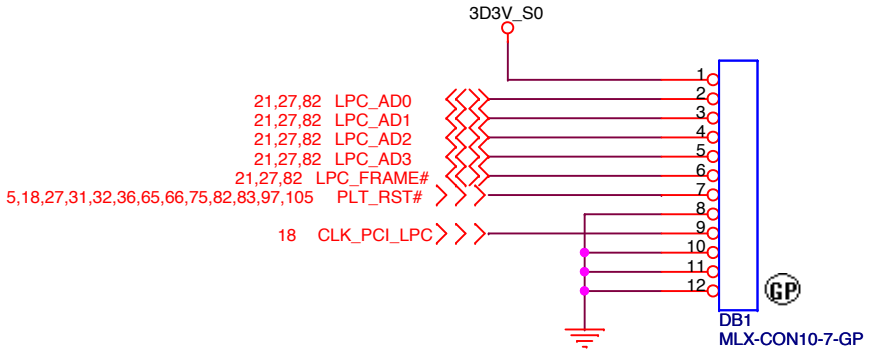
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 70 of 108

SB modify to test pad



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 71 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BAD40_HC	1

(Blanking)

<Variant Name>

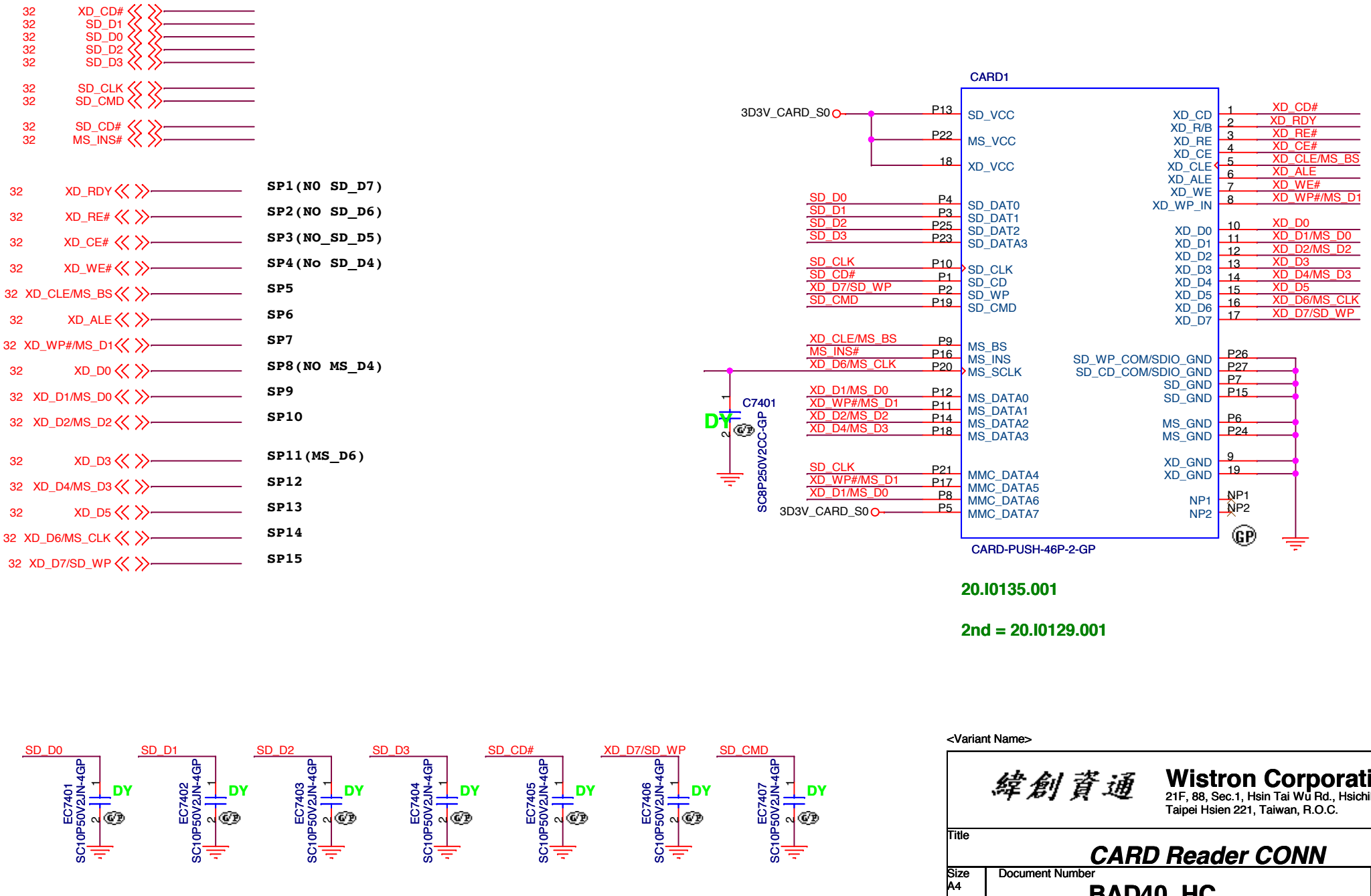
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	BAD40_HC	1

SD/XD/MS Card Reader

SSID = SDIO



20.I0135.001

2nd = 20.I0129.001

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

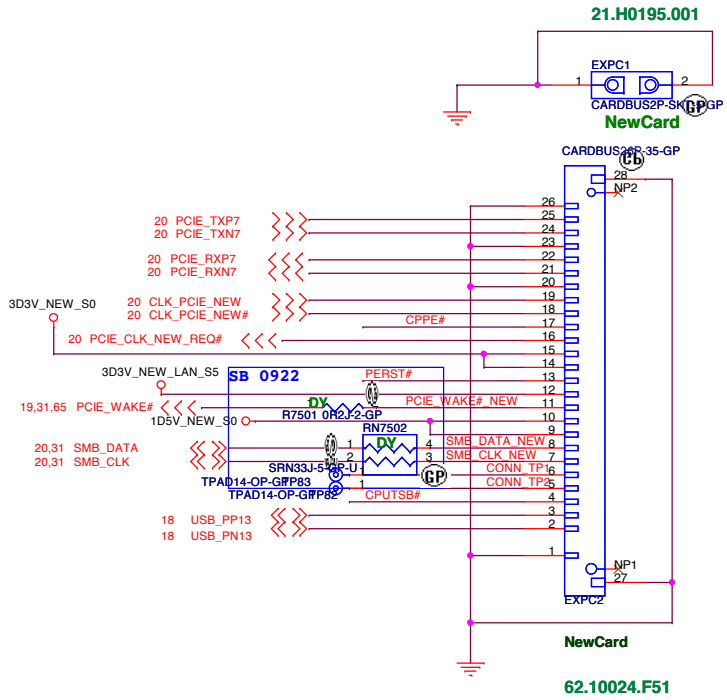
Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	BAD40_HC	1

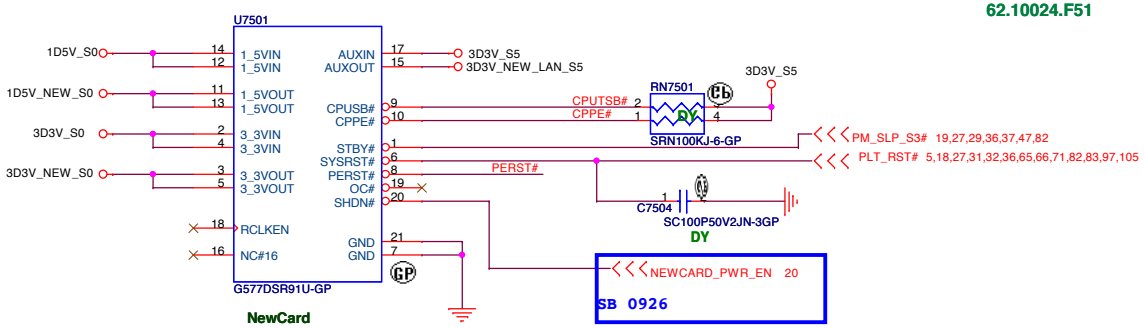
Date: Thursday, April 12, 2012 Sheet 74 of 108

SSID = ExpressCard

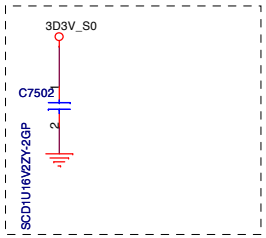
DIP階 For Expresscard socket



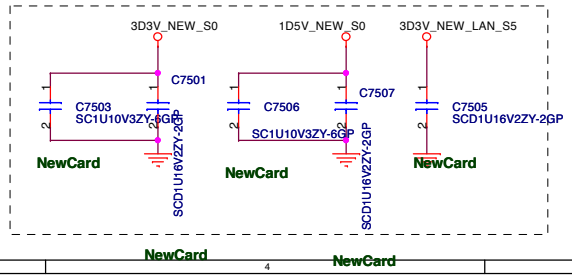
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



Place them Near to Chip



Place them Near to Connector



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 75 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 76 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 77 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

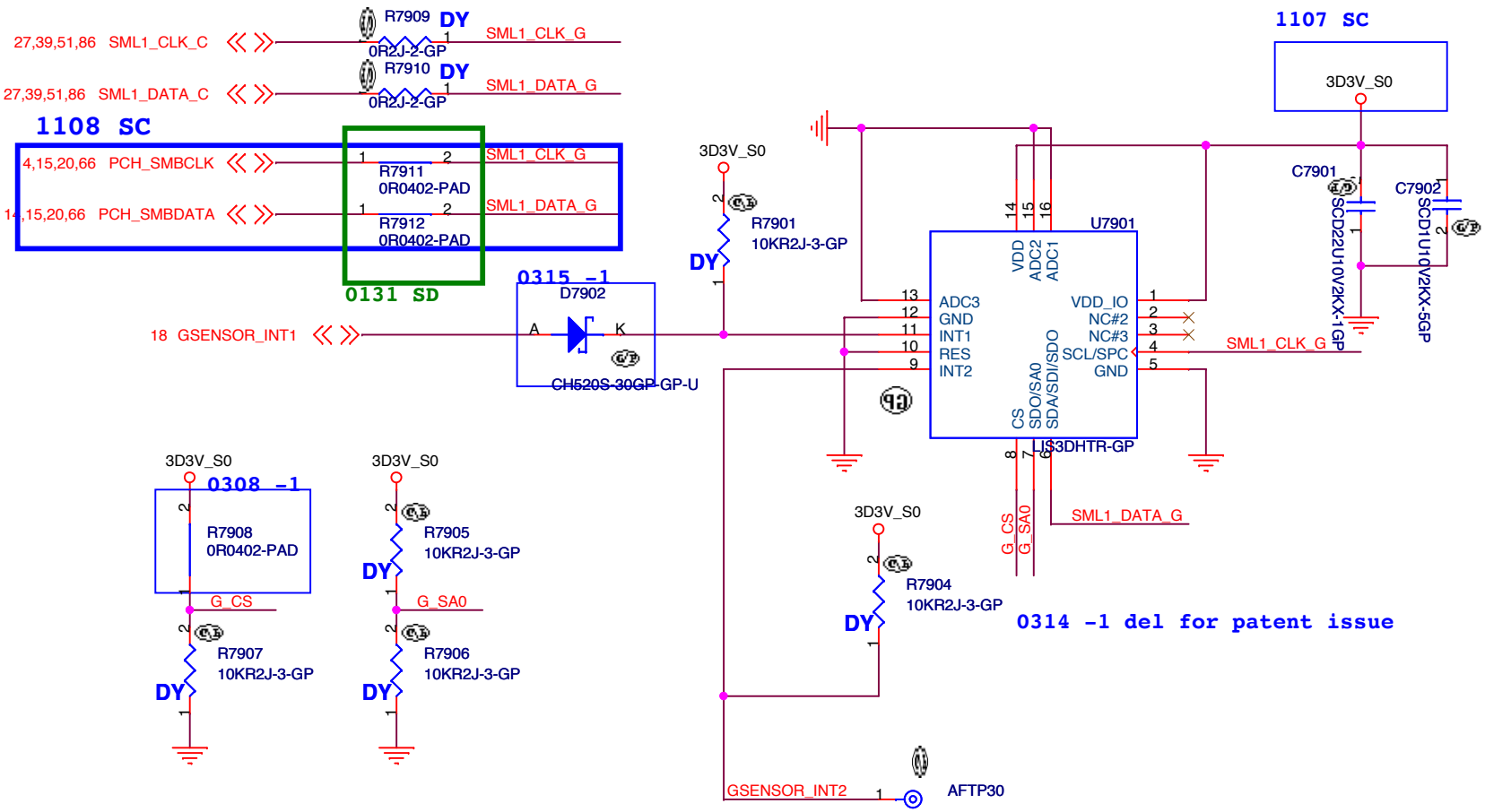
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 78 of 108

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
A4	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 79 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 80 of 108

<Variant Name>

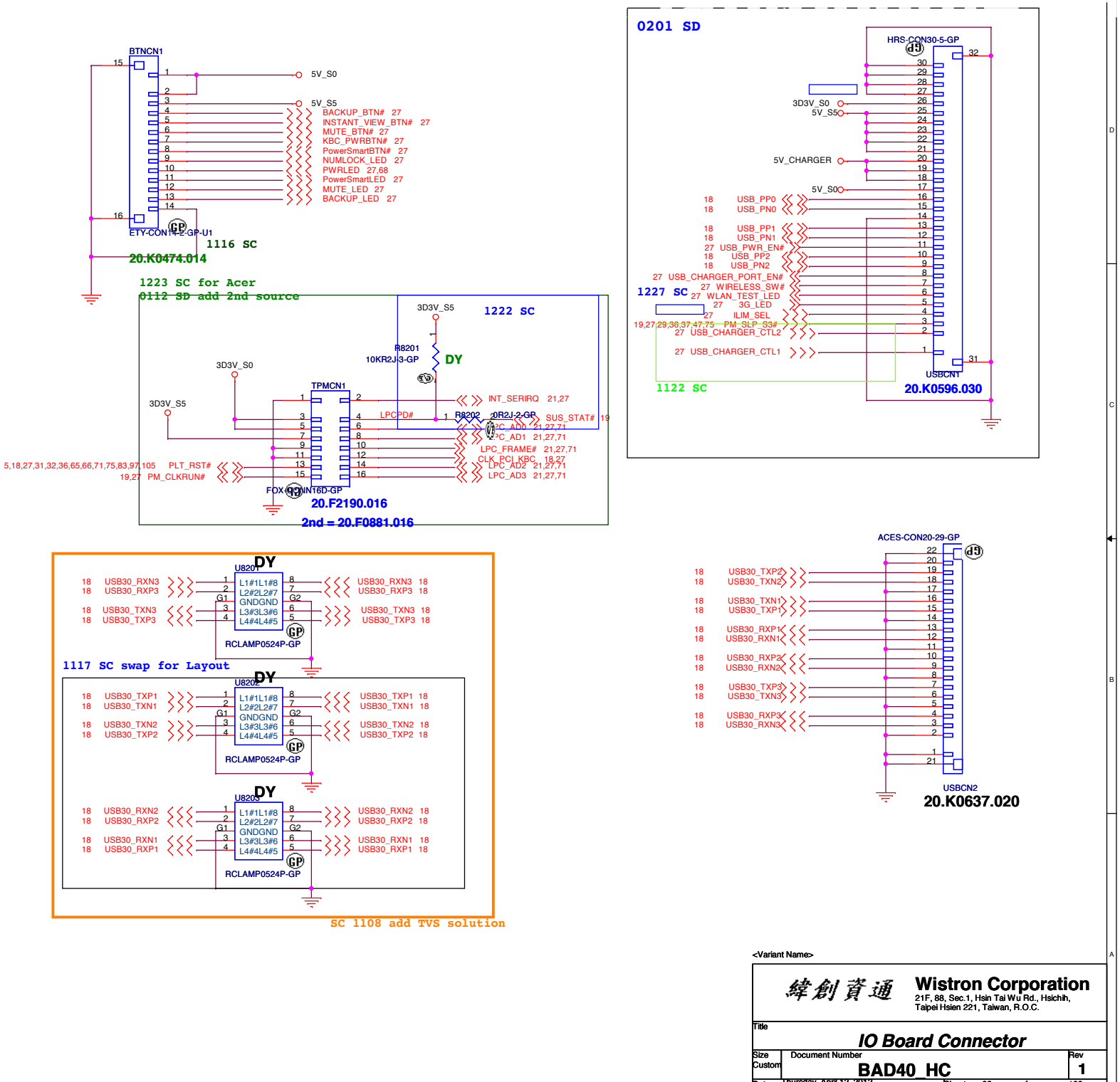
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

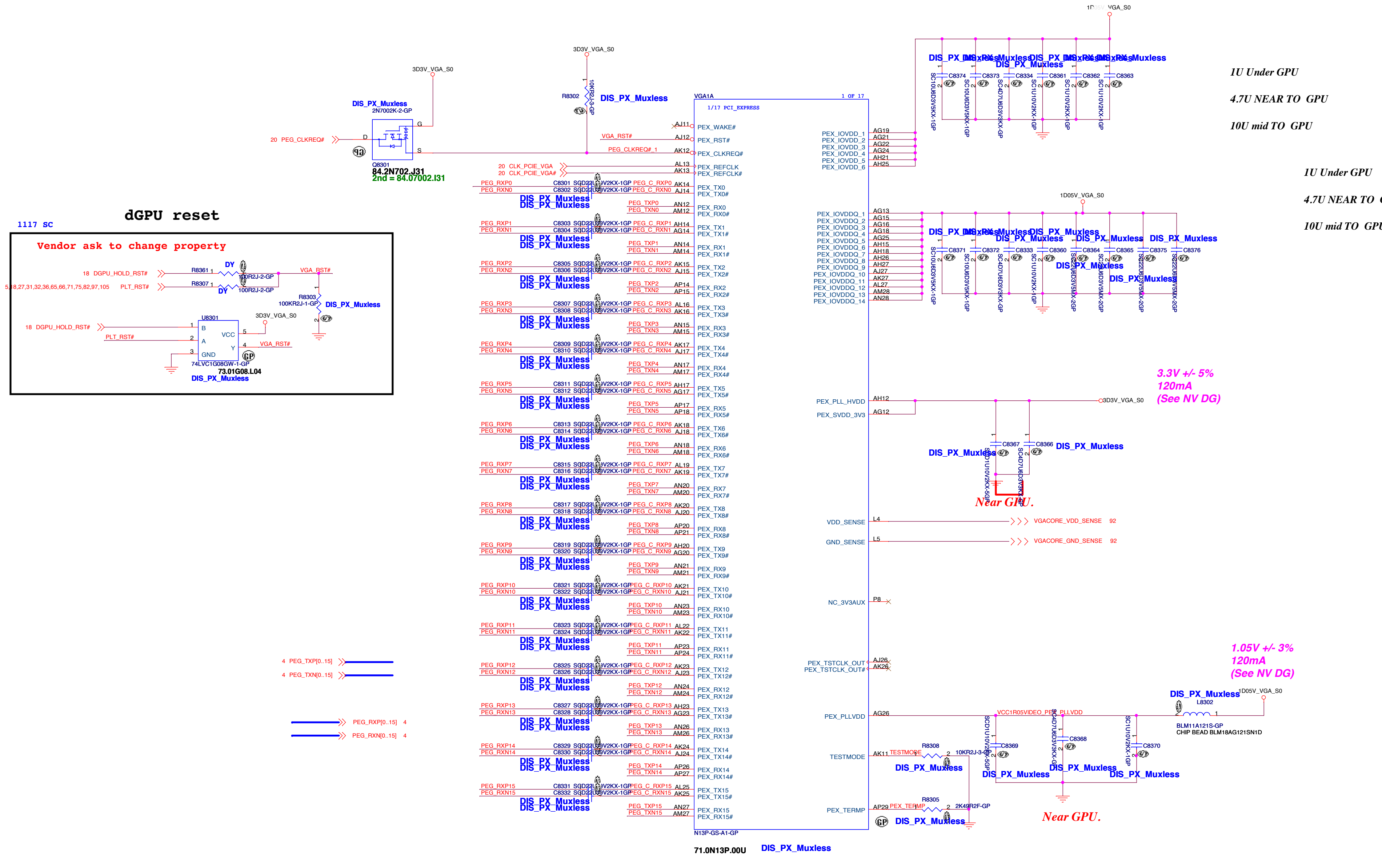
Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 81 of 108



<Variant Name>

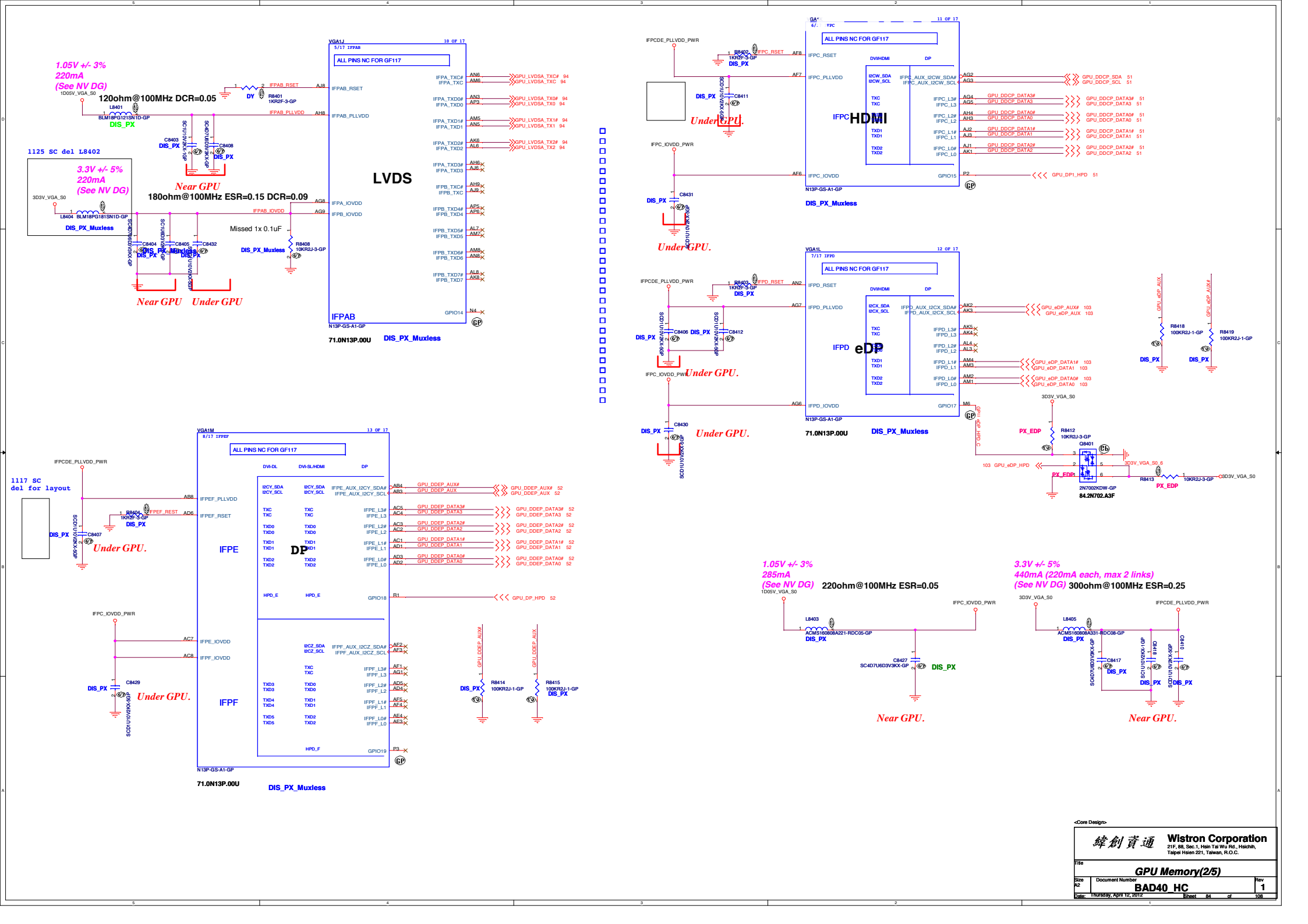
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *IO Board Connector*		
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 82 of 108	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_PCIE/STRAPPING(1/5)	
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 83 of 108	



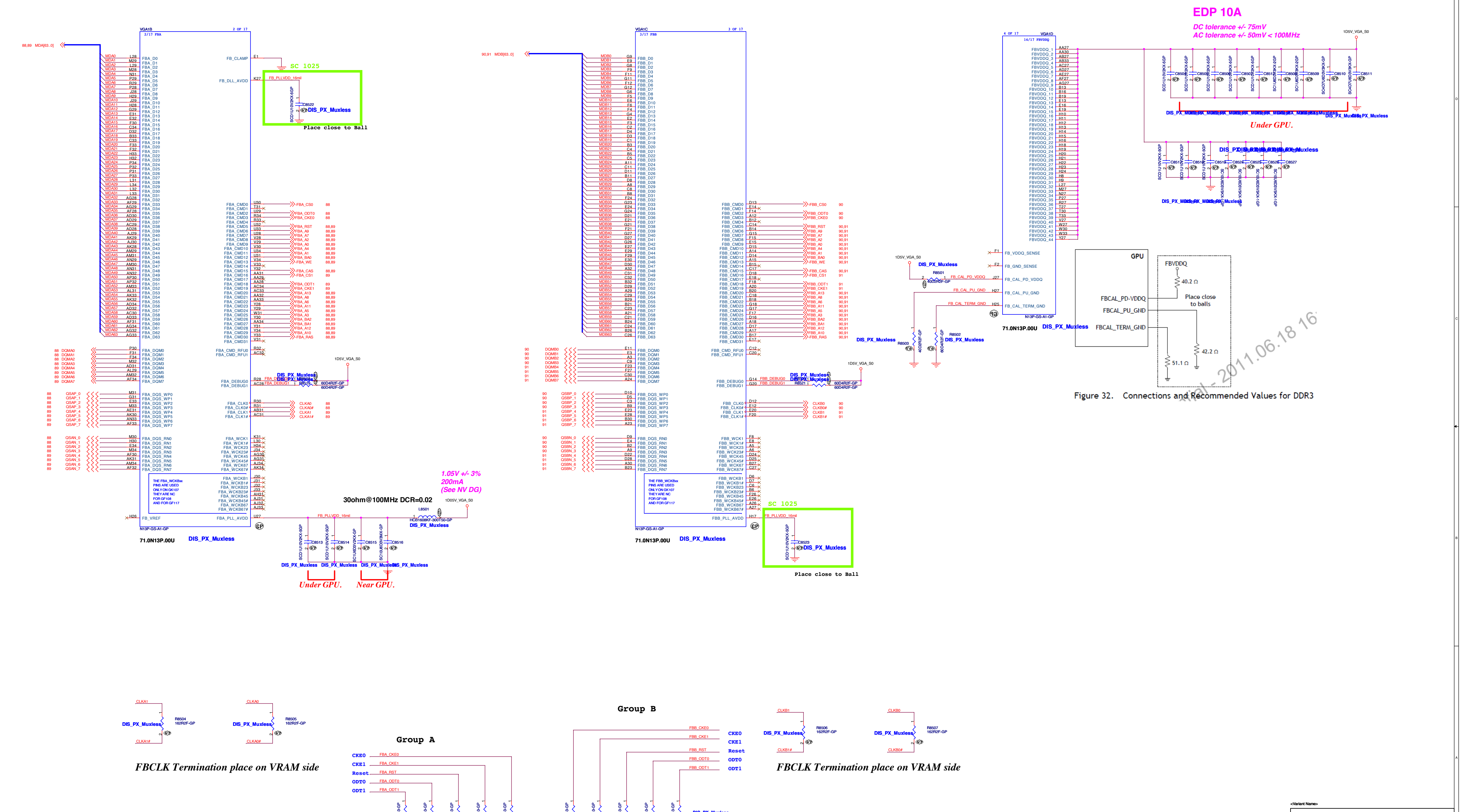
<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 84 of 108

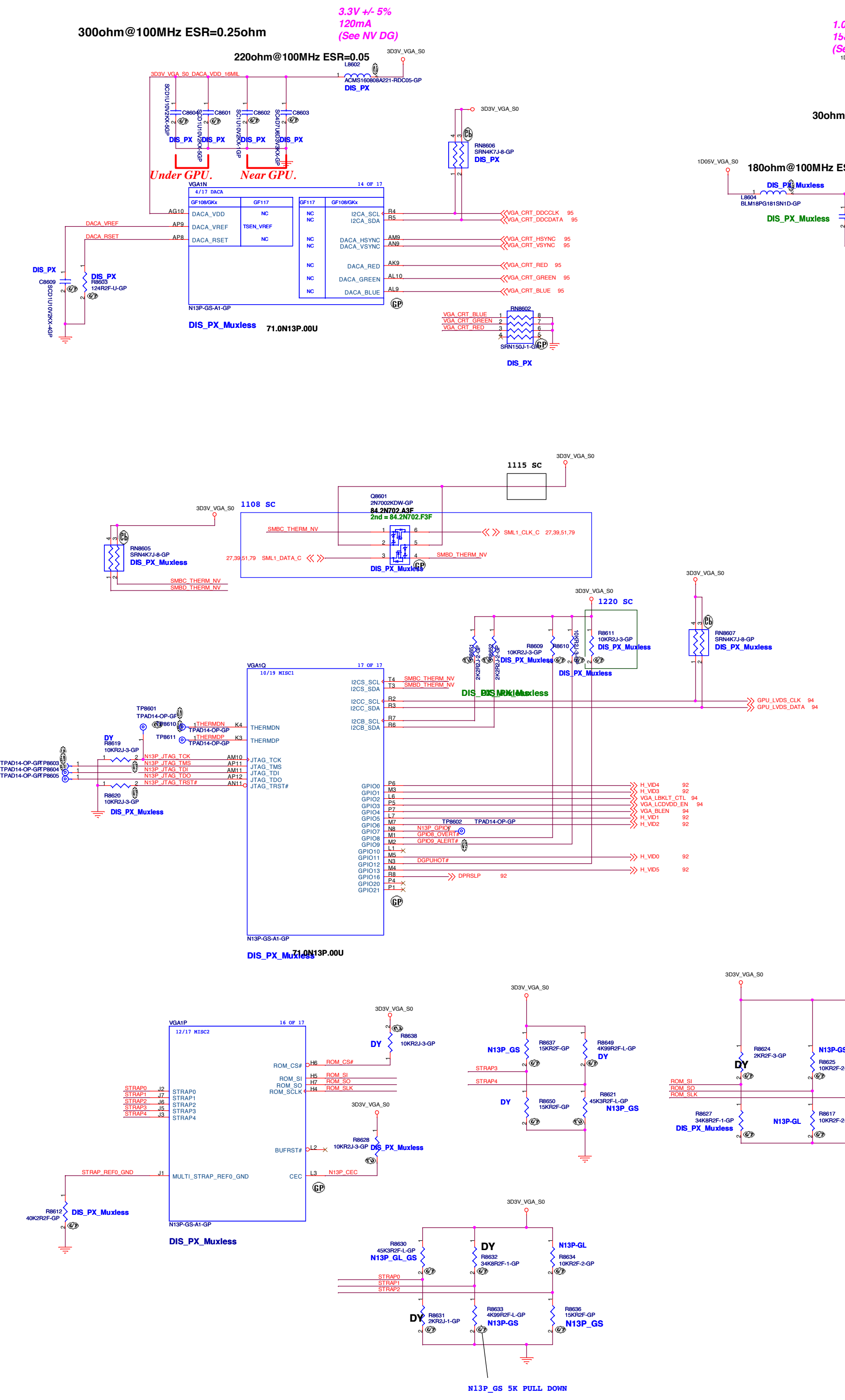


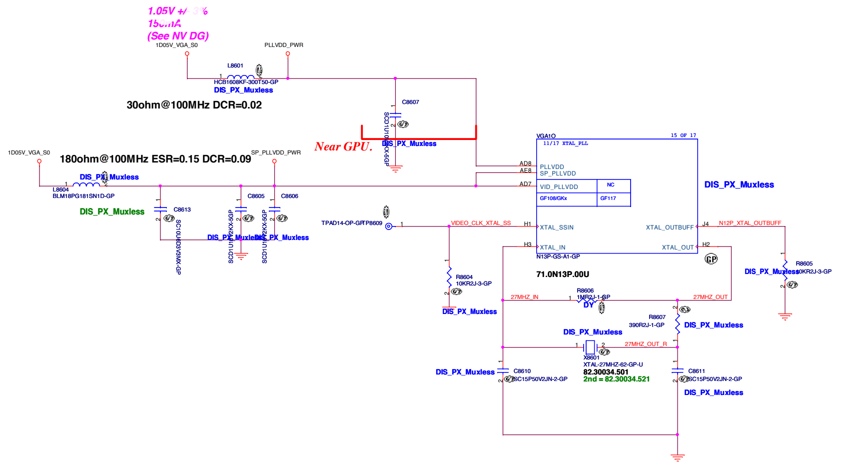
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 85 of 108





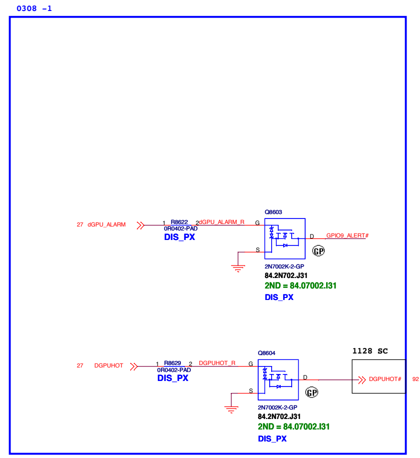


Table 15.3 Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD	Pull-down to GND
5k	1000	0000
10k	1001	0001
15k	1010	0010
20k	1011	0011
25k	1100	0100
30k	1101	0101
35k	1110	0110
45k	1111	0111

25Kohm	5Kohm	10Kohm	30Kohm
64.24925.6DL	64.49915.6DL	64.10025.6DL	64.30025.6DL

NVIDIA TABLE

	Hynix 2G 0110 128M*16*8 900MHZ	Hynix 1G 0010 64M*16*8 900MHZ	Samsung 1G 0011 64M*16*8 900MHZ	Samsung 2G 0111 128M*16*8 900MHZ
ROM_SI	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

Table 111. Display Link to SORx_EXPOSED Bit Mapping

Displays		DVI/HDMI/DP	LVDS	eDP	Not in Use
Dual Link Mode	IFPA/B		SOR0_EXPOSED = 0		SOR0_EXPOSED = 0
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE/F	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
Split Mode	IFPA/B				
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
	IFPF	SOR0_EXPOSED = 1			SOR0_EXPOSED = 0

Strap3

	DEVID	ROM-SCLK		strap2	
N13P-GL-A1	0x0DE9	0010	PD 15K	1001	PU 10K
N13P-GS-ES-A1	0x0FDB	1000	PU 4.99K	1011	PU 20K
N13P-GS-A1	0x0FD2	1000	PU 4.99K	0010	PD 15K

For N13P-GS-A1 0x0FD2

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_M	
	1	0	0	0	5K ohm pull-up
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
Hynix 2G	0	1	1	0	35K ohm pull-down
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
	1	0	0	1	10K ohm pull-up
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	0	0	0	5K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	0	0	1	0	15K ohm pull-down
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
	1	0	1	0	15K ohm pull-up
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	
	0	1	1	1	45K ohm pull-down

Table 15.8 User Straps

User[3:0]	Type	Resolution	Sync	Notes
0000	XGA	1024 x 768	-/-	
0001	XGA	1024 x 768	+/+	
0010	SXGA	1280 x 1024	-/-	
0011	SXGA+	1400 x 1050	-/-	
0100	UXGA	1600 x 1200	+/+	
0101	QXGA	2048 x 1536	+/+	Reduced Blanking
0110	SXGA+	1400 x 1050	-/-	
0111	SVGA	800 x 600	+/+	
1000 - 1100	-	-	-	Customer defined (Default)
1111	-	-	-	EDID is used

Strap0

EDP 50A
(TDP 37W)

VGA_CORE

Under GPU

DIS_PX_Muxless

C8704 C8703 C8702 C8701

SC4D7U6D3V9KX-GP

Under GPU

DIS_PX_Muxless

C8712 C8711 C8708 C8707 C8706 C8705

SC4D7U6D3V9KX-GP

CLOSE TO GPU

DIS_PX_Muxless

C8720 C8719 C8718 C8717

SC1U10V2KX-4GP

NEAR TO GPU

DIS_PX_Muxless

C8731 C8730 C8729 C8728 C8727

SC10U6D3V3MX-GP

DIS_PX_Muxless

C8732 C8733 C8734 C8752

SC10U6D3V3MX-GP

VGA1F 6 OF 17

13/17 NVVDD

AA12	VDD_1	VDD_73	AA13
AA14	VDD_2	VDD_74	AA15
AA16	VDD_3	VDD_75	AA17
AA19	VDD_4	VDD_76	AA18
AA21	VDD_5	VDD_77	AA20
AA23	VDD_6	VDD_78	AA22
AB13	VDD_7	VDD_79	AA24
AB15	VDD_8	VDD_80	AB12
AB17	VDD_9	VDD_81	AB14
AB18	VDD_10	VDD_82	AB16
AB20	VDD_11	VDD_83	AB19
AB22	VDD_12	VDD_84	AB21
AC12	VDD_13	VDD_85	AB24
AC14	VDD_14	VDD_86	AC13
AC16	VDD_15	VDD_87	AC15
AC19	VDD_16	VDD_88	AC17
AC21	VDD_17	VDD_89	AC18
AC23	VDD_18	VDD_90	AC20
M12	VDD_19	VDD_91	AC22
M14	VDD_20	VDD_92	AC24
M16	VDD_21	VDD_93	AD23
M19	VDD_22	VDD_94	AE24
M21	VDD_23	VDD_95	AF23
M23	VDD_24	VDD_96	AF24
N13	VDD_25	VDD_97	AG23
N15	VDD_26	VDD_98	AG24
N17	VDD_27	VDD_99	AH23
N18	VDD_28	VDD_100	AH24
N20	VDD_29	VDD_101	AJ23
N22	VDD_30	VDD_102	AJ24
P12	VDD_31	VDD_103	AK23
P14	VDD_32	VDD_104	AK24
P16	VDD_33	VDD_105	AL23
P19	VDD_34	VDD_106	AL24
P21	VDD_35	VDD_107	AM23
P23	VDD_36	VDD_108	AM24
R13	VDD_37	VDD_109	
R15	VDD_38	VDD_110	
R17	VDD_39	VDD_111	
R18	VDD_40	VDD_112	
R20	VDD_41	VDD_113	
R22	VDD_42	VDD_114	
T12	VDD_43	VDD_115	
T14	VDD_44	VDD_116	
T16	VDD_45	VDD_117	
T19	VDD_46	VDD_118	
T21	VDD_47	VDD_119	
T23	VDD_48	VDD_120	
U13	VDD_49	VDD_121	
U15	VDD_50	VDD_122	
U17	VDD_51	VDD_123	
U18	VDD_52	VDD_124	
U20	VDD_53	VDD_125	
U22	VDD_54	VDD_126	
V13	VDD_55	VDD_127	
V15	VDD_56	VDD_128	
V17	VDD_57	VDD_129	
V18	VDD_58	VDD_130	
V20	VDD_59	VDD_131	
V22	VDD_60	VDD_132	
W12	VDD_61	VDD_133	
W14	VDD_62	VDD_134	
W16	VDD_63	VDD_135	
W19	VDD_64	VDD_136	
W21	VDD_65	VDD_137	
W23	VDD_66	VDD_138	
Y13	VDD_67	VDD_139	
Y15	VDD_68	VDD_140	
Y17	VDD_69		
Y18	VDD_70		
Y20	VDD_71		
Y22	VDD_72		

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

VGA1G 7 OF 17

17/17 NC/VDD33

AC6	NC#AC6	VDD33_1	J8
AJ28	NC#AJ28	VDD33_2	K8
AJ4	NC#AJ4	VDD33_3	L8
AJ5	NC#AJ5	VDD33_4	M8
AL11	NC#AL11		
C15	NC#C15		
D19	NC#D19		
D20	NC#D20		
D23	NC#D23		
D26	NC#D26		
H31	NC#H31		
T8	NC#T8		
V32	NC#V32		

N13P-GS-A1-GP

DIS_PX_Muxless

71.0N13P.00U

3D3V_VGA_S0

C8710 C8735 C8739 C8740

SC1U6D3V2KX-GP

SC4D7U6D3V9KX-GP

DIS_PX_Muxless

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

VGA1E 5 OF 17

9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1	U1	XVDD_17	W2
XVDD_2	U2	XVDD_18	W3
XVDD_3	U3	XVDD_19	W4
XVDD_4	U4	XVDD_20	W5
XVDD_5	U5	XVDD_21	W7
XVDD_6	U6	XVDD_22	W8
XVDD_7	U7	XVDD_23	Y1
XVDD_8	U8	XVDD_24	Y2
XVDD_9	V1	XVDD_25	Y3
XVDD_10	V2	XVDD_26	Y4
XVDD_11	V3	XVDD_27	Y5
XVDD_12	V4	XVDD_28	Y6
XVDD_13	V5	XVDD_29	Y7
XVDD_14	V6	XVDD_30	Y8
XVDD_15	V7	XVDD_31	AA1
XVDD_16	V8	XVDD_32	AA2
		XVDD_33	AA3
		XVDD_34	AA4
		XVDD_35	AA5
		XVDD_36	AA6
		XVDD_37	AA7
		XVDD_38	AA8

N13P-GS-A1-GP

DIS_PX_Muxless

71.0N13P.00U

VGA1 8 OF 17

16/17 GND_2/2

A2	GND_1	GND_71	AM25
AA17	GND_5	GND_72	AN1
AA18	GND_6	GND_73	AN10
AA20	GND_7	GND_74	AN13
AA22	GND_8	GND_75	AN16
AB12	GND_9	GND_76	AN19
AB14	GND_10	GND_77	AN22
AB16	GND_11	GND_78	AN25
AB19	GND_12	GND_79	AN30
AB2	GND_13	GND_80	AN34
AB21	GND_14	GND_81	AN4
A33	GND_2	GND_82	AN7
AB23	GND_15	GND_83	AP2
AB28	GND_16	GND_84	AP33
AB30	GND_17	GND_85	B1
AB32	GND_18	GND_86	B10
AB5	GND_19	GND_87	B22
AB7	GND_20	GND_88	B25
AC13	GND_21	GND_89	B28
AC15	GND_22	GND_90	B31
AC17	GND_23	GND_91	B34
AC18	GND_24	GND_92	B4
AA13	GND_3	GND_93	B7
AC20	GND_25	GND_94	C10
AC22	GND_26	GND_95	C13
AE2	GND_27	GND_96	C19
AE28	GND_28	GND_97	C22
AE30	GND_29	GND_98	C25
AE32	GND_30	GND_99	C28
AE33	GND_31	GND_100	C7
AE5	GND_32	GND_101	D2
AE7	GND_33	GND_102	D31
AH10	GND_34	GND_103	D33
AA15	GND_4	GND_104	E10
AH13	GND_35	GND_105	E22
AH16	GND_36	GND_106	E25
AH19	GND_37	GND_107	E5
AH2	GND_38	GND_108	E7
AH22	GND_39	GND_109	F28
AH24	GND_40	GND_110	F7
AH28	GND_41	GND_111	G10
AH29	GND_42	GND_112	G13
AH30	GND_43	GND_113	G16
AH32	GND_44	GND_114	G19
AH33	GND_45	GND_115	G2
AH5	GND_46	GND_116	G22
AH7	GND_47	GND_117	G25
AJ7	GND_48	GND_118	G28
AK10	GND_49	GND_119	G3
AK7	GND_50	GND_120	G30
AL12	GND_51	GND_121	G32
AL14	GND_52	GND_122	G33
AL15	GND_53	GND_123	G5
AL17	GND_54	GND_124	G7
AL18	GND_55	GND_125	K2
AL2	GND_56	GND_126	K28
AL20	GND_57	GND_127	K30
AL21	GND_58	GND_128	K32
AL23	GND_59	GND_129	K33
AL24	GND_60	GND_130	K5
AL26	GND_61	GND_131	K7
AL28	GND_62	GND_132	M13
AL30	GND_63	GND_133	M15
AL32	GND_64	GND_134	M17
AL33	GND_65	GND_135	M18
AL5	GND_66	GND_136	M20
AM13	GND_67	GND_137	M22
AM16	GND_68	GND_138	N12
AM19	GND_69	GND_139	N14
AM22	GND_70	GND_140	N16

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

VGA1H 8 OF 17

16/17 GND_2/2

N19	GND_141	GND_170	T28
N2	GND_142	GND_171	T32
N21	GND_143	GND_172	T5
N23	GND_144	GND_173	T7
N28	GND_145	GND_174	U12
N30	GND_146	GND_175	U14
N32	GND_147	GND_176	U16
N33	GND_148	GND_177	U19
N5	GND_149	GND_178	U21
N7	GND_150	GND_179	U23
P13	GND_151	GND_180	V12
P15	GND_152	GND_181	V14
P17	GND_153	GND_182	V16
P18	GND_154	GND_183	V19
P20	GND_155	GND_184	V21
P22	GND_156	GND_185	V23
R12	GND_157	GND_186	W13
R14	GND_158	GND_187	W15
R16	GND_159	GND_188	W17
R19	GND_160	GND_189	W18
R21	GND_161	GND_190	W20
R23	GND_162	GND_191	W22
T13	GND_163	GND_192	W28
T15	GND_164	GND_193	Y12
T17	GND_165	GND_194	Y14
T18	GND_166	GND_195	Y16
T2	GND_167	GND_196	Y19
T20	GND_168	GND_197	Y21
T22	GND_169	GND_198	Y23
AG11	GND_F	GND_H	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

Optional GND GNDs (2)
NC for 4-Ly cards

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

<Core Design>

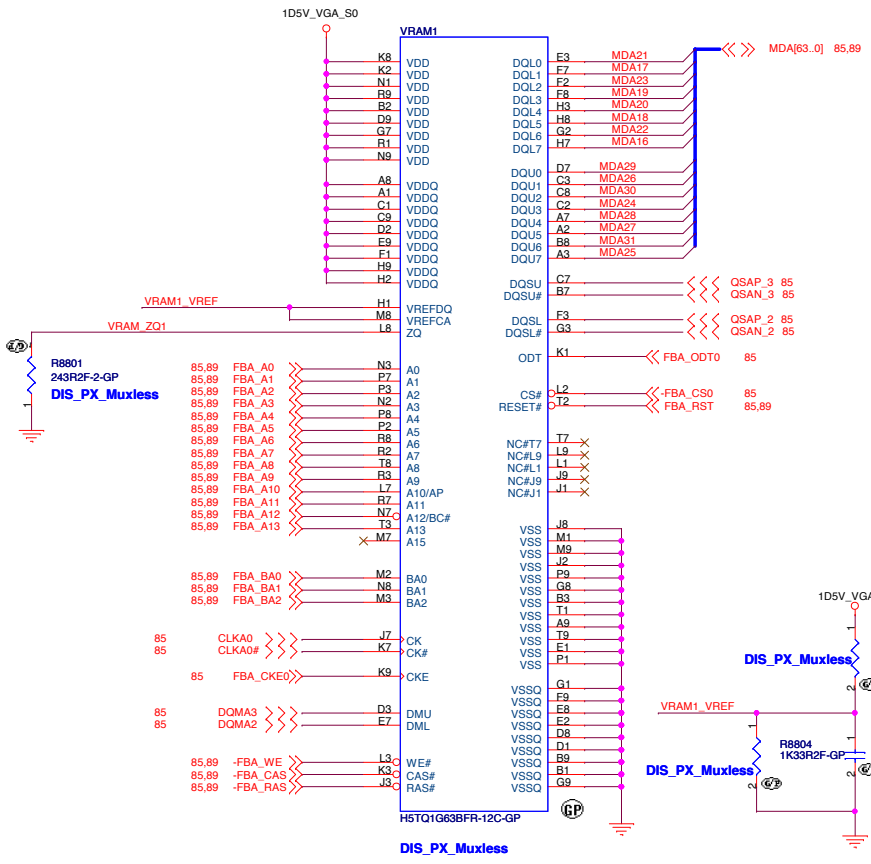
緯創資通 **Wistron Corporation**

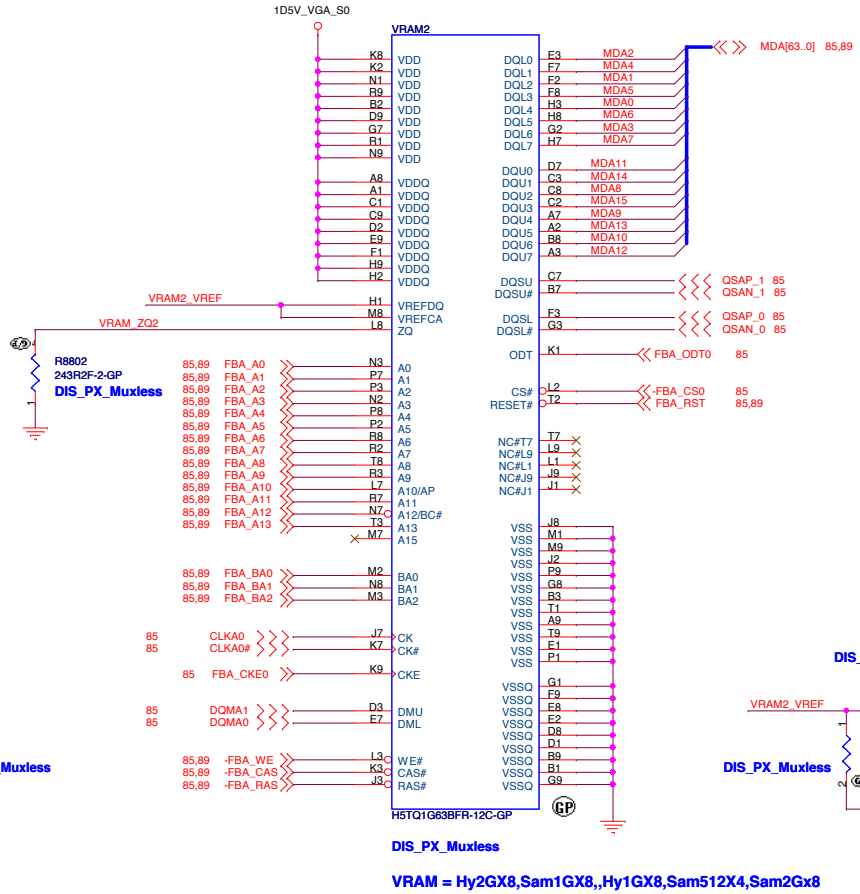
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU_DPPWR/GND(5/5)*

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 87 of 108





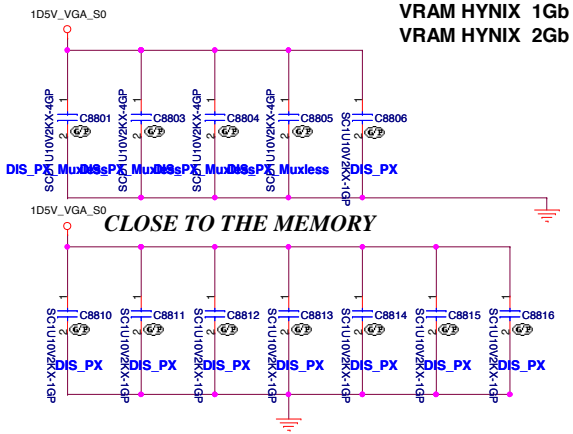
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

FB CMD mapping Mode D-N12x

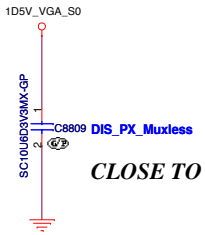
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

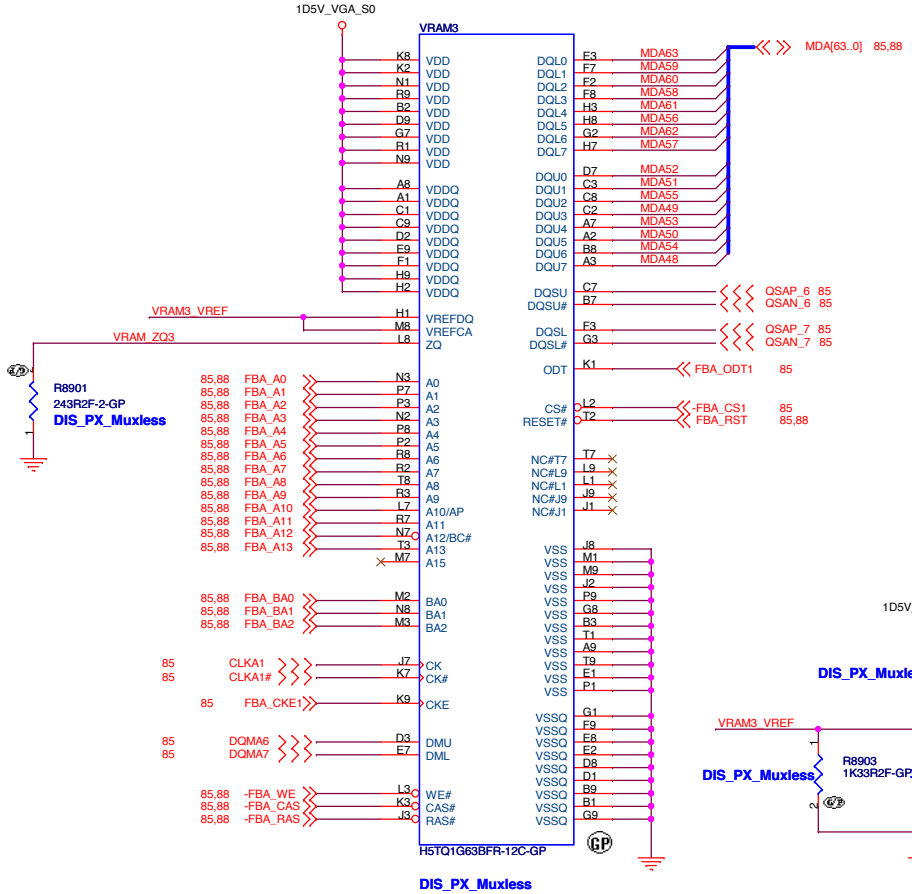
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

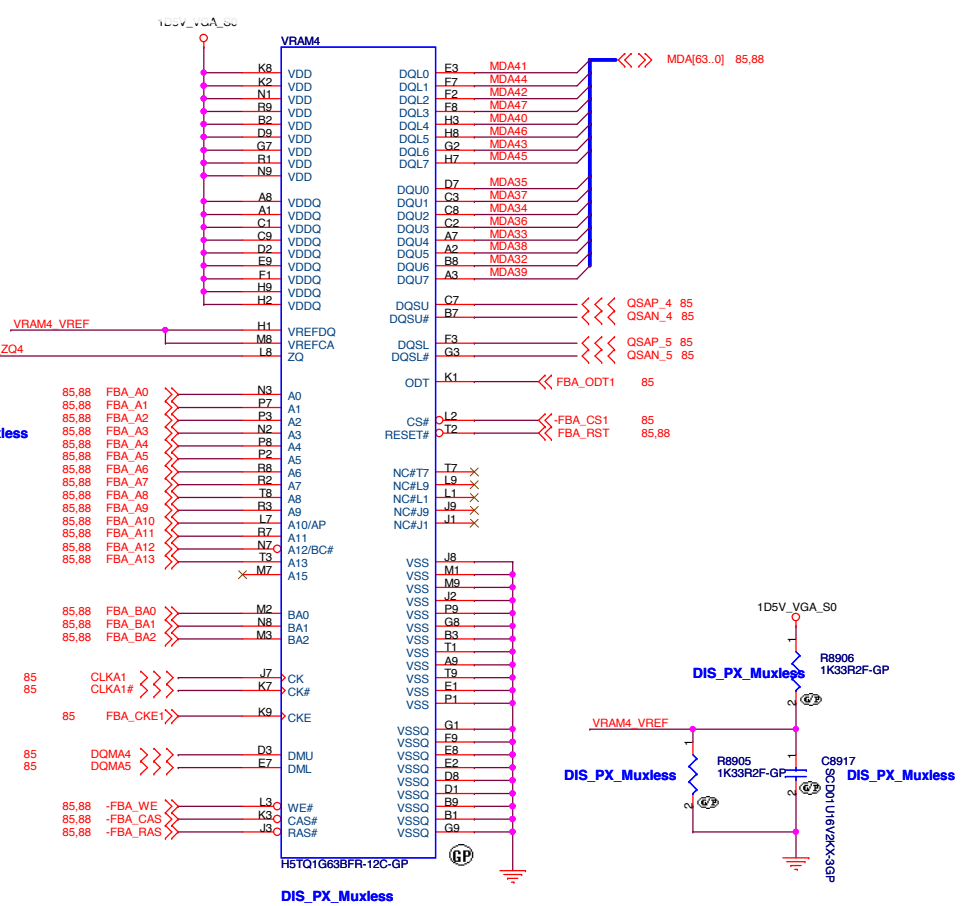
Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	**BAD40_HC**	**1**

Date: Thursday, April 12, 2012 Sheet 88 of 108



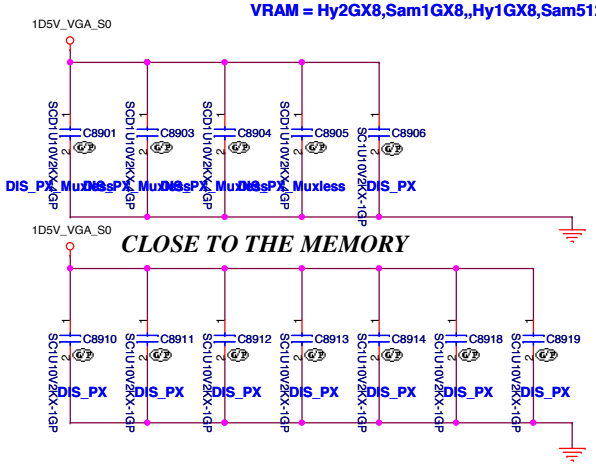
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8



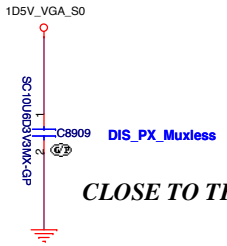
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY

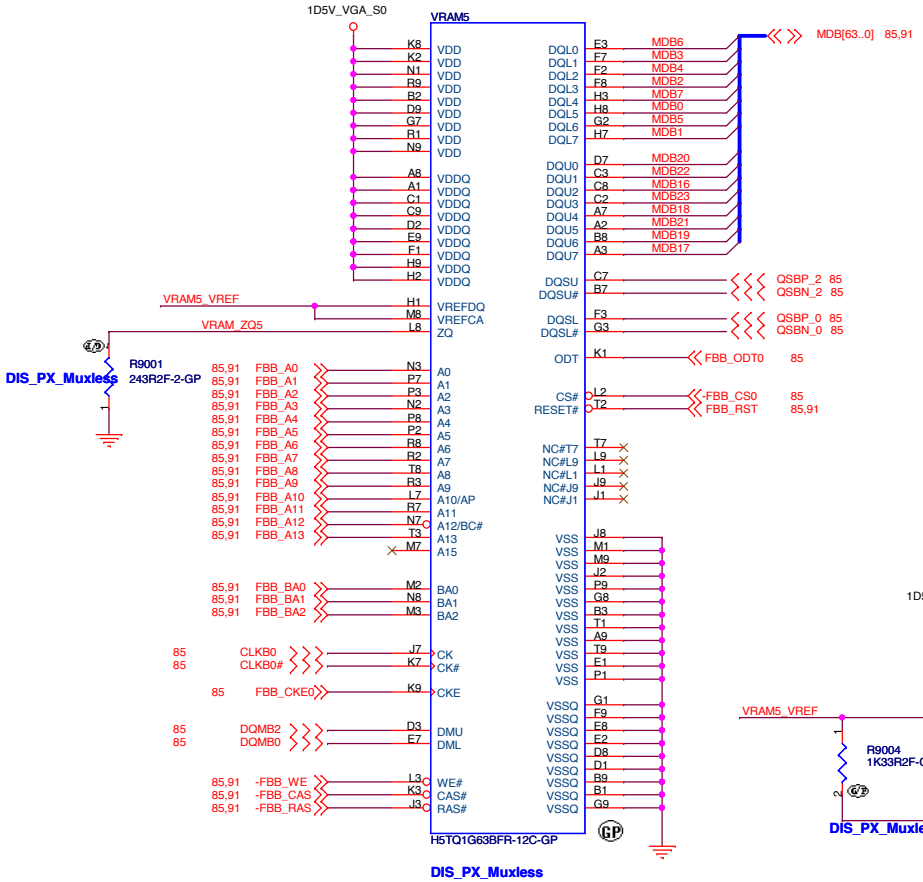


CLOSE TO THE MEMORY

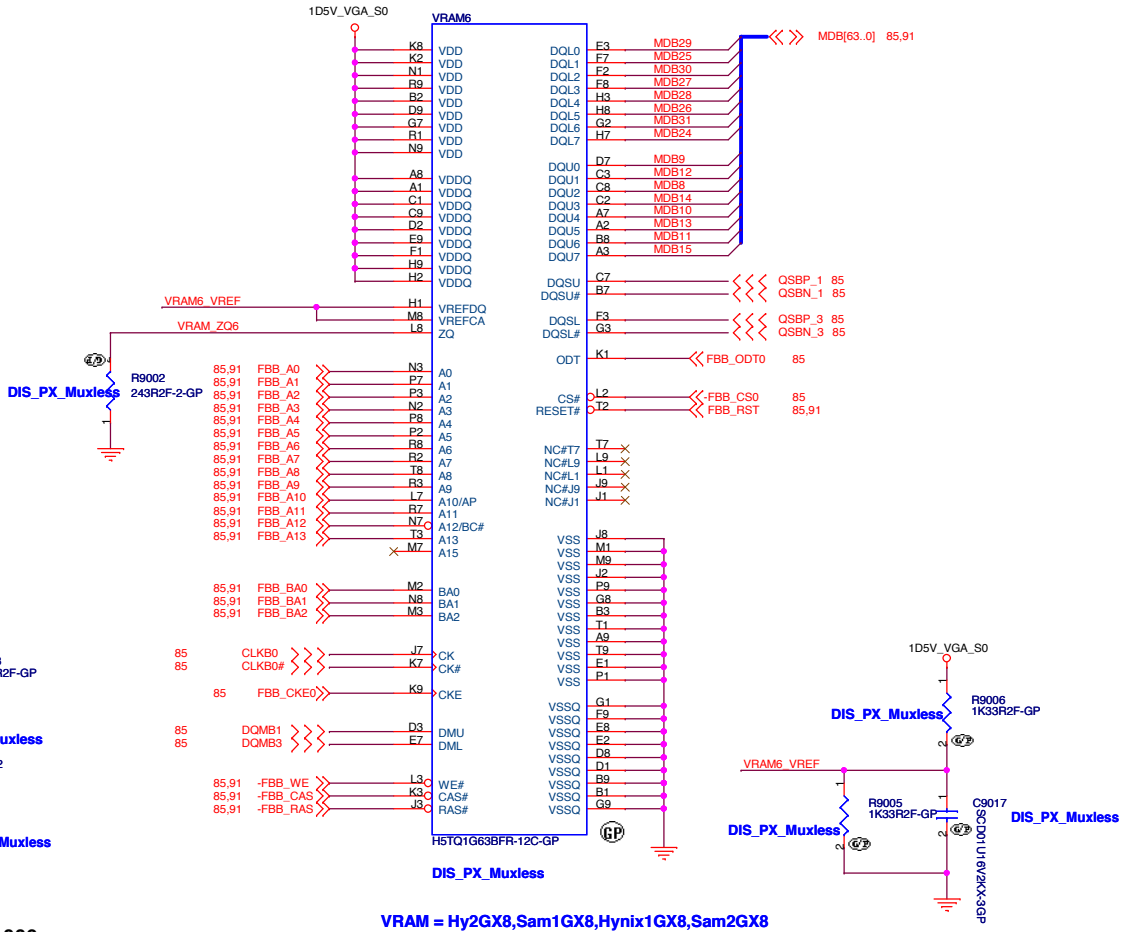
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***GPU-VRAM3,4 (2/4)***	
Size: Custom	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 89 of 108	

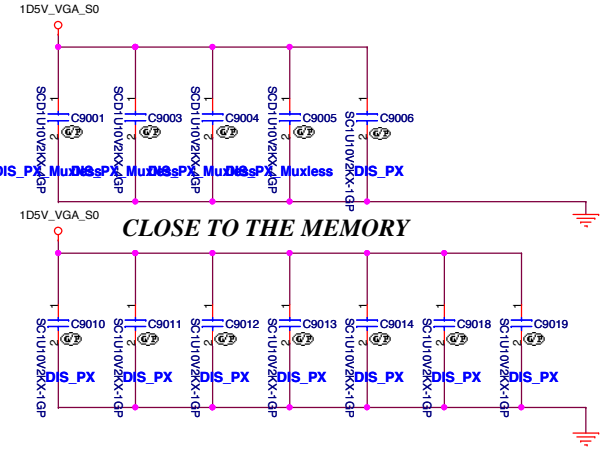


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8



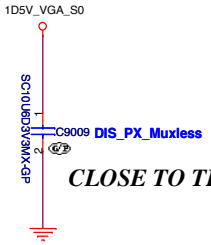
VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

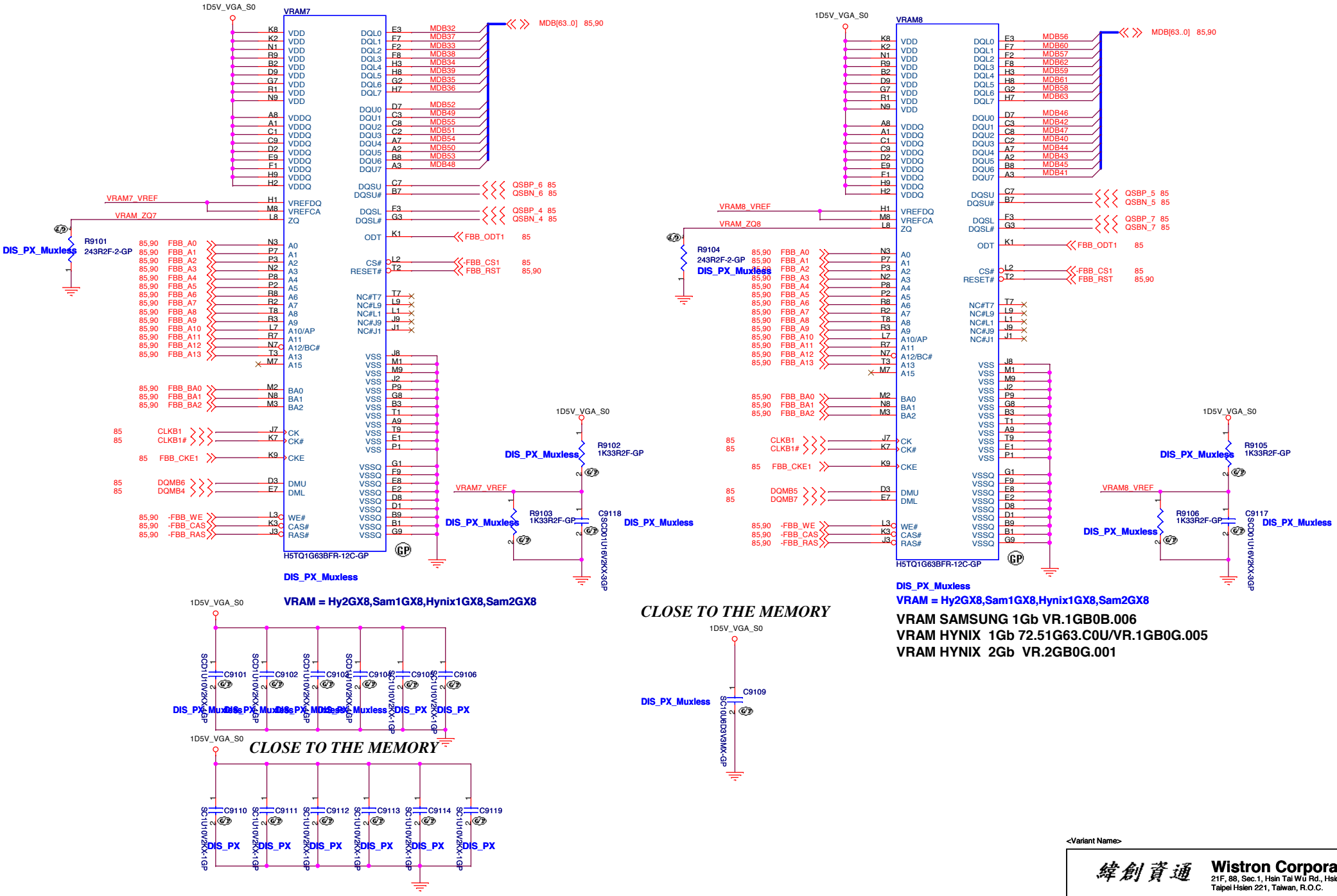
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
Custom	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 90 of 108



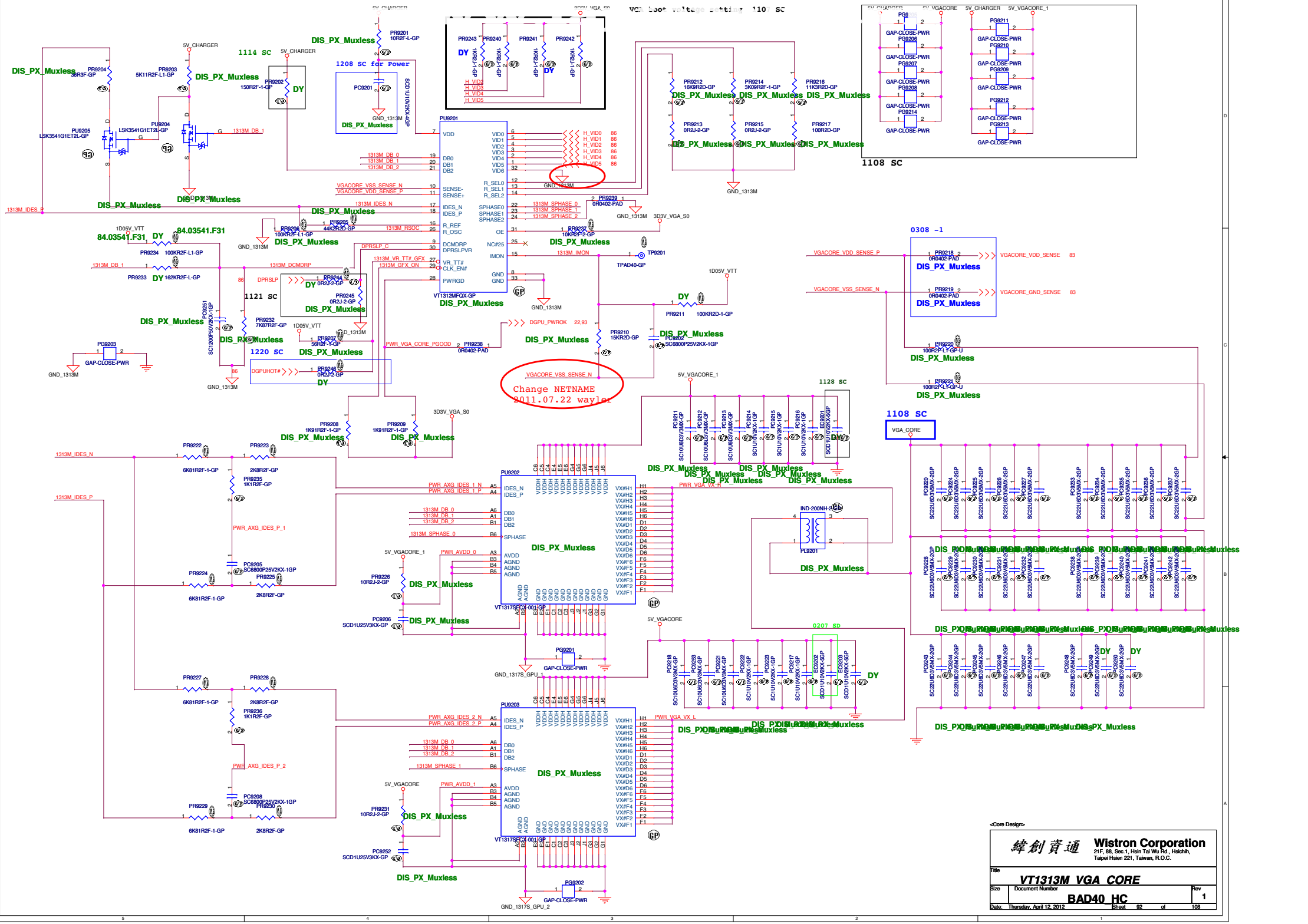
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

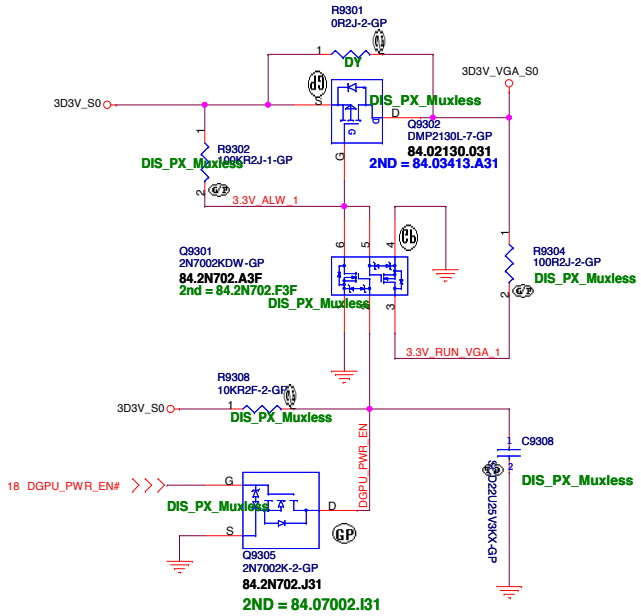
Title: GPU-VRAM7,8 (4/4)

Size: Custom | Document Number: BAD40_HC | Rev: 1

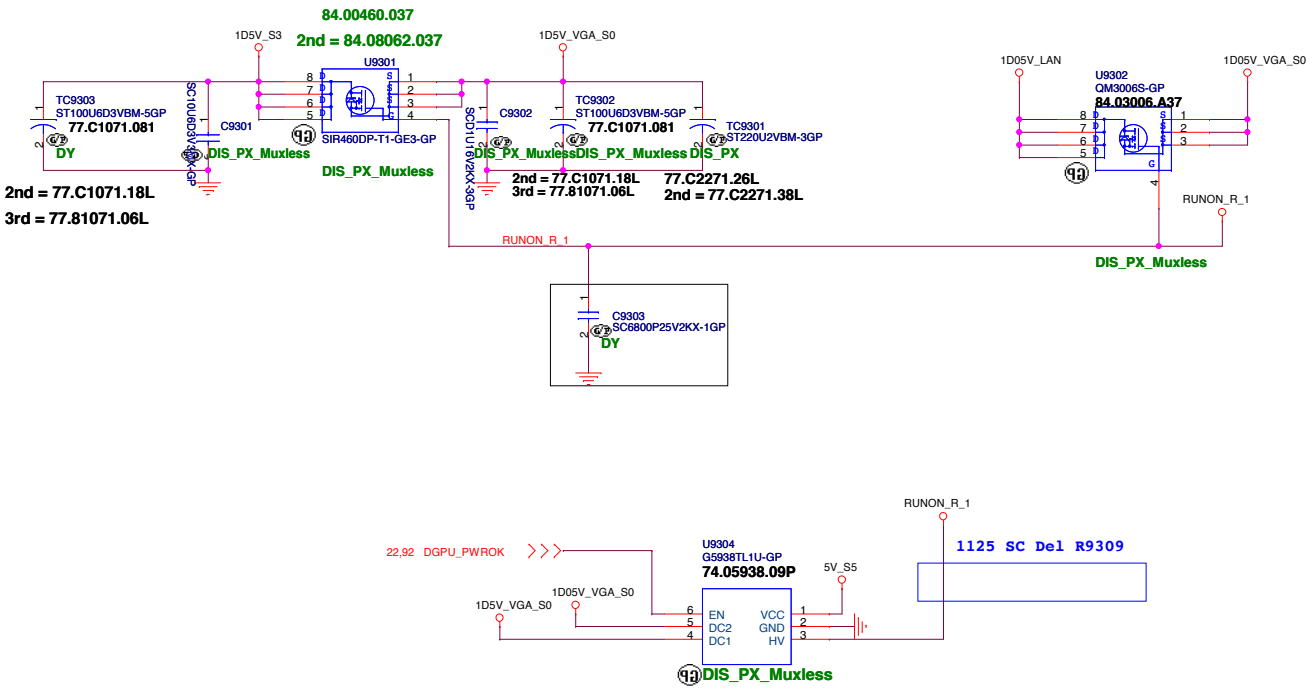
Date: Thursday, April 12, 2012 | Sheet 91 of 108


1114 SC
1208 SC for Power
1108 SC
1121 SC
1220 SC
1128 SC
0308 -1
0207 SP
Change NETNAME
2011.07.22 waylor
VT1312MFQX-GP
VT1317SFCX-001-GP
DIS_PX_Muxless
DY
5V_CHARGER
5V_VGACORE
5V_VGACORE_1
3D3V_VGA_S0
1D05V_VTT
GND_1313M
GND_1317S_GPU_1
GND_1317S_GPU_2
VGA_CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VT1313M VGA CORE
BAD40_HC
Rev 1
Thursday, April 12, 2012
Sheet 92 of 108

+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1D8V_S0 to 1D8V_VGA_S0

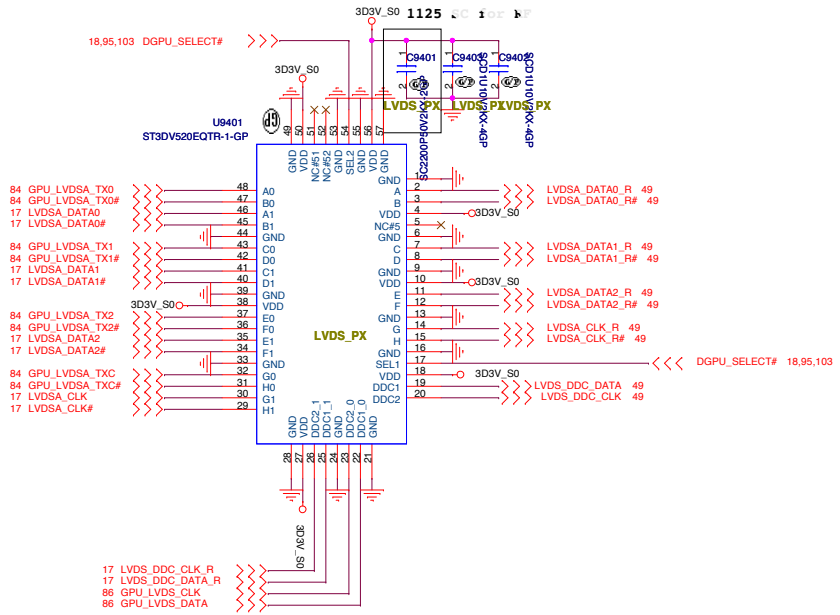
1125 SC Del Q9306

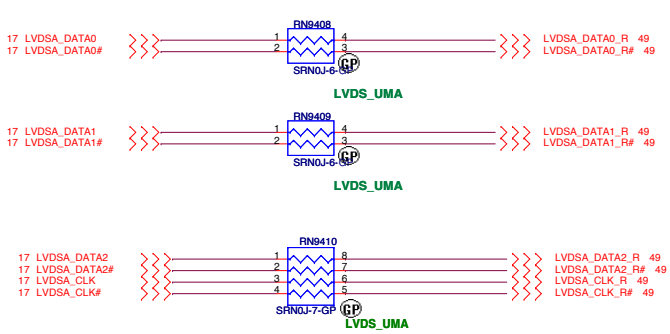
1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISCRETE VGA POWER		
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 93 of 108	

LVDS

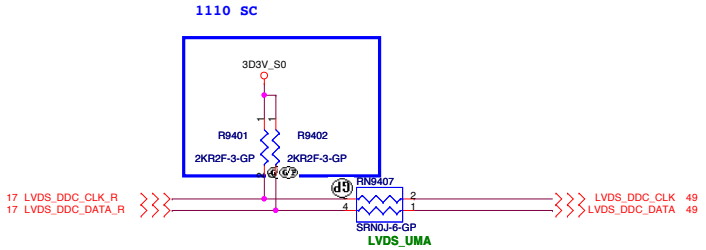




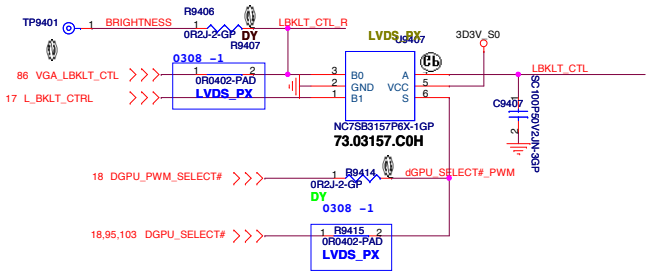
SEL->L(X=nX0),H(X=nX1)

SEL1 Control A~H

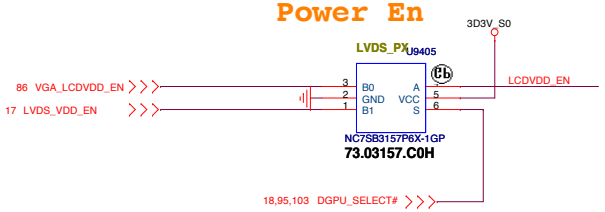
SEL2 Control DDC1,DDC2



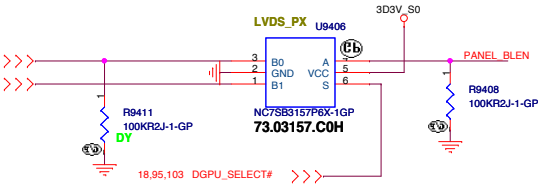
Panel BL brightness



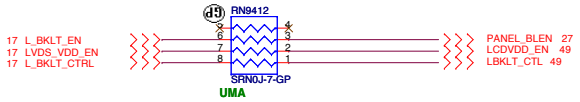
Power En



BL En



Panel BL brightness/Power En/BL En



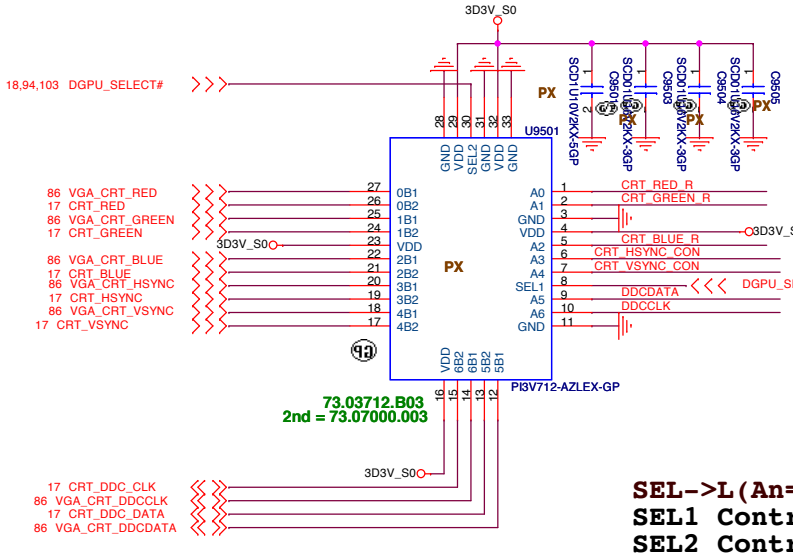
<Variant Name>

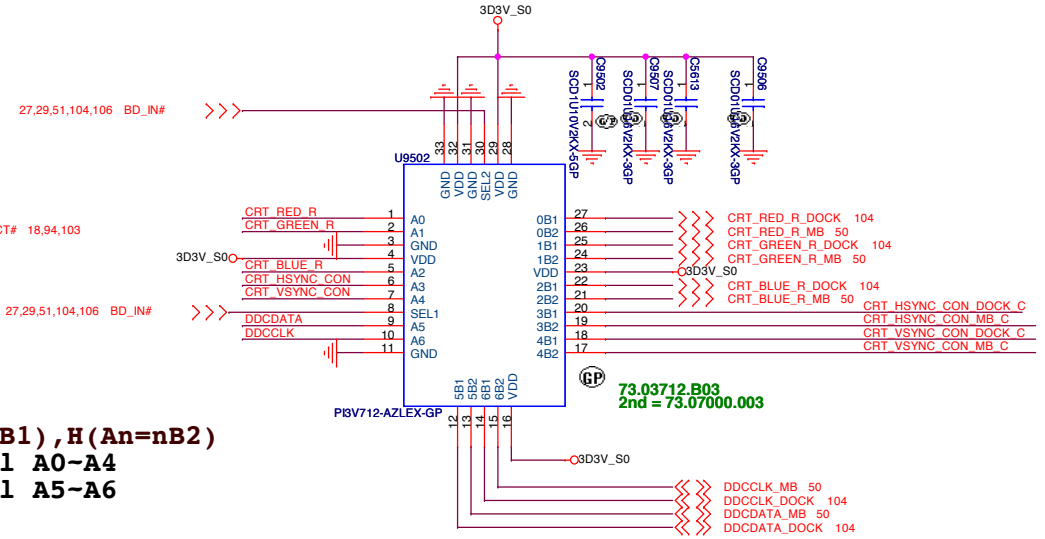
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
Custom	BAD40_HC	1
Date: Thursday, April 12, 2012	Sheet 94 of 108	

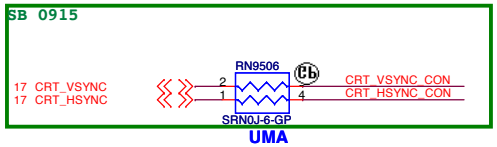
CRT DDCDATA & DDCCLK

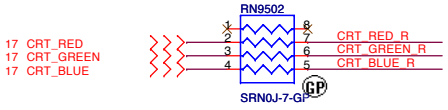




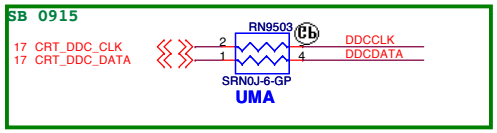
SEL->L(An=nB1),H(An=nB2)
SEL1 Control A0~A4
SEL2 Control A5~A6

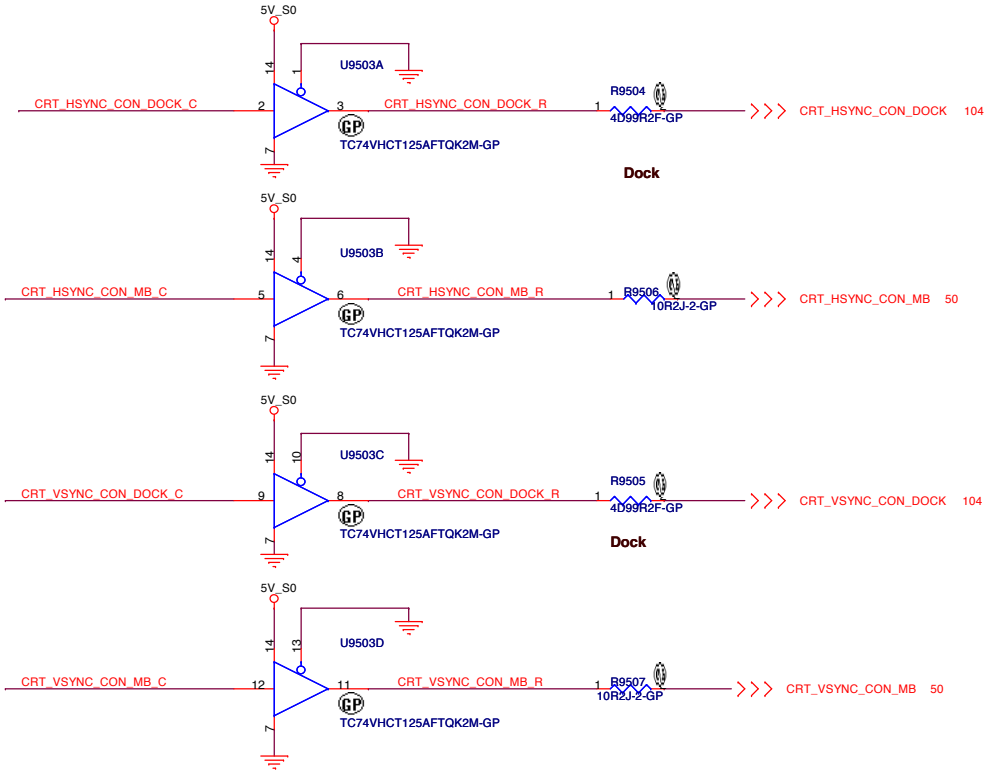
SB 0915





SB 0915





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT_Switch**

Size: A3 | Document Number: **BAD40_HC** | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 95 of 108

SSID = SDIO

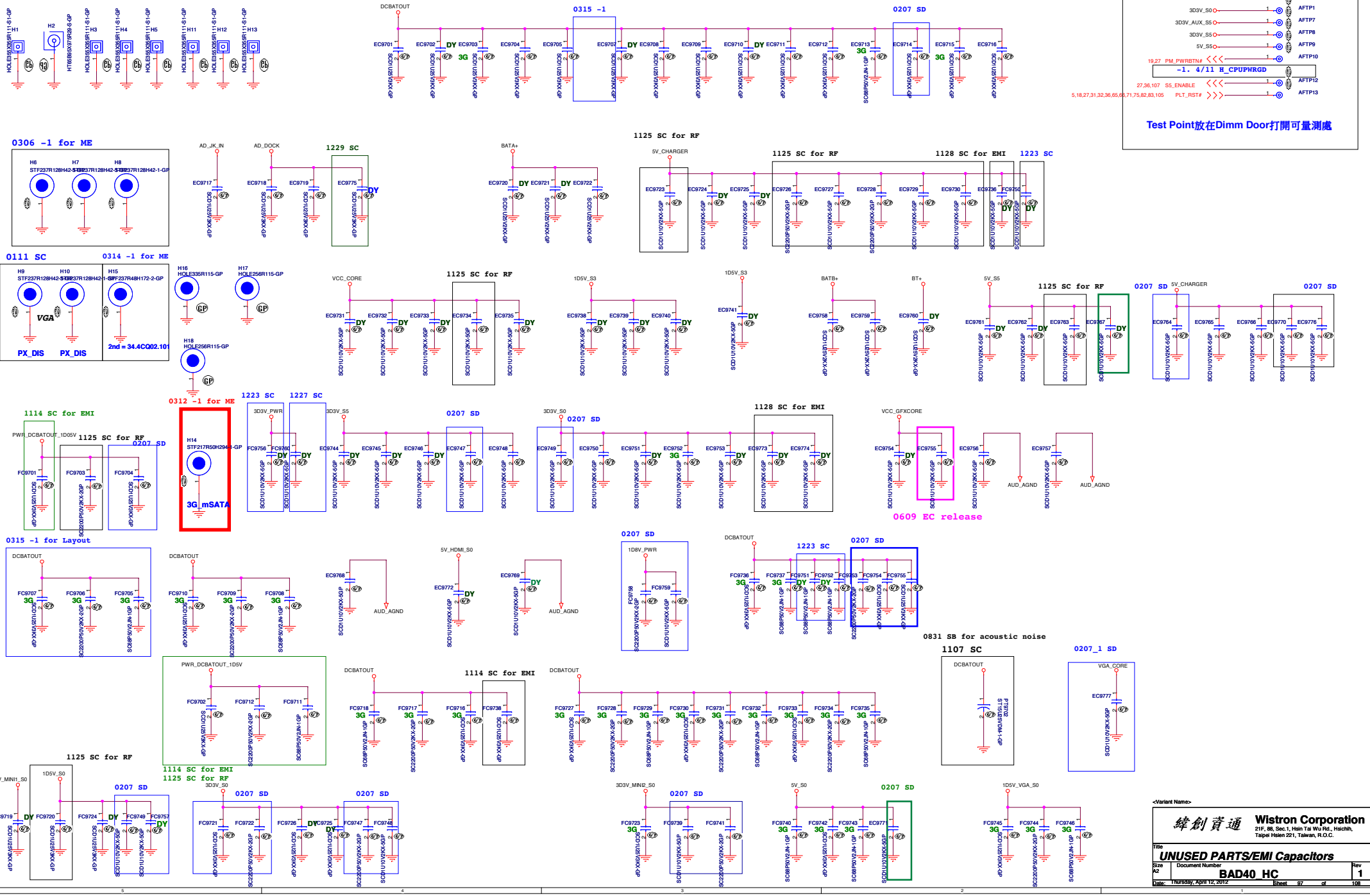
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

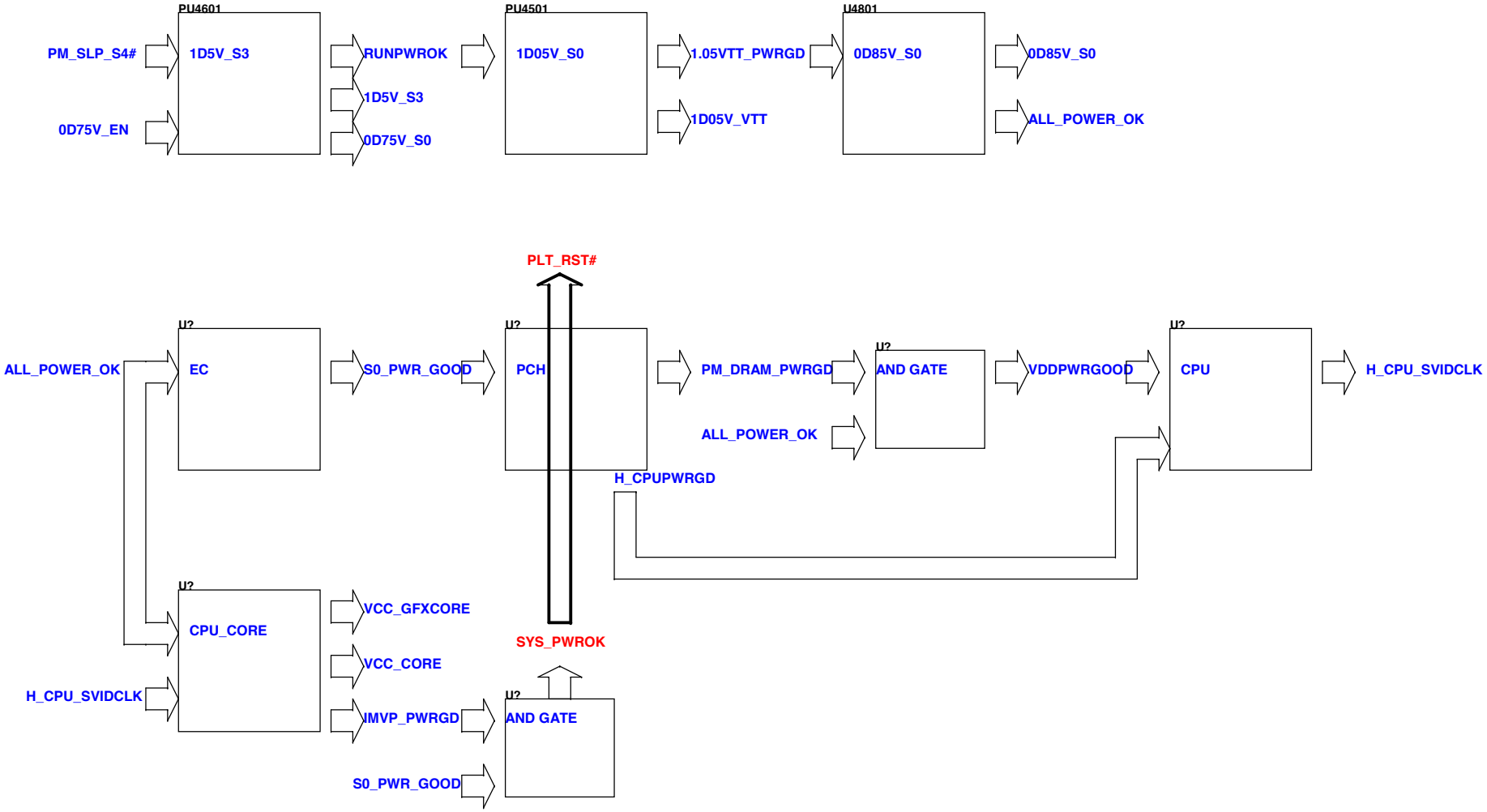
Title: ***TOUCH PANEL***

Size	Document Number	Rev
A2	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 96 of 108


Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
19,27 PM_PWRBTN#
-1. 4/11 H_CPUPWRGD
27,36,107 S5_ENABLE
5,18,27,31,32,36,65,68,71,75,82,83,105 PLT_RST#
AFTP1
AFTP7
AFTP8
AFTP9
AFTP10
AFTP12
AFTP13
Test Point放在Dimm Door打開可量測處
0315 -1
0207 SD
0306 -1 for ME
1125 SC for RF
1128 SC for EMI
1223 SC
1229 SC
0111 SC
0314 -1 for ME
VGA
PX_DIS
2nd = 34.4CQ02.101
0312 -1 for ME
3G_mSATA
1114 SC for EMI
1227 SC
0609 EC release
0315 -1 for Layout
0831 SB for acoustic noise
1107 SC
0207_1 SD
1125 SC for RF
1114 SC for EMI
1125 SC for RF
0609 EC release
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size A2
Document Number
BAD40_HC
Rev 1
Date: Thursday, April 12, 2012
Sheet 97 of 108

Power Sequence



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

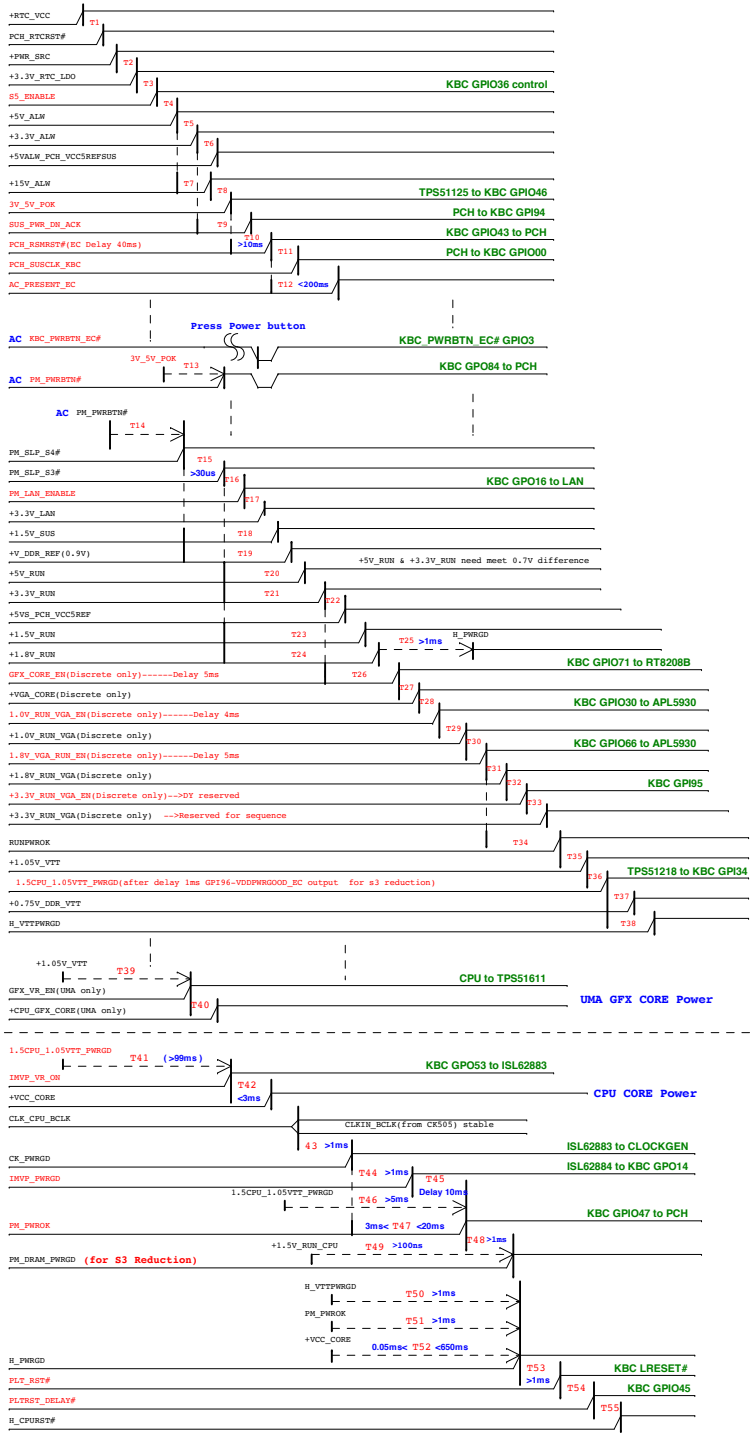
Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 98 of 108

Intel-Power Up Sequence

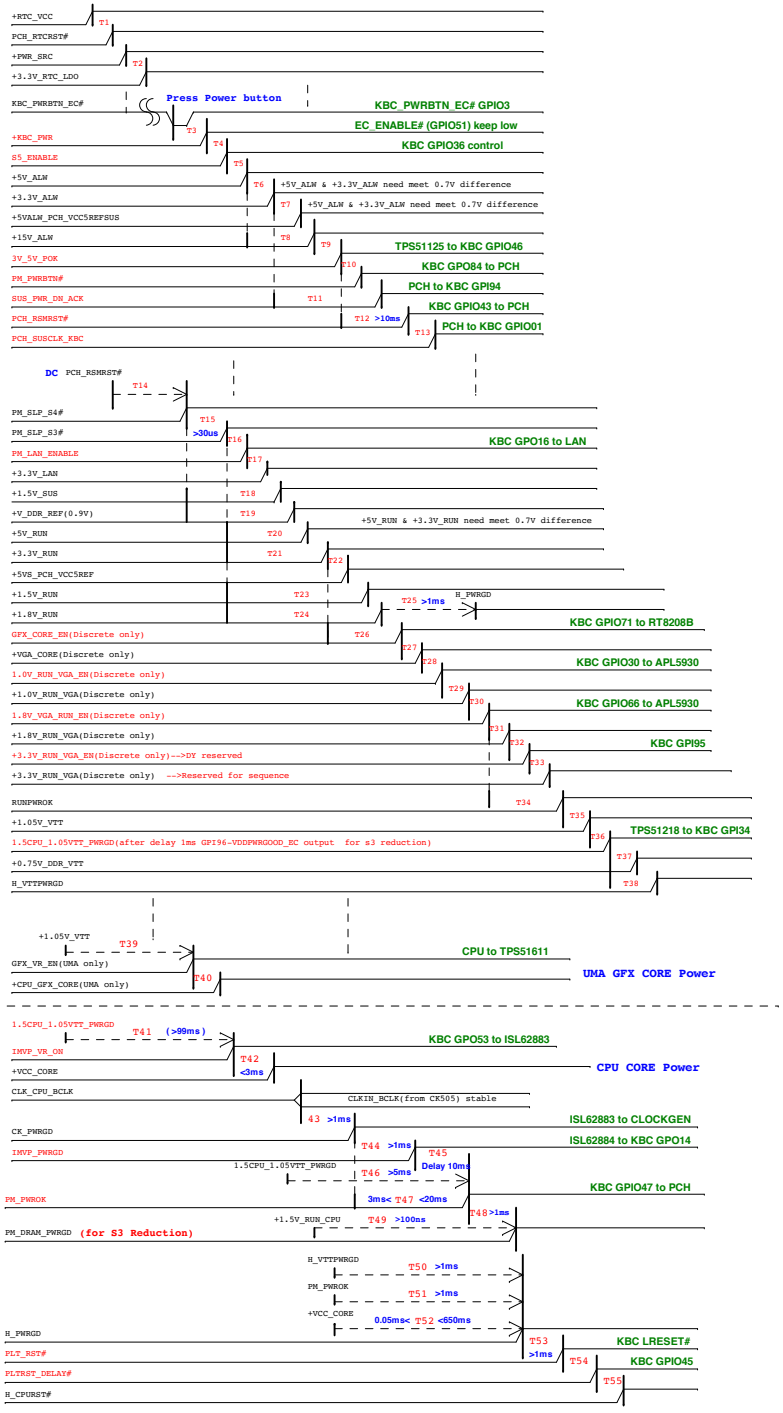
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



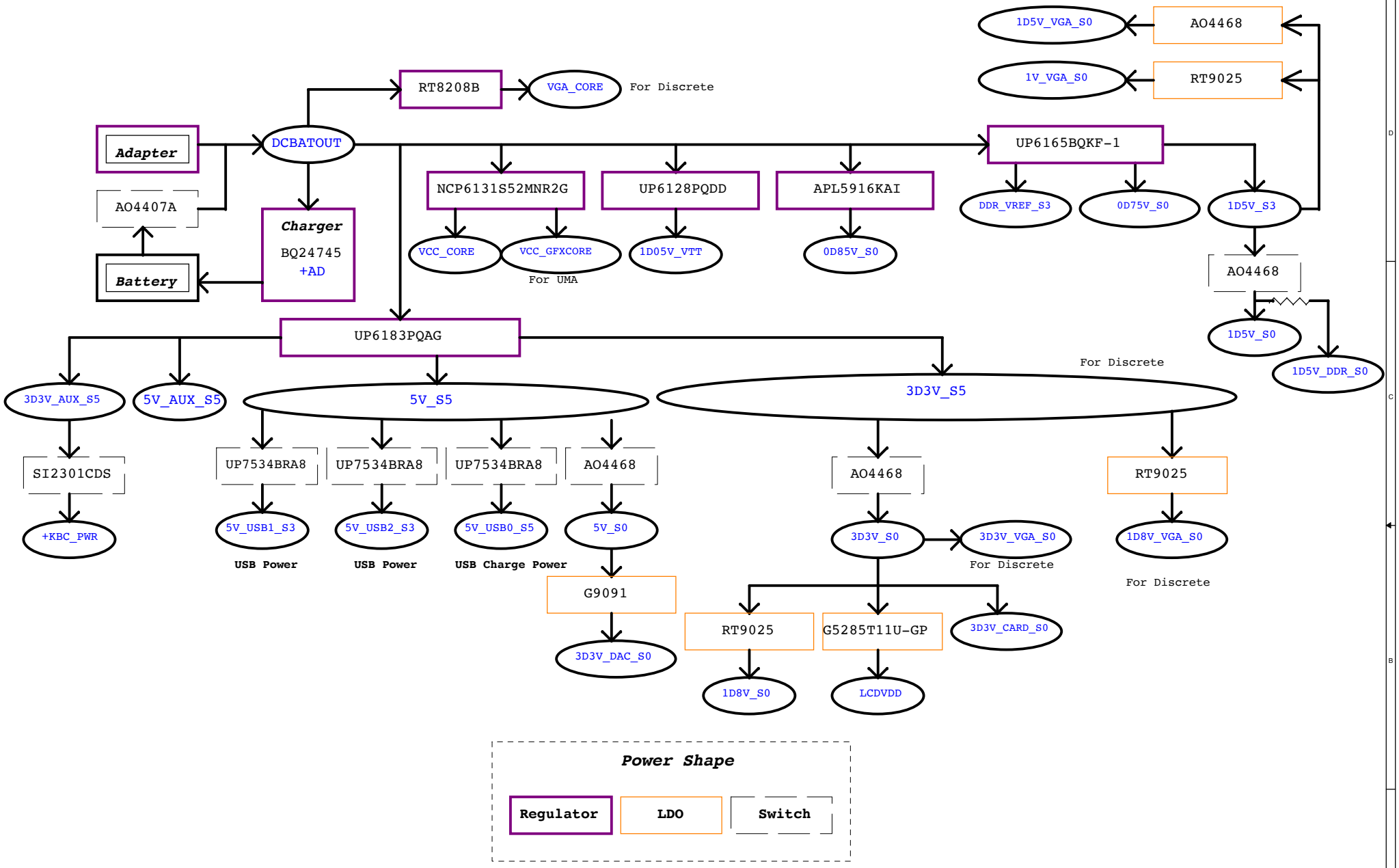
HR PX

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
M	BAD40_HC	1

Date: Thursday, April 15, 2010 Sheet 59 of 109



HR PX

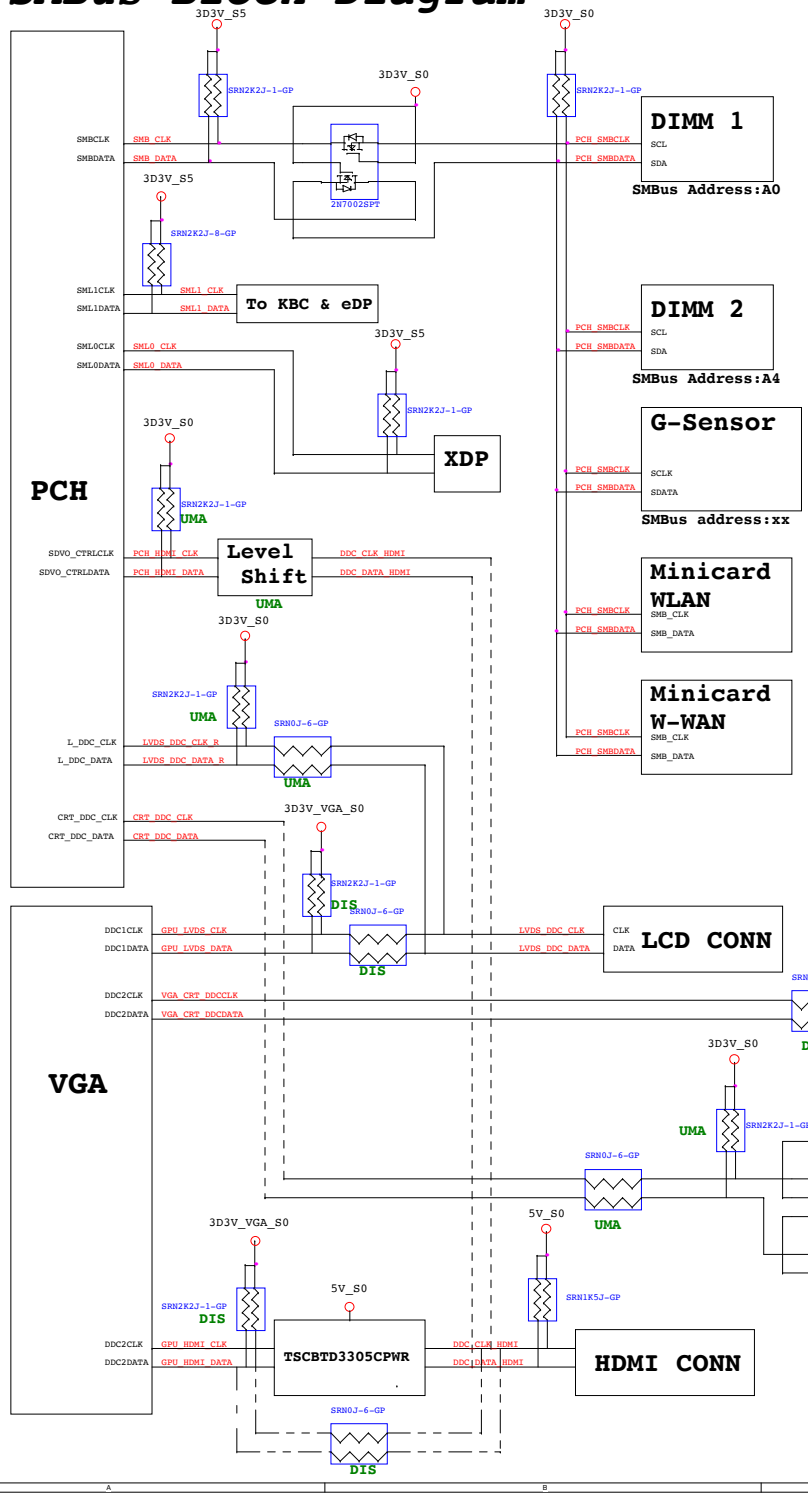
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

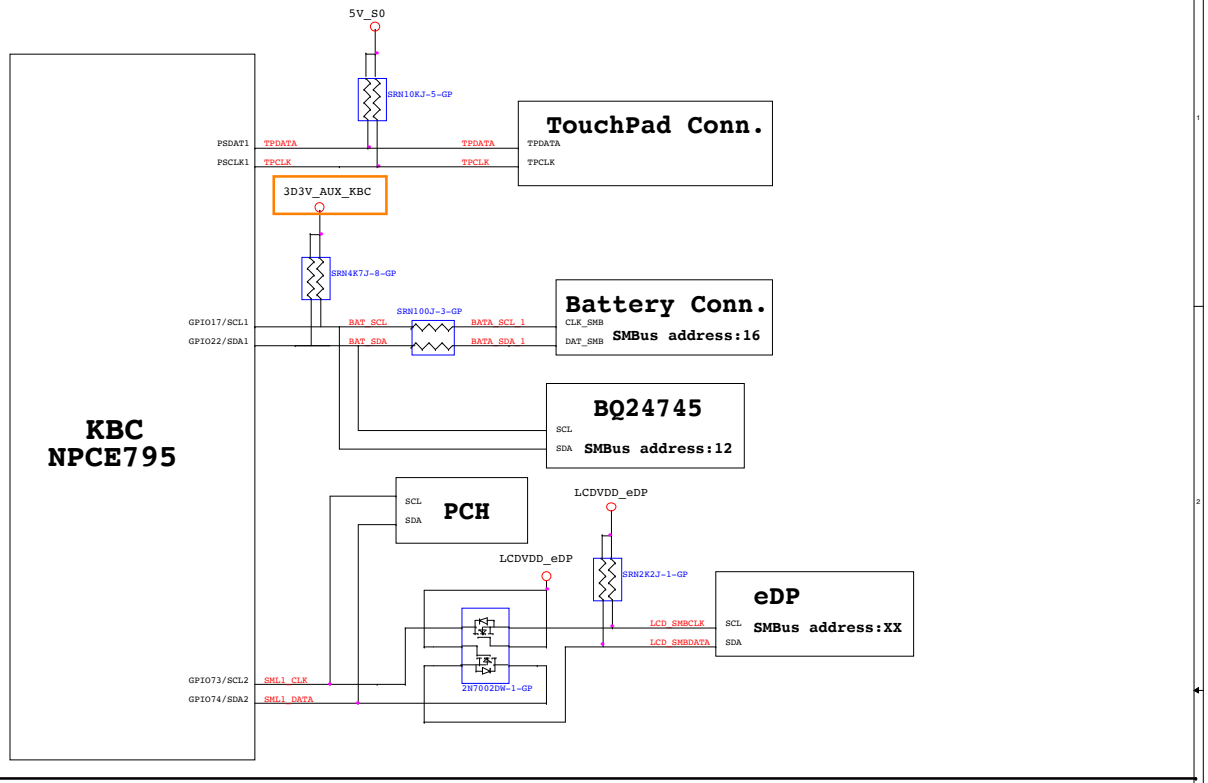
Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 100 of 108

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

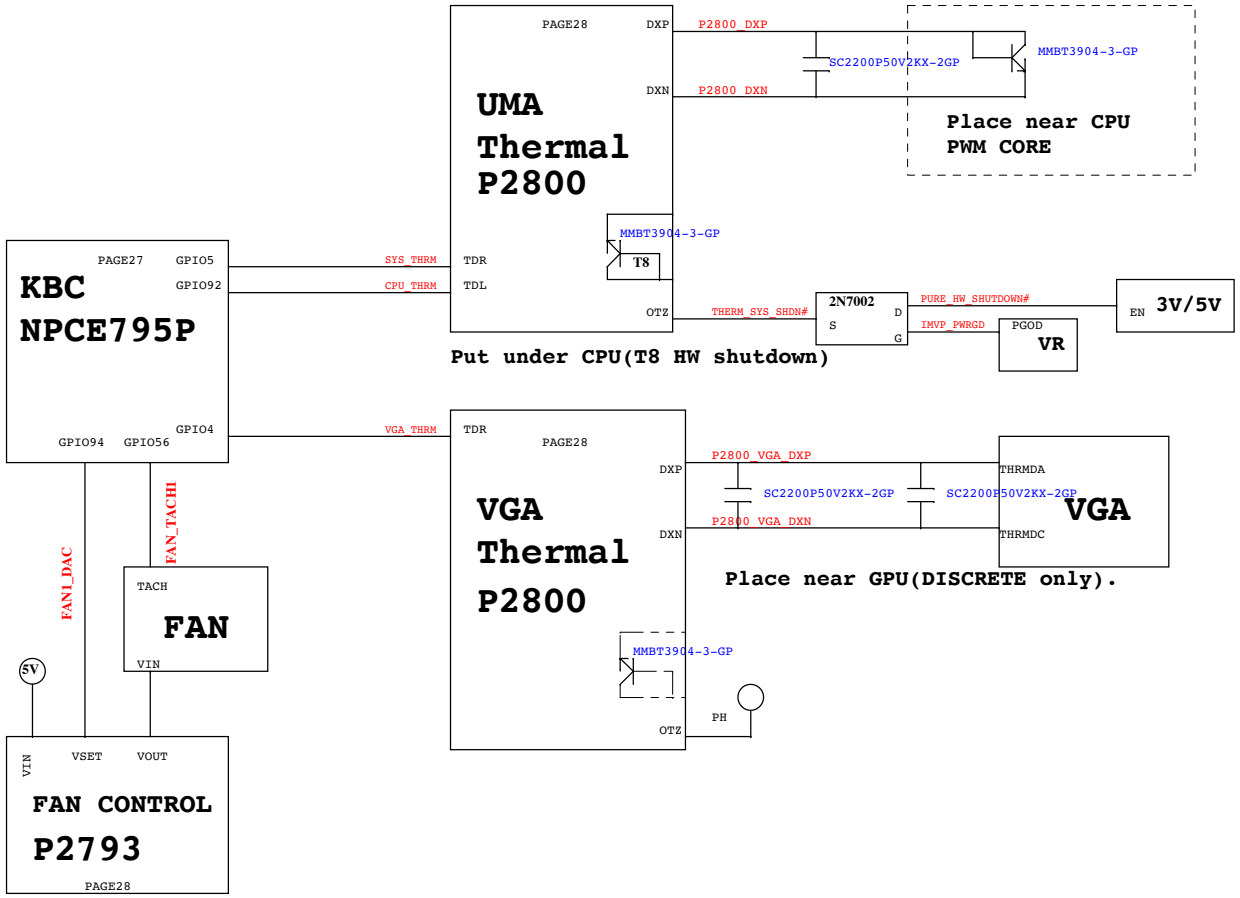
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

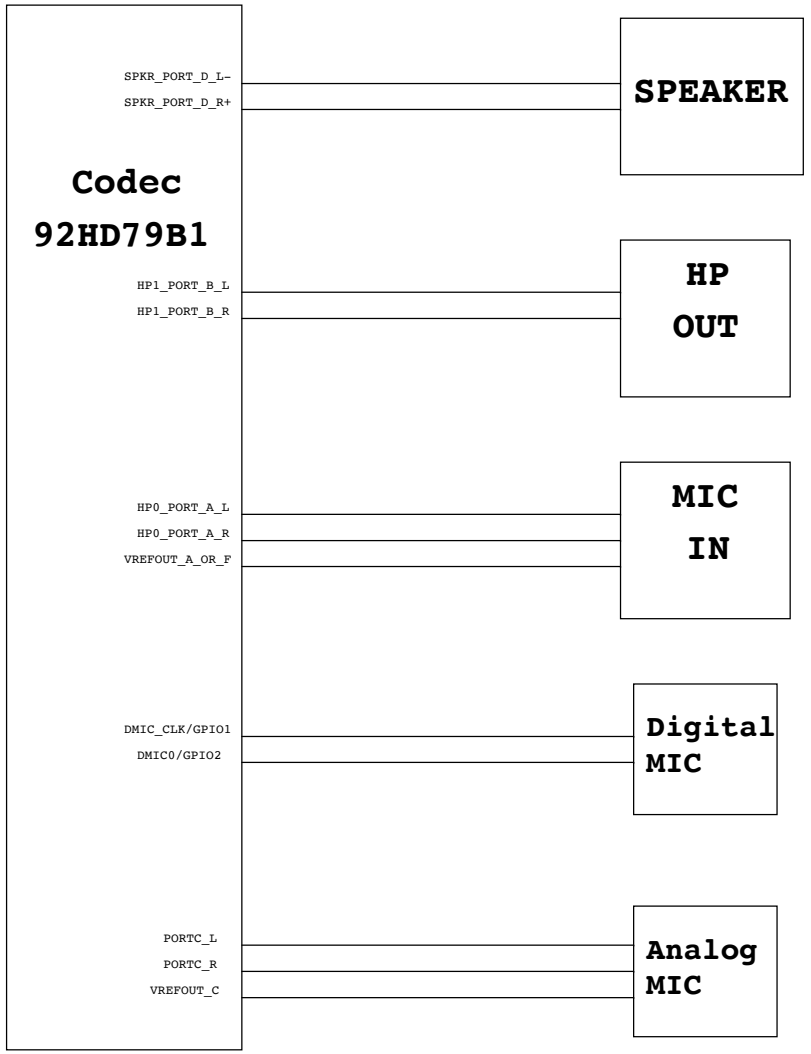
Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 101 of 108

Thermal Block Diagram



Audio Block Diagram



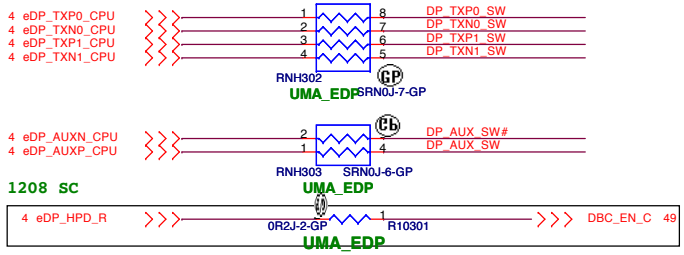
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

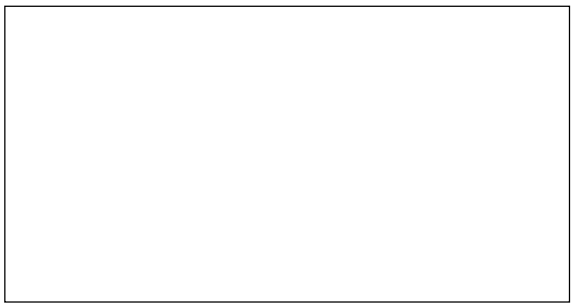
Title: Thermal/Audio Block Diagram

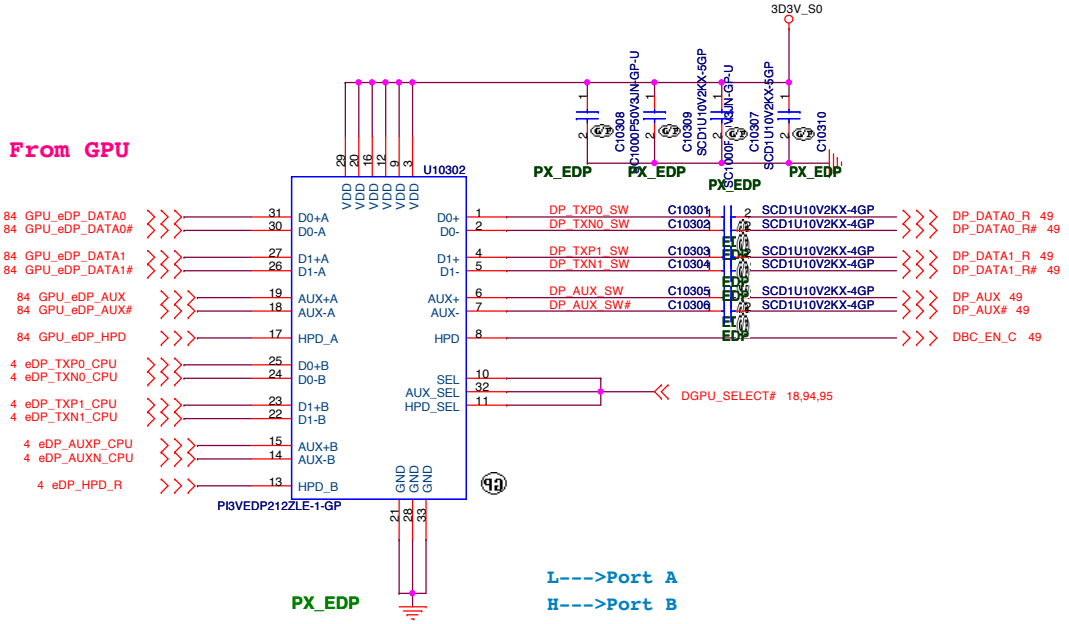
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 102 of 108



1117 SC del eDP SMBUS

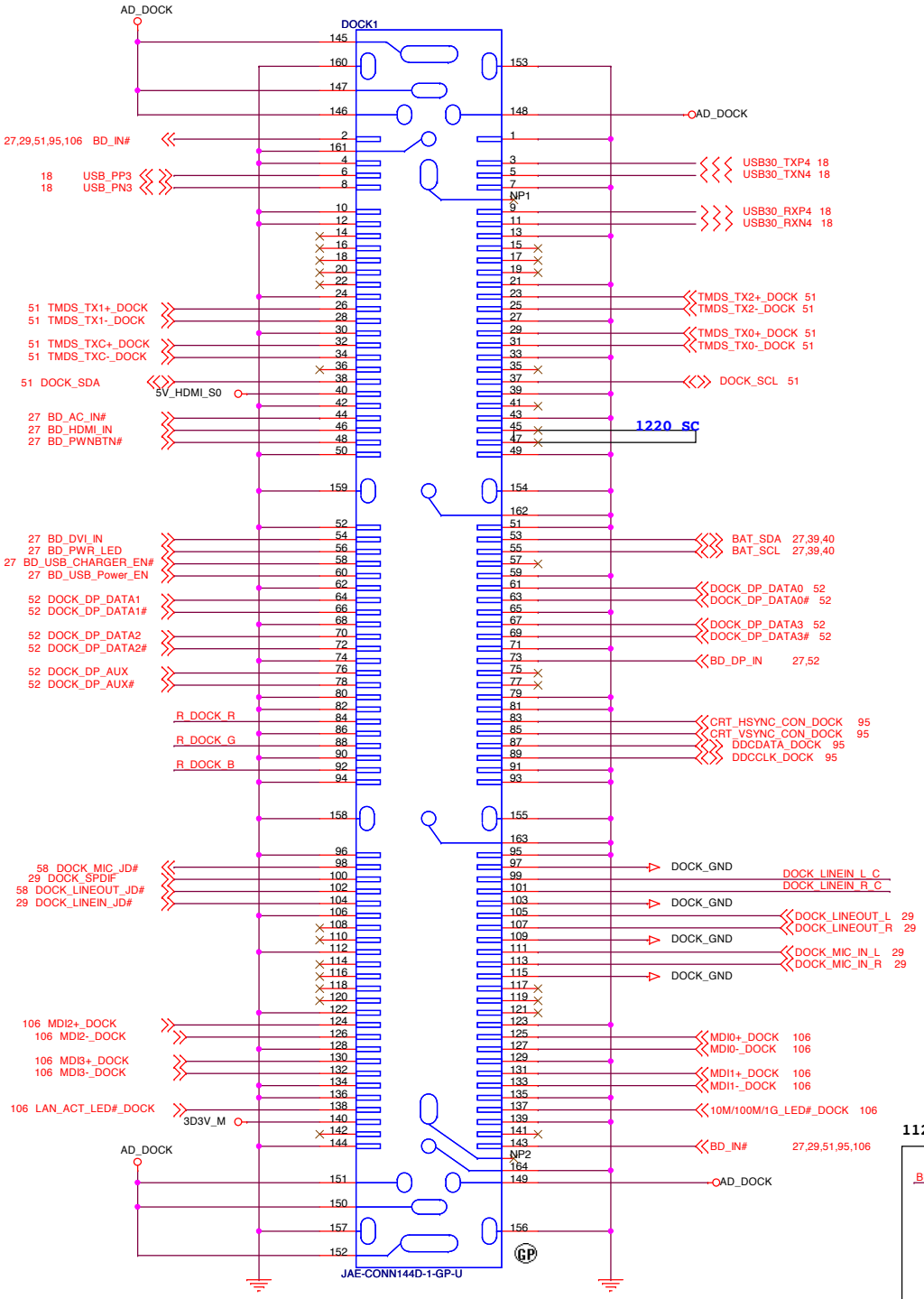


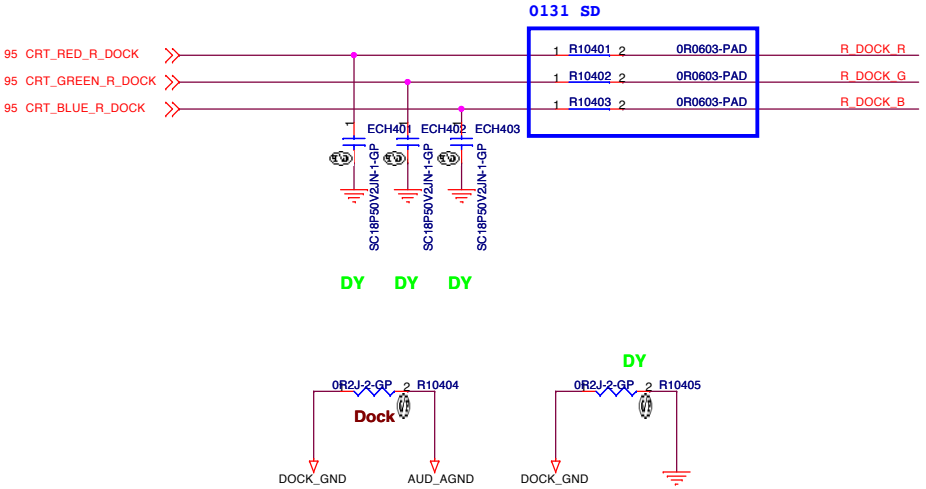


<Variant Name>

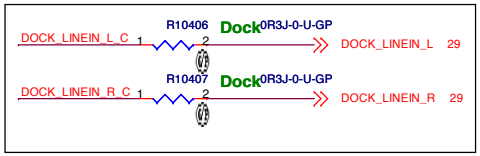
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Switch GFX DP	
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 103 of 108	

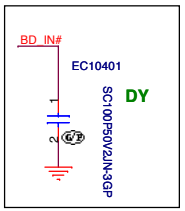




1128 SC for EMI



1128 SC for EMI



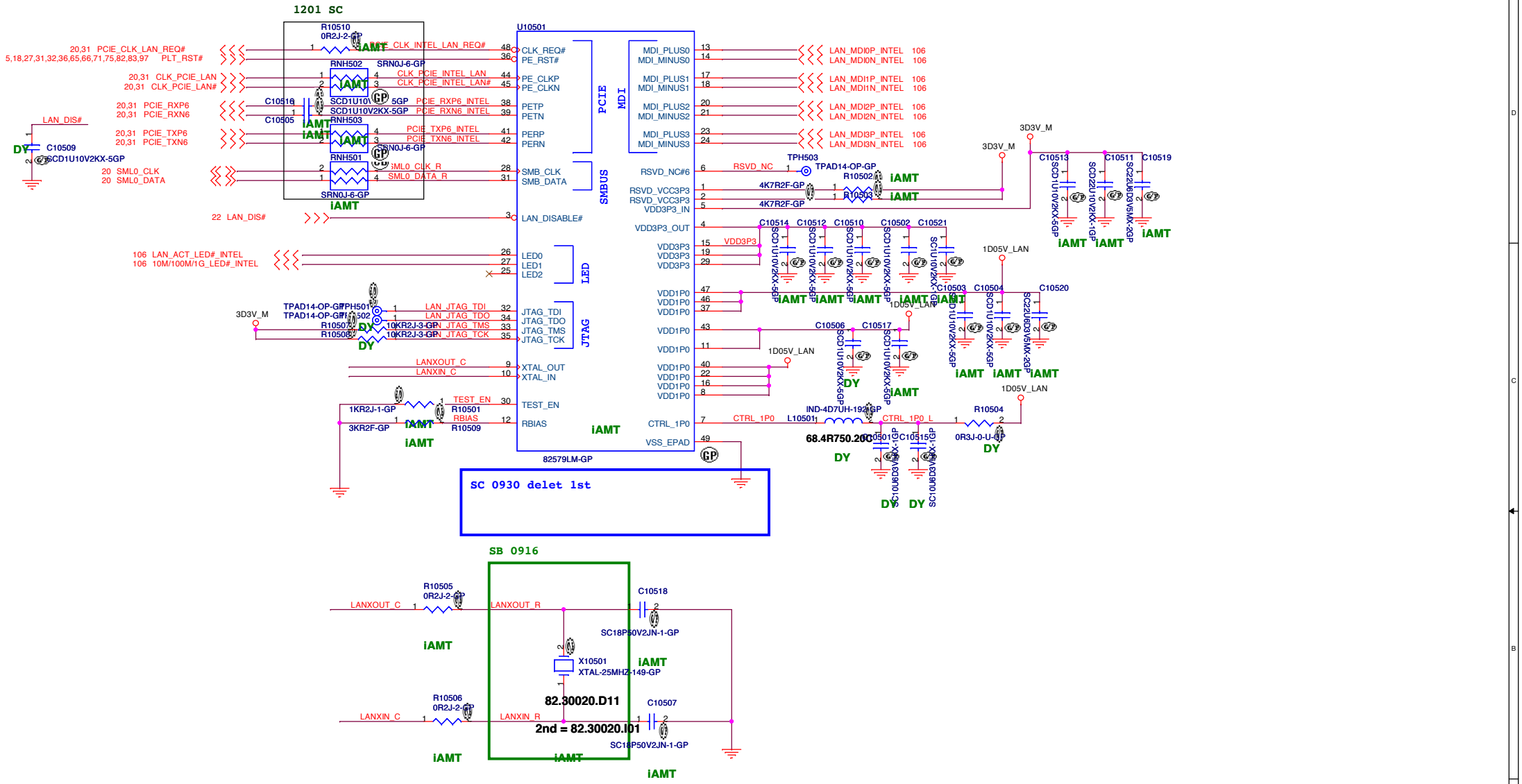
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BOTTOM DOCKING

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 104 of 108

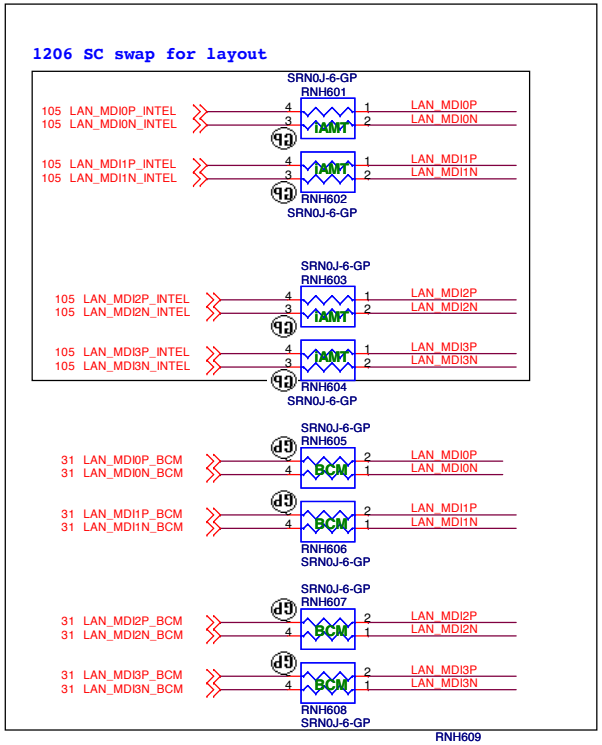


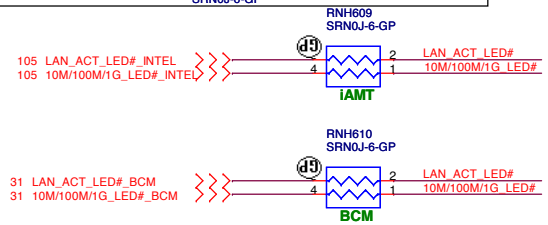
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LAN INTEL 82579*		
Size: A3	Document Number: BAD40 HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 105 of 108	

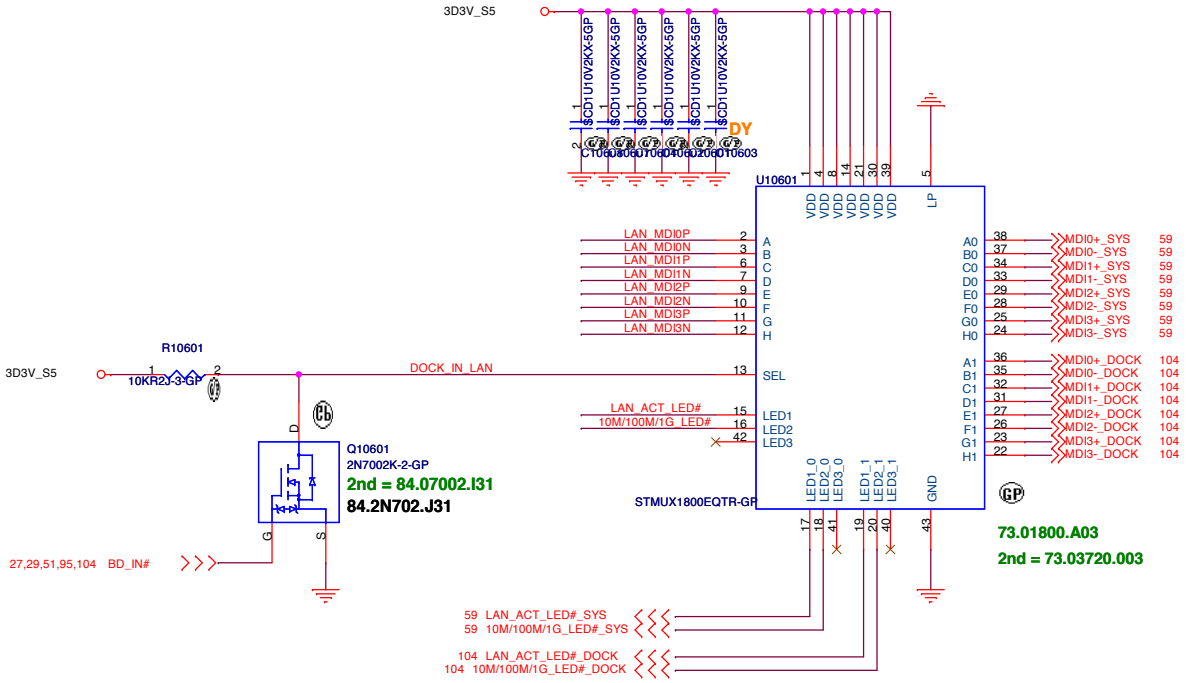
1201 SC

1206 SC swap for layout





LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

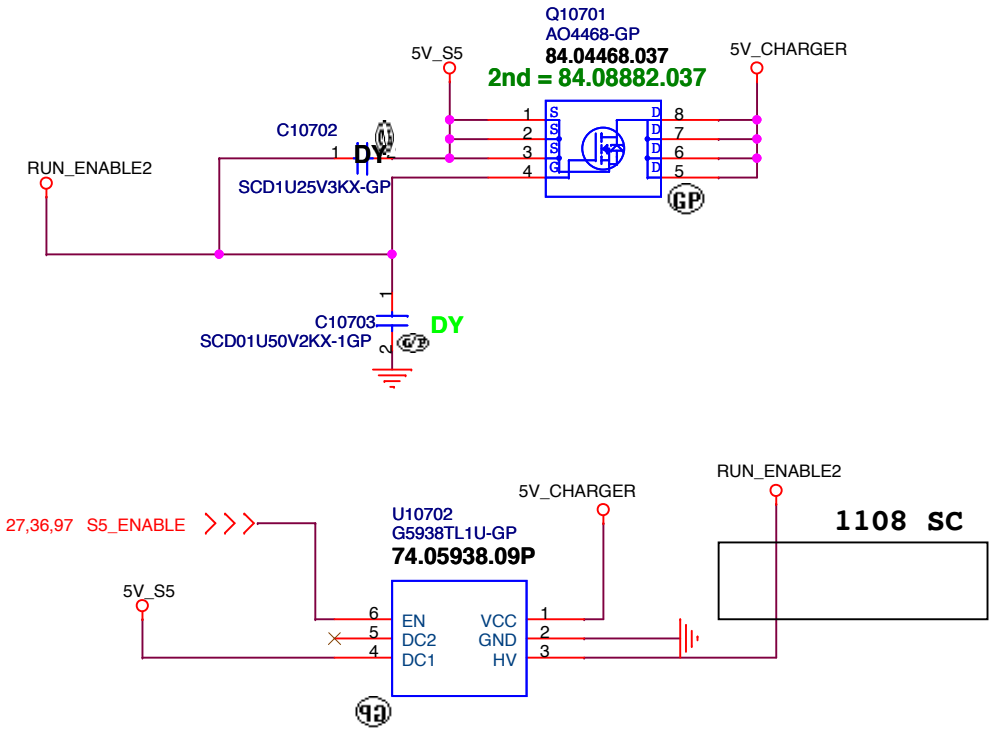
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN SWITCH

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 106 of 108



USB charger @ USB30 BD

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB Charger/ 5V_S5*	
Size A4	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 107 of 108	

reserve

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2 HUB AU6256**

Size	Document Number	Rev
	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 108 of 108