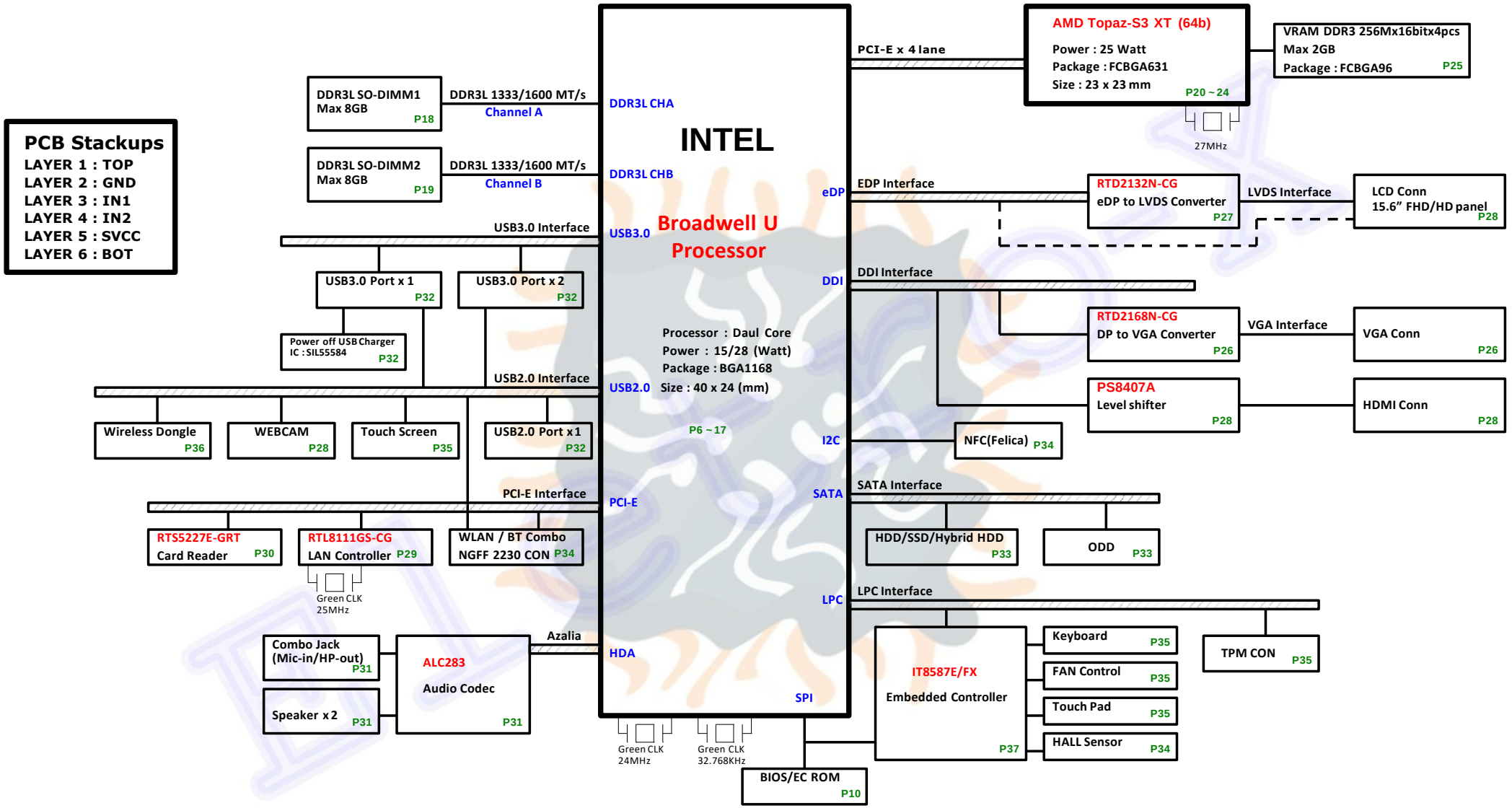
FH9 DIS (15.6") Broadwell Platform Block Diagram



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BLOCK DIAGRAM | 2A
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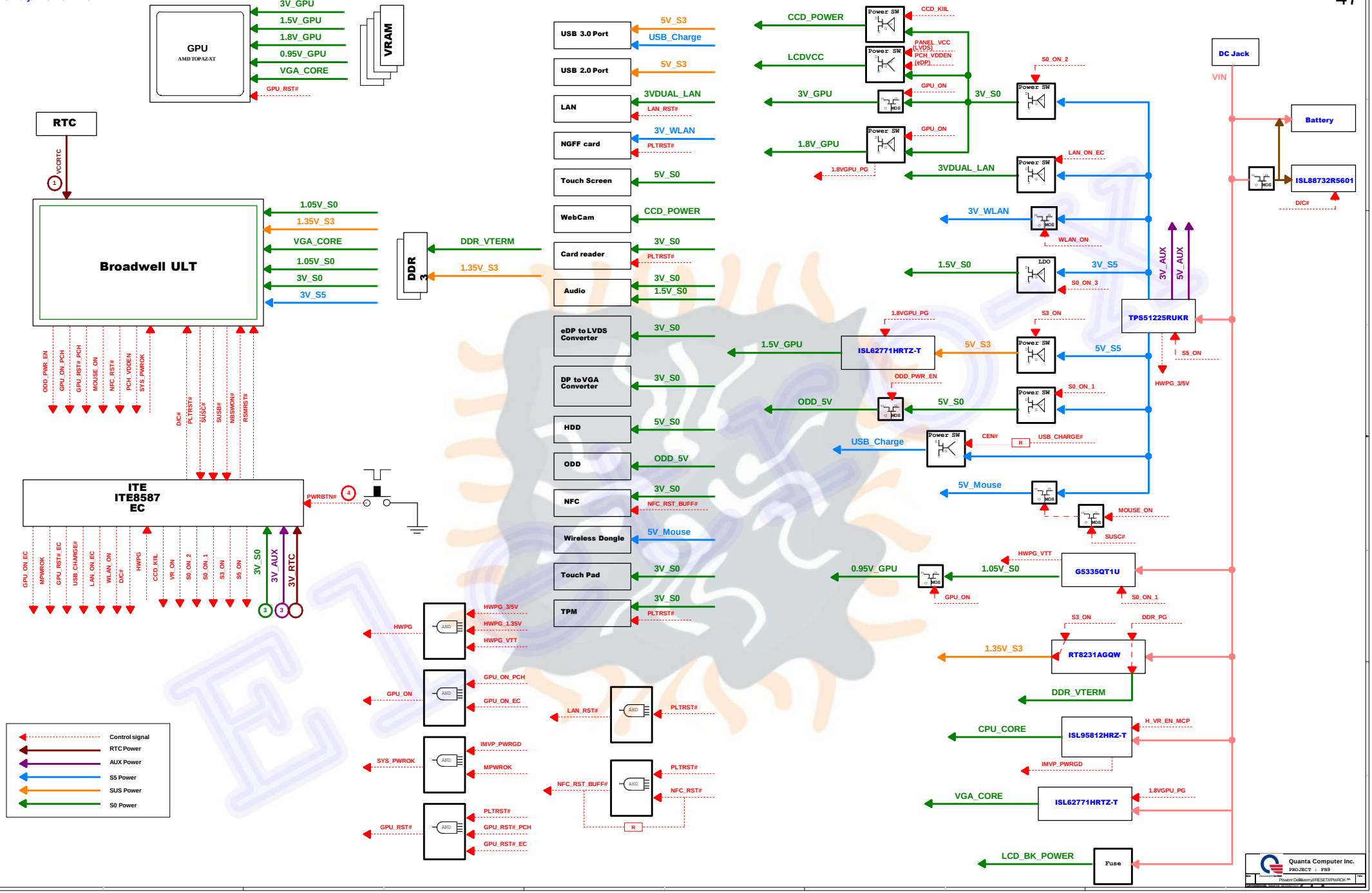
GPU
AMD TOPAZ-XT
VRAM
3V_GPU
1.5V_GPU
1.8V_GPU
0.95V_GPU
VGA_CORE
GPU_RST#
RTC
VCCRTC
Broadwell ULT
1.05V_S0
1.35V_S3
VGA_CORE
1.05V_S0
3V_S0
3V_S5
DDR 3
DDR_VTERM
1.35V_S3
ODD_PWR_EN
GPU_ON_PCH
GPU_RST#_PCH
MOUSE_ON
NFC_RST#
PCH_VDDEN
SYS_PWROK
DIC#
PLTRST#
SUSC#
SUSB#
NBSWON#
RSMRST#
ITE
ITE8587
EC
PWRBTN#
GPU_ON_EC
MPWROK
GPU_RST#_EC
USB_CHARGE#
LAN_ON_EC
WLAN_ON
DIC#
HWPG
CCD_KILL
VR_ON
S0_ON_2
S0_ON_1
S3_ON
S5_ON
3V_S0
3V_AUX
3V_RTC
USB 3.0 Port
5V_S3
USB_Charge
USB 2.0 Port
5V_S3
LAN
3VDUAL_LAN
LAN_RST#
NGFF card
3V_WLAN
PLTRST#
Touch Screen
5V_S0
WebCam
CCD_POWER
Card reader
3V_S0
PLTRST#
Audio
3V_S0
1.5V_S0
eDP to LVDS Converter
3V_S0
DP to VGA Converter
3V_S0
HDD
5V_S0
ODD
ODD_5V
NFC
3V_S0
NFC_RST_BUFF#
Wireless Dongle
5V_Mouse
Touch Pad
3V_S0
TPM
3V_S0
PLTRST#
HWPG_3/5V
HWPG_1.35V
HWPG_VTT
GPU_ON_PCH
GPU_ON_EC
IMVP_PWRGD
MPWROK
PLTRST#
GPU_RST#_PCH
GPU_RST#_EC
LAN_RST#
PLTRST#
NFC_RST_BUFF#
PLTRST#
NFC_RST#
R
CCD_POWER
LCDVCC
3V_GPU
1.8V_GPU
Power SW
CCD_KILL
PANEL_VCC (LVDS)
PCH_VDDEN (eDP)
GPU_ON
1.8VGPU_PG
3V_S0
S0_ON_2
3VDUAL_LAN
LAN_ON_EC
3V_WLAN
WLAN_ON
1.5V_S0
LDO
3V_S5
S0_ON_3
3V_AUX
5V_AUX
TPS51225RUKR
S5_ON
HWPG_3/5V
1.8VGPU_PG
1.5V_GPU
ISL62771HRTZ-T
5V_S3
S3_ON
5V_S5
ODD_PWR_EN
ODD_5V
5V_S0
S0_ON_1
USB_Charge
CEN#
R
USB_CHARGE#
5V_Mouse
MOUSE_ON
SUSC#
0.95V_GPU
1.05V_S0
G5335QT1U
HWPG_VTT
GPU_ON
S0_ON_1
1.35V_S3
RT8231AGQW
S3_ON
DDR_PG
DDR_VTERM
CPU_CORE
ISL95812HRZ-T
H_VR_EN_MCP
IMVP_PWRGD
VGA_CORE
ISL62771HRTZ-T
1.8VGPU_PG
LCD_BK_POWER
Fuse
DC Jack
VIN
Battery
ISL88732R5601
D/C#
Control signal
RTC Power
AUX Power
S5 Power
SUS Power
S0 Power
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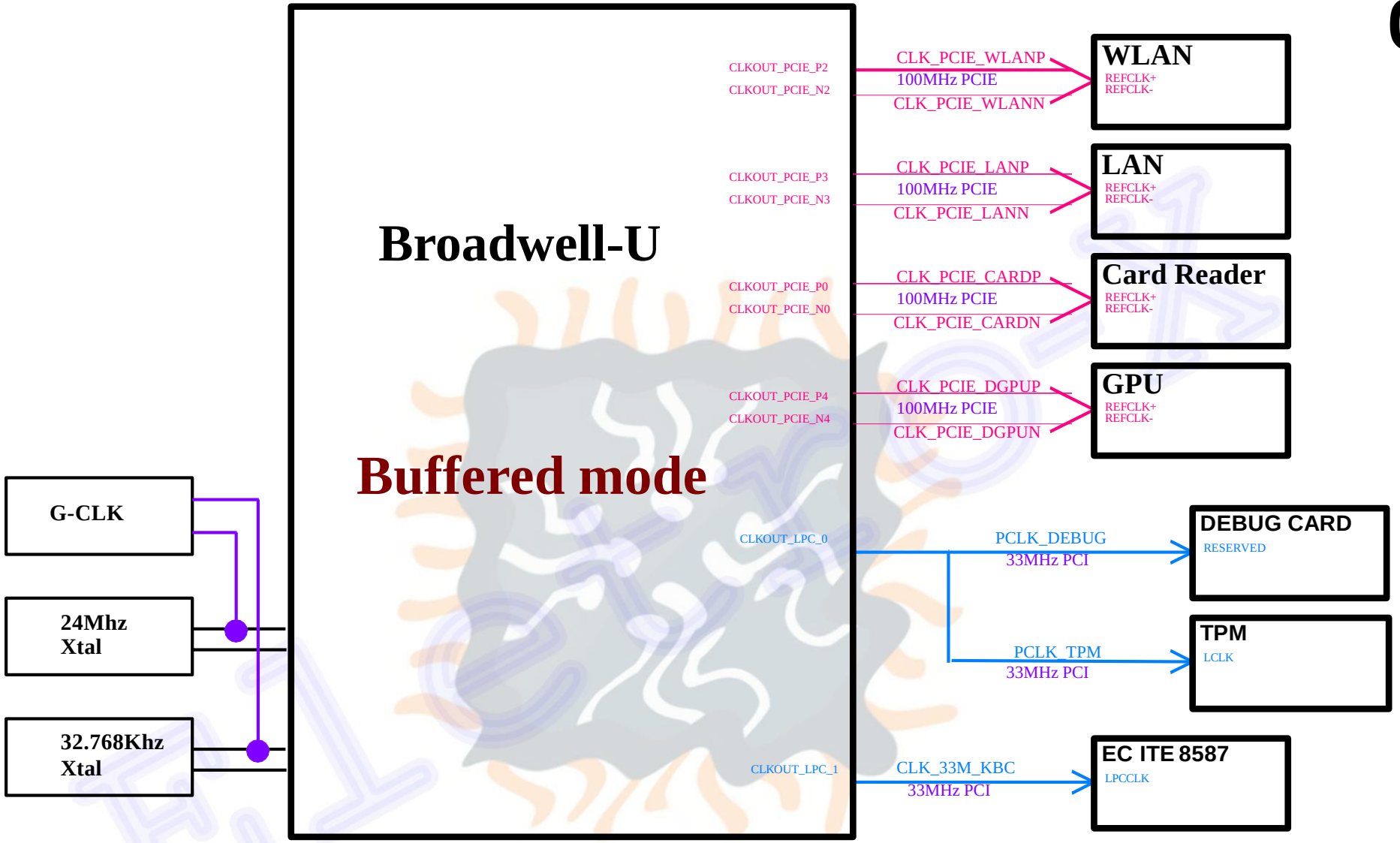

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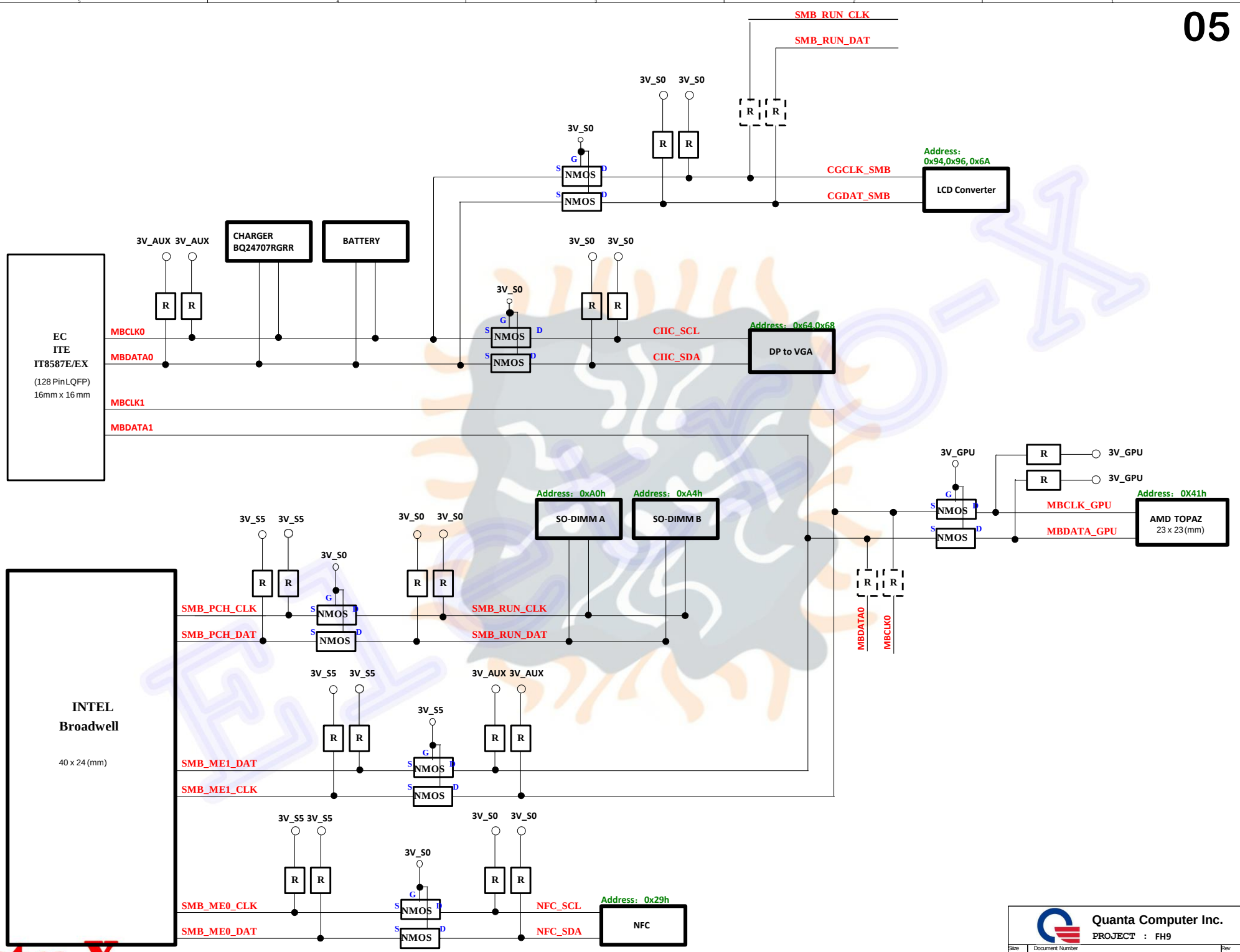

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Table of Contents

Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	S5_ON
1.35V_S3	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
3VDUAL_LAN	3.3V	ON	OFF	OFF	OFF	OFF	LAN_ON_EC
3V_WLAN	3.3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_3
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
1.05V_VCCST	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
DDR_VTERM	0.675V	ON	OFF	OFF	OFF	OFF	DDR_PG
VCC_CORE	1.7V	ON	OFF	OFF	OFF	OFF	H_VR_EN_MCP
VGA_CORE	1V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
3V_GPU	3.3V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.8V_GPU	1.8V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.5V_GPU	1.5V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
0.95V_GPU	0.95V	ON	OFF	OFF	OFF	OFF	GPU_ON

Function List

USB2		PCIE		Display		USB3		SATA	
Port 0	Co-lay USB3.0	Port 1	Card Reader	eDP Port 1	LVDS or eDP	Port 1	USB3.0 Conn	Port 0	HDD
Port 1	Co-lay USB3.0	Port 2	USB3.0 Conn	eDP Port 2	NC	Port 2	USB3.0 Conn	Port 1	ODD
Port 2	Co-lay USB3.0	Port 3	WLAN	DDI Port 1	HDMI	Port 3	Card Reader	Port 2	NC
Port 3	Touch screen	Port 4	GLAN	DDI Port 2	CRT	Port 4	USB3.0 Conn	Port 3	NC
Port 4	Camera	Port 5	GPU(TOPAZ)						
Port 5	USB2.0 Conn								
Port 6	Bluetooth								
Port 7	USB HUB								

Function Select

S@	TOPAZ + VRAM
L@	RTD2132N-CG
E@	Internal eDP
V@	RTD2168
N@	NFC
M@	MMB
TS@	Touch screen
WL@	Wireless Dongle

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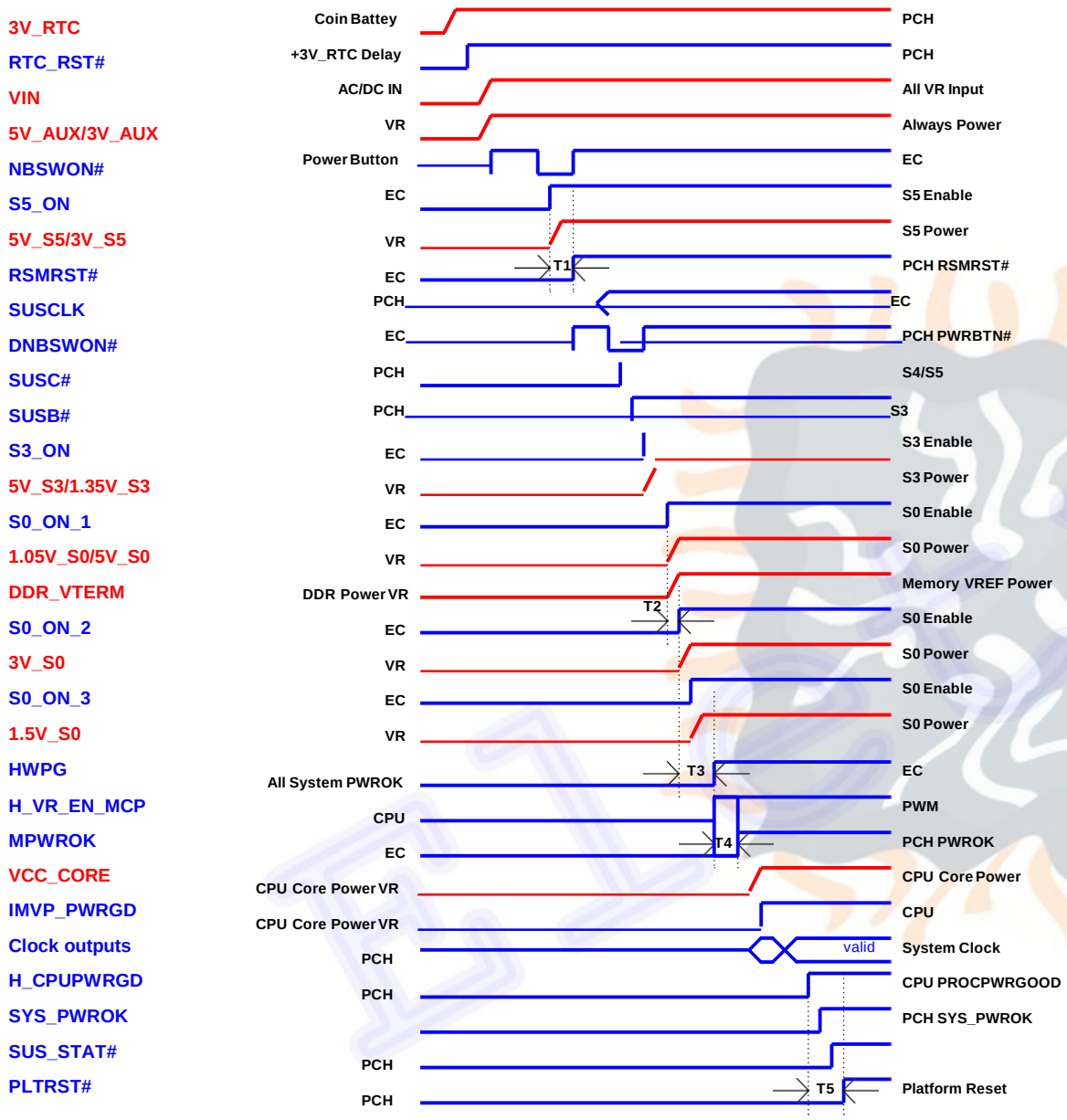
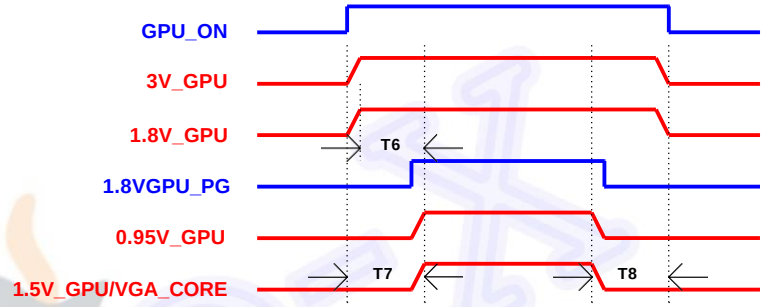
System Power On Sequencing Timing Diagram



System Power Sequence

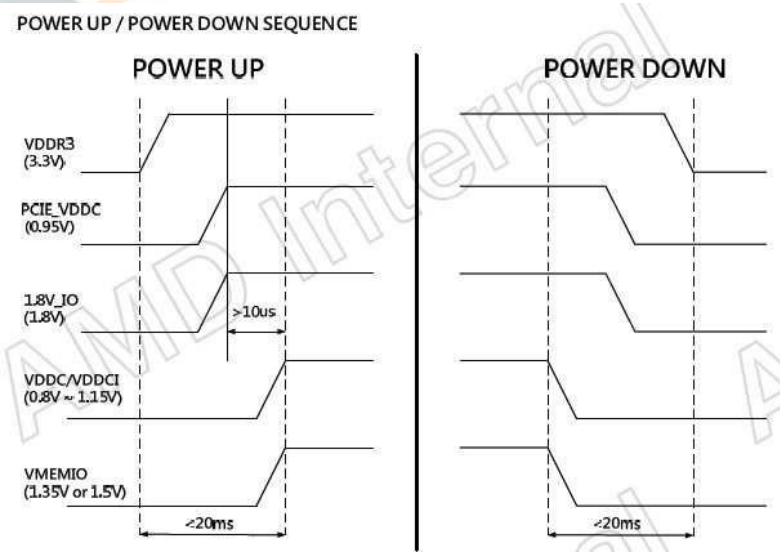
- T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
- T2: S0_ON_1 TO S0_ON_2 = 500us
- T3: S0_ON_2 TO VRON = 10ms
- T4: HWPG TO MPWROK = 110ms (spec：>5~ 99ms)
- T5: H_CPUPWRGD to PLTRST# >1ms

dGPU Power On/Off Sequencing Timing Diagram



dGPU Power Sequence

- T6：1.8V_GPU to 1.5V_GPU > 10us
- T7：3V_GPU to 1.5V_GPU < 20ms
- T8：1.5V_GPU to 3V_GPU < 20ms



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Power Sequence
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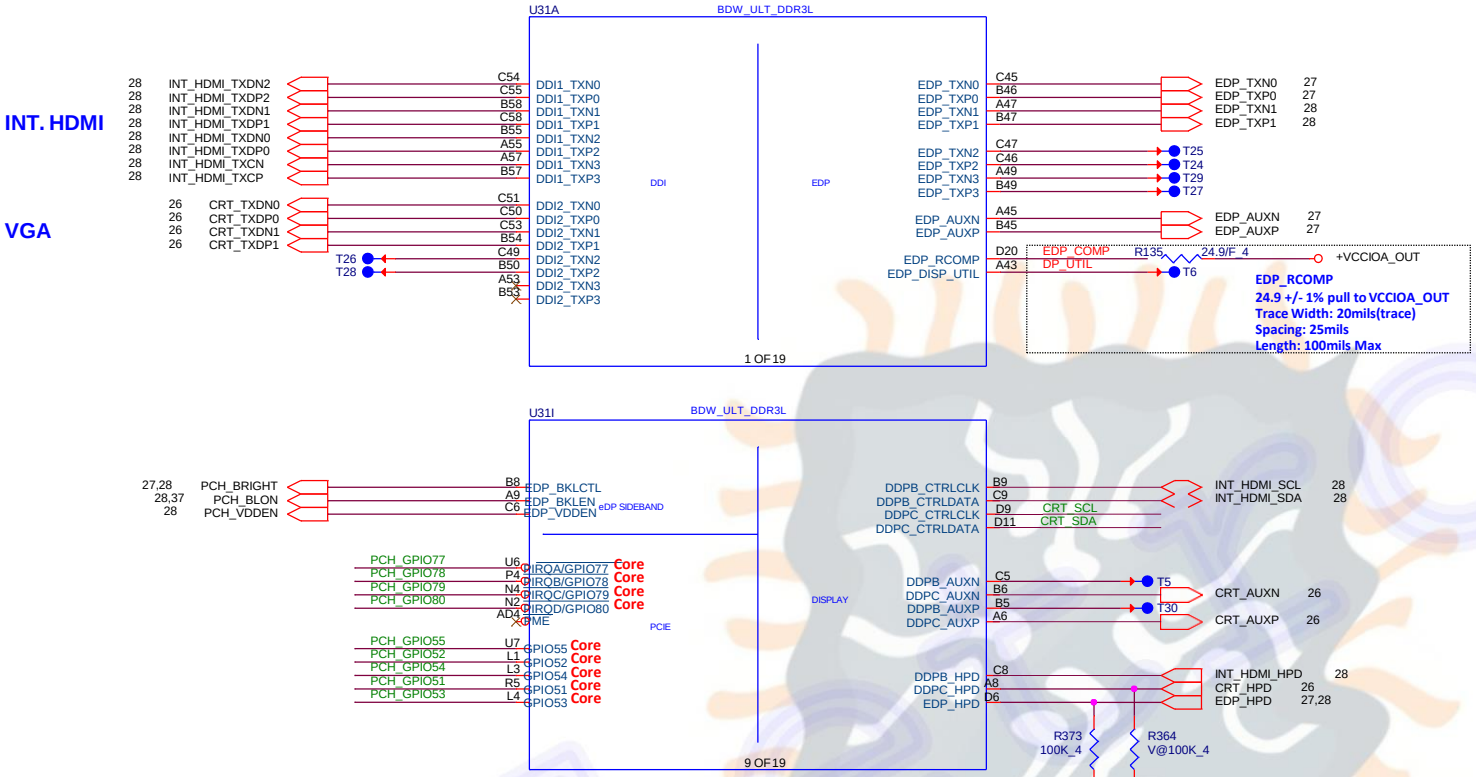
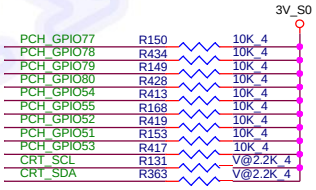
Broadwell Type-U ULT (DISPLAY)



GPIO PU/PD



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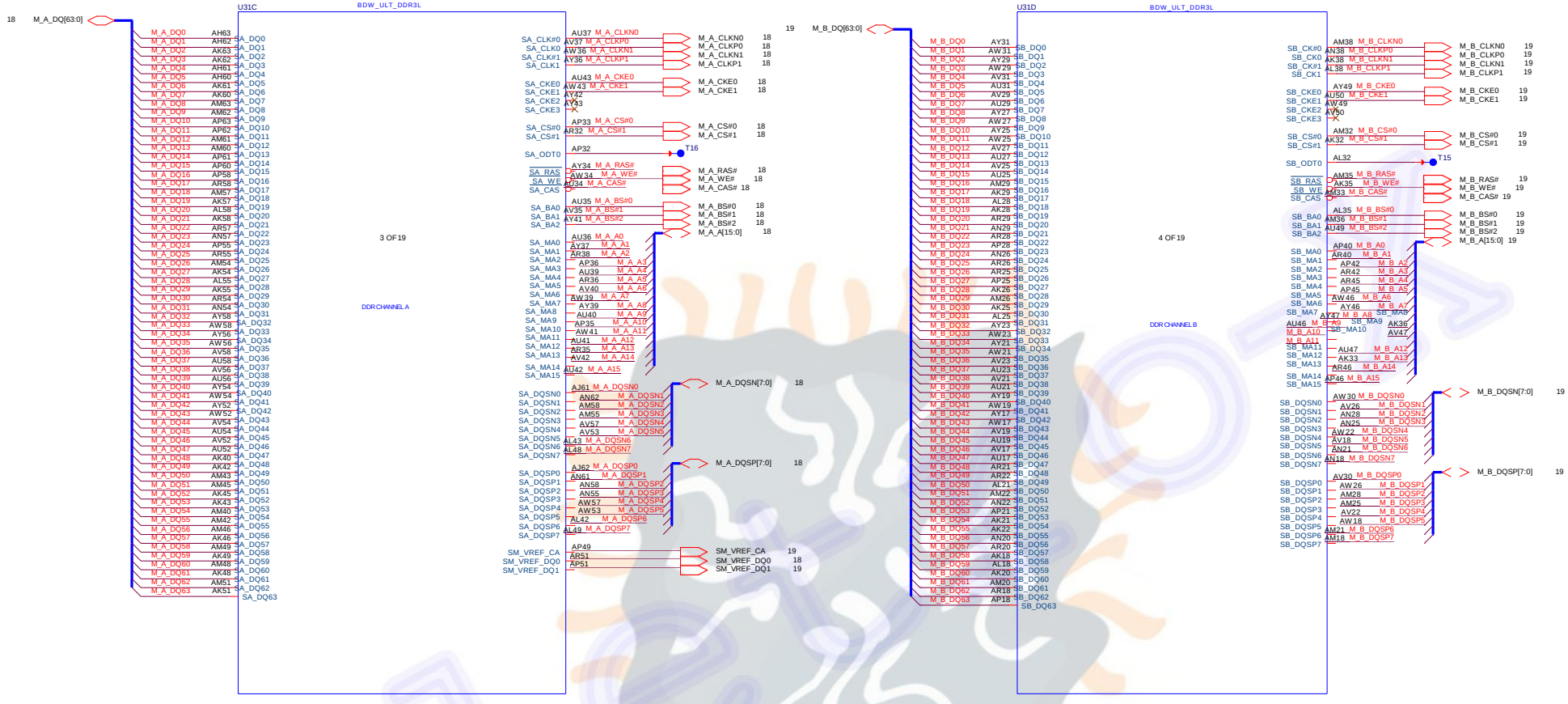
Boardwell Type-U ULT (DDR3L CHA)

Boardwell Type-U ULT (DDR3L CHB)



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	BDW MCP(LPDDR3)	2A
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Broadwell Type-U ULT(GPIO,LPIO,MISC)

08

GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

U31J — BDW_ULT_DDR3L

1.05V_VCCST

R400 1K_4 / R411 1K_4

PCH_THRMTRIP# → Q28 PMBT3904 → S5_ON 37,39

THRMTRIP — RCIN/GPIO82 — SERIRQ — PCH_OPI_RCOMP — RSVD — RSVD

EC_RCIN# 37 → EC_RCIN# → SERIRQ 35,37

PCH_OPIRCOMP — R512 49.9/F_4

PCH_OPI_RCOMP
50 +/- 1% pull to VSS
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max

For GPU use
37,44,45 GPU_PWRGD

PCH_GPIO76 — SMBUSY/GPIO76 — Core
SIO_EXT_SWI# 37 — PCH_GPIO12 — GPIO8 — Sus
PCH_GPIO15 10 — LAN_PHY_PWR_CTRL/GPIO12 — DSW
PCH_GPIO16 — GPIO15 — Sus
GPU_PWRGD — GPIO16 — Core
PCH_GPIO24 — GPIO17 — Core
PCH_GPIO27 — GPIO24 — Sus
NFC_RST# — GPIO27 — DSW
PCH_GPIO26 — GPIO28 — Sus
GPIO26 — Sus

For GPU use
20,37 GPU_RST#_PCH → R583 *0_4 → SIO_EXT_SMI_49 → GPIO48 — Core
37 SIO_EXT_SMI# — SIO_EXT_SCI# 37 — GPIO49 — Core
SIO_EXT_SCI# — GPIO50 — Core
PCH_GPIO71 — SIOPC/GPIO71 — Core
PCH_GPIO13 — GPIO13 — Sus
PCH_GPIO14 — GPIO14 — Sus
PCH_GPIO25 — GPIO25 — DSW
PCH_GPIO45 — GPIO45 — Sus
SIO_EXT_SMI# R584 0_4 — SIO_EXT_SMI#_46 — GPIO46 — Sus
B-34

PCH_GPIO9 — GPIO9 — Sus
PCH_GPIO10 — GPIO10 — Sus
34 NFC_DWL_REQ — R130 N@0_4 — NFC_DWL_REQ_R — DEVSLP0/GPIO33 — Core
PCH_GPIO38 — SDIO_POWER_EN/GPIO70 — Core
PCH_GPIO39 — DEVSLP1/GPIO38 — Core
10,31 ACZ_SPKR — DEVSLP2/GPIO39 — Core
SPKR/GPIO81 — Core

C283 *100P/50V_4

GPIO

10 OF 19 — GPIO

Core: GSPI0_CS/GPIO83, GSPI0_CLK/GPIO84, GSPI0_MISO/GPIO85, GSPI0_MOSI/GPIO86, GSPI1_CS/GPIO87, GSPI1_CLK/GPIO88, GSPI1_MISO/GPIO89, GSPI_MOSI/GPIO90, UART0_RXD/GPIO91, UART0_TXD/GPIO92, UART0_RTS/GPIO93, UART0_CTS/GPIO94, UART1_RXD/GPIO0, UART1_TXD/GPIO1, UART1_RST/GPIO2, UART1_CTS/GPIO3, I2C0_SDA/GPIO4, I2C0_SCL/GPIO5, I2C1_SDA/GPIO6, I2C1_SCL/GPIO7, SDIO_CLK/GPIO64, SDIO_CMD/GPIO65, SDIO_D0/GPIO66, SDIO_D1/GPIO67, SDIO_D2/GPIO68, SDIO_D3/GPIO69

PCH_GPIO83 — GPU_ON_PCH — PCH_GPIO85 → GPU_ON_PCH 20,37 — **For GPU use**
PCH_GPIO87 → BBS 10
PCH_GPIO88, PCH_GPIO89, PCH_GPIO90, PCH_GPIO91, PCH_GPIO92, PCH_GPIO93, PCH_GPIO94, BOARD_ID0, BOARD_ID1, ODD_DM#_PCH → ODD_DM#_PCH 33, BOARD_ID2, BOARD_ID3, PCH_GPIO5, NFC_DETECT# → NFC_DETECT# 34, PCH_GPIO7, PCH_GPIO64, PCH_GPIO65, PCH_GPIO66 → PCH_GPIO66 10, PCH_GPIO67, ODD_PWR_EN → ODD_PWR_EN 33, PCH_GPIO69

Note:
GSPI,UART,I2C and SDIO are only supported on the system that enable Connected Stanby

CPU MISC PU/PD

3V_S0
EC_RCIN# — R183 10K_4
SERIRQ — R161 10K_4

GPIO PU/PD

3V_S5
PCH_GPIO58 R224 10K_4
PCH_GPIO44 R464 10K_4
PCH_GPIO24 R180 10K_4
PCH_GPIO13 R504 10K_4
SIO_EXT_SWI# R493 10K_4
PCH_GPIO56 R211 10K_4
PCH_GPIO45 R202 10K_4
PCH_GPIO9 R468 10K_4
PCH_GPIO14 R217 10K_4
PCH_GPIO59 R510 10K_4

3V_S0
GPU_PWRGD R156 *10K_4
ODD_PWR_EN R387 10K_4
ODD_DM#_PCH R403 10K_4
PCH_GPIO38 R409 10K_4
PCH_GPIO39 R144 10K_4
PCH_GPIO5 R177 10K_4
GPU_RST# PCH R467 *10K_4
GPU_ON_PCH R151 10K_4
PCH_GPIO16 R447 10K_4
SIO_EXT_SCI# R433 10K_4
SIO_EXT_SMI# 49 R450 10K_4
NFC_DETECT# R147 10K_4
PCH_GPIO7 R143 10K_4
NFC_DWL_REQ_R R129 10K_4

3V_S5
PCH_GPIO27 R227 10K_4
PCH_GPIO12 R507 10K_4
PCH_GPIO25 R231 10K_4
PCH_GPIO26 R476 10K_4
PCH_GPIO10 R216 10K_4
PCH_GPIO47 R195 10K_4
SIO_EXT_SMI# 46 R191 10K_4

3V_S0
PCH_GPIO88 1 2
PCH_GPIO85 3 4
PCH_GPIO87 5 6
PCH_GPIO83 7 8
RN2 10KX4
PCH_GPIO89 1 2
PCH_GPIO90 3 4
PCH_GPIO91 5 6
PCH_GPIO92 7 8
RN4 10KX4
PCH_GPIO71 1 2
PCH_GPIO64 3 4
PCH_GPIO93 5 6
PCH_GPIO94 7 8
RN1 10KX4
PCH_GPIO76 1 2
PCH_GPIO67 3 4
PCH_GPIO69 5 6
PCH_GPIO65 7 8
RN3 10KX4

Board ID:

3V_S0 ×4
R393 *10K_4 — BOARD_ID0
R408 *10K_4 — BOARD_ID1
R397 *10K_4 — BOARD_ID2
R157 *10K_4 — BOARD_ID3
R394 10K_4
R415 10K_4
R399 10K_4
R155 10K_4

BOARD_ID0	PCH_GPIO0
UMA	0
DIS	1

BOARD_ID1	PCH_GPIO1
LVDS	0
eDP	1

BOARD_ID2	PCH_GPIO3
VGA	0
Non-VGA	1

BOARD_ID3	PCH_GPIO4
TOUCH	0
Non-TOUCH	1

3V_S0 — S@0.1U/10V_4_X7R_C263
44 GPU_PWRGD_SVID_REG → U10 S@TC7SH08FU(F) → GPU_PWRGD, PLTRST# → PLTRST# 12,20,29,30,34,35,37

3V_S0 — U15 *N@TC7SH08FU
34 NFC_RST_BUFF# → PLTRST# → NFC_RST# → R275 100K_4
R277 N@0_4

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Broadwell Type-U ULT (PCIE,USB)

09

For GPU use

TOPAZ

WLAN(NGFF)

GLAN

Card Reader

USB3.0

U31K

BDW_ULT_DDR3L

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PCIE

USB

USB debug port

PEG_RXN0 / PEG_RXP0 → F10 / E10 PERN5_L0 / PERP5_L0
PEG_TXN0 / PEG_TXP0 → C141 / C152 0.1uF/16V/X7R_4 → PEG_TXN0_C / PEG_TXP0_C → C23 / C22 PETN5_L0 / PETP5_L0
PEG_RXN1 / PEG_RXP1 → F8 / E8 PERN5_L1 / PERP5_L1
PEG_TXN1 / PEG_TXP1 → C131 / C138 0.1uF/16V/X7R_4 → PEG_TXN1_C / PEG_TXP1_C → B23 / A23 PETN5_L1 / PETP5_L1
PEG_RXN2 / PEG_RXP2 → H10 / G10 PERN5_L2 / PERP5_L2
PEG_TXN2 / PEG_TXP2 → C166 / C170 0.1uF/16V/X7R_4 → PEG_TXN2_C / PEG_TXP2_C → B21 / C21 PETN5_L2 / PETP5_L2
PEG_RXN3 / PEG_RXP3 → E6 / F6 PERN5_L3 / PERP5_L3
PEG_TXN3 / PEG_TXP3 → C156 / C164 0.1uF/16V/X7R_4 → PEG_TXN3_C / PEG_TXP3_C → B22 / A21 PETN5_L3 / PETP5_L3

PCIE_RXN_WLAN / PCIE_RXP_WLAN → G11 / F11 PERN3 / PERP3
PCIE_TXN_WLAN / PCIE_TXP_WLAN → C466 / C467 0.1uF/16V/X7R_4 → PCIE_TXN_WLAN_C / PCIE_TXP_WLAN_C → C29 / B30 PETN3 / PETP3
PCIE_RXN_LAN / PCIE_RXP_LAN → F13 / G13 PERN4 / PERP4
PCIE_TXN_LAN / PCIE_TXP_LAN → C468 / C469 0.1uF/16V/X7R_4 → PCIE_TXN_LAN_C / PCIE_TXP_LAN_C → B29 / A29 PETN4 / PETP4
PCIE_RXN_CARD / PCIE_RXP_CARD → G17 / F17 PERN1/USB3RN3 / PERP1/USB3RP3
PCIE_TXN_CARD / PCIE_TXP_CARD → C465 / C471 0.1uF/16V/X7R_4 → PCIE_TXN_CARD_C / PCIE_TXP_CARD_C → C30 / C31 PETN1/USB3TN3 / PETP1/USB3TP3
USB3_RXN4 / USB3_RXP4 → F15 / G15 PERN2/USB3RN4 / PERP2/USB3RP4
USB3_TXN4 / USB3_TXP4 → B31 / A31 PETN2/USB3TN4 / PETP2/USB3TP4

+V1.05S_AUSB3PLL
R117 3K/F_4 PCIE_RCOMP
R120 SHORT_4 PCIE_IREF
B-9

PCIE_RCOMP
3K+/- 1% pull to VCCUSB3PLL
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max

PCIE_IREF
Directly connect to VCCUSB3PLL
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max

E15 RSVD
E12 RSVD
A27 RSVD
B27 PCIE_RCOMP
PCIE_IREF

USB2N0 / USB2P0 → AN8 / AM8 → USBP0- / USBP0+ → 32 / 32 — USB2.0 Port (Co-lay USB3.0)
USB2N1 / USB2P1 → AR7 / AT7 → USBP1- / USBP1+ → 32 / 32 — USB2.0 Port (Co-lay USB3.0)
USB2N2 / USB2P2 → AR8 / AP8 → USBP2- / USBP2+ → 32 / 32 — USB2.0 Port (Co-lay USB3.0)
USB2N3 / USB2P3 → AR10 / AT10 → USB_TS# / USB_TS → 35 / 35 — Touch screen
USB2N4 / USB2P4 → AM15 / AL15 → USB_C# / USB_C → 28 / 28 — Camera
USB2N5 / USB2P5 → AM13 / AN13 → USB_BT# / USB_BT → 34 / 34 — Bluetooth
USB2N6 / USB2P6 → AP11 / AN11 → USB_Conn# / USB_Conn → 32 / 32 — USB2.0 Port
USB2N7 / USB2P7 → AR13 / AP13 → USB_WL# / USB_WL → 36 / 36 — Wireless Dongle

USB3RN1 / USB3RP1 → G20 USB3_RXN1 / H20 USB3_RXP1 → USB3_RXN1 / USB3_RXP1 → 32 / 32
USB3TN1 / USB3TP1 → C33 USB3_TXN1 / B34 USB3_TXP1 → USB3_TXN1 / USB3_TXP1 → 32 / 32 — USB3.0
USB3RN2 / USB3RP2 → E18 USB3_RXN2 / F18 USB3_RXP2 → USB3_RXN2 / USB3_RXP2 → 32 / 32
USB3TN2 / USB3TP2 → B33 USB3_TXN2 / A33 USB3_TXP2 → USB3_TXN2 / USB3_TXP2 → 32 / 32 — USB3.0

USBRBIAS / USBRBIAS → AJ10 / AJ11 USB_BIAS → R198 22.6/F_4
RSVD → AN10
RSVD → AM10

USBBIAS & USBBIAS#
Short the USBRBIAS and the USBRBIAS# pins and one end of 22.6 +/- 1% to GND
Route signal using 50 ohm single-ended impedance
Spacing: 15mils
Length: 500mils Max

Sus OC0/GPIO40 → AL3 USB_OC0# → USB_OC0# → 32
Sus OC1/GPIO41 → AT1 USB_OC1#
Sus OC2/GPIO42 → AH2 → MOUSE_ON → 36
Sus OC3/GPIO43 → AV3 USB_OC3#

3V_S5
USB_OC3# R233 10K_4
USB_OC0# R469 10K_4
USB_OC1# R230 10K_4

Quanta Computer Inc.
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	BDW PCH(PCIE/USB)	2A
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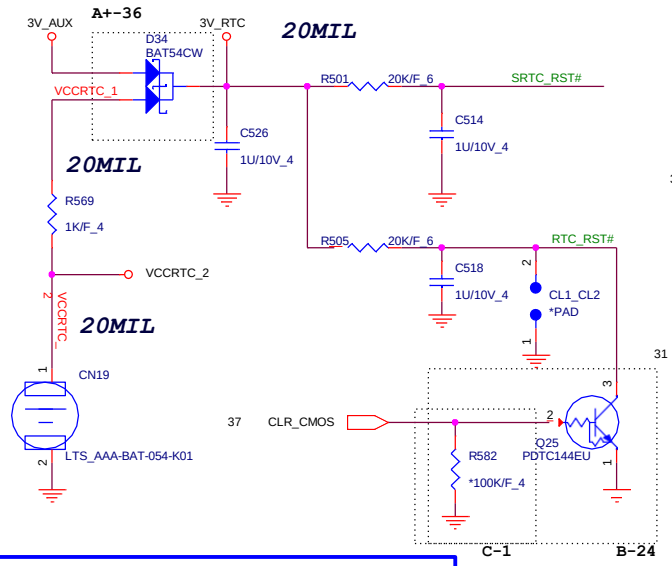
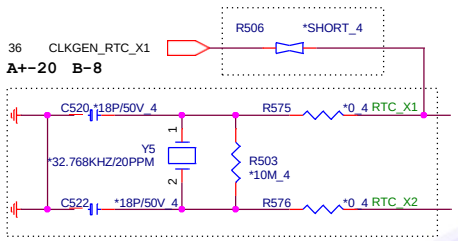
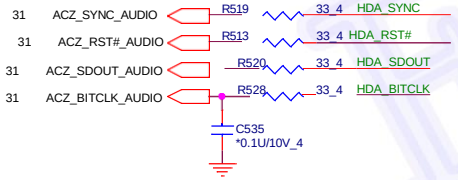
RTC Circuitry(RTC)



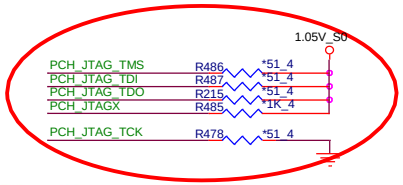
RTC XTAL 32.768KHz



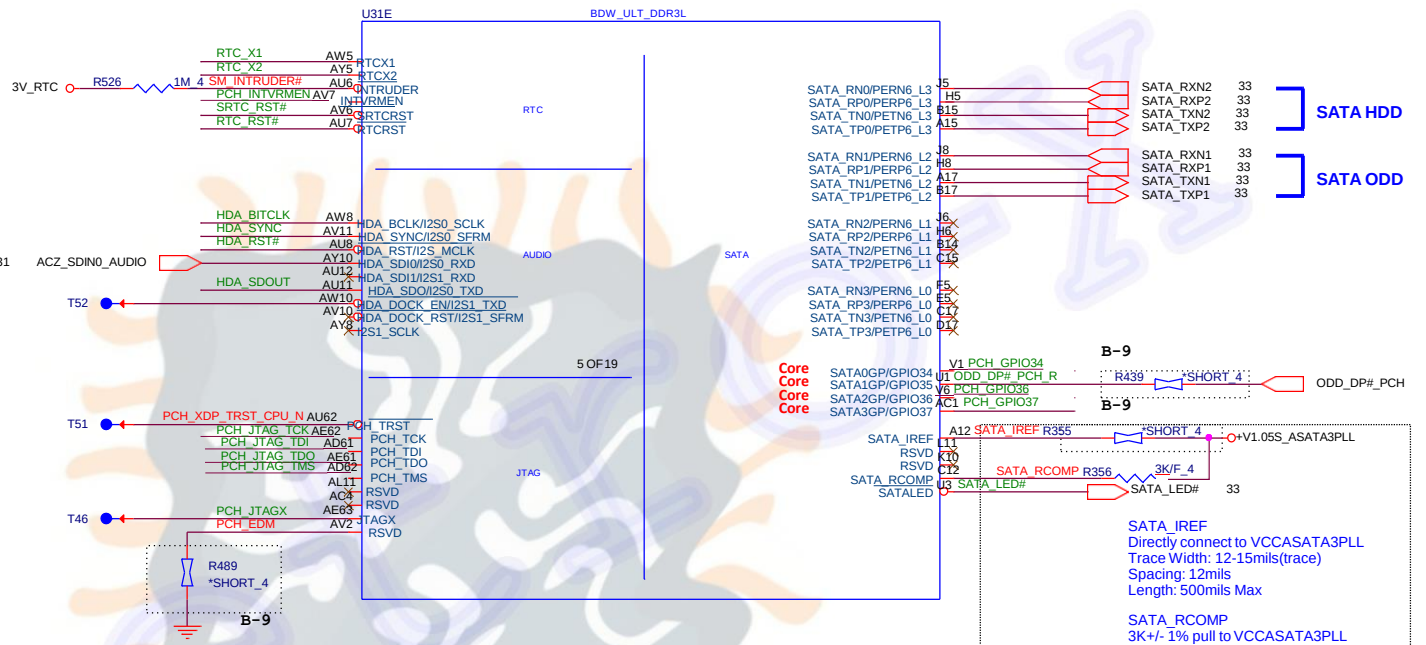
HDA Audio (CLG)

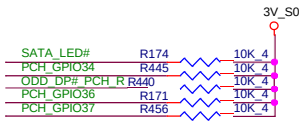


PCH JTAG Debug (CLG)



Broadwell Type-U ULT (RTC,HDA,JTAG,SATA)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Schematic
HDA_SDO/I2S0_TXD	Flash Descriptor Security Override	PWROK	0 = Enable Flash Descriptor security. (Int PD) 1 = Disable Flash Descriptor Security	3V_S5 R518 *1K_4 HDA_SDOUT 37
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = DCPSUSx are powered from an ext. power source 1 = Integrated VRM enabled (330K PU VccRTC)	3V_RTC R515 330K_4 PCH_INTVRMEN R517 *330K_4
DSWVRMEN	DeepSx Well On-Die VRM Enable	ALWAYS	0 = Disable Integrated DSW On-Die VRM 1 = Enable Integrated DSW On-Die VRM (Must be PU)	3V_RTC R514 330K_4 DSW VRMEN 12
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable Intel ME Crypto TLS cipher suite (Int PD) 1 = Enable Intel ME Crypto Transport	8 PCH_GPIO15 3V_S5 R197 8.2K_4 R200 *1K_4
SPKR/GPIO81	No reboot mode setting	PWROK	0 = Disable No Reboot mode (Int PD). 1 = Enable No Reboot mode.	3V_S0 R181 *1K_4 ACZ_SPKR 8,31
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit	PWROK	0 = Boot from SPI 1 = Boot from LPC	3V_S0 R392 *1K_4 R396 *1K_4 BBS 8
SDIO_D0/GPIO66	Top Swap Override	PWROK	0 = Disable Top Swap mode. (Int PD) 1 = Enable Top Swap mode.	+V3.3S_1.8S_LPSS_SDIO R391 *1K_4 R389 1K_4 PCH_GPIO66 8

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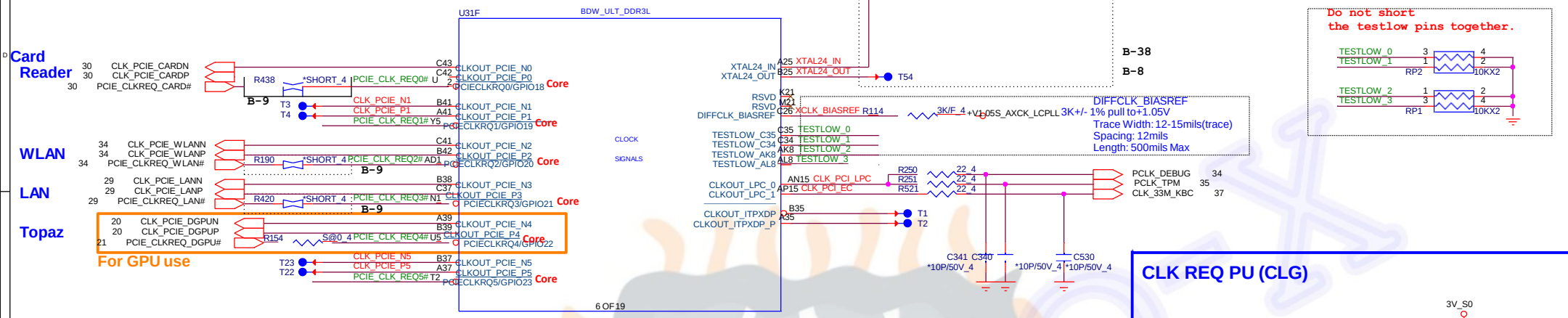
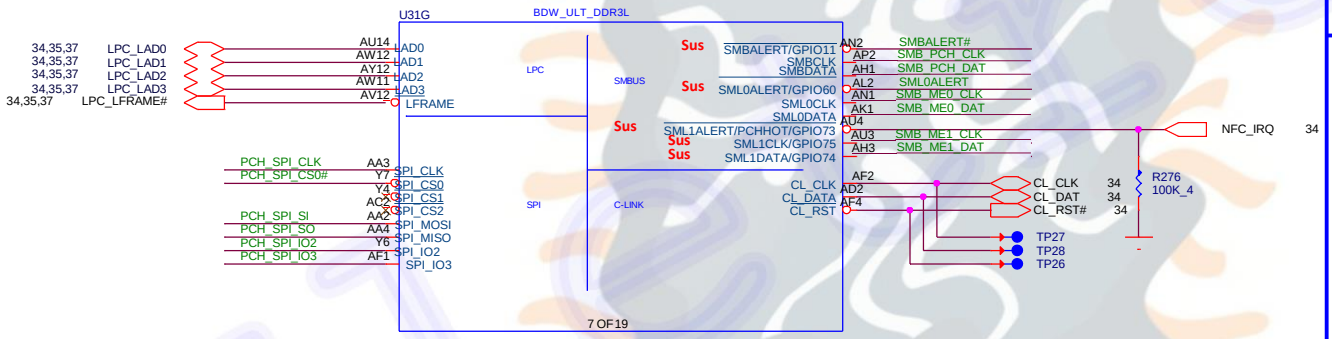
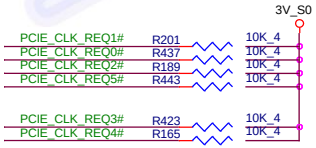
Broadwell Type-U ULT (CLK)



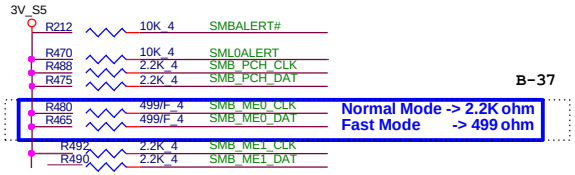
Broadwell Type-U ULT (LPC/SPI/SMB/CLINK)



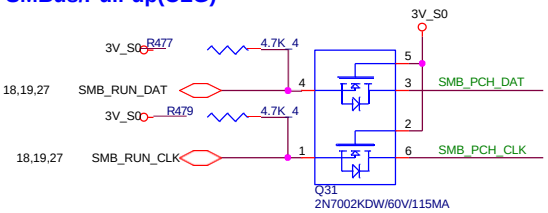
CLK REQ PU (CLG)



SMBus



SMBus/Pull-up(CLG)

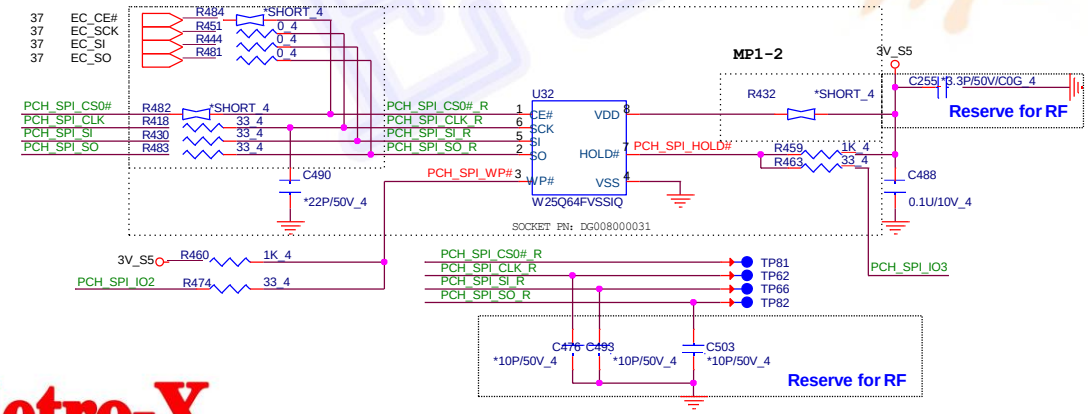


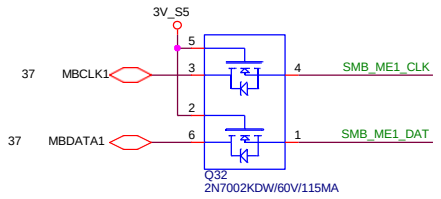
PCH Dual SPI

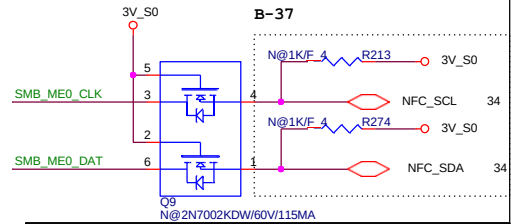
EC & BIOS & ME F/W ROM 8MB B-69

B-25 B-9

Use one 33-Ω series-resistor per device if using two SPI devices.
15-Ω series resistor required if a single device is used.







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	BDW PCH(CLK/LPC/SPI/SMB)	2A
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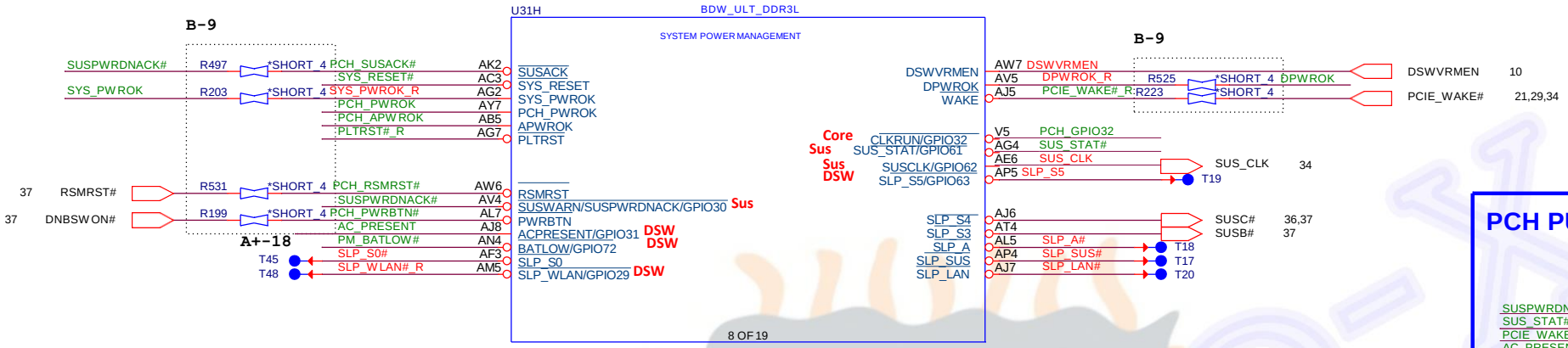
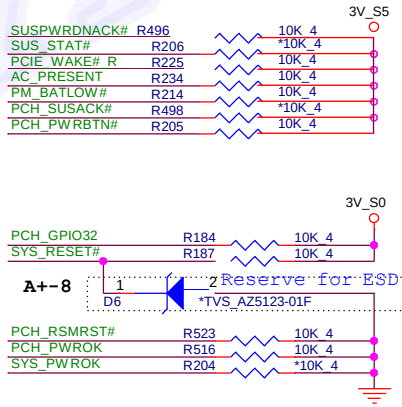
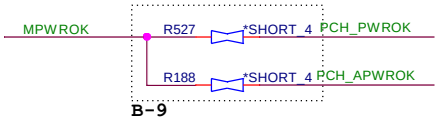
Broadwell U-Type ULT (SYSTEM POWER MANAGEMENT)



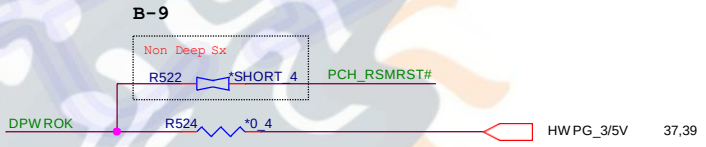
PCH PU/PD (CLG)



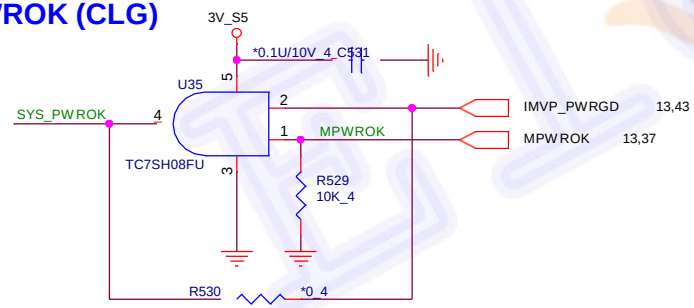
PCH PWROK (CLG)



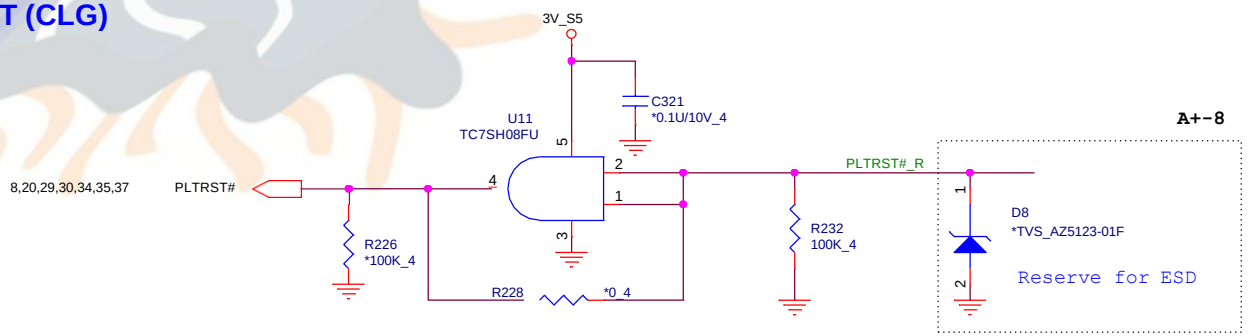
DSW Circuit



SYS PWROK (CLG)



PLTRST (CLG)



Quanta Computer Inc.

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	BDW PCH(PWR MANAGEMENT)	2A
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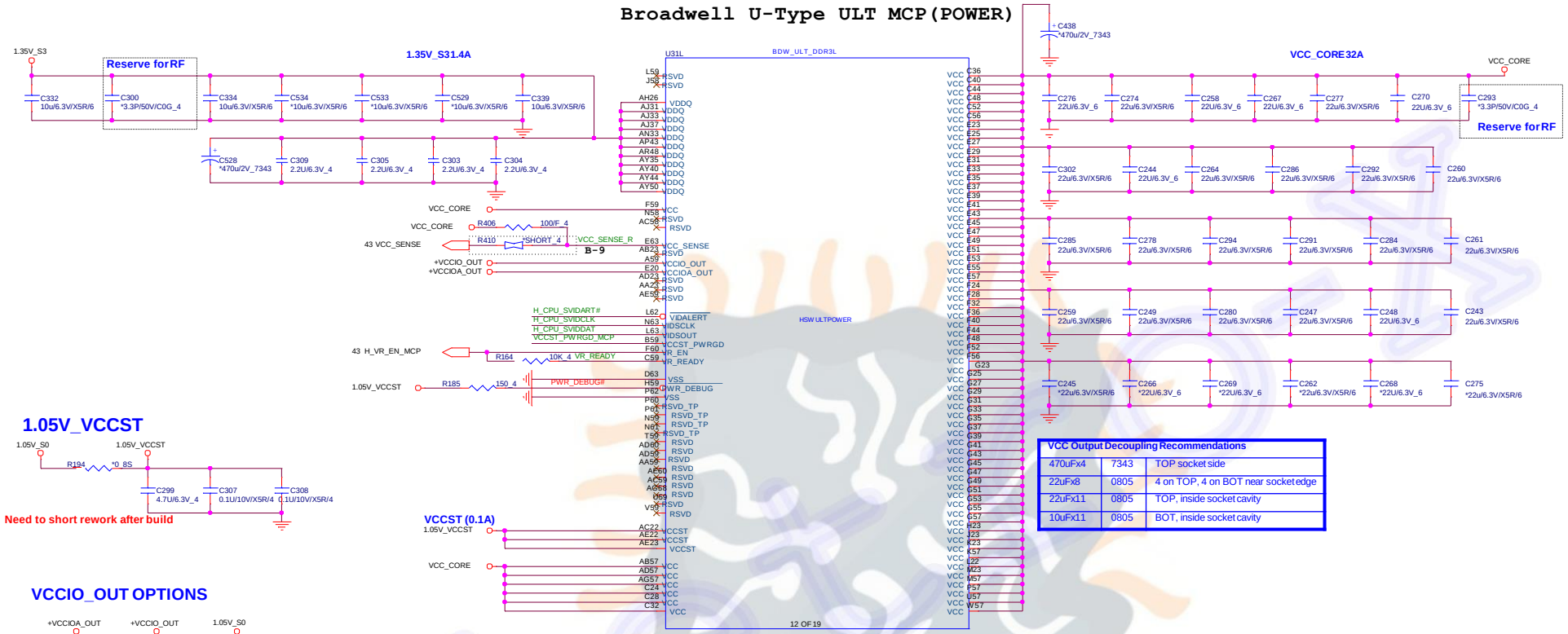
VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

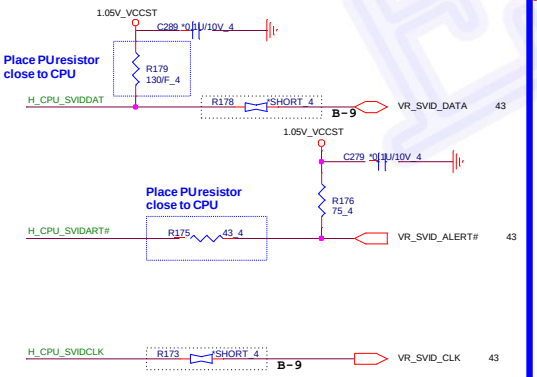
Broadwell U-Type ULT MCP(POWER)

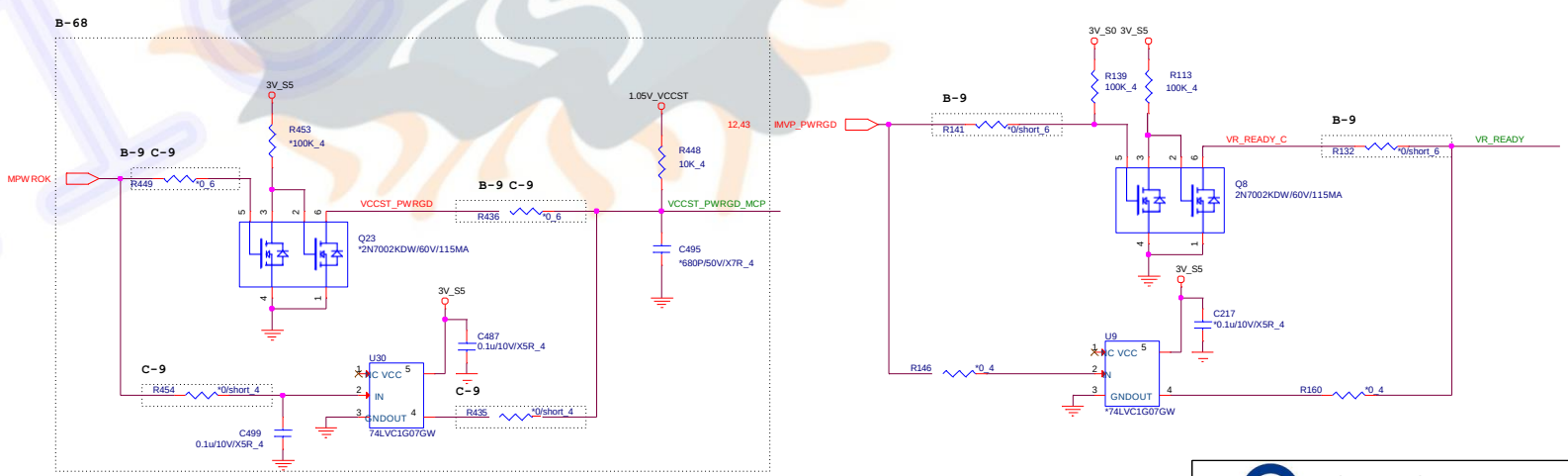


VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

SVID

Layout note: need routing together and ALERT need between CLK and DATA.





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	BDW MCP(POWER)	
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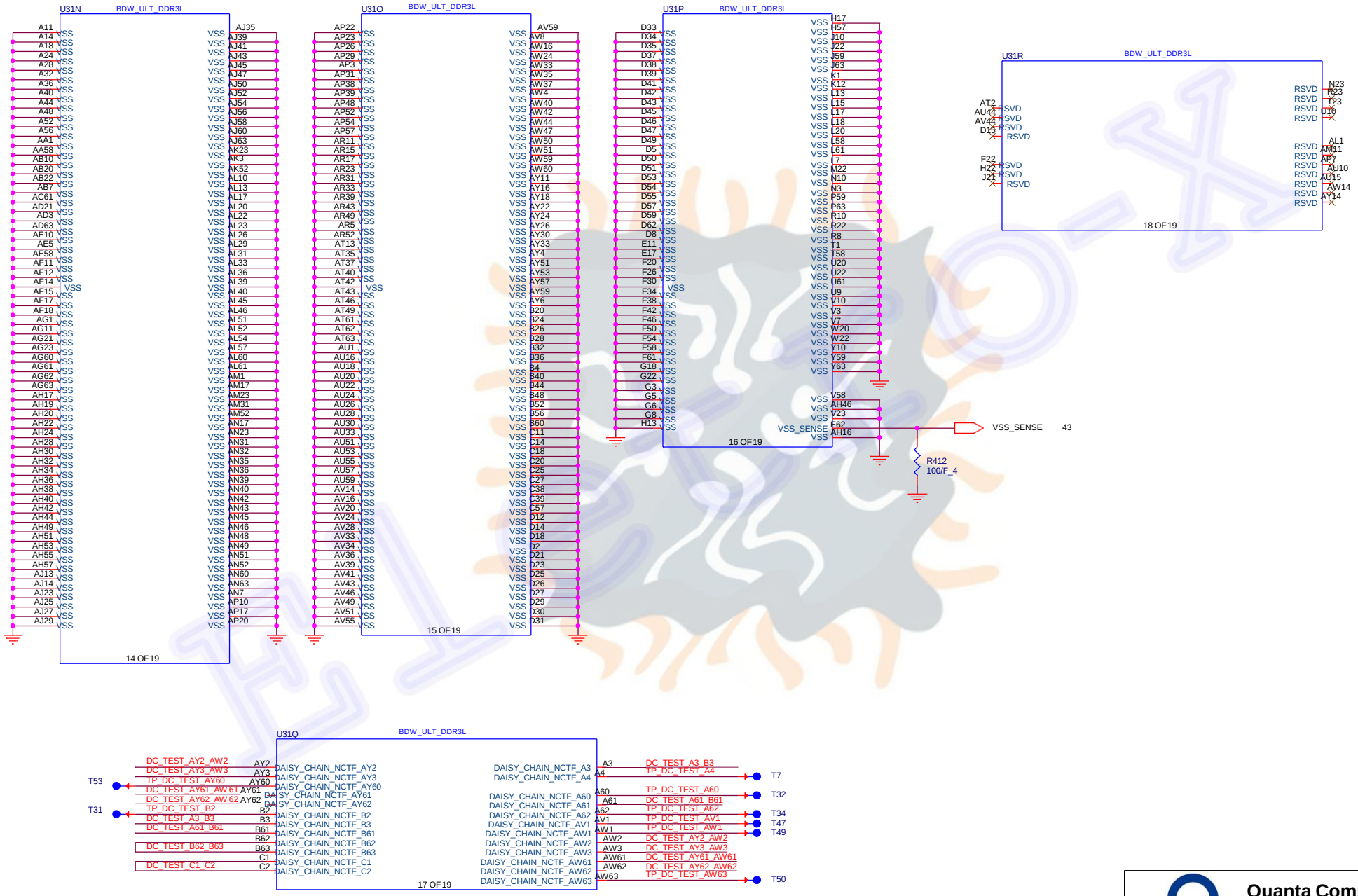
Broadwell U-Type ULT (RSVD,GND)



Quanta Computer Inc.

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	BDW MCP(GND/DAISY/RSVD)	2U
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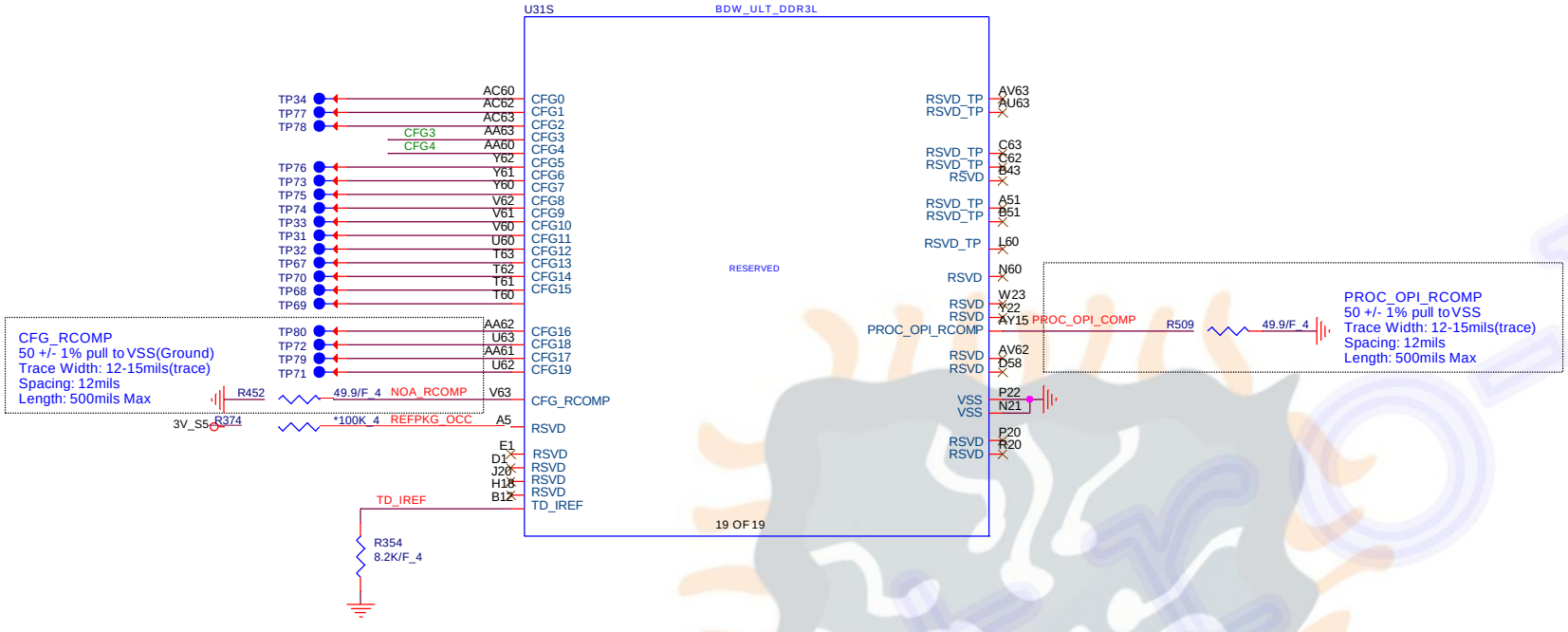
Broadwell U-Type ULT PCH (CFG)



Processor Strapping

	1	0	
CFG3 **MSR Privacy Bit Feature**	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R471 *1K_4
CFG4 **eDP Enable**	DISABLED	ENABLED	CFG4 R210 1K_4

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	BDW MCP(CFG)	2A
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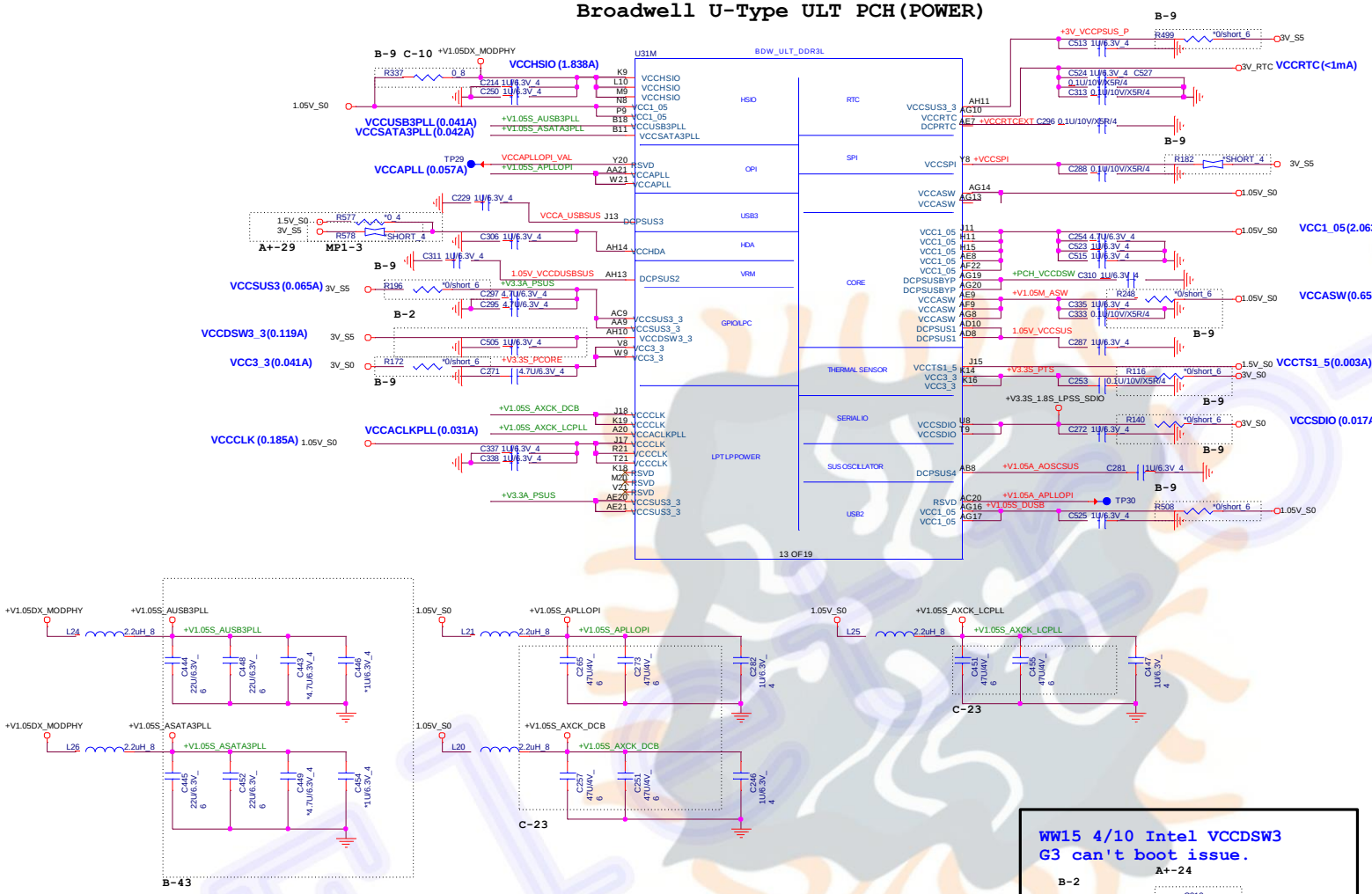
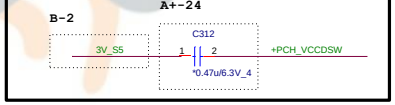
Broadwell U-Type ULT PCH(POWER)



WW15 4/10 Intel VCCDSW3 G3 can't boot issue.



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	BDW PCH(POWER)	2A

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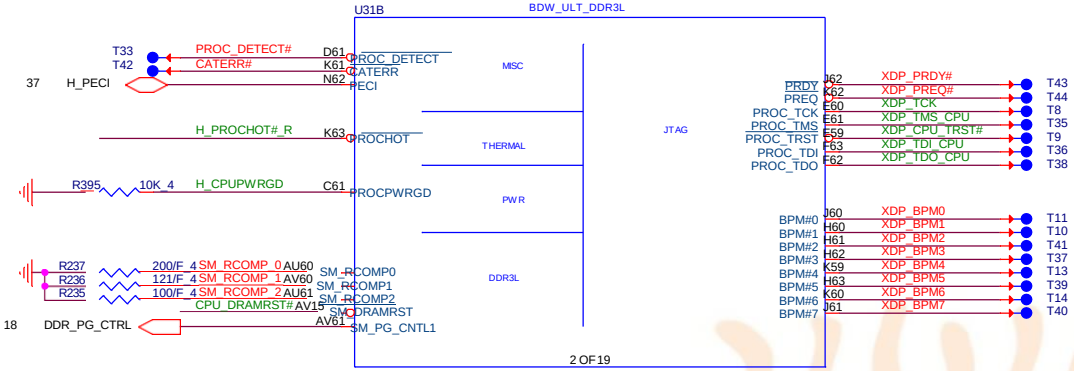
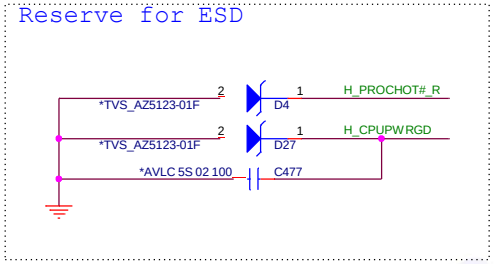
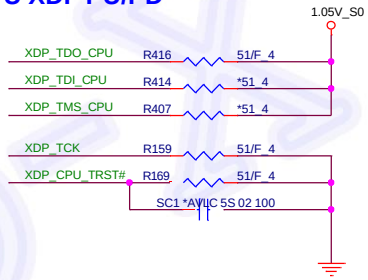
Broadwell U-Type ULT MCP(SIDEBAND)



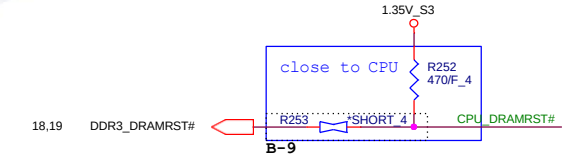
A+-8



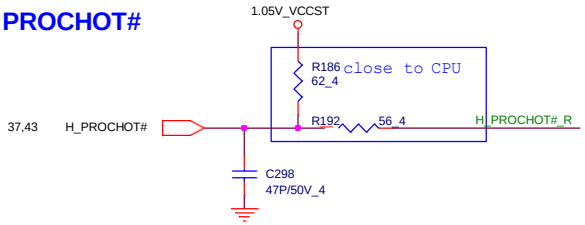
CPU XDP PU/PD



SM_DRAMRST#



PROCHOT#



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	BDW MCP(SIDEBAND)	2A
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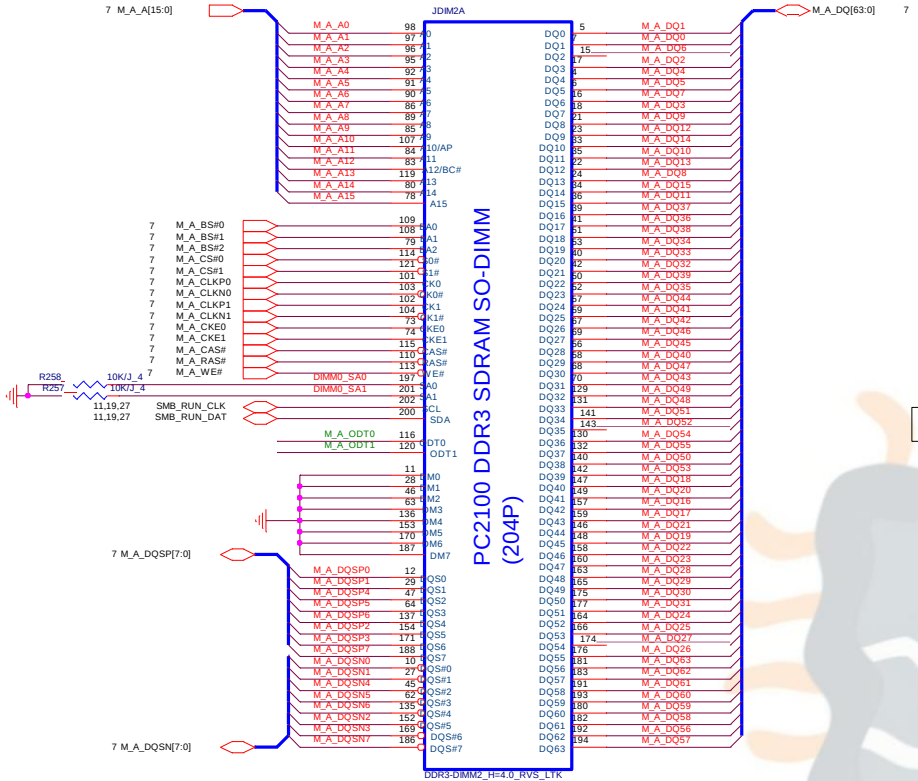
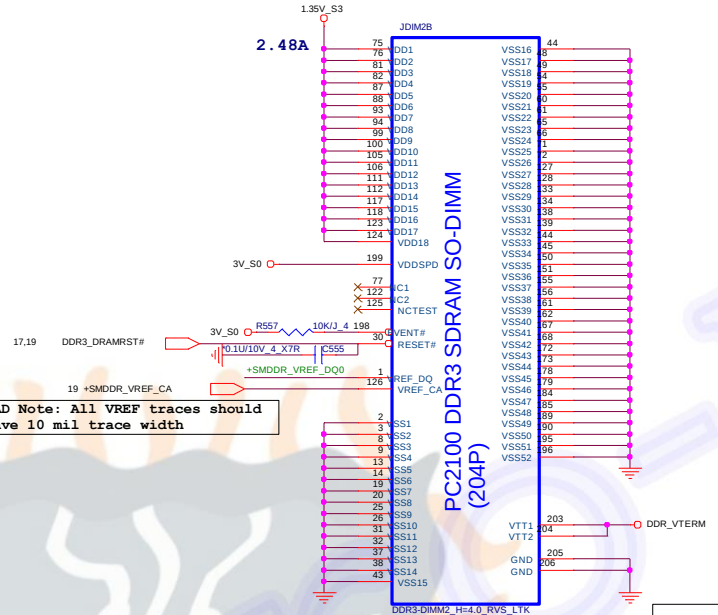
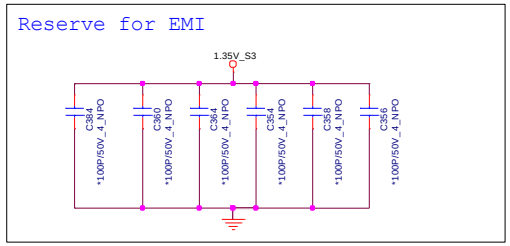
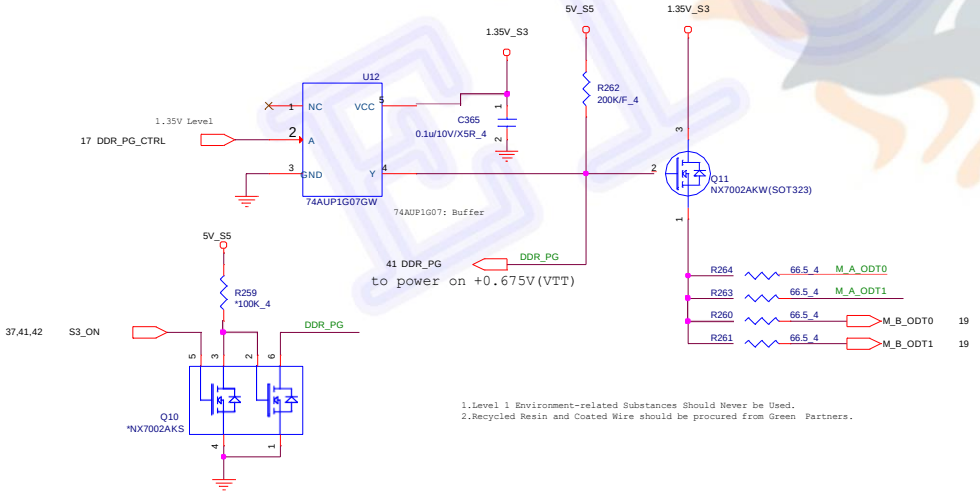
DDR_RVS (DDR)



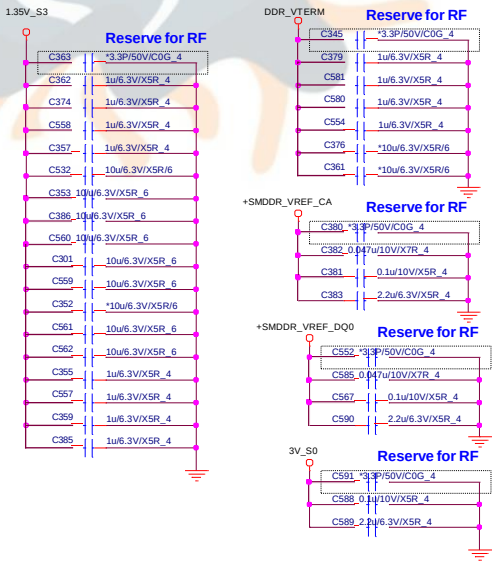




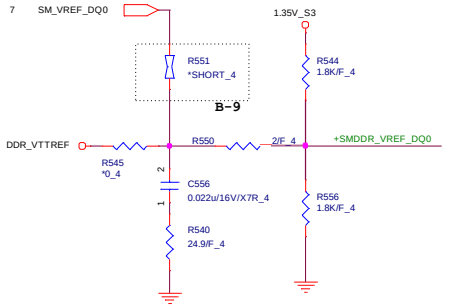
DDR3L SODIMM ODT GENERATION



Place these Caps near So-Dimm0.



VREF DQ0 M1/M3 Solution



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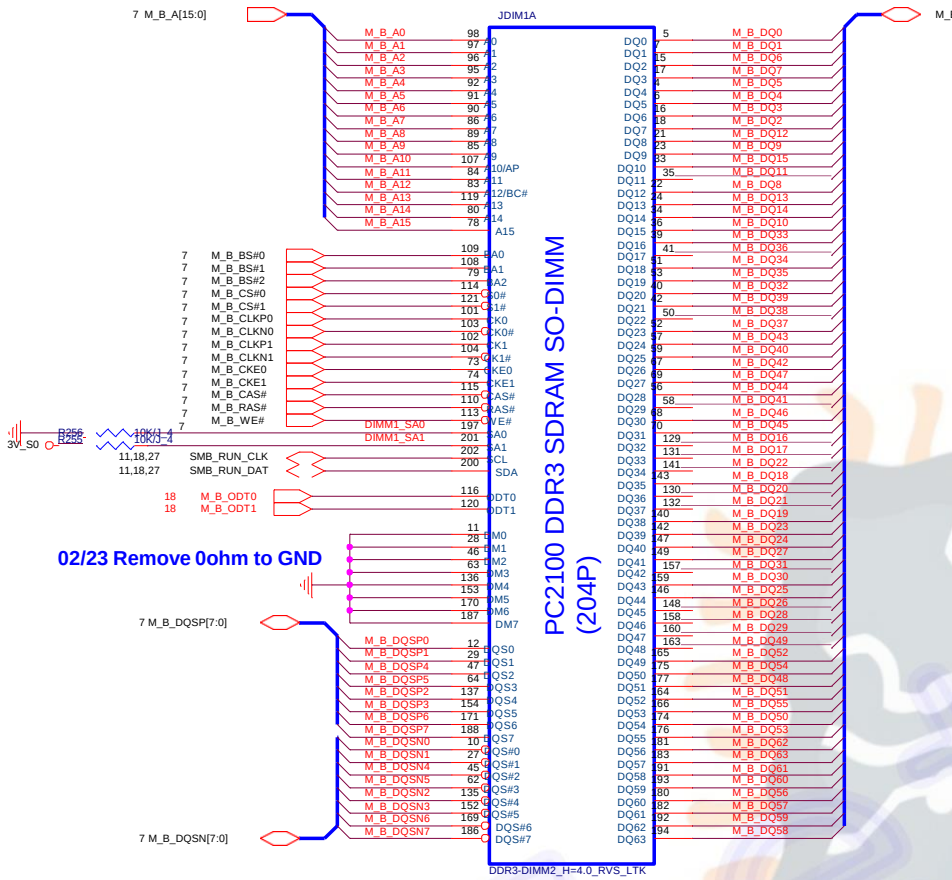
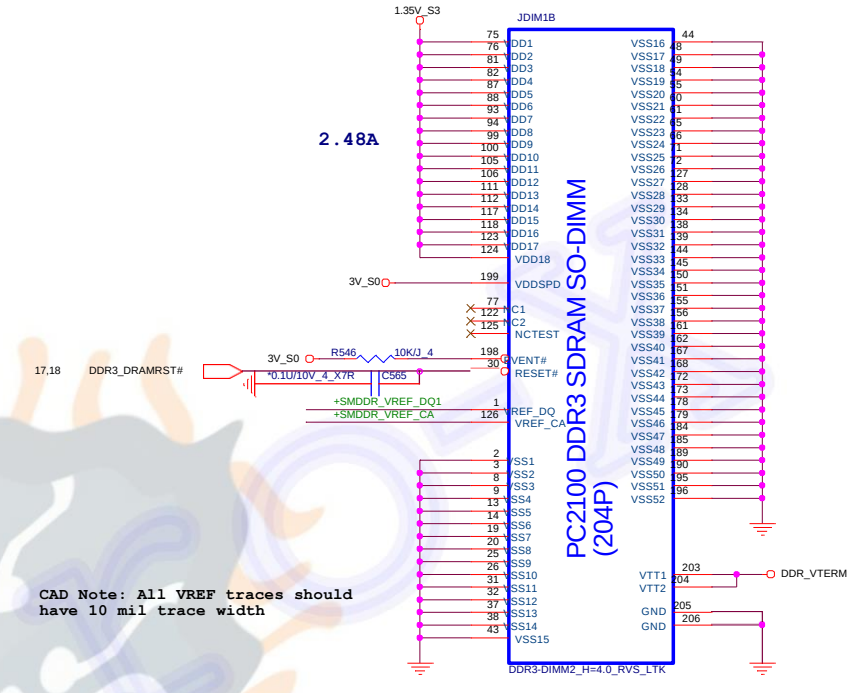
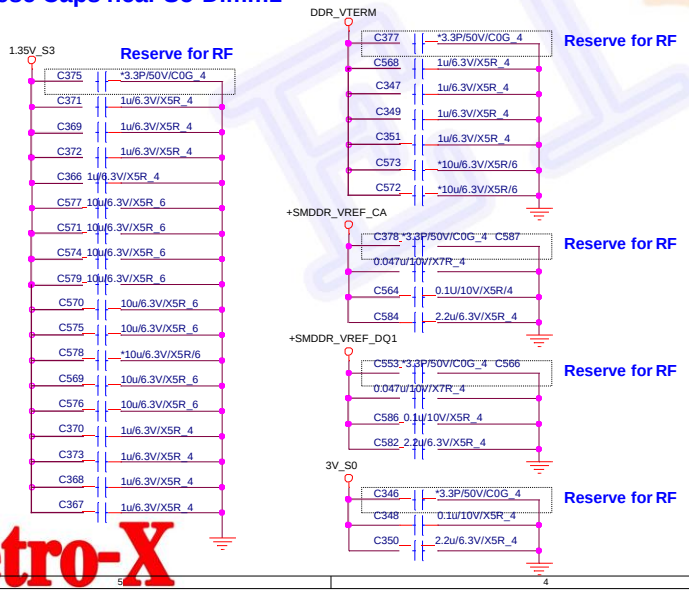
Eletro-X

DDR_RVS (DDR)

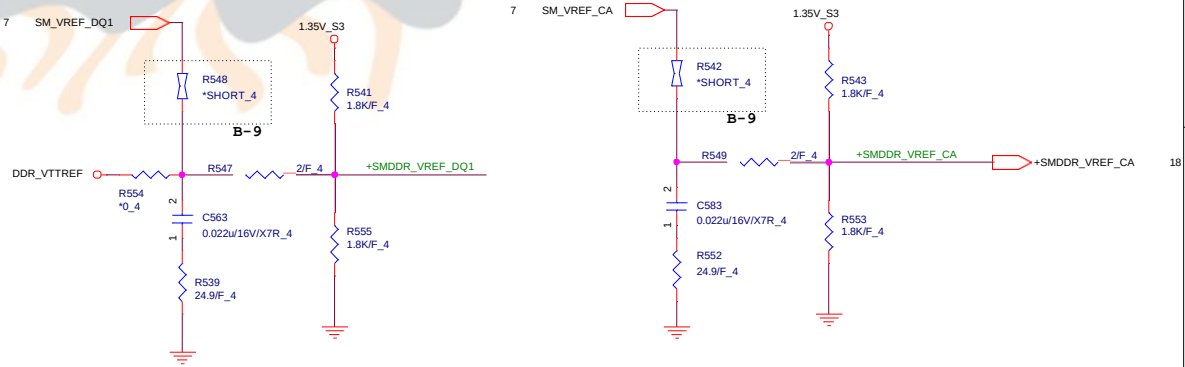




Place these Caps near So-Dimm1



VREF DQ1 Solution



1.Level 1 Environment-related Substances Should Never be Used. 2.Recycled Resin and Coated Wire should be procured from Green Partners.

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	DDR3L DIMM-2-RVS(H4.0)	2A
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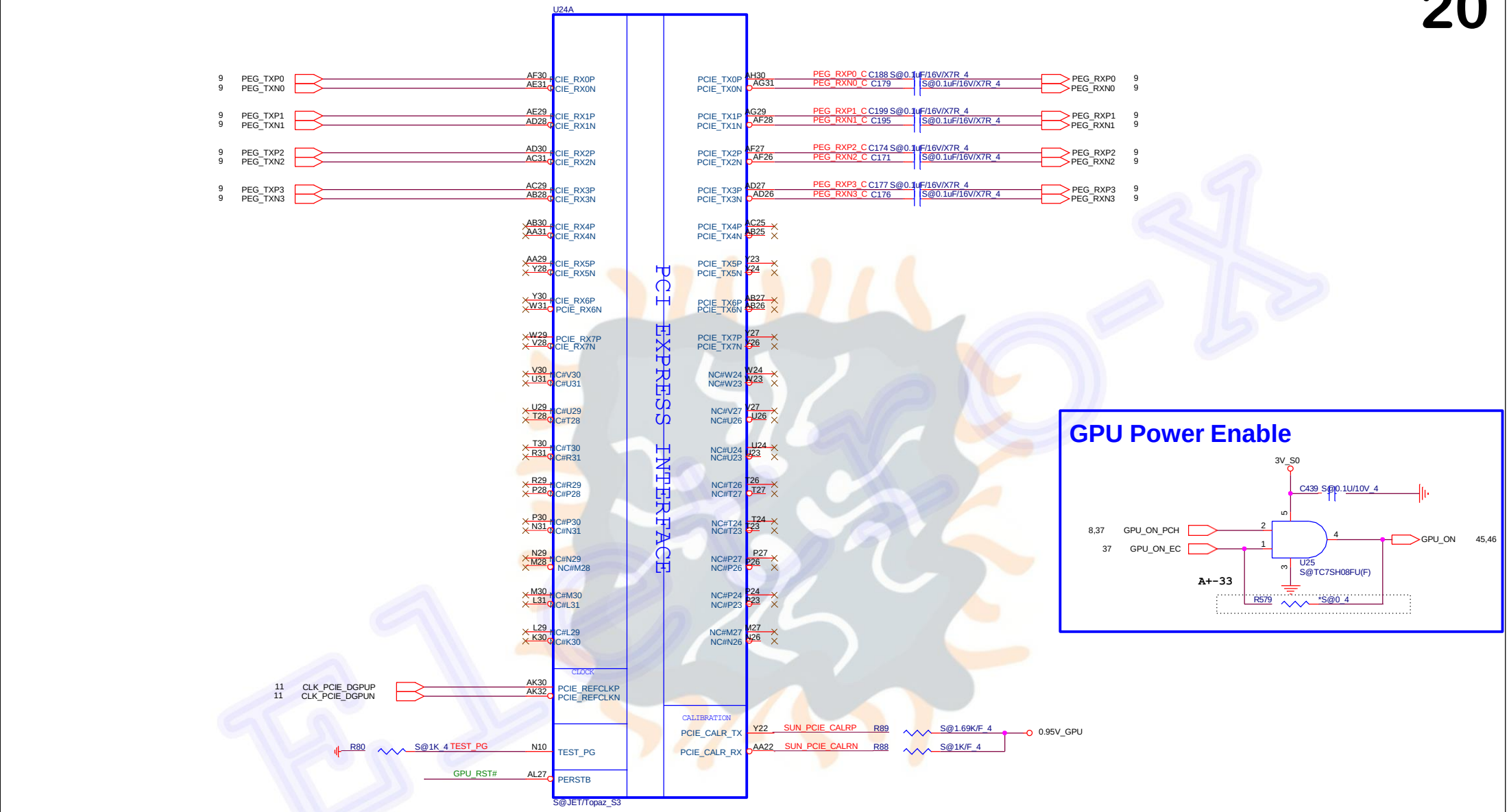
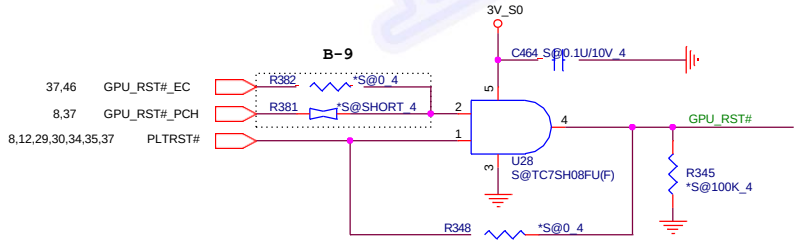


GPU Power Enable



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Rev
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GPU PU/PD

X'tal 27MHz

Reserve for Power Play

Thermal from EC

PS_3[3:1]	Vendor	Type	Vendor P/N	Quanta P/N	R375	R376	C472
000	Hynix	256Mx16 *4	H5TC4G63AFR-11C	AKD5PGWTW20	NC	4.75K	NC
001	Samsung	256Mx16 *4	K4W4G1646D-BC11	AKD5PGST513	8.45K	2K	NC

PS	R_pu	R_pd	C
	R350	R362	C458
PS_0	8.45K	2K	NC

PS	R_pu	R_pd	C
	R365	R366	C459
PS_1	NC	4.75K	NC

PS	R_pu	R_pd	C
	R351	R369	C463
PS_2	NC	4.75K	NC

PS	R_pu	R_pd	C
	R375	R376	C472
PS_3	NC	4.75K	NC

BIT5 => BIT0

PS0 => 11001

PS1 => 11000

PS2 => 11000

PS3 => 11xxx

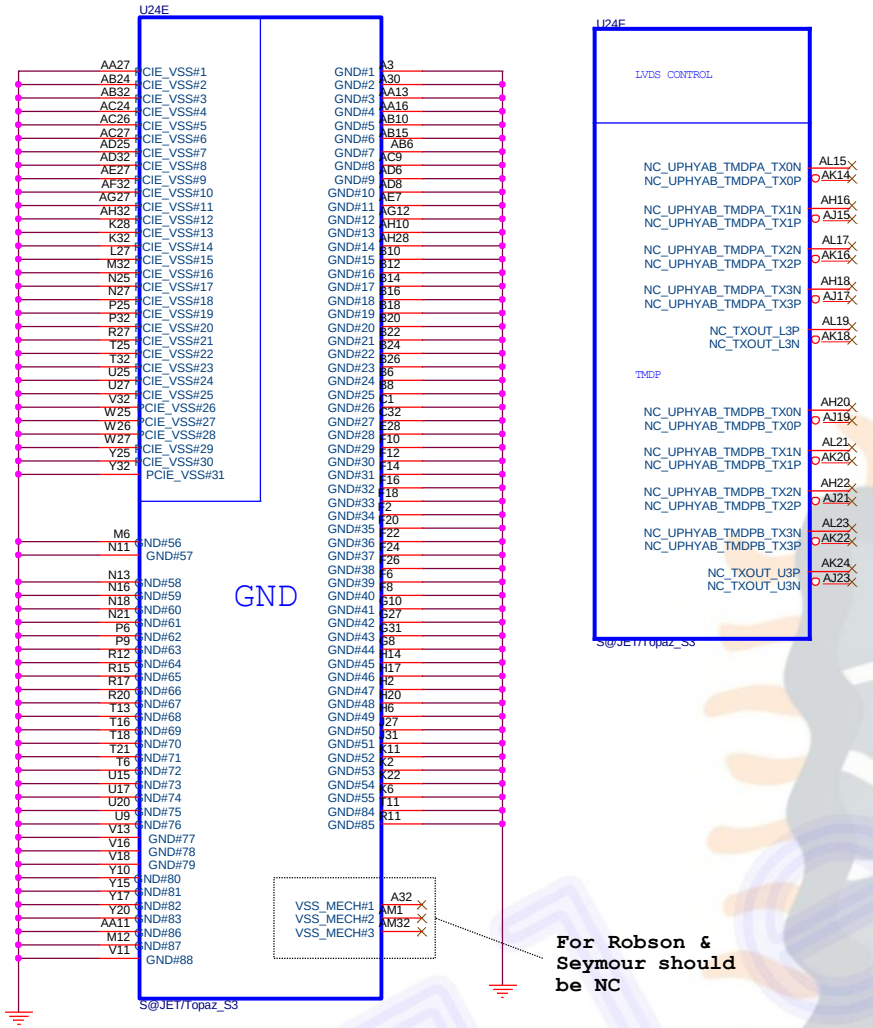
MLPS Circuit

Table 3-21 Resistor Divider Lookup Table for Bits [3:

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Quanta Computer Inc.
PROJECT : FH9
JET/TOPAZ_S3_Main
Rev 2A
Wednesday, November 19, 2014



For Robson & Seymour should be NC

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0 X
RSVD RSVD	GPIO2 GPIO8	RESERVED RESERVED	0 0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

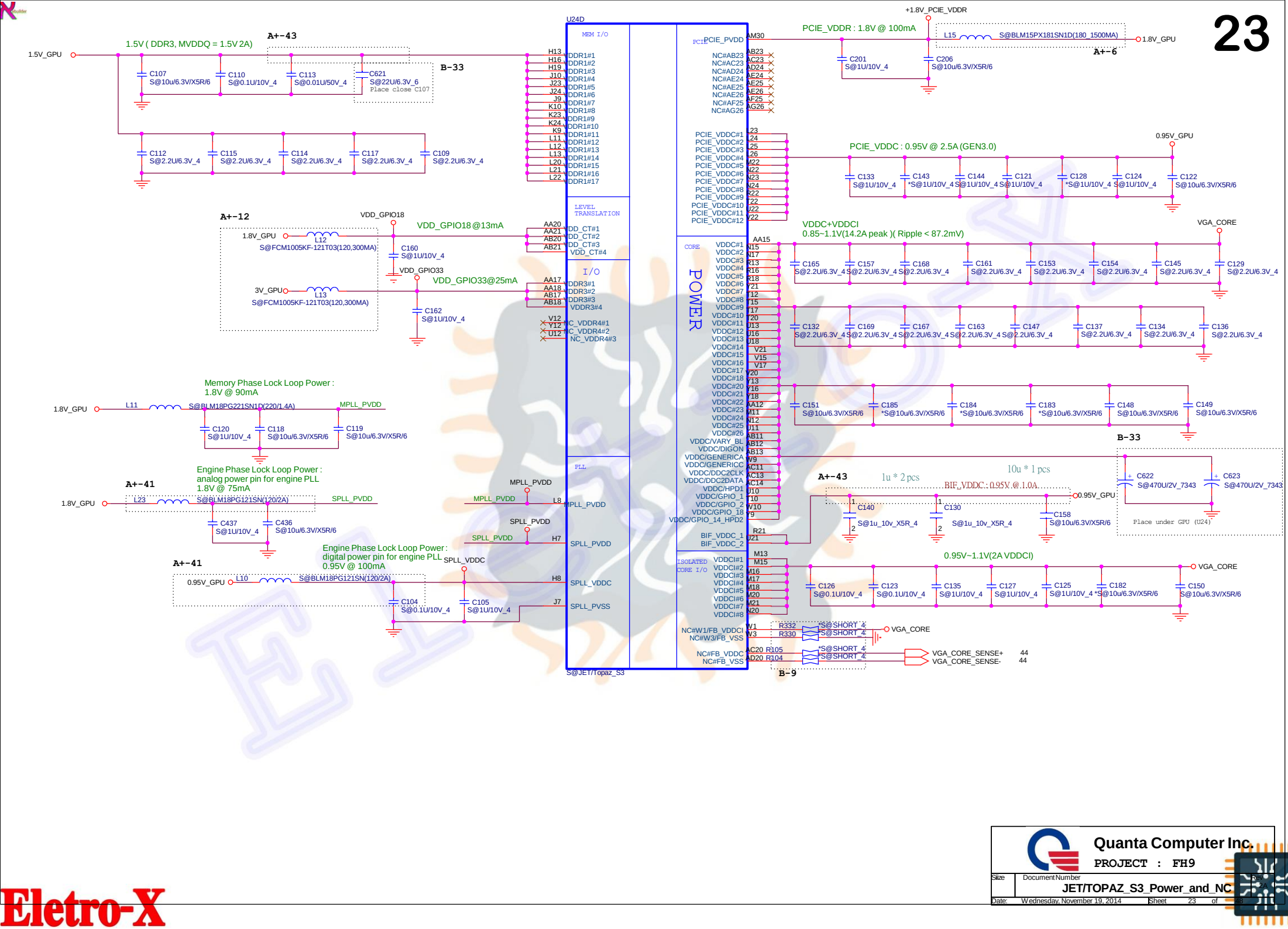
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

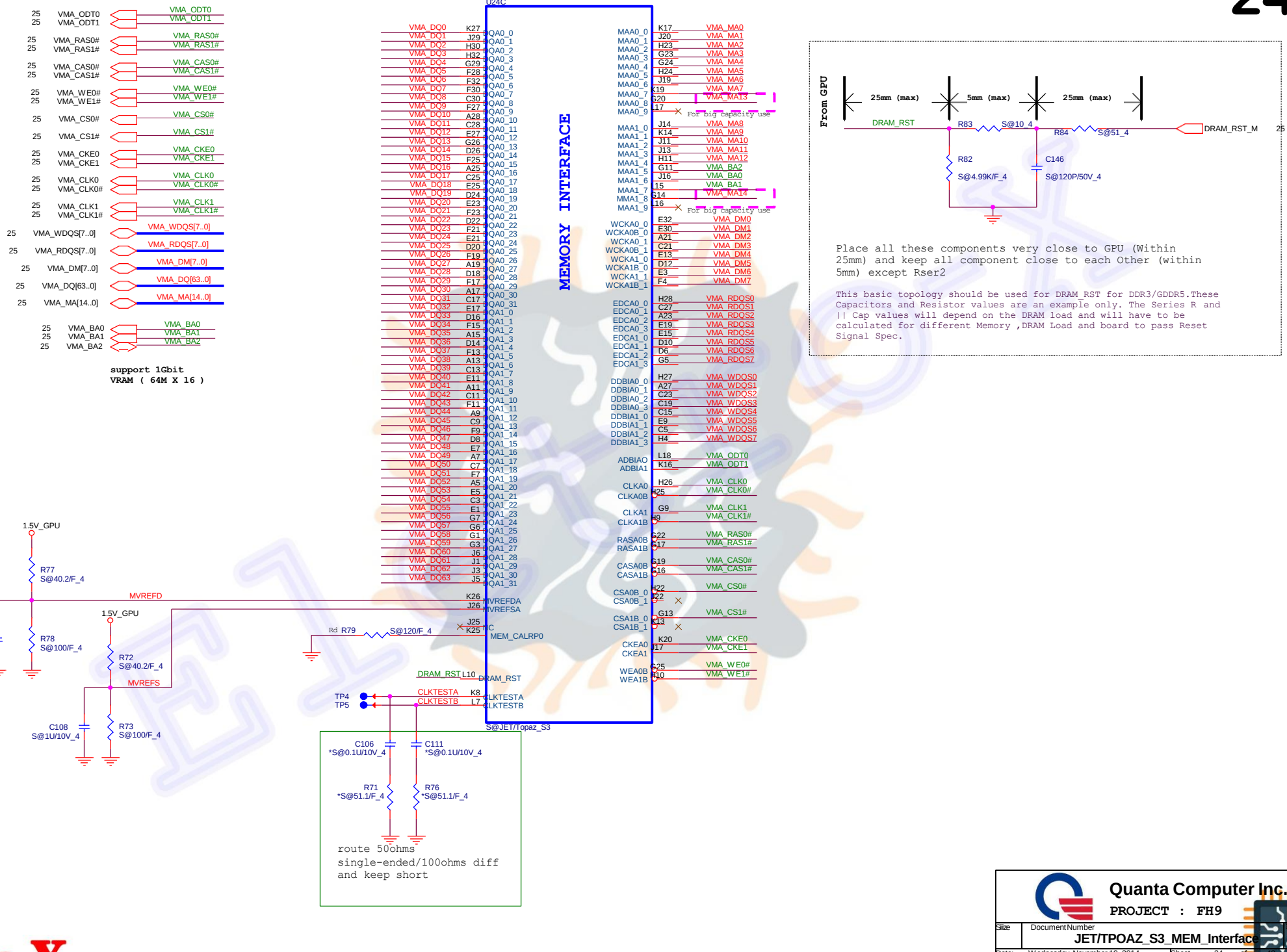
Memory Aperture size

GPIO_9 BIOSROM		GPIO_13 ROMIDCFG2	GPIO_12 ROMIDCFG1	GPIO_11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1
0	512M	Not Supported		
0	1G	Not Supported		
0	2G	Not Supported		
0	4G	Not Supported		

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

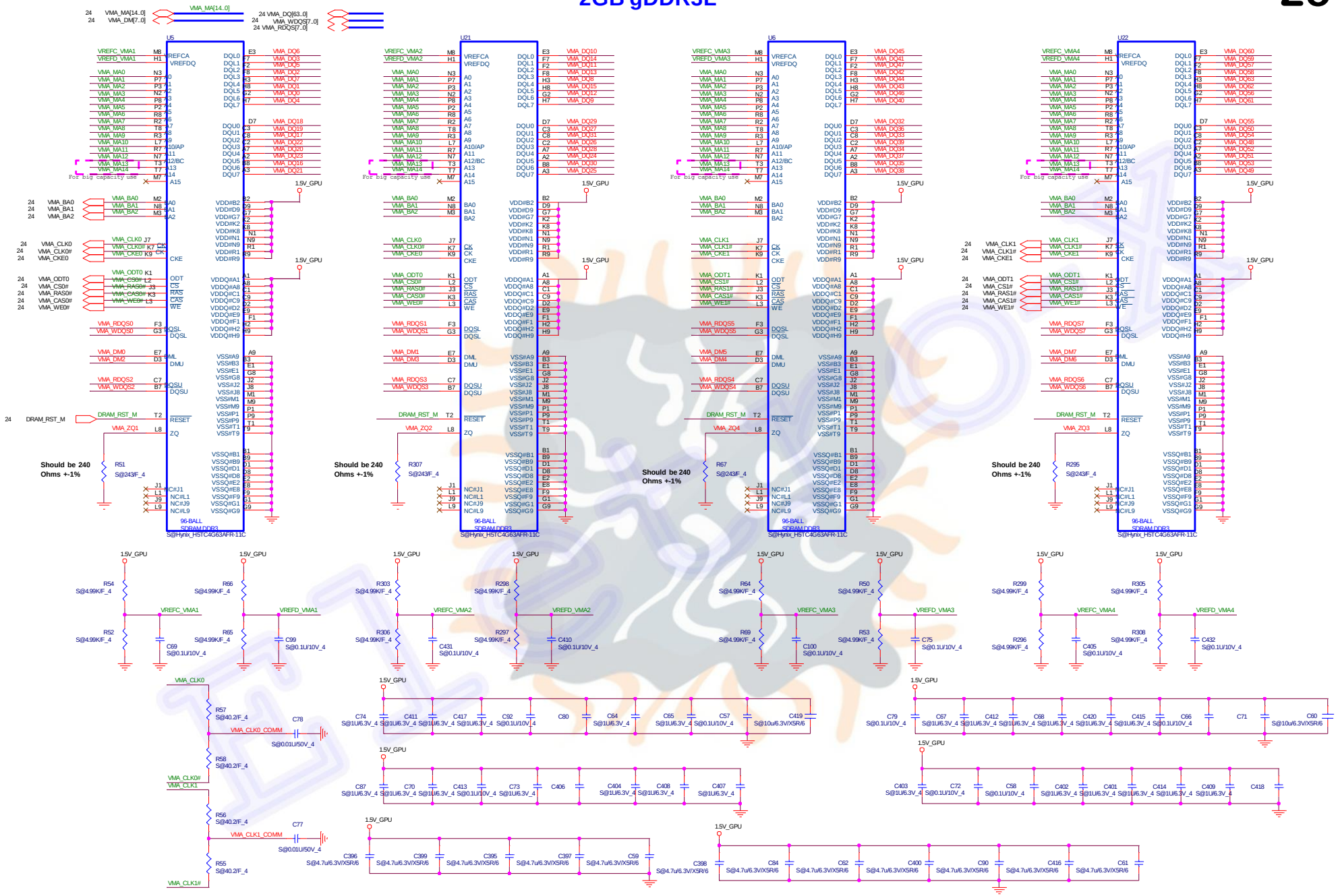


Quanta Computer Inc.
PROJECT : FH9
Size
Document Number JET/TOPAZ_S3_Power_and_NC
Rev
Date: Wednesday, November 19, 2014 Sheet 23 of 48



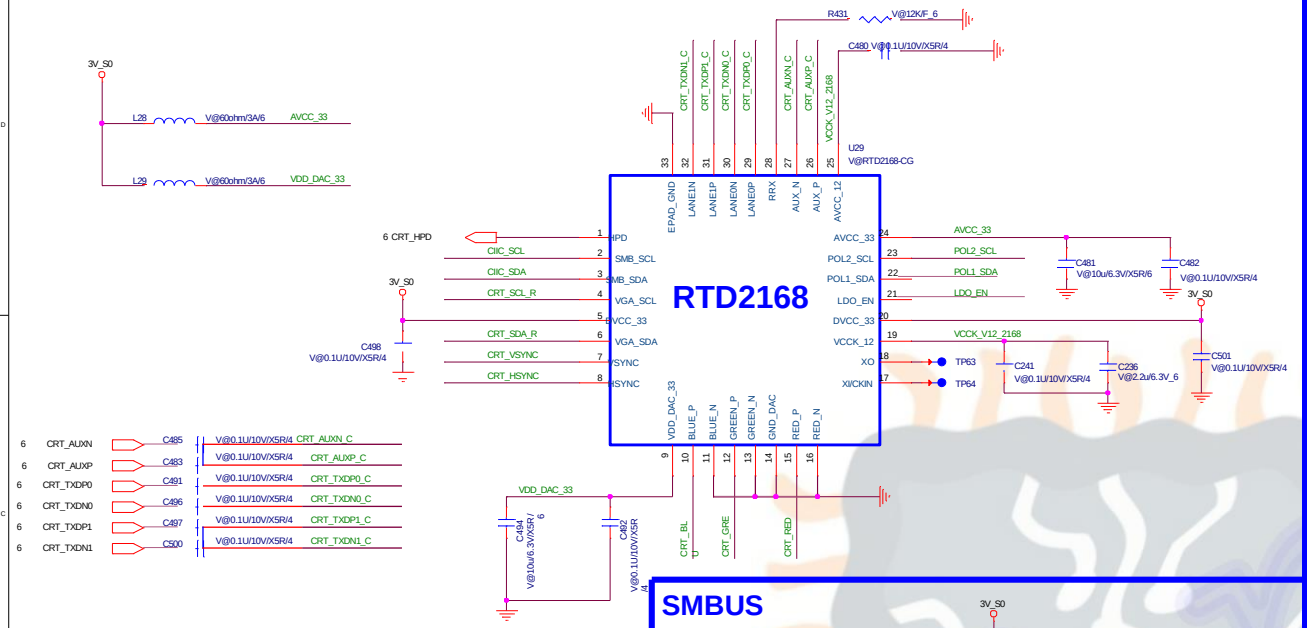
Quanta Computer Inc.
PROJECT : FH9
Size | Document Number | Rev
JET/TPOAZ_S3_MEM_Interface | 4
Date: Wednesday, November 19, 2014 | Sheet 24 of 48

2GB gDDR3L



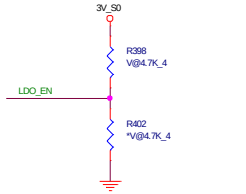
Quanta Computer Inc.
PROJECT : FH9
Size | Document Number: JET/TOPAZ_S3_VRAM_DDR3 BGA96 | Rev 2A
Date: Wednesday, November 19, 2014 | Sheet 25 of 48

DP to VGA converter (Low level Only)



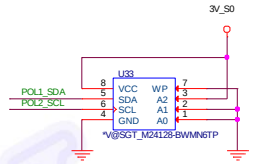
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12from External 1.2V	VCCK_V12from Embedded LDO



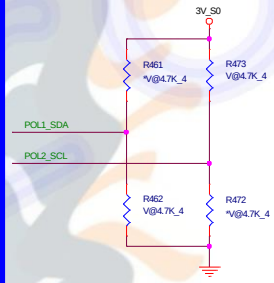
EEPROM MODE

I2C address=0xA8



Mode Configuration

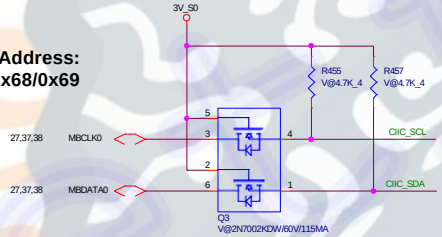
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



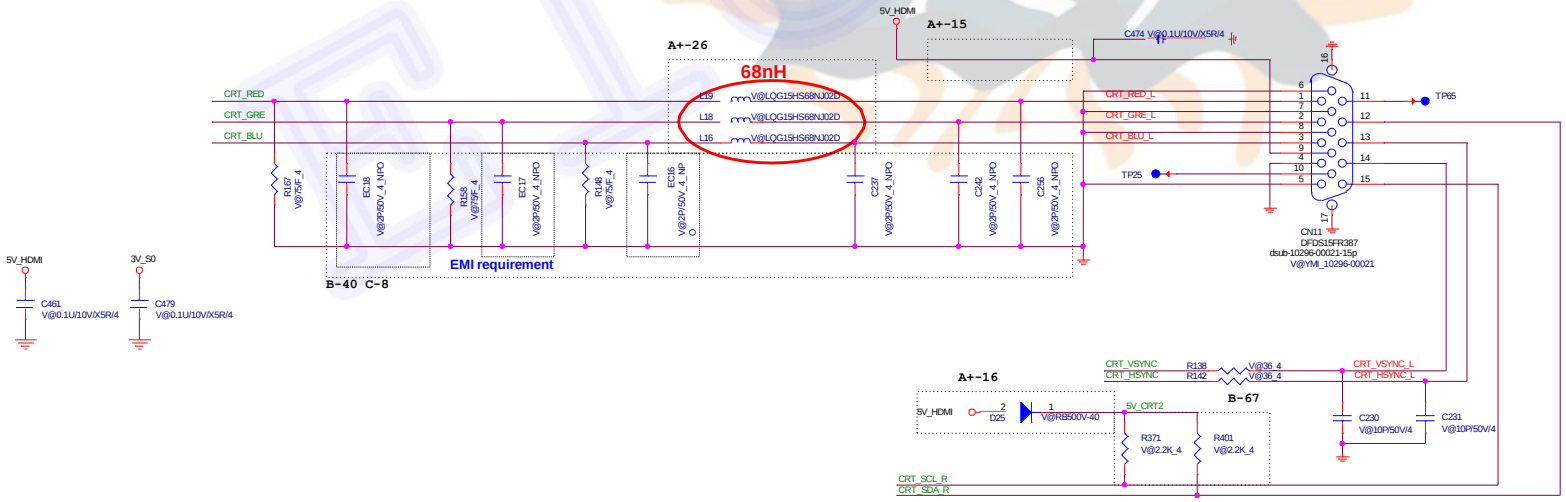
RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

SMBUS

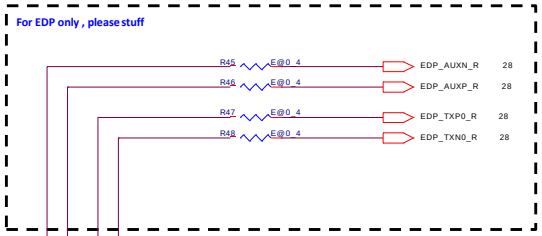
RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

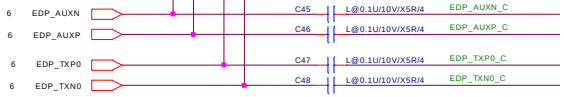


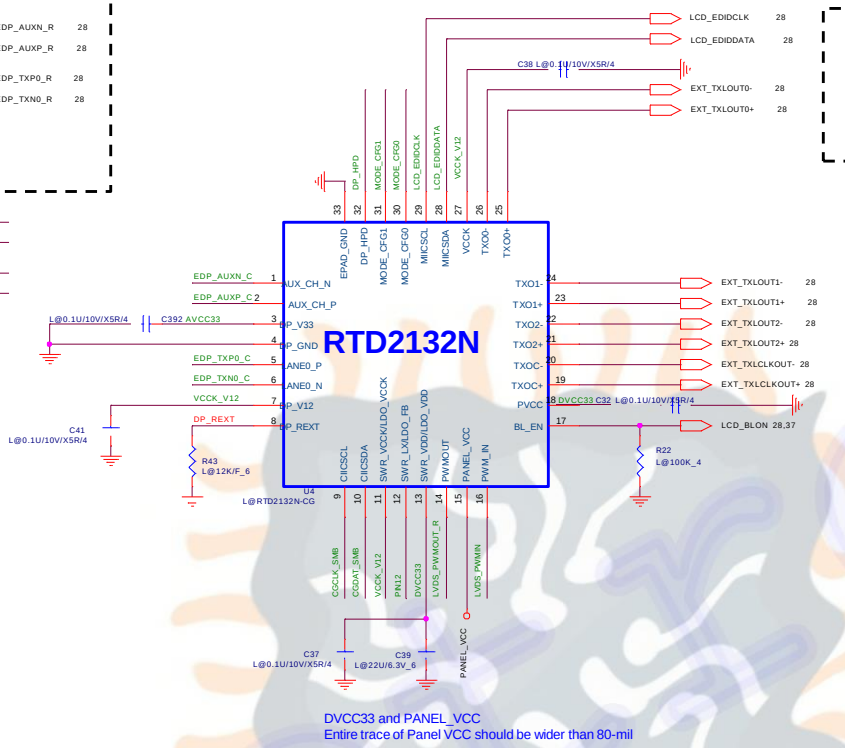
CRT PORT



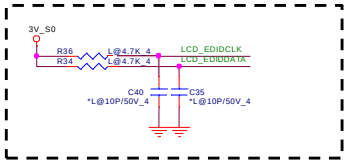
Converter RTD2132N-CG

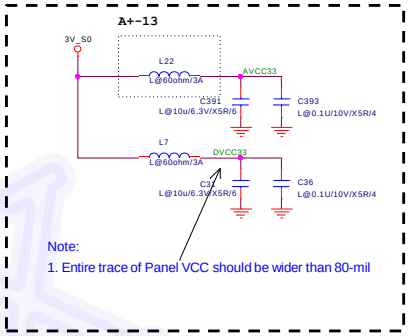






DVCC33 and PANEL_VCC
Entire trace of Panel VCC should be wider than 80-mil

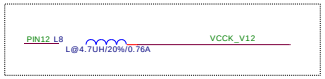




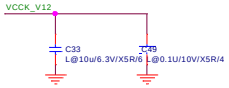
Note:
1. Entire trace of Panel VCC should be wider than 80-mil

	4.7-uH(L8)	0 Olm(L8)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE



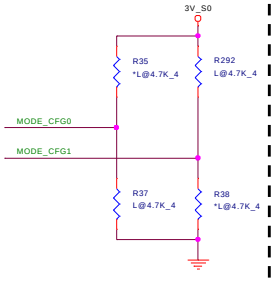
LDO MODE



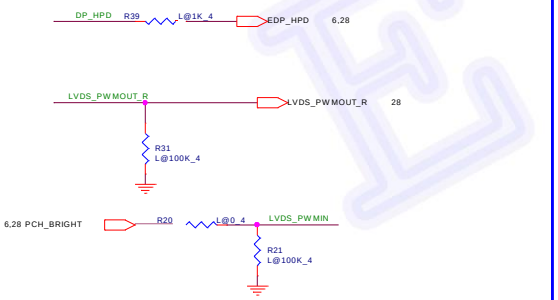
1. C33 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN12

Mode Configuration

		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

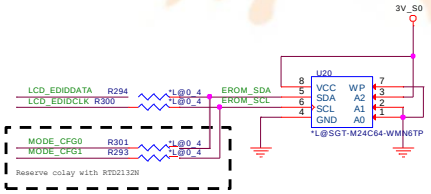


HPD/ Back Light/ BL PWM



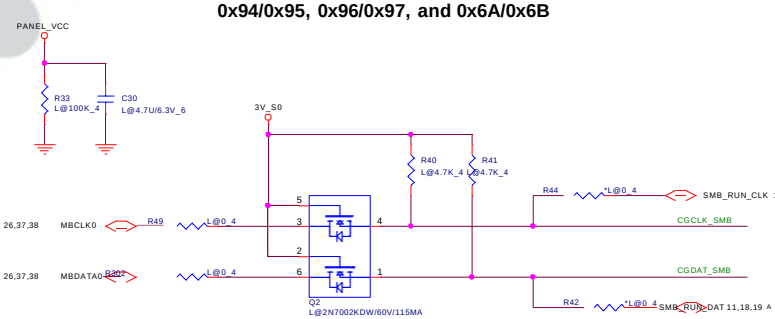
Reserve EEPROM

Address=0xA8



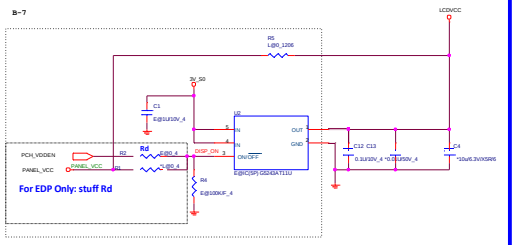
SMBUS & Panel VCC

RTD2132N Slave Address:
0x94/0x95, 0x96/0x97, and 0x6A/0x6B

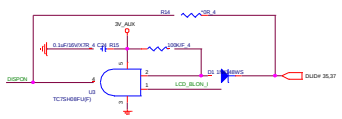


Quanta Computer Inc.
PROJECT : FH9
Size: Document Number: eDP to LVDS (RTD2132N-CG) Rev:
Date: Wednesday, November 19, 2014 Sheet

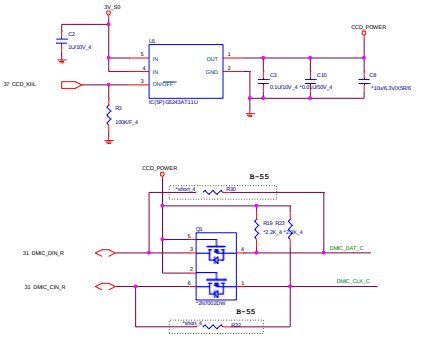
LCD POWER SWITCH



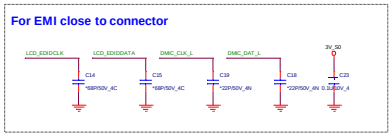
PANEL BACKLIGHT CONTROL

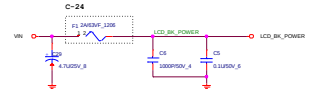


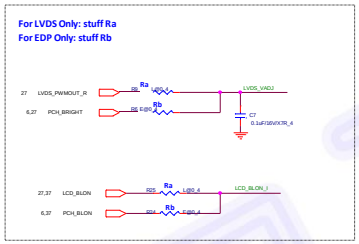
CCD KILL

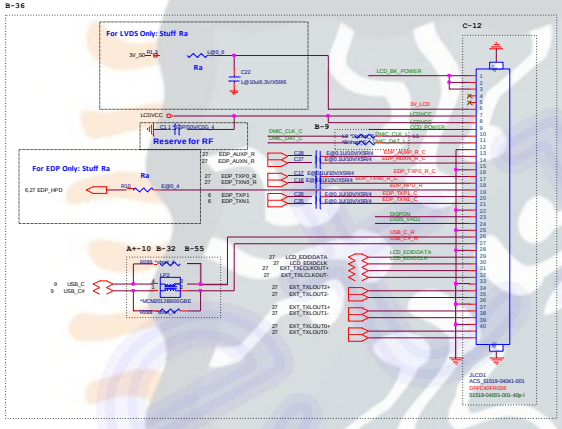


LCD CONNECTOR

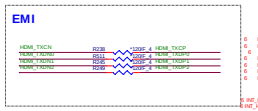


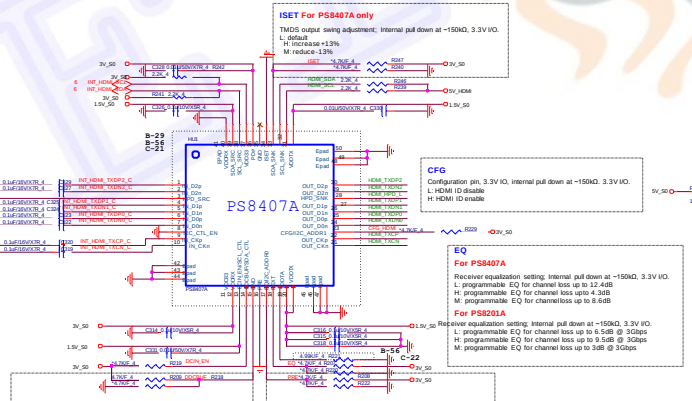




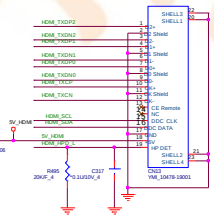


HDMI



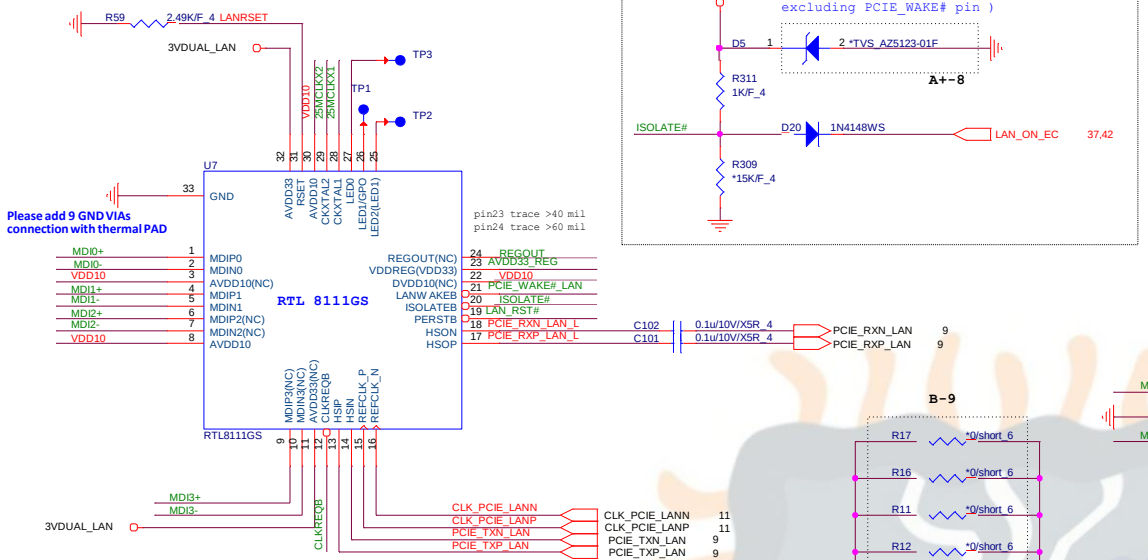


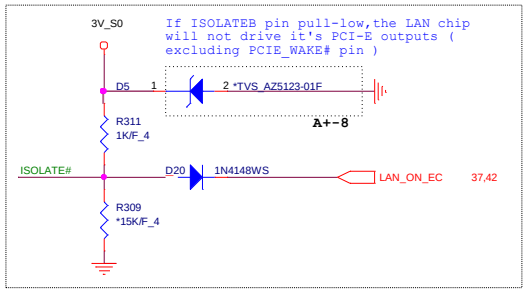
HDMI PORT



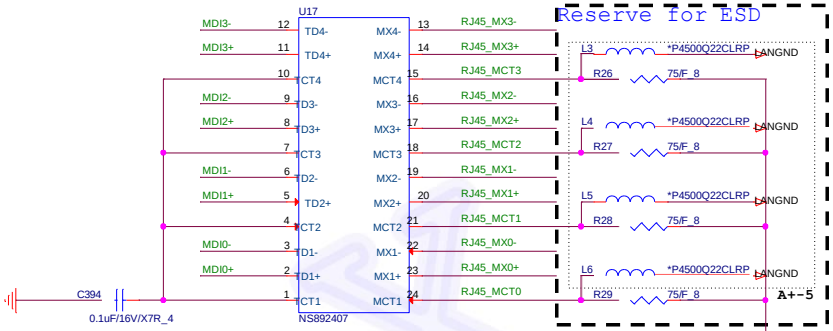
Quanta Computer Inc.		
PROJECT : FH9		
Size/Document Number: HDMI/LVDS		Rev: 2A
Date: Wednesday, November 20, 2024	Sheet 28 of 48	

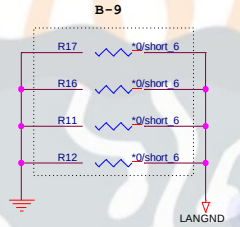
LAN RTL-8111GS

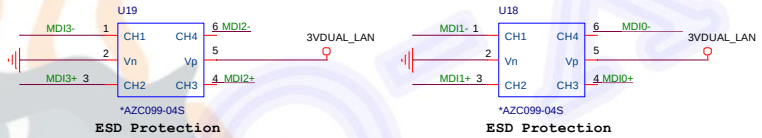


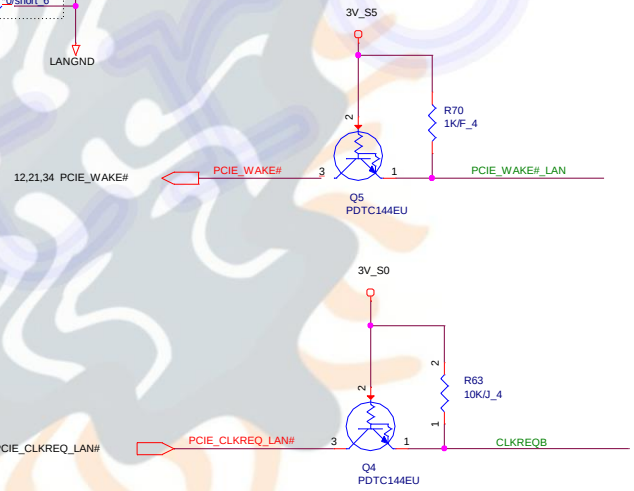


LAN Tramsformer



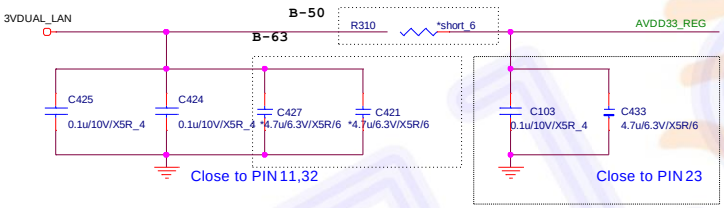




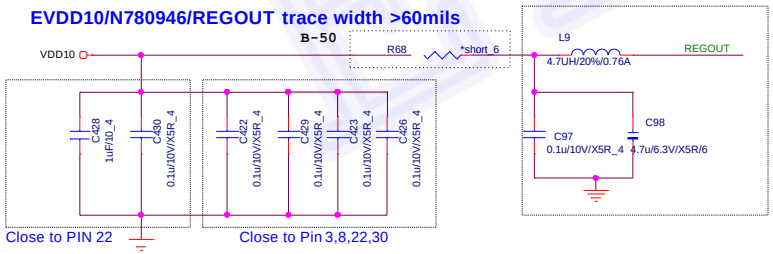


LAN POWER

EVDD10/AVDD33_REG trace width >40mils

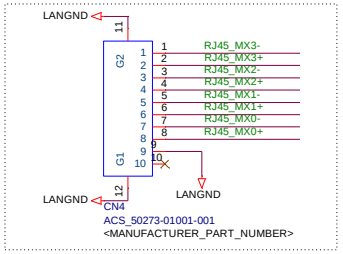


EVDD10/N780946/REGOUT trace width >60mils



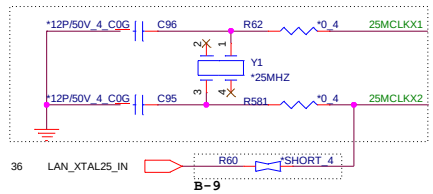
To RJ45 Conn

B-10 MP1-22



X'tal 25MHz

B-8

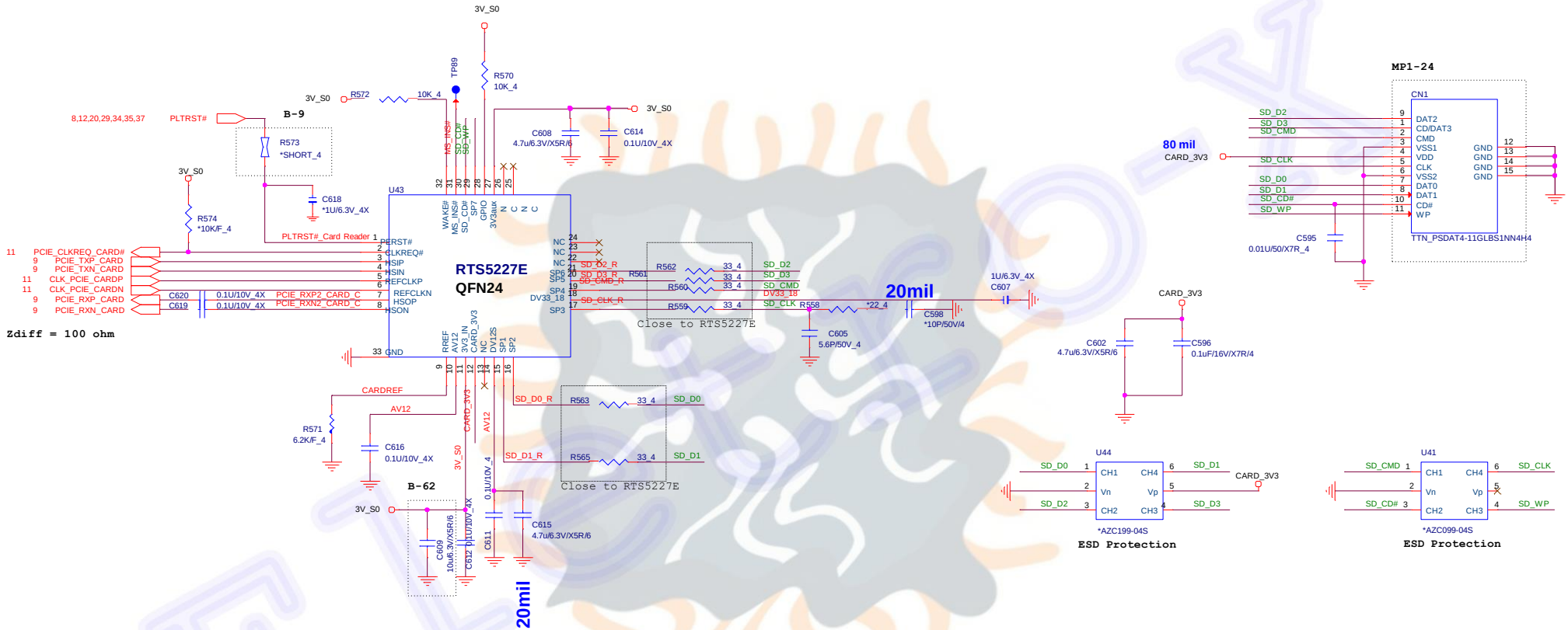


Quanta Computer Inc.

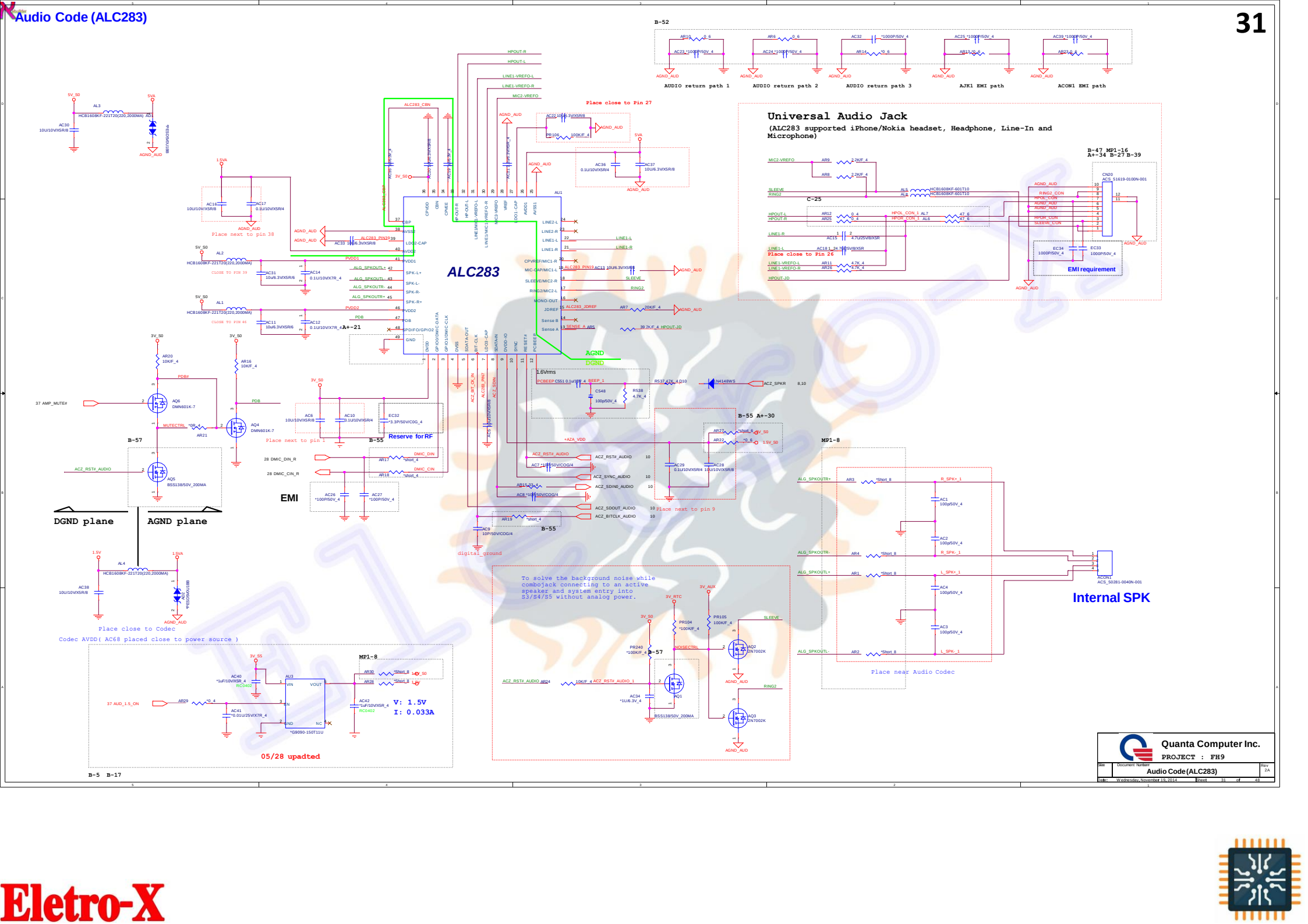
PROJECT : FH9

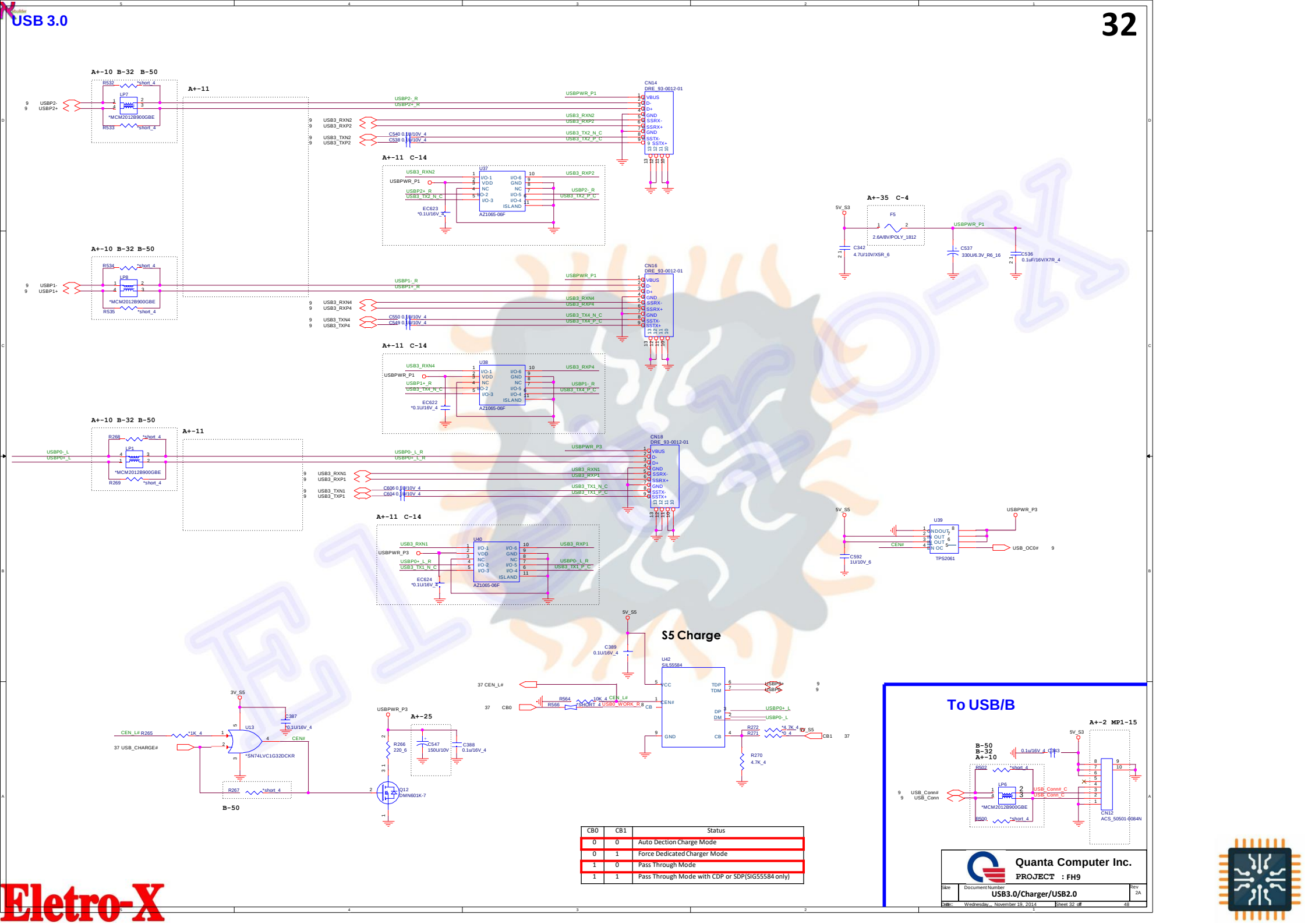
Size	Document Number	Rev
	LAN RTL8111GS/RJ45 conn	3A
Date: Wednesday, November 19, 2014	Sheet 29 of 40	

Card Reader RTS5227E



Quanta Computer Inc.			
PROJECT : FH9			
Size	Document Number		Rev
	CARD READER (RTS5227E)		1A
Date:	Wednesday, November 19, 2014	Sheet	30 of 48

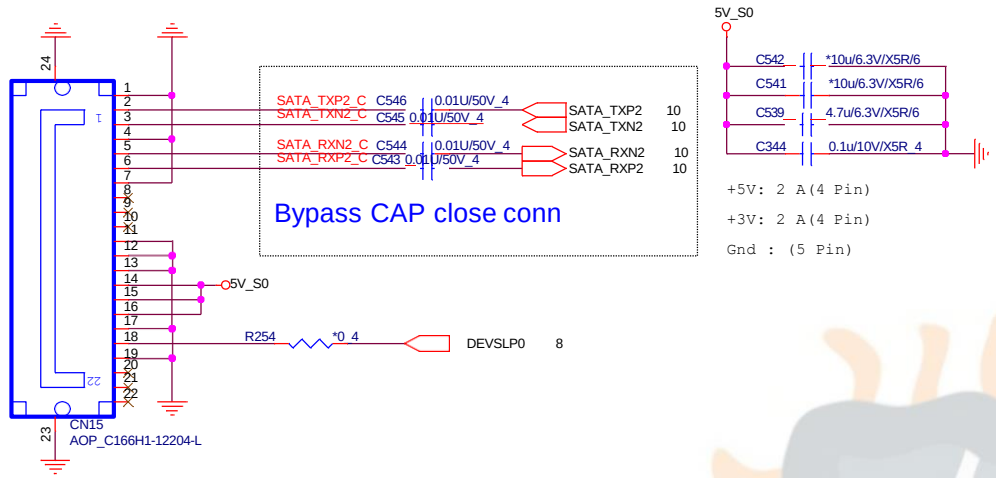

ALC283
Universal Audio Jack
(ALC283 supported iPhone/Nokia headset, Headphone, Line-In and Microphone)
EMI requirement
Internal SPK
Reserve for RF
EMI
DGND plane
AGND plane
Place close to Pin 27
Place close to Pin 26
Place close to Codec
Place next to pin 38
Place next to pin 1
Place next to pin 9
Place near Audio Codec
AUDIO return path 1
AUDIO return path 2
AUDIO return path 3
AJK1 EMI path
ACON1 EMI path
To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.
Codec AVDD(AC68 placed close to power source)
V: 1.5V
I: 0.033A
05/28 upadted
Quanta Computer Inc.
PROJECT : FH9
Audio Code (ALC283)



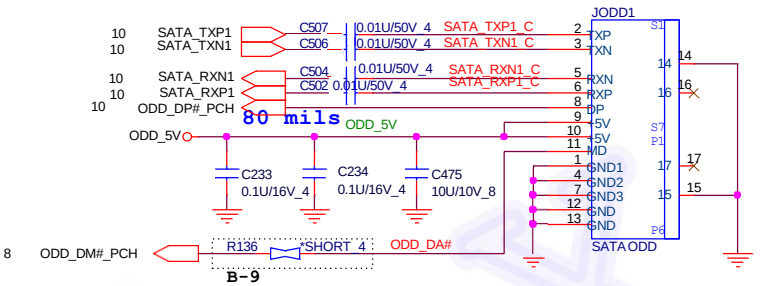
CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG55584 only)

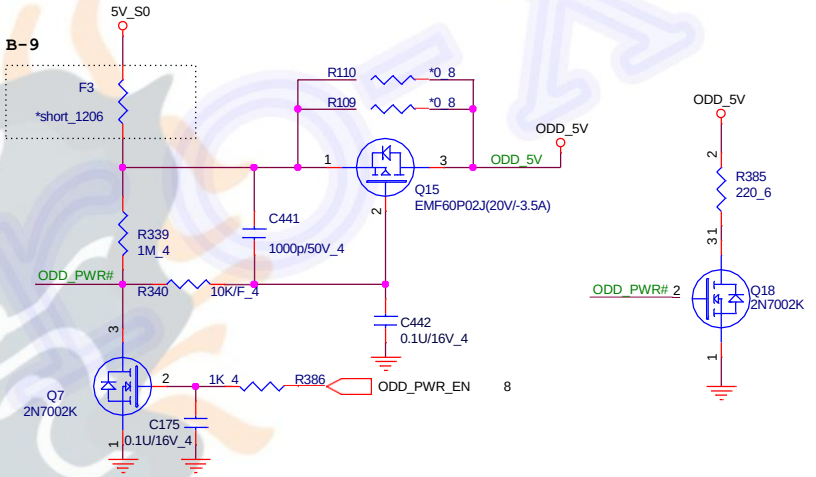
Quanta Computer Inc.
PROJECT : FH9
Size: Document Number: USB3.0/Charger/USB2.0 Rev: 2A
Date: Wednesday, November 19, 2014 Sheet 32 of 48

SATA HDD Connector

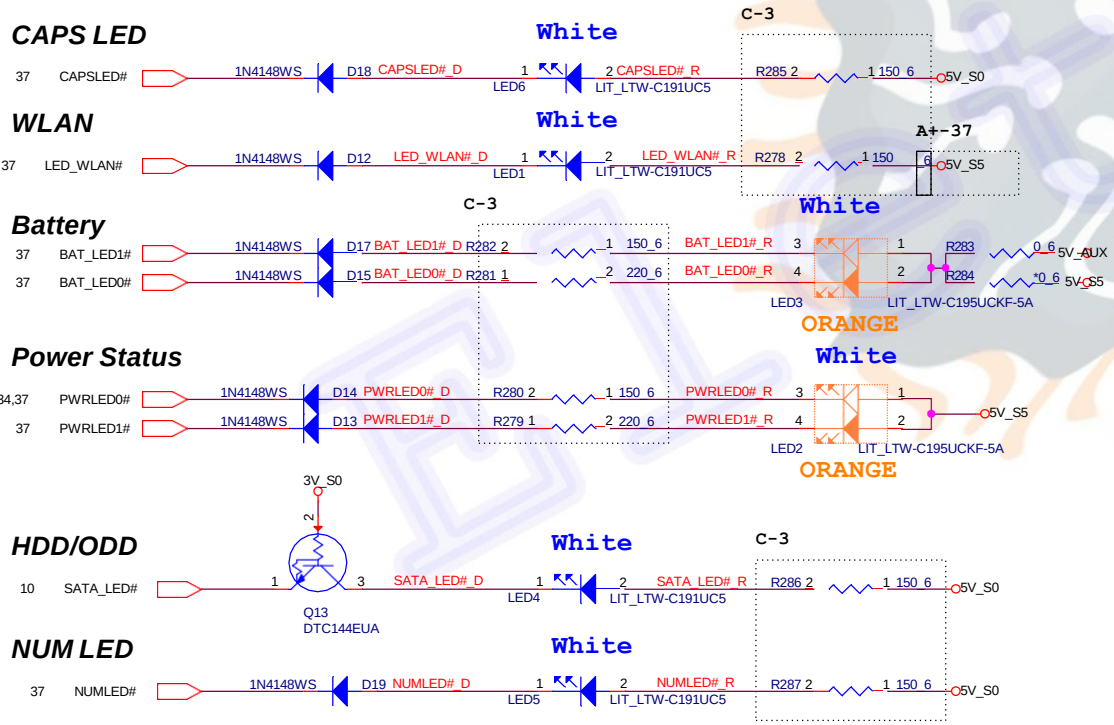


SATA ODD Connector





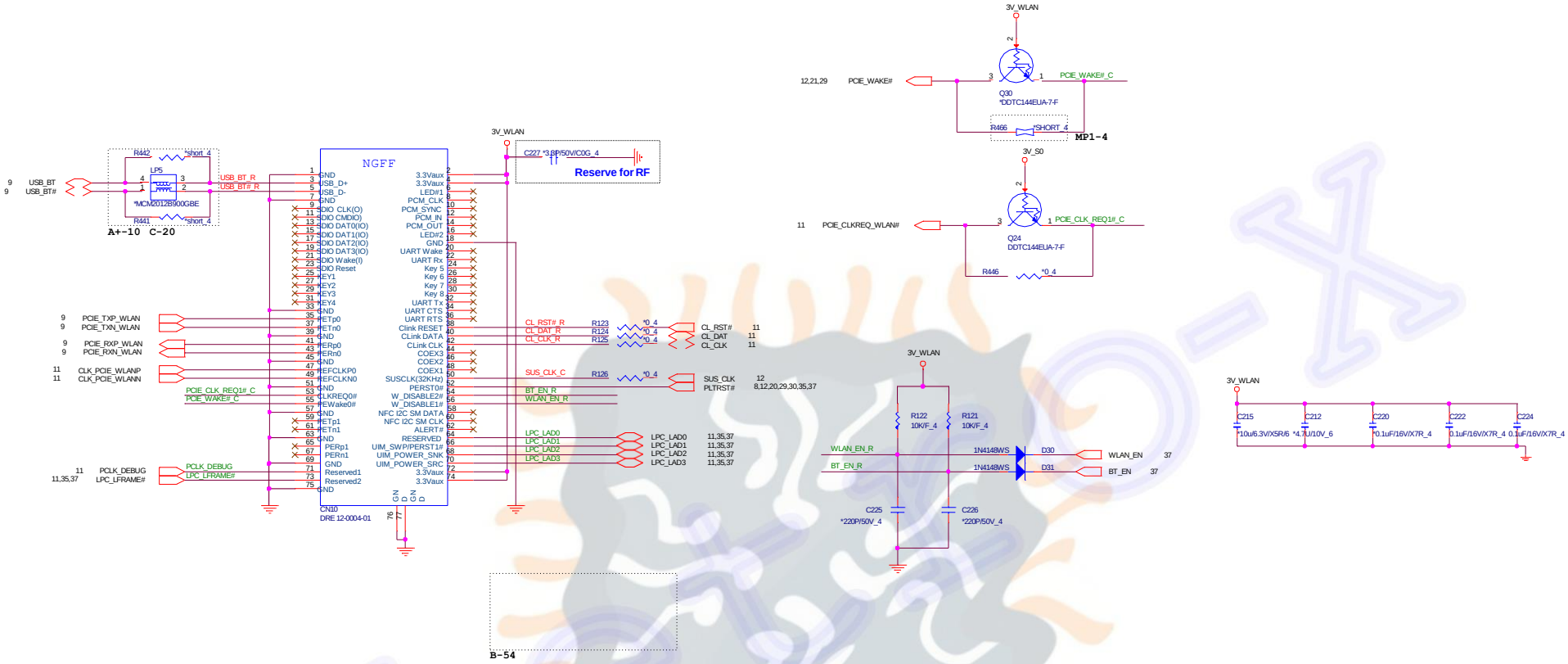
LED



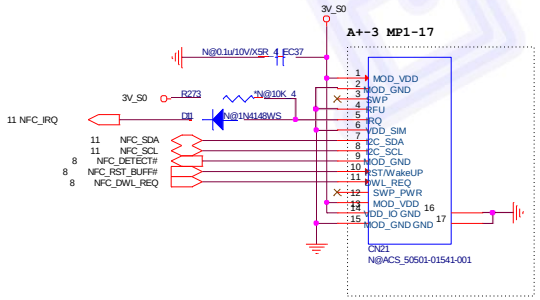
Quanta Computer Inc.
PROJECT : FH9

Size	Document Number	Rev
	HDD/ODD/LED	2A
Date: Wednesday, November 19, 2014	Sheet 33 of 48	

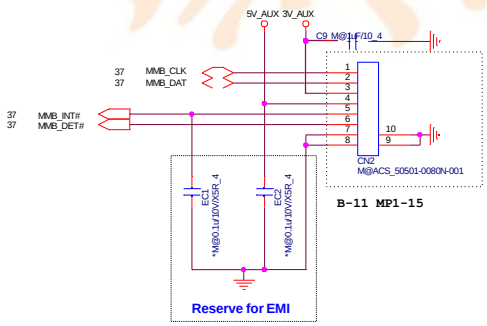
WLAN + BT(NGFF Socket Slot A-SD)



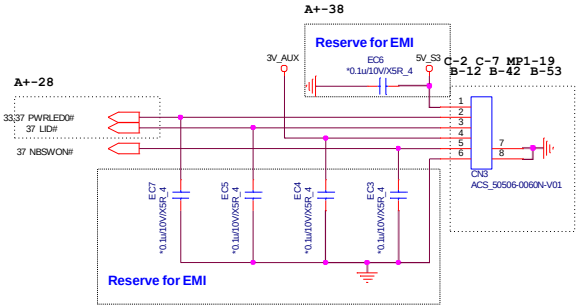
NFC



TO MMB/B



TO PWR/B



Quanta Computer Inc.			
PROJECT : FH9			
Size	Document Number		Rev
	WLAN/BT/NFC/MMB/PWR		2A
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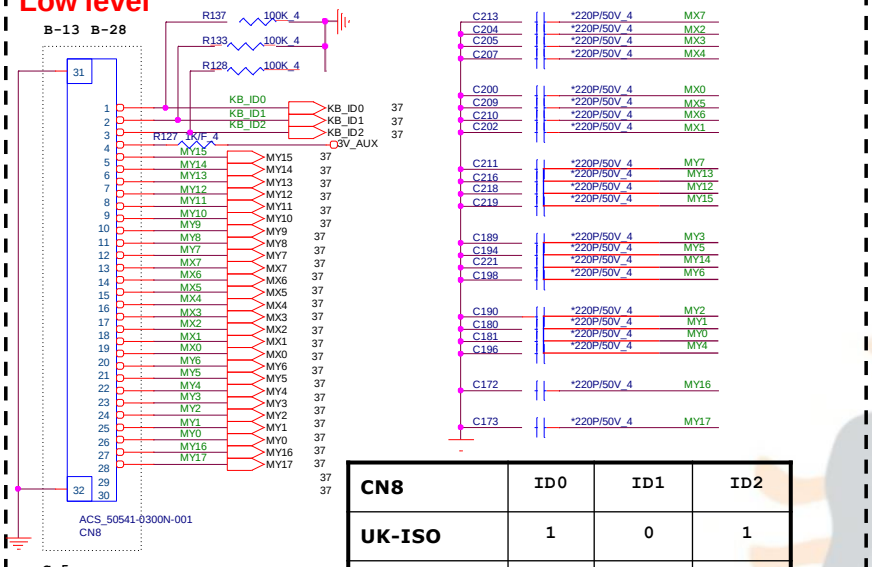
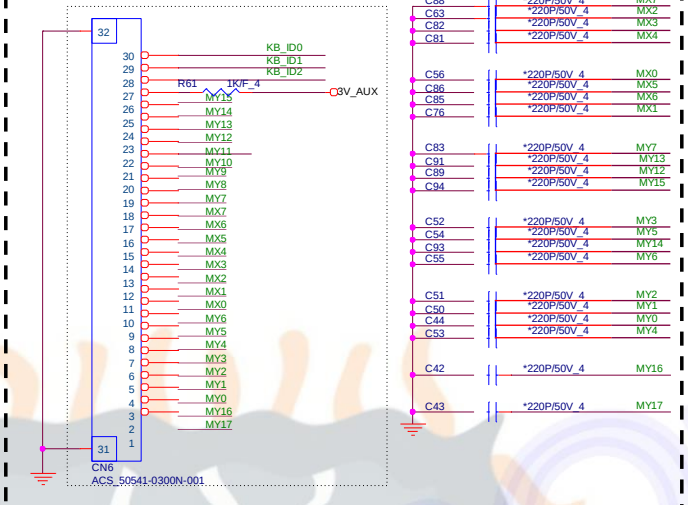
Keyboard Connector

Low level



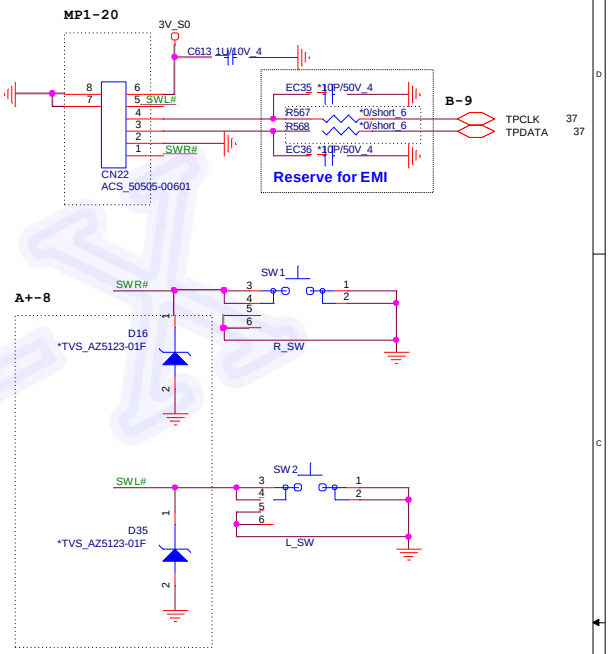
CN8	ID0	ID1	ID2
UK-ISO	1	0	1
US-ISO	0	1	1
JP-Low-ISO	1	1	1
JP-High-ISO	0	0	1

High level

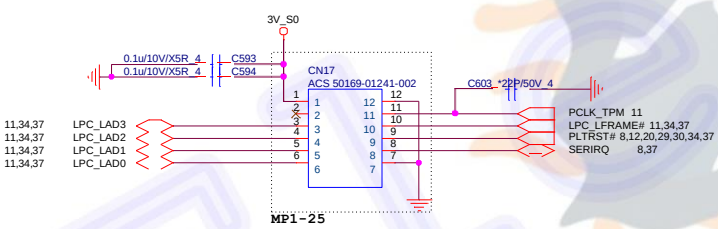


CN6	ID0	ID1	ID2
UK-CHO	1	0	0
US-CHO	0	1	0
JP-Low-CHO	1	1	0

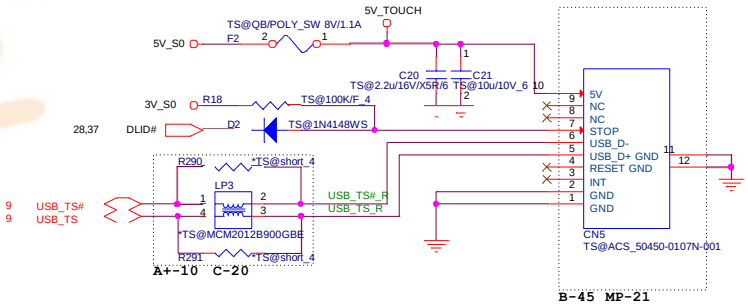
Touch Pad Connector



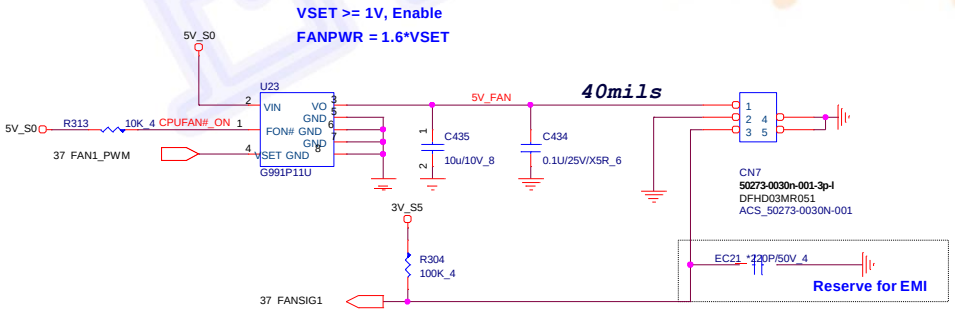
TPM

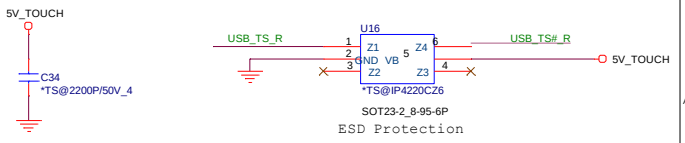


Touch Screen



FAN Control





Quanta Computer Inc.
PROJECT : FH9

Size	Document Number	Rev
	KB/FAN/TP/TPM/Touch screen	1A
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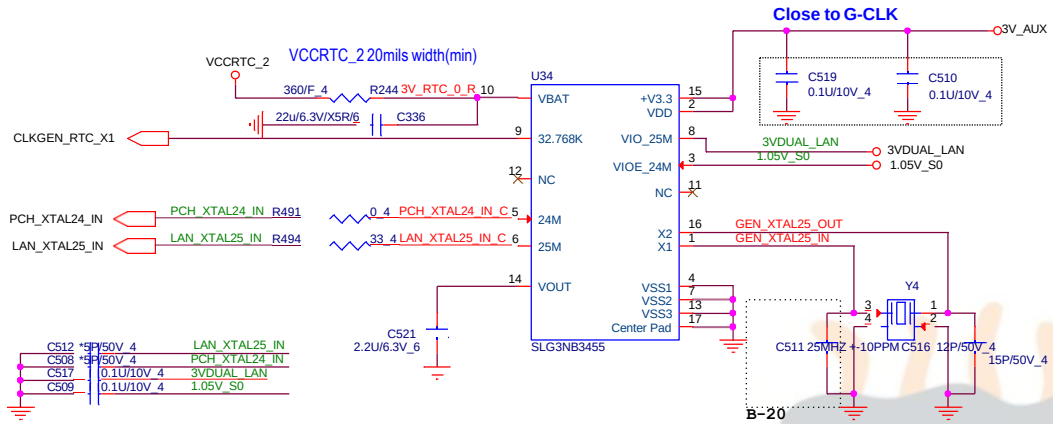
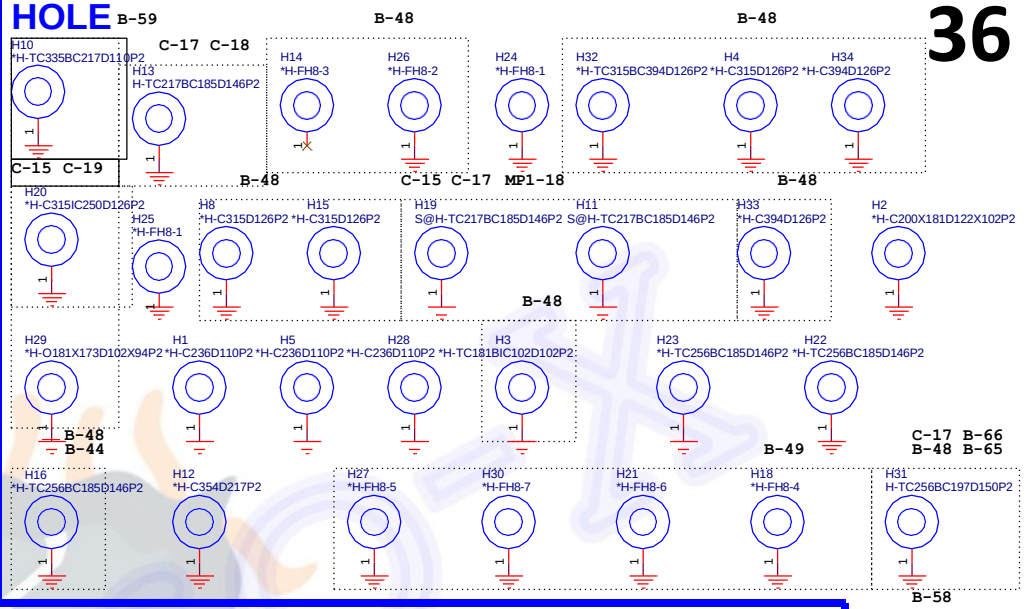
Green CLK Circuitry

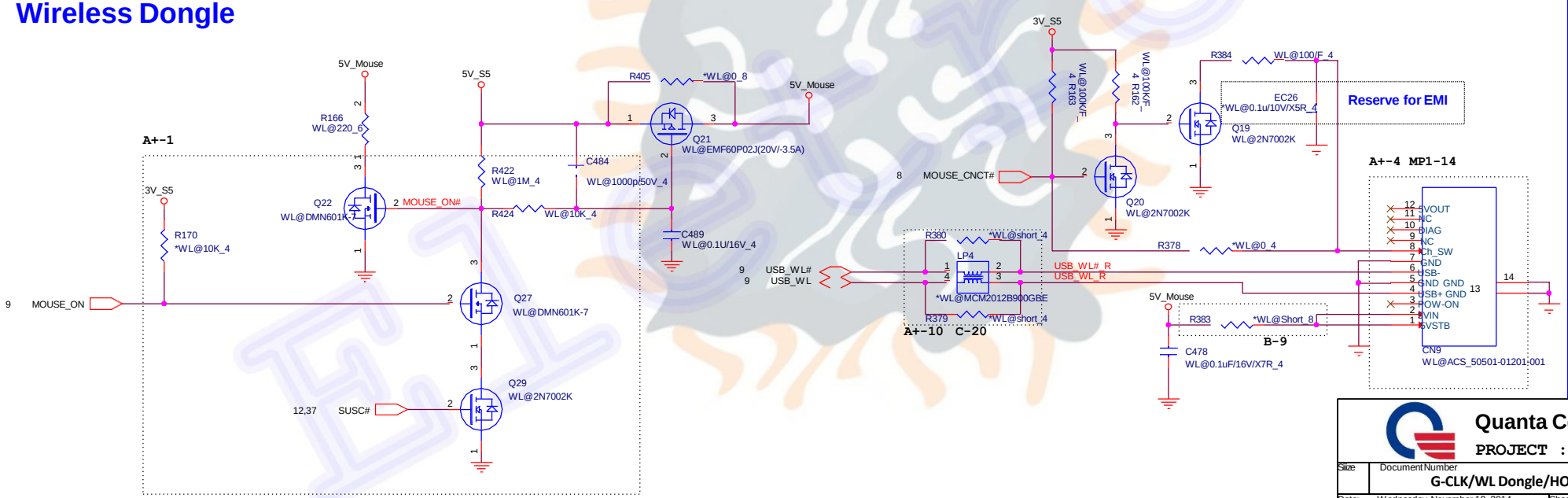


HOLE



36

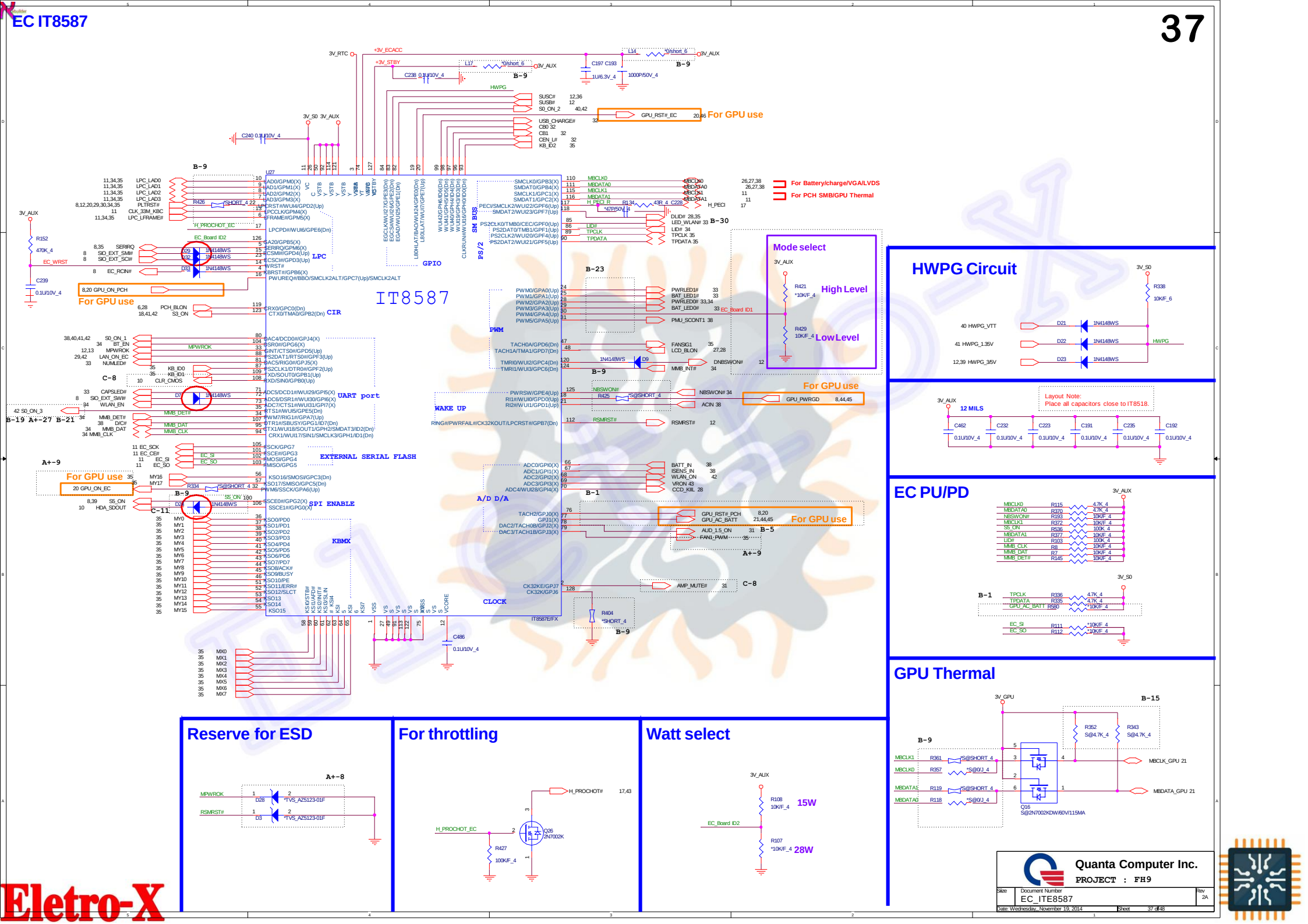
Wireless Dongle



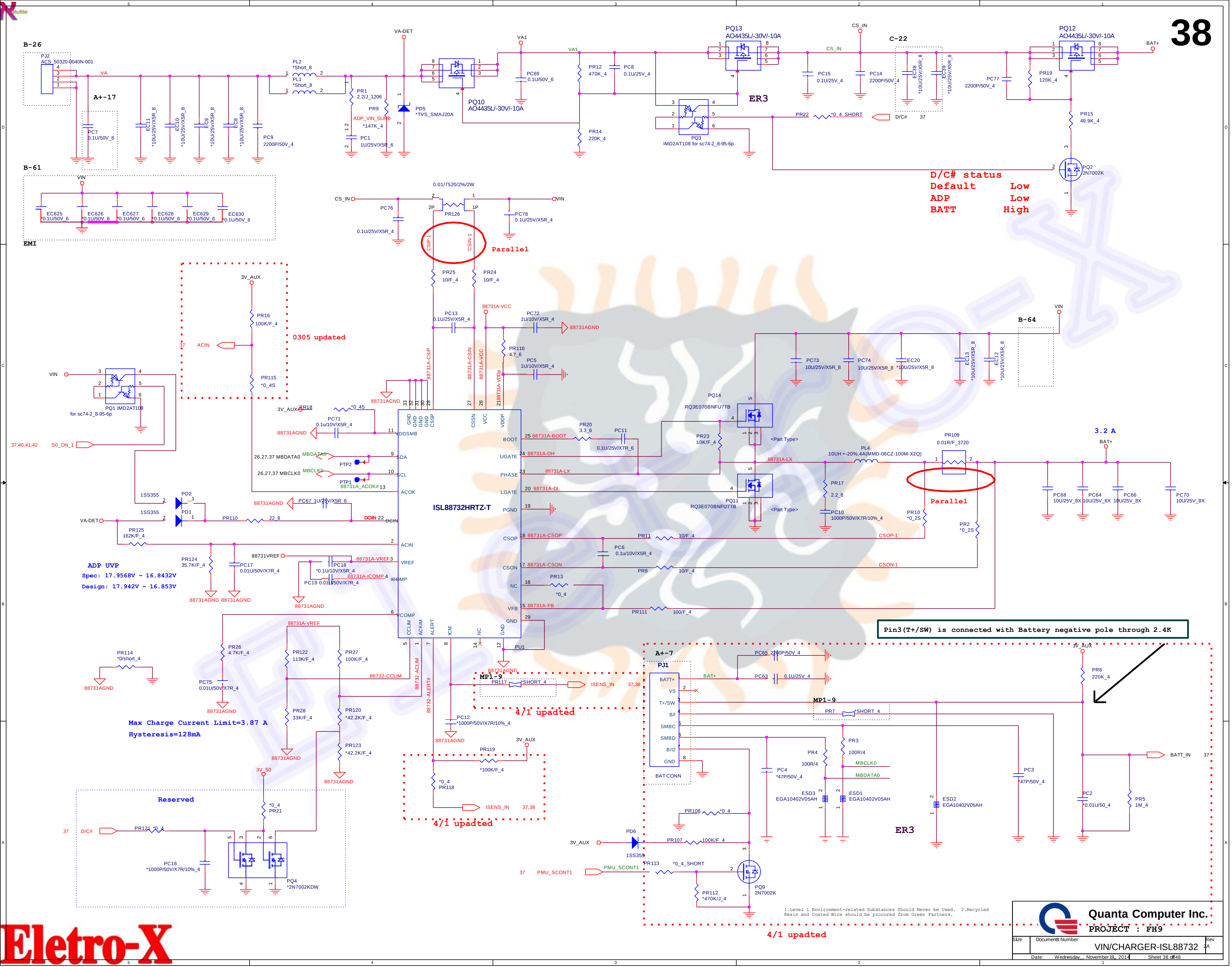
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	G-CLK/WL Dongle/HOLE	2A
Date: Wednesday, November 19, 2014	Sheet 36 of 48	

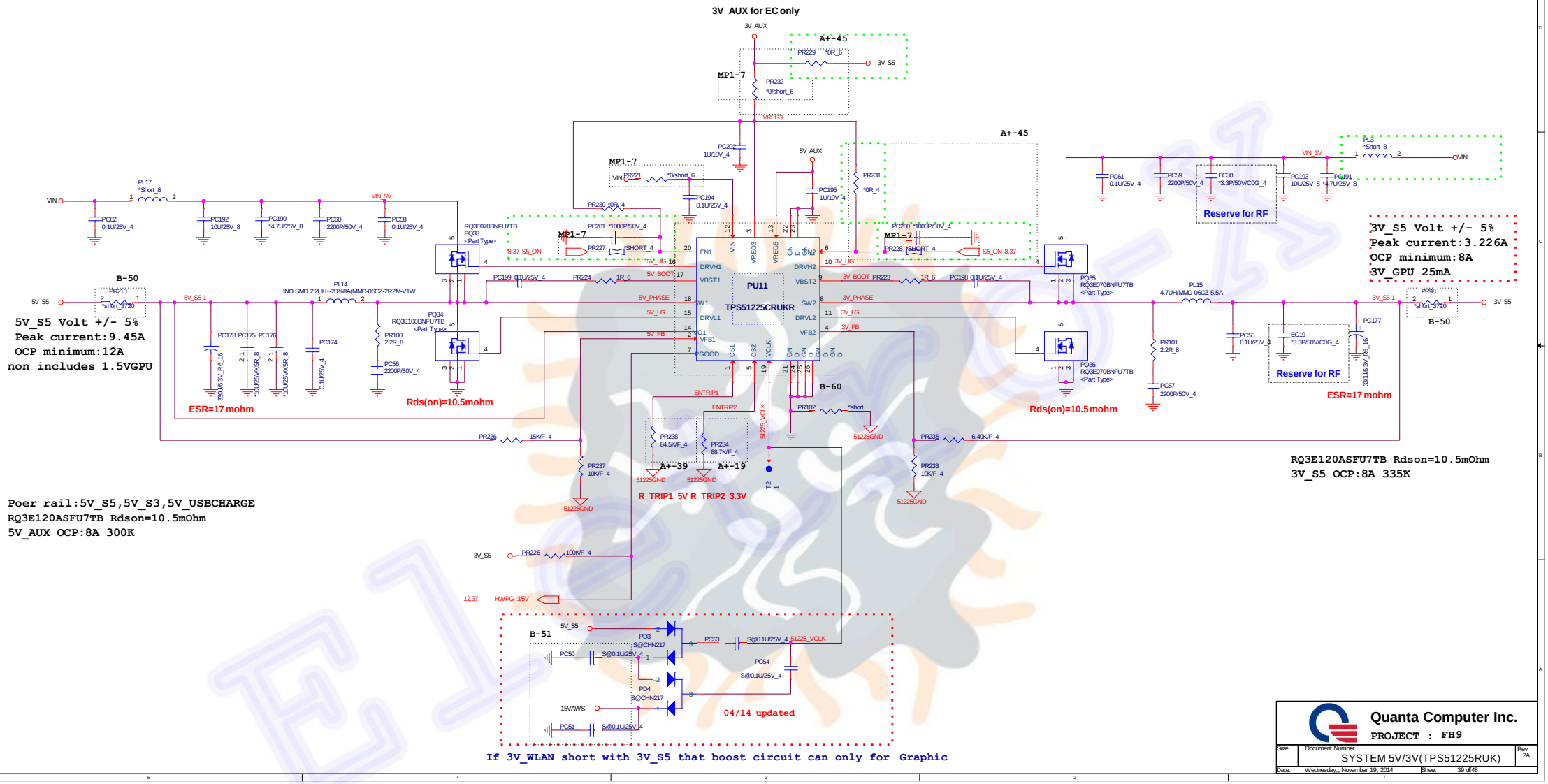


Quanta Computer Inc.
PROJECT : FH9
Size | Document Number EC_ITE8587 | Rev 2A
Date: Wednesday, November 19, 2014 | Sheet 37 of 48



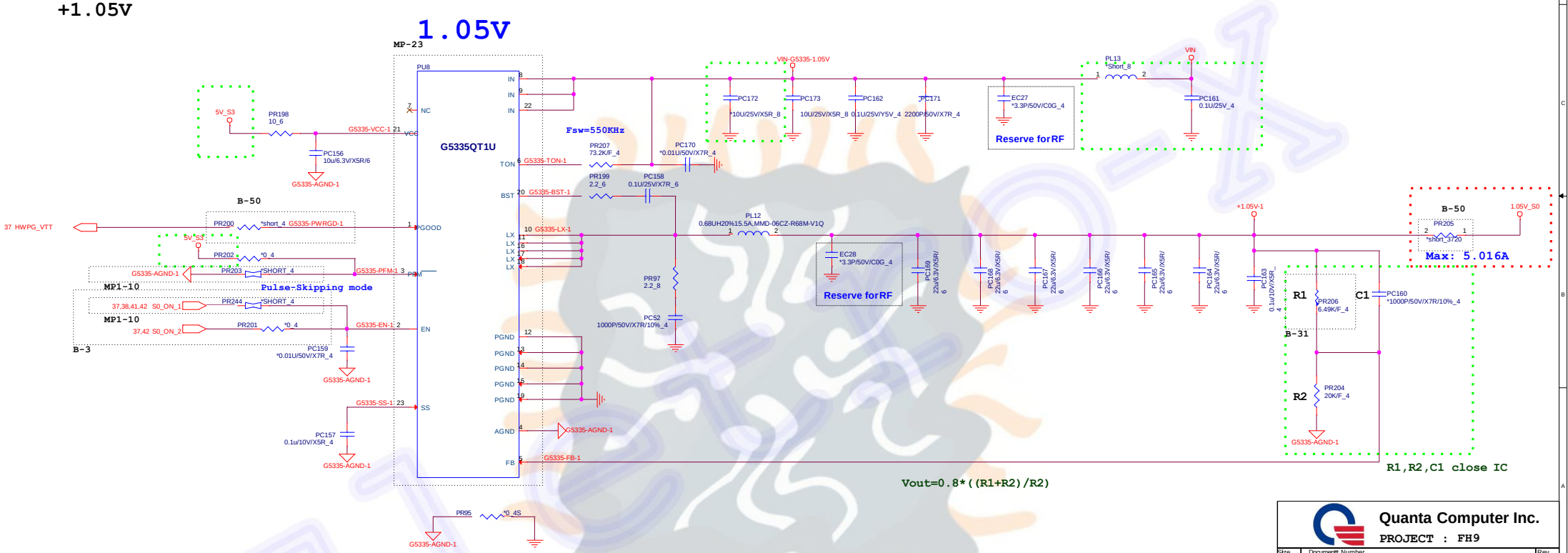
B-26
PJ2 ACS_50320-0040N-001
A+-17
B-61
EMI
PL2 *Short_8
PL1 *Short_8
PR1 2.2/J_1206
PR9 *147K_4
ADP_VIN_SUNB
PD5 *TVS_SMAJ20A
PC1 1U/25V/X5R_6
PC7 0.1U/50V_6
EC11 *10U/25V/X5R_8
EC10 *10U/25V/X5R_8
EC9 *10U/25V/X5R_8
EC8 *10U/25V/X5R_8
PC9 2200P/50V_4
EC625 *0.1U/50V_6
EC626 *0.1U/50V_6
EC627 *0.1U/50V_6
EC628 *0.1U/50V_6
EC629 *0.1U/50V_6
EC630 *0.1U/50V_6
VA-DET
VA1
PQ10 AO4435L/-30V/-10A
PC69 0.1U/50V_6
PR12 470K_4
PC8 0.1U/25V_4
PR14 220K_4
PQ13 AO4435L/-30V/-10A
PQ3 IMD2AT108 for sc74-2_8-95-6p
ER3
CS_IN
C-22
PC15 0.1U/25V_4
PC14 2200P/50V_4
EC38 *10U/25V/X5R_8
EC39 *10U/25V/X5R_8
PR22 *0_4_SHORT
D/C# 37
PQ12 AO4435L/-30V/-10A
PC77 2200P/50V_4
PR19 120K_4
PR15 49.9K_4
PQ2 2N7002K
BAT+
D/C# status
Default Low
ADP Low
BATT High
0.01/7520/2%/2W
PR126
PC76 0.1U/25V/X5R_4
PC78 0.1U/25V/X5R_4
CSIP-1
CSIN-1
Parallel
PR25 10/F_4
PR24 10/F_4
3V_AUX
PR16 100K/F_4
ACIN
PR115 *0_4S
0305 updated
VIN
PQ1 IMD2AT108 for sc74-2_8-95-6p
37,40,41,42 S0_ON_1
PD2 1SS355
PD1 1SS355
PR110 22_8
PR125 162K/F_4
PR124 35.7K/F_4
PC17 0.01U/50V/X7R_4
88731AGND
ADP UVP
Spec: 17.9568V ~ 16.8432V
Design: 17.942V ~ 16.853V
PC13 0.1U/25V/X5R_4
88731A-VCC
PC72 1U/10V/X5R_4
PR116 4.7_6
PC5 1U/10V/X5R_4
PR18 *0_4S
PC71 0.1u/10V/X5R_4
26,27,37 MBDATA0
26,27,37 MBCLK0
PTP2
PTP1
88731A_ACOK#
PC67 1U/25V/X5R_6
DCIN
88731VREF
PC18 *0.1U/10V/X5R_4
PC19 0.01U/50V/X7R_4
88731A-VREF3
88731A-ICOMP
ISL88732HRTZ-T
VDDSMB SDA SCL ACOK DCIN ACIN VREF ICOMP VCOMP
BOOT UGATE PHASE LGATE PGND CSOP CSON NC VFB GND
CCLIM ACKIM ALERT ICM NC GND
CSSN VCC VDDP
PR20 3.3_6
PC11 0.1U/25V/X7R_6
PR23 10K/F_4
PQ14 RQ3E070BNFU7TB
PQ11 RQ3E070BNFU7TB
<Part Type>
PC73 10U/25V/X5R_8
PC74 10U/25V/X5R_8
EC20 *10U/25V/X5R_8
EC13 *10U/25V/X5R_8
EC12 *10U/25V/X5R_8
B-64
PR17 2.2_8
PC10 1000P/50V/X7R/10%_4
PL4 10UH+-20%,4A(MMD-06CZ-100M-X2Q)
PR109 0.01R/F_3720
3.2 A
PC68 10U/25V_8X
PC64 10U/25V_8X
PC66 10U/25V_8X
PC70 10U/25V_8X
PR10 *0_2S
PR2 *0_2S
PR11 10/F_4
PC6 0.1u/10V/X5R_4
PR8 10/F_4
PR13 *0_4
PR111 100/F_4
CSOP-1
CSON-1
Pin3(T+/SW) is connected with Battery negative pole through 2.4K
PR114 *0/short_4
PR26 4.7K/F_4
PC75 0.01U/50V/X7R_4
PR122 113K/F_4
PR27 100K/F_4
88732-CCLIM
PR28 33K/F_4
PR120 *42.2K/F_4
PR123 *42.2K/F_4
Max Charge Current Limit=3.87 A
Hysteresis=128mA
PU1
MP1-9
PR117 *SHORT_4
ISENS_IN 37,38
4/1 updated
PC12 *1000P/50V/X7R/10%_4
PR119 *100K/F_4
PR118 *0_4
4/1 updated
Reserved
3V_S0
PR121 *0_4
PR21 *0_4
37 D/C#
PC16 *1000P/50V/X7R/10%_4
PQ4 *2N7002KDW
A+-7
PJ1
BATT+ VS T+/SW B/I SMBC SMBD B/I2 GND
BAT CONN
PC65 2200P/50V_4
PC63 0.1U/25V_4
PR7 *SHORT_4
PR6 220K_4
PR3 100R/4
PR4 100R/4
MBCLK0
MBDATA0
PC4 *47P/50V_4
ESD3 EGA10402V05AH
ESD1 EGA10402V05AH
ESD2 EGA10402V05AH
PC3 *47P/50V_4
PC2 *0.01U/50_4
PR5 1M_4
BATT_IN 37
ER3
PR108 *0_4
PD6 1SS355
PR107 100K/F_4
PR113 *0_4_SHORT
37 PMU_SCONT1
PQ9 2N7002K
PR112 *470K/J_4
4/1 updated
1.Level 1 Environment-related Substances Should Never be Used. 2.Recycled Resin and Coated Wire should be procured from Green Partners.
Quanta Computer Inc.
PROJECT : FH9
VIN/CHARGER-ISL88732
Size Document Number Rev 2A
Date: Wednesday, November 19, 2014 Sheet 38 of 48

System 3V / 5V (TPS51225RUKR)



Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number	Rev
	SYSTEM 5V/3V(TPS51225RUK)	2A
Date: Wednesday,, November 19, 2014	Sheet 39 of 48	

+1.05V



Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number	Rev
	1.05V-G5335	2A
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1.35V_VDDQ(RT8231AGQW)

4/1 upadted

3V_S5
PR212 *100K/F_4
Frequency around 400KHz
37 HWPG_1.35V
8231GND
18,37,42 S3_ON *SHORT_4 PR208 RT8231_S5
A+-23 B-50
18 DDR_PG PR210 *short_4
37,38,40,42 S0_ON_1 PR209 *0_4 RT8231_S3
PR218 165K/F_4
1.35V_CS
1.35V_TON PR211 620K/F_4
4/1 upadted
S3 S5 PGOOD CS TON
DDR_VTERM
1000mA
VTT VTTSNS VTTGND VTTREF VLDOIN
PC181 10u/6.3V/X5R/6
DDR_VTTREF
20mA
PC179 0.033U/10V_4
8231GND
PC183 10u/6.3V/X5R/6
PU9 RT8231AGQW
UGATE BOOT1 PHASE LGATE VDD
1.35V_UGATE
1.35V_BOOT PR219
1.35V_PHASE
1.35V_LGATE
PC182 1R_6 0.1U/25V_4
PC180 1U/10V_4
5V_S5
4/1 upadted
LPMB VID PGND FB VDDQ PAD
4/1 upadted
PR217 *0_2/S RT8131_PIN3
MP1-6
PR216 *SHORT_4
5V_S5
1.35V_VID
1.35V_FB
1.35V_VDDQ
PR214 10.2K/F_4
PR215 10K/F_4
8231GND
(Power GND for Low-Side MosFET)
VO=0.675*(R1+R2)/R2
PQ38 RQ3E070BNFU7TB <Part Type>
PQ37 RQ3E100BNFU7TB <Part Type>
Rdson 10.5m ohm
VIN_1.35V
EC29 *3.3P/50V/C0G_4
Reserve for RF
PC187 0.1U/25V_4
PC188 2200P/50V_4
PC184 10U/25V_8
PC186 *4.7U/25V_8
PL16 *Short_8
VIN
PC185 0.1U/25V_4
B-46
PL18 1.5UH/MMD-06CZ-1R0M-V1W
PR220 2.2R_8
PC189 2200P/50V_4
PR103 *0_2/S
EC31 *3.3P/50V/C0G_4
Reserve for RF
B-50
1.35V_S3
1.35V_1
PR239 *short_3720
PC204 0.1U/25V_4
PC203 560U/2.5V_R6_16
Peak current:6.364A(includ VTTERM and VTTREF)
OCP minimum:12A
RQ3E120ASFU7TB Rdson=10.5mOhm
1.35V_VDDQ OCP:12A 400K
8231GND PR99 *short
4/1 upadted

Quanta Computer Inc.
PROJECT : FH9

Size	Document Number	Rev
	DDR3L 1.35V(RT8231AGQW)	2A
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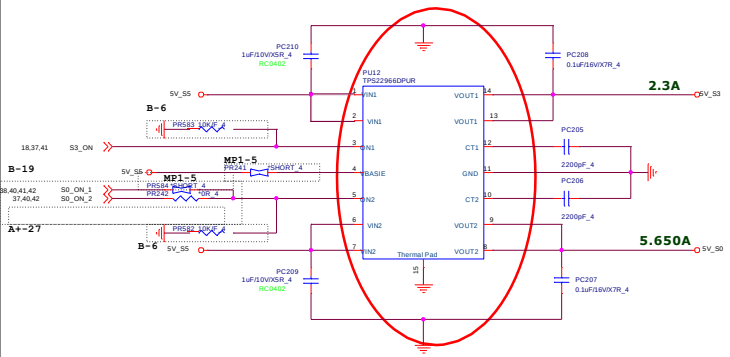
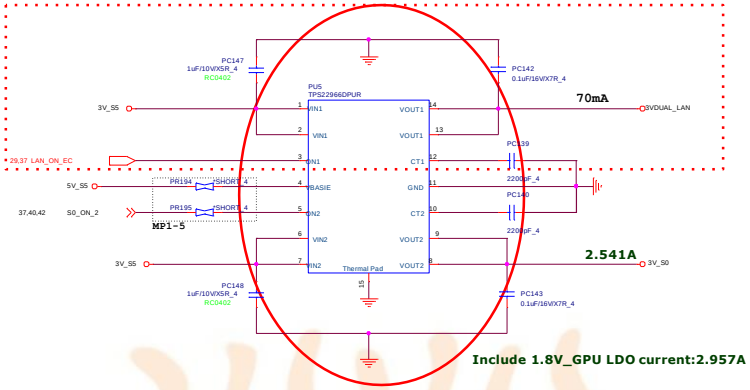
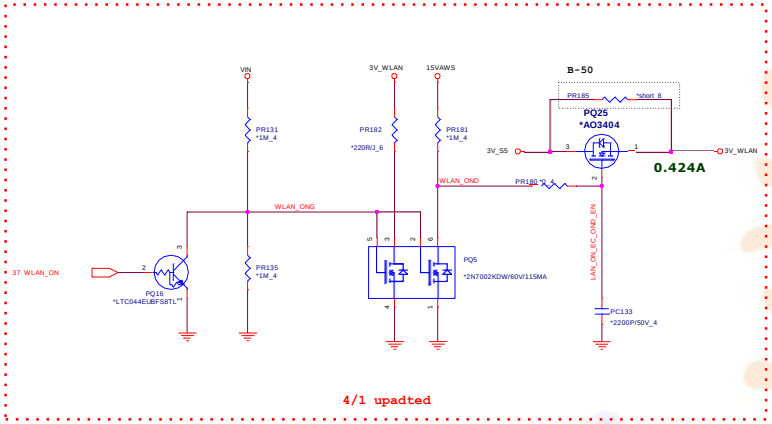
No footprint



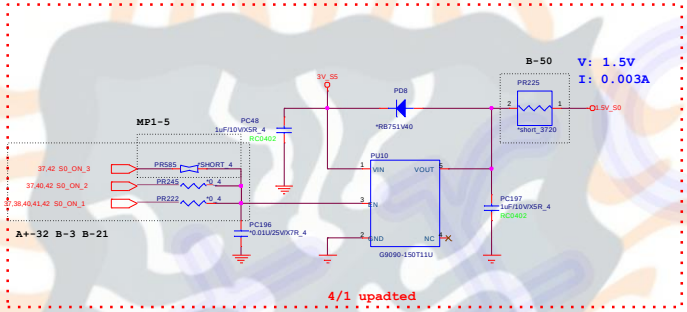
04/14 updated No footprint



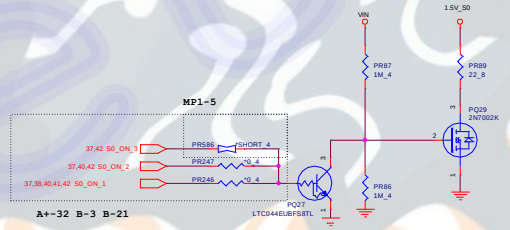
Include 1.8V_GPU LDO current:2.957A



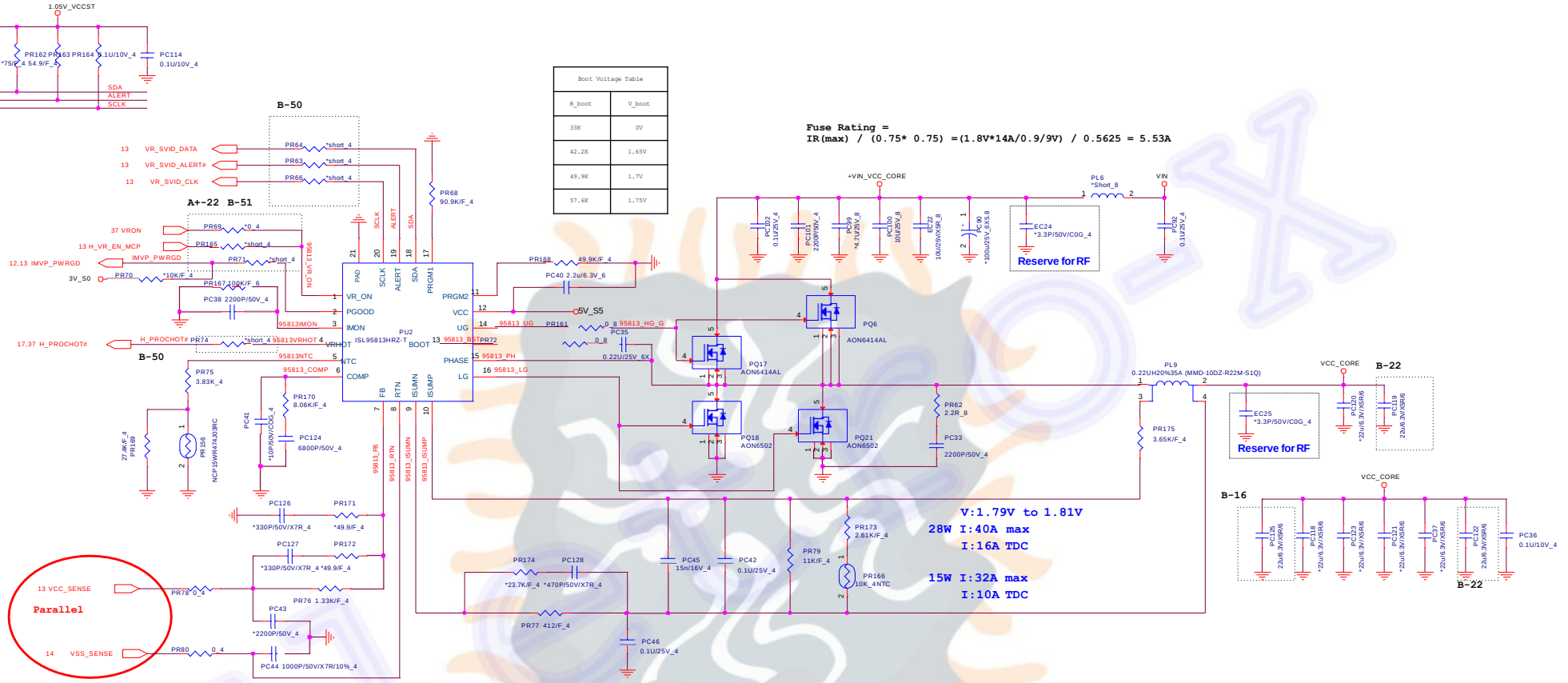
4/1 upadted



4/1 upadted



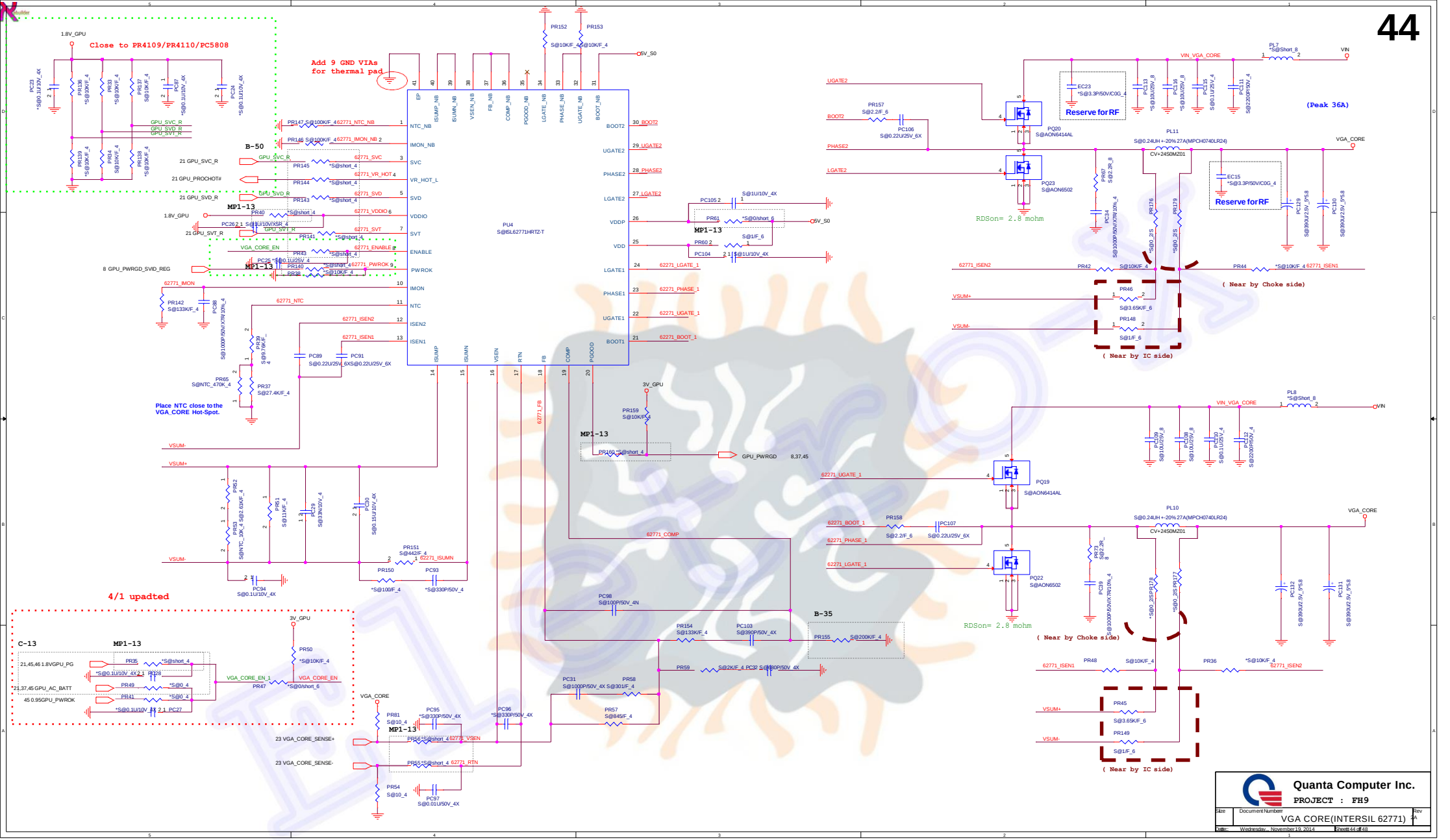
Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number	Rev 2A
	SWITCH	
Date: Wednesday, November 19, 2014	Sheet 42 of 48	

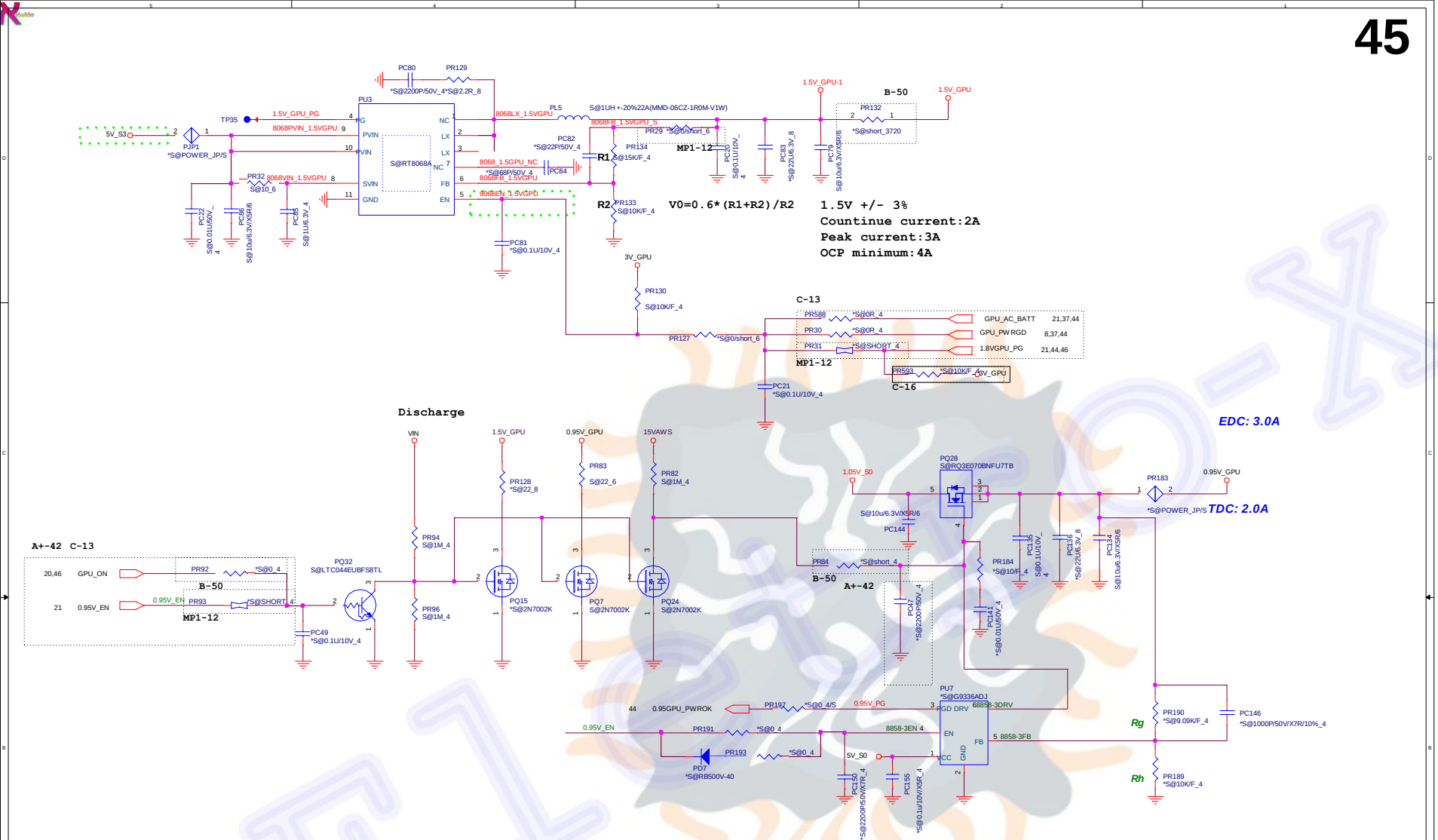


		28W	15W
B-41	(Iccmax)	PR68	113K(CS41132FB17)	90.9K(CS39092FB11)
	(IMON)	PR167	105K(CS41053F919)	100K(CS41003F932)
	(Loadline)	PR76	1.65K(CS21652FB29)	1.33K(CS21332FB11)
	(OCP)	PR77	510(CS15102FB19)	412(CS14122FB15)

1.Level 1 Environment-related Substances Should Never be Used. 2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FH9
Size | Document Number | Rev
CPU Core (ISL95813HRZ-UL)
Date: Wednesday, November 19, 2014 | Sheet


Close to PR4109/PR4110/PC5808
Add 9 GND VIAs for thermal pad
B-50
MP1-13
PU4
S@ISL62771HRTZ-T
NTC_NB
IMON_NB
SVC
VR_HOT_L
SVD
VDDIO
SVT
ENABLE
PWROK
IMON
NTC
ISEN2
ISEN1
ISUMP
ISUMN
VSEN
RTN
FB
COMP
PGOOD
VDDP
VDD
LGATE1
PHASE1
UGATE1
BOOT1
UGATE2
PHASE2
LGATE2
BOOT2
5V_S0
3V_GPU
1.8V_GPU
VSUM+
VSUM-
62771_ISEN1
62771_ISEN2
62771_NTC
62771_IMON
62771_FB
62771_COMP
62771_ISUMN
62771_VSEN
62771_RTN
62771_PHASE_1
62771_UGATE_1
62771_LGATE_1
62771_BOOT_1
GPU_PWRGD
8,37,45
VGA_CORE_EN
VGA_CORE_EN_1
Place NTC close to the VGA_CORE Hot-Spot.
4/1 upadted
C-13
B-35
PQ19
S@AON6414AL
PQ22
S@AON6502
PQ20
S@AON6414AL
PQ23
S@AON6502
PL11
S@0.24UH +-20%27A(MPCH0740LR24)
CV+24S0M201
PL10
S@0.24UH +-20%27A(MPCH0740LR24)
CV+24S0M201
VIN_VGA_CORE
VGA_CORE
VIN
Reserve for RF
(Peak 36A)
RDSon= 2.8 mohm
(Near by Choke side)
(Near by IC side)



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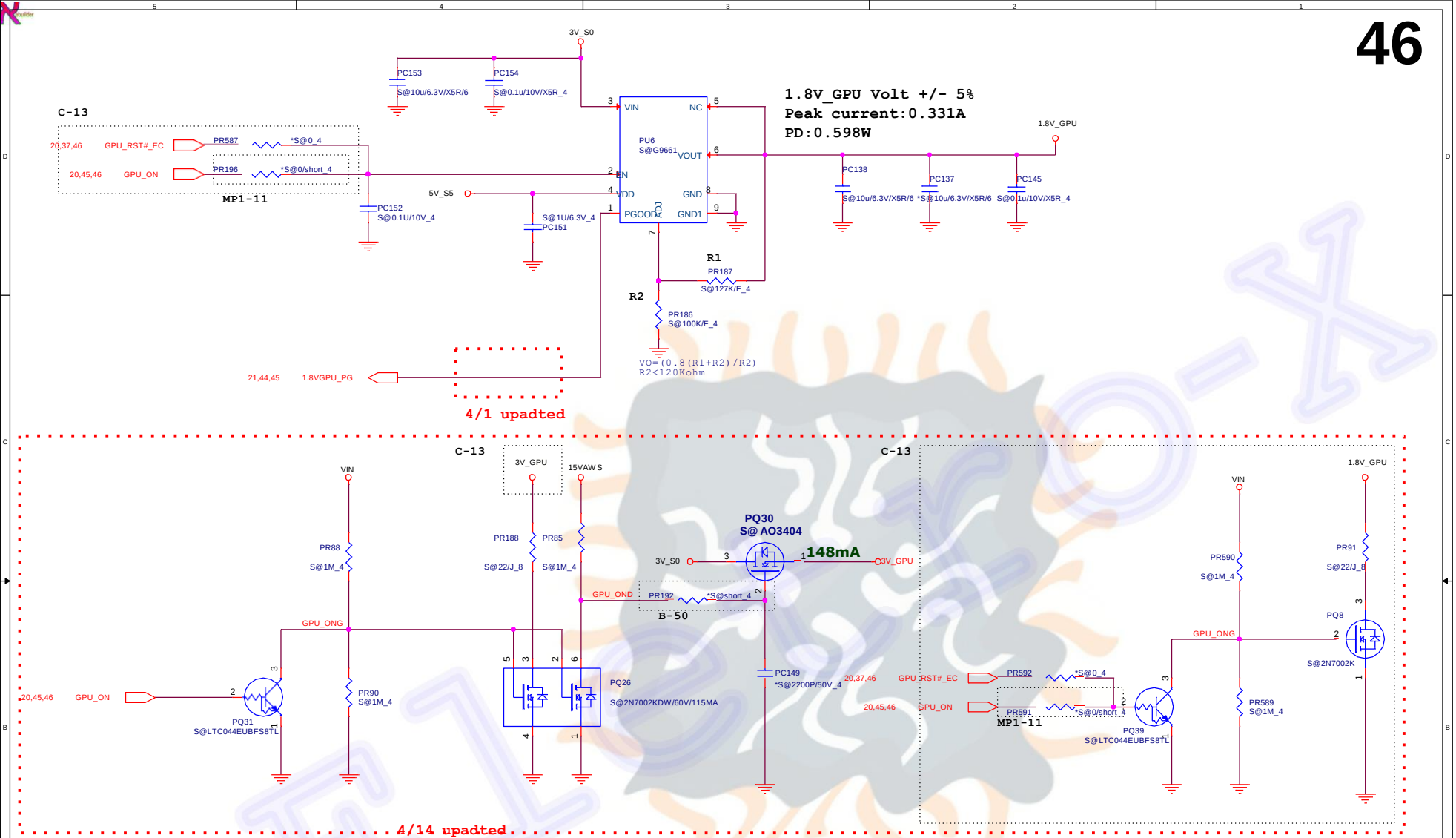

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Change List

Item	Stage	Page	Owner	Change explanation
01	A->A+	36	FJ	delete R458, change SUSC# control for unstable when mouse_on is High SUSC# is LOW
02	A->A+	32	HW	change CN12 footprint to 50501-00801-001-8p-l
03	A->A+	34	HW	change CN21 footprint to 50501-0150n-001-15p-l
04	A->A+	36	HW	change CN9 FP to 50501-0120n-001-12p-l
05	A->A+	29	ESD	change L3~L6 PN to CY4500Q2Z00, F/P to qfn2-3_3x3_3-2_77 for ME hight limit
06	A->A+	23	HW	change L15 PN to CX5PX181000, F/P to f1x0_5-0_8 for DGS STD part
07	A->A+	38	PWR	change PJ1 F/P to bat-btd-08cabdab-8p-l for DFAD08MR071
08	A->A+	12,17,29 35,37	ESD	change D3,D4,D5,D6,D8,D16,D27,D28,D35 PN to BC512301Z02, F/P to d-1x0_6-0_6h for DGS STD part
09	A->A+	37	EE	exchange EC signal: GPU_ON_EC & FAN1_PWM for FAN DAC control
10	A->A+	28,32,34 35,36	EMI	exchange LP1~LP8 PN to CX12B900000, F/P to choke-dlw21s-4p for STD part
11	A->A+	32	ESD	change U37,U38,U40 PN to BC106506000, F/P to esd10-4_1x2-8-11p for STD part, reserve EC622~624 ,and DEL U14,U36
12	A->A+	23	EE	change L12,L13 PN to CX121T03000, F/P to RC0402 for STD part
13	A->A+	27	EE	change L22 PN to CX08T600000, F/P to RC0603 for STD part
14	A->A+	21	EE	change L27 to 0ohm_6 for AMD CRB no request
15	A->A+	26	EE	Change connection around D26 for solve when "5V_HDMI" to GND short, D26 will break at first
16	A->A+	26	EE	change D25 PN to BCRB500VZ29, F/P to DSM for STD part
17	A->A+	38	PWR	change PC7 F/P to CC0603
18	A->A+	12	EE	Delete D/C# to AC_PRESENT through R243, will cause D/C# lock unknow state.
19	A->A+	39	EE	change PR234 to 8.8K(CS38872FB18) to modify the OCP of 3V_S0
20	A->A+	10	EE	reserve R575,R576 for GREEN CLK & X'TAL option PWR
21	A->A+	31		connect AU1.49 to GND for better disssipate heat
22	A->A+	43	EE	stuff PR165(CPU control), unstuff PR69(EC control),for CPU contol VR-EN power sequency EE
23	A->A+	41		stuff PR210(DDR_PG control), unstaff PR209(S0_ON_1),for contol DDR_VTERM power sequency
24	A->A+	16	EE	unstuff C312 only reserve for WW15 4/10 Intel VCCDSW3 G3 can't boot issue.
25	A->A+	32	SMT	change C547 F/P to ECAP6_3X6_1-7_2 for solve SMT solder open easily issue
26	A->A+	26	EE	change L16,L18,L19 F/P to RC0402 for CVA6802JN17
27	A->A+	27	EE	reserve S0_ON_3 for control 5V_S0 to meet intel DGS power sequency
28	A->A+	34	EE	change PWR/B LED controled by PWRLED0#
29	A->A+	16	EE	reserve (R577, R578)1.5V_S0 for VCCHDA by intel :If the circuit is designed and configured for HD Audio VCCHDA should be connected to 3.3V or 1.5V
30	A->A+	31	EE	reserve Audio Codec DVDD-IO to 1.5V_S0 (AR22), default stuff AR27 (3V_S0)
31	A->A+	40	EE	reserve S0_ON_1(PR244) to control 1.05V_S0
32	A->A+	41	EE	reserve S0_ON_2(PR245,PR246,PR247) to control 1.5V_S0
33	A->A+	20	EE	reserve GPU_ON_EC(R579) to control GPU_ON directly
34	A->A+	31	EE	change CN20 F/P to 50501-00801-001-8p-l
35	A->A+	32	EE	change F5 P/N to DK300WFU007, F/P to f3_18x1_52-2_665
36	A->A+	10	EE	change D34 P/N to BCBAT54CZ01, F/P to sot323_213-2_1-1_3-bat54sw-7-f and delete D36 for DGS EE
37	A->A+	33		change WLAN LED power source to 5V_S5 by FJ SPEC
38	A->A+	34	EE	change PWR/B LED power source to 5V_S3 by FJ SPEC
39	A->A+	39	PWR	change PR238 to 84.5K
40	A->A+	21	EE	add Topaz PS_3 bits strap table
41	A->A+	23	EE	Change L10,L23 PN to CX8PG121009 for RDC STD parts
42	A->A+	45	EE	un-stuff PC47, PR93, Stuff PR92(0.95V_GPU control by GPU_ON) for GPU power sequency. EE
43	A->A+	23	DEL	net alias BIF_VDDC. DEL VMEMIO power symbol for same net name.
44	A->A+	21	EE	unstuff R95,R85,R90,C159 for 3V_GPU leakage from EC
45	A->A+	39	EE	unstuff PR229,PR231,stuff PR232,PR228 for 3V_S0 have leakage level while AC is inserted
				B stage
1	A+->B	21,37	EE	delete R95, add Q33 on GPU_AC_BATT to avoid 3V_GPU leakage from EC. Change GPU_AC_BATT# net name to GPU_AC_BATT.Reserve R580 PU to 3V_S0 for GPU_AC_BATT. delete GPU_PROCHOT# control from EC and add GPIO as TP90, stuff C159, R85 to avoid 3V_GPU leakage from EC.
2	A+->B	16	EE	change +VCC_DSW net name to 3V_S5 for same net.
3	A+->B	40,42	EE	Stuff PR244, un-stuff PR201, 1.05V_S0 controled by S0_ON_1; stuff PR245,PR247, un-stuff PR246,PR222, 1.5V_S0 controled by S0_ON_2
4	A+->B	40,43	EE	Stuff PR244, un-stuff PR201, 1.05V_S0 controled by S0_ON_1; stuff PR245,PR247, un-stuff PR246,PR222, 1.5V_S0 controled by S0_ON_2
5	A+->B	31,37	PWR	Add AU3,AR28,AR29,AC40,AC41,AC42 for Audio codec sequence. EC add LDO enable pin AUD_1.5_ON.
6	A+->B	42	PWR	Add PR583,PR582 for S3_ON/S0_ON_2 PD for pulse issue.
7	A+->B	28	EE	un-stuff R1,R4,C1,U2, stuff R5 for LVDS BOM for H/W C/D.
8	A+->B	10,11,29	EE	un-stuff Y3,Y5,R359,R503,C456,C457,C520,C522; change R62 to RC0402 unstaff & add R581 for green CLK solution.
9	A+->B	9,10,11, 12,13,16, 17,18,19, 20,21,23, 28,29,30, 33,35,36, 37	EE	change 0 ohm to shrot pad for SMT rule: R120; R489,R355,R439;R438,R190,R420,R358,R484,R451, R444,R481,R482;R527,R188,R522,R497,R203,R531,R199,R525,R223;R449,R436,R141,R132,R178,R173,R410; R387,R196,R172,R508,R140,R116,R248,R182,R499;R253;R551;R548,R542;R381;R328,R98,R353,R360,R349, R332,R330,R105,R104;R342;L2,L1;R17,R16,R11,R12,R60;R573;R136,F3;R567,R568;R383;L17,R426,L14, R425,R404,R334,R361,R119.
10	A+->B	29	ME	change CN4 to 10pin (DFWF10MR004) for STD part
11	A+->B	34	ME	change CN2 to DFFC08FR031, F/P to 50501-00801-001-8p-l
12	A+->B	34	ME	change CN3 to DFFC06FR050, F/P to 88194-0641-6p-l
13	A+->B	35	ME	change CN6 to DFFC30FR093, F/P to 50696-0300m-001-30p-l, change CN8 to DFFC30FR093, F/P to 50696-0300m-001-30p-l
14	A+->B	21	EE	change C203,C208 to 10p for X'tal
15	A+->B	37	EE	change R343,R352 to 4.7K for EC sometime can not detect GPU thermal
16	A+->B	43	EE	Stuff PC125 for USB3.0 can't reconize device issue
17	A+->B	31	EE	un-stuff AR29,AC40,AU3,AC42, stuff AR30 for audio codec 1.5V power change to 1.5V_S0
18	A+->B	21	EE	un-stuff R346, Q17, stuff Q17 for GPU S3,S4 will wake up.
19	A+->B	37,42	EE	un-stuff PR242, add PR584, del PR243, change 5V_S0 control by S0_ON_1 , change EC S0_ON_3 to TP54
20	A+->B	36	EE	change C511 to 12p for X'tal
21	A+->B	37,42	EE	change 1.5V_S0 controled by S0_ON_3: ADD PR585,PR586
22	A+->B	43	EE	stuff PC119, PC122 for USB3.0 TSSC
23	A+->B	37	EE	Del EC EC_Board ID, change to TP90 for unuse pin.
24	A+->B	10	EE	stuff Q25 and add R582 for EC clear CMOS.
25	A+->B	11	EE	change R451,R444,R481,R418,R430,R483 to 33ohm for SPI signal waveform.
26	A+->B	38	PWR	change PJ2 pin define for FJ in common use
27	A+->B	31	PWR	change CN20 to 10 pin & add sleeve, ring2 pin for MIC cross talk issue
28	A+->B	35	EE	reverse CN8(low SKU) KB CON for ME change location form BOT to TOP
29	A+->B	28	EE	change HDMI level shifter to PS8407A for 4Kx2K eye diagram fail
30	A+->B	37	EE	ADD High SKU,LOW SKU BOARD ID for MMB
31	A+->B	40	PWR	PR206 change to 6.49K
32	A+->B	28,32	EE	change USB LP1,LP6,LP7,LP8,LP2 to 0 ohm for C/D
33	A+->B	23	EE	add 22uF(C621) for 1.5V_GPU ripple, add 470uF*2(C622,C623) for VGA_CORE ripple.
34	A+->B	08	BIOS	cahnge to GPIO46 reserve GPIO49 as SMI event control pin for more customer request function.
35	A+->B	44	PWR	cahnge PR155 to 200K ohm for VGA_CORE offset.
36	A+->B	28	EE	cahnge LCD conn power & signal pin define to avoid RTD2132 damaged.
37	A+->B	11	EE	change R213, R274 to 1K & R480, R465 to 499 ohm for NFC fast mode.
38	A+->B	11	EE	DEL Y3,C456,C457,R359,R367,R368 and ADD T54 for VCC_CORE layout spacing.
39	A+->B	31	PWR	Reverse CN20 pin define for typo.
40	A+->B	26	EE	change EC16,EC17,EC18,C237,C242,C256 to 5p for VSIS fine-tuned.
41	A+->B	43	PWR	change PR167 to 105K(CS41053F919) for Imon adjustment
42	A+->B	34	EE	change CN3 FP to 50506-00641-v01-6p-l
43	A+->B	16	EE	follow PDG:change C444,C448,C445,C452 22F, unstuff C443,C446,C449,C454
44	A+->B	36	ME	change H16 FP to H-FH8-2
45	A+->B	35	ME	change CN5 to DFHD10MS119 and reverse pin define.
46	A+->B	41	PWR	Change PL18 to CV-10M0MZ02 for Standard part
47	A+->B	42	PWR	change CN20 for SCH & BRD pindefine not mactch.
48	A+->B	36	ME	change H16 FP back to H-TC256BC185D146P2, H26 to H-FH8-2, H3 to H-TC181BIC102D102P2, H4,H8,H15,H20 to H-C315D126P2, H9 to H-TC315BC236D126P2, H10 to H-TC315BC217D110P2, H14 to H-FH8-3, H29 to H-O181X173D102X94P2,H32 to H-TC315BC394D126P2, H31 to H-TC197BC256D150P2, H33 to H-C394D126P2, H34 to H-C394D126P2, for layout
49	A+->B	36	ME	change H18 FP to H-FH8-4, H21 to H-FH8-6, H27 to H-FH8-5, H30 to H-FH8-7
50	A+->B	39,40,41 42,43,45 46,44,32 29	EE/PWR	change PR98,PR213,PR205,PR200,PR239,PR210,PR225,PR185,6P,R63,PR64,PR66,PR165,PR71,PR74,PR132 PR31,PR196,PR192,PR84,PR92,PR35,PR145,PR144,PR143,PR141,PR43,R532,R533,R534,R535,R267,R269 R267,R502,R500,R310,R68 to short PAD
51	A+->B	39	PWR	change PC50, PC51 to 0.1uF/0402
52	A+->B	31	PWR	unstuff AR13,AR14,AC23,AC24,AC25,AC32,AC39 for audio noise.
53	A+->B	34,35	ME	change PWR CONN(CN3) to DFFC06FR106 , High SKU KB CON(CN6) to DFFC30FR091
54	A+->B	34	EE	Del TP83,TP84,TP85,TP86,TP87,TP88
55	A+->B	31	EE	change to short pad: AR17,AR18,AR19,AR27,R289,R288,R30,R32
56	A+->B	28	EE	change HU1 to PS8201A & R221 to 3.3K ohm for C/D
57	A+->B	31	PWR	change AQ1,AQ5 F/P to sot323_213-2_1-1_3-1_1h
58	A+->B	36	ME	Del H17
59	A+->B	36	ME	change H9 F/P to H-TC315BC276D126P2, H10 to H-TC335BC217D110P2
60	A+->B	39	PWR	change PU11 to TPS51225CRUKR(AL051225001) for MMB
61	A+->B	38	EMI	reserve EC625-EC630 for EMI
62	A+->B	30	EE	change C609 to 10uF for vender suggest.
63	A+->B	29	EE	Unstuff C421 & C427 for vender suggest
64	A+->B	38	PWR	Del EC14 for ME request
65	A+->B	36	ME	change H31 F/P to h-tc217bc256d150p2
66	A+->B	36	ME	change H31 F/P to h-tc197bc256d150p2
67	A+->B	26	EE	change R371 & R401 to 2.2K for verder suggest.
68	A+->B	13	EE	stuff R454,R435,U30,C487,C499; un-stuff R453,Q23,C495; change R448 to 10k ohm for VCCST_PWRGD to VR_EN timing.
69	A+->B	11	EE	change R474,R463 to 33 ohm, R451,R444,R481 to 0 ohm for SPI signal quilty.
				C stage
1	B->C	10	EE	unstaff R582 for PDTC144EU already have internal PD.
2	B->C	34	ME	Change CN3 to DFFC06FR050 for ASSY. line request ME change connector type.
3	B->C	33	EE	change R285,R278,R282,R280,R286,R287 to 150 ohm, R281,R279 to 220 ohm for LED brightness. EE
4	B->C	32		change F5 to DK260TPU003, F/P to f1812 for STD parts.
5	B->C	35	ME	change CN8 to DFFC30FR091, F/P to 50541-0300n-001-30p-l for ASSY. line request.
6	B->C	37	EE	swap U27 AMP_MUTE# & CLR_CMOS (pin 108 & 2) for G3 boot to S0 will have a pluse to clear CMOS.
7	B->C	34	EE	change CN3 F/P to 50506-00641-v01-6p-l for DGS.
8	B->C	26	EE	change EC16,EC17,EC18,C237,C242,C256 to 2pF for VISI.
9	B->C	13	EE	change R449,R436 to 0ohm and un-stuff, R454, R435 to short PAD for reducing 0ohm.
10	B->C	16	EE	change R337 to 0 ohm from short pad for follow intel CRB add 0ohm.
11	B->C	37	EE	change D24 direction for ME can't unlock issue
12	B->C	28	EE	change JLCD1 F/P to 51519-04001-001-40p-L for DGS change

Item	Stage	Page	Owner	Change explanation
13	B->C	44,45,46	EE	for reserve EC control GPU power sequence: PR92 change to 0ohm un-stuff, PR93 change to 0ohm stuff. PR196 change to 0ohm stuff. reserve PR587 for GPU_RST#_EC control. add dis-charge SCH for option. PR31 change to 0ohm and reserve PR588 for GPU_AC_BATT control 1.5V_GPU. PR35 change to 0ohm stuff, VGA_CORE reserve control 0.95_EN change to GPU_AC_BATT.
14	B->C	32	EE	stuff U37,U38,U40 for USB3 ESD solution
15	B->C	36	ESD	change H20 F/P to H-C315IC285D126P2for ESD request.
16	B->C	45	EE	reserve PR593 PU to 3V_GPU.
17	B->C	36	ME	change H31 F/P to H-TC236BC185D146P2, H11,H19 to H-TC217BC185D146P2 , H31 to H-TC256BC197D150P2 for ME change
18	B->C	36	ME	change H13 F/P to H-TC217BC185D146P2 for ME change.
19	B->C	36	ME	change H20 F/P to H-C315IC250D126P2 for ME change.
20	B->C	34,35,36	EE	change R380,R379,R290,R291,R441,R442 to short pad, un-stuff LP3,LP4,LP5 for C/D.
21	B->C	28	EE	change HU1 to PS8407A and R221 to 4.99Kohm for HDMI EA item 7-10
22	B->C	38	EMI	Reserve EC38, EC39(10u/25V) on CS_IN
23	B->C	16	EE	Change the cap's value of C265,C273,C257,C251,C451,C455 from 4.7U/6.3V_4 to 47U/4V_6 And del C290, C252, C450 for meet Intel DG suggestion
24	B->C	28	EE	cahnge F1 to DK200UFU002 for PDC suggest DGS.
25	B->C	31	PWR	change AR12,AR25 to 0ohm, AL6,AL7 to 47ohm for pop noise.
				MP1 stage
01	C->D	10	EE	R506 change short PAD from 0 ohm for cost down
02	C->D	11	EE	R432 change short PAD from 0 ohm for cost down
03	C->D	16	EE	R578 change short PAD from 0 ohm for cost down
04	C->D	34	EE	R466 change short PAD from 0 ohm for cost down
05	C->D	42	PWR	PR194/PR195/PR584/PR241/PR586/PR585 change short PAD from 0 ohm for cost down
06	C->D	41	PWR	PR216 change short PAD from 0 ohm for cost down
07	C->D	39	PWR	PR221/PR232/PR227/PR228 change short PAD from 0 ohm for cost down
08	C->D	31	ADO	AR1/AR2/AR3/AR4/AR30 change short PAD from 0 ohm for cost down
09	C->D	38	PWR	PR117/PR7 change short PAD from 0 ohm for cost down
10	C->D	40	PWR	PR203/PR244 change short PAD from 0 ohm for cost down
11	C->D	46	PWR	PR591/PR196 change short PAD from 0 ohm for cost down
12	C->D	45	PWR	PR29/PR31/PR93 change short PAD from 0 ohm for cost down
13	C->D	44	PWR	PR40/PR140/PR35/PR160/PR56/PR55/PR61 change short PAD from 0 ohm for cost down
14	C->D	36	ME	CN9 change PN to DFFC12FR117 & DFFC12FS000 , and F/P to 50501-01201-001-12p-l for ME request.
15	C->D	32,34	ME	CN2,CN12 change PN to DFFC08FR093 & DFFC08FR055,F/P to 50501-0080n-001-8p-l for ME request.
16	C->D	31	ME	CN20 change PN to DFFC10FR123,F/P to 51619-0100n-001-10p-l for ME request.
17	C->D	34	ME	CN21 change PN to DFFC15FR010 & DFFC15FR013, F/P to 50501-01541-001-15p-l for ME request.
18	C->D	36	ME	H11,H19 change PN to FBAJ2003010 for ASSY request.
19	C->D	34	ME	CN3 change PN to DFFC06FR177 & DFFC06FR172,F/P to 50506-0060n-v01-6p-l for ME request
20	C->D	35	ME	CN22 add 2nd source PN DFFC06FR179 for ME request
21	C->D	35	ME	CN5 change to DFHD10MS236 & DFHD10MS235 for ME request
22	C->D	36	ME	CN4 change to DFHD10MS237 & DFHD10MS238, F/P to 50273-01001-001-10p-l for ME request
23	C->D	40	EE	PU8 del pin24.25 for layout symbol change EE
24	C->D	30		CN1 DFHD11MR028 EOL, change to DFHD11FR163
25	C->D	35	EE	CN17 change to DFHS12FS032,F/P to 50169-01241-002-12p-ldh for SMT add Mylar

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