MS-7687 Version :1.0

CPU :

INTEL Sandy Bridge Processor

System Chipset :

INTEL Cougar Point Chipset

On Board Chipset :

VRM 12 -- NCP6151S52
Gigabit LAN -- RTL8111E-VB-GR-RH
HDA Codec -- Realtek ALC662
Super I/O -- SIO-NCT6776F
SPI Flash 32Mb

Main Memory :

2 Channel DDR III * 2(Max 8GB)

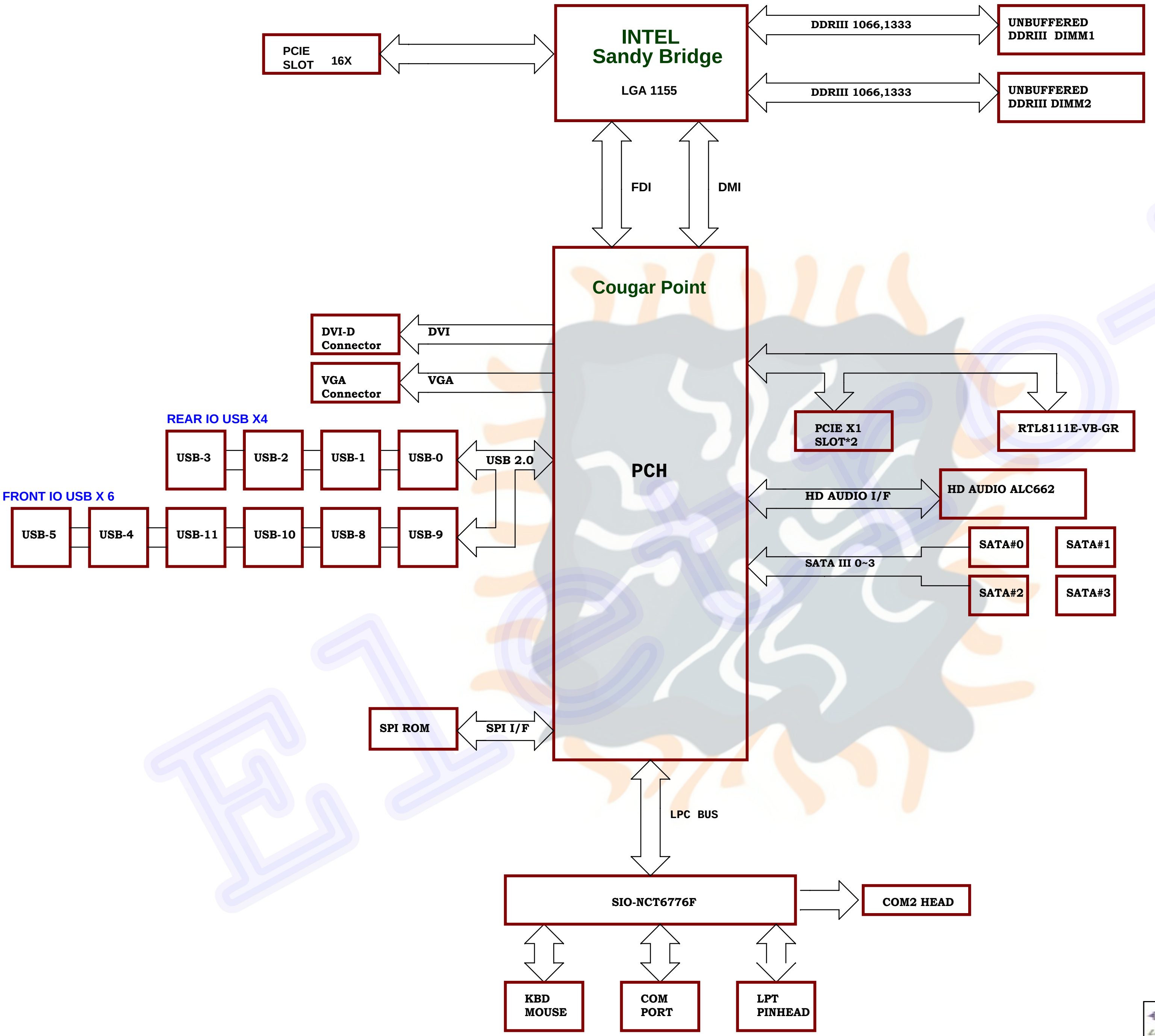
Expansion Slot :

PCI Express x16 Slot * 1
PCI Express x1 Slot * 2

lenovo

MICRO-START INT'L CO.,LTD.

Title	Cover Sheet	
Size	Document Number: Lenovo IH61M	Rev 1.0
Date: Wednesday, February 23, 2011	Sheet 1	of 33



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title		
Block Diagram		
Size	Document Number: Lenovo IH61M	Rev: 1.0
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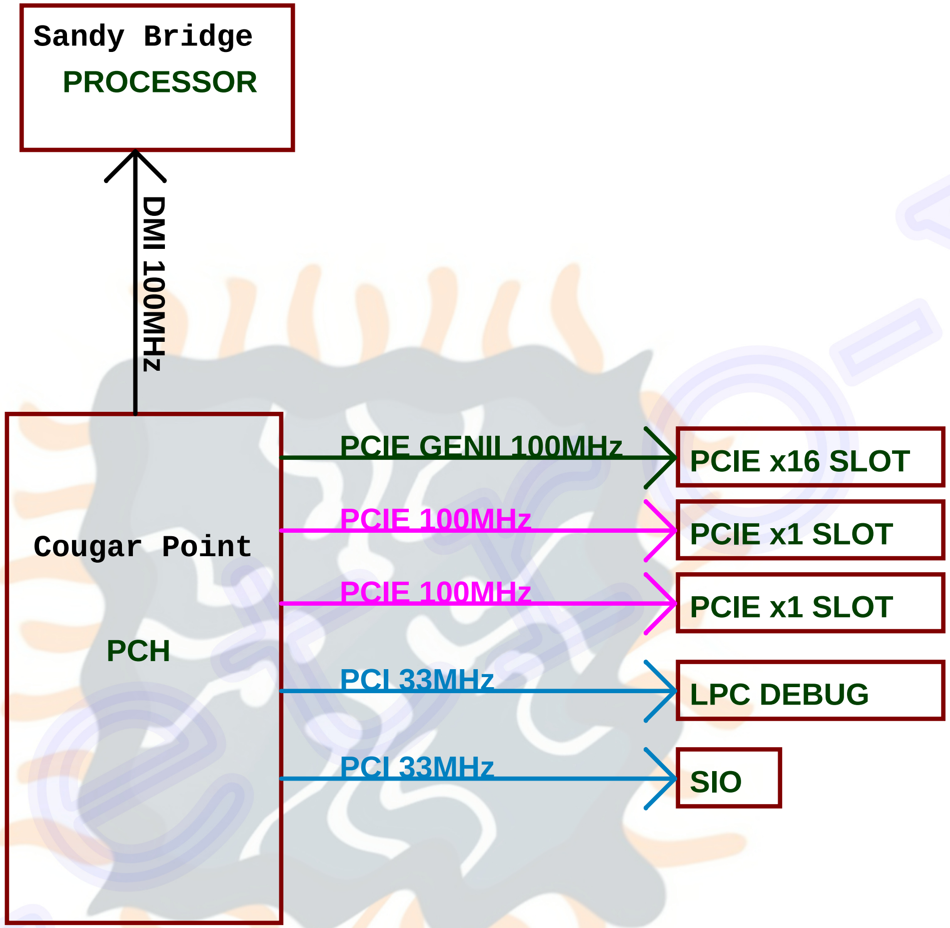
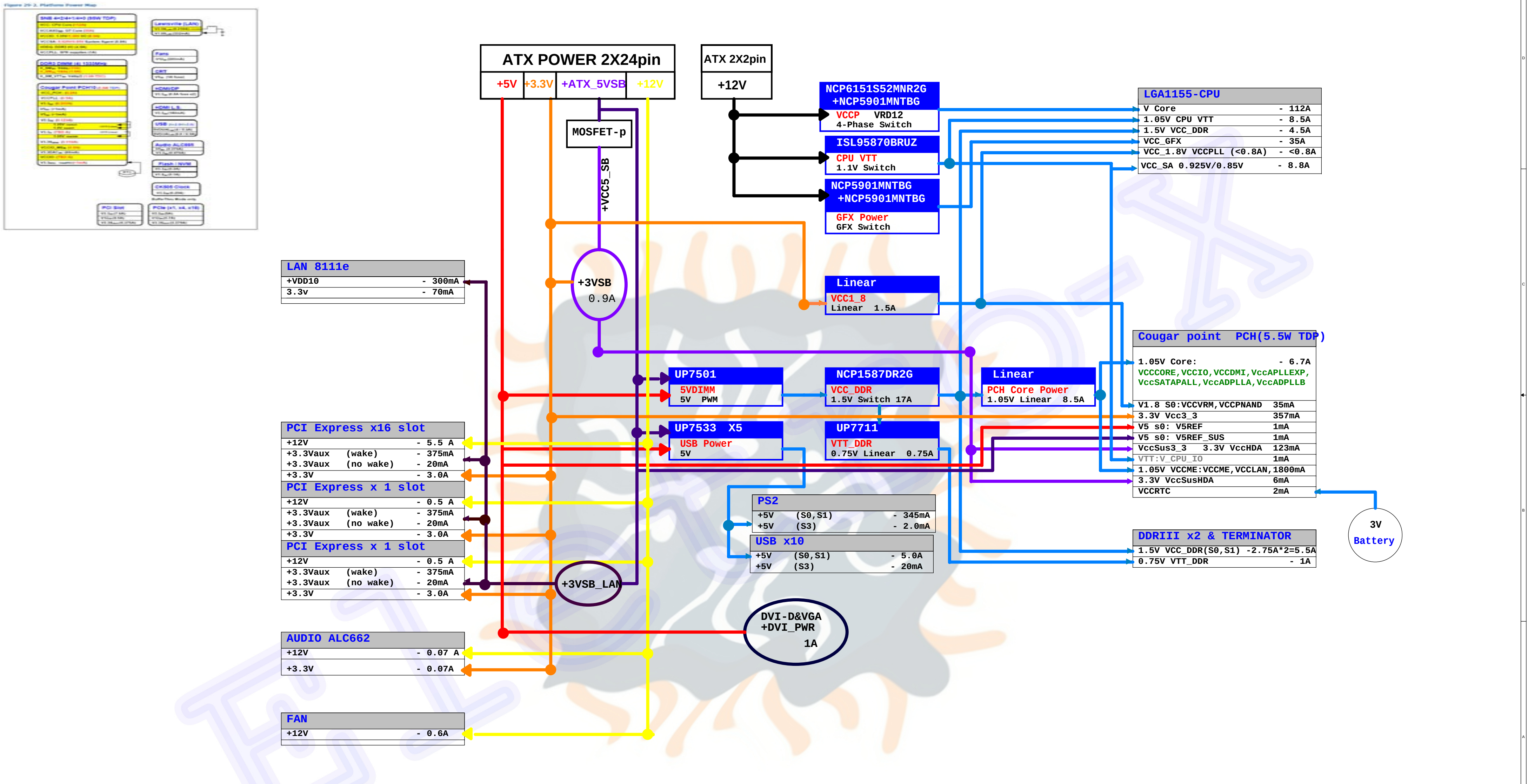


MSI MICRO-START INT'L CO.,LTD.

Title	Clock MAP	
Size	Document Number: Lenovo IH61M	Rev 1.0
Date: Wednesday, February 23, 2011	Sheet 3 of 33	



MSI MICRO-START INT'L CO.,LTD.

Title	Power comsumption	
Size	Document Number: Lenovo IH61M	Rev 1.0
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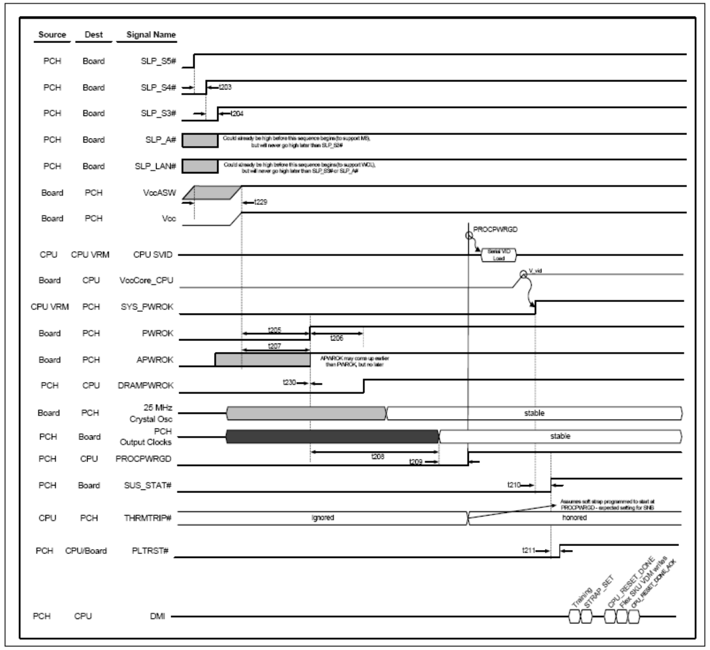
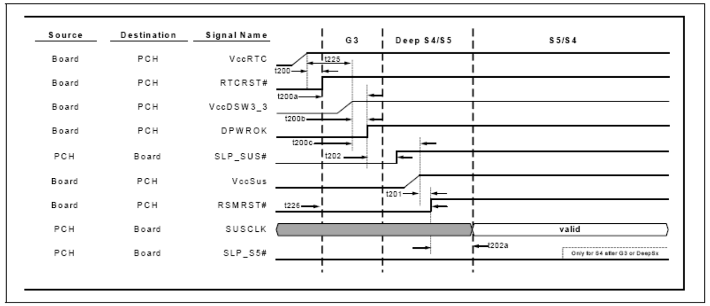
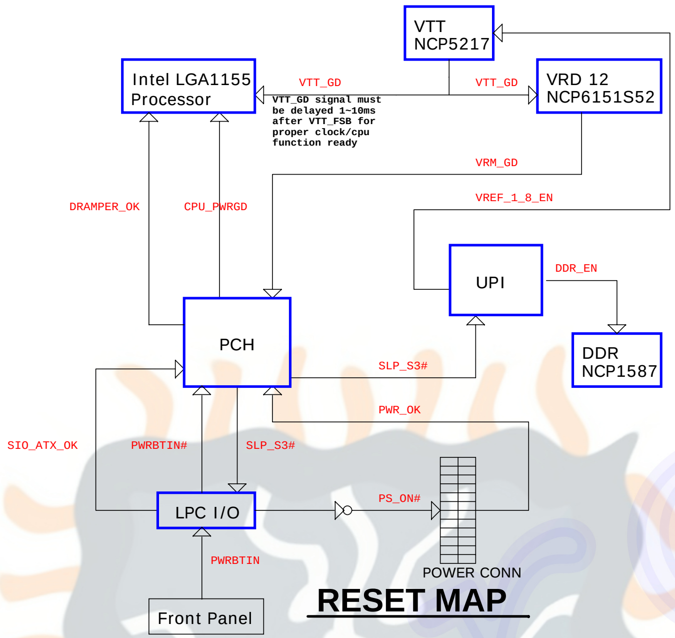
PWROK MAP

S5 to S0 Timing Diagram

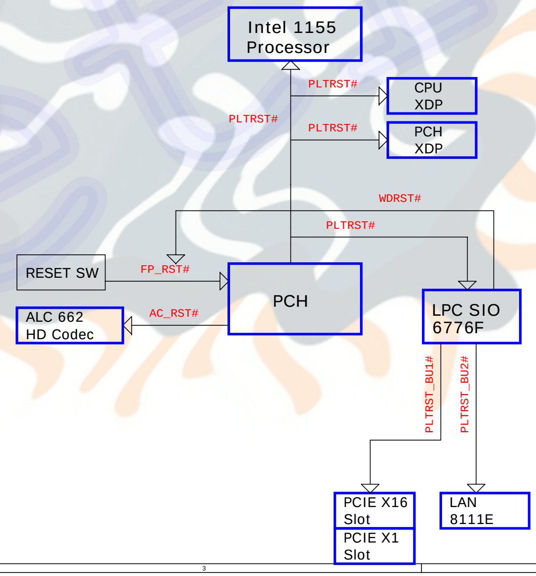


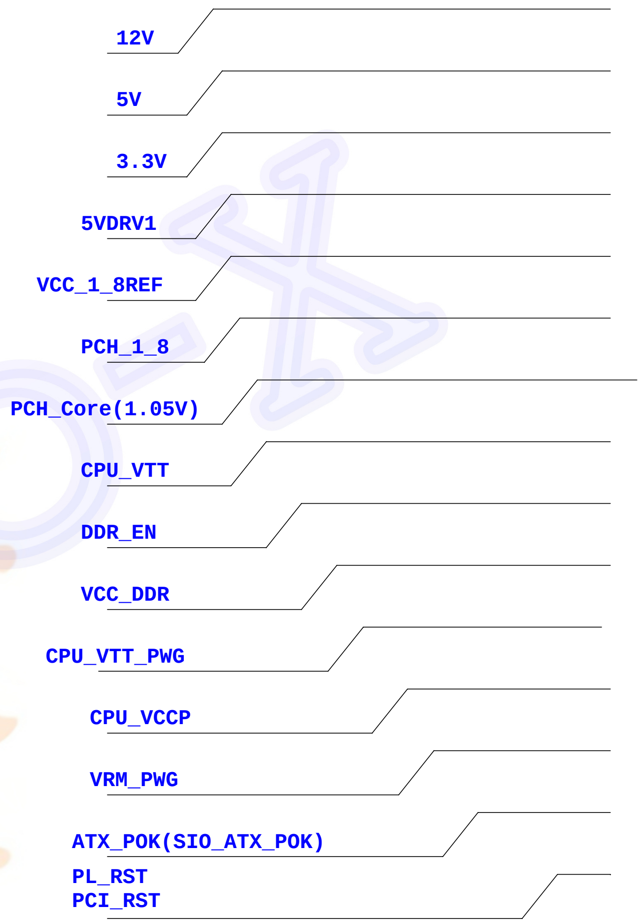
G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram





RESET MAP





MSI	MICRO-START INT'L CO.,LTD.
Title	Reset & PWROK map
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Table 2-27. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled low

Table 2-27. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT3# / GPIO55	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (Cougar Point inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high
GNT1#/ GPIO51/	Boot BIOS Strap bit 1 BBS1	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. **NOTE:** PCI Boot BIOS destination is not supported on Mobile

Table 2-27. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
SATA1GP/ GPIO19	Boot BIOS Strap bit 0 BBS0	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. **NOTE:** PCI Boot BIOS destination is not supported on mobile.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.

Table 2-27. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Port B Detected	Rising edge of PWROK	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts. **NOTE:** This signal should not be pulled high when strap is sampled.

NOTE: See Section 3.1 for full details on pull-up/pull-down resistors.

Table 2-27. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of RSMRST#	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. **NOTE:** The weak internal pull-down is disabled after PLTRST# deasserts. **NOTE:** Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	This signal has a weak internal pull-up. **NOTE:** The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. **NOTE:** The weak internal pull-down is disabled after RSMRST# deasserts. **NOTE:** A strong pull-up may be needed for GPIO functionality **NOTE:** This signal must be pulled up to support Intel RPAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.

Title: History		
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PCH

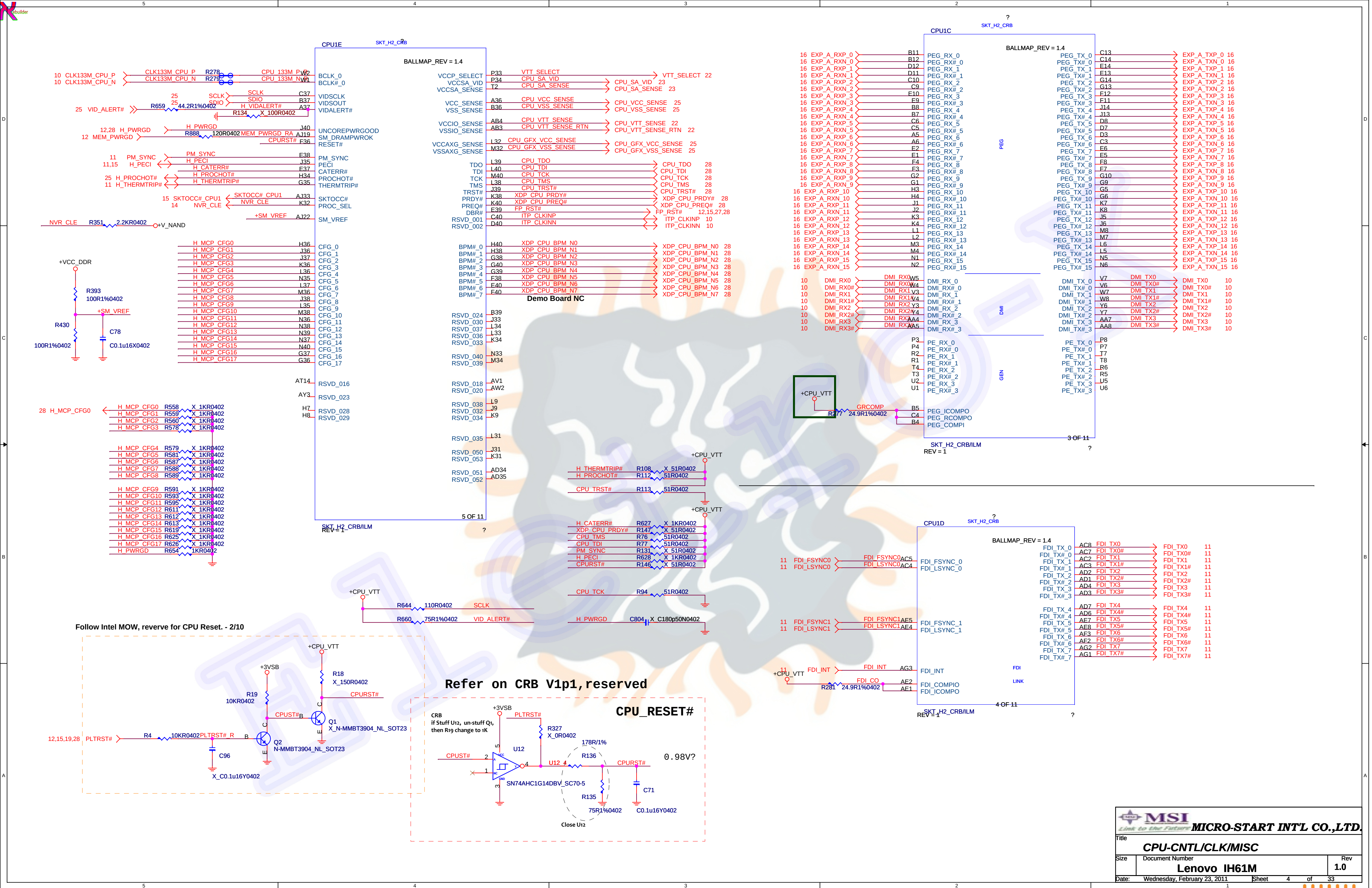
GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BMBUSY#	I/O	Core	3.3V	GPI	BM_BUSY#
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	NC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	NC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	GPI	NC
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	USB_OCP#7
GPIO[15]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[16]	SATA4GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	NC
GPIO[18]	PCIECLKRQ1#	I/O	Core	3.3V	Native	Pull-Hi
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[20]	PCIECLKRQ2#	I/O	Core	3.3V	Native	Pull-Hi
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	NC
GPIO[24]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[25]	PCIECLKRQ3#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[26]	PCIECLKRQ4#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[27]	unmuxed	I/O	Resume	3.3V	GPO	NC
GPIO[28]	unmuxed	I/O	Resume	3.3V	GPO	USB_MODE
GPIO[29]	SLP_LAN#	I/O	Resume	3.3V	GPI	NC
GPIO[30]	SUS_PWR_DN_ACK	I/O	Resume	3.3V	GPI	Pull-Hi
GPIO[31]	ACPRESENT	I/O	Resume	3.3V	GPI	Pull-Hi
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	NC
GPIO[34]	STP_PCI#	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	NC
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	USB_OCP#[1:4]
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[47]	PEG_A_CLKRQ#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	NC
GPIO[49]	SATA5GP	I/O	Core	3.3V	GPI	Pull-Hi
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ#1
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT#1
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ#2
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT#2
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ#3
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT#3
GPIO[56]	PEG_B_CLKRQ#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[57]	unmuxed	I/O	Resume	3.3V	GPI	USB_DET1
GPIO[58]	SML1CLK	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	USB_DET2
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	NC
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64:67]	CLKOUTFLEX	I/O	Core	3.3V	Native	NC
GPIO[72]	unmuxed	I/O	Resume	3.3V	Native	USB_DET3
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	PCIECLKRQ0#
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	Pull-Hi
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	Pull-Hi

SIO(6776F)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[5:0]	UNUSED		
GPIO6	SKTOCC#	INPUT	
GPIO7	UNUSED		
GPIO10	BOARD_ID1		
GPIO11	BOARD_ID0		
GPIO12	LOW_PWR		
GPIO13	UNUSED		
GPIO14	UNUSED		
GPIO15	LED_VSB	OUTPUT	
GPIO16	LED_VCC	OUTPUT	
GPIO17	PAS_DET#	INPUT	
GPIO20	PLTRST_BUS1#	OUTPUT	PCI RESET BUFFER1
GPIO21	PLTRST_BUS2#	OUTPUT	PCI RESET BUFFER2
GPIO22	UNUSED		
GPIO23	UNUSED		
GPIO24	ATX_PWROK	INPUT	ATX POWER OK INPUT
GPIO26	PSIN#	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	SIO_PWROK	OUTPUT	RESERVE FOR PWRGD_3V
GPIO33	RSMRST#	OUTPUT	
GPIO40	UNUSED		
GPIO41	DVI_C_HPD_DP		
GPIO42	FP_AUD_DET#	INPUT	FRONT AUDIO CABLE DETECTION
GPIO43	UNUSED		

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	10	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1



CPU1E
SKT_H2_CRB
BALLMAP_REV = 1.4
BCLK_0
BCLK#_0
VIDSCLK
VIDSOUT
VIDALERT#
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
PM_SYNC
PECI
CATERR#
PROCHOT#
THERMTRIP#
SKTOCC#
PROC_SEL
SM_VREF
CFG_0 … CFG_17
VCCP_SELECT
VCCSA_VID
VCCSA_SENSE
VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSSIO_SENSE
VCCAXG_SENSE
VSSAXG_SENSE
TDO
TDI
TCK
TMS
TRST#
PRDY#
PREQ#
DBR#
BPM#_0 … BPM#_7
Demo Board NC
5 OF 11
SKT_H2_CRB/ILM
REV = 1
CPU1C
PEG_RX_0 … PEG_RX#_15
PEG_TX_0 … PEG_TX#_15
DMI_RX_0 … DMI_RX#_3
DMI_TX_0 … DMI_TX#_3
PE_RX_0 … PE_RX#_3
PE_TX_0 … PE_TX#_3
PEG_ICOMPO
PEG_RCOMPO
PEG_COMPI
+CPU_VTT
R277 24.9R1%0402
GRCOMP
3 OF 11
CPU1D
FDI_FSYNC_0
FDI_LSYNC_0
FDI_FSYNC_1
FDI_LSYNC_1
FDI_INT
FDI_COMPIO
FDI_ICOMPO
FDI_TX_0 … FDI_TX#_7
R281 24.9R1%0402
4 OF 11
+VCC_DDR
R393 100R1%0402
R430 100R1%0402
+SM_VREF
C78 C0.1u16X0402
28 H_MCP_CFG0
+CPU_VTT
R644 110R0402 SCLK
R660 75R1%0402 VID_ALERT#
H_PWRGD C804 X_C180p50N0402
Follow Intel MOW, reverve for CPU Reset. - 2/10
+CPU_VTT
+3VSB
R18 X_150R0402
CPURST#
R19 10KR0402
Q1 X_N-MMBT3904_NL_SOT23
Q2 N-MMBT3904_NL_SOT23
12,15,19,28 PLTRST#
R4 10KR0402 PLTRST#_R
C96 X_C0.1u16Y0402
Refer on CRB V1p1,reserved
CPU_RESET#
CRB
if Stuff U12, un-stuff Q1, then R19 change to 1K
PLTRST#
R327 X_0R0402
U12
SN74AHC1G14DBV_SC70-5
178R/1%
R136
R135 75R1%0402
C71 C0.1u16Y0402
0.98V?
Close U12
MSI
MICRO-START INT'L CO.,LTD.
Title
CPU-CNTL/CLK/MISC
Size
Document Number
Lenovo IH61M
Rev
1.0
Date: Wednesday, February 23, 2011
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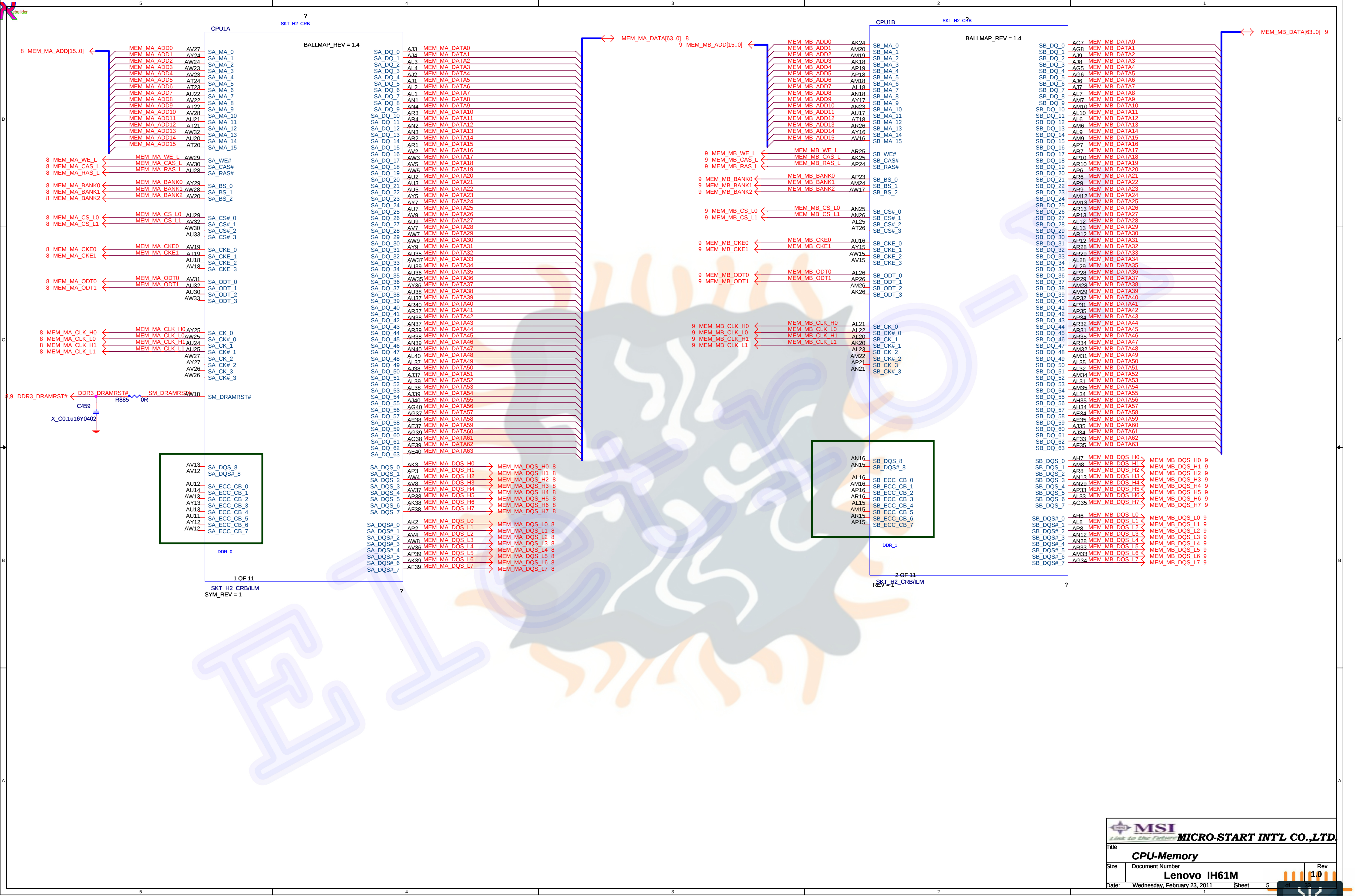
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SKT_H2_CRB
BALLMAP_REV = 1.4
8 MEM_MA_ADD[15..0]
MEM_MA_ADD0 … MEM_MA_ADD15
SA_MA_0 … SA_MA_15
8 MEM_MA_WE_L
8 MEM_MA_CAS_L
8 MEM_MA_RAS_L
SA_WE#
SA_CAS#
SA_RAS#
8 MEM_MA_BANK0
8 MEM_MA_BANK1
8 MEM_MA_BANK2
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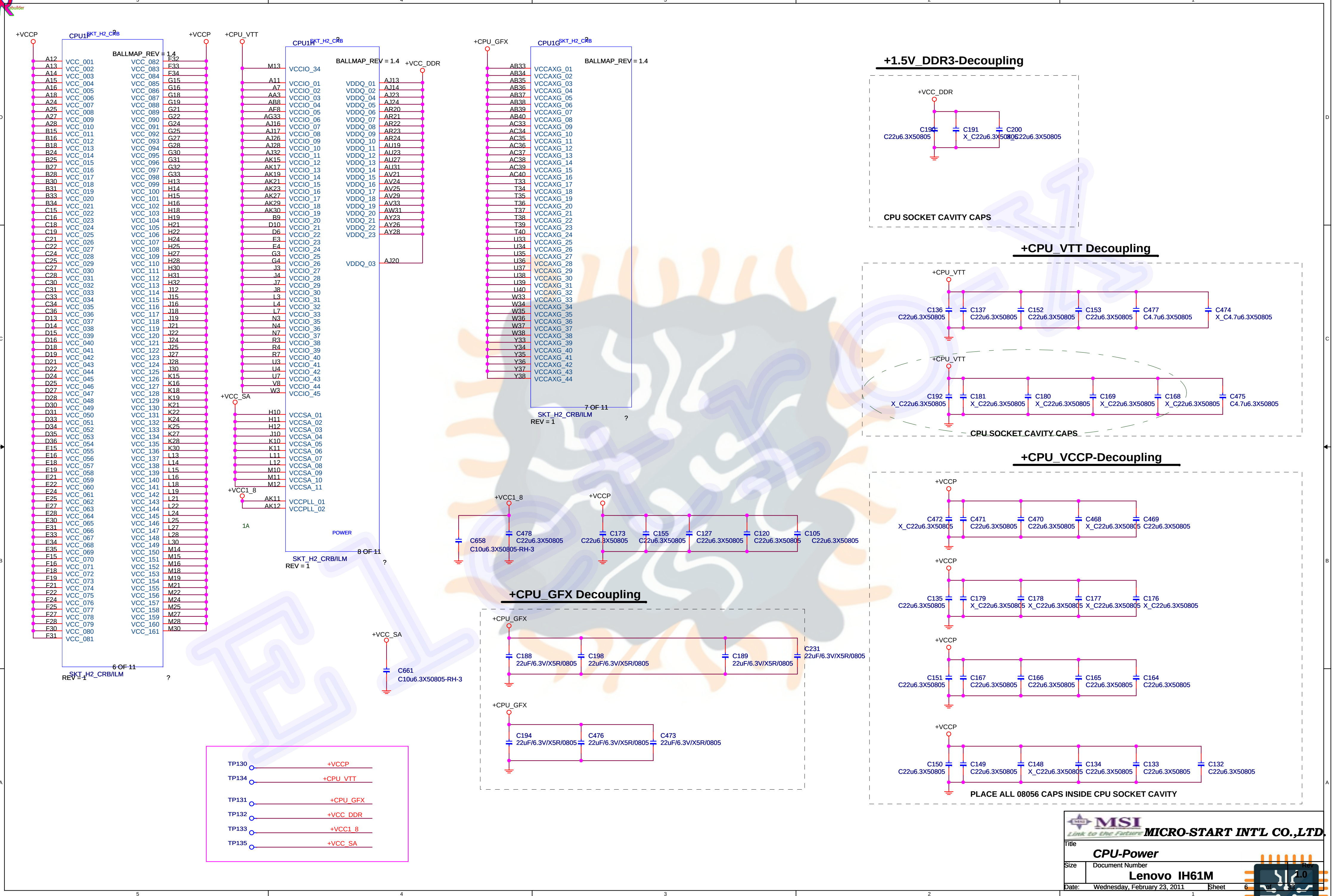
SA_BS_1
SA_BS_2
8 MEM_MA_CS_L0
8 MEM_MA_CS_L1
SA_CS#_0 … SA_CS#_3
8 MEM_MA_CKE0
8 MEM_MA_CKE1
SA_CKE_0 … SA_CKE_3
8 MEM_MA_ODT0
8 MEM_MA_ODT1
SA_ODT_0 … SA_ODT_3
8 MEM_MA_CLK_H0
8 MEM_MA_CLK_L0
8 MEM_MA_CLK_H1
8 MEM_MA_CLK_L1
SA_CK_0 … SA_CK_3
SA_CK#_0 … SA_CK#_3
8,9 DDR3_DRAMRST#
DDR3_DRAMRST#
SM_DRAMRST#
R885
0R
C459
X_C0.1u16Y0402
SA_DQS_8
SA_DQS#_8
SA_ECC_CB_0 … SA_ECC_CB_7
DDR_0
SA_DQ_0 … SA_DQ_63
MEM_MA_DATA0 … MEM_MA_DATA63
MEM_MA_DATA[63..0] 8
SA_DQS_0 … SA_DQS_7
MEM_MA_DQS_H0 … MEM_MA_DQS_H7 8
SA_DQS#_0 … SA_DQS#_7
MEM_MA_DQS_L0 … MEM_MA_DQS_L7 8
1 OF 11
SKT_H2_CRB/ILM
SYM_REV = 1
CPU1B
SKT_H2_CRB
BALLMAP_REV = 1.4
9 MEM_MB_ADD[15..0]
MEM_MB_ADD0 … MEM_MB_ADD15
SB_MA_0 … SB_MA_15
9 MEM_MB_WE_L
9 MEM_MB_CAS_L
9 MEM_MB_RAS_L
SB_WE#
SB_CAS#
SB_RAS#
9 MEM_MB_BANK0
9 MEM_MB_BANK1
9 MEM_MB_BANK2
SB_BS_0
SB_BS_1
SB_BS_2
9 MEM_MB_CS_L0
9 MEM_MB_CS_L1
SB_CS#_0 … SB_CS#_3
9 MEM_MB_CKE0
9 MEM_MB_CKE1
SB_CKE_0 … SB_CKE_3
9 MEM_MB_ODT0
9 MEM_MB_ODT1
SB_ODT_0 … SB_ODT_3
9 MEM_MB_CLK_H0
9 MEM_MB_CLK_L0
9 MEM_MB_CLK_H1
9 MEM_MB_CLK_L1
SB_CK_0 … SB_CK_3
SB_CK#_0 … SB_CK#_3
SB_DQS_8
SB_DQS#_8
SB_ECC_CB_0 … SB_ECC_CB_7
DDR_1
SB_DQ_0 … SB_DQ_63
MEM_MB_DATA0 … MEM_MB_DATA63
MEM_MB_DATA[63..0] 9
SB_DQS_0 … SB_DQS_7
MEM_MB_DQS_H0 … MEM_MB_DQS_H7 9
SB_DQS#_0 … SB_DQS#_7
MEM_MB_DQS_L0 … MEM_MB_DQS_L7 9
2 OF 11
SKT_H2_CRB/ILM
REV = 1
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
CPU-Memory
Size
Document Number
Lenovo IH61M
Rev
1.0
Date: Wednesday, February 23, 2011
Sheet 5



+1.5V_DDR3-Decoupling
+VCC_DDR
C190 C22u6.3X50805
C191 X_C22u6.3X50805
C200 X_C22u6.3X50805
CPU SOCKET CAVITY CAPS
+CPU_VTT Decoupling
+CPU_VTT
C136 C22u6.3X50805
C137 C22u6.3X50805
C152 C22u6.3X50805
C153 C22u6.3X50805
C477 C4.7u6.3X50805
C474 X_C4.7u6.3X50805
C192 X_C22u6.3X50805
C181 X_C22u6.3X50805
C180 X_C22u6.3X50805
C169 X_C22u6.3X50805
C168 X_C22u6.3X50805
C475 C4.7u6.3X50805
CPU SOCKET CAVITY CAPS
+CPU_VCCP-Decoupling
+VCCP
C472 X_C22u6.3X50805
C471 C22u6.3X50805
C470 C22u6.3X50805
C468 X_C22u6.3X50805
C469 C22u6.3X50805
C135 C22u6.3X50805
C179 X_C22u6.3X50805
C178 X_C22u6.3X50805
C177 X_C22u6.3X50805
C176 X_C22u6.3X50805
C151 C22u6.3X50805
C167 C22u6.3X50805
C166 C22u6.3X50805
C165 C22u6.3X50805
C164 C22u6.3X50805
C150 C22u6.3X50805
C149 C22u6.3X50805
C148 X_C22u6.3X50805
C134 C22u6.3X50805
C133 C22u6.3X50805
C132 C22u6.3X50805
PLACE ALL 08056 CAPS INSIDE CPU SOCKET CAVITY
+CPU_GFX Decoupling
+CPU_GFX
C188 22uF/6.3V/X5R/0805
C198 22uF/6.3V/X5R/0805
C189 22uF/6.3V/X5R/0805
C231 22uF/6.3V/X5R/0805
C194 22uF/6.3V/X5R/0805
C476 22uF/6.3V/X5R/0805
C473 22uF/6.3V/X5R/0805
+VCC1_8
C658 C10u6.3X50805-RH-3
C478 C22u6.3X50805
C173 C22u6.3X50805
C155 C22u6.3X50805
C127 C22u6.3X50805
C120 C22u6.3X50805
C105 C22u6.3X50805
+VCC_SA
C661 C10u6.3X50805-RH-3
CPU1F SKT_H2_CRB
BALLMAP_REV = 1.4
VCC_001 … VCC_161
6 OF 11
SKT_H2_CRB/ILM
REV = 1
CPU1H SKT_H2_CRB
+CPU_VTT
VCCIO_01 … VCCIO_45
VCCIO_34
VDDQ_01 … VDDQ_23
+VCC_DDR
VCCSA_01 … VCCSA_11
VCCPLL_01
VCCPLL_02
1A
POWER
8 OF 11
SKT_H2_CRB/ILM
REV = 1
CPU1G SKT_H2_CRB
+CPU_GFX
BALLMAP_REV = 1.4
VCCAXG_01 … VCCAXG_44
7 OF 11
SKT_H2_CRB/ILM
REV = 1
TP130 +VCCP
TP134 +CPU_VTT
TP131 +CPU_GFX
TP132 +VCC_DDR
TP133 +VCC1_8
TP135 +VCC_SA
MSI MICRO-START INT'L CO.,LTD.
Title
CPU-Power
Size
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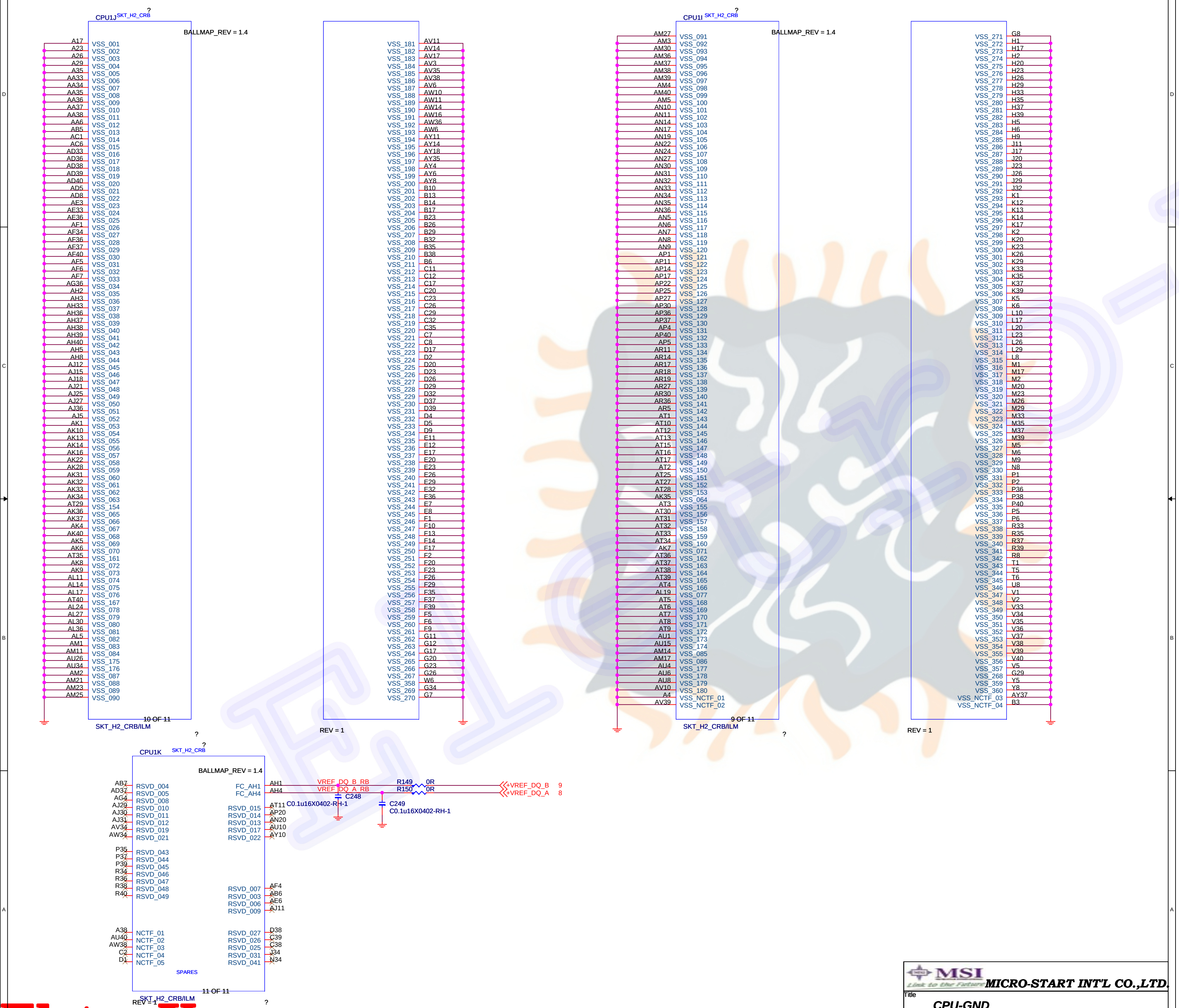

MSI MICRO-START INT'L CO.,LTD.

Title	CPU-GND	
Size	Document Number: Lenovo IH61M	Rev 1.0
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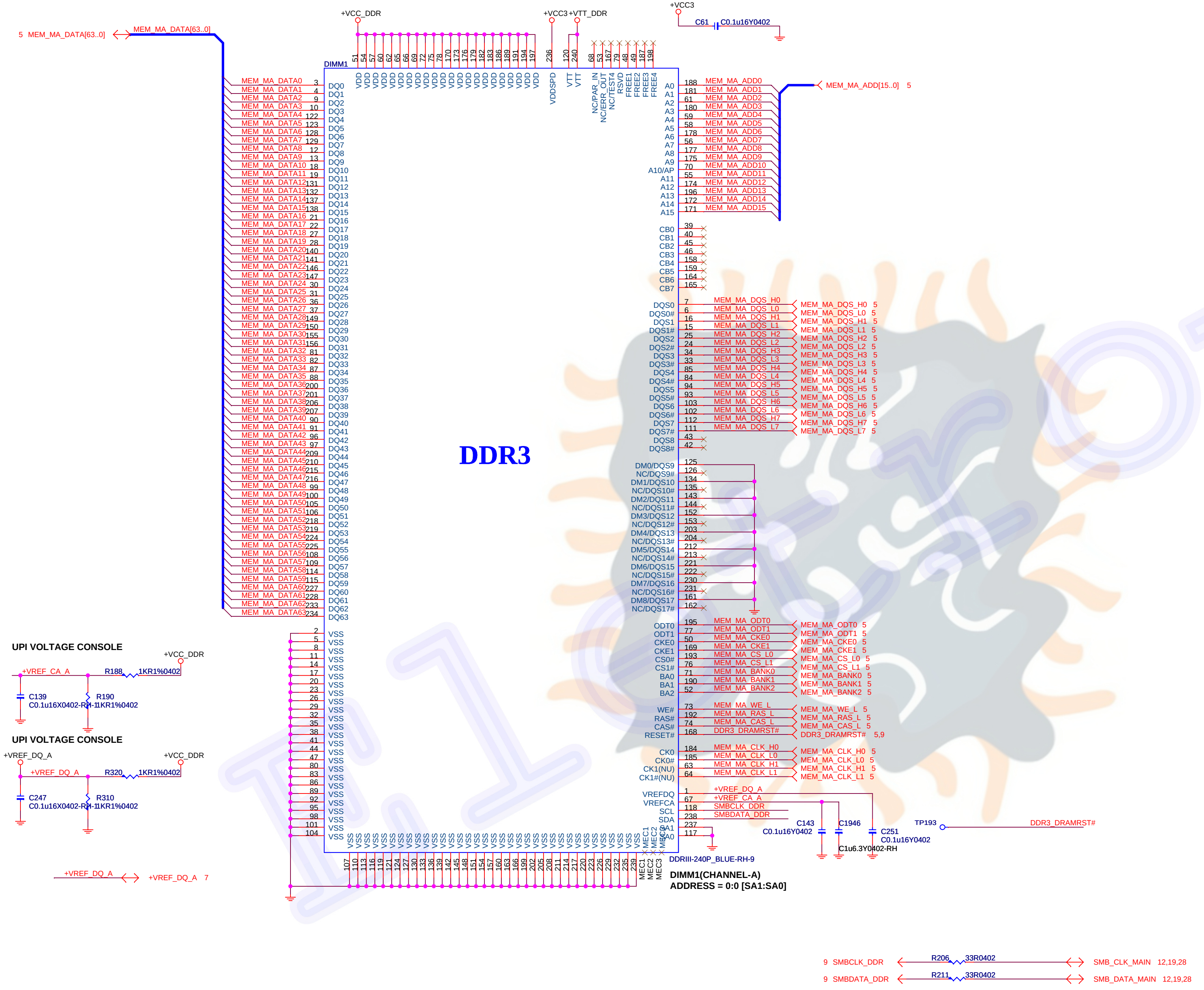
Eletro-X

DDRIII DIMM_A1



MSI MICRO-START INT'L CO.,LTD.

Title	DDR3 Chanel-A DIMM1	
Size	Document Number: Lenovo IH61M	Rev 1.0
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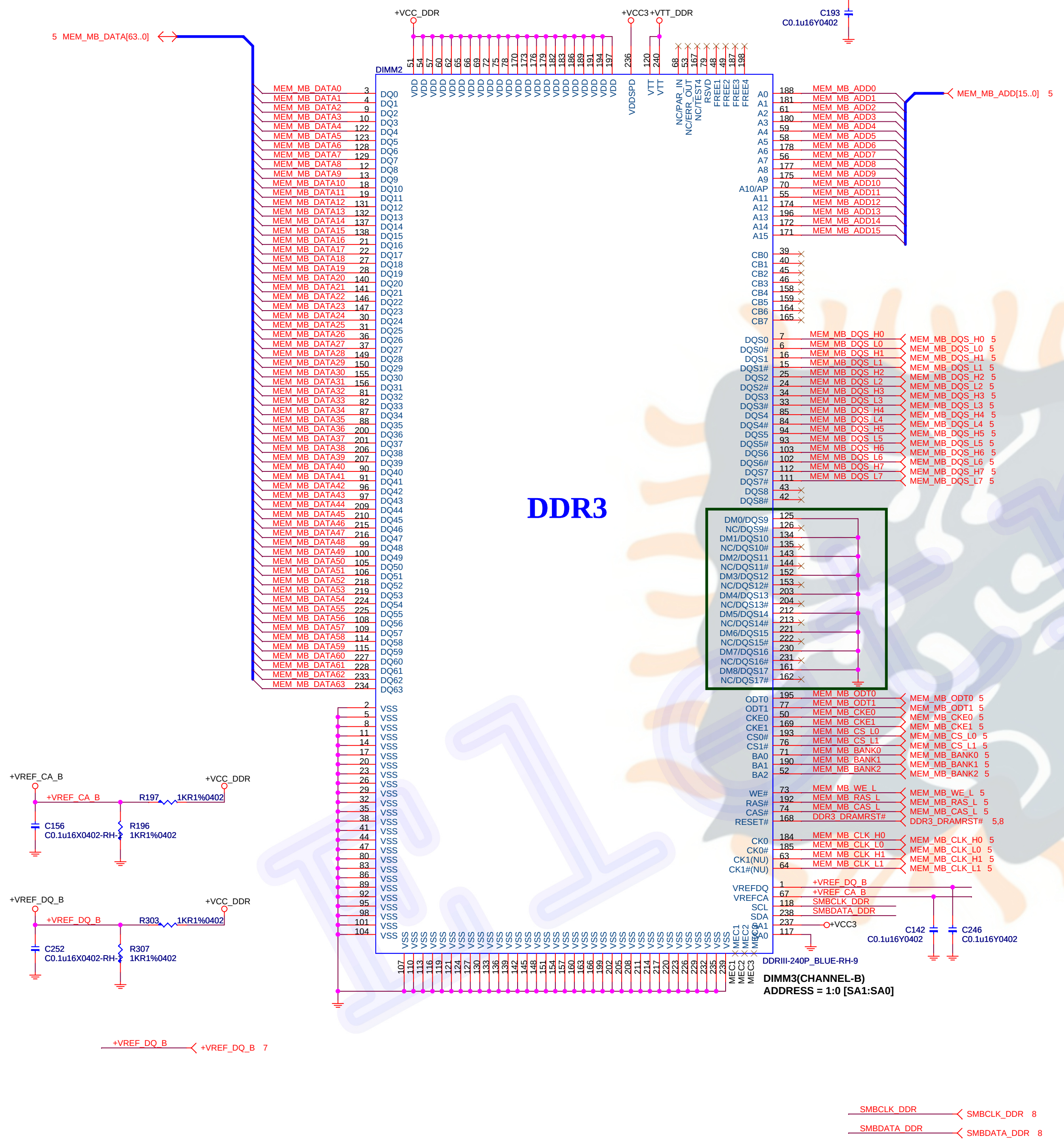
Eletro-X

DDRIII DIMM_B1



MSI MICRO-START INT'L CO.,LTD.

Title: DDR3 Chanel-B DIMM2

Document Number: Lenovo IH61M

Rev: 1.0

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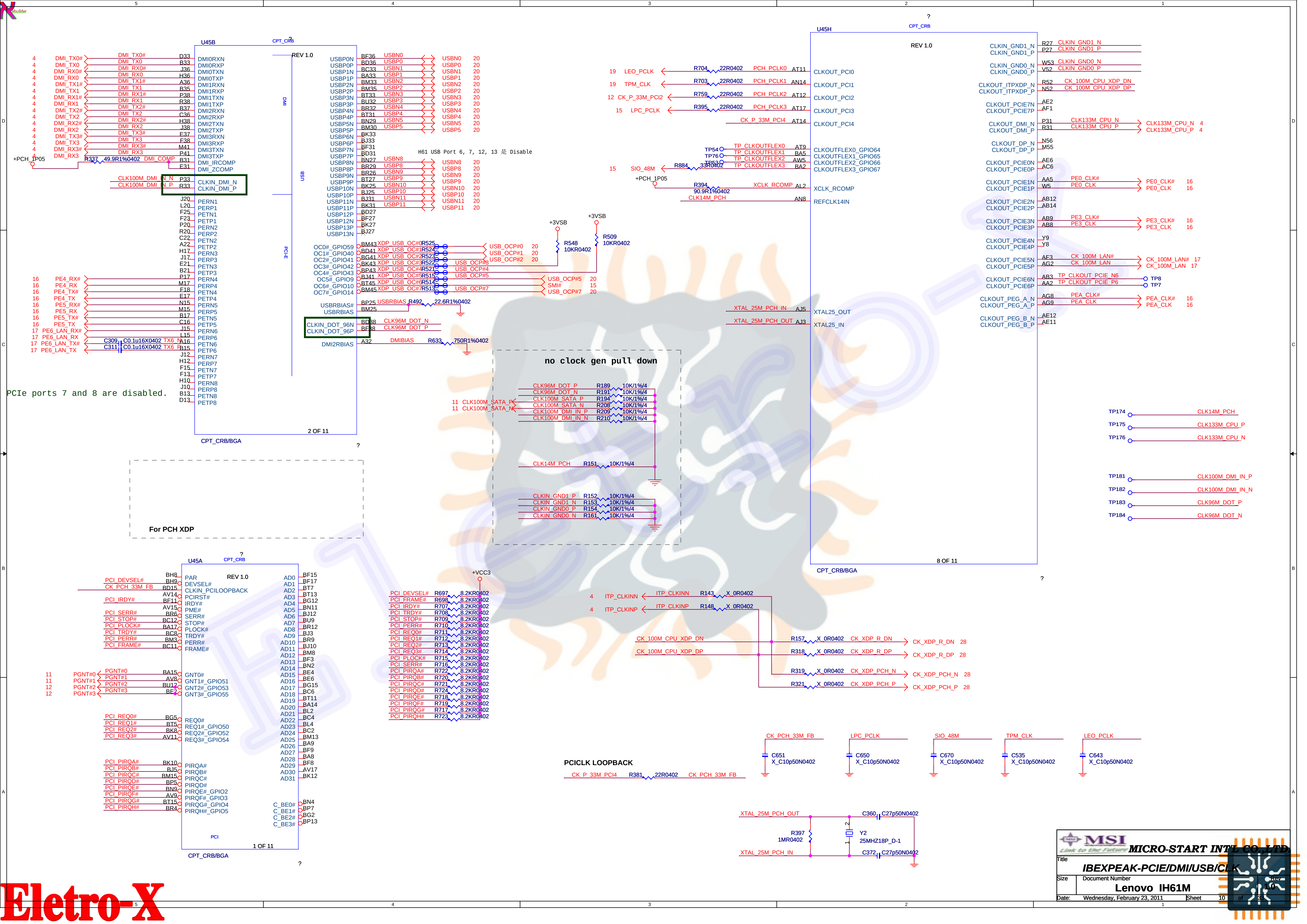
U45B
CPT_CRB
REV 1.0
DMI
USB
PCI-E
2 OF 11
CPT_CRB/BGA
H61 USB Port 6, 7, 12, 13 是 Disable
PCIe ports 7 and 8 are disabled.
For PCH XDP
no clock gen pull down
U45H
CPT_CRB
REV 1.0
8 OF 11
CPT_CRB/BGA
U45A
CPT_CRB
REV 1.0
PCI
1 OF 11
CPT_CRB/BGA
PCICLK LOOPBACK
Y2
25MHZ18P_D-1
MICRO-START INTL CO.,LTD.
Title
IBEXPEAK-PCIE/DMI/USB/CLK
Size
Document Number
Lenovo IH61M
Rev
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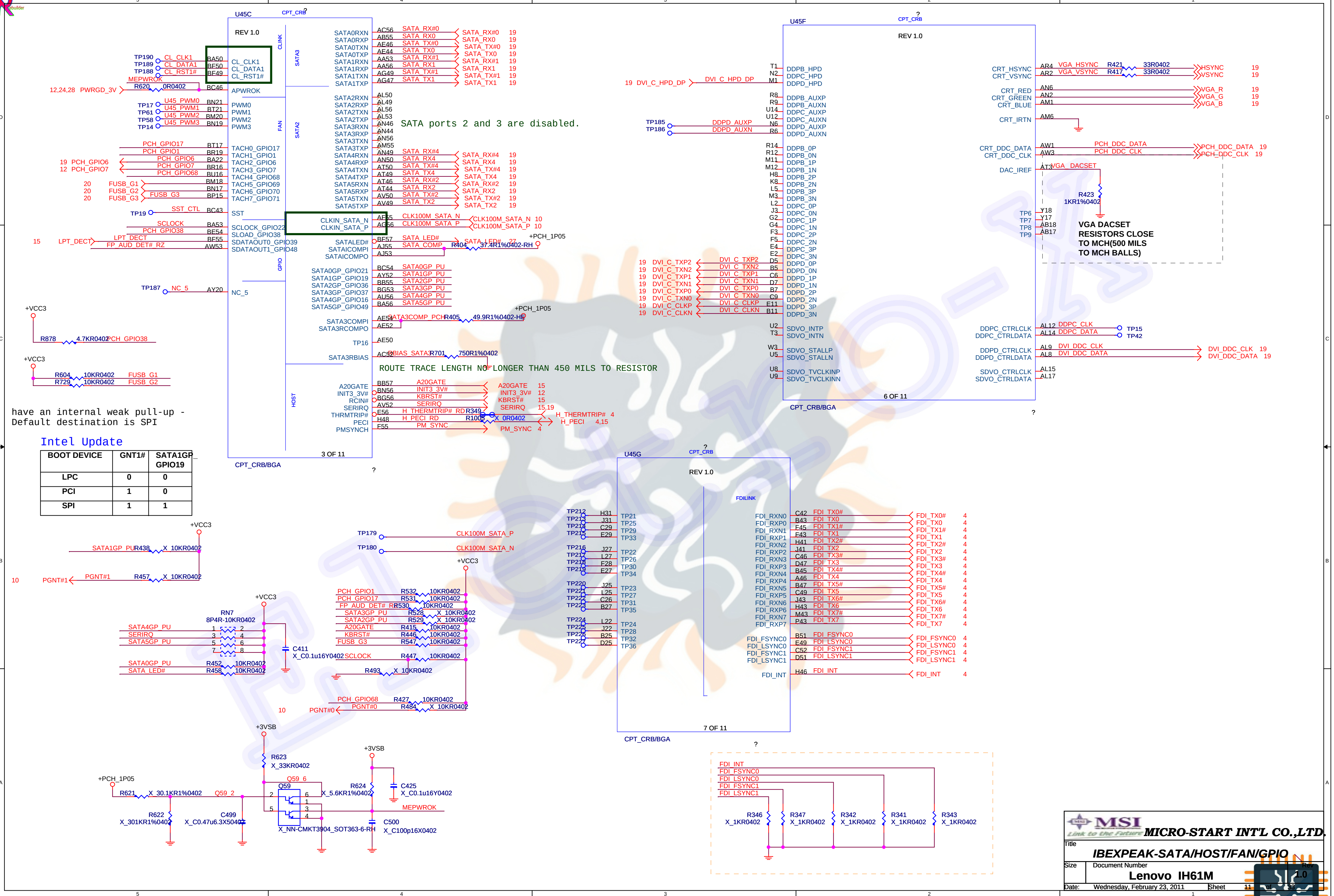

have an internal weak pull-up -
Default destination is SPI

Intel Update

BOOT DEVICE	GNT1#	SATA1GP_GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

MICRO-START INT'L CO.,LTD.

Title: IBEXPEAK-SATA/HOST/FAN/GPIO

Document Number: Lenovo IH61M

Rev: 1.0

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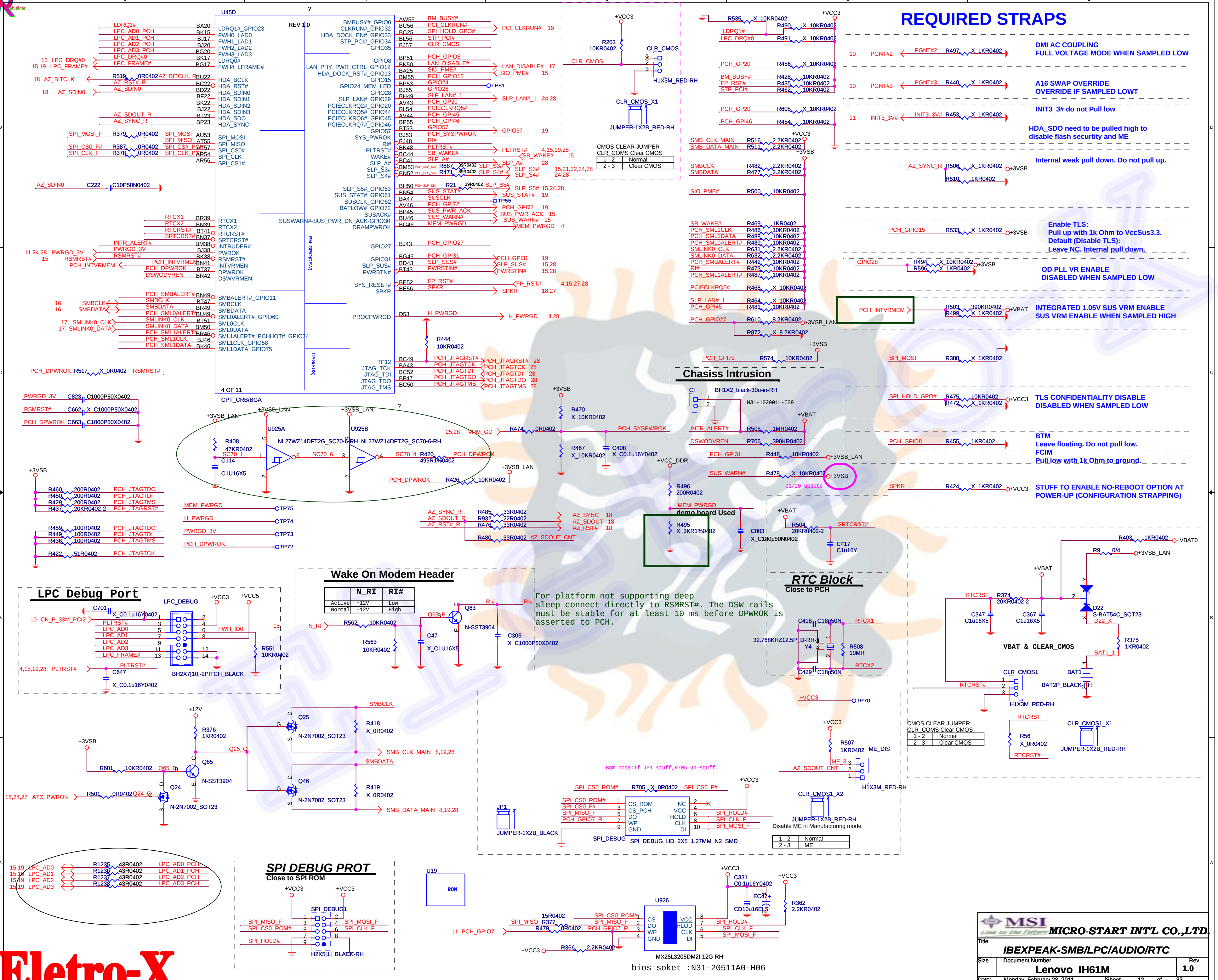

MICRO-START INT'L CO.,LTD.

Title: IBEXPEAK-SMB/LPC/AUDIO/RTC

Size	Document Number	Rev
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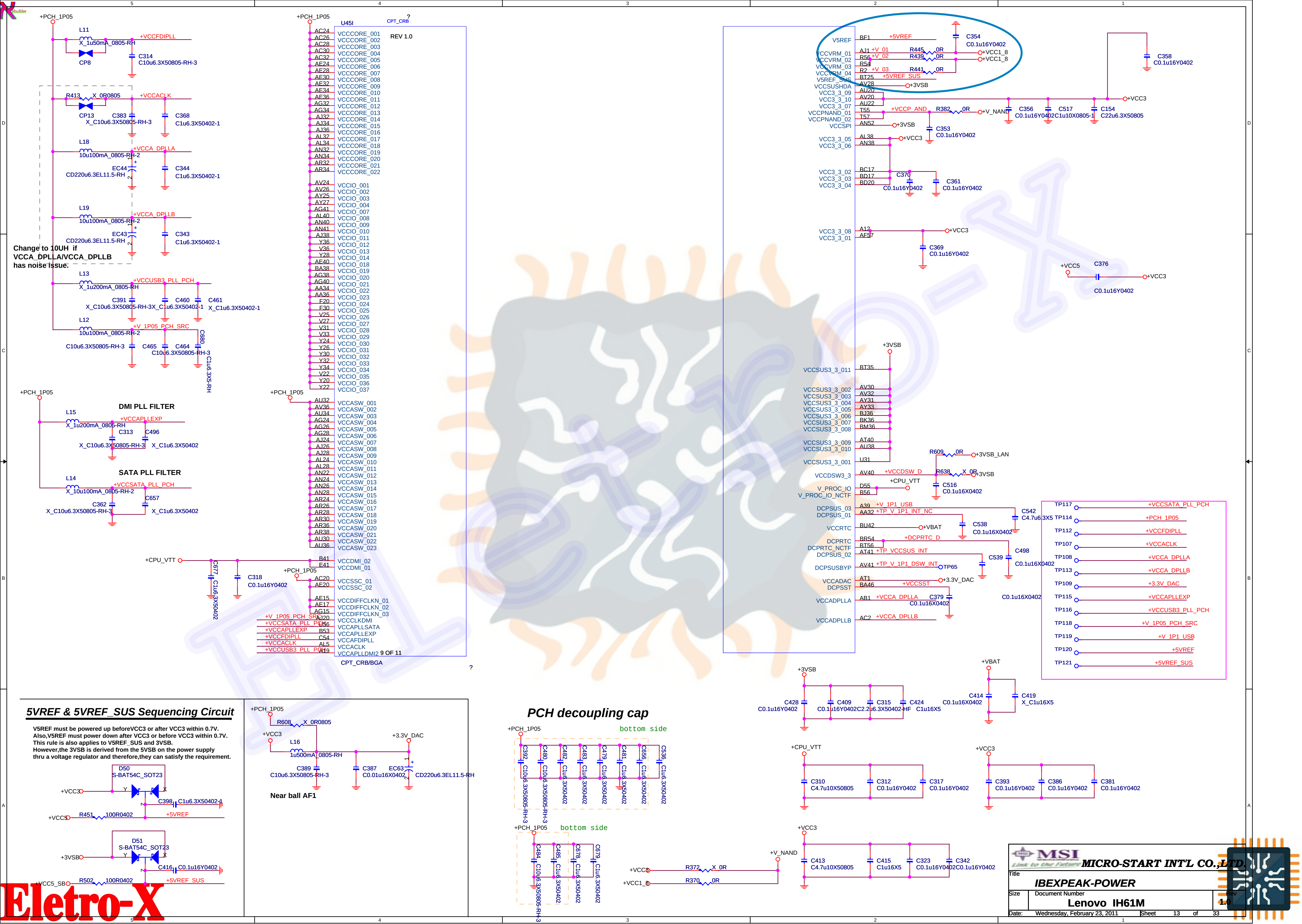
Eletro-X


DMI PLL FILTER
SATA PLL FILTER
Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
U45I
CPT_CRB
REV 1.0
9 OF 11
CPT_CRB/BGA
5VREF & 5VREF_SUS Sequencing Circuit
V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.
D50
S-BAT54C_SOT23
D51
S-BAT54C_SOT23
Near ball AF1
PCH decoupling cap
bottom side
bottom side
MSI
MICRO-START INT'L CO.,LTD.
Title
IBEXPEAK-POWER
Size
Document Number
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1.0
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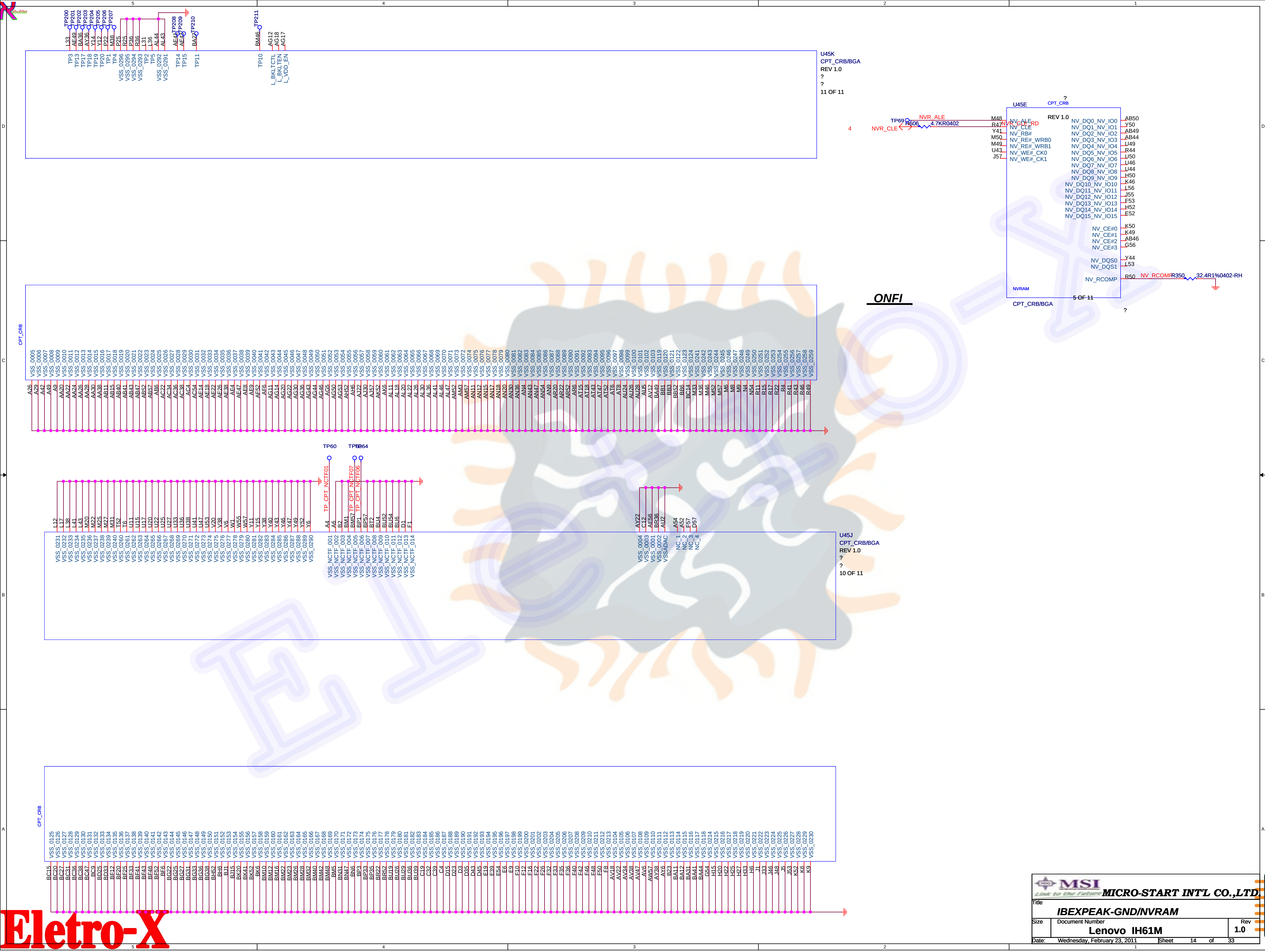

MICRO-START INT'L CO.,LTD.

Title: IBEXPEAK-GND/NVRAM

Size | Document Number: Lenovo IH61M | Rev 1.0

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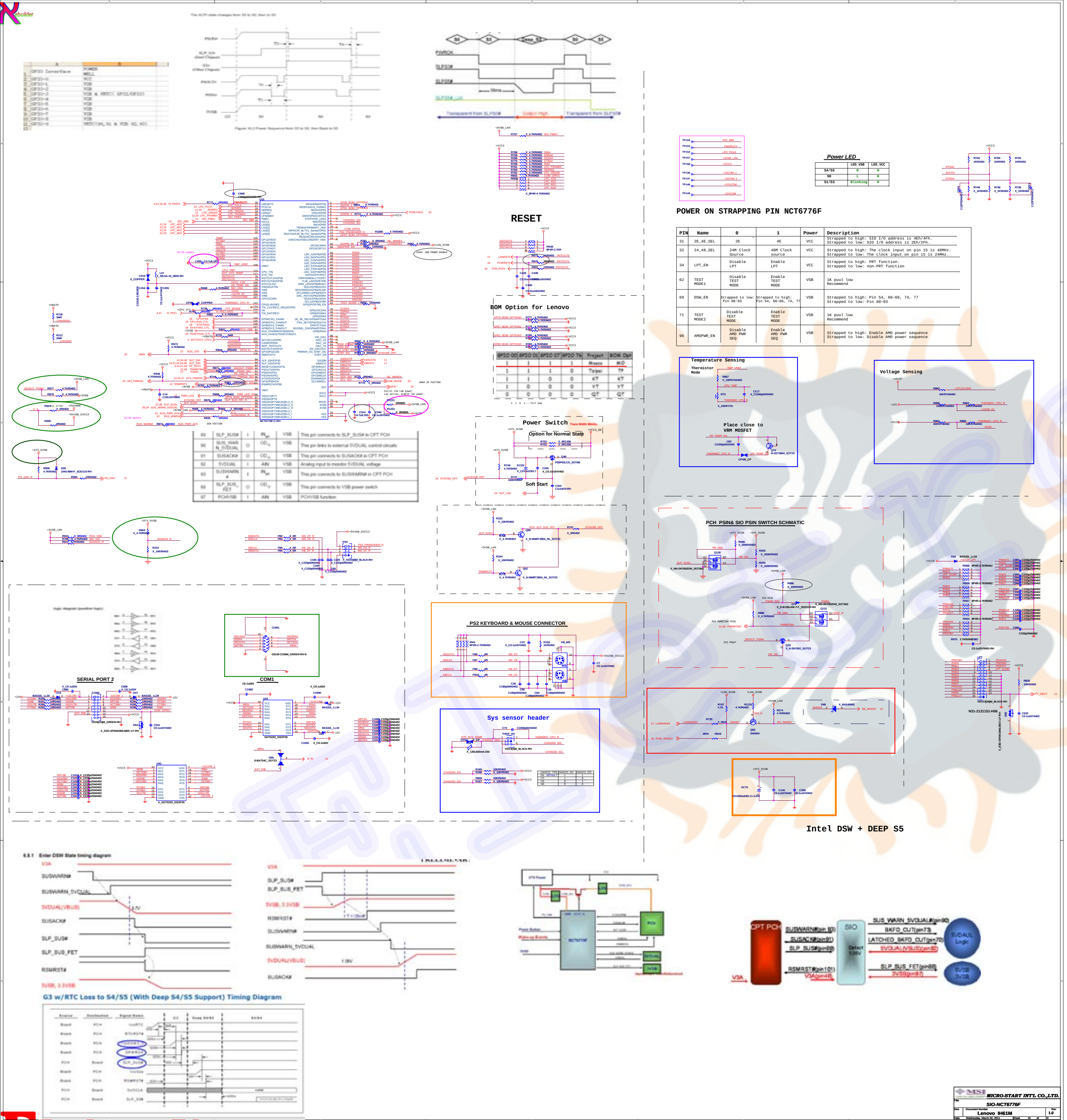
Eletro-X



POWER ON STRAPPING PIN NCT6776F

PIN	Name	0	1	Power	Description
31	2E_4E_SEL	2E	4E	VCC	Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
32	24_48_SEL	24M Clock Source	48M Clock source	VCC	Strapped to high: The clock input on pin 15 is 48MHz. Strapped to low: The clock input on pin 15 is 24MHz.
34	LPT_EN	Disable LPT	Enable LPT	VCC	Strapped to high: PRT function. Strapped to low: non-PRT function
62	TEST MODE1	Disable TEST MODE	Enable TEST MODE	VSB	1K puul low Recommend
69	DSW_EN	Strapped to low: Pin 88~93	Strapped to high: Pin 54, 66~68, 74, 77	VSB	Strapped to high: Pin 54, 66~68, 74, 77 Strapped to low: Pin 88~93
71	TEST MODE2	Disable TEST MODE	Enable TEST MODE	VSB	1K puul low Recommend
96	AMDPWR_EN	Disable AMD PWR SEQ	Enable AMD PWR SEQ	VSB	Strapped to high: Enable AMD power sequence Strapped to low: Disable AMD power sequence

Power LED

	LED_VSB	LED_VCC
S4/S5	H	H
S0	L	H
S1/S3	Blinking	H

BOM Option for Lenovo

GPIO 00	GPIO 01	GPIO 07	GPIO 76	Project	BOM Opt
1	1	1	1	Moana	MD
1	1	1	0	Taipei	TP
1	1	0	0	KT	KT
1	0	0	0	VT	VT
0	0	0	0	QT	QT

1 1 0 1----full bom

89	SLP_SUS#	I	IN	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WARN_5VDUAL	O	OD	VSB	This pin links to external 5VDUAL control circuits
91	SUSACK#	O	OD	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN#	I	IN	VSB	This pin connects to SUSWARN# in CPT PCH
88	SLP_SUS_FET	O	OD	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

Intel DSW + DEEP S5

6.8.1 Enter DSW State timing diagram

G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram

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Title	SIO-NCT6776F
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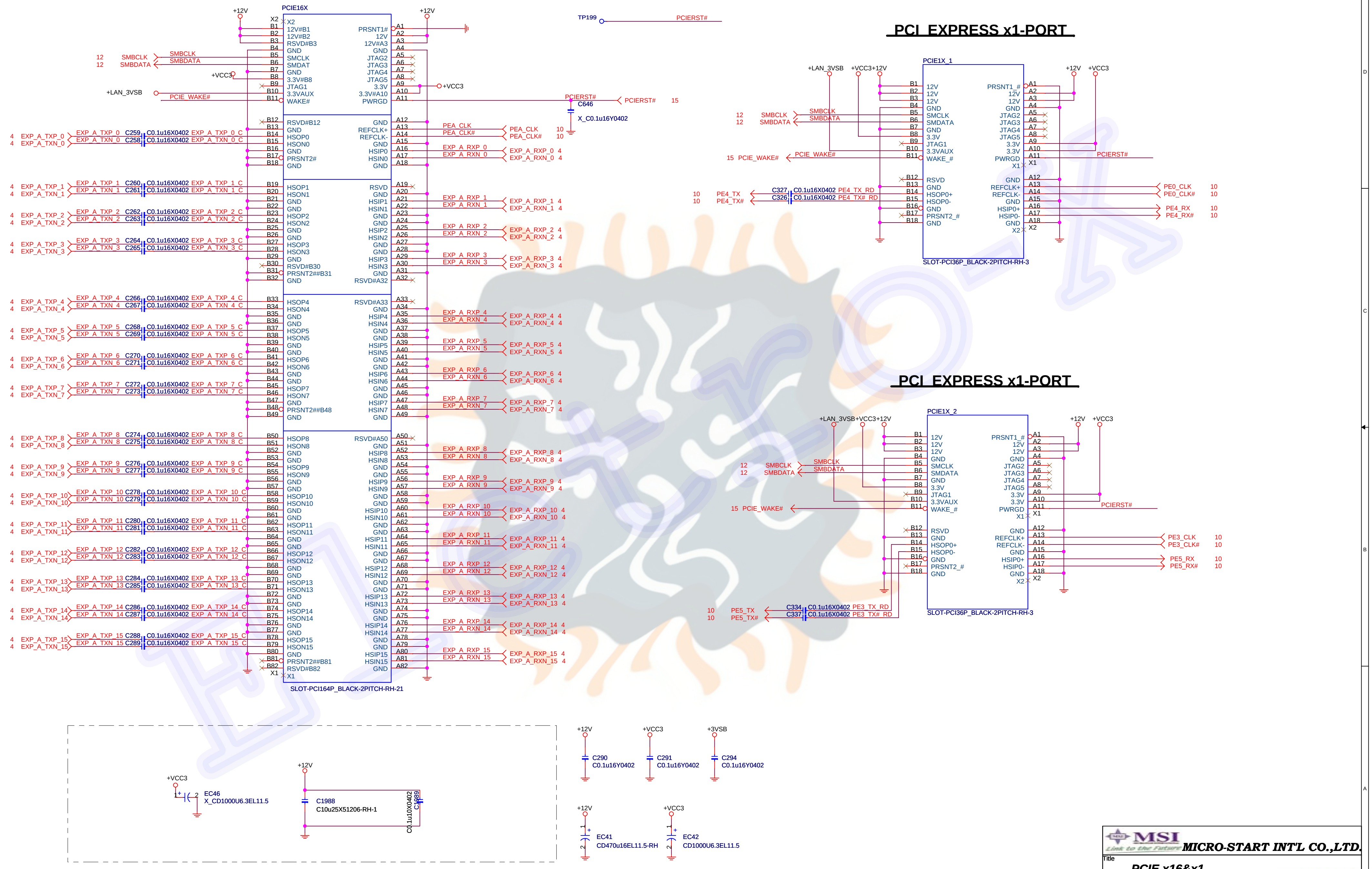
PCI_EXPRESS X16 SLOT

PCI_EXPRESS x1-PORT

PCI_EXPRESS x1-PORT



MSI MICRO-START INT'L CO.,LTD.

Title: PCIE x16&x1

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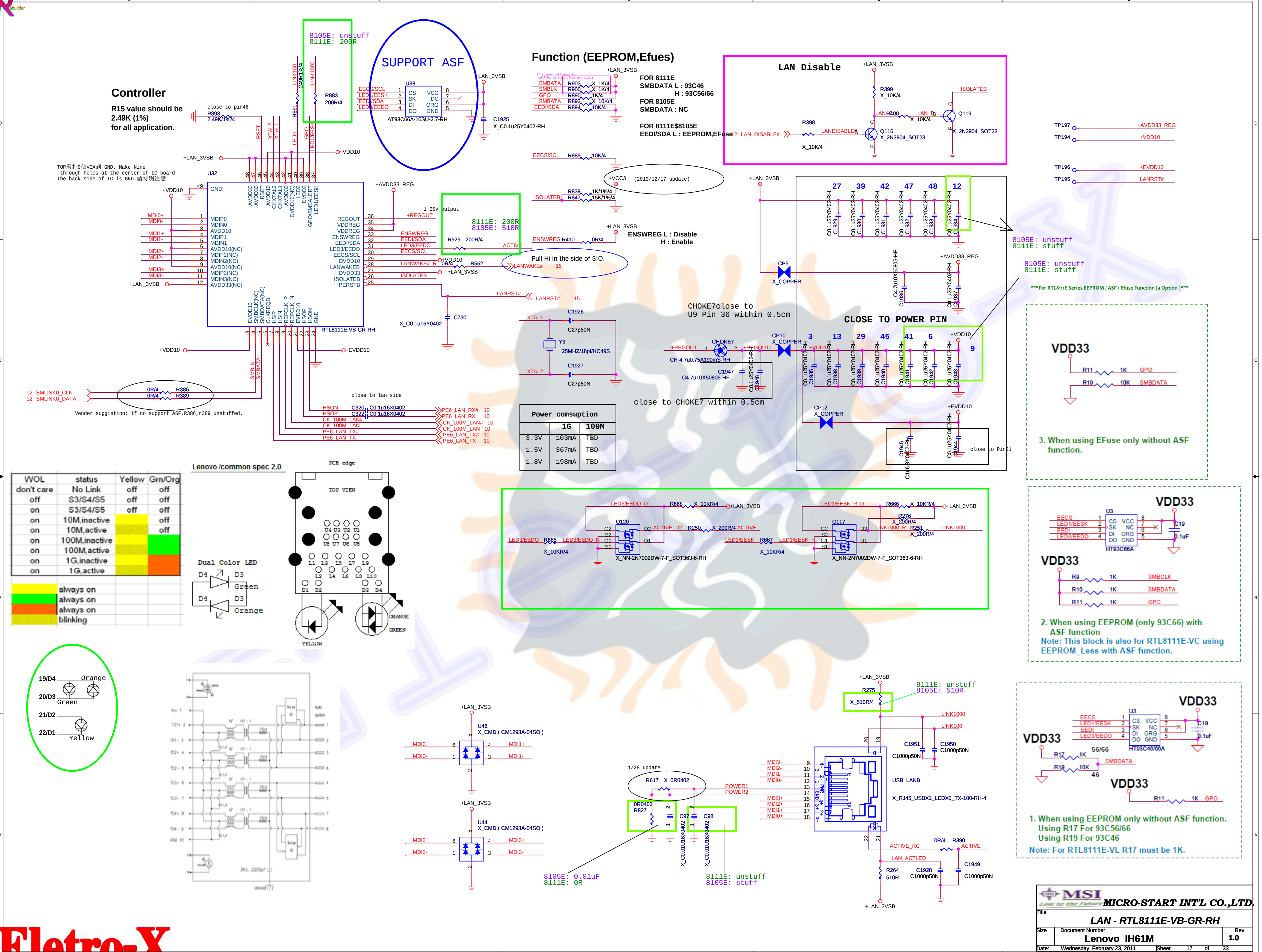
Eletro-X



	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

Power comsuption

WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

	always on
	always on
	always on
	blinking

MICRO-START INT'L CO.,LTD.

Title	LAN - RTL8111E-VB-GR-RH	
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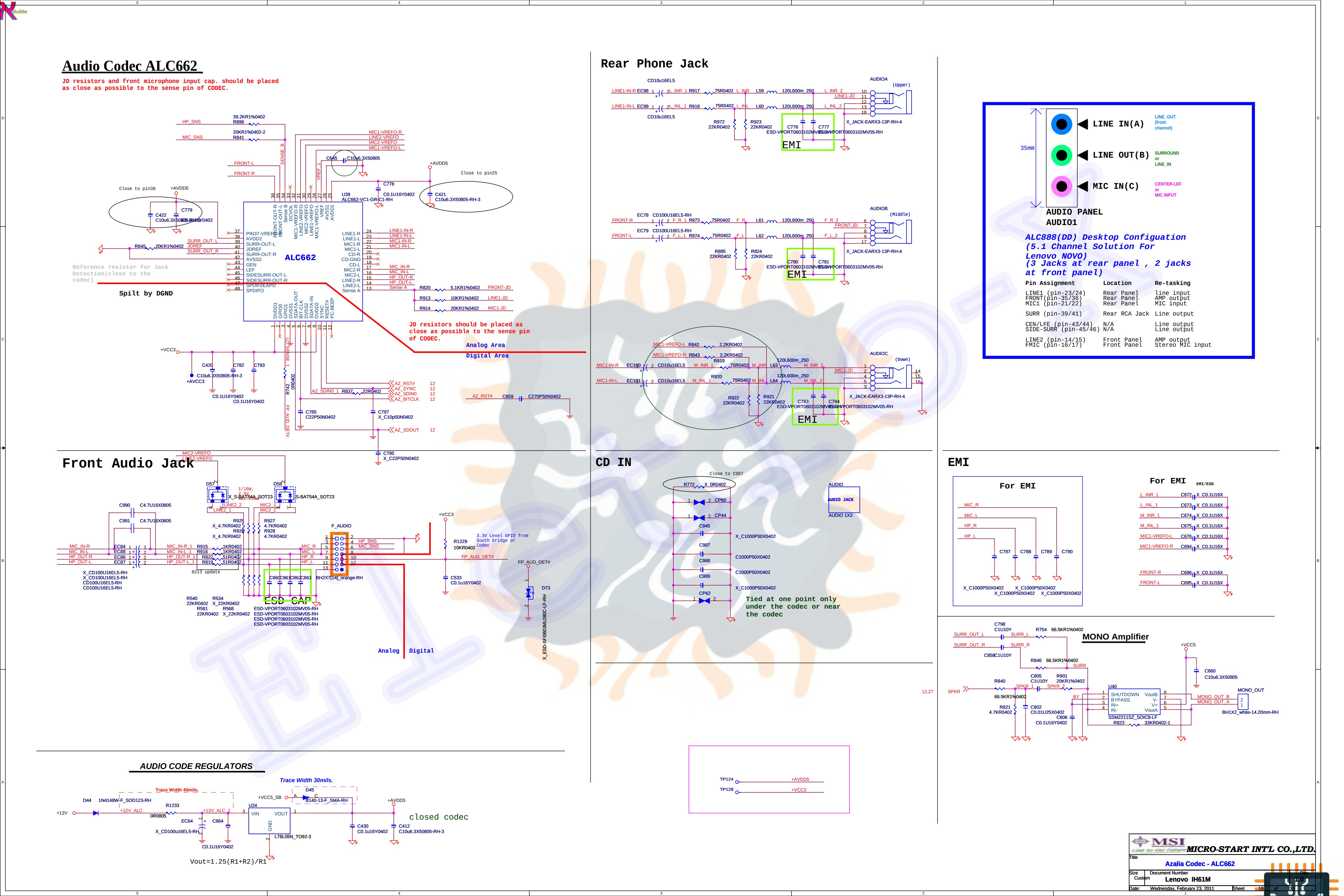
Audio Codec ALC662
JD resistors and front microphone input cap. should be placed
as close as possible to the sense pin of CODEC.
Close to pin38
Close to pin25
ALC662
U39
ALC662-VC1-GR-C1-RH
Reference resistor for Jack
Detection(close to the
codec)
Spilt by DGND
JD resistors should be placed as
close as possible to the sense pin
of CODEC.
Analog Area
Digital Area
Rear Phone Jack
AUDIOA
(Upper)
AUDIOB
(Middle)
AUDIOC
(Down)
X_JACK-EARX3-13P-RH-4
EMI
LINE IN(A)
LINE OUT(B)
MIC IN(C)
35mm
AUDIO PANEL
AUDIO1
ALC888(DD) Desktop Configuation
(5.1 Channel Solution For
Lenovo NOVO)
(3 Jacks at rear panel , 2 jacks
at front panel)
Pin Assignment
Location
Re-tasking
LINE1 (pin-23/24)
FRONT(pin-35/36)
MIC1 (pin-21/22)
Rear Panel
Rear Panel
Rear Panel
line input
AMP output
MIC input
SURR (pin-39/41)
Rear RCA Jack
Line output
CEN/LFE (pin-43/44)
SIDE-SURR (pin-45/46)
N/A
N/A
Line output
Line output
LINE2 (pin-14/15)
FMIC (pin-16/17)
Front Panel
Front Panel
AMP output
Stereo MIC input
Front Audio Jack
F_AUDIO
BH2X7[14]_orange-RH
ESD CAP
3.3V Level GPIO from
South bridge or
Codec
Analog
Digital
CD IN
Close to C987
Tied at one point only
under the codec or near
the codec
AUDIO JACK
AUDIO 1X3
EMI
For EMI
MONO Amplifier
SSM2211SZ_SOIC8-LF
MONO_OUT
AUDIO CODE REGULATORS
Trace Width 40mils.
Trace Width 30mils.
L78L05N_TO92-3
closed codec
Vout=1.25(R1+R2)/R1
MSI
MICRO-START INT'L CO.,LTD.
Title
Azalia Codec - ALC662
Size
Custom
Document Number
Lenovo IH61M
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1.0
Date:
Wednesday, February 23, 2011
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of
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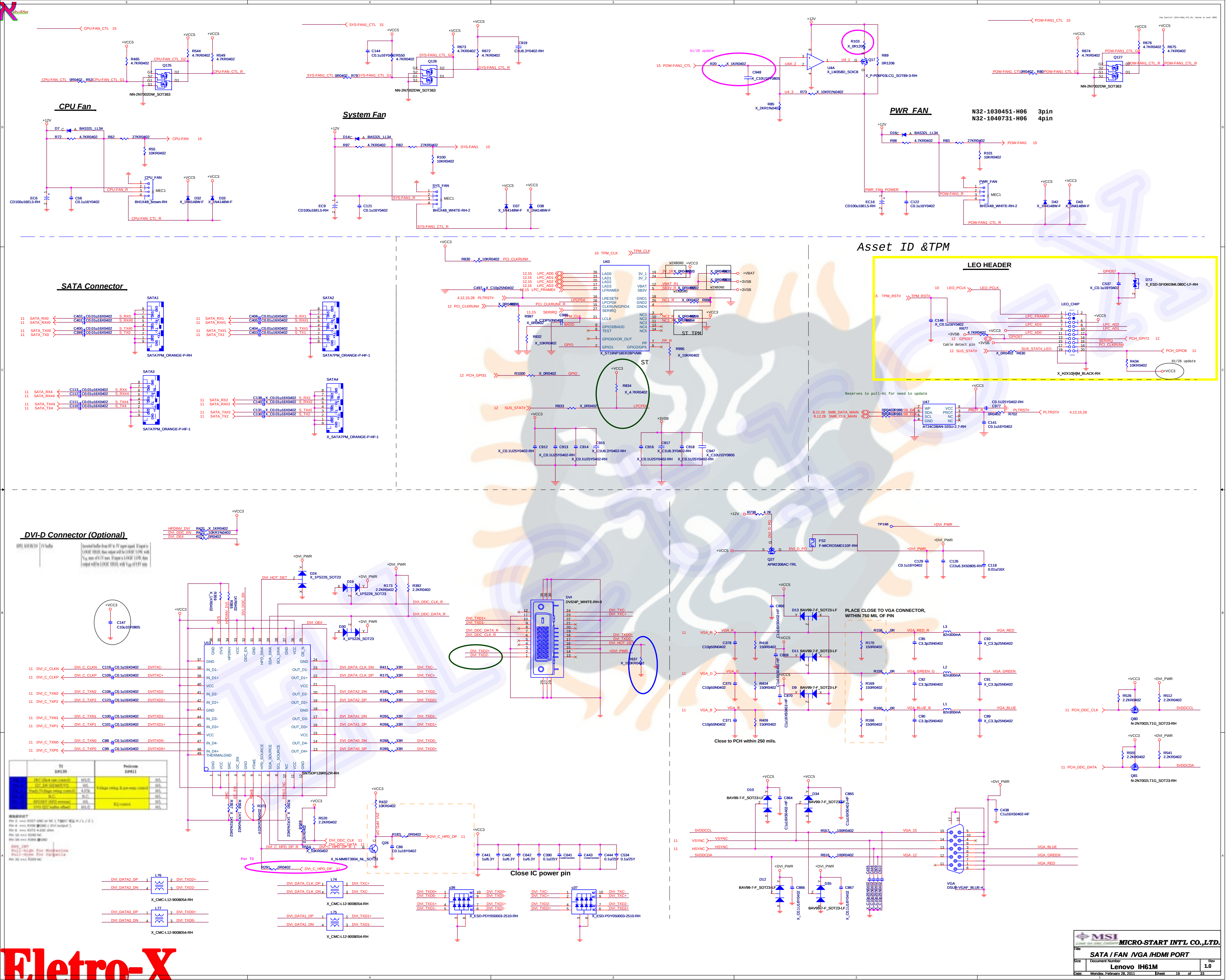

CPU Fan
System Fan
PWR FAN
N32-1030451-H06 3pin
N32-1040731-H06 4pin
SATA Connector
Asset ID &TPM
LEO HEADER
DVI-D Connector (Optional)
Close IC power pin
PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN
Close to PCH within 250 mils.
MICRO-START INT'L CO.,LTD.
SATA / FAN /VGA /HDMI PORT
Lenovo IH61M
Rev 1.0
Date: Monday, February 28, 2011
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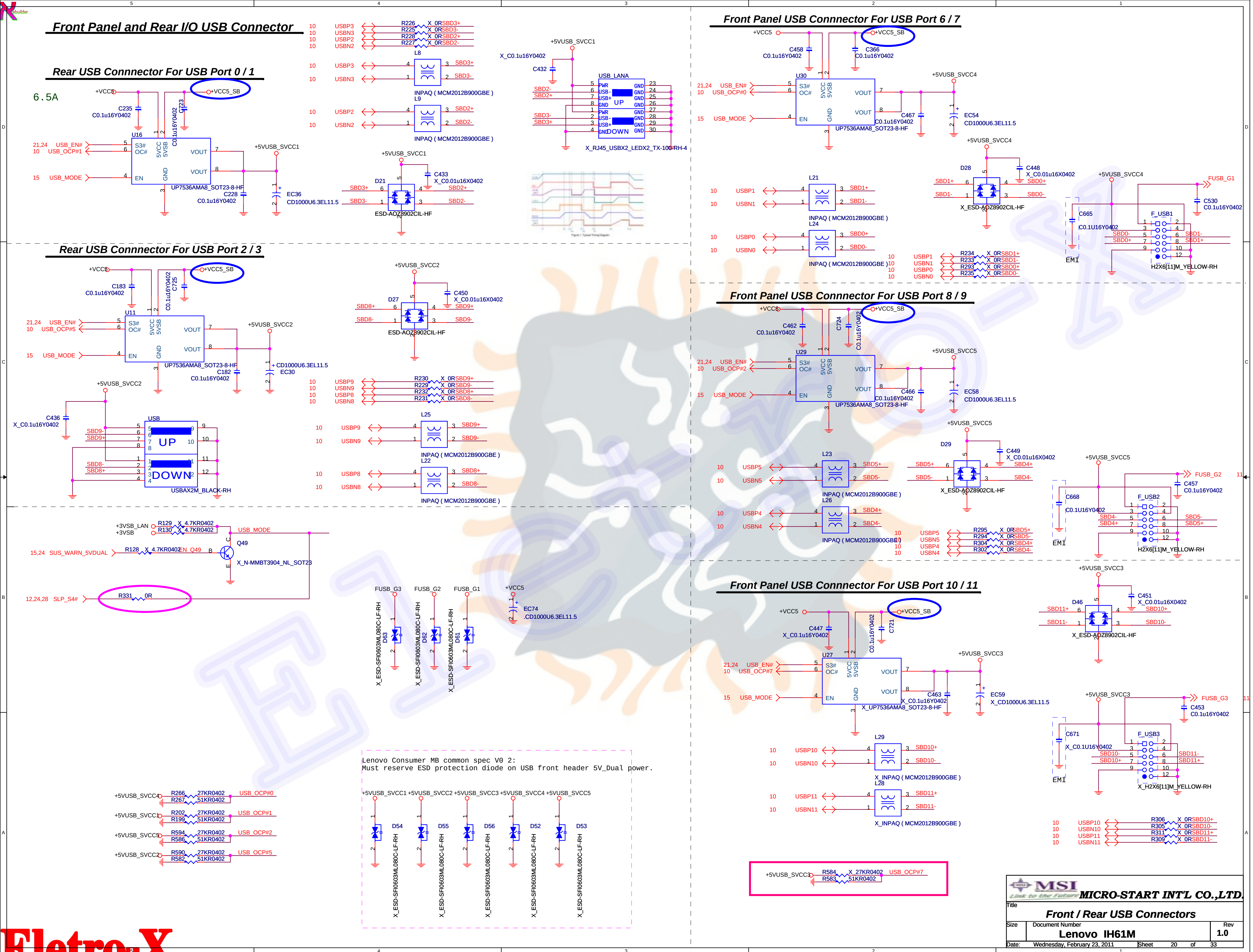
Front Panel and Rear I/O USB Connector
Rear USB Connnector For USB Port 0 / 1
6.5A
Rear USB Connnector For USB Port 2 / 3
Front Panel USB Connnector For USB Port 6 / 7
Front Panel USB Connnector For USB Port 8 / 9
Front Panel USB Connnector For USB Port 10 / 11
UP7536AMA8_SOT23-8-HF
INPAQ (MCM2012B900GBE)
ESD-AOZ8902CIL-HF
X_RJ45_USBX2_LEDX2_TX-100-RH-4
USBAX2M_BLACK-RH
H2X6[11]M_YELLOW-RH
X_N-MMBT3904_NL_SOT23
CD1000U6.3EL11.5
Lenovo Consumer MB common spec V0 2:
Must reserve ESD protection diode on USB front header 5V_Dual power.
MSI
MICRO-START INT'L CO.,LTD.
Title
Front / Rear USB Connectors
Size
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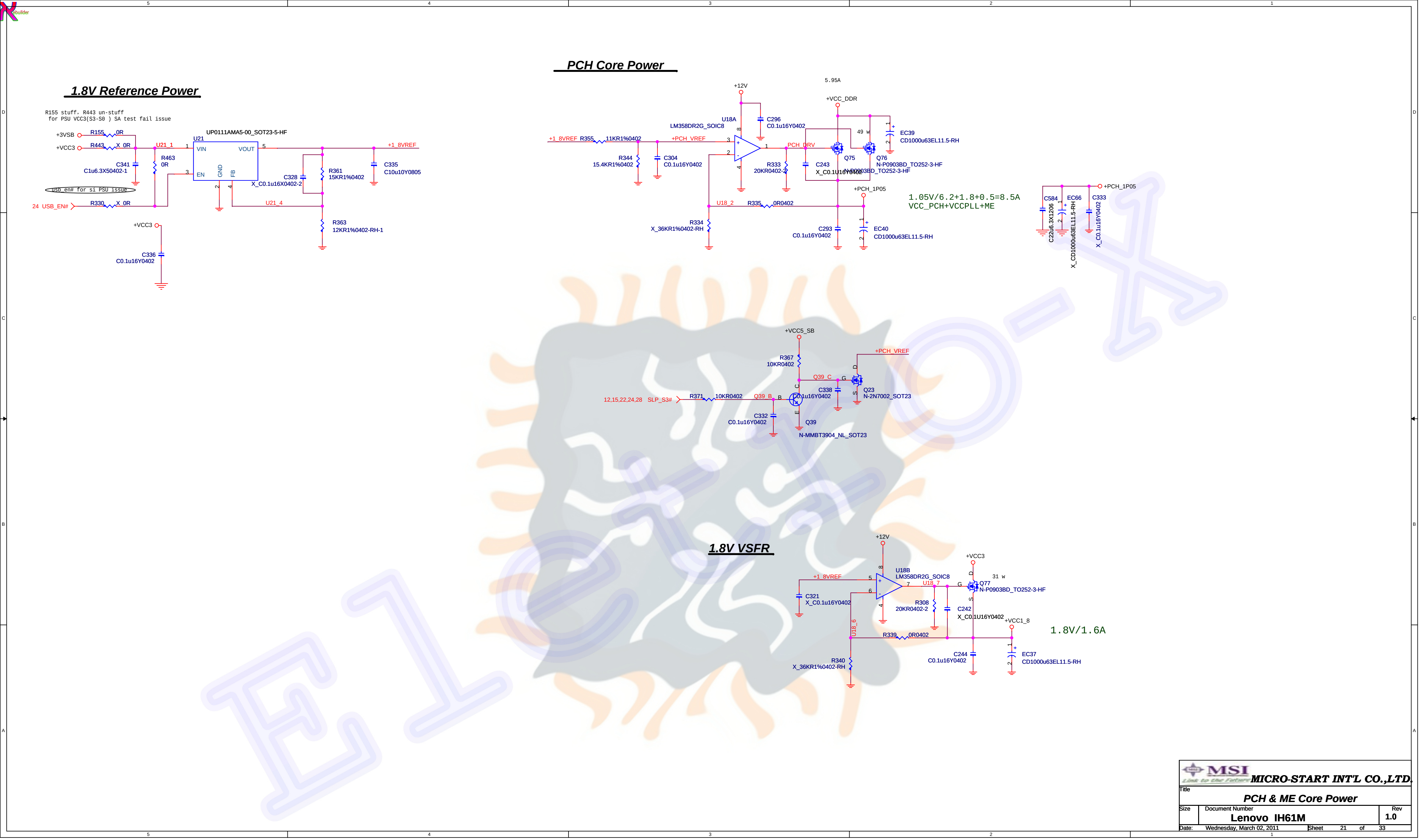

PCH Core Power
1.8V Reference Power
R155 stuff. R443 un-stuff
for PSU VCC3(S3-S0) SA test fail issue
+3VSB
R155 0R
+VCC3
R443 X_0R
U21_1
U21
UP0111AMA5-00_SOT23-5-HF
VIN
VOUT
EN
GND
FB
+1_8VREF
C341
C1u6.3X50402-1
R463
0R
C328
X_C0.1u16X0402-2
R361
15KR1%0402
C335
C10u10Y0805
USB_en# for s1 PSU issue
24 USB_EN#
R330 X_0R
U21_4
R363
12KR1%0402-RH-1
+VCC3
C336
C0.1u16Y0402
+12V
5.95A
+VCC_DDR
U18A
LM358DR2G_SOIC8
C296
C0.1u16Y0402
EC39
CD1000u63EL11.5-RH
49 w
+1_8VREF R355 11KR1%0402
+PCH_VREF
PCH_DRV
R344
15.4KR1%0402
C304
C0.1u16Y0402
R333
20KR0402-2
C243
X_C0.1U16Y0402
Q75
N-P0903BD_TO252-3-HF
Q76
N-P0903BD_TO252-3-HF
+PCH_1P05
U18_2
R335 0R0402
R334
X_36KR1%0402-RH
C293
C0.1u16Y0402
EC40
CD1000u63EL11.5-RH
1.05V/6.2+1.8+0.5=8.5A
VCC_PCH+VCCPLL+ME
+PCH_1P05
C584
C22u6.3X1206
EC66
X_CD1000u63EL11.5-RH
C333
X_C0.1u16Y0402
+VCC5_SB
R367
10KR0402
+PCH_VREF
Q39_C
C338
C0.1u16Y0402
Q23
N-2N7002_SOT23
12,15,22,24,28 SLP_S3#
R371 10KR0402
Q39_B
C332
C0.1u16Y0402
Q39
N-MMBT3904_NL_SOT23
1.8V VSFR
+12V
U18B
LM358DR2G_SOIC8
+VCC3
31 w
Q77
N-P0903BD_TO252-3-HF
+1_8VREF
U18_7
C321
X_C0.1u16Y0402
R308
20KR0402-2
C242
X_C0.1U16Y0402
+VCC1_8
1.8V/1.6A
U18_6
R339 0R0402
R340
X_36KR1%0402-RH
C244
C0.1u16Y0402
EC37
CD1000u63EL11.5-RH
MSI
MICRO-START INT'L CO.,LTD.
Title
PCH & ME Core Power
Size
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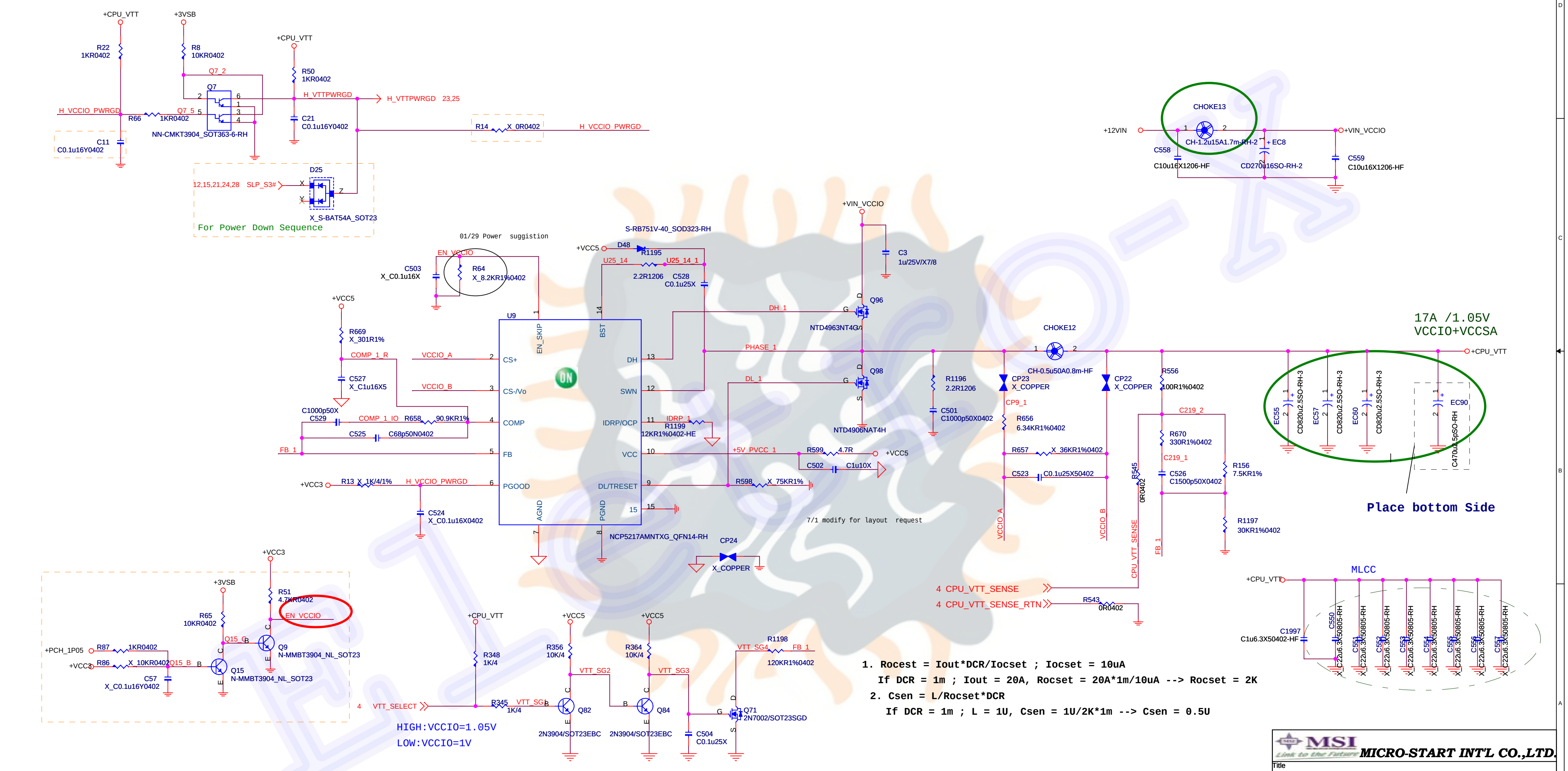
CPU VTT Power

1.1V - 30A - 29W



1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 1m ; Iout = 20A, Rocest = 20A*1m/10uA --> Rocest = 2K
2. Csen = L/Rocset*DCR
   If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

MSI MICRO-START INT'L CO.,LTD.		
Title: CPU VTT VR		
Size	Document Number: Lenovo IH61M	Rev: 1.0
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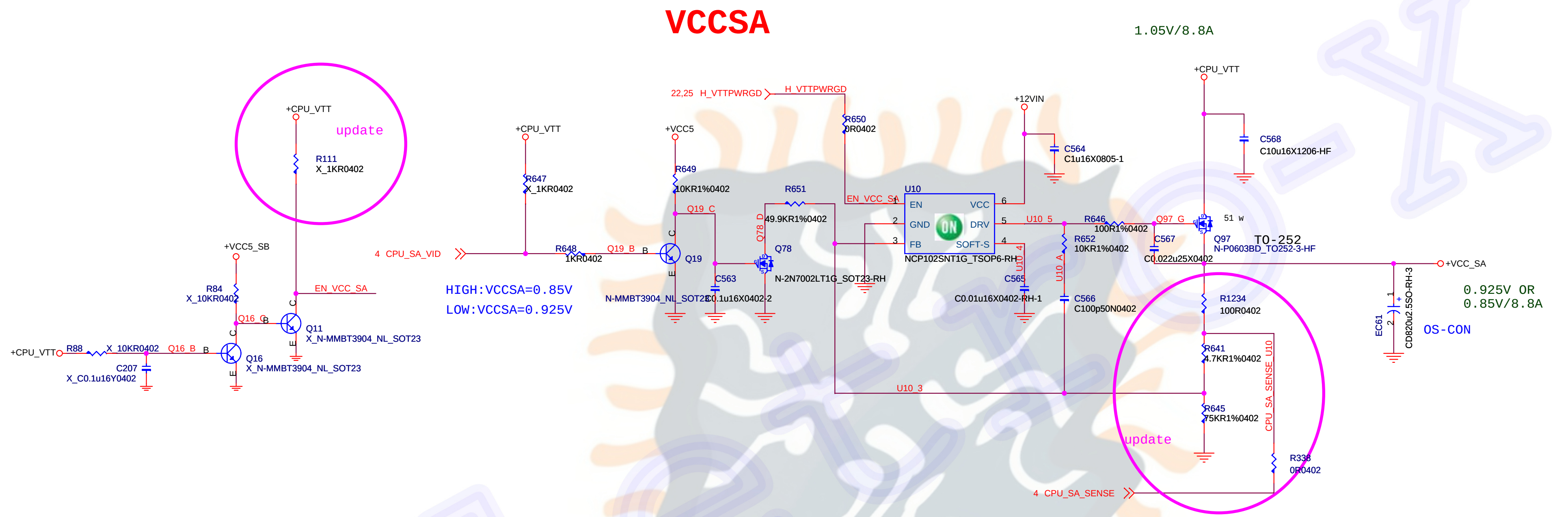

MICRO-START INT'L CO.,LTD.

Title: CPU VCC_SA

Size	Document Number	Rev
	Lenovo IH61M	1.0

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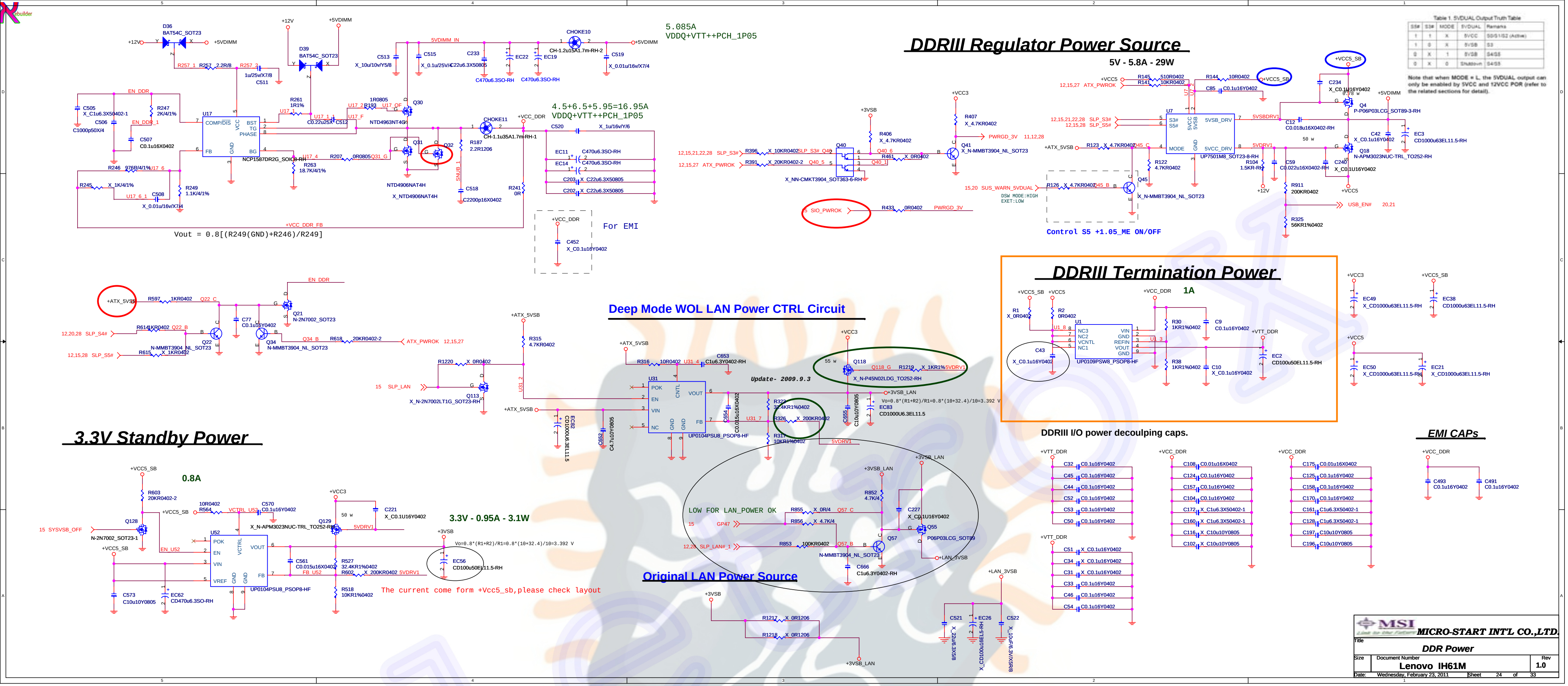
DDRIII Regulator Power Source
5V - 5.8A - 29W
5.085A
VDDQ+VTT++PCH_1P05
4.5+6.5+5.95=16.95A
VDDQ+VTT++PCH_1P05
Vout = 0.8[(R249(GND)+R246)/R249]
For EMI
Control S5 +1.05_ME ON/OFF
DSW MODE:HIGH
EXIT:LOW
Table 1. 5VDUAL Output Truth Table
Note that when MODE = L, the 5VDUAL output can only be enabled by 5VCC and 12VCC POR (refer to the related sections for detail).
DDRIII Termination Power
1A
Deep Mode WOL LAN Power CTRL Circuit
Update- 2009.9.3
Vo=0.8*(R1+R2)/R1=0.8*(10+32.4)/10=3.392 V
3.3V Standby Power
0.8A
3.3V - 0.95A - 3.1W
Vo=0.8*(R1+R2)/R1=0.8*(10+32.4)/10=3.392 V
The current come form +Vcc5_sb,please check layout
LOW FOR LAN_POWER OK
Original LAN Power Source
DDRIII I/O power decoupling caps.
EMI CAPs
MSI
MICRO-START INT'L CO.,LTD.
Title
DDR Power
Size
Document Number
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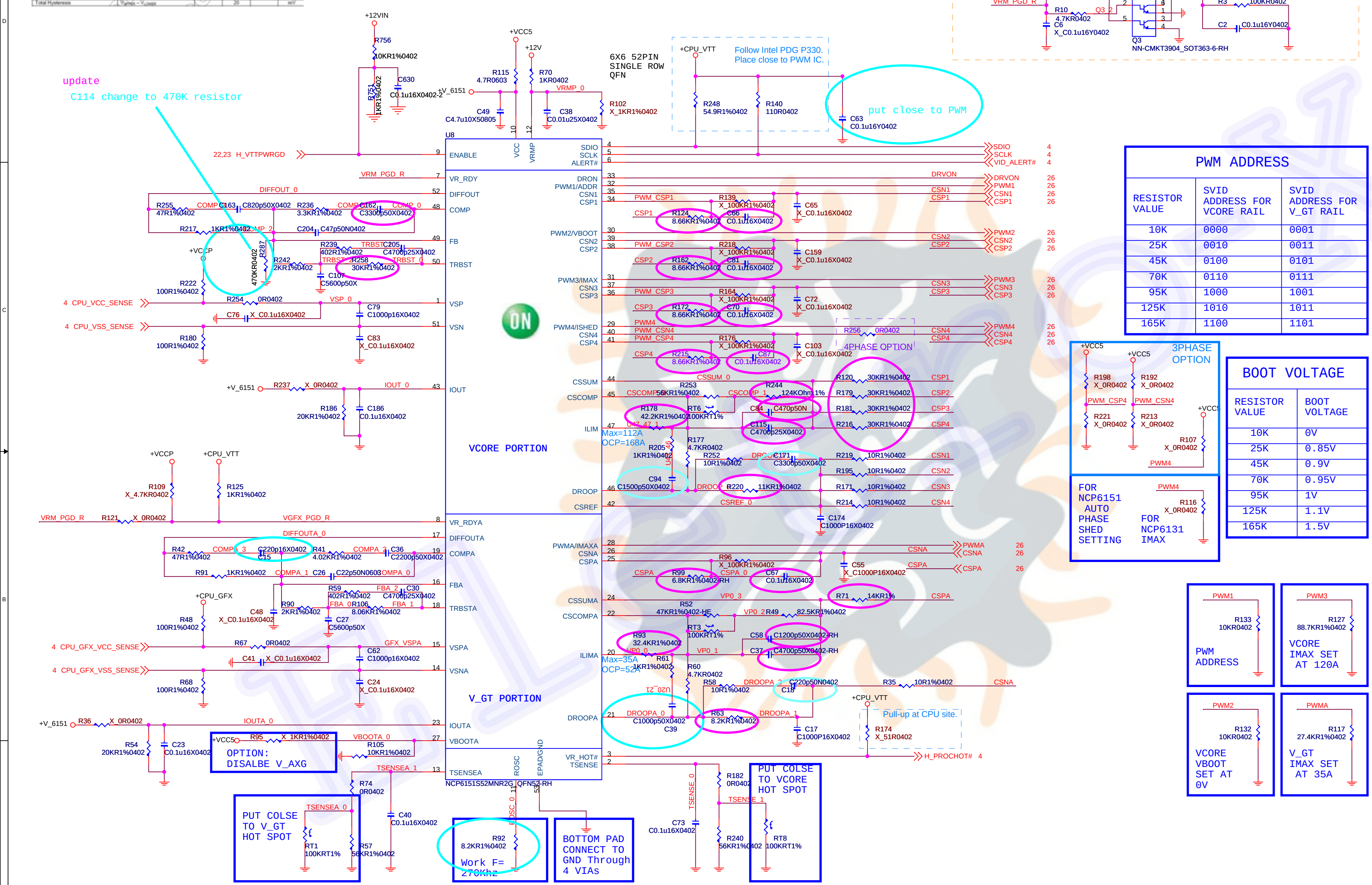
CPU CRORE : OCP Min=134A , OCP Max=168A , OVP=DAC+175mV
GFX CRORE : OCP Min=42A , OCP Max=52.5A , OVP=DAC+175mV

VOLTAGE REGULATOR MODULE (VRD12)



PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

MSI MICRO-START INT'L CO.,LTD.

Title	NCP6151S52MNR2G_QFN52-RH	
Size	Document Number: Lenovo IH61M	Rev 1.0
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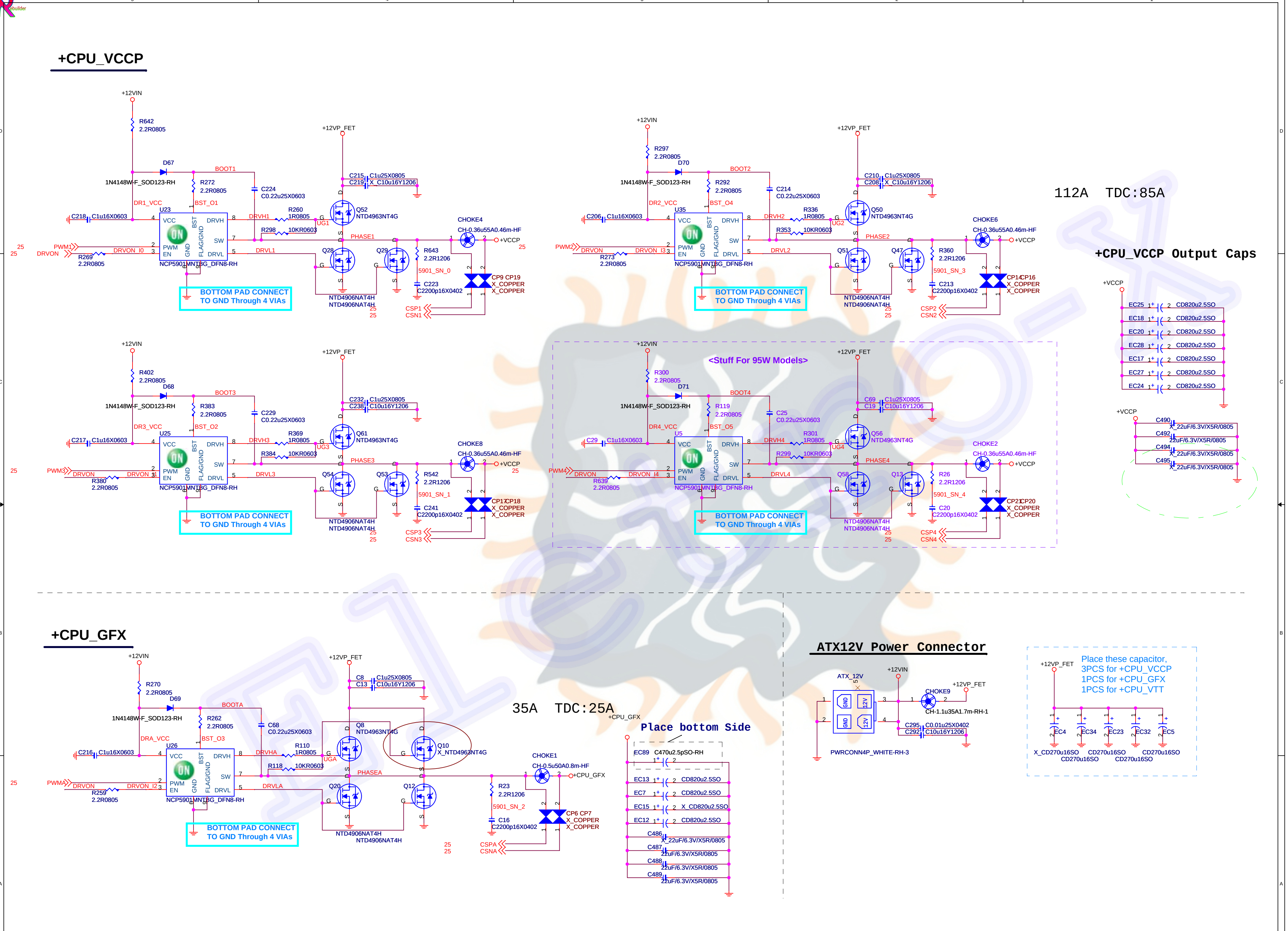
Eletro-X



MSI MICRO-START INT'L CO.,LTD.

Title: VCORE & VGFX POWER

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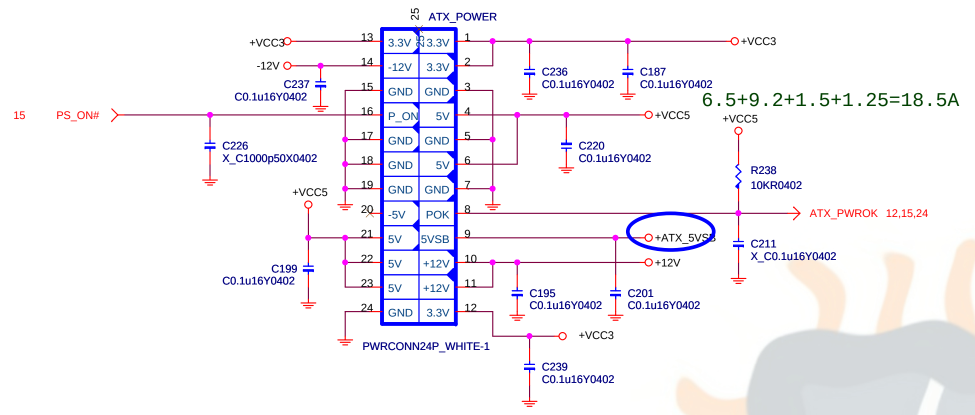
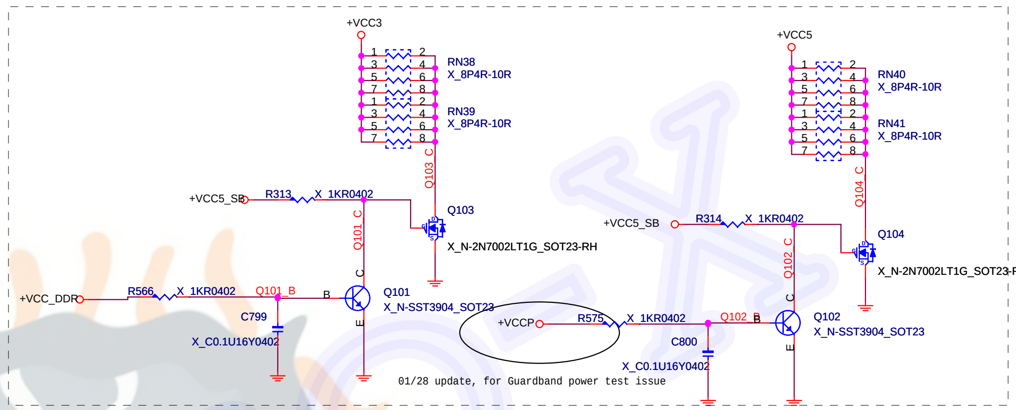
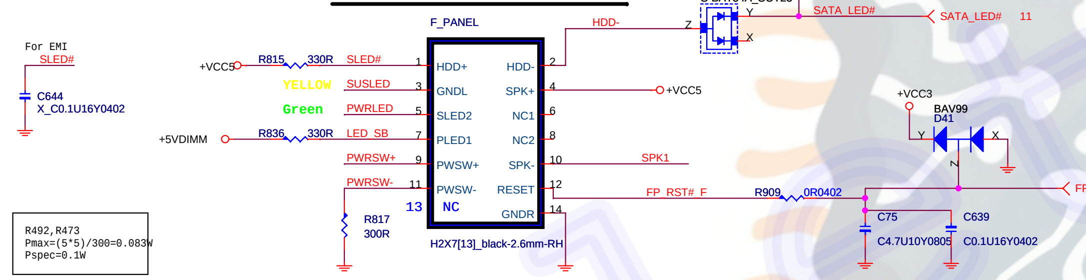
ATX Power Connector / Front Panel / LED

24 Pin ATX Power Connector

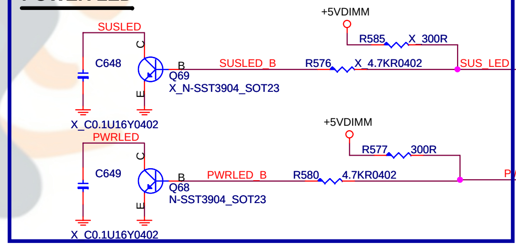




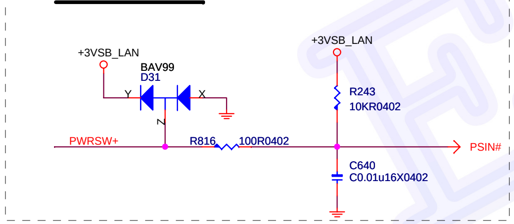
LENOVO Front Panel Connector



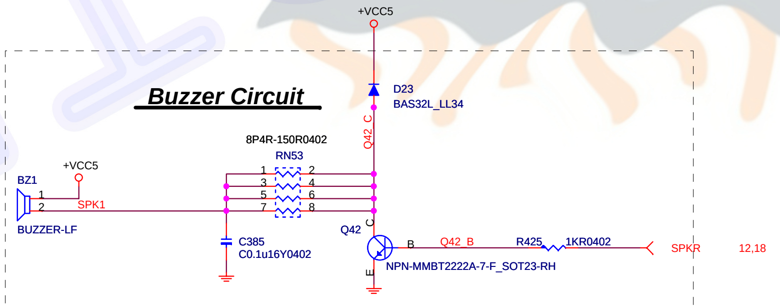
POWER LED



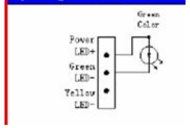
POWER BUTTON



Buzzer Circuit



2-pin single color Power LED



HD (IDE Hard Disk Active LED)	Pin 1:LED anode(+) Pin 8:LED cathode(-)
(Power LED)	Pin 3:LED cathode(-) (green) Pin 2:LED cathode(-) (yellow)
Power Switch	Open:Normal Operation Close:Power on /Off

LED Status (Dual color LED)

System State	Dual Color POWER LED State
S0	Steady Green
S1	Green Blinking (frequency is under 1Hz)
S3	Steady Yellow
S4/S5	Off
Default S5 in lose power .	Note series resistor is 330Ω

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Title	ATX Connector / Front Panel / LED		
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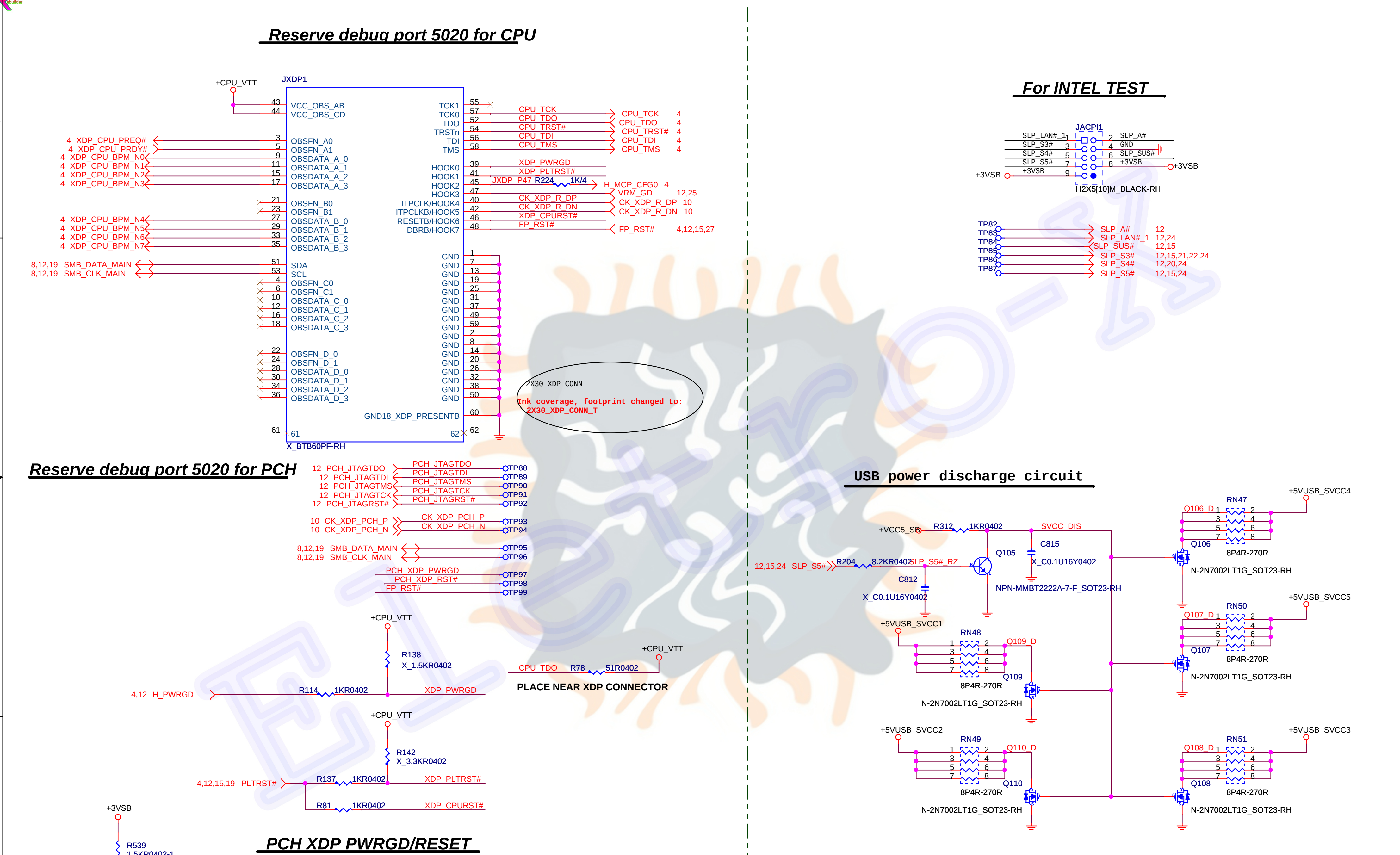

MSI MICRO-START INT'L CO.,LTD.

Title: USB PW-Discharge/BIOS_WP

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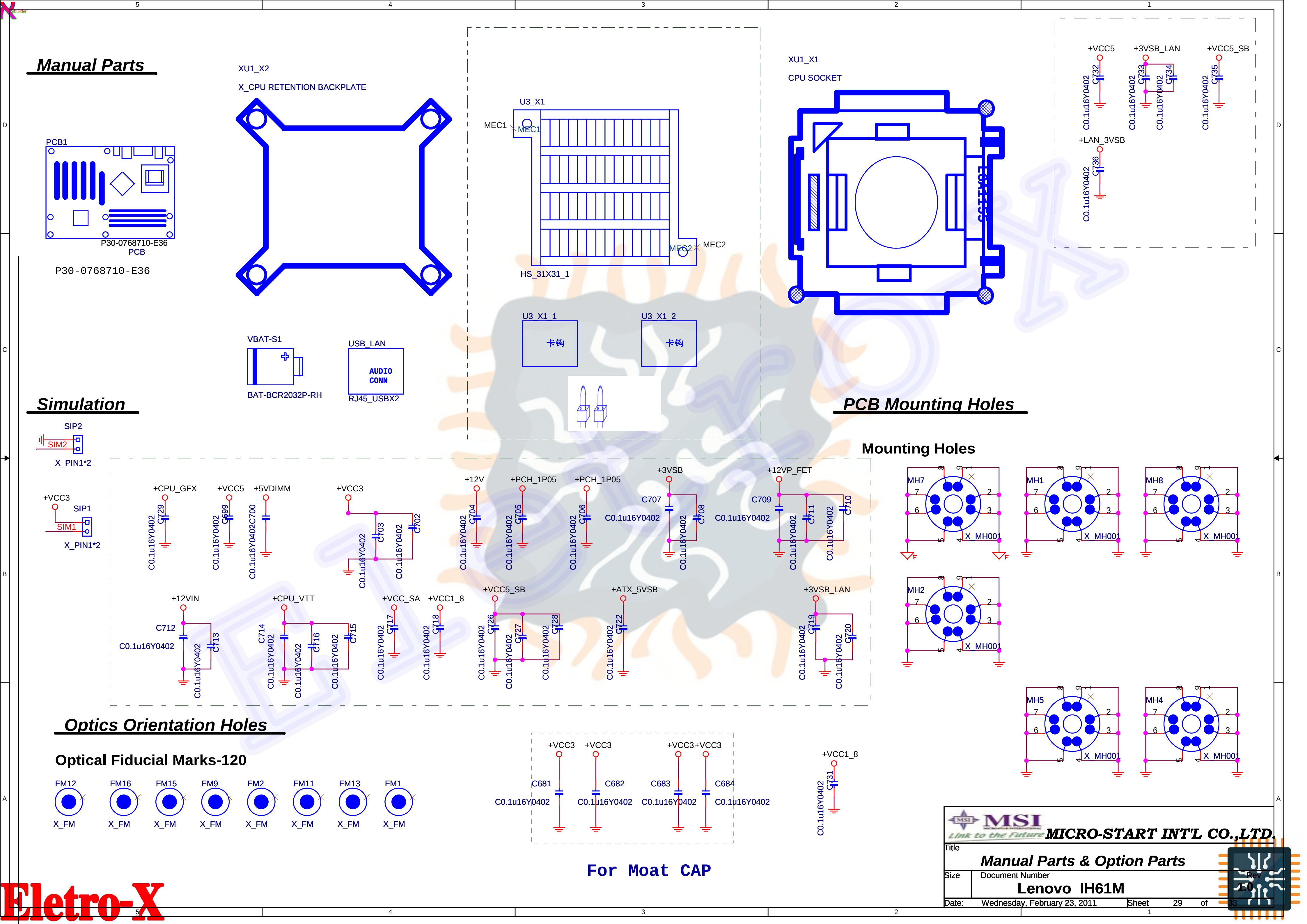

Manual Parts
PCB1
P30-0768710-E36
PCB
P30-0768710-E36
XU1_X2
X_CPU RETENTION BACKPLATE
U3_X1
MEC1
MEC1
MEC2
MEC2
HS_31X31_1
XU1_X1
CPU SOCKET
+VCC5
+3VSB_LAN
+VCC5_SB
C732
C733
C734
C735
C0.1u16Y0402
+LAN_3VSB
C736
VBAT-S1
BAT-BCR2032P-RH
USB_LAN
AUDIO
CONN
RJ45_USBX2
U3_X1_1
卡钩
U3_X1_2
卡钩
Simulation
SIP2
SIM2
X_PIN1*2
+VCC3
SIP1
SIM1
X_PIN1*2
PCB Mounting Holes
Mounting Holes
MH7
MH1
MH8
MH2
MH5
MH4
X_MH001
+CPU_GFX
+VCC5
+5VDIMM
+VCC3
+12V
+PCH_1P05
+PCH_1P05
+3VSB
+12VP_FET
C729
C699
C700
C703
C702
C704
C705
C706
C707
C708
C709
C711
C710
+12VIN
+CPU_VTT
+VCC_SA
+VCC1_8
+VCC5_SB
+ATX_5VSB
+3VSB_LAN
C712
C713
C714
C716
C715
C717
C718
C726
C727
C728
C722
C719
C720
C0.1u16Y0402
Optics Orientation Holes
Optical Fiducial Marks-120
FM12
FM16
FM15
FM9
FM2
FM11
FM13
FM1
X_FM
+VCC3
+VCC3
+VCC3+VCC3
C681
C682
C683
C684
C0.1u16Y0402
+VCC1_8
C731
For Moat CAP
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
Manual Parts & Option Parts
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