IPM61-BE
Revision: 1.00

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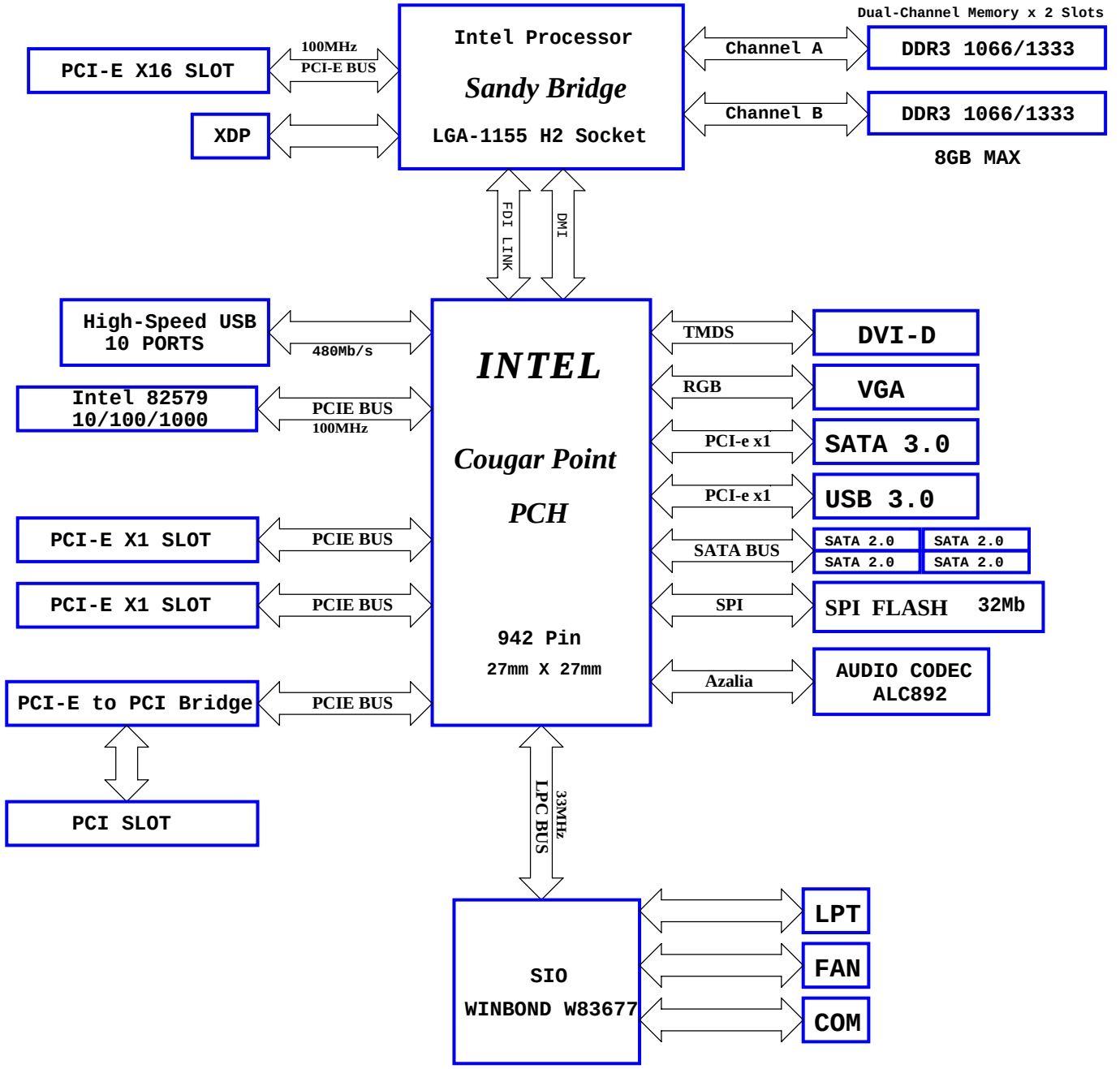
66	+0P925V_SA & +1P05V_PCH
67	5V DUAL POWER
68	+1P8V_SFR
69	+1V_USB3 & VRM_EN
70	+3P3V_LAN & +3P3V_ME
71~72	+1P05V_CPUIO
73~75	VCORE CONTROLLER + DRIVER
76	+V_AXG DRIVER
77	PS2 + USB CONN

78	EMI CAP
79	RTC/LED/SPKR/SCREW
80	BIOS and LPC header
81	Heceta Fan Control
82	CPU XDP DEBUG CONNECTOR
83	PCH XDP DEBUG CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 1 of 83

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Schematics Change History

Version	Date	Comments

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.

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Schematics Change History

Version	Date	Comments

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.

PROTO = PROTO Phase Only.
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PEGATRON Title : CHANGE HISTORY-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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PCH Buffer Through Mode for Pre-Silicon

XMM3 / XMM4

XMM1 / XMM2

M_CHA_CLK[0..3]/#

M_CHB_CLK[0..3]/#

Intel Processor

Sandy Bridge

LGA-1155 Pin Socket

RSVD_001/002

BCLK/#_0

CPU XDP

CK_100M_DMI/#

Intel

Platform Controller Hub

Cougar Point

942 Pin

CK_100M_CPUXDP/#
100 MHz

CK_100M_CPU_XDP/#_CK505

CK_100M_PCHXDP/#
100 MHz

PCH XDP

CK_100M_PE16/#
100 MHz

PCIEx16 Slot

CK_100M_PE1/#
100 MHz

PCIEx1 Slot

CK_100M_LAN/#
100 MHz

Intel 82579

25 MHz

CK505

SLG8SP424VTR
ICS9LRS4180A/B

32 Pin

14.318MHz

CK_100M_DMI2/#_CK505

CK_133M_BCLK_CK505/#

CK_100M_DMI_CK505/#

CK_100M_SATA_CK505/#

CK_96M_DOT_CK505/#

CK_14M_REF_CK505

CLKIN_GND1_P/N

CLKIN_GND0_P/N

CLKIN_DMI_P/N

CLKIN_SATA_P/N

CLKIN_DOT_96_P/N

REFCLK14IN

NOTE:
Reserved PD resistors for FCIM

CK_33M_TPM
33 MHz

TPM Header

CK_48M_SIO
48 MHz

W83677

CK_48M_SIO_CK505
48 MHz

CK_33M_SIO
33 MHz

CK_33M_SL1
33 MHz

PCI Slot

CK_33M_PCIFB

CKKIN_PCILOOPBACK

HDA_BCLK

AZ_BITCLK
24 MHz

AUDIO CODEC
ALC892

SPI_CLK

SPI_CLK
33 MHz

SPI ROM

XTAL25_IN

RTCX

25MHz

32.768KHz

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CLCOK DISTRIBUTION

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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Intel AMT 7.0 and non-DSW supported

PCI_Express x 16 PWRGD
PCI_Express x 4 PWRGD
PCI_Express x 1 PWRGD
<28>PCIE_RST#
<28>PCIE_RST#
<28>PCIE_RST#

<29>PCH_PCIRST# → RST# PCI SLOT #1
<27>PLTRST# → PE_RSTN LAN 82579
USB3.0 PERSTB
<27.1>PLTRST_CPU#

RESET_SWITCH

POWER_SWITCH
<4>PWRBTN#

W83677
PWSIN#
PCIRST3#
PCIRST2#
PCIRST1#
LRESET#
KBRST#
RSMRST#
PWSOUT#
S3#
S4#
PS_ON#
ATXPG_IN
PWROK

<27>PLTRST#
RST_KB#
<9>RSMRST#
<4>SB_PWRBTN#

2X12 ATX PSU
PSON#
PWROK
<15>PSON#
<21>ATX_PWRGD

PCH
HDA_RST# → AZ_RST# → RESET# AUDIO ALC8889
SYS_RESET# ← SYS_RESET#
PCIRST#
PLTRST#
RCIN#
RSMRST#
PWRBTN#
SLP_S3#
SLP_S4#
SLP_A#
SLP_LAN#
SLP_SUS#
SUS_WARN#
SUS_ACK#
DPWROK
PWROK
APWROK
DRAMPWROK → <23>DRAM_PWROK
RTCRST# ← <1>RTCRST# ← BATTERY
PROCPWROGD → <24>CPUPWRGD
SYS_PWROK → <26>VRM_PWRGD

<13>SLP_S3#
<12>SLP_S4#
<11>SLP_A#
<10>SLP_LAN#
<7>SLP_SUS#
<5>SUS_WARN#
<6>SUS_ACK#
<3>PCH_DPWROK

PROCESSOR
DBR#
RESET#
SM_DRAMPWROK
UNCOREPWRGOOD
VIDSOUT/VIDSCLK
VCORE

CPU SVID buffers are Hi-Z once +1P05V_CPUIO is stable and UNCOREPWRGOOD = 0
<20~24>SVIDs

<22>PWROK
<14>APWROK

ME & LAN POWER
+1P05V_ME
+3P3V_LAN
+3P3V_ME

STANDBY POWER
<8> +5VSB
+3P3VSB

<2>+5VA
2X12 ATX PSU
<2>+5VA

MB Logic
MB Logic
MB Logic

CK505
CKPWRGD/PD#
<22>CK505_PWRGD

Vcore Controller
VR_RDY
VDIO/VCLK
VCORE
EN
<25>VCORE
<16>+1P05V_CPUIO
<19>+1P05V_CPUIO
RT8859AGQW

<16>
+1P05V_CPUIO
PWRGD
NCP5380MNTXG
<17>1P05V_CPUIO_PWRGD

<18>
+0P925V_SA
EN
LM358

ONBOARD POWER
CHIP
SOCKET or SLOT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIGNAL&RESET MAP
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
Date: Friday, September 24, 2010 | Sheet 5 of 83

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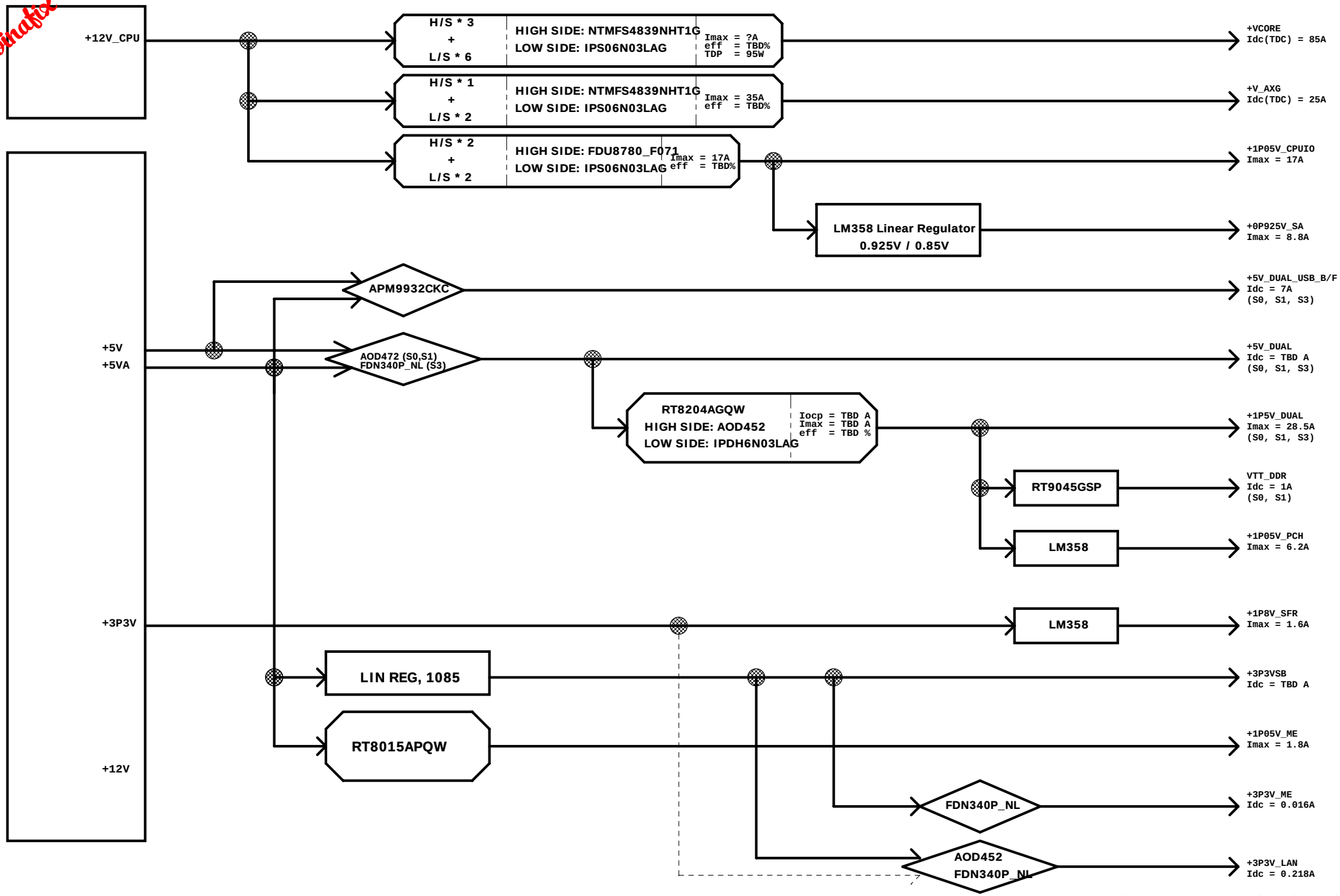

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER FLOW

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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CPU Sandy Bridge	
+VCORE	-> 95A(TDC) - 95W
+1P05V_CPUIO	-> 17A(Imax) - W
+0P925V_SA	-> 8.8A(Imax) - W
+V_AXG	-> 25A(TDC) - W

CLOCK GEN	
+3P3V	-> 125mA - W

PCH	
+1P05V_PCH	-> 5.831A - W
+1P05V_CPUIO	-> 0.043A - W
+1P8V_SFR	-> 0.16A - W
+3P3V	-> 0.267A - W
+3P3VSB	-> 0.107A - W
+1P05V_ME	-> 1.01A - W
+3P3V_ME	-> 0.02A - W
+3P3VA	-> 0.002A - W
+BATT	RTC(G3) -> 6uA - 0.0198mW

DDR2 DIMM (4) & Termination	
+1P5V_DAUL	VDD (S0, S1,S3) ->7.5 A - 11.25W
+VTT_DDR(0.75V)	SM VTT (S0, S1) -> 1A - 0.75W

PCI Express x 1	
+12V	-> 5A - 60W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

PCI Express x 16	
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

PCI SLOTS	
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.6A - 25.08W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

INTEL 82579	
+3P3V_LAN	-> mA - 720mW

83677	
+3P3V	-> 35mA - mW

ALC892	
+3P3V	-> mA - mW

FL1009 USB3.0	
+3P3V	-> mA - W
+1P05V_USB	-> mA - W

USB 14 PORTS	
+5V_DUAL_B/F	(S0, S1) -> 7A - 35W

DVI	
+5V	-> mA - mW
	-> mA - mW

FANS	
+12V	-> 1.2A - 14.4W

PS2 KB/MS	
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW

SPI	
+3P3V_ME	-> 30mA - 99mW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER DISTRIBUTION

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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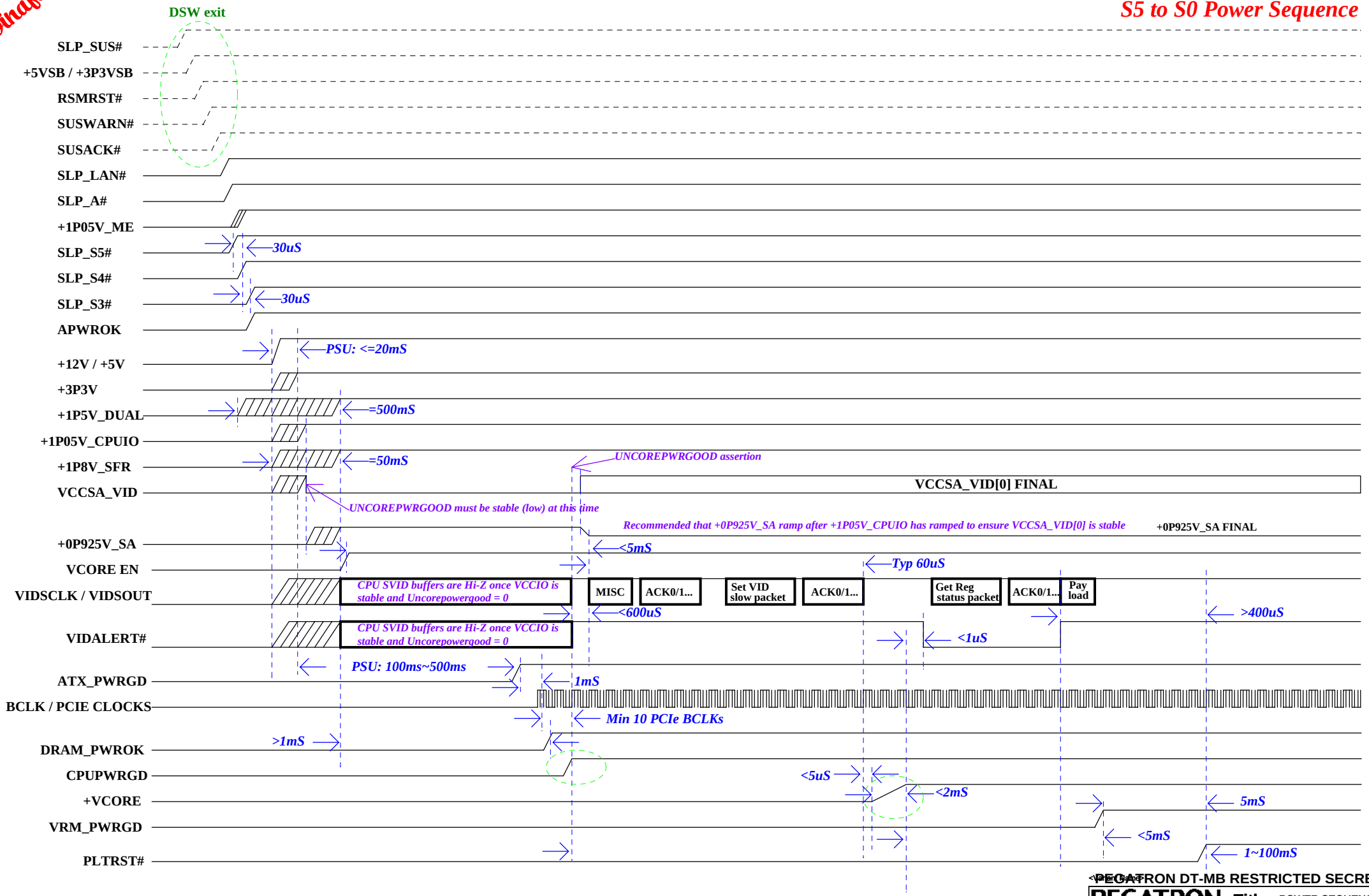
S5 to S0 Power Sequence



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER SEQUENCE

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 8 of 83

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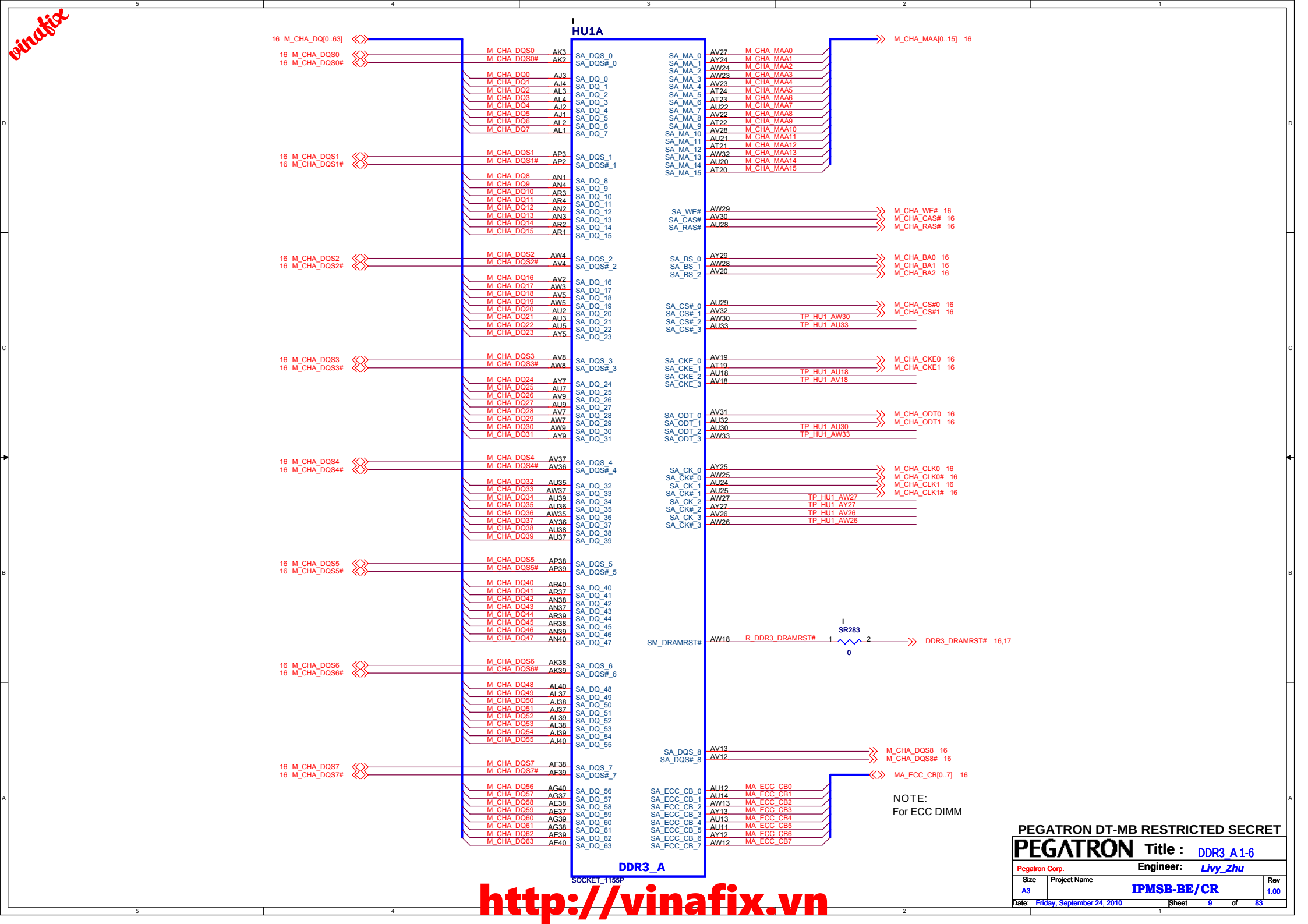

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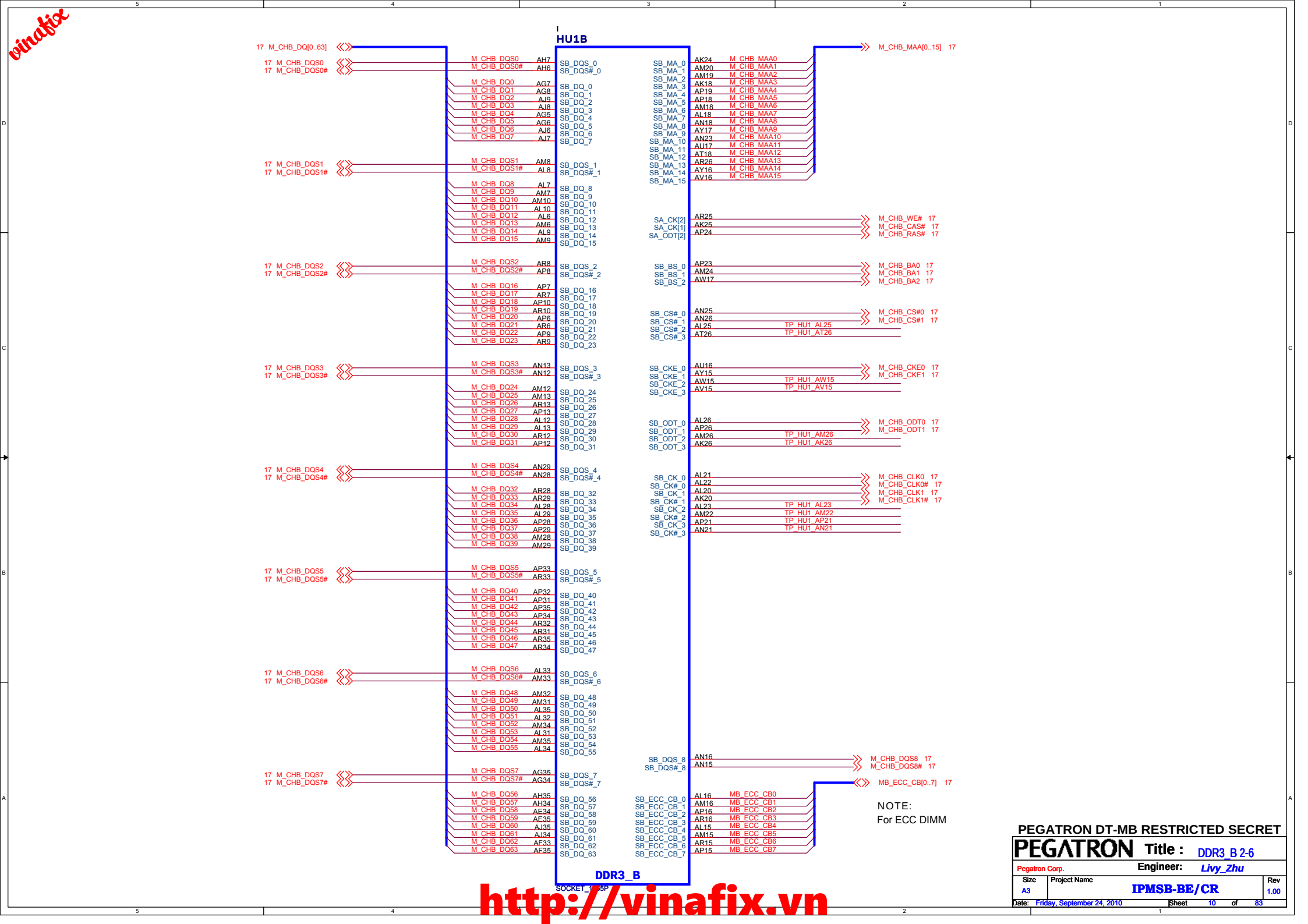
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3_A 1-6	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 9 of 83	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3_B 2-6	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 10 of 83	

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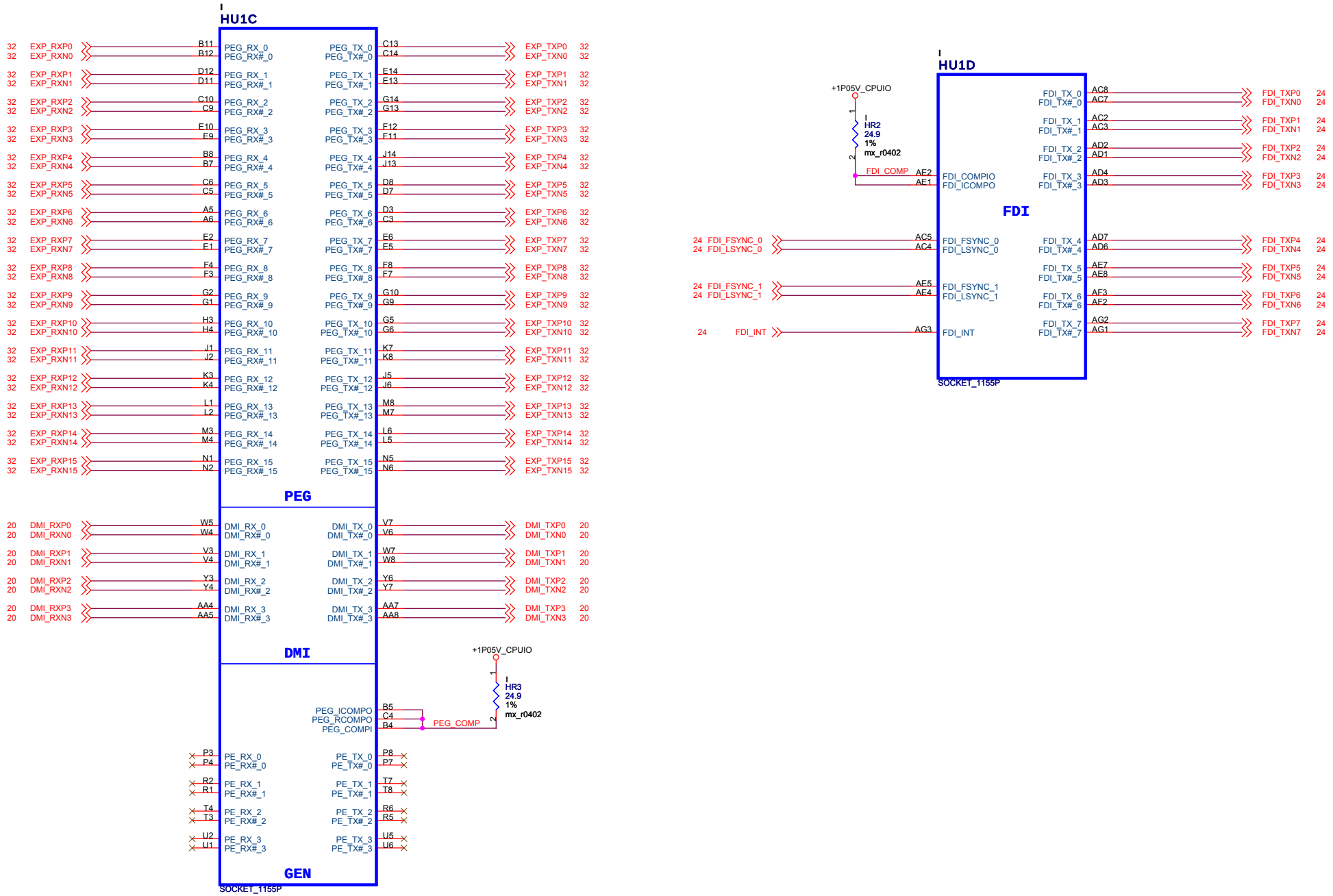

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/DMI/FDI 3-6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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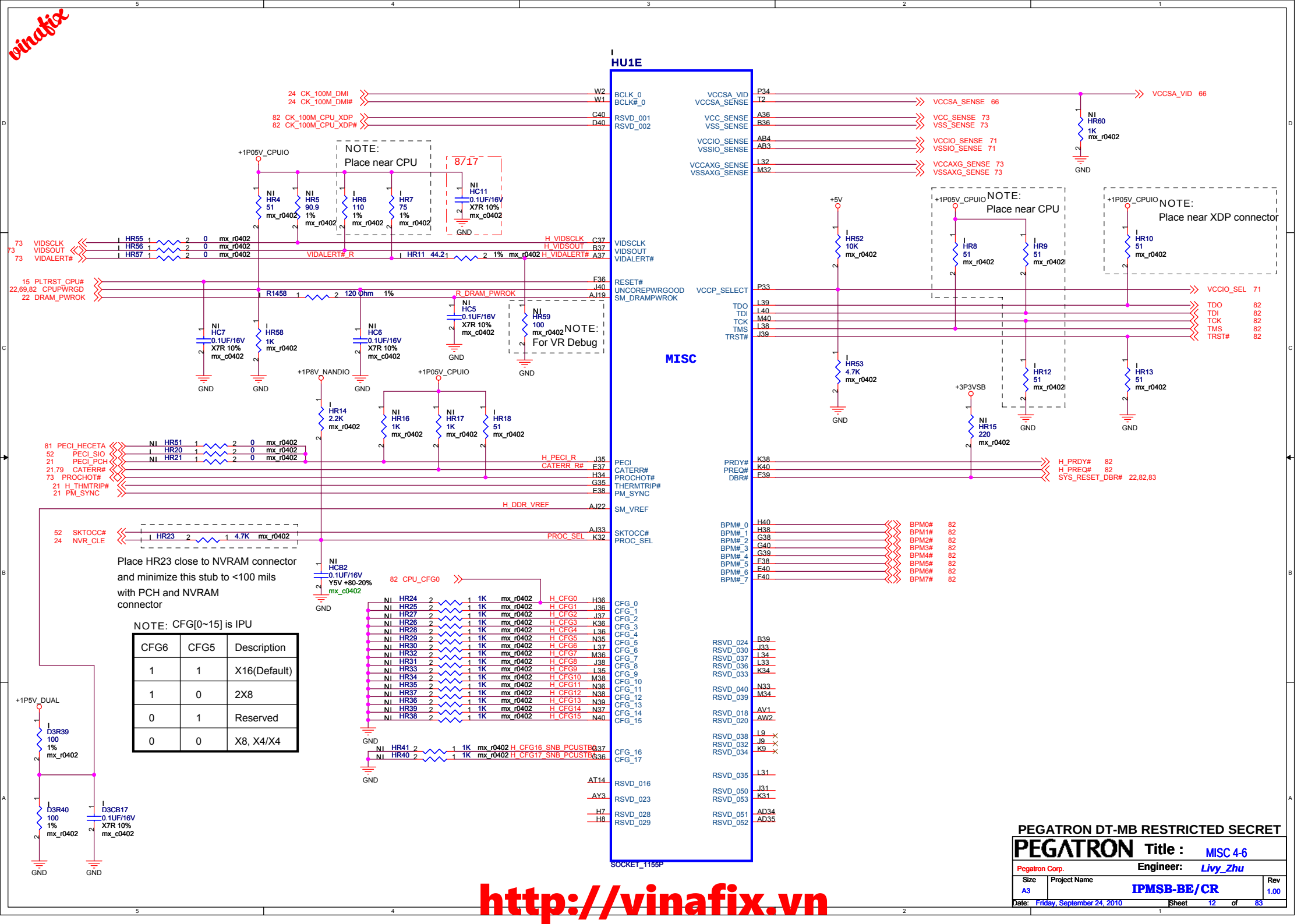
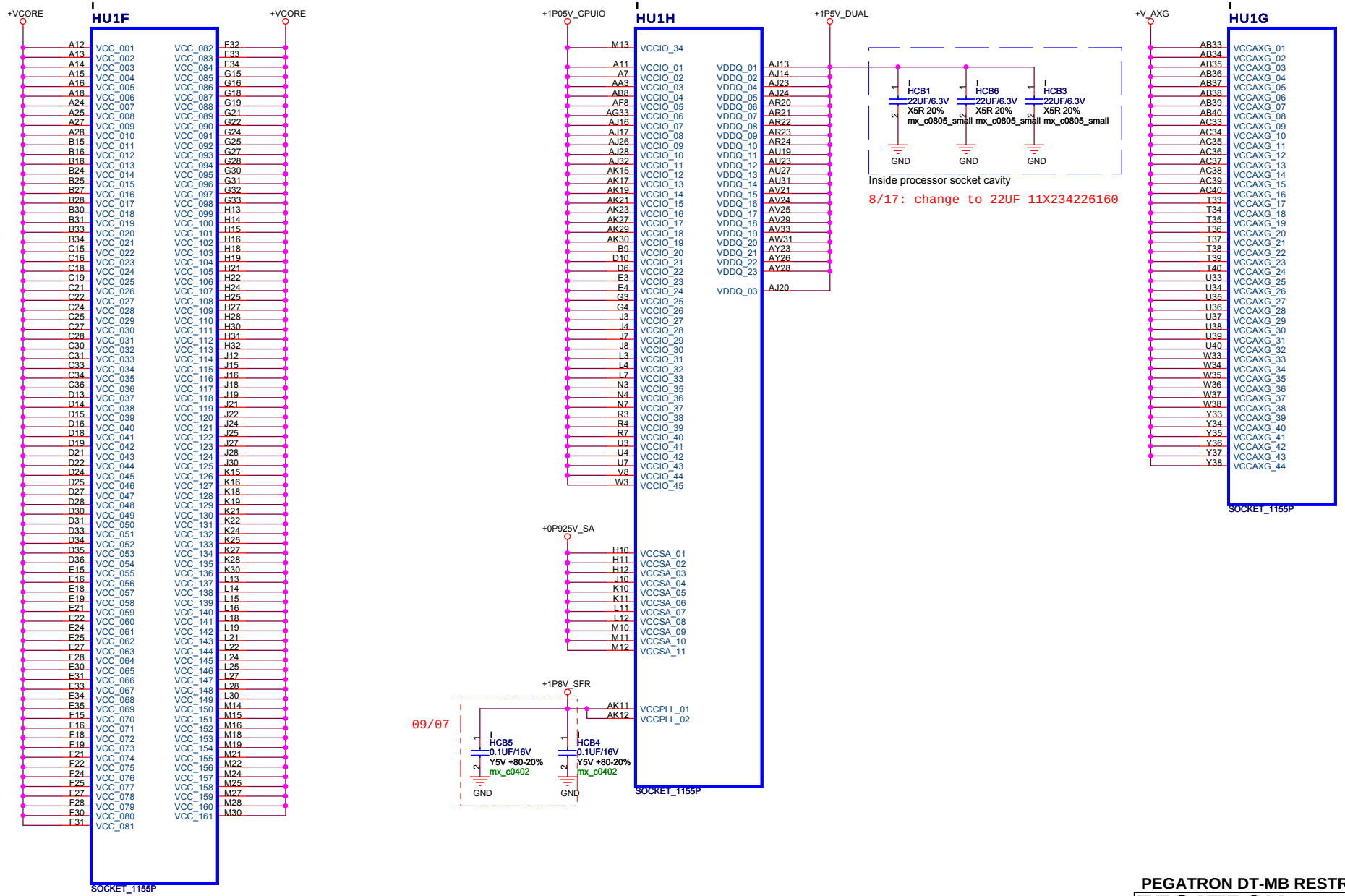

HU1E
MISC
SOCKET_1155P
NOTE: Place near CPU
NOTE: For VR Debug
NOTE: Place near XDP connector
Place HR23 close to NVRAM connector and minimize this stub to <100 mils with PCH and NVRAM connector
NOTE: CFG[0~15] is IPU
CFG6 CFG5 Description
1 1 X16(Default)
1 0 2X8
0 1 Reserved
0 0 X8, X4/X4
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : MISC 4-6
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 12 of 83
http://vinafix.vn



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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCC 5 - 6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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HU1I

SOCKET_1155P

A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AN10
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AN14
AC1	VSS_014	VSS_104	AN17
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AN22
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD5	VSS_021	VSS_111	AN32
AD8	VSS_022	VSS_112	AN33
AE3	VSS_023	VSS_113	AN34
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	AN36
AF1	VSS_026	VSS_116	AN5
AF34	VSS_027	VSS_117	AN6
AF36	VSS_028	VSS_118	AN7
AF37	VSS_029	VSS_119	AN8
AF40	VSS_030	VSS_120	AN9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH33	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP37
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP40
AH5	VSS_043	VSS_133	AP5
AH8	VSS_044	VSS_134	AR11
AJ12	VSS_045	VSS_135	AR14
AJ15	VSS_046	VSS_136	AR17
AJ18	VSS_047	VSS_137	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
AM21	VSS_088	VSS_178	AU6
AM23	VSS_089	VSS_179	AU8
AM25	VSS_090	VSS_180	AV10
A4	VSS_NCTF_01		
AV39	VSS_NCTF_02		

GND

HU1J

SOCKET_1155P

AV11	VSS_181	VSS_271	G8
AV14	VSS_182	VSS_272	H1
AV17	VSS_183	VSS_273	H17
AV3	VSS_184	VSS_274	H2
AV35	VSS_185	VSS_275	H20
AV38	VSS_186	VSS_276	H23
AV6	VSS_187	VSS_277	H26
AW10	VSS_188	VSS_278	H29
AW11	VSS_189	VSS_279	H33
AW14	VSS_190	VSS_280	H35
AW16	VSS_191	VSS_281	H37
AW36	VSS_192	VSS_282	H39
AW6	VSS_193	VSS_283	H5
AY11	VSS_194	VSS_284	H6
AY14	VSS_195	VSS_285	H9
AY18	VSS_196	VSS_286	J11
AY35	VSS_197	VSS_287	J17
AY4	VSS_198	VSS_288	J20
AY6	VSS_199	VSS_289	J23
AY8	VSS_200	VSS_290	J26
B10	VSS_201	VSS_291	J29
B13	VSS_202	VSS_292	J32
B14	VSS_203	VSS_293	K1
B17	VSS_204	VSS_294	K12
B23	VSS_205	VSS_295	K13
B26	VSS_206	VSS_296	K14
B29	VSS_207	VSS_297	K17
B32	VSS_208	VSS_298	K2
B35	VSS_209	VSS_299	K20
B38	VSS_210	VSS_300	K23
B6	VSS_211	VSS_301	K26
C11	VSS_212	VSS_302	K29
C12	VSS_213	VSS_303	K33
C17	VSS_214	VSS_304	K35
C20	VSS_215	VSS_305	K37
C23	VSS_216	VSS_306	K39
C26	VSS_217	VSS_307	K5
C29	VSS_218	VSS_308	K6
C32	VSS_219	VSS_309	L10
C35	VSS_220	VSS_310	L17
C7	VSS_221	VSS_311	L20
C8	VSS_222	VSS_312	L23
D17	VSS_223	VSS_313	L26
D2	VSS_224	VSS_314	L29
D20	VSS_225	VSS_315	L8
D23	VSS_226	VSS_316	M1
D26	VSS_227	VSS_317	M17
D29	VSS_228	VSS_318	M2
D32	VSS_229	VSS_319	M20
D37	VSS_230	VSS_320	M23
D39	VSS_231	VSS_321	M26
D4	VSS_232	VSS_322	M29
D5	VSS_233	VSS_323	M33
D9	VSS_234	VSS_324	M35
E11	VSS_235	VSS_325	M37
E12	VSS_236	VSS_326	M39
E17	VSS_237	VSS_327	M5
E20	VSS_238	VSS_328	M6
E23	VSS_239	VSS_329	M9
E26	VSS_240	VSS_330	N8
E29	VSS_241	VSS_331	P1
E32	VSS_242	VSS_332	P2
E36	VSS_243	VSS_333	P36
E7	VSS_244	VSS_334	P38
E8	VSS_245	VSS_335	P40
F1	VSS_246	VSS_336	P5
F10	VSS_247	VSS_337	P6
F13	VSS_248	VSS_338	R33
F14	VSS_249	VSS_339	R35
F17	VSS_250	VSS_340	R37
F2	VSS_251	VSS_341	R39
F20	VSS_252	VSS_342	R8
F23	VSS_253	VSS_343	T1
F26	VSS_254	VSS_344	T5
F29	VSS_255	VSS_345	T6
F35	VSS_256	VSS_346	U8
F37	VSS_257	VSS_347	V1
F39	VSS_258	VSS_348	V2
F5	VSS_259	VSS_349	V33
F6	VSS_260	VSS_350	V34
F9	VSS_261	VSS_351	V35
G11	VSS_262	VSS_352	V36
G12	VSS_263	VSS_353	V37
G17	VSS_264	VSS_354	V38
G20	VSS_265	VSS_355	V39
G23	VSS_266	VSS_356	V40
G26	VSS_267	VSS_357	V5
G29	VSS_268	VSS_358	W6
G34	VSS_269	VSS_359	Y5
G7	VSS_270	VSS_360	Y8
AY37	VSS_NCTF_03		
B3	VSS_NCTF_04		

GND

HU1K

SOCKET_1155P

AB7	RSVD_04	FC_AH1	AH1
AD37	RSVD_05	FC_AH4	AH4
AG4	RSVD_08		
AJ29	RSVD_10	RSVD_15	AT11
AJ30	RSVD_11	RSVD_14	AP20
AJ31	RSVD_12	RSVD_13	AN20
AV34	RSVD_19	RSVD_17	AU10
AW34	RSVD_21	RSVD_22	AY10
P35	RSVD_43		
P37	RSVD_44		
P39	RSVD_45		
R34	RSVD_46		
R36	RSVD_47		
R38	RSVD_48	RSVD_07	AF4
R40	RSVD_49	RSVD_03	AB6
		RSVD_06	AE6
		RSVD_09	AJ11
A38	NCTF_01	RSVD_27	D38
AU40	NCTF_02	RSVD_26	C39
AW38	NCTF_03	RSVD_25	C38
C2	NCTF_04	RSVD_31	J34
D1	NCTF_05	RSVD_41	N34
		NP_NC1	1
		NP_NC2	2
		NP_NC3	3
		NP_NC4	4
		NP_NC5	5
		NP_NC6	6
		NP_NC7	7

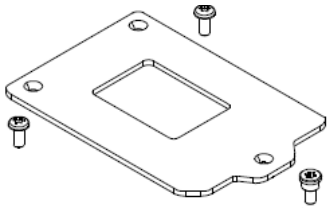
NOBOM HT38 1 TP_H_NCTF_A38

SA_DIMM_VR
SB_DIMM_VR

HR42 1 2 0 mx_r0402 DIMM_DQ_VREF_A 16
HR43 1 2 0 mx_r0402 DIMM_DQ_VREF_B 17

HC2 0.1UF/16V Y5V +80-20% mx_c0402 GND
HC3 0.1UF/16V Y5V +80-20% mx_c0402 GND

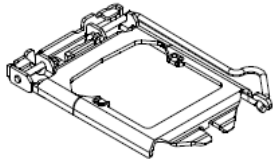
BACKPLATE1



INTEL LGA 1156P BACK PLATE,3 SCREW

PT44P11-6401

ILM1



INTEL LGA1156 SOCKET ILM

SOCKET1156_ILM

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 6 - 6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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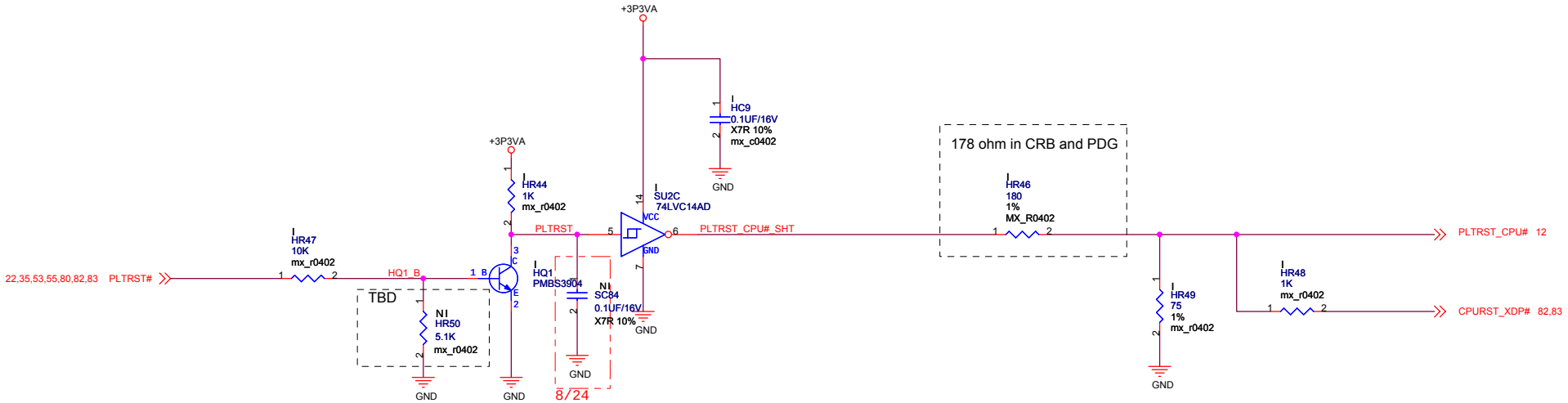
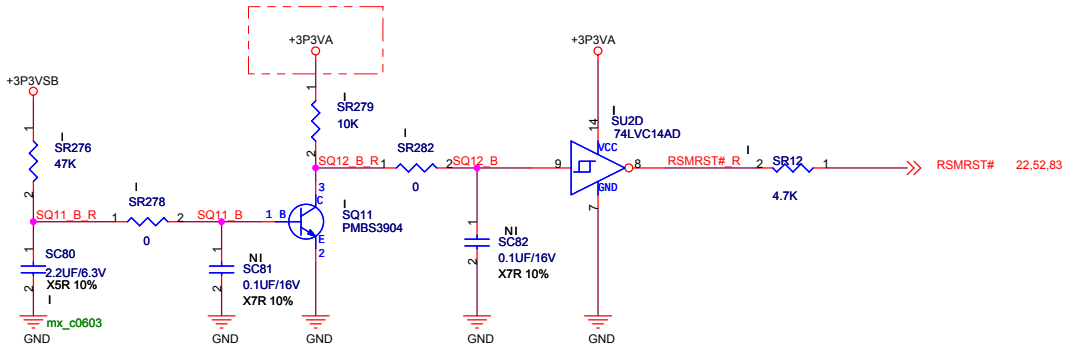


PLTRST_CPU#



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PLTRST_CPU#	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 15 of 83	

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XMM1 COLOR: BLUE

IDIMMA0A

M_CHA_MAA0 188 A0
M_CHA_MAA1 181 A1
M_CHA_MAA2 61 A2
M_CHA_MAA3 180 A3
M_CHA_MAA4 59 A4
M_CHA_MAA5 58 A5
M_CHA_MAA6 178 A6
M_CHA_MAA7 56 A7
M_CHA_MAA8 177 A8
M_CHA_MAA9 175 A9
M_CHA_MAA10 70 A10/AP
M_CHA_MAA11 55 A11
M_CHA_MAA12 174 A12
M_CHA_MAA13 196 A13
M_CHA_MAA14 172 A14
M_CHA_MAA15 171 A15

9 M_CHA_CLK1 63 CK1P/NU
9 M_CHA_CLK1# 64 CK1N/NU
9 M_CHA_CLK0 184 CK0P
9 M_CHA_CLK0# 185 CK0N

9 M_CHA_CS#1 76 CS1#
9 M_CHA_CS#0 193 CS0#

9 M_CHA_CKE1 169 CKE1
9 M_CHA_CKE0 50 CKE0

9 M_CHA_BA2 52 BA2
9 M_CHA_BA1 190 BA1
9 M_CHA_BA0 71 BA0

17,54,81,82,83 SMB_DATA_MAIN 238 SDA
17,54,81,82,83 SMB_CLK_MAIN 118 SCL

9 MA_ECC_CB[0..7]
MA_ECC_CB7 165 CB7
MA_ECC_CB6 164 CB6
MA_ECC_CB5 159 CB5
MA_ECC_CB4 158 CB4
MA_ECC_CB3 46 CB3
MA_ECC_CB2 45 CB2
MA_ECC_CB1 40 CB1
MA_ECC_CB0 39 CB0

237 SA1
117 SA0
GND

9 M_CHA_WE# 73 WE#
9 M_CHA_RAS# 192 RAS#
9 M_CHA_CAS# 74 CAS#

9 M_CHA_ODT1 77 ODT1
9 M_CHA_ODT0 195 ODT0

9,17 DDR3_DRAMRST# 168 RESET#

NI
HC1
150PF/50V
NPO 5%
mx_c0402
GND

161 DM8/DQS17P
162 NC/DQS17N
230 DM7/DQS16P
231 NC/DQS16N
221 DM6/DQS15P
222 NC/DQS15N
212 DM5/DQS14P
213 NC/DQS14N
203 DM4/DQS13P
204 NC/DQS13N
152 DM3/DQS12P
153 NC/DQS12N
143 DM2/DQS11P
144 NC/DQS11N
134 DM1/DQS10P
135 NC/DQS10N
126 DM0/DQS9P
125 NC/DQS9N
43 NC/DQS8P
42 NC/DQS8N

9 M_CHA_DQS8
9 M_CHA_DQS8#

198 FREE1
187 FREE2
49 FREE3
48 FREE4

GND

DQ63 234 M_CHA_DQ63
DQ62 233 M_CHA_DQ62
DQ61 228 M_CHA_DQ61
DQ60 227 M_CHA_DQ60
DQ59 115 M_CHA_DQ59
DQ58 114 M_CHA_DQ58
DQ57 109 M_CHA_DQ57
DQ56 108 M_CHA_DQ56
DQ55 225 M_CHA_DQ55
DQ54 224 M_CHA_DQ54
DQ53 219 M_CHA_DQ53
DQ52 218 M_CHA_DQ52
DQ51 106 M_CHA_DQ51
DQ50 105 M_CHA_DQ50
DQ49 100 M_CHA_DQ49
DQ48 99 M_CHA_DQ48
DQ47 216 M_CHA_DQ47
DQ46 215 M_CHA_DQ46
DQ45 210 M_CHA_DQ45
DQ44 209 M_CHA_DQ44
DQ43 97 M_CHA_DQ43
DQ42 96 M_CHA_DQ42
DQ41 91 M_CHA_DQ41
DQ40 90 M_CHA_DQ40
DQ39 207 M_CHA_DQ39
DQ38 206 M_CHA_DQ38
DQ37 201 M_CHA_DQ37
DQ36 200 M_CHA_DQ36
DQ35 88 M_CHA_DQ35
DQ34 87 M_CHA_DQ34
DQ33 82 M_CHA_DQ33
DQ32 81 M_CHA_DQ32
DQ31 156 M_CHA_DQ31
DQ30 155 M_CHA_DQ30
DQ29 150 M_CHA_DQ29
DQ28 149 M_CHA_DQ28
DQ27 37 M_CHA_DQ27
DQ26 36 M_CHA_DQ26
DQ25 31 M_CHA_DQ25
DQ24 30 M_CHA_DQ24
DQ23 147 M_CHA_DQ23
DQ22 146 M_CHA_DQ22
DQ21 141 M_CHA_DQ21
DQ20 140 M_CHA_DQ20
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DQ18 27 M_CHA_DQ18
DQ17 22 M_CHA_DQ17
DQ16 21 M_CHA_DQ16
DQ15 138 M_CHA_DQ15
DQ14 137 M_CHA_DQ14
DQ13 132 M_CHA_DQ13
DQ12 131 M_CHA_DQ12
DQ11 19 M_CHA_DQ11
DQ10 18 M_CHA_DQ10
DQ9 13 M_CHA_DQ9
DQ8 12 M_CHA_DQ8
DQ7 129 M_CHA_DQ7
DQ6 128 M_CHA_DQ6
DQ5 123 M_CHA_DQ5
DQ4 122 M_CHA_DQ4
DQ3 10 M_CHA_DQ3
DQ2 9 M_CHA_DQ2
DQ1 4 M_CHA_DQ1
DQ0 3 M_CHA_DQ0

DQS7P 112 M_CHA_DQS7 9
DQS7N 111 M_CHA_DQS7# 9
DQS6P 103 M_CHA_DQS6 9
DQS6N 102 M_CHA_DQS6# 9
DQS5P 94 M_CHA_DQS5 9
DQS5N 93 M_CHA_DQS5# 9
DQS4P 85 M_CHA_DQS4 9
DQS4N 84 M_CHA_DQS4# 9
DQS3P 34 M_CHA_DQS3 9
DQS3N 33 M_CHA_DQS3# 9
DQS2P 25 M_CHA_DQS2 9
DQS2N 24 M_CHA_DQS2# 9
DQS1P 16 M_CHA_DQS1 9
DQS1N 15 M_CHA_DQS1# 9
DQS0P 7 M_CHA_DQS0 9
DQS0N 6 M_CHA_DQS0# 9

RESERVED 79

NC/PAR_IN 68
NC/ERR_OUT 53
NC/TEST4 167

DDR3_DIMM_240P

M_CHA_DQ[0..63] 9
M_CHA_MAA[0..15] 9

SMB_DATA_MAIN
SMB_CLK_MAIN

NI
SC7
150PF/50V
NPO 5%
mx_c0402
GND

NI
SC10
150PF/50V
NPO 5%
mx_c0402
GND

+1P5V_DUAL
+1P5V_DUAL

D3R1 1K 1% mx_r0402
D3R2 1K 1% mx_r0402
D3R3 1K 1% mx_r0402
D3R4 1K 1% mx_r0402
GND

14 DIMM_DQ_VREF_A

D3CB3 0.1UF/16V X7R 10% mx_c0402
D3CB4 0.1UF/16V X7R 10% mx_c0402
GND

DIMM_CA_VREF_A
DIMM_DQ_VREF_A

+VTT_DDR

D3CB1 4.7UF/6.3V X5R 10% mx_c0805
D3CB2 0.1UF/16V X7R 10% mx_c0402
GND

+1P5V_DUAL
+1P5V_DUAL

78 VDD10
75 VDD9
72 VDD8
69 VDD7
66 VDD6
65 VDD5
62 VDD4
60 VDD3
57 VDD2
54 VDD1
51 VDD0

240 VTT2
120 VTT1

113 GND27
110 GND26
107 GND25
104 GND24
101 GND23
98 GND22
95 GND21
92 GND20
89 GND19
86 GND18
83 GND17
80 GND16
47 GND15
44 GND14
41 GND13
38 GND12
35 GND11
32 GND10
29 GND9
26 GND8
23 GND7
20 GND6
17 GND5
14 GND4
11 GND3
8 GND2
5 GND1
2 GND0

67 VREFCA
1 VREFDQ

NP_NC1
NP_NC2
NP_NC3
VDDSPD

DDR3_DIMM_240P

VDD21 197
VDD20 194
VDD19 191
VDD18 189
VDD17 186
VDD16 183
VDD15 182
VDD14 179
VDD13 176
VDD12 173
VDD11 170

GND59 239
GND58 235
GND57 232
GND56 229
GND55 226
GND54 223
GND53 220
GND52 217
GND51 214
GND50 211
GND49 208
GND48 205
GND47 202
GND46 199
GND45 166
GND44 163
GND43 160
GND42 157
GND41 154
GND40 151
GND39 148
GND38 145
GND37 142
GND36 139
GND35 136
GND34 133
GND33 130
GND32 127
GND31 124
GND30 121
GND29 119
GND28 116

241
242
243
236

GND

IDIMMA0B

+3P3V

D3CB48 0.1UF/16V X7R 10% mx_c0402
GND

PEGATRON DT-MB RESTRICTED SECRET

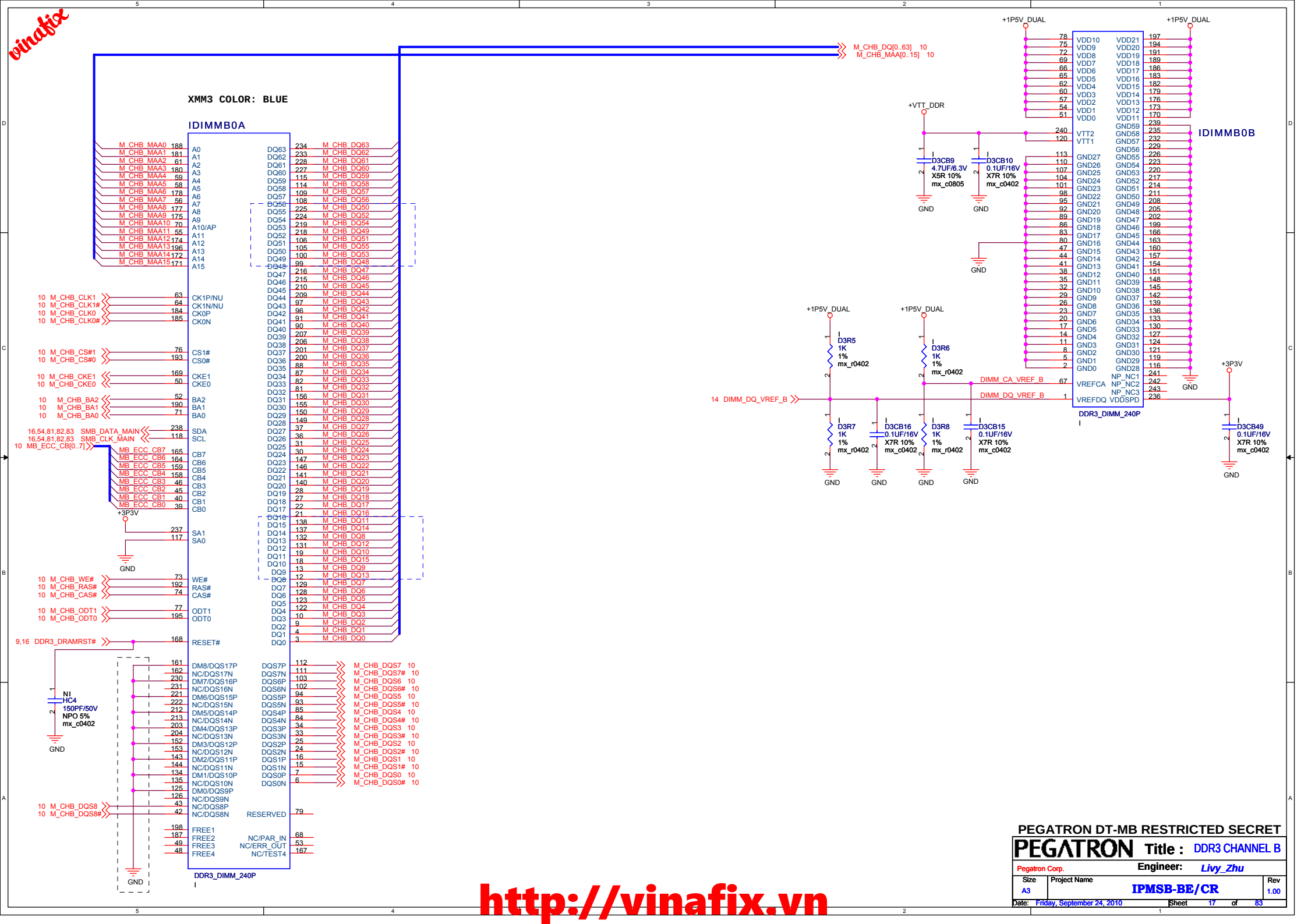
PEGATRON Title : DDR3 CHANNEL A

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 16 of 83

http://vinafix.vn



http://vinafix.vn

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 CHANNEL B

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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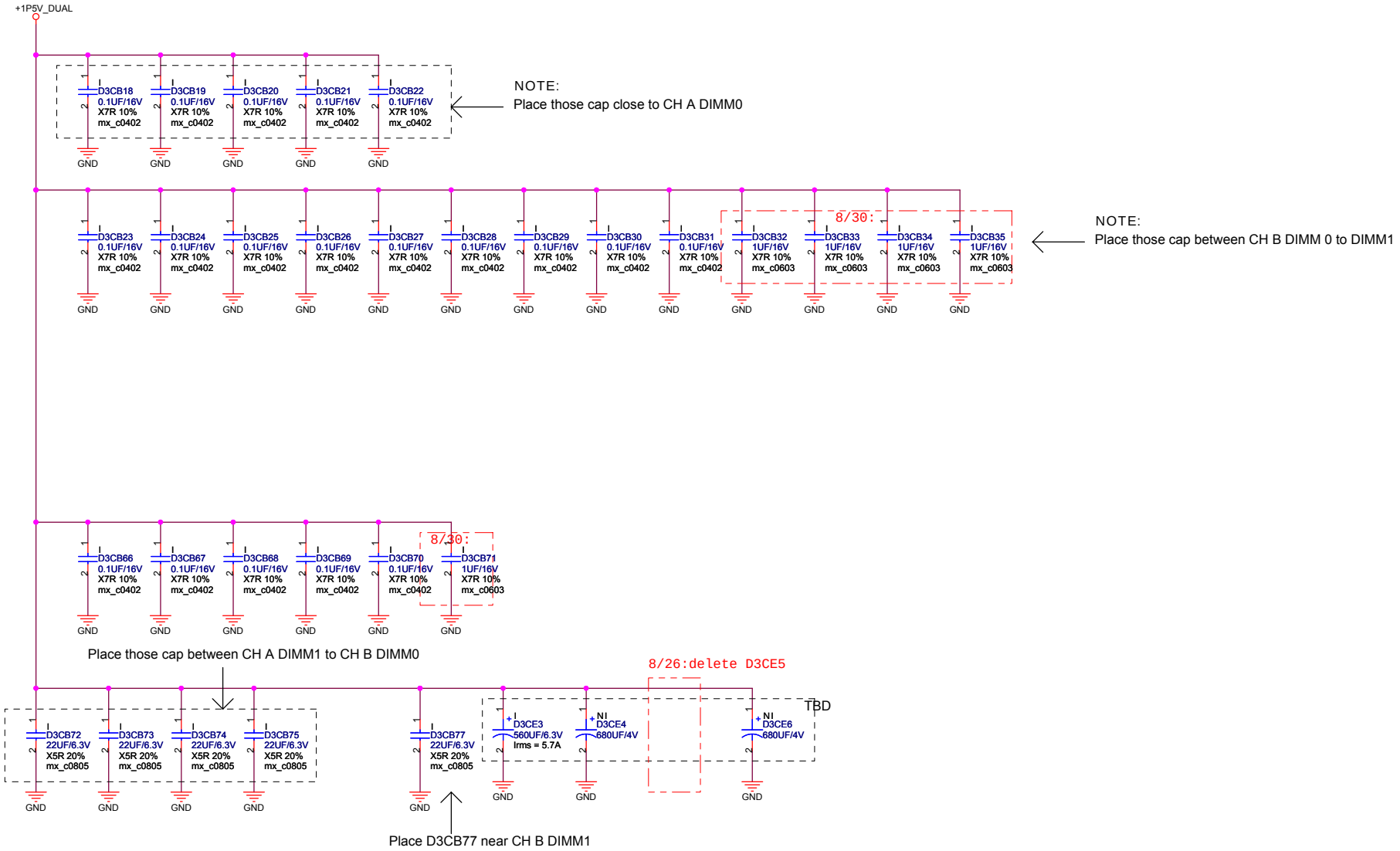
vinafix



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR3 TERMINATION A&B	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 18 of 83	

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NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

SU1A

PCI

SMBUS

RTC

SPI

Rev=1.0

COUGARPOINT

XY5
Crystal Holder

8/17:change 18pF to 12pF

0901: Change PCH P/N directly to 0200-00J80IN
(ES2 C.S 908095 B0 QMZP BGA942)

http://vinafix.vn

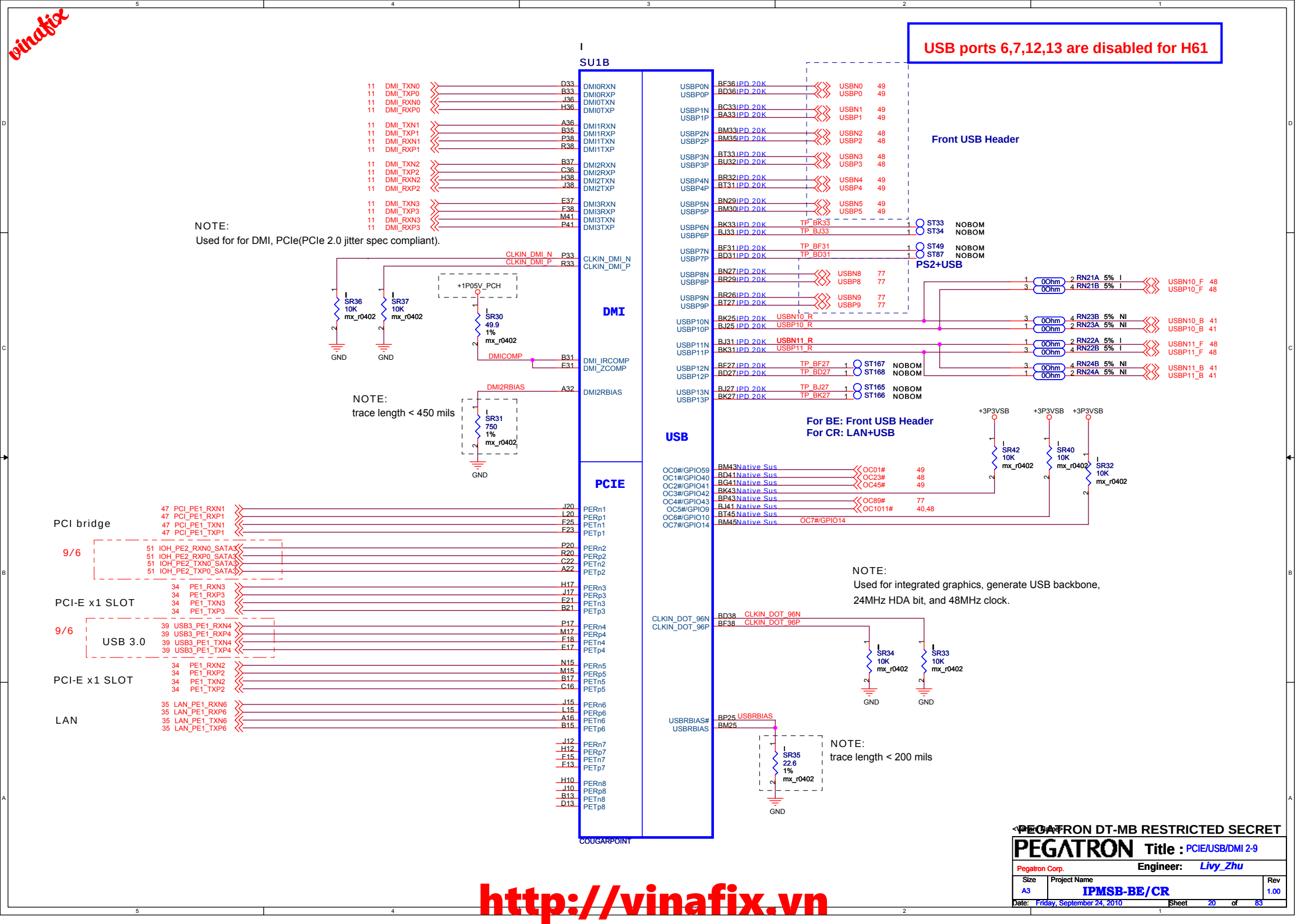
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCI/SM/SPI/RTC 1-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 19 of 83



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/USB/DMI 2-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 20 of 83

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NOTE:

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

SU1C

CLINK
FAN
GPIO
HOST
COUGARPOINT

Board ID

	GPIO21	GPIO48	GPIO39	GPIO38
BE	0	0	0	0
CR	0	0	0	1

Fab.ID

	GPIO49	GPIO16
1.00	0	0
1.01	0	1

EDS 1.0 SATA2GP/SATA3GP should not be pulled high when strap is sampled.

NOTE: trace length < 500 mils

NOTE: trace length < 450 mils

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA/HOST/FAN 3-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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SU1D

LPC
AUDIO
COUGARPOINT

NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.

NOTE: HDA_SDO
Disable ME in Manufacturing Mode
--> connect to GND.

8/28:deletet JE50

8/17:NI

NOTE:
For platform not supporting deep sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.

TBD: Both are 390Kohm in CRB 0.7

08/11

8/28 : deltet 0V

NOTE:
GPIO27 can be configured as wake input to allow wakes from Deep Sleep.

NOTE:
External PU resistor required if used for CLKREQ# functionality.

TBD

NOTE:
SUSACK# and SUSWARN# can be tied together if EC/SIO does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

8/24

NOTE:

PIN	HIGH	LOW	DESCRIPTION
GPIO8	BTM	FCIM	Clock validation
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR

8/17:delete reserved PWRBTN#

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : AUDIO/LPC/MISC 4-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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SU1E

Y18 TP6
Y17 TP7
AB18 TP8
AB17 TP9

CRT_HSYNC AR4 VGA_HSYNC_3P3V — SR245 1 2 33 mx_r0402 — VGA_HSYNC 30
CRT_VSYNC AR2 VGA_VSYNC_3P3V — SR246 1 2 33 mx_r0402 — VGA_VSYNC 30
CRT_RED AN6 VGA_RED_S — JP20 1 2 SHORT_PIN NOBOM — VGA_RED 30
CRT_GREEN AN2 VGA_GREEN_S — JP21 1 2 SHORT_PIN NOBOM — VGA_GREEN 30
CRT_BLUE AM1 VGA_BLUE_S — JP22 1 2 SHORT_PIN NOBOM — VGA_BLUE 30

30 VGA_DDCA_CLK
30 VGA_DDCA_DATA
AW3 CRT_DDC_CLK
AW1 CRT_DDC_DATA

SR247 150 1% mx_r0402 — GND
SR248 150 1% mx_r0402 — GND
SR249 150 1% mx_r0402 — GND

NOTE:
Place RGB resistors close to PCH within 250mils

DAC_IREF AT3 DACREFSET
CRT_IRTN AM6

SR131 1K 1% mx_r0402 — GND
Replace DACREFSET resistor close to PCH within 500mils

GND

NOTE:
DDP[B..D]_HPD are 3.3V tolerant.

+3P3V
SR79 1M mx_r0402

NOBOM ST72 TP_PCH_DDPBAUXP R8 — DDPB_AUXP
NOBOM ST73 TP_PCH_DDPBAUXN R9 — DDPB_AUXN
31 SDVO_CTRL_CLK — AL15 SDVO_CTRLCLK
31 SDVO_CTRL_DATA — IPD 20K AL17 SDVO_CTRLDATA
31 DDPB_HPD_DVI — T1 DDPB_HPD

CRB 0.7 do not implement.

NI SR120 1K mx_r0402 — GND

DDPB_0P R14
DDPB_0N R12
DDPB_1P M11
DDPB_1N M12
DDPB_2P H8
DDPB_2N K8
DDPB_3P L5
DDPB_3N M3
→ DVI_TMDSB_DATA0 31, DVI_TMDSB_DATA0# 31, DVI_TMDSB_DATA1 31, DVI_TMDSB_DATA1# 31, DVI_TMDSB_DATA2 31, DVI_TMDSB_DATA2# 31, DVI_TMDSB_CLK 31, DVI_TMDSB_CLK# 31

DVI

SDVO_INTP U2 IPD 50 — SDVO_INTP — ST78 NOBOM
SDVO_INTN T3 IPD 50 — SDVO_INTN — ST79 NOBOM
SDVO_STALLP W3 IPD 50
SDVO_STALLN U5 IPD 50
SDVO_TVCLKINP U8 IPD 50
SDVO_TVCLKINN U9 IPD 50

NOBOM ST84 TP_PCH_DDPCAUXP U14 — DDPC_AUXP
NOBOM ST83 TP_PCH_DDPCAUXN U12 — DDPC_AUXN
NOBOM ST86 TP_PCH_DDPC_CTRLCLK AL12 — DDPC_CTRLCLK
NOBOM ST85 TP_PCH_DDPC_CTRLDATA IPD 20K AL14 — DDPC_CTRLDATA
N2 DDPC_HPD

DDPC_0P L2 — TP_PCH_L2 — ST90 NOBOM
DDPC_0N J3 — TP_PCH_J3 — ST93 NOBOM
DDPC_1P G2 — TP_PCH_G2 — ST94 NOBOM
DDPC_1N G4 — TP_PCH_G4 — ST102 NOBOM
DDPC_2P F3 — TP_PCH_F3 — ST103 NOBOM
DDPC_2N F5 — TP_PCH_F5 — ST104 NOBOM
DDPC_3P E4 — TP_PCH_E4 — ST130 NOBOM
DDPC_3N E2 — TP_PCH_E2 — ST139 NOBOM

SR121 1K mx_r0402 — GND

NOBOM ST76 TP_PCH_DDPDAUXP N6 — DDPD_AUXP
NOBOM ST77 TP_PCH_DDPDAUXN R6 — DDPD_AUXN
NOBOM ST89 TP_PCH_DDPD_CTRLCLK AL9 — DDPD_CTRLCLK
NOBOM ST88 TP_PCH_DDPD_CTRLDATA IPD 20K AL8 — DDPD_CTRLDATA
M1 DDPD_HPD

DDPD_0P D5 — TP_PCH_D5 — ST146 NOBOM
DDPD_0N B5 — TP_PCH_B5 — ST147 NOBOM
DDPD_1P C6 — TP_PCH_C6 — ST141 NOBOM
DDPD_1N D7 — TP_PCH_D7 — ST140 NOBOM
DDPD_2P B7 — TP_PCH_B7 — ST143 NOBOM
DDPD_2N C9 — TP_PCH_C9 — ST142 NOBOM
DDPD_3P E11 — TP_PCH_E11 — ST145 NOBOM
DDPD_3N B11 — TP_PCH_B11 — ST144 NOBOM

SR122 1K mx_r0402 — GND

COUGARPOINT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VGA/DP/HDMI 5-9
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
Date: Friday, September 24, 2010 | Sheet 23 of 83

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SU1F

FDI

RSD

CLOCK

NOTE:
CLKIN_BCLK(CLKIN_GND0): Optional(BTM usage)
CLKIN_DMI2(CLKIN_GND1): Optional(BTM usage)

NOTE:
1.Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2.Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2
if more than 2 PCI clocks + PCI loopback are routed.
3.With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3

COUGARPOINT

PEGATRON DT-MB RESTRICTED SECRET

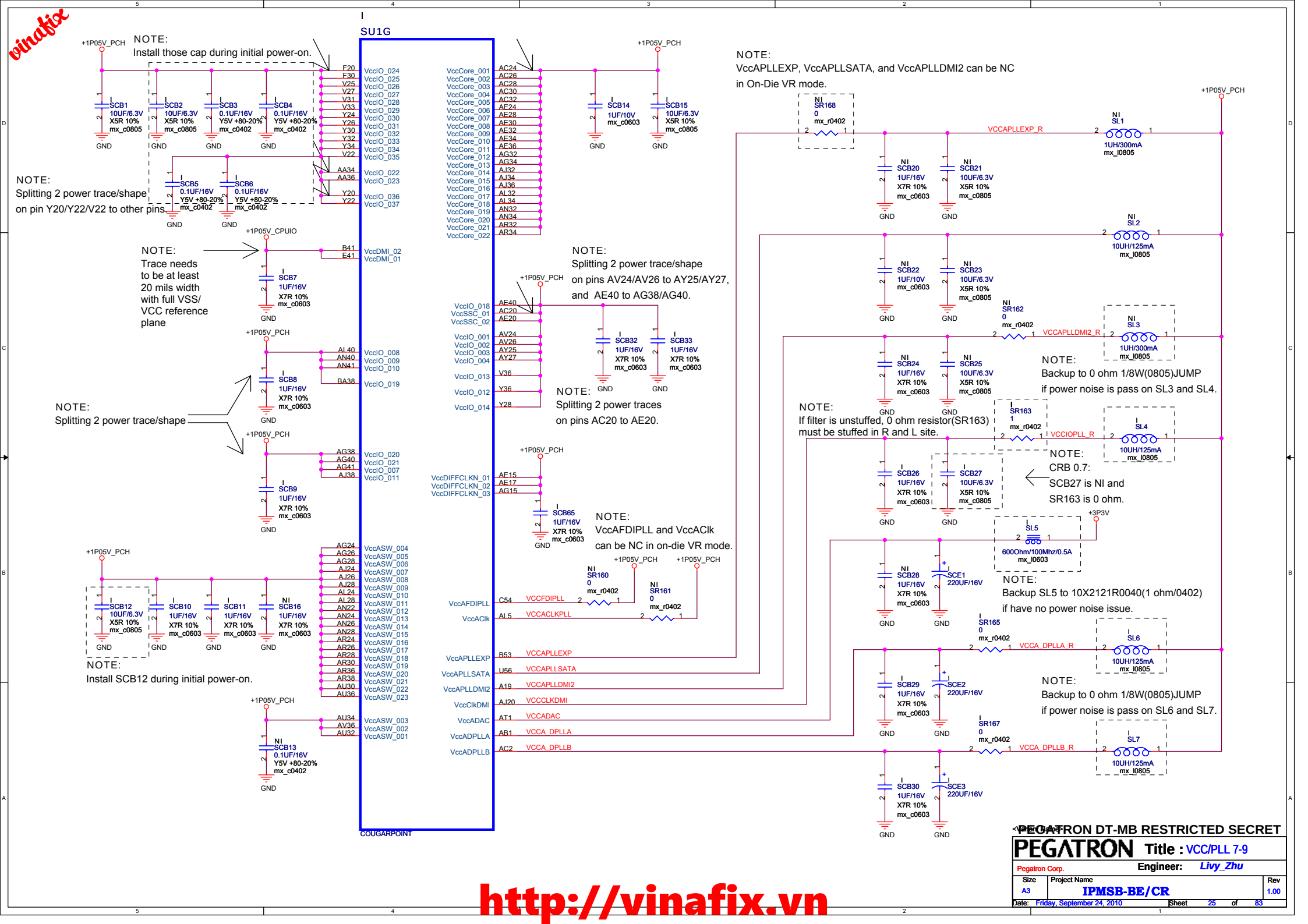
PEGATRON Title : CLK/NVRAM/FDI 6-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 24 of 83

http://vinafix.vn



http://vinafix.vn

vinafix

SU1H

NOTE:
Place SCB59 and SCB66 near pin AU20,
SCB60 near pin AL38,
SCB61 and SCB67 near BC17.

NOTE:
Splitting 2 power trace/shape on
pin AV20/AU20 and AU22.

NOTE:
Install SCB58 during initial power-on.

NOTE:
Install SCB31 during initial power-on.

NOTE:
NI or install is decided to DSW support or not.

NOTE:
Splitting 2 power trace/shape on
pin AV28, AY31/AY33, and AV30/AV32.

NOTE:
Place SCB53 near pin BT35, SCB54 near pin U31.
,and SCB69 near pin AV30/AT40.

NOTE:
Place SCB56 near PCH within 40mils.

NOTE:
Just for measurement.

CRB 0.7 is 1uF

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCCSUS 8-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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SU1I

COUGARPOINT

BC15	Vss_0125	Vss_0005	A26
BC20	Vss_0126	Vss_0006	A29
BC27	Vss_0127	Vss_0007	A42
BC31	Vss_0128	Vss_0008	A49
BC36	Vss_0129	Vss_0009	A9
BC38	Vss_0130	Vss_0010	AA20
BC47	Vss_0131	Vss_0011	AA22
BC9	Vss_0132	Vss_0012	AA24
BD25	Vss_0133	Vss_0013	AA26
BD33	Vss_0134	Vss_0014	AA28
BF12	Vss_0135	Vss_0015	AA30
BF20	Vss_0136	Vss_0016	AA38
BF25	Vss_0137	Vss_0017	AB11
BF33	Vss_0138	Vss_0018	AB15
BF41	Vss_0139	Vss_0019	AB40
BF43	Vss_0140	Vss_0020	AB41
BF46	Vss_0141	Vss_0021	AB43
BF52	Vss_0142	Vss_0022	AB47
BF6	Vss_0143	Vss_0023	AB52
BG22	Vss_0144	Vss_0024	AB57
BG25	Vss_0145	Vss_0025	AB6
BG27	Vss_0146	Vss_0026	AC22
BG31	Vss_0147	Vss_0027	AC34
BG33	Vss_0148	Vss_0028	AC36
BG36	Vss_0149	Vss_0029	AC38
BG38	Vss_0150	Vss_0030	AC4
BH52	Vss_0151	Vss_0031	AC54
BH6	Vss_0152	Vss_0032	AE14
BJ1	Vss_0153	Vss_0033	AE18
BJ15	Vss_0154	Vss_0034	AE22
BK20	Vss_0155	Vss_0035	AE26
BK41	Vss_0156	Vss_0036	AE38
BK52	Vss_0157	Vss_0037	AE4
BK6	Vss_0158	Vss_0038	AE47
BM10	Vss_0159	Vss_0039	AE8
BM12	Vss_0160	Vss_0040	AE9
BM16	Vss_0161	Vss_0041	AF52
BM22	Vss_0162	Vss_0042	AF6
BM23	Vss_0163	Vss_0043	AG11
BM26	Vss_0164	Vss_0044	AG14
BM28	Vss_0165	Vss_0045	AG20
BM32	Vss_0166	Vss_0046	AG22
BM40	Vss_0167	Vss_0047	AG30
BM42	Vss_0168	Vss_0048	AG36
BM48	Vss_0169	Vss_0049	AG43
BM5	Vss_0170	Vss_0050	AG44
BN31	Vss_0171	Vss_0051	AG46
BN47	Vss_0172	Vss_0052	AG5
BN6	Vss_0173	Vss_0053	AG50
BP3	Vss_0174	Vss_0054	AG53
BP33	Vss_0175	Vss_0055	AH52
BP35	Vss_0176	Vss_0056	AH6
BR22	Vss_0177	Vss_0057	AJ22
BR52	Vss_0178	Vss_0058	AJ30
BU19	Vss_0179	Vss_0059	AJ57
BU26	Vss_0180	Vss_0060	AK52
BU29	Vss_0181	Vss_0061	AK6
BU36	Vss_0182	Vss_0062	AL11
BU39	Vss_0183	Vss_0063	AL18
C19	Vss_0184	Vss_0064	AL20
C32	Vss_0185	Vss_0065	AL22
C39	Vss_0186	Vss_0066	AL26
C4	Vss_0187	Vss_0067	AL30
D15	Vss_0188	Vss_0068	AL36
D23	Vss_0189	Vss_0069	AL41
D3	Vss_0190	Vss_0070	AL46
D35	Vss_0191	Vss_0071	AL47
D43	Vss_0192	Vss_0072	AM52
D45	Vss_0193	Vss_0073	AM3
E19	Vss_0194	Vss_0074	AM57
E39	Vss_0195	Vss_0075	AN11
E54	Vss_0196	Vss_0076	AN12
E6	Vss_0197	Vss_0077	AN15
E9	Vss_0198	Vss_0078	AN17
F10	Vss_0199	Vss_0079	AN18
F12	Vss_0200	Vss_0080	AN20
F16	Vss_0201	Vss_0081	AN30
F22	Vss_0202	Vss_0082	AN36
F26	Vss_0203	Vss_0083	AN4
F32	Vss_0204	Vss_0084	AN43
F33	Vss_0205	Vss_0085	AN47
F35	Vss_0206	Vss_0086	AN54
F36	Vss_0207	Vss_0087	AN9
F40	Vss_0208	Vss_0088	AR20
F42	Vss_0209	Vss_0089	AR22
F46	Vss_0210	Vss_0090	AR52
F48	Vss_0211	Vss_0091	AR6
F50	Vss_0212	Vss_0092	AT15
F8	Vss_0213	Vss_0093	AT18
		Vss_0094	AT43
		Vss_0095	AT47
		Vss_0096	AT52
		Vss_0097	AT6
		Vss_0098	AT8
		Vss_0099	AU24
		Vss_0100	AU26
		Vss_0101	AU28
		Vss_0102	AU5
		Vss_0103	AV12

GND

SU1J

COUGARPOINT

L12	Vss_0231	TP1	P22
L17	Vss_0232	TP2	L31
L38	Vss_0233	TP3	L33
L41	Vss_0234	TP4	M38
L43	Vss_0235	TP5	L36
M20	Vss_0236	TP10	BM46
M22	Vss_0237	TP11	BA27
M25	Vss_0238	TP13	AE49
M27	Vss_0239	TP14	AE41
M31	Vss_0240	TP15	AE43
T52	Vss_0260	TP17	BA36
T6	Vss_0261	TP18	AY36
U11	Vss_0262	TP19	Y14
U15	Vss_0263	TP20	Y12
U17	Vss_0264		
U20	Vss_0265		
U22	Vss_0266		
U25	Vss_0267		
U27	Vss_0268		
U33	Vss_0269		
U36	Vss_0270		
U38	Vss_0271		
U41	Vss_0272	VSS_NCTF_001	A4
U47	Vss_0273	VSS_NCTF_005	BM57
U53	Vss_0274	VSS_NCTF	BP1
V20	Vss_0275		
V38	Vss_0276		
V6	Vss_0277		
W1	Vss_0278		
W55	Vss_0279		
W57	Vss_0280		
Y11	Vss_0281		
Y15	Vss_0282	L_BKLTCTL	AG12
Y38	Vss_0283	L_BKLTEN	AG18
Y40	Vss_0284	L_VDD_EN	AG17
Y43	Vss_0285		
Y46	Vss_0286		
Y47	Vss_0287	Vss_0241	M33
Y49	Vss_0288	Vss_0242	M36
Y52	Vss_0289	Vss_0243	M46
Y6	Vss_0290	Vss_0244	M52
AL43	Vss_0291	Vss_0245	M57
AL44	Vss_0292	Vss_0246	M6
R36	Vss_0293	Vss_0247	M8
P36	Vss_0294	Vss_0248	M9
R25	Vss_0295	Vss_0249	N4
P25	Vss_0296	Vss_0250	N54
		Vss_0251	R11
		Vss_0252	R15
A6	VSS_NCTF_002	Vss_0253	R17
B2	VSS_NCTF_003	Vss_0254	R22
BM1	VSS_NCTF_004	Vss_0255	R4
BP57	VSS_NCTF_007	Vss_0256	R41
BT2	VSS_NCTF_008	Vss_0257	R43
BU4	VSS_NCTF_009	Vss_0258	R46
BU52	VSS_NCTF_010	Vss_0259	R49
BU54	VSS_NCTF_011		
BU6	VSS_NCTF_012	Vss_0214	G54
D1	VSS_NCTF_013	Vss_0215	H15
F1	VSS_NCTF_014	Vss_0216	H20
		Vss_0217	H22
		Vss_0218	H25
		Vss_0219	H27
		Vss_0220	H33
		Vss_0221	H6
		Vss_0222	J1
		Vss_0223	J33
		Vss_0224	J46
		Vss_0225	J48
		Vss_0226	J5
		Vss_0227	J53
		Vss_0228	K52
		Vss_0229	K6
		Vss_0230	K9
		Vss_0119	BA49
		Vss_0120	BB1
AY22	Vss_0004	Vss_0121	BB3
C12	Vss_0003	Vss_0122	BB52
AE56	Vss_0001	Vss_0123	BB6
BR36	Vss_0002	Vss_0124	BC14
AU2	VssADAC	Vss_0104	AV18
		Vss_0105	AV22
		Vss_0106	AV34
		Vss_0107	AV38
		Vss_0108	AV47
		Vss_0109	AV6
A54	TS_VSS1	Vss_0110	AW57
A52	TS_VSS2	Vss_0111	AY38
F57	TS_VSS3	Vss_0112	AY6
D57	TS_VSS4	Vss_0113	B23
		Vss_0114	BA11
		Vss_0115	BA12
		Vss_0116	BA31
		Vss_0117	BA41
		Vss_0118	BA44

GND

08/11

TP_PCH_BKLCTL	1	ST80	NOBOM
TP_PCH_BKLTEN	1	ST81	NOBOM
TP_PCH_VDD_EN	1	ST82	NOBOM

NOTE:
BOM option depend on thermal result

SHS1
HEATSINK_2ANCHOR

CLIP1
ANCHOR_CLIP
ANGLE_45

CLIP2
ANCHOR_CLIP
ANGLE_45

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 9-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 27 of 83

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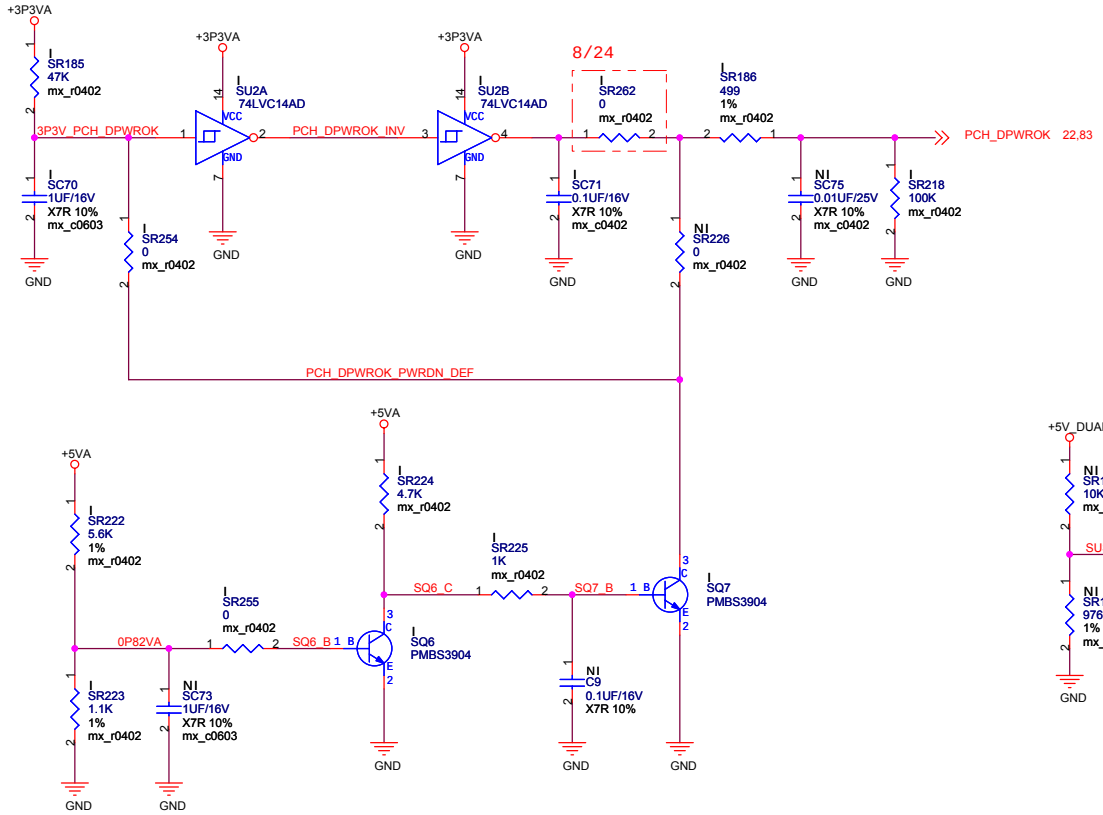
PCH_DPWROK



SUS_ACK#

NOTE:
Check voltage level of SUS_ACK# of PCH and decide resistor value of SR199.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH_DPWROK & SUS_ACK#	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 28 of 83	

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title :

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 29 of 83

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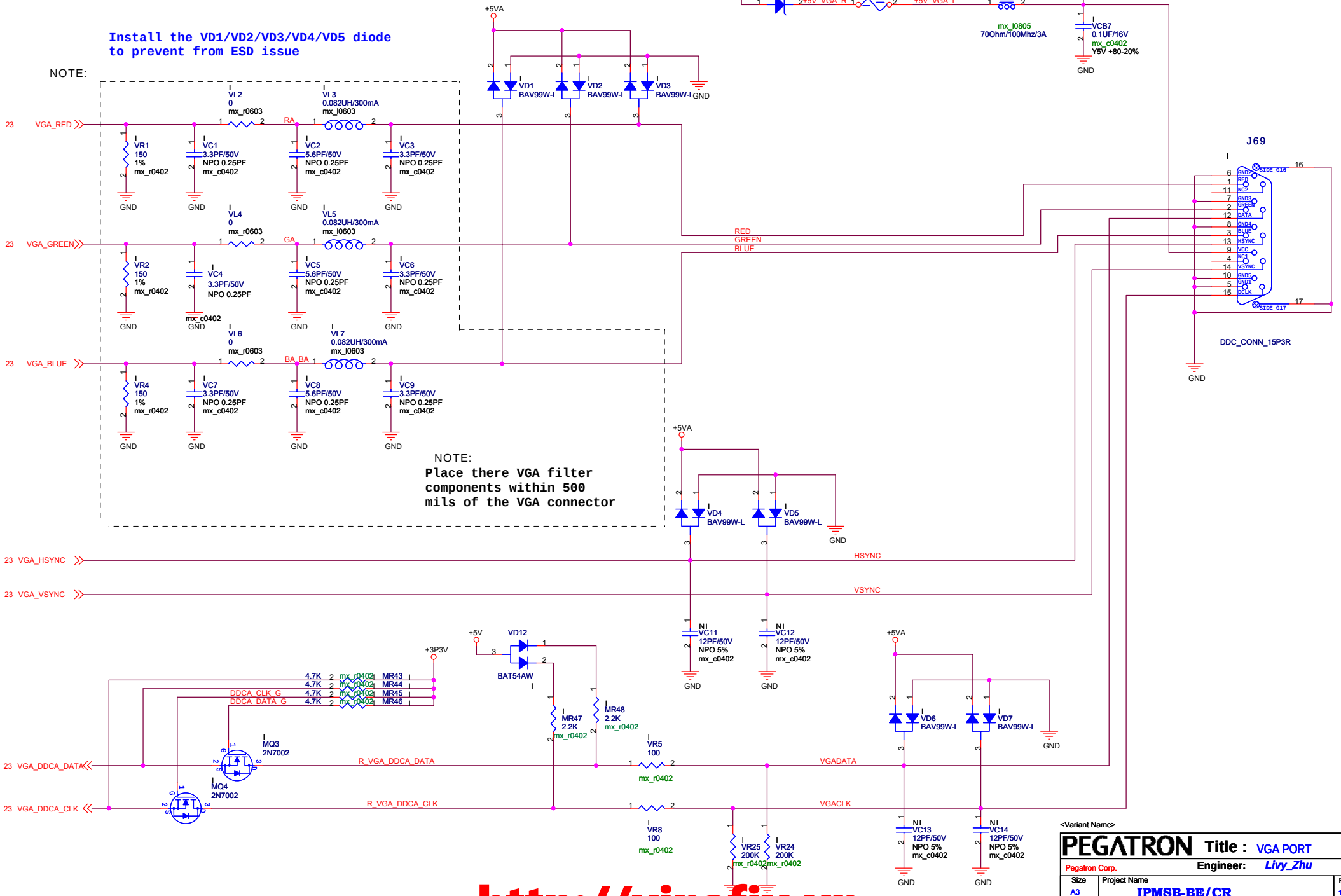
Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:



<Variant Name>

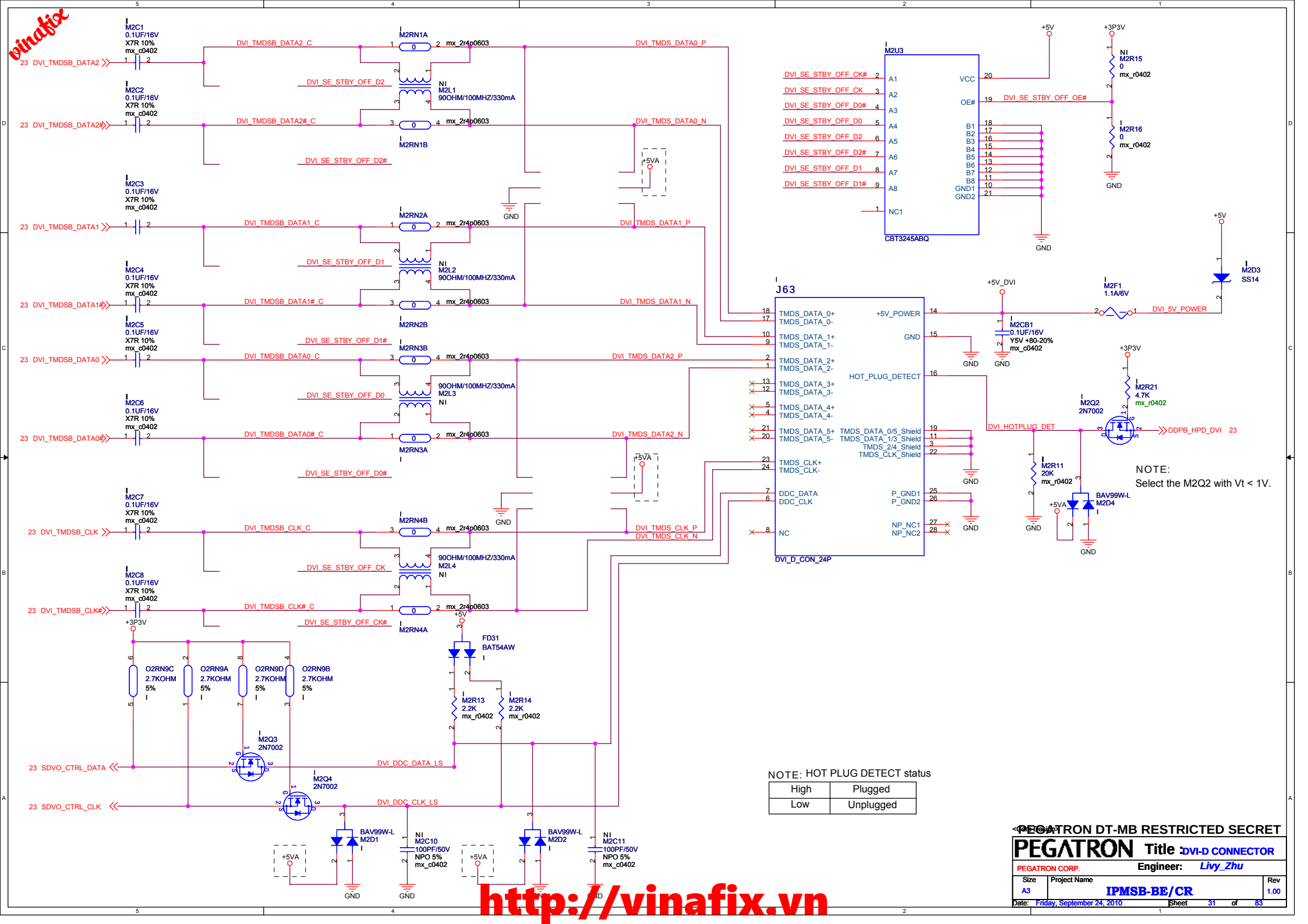
PEGATRON Title : VGA PORT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Wednesday, October 13, 2010 Sheet 30 of 83

http://vinafix.vn



http://vinafix.vn

vinafix

PCI EXPRESS X16 Graphics Card Slot

BLUE

IJ41

PCI_EXPRESS_X16

TOP SIDE VIEW

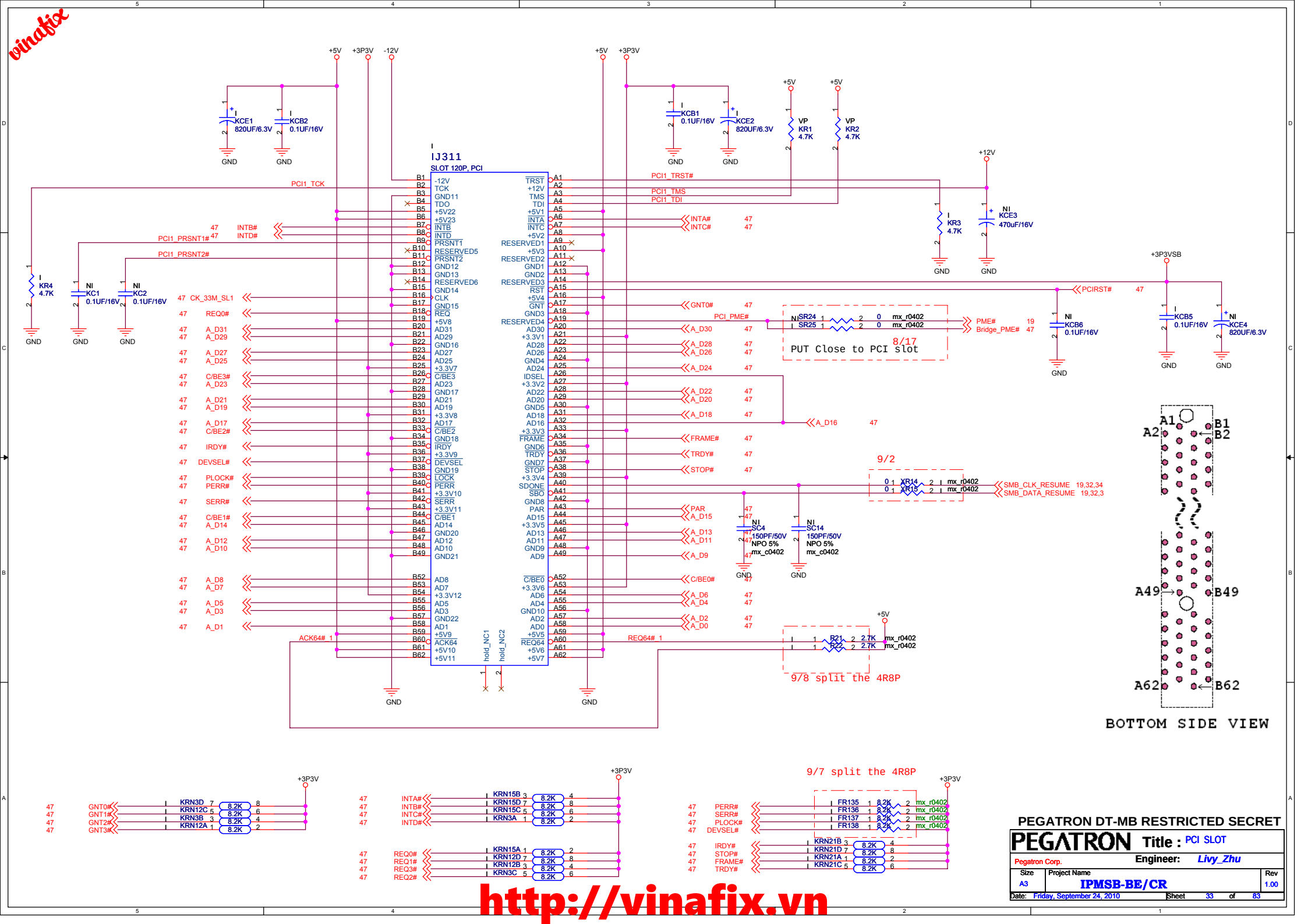
BOTTOM SIDE VIEW

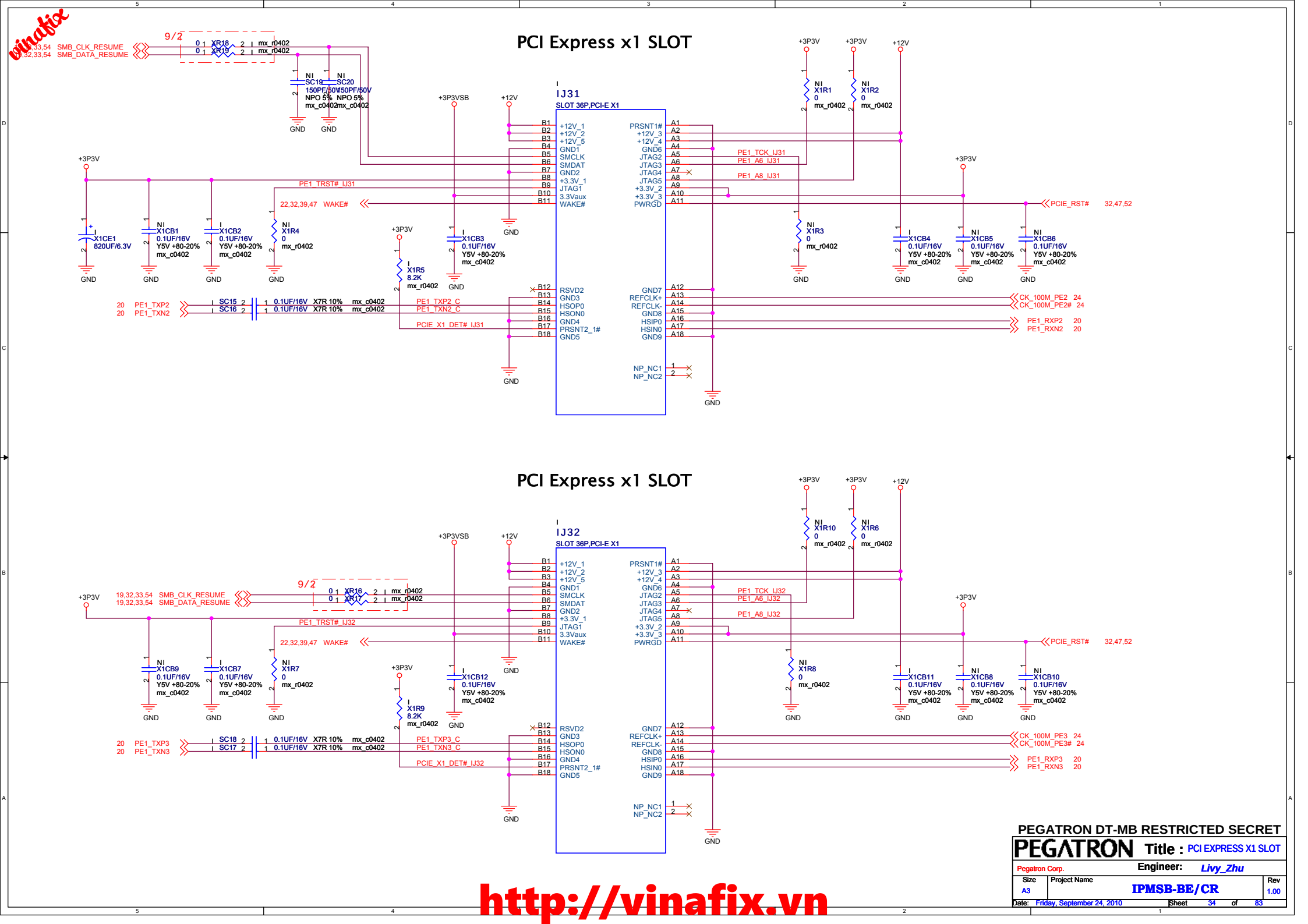
PEGATRON DT-MB RESTRICTED SECRET

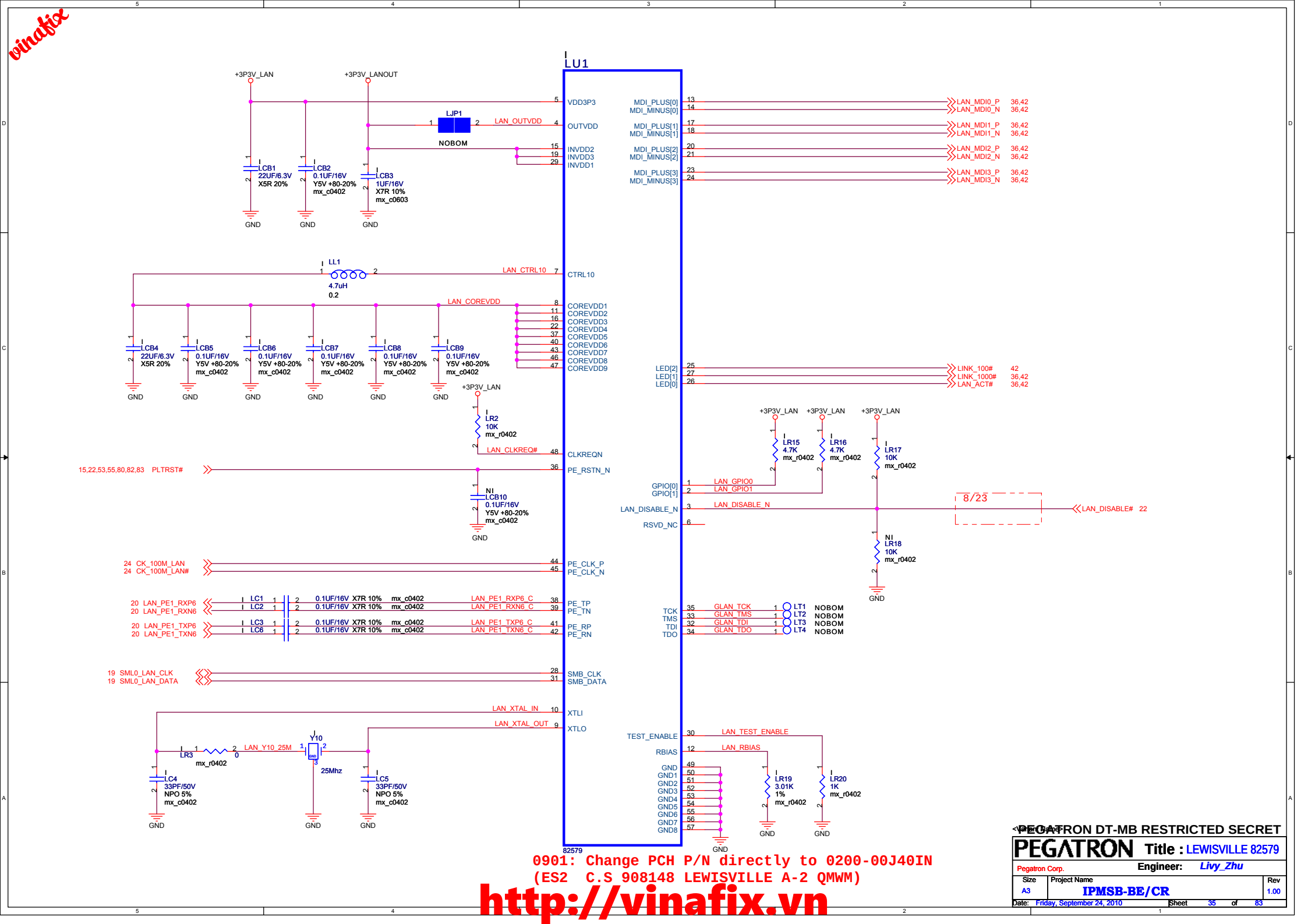
PEGATRON	Title : PCI EXPRESS X16 SLOT	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 32 of 83	

8/23 : change P/N to 12X313164U0N

http://vinafix.vn


IJ311
SLOT 120P, PCI
PUT Close to PCI slot
8/17
9/2
9/8 split the 4R8P
9/7 split the 4R8P
BOTTOM SIDE VIEW
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCI SLOT
Pegatron Corp.
Engineer: Livy_Zhu
Size A3
Project Name IPMSB-BE/CR
Rev 1.00
Date: Friday, September 24, 2010
Sheet 33 of 83
http://vinafix.vn


PCI Express x1 SLOT
IJ31
SLOT 36P,PCI-E X1
PCI Express x1 SLOT
IJ32
SLOT 36P,PCI-E X1
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCI EXPRESS X1 SLOT
Pegatron Corp.
Engineer: Livy_Zhu
Size A3
Project Name IPMSB-BE/CR
Rev 1.00
Date: Friday, September 24, 2010
Sheet 34 of 83
http://vinafix.vn



0901: Change PCH P/N directly to 0200-00J40IN
(ES2 C.S 908148 LEWISVILLE A-2 QMWM)

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<Variant Name>
PEGATRON DT-MB RESTRICTED SECRET

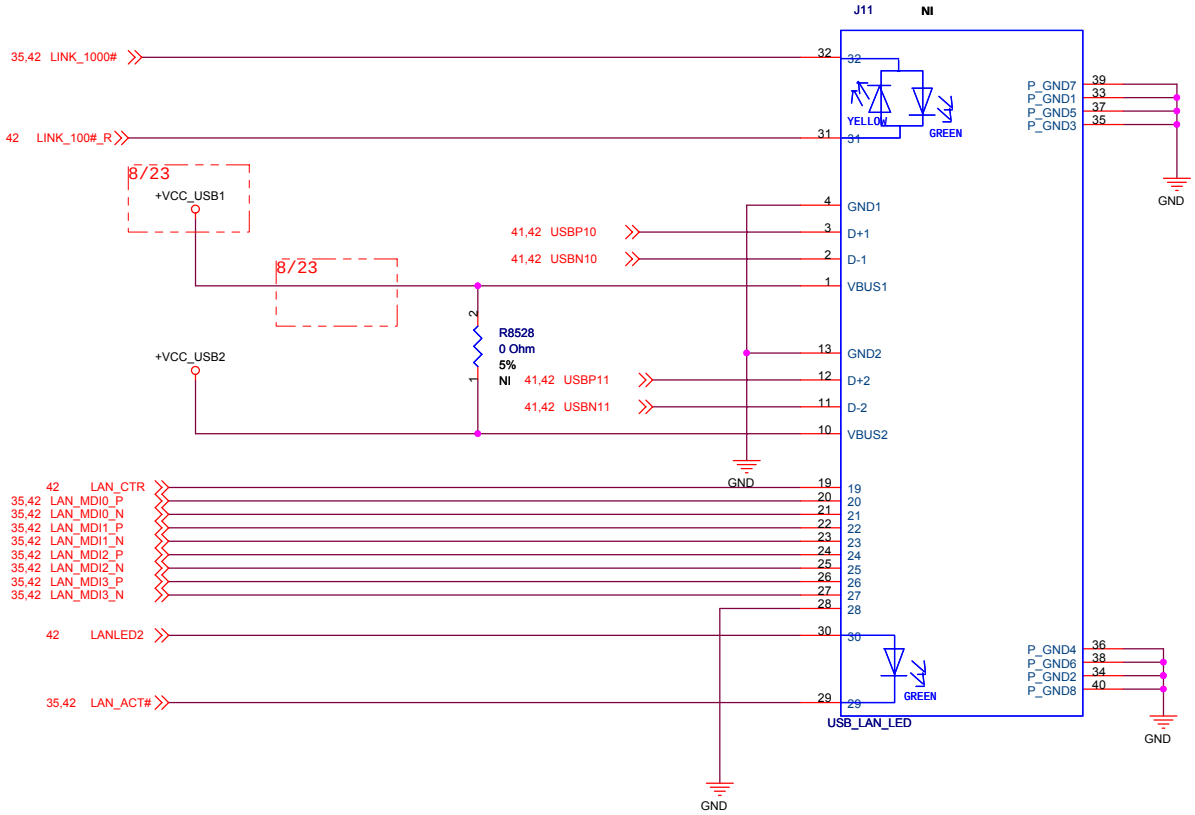
PEGATRON Title : LEWISVILLE 82579

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 35 of 83

vinafix



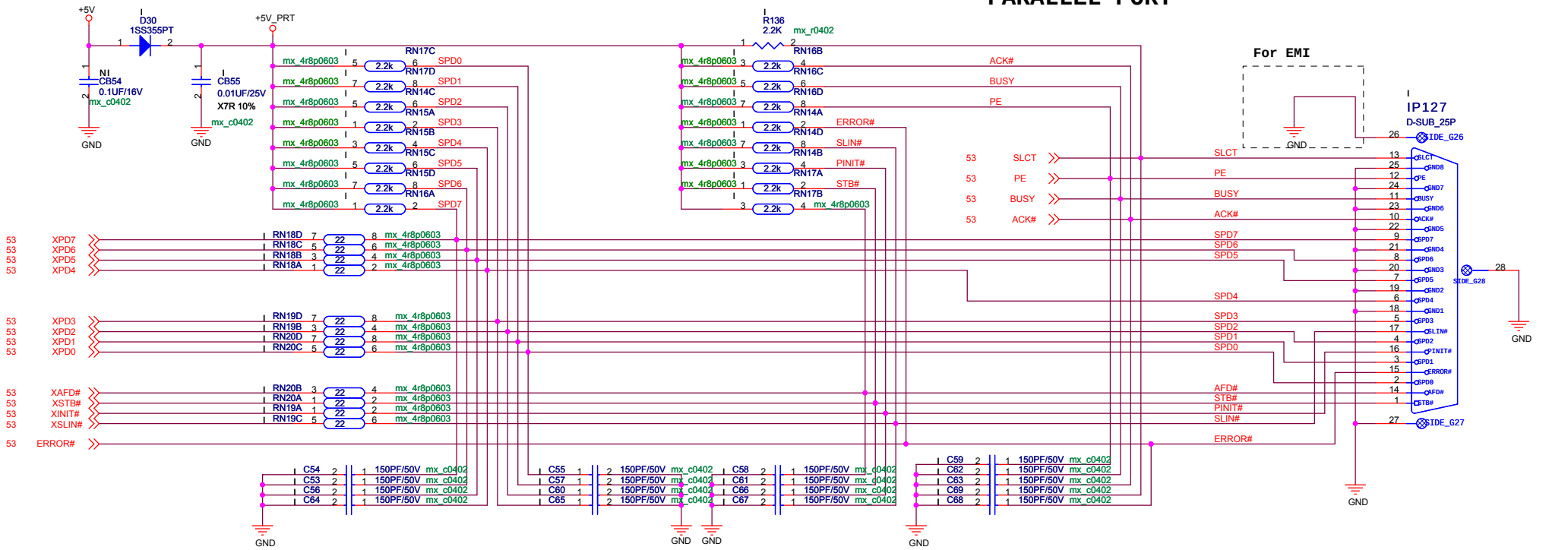
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : RJ45+USB2.0	
PEGATRON CORP.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 36 of 83	

http://vinafix.vn

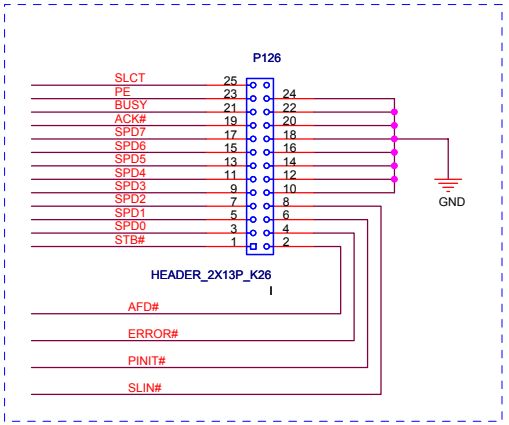
vinafix

PARALLEL PORT



08/13: NI LPT header From Fab.B

8/18:
change LPT header from 12X60202DB10 to 12X60202DIW0



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PRINT PORT

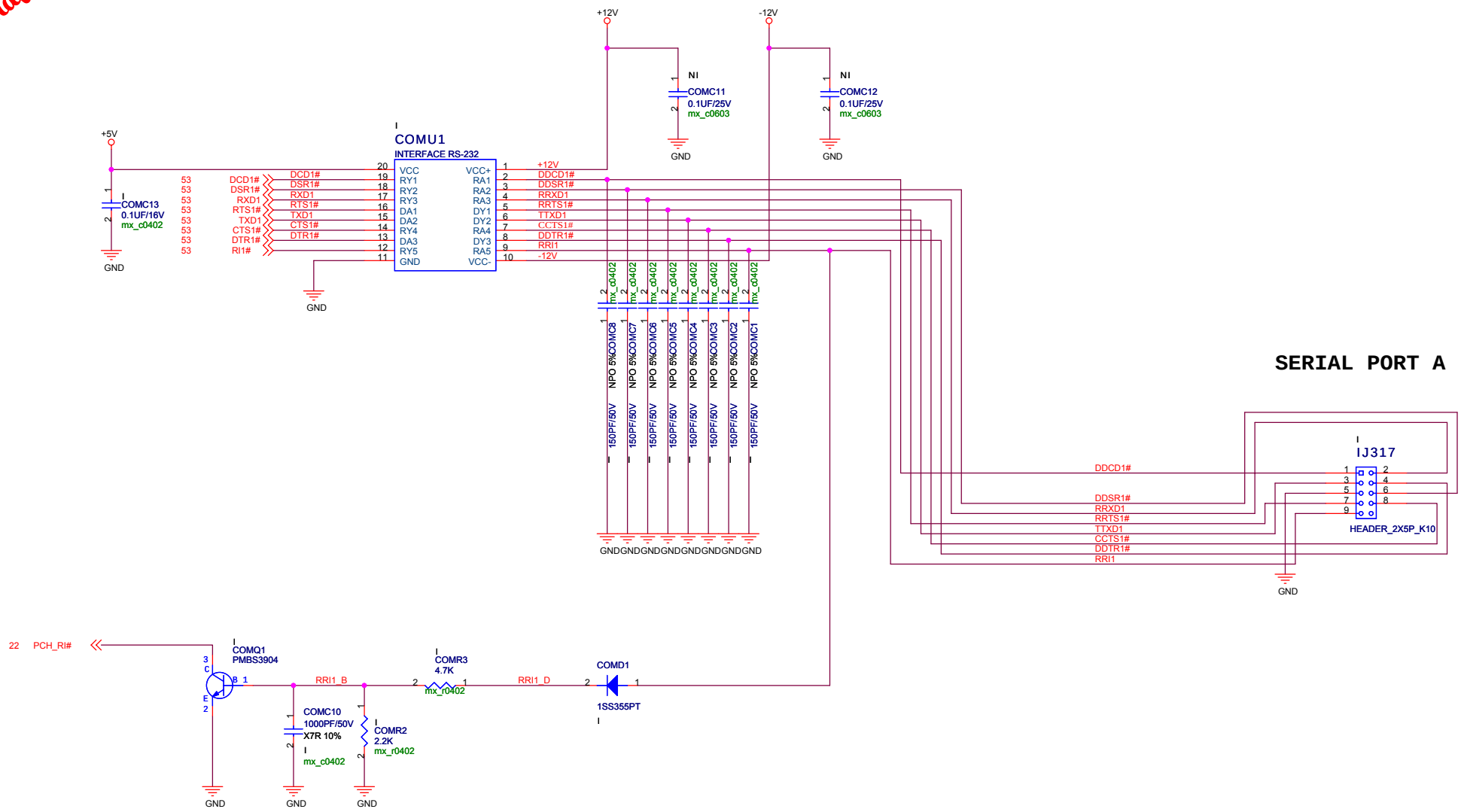
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 37 of 83

http://vinafix.vn

vinafix



PEGATRON DT-MB RESTRICTED SECRET

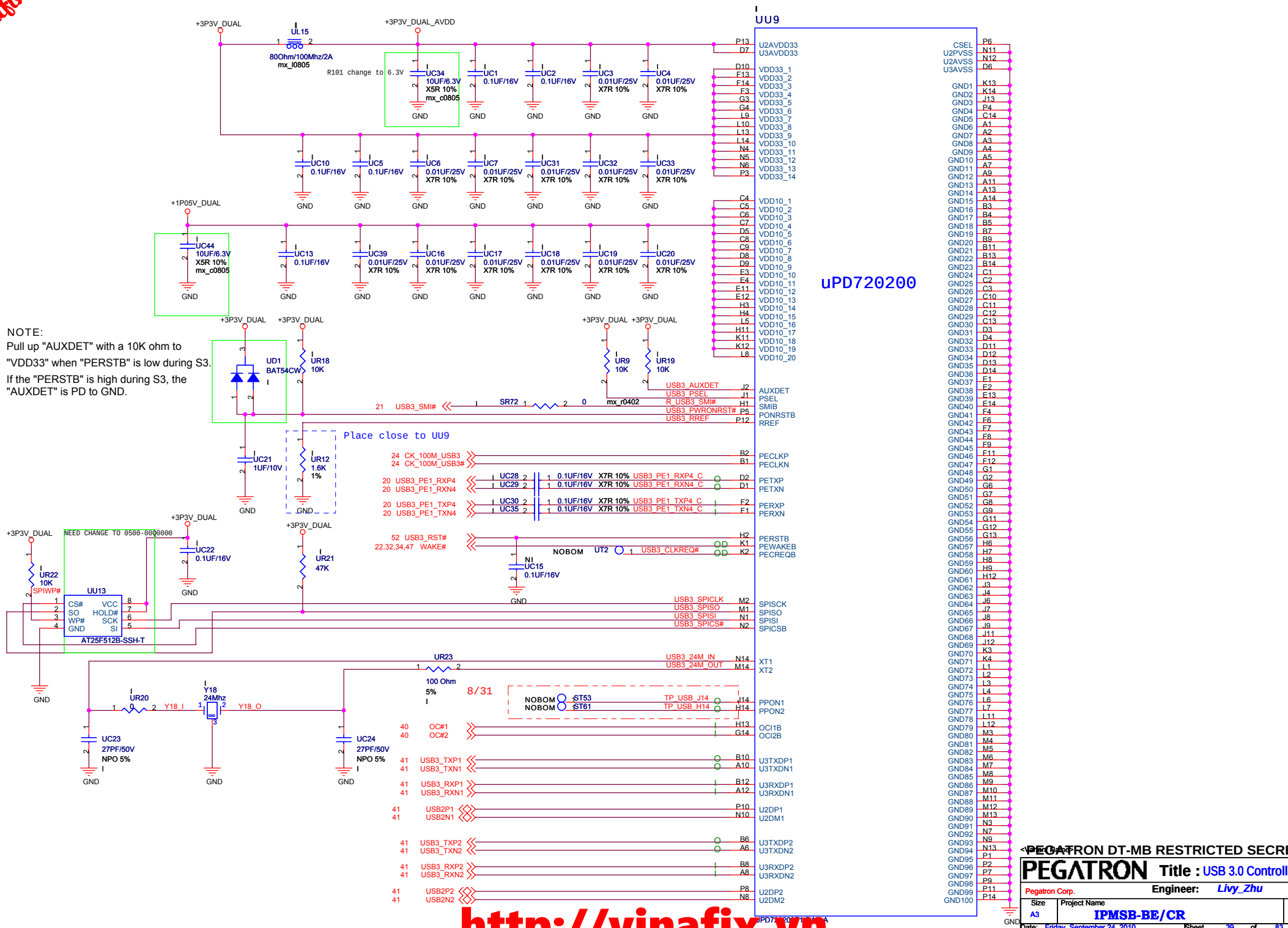
PEGATRON Title : SERIAL PORT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

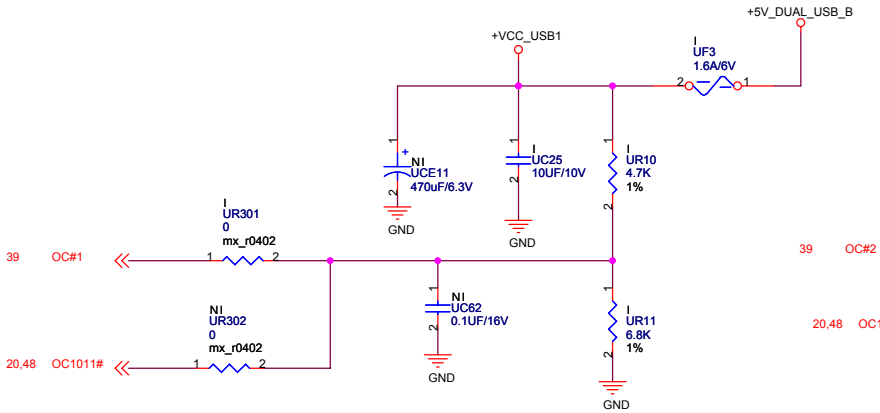
Date: Friday, September 24, 2010 Sheet 38 of 83

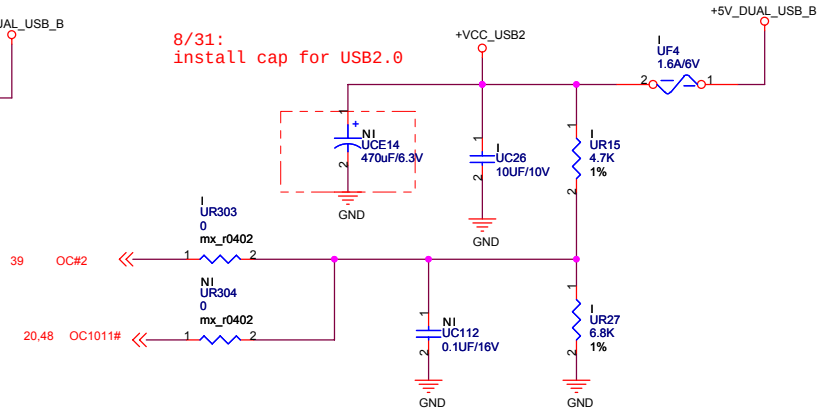
http://vinafix.vn

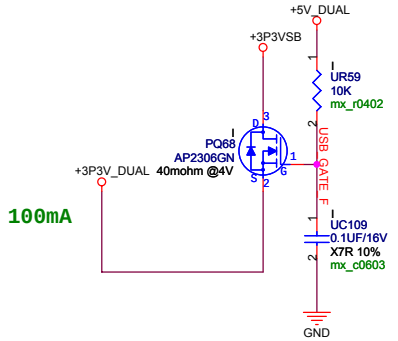


http://vinafix.vn

vinafix







PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB 3.0 power

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 40 of 83

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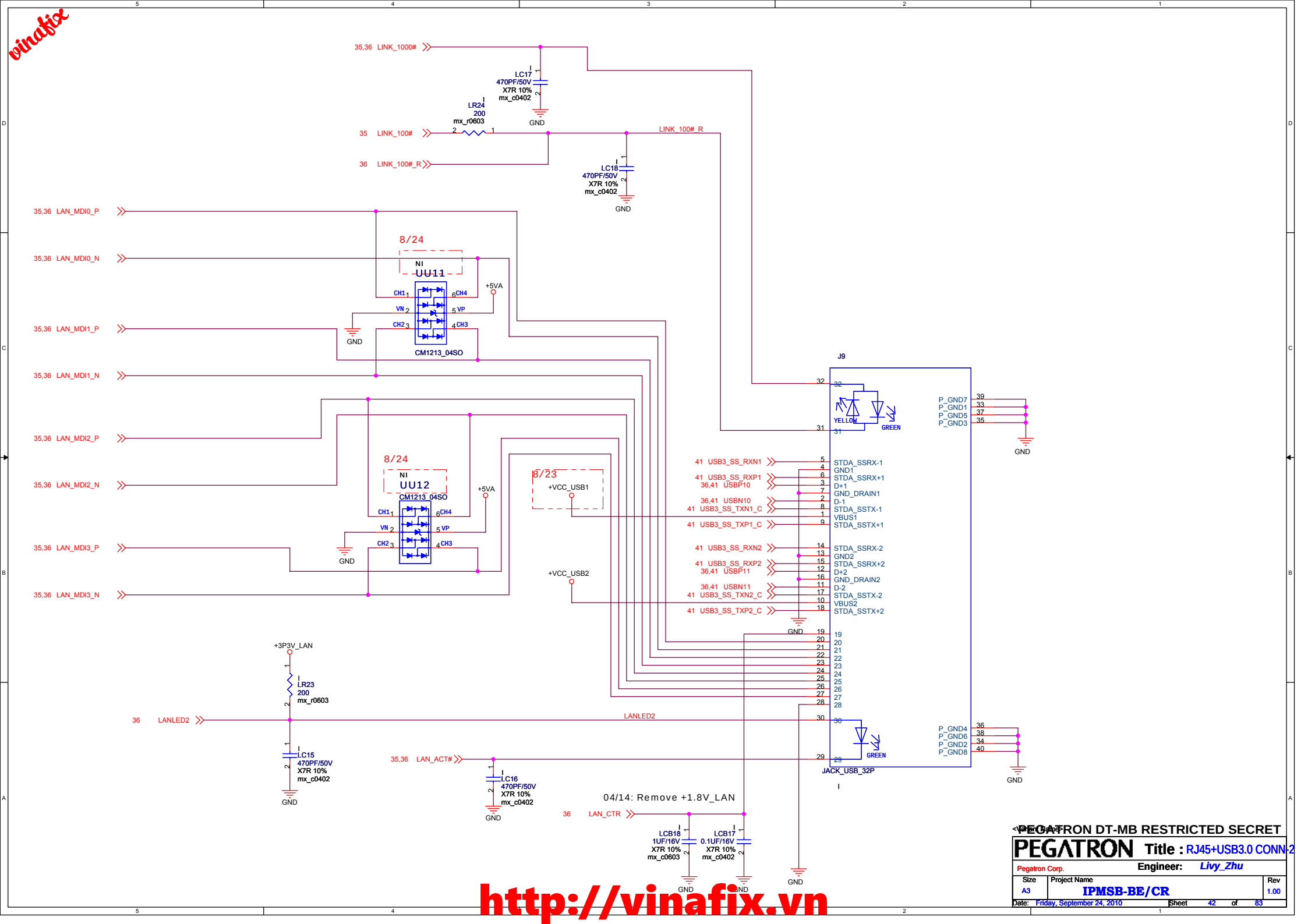
NOTE:
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

URN56A / URN56B: 0 Ohm
UL21: 90OHM/100MHZ/330mA
UC42, UC40: 0.1UF/16V X7R 10%
8/17: install ESD protection
UU18: IP4284CZ10-TB (TMDS_CH1-, TMDS_CH1+, GND1, TMDS_CH2-, TMDS_CH2+, NC4, NC3, GND2, NC2, NC1)
URN61A / URN61B: 0 Ohm
UL6: 90OHM/100MHZ/330mA
RN25A 5% 0Ohm, RN25B 5% 0Ohm
URN62B / URN62A: 0 Ohm
UL22: 90OHM/100MHZ/330mA
SWAP
+5VA
RN26A 5% 0Ohm, RN26B 5% 0Ohm
URN60B / URN60A: 0 Ohm
UL18: 90OHM/100MHZ/330mA
URN15A / URN15B: 0 Ohm
UL19: 90OHM/100MHZ/330mA
UC38, UC41: 0.1UF/16V X7R 10%
8/17: install ESD protection
UU19: IP4284CZ10-TB (TMDS_CH1-, TMDS_CH1+, GND1, TMDS_CH2-, TMDS_CH2+, NC4, NC3, GND2, NC2, NC1)
URN59A / URN59B: 0 Ohm
UL20: 90OHM/100MHZ/330mA

http://vinafix.vn

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RJ45+USB 3.0 CONN-1
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
Date: Friday, September 24, 2010 | Sheet 41 of 83



PEGATRON DT-MB RESTRICTED SECRET

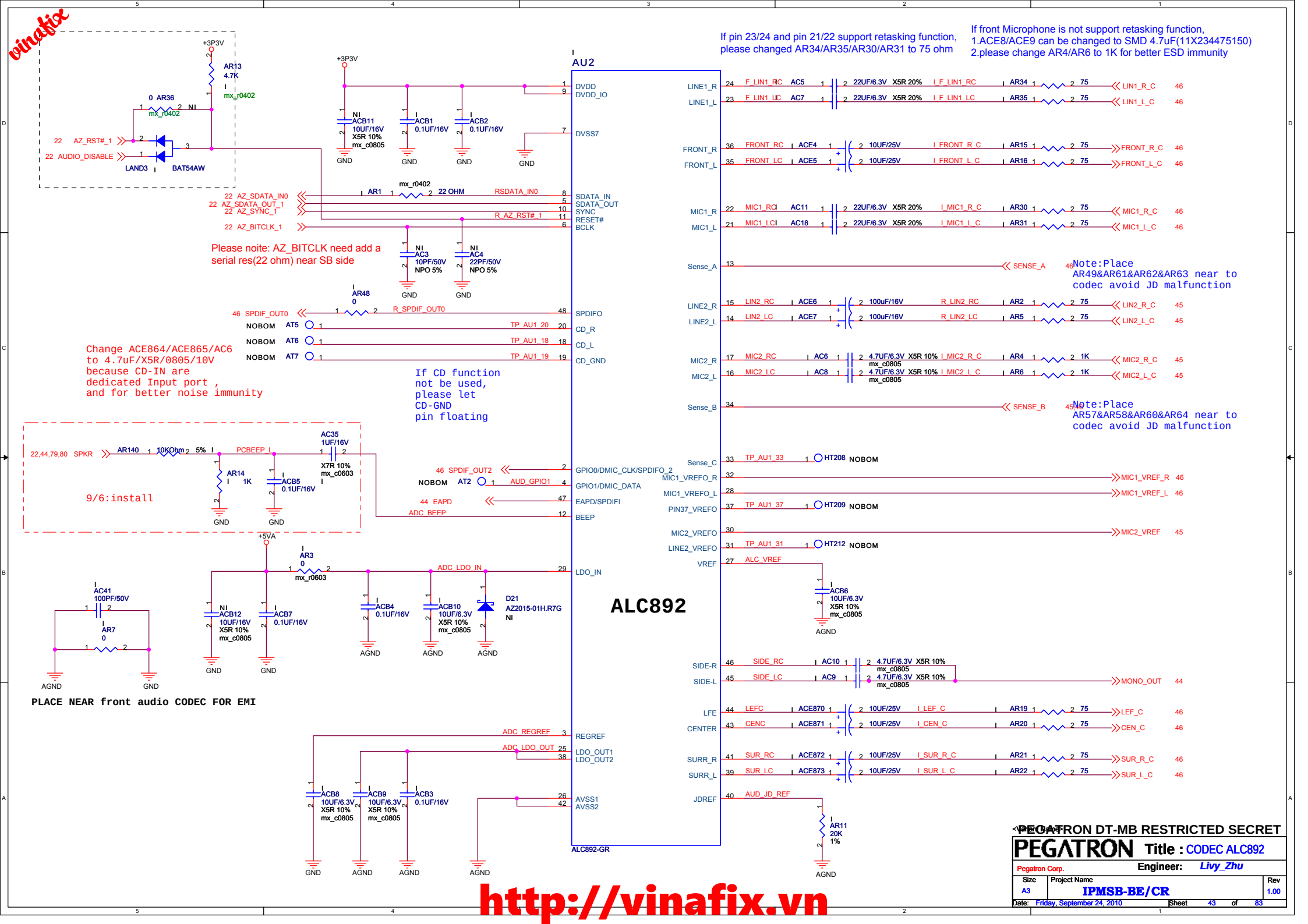
PEGATRON Title : RJ45+USB3.0 CONN-2

Pegatron Corp. Engineer: Livy_Zhu

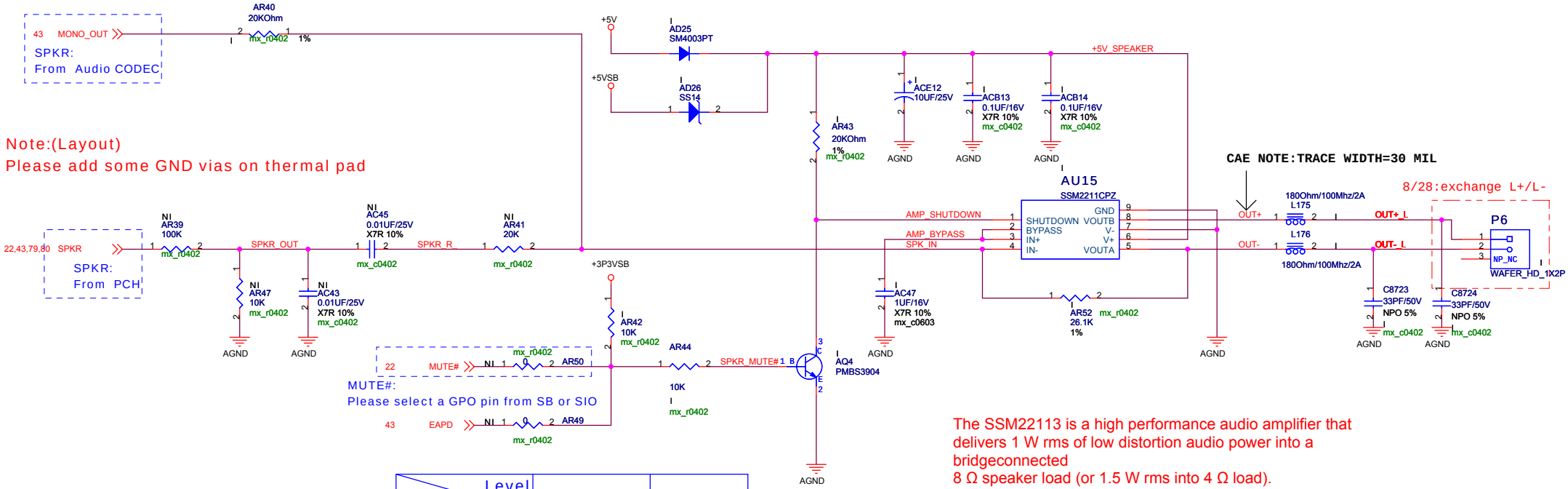
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 42 of 83

http://vinafix.vn


If pin 23/24 and pin 21/22 support retasking function, please changed AR34/AR35/AR30/AR31 to 75 ohm
If front Microphone is not support retasking function,
1.ACE8/ACE9 can be changed to SMD 4.7uF(11X234475150)
2.please change AR4/AR6 to 1K for better ESD immunity
AU2
ALC892
ALC892-GR
Please noite: AZ_BITCLK need add a serial res(22 ohm) near SB side
Change ACE864/ACE865/AC6 to 4.7uF/X5R/0805/10V because CD-IN are dedicated Input port , and for better noise immunity
If CD function not be used, please let CD-GND pin floating
Note:Place AR49&AR61&AR62&AR63 near to codec avoid JD malfunction
Note:Place AR57&AR58&AR60&AR64 near to codec avoid JD malfunction
9/6:install
PLACE NEAR front audio CODEC FOR EMI
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : CODEC ALC892
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 43 of 83
http://vinafix.vn

INTERNAL SPEAKER HEADER



Net \ Level	H Level	L Level
Mute# Default	Non-Mute	Mute
AZ_GPIO0#	Non-Mute	Mute

The SSM22113 is a high performance audio amplifier that delivers 1 W rms of low distortion audio power into a bridgeconnected
8 Ω speaker load (or 1.5 W rms into 4 Ω load).

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTERNAL SPEAKER

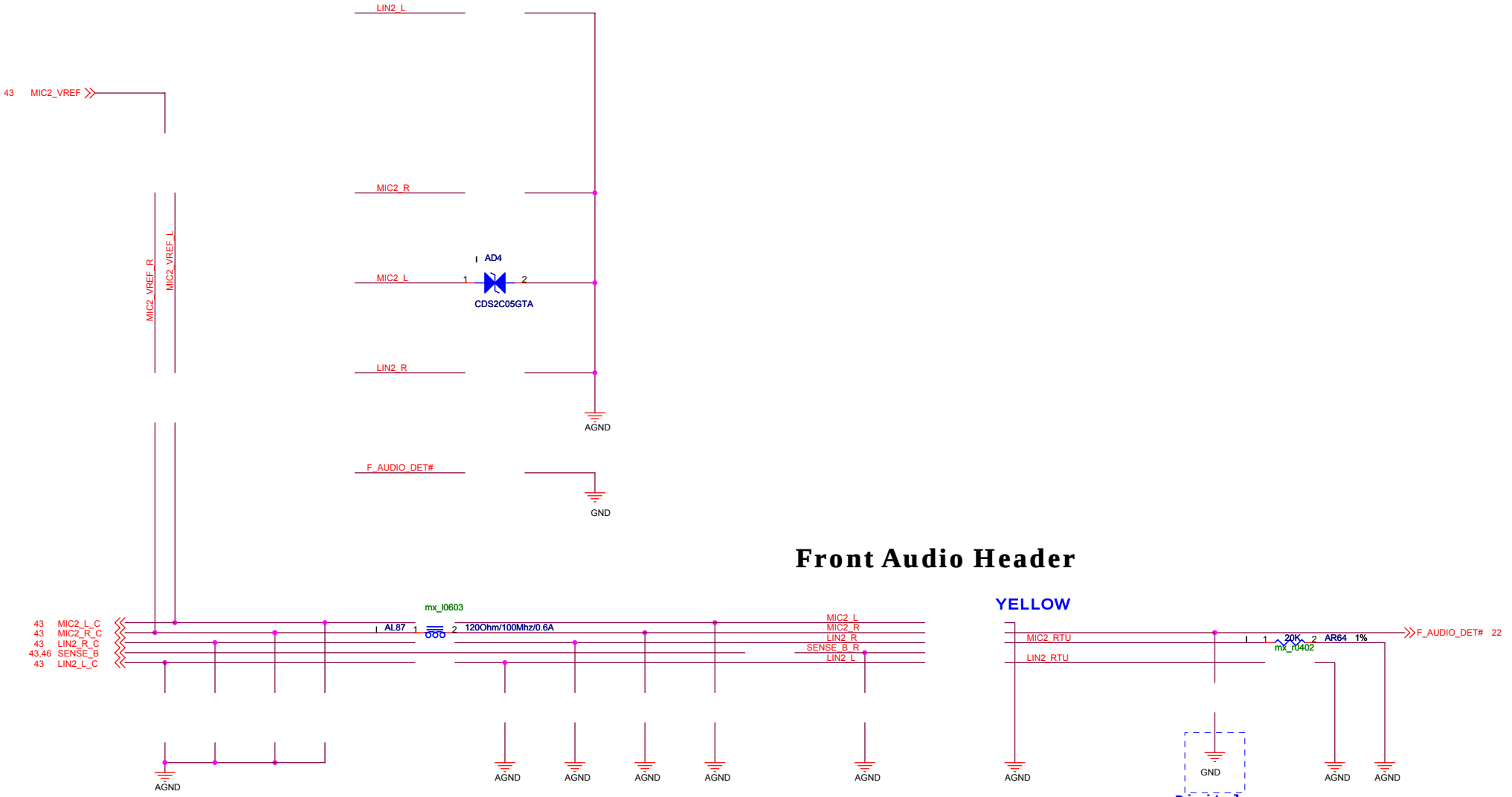
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 44 of 83

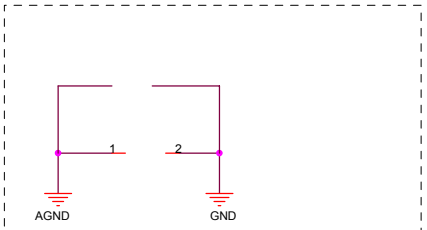
http://vinafix.vn

vinafix



Front Audio Header

If front HP-OUT is not support retasking,
these Vreference circuit can be removed.



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : FRONT AUDIO HEADER	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 45 of 83	

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Azalia Rear Audio Connector

AL87/AL89/AL91/AL93/AL95/AL97;Please use 09X131216000 instead of 0 ohm if you found have EMI issue

Note:
AR61& AR67& AR73 placed near to codec for avoid JD malfunction

Note:
AR82 & AR74 placed near to codec for avoid JD malfunction

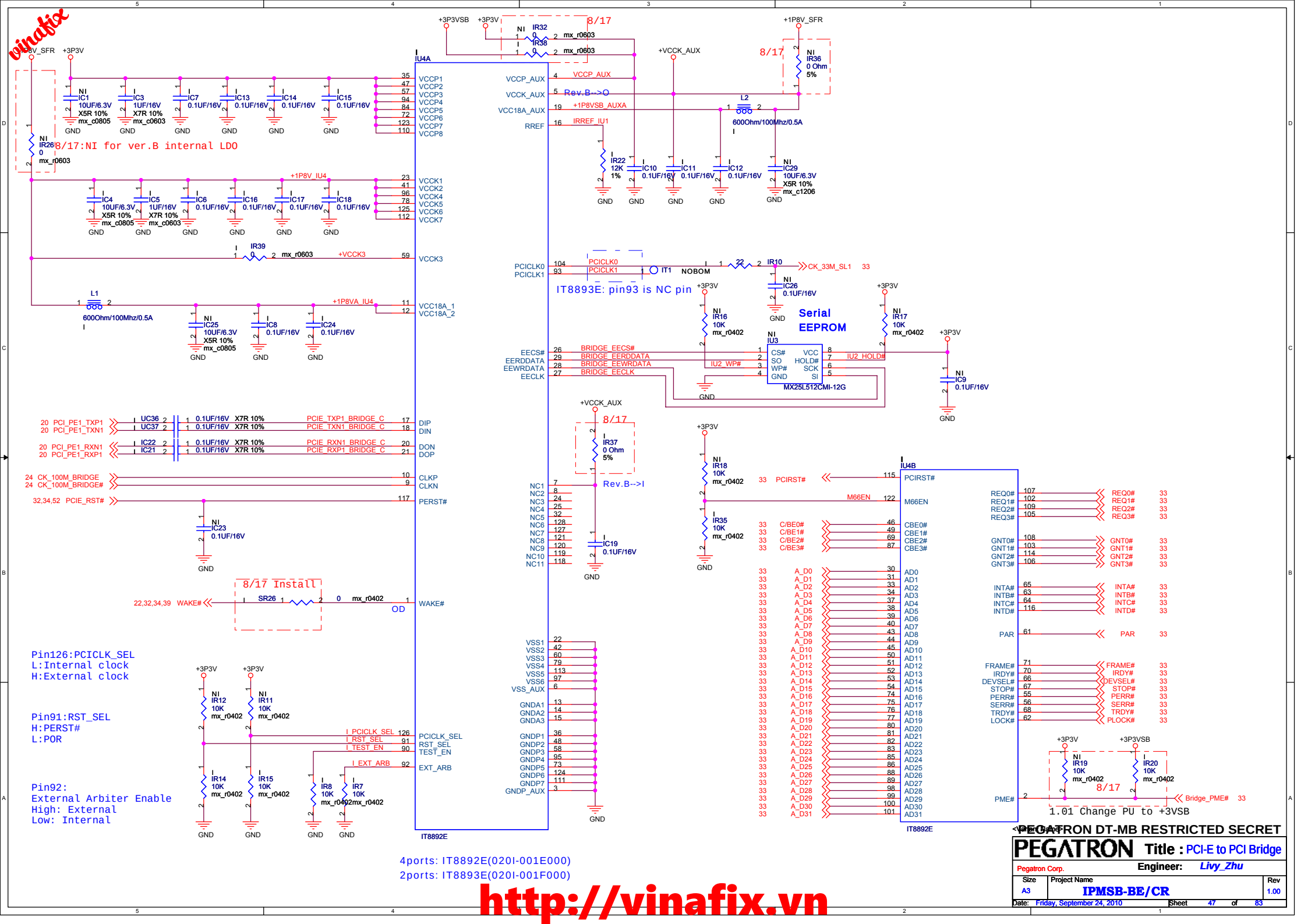
Note(CD_IN_JD):
If LINE1(PIN23/24) are used to be rear Line-in port , please change this connection to "SENSE_A"(serial resistor : 10K)

If for HP CPC 6+3 configuration just keep "CD_IN_JD"

AL88/AL90/AL92/AL94/AL96/AL98;Please use 09X131216000 instead of 0 ohm if you found have EMI issue

SPDIF OUT2 CONNECTOR

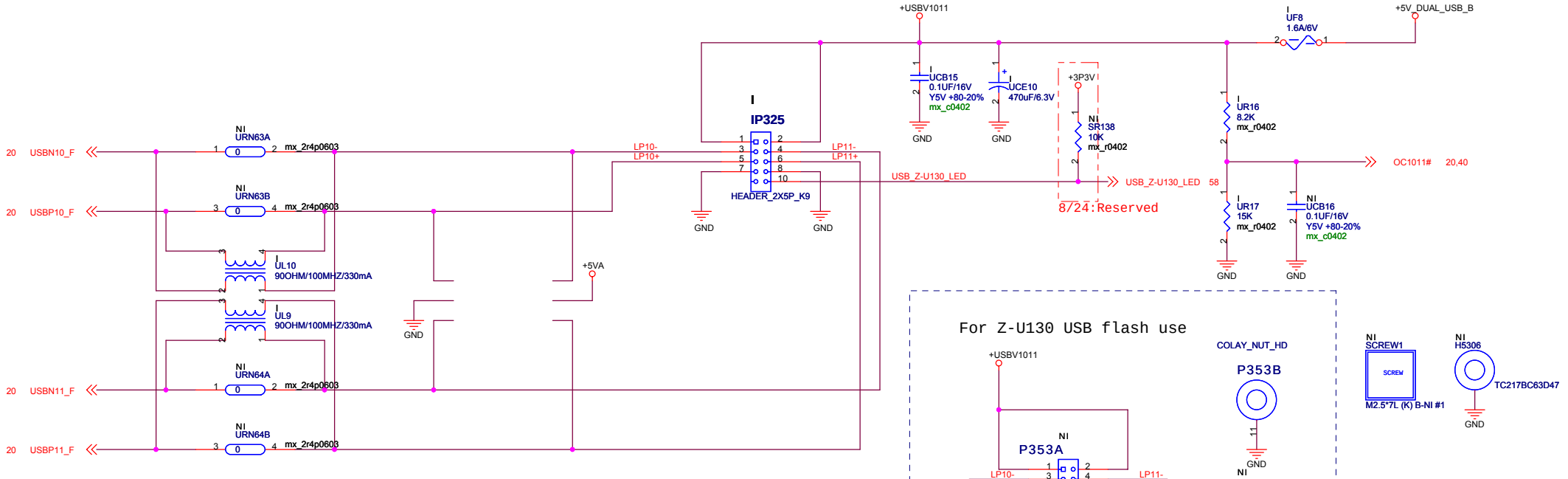
http://vinafix.vn



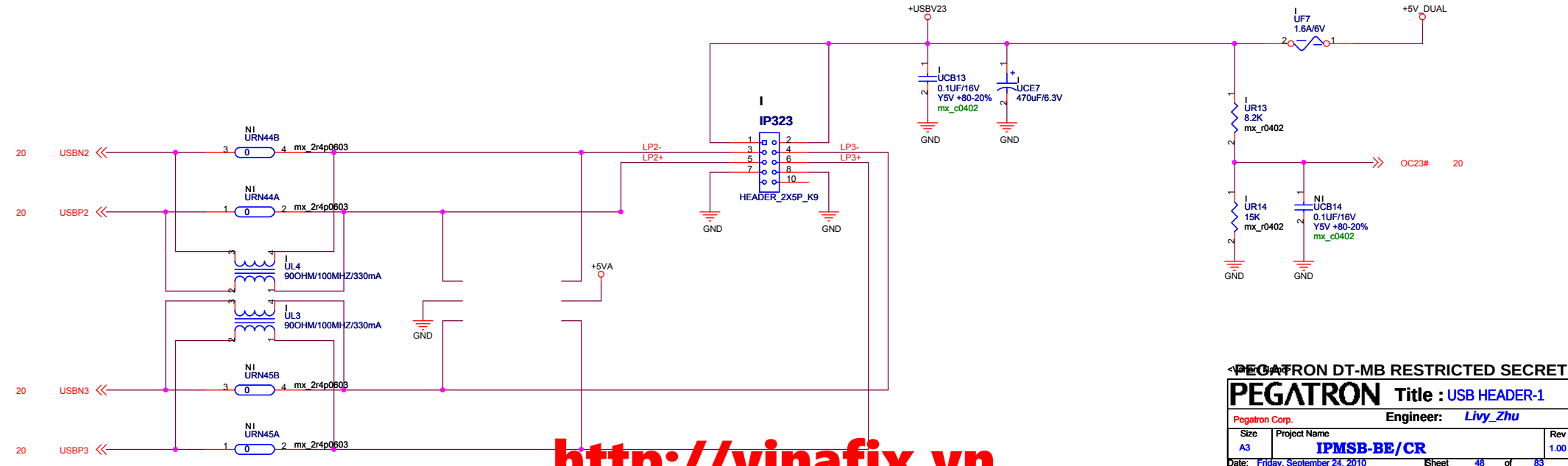
http://vinafix.vn

vinafix

FRONT USB HEADER Port 7 & 8



FRONT USB HEADER Port 5 & 6



http://vinafix.vn

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB HEADER-1

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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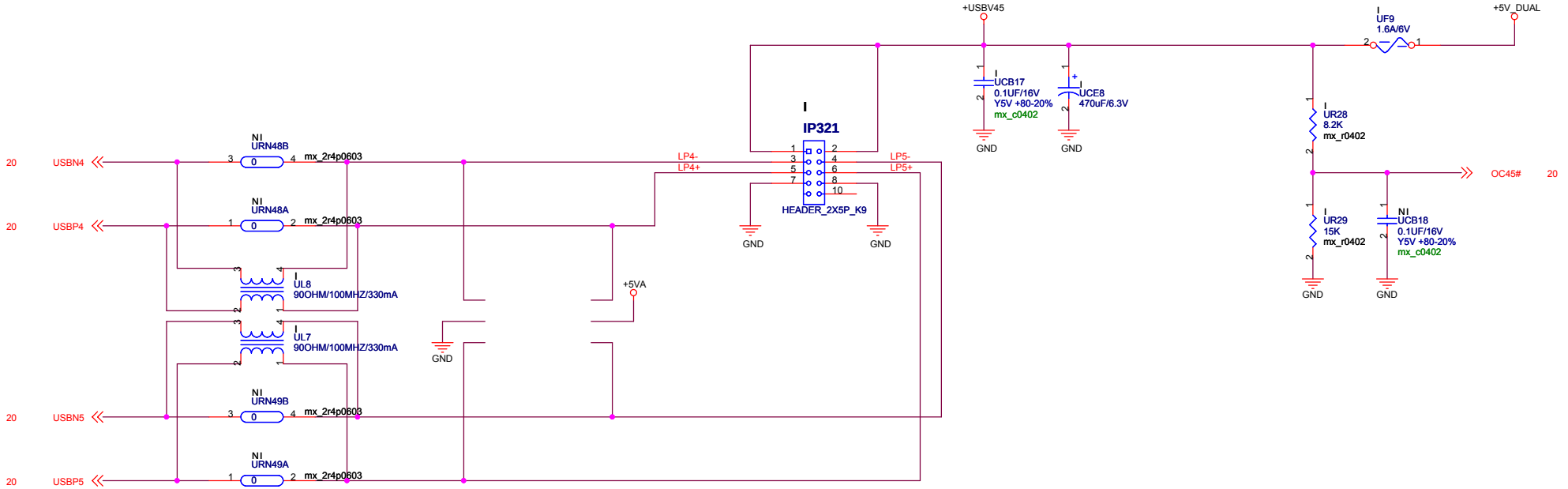
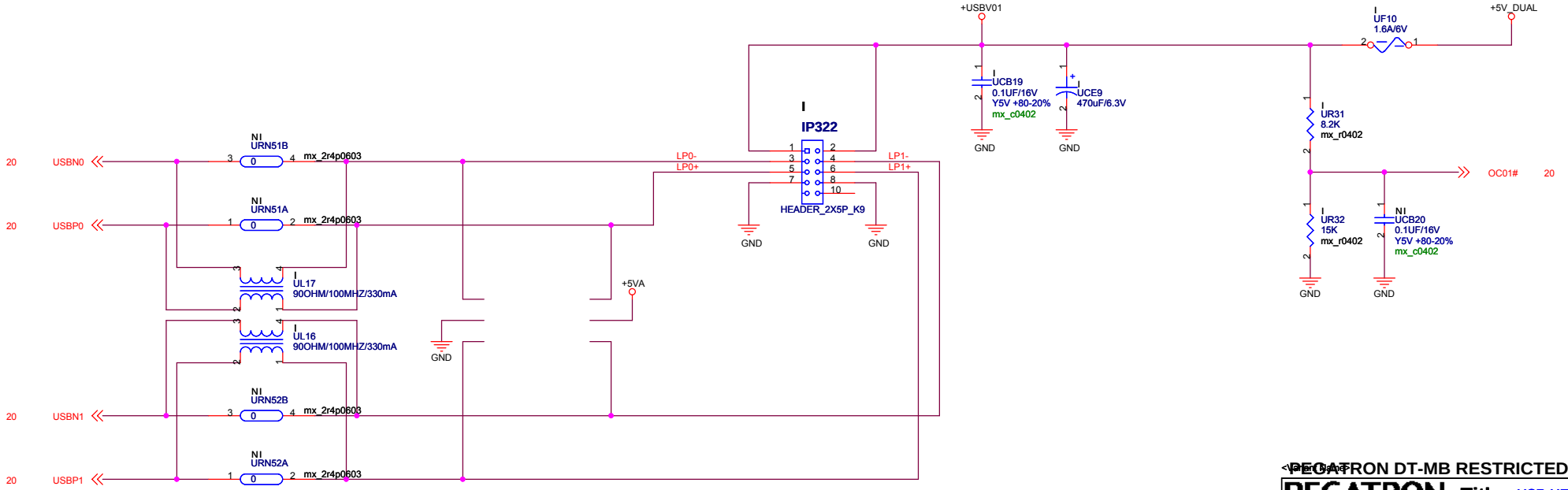
FRONT USB HEADER Port 1 & 2



FRONT USB HEADER Port 3 & 4



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB HEADER-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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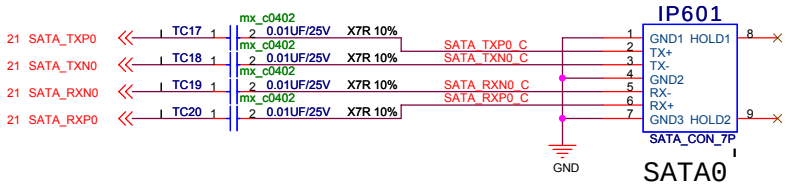
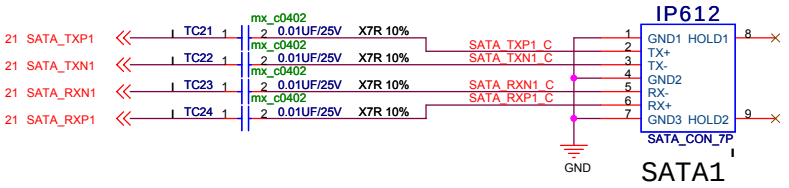
vinafix



COLOR = BLACK



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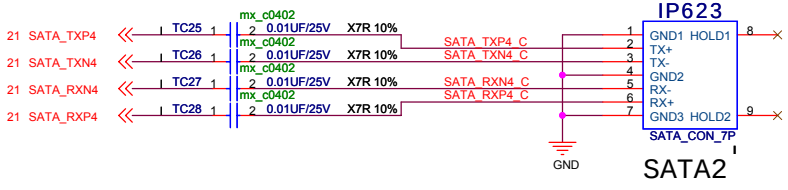

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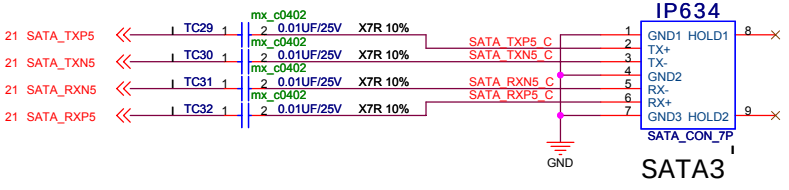

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA CONN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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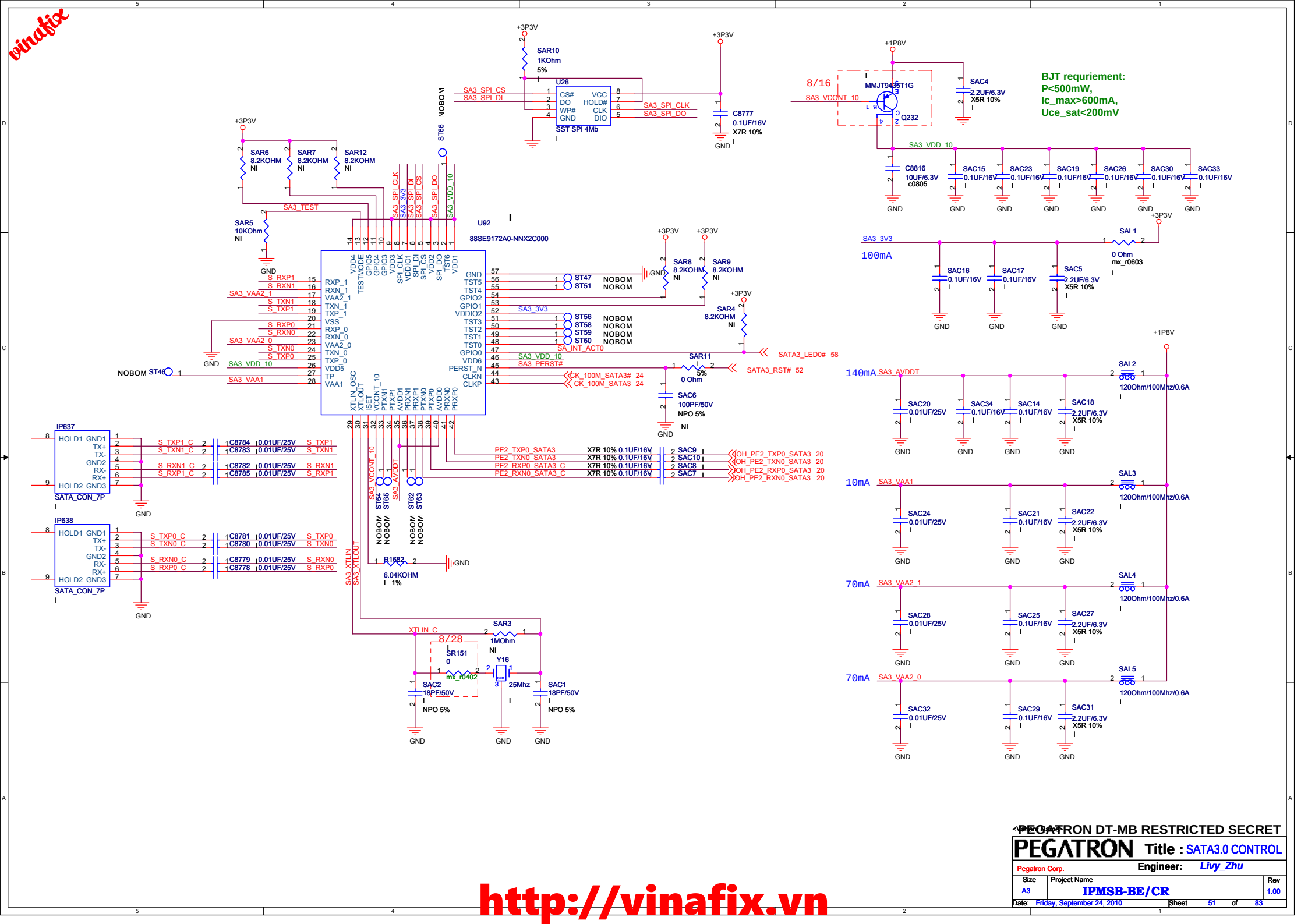
http://vinafix.vn


U92
88SE9172A0-NNX2C000
U28
SST SPI 4Mb
Q232
MMJT9435T1G
BJT requriement:
P<500mW,
Ic_max>600mA,
Uce_sat<200mV
IP637
IP638
SATA_CON_7P
SA3_VCONT_10
SA3_3V3
SA3_VDD_10
SA3_VAA1
SA3_VAA2_0
SA3_VAA2_1
SA3_AVDDT
SA3_TEST
SA_INT_ACT0
SATA3_LED0# 58
SATA3_RST# 52
100mA
140mA
10mA
70mA
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : SATA3.0 CONTROL
Pegatron Corp.
Engineer: Livy_Zhu
Size A3
Project Name IPMSB-BE/CR
Rev 1.00
Date: Friday, September 24, 2010
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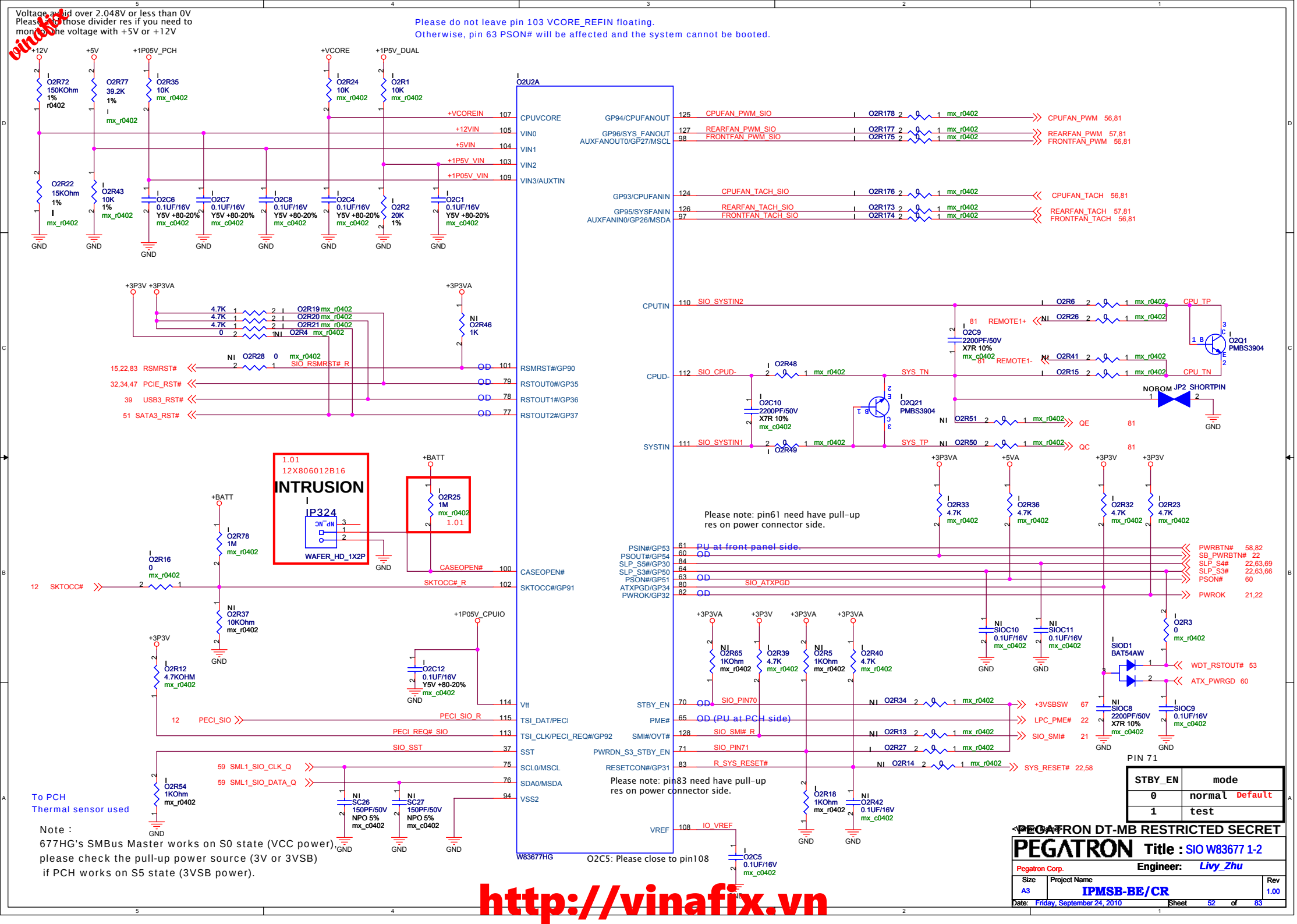
http://vinafix.vn

Voltage avoid over 2.048V or less than 0V
Please add those divider res if you need to monitor the voltage with +5V or +12V

Please do not leave pin 103 VCORE_REFIN floating.
Otherwise, pin 63 PSON# will be affected and the system cannot be booted.



STBY_EN	mode
0	normal Default
1	test

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIO W83677 1-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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SM BUS

StandBy: To PCH, PCI-Ex16,PCI-Ex1, PCI, SIO

Main Power: To SIO, DDR, VCORE_CONTROLLER, HECETA, CPU_XDP, PCH_XDP

NOTE :
PIN51/52/54/55 is OD PIN
Please check if another side already Pull-up

NOTE :
PIN56/57/58/59 is OD PIN
Please check if another side already Pull-up

W83677HG

PIN73 :
If we want to use 2.0 SW function, please pull up RSVD to 3VSB with 4.7Kohm
Else we pull up RSVD with 2.7Kohm then pin70 is STBY_EN function.

PORT80_EN(PIN62)

PORT80_EN	FUNCTION
0	GPIO Print Port Program
1	PIN 38~45,47~55 function selection

PWROK signal deley selection (PIN 81)

PGD100	PWROK DELEY
0	0 ms
1	100 ms Default

EN_DACOUT (PIN 74)

EN_DACOUT	DAC OUTPUT
0	Disable Default
1	Enable

LPC address selection (PIN 31)

RTSA#	CONFIG PORT ADDR
0	0x002E Default
1	0x004E

BUSSEL function enable/disable (PIN32)

DTR1#	BUSSSEL_EN	PIN.88~93
0	DISABLE	VIDO
1	ENABLE	BUSSEL IN/OUT

Fan initial speed selection(PIN 34)

TXD1	FANSET
0	50% Default
1	100%

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIO W83677 2-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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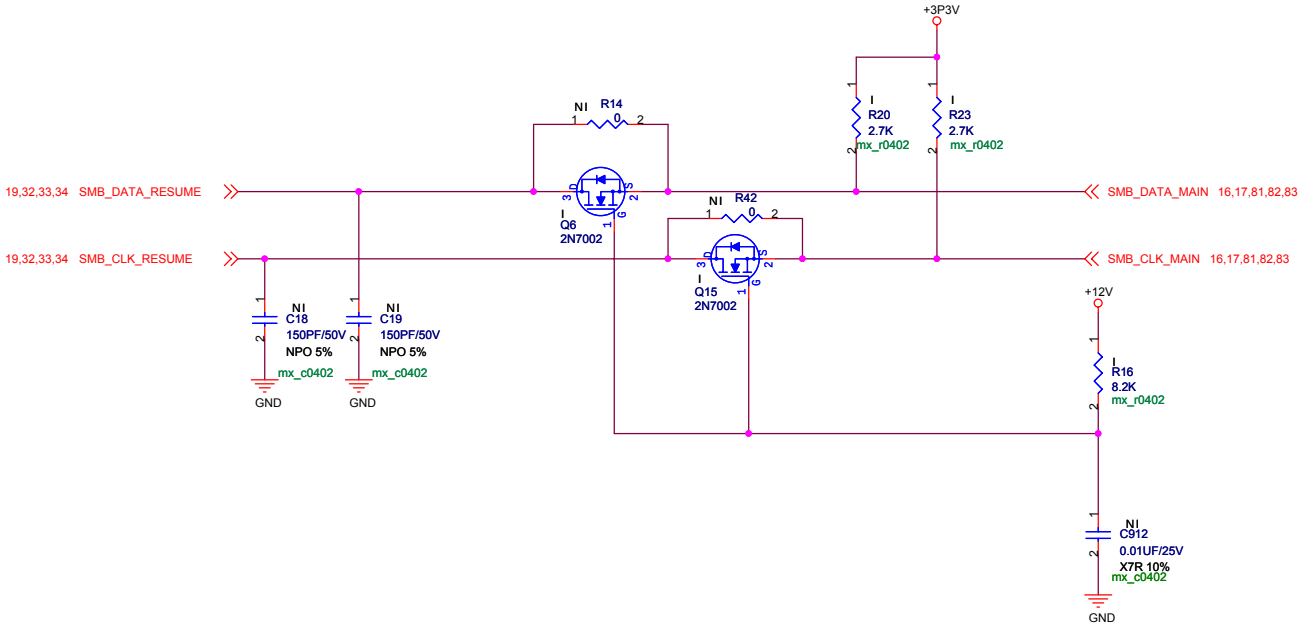
SM BUS Control



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SMBUS CONTROL	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 54 of 83	

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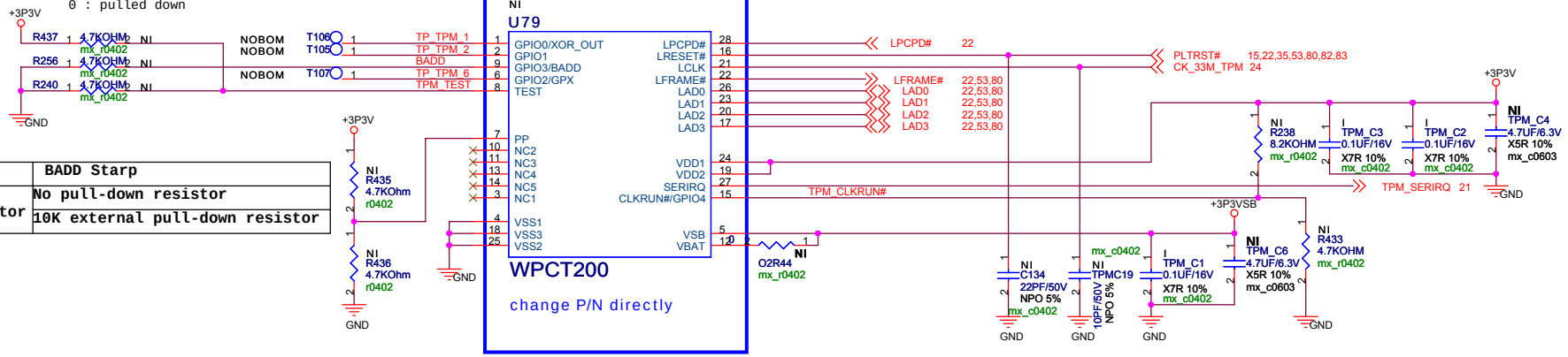
08/13: NI TPM From Fab.B

BADD	SELECTION
0	EEh-EFh
1	7Eh-7Fh

1 : left open
0 : pulled down

change to W210I
023E-000D000



Test Mode	Test Starp	BADD Starp
XOR tree	4.7K external pull-up resistor	No pull-down resistor
TRI-state		10K external pull-down resistor

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TPM

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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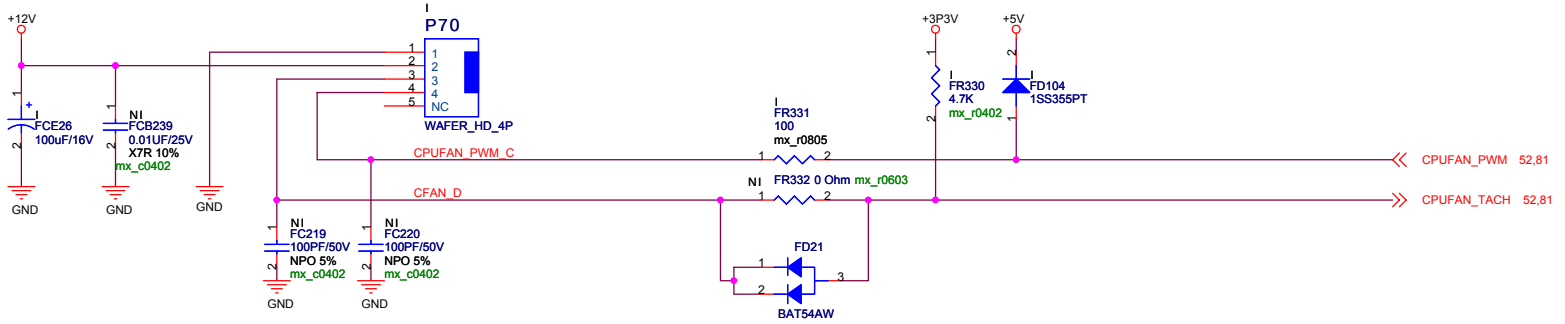
CPU FAN

COLOR: WHITE

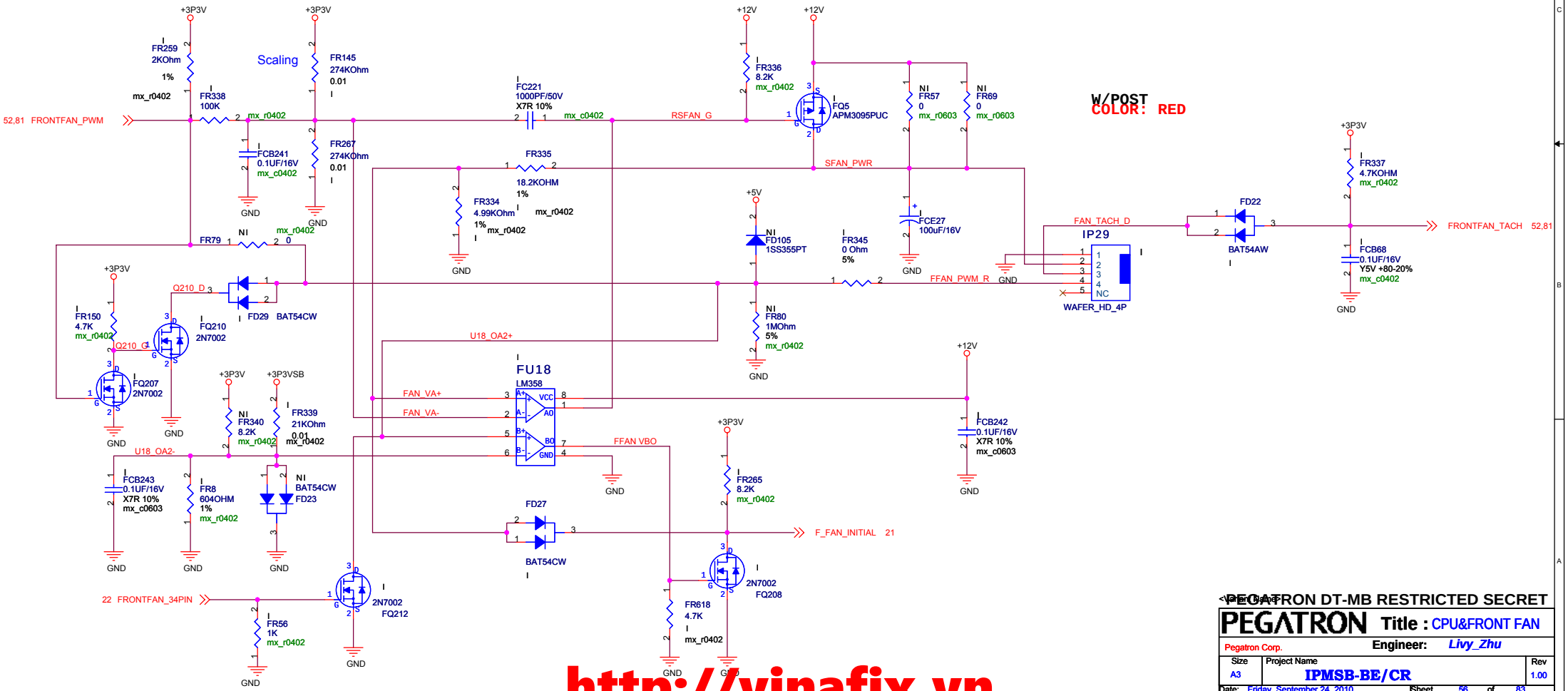
W/POST



FRONT FAN

W/POST

COLOR: RED



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU&FRONT FAN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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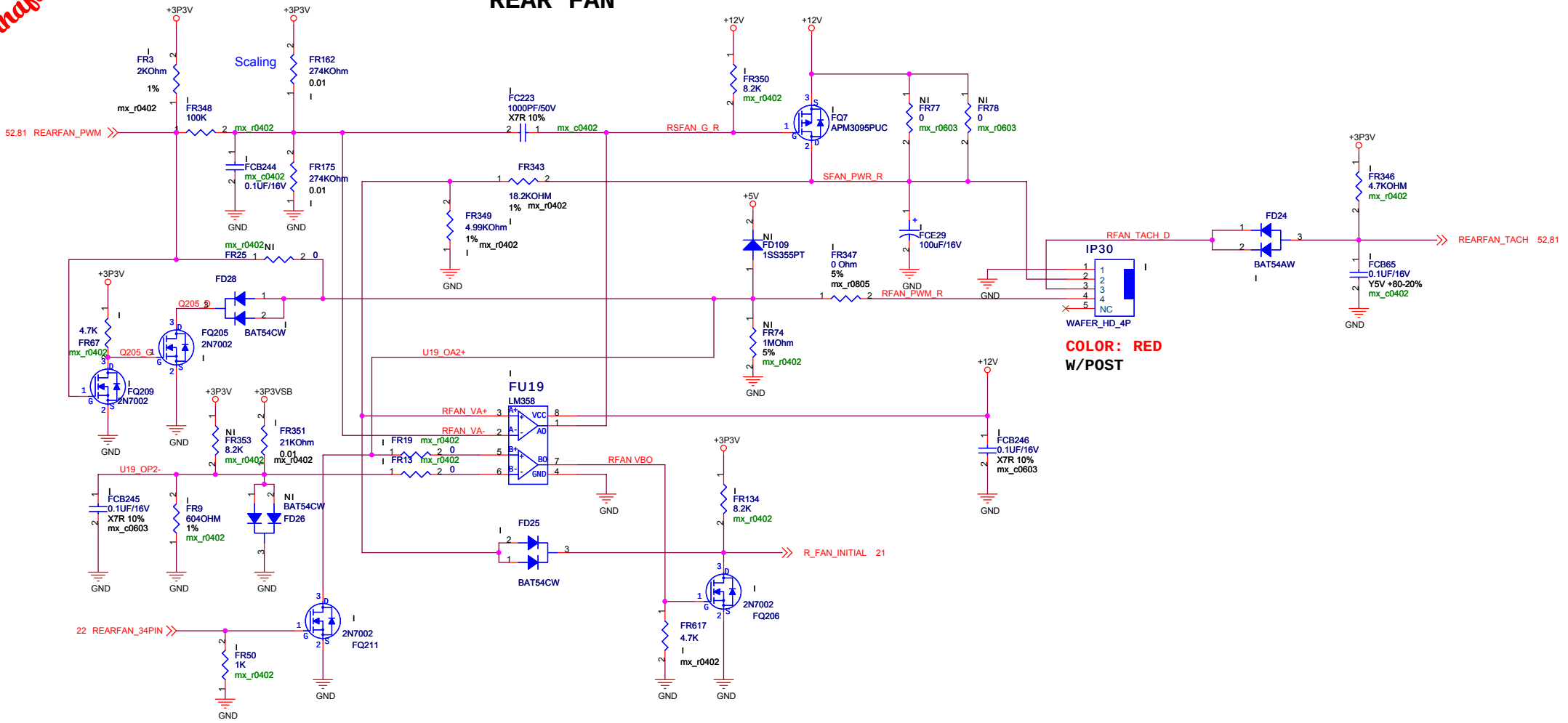
REAR FAN



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : REAR FAN CIRCUIT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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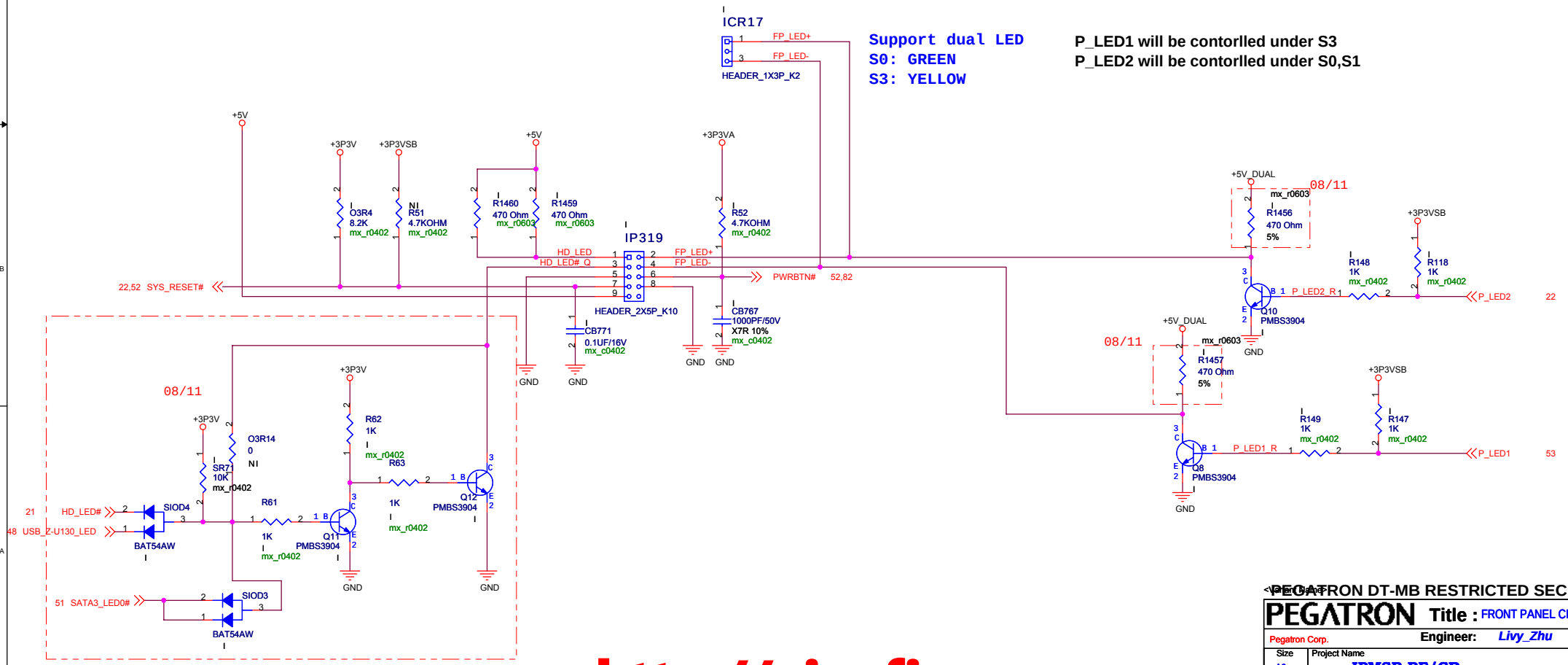
vinafix

FRONT PANEL / LED CIRCUITRY

NOTE:
PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V standby through a weak pull-up 24Kohm.



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FRONT PANEL CIRCUIT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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http://vinafix.vn

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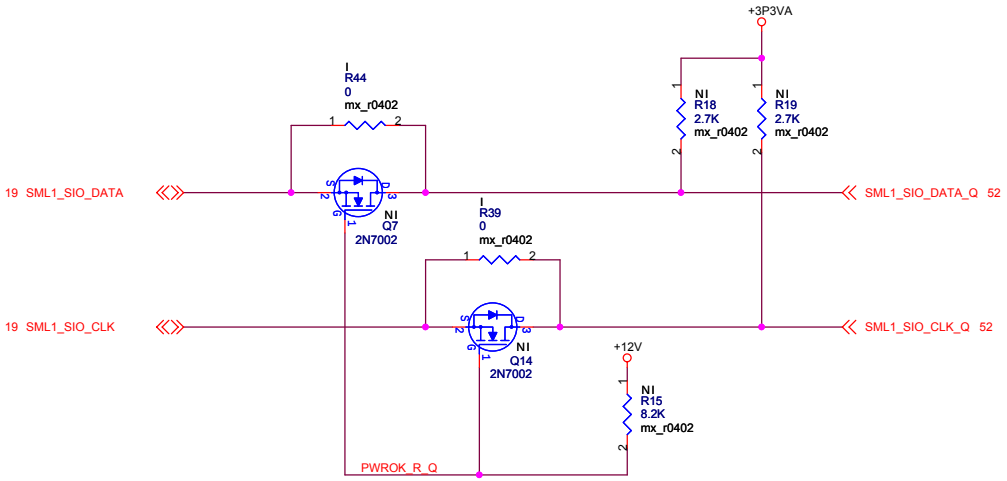
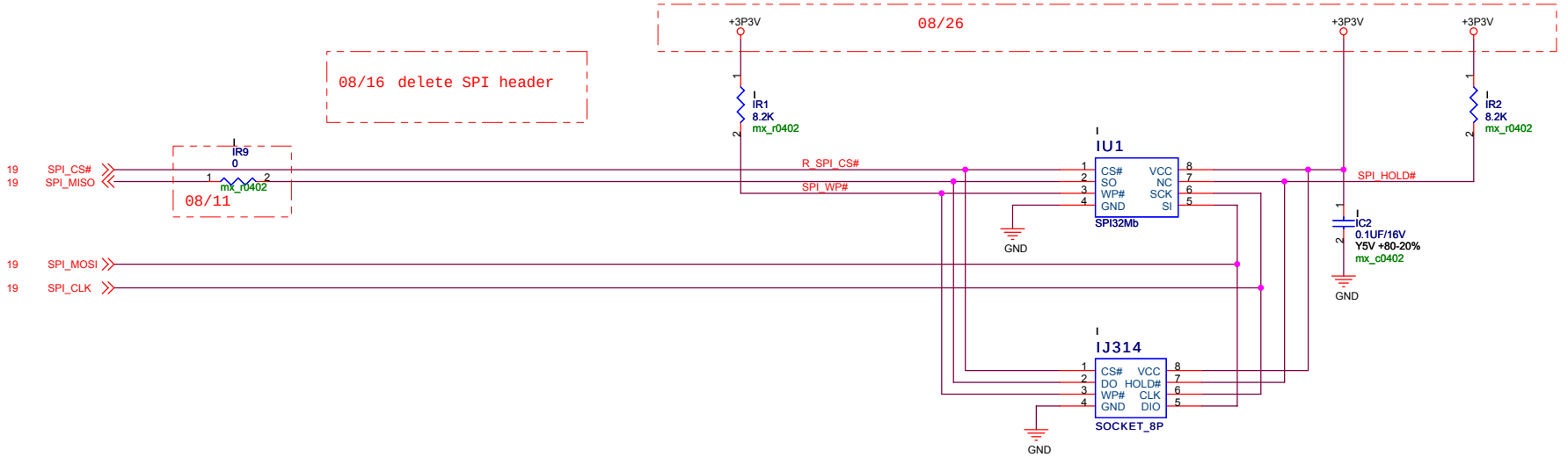
SM BUS Control



SPI BIOS ROM - 32 Mbit



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SPI ROM

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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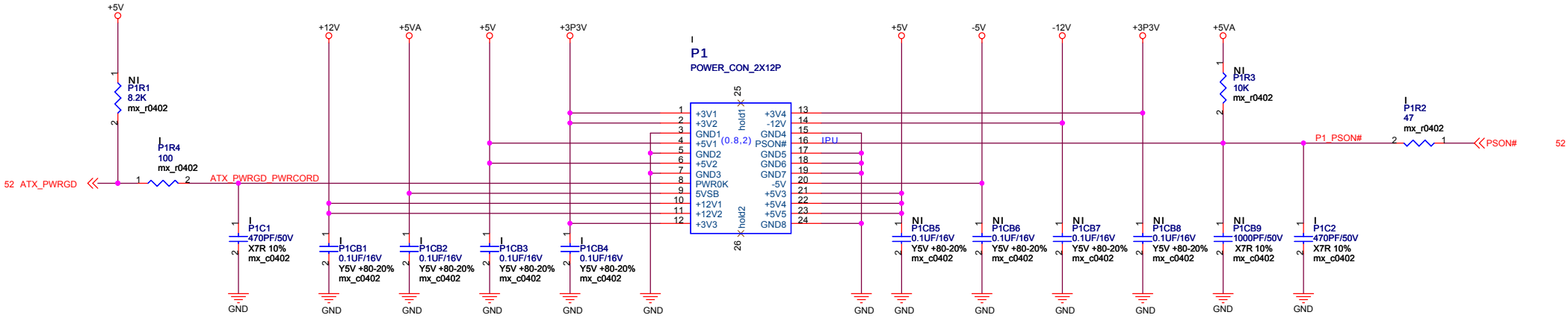
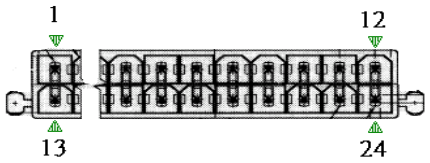
ATX POWER_24P SUPPLY CONNECTOR



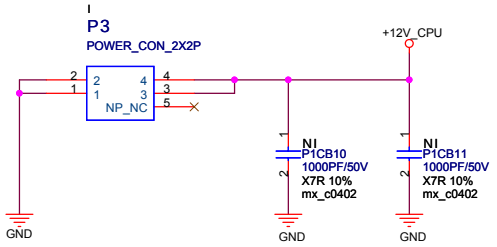
BOTTOM SIDE VIEW

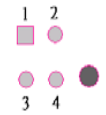


TOP SIDE VIEW

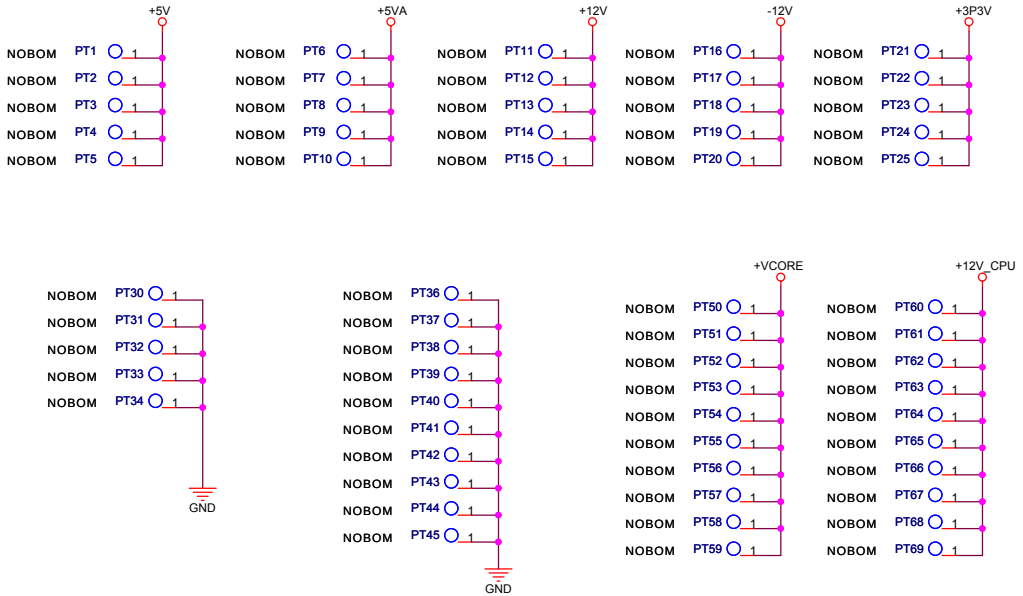
PCB

VRM POWER_4P SUPPLY CONNECTOR





BOTTOM SIDE VIEW



Nodes related to different power planes

Node	Goal Q'ty
+5V	5
+5VSB	5
+12V	5
-12V	5
+3V	5
+Vcore	10
GND	15
+12V_CPU	10

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : ATX 24P CONN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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http://vinafix.vn

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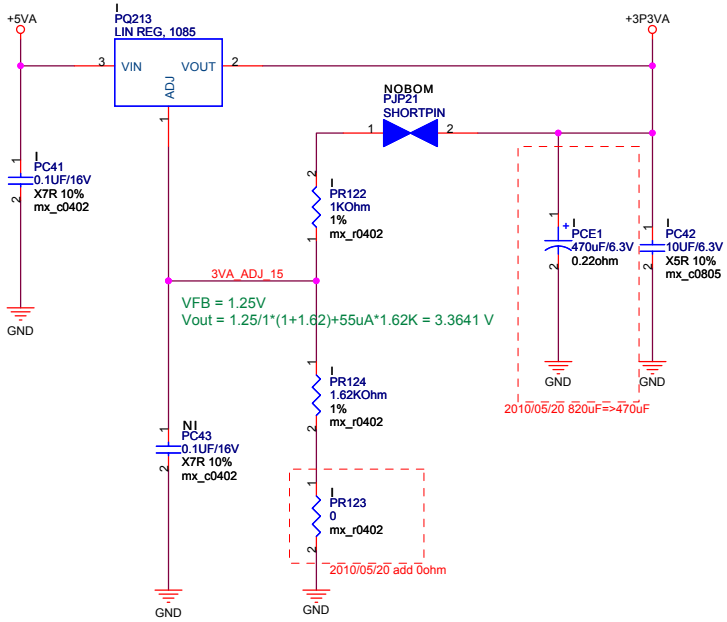
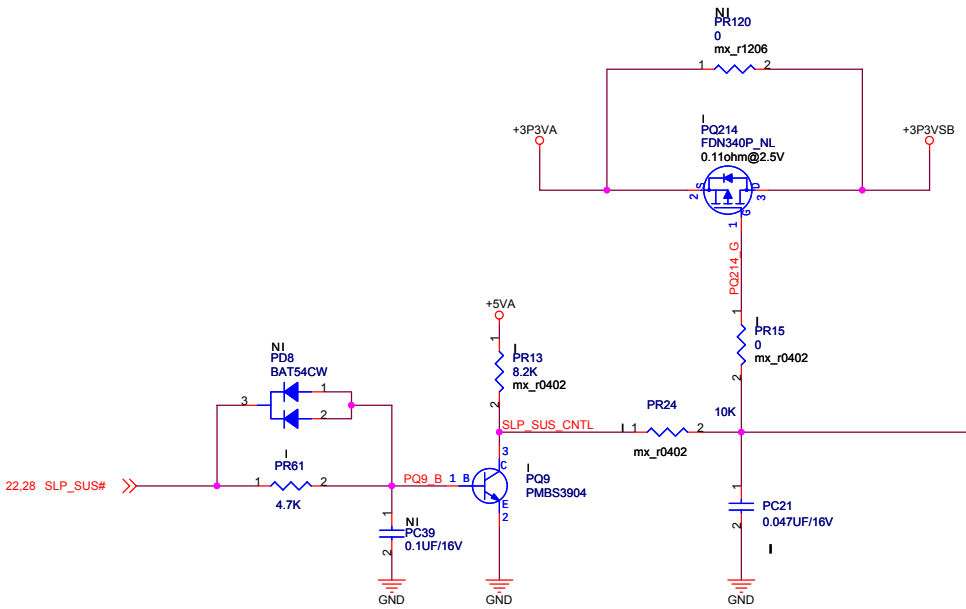
+3P3VA

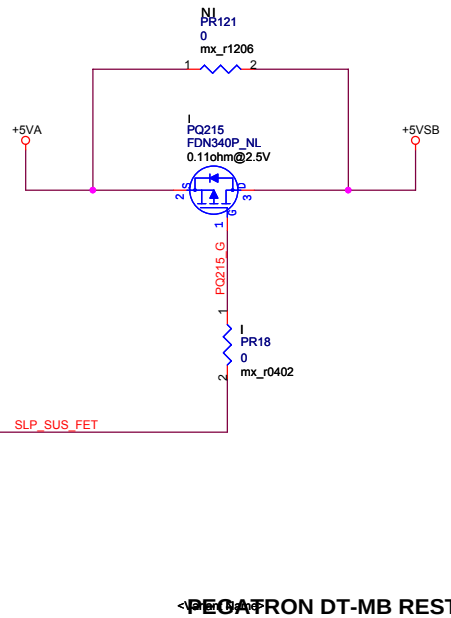
Imax = 1.5A
Pd = 2.55W



+3P3VA => +3VSB



+5VA => +5VSB



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +3VA,+3VSB,+5VSB

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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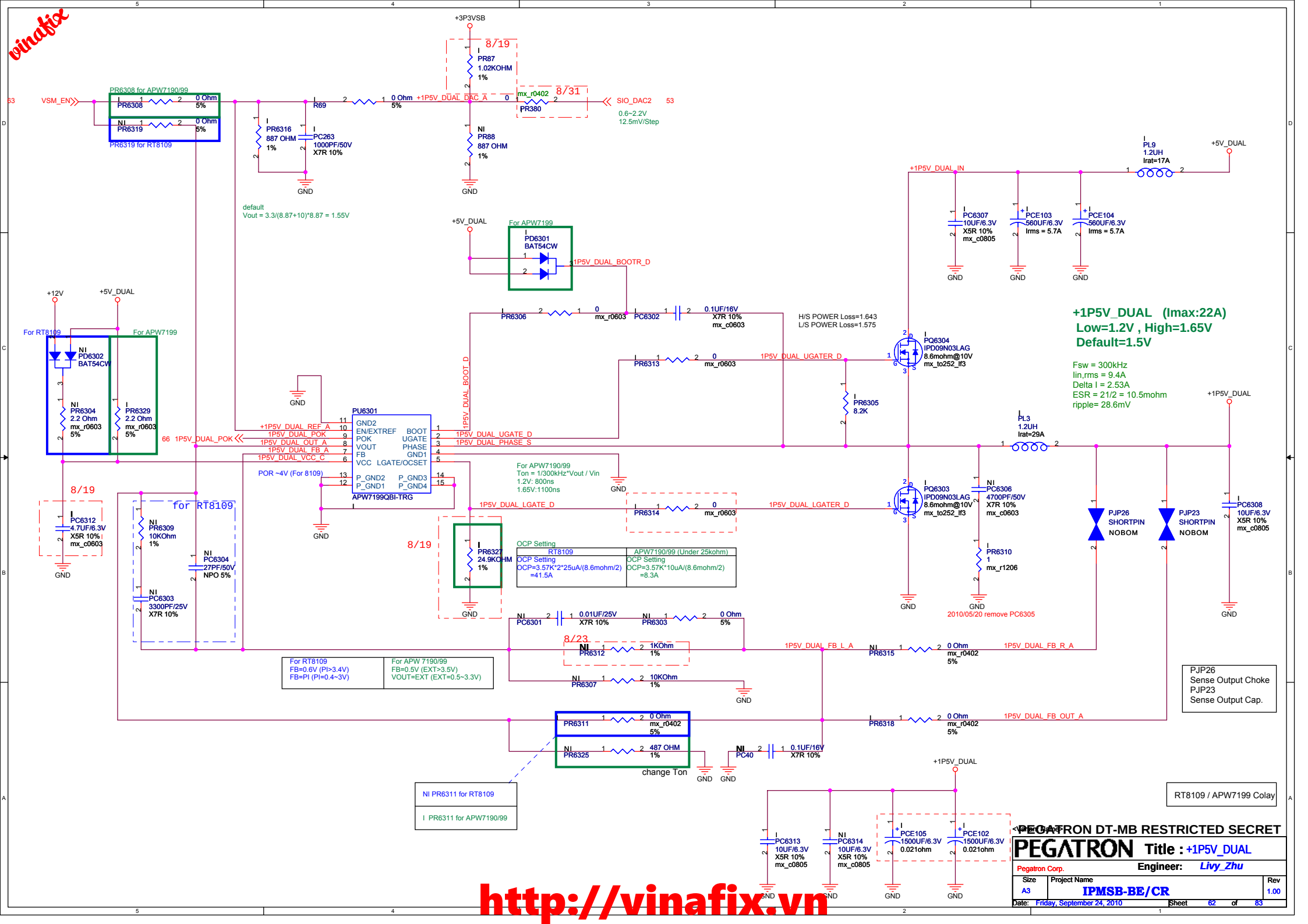
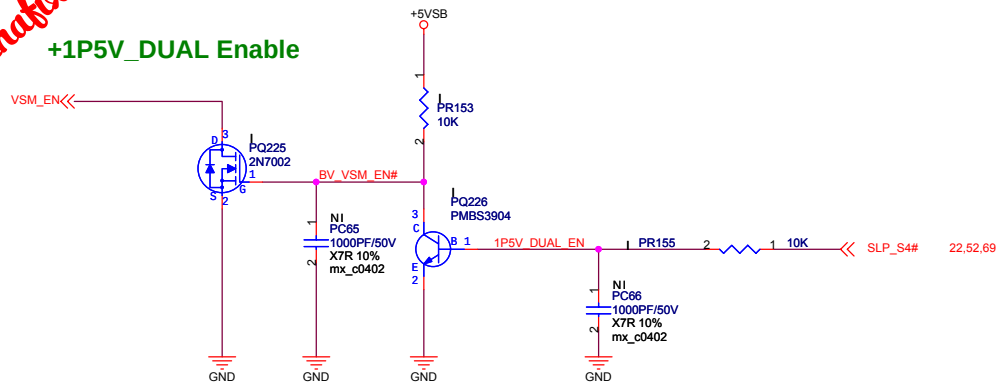

+1P5V_DUAL (Imax:22A)
Low=1.2V , High=1.65V
Default=1.5V
Fsw = 300kHz
Iin,rms = 9.4A
Delta I = 2.53A
ESR = 21/2 = 10.5mohm
ripple= 28.6mV
PU6301
APW7199QBI-TRG
PJP26
Sense Output Choke
PJP23
Sense Output Cap.
RT8109 / APW7199 Colay
change Ton
NI PR6311 for RT8109
I PR6311 for APW7190/99
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : +1P5V_DUAL
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 62 of 83
http://vinafix.vn

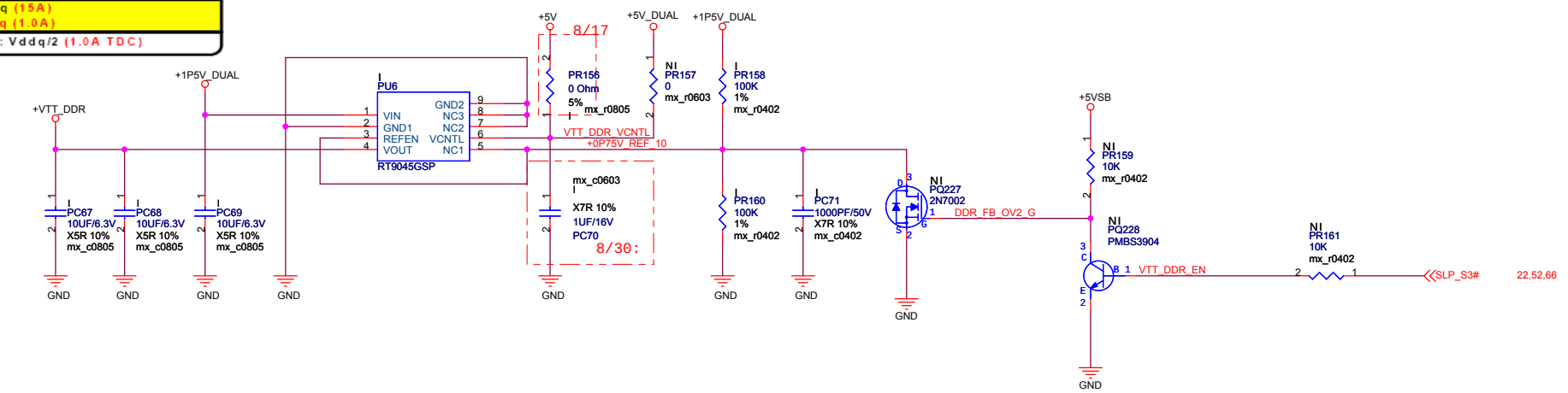
vinafix

+1P5V_DUAL Enable



DDR3 DIMM (4) 1333MHz
V_SM_S0: Vddq (15A)
V_SM_S3: Vddq (1.0A)
V_SM_VTT_S0: Vddq/2 (1.0A TDC)

+1P5V_DUAL ==> +VTT_DDR...(1A)



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +VTT_DDR&+1P5V_DUAL_EN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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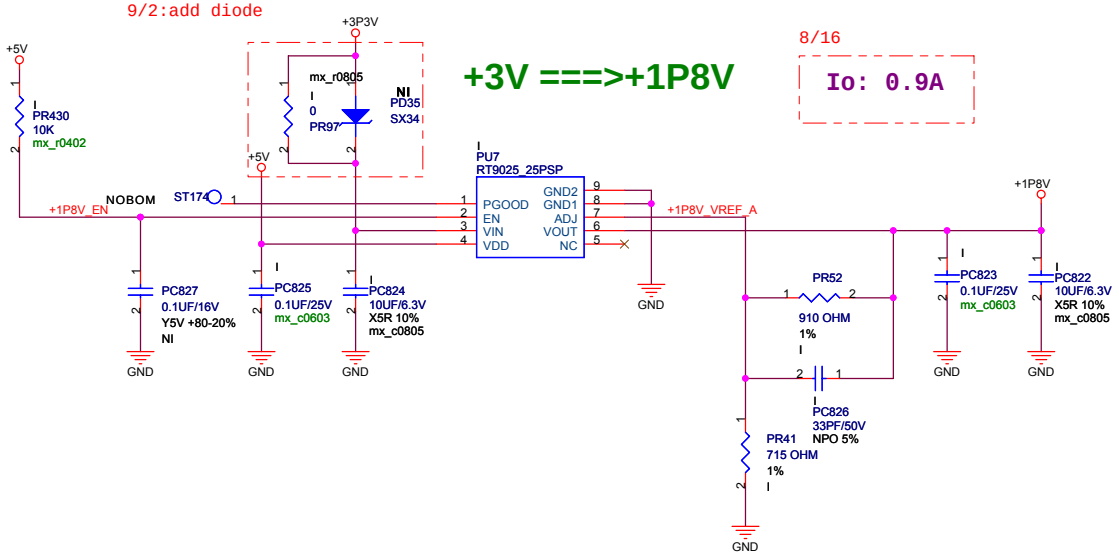
http://vinafix.vn

vinafix

9/2:add diode



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P8V FOR SATA3.0	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 64 of 83	

http://vinafix.vn

vinafix

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSA_OV_FUNCTION

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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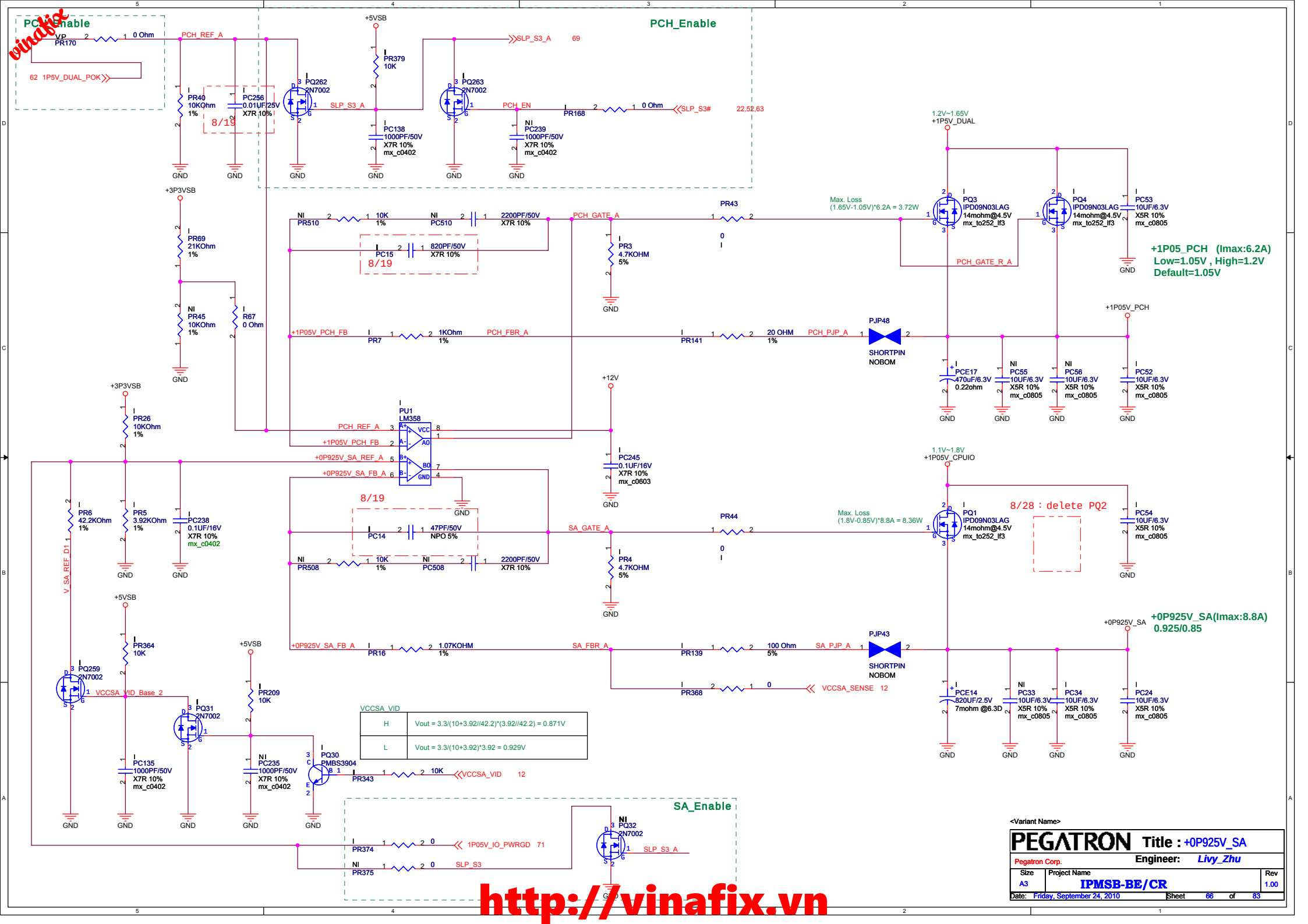
http://vinafix.vn


PCH_Enable
PR170 0 Ohm
62 1P5V_DUAL_POK
PCH_REF_A
PR40 10KOhm 1%
PC256 0.01UF/25V X7R 10%
8/19
PQ262 2N7002
SLP_S3_A
+5VSB
PR379 10K
PC138 1000PF/50V X7R 10% mx_c0402
PQ263 2N7002
SLP_S3_A 69
PCH_EN
PR168 0 Ohm
SLP_S3# 22,52,63
NI PC239 1000PF/50V X7R 10% mx_c0402
GND
+3P3VSB
PR69 21KOhm 1%
NI PR45 10KOhm 1%
R67 0 Ohm
NI PR510 10K 1%
NI PC510 2200PF/50V X7R 10%
PC15 820PF/50V X7R 10%
8/19
PCH_GATE_A
PR3 4.7KOHM 5%
PR43 0
Max. Loss (1.65V-1.05V)*6.2A = 3.72W
PQ3 IPD09N03LAG 14mohm@4.5V mx_to252_lf3
PQ4 IPD09N03LAG 14mohm@4.5V mx_to252_lf3
PCH_GATE_R_A
1.2V~1.65V +1P5V_DUAL
PC53 10UF/6.3V X5R 10% mx_c0805
+1P05_PCH (Imax:6.2A)
Low=1.05V , High=1.2V
Default=1.05V
+1P05V_PCH_FB
PR7 1KOhm 1%
PCH_FBR_A
PR141 20 OHM 1%
PCH_PJP_A
PJP48 SHORTPIN NOBOM
+1P05V_PCH
PCE17 470uF/6.3V 0.22ohm
NI PC55 10UF/6.3V X5R 10% mx_c0805
NI PC56 10UF/6.3V X5R 10% mx_c0805
PC52 10UF/6.3V X5R 10% mx_c0805
+12V
PU1 LM358
PCH_REF_A
+1P05V_PCH_FB
+0P925V_SA_REF_A
+0P925V_SA_FB_A
PC245 0.1UF/16V X7R 10% mx_c0603
PR26 10KOhm 1%
PR6 42.2KOhm 1%
PR5 3.92KOhm 1%
PC238 0.1UF/16V X7R 10% mx_c0402
V_SA_REF_D1
8/19
PC14 47PF/50V NPO 5%
NI PR508 10K 1%
NI PC508 2200PF/50V X7R 10%
SA_GATE_A
PR4 4.7KOHM 5%
PR44 0
Max. Loss (1.8V-0.85V)*8.8A = 8.36W
PQ1 IPD09N03LAG 14mohm@4.5V mx_to252_lf3
8/28 : delete PQ2
1.1V~1.8V +1P05V_CPUIO
PC54 10UF/6.3V X5R 10% mx_c0805
+0P925V_SA_FB_A
PR16 1.07KOHM 1%
SA_FBR_A
PR139 100 Ohm 5%
SA_PJP_A
PJP43 SHORTPIN NOBOM
+0P925V_SA
+0P925V_SA(Imax:8.8A)
0.925/0.85
PCE14 820UF/2.5V 7mohm @6.3D
NI PC33 10UF/6.3V X5R 10% mx_c0805
PC34 10UF/6.3V X5R 10% mx_c0805
PC24 10UF/6.3V X5R 10% mx_c0805
PR368 0
VCCSA_SENSE 12
PQ259 2N7002
VCCSA_VID_Base_2
PR364 10K
PQ31 2N7002
PR209 10K
PC135 1000PF/50V X7R 10% mx_c0402
NI PC235 1000PF/50V X7R 10% mx_c0402
PQ30 PMBS3904
PR343 10K
VCCSA_VID 12
VCCSA_VID
H Vout = 3.3/(10+3.92//42.2)*(3.92//42.2) = 0.871V
L Vout = 3.3/(10+3.92)*3.92 = 0.929V
SA_Enable
PR374 0
1P05V_IO_PWRGD 71
NI PR375 0
SLP_S3
NI PQ32 2N7002
SLP_S3_A
<Variant Name>
PEGATRON Title : +0P925V_SA
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
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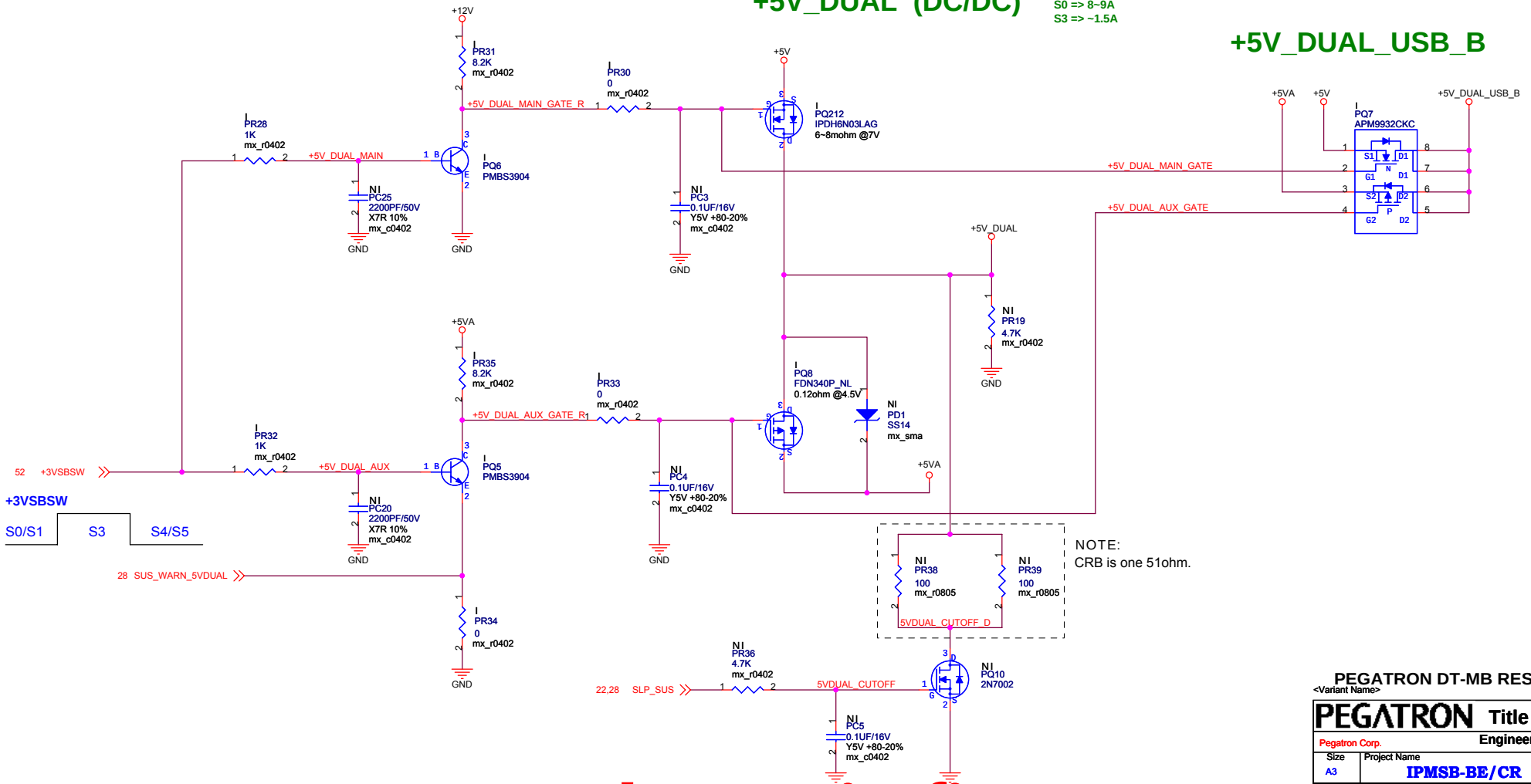
http://vinafix.vn

vinafix

+5V_DUAL (DC/DC)

+5V_DUAL
S0 => 8~9A
S3 => ~1.5A

+5V_DUAL_USB_B



NOTE:
CRB is one 51ohm.

PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON Title : DUAL POWER

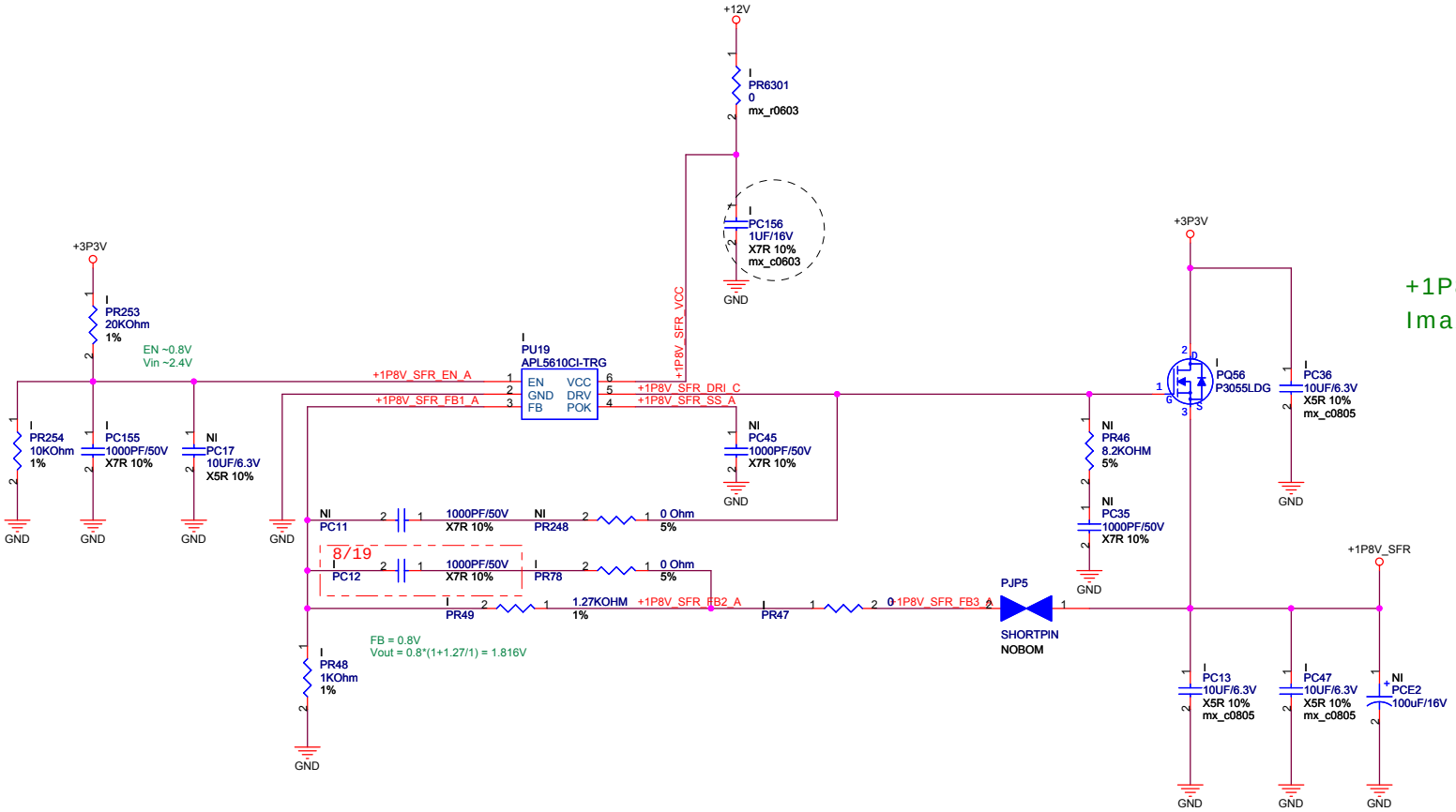
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 67 of 83

http://vinafix.vn

vinafix



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P8V_SFR	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
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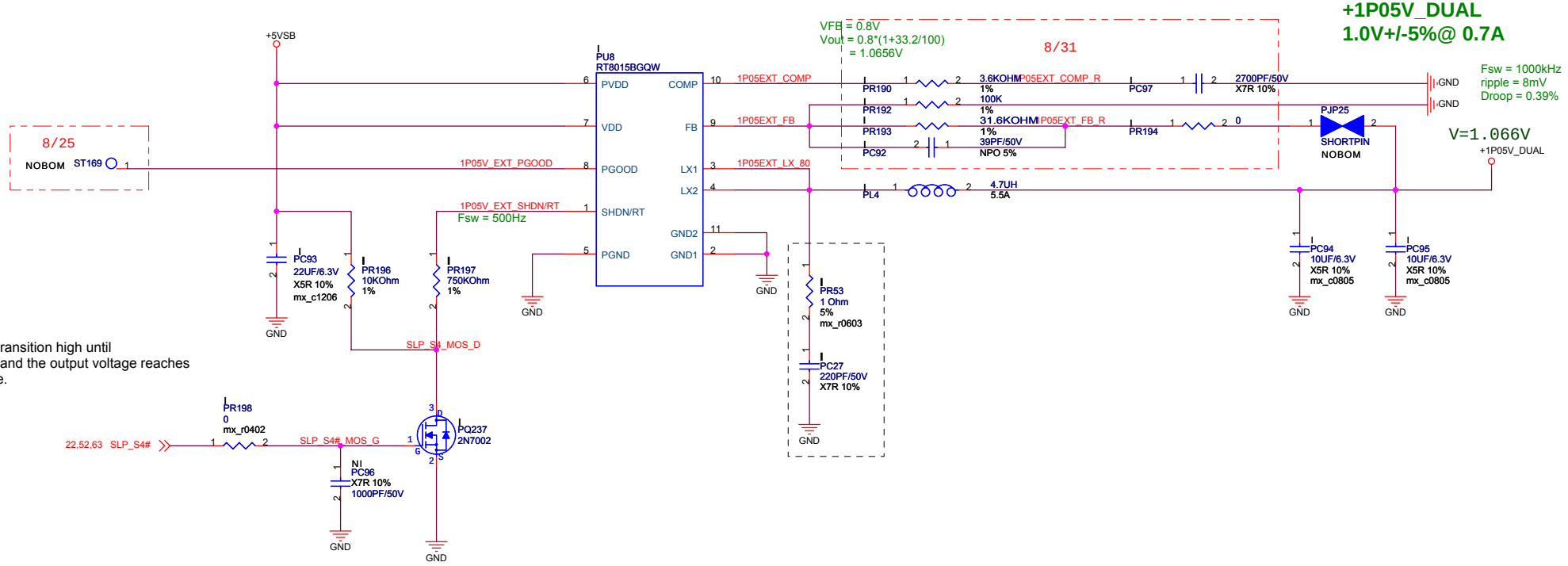
http://vinafix.vn

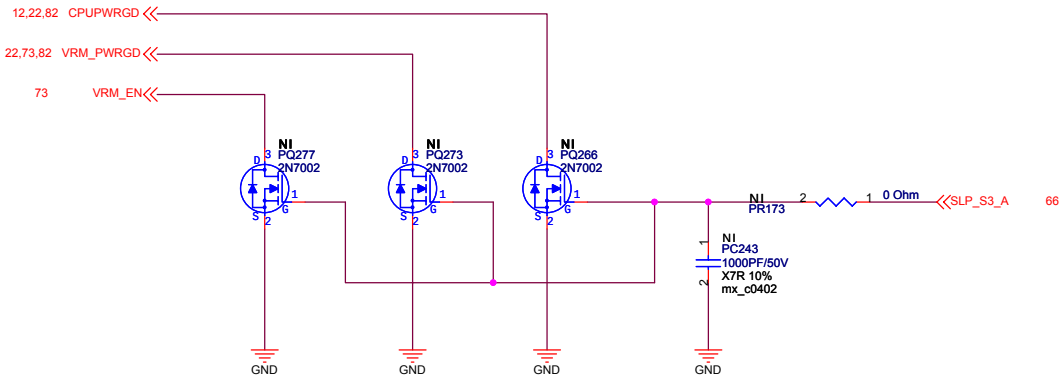
vinafix

+1P05V_DUAL
1.0V+/-5%@ 0.7A



NOTE:
PGOOD is allowed to transition high until soft start finished over and the output voltage reaches 87.5% of its set voltage.

VRM_EN



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1V_DUAL

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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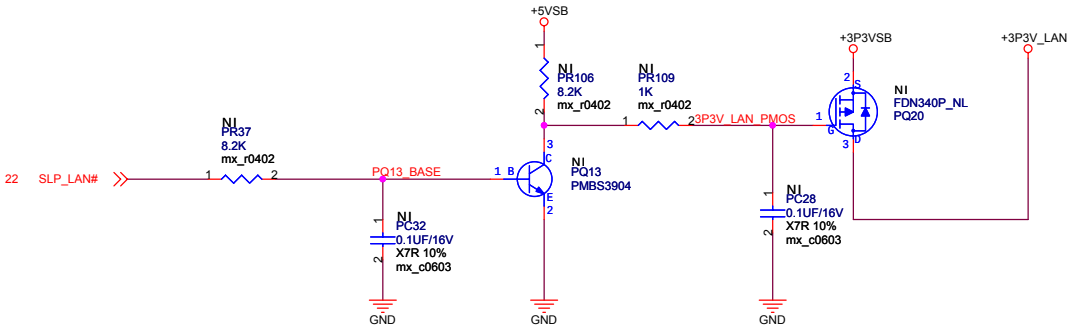
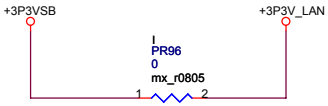
Lewisville (LAN)
V3.3S_LAN (0.218A) (OPTION)
V1.0S_LAN (332mA)





+3P3V_LAN

8/26:delete +3P3V_ME

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +3P3V_LAN +3P3V_ME

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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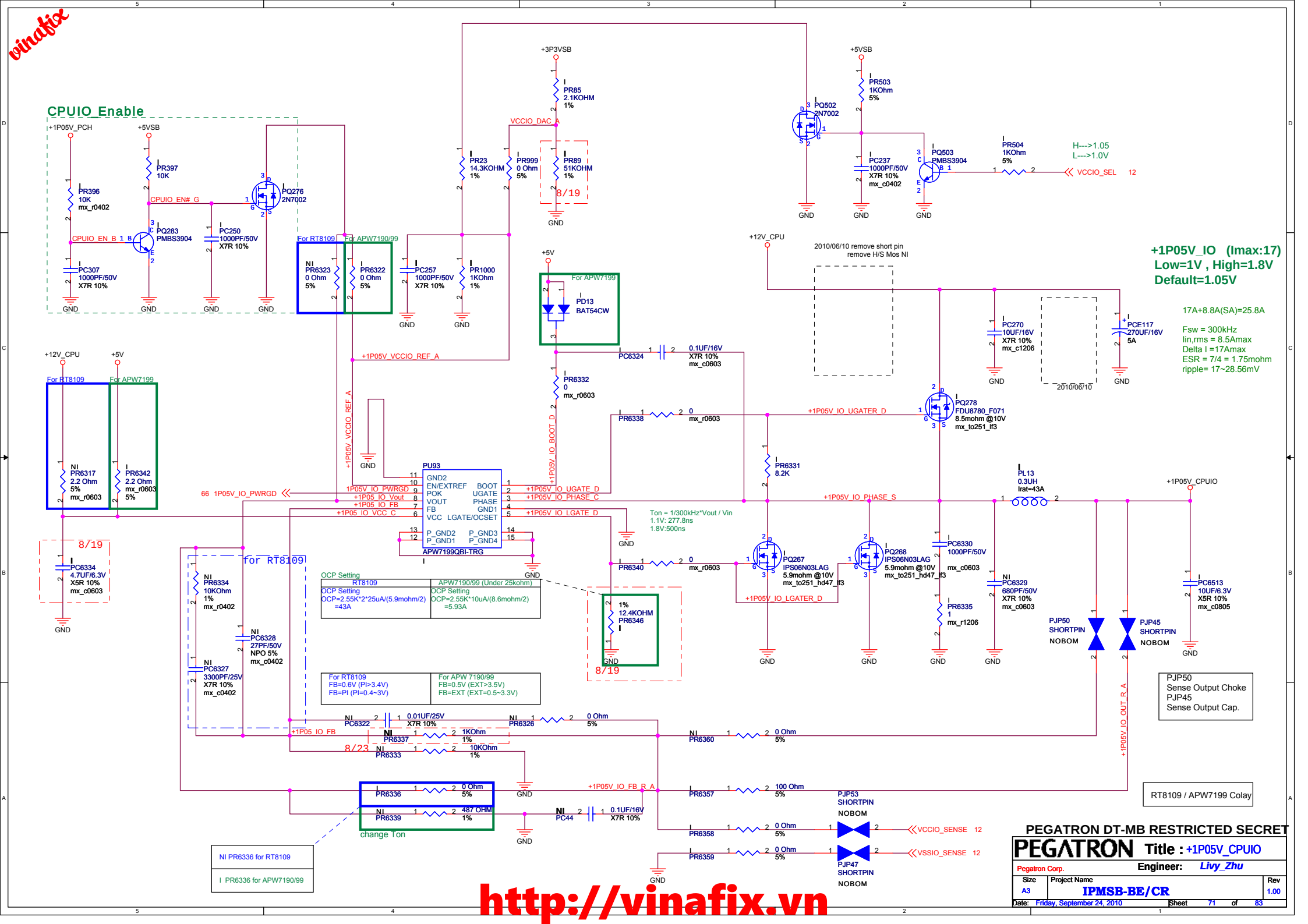
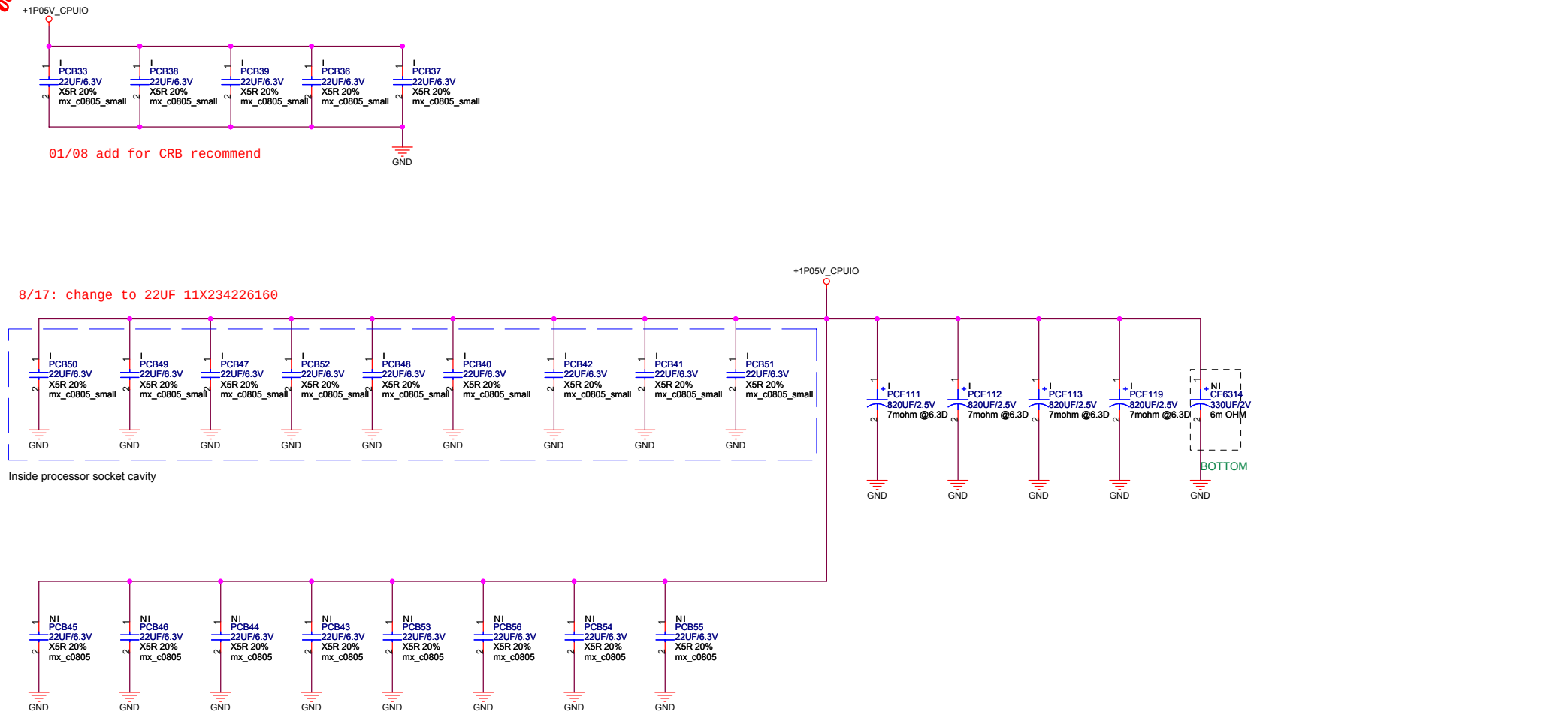
http://vinafix.vn


CPUIO_Enable
+1P05V_IO (Imax:17)
Low=1V , High=1.8V
Default=1.05V
17A+8.8A(SA)=25.8A
Fsw = 300kHz
Iin,rms = 8.5Amax
Delta I =17Amax
ESR = 7/4 = 1.75mohm
ripple= 17~28.56mV
2010/06/10 remove short pin
remove H/S Mos NI
PU93
APW7199QBI-TRG
PJP50
SHORTPIN
NOBOM
PJP45
SHORTPIN
NOBOM
PJP53
SHORTPIN
NOBOM
PJP47
SHORTPIN
NOBOM
PJP50
Sense Output Choke
PJP45
Sense Output Cap.
RT8109 / APW7199 Colay
change Ton
NI PR6336 for RT8109
I PR6336 for APW7190/99
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : +1P05V_CPUIO
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 71 of 83
http://vinafix.vn

vinafix



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P05V_CPUIO CAP

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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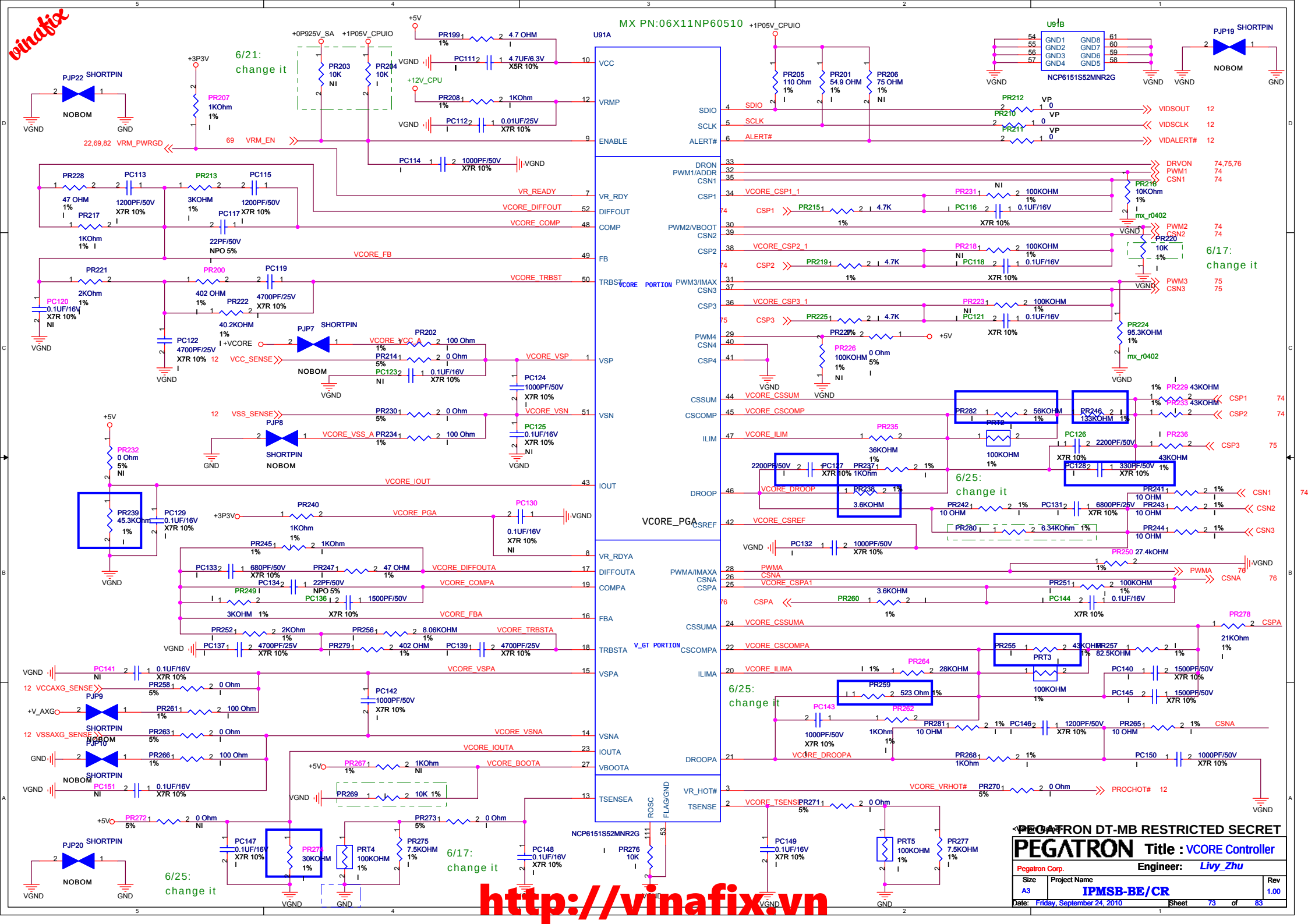
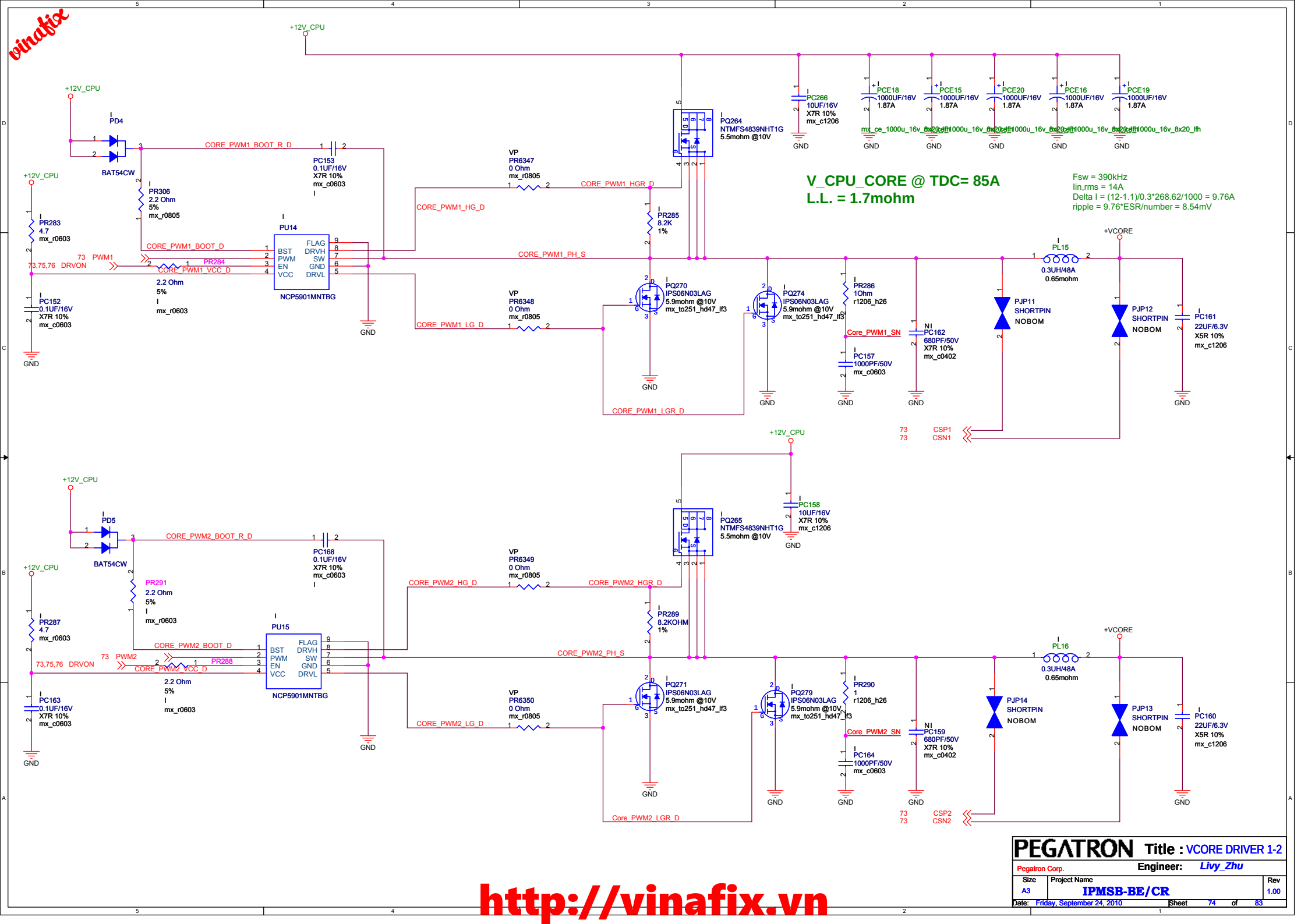
http://vinafix.vn


MX PN:06X11NP60510
U91A
VCORE_PGA
VCORE PORTION
V_GT PORTION
NCP6151S52MNR2G
U91B
NCP6151S52MNR2G
6/21: change it
6/17: change it
6/25: change it
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : VCORE Controller
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 73 of 83
http://vinafix.vn



PEGATRON Title : VCORE DRIVER 1-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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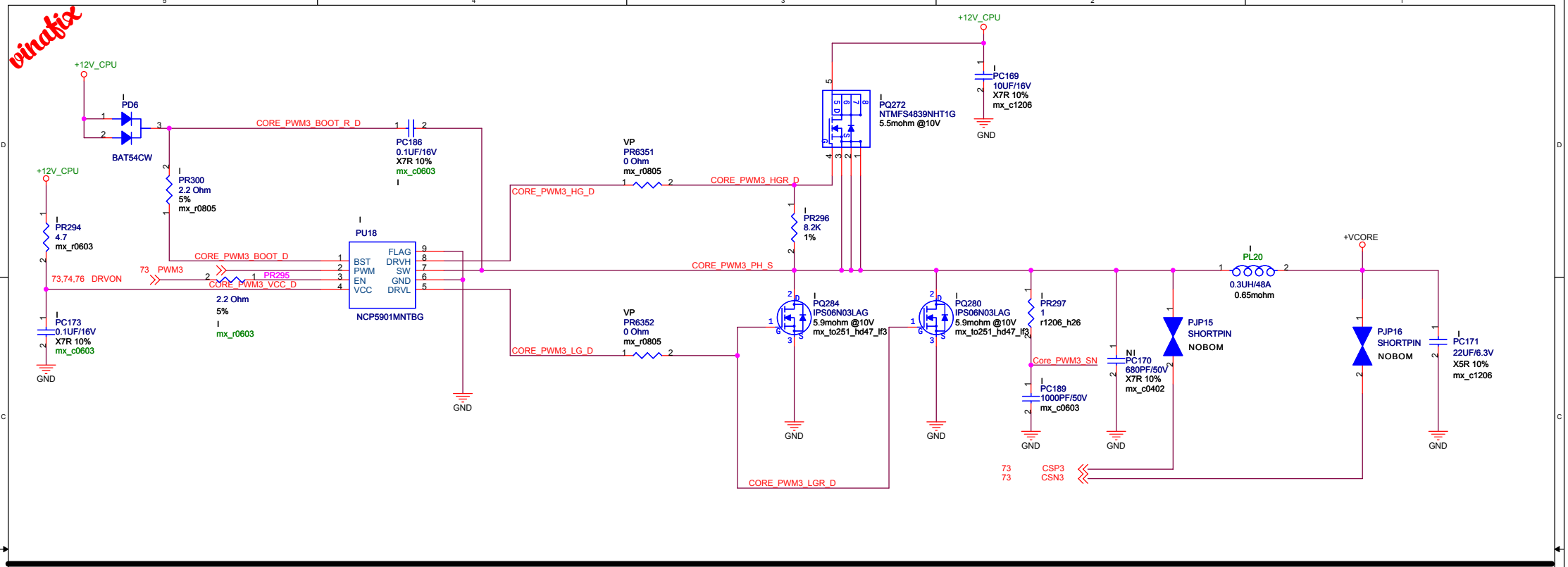
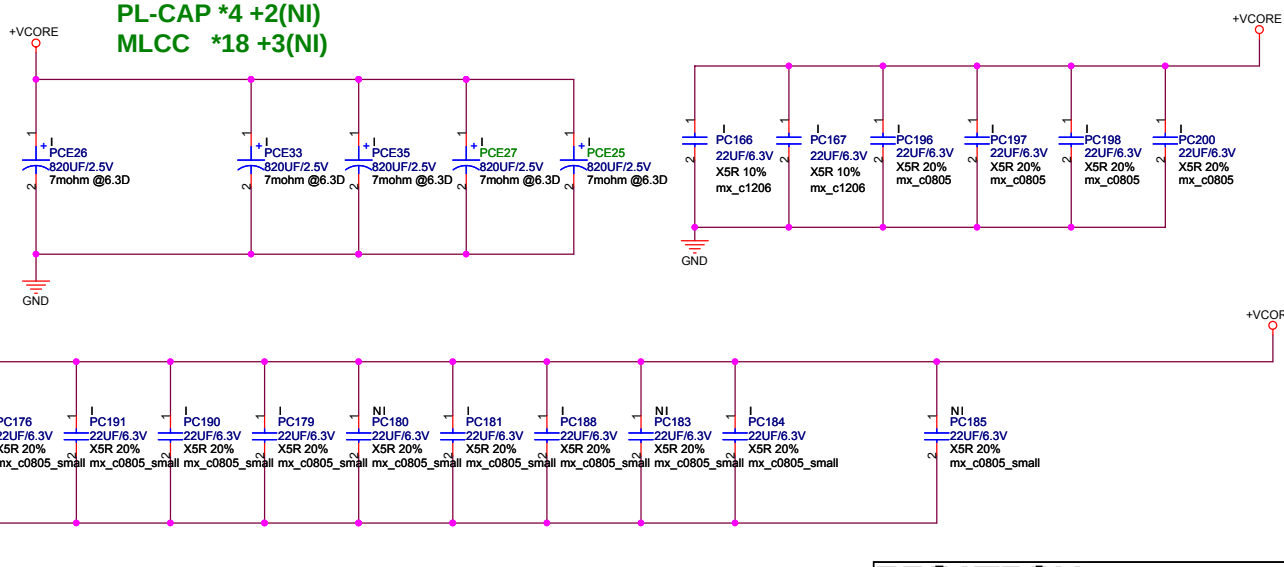


Output CAP

Table 30-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



PEGATRON Title : VCORE DRIVER 2-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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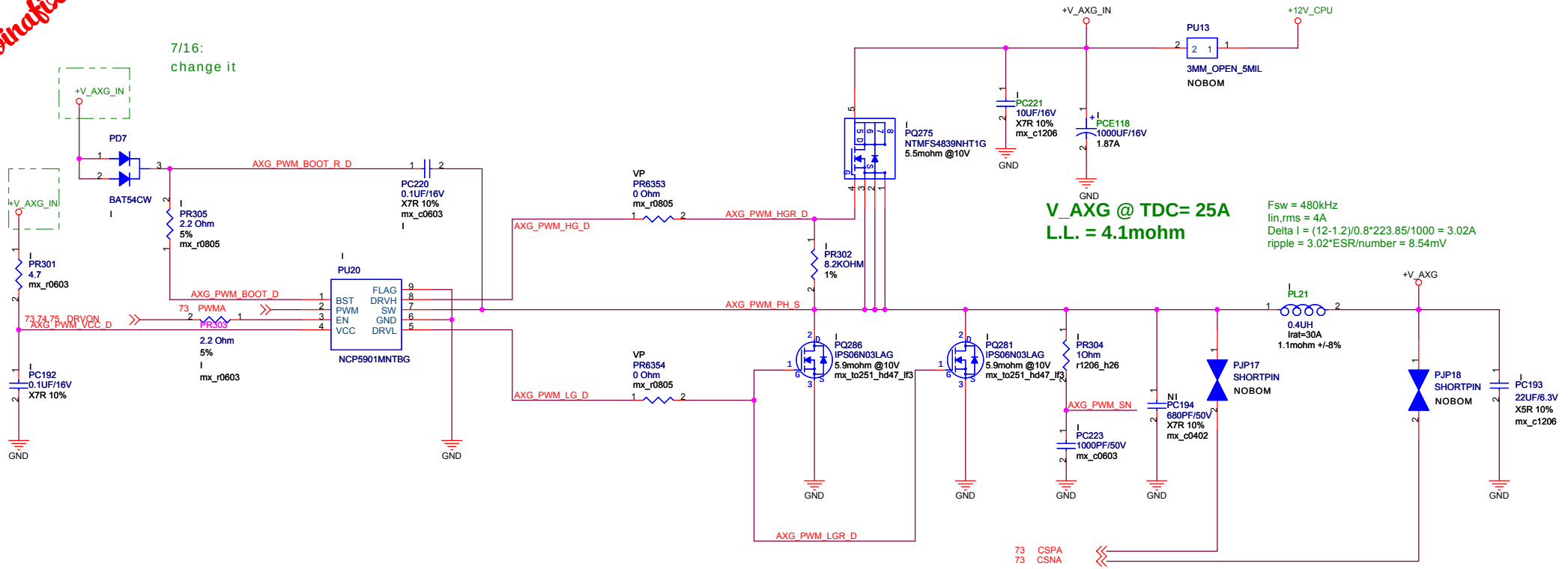
vinafix

7/16:
change it

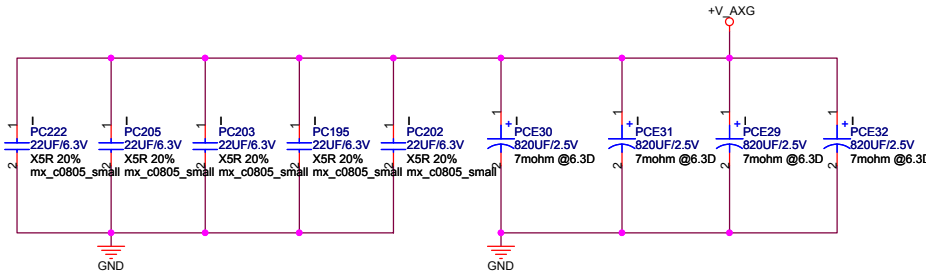


Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +VAXG_DRIVER
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
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http://vinafix.vn

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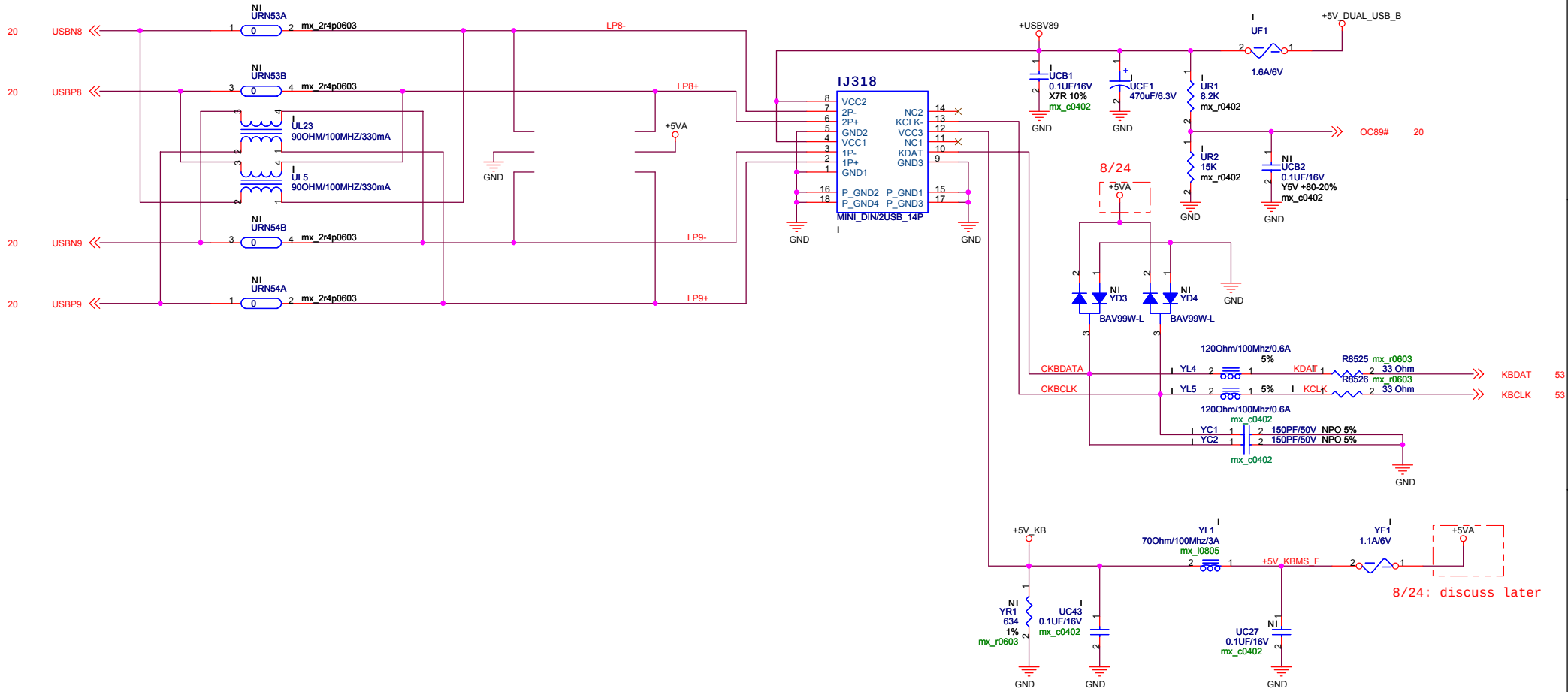
Back PS/2 with dual USB connector



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PS2+USB CONN	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
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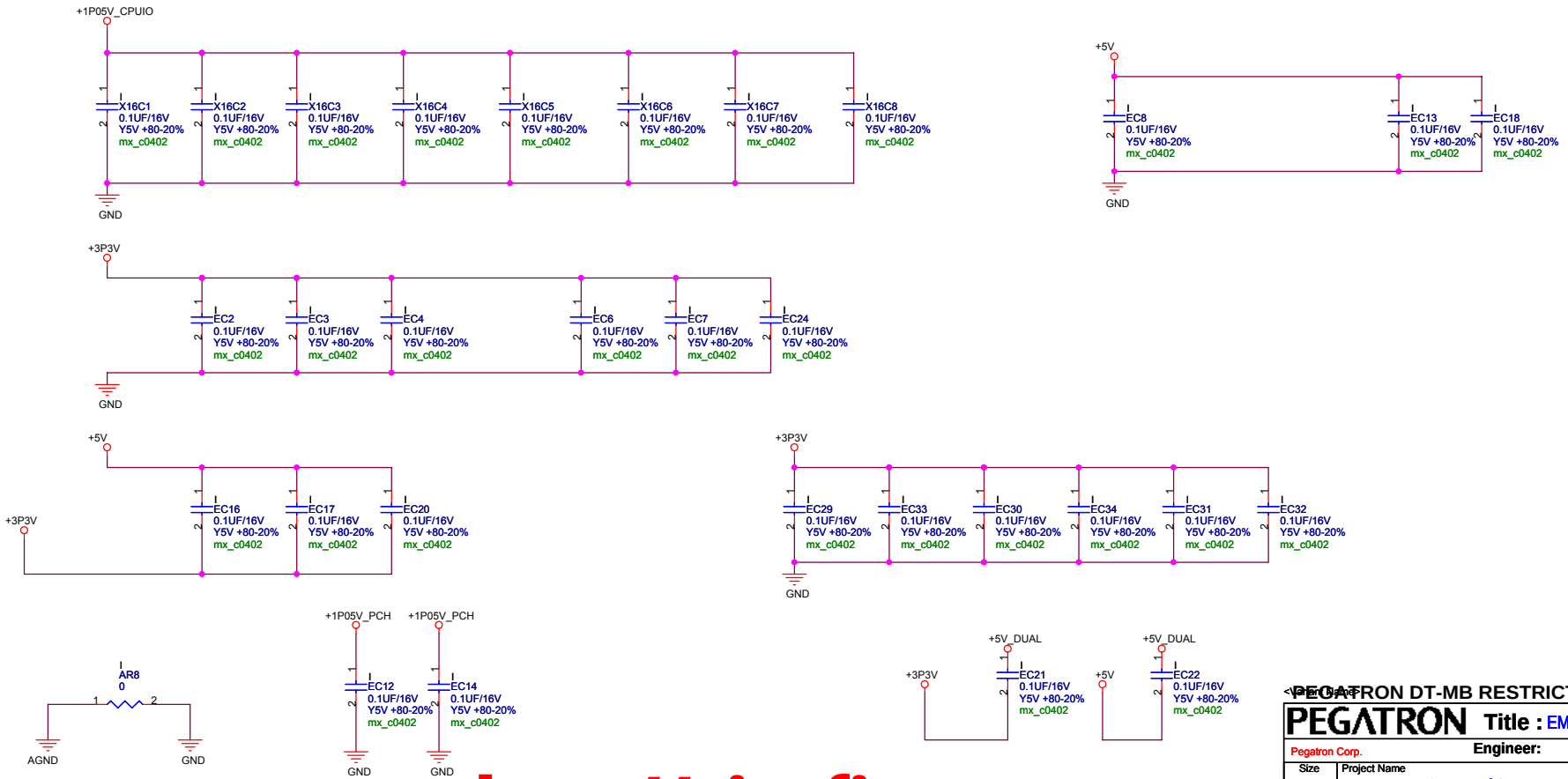
http://vinafix.vn

vinafix



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : EMI CAP

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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http://vinafix.vn

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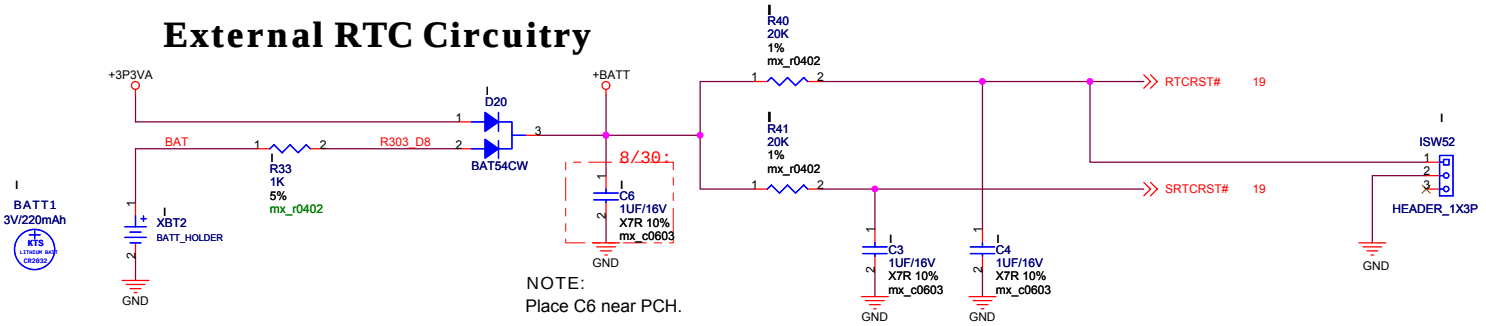
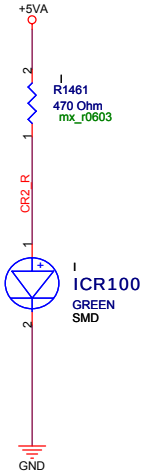
External RTC Circuitry



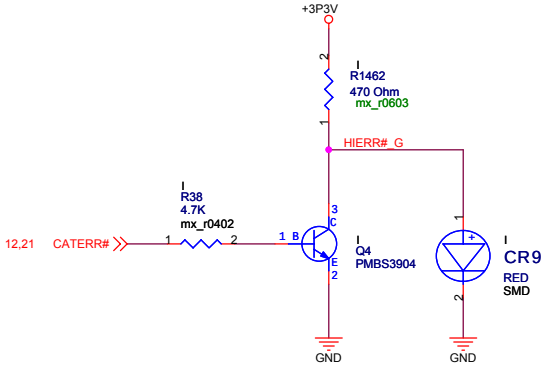
NOTE:
Place C6 near PCH.

Battery Socket

Standby LED

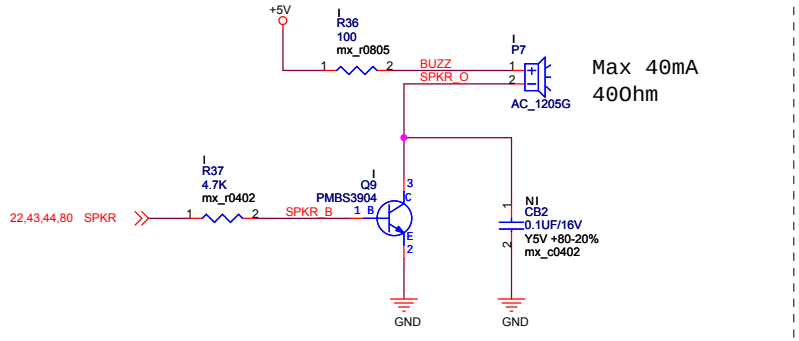


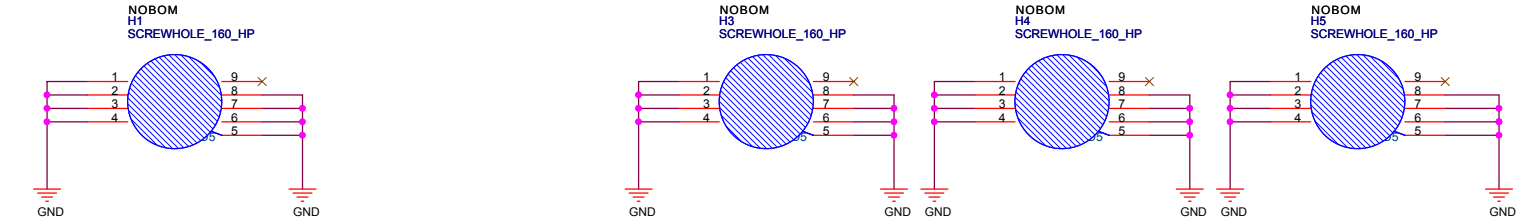
IERR# : RED



SPEAKER

I=5/(100+40)=35.7mA





ONLY FOR INTEL SCREW HOLE

LB1
1.375X0.25
WHITE
1D375X0D25_WHITE

LB2
1.0X0.187
WHITE
1D0X0D187_WHITE

AA# : 1510-03MQ0IN (S : 1510-03MR0IN)

Product code : 1510-06DE0IN

8/12 DIP

LB4
1.0X0.187
WHITE
1D0X0D187_WHITE

Product code : 1510-06DE0IN

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RTC/CMOS/SPKR

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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http://vinafix.vn

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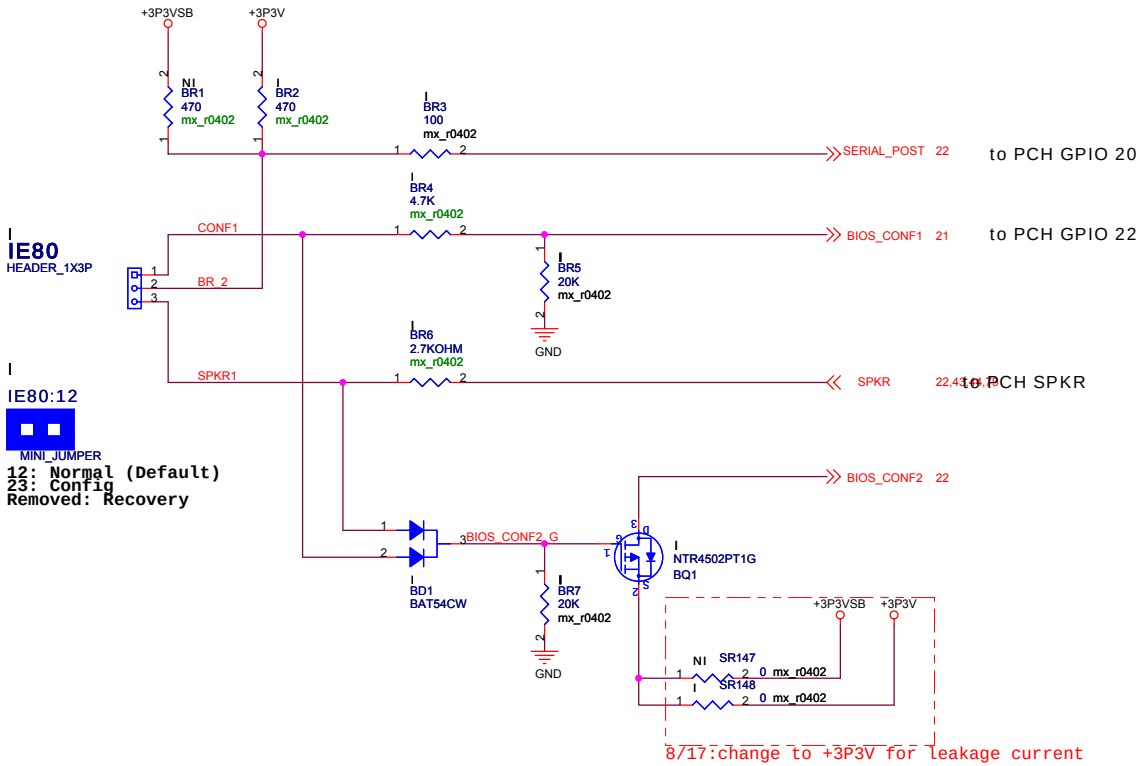
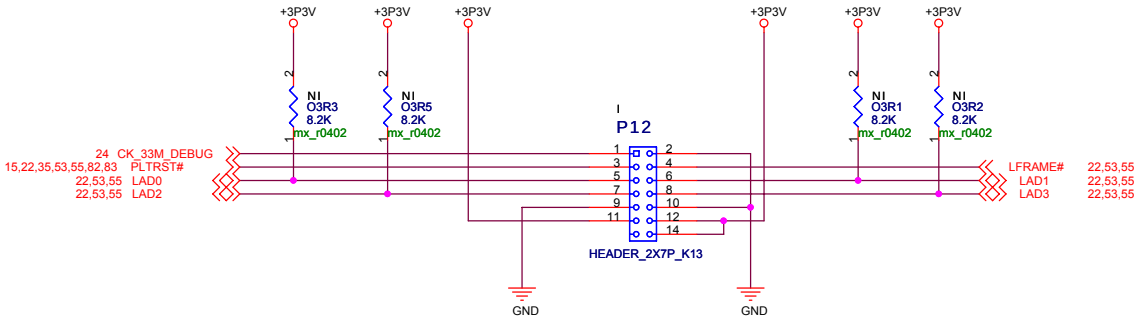
BIOS CONFIGURATION



LPC DEBUG PORT

08/13: NI LPC From Fab.B
(after PCI debug verified)



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BIOS and LPC header

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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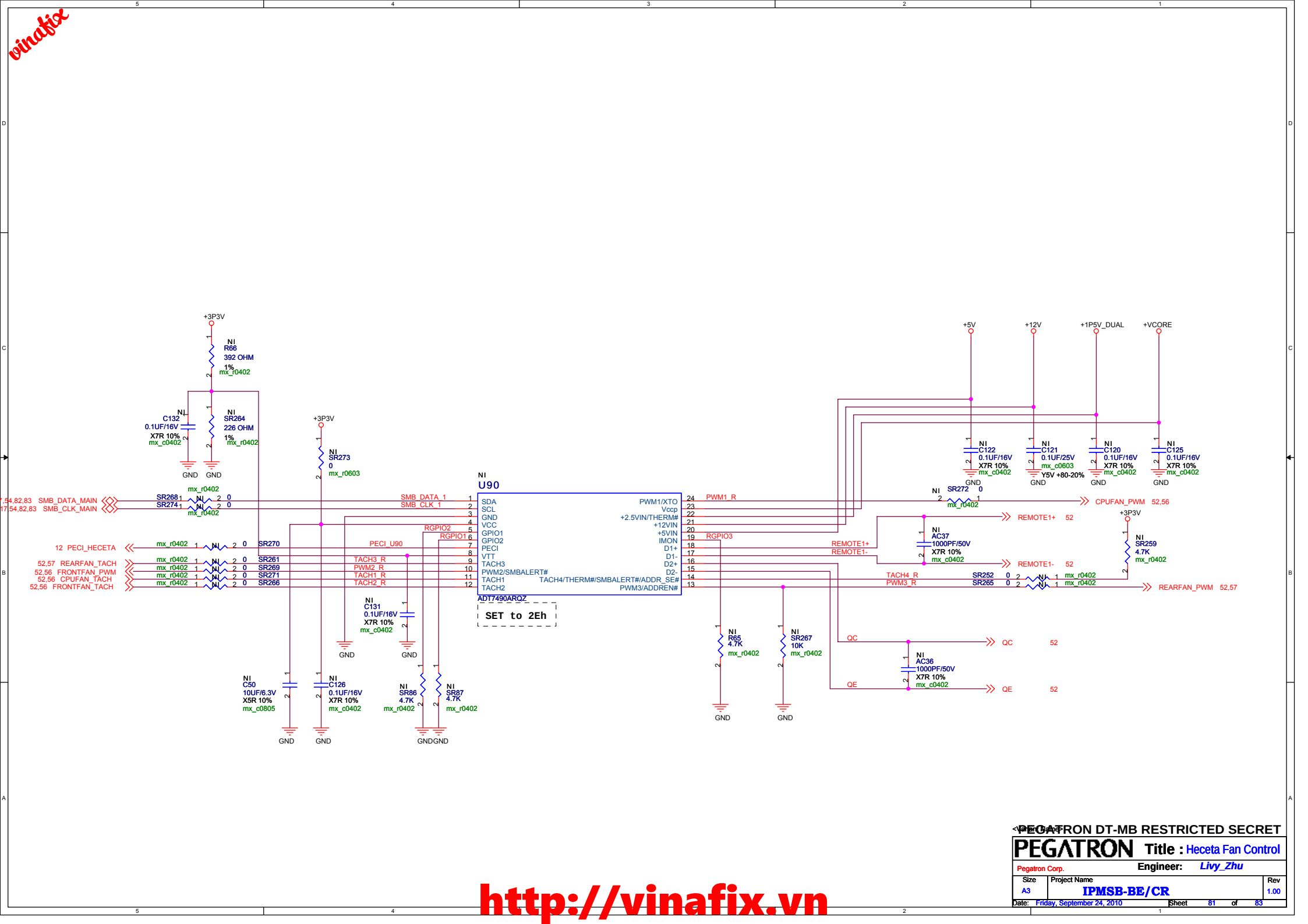

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Heceta Fan Control

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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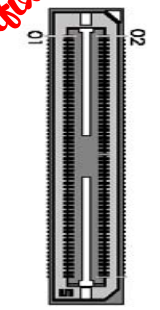
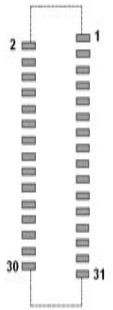
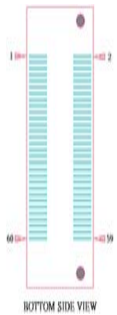
vinafix



TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



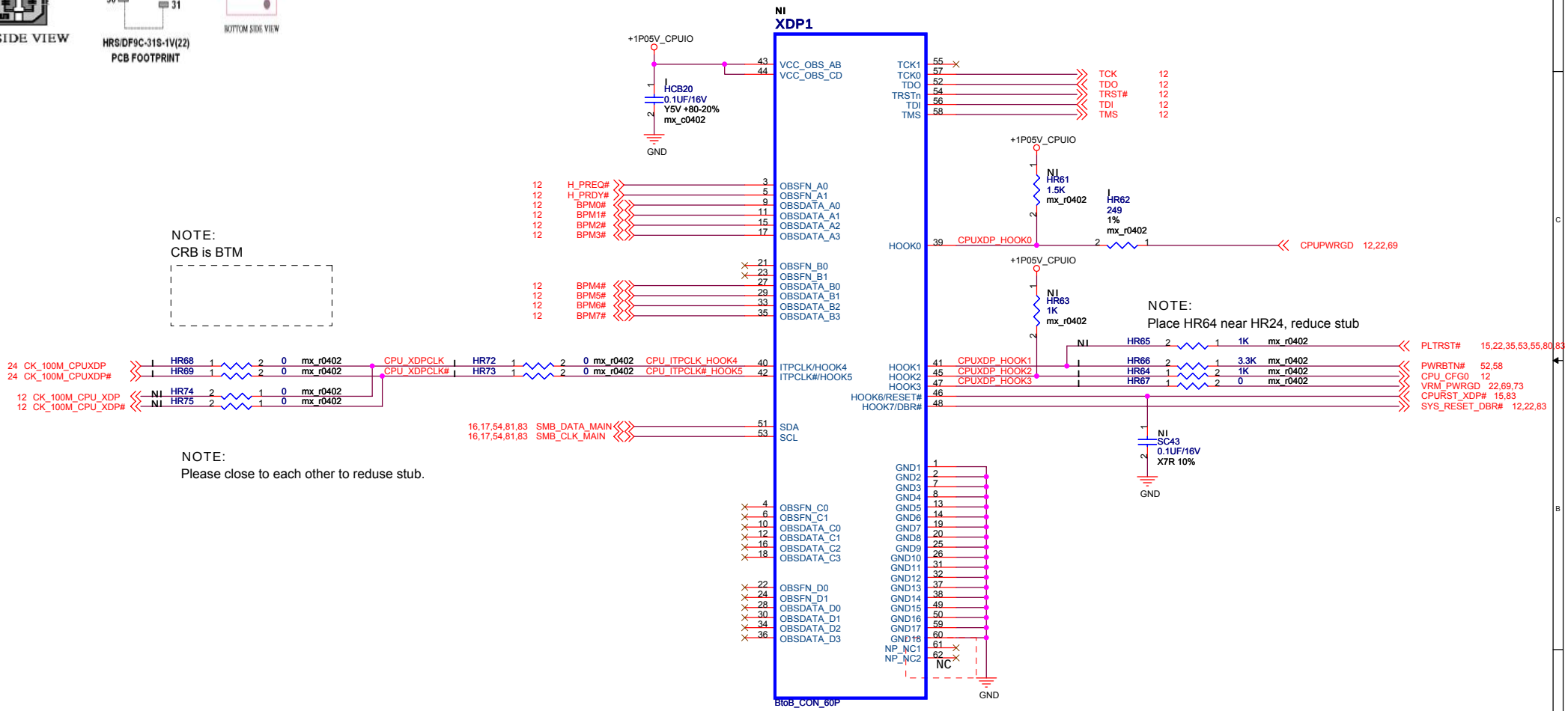
BOTTOM SIDE VIEW

INTEL CPU XDP DEBUG PORT

NOTE:
CRB is BTM

NOTE:
Please close to each other to reduse stub.

NOTE:
Place HR64 near HR24, reduce stub



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU XDP DEBUG

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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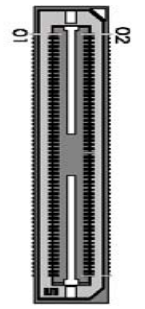
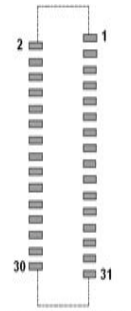
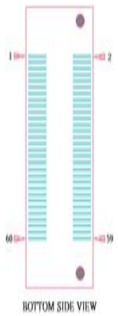
INTEL PCH XDP DEBUG PORT







NOTE:
Place strap resistors of TDO near to XDP connector, and TDI and TMS near to CPU.

NOTE:
Place SR214 near to source in order to avoid stub.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH XDP DEBUG

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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