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MS-7758

Intel -MahoBay plamform H77

ATX

Ver: 10(304.8x243.84)

CPU:

System Chipset:

IVY bridge LGA1155

Panther Point H77(CO-LAY Z77)

Onboard Chip:

HD Audio Codec:ALC892 colay 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UT501 3+1 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot * 1

SATA3.0 x2+SATA2.0 x4 (PCH)

PCI Express (X1) Slot * 2

USB2.0 *10

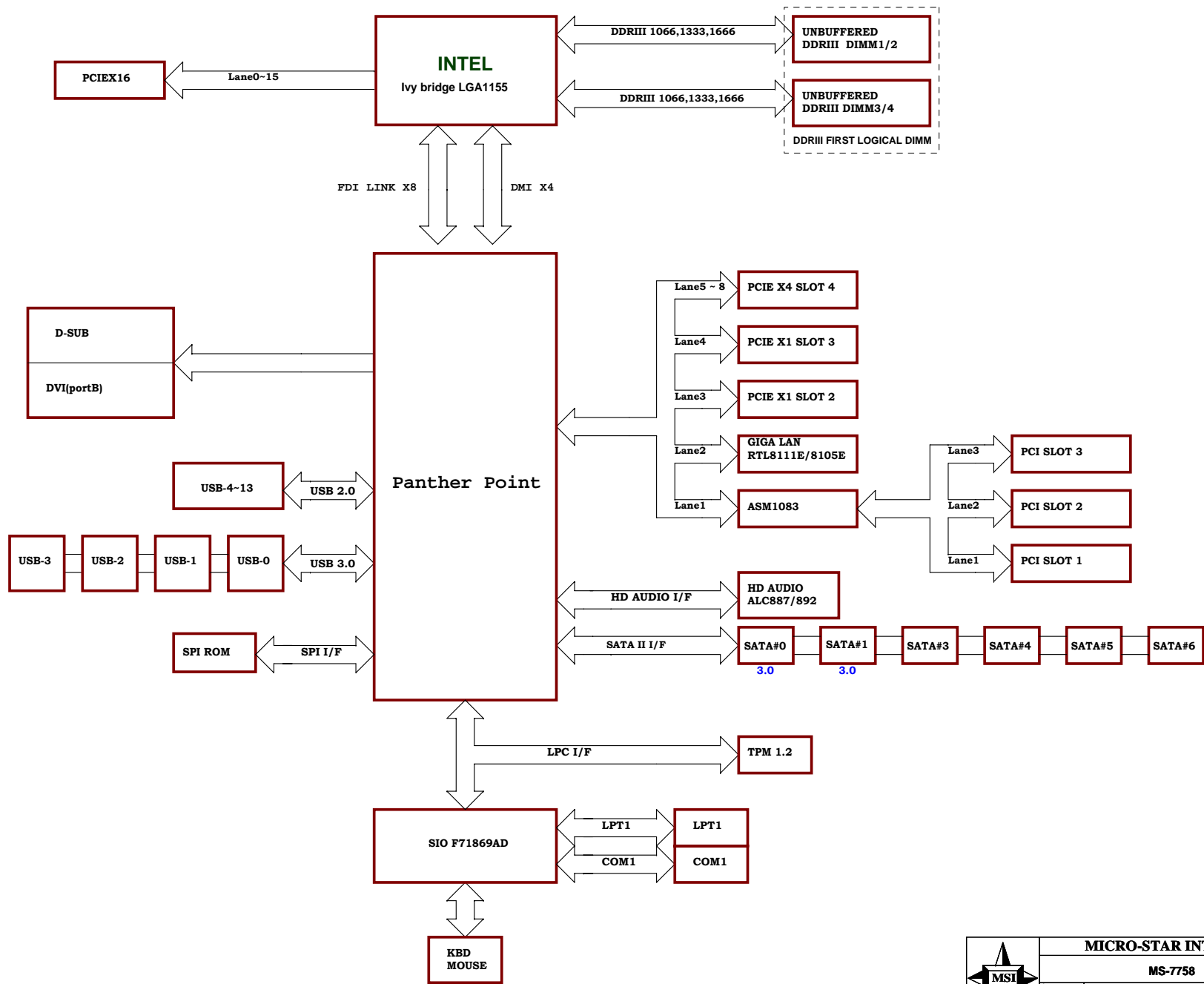
PCI Express (X4) Slot * 1

REAL USB3.0 *2

PCI Slot * 3

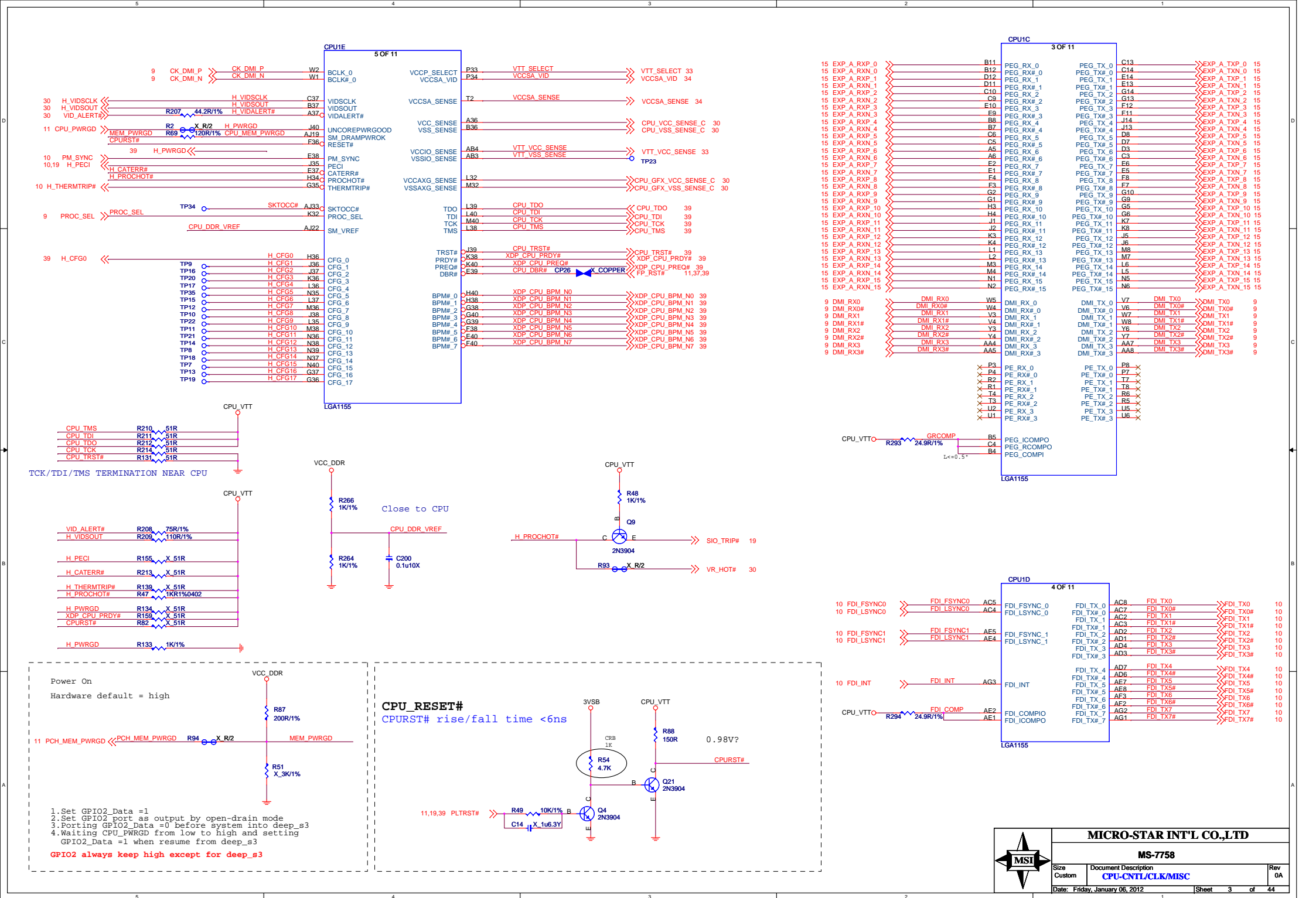
FRONT USB3.0 *2

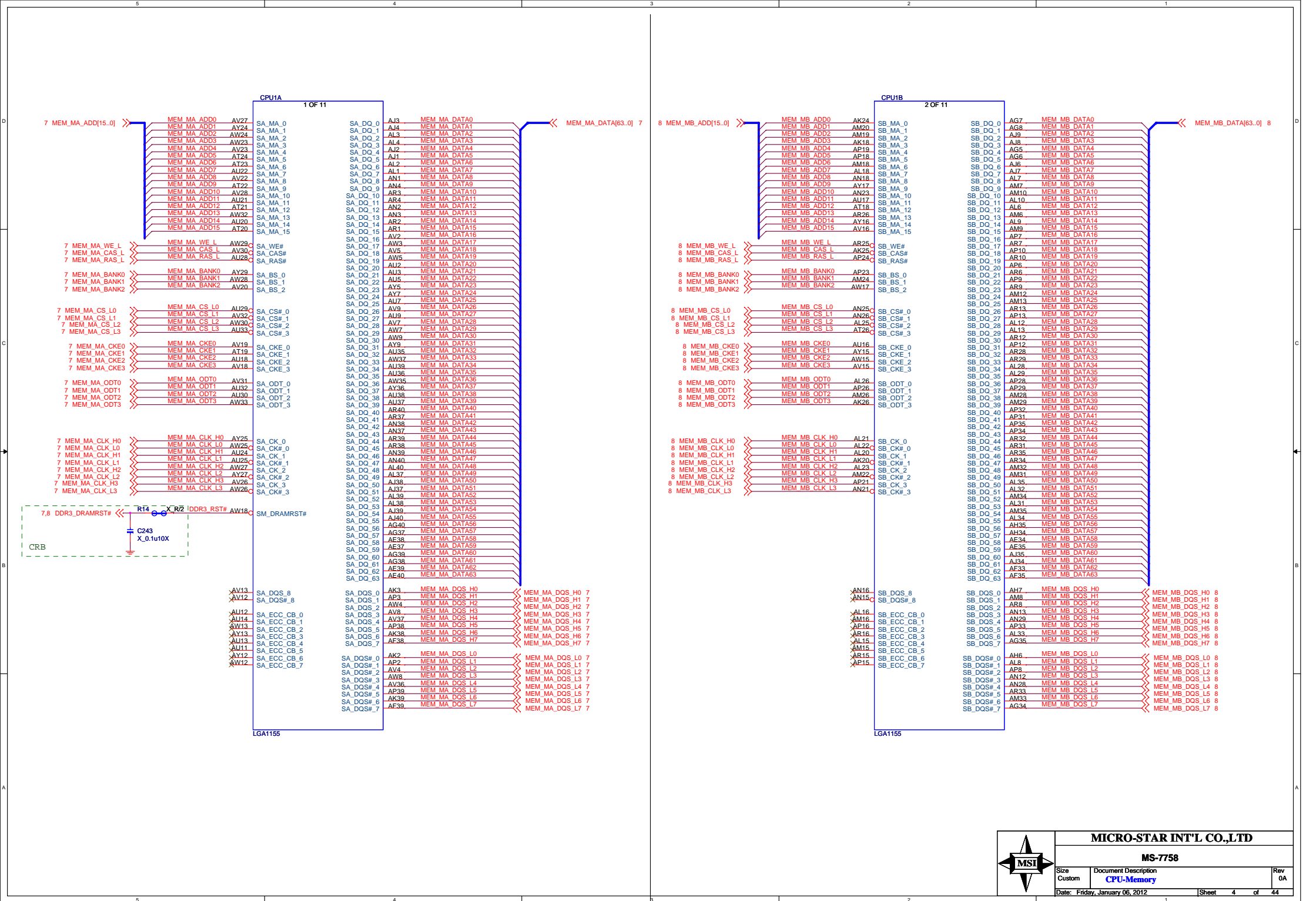
MS-7758 Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16
- PCIE X1
- PCI SLOT
- PCIE X16(X4)
- PCI SLOT
- PCI SLOT





CPU1F 6 OF 11	CPU1F 6 OF 11	CPU1F 6 OF 11
A12	VCC_001	VCC_082
A13	VCC_002	VCC_083
A14	VCC_003	VCC_084
A15	VCC_004	VCC_085
A16	VCC_005	VCC_086
A18	VCC_006	VCC_087
A24	VCC_007	VCC_088
A25	VCC_008	VCC_089
A27	VCC_009	VCC_090
A28	VCC_010	VCC_091
B15	VCC_011	VCC_092
B16	VCC_012	VCC_093
B18	VCC_013	VCC_094
B24	VCC_014	VCC_095
B25	VCC_015	VCC_096
B27	VCC_016	VCC_097
B28	VCC_017	VCC_098
B30	VCC_018	VCC_099
B31	VCC_019	VCC_100
B33	VCC_020	VCC_101
B34	VCC_021	VCC_102
C15	VCC_022	VCC_103
C16	VCC_023	VCC_104
C18	VCC_024	VCC_105
C19	VCC_025	VCC_106
C21	VCC_026	VCC_107
C22	VCC_027	VCC_108
C24	VCC_028	VCC_109
C25	VCC_029	VCC_110
C27	VCC_030	VCC_111
C28	VCC_031	VCC_112
C30	VCC_032	VCC_113
C31	VCC_033	VCC_114
C33	VCC_034	VCC_115
C34	VCC_035	VCC_116
C36	VCC_036	VCC_117
D13	VCC_037	VCC_118
D14	VCC_038	VCC_119
D15	VCC_039	VCC_120
D16	VCC_040	VCC_121
D18	VCC_041	VCC_122
D19	VCC_042	VCC_123
D21	VCC_043	VCC_124
D22	VCC_044	VCC_125
D24	VCC_045	VCC_126
D25	VCC_046	VCC_127
D27	VCC_047	VCC_128
D28	VCC_048	VCC_129
D30	VCC_049	VCC_130
D31	VCC_050	VCC_131
D33	VCC_051	VCC_132
D34	VCC_052	VCC_133
D35	VCC_053	VCC_134
E15	VCC_054	VCC_135
E16	VCC_055	VCC_136
E18	VCC_056	VCC_137
E19	VCC_057	VCC_138
E21	VCC_058	VCC_139
E22	VCC_059	VCC_140
E24	VCC_060	VCC_141
E25	VCC_061	VCC_142
E27	VCC_062	VCC_143
E28	VCC_063	VCC_144
E30	VCC_064	VCC_145
E31	VCC_065	VCC_146
E33	VCC_066	VCC_147
E34	VCC_067	VCC_148
E35	VCC_068	VCC_149
F15	VCC_069	VCC_150
F18	VCC_070	VCC_151
F19	VCC_071	VCC_152
F21	VCC_072	VCC_153
F22	VCC_073	VCC_154
F24	VCC_074	VCC_155
F25	VCC_075	VCC_156
F27	VCC_076	VCC_157
F28	VCC_077	VCC_158
F30	VCC_078	VCC_159
F31	VCC_079	VCC_160
	VCC_080	VCC_161
	VCC_081	

(1.05V / 1.00V)

CPU1H 8 OF 11	CPU1H 8 OF 11	CPU1H 8 OF 11
A11	VCCIO_01	VDDQ_01
A7	VCCIO_02	VDDQ_02
AA3	VCCIO_03	VDDQ_03
AB8	VCCIO_04	VDDQ_04
AF8	VCCIO_05	VDDQ_05
AG33	VCCIO_06	VDDQ_06
AJ16	VCCIO_07	VDDQ_07
AJ17	VCCIO_08	VDDQ_08
AJ26	VCCIO_09	VDDQ_09
AJ28	VCCIO_10	VDDQ_10
AJ32	VCCIO_11	VDDQ_11
AK15	VCCIO_12	VDDQ_12
AK17	VCCIO_13	VDDQ_13
AK19	VCCIO_14	VDDQ_14
AK21	VCCIO_15	VDDQ_15
AK23	VCCIO_16	VDDQ_16
AK27	VCCIO_17	VDDQ_17
AK29	VCCIO_18	VDDQ_18
AK30	VCCIO_19	VDDQ_19
B9	VCCIO_20	VDDQ_20
D10	VCCIO_21	VDDQ_21
D6	VCCIO_22	VDDQ_22
E3	VCCIO_23	VDDQ_23
F4	VCCIO_24	VDDQ_24
G3	VCCIO_25	VDDQ_25
G4	VCCIO_26	VDDQ_26
H27	VCCIO_27	VDDQ_27
H28	VCCIO_28	VDDQ_28
H30	VCCIO_29	VDDQ_29
H31	VCCIO_30	VDDQ_30
H32	VCCIO_31	VDDQ_31
H33	VCCIO_32	VDDQ_32
H34	VCCIO_33	VDDQ_33
I12	VCCIO_34	VDDQ_34
I15	VCCIO_35	VDDQ_35
I16	VCCIO_36	VDDQ_36
I18	VCCIO_37	VDDQ_37
I19	VCCIO_38	VDDQ_38
J21	VCCIO_39	VDDQ_39
J25	VCCIO_40	VDDQ_40
J27	VCCIO_41	VDDQ_41
J28	VCCIO_42	VDDQ_42
J30	VCCIO_43	VDDQ_43
K15	VCCIO_44	VDDQ_44
K16	VCCIO_45	VDDQ_45
K18	VCCIO_46	VDDQ_46
K19	VCCIO_47	VDDQ_47
K21	VCCIO_48	VDDQ_48
K22	VCCIO_49	VDDQ_49
K24	VCCIO_50	VDDQ_50
K25	VCCIO_51	VDDQ_51
K27	VCCIO_52	VDDQ_52
K30	VCCIO_53	VDDQ_53
L13	VCCIO_54	VDDQ_54
L14	VCCIO_55	VDDQ_55
L15	VCCIO_56	VDDQ_56
L16	VCCIO_57	VDDQ_57
L18	VCCIO_58	VDDQ_58
L19	VCCIO_59	VDDQ_59
L21	VCCIO_60	VDDQ_60
L22	VCCIO_61	VDDQ_61
L24	VCCIO_62	VDDQ_62
L25	VCCIO_63	VDDQ_63
L27	VCCIO_64	VDDQ_64
L28	VCCIO_65	VDDQ_65
L30	VCCIO_66	VDDQ_66
M14	VCCIO_67	VDDQ_67
M15	VCCIO_68	VDDQ_68
M16	VCCIO_69	VDDQ_69
M19	VCCIO_70	VDDQ_70
M21	VCCIO_71	VDDQ_71
M22	VCCIO_72	VDDQ_72
M24	VCCIO_73	VDDQ_73
M25	VCCIO_74	VDDQ_74
M27	VCCIO_75	VDDQ_75
M28	VCCIO_76	VDDQ_76
M30	VCCIO_77	VDDQ_77

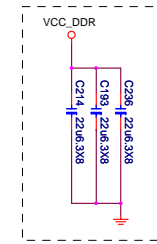
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

(0.925V / 0.85V)

CPU1G 7 OF 11	CPU1G 7 OF 11	CPU1G 7 OF 11
AB33	VCCAXG_01	VCCAXG_23
AB34	VCCAXG_02	VCCAXG_24
AB35	VCCAXG_03	VCCAXG_25
AB36	VCCAXG_04	VCCAXG_26
AB37	VCCAXG_05	VCCAXG_27
AB38	VCCAXG_06	VCCAXG_28
AB39	VCCAXG_07	VCCAXG_29
AB40	VCCAXG_08	VCCAXG_30
AC33	VCCAXG_09	VCCAXG_31
AC34	VCCAXG_10	VCCAXG_32
AC35	VCCAXG_11	VCCAXG_33
AU23	VCCAXG_12	VCCAXG_34
AU27	VCCAXG_13	VCCAXG_35
AR23	VCCAXG_14	VCCAXG_36
AR24	VCCAXG_15	VCCAXG_37
AU19	VCCAXG_16	VCCAXG_38
AU23	VCCAXG_17	VCCAXG_39
AV25	VCCAXG_18	VCCAXG_40
AV29	VCCAXG_19	VCCAXG_41
AV33	VCCAXG_20	VCCAXG_42
AW31	VCCAXG_21	VCCAXG_43
AY23	VCCAXG_22	VCCAXG_44
AY26		
AY28		

+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



+CPU_SA Decoupling

Backside



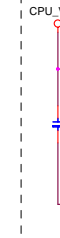
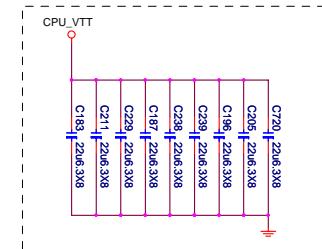
+VCC1_8 Decoupling

Backside



+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

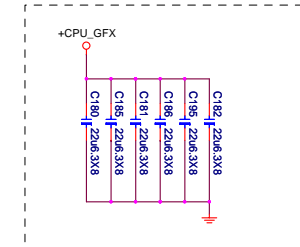


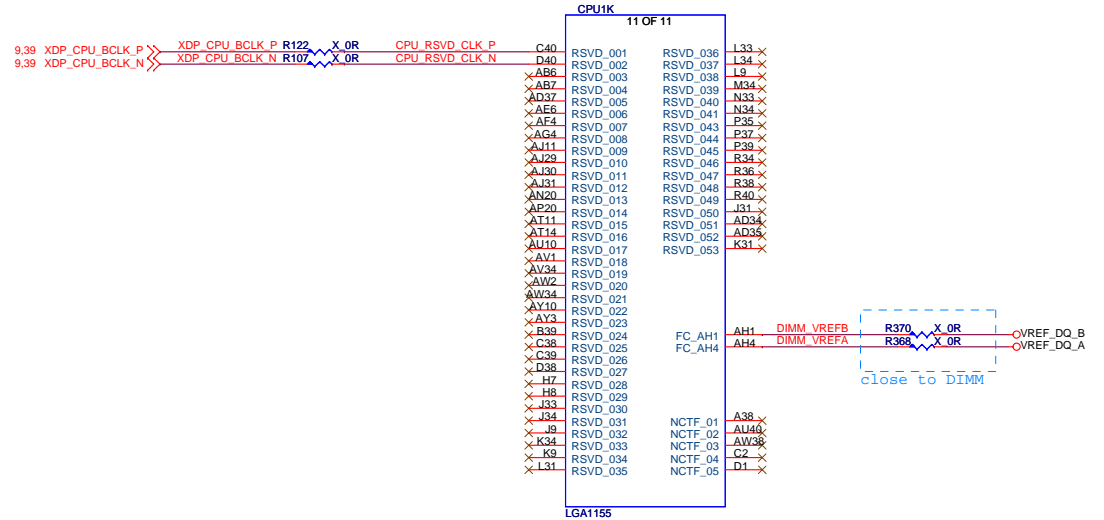
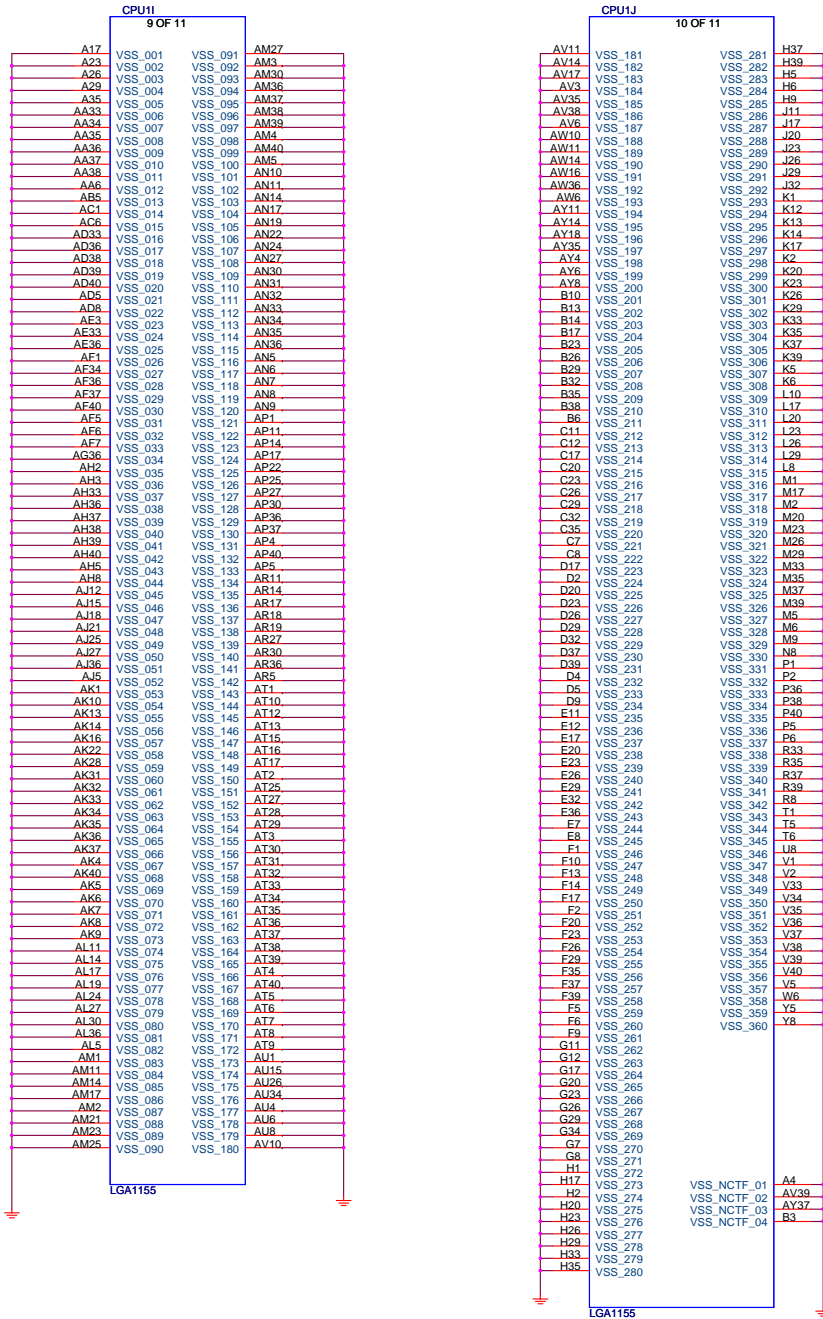
Backside



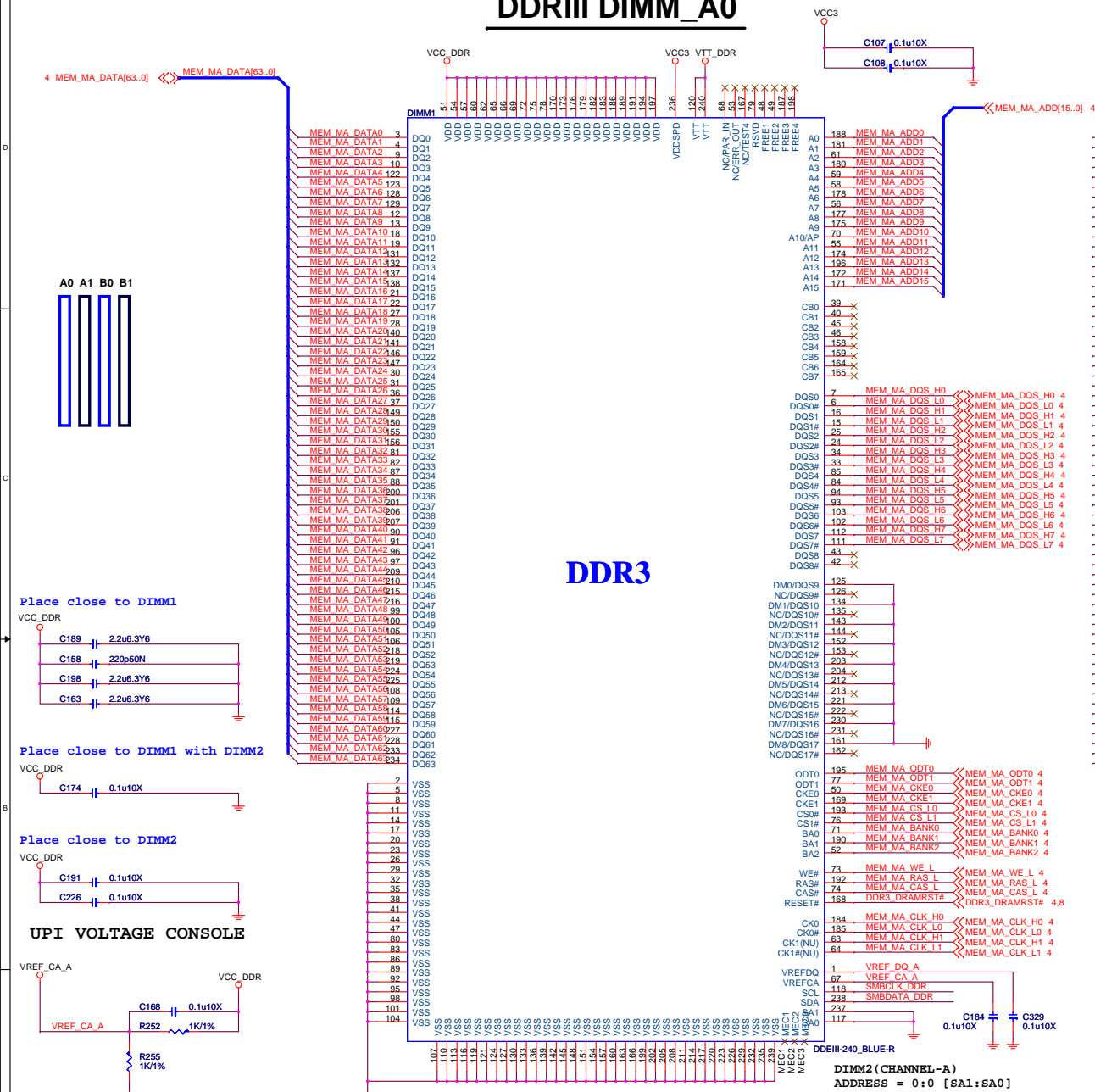
+CPU GFX Decoupling

CPU SOCKET CAVITY CAPS



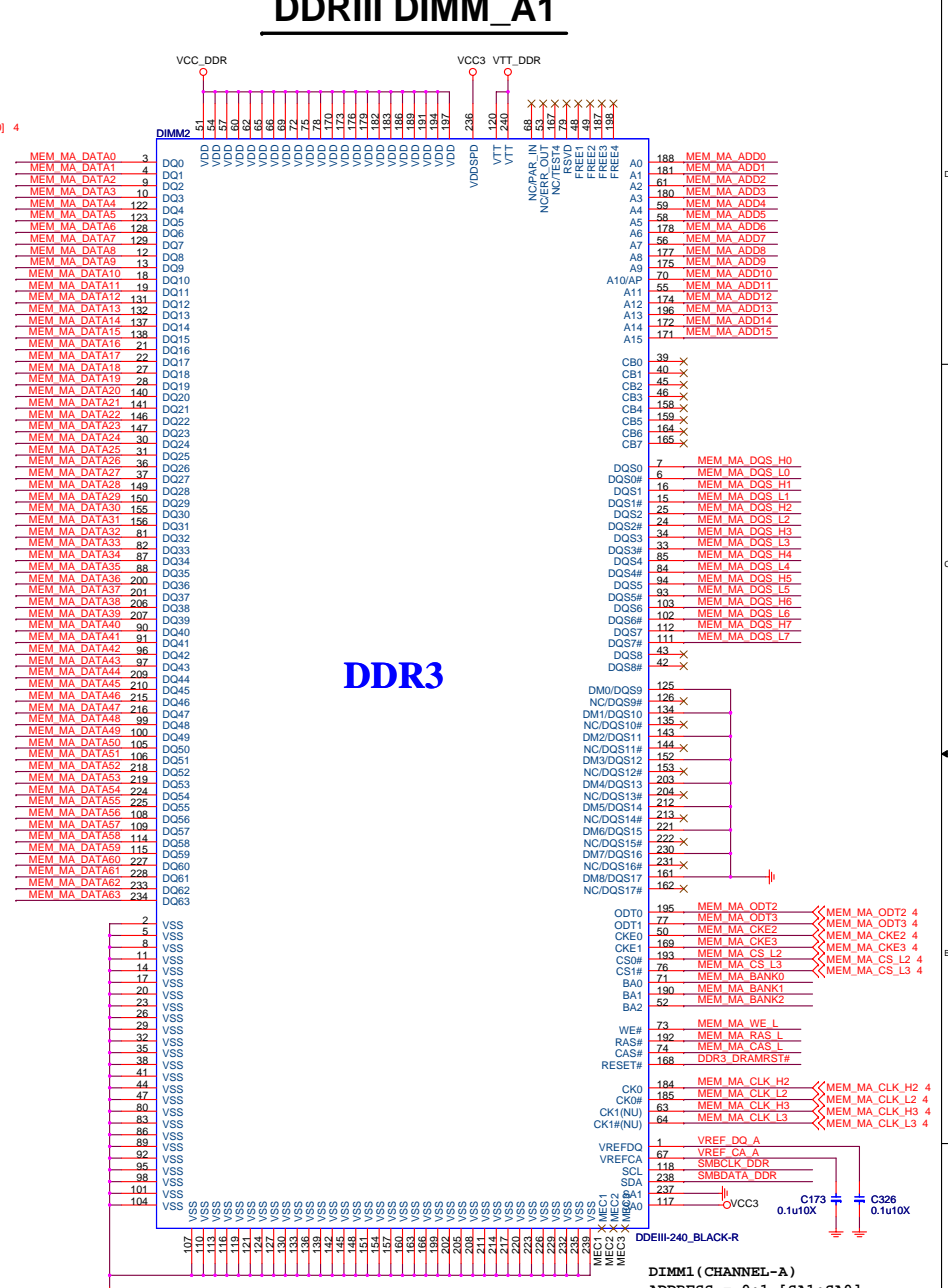


DDRIII DIMM_A0



DDR3

DDRIII DIMM_A1



DDR3

DIMM1 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

MICRO-STAR INT'L CO.,LTD

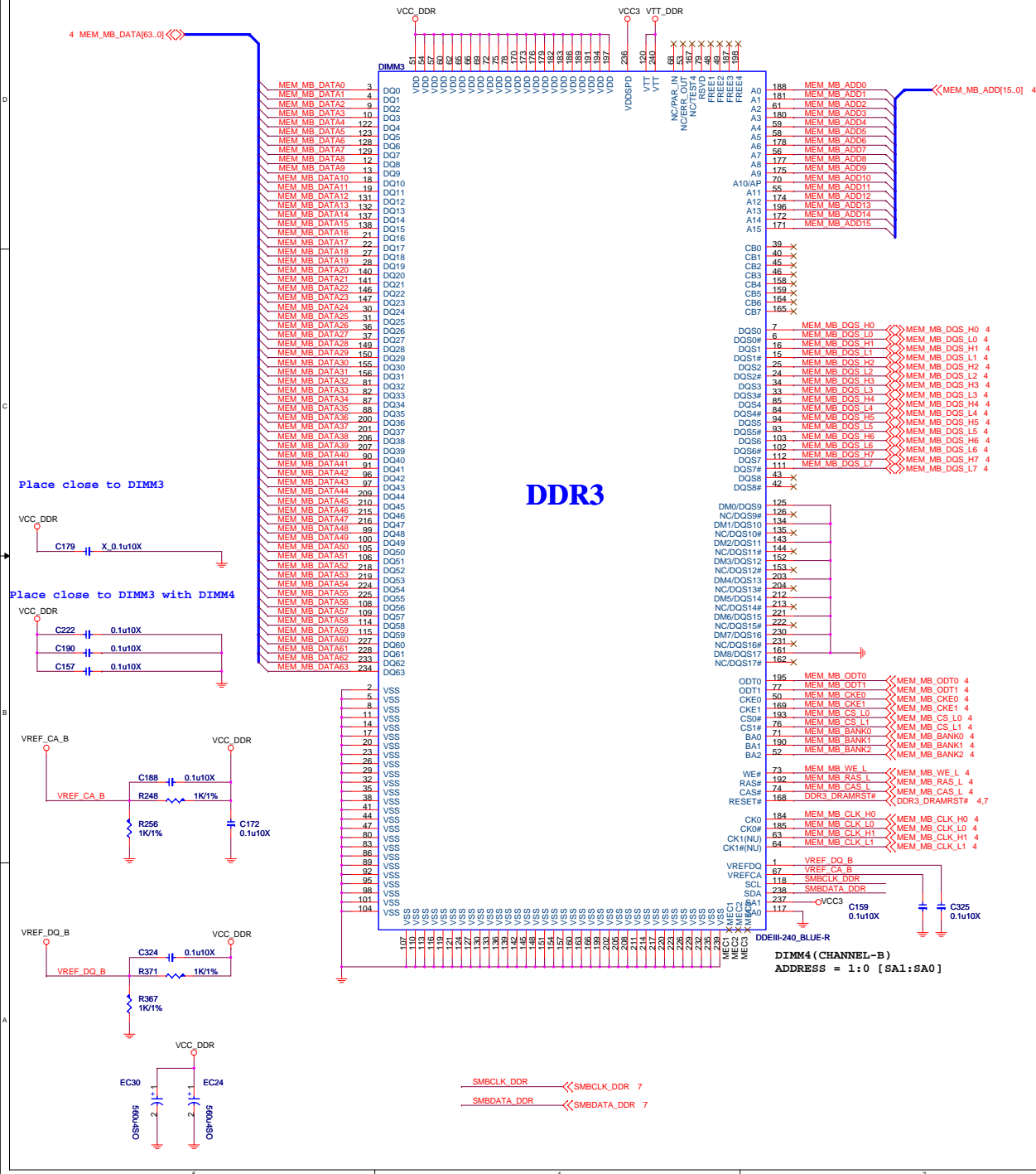
MS-7758

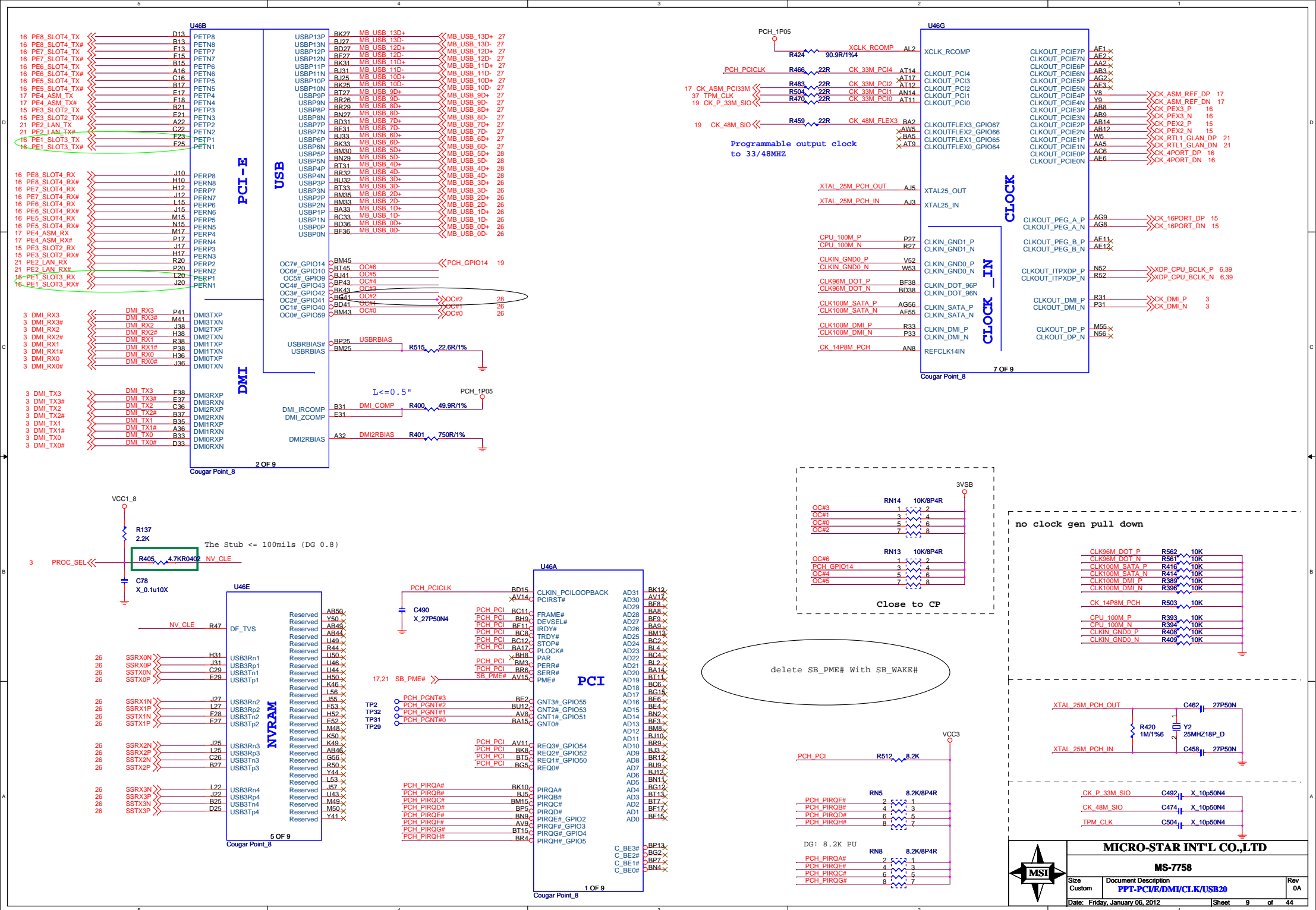
Size	Document Description
Custom	DDR3 Chanel-A DIMM1/2

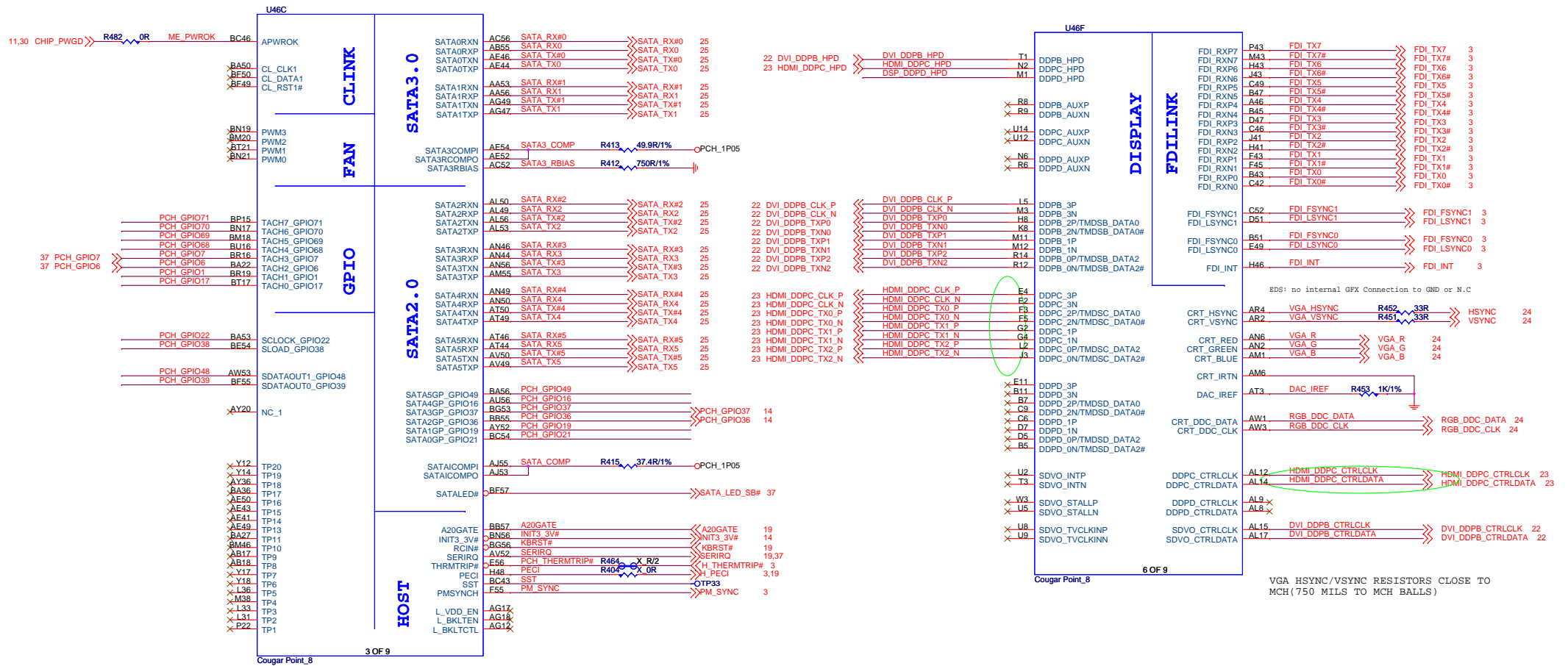
Rev
0A

DDR3 DIMM_B0

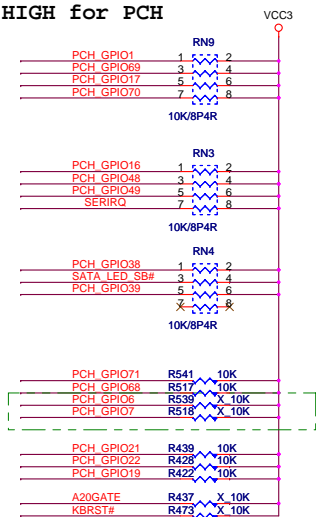
DDR3 DIMM_B1







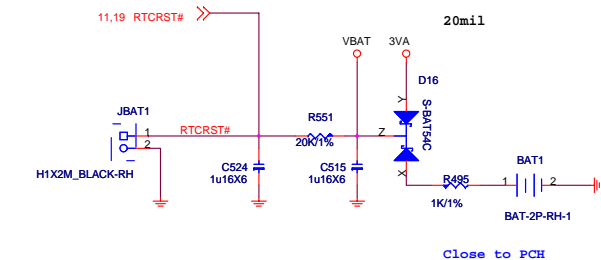
Pull HIGH for PCH



RTC and CLR_CMOS

Clear CMOS

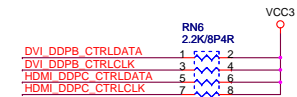
CMOS CLEAR JUMPER	
1-2	Clear CMOS



No Display port(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



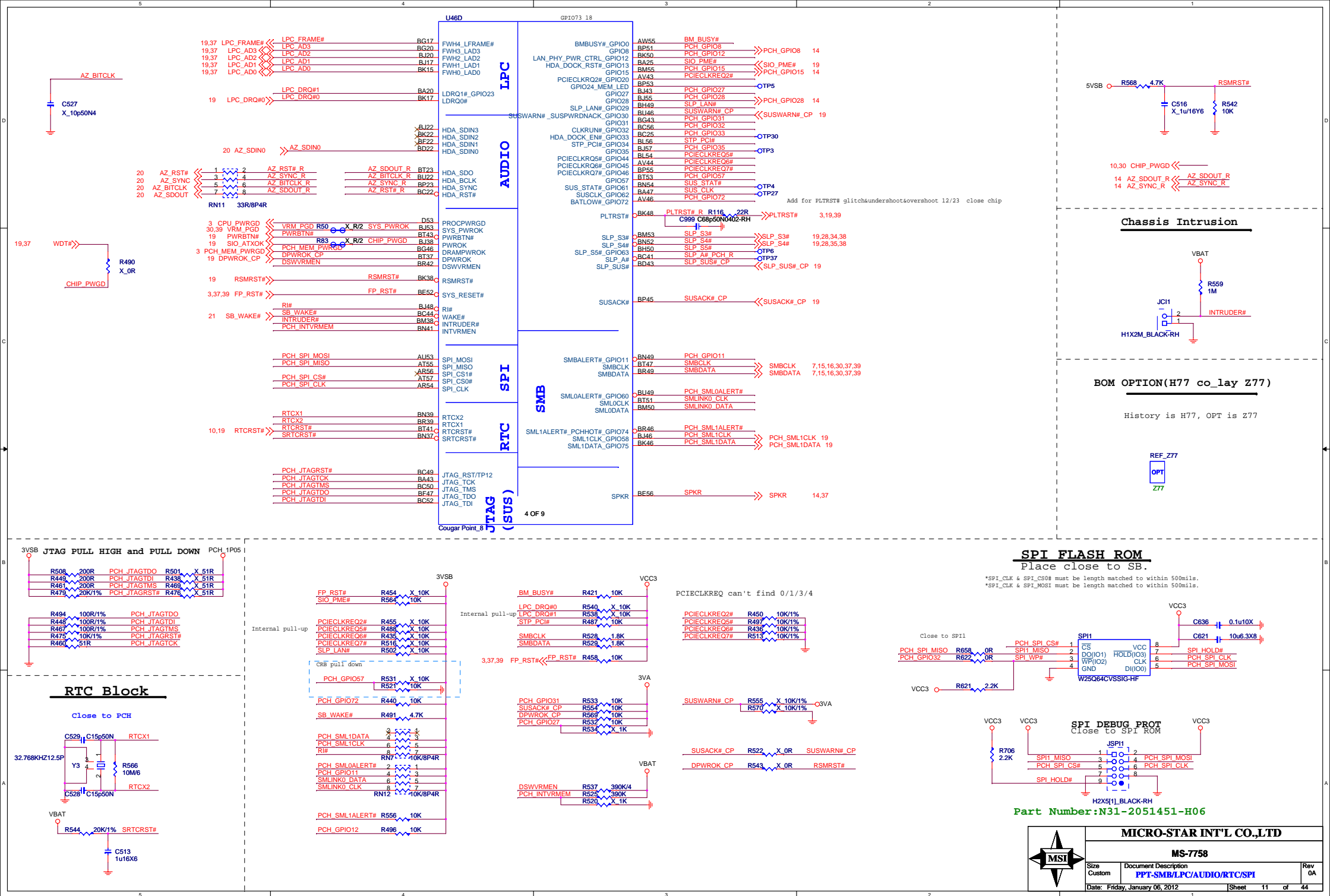
Close to PCH within 250 mils.

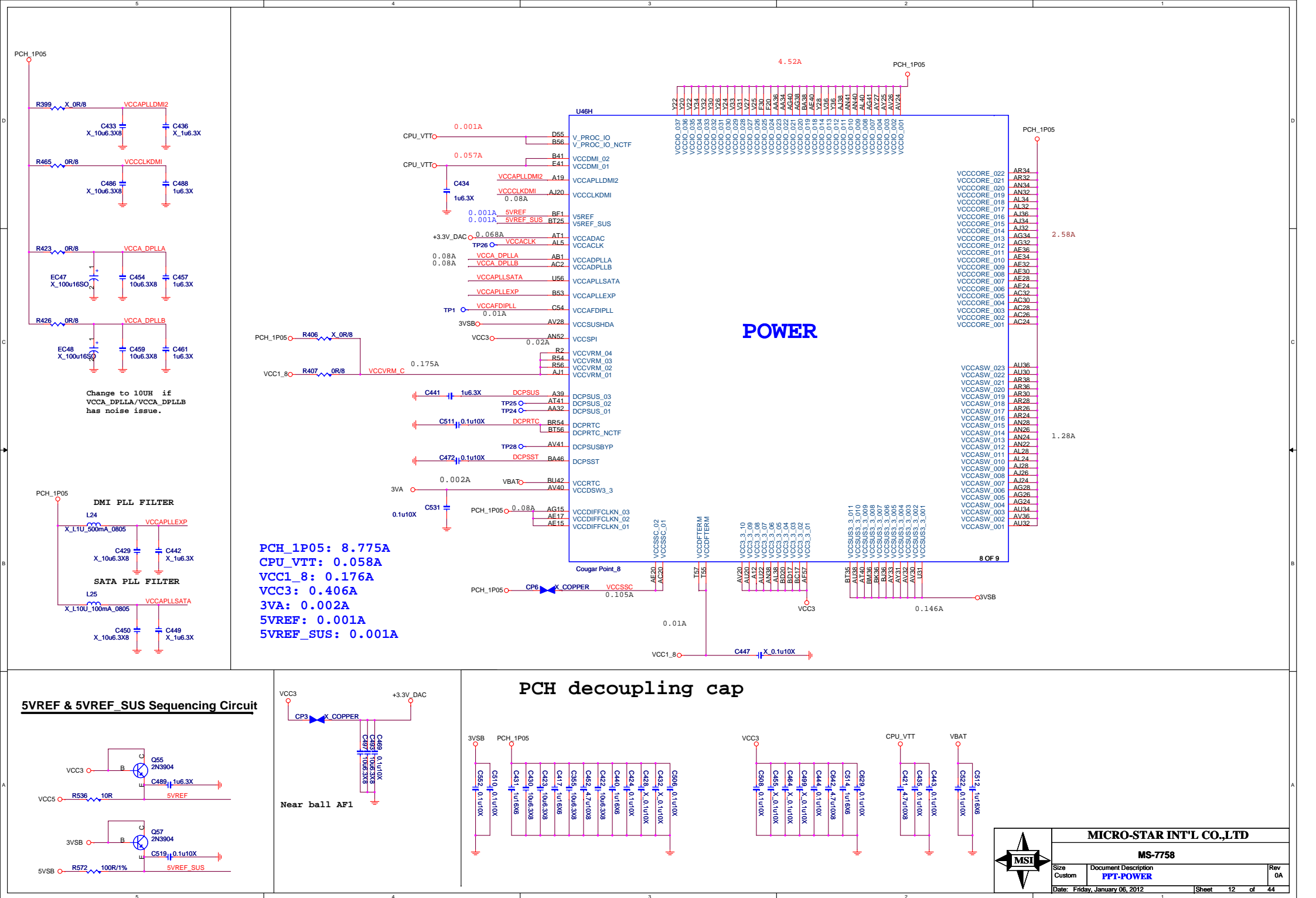


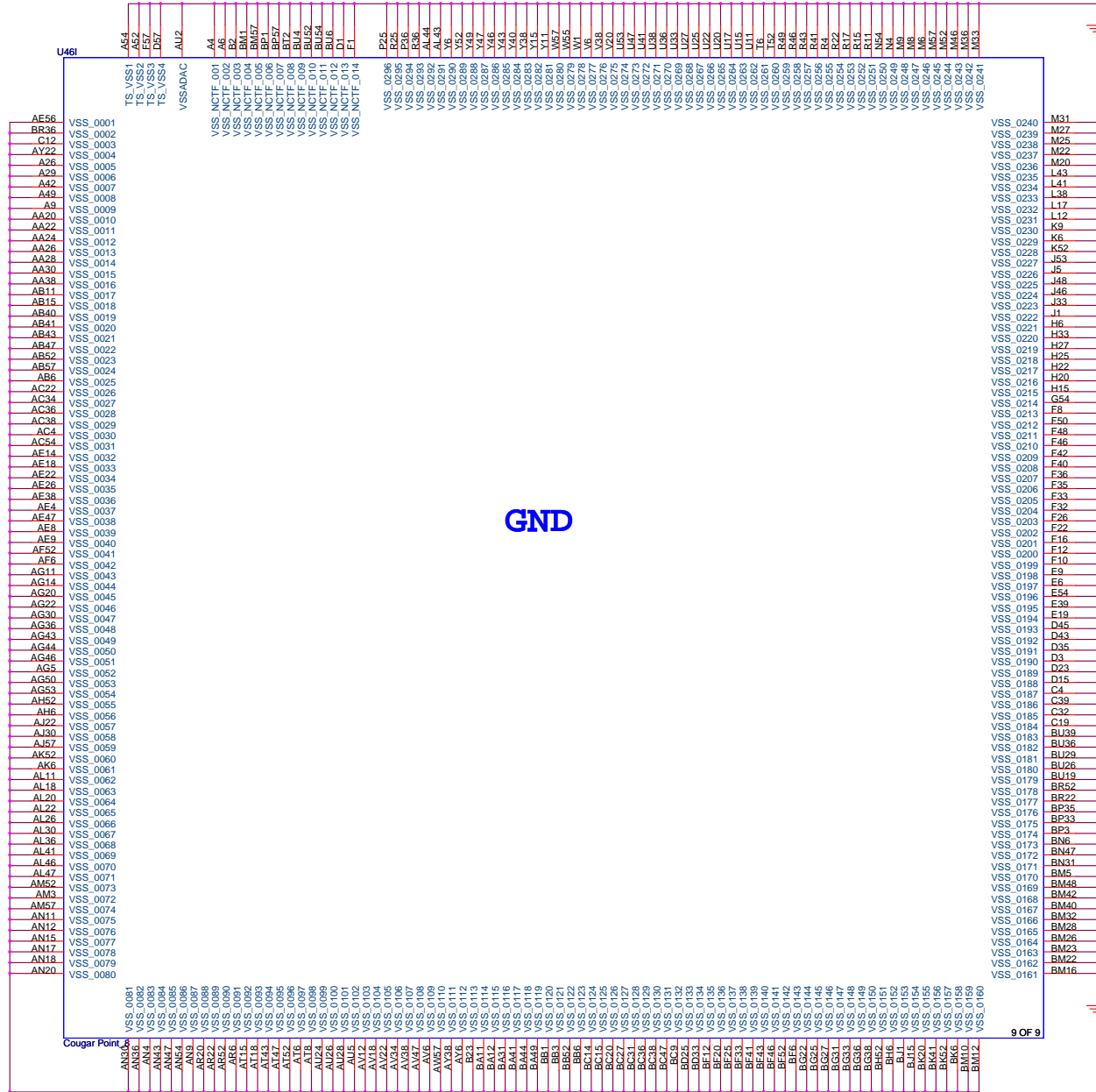
MICRO-STAR INT'L CO.,LTD

MS-7758

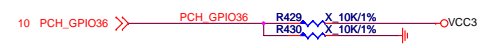
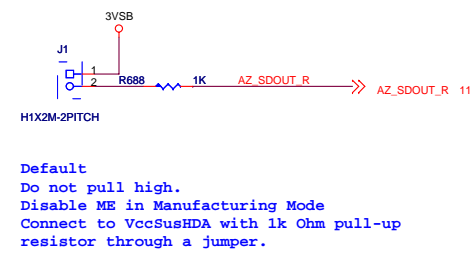
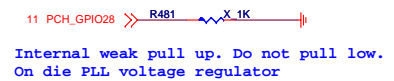
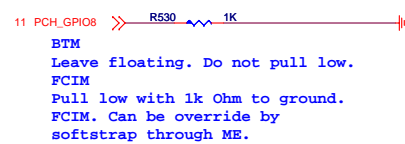
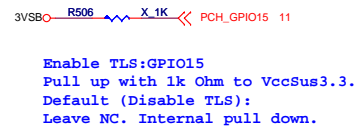
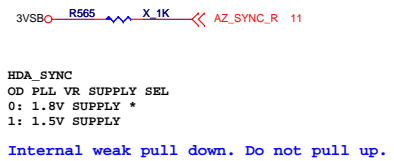
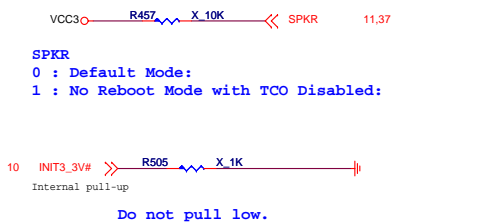
Size	Document Description	Rev
Custom	PPT-SATA/HOST/GPIO/VGA/CCMOS	0A
Date: Friday, January 06, 2012	Sheet 10 of 44	







PCH Straps

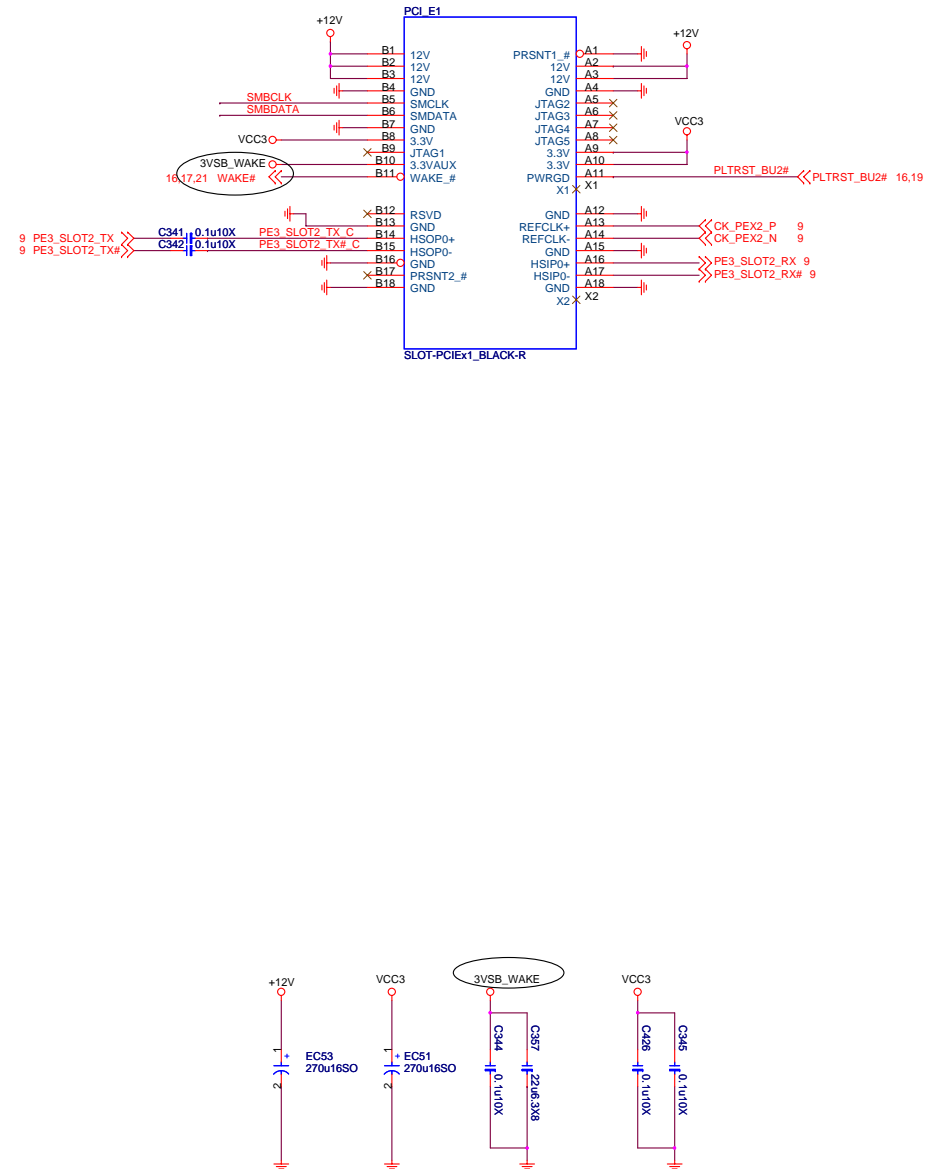


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



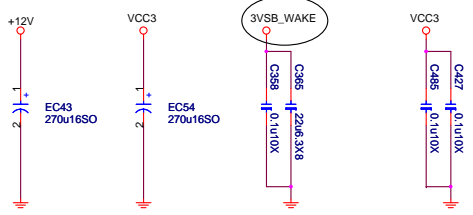
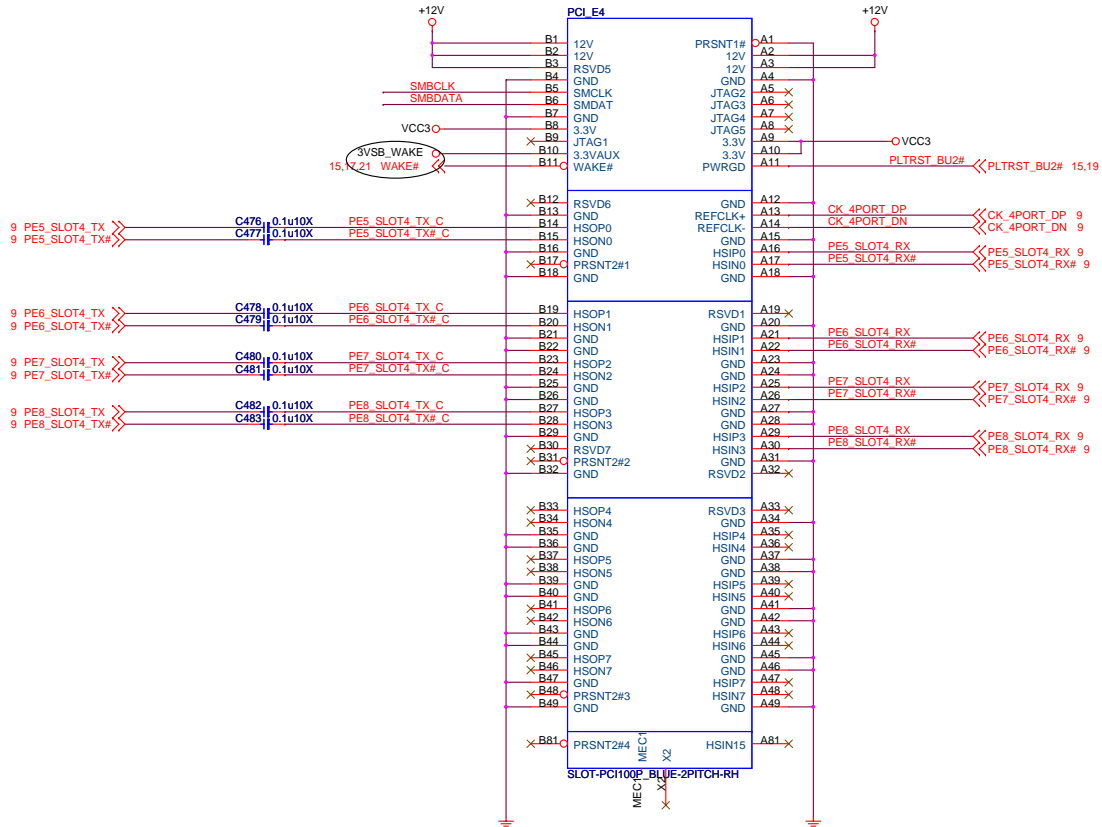
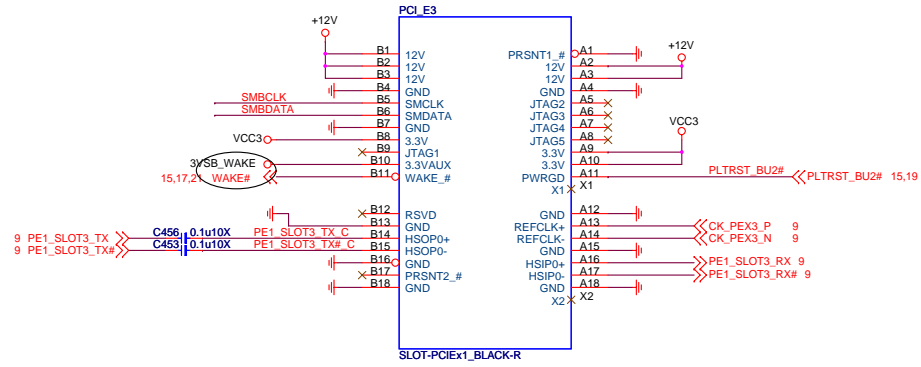
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

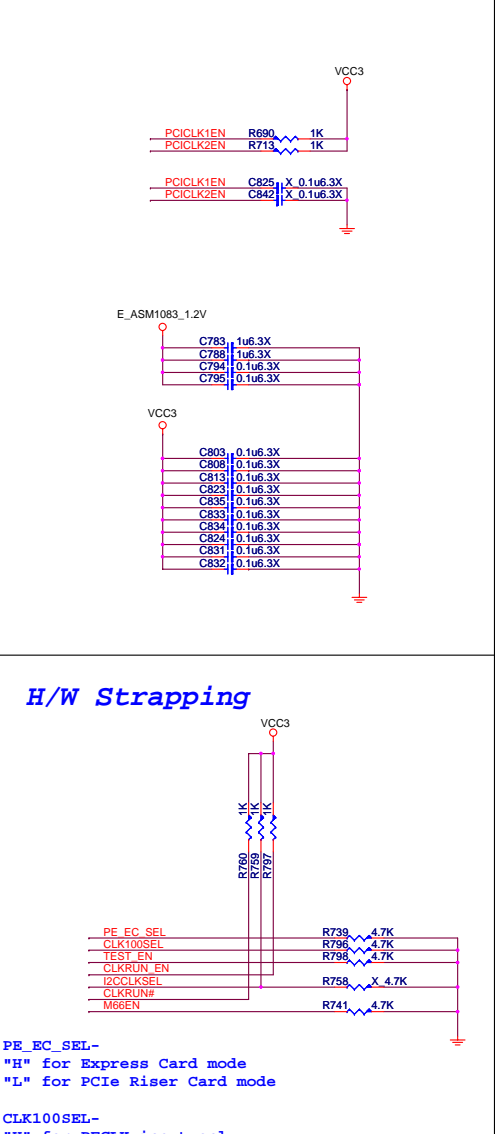
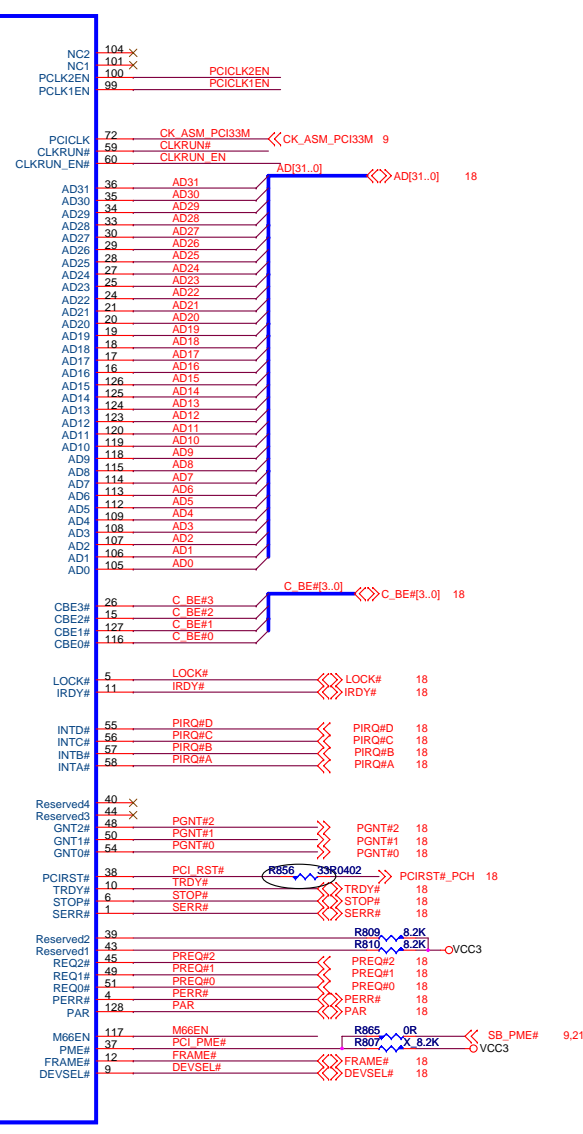
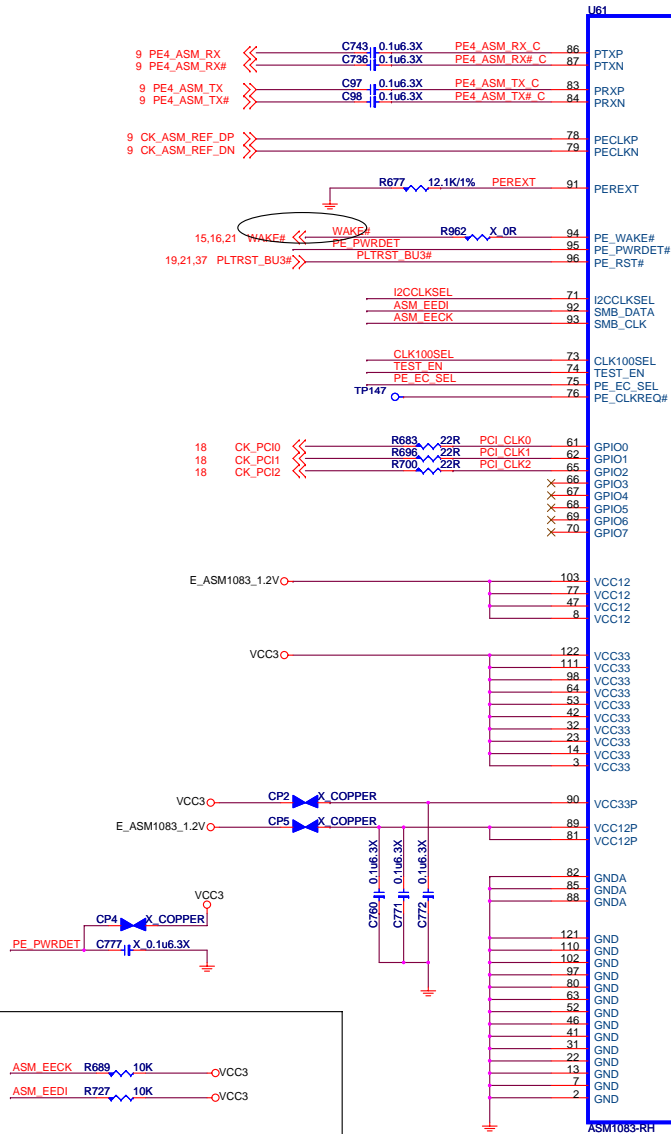
7,11,16,30,37,39 SMBCLK
7,11,16,30,37,39 SMBDATA

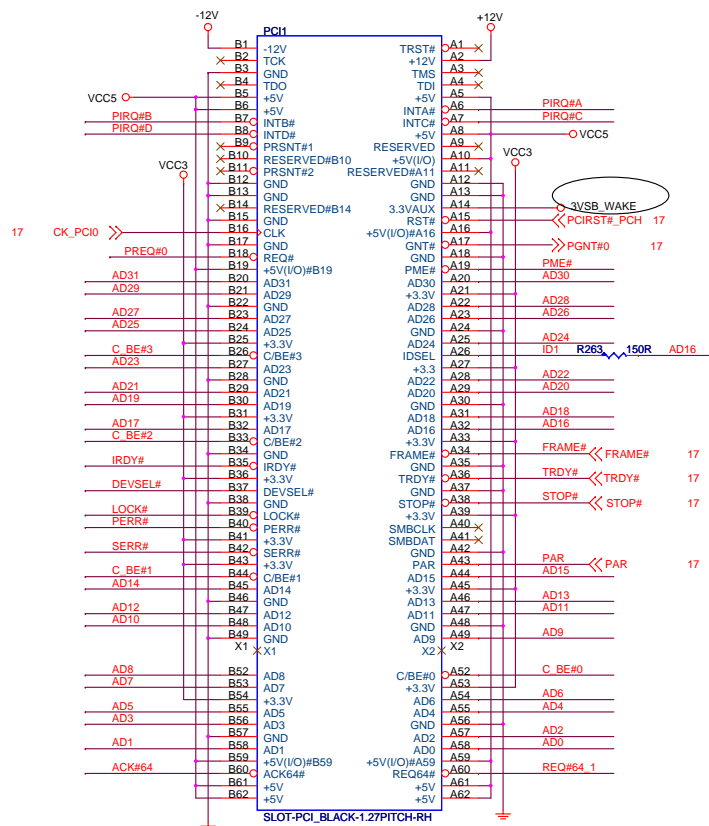


7,11,15,30,37,39 SMBCLK SMBCLK
7,11,15,30,37,39 SMBDATA SMBDATA

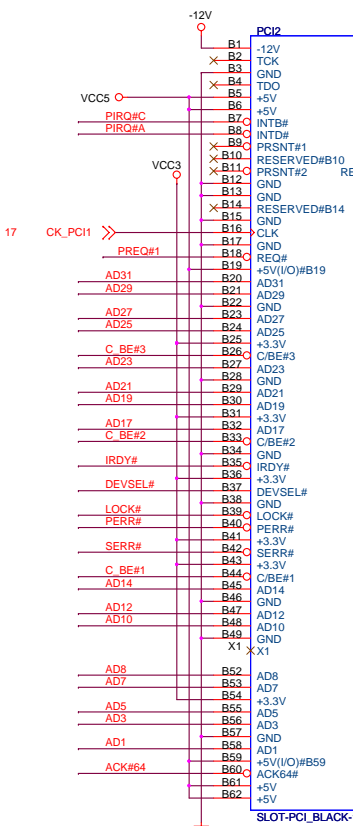
PCI Express X4 Slot



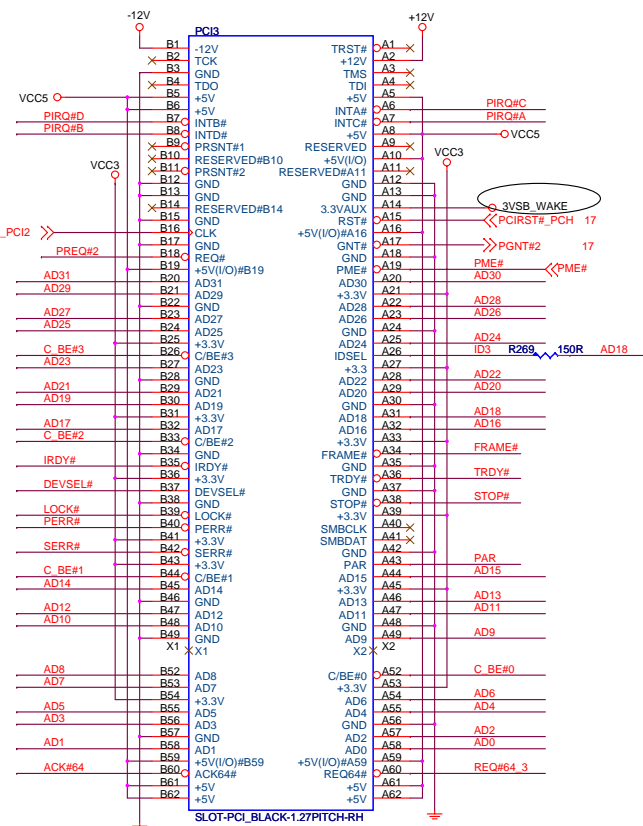




IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



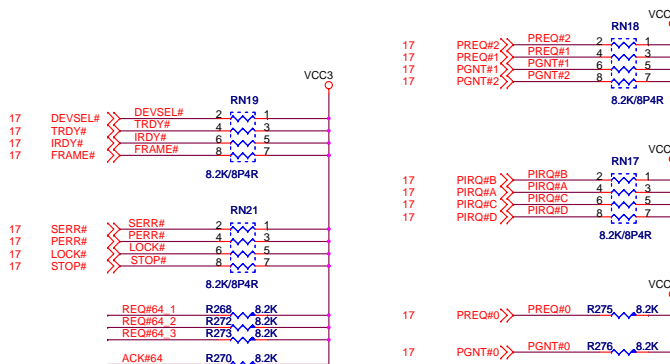
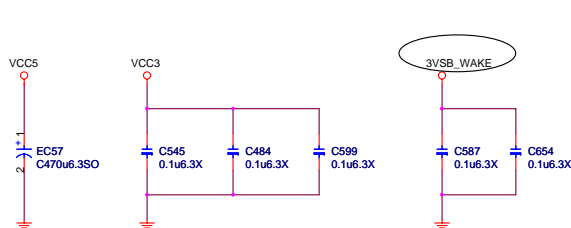
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

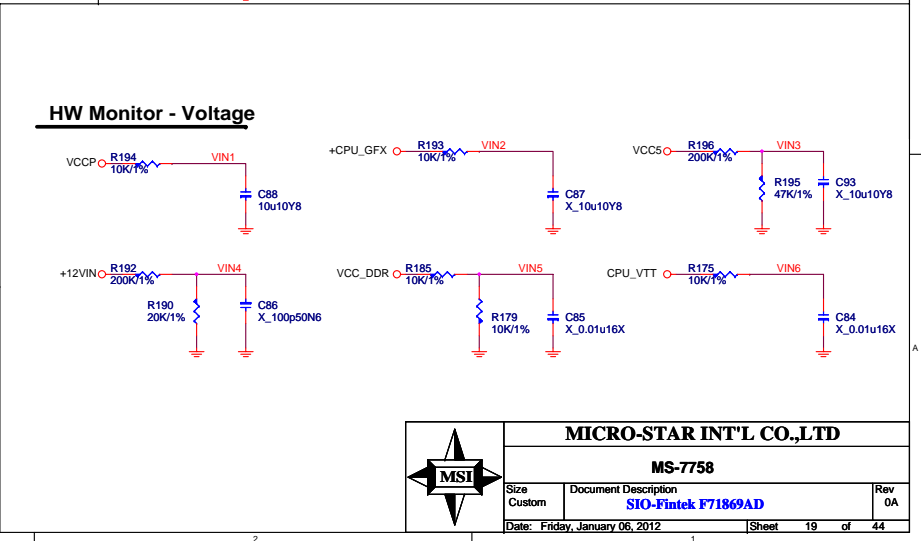


IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

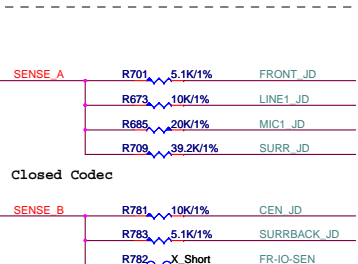
AD[31..0] <>> AD[31..0] 17
C_BE#[3..0] <>> C_BE#[3..0] 17

PCI PULL-UP / DOWN RESISTORS

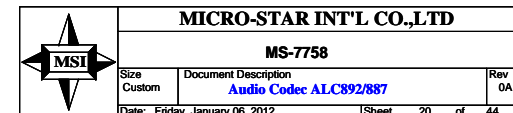
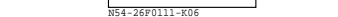
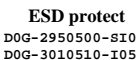
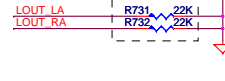
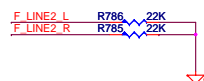
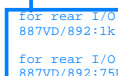




ALC892

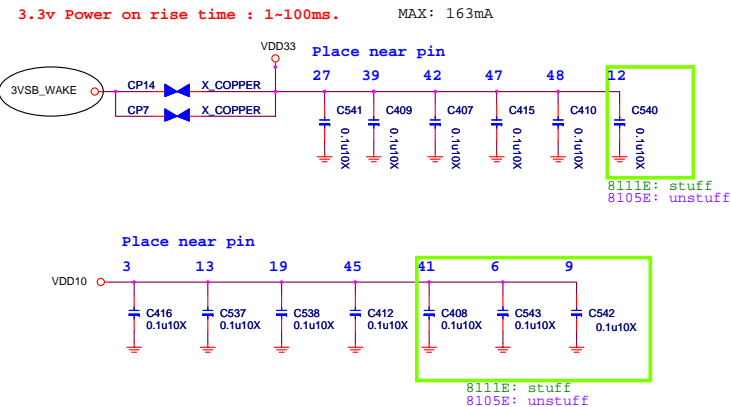
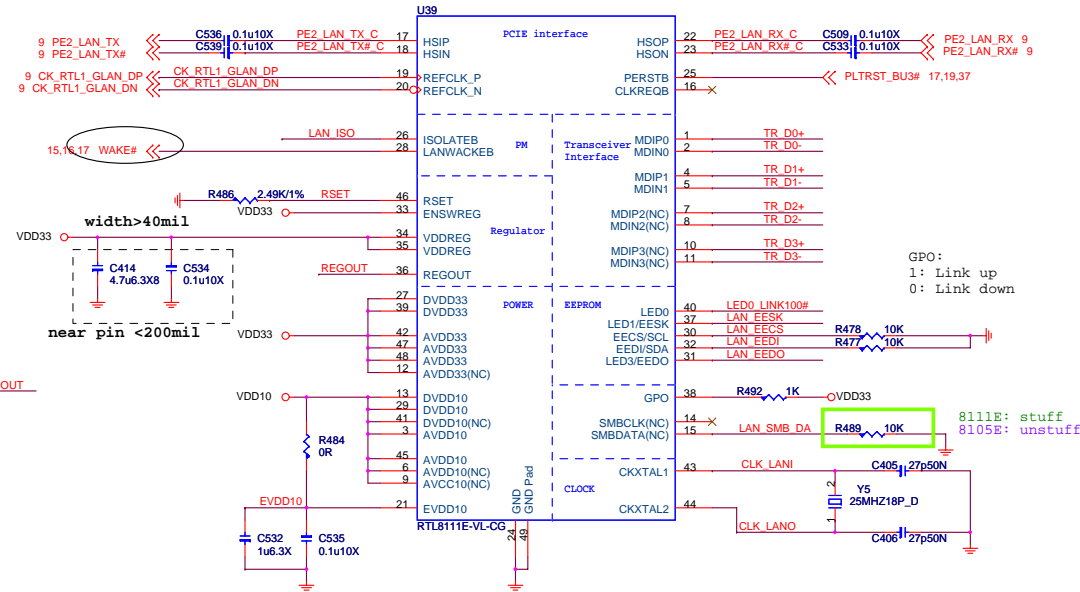
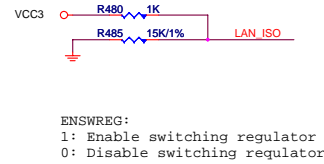


SPDIF OUT



RTL8111E Giga LAN

RTL8105E 10/100M LAN

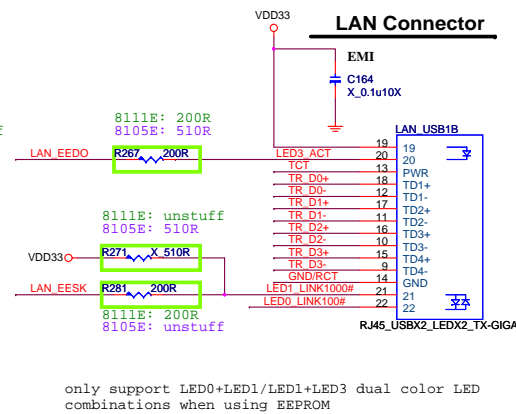


8111E POWER Consumption

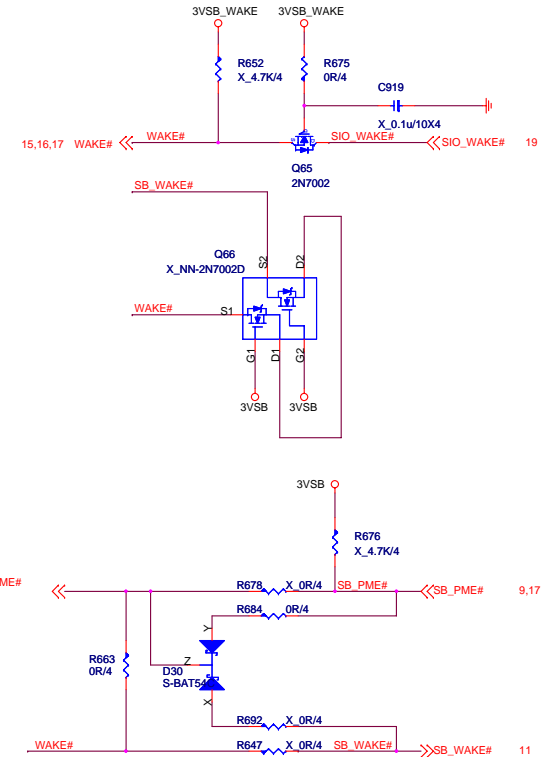
	3.3v	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3v	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

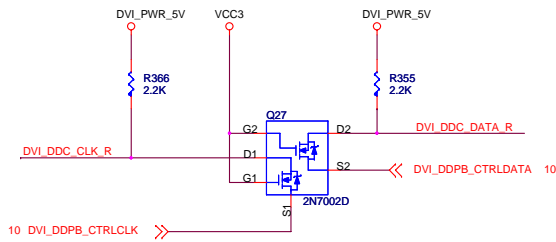
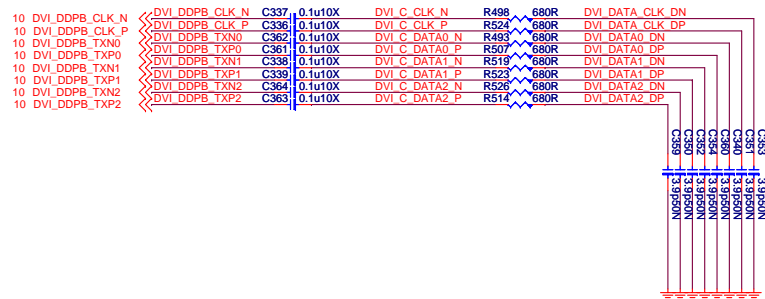


LAN/PCIE/PCI Wake Up CTRL Circuit

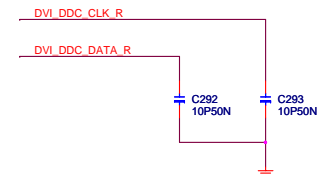
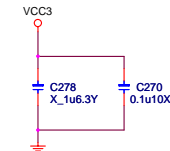
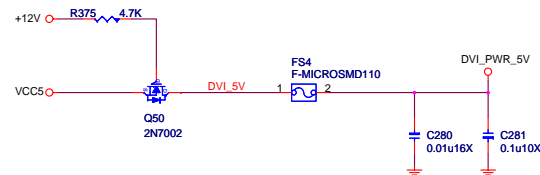
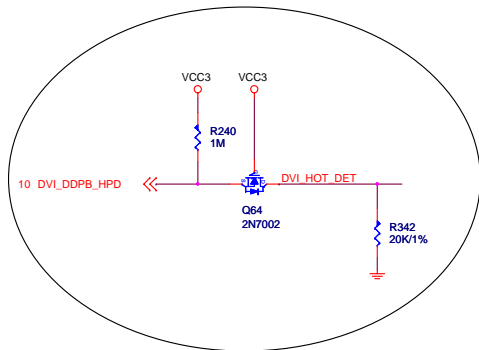
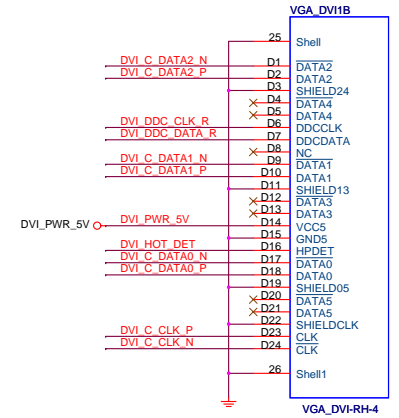
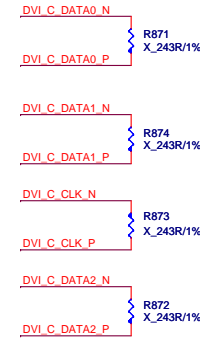


Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	250R Yellow	20	Yellow
21	Orange	21	
22	250R Green	22	Green

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

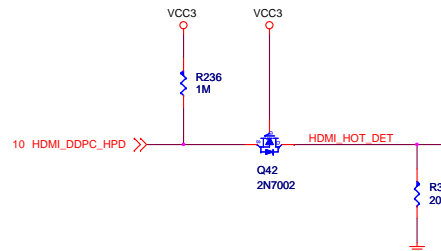
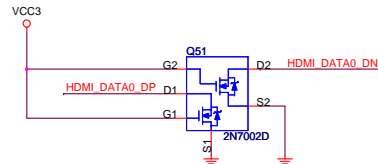
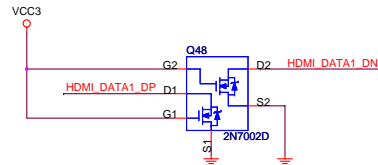
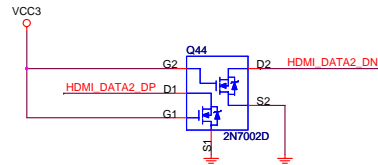
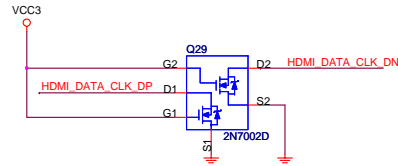
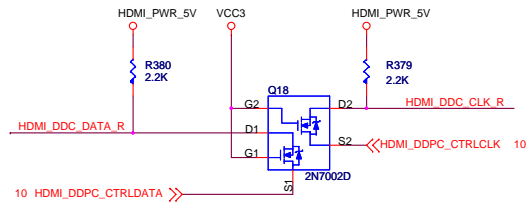


For EMI



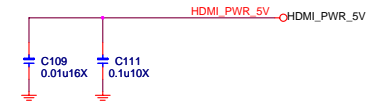
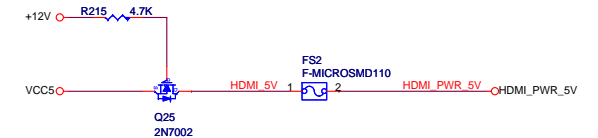
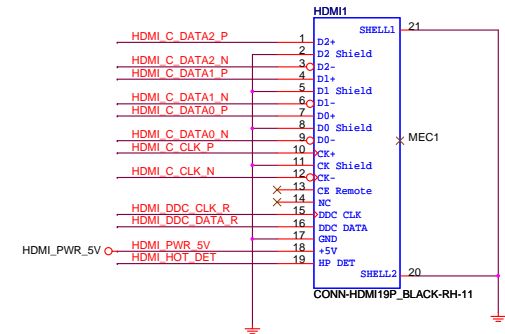
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

10 HDMI_DDPC_CLK_P	HDMI_DDPC_CLK_P	C140	0.1u10X	HDMI_C_CLK_P	R545	680R	HDMI_DATA_CLK_DP
10 HDMI_DDPC_CLK_N	HDMI_DDPC_CLK_N	C142	0.1u10X	HDMI_C_CLK_N	R553	680R	HDMI_DATA_CLK_DN
10 HDMI_DDPC_TX2_P	HDMI_DDPC_TX2_P	C134	0.1u10X	HDMI_C_DATA2_P	R527	680R	HDMI_DATA2_DP
10 HDMI_DDPC_TX2_N	HDMI_DDPC_TX2_N	C132	0.1u10X	HDMI_C_DATA2_N	R547	680R	HDMI_DATA2_DN
10 HDMI_DDPC_TX1_P	HDMI_DDPC_TX1_P	C136	0.1u10X	HDMI_C_DATA1_P	R548	680R	HDMI_DATA1_DP
10 HDMI_DDPC_TX1_N	HDMI_DDPC_TX1_N	C138	0.1u10X	HDMI_C_DATA1_N	R549	680R	HDMI_DATA1_DN
10 HDMI_DDPC_TX0_P	HDMI_DDPC_TX0_P	C124	0.1u10X	HDMI_C_DATA0_P	R552	680R	HDMI_DATA0_DP
10 HDMI_DDPC_TX0_N	HDMI_DDPC_TX0_N	C121	0.1u10X	HDMI_C_DATA0_N	R546	680R	HDMI_DATA0_DN



For EMI

HDMI_C_CLK_N	R235	X_180R/1%
HDMI_C_CLK_P	R235	X_180R/1%
HDMI_C_DATA0_N	R225	X_180R/1%
HDMI_C_DATA0_P	R225	X_180R/1%
HDMI_C_DATA1_N	R233	X_180R/1%
HDMI_C_DATA1_P	R233	X_180R/1%
HDMI_C_DATA2_N	R231	X_180R/1%
HDMI_C_DATA2_P	R231	X_180R/1%



EMI

HDMI_DDC_CLK_R	C572	X 0.1u16X
HDMI_DDC_DATA_R	C571	X 0.1u16X
HDMI_HOT_DET	C570	X 0.1u16X



MICRO-STAR INT'L CO.,LTD

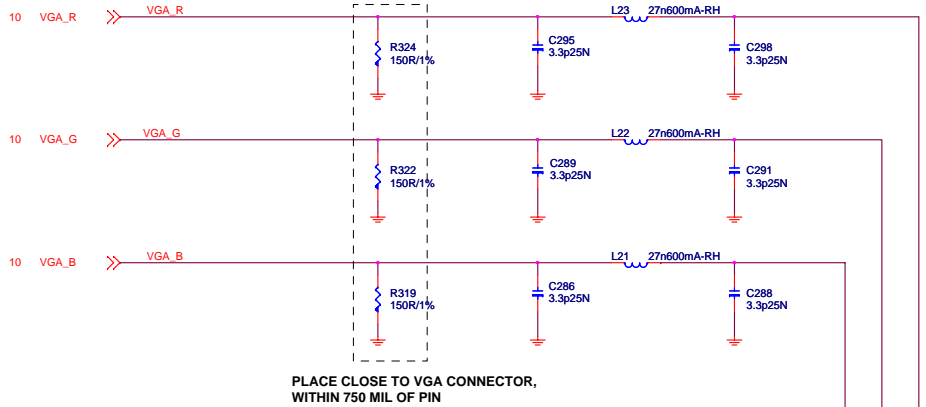
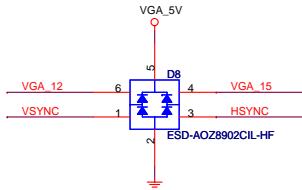
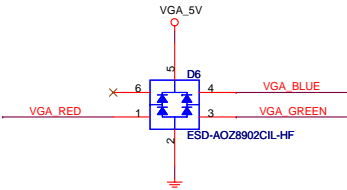
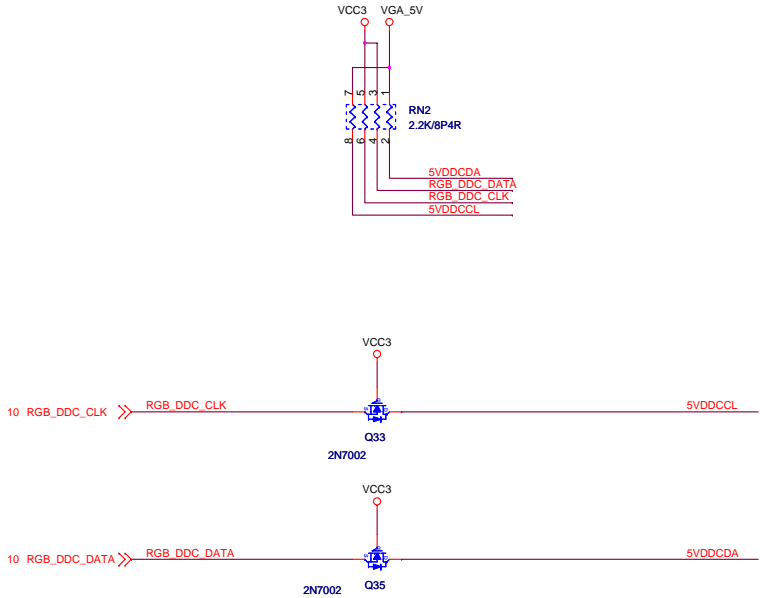
MS-7758

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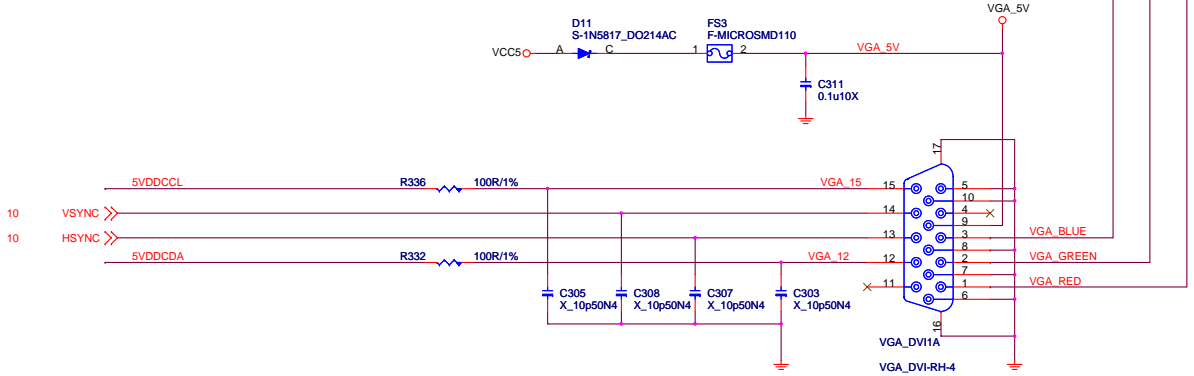
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift

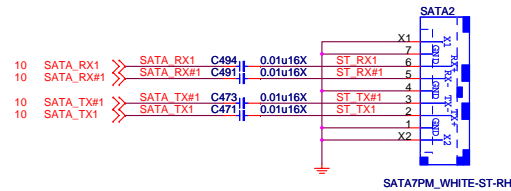
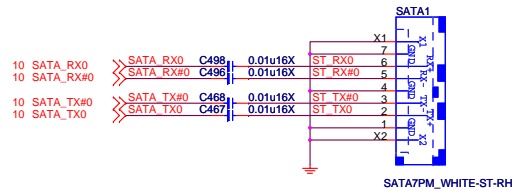


PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

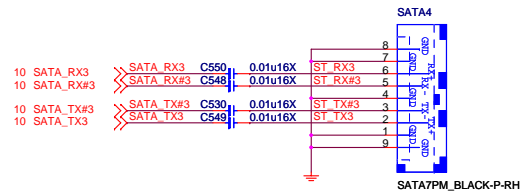
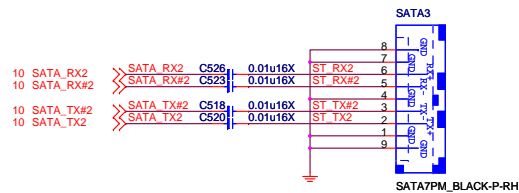


SATA 6G PORT 0,1

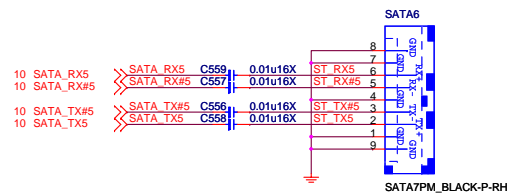
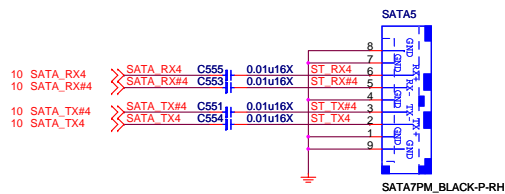
3.0 white



SATA 3G PORT 2,3



SATA 3G PORT 4,5



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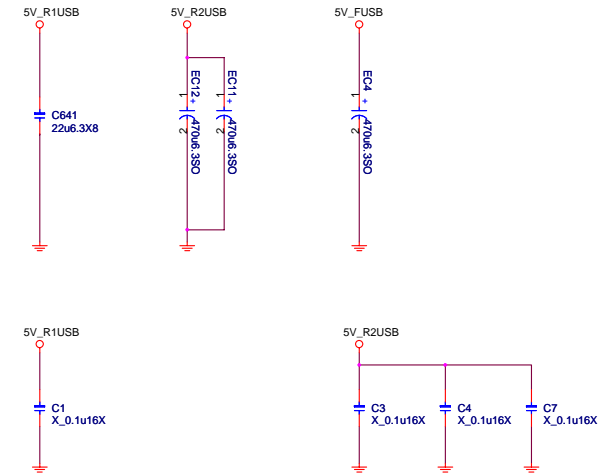
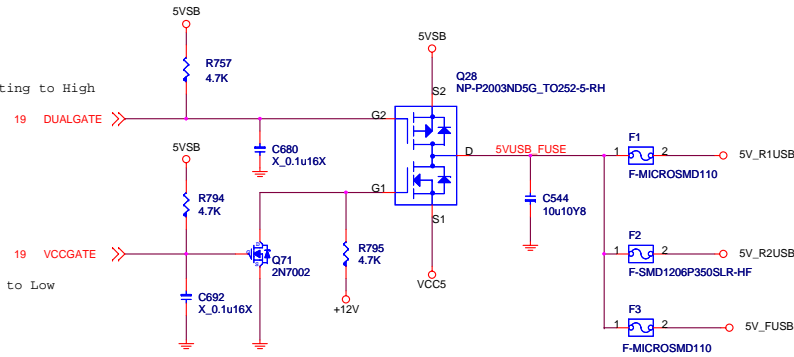
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

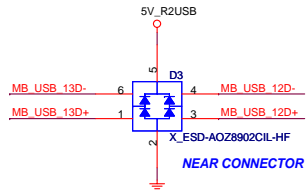
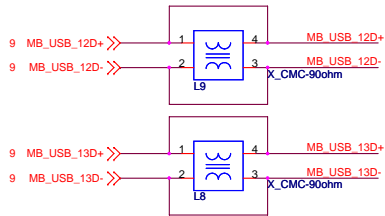
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

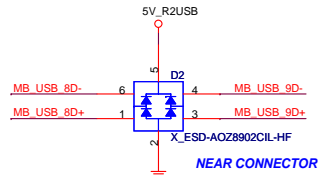
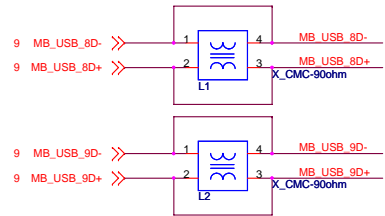
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



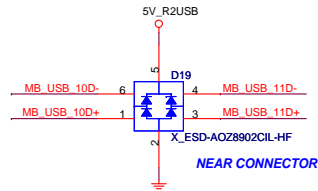
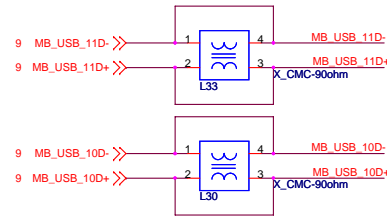
REAR USB PORT 12,13 (With LAN)



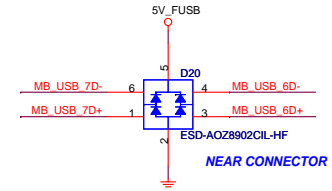
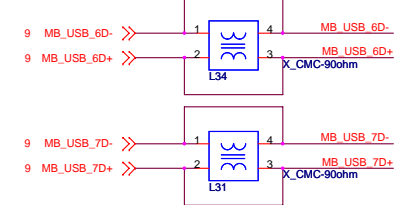
REAR USB PORT 8,9 (With HDMI)



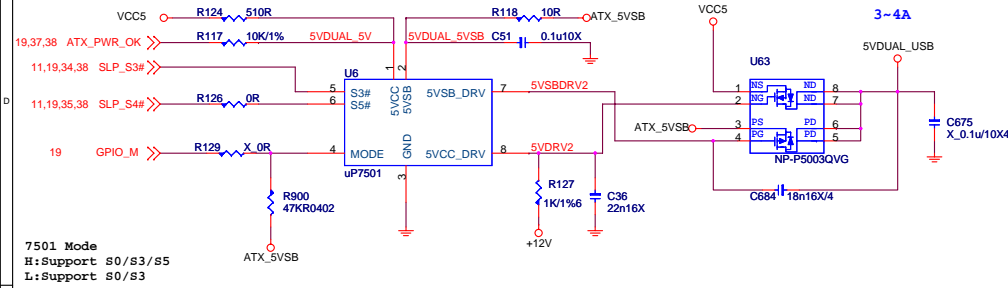
FRONT USB PORT 10,11(With PS2)



FRONT USB PORT 6,7



5VDUAL_USB



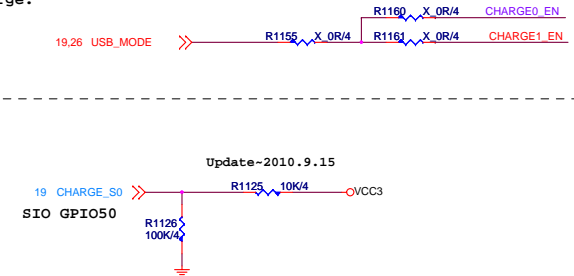
SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)

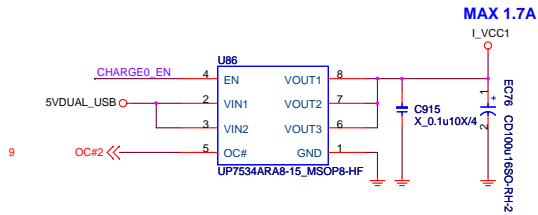
0: Don't support USB charge and resume.
1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

Pin power I_3VSB or VBAT
Register power I_3VSB or
VBAT
Register reset I_3VSB or
VBAT



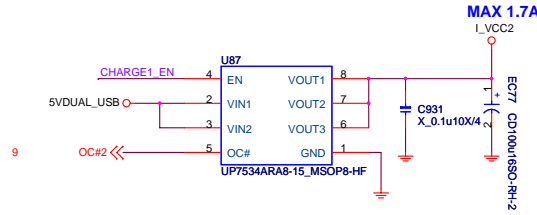
USB POWER PORT 0 For USB Charging



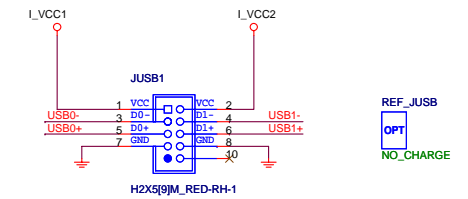
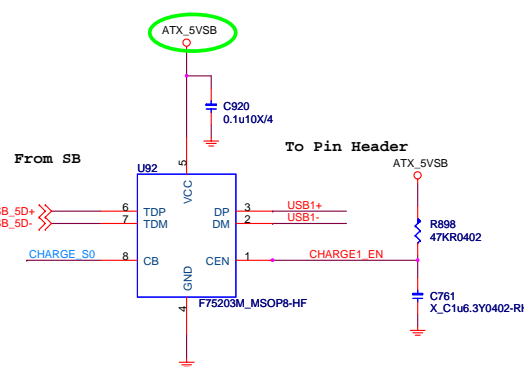
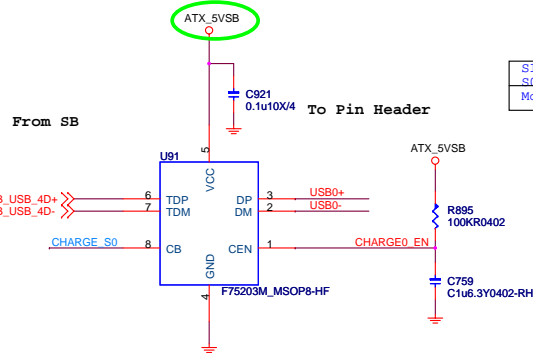
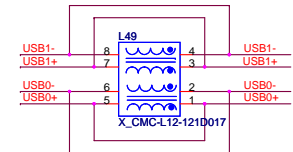
** If your spec will not need bom option, please don't co-lay blue labels.

S1	0		0	1
S0	0		1	1
Mode	AUTO		A	Y

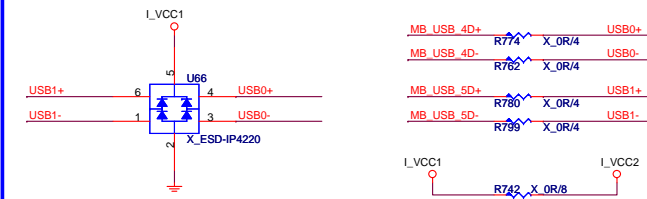
USB POWER PORT 1 For USB Charging



FRONT USB PORT 0,1



COLAY remove USB charger ic



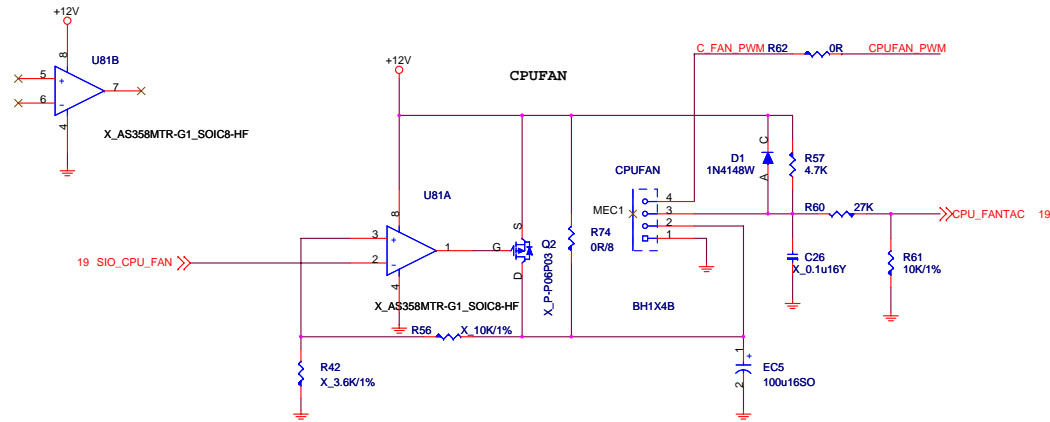
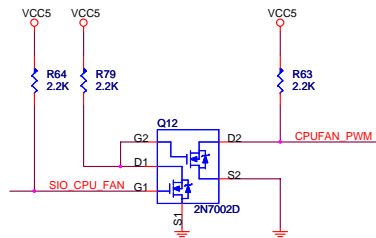
A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

Please name the pin header JUSB1 and use SB
USB0,1 link for charger port.

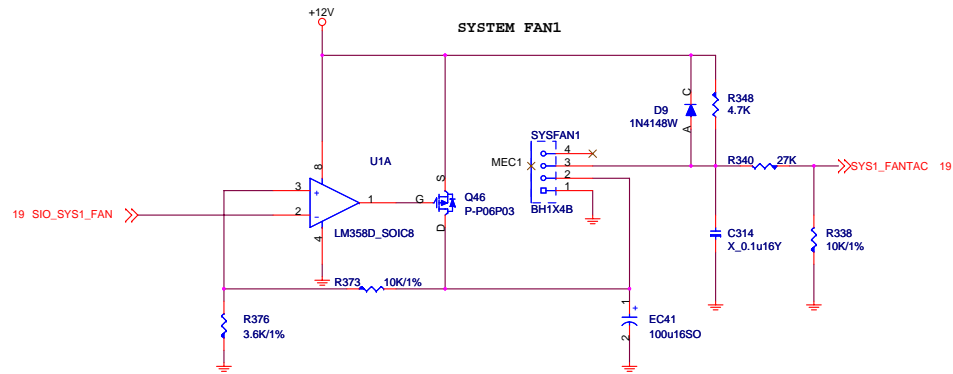
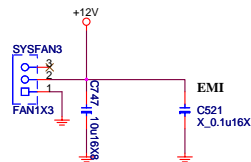
PI5USB14550 has internal EDS diode.

Title			USB FULL CHARGE
Size	Document Number	Rev	
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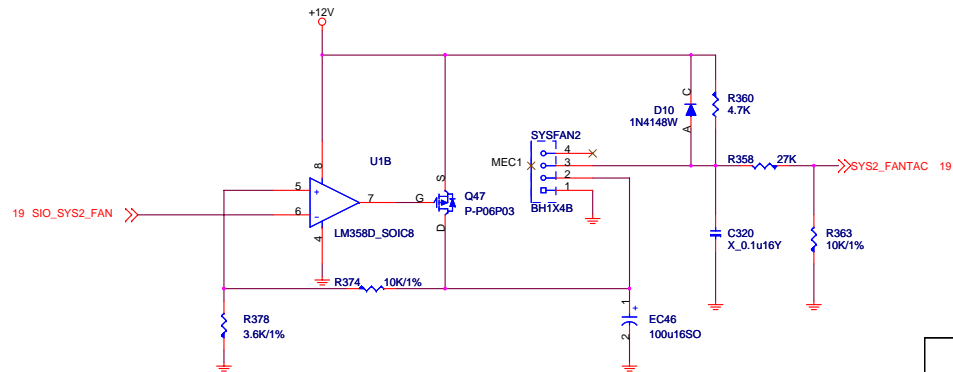
FAN-COUNTROL CIRCUIT



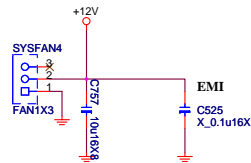
SYSTEM FAN3

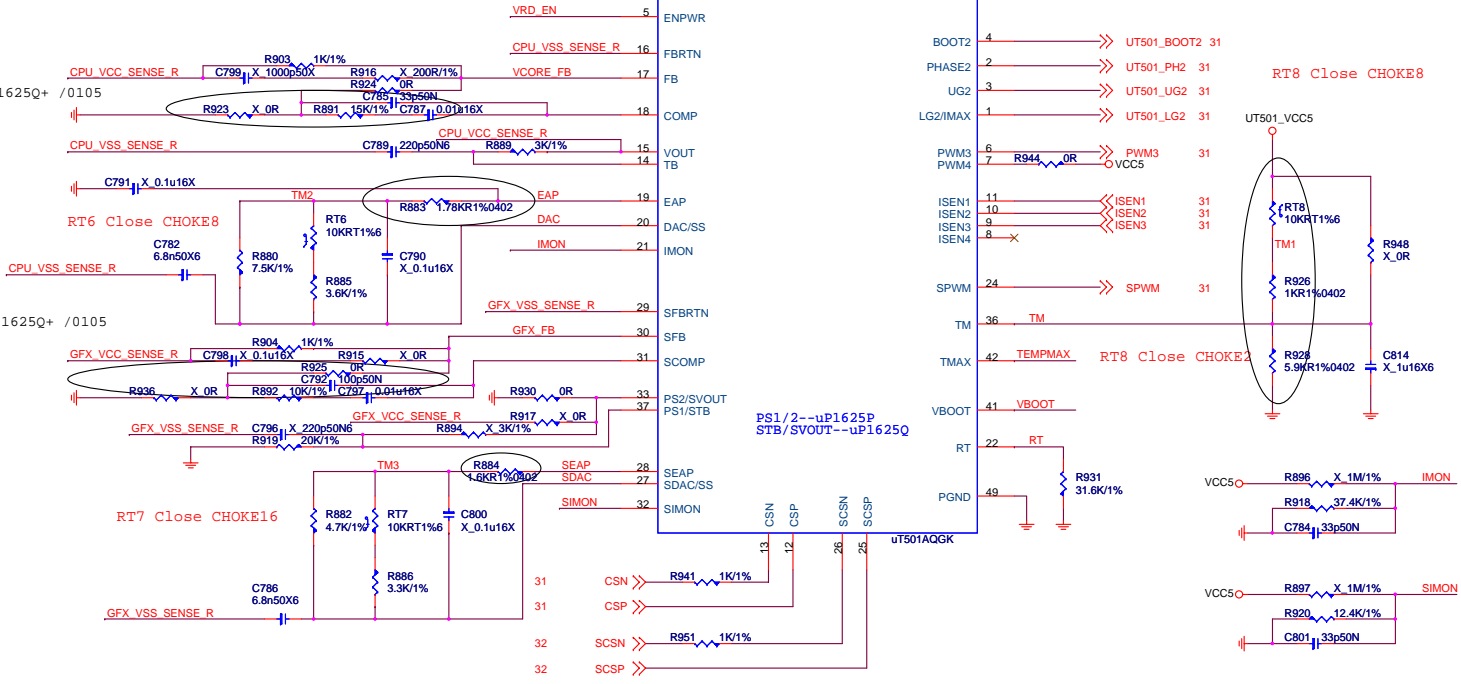
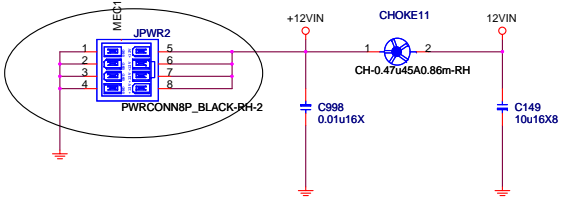
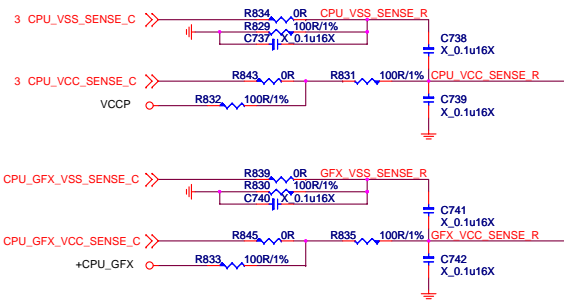
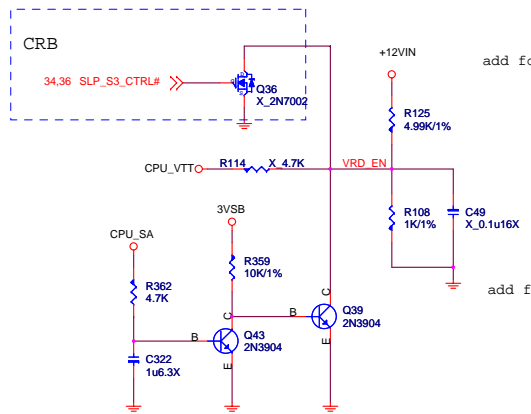


SYSTEM FAN2

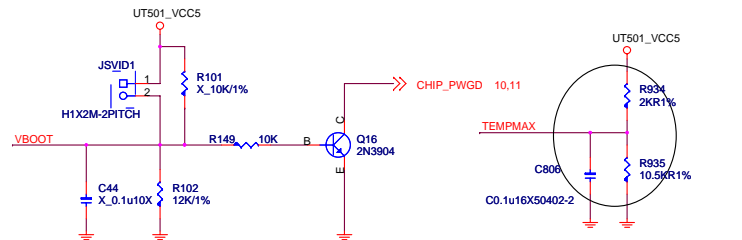
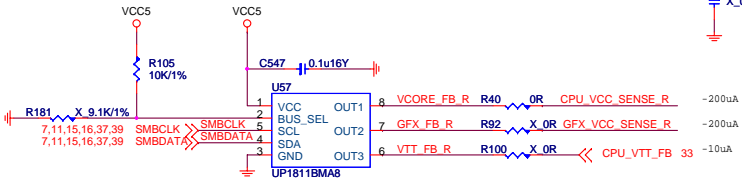


SYSTEM FAN4



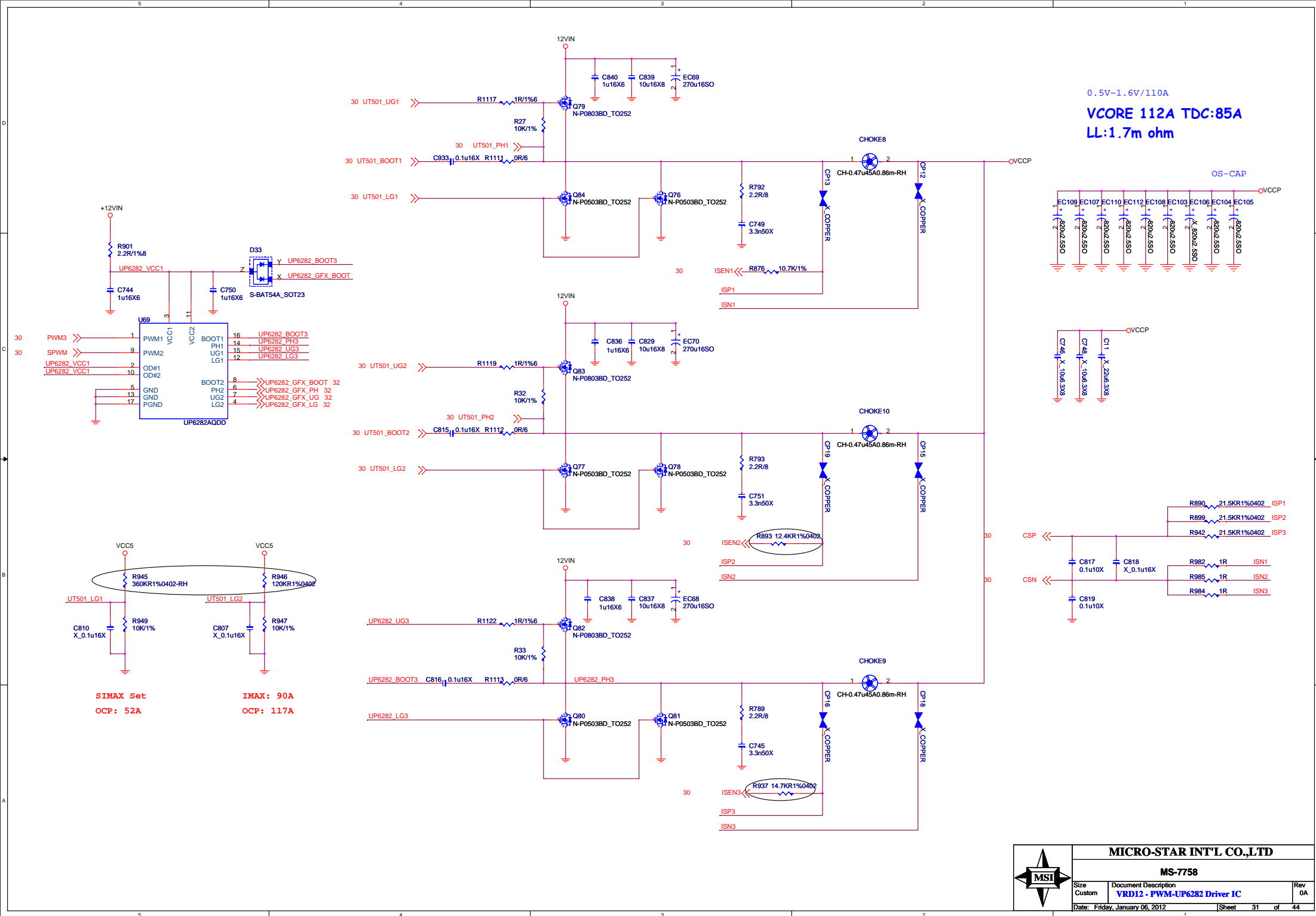


0x20:RH=10K,RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



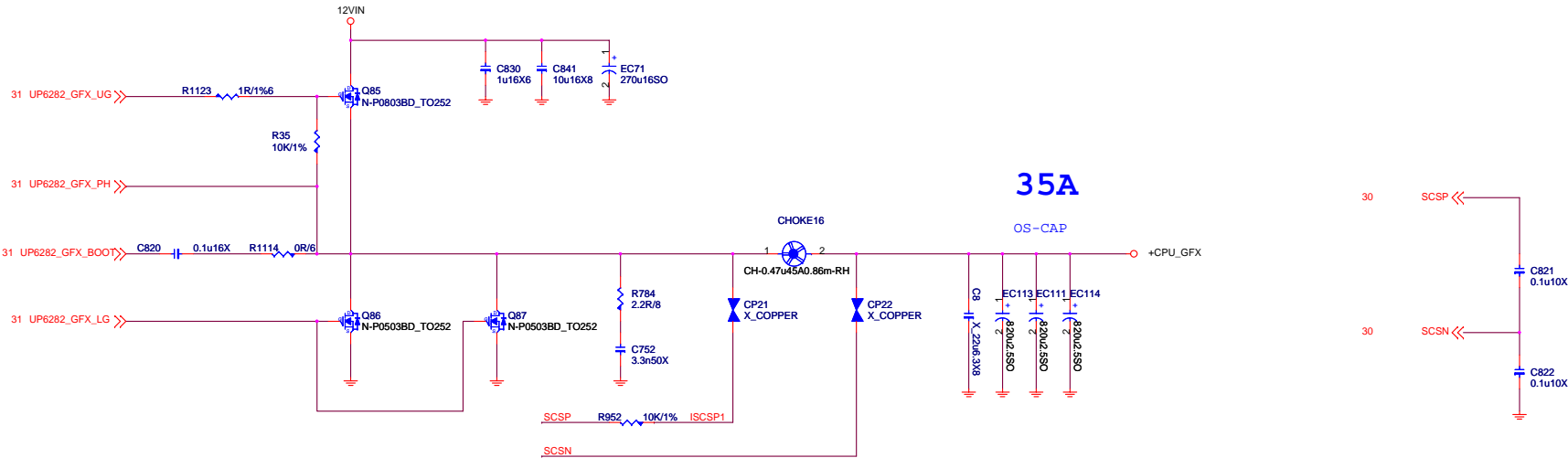
MS-7758

Size Custom	Document Description VRD12 - PWM-UT501	Rev 0A
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CPU_GFX:0.25-1.52

35A FOR CPU

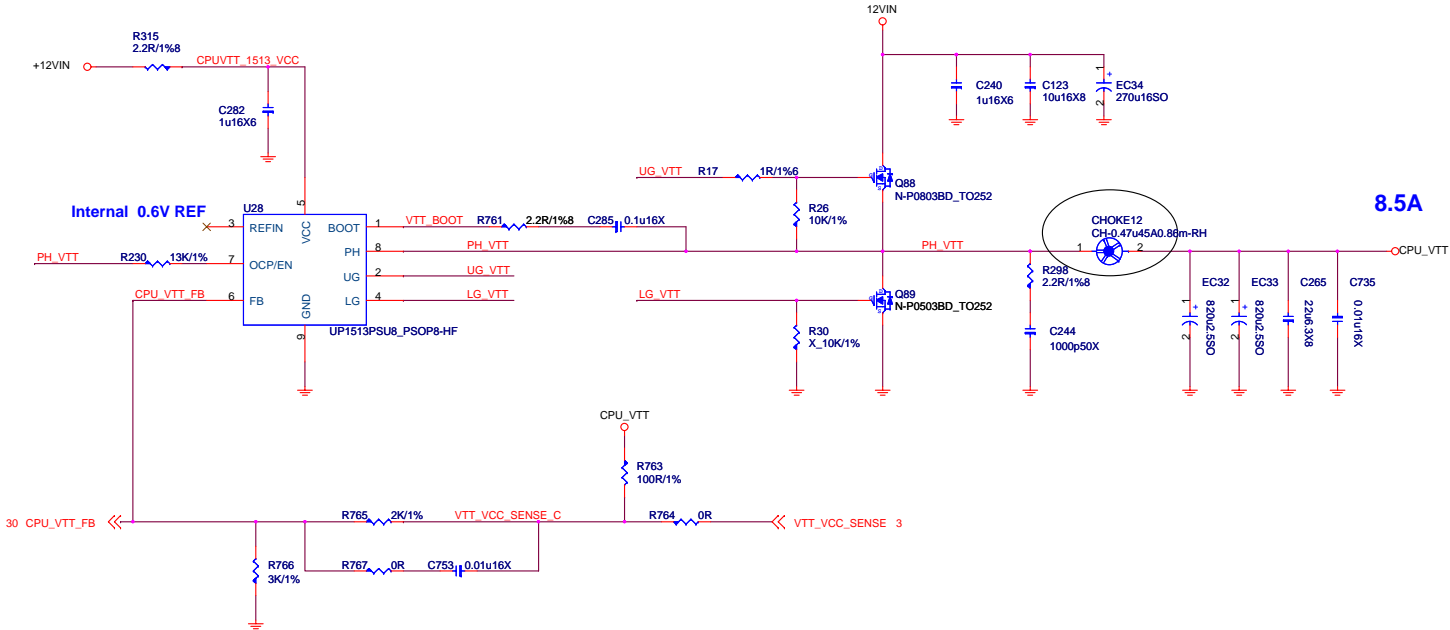


CPU_VTT:1.05/1.00 MAX 17.3A

CPU VTT 8.5A SA Core =8.8A

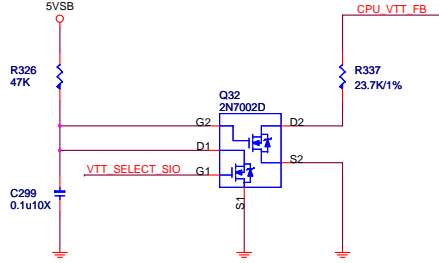
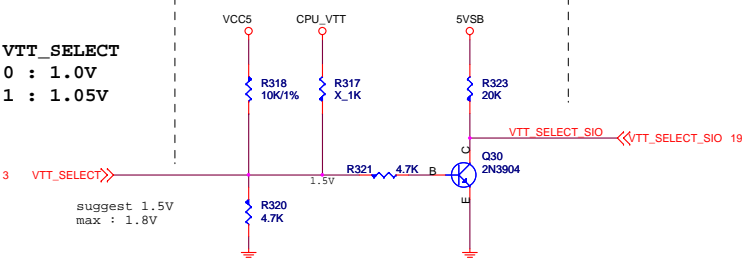
8.5A FOR CPU

$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$
 $5 * 1 = 5A > 3.8A$



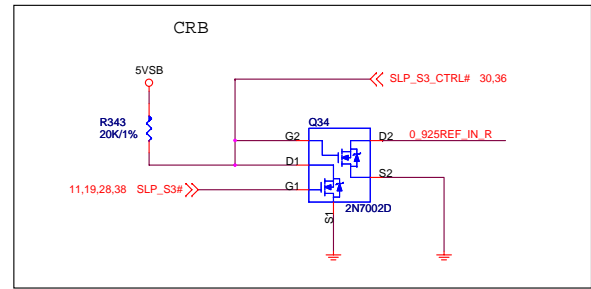
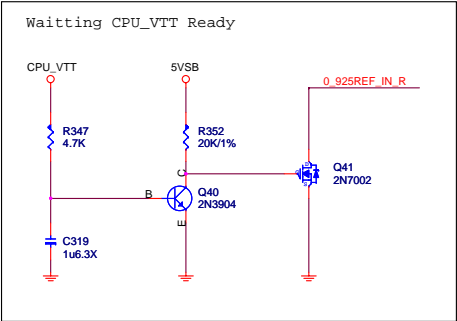
VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



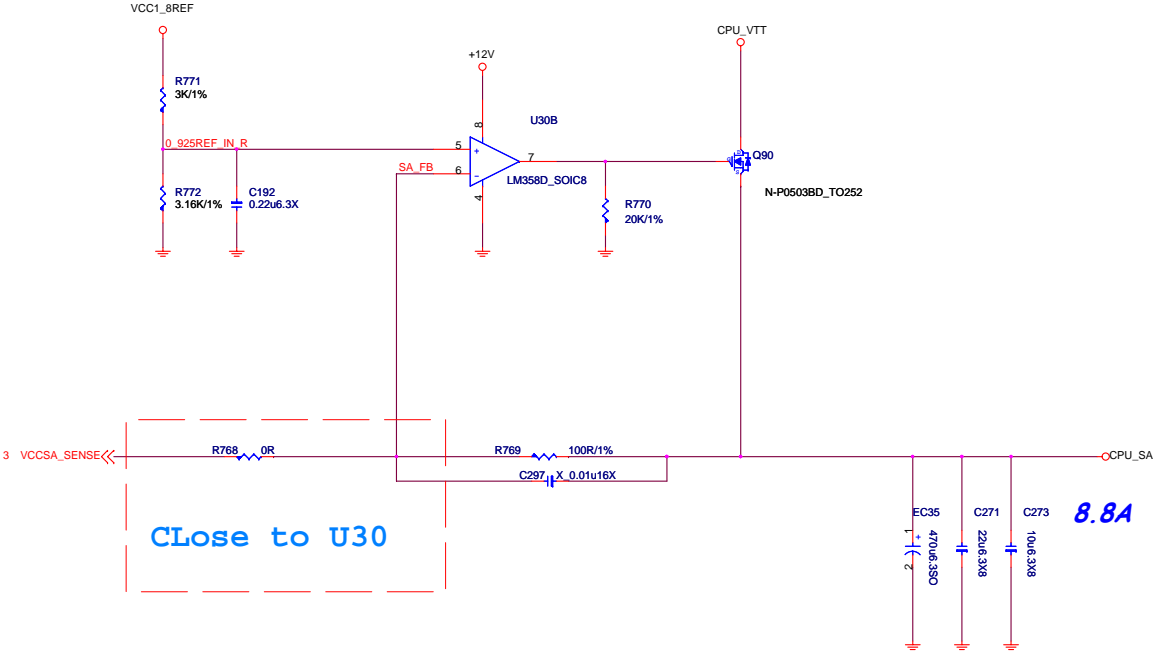
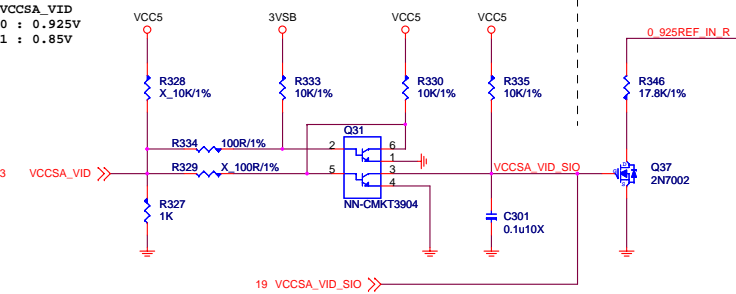
CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



DDR Power:1.5V

DDR3_1.5V 4.75A+15A+1A=20.75A

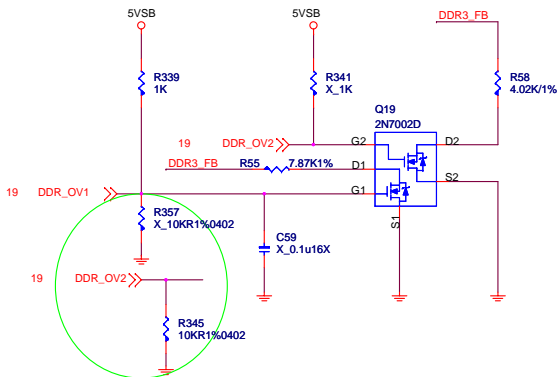
4.75A FOR CPU

15A FOR 4DIMM

1A FOR DDR VTT

Tripple=8A
4.7*2*1=9.4A>8A

DDR OV

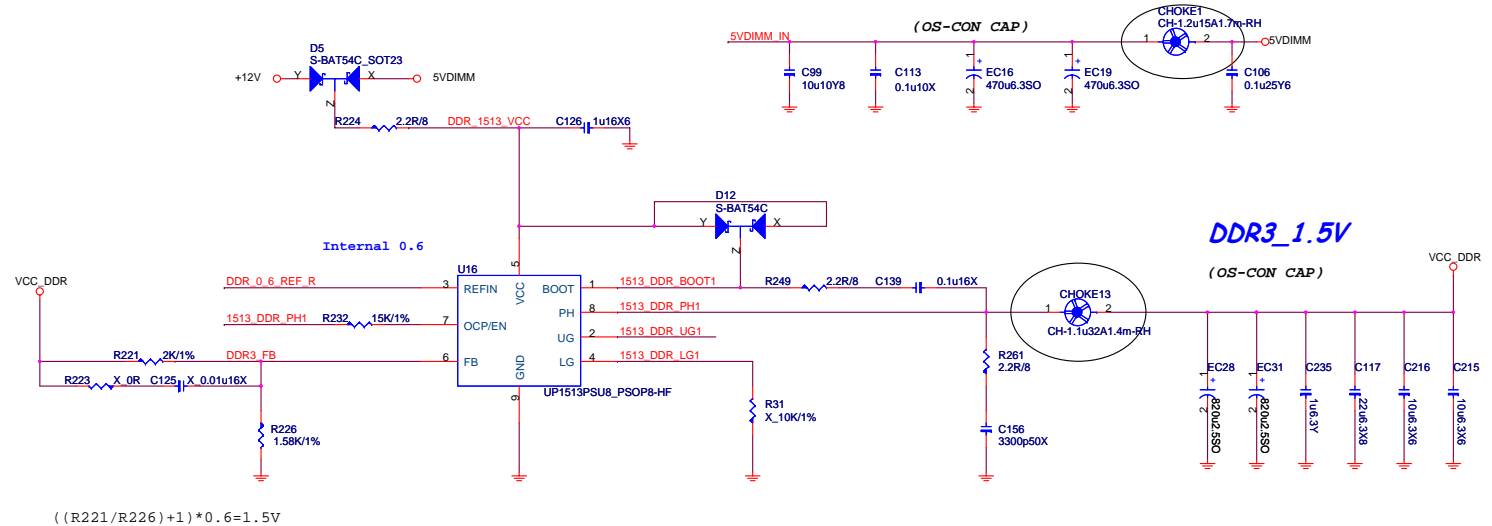


*Default 1.5V

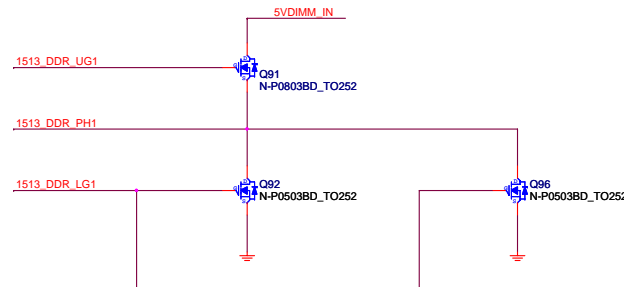
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)

DDR_OV2 = GPIO02(S/IO)



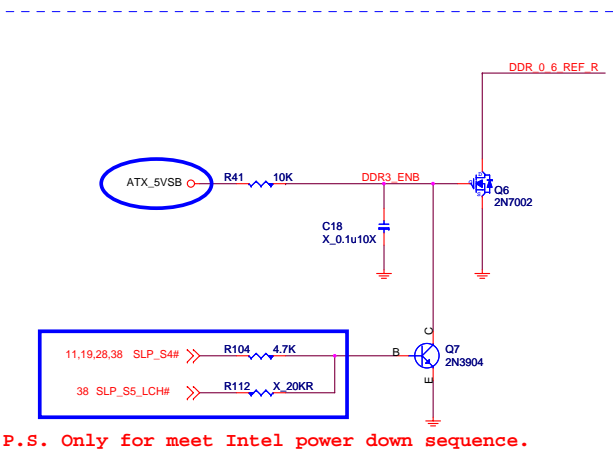
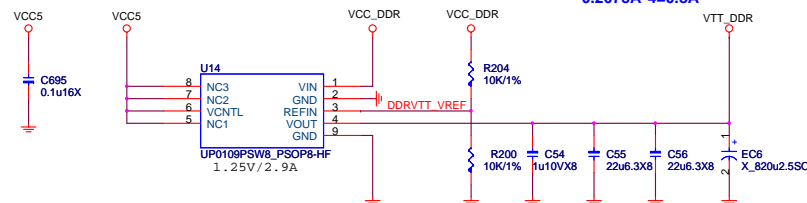
$$((R221/R226)+1)*0.6=1.5V$$



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$



P.S. Only for meet Intel power down sequence.



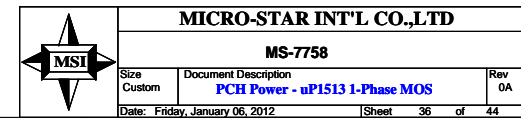
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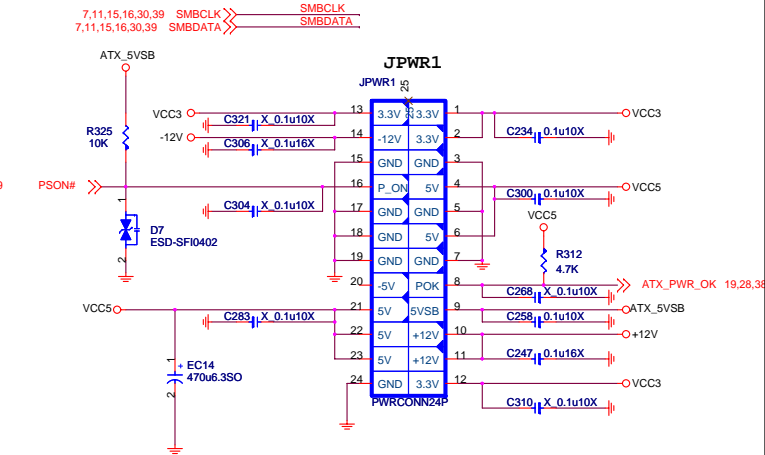
Size	Document Description	Rev
Custom	DDR Power - UP1513 1-Phase MOS	0A
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1.8A FOR ME CORE

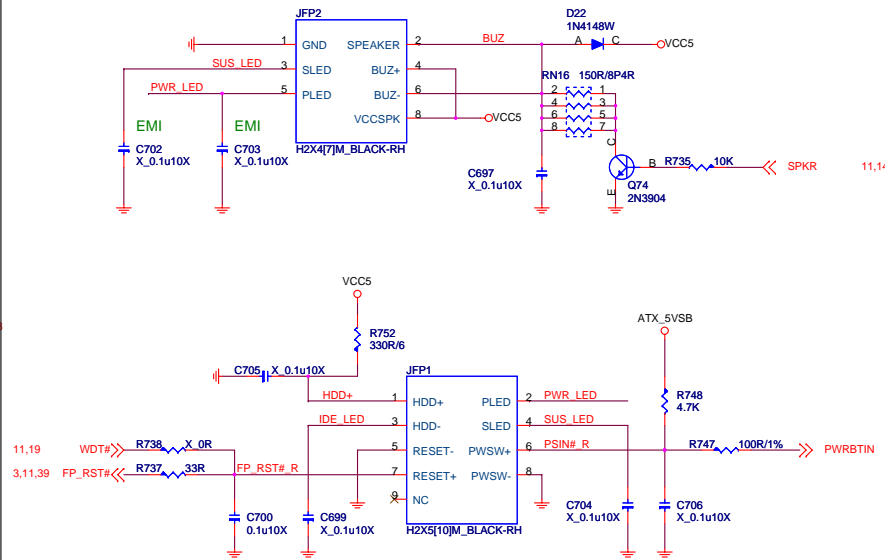
8A



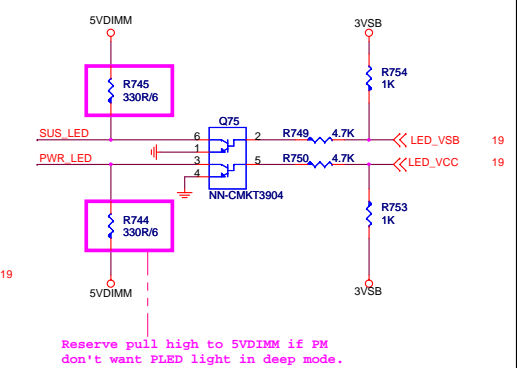
ATX POWER CONNECTOR



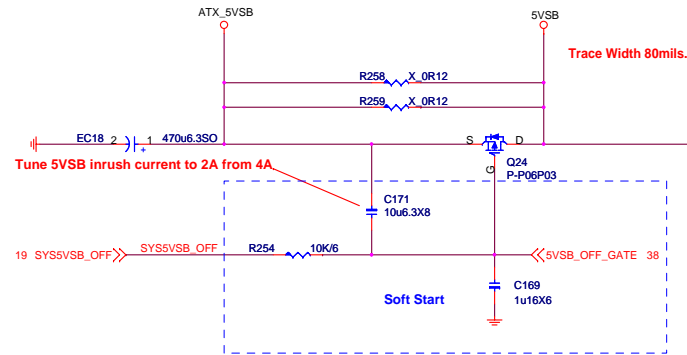
FRONT PANNEL



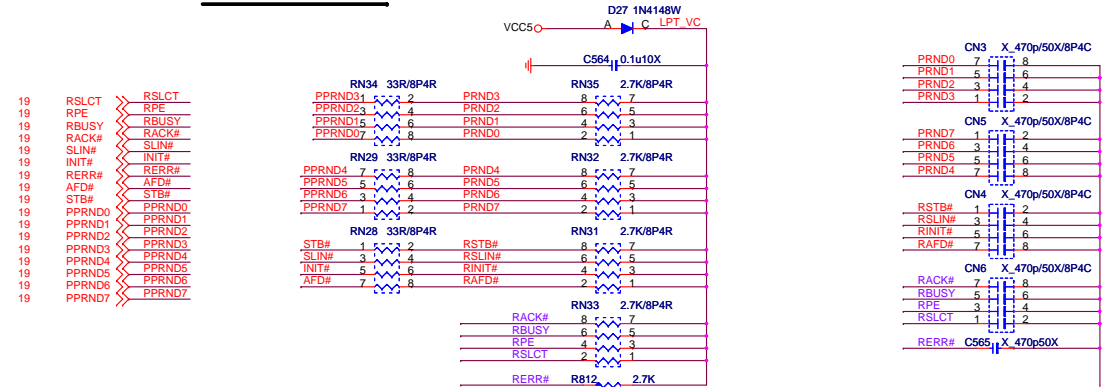
LED (for Fintek 71869)



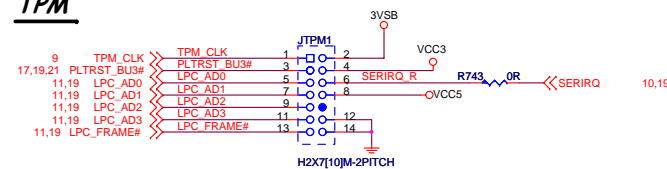
5VSB Power Switch



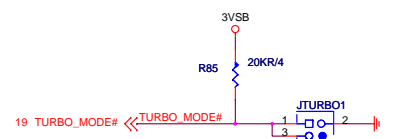
PARALLAL PORT



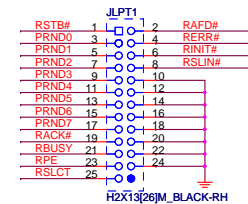
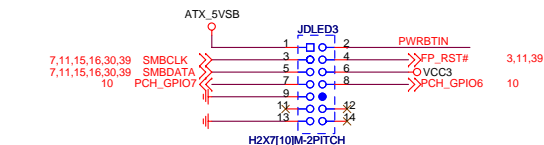
TPM



Turbo Button



JDLED3



N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm

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Custom	ATX F_Panel/EMI/TPM	0A	
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[illegible][illegible]

3VSB

3VSB_WAKE

R260 X 0R12

R274 X 0R12

ATX_5VSB

R617 47KR0402

3VSB_WAKE_EN

C597 X 1u/6.3X/4

C585 10u16X8

U134 POK EN VIN NC

U134 CNTL VOUT

UP0104SSW8_PSOP8-HF

R674 10R/4

C609 1u/6.3X/4

VCC3

Q67 N-P0603BD_TO252-3-HF

5VDRV1

3VSB_WAKE

C703 1

C706.3 2

R598 10K/1%4

R610 200K1%4

R702 3.3KR1%0402

C652 0.015u16X/4

Q59 2N7002

19 3VSB_LAN_EN# 3VSB_LAN_EN#

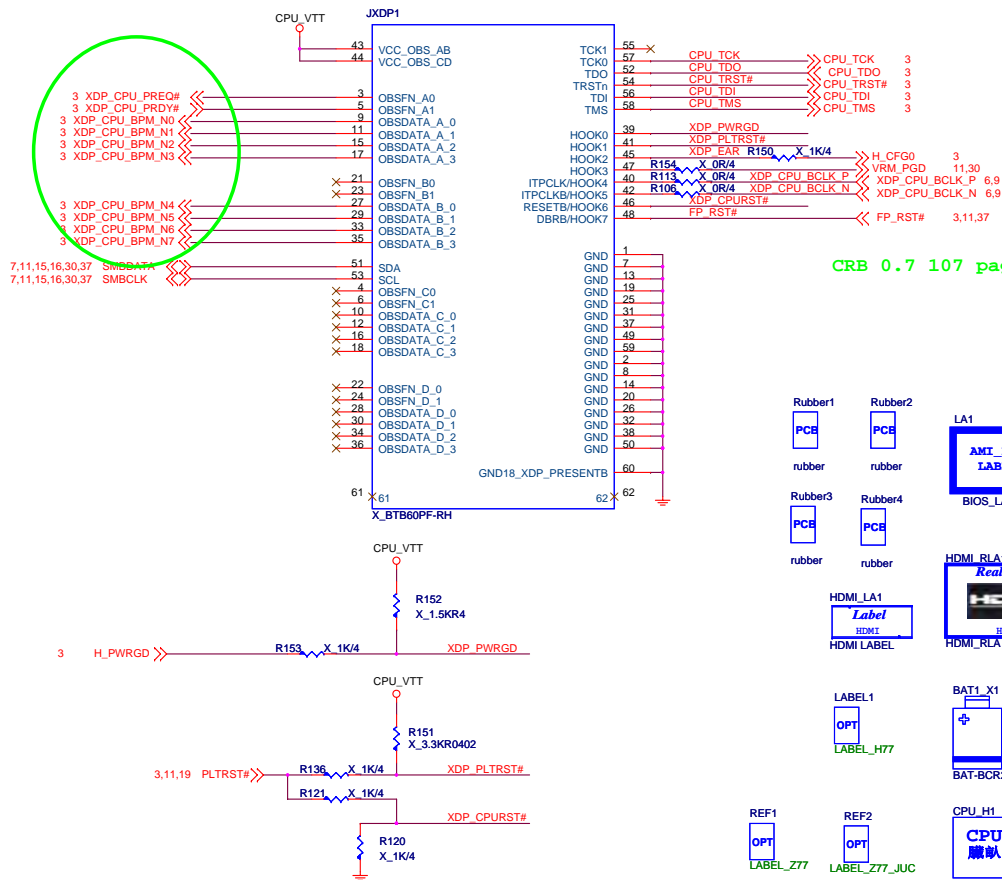
$$R2 = R1 / [(Vout/0.8V) - 1]$$

[illegible]

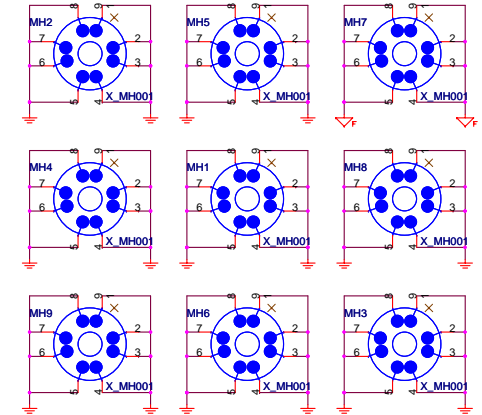
[illegible]

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Size Custom	Document Description ACPI controller UPI		Rev 0A
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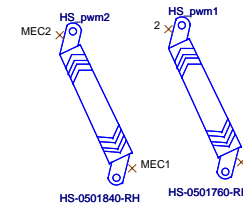
Reserve debug port 5020



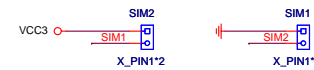
Mounting Holes



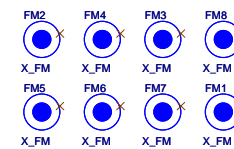
HEATSINK



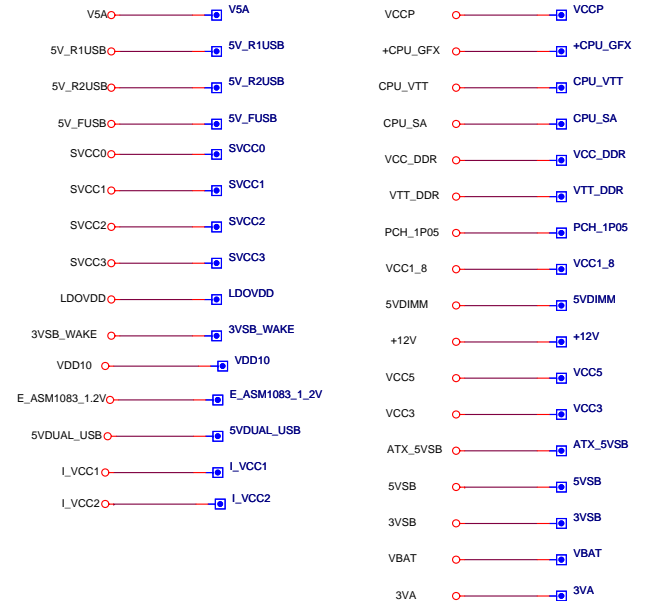
Simulation



Optical Fiducial Marks-120



Voltage test point

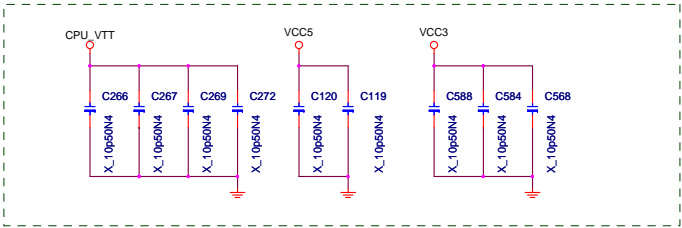


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EMI:cap. for signal return path



EMI

