Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

SKYY

2007-10-26

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: LA-4021P	Rev: 0.1
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SKYY

Docking CONN.(Opus 1.0)
*RJ-45(LED*2)
*CRT
*S-VIDEO OUT
*LINE IN
*LINE OUT
*USB x4
*DC JACK

*Power on signal
*Docked indicator signal
*AC present indicator signal

Thermal Sensor
EMC2103
page 4

Fan Control
page 4

Mobile Penym
LV/ULV Dual Core
uFCPGA-956 CPU - SFF
page 4,5,6,7

CK505
Clock Generator
ICS9LPRS397
page 16

Accelerometer
LIS302DLTR
page 26

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz 1.05V

LCD conn page 18
CRT page 17
CRT to docking page 34
S-Video to Docking page 34

Intel Cantiga GMS
FCBGA 1363 - SFF
page 8,9,10,11,12,13

DDR2 800MHz 1.8V
Dual Channel

DDR2-SO-DIMM X 2
BANK 0, 1, 2, 3 page 14,15

DMI X4

Express Card 54
PCIE X1 + USB X1
page 25

WWAN Card
WWAN + PCIE X1 + USB X1
page 25

PCI-E BUS

Intel ICH9-M
WBMMAP-569 - SFF
page 20,21,22,23

USB2.0
Azalia
SATA0
SATA1

USB x1(Docking) page 34
FingerPrinter AES2810 USBx1 page 31
daughter board
USB conn x 3(For I/O)
BT Conn USB x 1 page 31
USB x1(Camara) page 18
MDC V1.5 page 30
Audio CKT AD1984HD page 28
TPA6043 AMP & Audio Jack page 29
2.5" SATA HDD Connector OR SATA ODD Connector page 21
1.8" SATA HDD Connector page 21

10/100/1000 LAN
Intel Boaz GbE PHY
page 24

24HST1041A-3
RJ45 CONN
page 25

CardBus Controller
Rico R5C833
page 27

PCI BUS

1394 port
SD/MMC Slot

SPI

SPI ROM
AT26DF321
page 32

LPC BUS

TPM1.2
SLB9635TT
page 32

SMSC KBC 1091
page 33

Touch Pad CONN. page 30
TrackPoint CONN. page 30
Int.KBD page 30

LED page 19
RTC CKT. page 21
Power OK CKT. page 35
Power On/Off CKT. page 30
DC/DC Interface CKT. page 36

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Title: Block Diagram

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
KB926	X	V	V	X	X	X	X	X
KB926	X	X	X	V	X	X	X	X
ICH9	X	X	X	X	V	V	V	X
Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Title: Notes List

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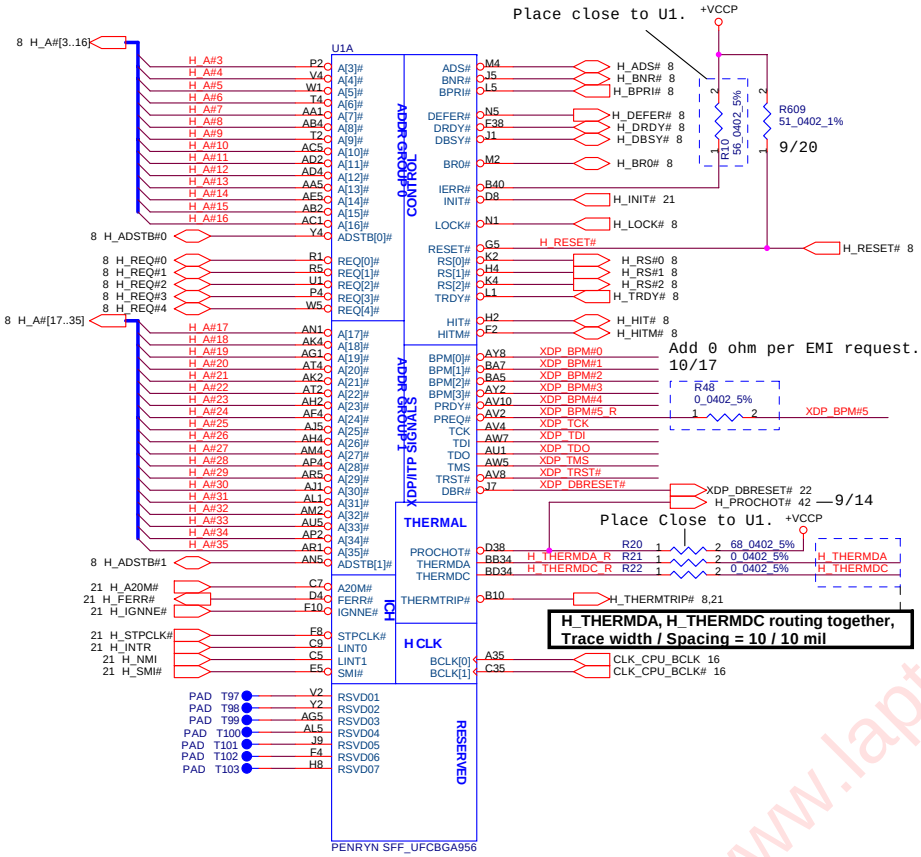

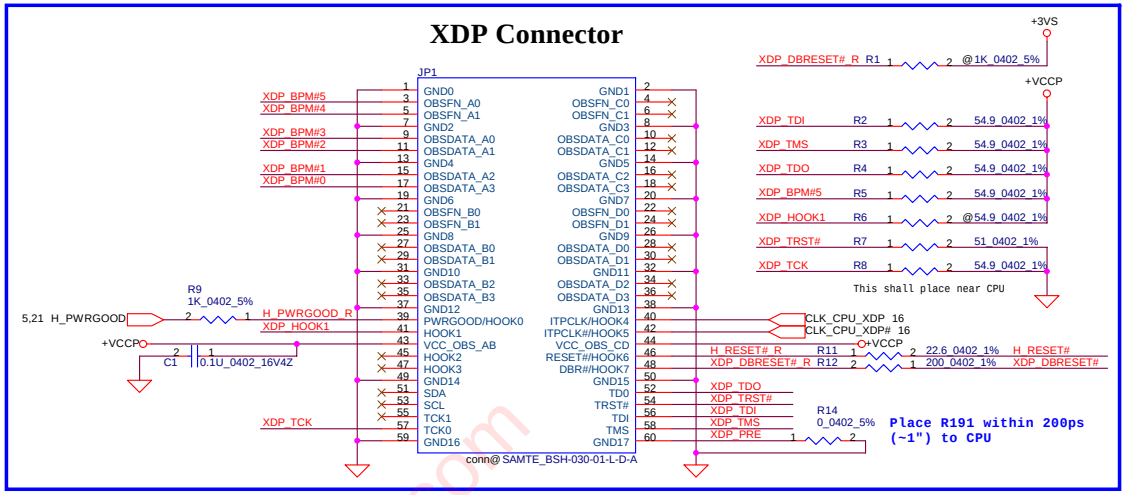

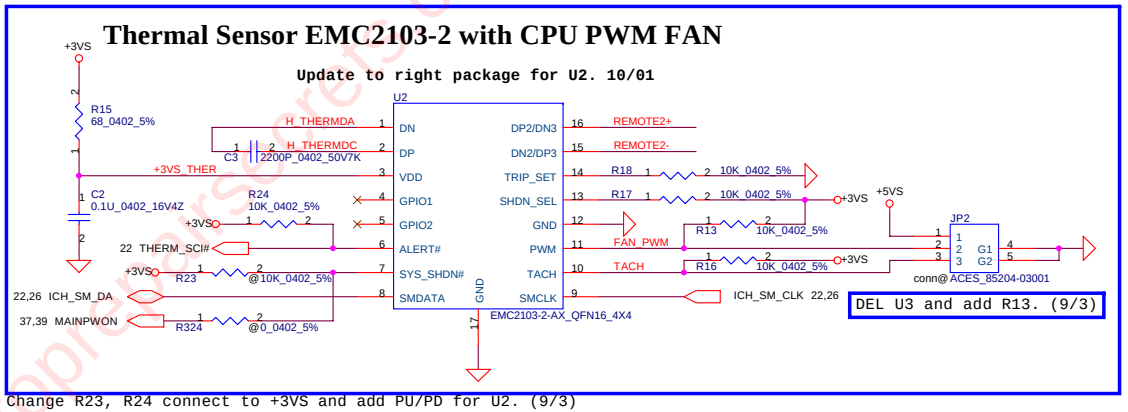

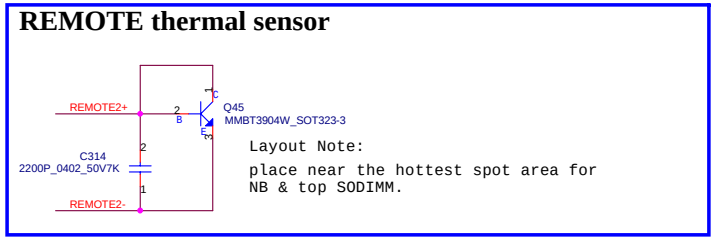

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Title	Penryn(1/3)-AGTL+/ITP-XDP		
Size: Custom	Document Number: LA-4021P		Rev: 0.1
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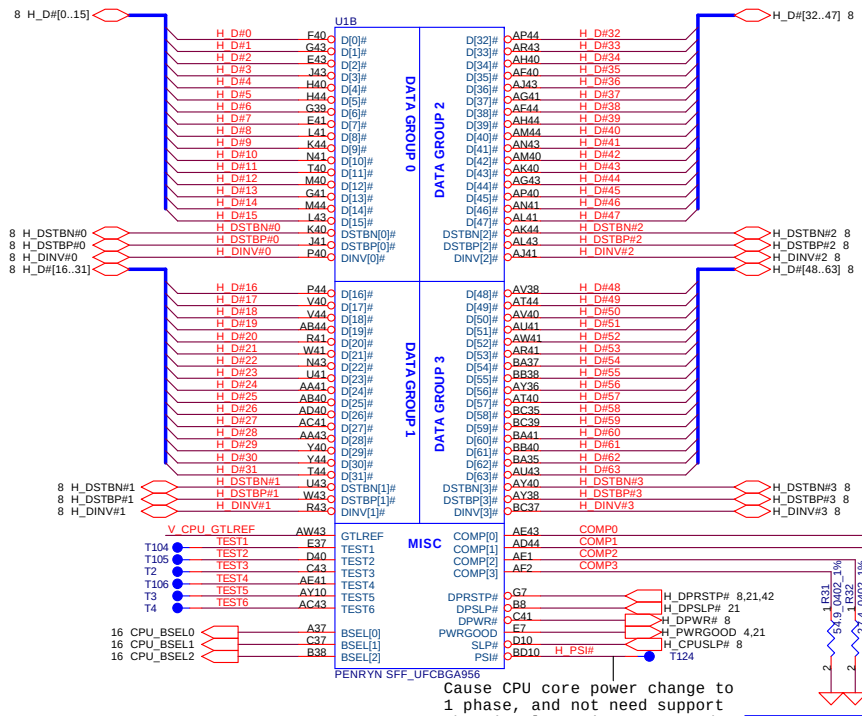
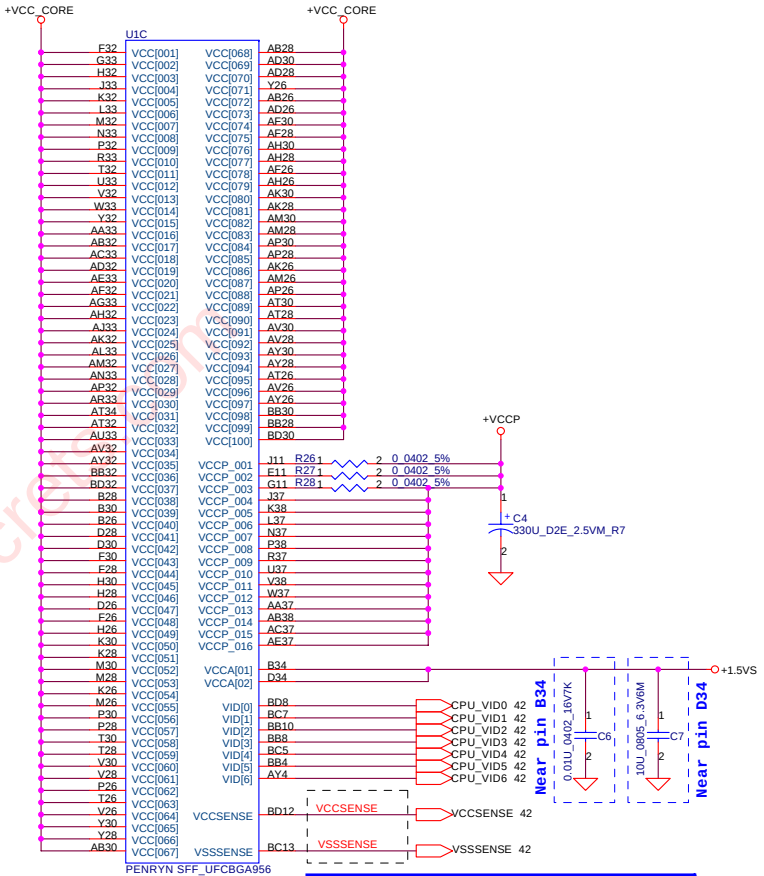


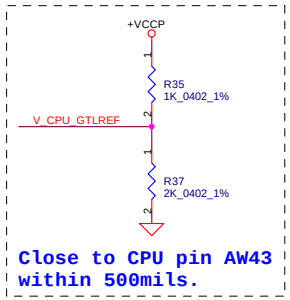


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

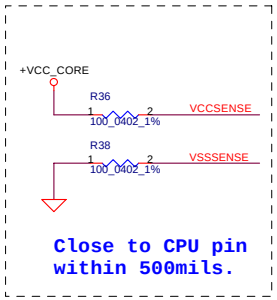
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.

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Title: **Penryn(2/3)-AGTL+/ITP-XDP**

Size	Document Number	Rev
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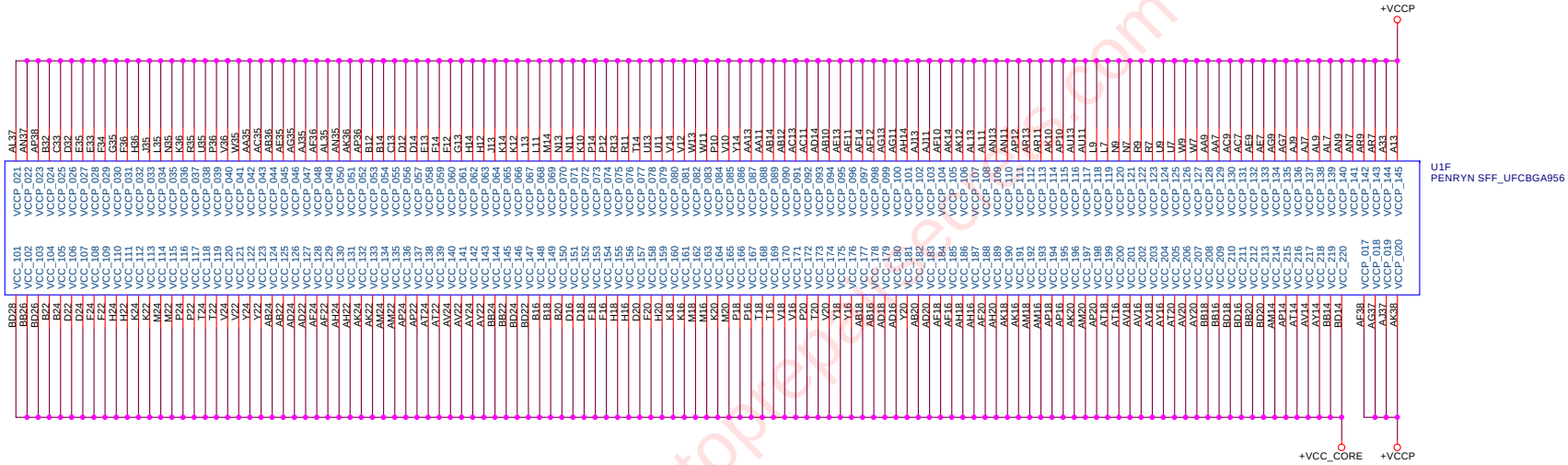

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Penryn(3/3)-Power**

Size	Document Number	Rev
Custom	LA-4021P	0.1

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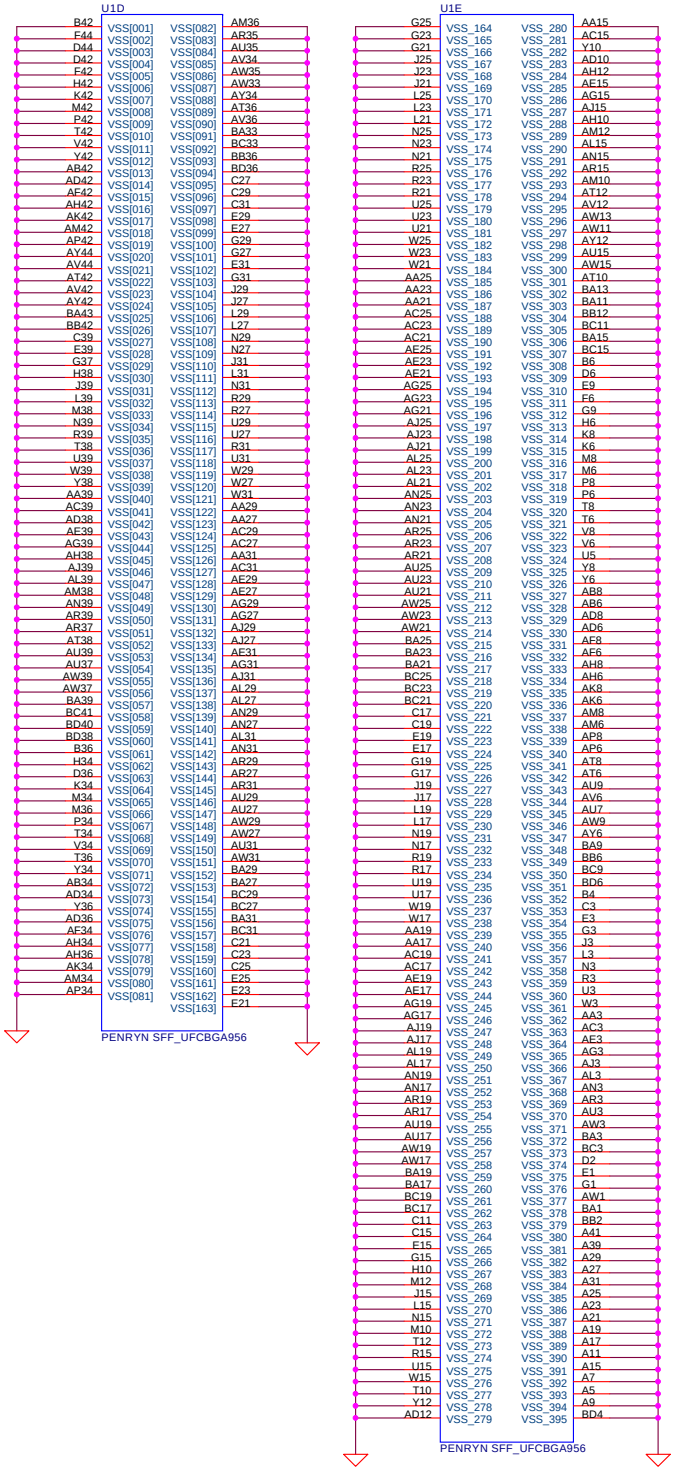
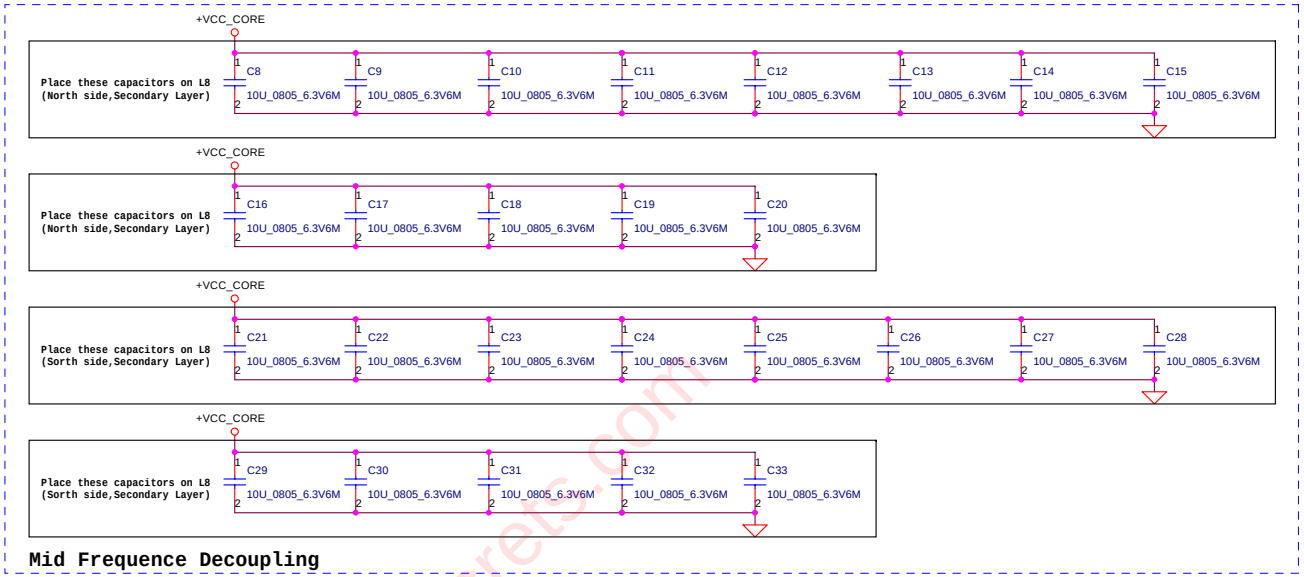
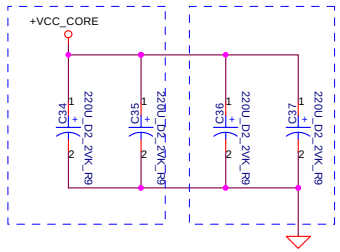


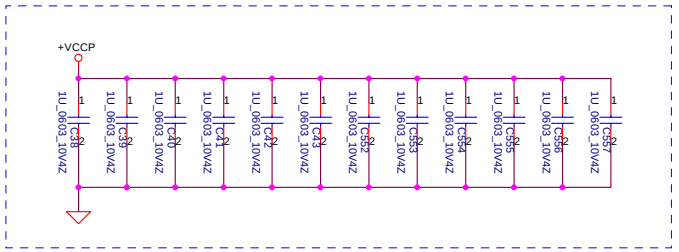


Mid Frequence Decoupling

Near CPU CORE regulator

ESR <= 1.5m ohm





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Compal Electronics, Inc.

Title: **Penryn(3/3)-GND/Bypass**

Size	Document Number	Rev
Custom	LA-4021P	0.1

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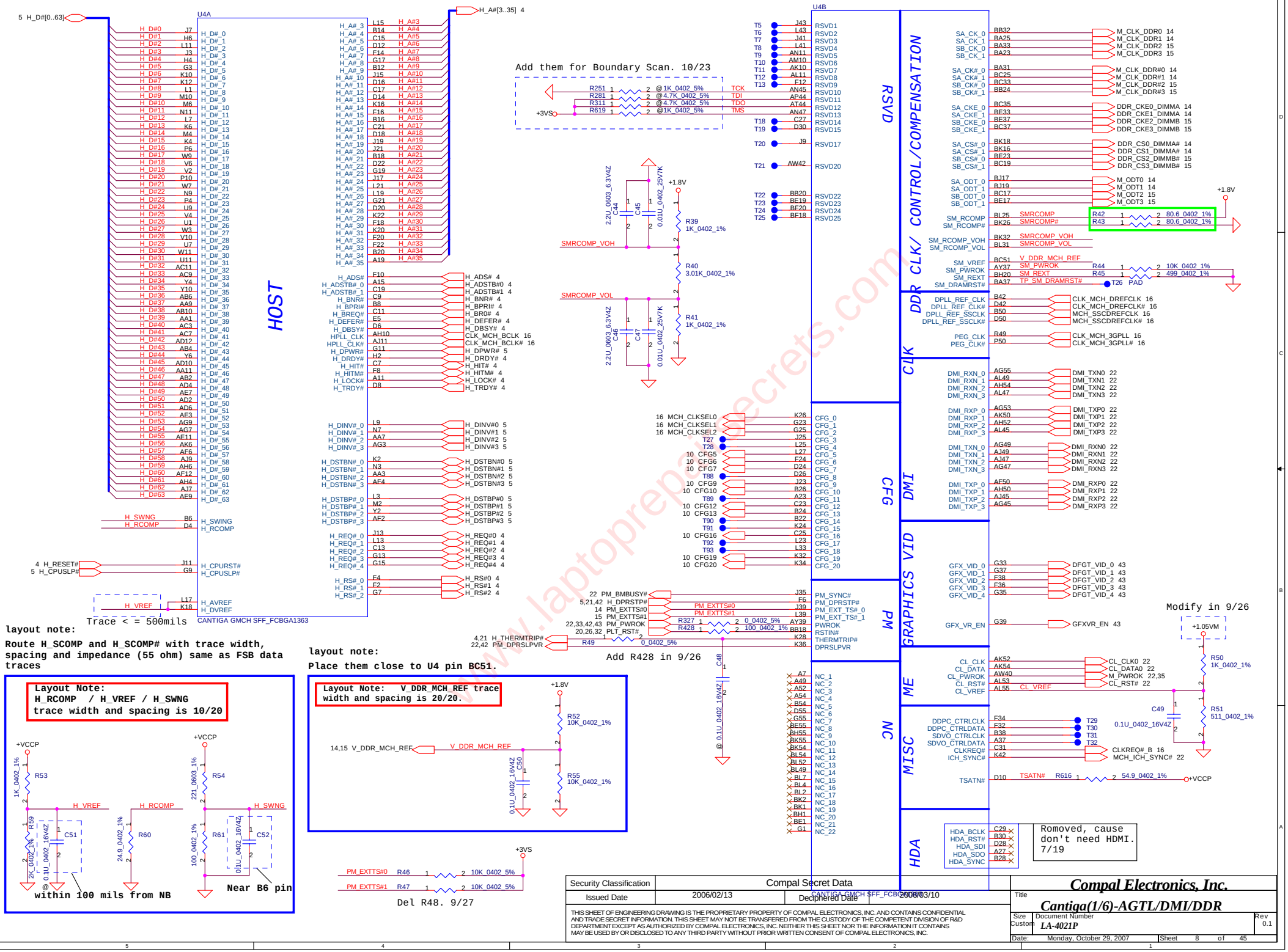
HOST
CANTIGA GMCH SFF_FCBGA1363
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
Add them for Boundary Scan. 10/23
TCK
TDI
TDO
TMS
SMRCOMP_VOH
SMRCOMP_VOL
Add R428 in 9/26
Modify in 9/26
Removed, cause don't need HDMI. 7/19
Trace < = 500mils
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB
Near B6 pin
layout note:
Place them close to U4 pin BC51.
Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.
Del R48. 9/27
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Compal Secret Data
Issued Date
2006/02/13
Deciphered Date
2006/03/10
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Cantiga(1/6)-AGTL/DMI/DDR
Size: Custom
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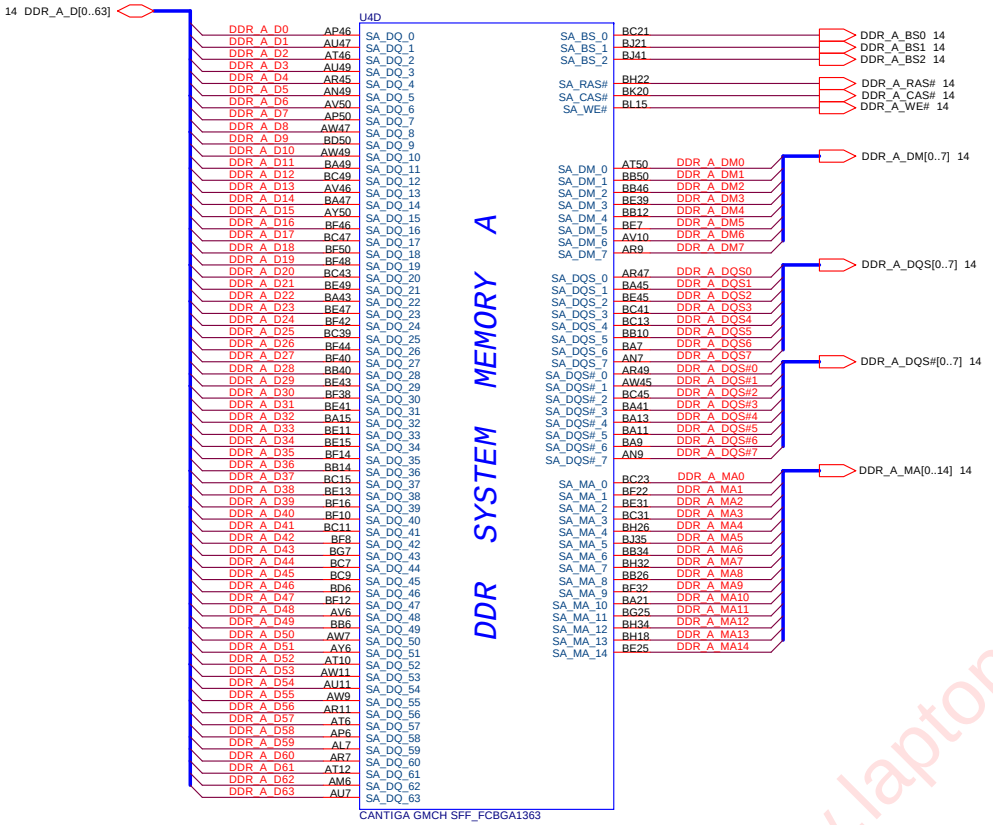

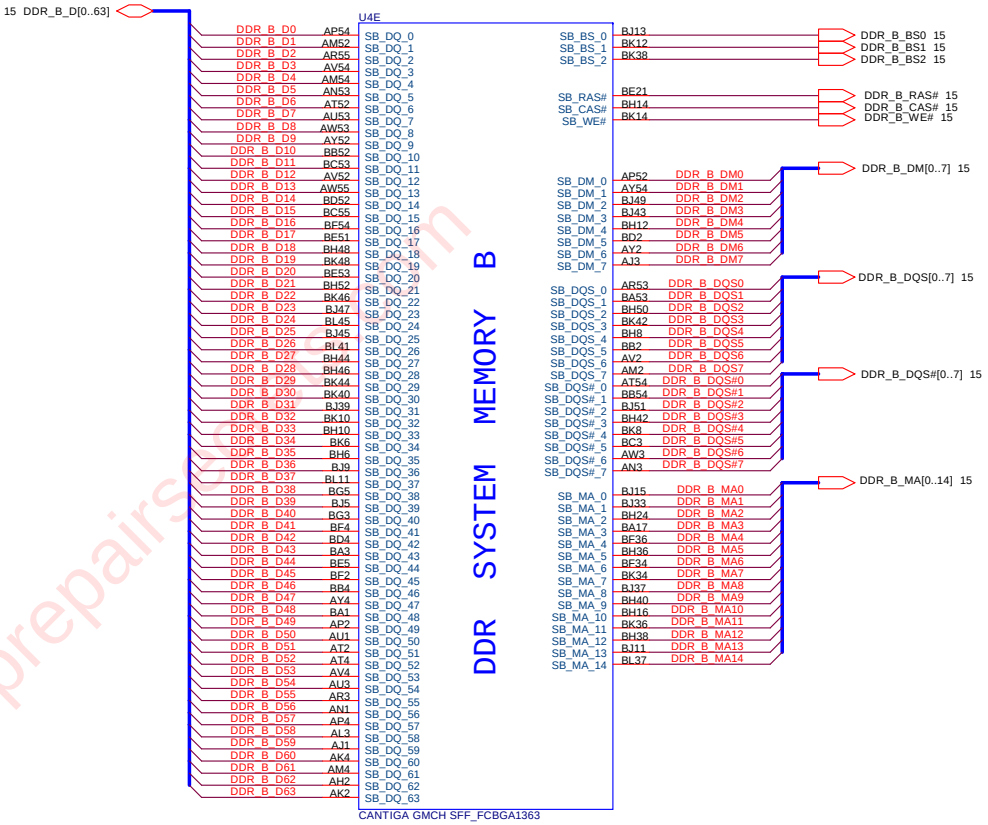

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Title: **Cantiga(2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	LA-4021P	0.1

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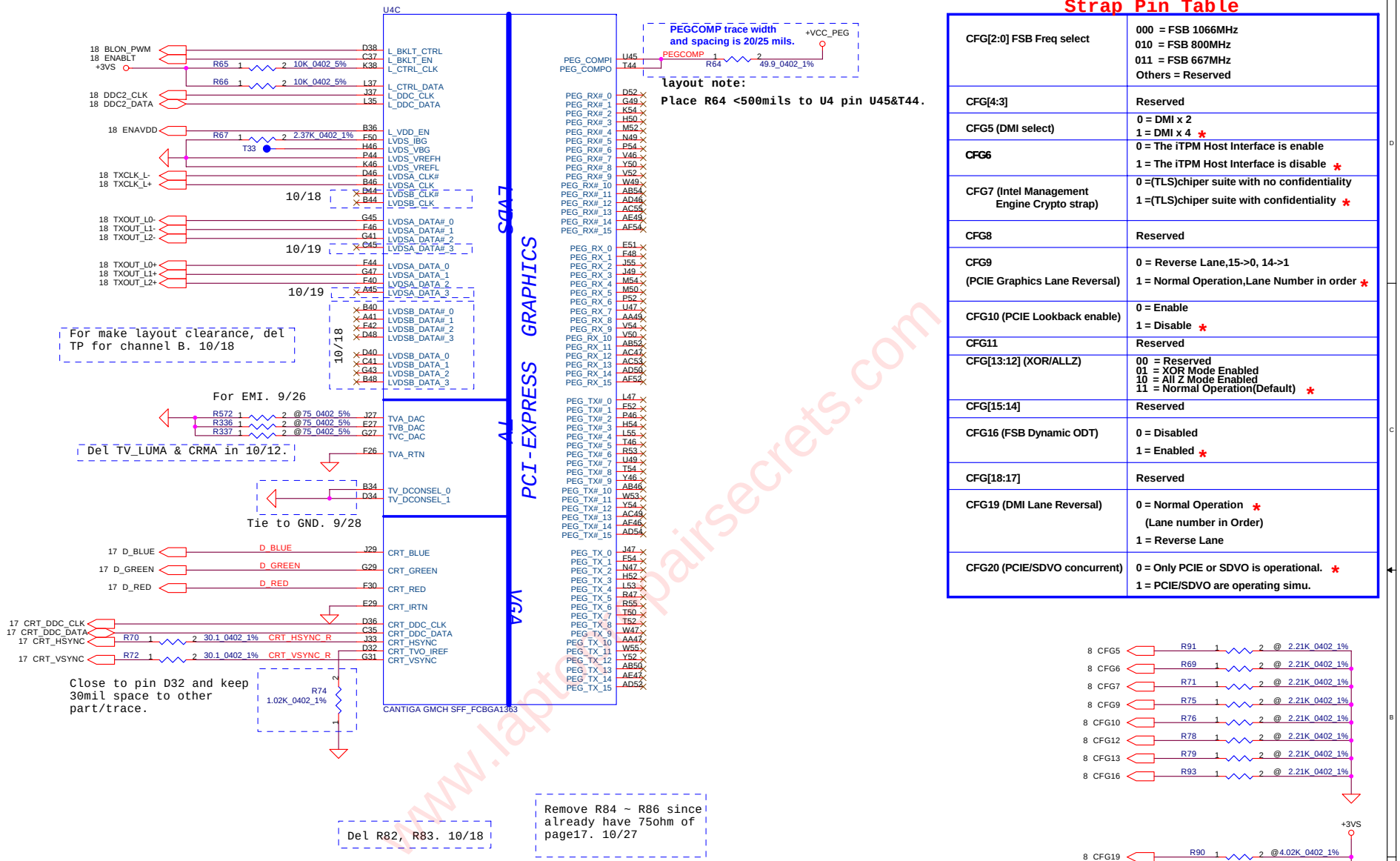

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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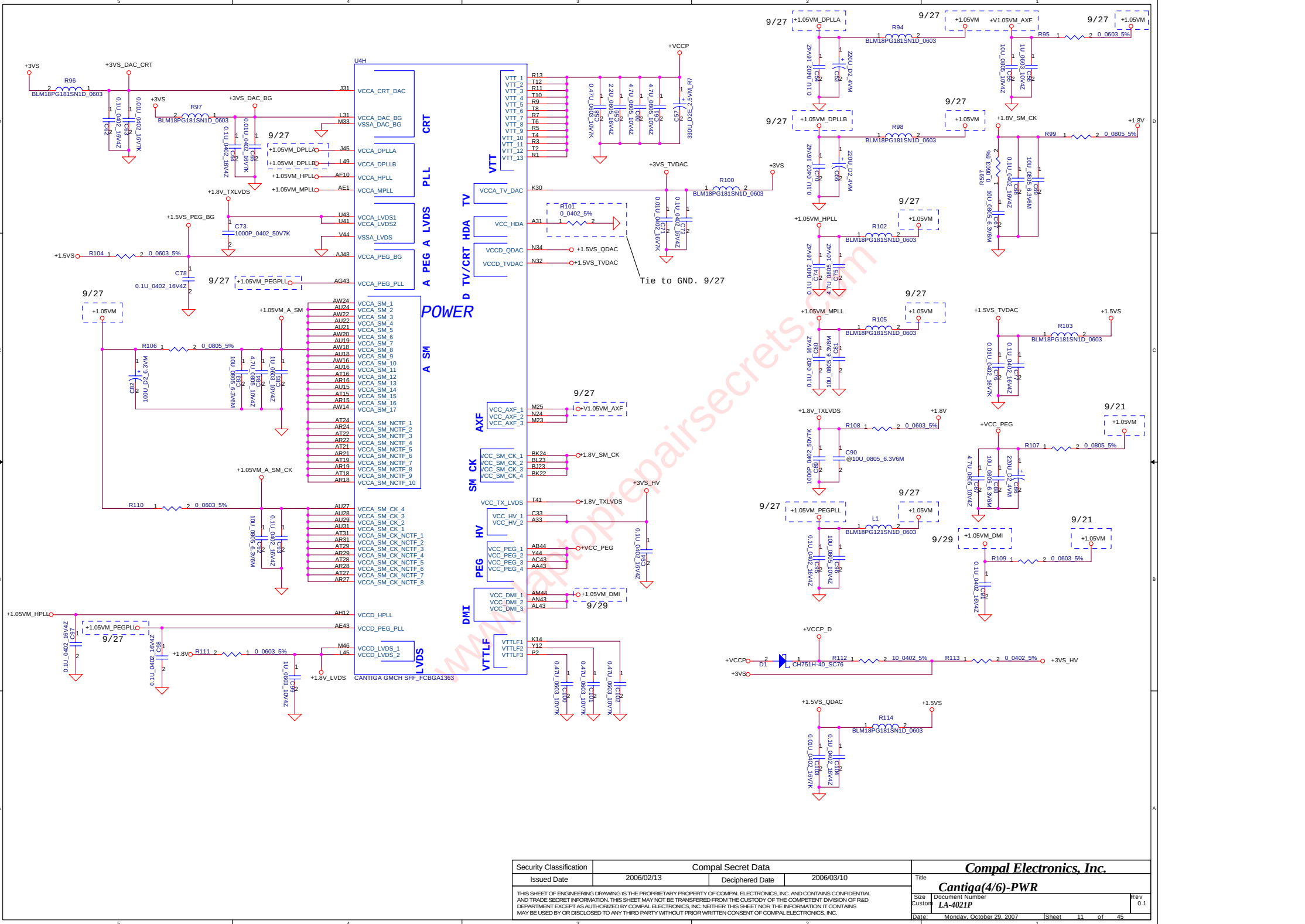
Custom	LA-4021P	0.1

Date: Monday, October 29, 2007 Sheet 10 of 45



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Title: **Cantiga(4/6)-PWR**

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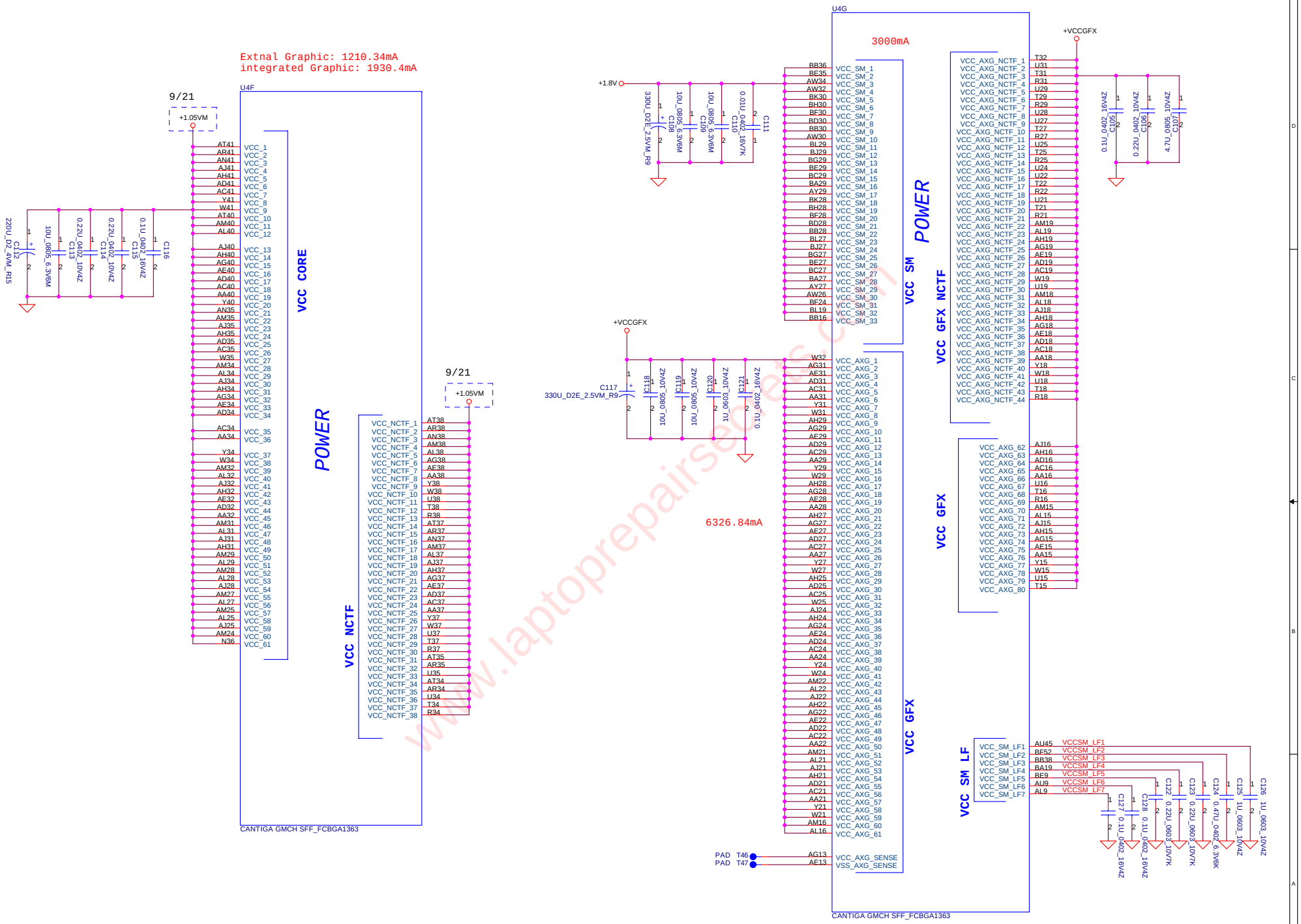

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Title: **Cantiga(5/6)-PWR/GND**

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Custom	LA-4021P	0.1

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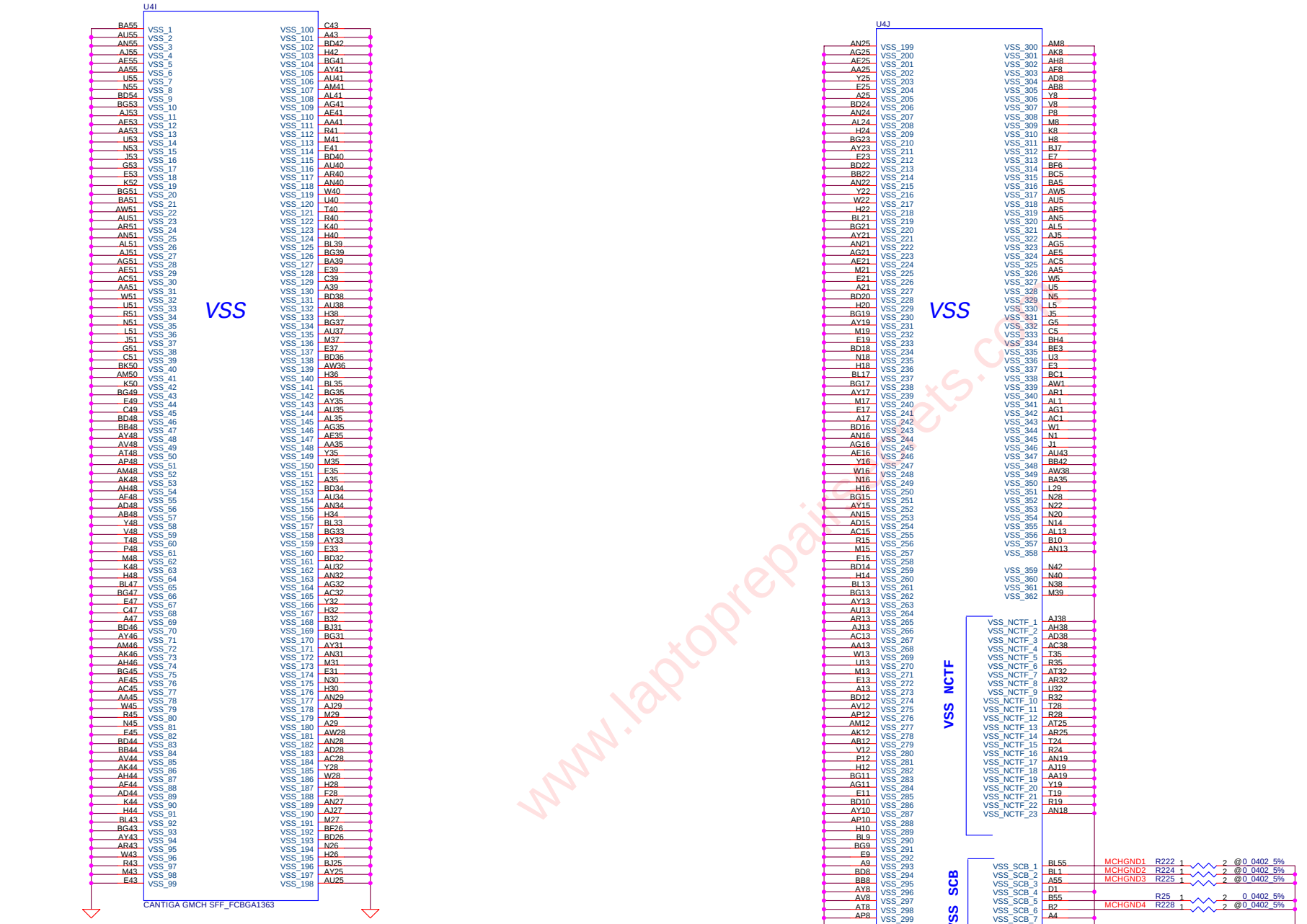

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Title: **Cantiga(6/6)-PWR/GND**

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9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]

Layout Note:
Place near JP36

+1.8V

Change C131 to 330uF. 9/26

C131 330U_D2E_2.5VM_R9
C132 2.2U_0805_16V4Z
C133 2.2U_0805_16V4Z
C134 2.2U_0805_16V4Z
C135 2.2U_0805_16V4Z
C136 2.2U_0805_16V4Z
C137 0.1U_0402_16V4Z
C138 0.1U_0402_16V4Z
C139 0.1U_0402_16V4Z
C140 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V

C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 0.1U_0402_16V4Z

+0.9V

DDR_A_MA5, DDR_A_MA8	RP1	RP2	DDR_A_BS2, DDR_CKE0_DIMMA
DDR_A_MA1, DDR_A_MA3	RP3	RP4	DDR_A_MA6, DDR_A_MA7
DDR_CS0_DIMMA#, DDR_A_RAS#	RP5	RP6	DDR_A_MA9, DDR_A_MA12
DDR_A_BS0, DDR_A_MA10	RP7	RP8	DDR_A_MA2, DDR_A_MA4
DDR_A_CAS#, DDR_A_WE#	RP9	RP10	DDR_A_BS1, DDR_A_MA0
DDR_CS1_DIMMA#, M_ODT1	RP11	RP12	DDR_A_MA13, M_ODT0
DDR_A_MA11	R117	RP13	DDR_A_MA14, DDR_CKE1_DIMMA

All: 56_0404_4P2R_5%, 56_0402_5%

Layout Note:
Place these resistor closely JP9,all trace length Max=1.5"

+1.8V +1.8V V_DDR_MCH_REF → V_DDR_MCH_REF 8,15

C129 2.2U_0805_16V4Z C130 0.1U_0402_16V4Z

JP36

	VREF	VSS	
DDR_A_D4	VSS	DQ4	DDR_A_D6
DDR_A_D1	DQ0	DQ5	DDR_A_D0
	DQ1	VSS	
DDR_A_DQS#0	VSS	DM0	DDR_A_DM0
DDR_A_DQS0	DQS#	VSS	
	DQS0	DQ6	DDR_A_D5
DDR_A_D2	VSS	DQ7	DDR_A_D7
DDR_A_D3	DQ2	VSS	
	DQ3	DQ12	DDR_A_D13
DDR_A_D8	VSS	DQ13	DDR_A_D12
DDR_A_D14	DQ8	VSS	
	DQ9	DM1	DDR_A_DM1
DDR_A_DQS#1	VSS	VSS	
DDR_A_DQS1	DQS1#	CK0	M_CLK_DDR0 8
	DQS1	CK0#	M_CLK_DDR#0 8
DDR_A_D9	VSS	VSS	
DDR_A_D15	DQ10	DQ14	DDR_A_D11
	DQ11	DQ15	DDR_A_D10
	VSS	VSS	
	VSS	VSS	
DDR_A_D16	DQ16	DQ20	DDR_A_D20
DDR_A_D17	DQ17	DQ21	DDR_A_D21
	VSS	VSS	
DDR_A_DQS#2	DQS2#	NC	PM_EXTTS#0 8
DDR_A_DQS2	DQS2	DM2	DDR_A_DM2
	VSS	VSS	
DDR_A_D18	DQ18	DQ22	DDR_A_D23
DDR_A_D19	DQ19	DQ23	DDR_A_D22
	VSS	VSS	
DDR_A_D29	DQ24	DQ28	DDR_A_D28
DDR_A_D24	DQ25	DQ29	DDR_A_D25
	VSS	VSS	
DDR_A_DM3	DM3	DQS3#	DDR_A_DQS#3
	NC	DQS3	DDR_A_DQS3
	VSS	VSS	
DDR_A_D26	DQ26	DQ30	DDR_A_D31
DDR_A_D27	DQ27	DQ31	DDR_A_D30
	VSS	VSS	
8 DDR_CKE0_DIMMA	CKE0	NC/CKE1	DDR_CKE1_DIMMA 8
	VDD	VDD	
	NC	NC/A15	
9 DDR_A_BS2	BA2	NC/A14	DDR_A_MA14
	VDD	VDD	
DDR_A_MA12	A12	A11	DDR_A_MA11
DDR_A_MA9	A9	A7	DDR_A_MA7
DDR_A_MA8	A8	A6	DDR_A_MA6
	VDD	VDD	
DDR_A_MA5	A5	A4	DDR_A_MA4
DDR_A_MA3	A3	A2	DDR_A_MA2
DDR_A_MA1	A1	A0	DDR_A_MA0
	VDD	VDD	
DDR_A_MA10	A10/AP	BA1	DDR_A_BS1 9
9 DDR_A_BS0 DDR_A_BS0	BA0	RAS#	DDR_A_RAS# 9
9 DDR_A_WE# DDR_A_WE#	WE#	S0#	DDR_CS0_DIMMA# DDR_CS0_DIMMA# 8
	VDD	VDD	
9 DDR_A_CAS# DDR_A_CAS#	CAS#	ODT0	M_ODT0 8 M_ODT0
8 DDR_CS1_DIMMA# DDR_CS1_DIMMA#	NC/S1#	NC/A13	DDR_A_MA13
	VDD	VDD	
8 M_ODT1 M_ODT1	NC/ODT1	NC	
	VSS	VSS	
DDR_A_D37	DQ32	DQ36	DDR_A_D39
DDR_A_D36	DQ33	DQ37	DDR_A_D38
	VSS	VSS	
DDR_A_DQS#4	DQS4#	DM4	DDR_A_DM4
DDR_A_DQS4	DQS4	VSS	
	VSS	DQ38	DDR_A_D34
DDR_A_D35	DQ34	DQ39	DDR_A_D33
DDR_A_D32	DQ35	VSS	
	VSS	DQ44	DDR_A_D45
DDR_A_D40	DQ40	DQ45	DDR_A_D43
DDR_A_D44	DQ41	VSS	
	VSS	DQS5#	DDR_A_DQS#5
DDR_A_DM5	DM5	DQS5	DDR_A_DQS5
	VSS	VSS	
DDR_A_D41	DQ42	DQ46	DDR_A_D47
DDR_A_D46	DQ43	DQ47	DDR_A_D42
	VSS	VSS	
DDR_A_D49	DQ48	DQ52	DDR_A_D52
DDR_A_D48	DQ49	DQ53	DDR_A_D53
	VSS	VSS	
	NC,TEST	CK1	M_CLK_DDR1 8
	VSS	CK1#	M_CLK_DDR#1 8
DDR_A_DQS#6	DQS6#	VSS	
DDR_A_DQS6	DQS6	DM6	DDR_A_DM6
	VSS	VSS	
DDR_A_D54	DQ50	DQ54	DDR_A_D51
DDR_A_D50	DQ51	DQ55	DDR_A_D55
	VSS	VSS	
DDR_A_D61	DQ56	DQ60	DDR_A_D57
DDR_A_D60	DQ57	DQ61	DDR_A_D56
	VSS	VSS	
DDR_A_DM7	DM7	DQS7#	DDR_A_DQS#7
	VSS	DQS7	DDR_A_DQS7
DDR_A_D59	DQ58	VSS	
DDR_A_D58	DQ59	DQ62	DDR_A_D62
	VSS	DQ63	DDR_A_D63
15,16,22 ICH_SMBDATA	SDA	VSS	
15,16,22 ICH_SMBCLK	SCL	SA0	
+3VM	VDDSPD	SA1	

conn@ FOX_ASOA426-M2RN-7F

C154 2.2U_0603_6.3V6K C155 0.1U_0402_16V4Z

R115 10K_0402_5% R116 10K_0402_5%

SO-DIMM A
4mm Height
Top side

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT**

Size	Document Number	Rev
	LA-4021P	0.1

Date: Monday, October 29, 2007 Sheet 14 of 45

9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..14]

Layout Note:
Place near JP34

+1.8V

Reserve C524. 9/26

C524 330U_D2E_2.5VM_R9 @
C566 2.2U_0805_16V4Z
C567 2.2U_0805_16V4Z
C568 2.2U_0805_16V4Z
C569 2.2U_0805_16V4Z
C570 2.2U_0805_16V4Z
C571 0.1U_0402_16V4Z
C572 0.1U_0402_16V4Z
C573 0.1U_0402_16V4Z
C574 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V

C575 C576 C577 C578 C579 C580 C581 C582 C583 C584 C585 C586 C587 0.1U_0402_16V4Z

Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"

+0.9V

DDR_B_MA1 / DDR_B_MA3	RP22	RP23	DDR_B_MA9 / DDR_B_MA12
DDR_B_BS0 / DDR_B_MA10	RP24	RP25	DDR_CKE3_DIMMB / DDR_B_MA14
DDR_B_MA0 / DDR_B_BS1	RP26	RP27	DDR_B_MA5 / DDR_B_MA8
DDR_B_RAS# / DDR_CS2_DIMMB#	RP28	RP29	DDR_B_MA7 / DDR_B_MA6
DDR_B_CAS# / DDR_B_WE#	RP30	RP31	DDR_B_MA4 / DDR_B_MA2
DDR_CS3_DIMMB# / M_ODT3	RP32	RP33	M_ODT2 / DDR_B_MA13
DDR_B_MA11	RP34		DDR_B_BS2 / DDR_CKE2_DIMMB

56_0404_4P2R_5%
R80 56_0402_5%

+1.8V +1.8V

V_DDR_MCH_REF → V_DDR_MCH_REF 8,14

C564 2.2U_0805_16V4Z
C565 0.1U_0402_16V4Z

JP3

	VREF	VSS			
DDR_B_D57 / DDR_B_D56	VSS	DQ4	DDR_B_D60 / DDR_B_D61		
	DQ0	DQ5			
	DQ1	VSS	DDR_B_DM7		
DDR_B_DQS#7 / DDR_B_DQS7	VSS	DM0			
	DQS0#	VSS			
	DQS0	DQ6	DDR_B_D62 / DDR_B_D59		
DDR_B_D58 / DDR_B_D63	VSS	DQ7			
	DQ2	VSS			
	DQ3	DQ12	DDR_B_D52 / DDR_B_D53		
DDR_B_D48 / DDR_B_D49	VSS	DQ13			
	DQ8	VSS			
	DQ9	DM1	DDR_B_DM6		
DDR_B_DQS#6 / DDR_B_DQS6	VSS	VSS			
	DQS1#	CK0	M_CLK_DDR3 8		
	DQS1	CK0#	M_CLK_DDR#3 8		
DDR_B_D51 / DDR_B_D50	VSS	VSS			
	DQ10	DQ14	DDR_B_D54 / DDR_B_D55		
	DQ11	DQ15			
	VSS	VSS			
DDR_B_D40 / DDR_B_D44	VSS	VSS	DDR_B_D45 / DDR_B_D41		
	DQ16	DQ20			
	DQ17	DQ21			
DDR_B_DQS#5 / DDR_B_DQS5	VSS	VSS			
	DQS2#	NC	PM_EXTTS#1 8		
	DQS2	DM2	DDR_B_DM5		
DDR_B_D42 / DDR_B_D47	VSS	VSS			
	DQ18	DQ22	DDR_B_D46 / DDR_B_D43		
	DQ19	DQ23			
DDR_B_D37 / DDR_B_D32	VSS	VSS			
	DQ24	DQ28	DDR_B_D36 / DDR_B_D33		
	DQ25	DQ29			
DDR_B_DM4	VSS	VSS			
	DM3	DQS3#	DDR_B_DQS#4 / DDR_B_DQS4		
	NC	DQS3			
DDR_B_D39 / DDR_B_D35	VSS	VSS			
	DQ26	DQ30	DDR_B_D34 / DDR_B_D38		
	DQ27	DQ31			
8 DDR_CKE2_DIMMB	CKE0	NC/CKE1	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB 8	
	VDD	VDD			
9 DDR_B_BS2	NC	NC/A15			
	BA2	NC/A14	DDR_B_MA14		
DDR_B_MA12 / DDR_B_MA9 / DDR_B_MA8	VDD	VDD			
	A12	A11	DDR_B_MA11 / DDR_B_MA7 / DDR_B_MA6		
	A9	A7			
	A8	A6			
DDR_B_MA5 / DDR_B_MA3 / DDR_B_MA1	VDD	VDD			
	A5	A4	DDR_B_MA4 / DDR_B_MA2 / DDR_B_MA0		
	A3	A2			
	A1	A0			
DDR_B_MA10	VDD	VDD			
9 DDR_B_BS0 / DDR_B_BS0	A10/AP	BA1	DDR_B_BS1	DDR_B_BS1 9	
9 DDR_B_WE# / DDR_B_WE#	BA0	RAS#	DDR_B_RAS#	DDR_B_RAS# 9	
	WE#	S0#	DDR_CS2_DIMMB#	DDR_CS2_DIMMB# 8	
	VDD	VDD			
9 DDR_B_CAS# / DDR_B_CAS#	CAS#	ODT0	M_ODT2	M_ODT2 8	
8 DDR_CS3_DIMMB# / DDR_CS3_DIMMB#	NC/S1#	NC/A13	DDR_B_MA13		
	VDD	VDD			
8 M_ODT3 / M_ODT3	NC/ODT1	NC			
	VSS	VSS			
DDR_B_D30 / DDR_B_D27	DQ32	DQ36	DDR_B_D26 / DDR_B_D31		
	DQ33	DQ37			
	VSS	VSS			
DDR_B_DQS#3 / DDR_B_DQS3	DQS4#	DM4	DDR_B_DM3		
	DQS4	VSS			
	VSS	DQ38	DDR_B_D24 / DDR_B_D29		
DDR_B_D25 / DDR_B_D28	DQ34	DQ39			
	DQ35	VSS			
	VSS	DQ44	DDR_B_D18 / DDR_B_D19		
DDR_B_D23 / DDR_B_D22	DQ40	DQ45			
	DQ41	VSS			
DDR_B_DM2	VSS	DQS5#	DDR_B_DQS#2 / DDR_B_DQS2		
	DM5	DQS5			
	VSS	VSS			
DDR_B_D17 / DDR_B_D16	DQ42	DQ46	DDR_B_D21 / DDR_B_D20		
	DQ43	DQ47			
	VSS	VSS			
DDR_B_D11 / DDR_B_D10	DQ48	DQ52	DDR_B_D14 / DDR_B_D15		
	DQ49	DQ53			
	VSS	VSS			
	NC,TEST	CK1	M_CLK_DDR2 8		
	VSS	CK1#	M_CLK_DDR#2 8		
DDR_B_DQS#1 / DDR_B_DQS1	DQS6#	VSS			
	DQS6	DM6	DDR_B_DM1		
	VSS	VSS			
DDR_B_D12 / DDR_B_D9	DQ50	DQ54	DDR_B_D13 / DDR_B_D8		
	DQ51	DQ55			
	VSS	VSS			
DDR_B_D2 / DDR_B_D3	DQ56	DQ60	DDR_B_D7 / DDR_B_D6		
	DQ57	DQ61			
	VSS	VSS			
DDR_B_DM0	DM7	DQS7#	DDR_B_DQS#0 / DDR_B_DQS0		
	VSS	DQS7			
	DQ58	VSS			
DDR_B_D0 / DDR_B_D5	DQ59	DQ62	DDR_B_D1 / DDR_B_D4		
	VSS	DQ63			
	SDA	VSS			
14,16,22 ICH_SMBDATA / 14,16,22 ICH_SMBCLK	SCL	SAO			
	VDDSPD	SA1			

SUYIN_600008FB200G103ZL

+3VM

C588 2.2U_0603_9.3V6K
C589 0.1U_0402_16V4Z

R73 10K_0402_5% → +3VM
R77 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT**

Size	Document Number	Rev
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

Place close to U5

Add for PCIE port80 debug port. 10/18.

9/14

9/20

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

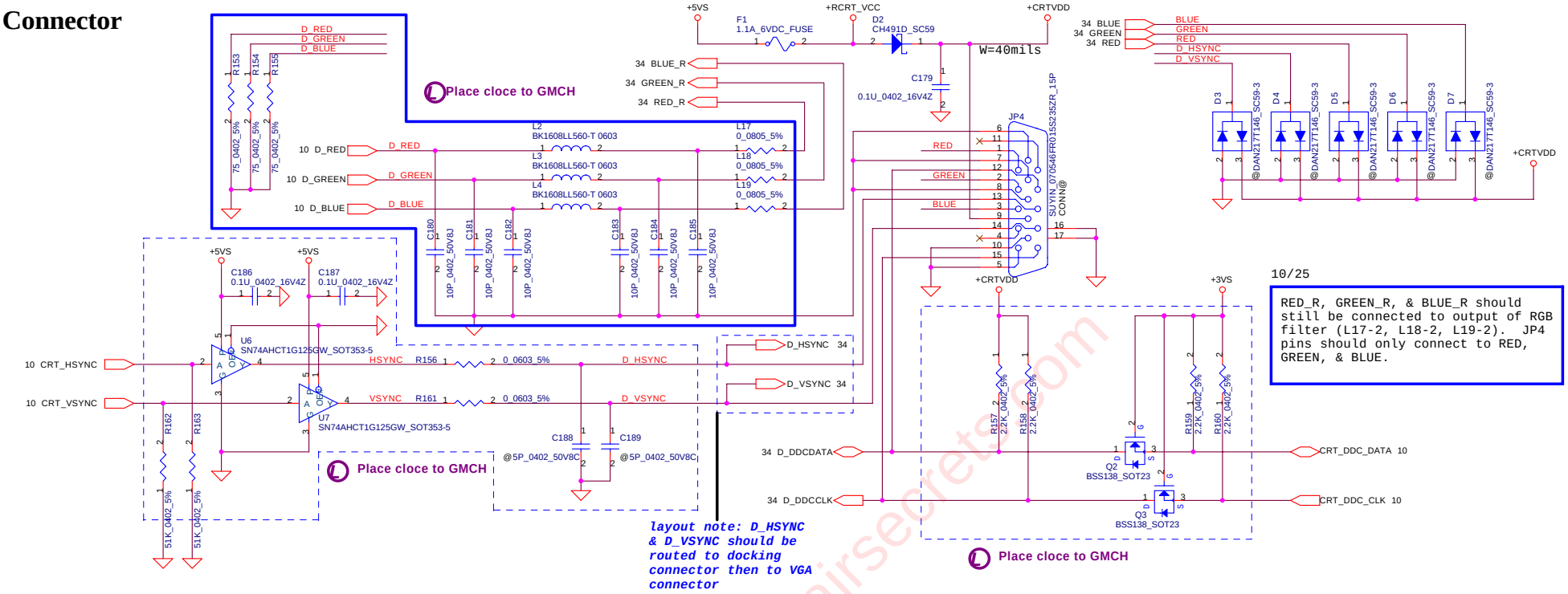
Compal Electronics, Inc.

Title: CLOCK GENERATOR

Size: | Document Number: LA-4021P | Rev: 0.1

Date: Monday, October 29, 2007 | Sheet 16 of 45

CRT Connector

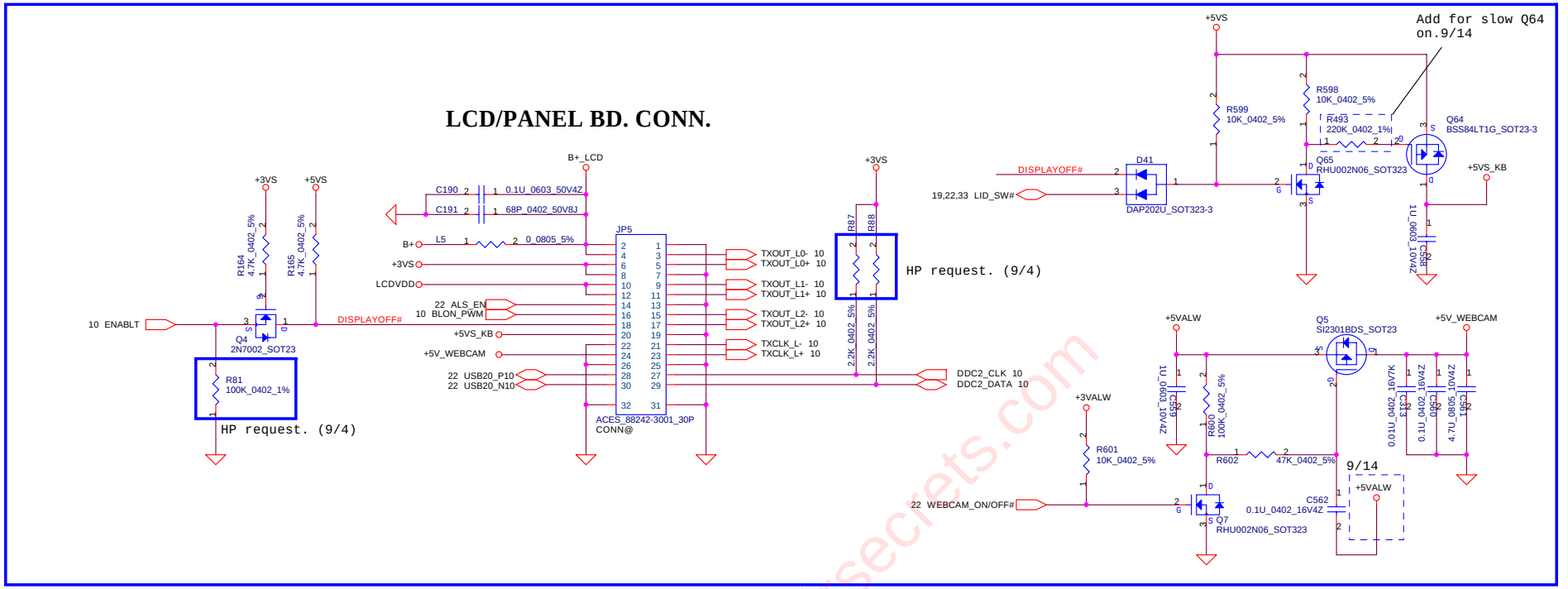


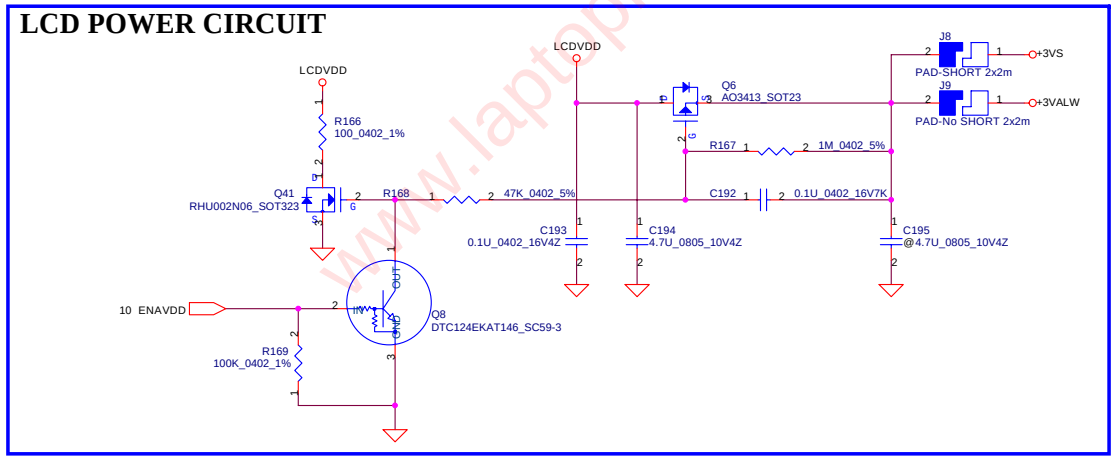
10/25

RED_R, GREEN_R, & BLUE_R should still be connected to output of RGB filter (L17-2, L18-2, L19-2). JP4 pins should only connect to RED, GREEN, & BLUE.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: CRT Connector			
Size	Document Number: LA-4021P		Rev: 0.1
Date: Monday, October 29, 2007	Sheet 17 of 45		





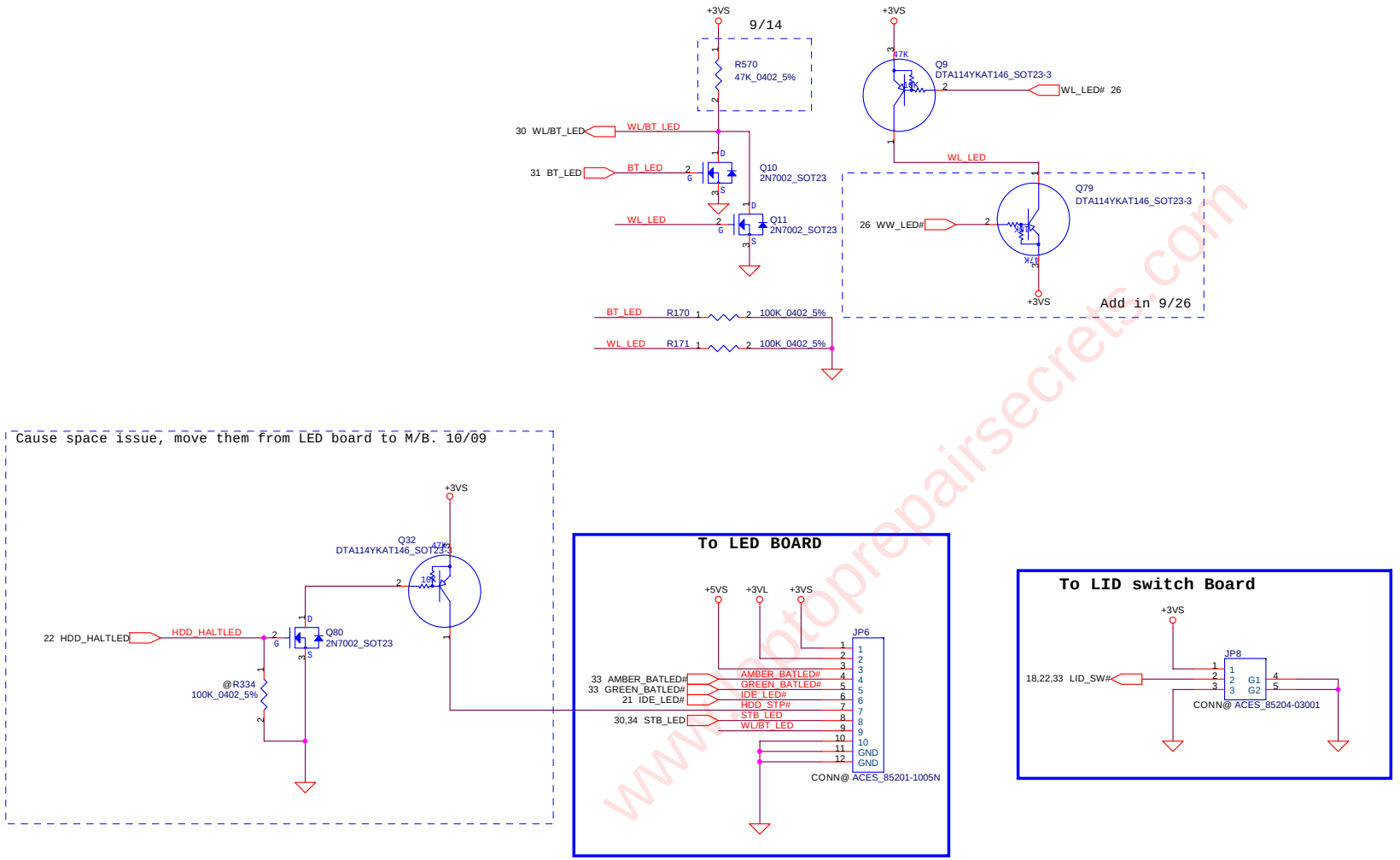
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **LCD CONN & Q-Switch & GPIO Ext.**

Size	Document Number	Rev
	LA-4021P	0.1

Date: Monday, October 29, 2007 | Sheet 18 of 45



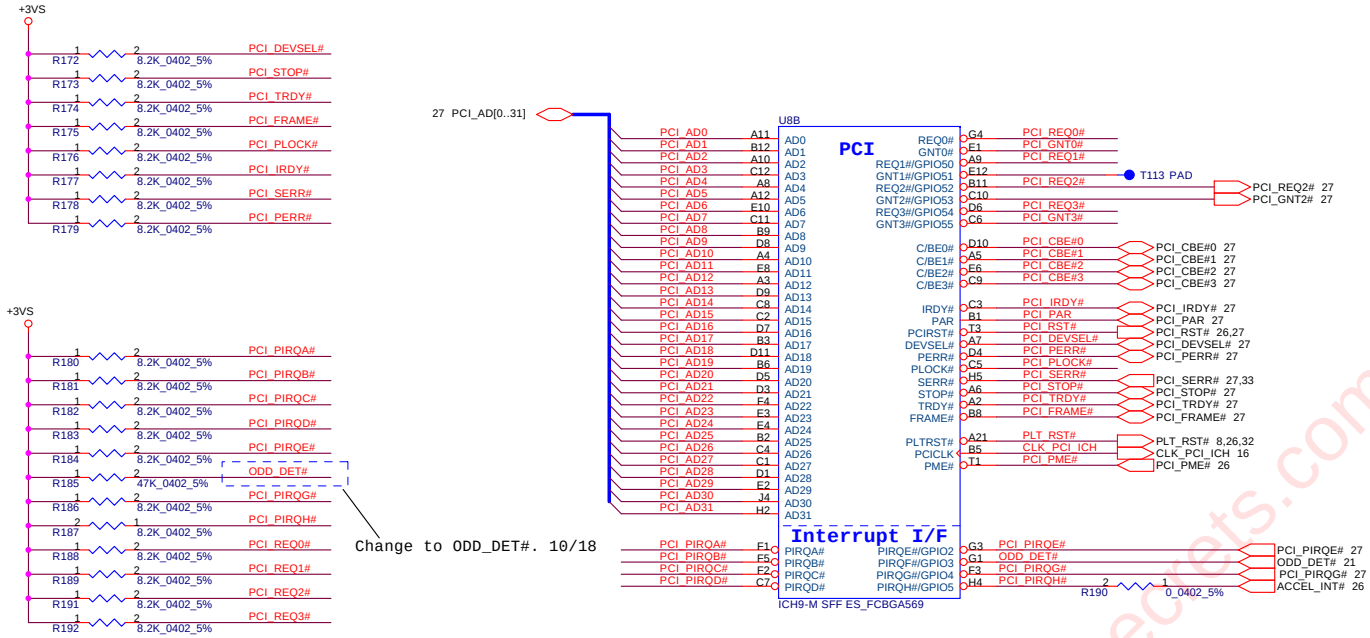
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

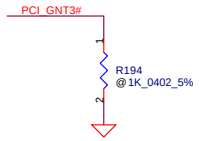
Title: **LEDS & LID**

Size	Document Number	Rev
Custom	LA-4021P	0.1

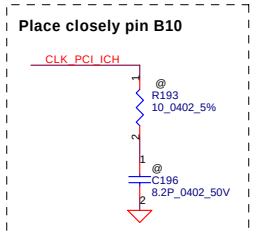
Date: Monday, October 29, 2007 | Sheet 19 of 45

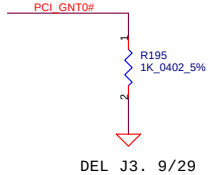


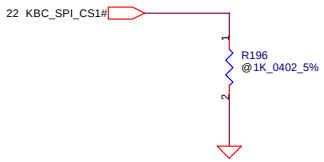
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



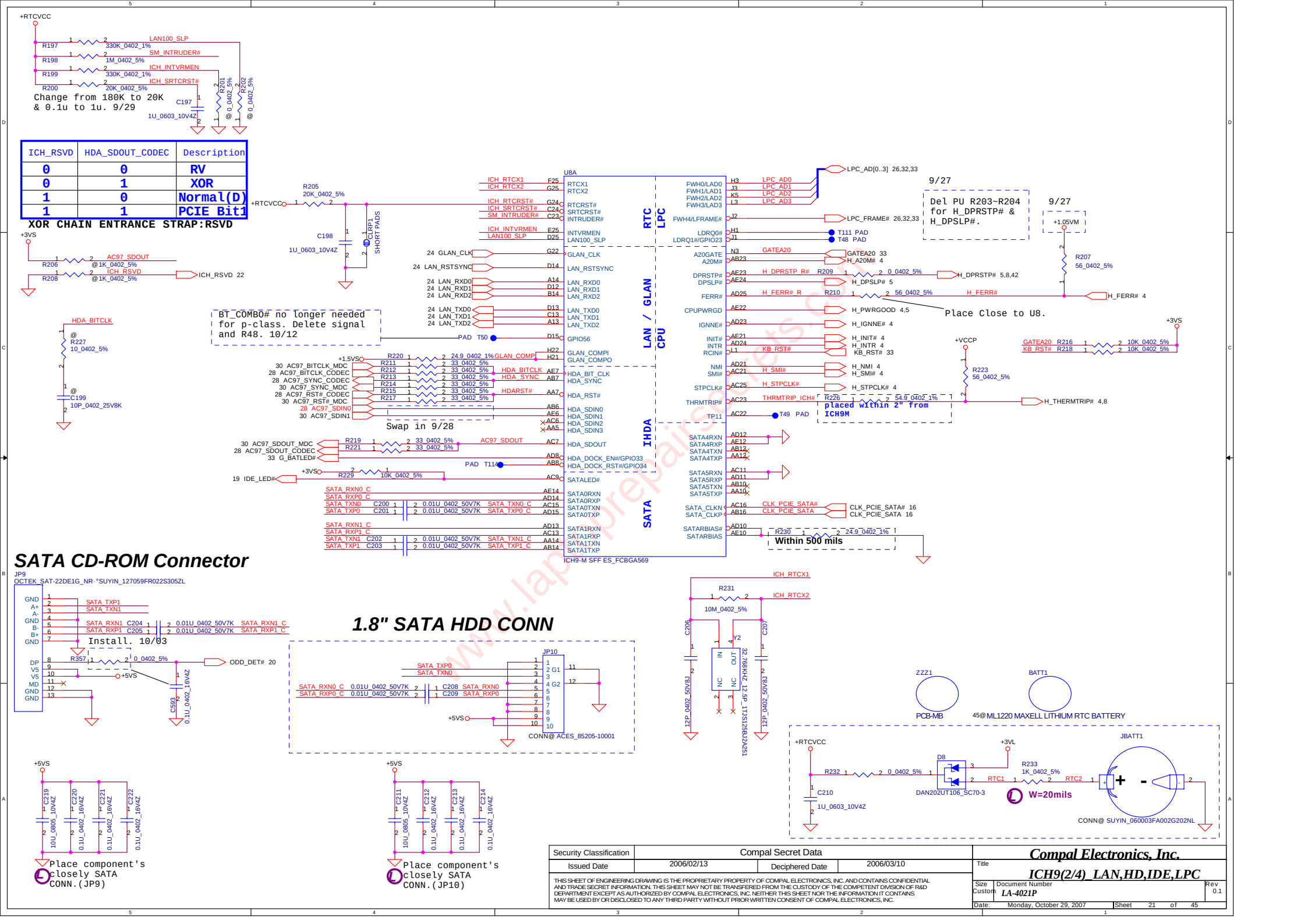




DEL J3. 9/29

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title	ICH9(1/4)-PCI/INT		
Size	Document Number LA-4021P		Rev 0.1
Date: Monday, October 29, 2007		Sheet 20 of 45	



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH9(2/4)_LAN,HD,IDE,LPC**

Size	Document Number	Rev
Custom	LA-4021P	0.1

Date: Monday, October 29, 2007 Sheet 21 of 45

Add R326 10K. 10/04

Del R244. 9/27

Del PU for GPIO39. 9/27

Change R238 connect to GPI011. 9/27

Change from ODD_DET# to GPIO19. 10/18

9/21

Add in 9/27

Add R321 in 10/03.

Add R331 in 10/08.
Change R269 to 10K. 9/29
Del R261, R264, R267 cause no used in 9/21.

Change in 7/13

Reserve in 10/08.

Change R251 to CH751. 10/04

Add EXP_RST# in 10/09.

R276 low -->default
High -->No boot

Change design in 10/08.

Add in 9/14.
Add RP15 back. 9/27
Add in 10/10.

Reserve for DB1 test. 10/05

Reserve R254 at 9/19.

Add for find tune timing.(If have glich issue)

Add WOL_EN back. 10/10

Add in 10/04.

Within 500 mils

Within 500 mils

Pin connection error, modify in 10/24.

Place closely pin AF3

Place closely pin H1

U8C

ICH9-M SFF ES_FCBGA569

U8D

ICH9-M SFF ES_FCBGA569

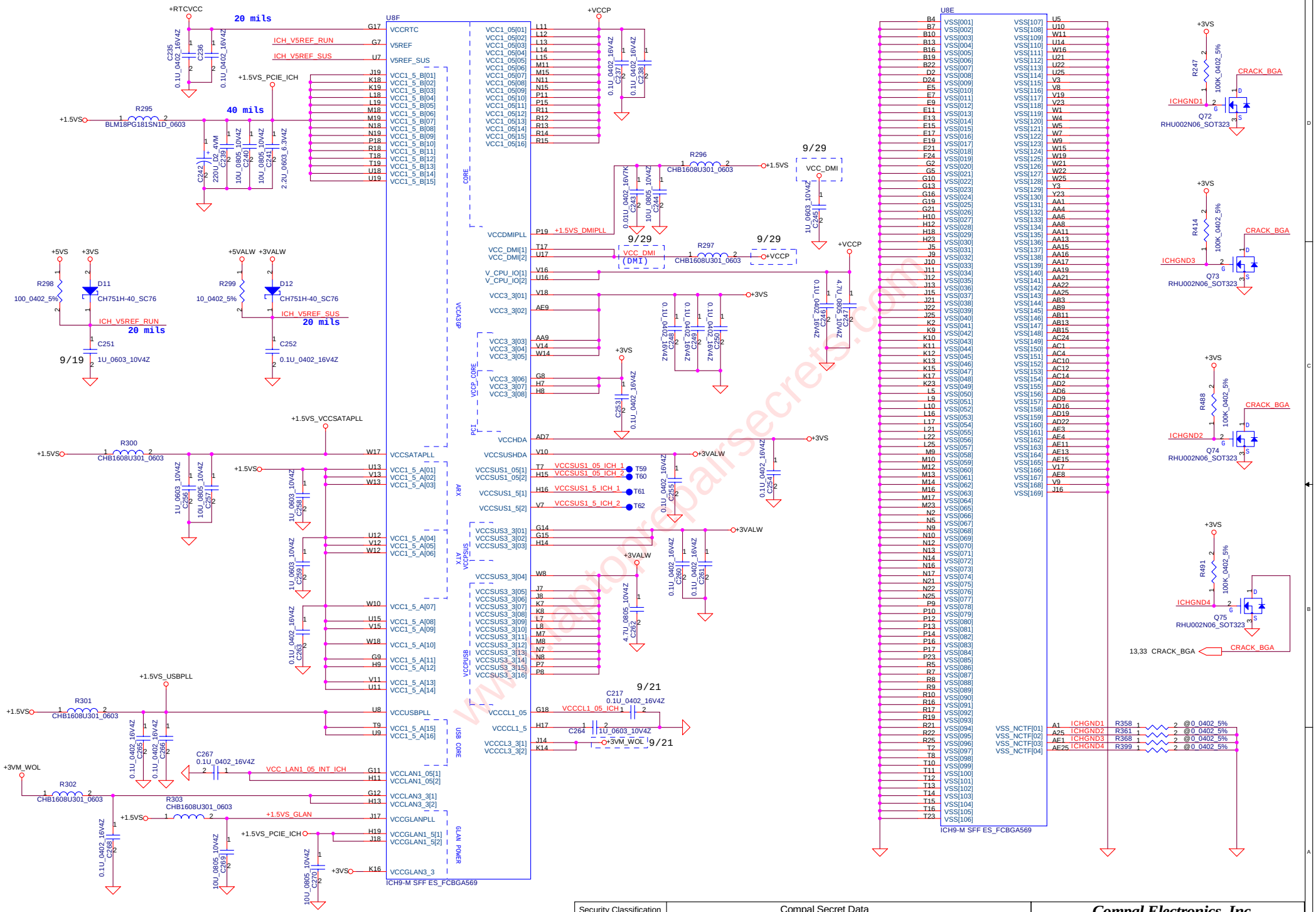
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH9(3/4)_DMI,USB,GPIO,PCIE**

Size	Document Number	Rev
Custom	LA-4021P	0.1

Date: Monday, October 29, 2007 Sheet 22 of 45



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH9(4/4)_POWER&GND**

Size	Document Number	Rev
Custom	LA-4021P	0.1

Date: Monday, October 29, 2007 | Sheet 23 of 45

ACBS is built into Nineveh, so reserve these parts for test. (9/4)

Install R308. 9/29

Add R309 back. 9/29

Change R315 to 1K and R316 to 10K. 10/10

Del R311 and modify net name to +V1.0M_LAN. 10/18

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

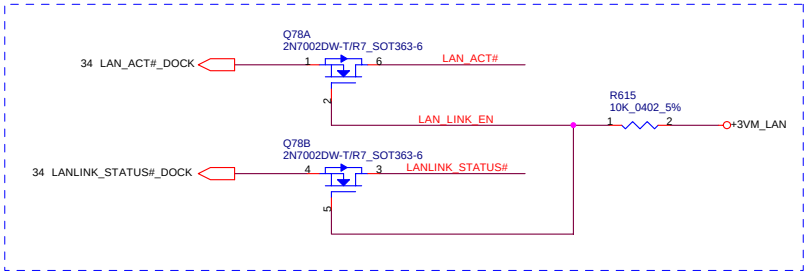
Title: **Intel 82566 Nineveh**

Size: | Document Number: *LA-4021P* | Rev: 0.1

Date: Monday, October 29, 2007 | Sheet 24 of 45

Del LAN ENERGY DET cause already inside the BOAZ. 9/27

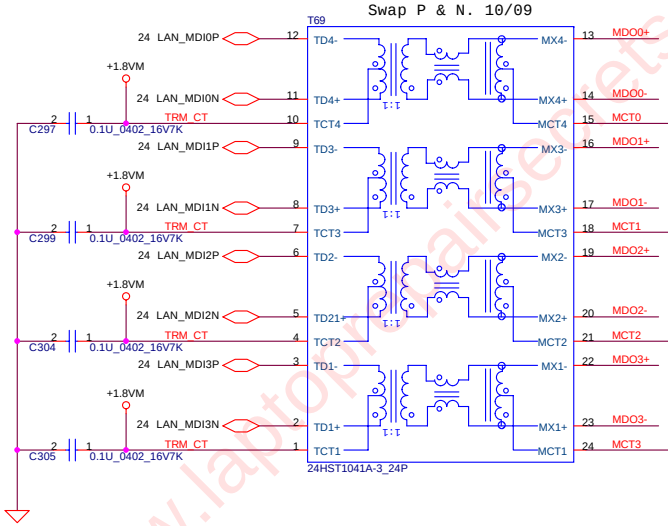
LAN status/link level shift. 9/21



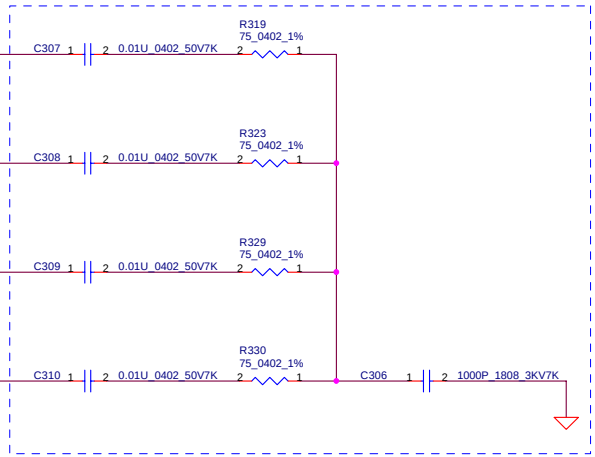
Delete all termination cause they are already inside BOAZMAN. 9/28

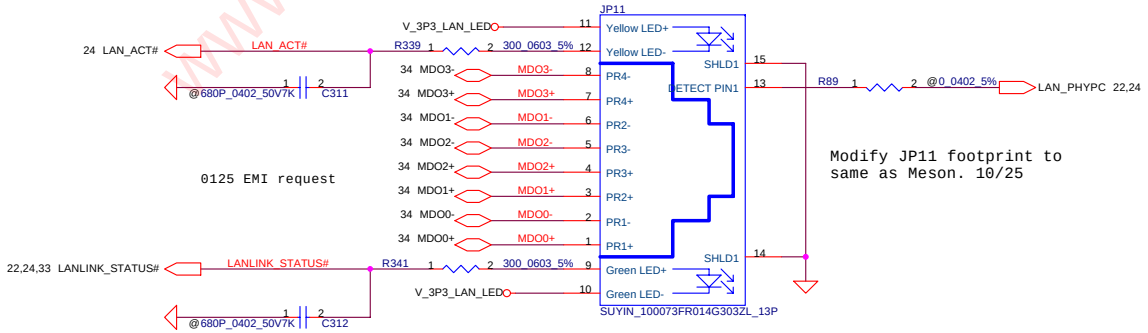
Pin Swap. 10/05

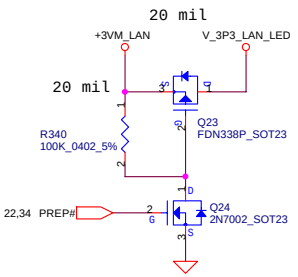
Swap P & N. 10/09



Change design. 10/12



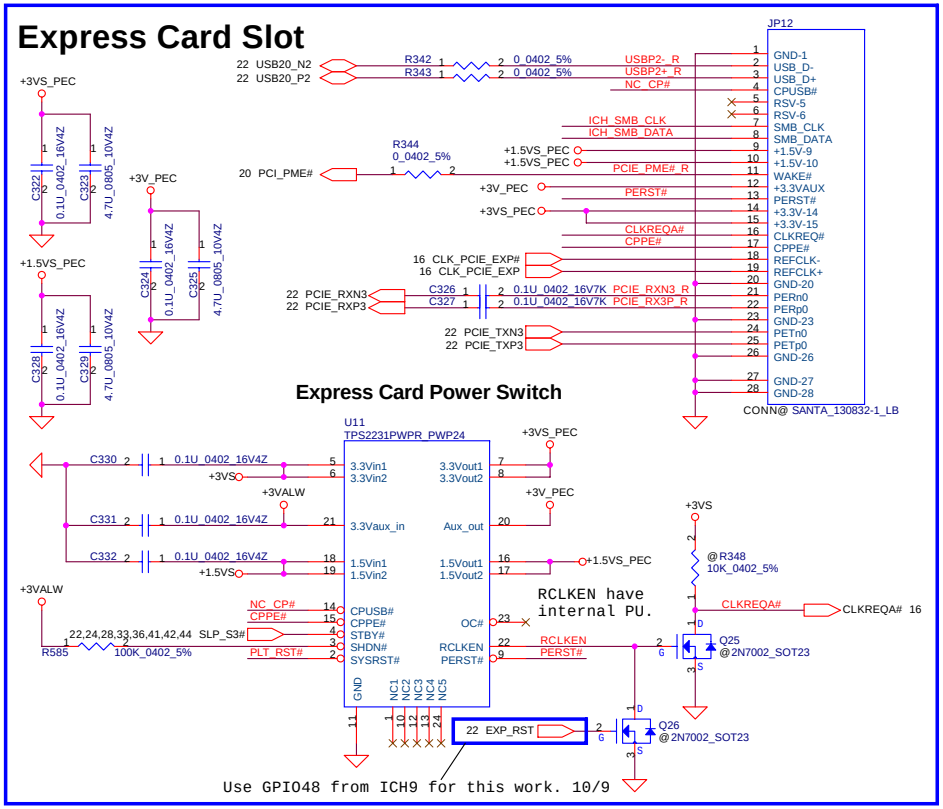




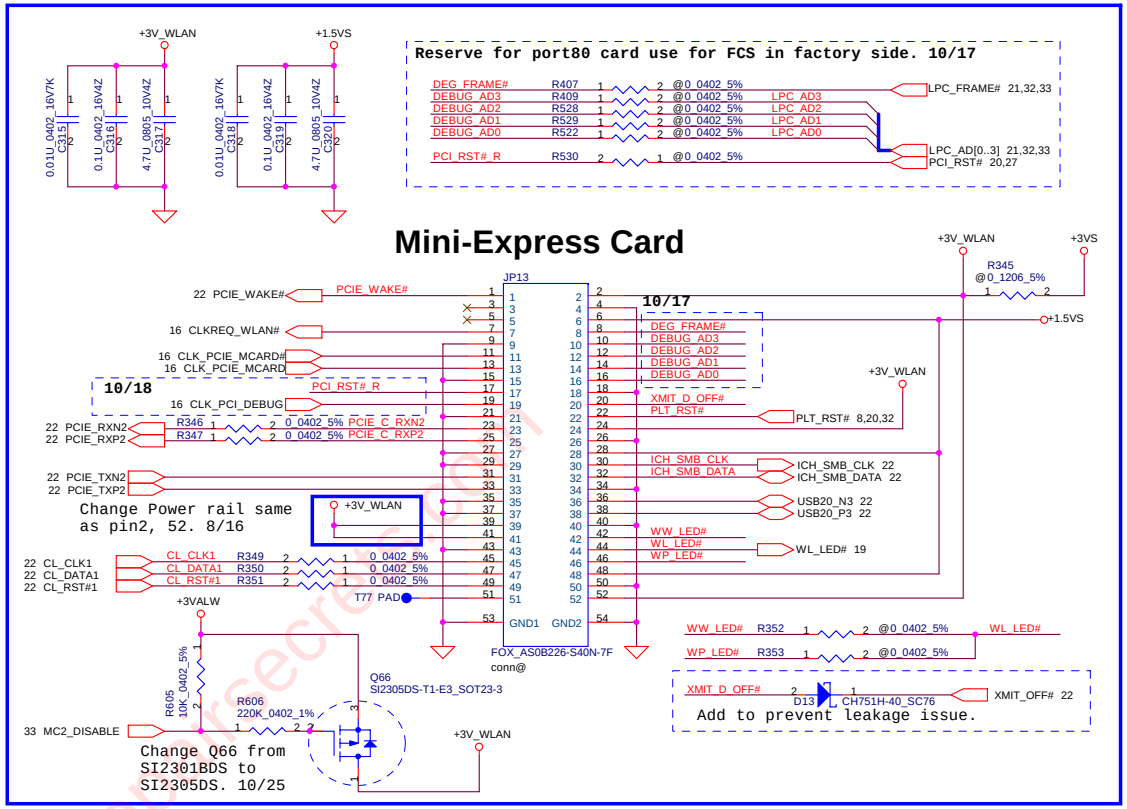
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title	Magnetic & RJ45		
Size	Document Number		Rev
	LA-4021P		0.1
Date:	Monday, October 29, 2007	Sheet	25 of 45

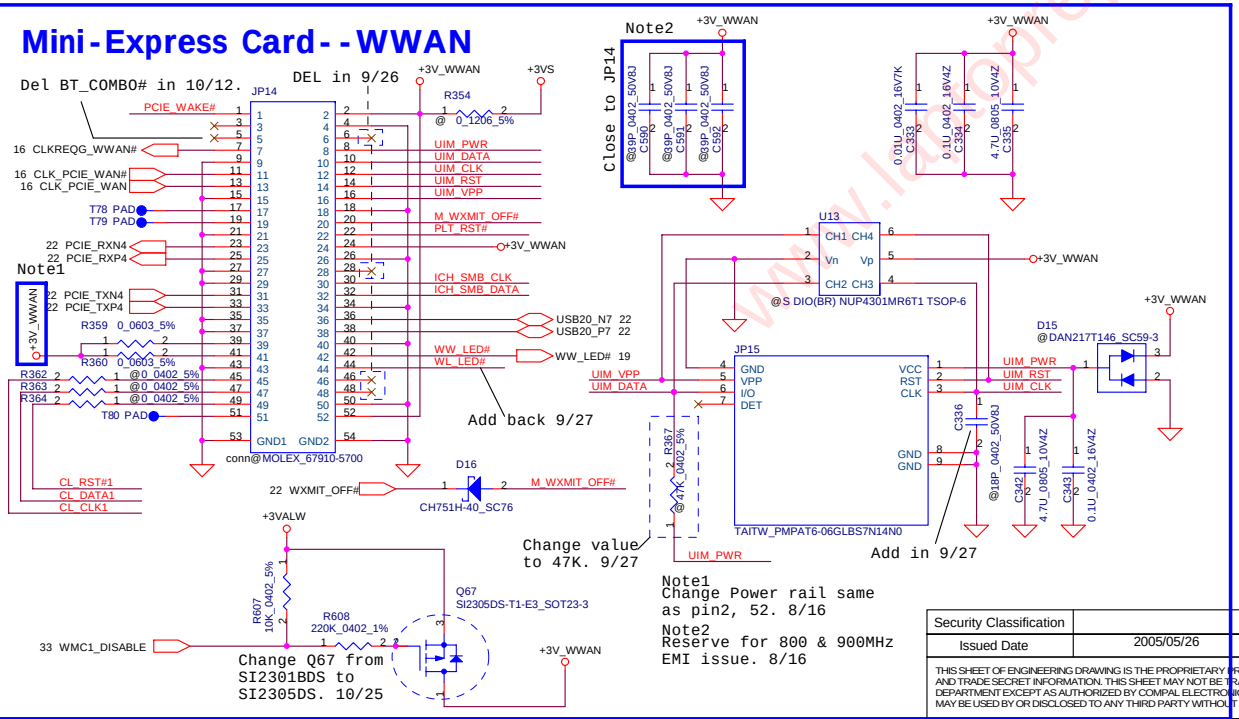
Express Card Slot



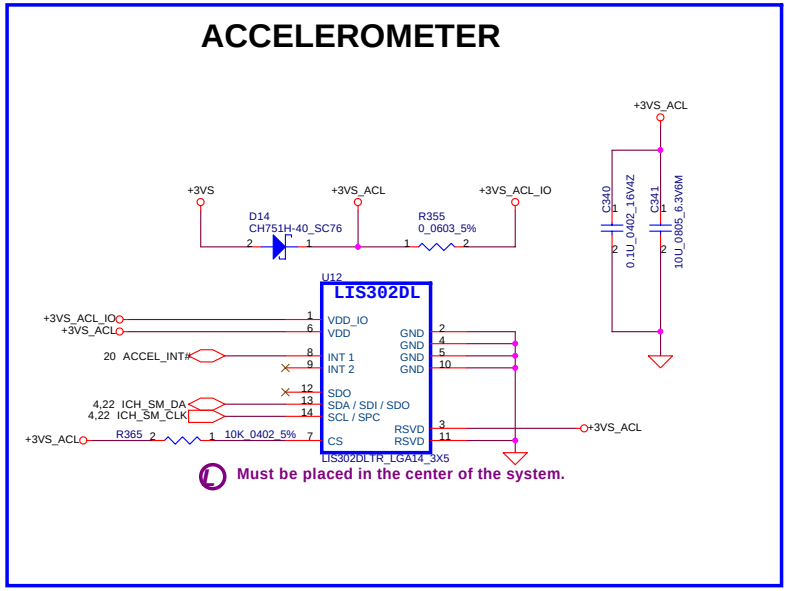
Mini-Express Card



Mini-Express Card--WWAN



ACCELEROMETER



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **WLAN&WWAN Mini-Card/Accelerometer**

Size	Document Number	Rev
	LA-4021P	0.1

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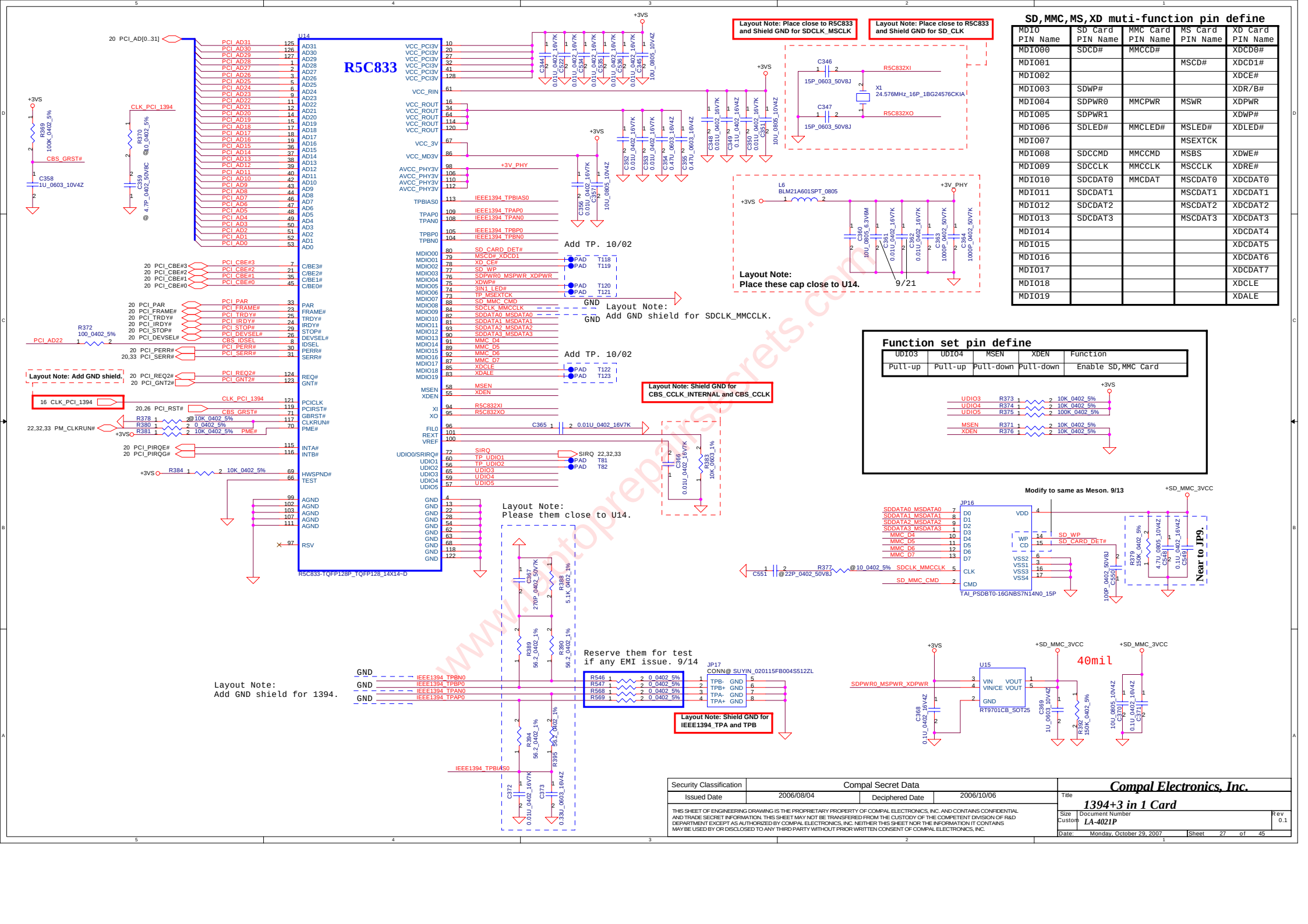


MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07			MSEXTCK	
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDALE

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-down	Pull-down	Enable SD,MMC Card

AMP. FOR INTERNAL SPEAKER

TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

Delete PCM_SPK, Q32, R407, C387, R409. Leave circuitry to support SB_SPKR. 10/8

Change in 9/26

Change value. 9/28

Correct net name. 10/02

Add R571, D37 in 9/26.

Place close to U14

Close to Pin29

Close to Pin30

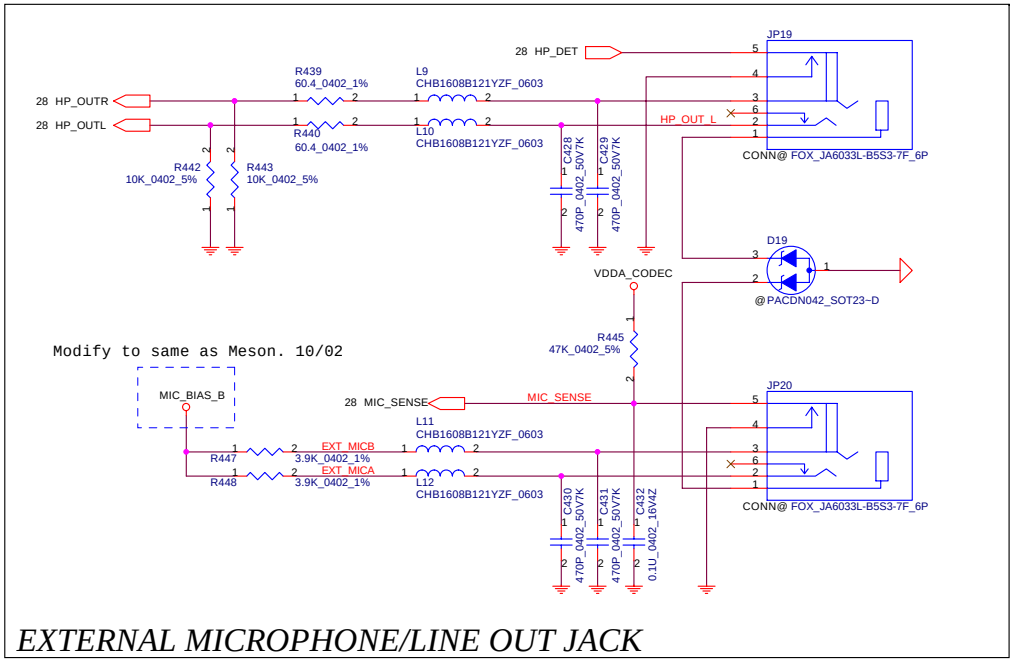
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

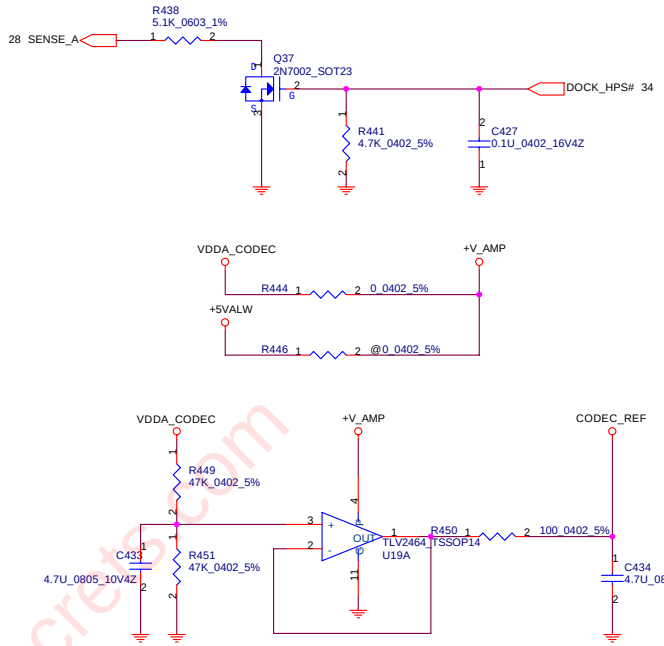
Compal Electronics, Inc.

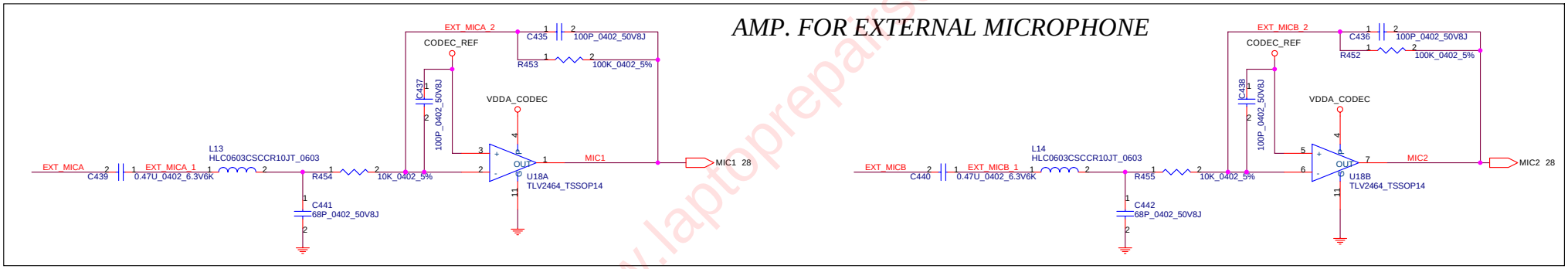
Title: **AC97 CODEC AD1981HD**

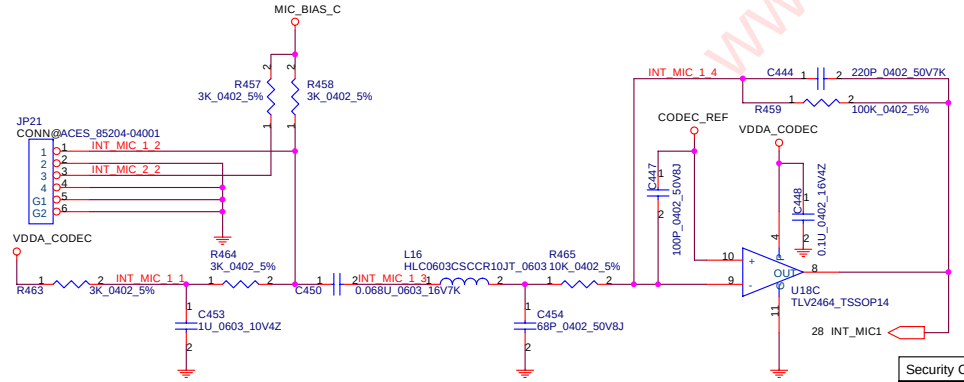
Size	Document Number	Rev
	LA-4021P	0.1

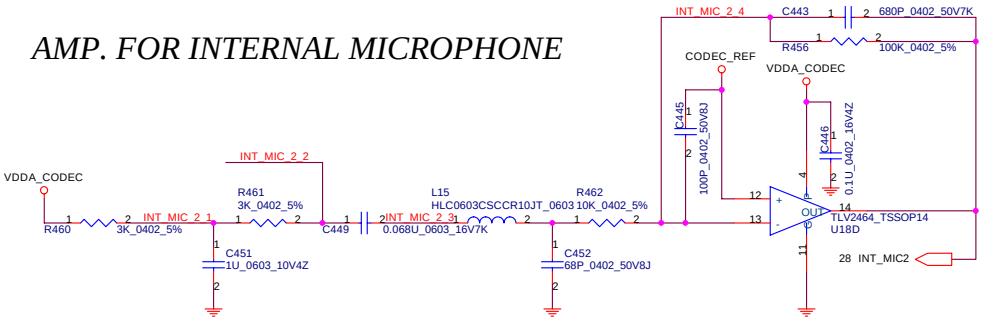
Date: Monday, October 29, 2007 | Sheet 28 of 45











Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

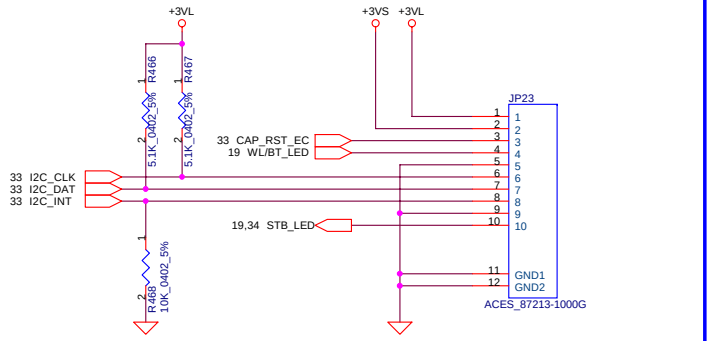
Compal Electronics, Inc.

Title: **AMP & Audio Jack**

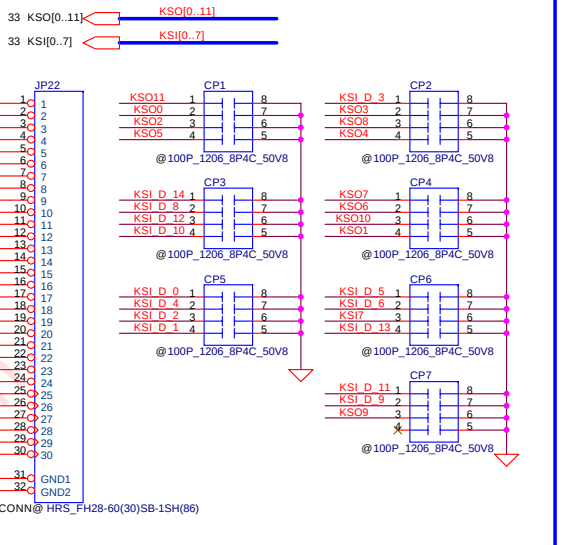
Size	Document Number	Rev
	LA-4021P	0.1

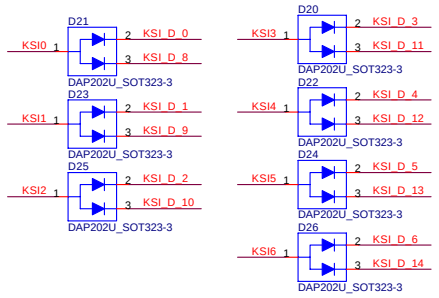
Date: Monday, October 29, 2007 | Sheet 29 of 45

SWITCH BOARD.

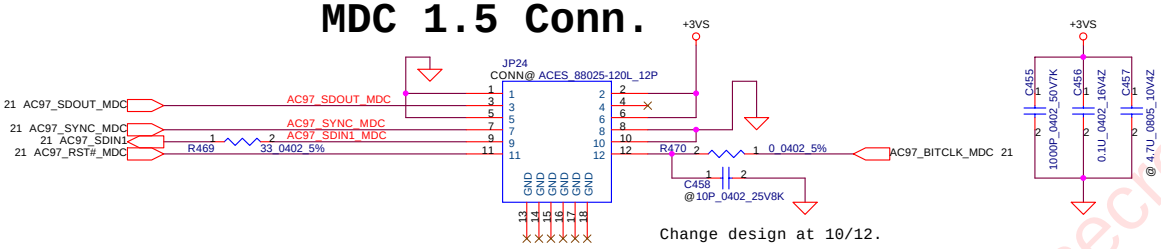


INT_KBD CONN.



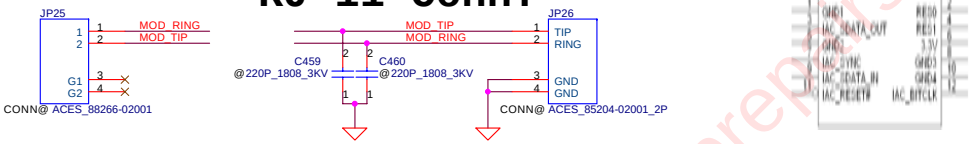


MDC 1.5 Conn.

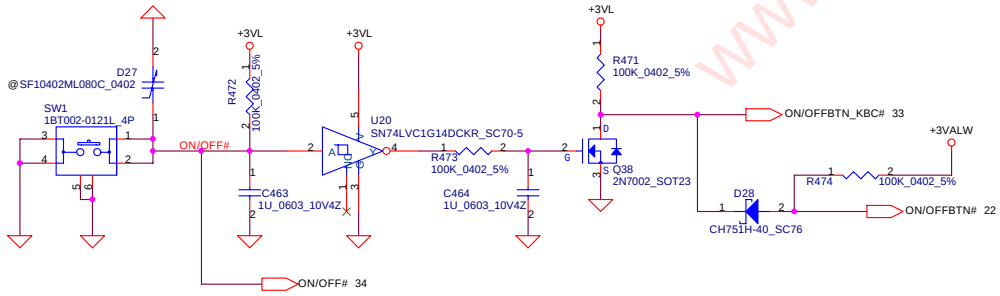


Change design at 10/12.

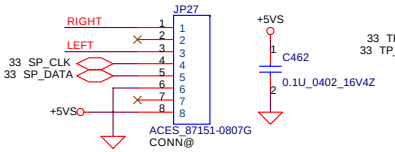
RJ-11 Conn.



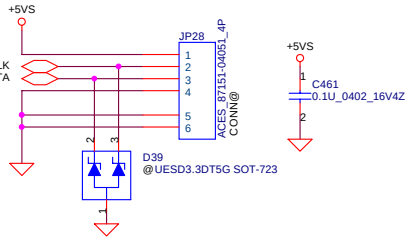
Power button



TrackPoint CONN.

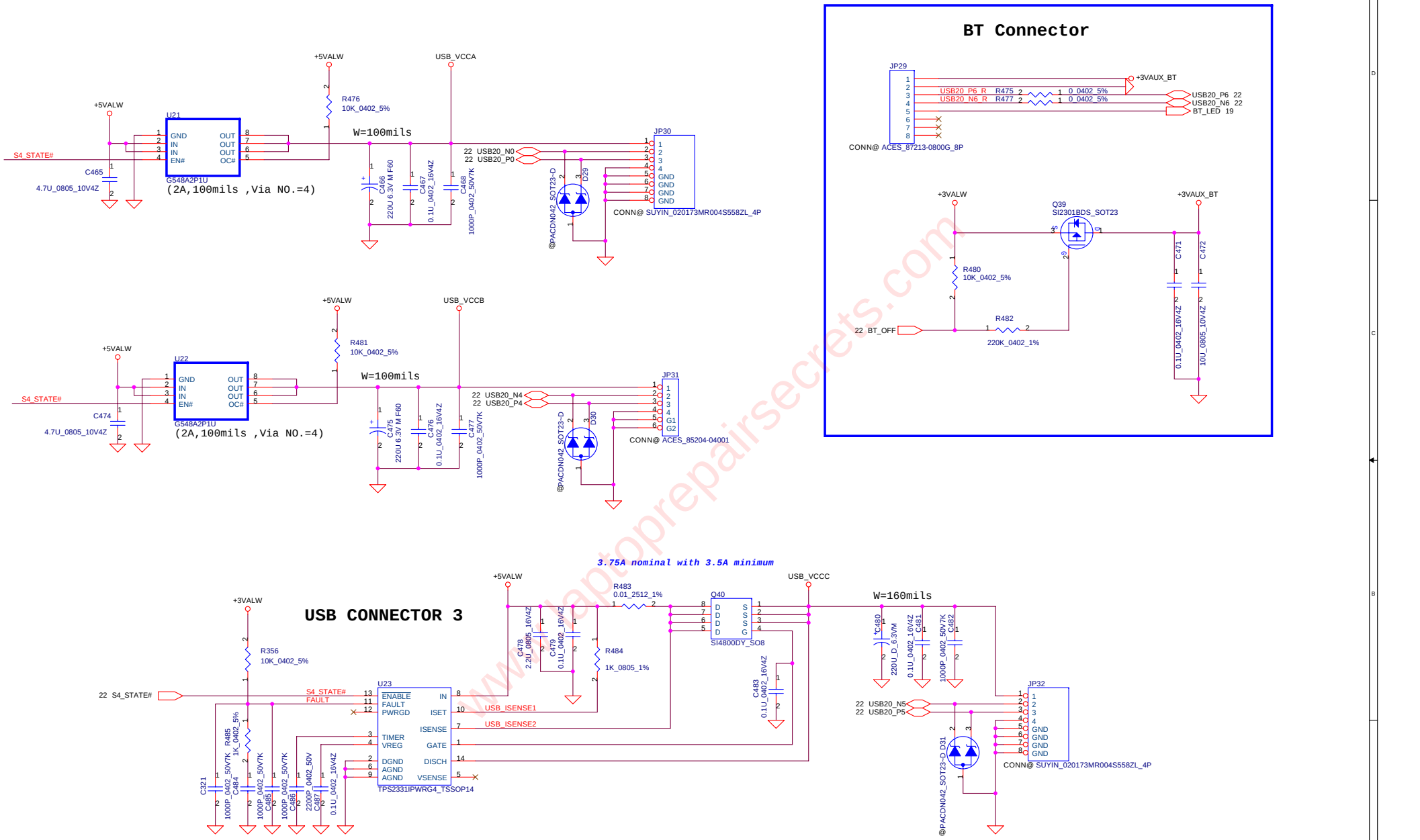


T/P BOARD.



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title	MDC/KBD/ON_OFF/LID		
Size	Document Number LA-4021P		Rev 0.1
Date: Monday, October 29, 2007		Sheet 30 of 45	



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

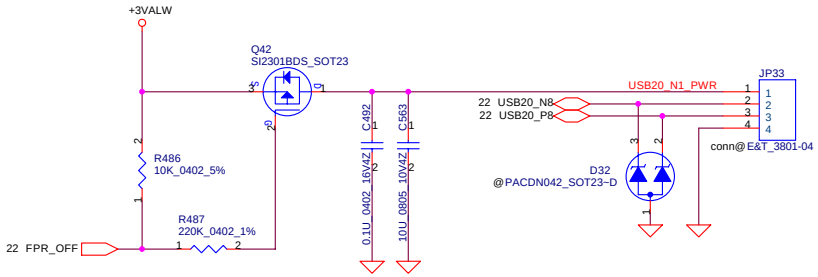
Compal Electronics, Inc.

Title: **USB & BT Connector**

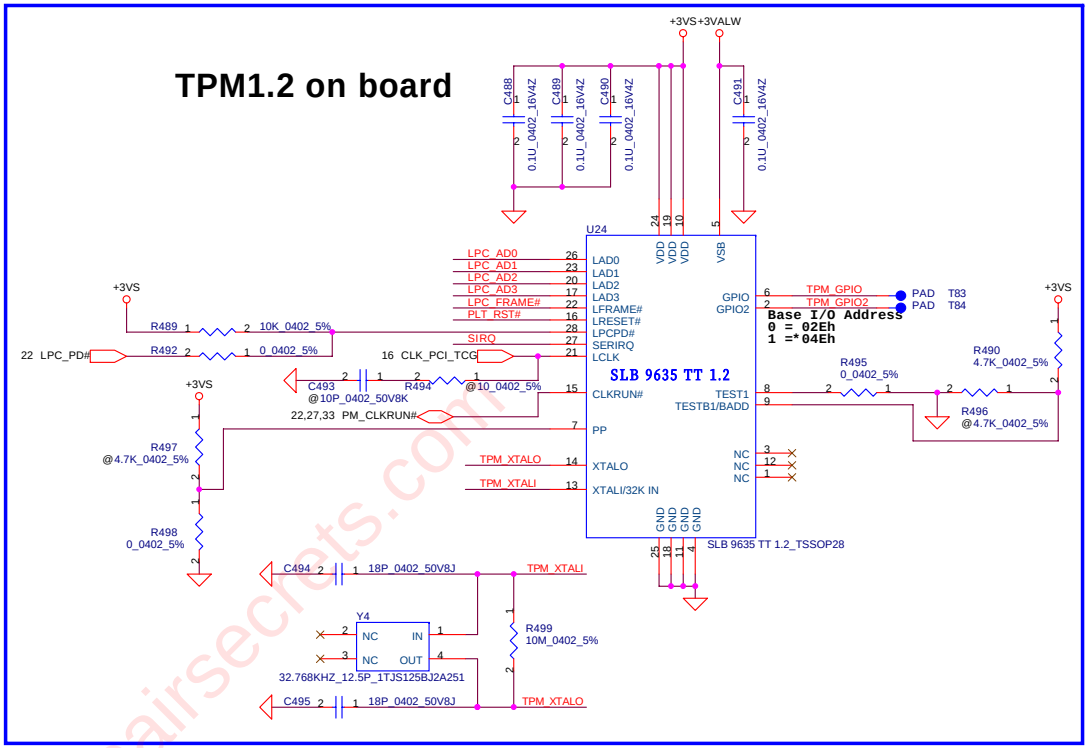
Size: | Document Number: **LA-4021P** | Rev: 0.1

Date: Monday, October 29, 2007 | Sheet 31 of 45

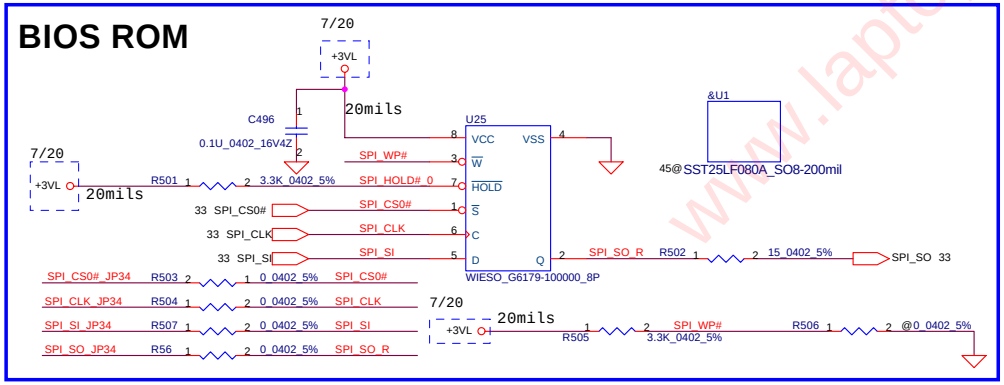
Finger printer



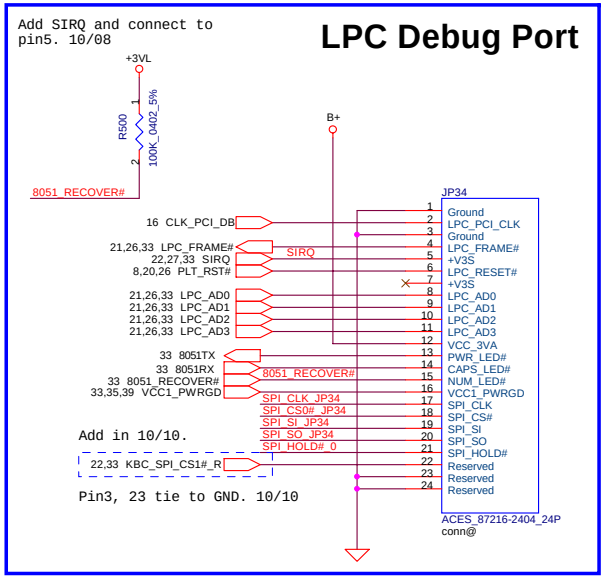
TPM1.2 on board



BIOS ROM



LPC Debug Port



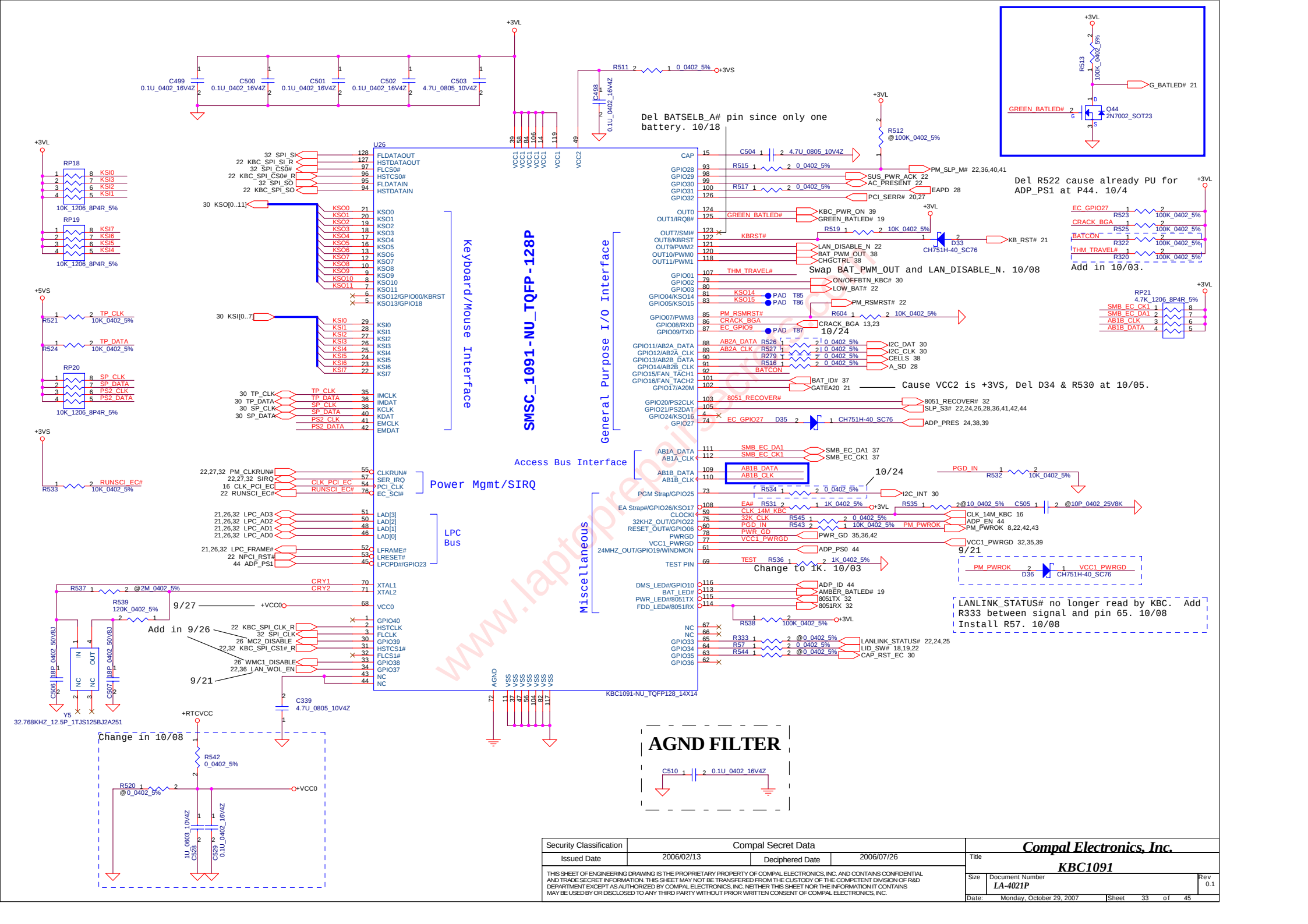
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **TCG/BIOS ROM/PS2/SW LPC DEBUG**

Size	Document Number	Rev
	LA-4021P	0.1

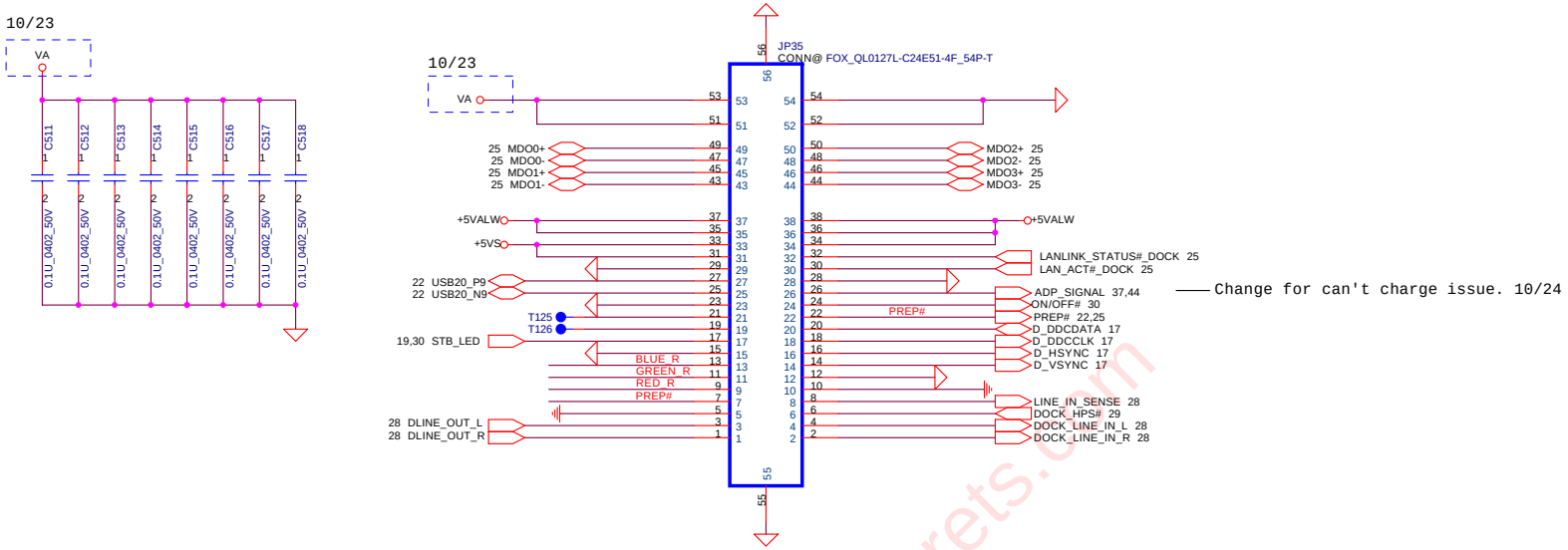
Date: Monday, October 29, 2007 Sheet 32 of 45



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: KBC1091			
Size	Document Number: LA-4021P		Rev: 0.1
Date: Monday, October 29, 2007		Sheet 33 of 45	

DOCKING CONNECT



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DOCK CONN**

Size	Document Number	Rev
Custom	LA-4021P	0.1

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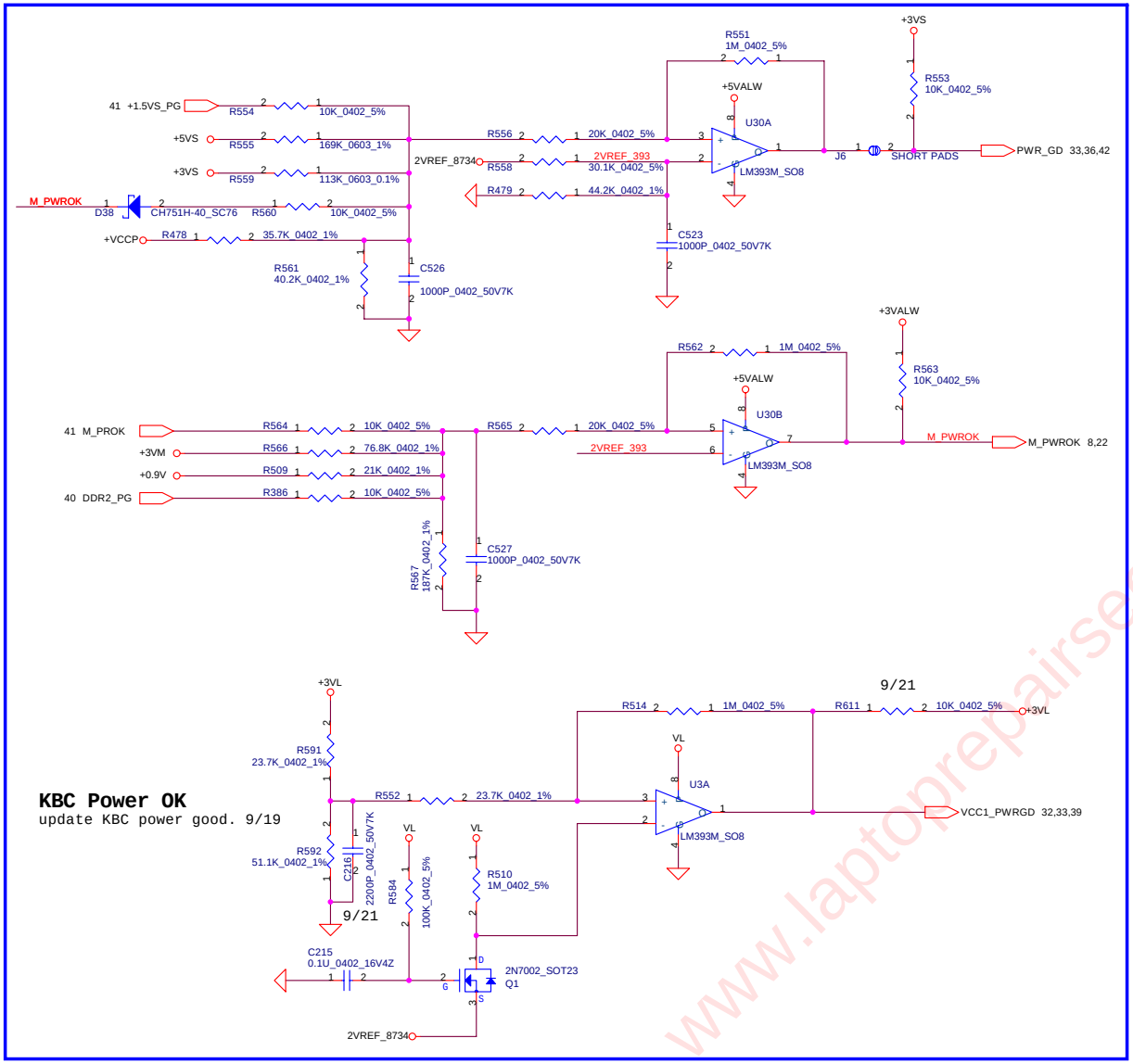
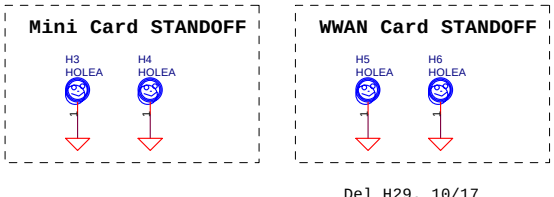
Update per change list. 9/14

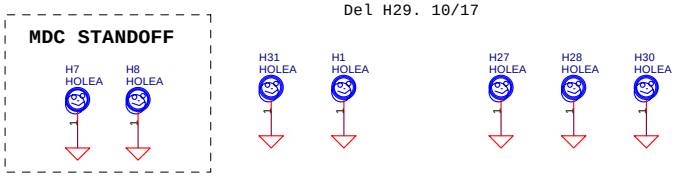


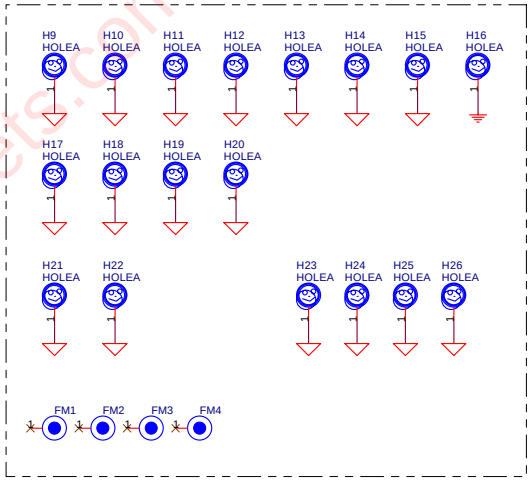
KBC Power OK

update KBC power good. 9/19



Del H29. 10/17





Del LAN reset schematic. 9/26

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

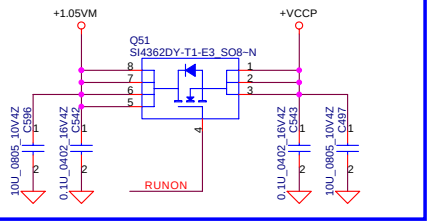
Title: **POK CKT**

Size	Document Number	Rev
	LA-4021P	0.1

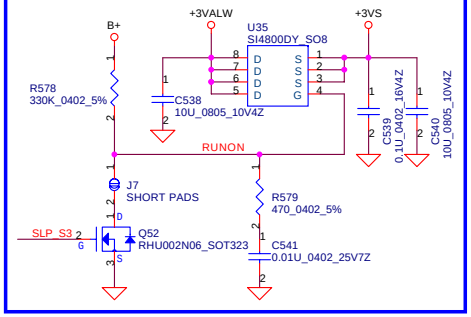
Date: Monday, October 29, 2007 Sheet 35 of 45

Modify at 7/31 after discuss with power team.

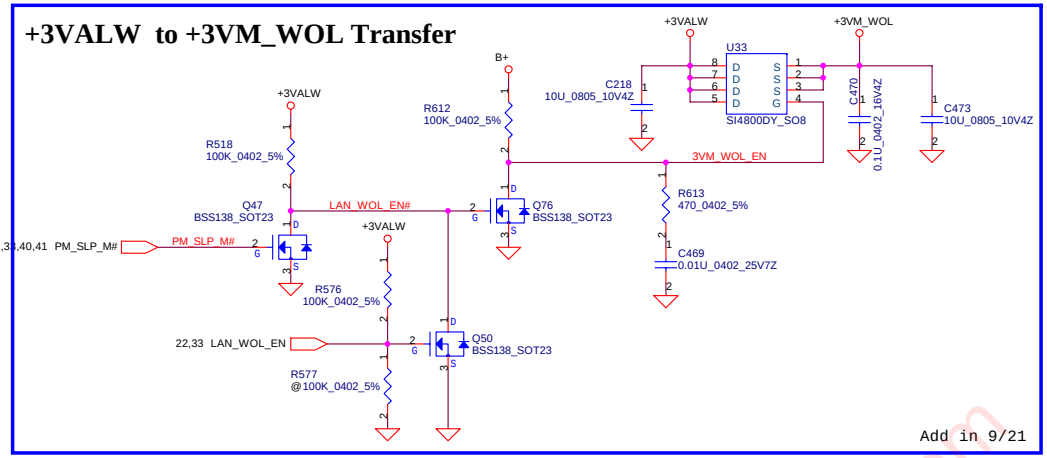
+1.05VM to +VCCP Transfer



+3VALW to +3VS Transfer

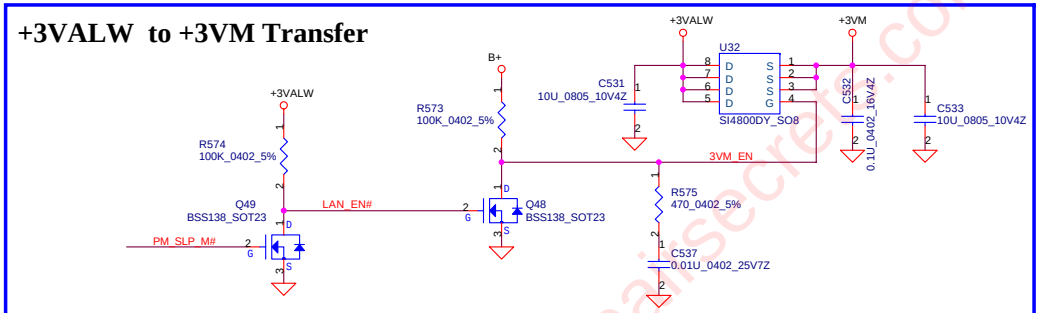


+3VALW to +3VM_WOL Transfer

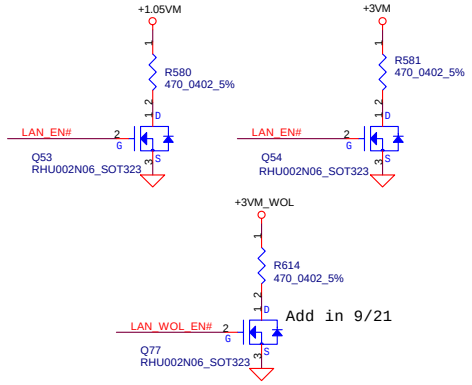


Add in 9/21

+3VALW to +3VM Transfer



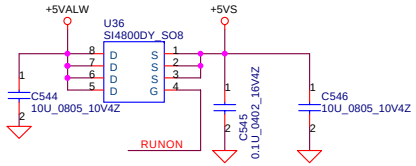
Discharge circuit-2 for V-M



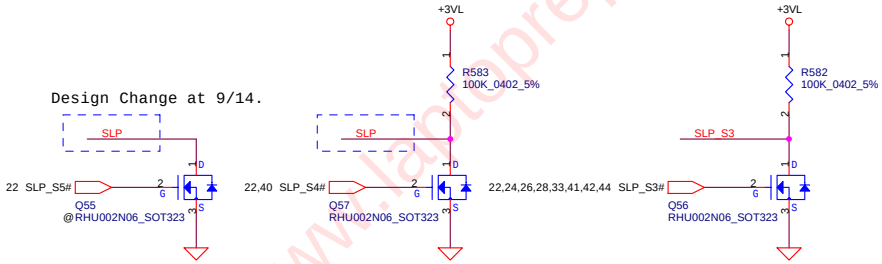
Add in 9/21

SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

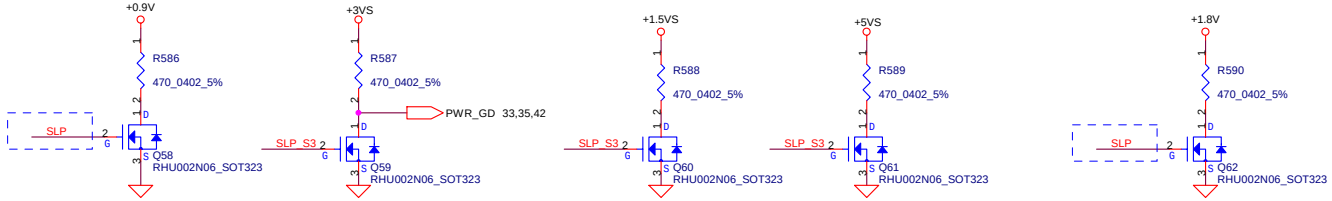
+5VALW to +5VS Transfer



Design Change at 9/14.



Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	DC/DC Circuits
Size	Document Number: LA-4021P
Rev	0.1
Date:	Monday, October 29, 2007
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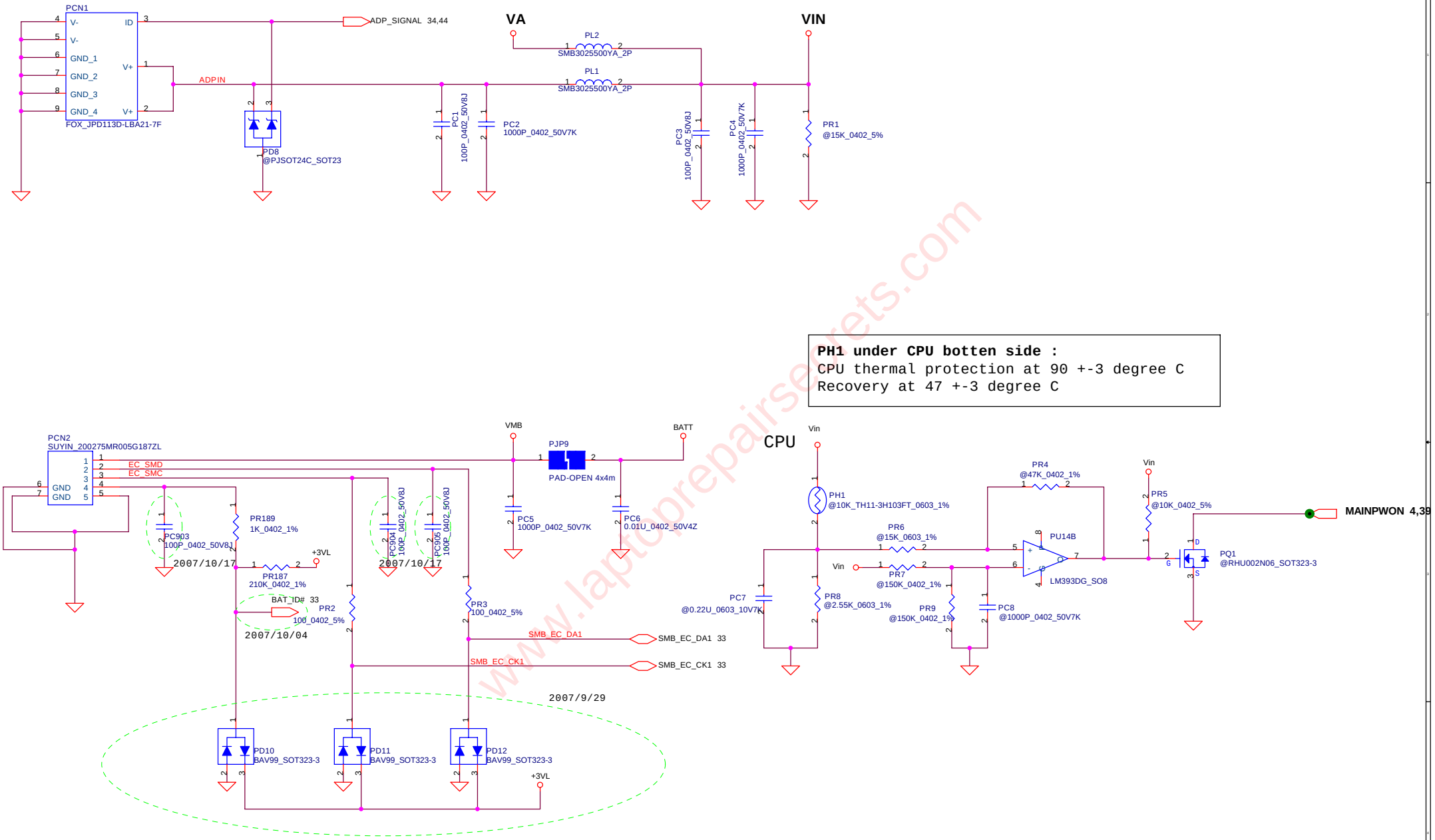


PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C

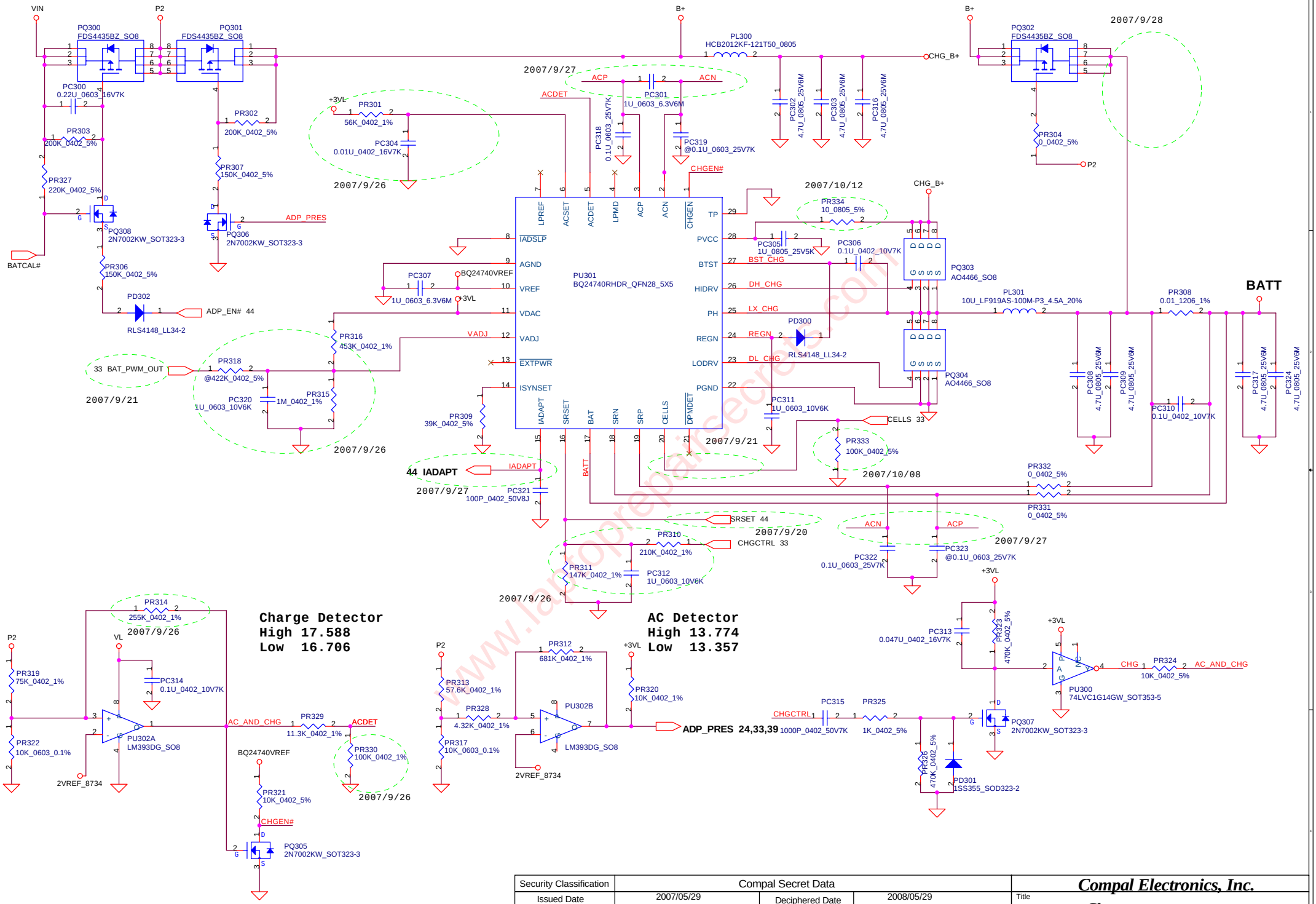
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA-3261P UMA	

Date: Monday, October 29, 2007 Sheet 37 of 45



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	LA-3941P	0.1

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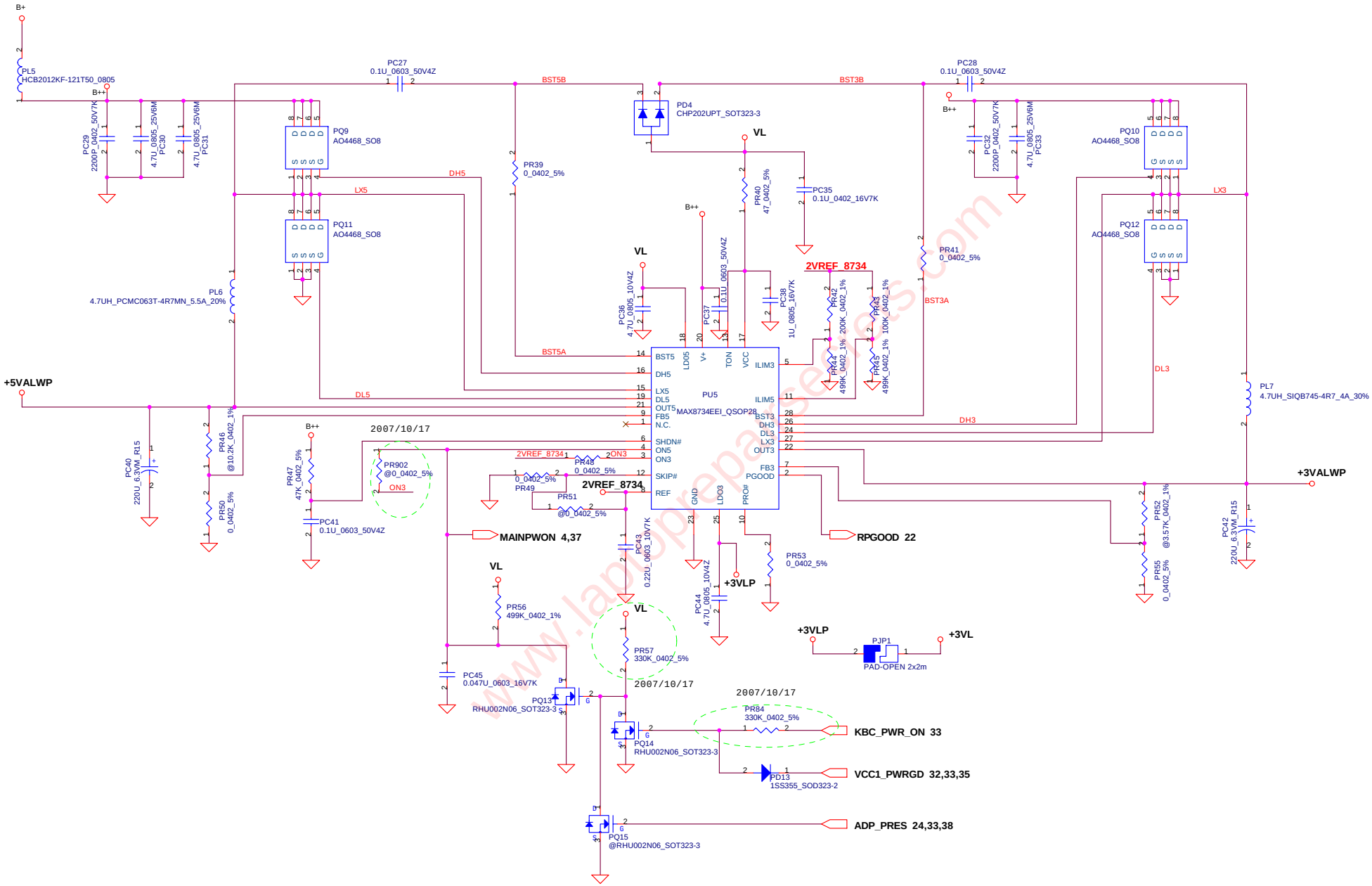
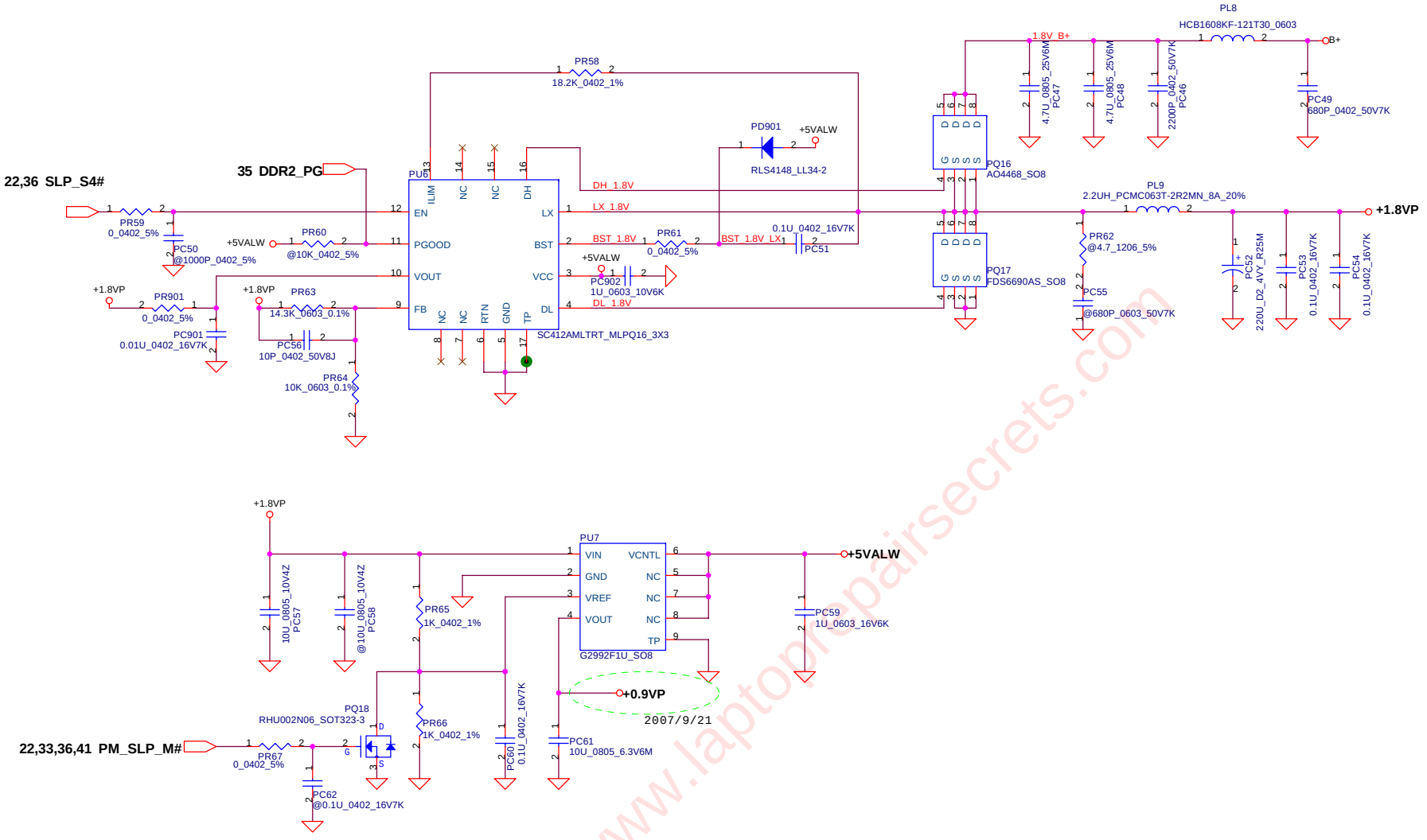
+3.3V/+5V



Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/01

Title	3.3V / 5V		
Size B	Document Number LA-3261P UMA		Rev 0.1
Date: Monday, October 29, 2007	Sheet 39 of 45		



PJP2 PAD-OPEN 4x4m — +5VALWP → +5VALW (4.5A,180mils ,Via NO.= 9)

PJP3 PAD-OPEN 4x4m — +3VALWP → +3VALW (3A,120mils ,Via NO.= 6)

PJP4 PAD-OPEN 4x4m — +1.8VP → +1.8V (6A,240mils ,Via NO.= 12)

PJP5 PAD-OPEN 3x3m — +0.9VP → +0.9V (2A,80mils ,Via NO.= 4)
2007/9/21

PJP11 PAD-OPEN 4x4m — +VCCGFX → +VCCP (5A,200mils ,Via NO.= 10)

PJP8 PAD-OPEN 4x4m — +1.05VMP → +1.05VM (8A,320mils ,Via NO.= 16)

PJP7 PAD-OPEN 4x4m — +1.5VSP → +1.5VS (4A,160mils ,Via NO.=8)

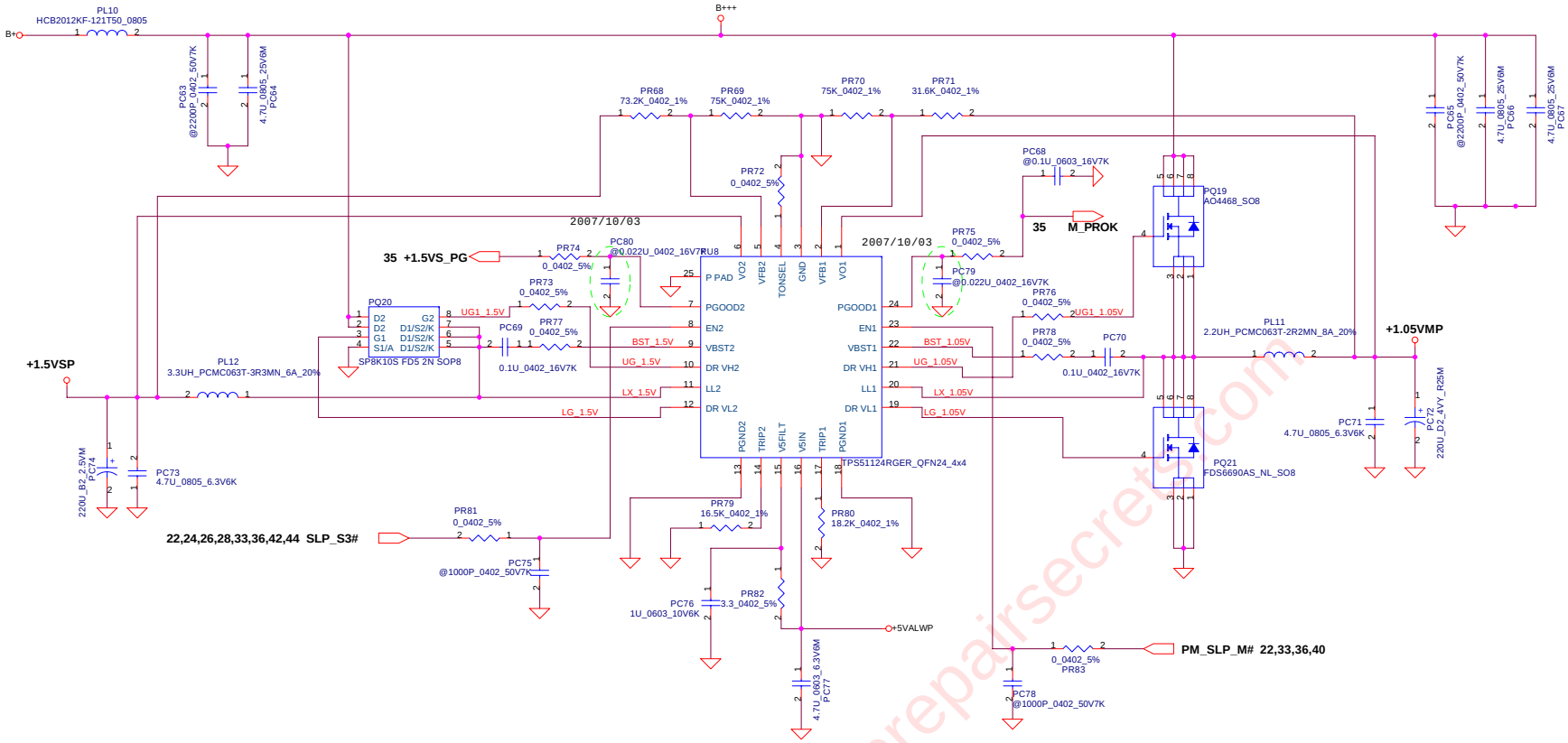
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.8VP/0.9VSP/2.5VSP**

Size	Document Number	Rev
	LA-3941P	0.1

Date: Monday, October 29, 2007 Sheet 40 of 45



Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **1.2V_VP/1.5VSP/1.05VP**

Size	Document Number	Rev
	LA-3732P	0.2

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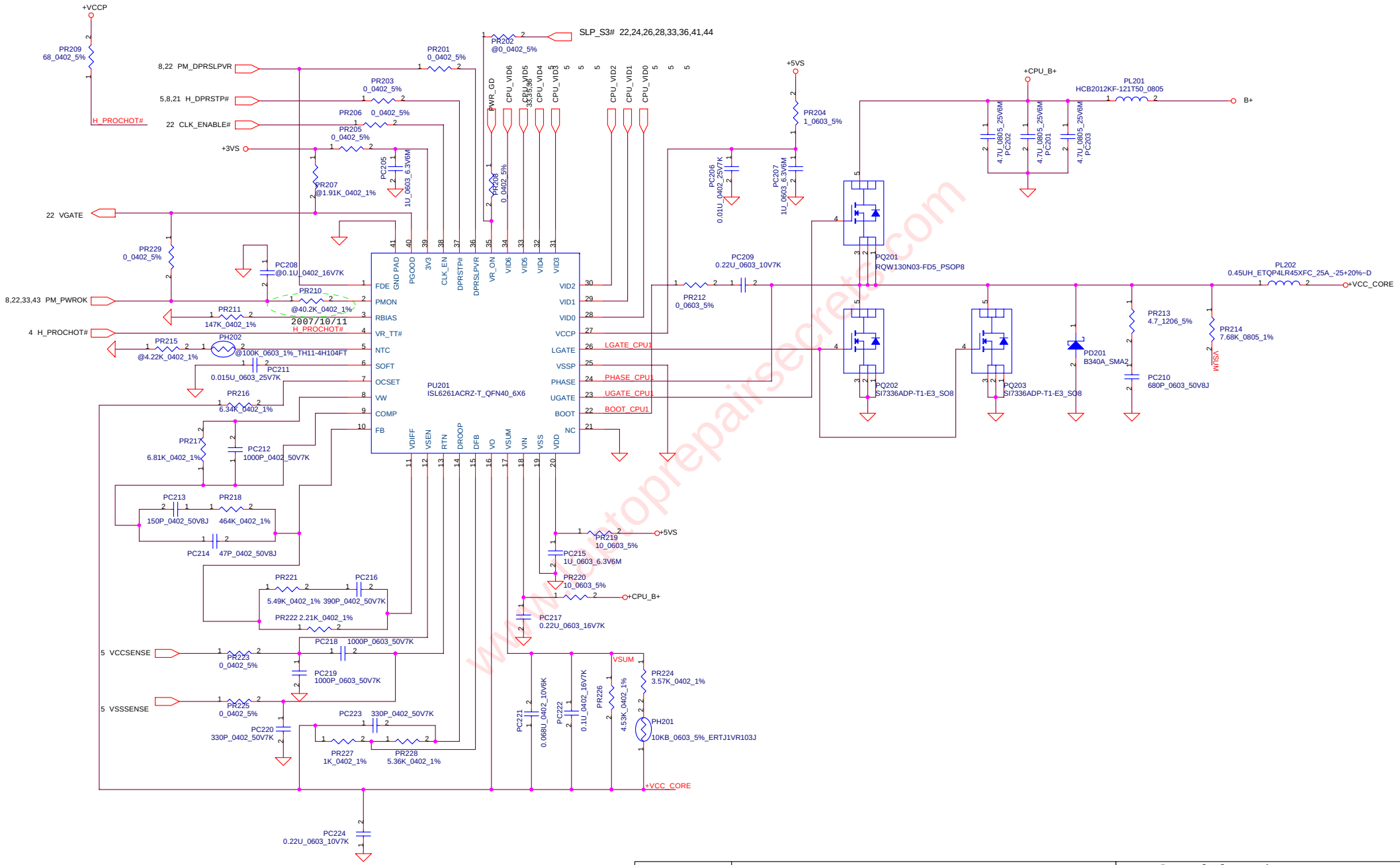


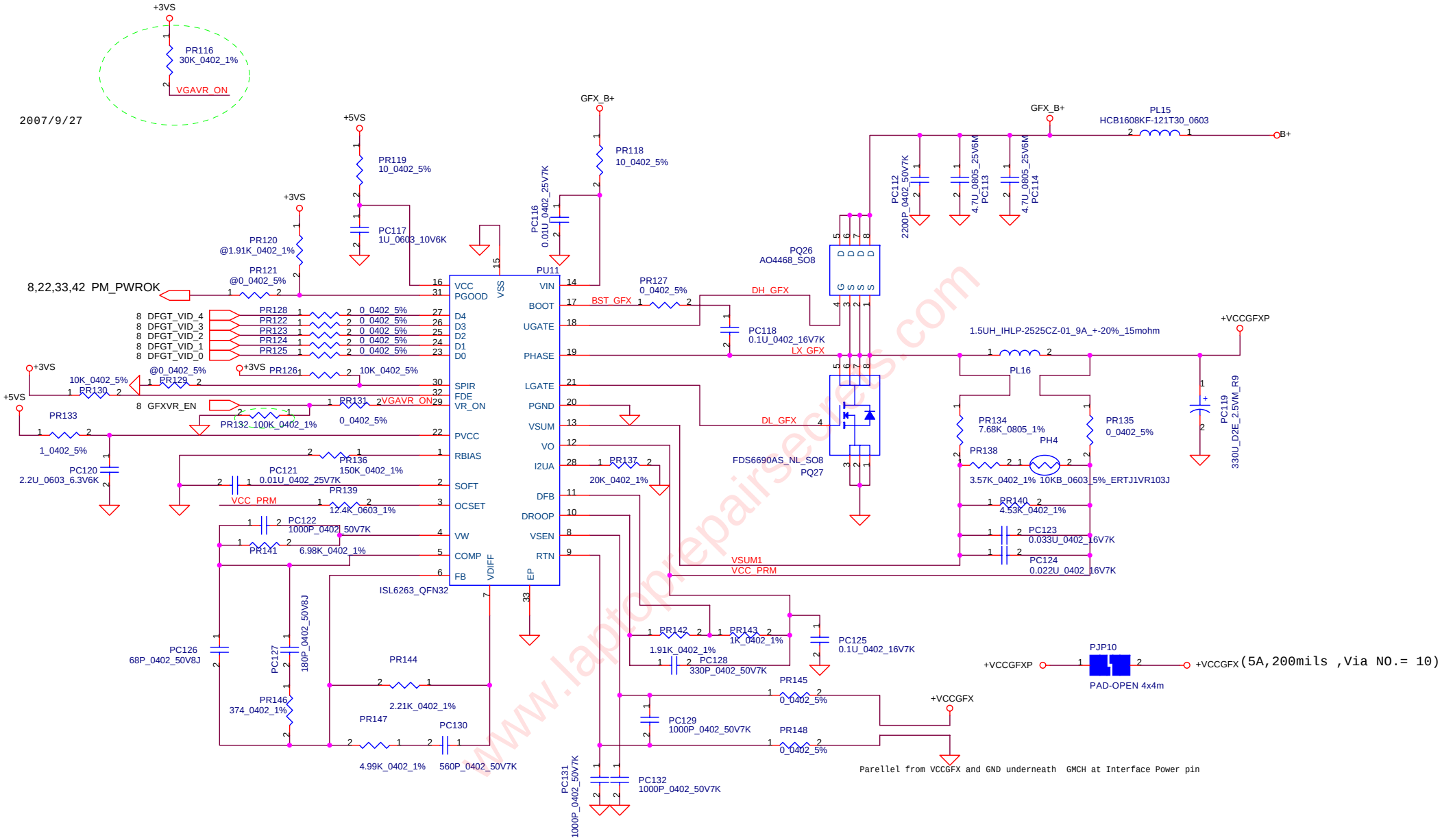
Security Classification	Compal Secret Data		
Issued Date	2005/06/23	Deciphered Date	2006/10/22

Compal Electronics, Inc.

Title: +CPU_CORE

Size: Custom | Document Number: IAX00 | Rev: 0.1

Date: Monday, October 29, 2007 | Sheet 42 of 45



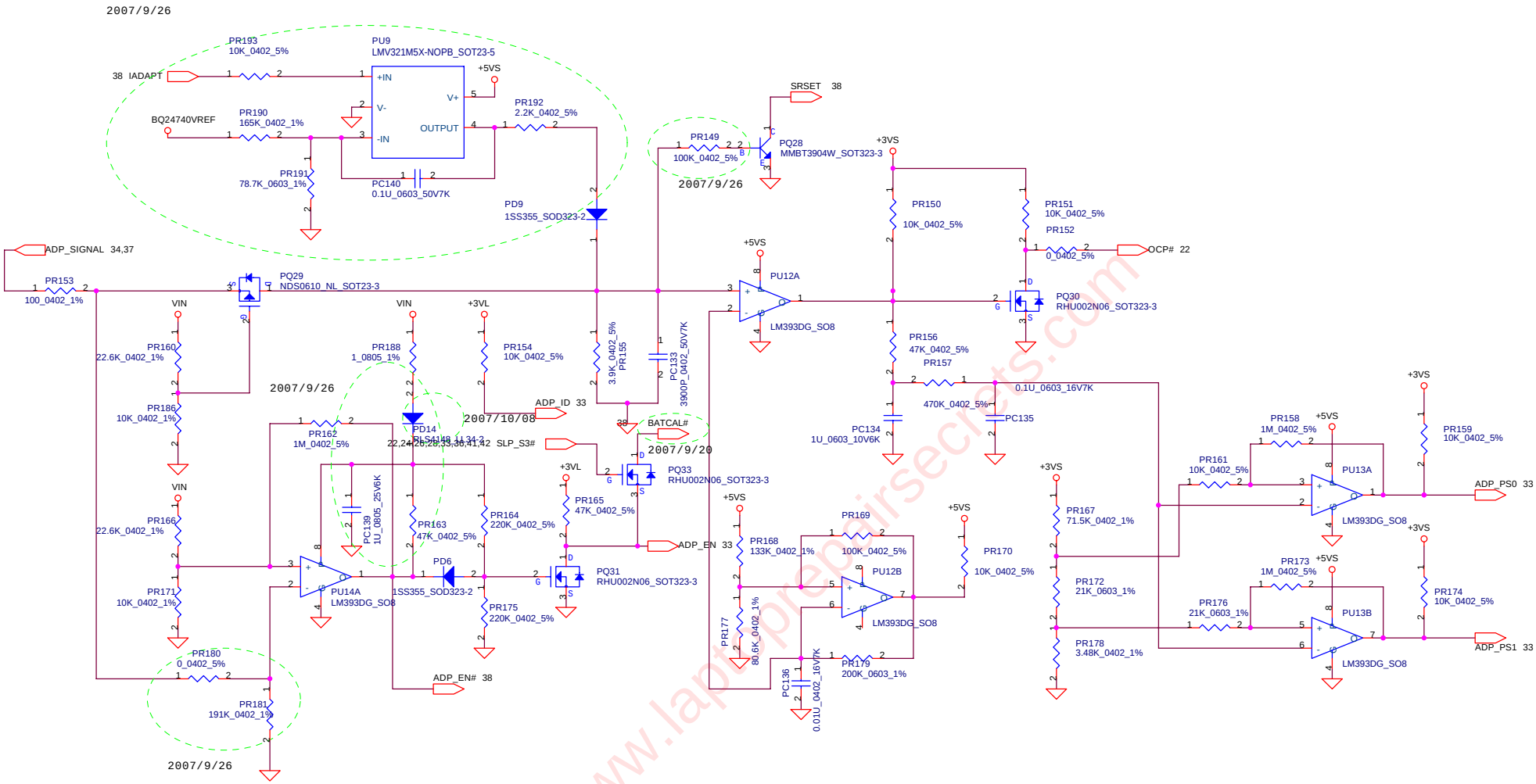
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **VCCGFX**

Size	Document Number	Rev
B	LA-3261P UMA	

Date: Monday, October 29, 2007 Sheet 43 of 45



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					

Compal Electronics, Inc.
Title: Changed-List History-1
Size: Document Number: LA-3732P Rev: 0.2
Date: Monday, October 29, 2007 Sheet 45 of 45