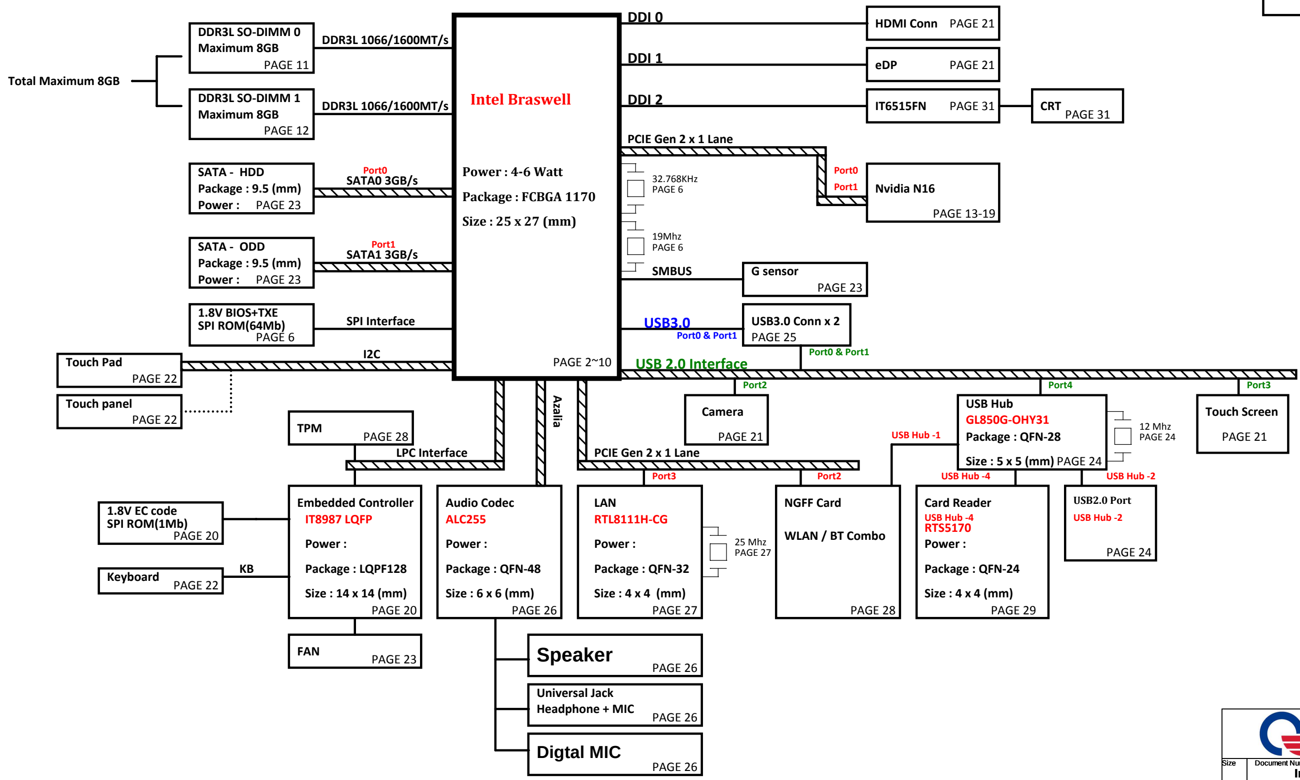
ZRV/ZRVA (15")
Intel Braswell Platform Block Diagram

01

PCB 6L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1(Low)
- LAYER 4 : IN2(High)
- LAYER 5 : SGND
- LAYER 6 : BOT



BOM option	Note
EV@	Discrete
TPS@	Touch Screen
KBL@	KB light
GS@	G-Sensor
EVG@	CG6 2.0 (N16S)
EVNG@	Non-CG6 2.0
AC@	IOAC
NAC@	Non-IOAC
TPM@	TPM

Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size | Document Number: Intel Block Diagram | Rev 1A

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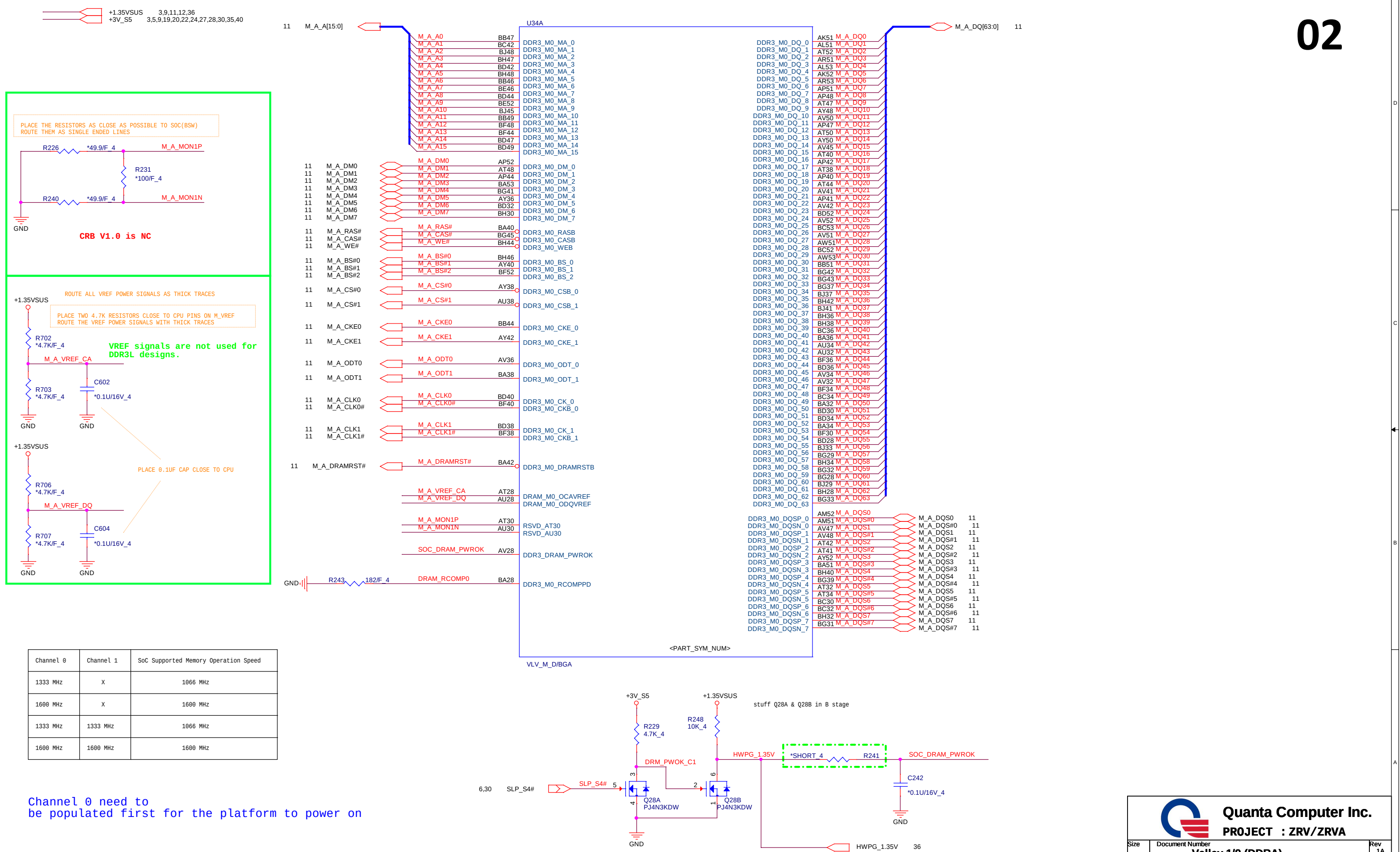
02



Channel 0	Channel 1	SoC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

Channel 0 need to
be populated first for the platform to power on

Quanta Computer Inc.
PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A

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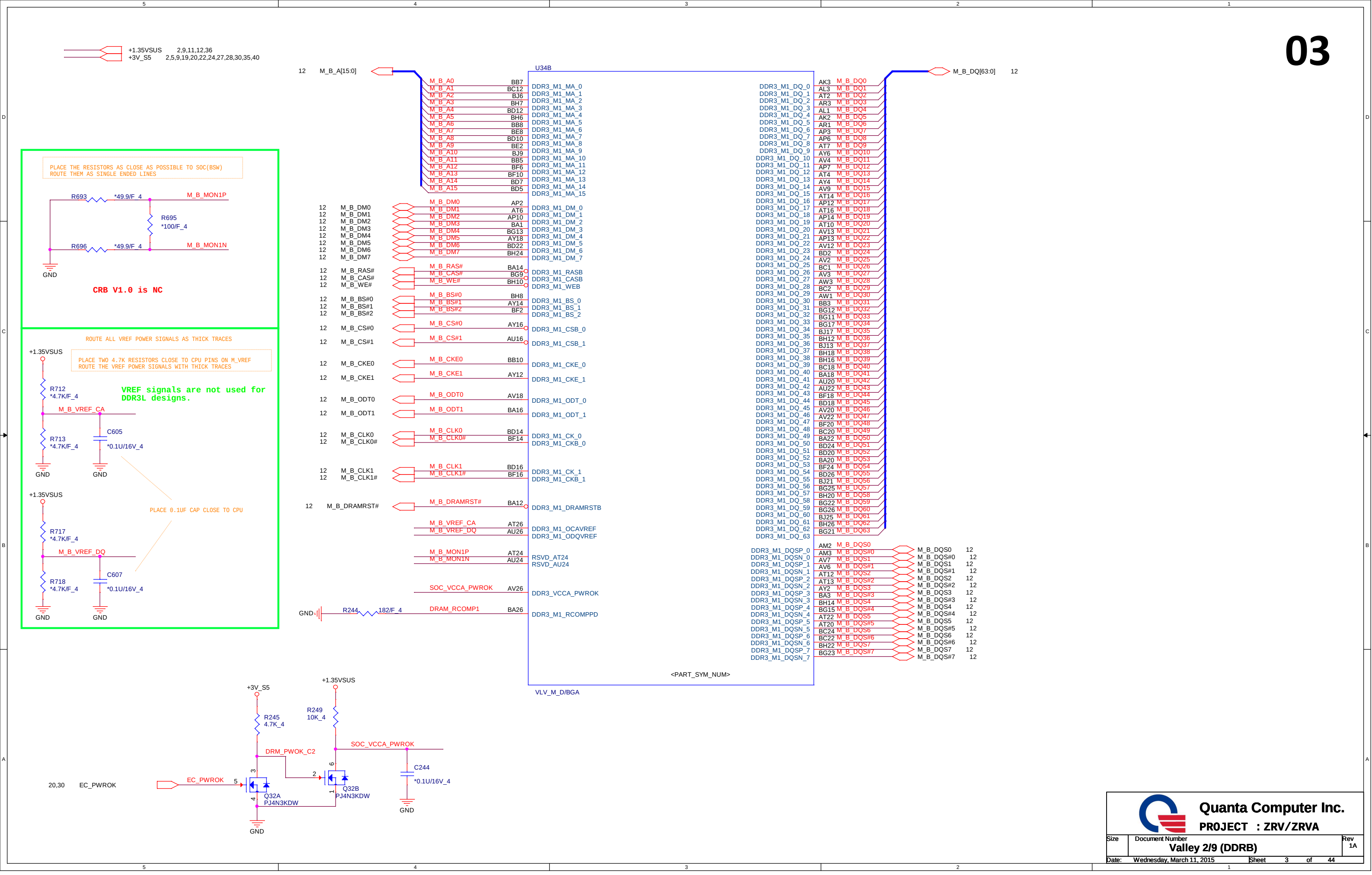

+1.35VSUS 2,9,11,12,36
+3V_S5 2,5,9,19,20,22,24,27,28,30,35,40
12 M_B_A[15:0]
U34B
M_B_DQ[63:0] 12
PLACE THE RESISTORS AS CLOSE AS POSSIBLE TO SOC(BSW)
ROUTE THEM AS SINGLE ENDED LINES
R693 *49.9/F_4 M_B_MON1P
R695 *100/F_4
R696 *49.9/F_4 M_B_MON1N
GND
CRB V1.0 is NC
ROUTE ALL VREF POWER SIGNALS AS THICK TRACES
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M_VREF
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES
+1.35VSUS
R712 *4.7K/F_4
VREF signals are not used for DDR3L designs.
M_B_VREF_CA
R713 *4.7K/F_4
C605 *0.1U/16V_4
PLACE 0.1UF CAP CLOSE TO CPU
R717 *4.7K/F_4
M_B_VREF_DQ
R718 *4.7K/F_4
C607 *0.1U/16V_4
M_B_DRAMRST# DDR3_M1_DRAMRSTB
M_B_VREF_CA DDR3_M1_OCAVREF
M_B_VREF_DQ DDR3_M1_ODQVREF
M_B_MON1P RSVD_AT24
M_B_MON1N RSVD_AU24
SOC_VCCA_PWROK DDR3_VCCA_PWROK
R244 182/F_4 DRAM_RCOMP1 DDR3_M1_RCOMPPD
<PART_SYM_NUM>
VLV_M_D/BGA
+3V_S5
R245 4.7K_4
+1.35VSUS
R249 10K_4
DRM_PWOK_C2
SOC_VCCA_PWROK
C244 *0.1U/16V_4
20,30 EC_PWROK
Q32A PJ4N3KDW
Q32B PJ4N3KDW
Quanta Computer Inc.
PROJECT : ZRV/ZRVA
Size
Document Number
Rev 1A
Valley 2/9 (DDRB)
Date: Wednesday, March 11, 2015
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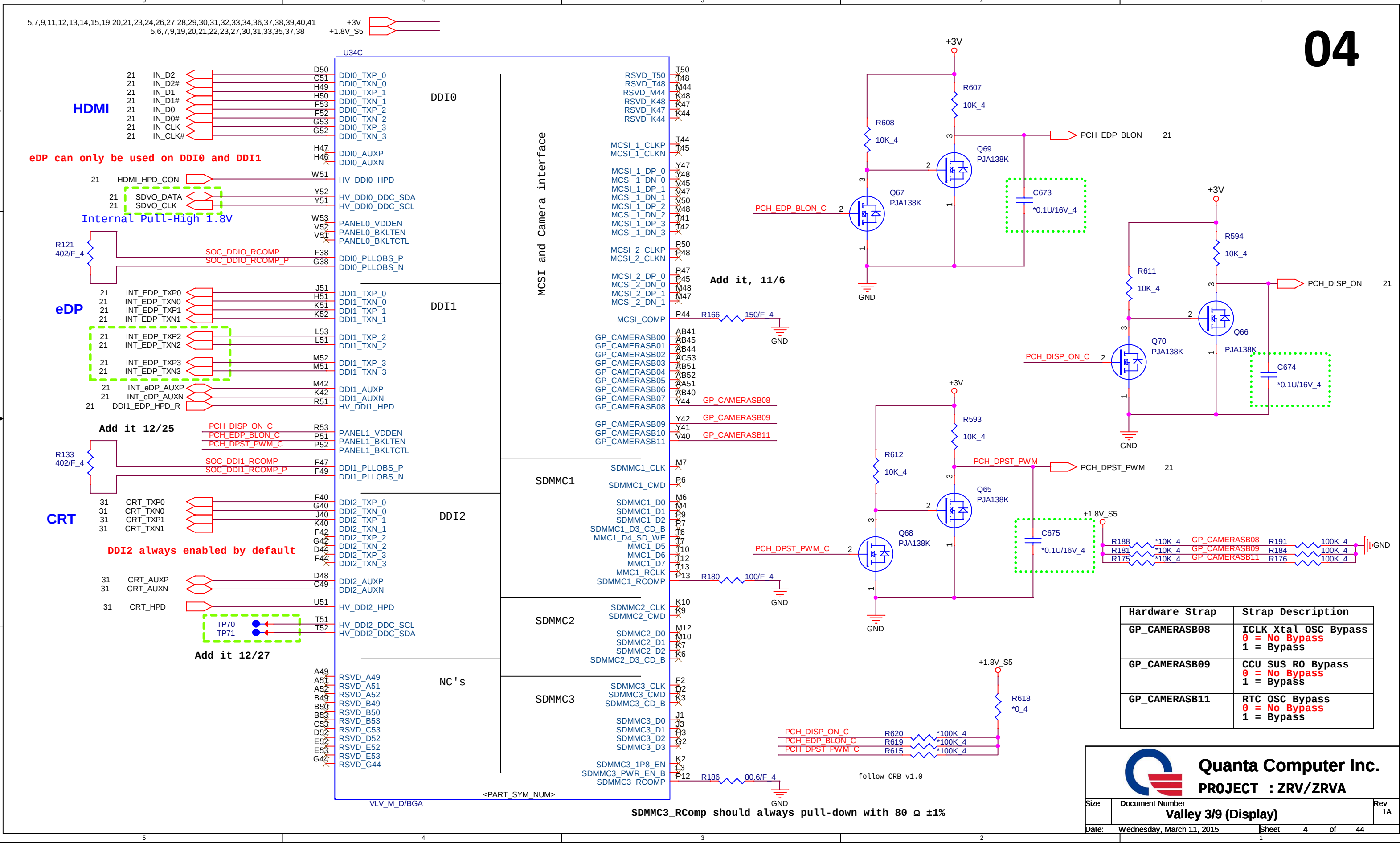

Hardware Strap	Strap Description
GP_CAMERASB08	ICLK Xtal OSC Bypass 0 = No Bypass 1 = Bypass
GP_CAMERASB09	CCU SUS RO Bypass 0 = No Bypass 1 = Bypass
GP_CAMERASB11	RTC OSC Bypass 0 = No Bypass 1 = Bypass

Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 3/9 (Display)	1A

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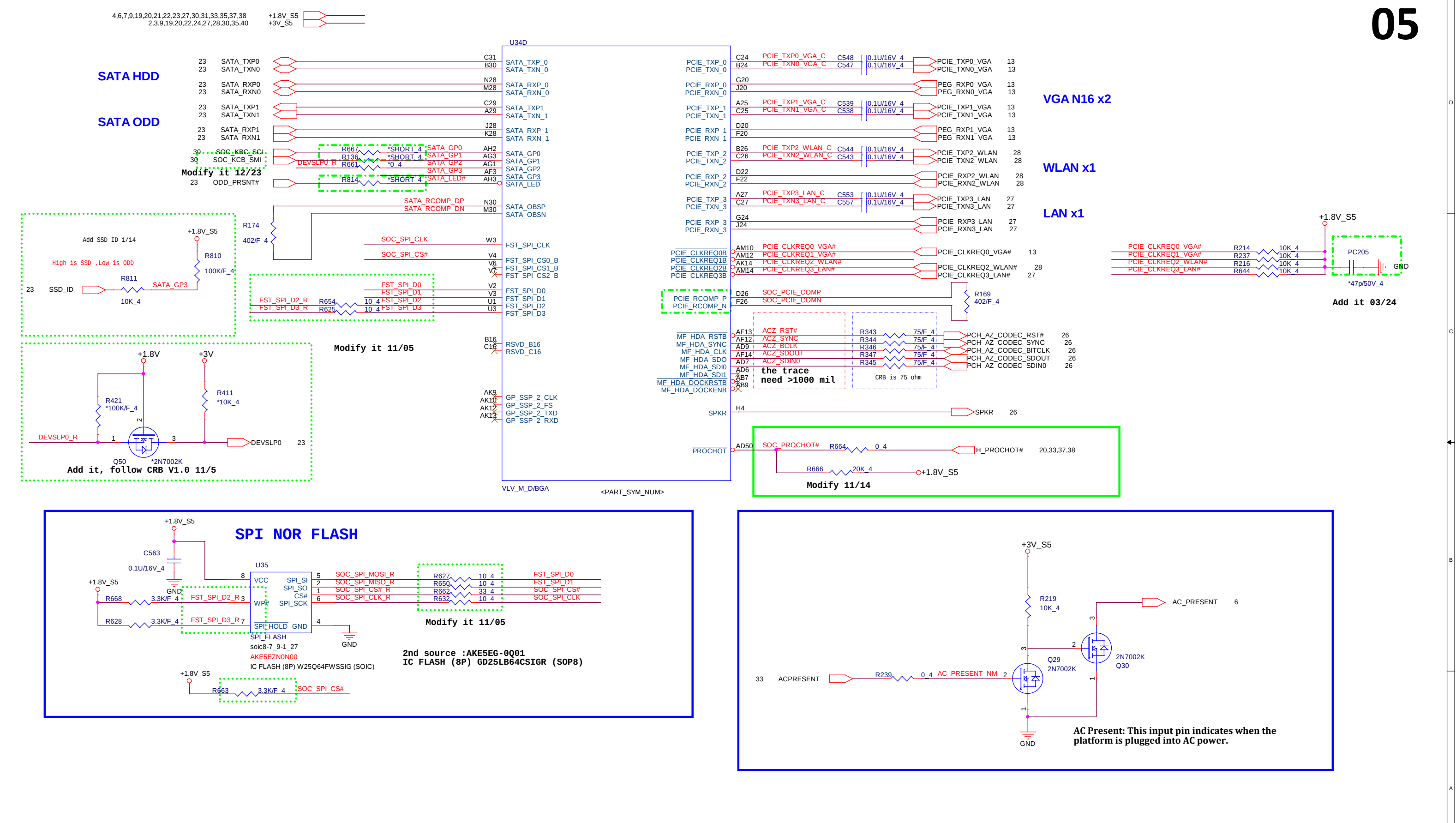
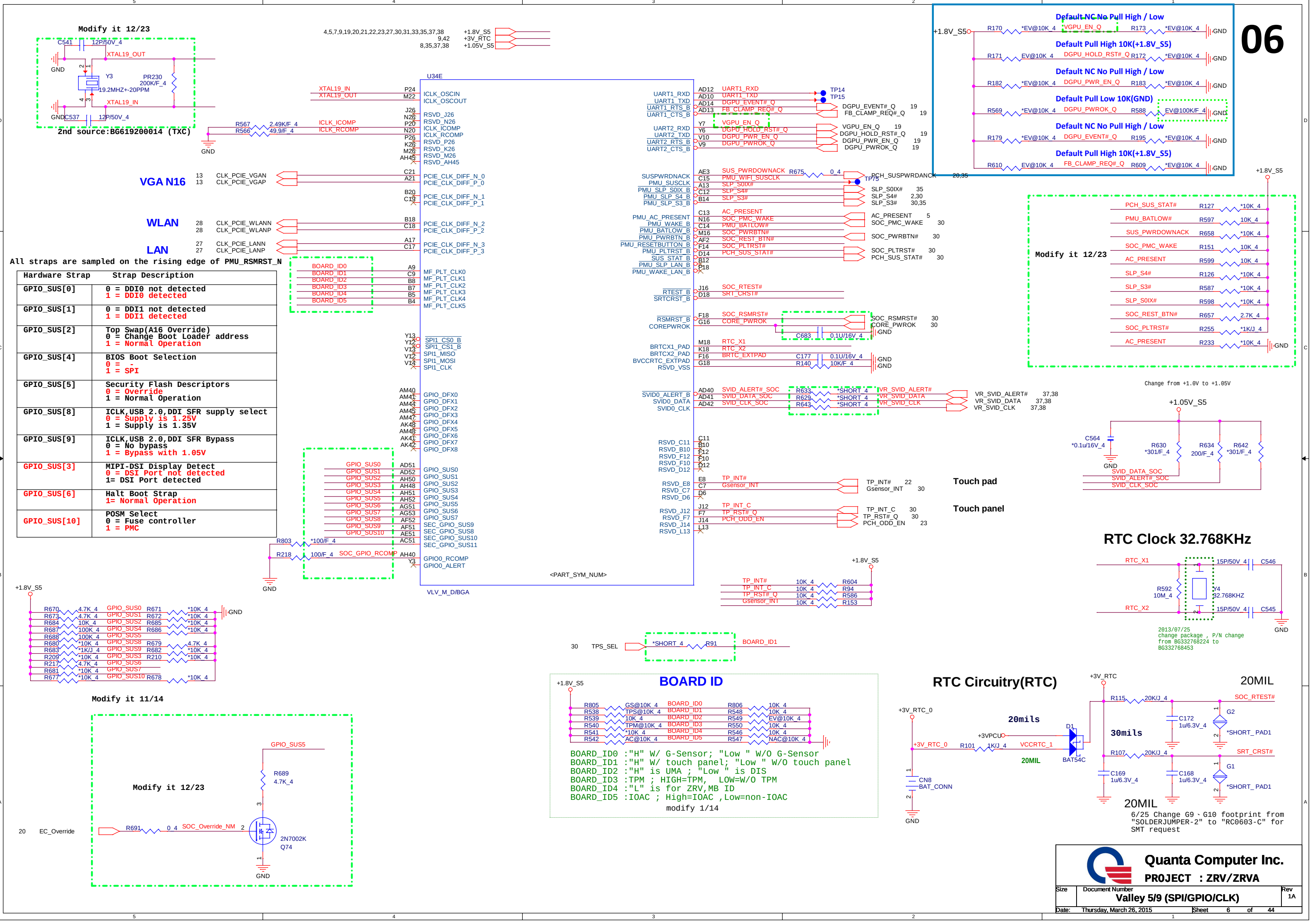


Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A

Date: Thursday, March 26, 2015 Sheet 5 of 44



All straps are sampled on the rising edge of PMU_RSMRST_N

Hardware Strap	Strap Description
GPIO_SUS[0]	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap(A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Security Flash Descriptors 0 = Override 1 = Normal Operation
GPIO_SUS[8]	ICLK,USB 2.0,DDI SFR supply select 0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK,USB 2.0,DDI SFR Bypass 0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[3]	MIPI-DSI Display Detect 0 = DSI Port not detected 1= DSI Port detected
GPIO_SUS[6]	Halt Boot Strap 1= Normal Operation
GPIO_SUS[10]	POSM Select 0 = Fuse controller 1 = PMC

BOARD ID

BOARD_ID0 :"H" W/ G-Sensor; "Low " W/O G-Sensor
BOARD_ID1 :"H" W/ touch panel; "Low " W/O touch panel
BOARD_ID2 :"H" is UMA ; "Low " is DIS
BOARD_ID3 :TPM ; HIGH=TPM, LOW=W/O TPM
BOARD_ID4 :"L" is for ZRV,MB ID
BOARD_ID5 :IOAC ; High=IOAC ,Low=non-IOAC

modify 1/14

6/25 Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" for SMT request

Quanta Computer Inc.
PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A

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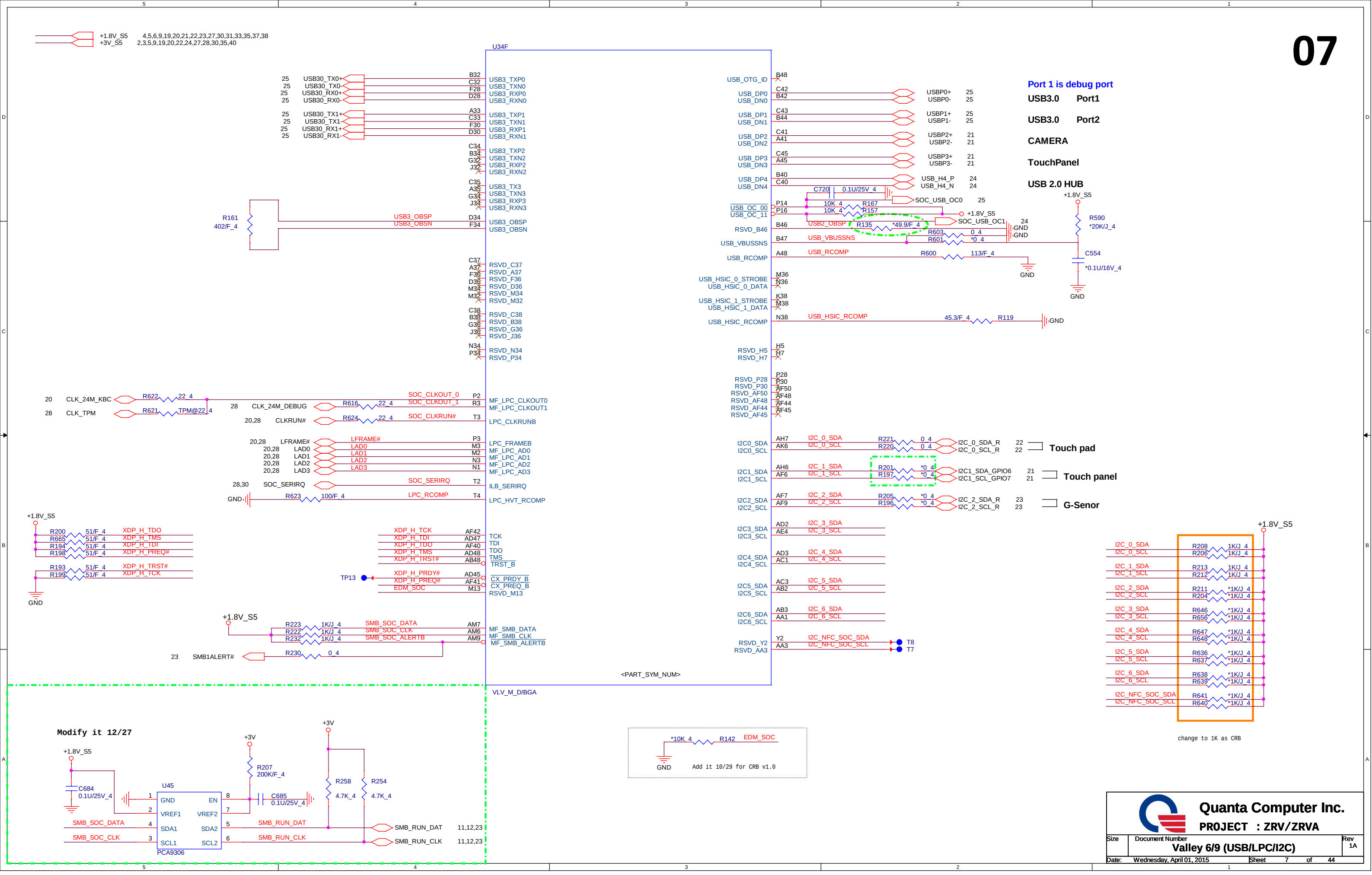
07
U34F
Port 1 is debug port
USB3.0 Port1
USB3.0 Port2
CAMERA
TouchPanel
USB 2.0 HUB
Touch pad
Touch panel
G-Senor
Modify it 12/27
U45
PCA9306
Add it 10/29 for CRB v1.0
change to 1K as CRB
VLV_M_D/BGA
<PART_SYM_NUM>
Quanta Computer Inc.
PROJECT : ZRV/ZRVA
Valley 6/9 (USB/LPC/I2C)
Date: Wednesday, April 01, 2015
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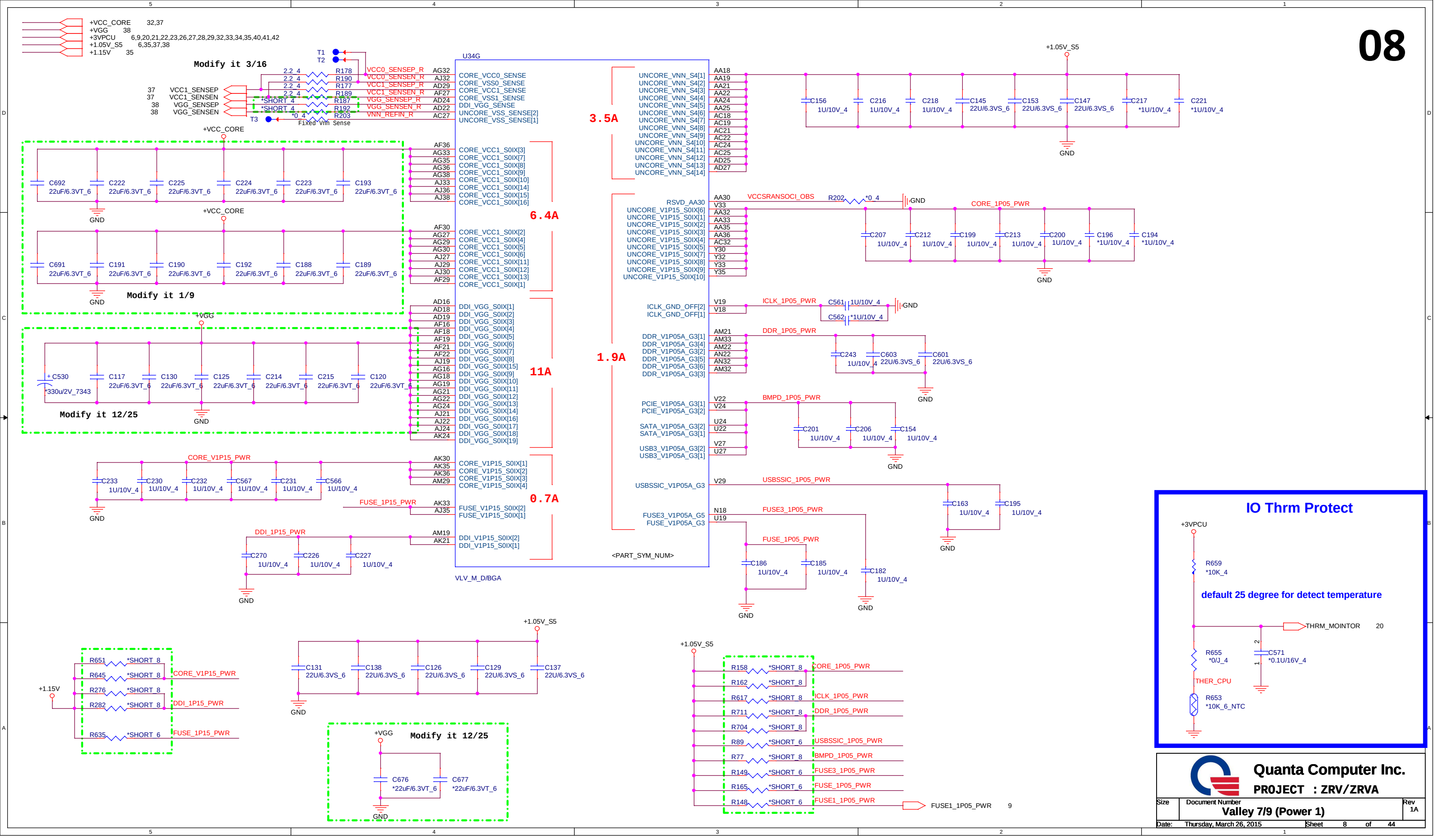

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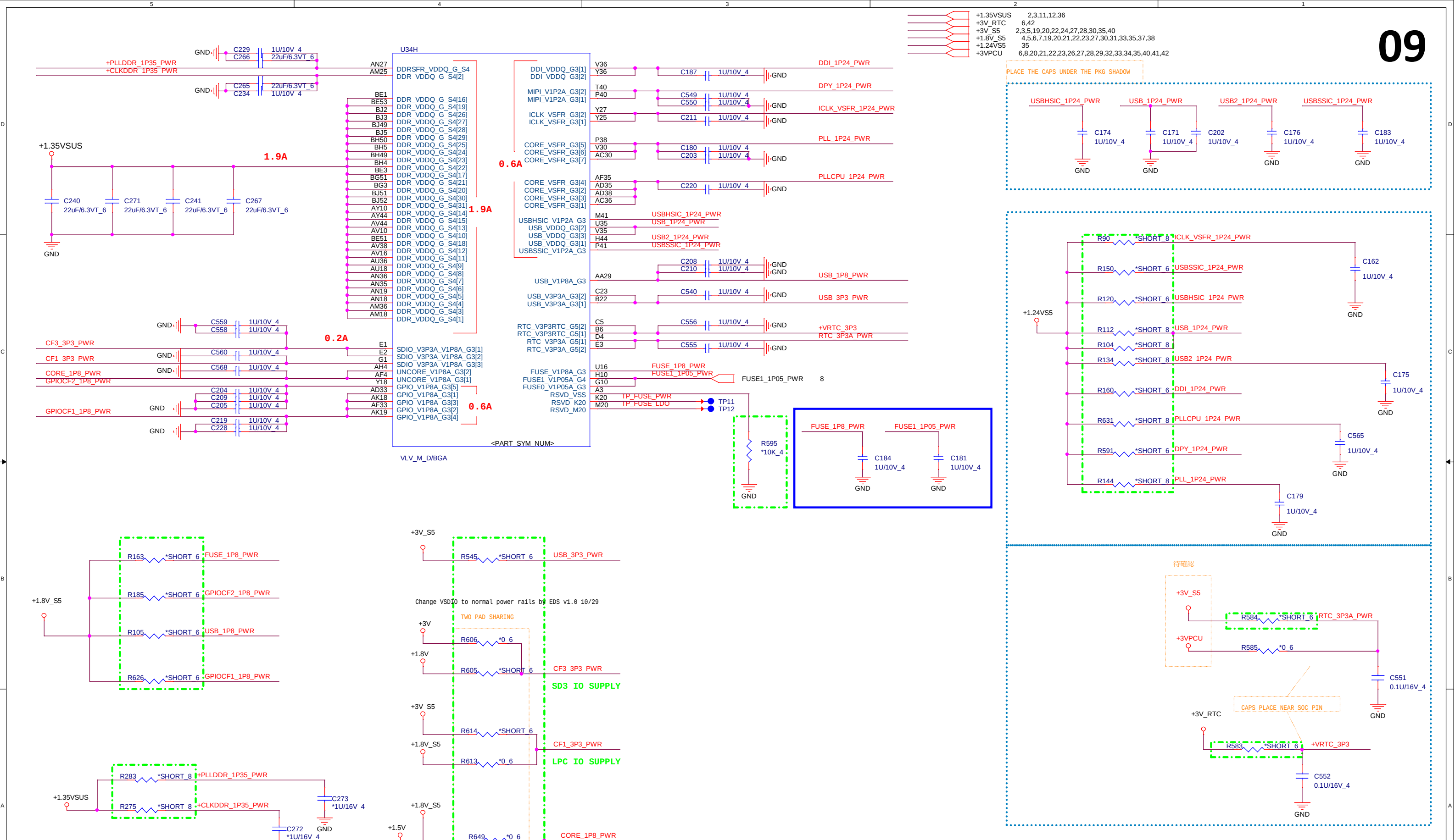

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PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 8/9 (Power 2)	1A

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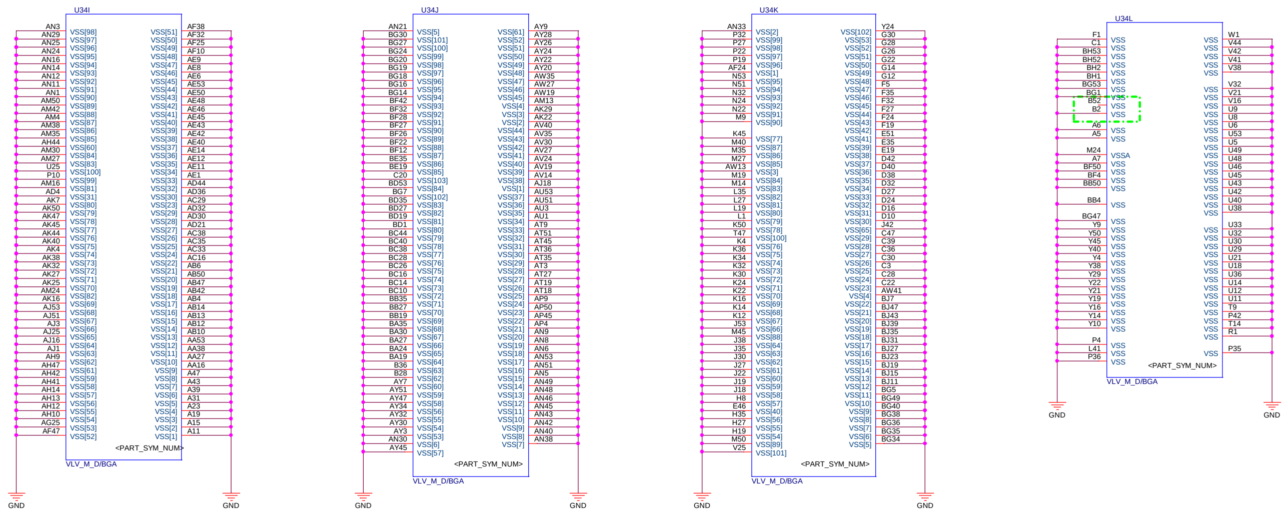
B52 is NC for layout issue



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PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

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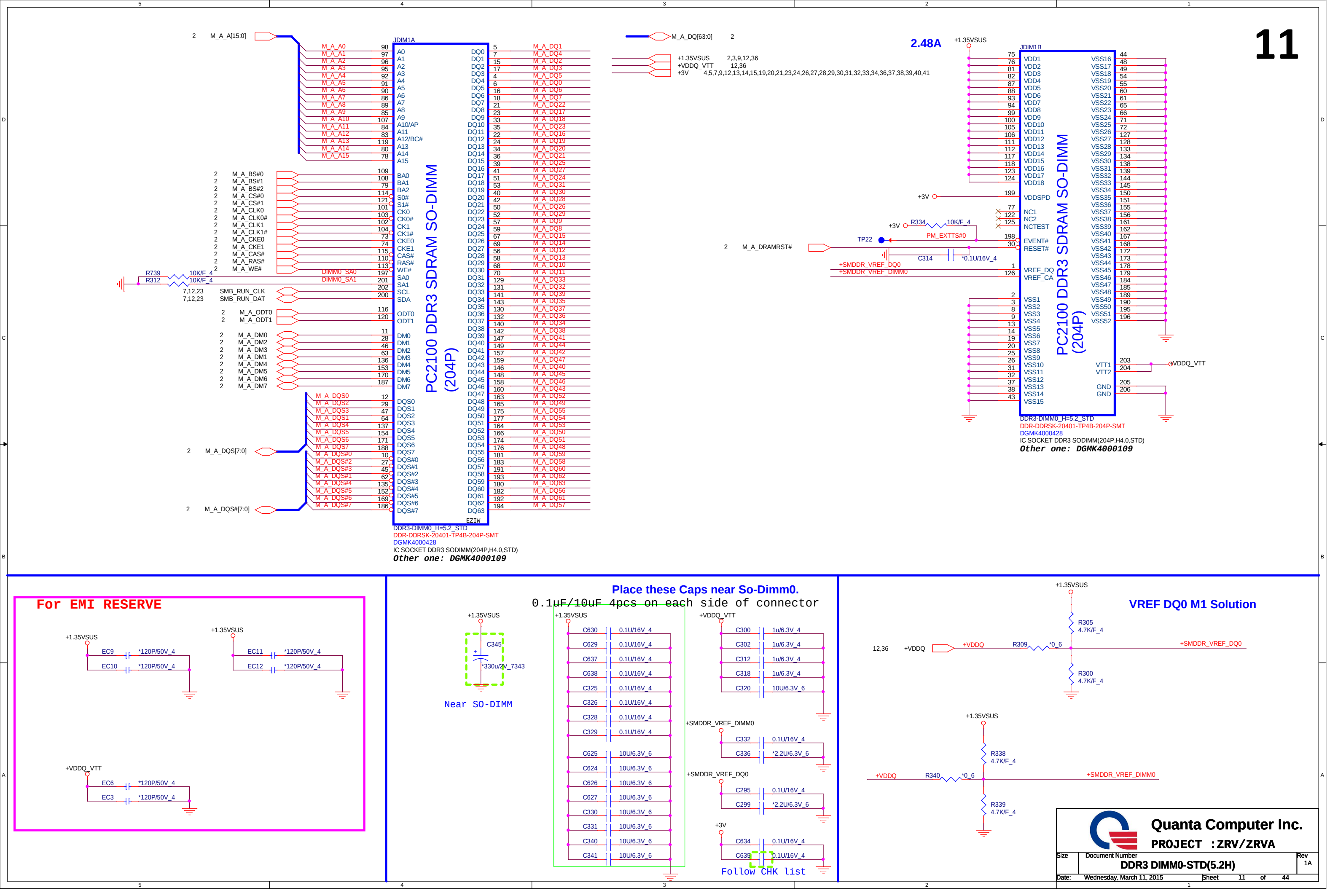
11
PC2100 DDR3 SDRAM SO-DIMM (204P)
JDIM1A
JDIM1B
2.48A
DDR3-DIMM0_H=5.2_STD
DDR-DDRSK-20401-TP4B-204P-SMT
DGMK4000428
IC SOCKET DDR3 SODIMM(204P,H4.0,STD)
Other one: DGMK4000109
For EMI RESERVE
Place these Caps near So-Dimm0.
0.1uF/10uF 4pcs on each side of connector
Near SO-DIMM
Follow CHK list
VREF DQ0 M1 Solution
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
Size
Document Number
Rev
DDR3 DIMM0-STD(5.2H)
1A
Date: Wednesday, March 11, 2015
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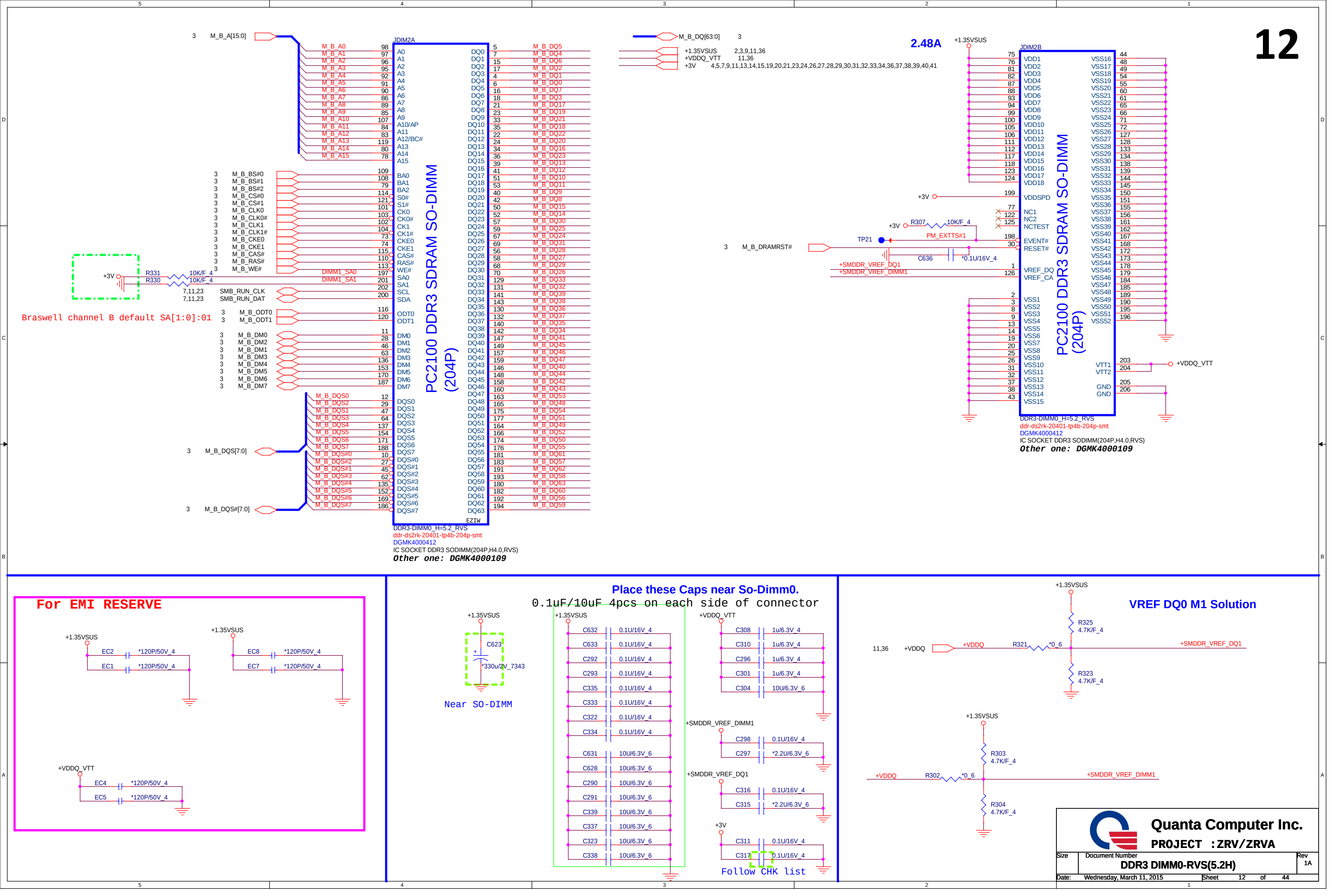
12
PC2100 DDR3 SDRAM SO-DIMM (204P)
JDIM2A
JDIM2B
DDR3-DIMM0_H=5.2_RVS
ddr-ds2rk-20401-tp4b-204p-smt
DGMK4000412
IC SOCKET DDR3 SODIMM(204P,H4.0,RVS)
Other one: DGMK4000109
2.48A
+1.35VSUS
M_B_A[15:0]
M_B_DQ[63:0]
M_B_DQS[7:0]
M_B_DQS#[7:0]
M_B_DRAMRST#
SMB_RUN_CLK
SMB_RUN_DAT
PM_EXTTS#1
+SMDDR_VREF_DQ1
+SMDDR_VREF_DIMM1
+VDDQ_VTT
Braswell channel B default SA[1:0]:01
For EMI RESERVE
Place these Caps near So-Dimm0.
0.1uF/10uF 4pcs on each side of connector
Near SO-DIMM
Follow CHK list
VREF DQ0 M1 Solution
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
DDR3 DIMM0-RVS(5.2H)
Rev 1A
Date: Wednesday, March 11, 2015
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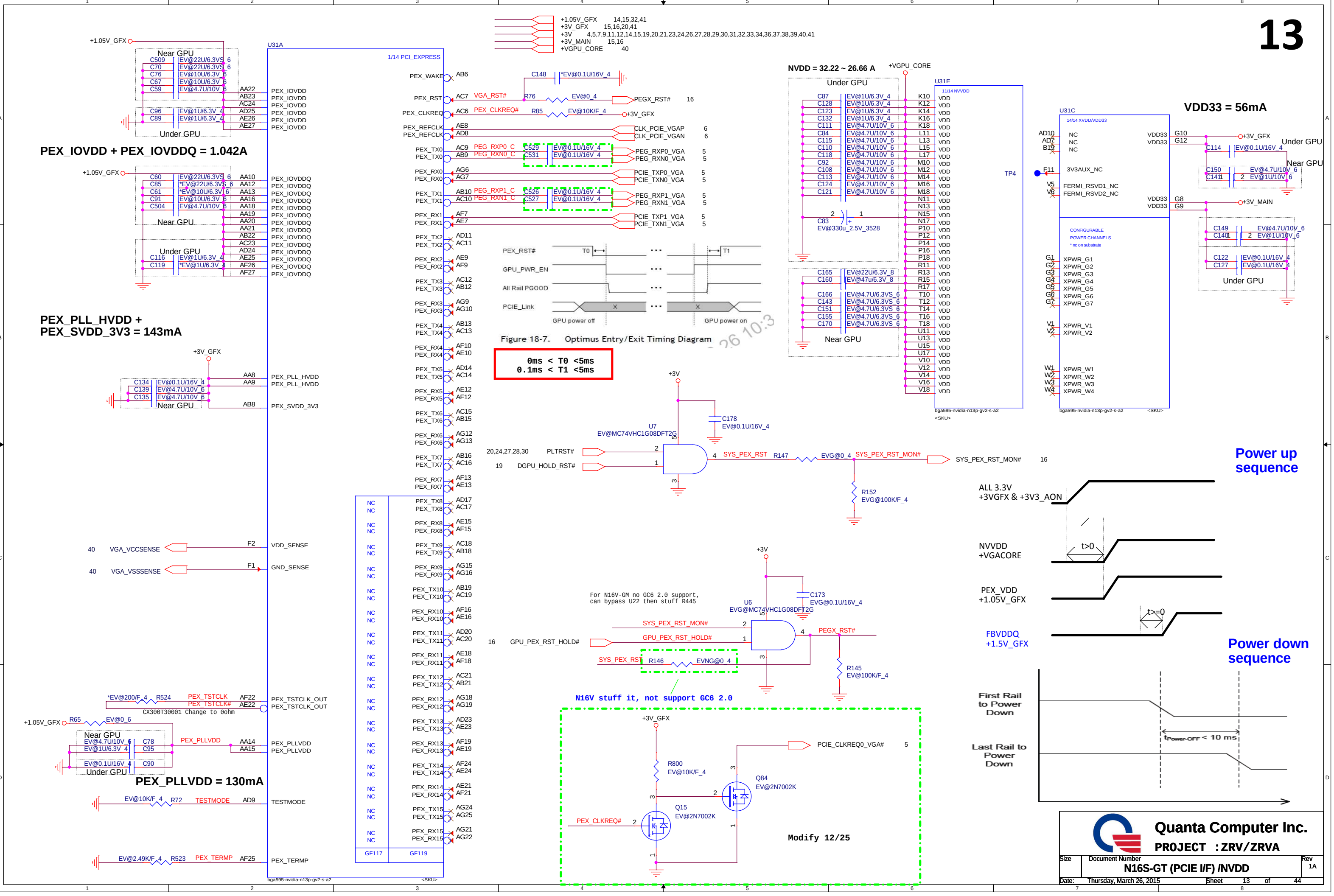
13
PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
U31A
1/14 PCI_EXPRESS
U31E
U31C
Near GPU
Under GPU
+1.05V_GFX 14,15,32,41
+3V_GFX 15,16,20,41
+3V 4,5,7,9,11,12,14,15,19,20,21,23,24,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41
+3V_MAIN 15,16
+VGPU_CORE 40
Figure 18-7. Optimus Entry/Exit Timing Diagram
PEX_RST#
GPU_PWR_EN
All Rail PGOOD
PCIE_Link
GPU power off
GPU power on
0ms < T0 <5ms
0.1ms < T1 <5ms
CX300T30001 Change to 0ohm
For N16V-GM no GC6 2.0 support, can bypass U22 then stuff R445
N16V stuff it, not support GC6 2.0
Modify 12/25
Power up sequence
ALL 3.3V
+3VGFX & +3V3_AON
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.5V_GFX
t>0
t>=0
Power down sequence
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
Size
Document Number
N16S-GT (PCIE I/F) /NVDD
Rev
1A
Date: Thursday, March 26, 2015
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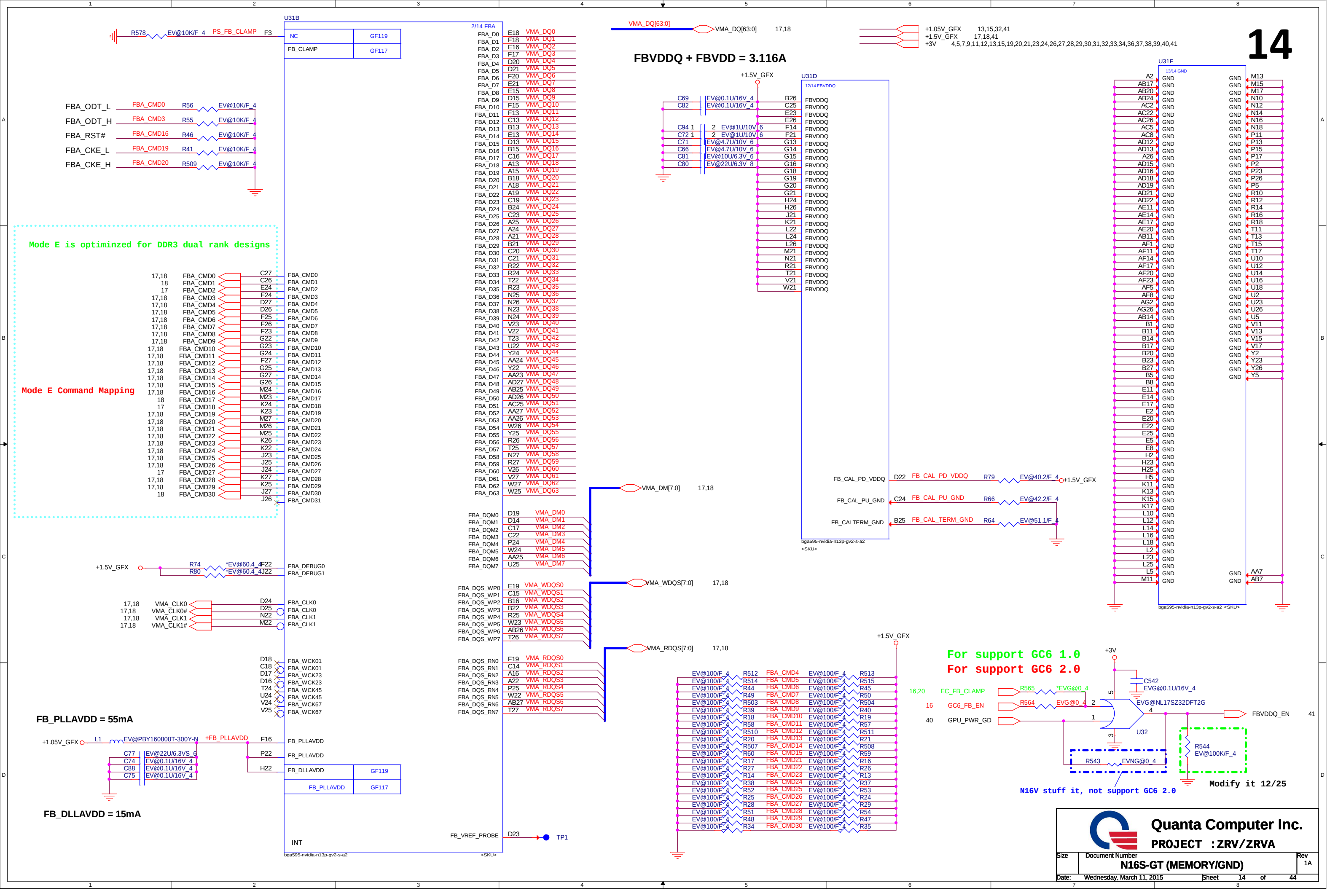
14
FBVDDQ + FBVDD = 3.116A
Mode E is optimized for DDR3 dual rank designs
Mode E Command Mapping
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
For support GC6 1.0
For support GC6 2.0
N16V stuff it, not support GC6 2.0
Modify it 12/25
U31B
U31D
U31F
U32
FBA_ODT_L
FBA_ODT_H
FBA_RST#
FBA_CKE_L
FBA_CKE_H
VMA_DQ[63:0]
VMA_DM[7:0]
VMA_WDQS[7:0]
VMA_RDQS[7:0]
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CALTERM_GND
FB_VREF_PROBE
FBVDDQ_EN
GC6_FB_EN
GPU_PWR_GD
EC_FB_CLAMP
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
Document Number
N16S-GT (MEMORY/GND)
Rev
1A
Date: Wednesday, March 11, 2015
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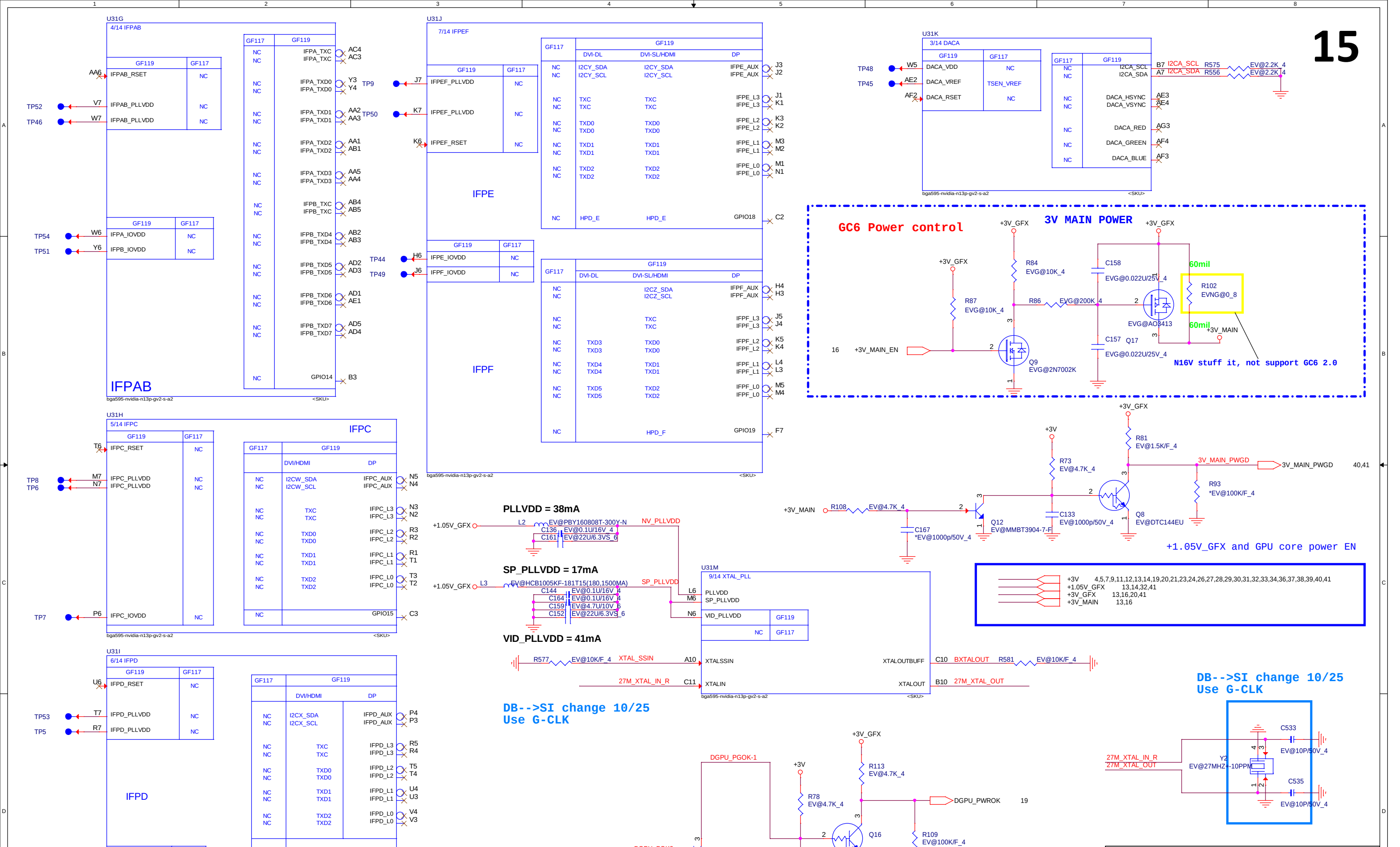

Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	N16S-GT (DISPLAY)	1A
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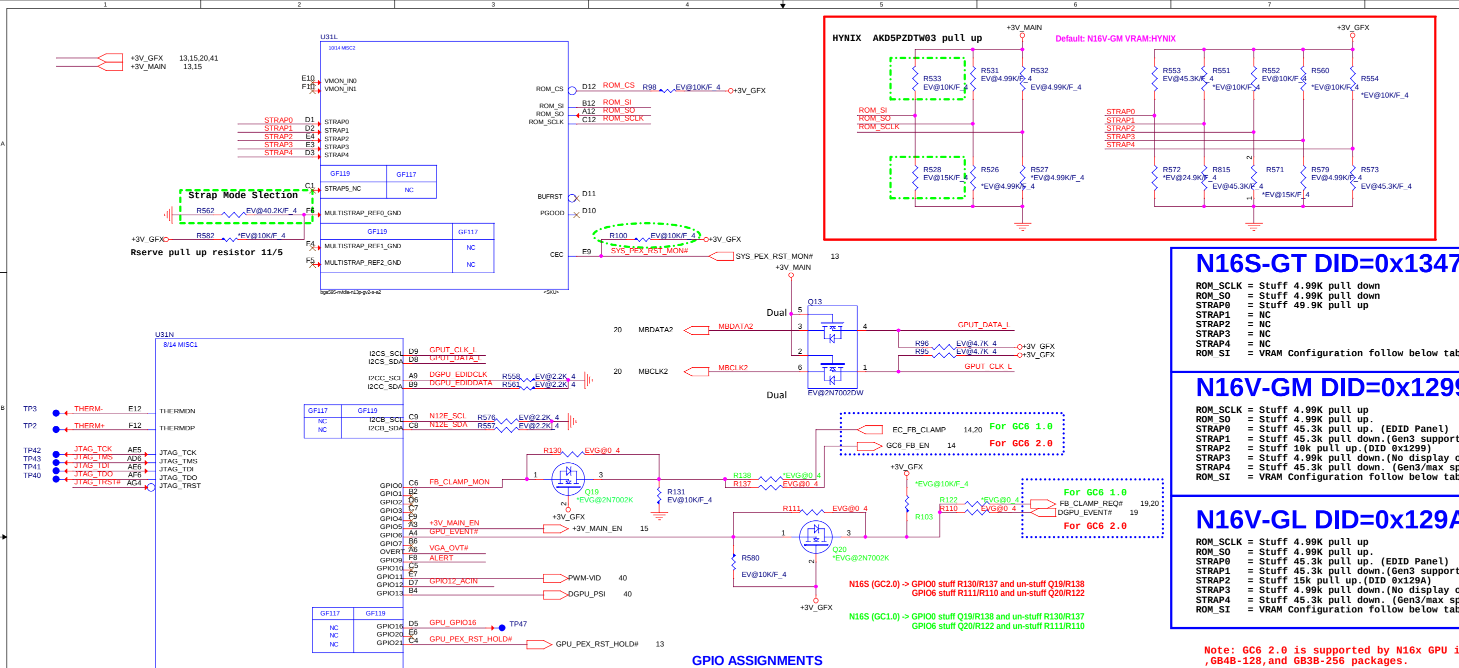


N16S-GT DID=0x1347 GB2B-64

ROM_SCLK = Stuff 4.99K pull down
ROM_SO = Stuff 4.99K pull down
STRAP0 = Stuff 49.9K pull up
STRAP1 = NC
STRAP2 = NC
STRAP3 = NC
STRAP4 = NC
ROM_SI = VRAM Configuration follow below table

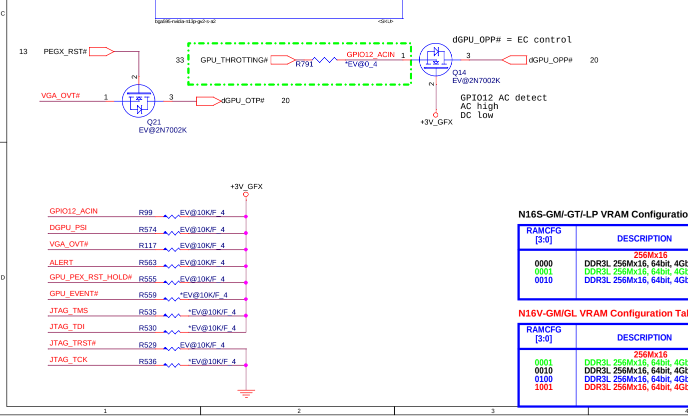
N16V-GM DID=0x1299 GB2-64

ROM_SCLK = Stuff 4.99K pull up
ROM_SO = Stuff 4.99K pull up.
STRAP0 = Stuff 45.3k pull up. (EDID Panel)
STRAP1 = Stuff 45.3k pull down.(Gen3 support)
STRAP2 = Stuff 10k pull up.(DID 0x1299)
STRAP3 = Stuff 4.99k pull down.(No display out)
STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI = VRAM Configuration follow below table

N16V-GL DID=0x129A GB2-64

ROM_SCLK = Stuff 4.99K pull up
ROM_SO = Stuff 4.99K pull up.
STRAP0 = Stuff 45.3k pull up. (EDID Panel)
STRAP1 = Stuff 45.3k pull down.(Gen3 support)
STRAP2 = Stuff 15k pull up.(DID 0x129A)
STRAP3 = Stuff 4.99k pull down.(No display out)
STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI = VRAM Configuration follow below table

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.



GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

N16S-GM/-GT/-LP VRAM Configuration Table ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					Single Rank or Single Rank stuffing for Dual Rank
0000	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63AFR-11C	PD 4.9K ohm	AKD5PGWTW13	
0001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	
0010	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG	K4W4G1646D-BC1A	PD 15K ohm	AKD5PGWT504	Dual Rank

N16V-GM/GL VRAM Configuration Table ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					Single Rank or Single Rank stuffing for Dual Rank
0001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	
0010	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63AFR-11C	PD 15K ohm	AKD5PGWTW13	
0100	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG	K4W4G1646D-BC1A	PD 24.9K ohm	AKD5PGWT504	
1001	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63CFR-N0C	PU 10K ohm	AKD5PZDTW03	

Quanta Computer Inc.
PROJECT : ZRV/ZRVA

Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev 1A
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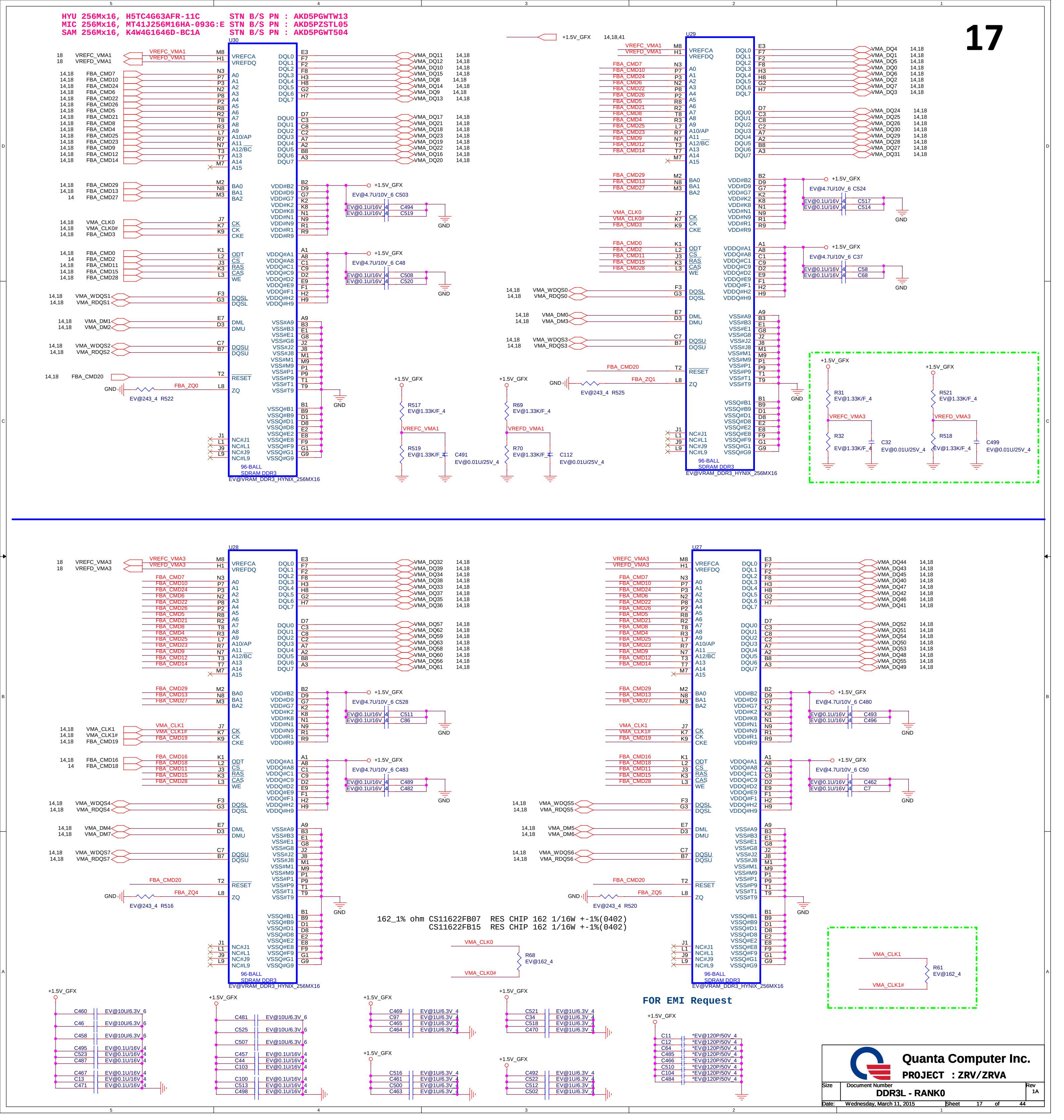

HYU 256Mx16, H5TC4G63AFR-11C STN B/S PN : AKD5PGWTW13
MIC 256Mx16, MT41J256M16HA-093G:E STN B/S PN : AKD5PZSTL05
SAM 256Mx16, K4W4G1646D-BC1A STN B/S PN : AKD5PGWT504
17
U30
U29
U28
U27
96-BALL SDRAM DDR3
EV@VRAM_DDR3_HYNIX_256MX16
+1.5V_GFX
GND
162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)
FOR EMI Request
Quanta Computer Inc.
PROJECT : ZRV/ZRVA
Size
Document Number
DDR3L - RANK0
Rev
1A
Date: Wednesday, March 11, 2015
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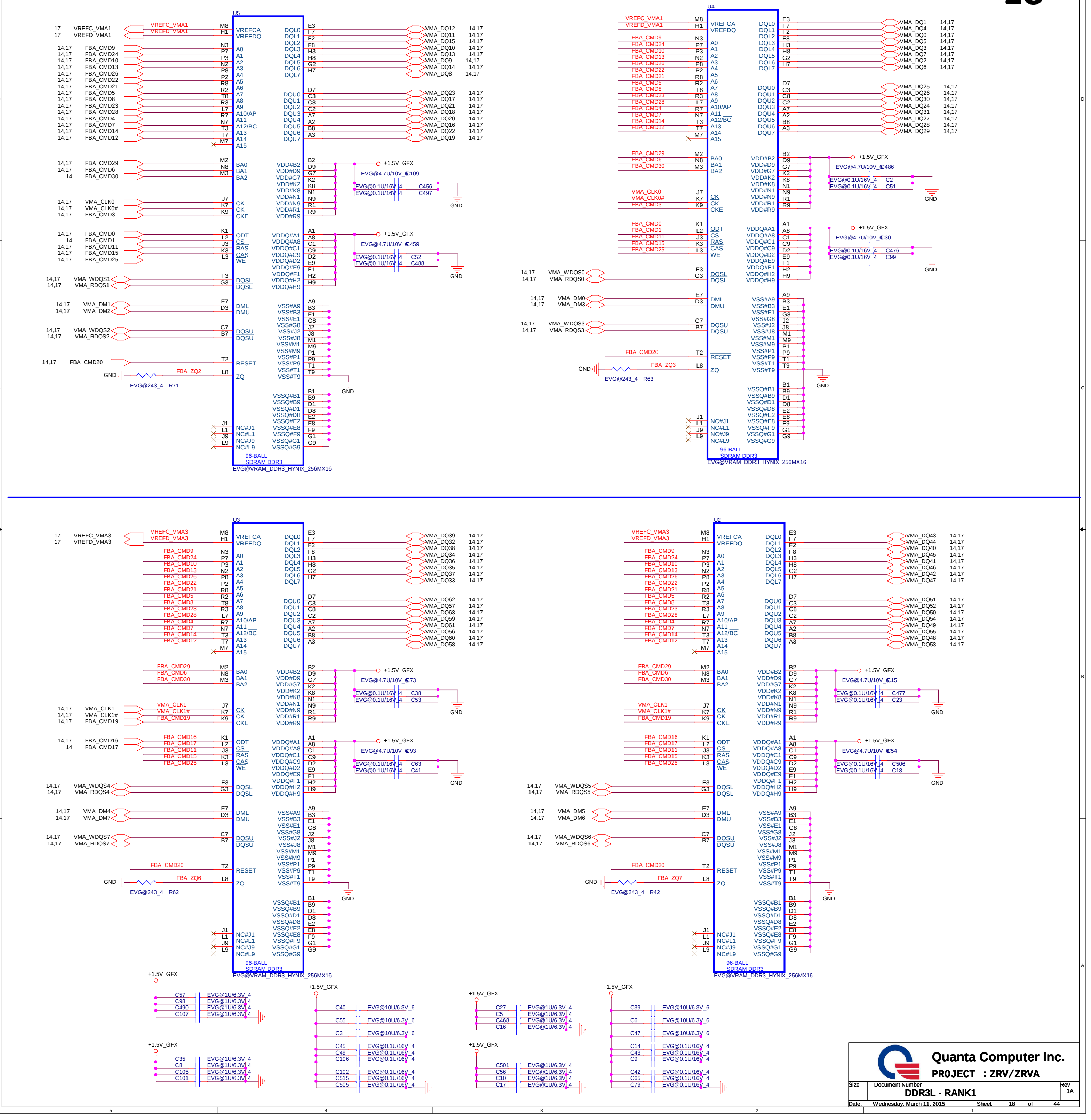
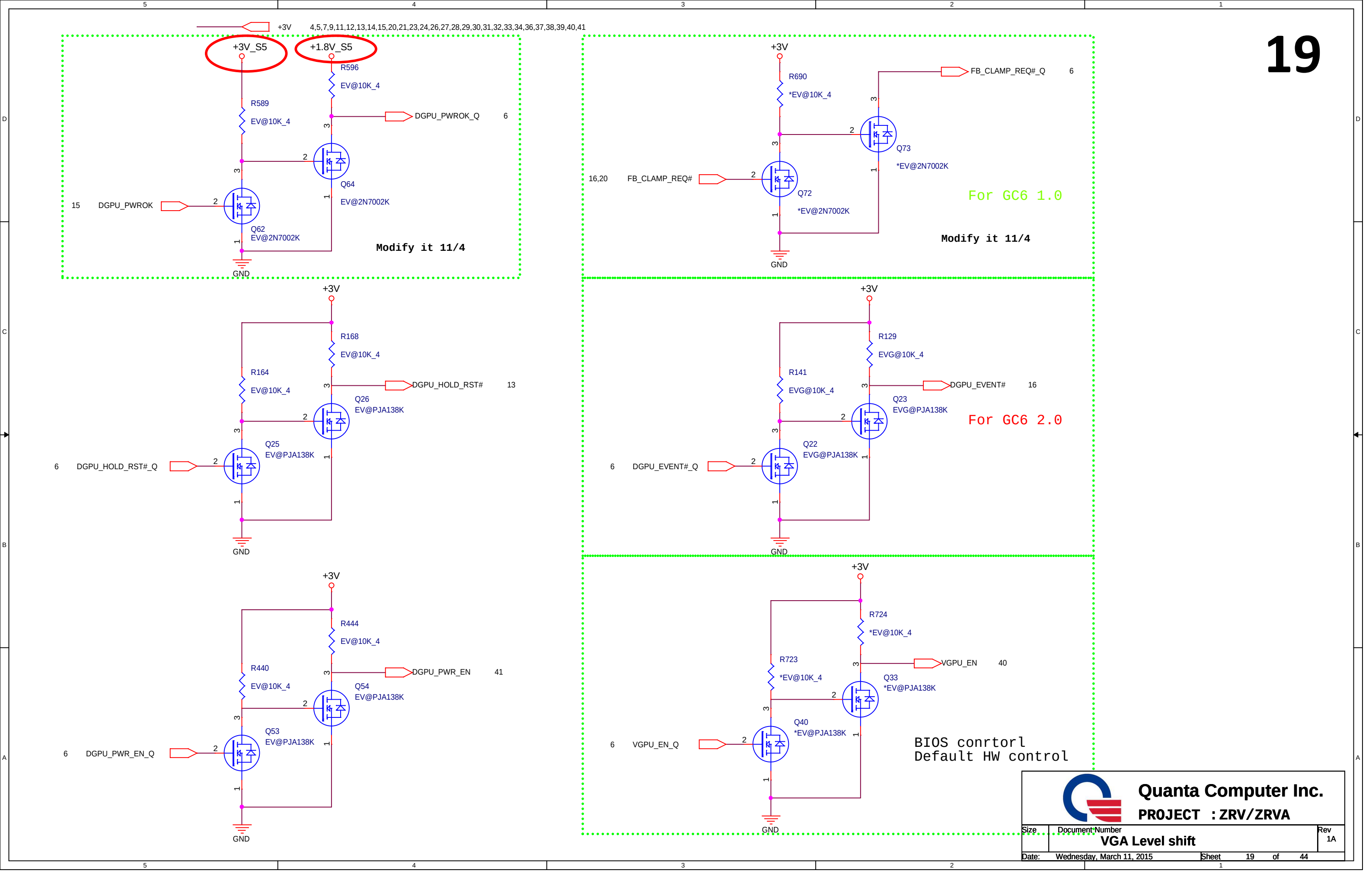
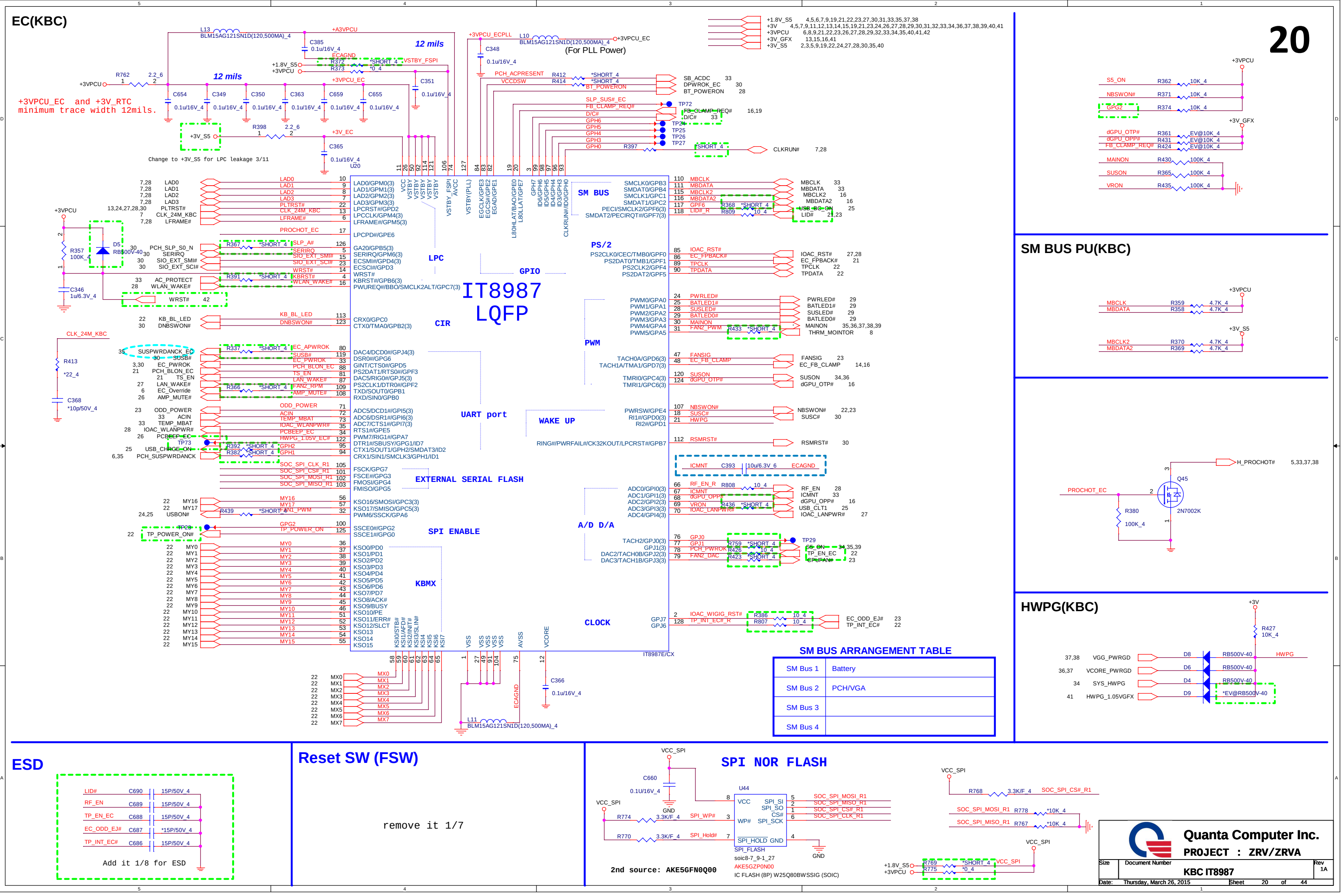
Rank 1 for N16S-GT(support Dual Rank)

HYU 256Mx16, H5TC4G63AFR-11C STN B/S PN : AKD5PGWTW13
MIC 256Mx16, MT41J256M16HA-093G:E STN B/S PN : AKD5PZSTL05
SAM 256Mx16, K4W4G1646D-BC1A STN B/S PN : AKD5PGWT504



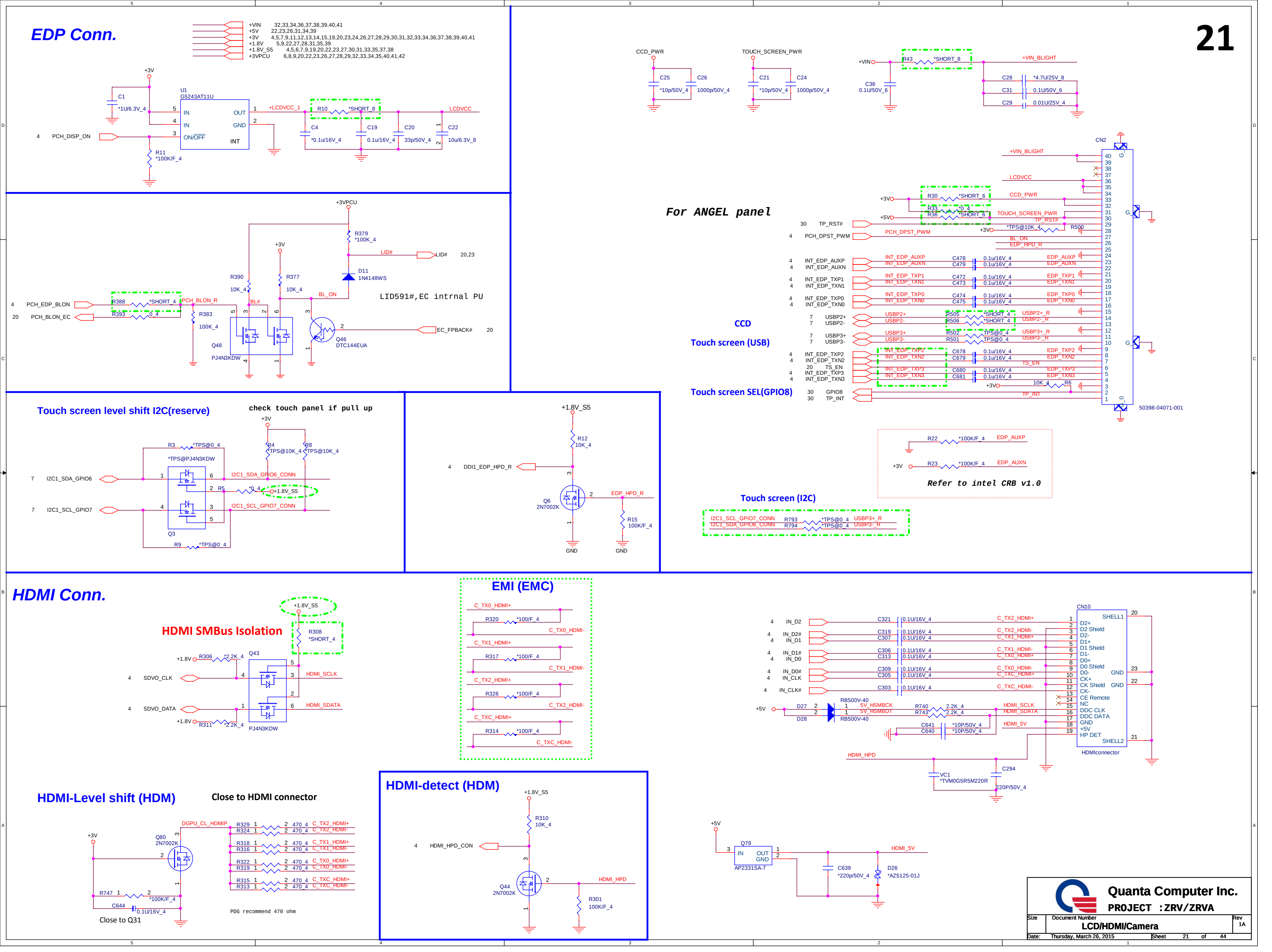


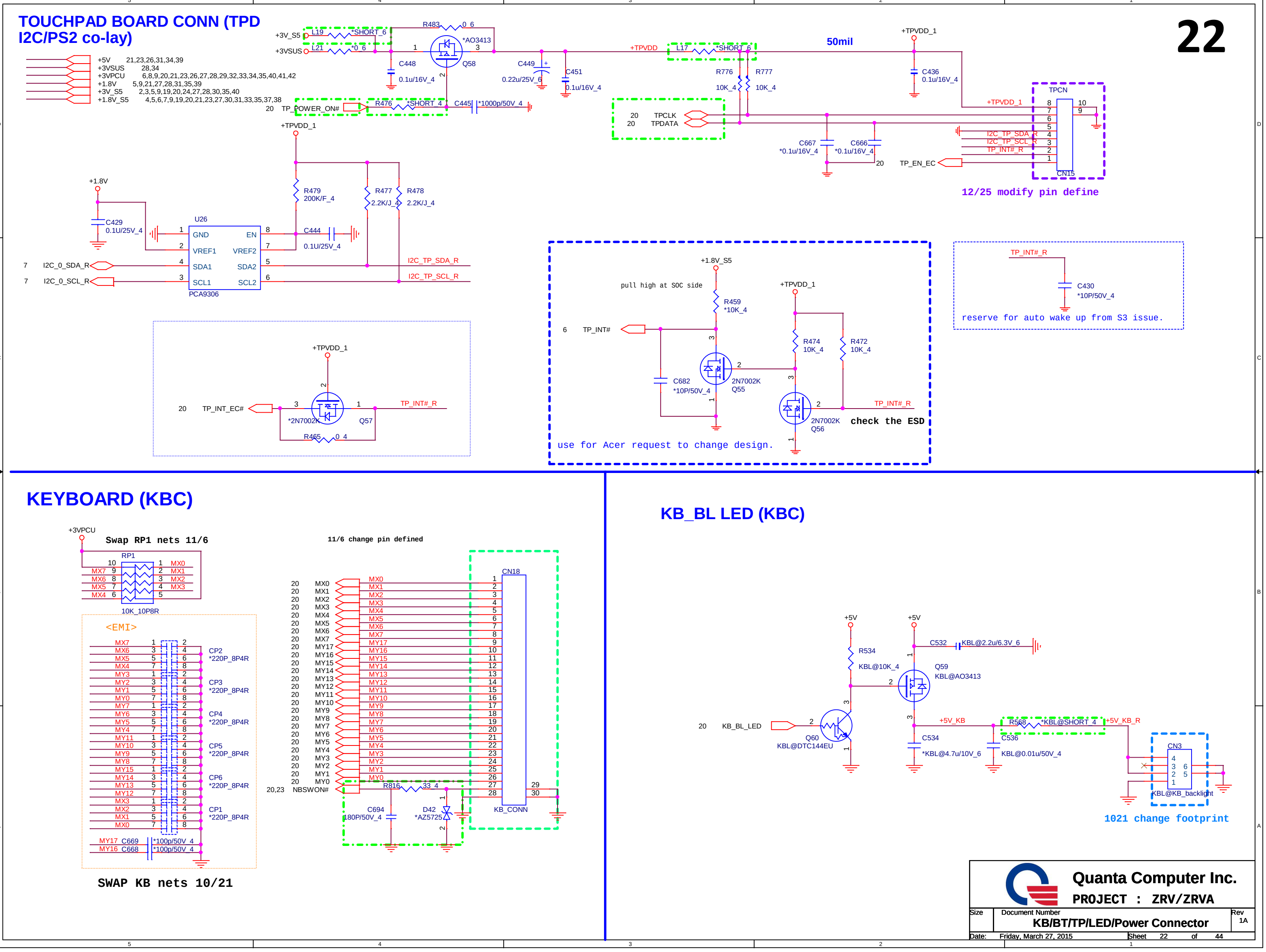
+3V 4,5,7,9,11,12,13,14,15,20,21,23,24,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41
+3V_S5
+1.8V_S5
R596
EV@10K_4
DGPU_PWROK_Q 6
R589
EV@10K_4
Q64
EV@2N7002K
15 DGPU_PWROK
Q62
EV@2N7002K
GND
Modify it 11/4
+3V
R690
*EV@10K_4
FB_CLAMP_REQ#_Q 6
Q73
*EV@2N7002K
16,20 FB_CLAMP_REQ#
Q72
*EV@2N7002K
For GC6 1.0
Modify it 11/4
GND
+3V
R168
EV@10K_4
R164
EV@10K_4
DGPU_HOLD_RST# 13
Q26
EV@PJA138K
Q25
EV@PJA138K
6 DGPU_HOLD_RST#_Q
GND
+3V
R129
EVG@10K_4
R141
EVG@10K_4
DGPU_EVENT# 16
Q23
EVG@PJA138K
For GC6 2.0
Q22
EVG@PJA138K
6 DGPU_EVENT#_Q
GND
+3V
R444
EV@10K_4
R440
EV@10K_4
DGPU_PWR_EN 41
Q54
EV@PJA138K
Q53
EV@PJA138K
6 DGPU_PWR_EN_Q
GND
+3V
R724
*EV@10K_4
R723
*EV@10K_4
VGPU_EN 40
Q33
*EV@PJA138K
Q40
*EV@PJA138K
6 VGPU_EN_Q
BIOS conrtorl
Default HW control
GND
Quanta Computer Inc.
PROJECT : ZRV/ZRVA
Size
Document Number
VGA Level shift
Rev
1A
Date: Wednesday, March 11, 2015
Sheet 19 of 44



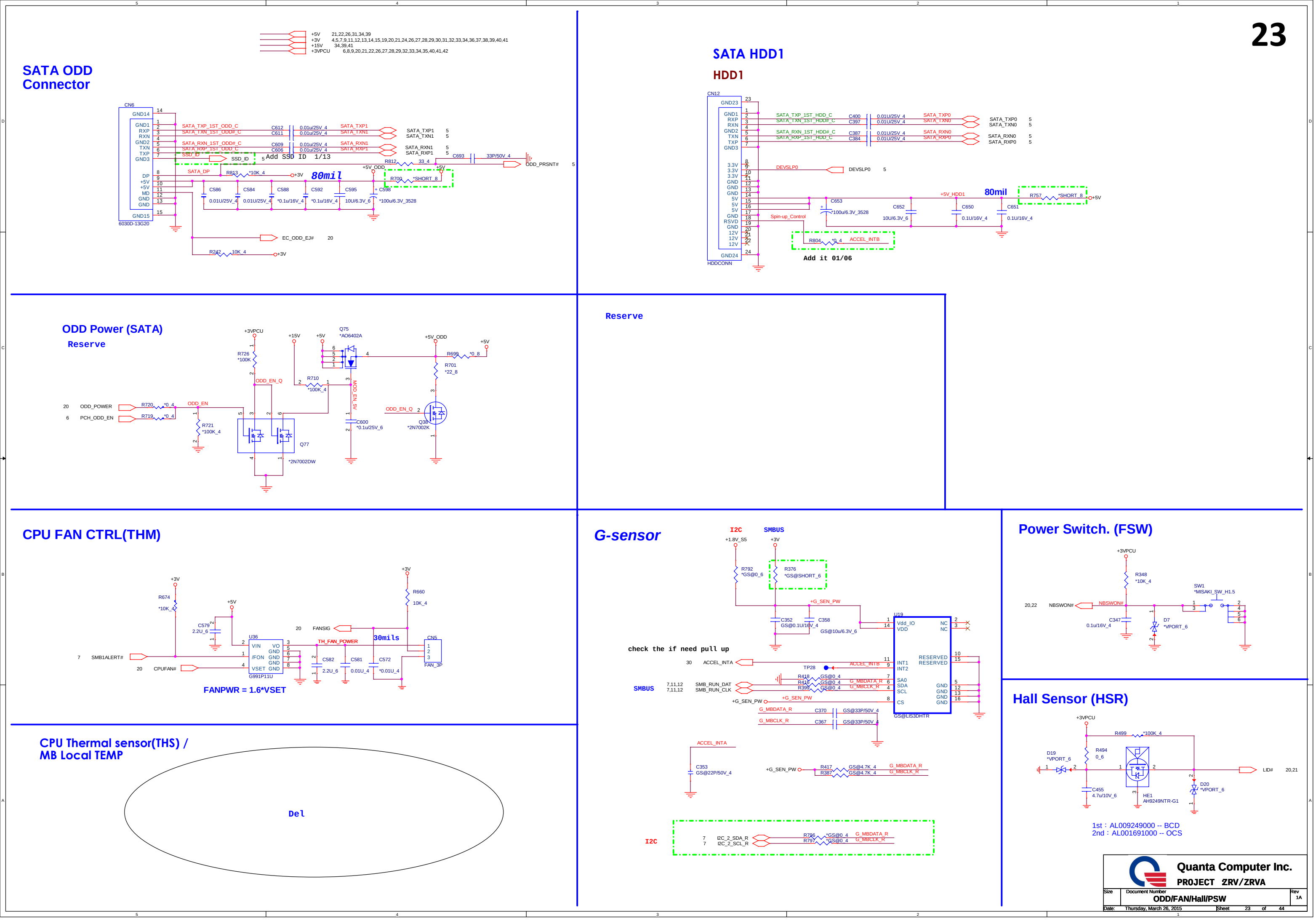
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

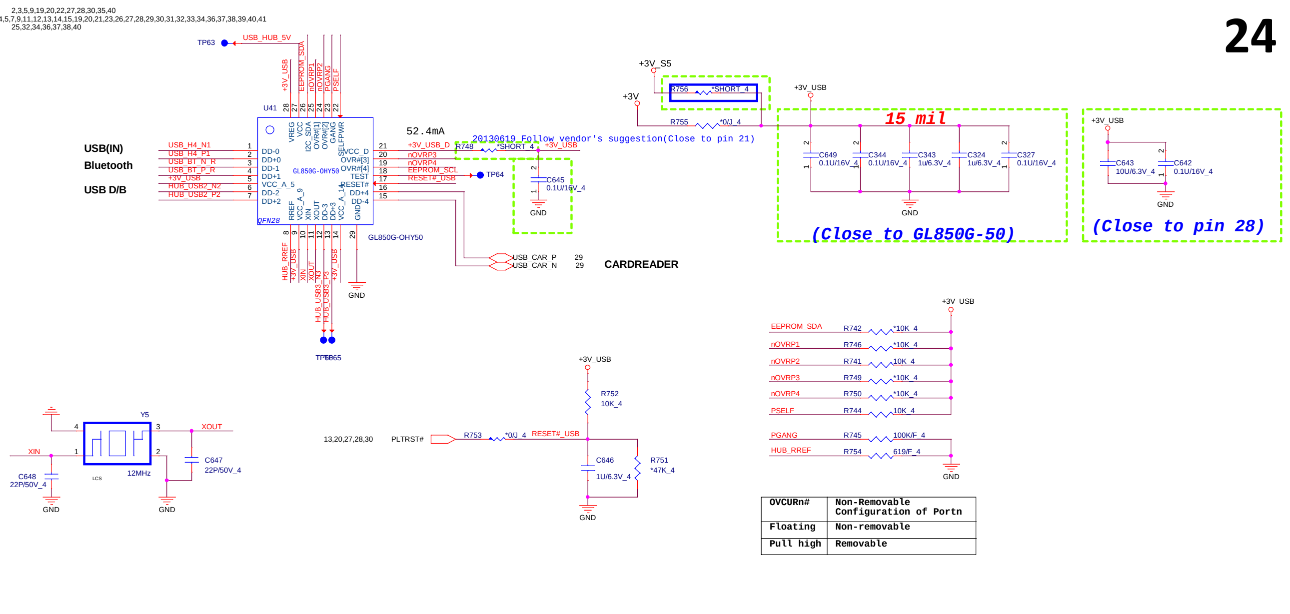

EDP Conn.
For ANGEL panel
CCD
Touch screen (USB)
Touch screen SEL(GPIO8)
LID591#,EC intrnal PU
Touch screen level shift I2C(reserve)
check touch panel if pull up
Refer to intel CRB v1.0
Touch screen (I2C)
HDMI Conn.
HDMI SMBus Isolation
EMI (EMC)
HDMI-Level shift (HDM)
Close to HDMI connector
HDMI-detect (HDM)
Close to Q31
PDG recommend 470 ohm
HDMIconnector
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
LCD/HDMI/Camera
Thursday, March 26, 2015
Sheet 21 of 44
Rev 1A



TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)
22
50mil
12/25 modify pin define
reserve for auto wake up from S3 issue.
pull high at SOC side
use for Acer request to change design.
check the ESD
U26
PCA9306
TPCN
KEYBOARD (KBC)
Swap RP1 nets 11/6
11/6 change pin defined
<EMI>
SWAP KB nets 10/21
KB_CONN
KB_BL LED (KBC)
1021 change footprint
Quanta Computer Inc.
PROJECT : ZRV/ZRVA
KB/BT/TP/LED/Power Connector
Rev 1A
Date: Friday, March 27, 2015
Sheet 22 of 44


23
SATA ODD Connector
+5V 21,22,26,31,34,39
+3V 4,5,7,9,11,12,13,14,15,19,20,21,24,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41
+15V 34,39,41
+3VPCU 6,8,9,20,21,22,26,27,28,29,32,33,34,35,40,41,42
CN6
SATA_TXP1
SATA_TXN1
SATA_RXN1
SATA_RXP1
SSD_ID
Add SSD ID 1/13
80mil
ODD_PRSNT#
EC_ODD_EJ#
60300-13G20
SATA HDD1
HDD1
CN12
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
DEVSLP0
Spin-up_Control
ACCEL_INTB
Add it 01/06
HDDCONN
ODD Power (SATA)
Reserve
ODD_POWER
PCH_ODD_EN
ODD_EN
ODD_EN_Q
Q75
*AO6402A
Q77
*2N7002DW
Q38
*2N7002K
Reserve
CPU FAN CTRL(THM)
SMB1ALERT#
CPUFAN#
FANSIG
TH_FAN_POWER
30mils
U36
G991P11U
CN5
FAN_3P
FANPWR = 1.6*VSET
CPU Thermal sensor(THS) / MB Local TEMP
Del
G-sensor
I2C
SMBUS
check the if need pull up
ACCEL_INTA
SMB_RUN_DAT
SMB_RUN_CLK
U19
GS@LIS3DHTR
G_MBDATA_R
G_MBCLK_R
I2C_2_SDA_R
I2C_2_SCL_R
Power Switch. (FSW)
NBSWON#
SW1
*MISAKI_SW_H1.5
Hall Sensor (HSR)
HE1
AH9249NTR-G1
LID#
1st：AL009249000 -- BCD
2nd：AL001691000 -- OCS
Quanta Computer Inc.
PROJECT ZRV/ZRVA
ODD/FAN/Hall/PSW
Thursday, March 26, 2015
Sheet 23 of 44
Rev 1A

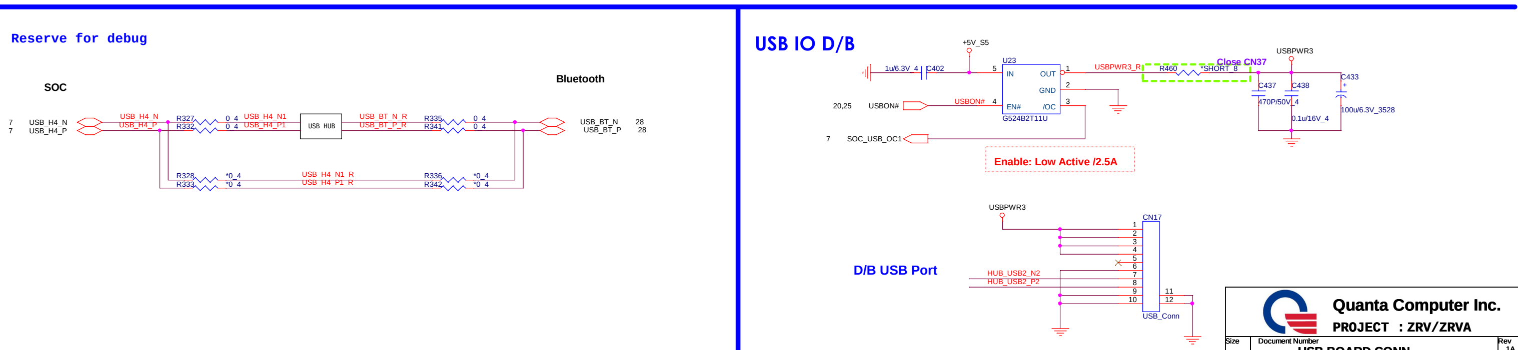
USB HUB



OVCURn#	Non-Removable Configuration of Portn
Floating	Non-removable
Pull high	Removable

Reserve for debug

USB IO D/B



Quanta Computer Inc.

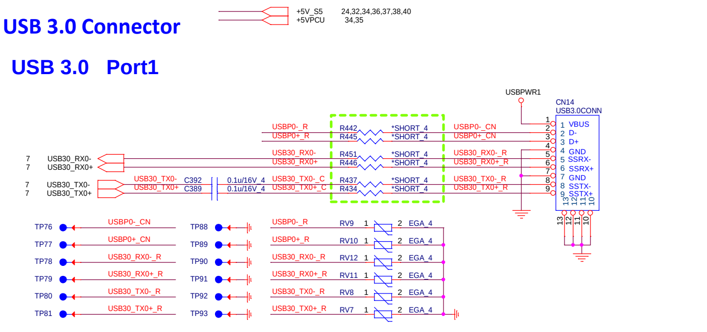
PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	USB BOARD CONN	1A

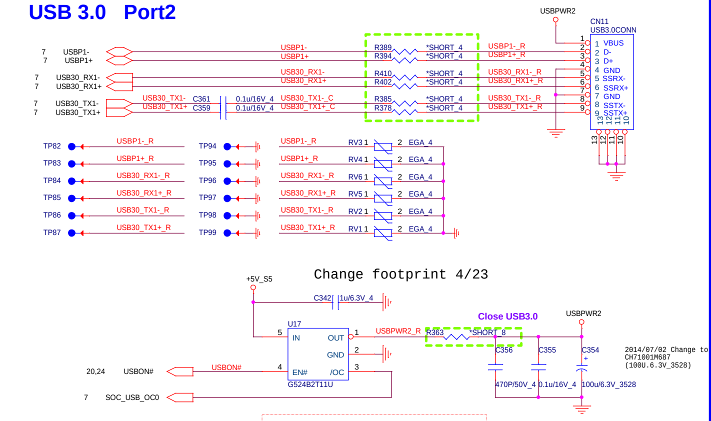
Date: Thursday, March 26, 2015 Sheet 24 of 44

USB 3.0 Connector

USB 3.0 Port1



USB 3.0 Port2



USB Charger for USB3.0 Port0 (UBC)

Truth Table

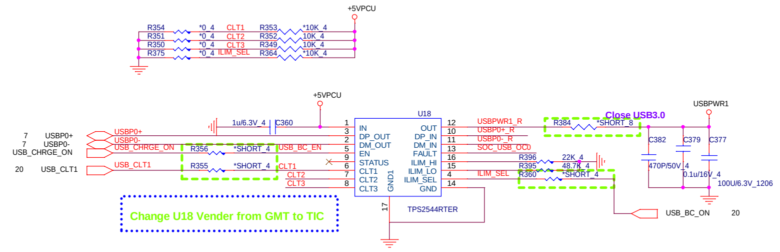
CTL1	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	DCP_Auto	ILIM_HI	OFF	Data disconnected
0	1	DCP_Auto	ILIM_HI	DCP	Data disconnected
1	0	SDP2(1)	ILIM_LO	OFF	Data connected
1	1	CDP(1)	ILIM_HI	CDP	Data connected

16.9kΩ <= RILIMx <= 750kΩ

I=50250/RILIMx

ILIM_HI: 2.28A

ILIM_LO: 1.03A

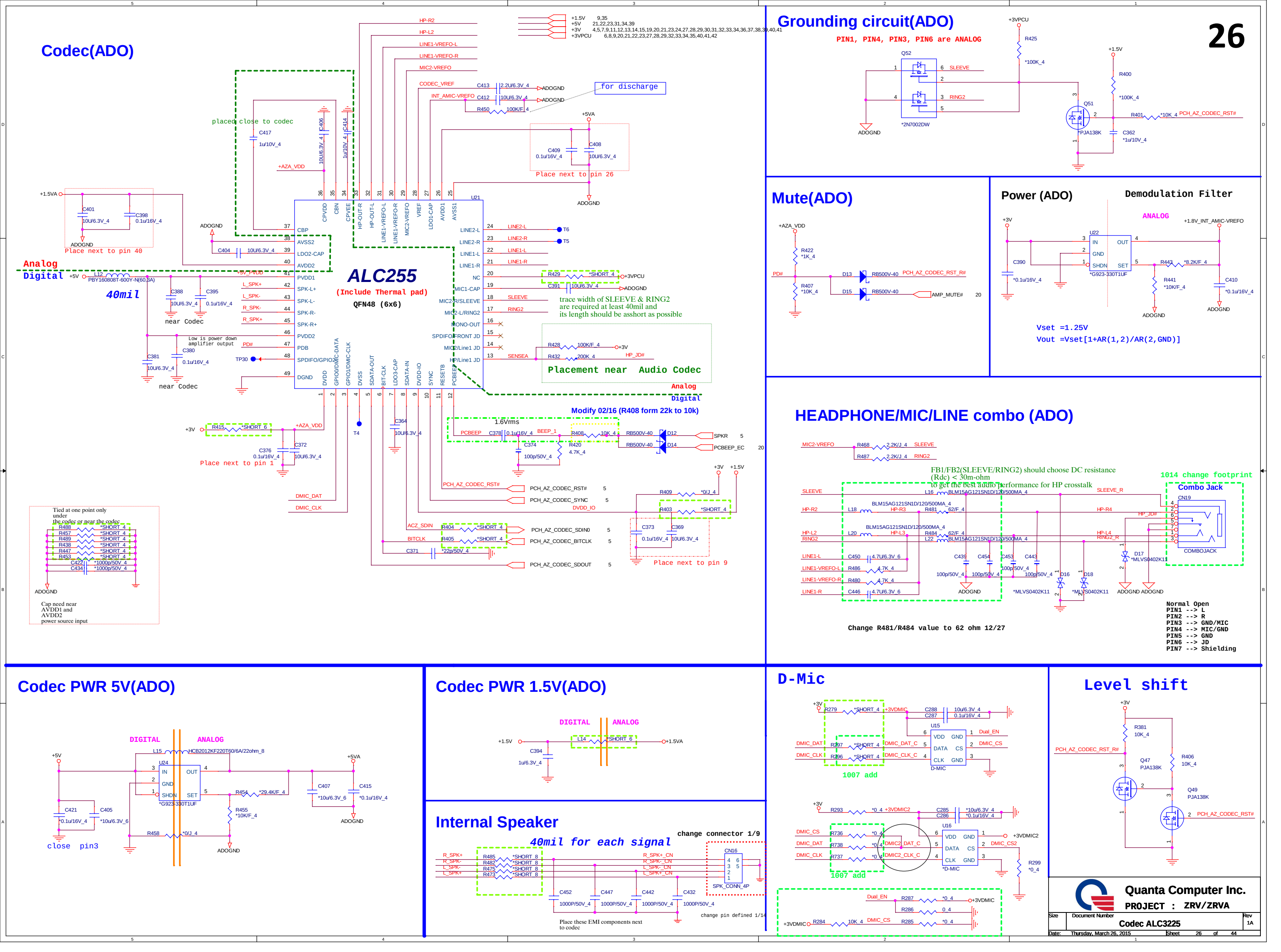


Quanta Computer Inc.

PROJECT :ZRV/ZRVA

Size	Document Number	Rev
	USB 3.0	1A

Date: Wednesday, April 01, 2015 Sheet 25 of 44



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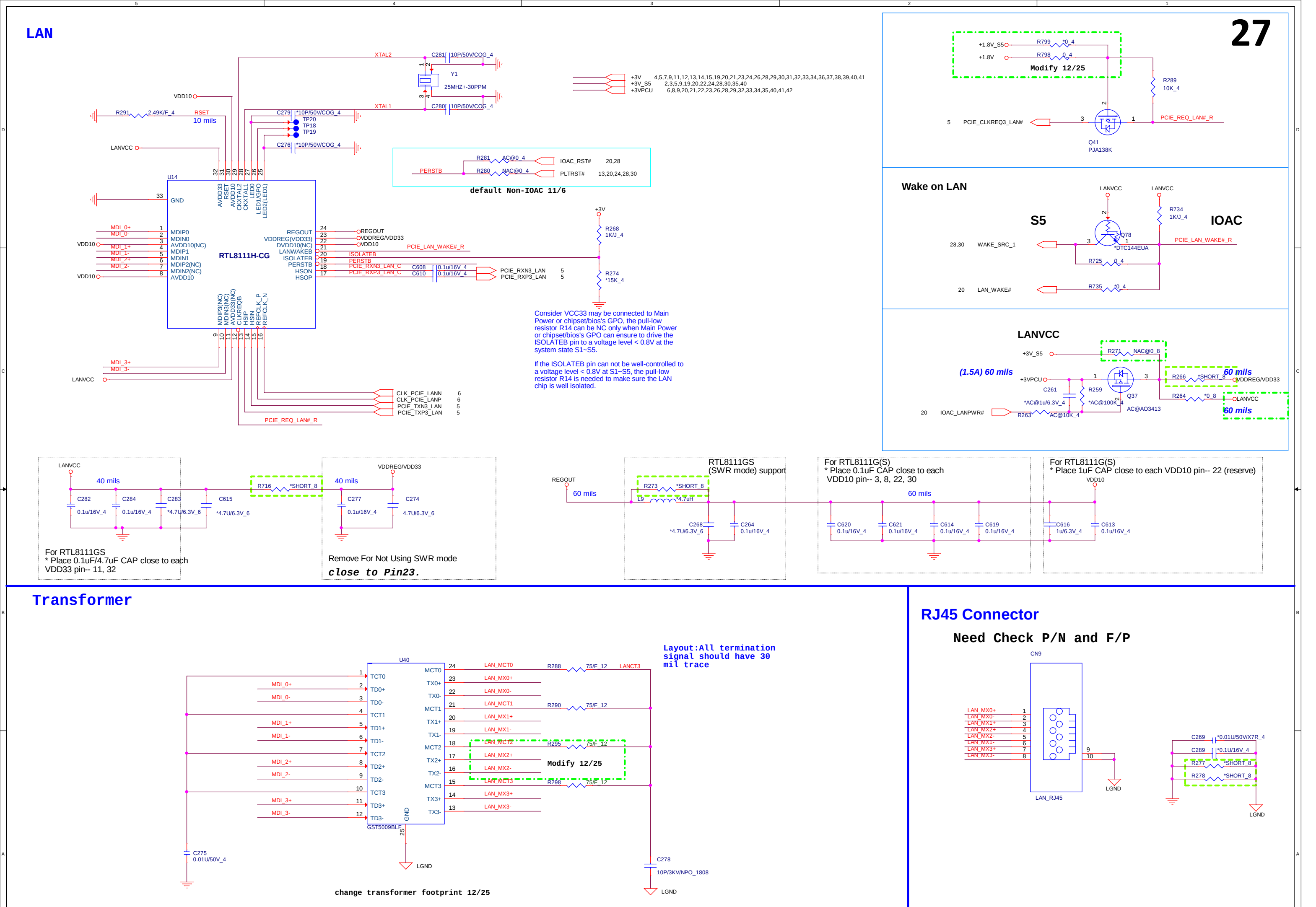

Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	LAN	1A

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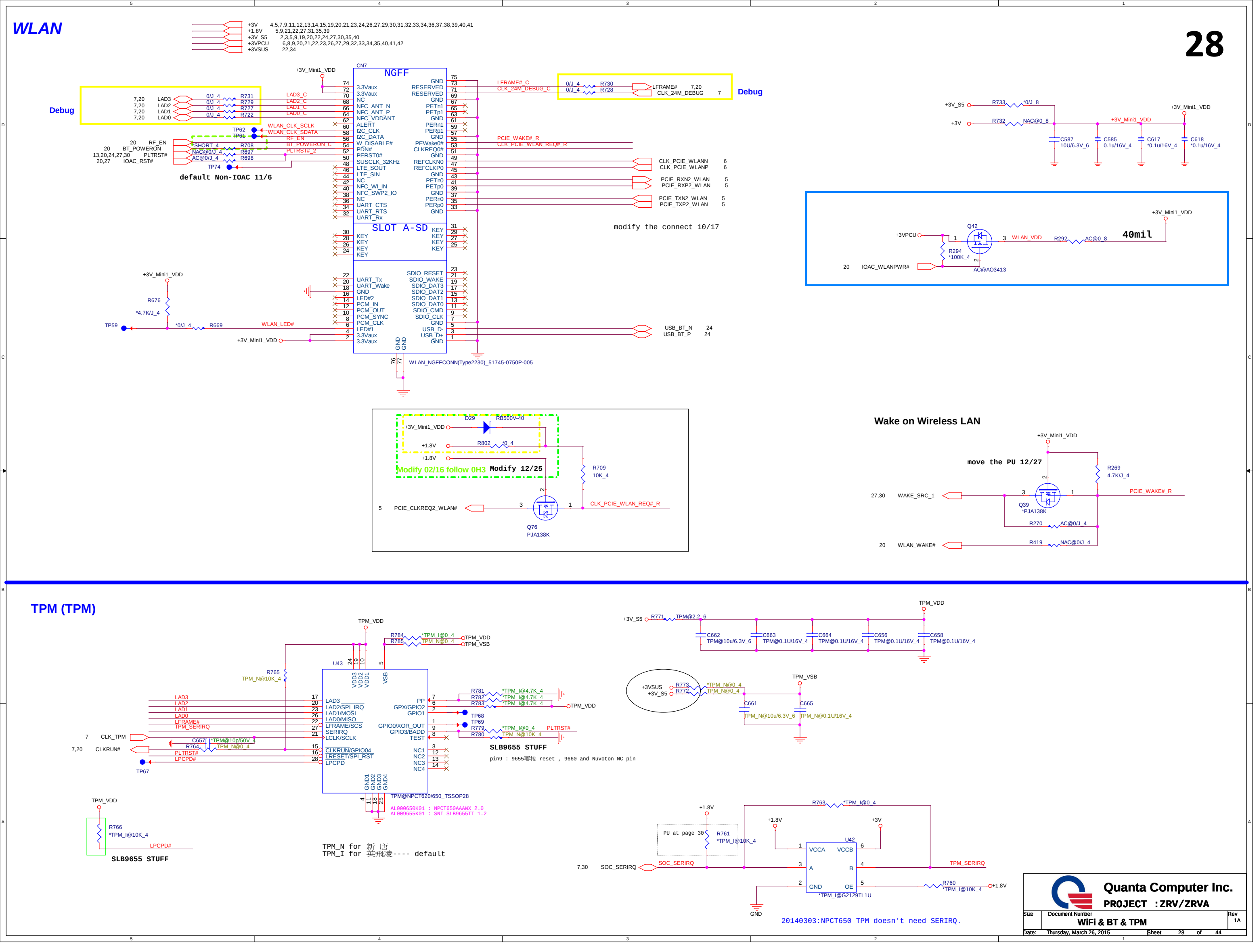
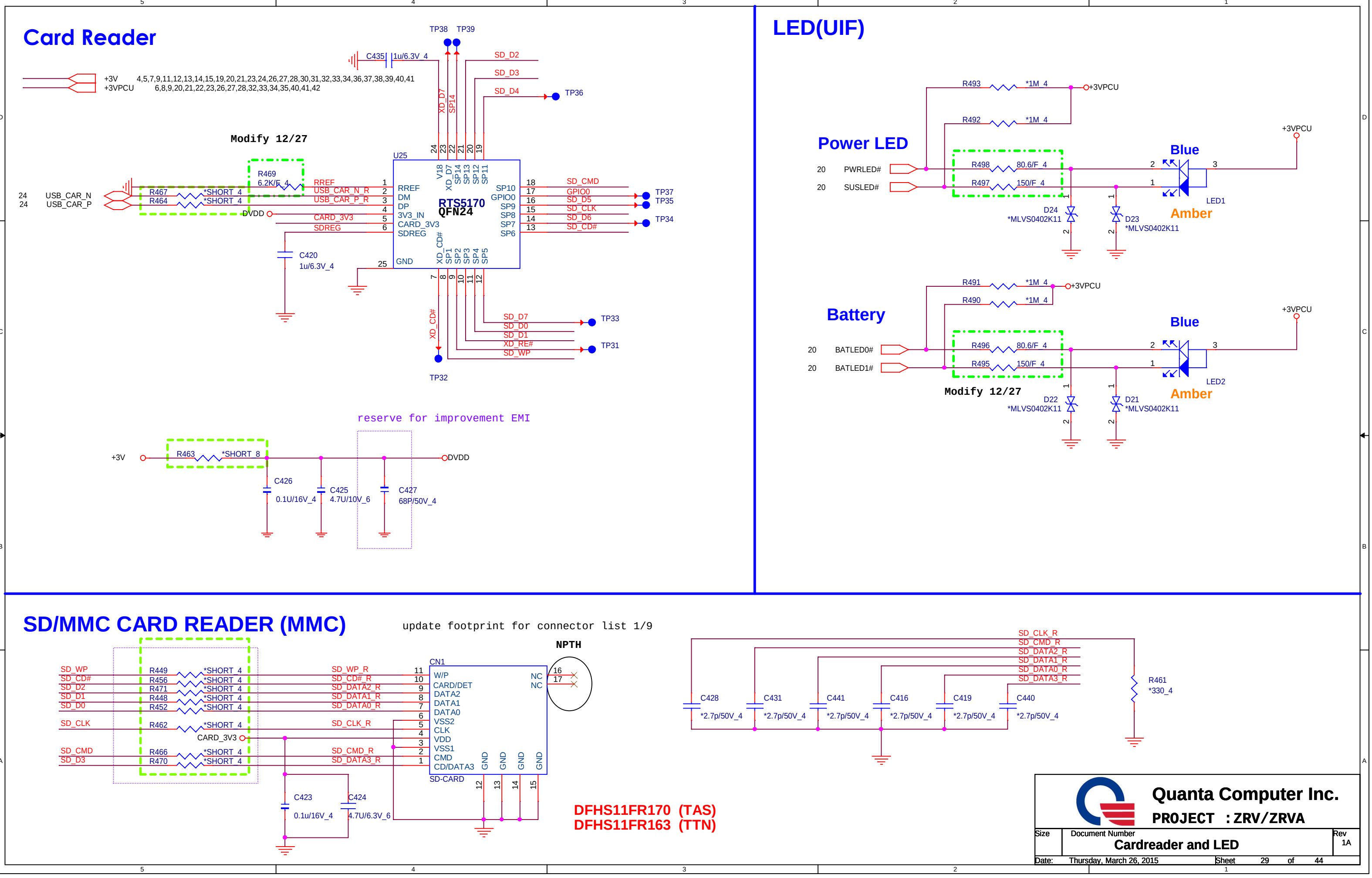


WLAN
28
Debug
NGFF
SLOT A-SD
default Non-IOAC 11/6
modify the connect 10/17
WLAN_NGFFCONN(Type2230)_51745-0750P-005
40mil
IOAC_WLANPWR#
AC@AO3413
Modify 02/16 follow 0H3
Modify 12/25
PCIE_CLKREQ2_WLAN#
CLK_PCIE_WLAN_REQ#_R
PJA138K
Wake on Wireless LAN
move the PU 12/27
WAKE_SRC_1
PCIE_WAKE#_R
WLAN_WAKE#
TPM (TPM)
SLB9655 STUFF
TPM@NPCT620/650_TSSOP28
pin9 : 9655要接 reset , 9660 and Nuvoton NC pin
TPM_N for 新 唐
TPM_I for 英飛凌---- default
PU at page 30
SOC_SERIRQ
TPM_SERIRQ
20140303:NPCT650 TPM doesn't need SERIRQ.
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
WiFi & BT & TPM
Thursday, March 26, 2015
Sheet 28 of 44
Rev 1A



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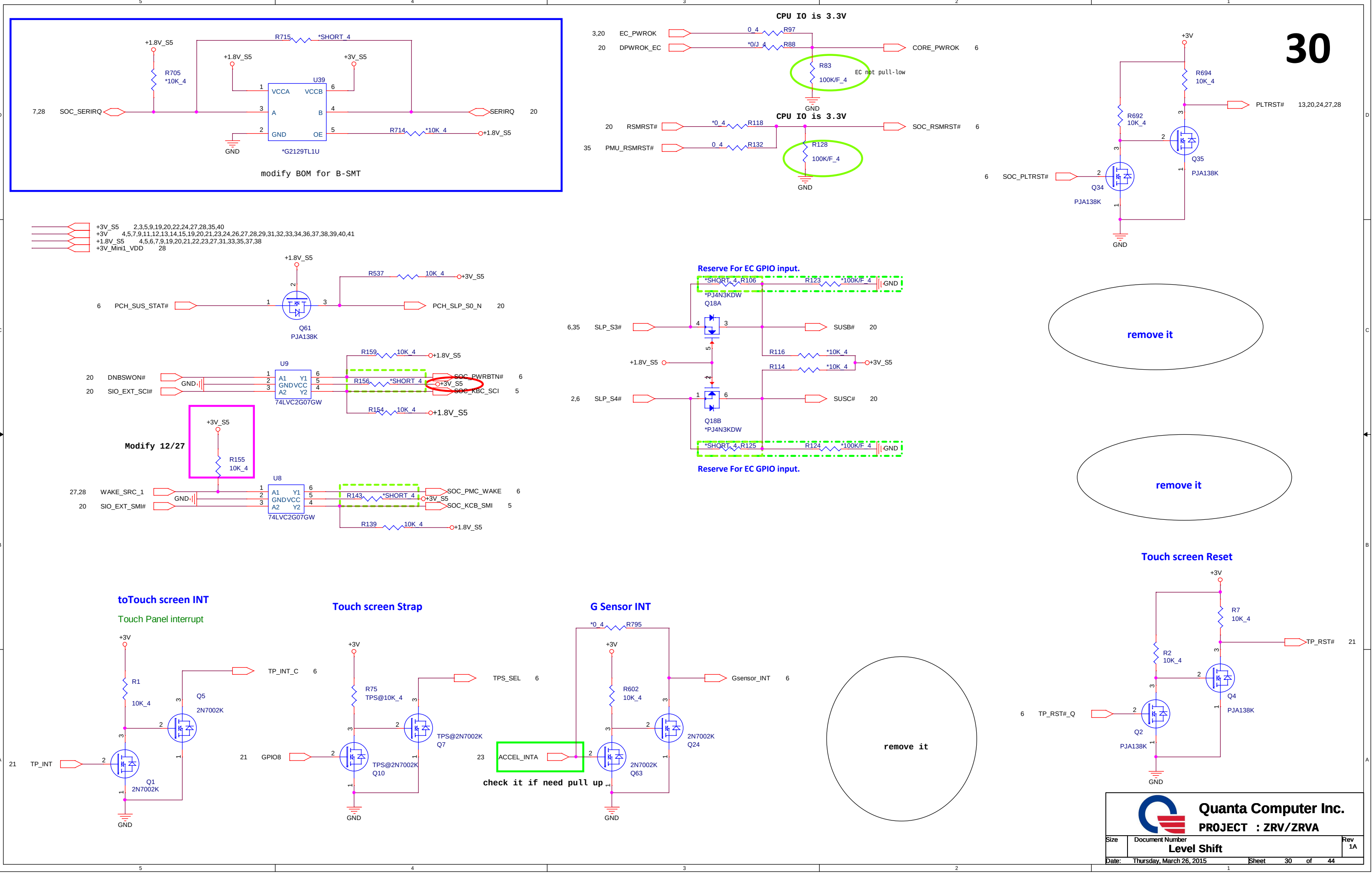
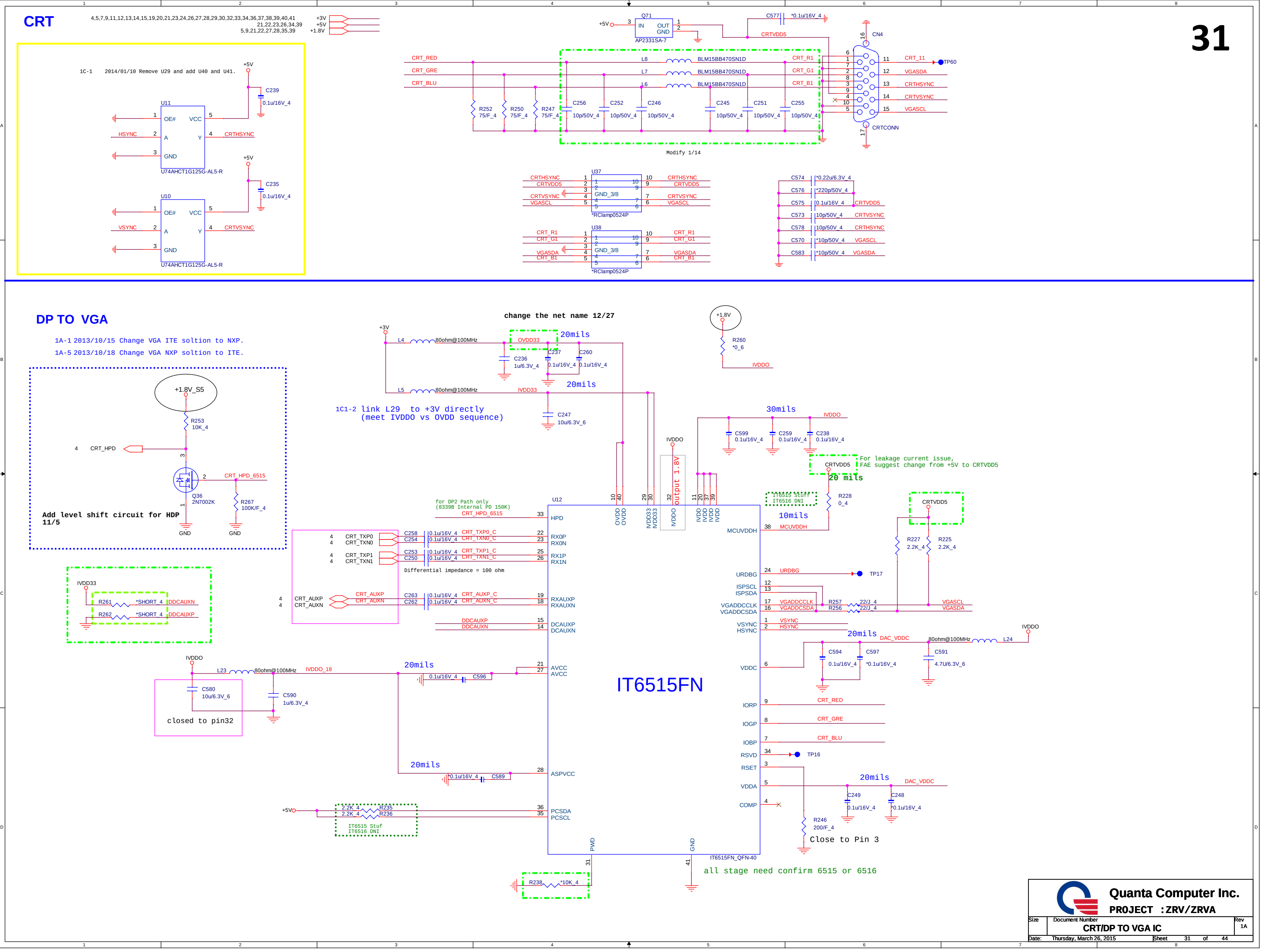


Quanta Computer Inc.

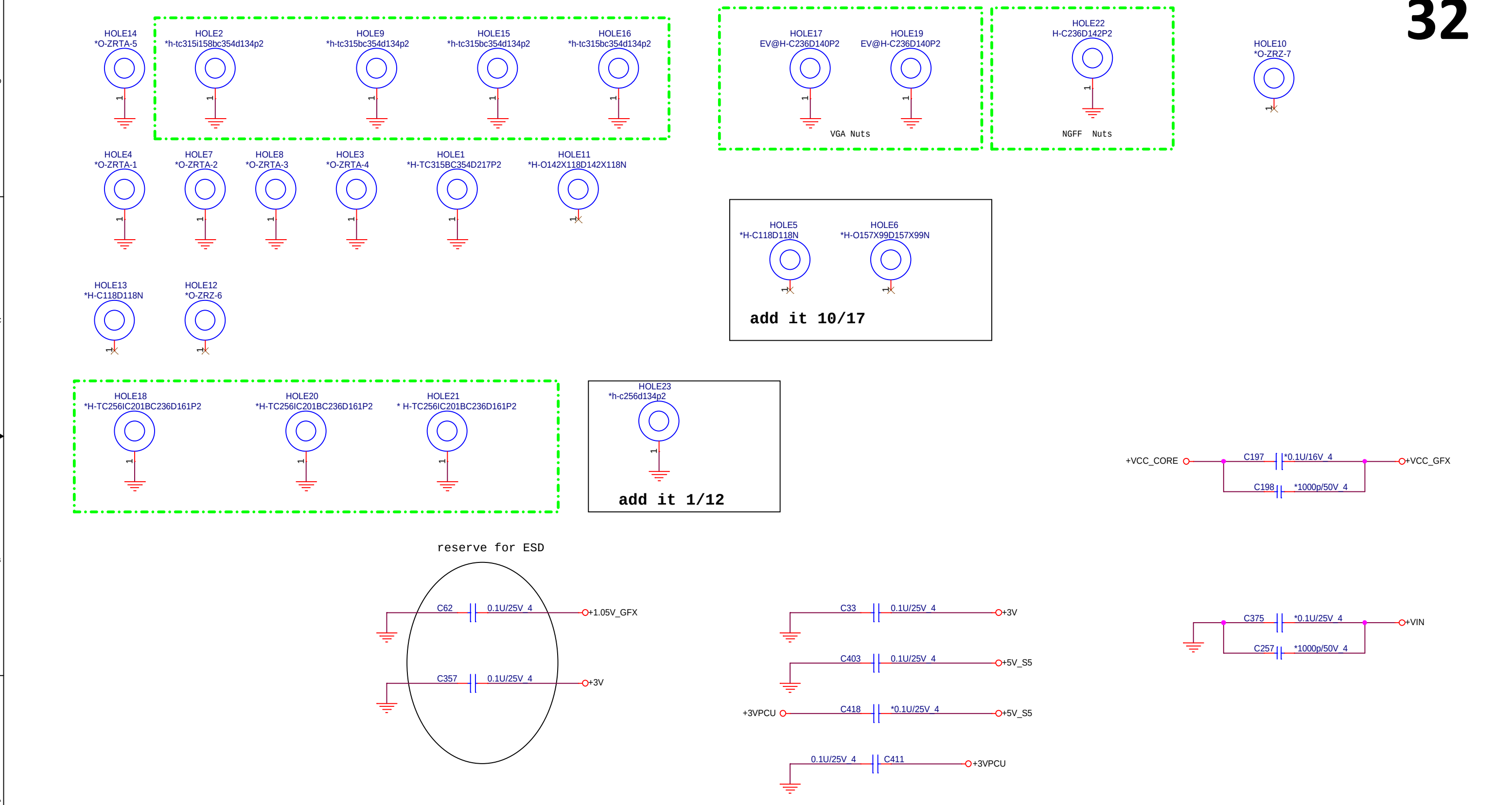
PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Level Shift	1A

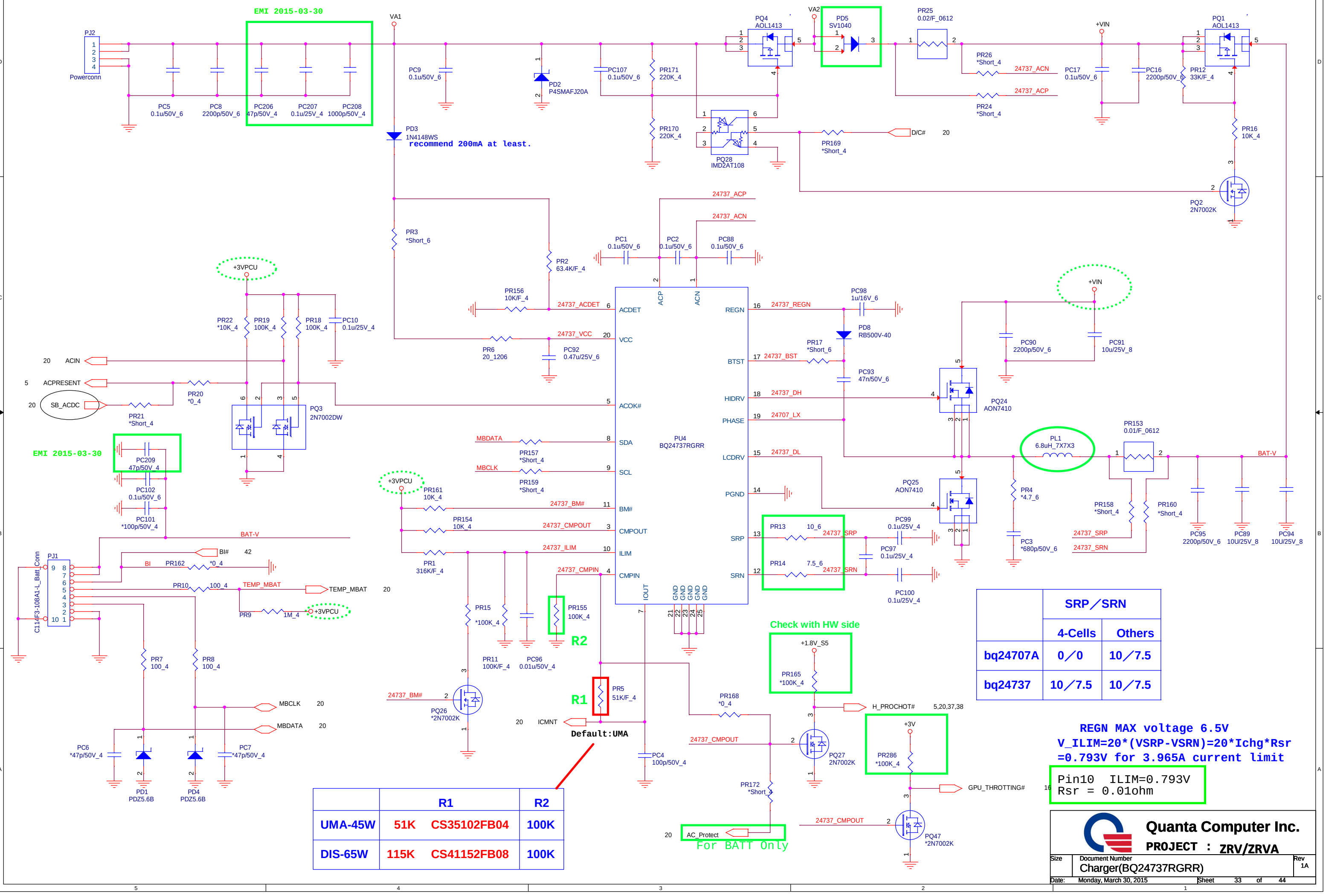
Date: Thursday, March 26, 2015 Sheet 30 of 44


CRT
1C-1 2014/01/10 Remove U29 and add U40 and U41.
U74AHCT1G125G-AL5-R
HSYNC
CRTHSYNC
VSYNC
CRTVSYNC
CRT_RED
CRT_GRE
CRT_BLU
BLM15BB470SN1D
Modify 1/14
AP2331SA-7
CRTVDD5
CRTCONN
*RClamp0524P
DP TO VGA
1A-1 2013/10/15 Change VGA ITE soltion to NXP.
1A-5 2013/10/18 Change VGA NXP soltion to ITE.
change the net name 12/27
1C1-2 link L29 to +3V directly
(meet IVDDO vs OVDD sequence)
Add level shift circuit for HDP 11/5
for DP2 Path only
(8339B Internal PD 150K)
Differential impedance = 100 ohm
For leakage current issue,
FAE suggest change from +5V to CRTVDD5
IT6515 Stuf
IT6516 DNI
output 1.8V
IT6515FN
IT6515FN_QFN-40
closed to pin32
Close to Pin 3
all stage need confirm 6515 or 6516
Quanta Computer Inc.
PROJECT :ZRV/ZRVA
CRT/DP TO VGA IC
Thursday, March 26, 2015
Sheet 31 of 44
Rev 1A

HOLE(OTH)



Quanta Computer Inc.		
PROJECT : ZRV/ZRVA		
Size	Document Number: USB BOARD CONN	Rev 1A
Date: Tuesday, March 24, 2015	Sheet 32 of 44	



	R1		R2
UMA-45W	51K	CS35102FB04	100K
DIS-65W	115K	CS41152FB08	100K

	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Charger(BQ24737RGRR)	1A

Date: Monday, March 30, 2015 Sheet 33 of 44

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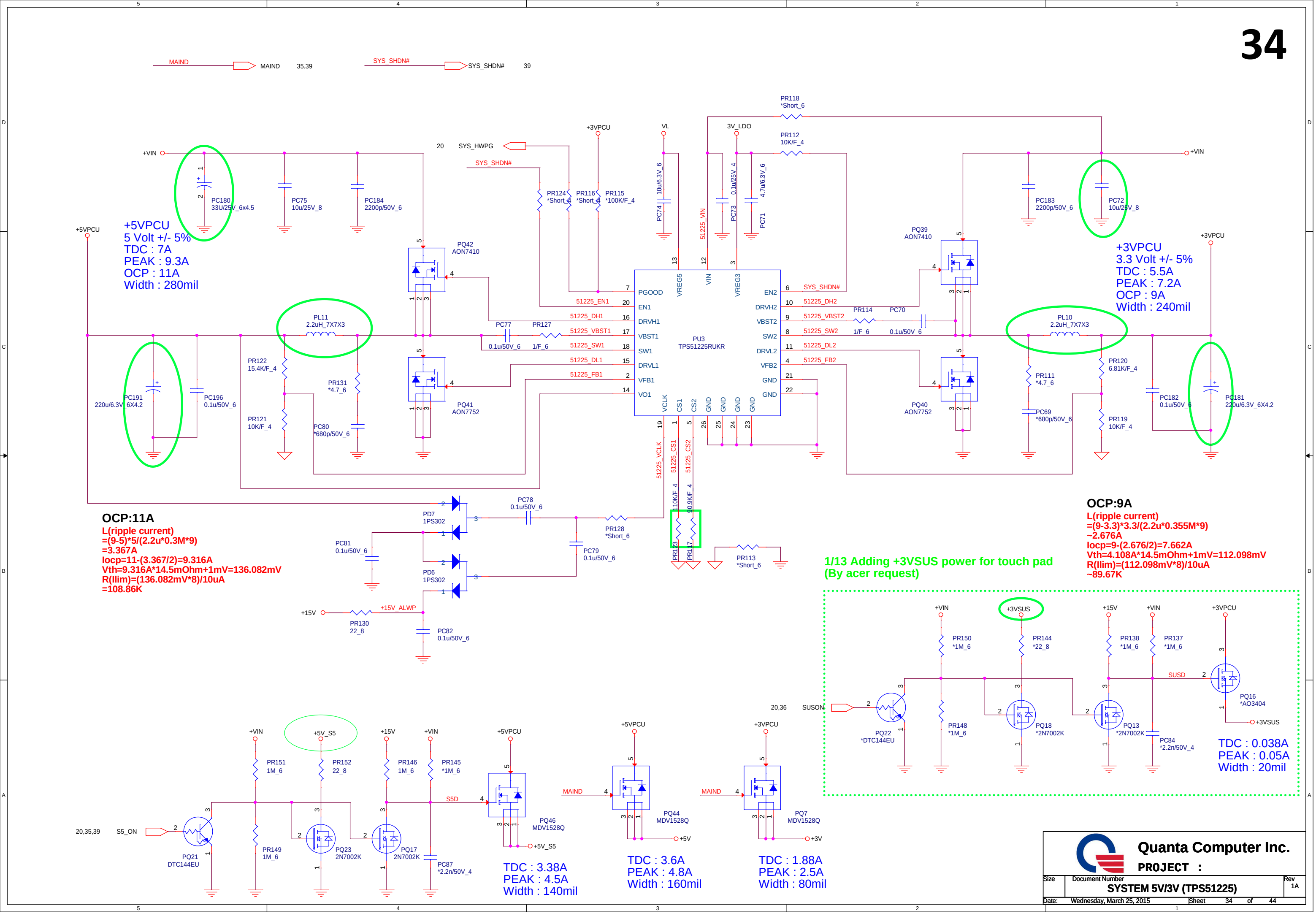
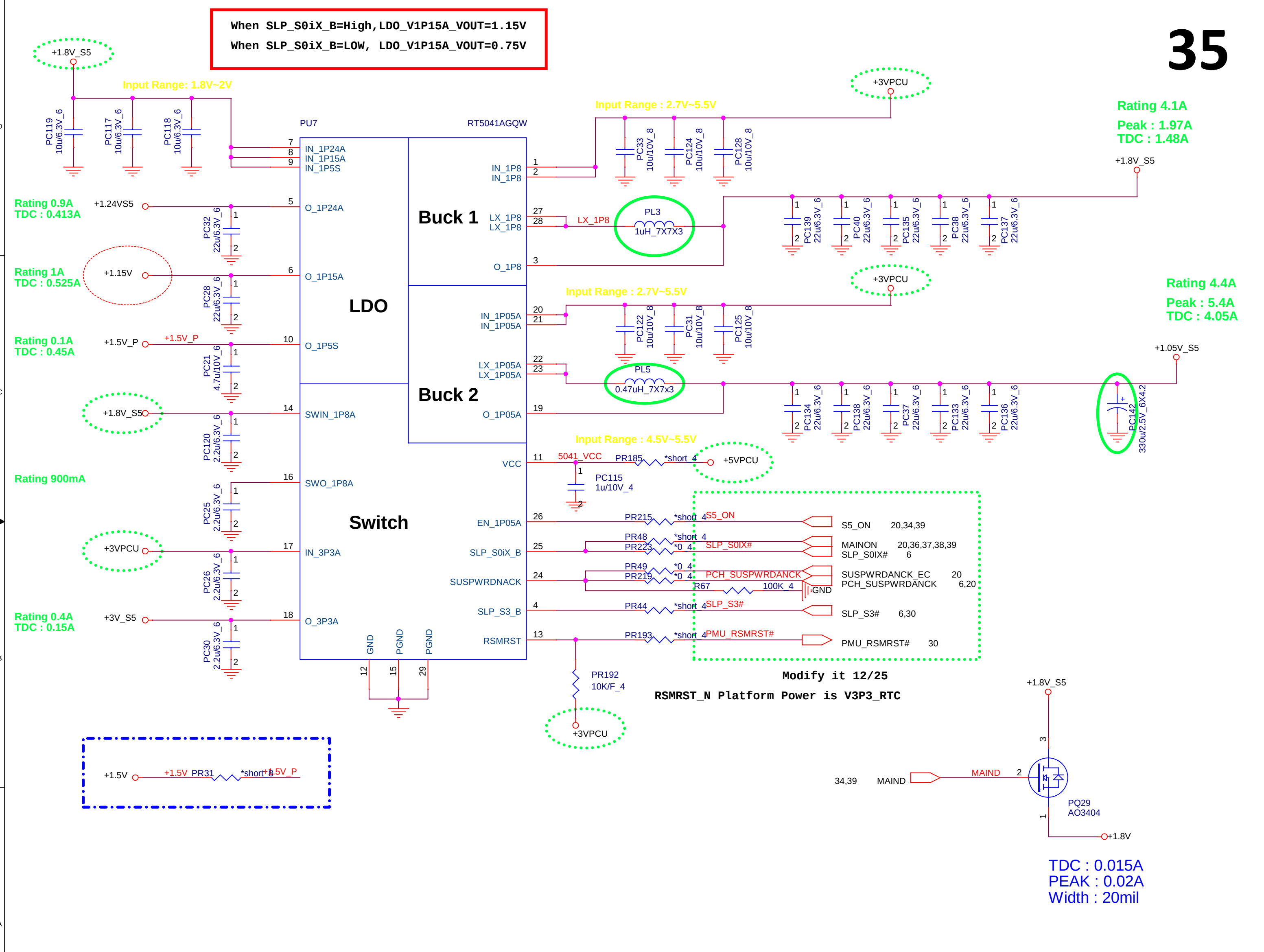

MAIND
SYS_SHDN#
+5VPCU
5 Volt +/- 5%
TDC : 7A
PEAK : 9.3A
OCP : 11A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 5.5A
PEAK : 7.2A
OCP : 9A
Width : 240mil
PU3
TPS51225RUKR
PQ42
AON7410
PQ41
AON7752
PQ39
AON7410
PQ40
AON7752
PL11
2.2uH_7X7X3
PL10
2.2uH_7X7X3
OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14.5mOhm+1mV=136.082mV
R(Ilim)=(136.082mV*8)/10uA
=108.86K
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.662A
Vth=4.108A*14.5mOhm+1mV=112.098mV
R(Ilim)=(112.098mV*8)/10uA
~89.67K
1/13 Adding +3VSUS power for touch pad
(By acer request)
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
TDC : 3.38A
PEAK : 4.5A
Width : 140mil
TDC : 3.6A
PEAK : 4.8A
Width : 160mil
TDC : 1.88A
PEAK : 2.5A
Width : 80mil
Quanta Computer Inc.
PROJECT :
Size
Document Number
Rev
1A
SYSTEM 5V/3V (TPS51225)
Date: Wednesday, March 25, 2015
Sheet 34 of 44

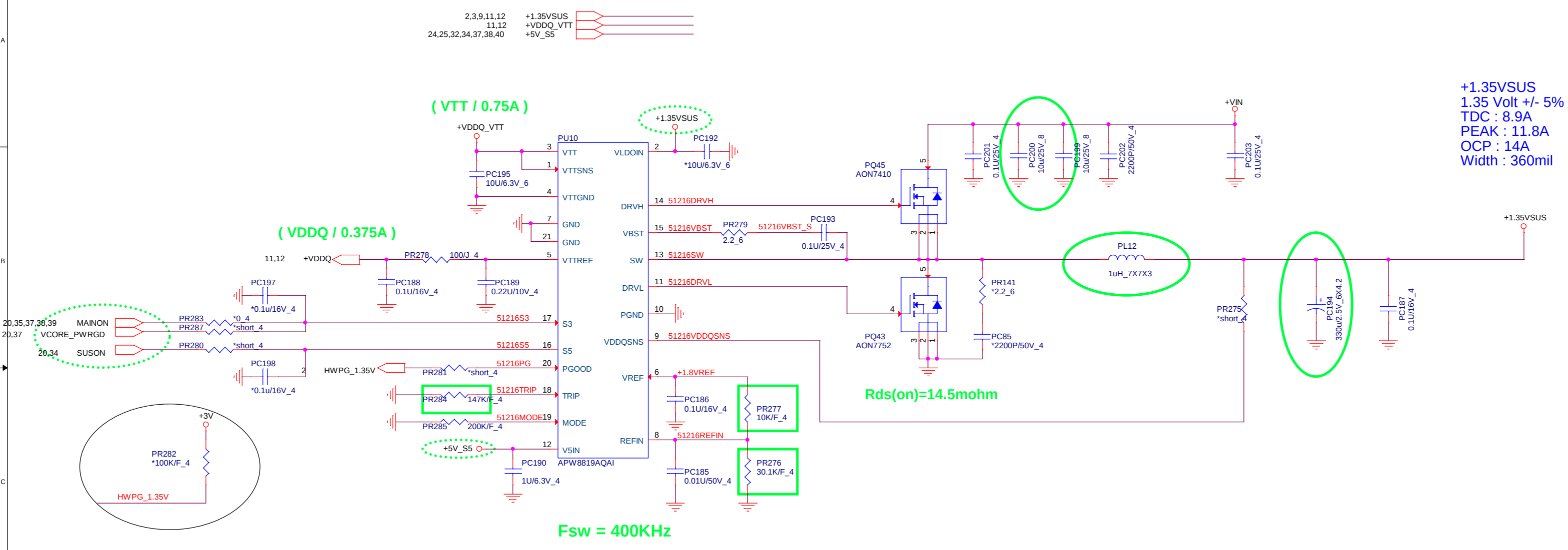


Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
Custom	PMIC (RT5041AGQW)	1A

Date: Tuesday, March 24, 2015 Sheet 35 of 44



OCP=14A
L ripple current
=(19-1.35)*1.35/(1u*400k*19)
=3.135A
Vtrip=14-(3.135/2)*14.5mohm
=180.269mV
Rlimit=180.269mV/10uA*8=144.21Kohm

DDR=1.35V
PR104=10K/F_4
PR106=30.1K/F_4

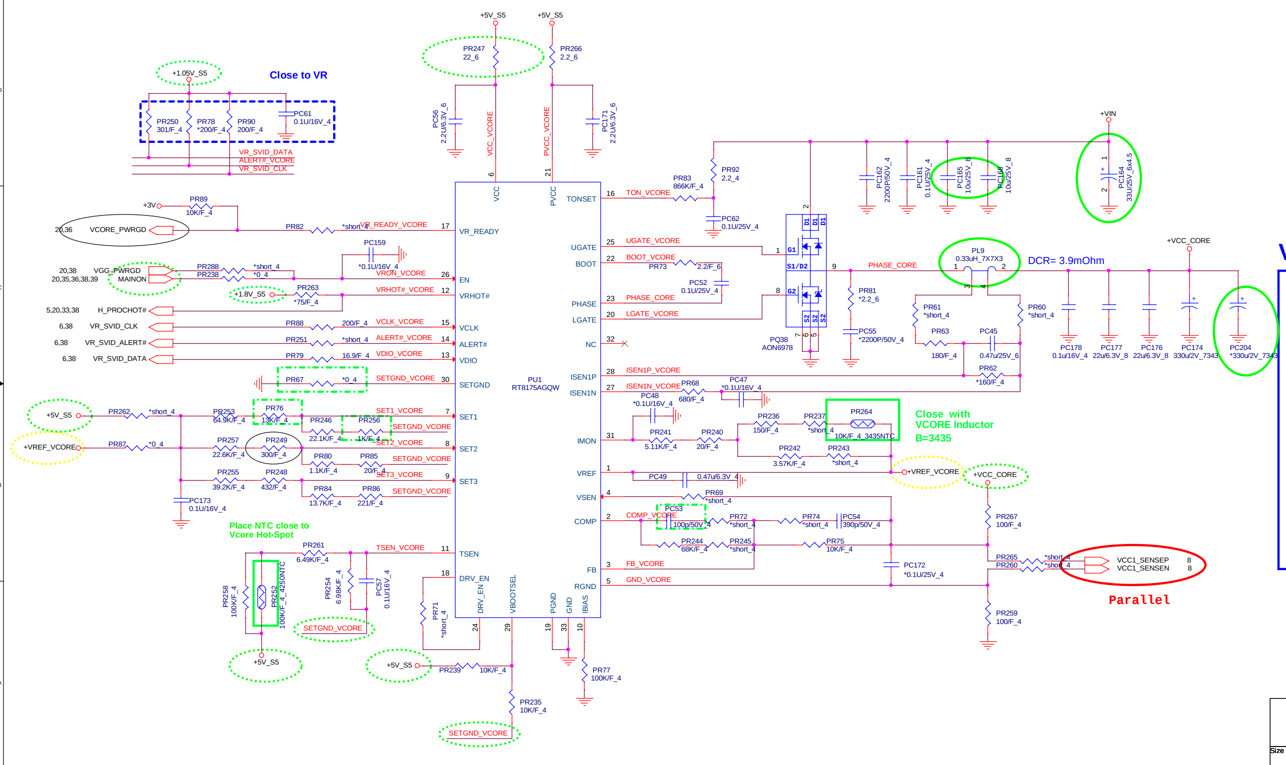
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	DDR3L (APW8819)	1A

Date: Tuesday, March 24, 2015 Sheet 36 of 44



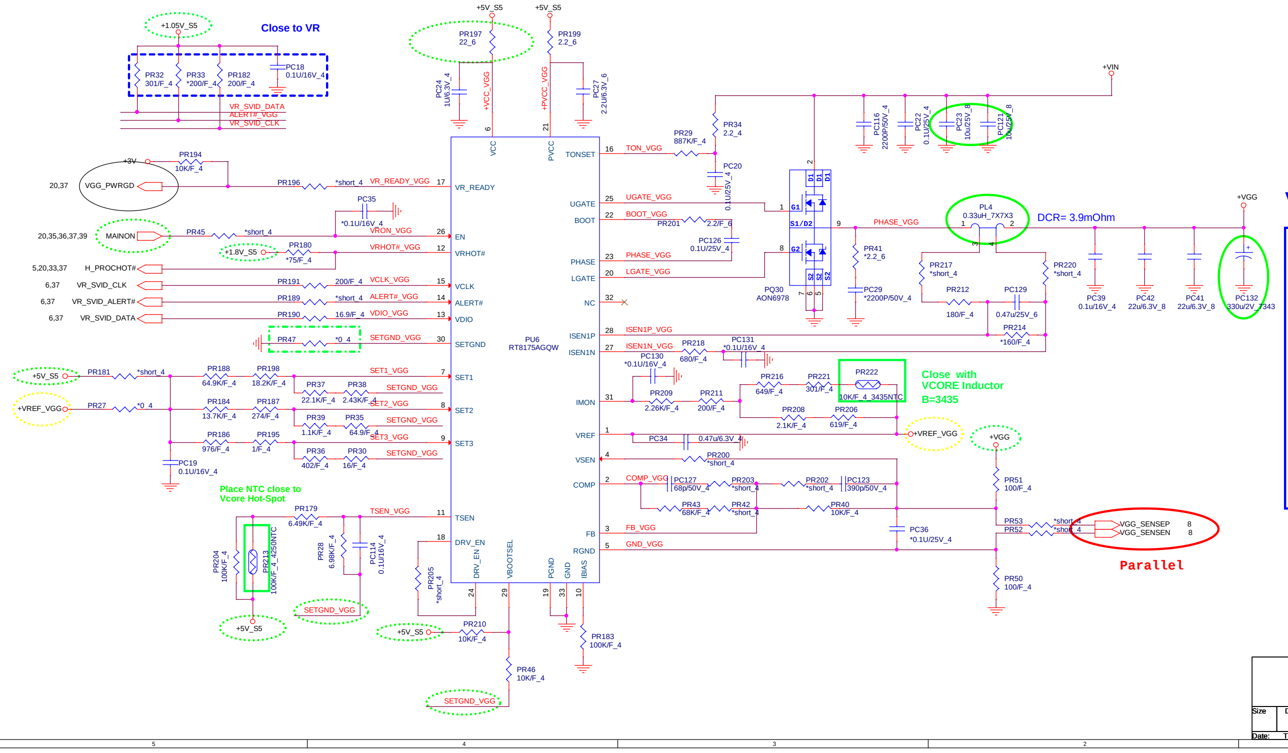
VR 12.1

Braswell - VCC0+1 (1 Phase)

Icc TDC PL2：TBD
Icc Max：7A
OCP：12.4A
Fsw：800KHz
Vboot：1V
VR address：0

VCC0+1 L/L：
R_DC_LL：0 mV/A
R_AC_LL：0 mV/A

Quanta Computer Inc.
PROJECT ：
Size | Document Number | Rev
VCC0+1 (RT8171BGQW) | 1A
Date: Tuesday, March 24, 2015 | Sheet 37 of 44



VR 12.1

Braswell - VGG (1 Phase)

Icc TDC PL2：TBD

Icc Max：15A

OCP：20.7A

Fsw：800KHz

VR Address：5

VCORE L/L：

R_DC_LL：0 mV/A

R_AC_LL：0 mV/A

Quanta Computer Inc.

PROJECT ：

Size	Document Number	Rev
	+VGG (RT8171BGQW)	1A

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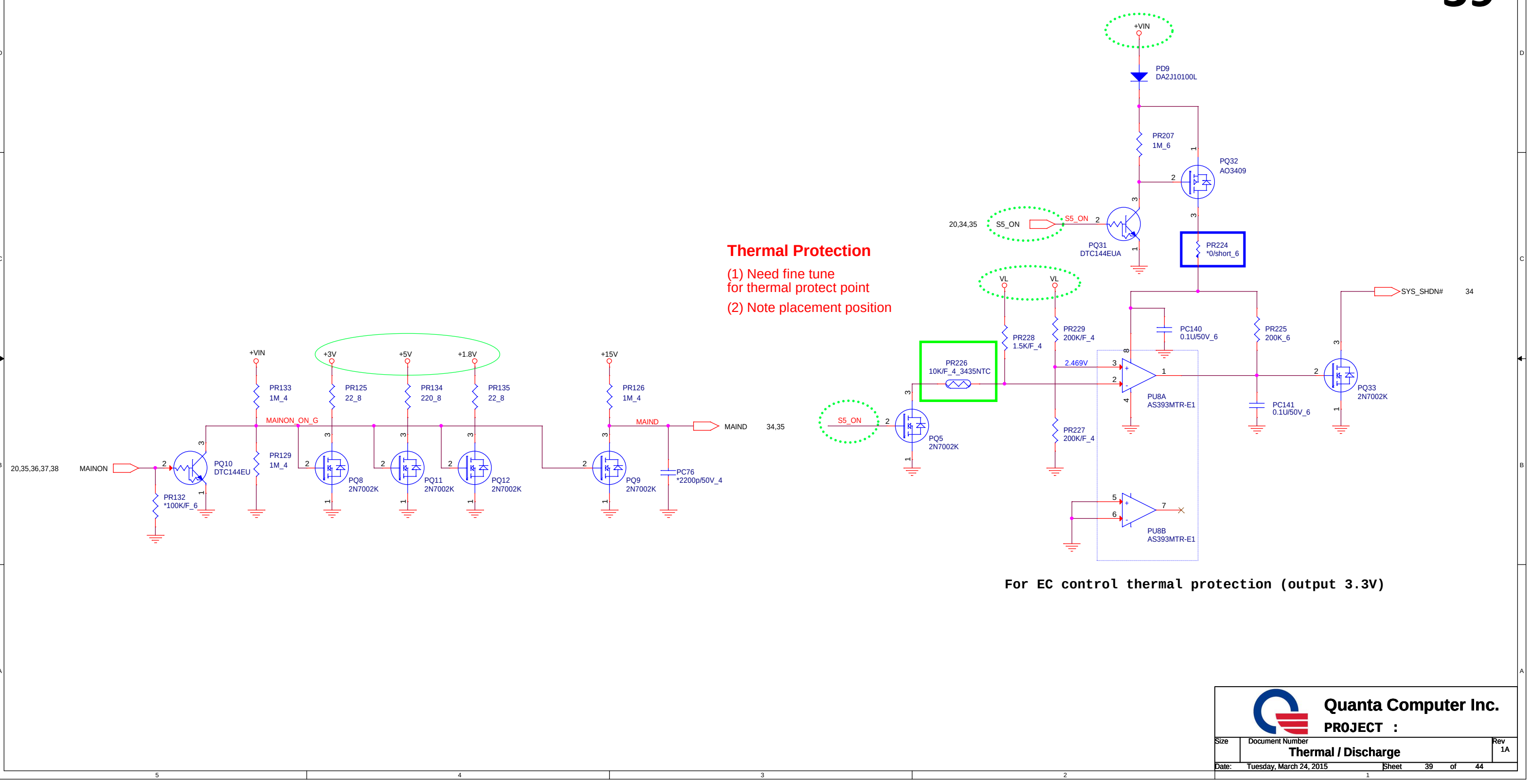
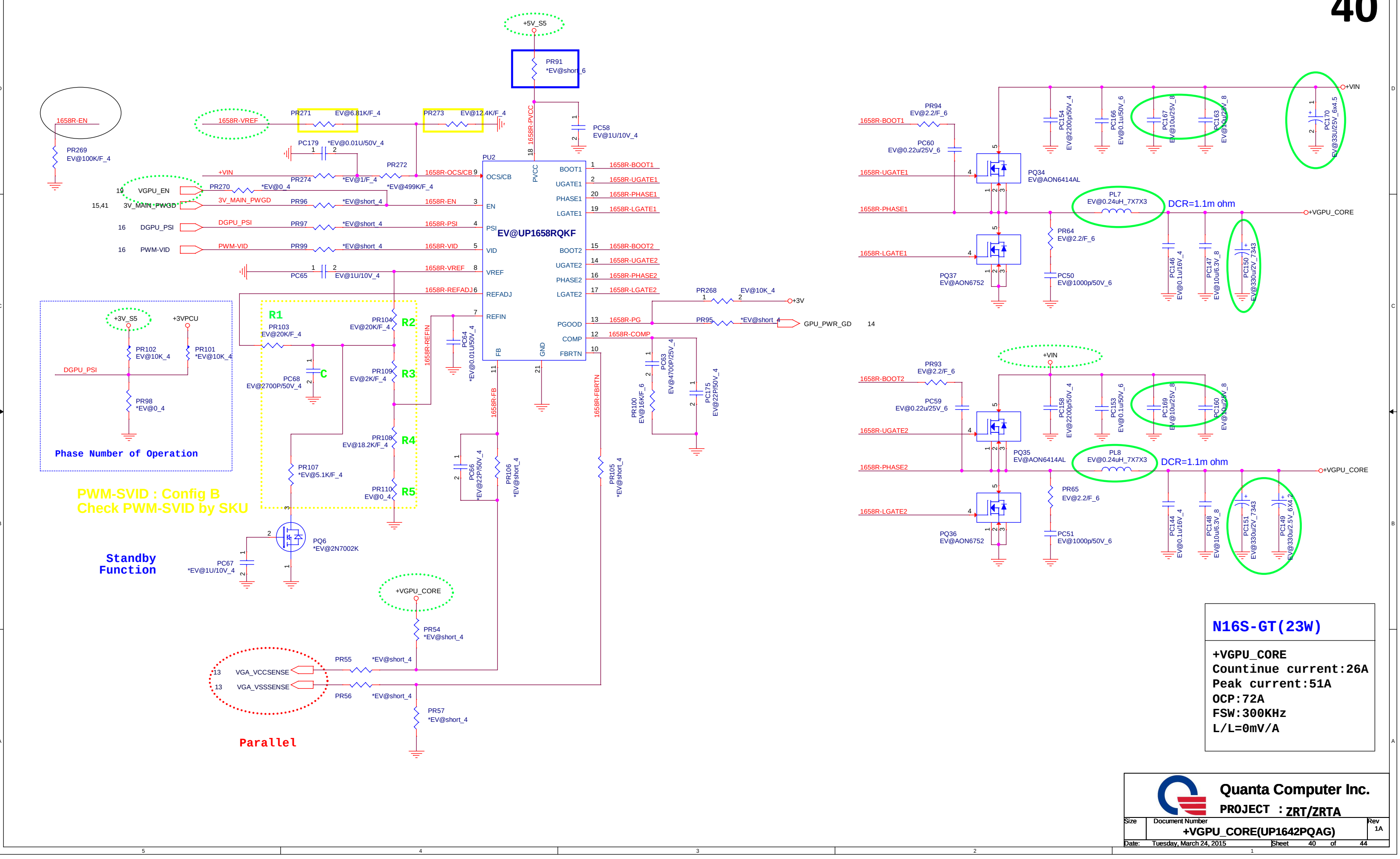


Thermal Protection
(1) Need fine tune
for thermal protect point
(2) Note placement position
For EC control thermal protection (output 3.3V)
+VIN
PD9
DA2J10100L
PR207
1M_6
PQ32
AO3409
20,34,35
S5_ON
PQ31
DTC144EUA
PR224
*0/short_6
VL
PR228
1.5K/F_4
PR229
200K/F_4
PC140
0.1U/50V_6
PR225
200K_6
SYS_SHDN#
34
PR226
10K/F_4_3435NTC
2.469V
PU8A
AS393MTR-E1
PQ33
2N7002K
PC141
0.1U/50V_6
PQ5
2N7002K
PR227
200K/F_4
PU8B
AS393MTR-E1
+3V
+5V
+1.8V
+15V
PR133
1M_4
PR125
22_8
PR134
220_8
PR135
22_8
PR126
1M_4
MAINON_ON_G
MAIND
34,35
20,35,36,37,38
MAINON
PQ10
DTC144EU
PR129
1M_4
PR132
*100K/F_6
PQ8
2N7002K
PQ11
2N7002K
PQ12
2N7002K
PQ9
2N7002K
PC76
*2200p/50V_4
Quanta Computer Inc.
PROJECT :
Size
Document Number
Thermal / Discharge
Rev
1A
Date: Tuesday, March 24, 2015
Sheet 39 of 44



N16S-GT(23W)

+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:72A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	1A

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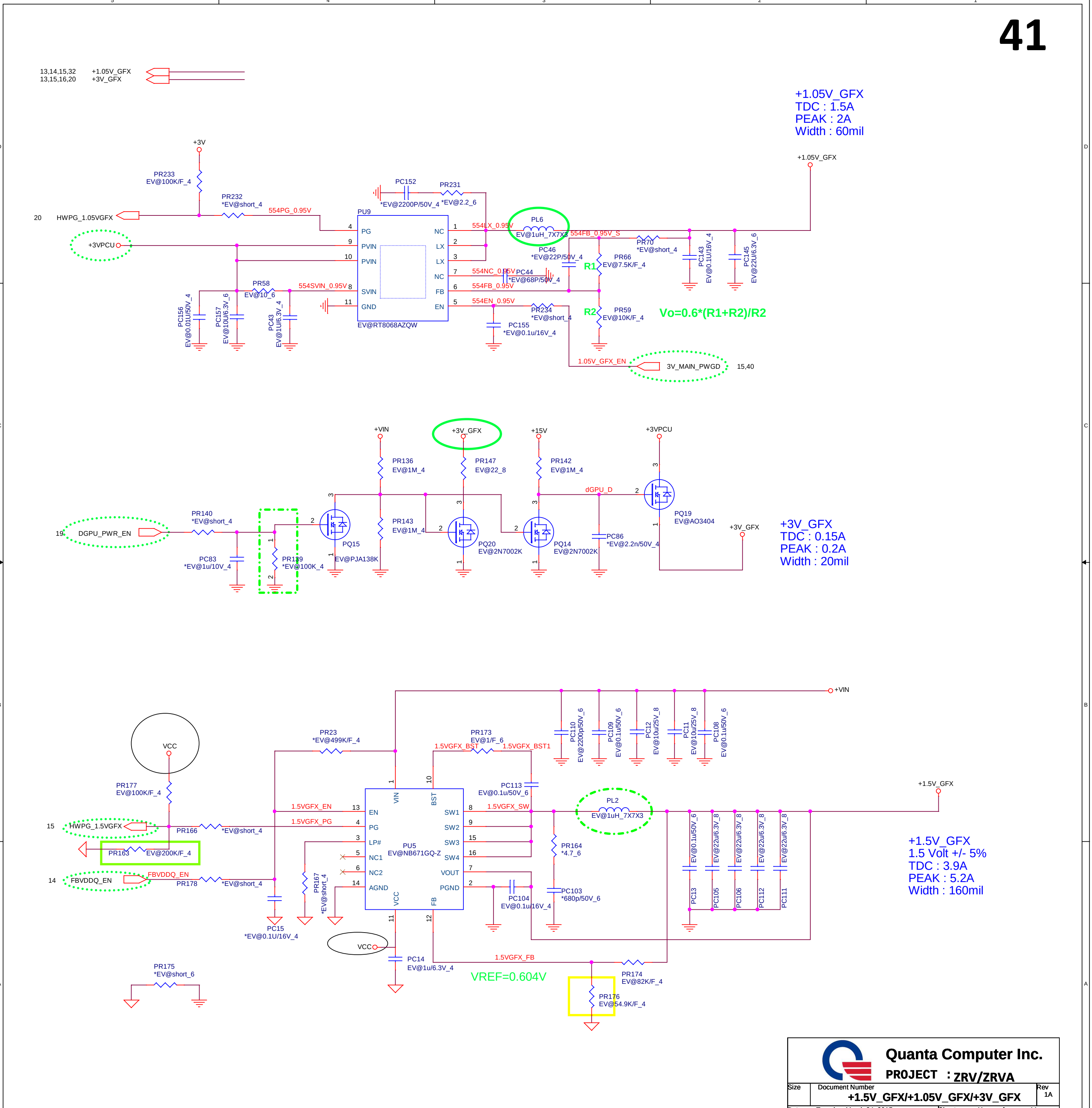

Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX	1A

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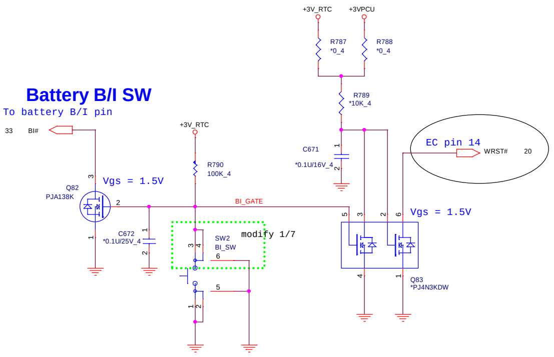
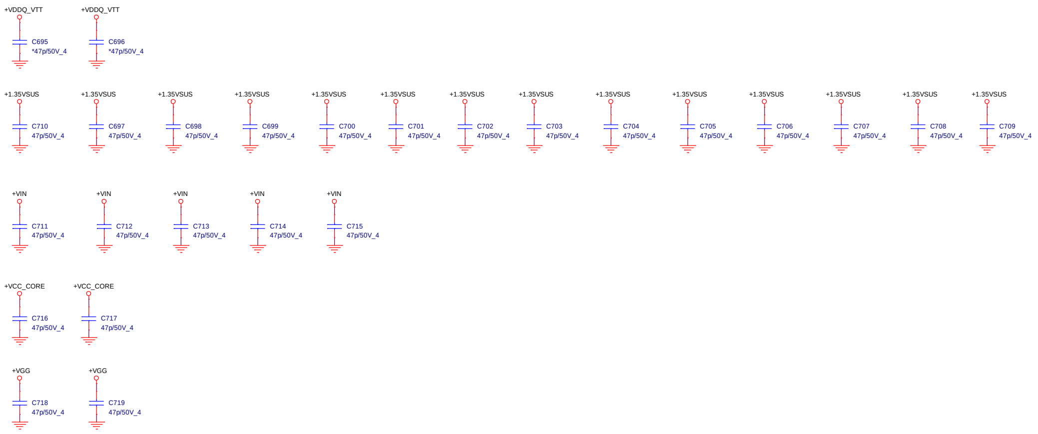
		G3		S0		S3		S4		S5		remark
control pin	power rail	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	
	+3V_RTC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
SYS_SHND#	+3VPCU	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
SYS_SHND#	+5VPCU	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
VGPU_EN	+VGPU_CORE	N	N	Y*	Y*	N	N	N	N	N	N	Y* at 3D enable
DGPU_PWR_EN	+1.05V_GFX	N	N	Y*	Y*	N	N	N	N	N	N	Y* at 3D enable
DGPU_PWR_EN	+1.5V_GFX	N	N	Y*	Y*	N	N	N	N	N	N	Y* at 3D enable
MAINON	+1.8V	N	N	Y	Y	N	N	N	N	N	N	
MAINON	+3V	N	N	Y	Y	N	N	N	N	N	N	
MAINON	+5V	N	N	Y	Y	N	N	N	N	N	N	
MAINON	+VDDQ_VTT	N	N	Y	Y	N	N	N	N	N	N	
MAINON	+VGG	N	N	Y	Y	N	N	N	N	N	N	
VGG_PWRGD	+VCC_CORE	N	N	Y	Y	N	N	N	N	N	N	
SUSON	+1.35VSUS	N	N	Y	Y	Y	Y	N	N	N	N	
SUSON	+3VSUS	N	N	Y	Y	Y	Y	N	N	N	N	
S5_ON	+1.05V_S5	N	N	Y	Y	Y	Y	Y	N*1	Y	N*1	if support WOL , the N*1 will Y
S5_ON	+1.8V_S5	N	N	Y	Y	Y	Y	Y	N*1	Y	N*1	if support WOL , the N*1 will Y
S5_ON	+3V_S5	N	N	Y	Y	Y	Y	Y	N*1	Y	N*1	if support WOL , the N*1 will Y
S5_ON	+5V_S5	N	N	Y	Y	Y	Y	Y	N*1	Y	N*1	if support WOL , the N*1 will Y

Battery B/I SW

To battery B/I pin



EMI 2015-03-30



Quanta Computer Inc.

PROJECT : ZRV/ZRVA

Size	Document Number	Rev
	Battery BI/Power Rail/EMI	1A

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ZRV/ZRVA MB

1 2014/10/14 Swap DDR signal for layuot (page 11/12)
2 2014/10/14 Follow EC pin defined (page 20)

1 2014/10/15 Modify SPI flash circuit (page 5/20)
2 2014/10/15 Modify DDI_VGG_S0 cap follow PDG (page 8)
3 2014/10/15 Modify eDP control circuit follow PDG (page 4)
4 2014/10/15 Change DDR SMBUS circuit for leakage (page 7)
5 2014/10/15 Change PCIE REQ pull up to S5 voltage for EDS (page 5)
6 2014/10/15 Change VGA level shift cirucit for leakage (page 19)
7 2014/10/15 Change TPS and HDMI level shift circuit (page 21)
8 2014/10/15 Change eDP and HDMI HDP circuit (page 21)
9 2014/10/15 Change KB pin defined (page 22)
10 2014/10/15 Change audio REST circuit (page 26)
11 2014/10/15 Change LAN REQ circuit (page 27)
12 2014/10/15 Change Level shift circuit (page 30)
13 2014/10/15 Change CPU footprint to bga1170-intel-braswell-test (page 2-10)
14 2014/10/15 Change LED footprint to ledltst-s326kgjrkt-3p-smt (page 29)
15 2014/10/15 Change Audio connector footprint to lphjk-2sj3080-077111f-6p (page 29)

1 2014/10/16 Recover TPS and HDMI level shifte circuit (page 21)
2 2014/10/16 Change eDP and HDMI HDP circuit (page 21)
3 2014/10/16 Change VGA level shift cirucit for leakage (page 19)
4 2014/10/16 Change LAN REQ circuit (page 27)
5 2014/10/16 Change WLAN REQ and Rest circuit (page 28)
6 2014/10/16 Change EC_Override (GPD7) \SUSPWRDANCK_EC (GPJ4)
\CPUFAN#(GPJ5, pin 81) to FAN2_DAC(GPJ3, pin 7\TS_EN (GPA6, pin32) to GPJ5(pin 81)9 (page 20)
7 2014/10/16 Del error net and correct the circuit (page 31)

1 2014/10/17 Modify DMIC circuit (page 26)
2 2014/10/17 Modify SVID CLK/DATA/Alert cirucit (page 6/37/38)
3 2014/10/17 Modify H_PROCHOT#t circuit (page 5/20/33/37/38)
4 2014/10/17 Add WLAN IOAC power cirucit and swap PICE signal (page 28)
5 2014/10/17 Add WLAN IOAC power cirucit (page 28)

1 2014/10/21 change level shift circuit for leakage (page 30)
2 2014/10/21 SWAP KB nets (page 22)
3 2014/10/21 SWAP DRAM DQ nets (page 11/12)
4 2014/10/21 SWAP VRAM DQ nets (page 17/18)
5 2014/10/21 add a pull up at PCH_ODD_EN and correct Gsensor_INT net name (page 6)
6 2014/10/21 Revese CN15(touch pad) pin define (page 22)
7 2014/10/21 Change CN3 (KB backlight)footprint (page 22)

1 2014/10/22 Change SOC_SERIRQ pull up to +1.8V_S5 (page 30)
2 2014/10/22 change HWPG_1.35V to HWPG_1.5VGFX (page 15)
3 2014/10/22 Add SOC_DRAM_PWROK circuit (page 2)
4 2014/10/22 change PR224/PR212/PR192/PR157/PR143 GND to SETGND_VCORE (page 37)
5 2014/10/22 change PR11/PR19/PR45/PR38/PR30 GND to SETGND_VCORE (page 38)
6 2014/10/22 change PR1004 to 57.6K for 45W ADP (page 33)
7 2014/10/22 Add resistors Pin76/83/100/109/99/32/98/96/117/97/69/95/4/94/2 for IT8887 (page 20)

1 2014/10/23 Change R206/R210/R207/R211 value to 2.2 ohm follow vender request(page 8)
2 2014/10/23 Exchange GPI2 (#68) -> GPD0 (#18) and Exchange GPG2 (#77) -> GPB1 (#109) for IT8887 (page 20)

1 2014/10/24 Delete R4099 (page 6)
2 2014/10/24 Modify EC pin 106 power for SPI power (page 20)

1 2014/10/28 Change S5_ON(pin100) to TP3154(pin77) and pull up pin 100 (page 20)
2 2014/10/28 Change HOLE2 footprint to H-C256I201D161P2 and HOLE15 footprint to H-TC315I158BC354D118P2 (page 32)
3 2014/10/28 Change RP146 to 866k, PR161/PR42 to 64.9K,PR241/PR46 to 18.2K,PR223/PR36 to 22.1K,PR224/PR11 to 2.43K
,PR7 to887K (page 37/38)

1 2014/10/28 Change CN17 footprint(page 26)
2 2014/10/28 update Y3 to correct part number (page 6)

1 2014/10/29 update Hardware strap by EDS v1.01 (page 4/6)
2 2014/10/29 add R4139/R4140 follow CRB v1.0 (page 7)
3 2014/10/29 add R4141 for Audio IO power +1.5V and Change VSDIO to S0 power rails by EDS v1.0 (page 9)
4 2014/10/29 add R4145/R4146/R4147/R4148 follow CRB v1.0 (page 4)

1 2014/10/30 update IC part number ,ROM/USB PW SW/CRT Buffer/LAN/Audio Codec/EC /USB HUB /EDP PW SW(page All)

1 2014/10/31 update connetor part number and footprint(page All)
2 2014/10/31 change holl 11 footprint to H-C236D142P2 (page 32)
3 2014/10/31 update N16x strap table and default to N16V-GM (page 16)
4 2014/10/31 BOM update R62 change to 10K,C638 change to 1uF,R638/R637/R646/R648 unstuff (page 24)
5 2014/10/31 Add PR1201 (page 41)
6 2014/10/31 Connect CLKRUN# to EC (page 20)

1 2014/11/3 CN1.16/CN1.17 disconnect to GND (page 29)
2 2014/11/3 Change CN16 P/N to DFFC10FR123 (page 24)
3 2014/11/3 Change CN13 P/N to DFFC10FR102 (page 23)

1 2014/11/4 Add D1001/D1002 and change the power rail to +3V (page 7)
2 2014/11/4 correct +3.3V_S5 to +3V_S5 (page 30)
3 2014/11/4 R3961 and R3962 nustuff (page 6)
4 2014/11/4 Change PR246 to 10K ohm and add R1202/1203 to control PMIC by EC (page 35)
5 2014/11/4 Remove Level shift circuit about SUSPWRDANCK (page 30)
6 2014/11/4 Pin 80 connect SUSPWRDANCK_EC,Pin 94 connect PCH_SUSPWRDANCK ,Pin 95 connect USB_CHRGE_ON (page 20)
7 2014/11/4 Change USB Charger Mode contorl cirucit by EC (page 25)
8 2014/11/4 Add R4153/R4154 (RCOMP) follow checklist v1.0 (page 4)
9 2014/11/4 Reserve GPIO_SUS7/GPIO_SUS10 follow checklist v1.0 (page 6)
10 2014/11/4 change R540 value to 20K ohm (page 5)
11 2014/11/4 DDR VREF circuit unstuff for DDR3L (page 2/3)

1 2014/11/5 Change R71 value to 100K ohm (page 6)
2 2014/11/5 Modify DGPU_PWROK/FB_CLAMP_REQ# level shift circuit (page 19)
3 2014/11/5 Change BOM about VRAM to EVG@ for N16S-GT/GC6 2.0 (page 18)
4 2014/11/5 update N16x information (page 16)
5 2014/11/5 Reserve pull up R4162 (page 16)
6 2014/11/5 RSMRST_N Platform Power is +3VPCU (page 35)
7 2014/11/5 change Series Termination of FST_SPI_CLK/FST_SPI_D[3:0]/FST_SPI_CS and PU 100K for SPI_CS (page 5)
8 2014/11/5 Add a level shift circuit about DEVSLP0 (page 5)
9 2014/11/5 Add level shift circuit for HDP and R275/R276 change to 100K (page 31)

1 2014/11/6 Add R4169 (page 4)
2 2014/11/6 Add R4170 (page 7)
3 2014/11/6 Add R4171/R4172 (page 21)
4 2014/11/6 un-stuff R230 (page 5)
5 2014/11/6 Correct U31E pin Y7 net name VGPU_EN to VGPU_EN_Q (page 6)
6 2014/11/6 SWAP KB and RP1 nets (page 22)
7 2014/11/6 Remove WAKE_SRC_1 pull up resistor to page 28 (page 30)
8 2014/11/6 rename (page All)

1 2014/11/7 Modify the G_SEN_PW net name to +G_SEN_PW (page 23)

1 2014/11/10 update BOM (page All)
2 2014/11/10 Change U1 P/N to G5243AT11U (page 21)

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Model	REV	CHANGE LIST
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1 2014/12/12 Add BI circuit (page 42)

1 2014/12/15 DGPU throttle path reserved on Comparator Design (page 16)

1 2014/12/23 change Q31B loaction to Q28B for BOM issue (page 2)
2 2014/12/23 change CPU footprint (page 2-10)
3 2014/12/23 Add C673/C674/C675 and add eDP lan3/4 for 4K/2K (page 4)
4 2014/12/23 Move SOC_KCB_SMI to SATA_GP1(pin AG3) ,R661/R411/R421/Q50 unstuff (page 5)
5 2014/12/23 Stuff R668/R628 for cold boot FF issue (page 5)
6 2014/12/23 Del BIOS_STRAP circiut for cost down and change R663 to 3.3K (page 5)
7 2014/12/23 Modify GPIO_SUS5 circuit for can't boot issue and change C541/C537 to 12p (page 6)
8 2014/12/23 R255/R598/R127/R658/R135 unstuff and R151 stuff (page 6)
9 2014/12/25 change G-Senosr to SMBUS and unstuff R135 for intel document (page 7)
10 2014/12/25 change C530 to 330u,C117/C130/C125/C214/C215/C120 and add C676/C677 for VGG (page 8)
11 2014/12/25 unstff R595 for intel document (page 9)
12 2014/12/25 change DDR3 channel B default SA[1:0]:01 (page 12)
13 2014/12/25 change R544 Bom option to EV@ (page 14)
14 2014/12/25 change R31/R32/C32/R521/R518/C499/R61 Bom option to EV@ for GB2B-64 (page 17)
15 2014/12/25 unstuff R690/Q72/Q73 (GC61.0) ,R723/Q40/Q33 and cahnge Q22/Q23/R141 BOM option to EVG@ (page 19)
16 2014/12/25 Exchange TP_POWER_ON and D/C# for battery issue (page 20)
17 2014/12/25 unstuff D9 for DGPU shutdown issue (page 20)
18 2014/12/25 Modify LCD connector circuit for Lans (page 21)
19 2014/12/25 Del CN13 (HDD connector) and modify G-sensor circuit (page 23)
20 2014/12/25 chang C378 to 0.1u and R408 to 22k ohm for PCBEEP issue (page 26)
21 2014/12/25 Modify transformer circuit and footprint for Lan issue, modify CLKREQ pull up power to 1.8V(OD) (page 27)
22 2014/12/25 Modify CLKREQ circuit (page 13)

1 2014/12/27 Add TP70 and TP71 (page 4)
2 2014/12/27 Add R803 for SEC_GPIO_SUS11 and add C683 for CORE_PWOK(page 6)
3 2014/12/27 Modify Q27 to U45 circuit for leakage (page 7)
4 2014/12/27 change R5 and R308pull up to +1.8V_S5 (page 21)
5 2014/12/27 modify CN5 pin defined (page 22)
6 2014/12/27 Remove the CPU thermal sensor circuit (page 23)
7 2014/12/27 Change R481/R484 62 ohm for vender suggested (page 26)
8 2014/12/27 Update LANVCC BOM option (page 27)
9 2014/12/27 R498/R496 change to 80.6 ohm(blue) and R497/R495 change to 150 ohm (amber) (page 29)
10 2014/12/27 Change R469 size from 0603 to 0402 (page 29)
11 2014/12/27 bypass SERIRQ and change R156 pull up +3V_S5 (page 30)
12 2014/12/27 bypass SLP_S3#/SLP_S4# and change R123/R124 value to 100K ohm (page 30)
13 2014/12/27 Remove SLP_S0IX# circuit to EC (page 30)
14 2014/12/27 U12 pin 38/17/16 pull up to CRTVDD5 and unstuff R238 follow ZRZ (page 31)
15 2014/12/27 R261/R262 change to 0 ohm and stuff it follow ZRZ (page 31)
16 2014/12/27 Correct Hole19/Hole17 to VGA Nuts and Hole22 to NGFF Nuts (page 31)
17 2014/12/27 change PR51 to 51K(UMA 45W) and PR5 to 112K(DIS-65W (page 33)
18 2014/12/27 Modify PMIC Power Sequnce (page 35)
19 2014/12/27 change DRAM VTT EN to Vcore power good (page 36)
20 2014/12/27 change Vcore EN to VGG power good (page 37)

1 2014/12/31 stuff R67 to modify PMIC power sequence (page 35)
2 2014/12/31 update parts for EOD (page all)
3 2014/12/31 Correct PR249 to 300 ohm (page 37)
4 2014/12/31 modify CN16 pin defined (page 26)

1 2015/01/06 Reserve HDD Spin-up control for G-senor (page 23)
2 2015/01/06 modify TPM BOM (page 28)

1 2015/01/07 remove SW2 for SYS_SHDN# (page 20)
2 2015/01/07 SW3 change to SW2 and keep SW2 location (page 44)
3 2015/01/07 Add BOARD_ID0 for G-senor(page 6)
4 2015/01/07 update Hynix H5TC4G63CFR-N0C strap (page 16)

1 2015/01/08 JDIM1 footprint change from DDR-DDRSK-20401-TP4B-204P-LDV to DDR-DDRSK-20401-TP4B-204P-SMT for SMT (page 11)
2 2015/01/08 JDIM2 footprint change from DDR-DDRRK-20401-TP5B-204P-RUV to ddr-ds2rk-20401-tp4b-204p-smt for SMT (page 12)
3 2015/01/08 change PU1/PU6 to RT8175 (AL008175004) (page 37/38)
4 2015/01/08 Add ESD/EOS solution for LID#/RF_EN/TP_EN_EC/EC_ODD_EJ#/TP_INT_EC# (page 20)

1 2015/01/09 change CN3 part number to DFFC04FR016 for connector list (page 22)
2 2015/01/09 change CN16 footprint 50224-00401-001-4p-l for connector list (page 26)
3 2015/01/09 change CN1 footprint sdcard-psdat4-11glbs1nn4h4-11pfor connector list (page 29)
4 2015/01/09 unstuff PR67/PR47 for S5 leakage (page 37/38)
5 2015/01/09 Add C691/C692 and change C224/C223/C193/C192/C188/C189 to 22u for power issue (page 8)

1 2015/01/12 change Hole18/20/21/9/15/16/2 footprint and add Hole 23 for DXF (page 32)
2 2015/01/12 change PR247 to 22 ohm,PR76 to 13K ohm,PR256 to 1K ohm and PC53 change to 100p (page 37)
3 2015/01/12 change PR197 to 22 ohm (page 38)
4 2015/01/12 Add PC204 for Vcore (page 37)
5 2015/01/12 Modify Hole 23 connect to GND (page 32)

1 2015/01/13 change PL2 to 1uH for Power (page 41)
2 2015/01/13 Add SSD ID of ODD (page 23)
3 2015/01/13 Board ID2 change for SSD (page 6)

1 2015/01/14 change L16/L18/L20/L22 part number to CX5AG121002 for RDC (page26)
2 2015/01/14 change SSD ID at pin AF3 (SATA_GP3) (page5)
3 2015/01/14 Change C256/C252/C246/C245/C251/C255 to 10p for EMI (page31)
4 2015/01/14 Change speaker connector pin defined 1/14 (page26)

1 2015/01/15 Modify Hole 23 footprint to h-c256d134p2 (page32)
2 2015/01/15 unstuff PR139 (page44)

1 2015/01/21 unstuff Q3 (page21) , R533 (page16) , SW1 (page23), R725 (page27) , PC159 (page37) , U13 C593 R272(page30) , stuff R735 (page27)

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1 2015/02/16 R498/R496 change to 71.5 ohm(blue) and R497/R495 change to 130 ohm (amber) (page 29)
2 2015/02/16 R408 change to 10k ohm for noise issue (page 26)
3 2015/02/16 U18 change Vender from GMT to TI for Usb3.0 issue (page 25)
4 2015/02/16 Unstuff TPN_I net , stuff TPM_N net (page 28)
5 2015/02/16 PL4(page 38) and PL9 (page 37) change Pn from CV+33K0MZ02 to CV+33K0MZ03
6 2015/02/16 Change PU9 from AL008804001 to AL008068000 (page 41)
7 2015/02/16 Change CN4 from DFDS15FR317 to DFDS15FR243 (page 31)

1 2015/02/24 Modify CN18 footprint to 50584-0280n-v01-28p-l (page22)
2 2015/02/24 Modify HOLE 5 footprint to h-o120x112d120x112n (page32)

1 2015/02/25 Modify ODD circuit SATA_DP connect to SATA_LED# (U34D AH3) , remove R251 , Add R813 812 C693 (page23 , page 5)
2 2015/02/25 R815 Change from 4.99K to 45.3K (page16)
3 2015/02/25 PR134 Change from 22 ohm to 220 ohm (page39)

1 2015/03/02 Remove U13 , R265 , C593 , R272 (page30)

1 2015/03/10 Change PQ15 to BAM138K0001 for S3 leakage (page41)

1 2015/03/11 Change to +3V_S5 for LPC leakage (EC pin11) (page20)

1 2015/03/16 ChangeTPM Power from +3V to +3V_S5 for LPC leakage (TPM Power) (page28)
2 2015/03/16 Change R178 , R190 , R177 , R189 from 2.2 ohm to 0 ohm for VCC drop issue (page8)

1 2015/03/24 TPS@ all stuff (page28)
2 2015/03/24 Add capacitance (47p) at +1.8V_S5 (PCIE_CLKREQ2_WLAN#) (page5)
3 2015/03/24 Change 0 ohm to Short Pad and remove JP (page33 to 41)

1 2015/03/25 Stuff RV1~12 and Change RV1~12 from CY402V05B00 to BCPJSD05Z06 (page 25)
2 2015/03/25 Change 0 ohm to Short Pad (page2 to 31)
3 2015/03/25 Change C529 C531 C526 C527 from 0.22u to 0.1u (page13)
4 2015/03/25 Unstuff R201/R197 (page7)

1 2015/03/27 Modify keyboard circuit (conn Pin27) , add R816/C694/D42 (page22)

1 2015/03/30 Add 25pcs capacitance (C695~719) for EMI (page42)
2 2015/03/30 Add 4pcs capacitance (PC206~209) for EMI (page33)

1 2015/04/01 Add 1pcs capacitance (C720) close to SOC for USB loss issue (page7)
2 2015/04/01 Add 12pcs TP (TP76~99) for ESD (page25)
3 2015/04/01 Change R451/R446/R437/R434/R410/R402/R385/R378 from 0 ohm to Short Pad (page25)

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