Commercial DT / M4.1 Chassis System
Project name: vHulk
SCH Ver: -1
PCB Number: 14065-1

PCB BOARD SIZE
4 Layer / 244 mm x 244 mm

Jomper SETTING

CMOS1	1-2 Short	With Jumper to Clear CMOS
WP1	1-2 Short	With Jumper to enable WP
OBR1	1-2 Open	Without Jumper to recovery
MECLR1	1-2 Short	With Jumper to enable ME

BOM Configuration

(R_) : unmount
(E_) : SATA Express
(Q_) : Q170
(B_) : B150
(D_) : VGA
(W_) : For WST/FXC MB
(T_) : TPM on board
(S_) : For ECS MB
(H_) : TPM header

Key IC

CPU1	Intel CPU Skylake S 65W
PCH1	Intel PCH Q170/B150
U7901	ITE SIO IT8733F-DX
U2701	RealTek Audio Codec ALC662-VD
U3	Realtek LAN RTL8111EPV-CG
TPM1	NuvoTon TPM NPCT650AAAWX
U72	INTEL LAN I219LM I219
U54	ITE PCI Bridge IC IT8893E
U6506	Realtek converter RTD2168-CG

Header

SPK1	21.63415.204
AUDF1	21.62895.205
FANC1	21.60626.104
FANS1	21.60626.104
CMOS1	21.61445.103
OBR1	21.60909.102
WP1	21.61445.103
PCHDR1	021.60235.0204
LPT1	021.60217.0213
COM1	21.62884.205
TPMH1	21.62900.210
CSOPN1	21.62874.102
MECLR1	21.61445.103

Power sates

	Name	G3	EUP	S5	S4	S3	S0
+12V	12V_S0 12V_CPU_S0						O
-12V	-12V_S0						O
5V	ATX_5VSB		O	O	O	O	O
	+5V_AUX1 +5V_AUX2 5V_USB20_RJUSB2			O	O	O	O
	5V_USB30P1 5V_USB30P2 5V_USB30H1 5V_USB20P1 5V_USB20_RJUSB1 5V_USB20H2 5V_USB20H1 5V_USB30H2				O	O	O
	5V_S0 5V_DVI						O
3.3V	ATX_3.3VSB 3P3V_LAN		O	O	O	O	O
	3P3V_S5 3D3V_VCCPGPPA_Sx 3D3V_1D8V_PCHSPI_Sx 3D3V_DVDDIO_AUDIO DVDD_IO			O	O	O	O
	3D3V_S0 3D3V_RTD2168						O
3.0V	3V_VBAT1_G3 3V_VRTC_G3 3D3V_VCCPRTC	O	O	O	O	O	O
2.5V	2D5V_VPP				O	O	O
1.2V	VDDQ				O	O	O
DIMM	DDR_VTT					O	O
PCH	1D0V_S5 1V_VCCF24_Sx 1V_VCCAMPHYPLL_Sx 1V_VCCAPLL_Sx			O	O	O	O
CPU	VCC_CORE GFX_CORE VCC_SA VCC_IO						O
	1V_VCCST_VCCPLL_S3					O	O

<Core Design>

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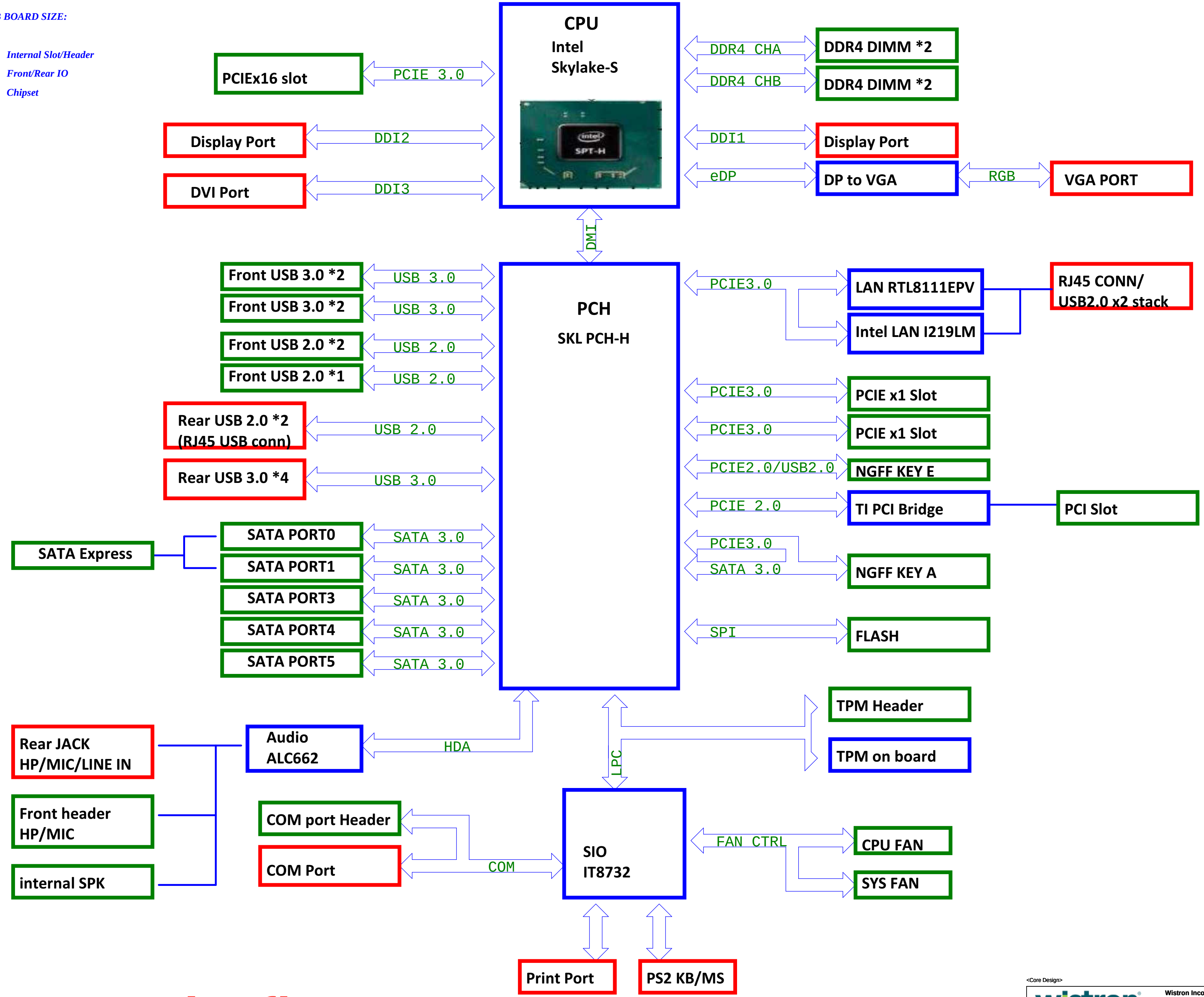
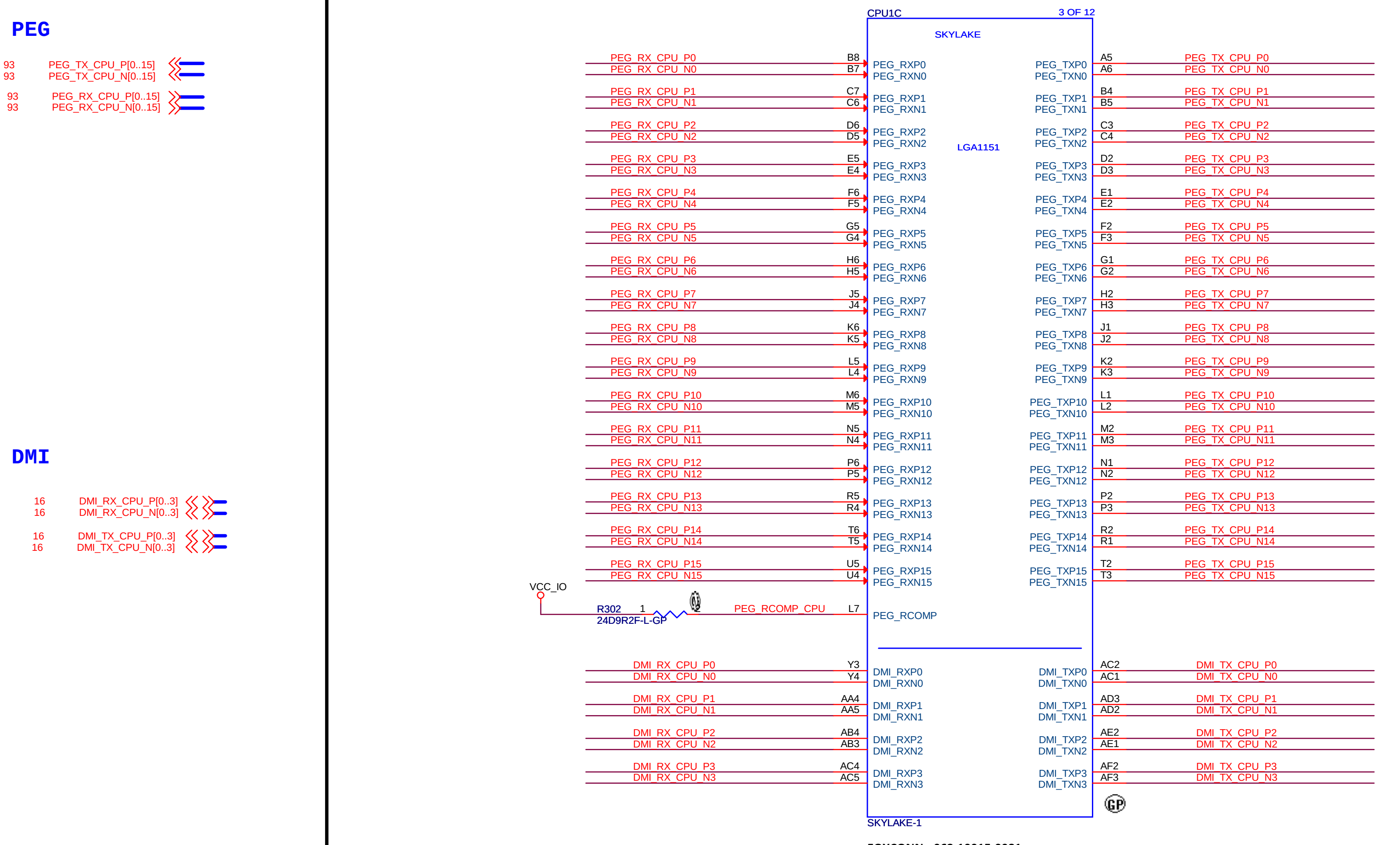
Title	COVER PAGE	
Size C	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 1 of 107	

PROJECT NAME: vHULK
MB VERSION: -1

PCB BOARD SIZE:

- *Internal Slot/Header*
- *Front/Rear IO*
- *Chipset*





FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

<Core Design>

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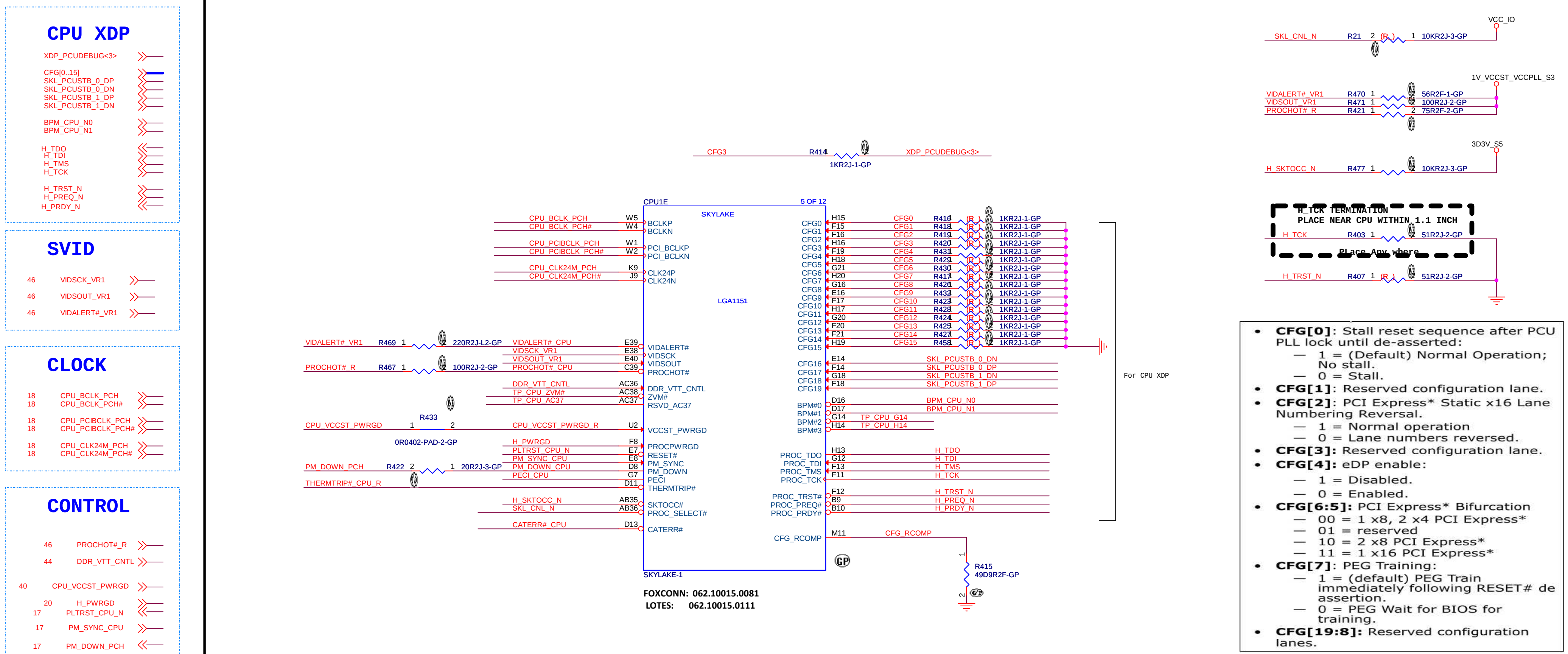
Title: CPU(PCIE/DMI)

Size	Document Number	Rev
Custom	vHulk	-1

Date: Wednesday, September 23, 2015 | Sheet 3 of 107



- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

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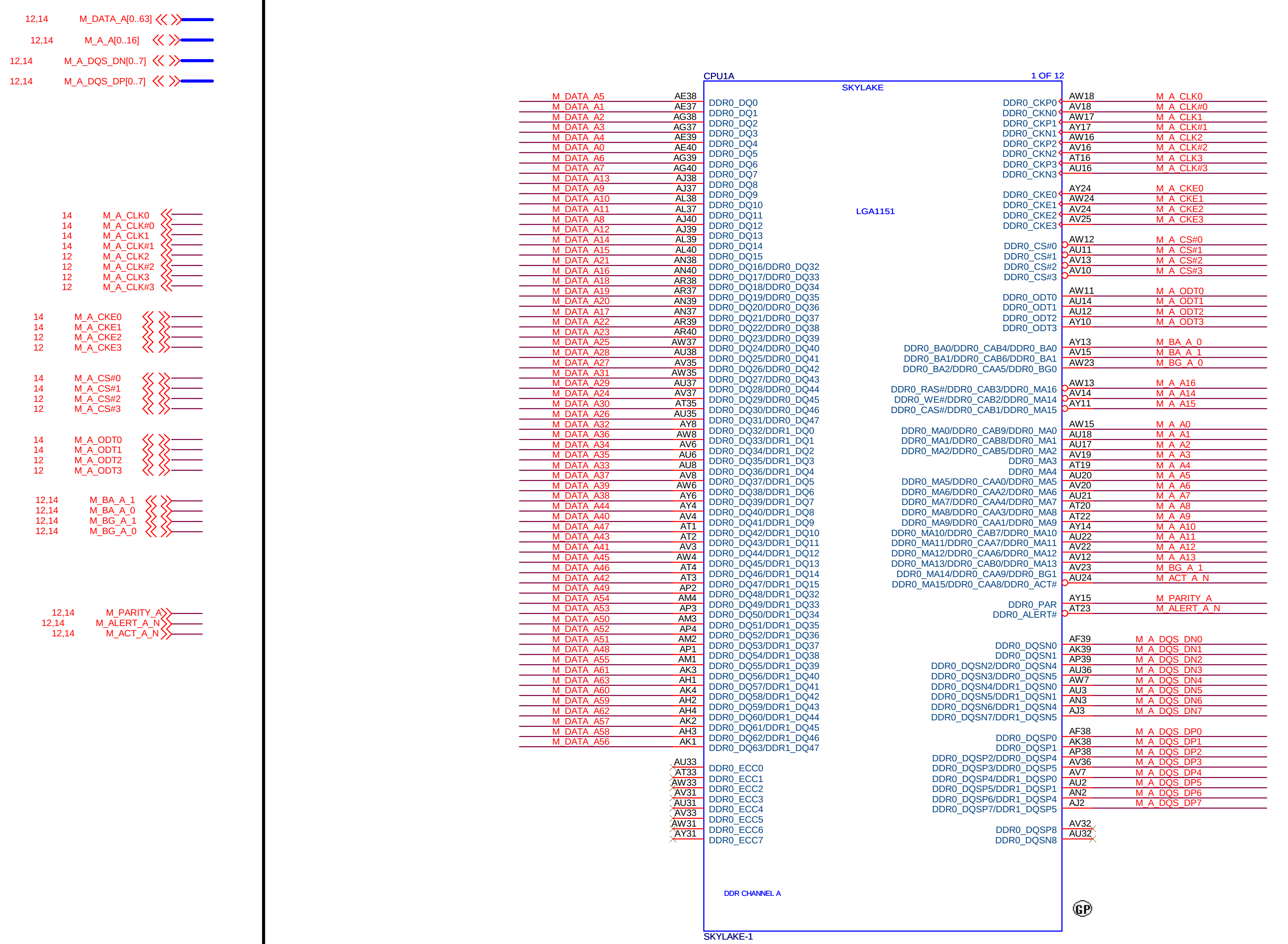
Title: CPU_(THERMAL/CLOCK/PM/CFG)

Size	Document Number	Rev
Custom	vHulk	-1

Date: Wednesday, September 23, 2015 | Sheet 4 of 107



FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

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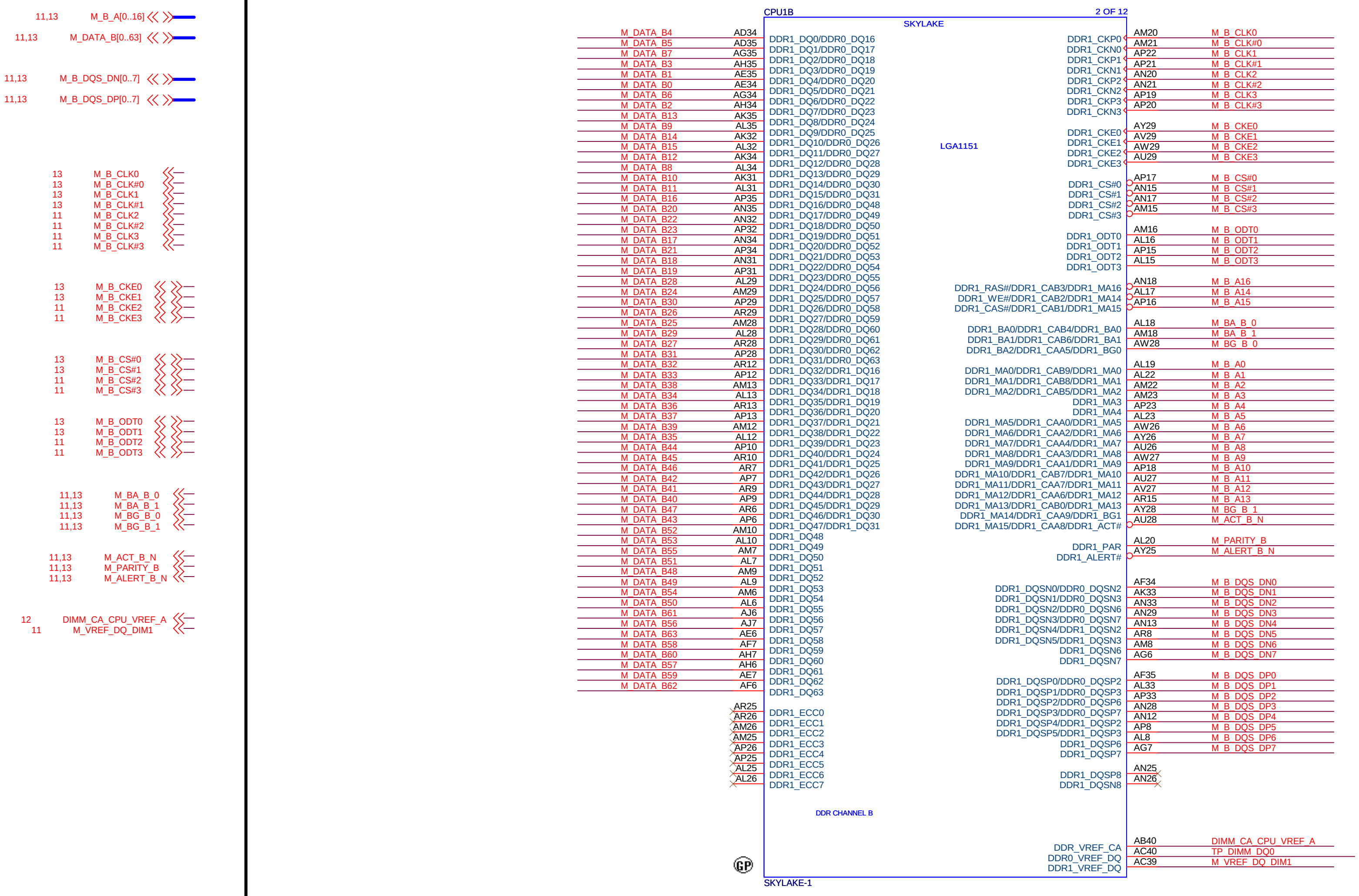
Title	CPU_(DDR_CHA)	
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 5 of 107	



FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

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Title	CPU (DDR_CHB)	
Size Custom	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 6 of 107	

57 DP_DATA_CPU_P0
57 DP_DATA_CPU_N0
57 DP_DATA_CPU_P1
57 DP_DATA_CPU_N1
57 DP_DATA_CPU_P2
57 DP_DATA_CPU_N2
57 DP_DATA_CPU_P3
57 DP_DATA_CPU_N3

57 DP_AUX_CPU_P
57 DP_AUX_CPU_N

56 DP2_DATA_CPU_P0
56 DP2_DATA_CPU_N0
56 DP2_DATA_CPU_P1
56 DP2_DATA_CPU_N1
56 DP2_DATA_CPU_P2
56 DP2_DATA_CPU_N2
56 DP2_DATA_CPU_P3
56 DP2_DATA_CPU_N3

56 DP2_AUX_CPU_P
56 DP2_AUX_CPU_N

55 DVI_DATA_CPU_P0
55 DVI_DATA_CPU_N0
55 DVI_DATA_CPU_P1
55 DVI_DATA_CPU_N1
55 DVI_DATA_CPU_P2
55 DVI_DATA_CPU_N2
55 DVI_DATA_CPU_P3
55 DVI_DATA_CPU_N3

58 DDI_VGA_DATA_CPU_N0
58 DDI_VGA_DATA_CPU_P0
58 DDI_VGA_DATA_CPU_N1
58 DDI_VGA_DATA_CPU_P1

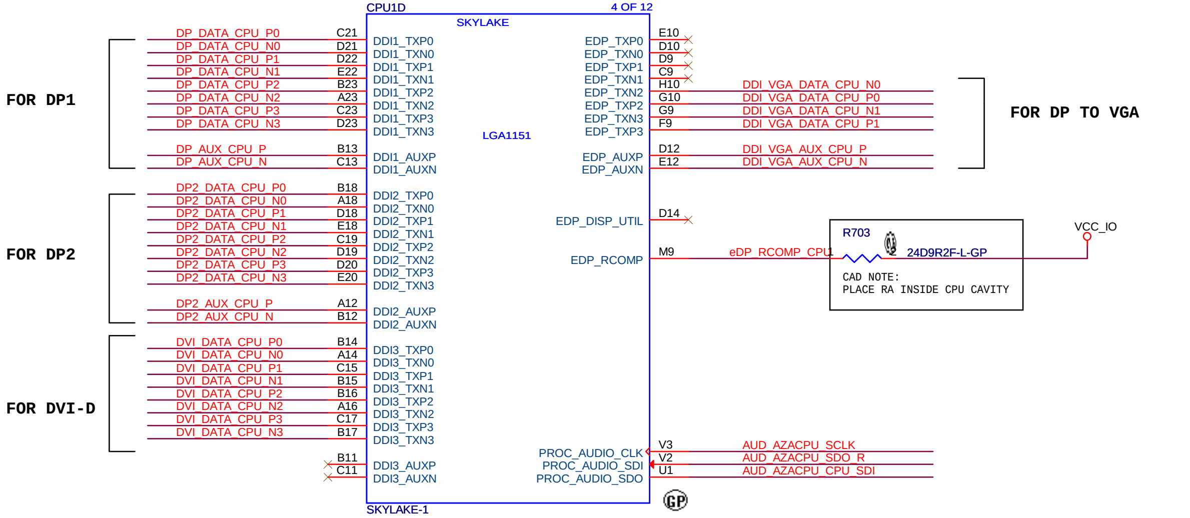
58 DDI_VGA_AUX_CPU_P
58 DDI_VGA_AUX_CPU_N

20 AUD_AZACPU_SCLK
20 AUD_AZACPU_SDO_R
20 AUD_AZACPU_CPU_SDI

VBIOS set as DP

Note:

1. When using eDP bifurcation:
   - x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
   - x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])



FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

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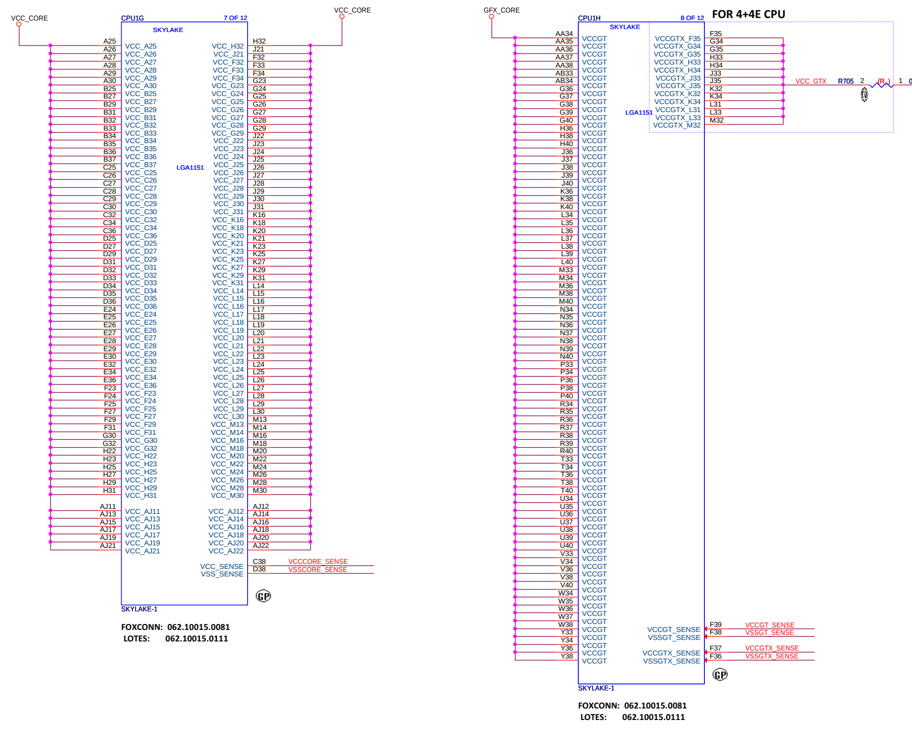
Title	CPU (DDI/EDP)
Size: Custom	Document Number: vHulk — Rev: -1
Date: Wednesday, September 23, 2015	Sheet 7 of 107

46 VCCGT_SENSE
46 VSSGT_SENSE
46 VCCCORE_SENSE
46 VSSCORE_SENSE
52 VCCSA_SENSE
53 VCCIO_SENSE
52 VSS_VCCSA_SSENSE
53 VSS_VCCIO_SSENSE
20,24,42,44 SLP_S4_N

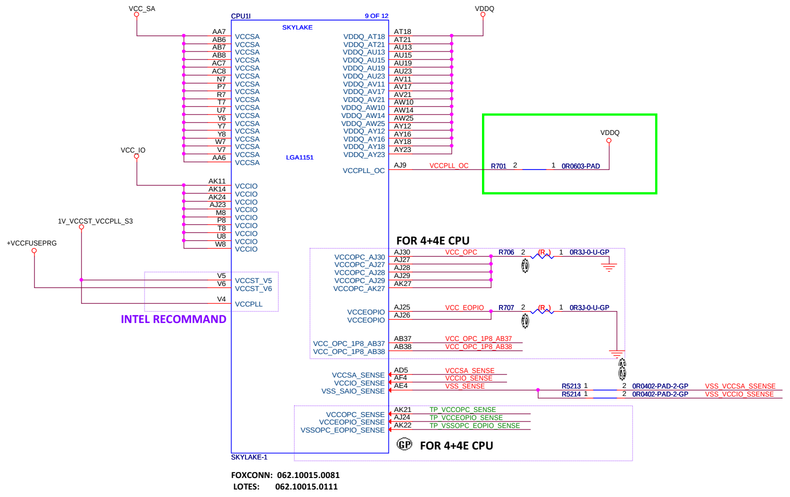


FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

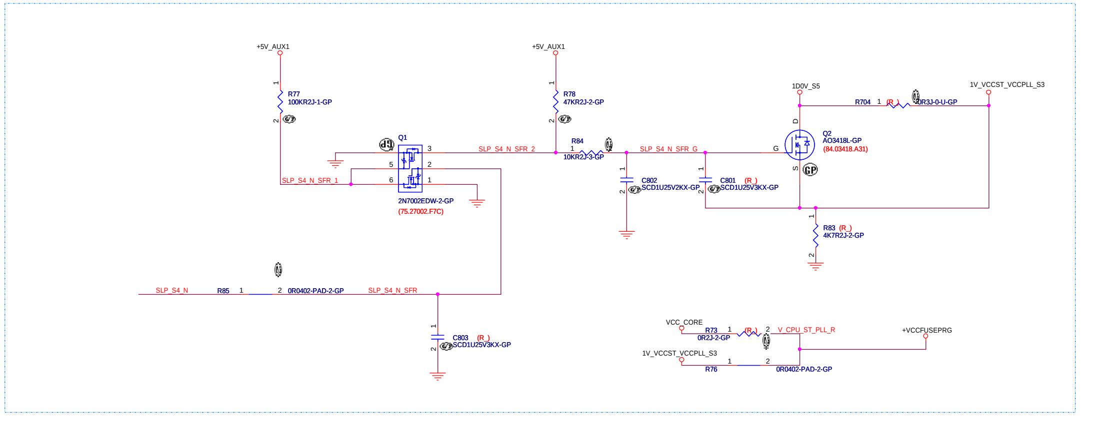
FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

Greenlow Server Reference Circuit: Unused Power Pins Handling

Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGTX, VCC_OPC_1P8, VCCOPC and VCCEOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.



FOXCONN: 062.10015.0081
LOTES: 062.10015.0111



<Core Design>

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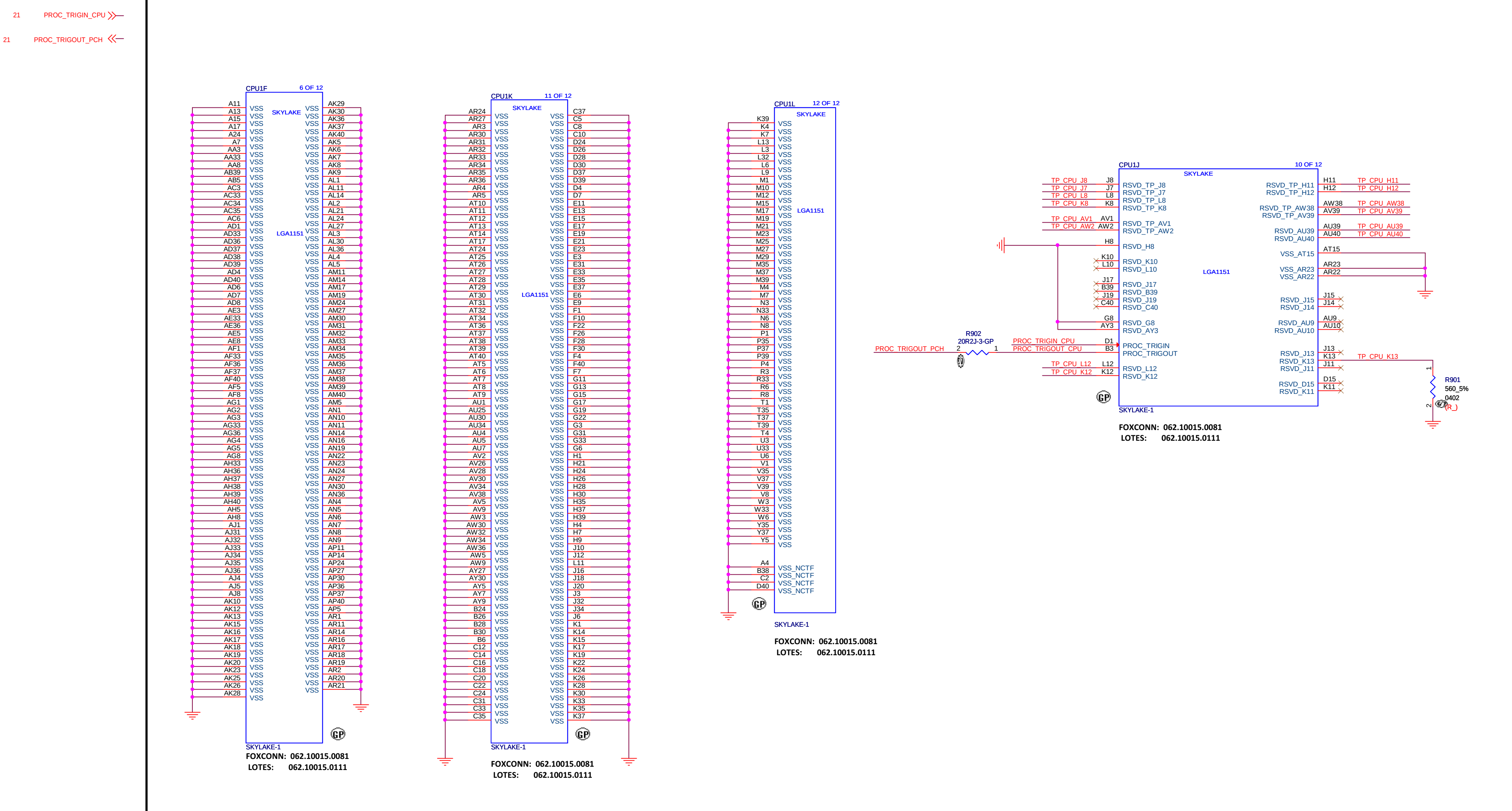
Title: CPU (CPU Power)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 8 of 107



<Core Design>

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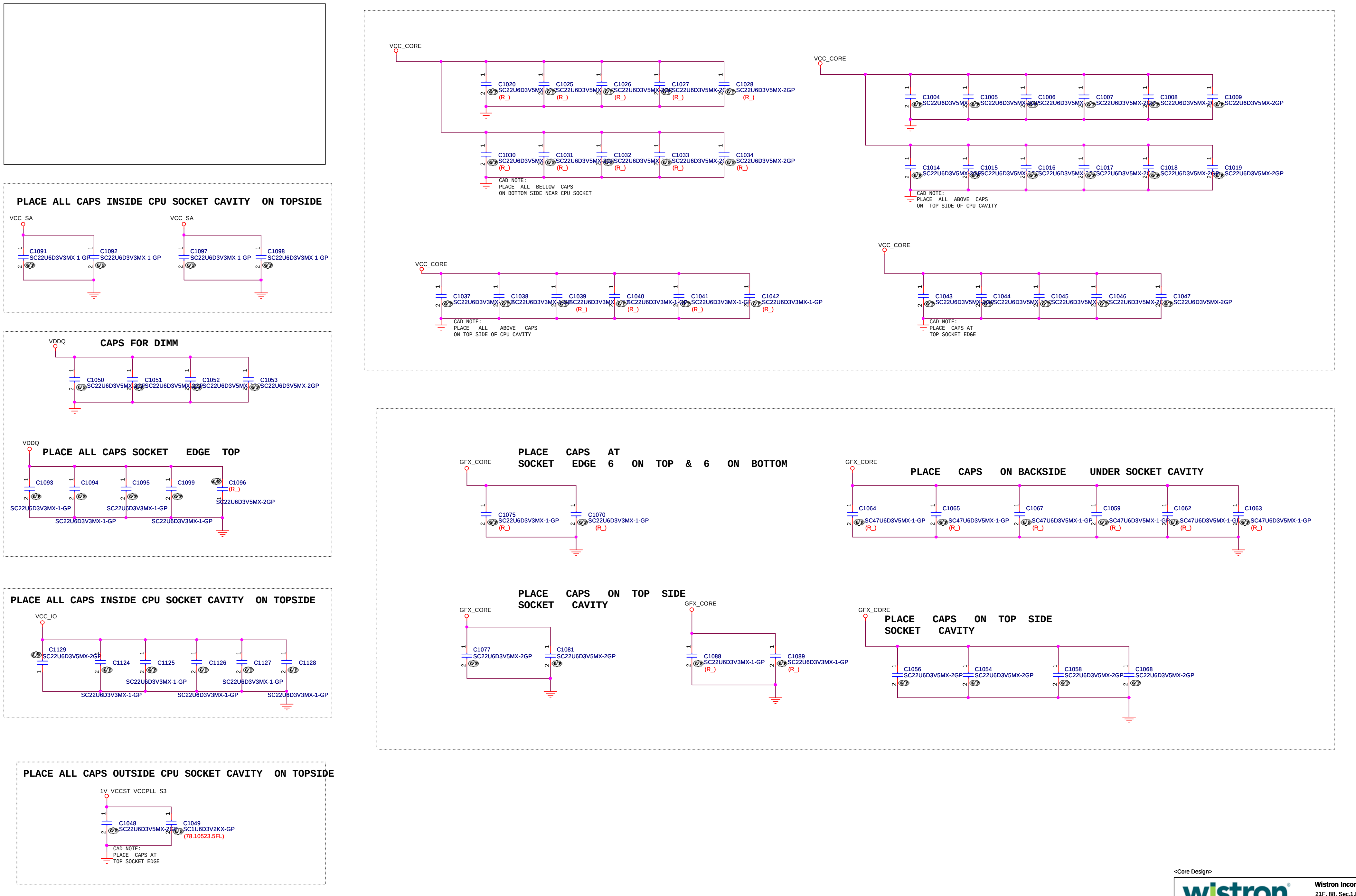
Title	CPU (VSS)
Size C	Document Number vHulk — Rev -1
Date: Wednesday, September 23, 2015	Sheet 9 of 107



<Core Design>

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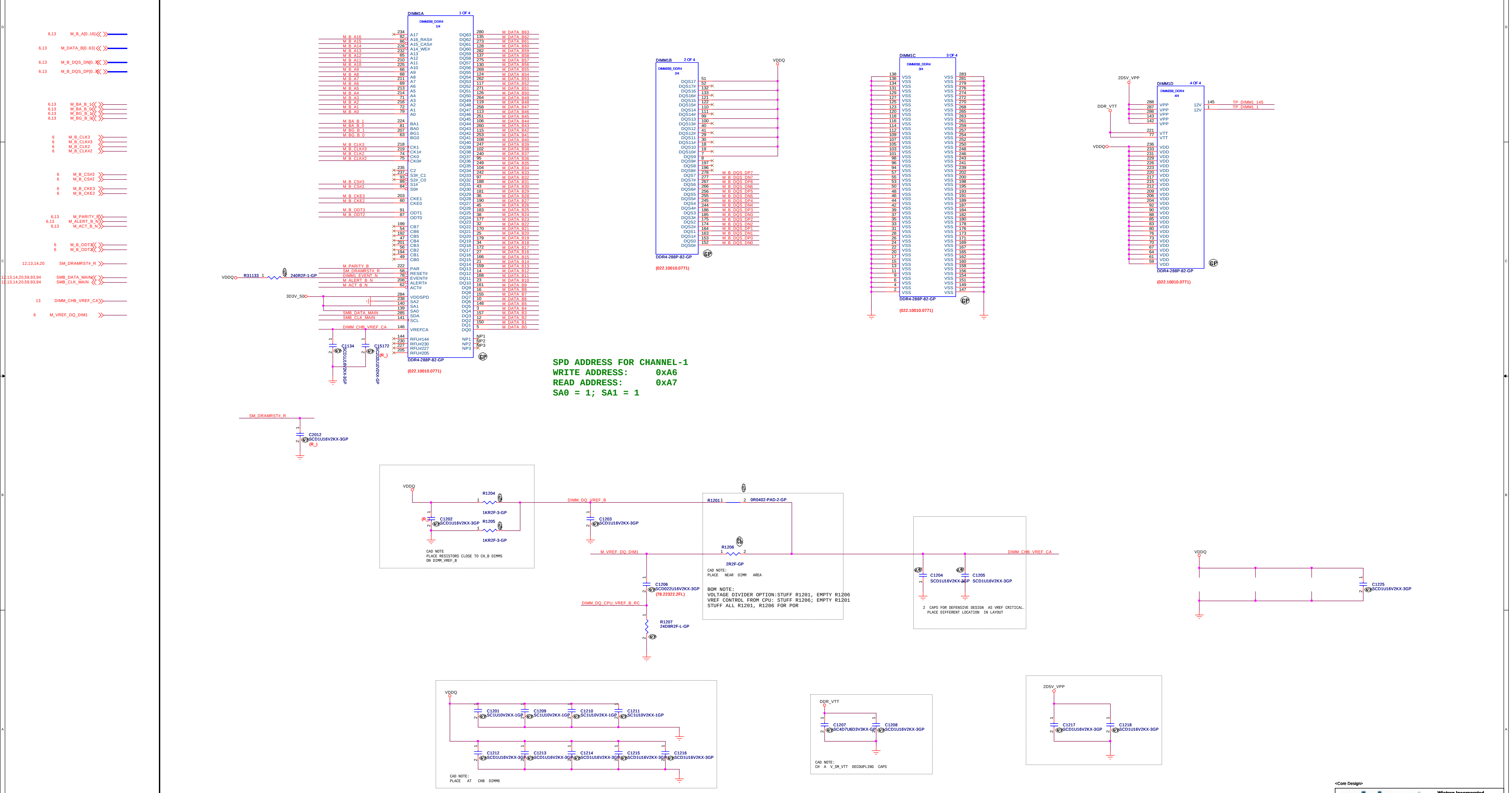
Title	CPU Power CAP	
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 10 of 107	

CHANNEL B -- DIMM1



<Core Design>

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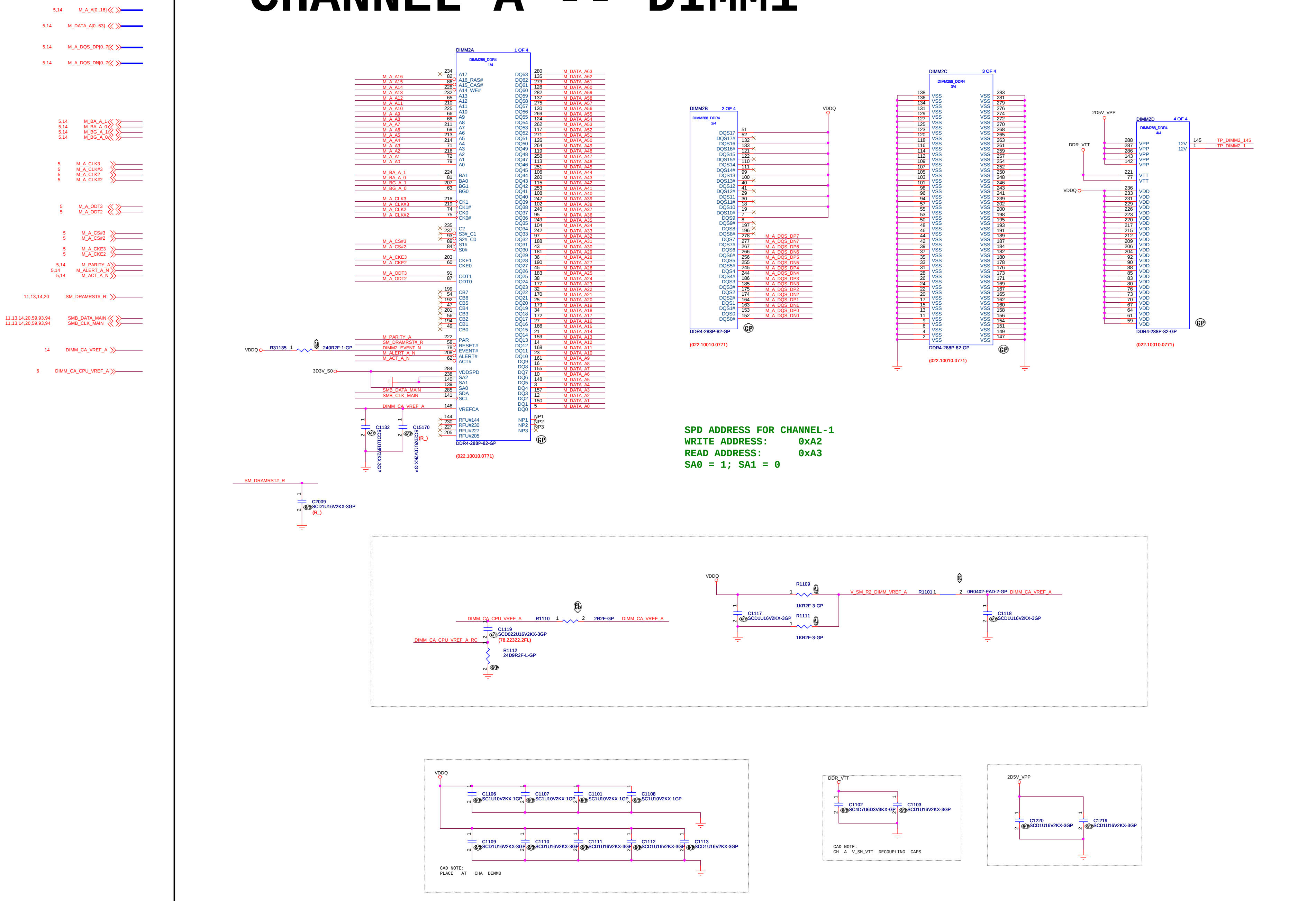
Title: DDR DIMM_1		
Size: D	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 11 of 107	

CHANNEL A -- DIMM1



SPD ADDRESS FOR CHANNEL-1
WRITE ADDRESS: 0xA2
READ ADDRESS: 0xA3
SA0 = 1; SA1 = 0

<Core Design>

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Title: DDR-DIMM_2
Size: Custom
Document Number: vHulk
Rev: -1
Date: Wednesday, September 23, 2015
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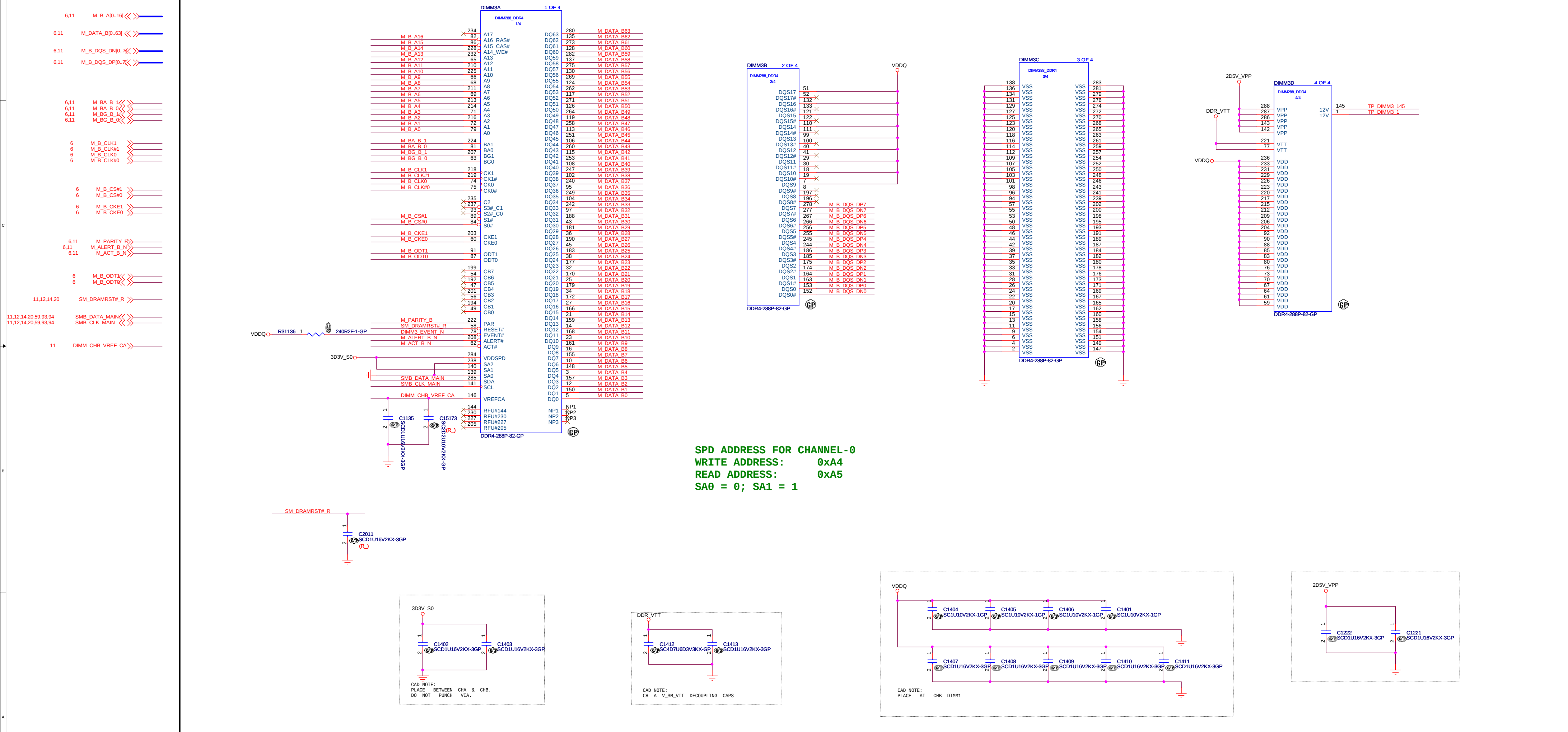
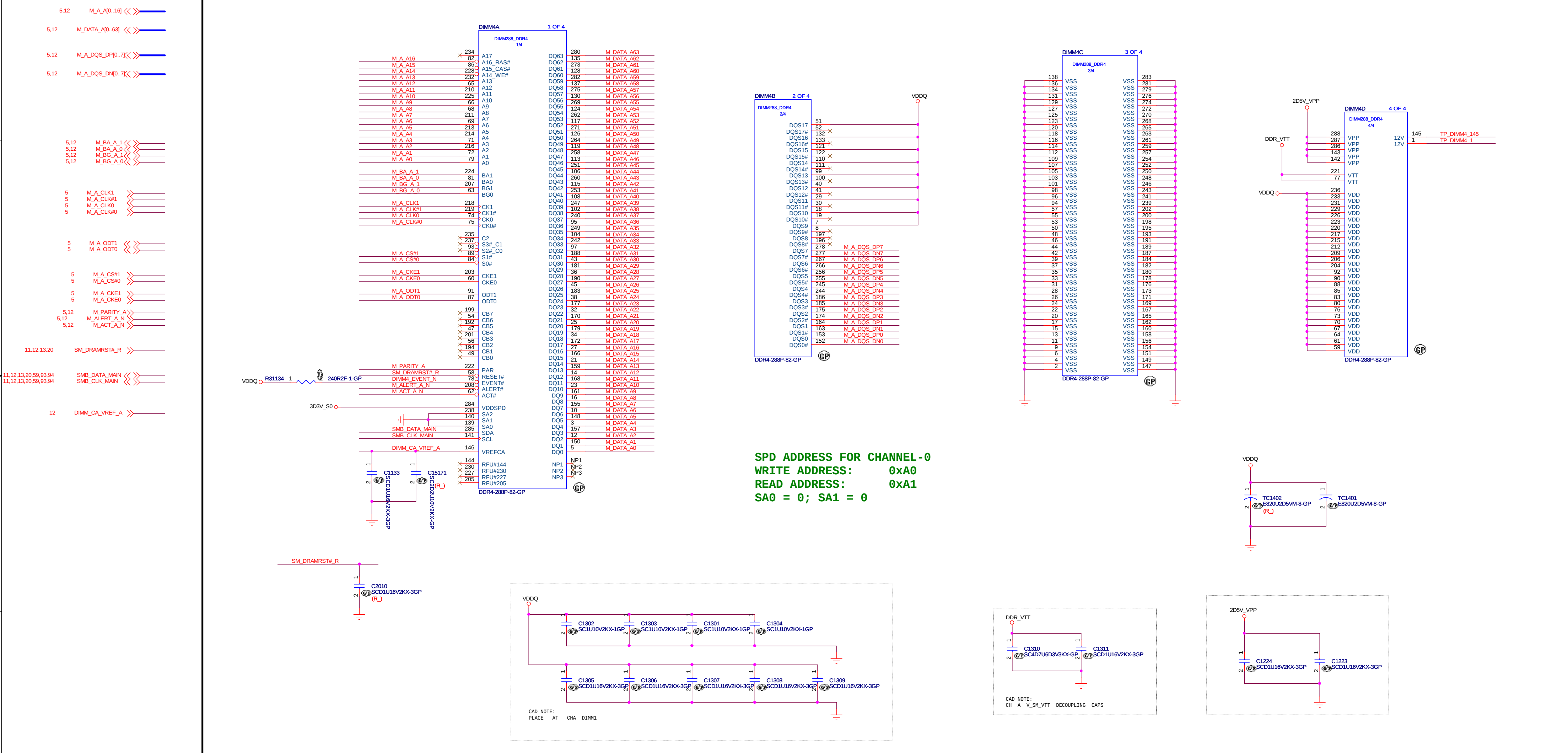
CHANNEL B -- DIMM0



<Core Design>

wistron	**Wistron Incorporated** 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	DDR DIMM_3
Size: Custom	Document Number: vHulk — Rev: -1
Date: Wednesday, September 23, 2015	Sheet 13 of 107

CHANNEL A -- DIMM0



SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS: 0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0

<Core Design>

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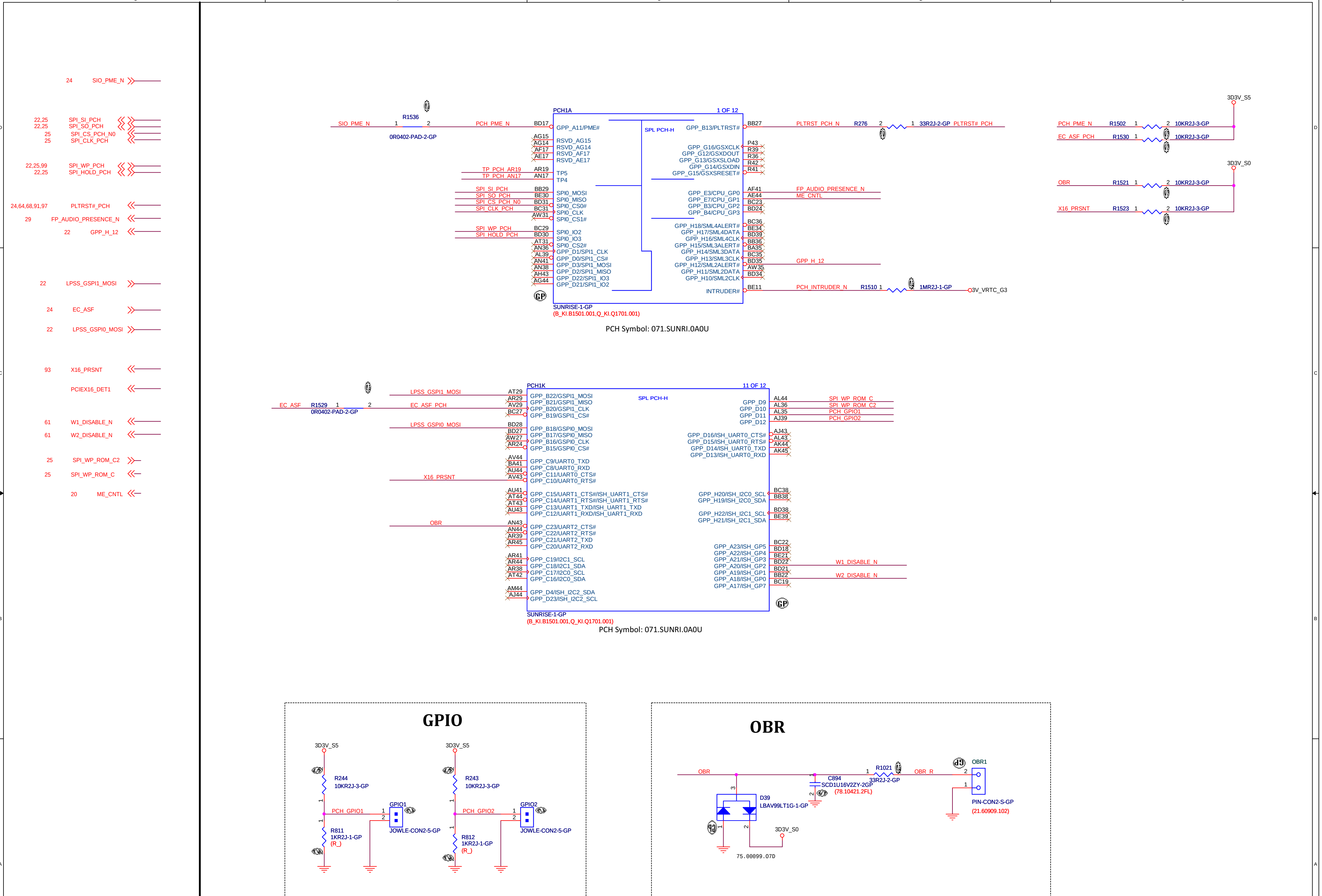
Title: DDR DIMM_4		
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 14 of 107	



<Core Design>

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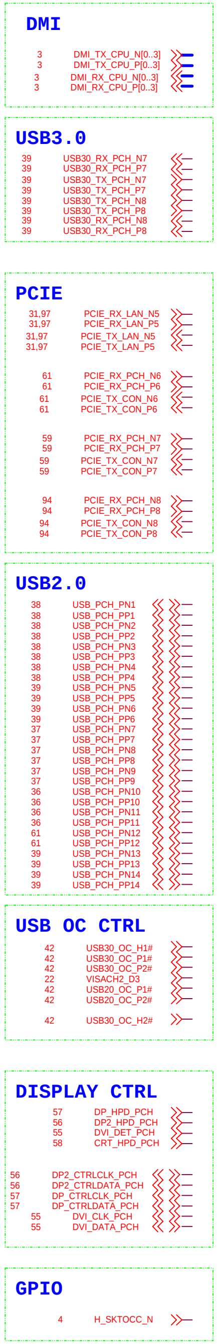
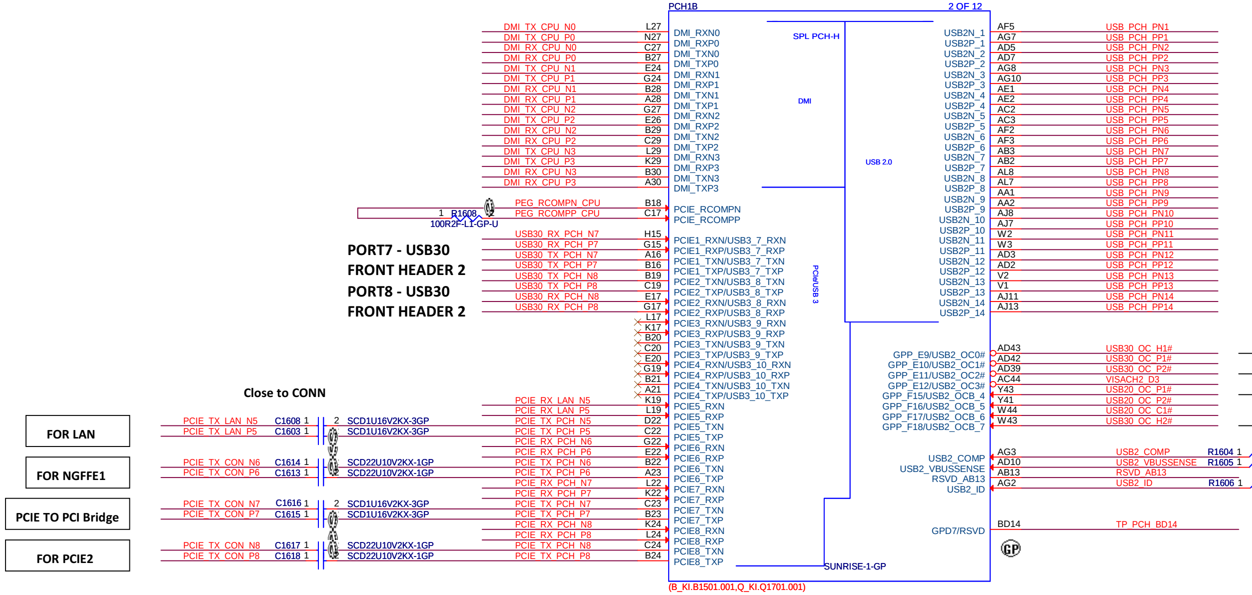
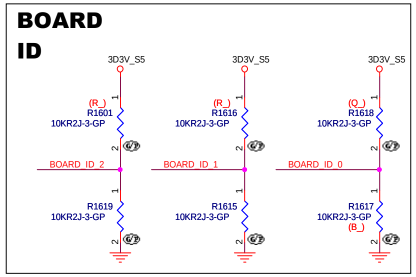
Title	PCH (SPI/UART/I2C)	
Size C	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 15 of 107	





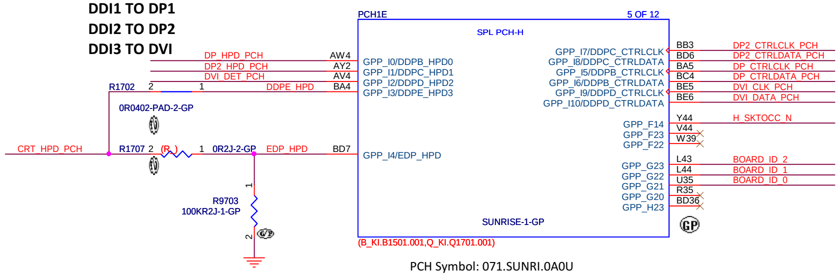
USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Rear)
2	USB3.0 Ext. port 2 (Rear)
3	USB3.0 Ext. port 3 (Rear)
4	USB3.0 Ext. port 4 (Rear)
5	USB3.0 Ext. Header (Front)
6	USB3.0 Ext. Header (Front)
7	USB2.0 Ext. Header (Front)
8	CR Ext. Header (Front)
9	USB2.0 Ext. Header (Front)
10	RJ45+USB Dual port
11	RJ45+USB Dual port
12	NGFFE1
13	USB3.0 Ext.Header (Front) for Q170 bom option
14	USB3.0 Ext.Header (Front) for Q170 bom option

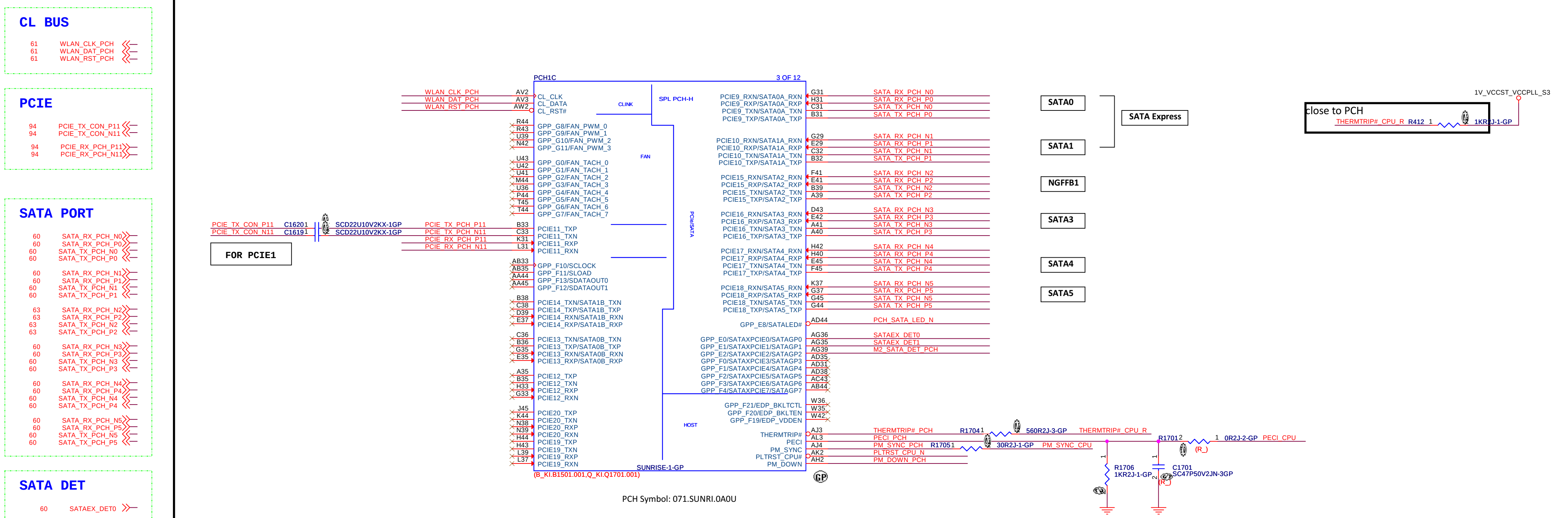


Board_ID_0
pull high for Q170
pull low for B150

2014/9/9
DDI1 TO DP1
DDI2 TO DP2
DDI3 TO DVI



PCH Symbol: 071.SUNRI.0A0U



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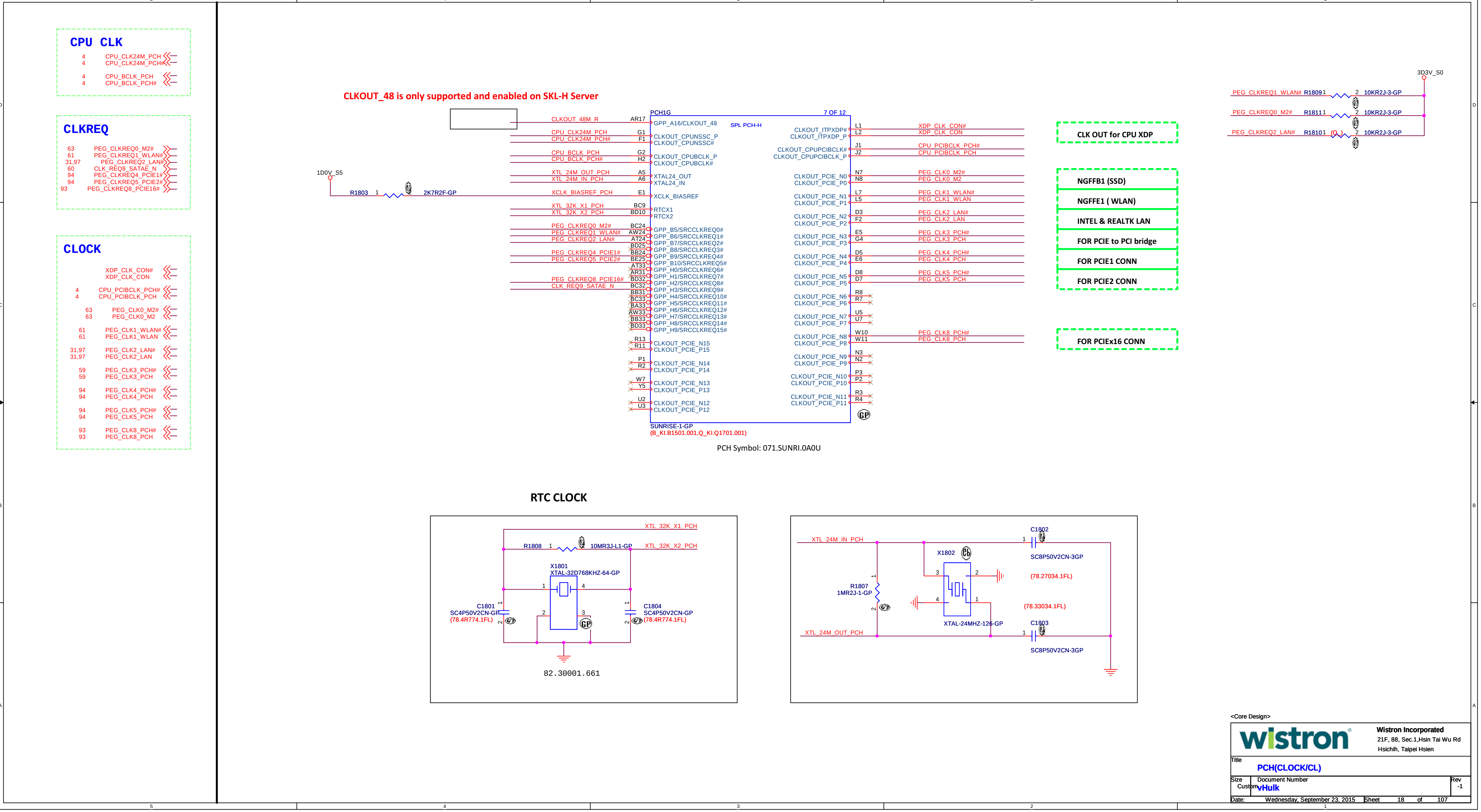
Title		
PCH (PCI-E/SATA)		
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 17 of 107	


CPU CLK
CPU_CLK24M_PCH
CPU_CLK24M_PCH#
CPU_BCLK_PCH
CPU_BCLK_PCH#
CLKREQ
PEG_CLKREQ0_M2#
PEG_CLKREQ1_WLAN#
PEG_CLKREQ2_LAN#
CLK_REQ9_SATAE_N
PEG_CLKREQ4_PCIE1#
PEG_CLKREQ5_PCIE2#
PEG_CLKREQ8_PCIE16#
CLOCK
XDP_CLK_CON#
XDP_CLK_CON
CPU_PCIBCLK_PCH#
CPU_PCIBCLK_PCH
PEG_CLK0_M2#
PEG_CLK0_M2
PEG_CLK1_WLAN#
PEG_CLK1_WLAN
PEG_CLK2_LAN#
PEG_CLK2_LAN
PEG_CLK3_PCH#
PEG_CLK3_PCH
PEG_CLK4_PCH#
PEG_CLK4_PCH
PEG_CLK5_PCH#
PEG_CLK5_PCH
PEG_CLK8_PCH#
PEG_CLK8_PCH
CLKOUT_48 is only supported and enabled on SKL-H Server
PCH1G
7 OF 12
SPL PCH-H
SUNRISE-1-GP
(B_KI.B1501.001,Q_KI.Q1701.001)
PCH Symbol: 071.SUNRI.0A0U
1D0V_S5
R1803
2K7R2F-GP
XCLK_BIASREF_PCH
3D3V_S0
R1809
R1811
R1810
10KR2J-3-GP
CLK OUT for CPU XDP
NGFFB1 (SSD)
NGFFE1 (WLAN)
INTEL & REALTK LAN
FOR PCIE to PCI bridge
FOR PCIE1 CONN
FOR PCIE2 CONN
FOR PCIEx16 CONN
RTC CLOCK
XTL_32K_X1_PCH
XTL_32K_X2_PCH
R1808
10MR3J-L1-GP
X1801
XTAL-32D768KHZ-64-GP
C1801
SC4P50V2CN-GP
(78.4R774.1FL)
C1804
SC4P50V2CN-GP
(78.4R774.1FL)
82.30001.661
XTL_24M_IN_PCH
XTL_24M_OUT_PCH
R1807
1MR2J-1-GP
X1802
XTAL-24MHZ-126-GP
C1802
SC8P50V2CN-3GP
C1803
SC8P50V2CN-3GP
(78.27034.1FL)
(78.33034.1FL)
<Core Design>
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Title
PCH(CLOCK/CL)
Size
Custom
Document Number
vHulk
Rev
-1
Date: Wednesday, September 23, 2015
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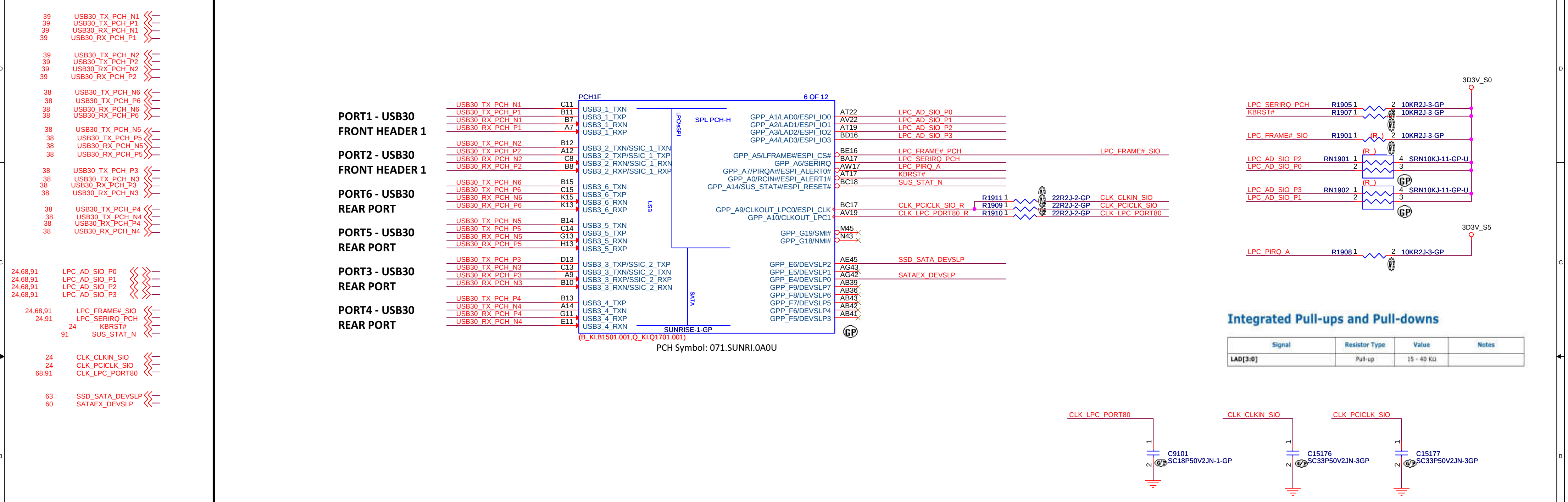

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 - 40 KΩ	

<Core Design>

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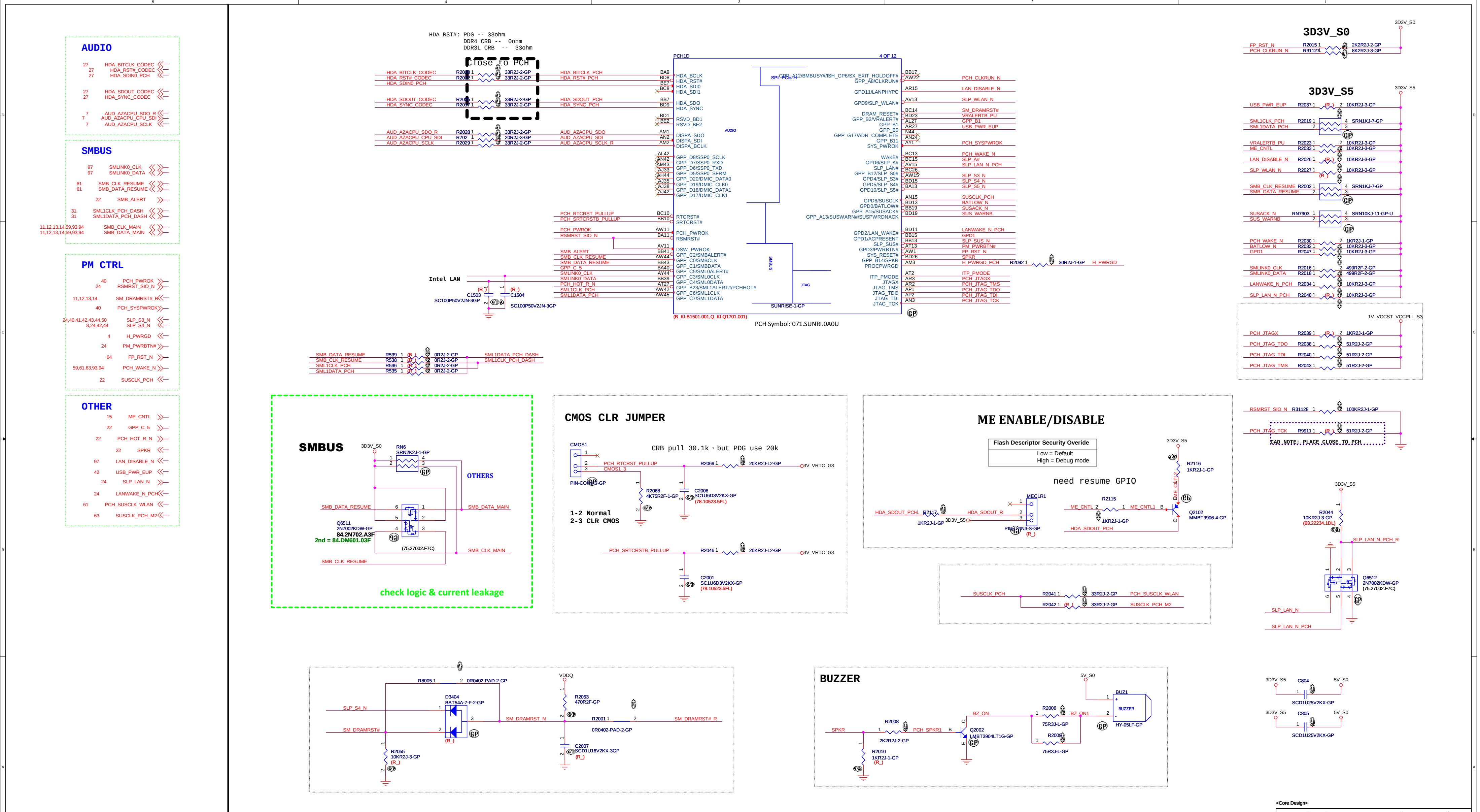
Title: PCH (USB/ESPI

Size: Custom | Document Number: vHulk | Rev: -1

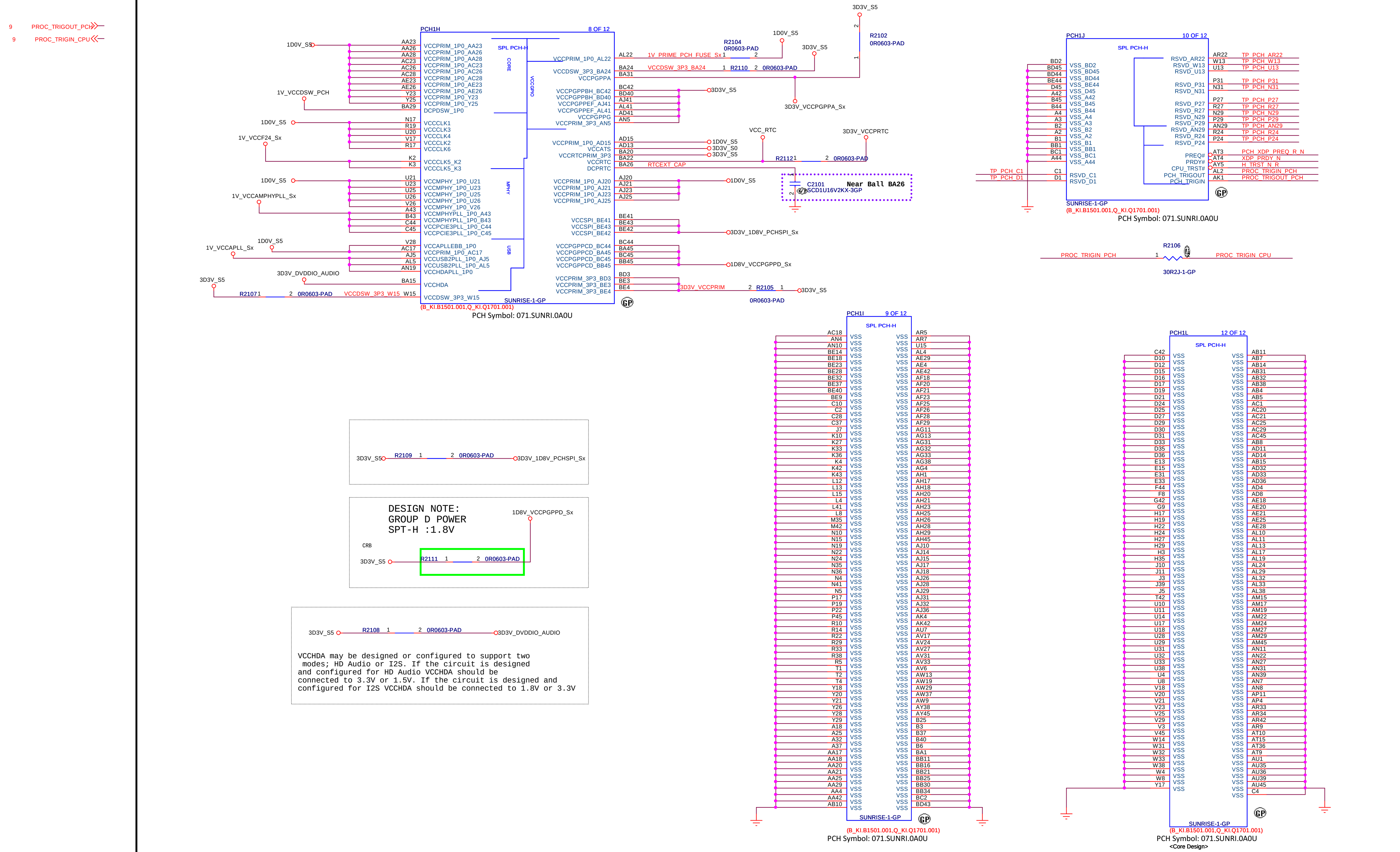
Date: Wednesday, September 23, 2015 | Sheet 19 of 107



Title: PCH (GPIO/CPU/SMBUS/IHDA/JTAG)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 |



DESIGN NOTE:
GROUP D POWER
SPT-H :1.8V

VCCHDA may be designed or configured to support two modes; HD Audio or I2S. If the circuit is designed and configured for HD Audio VCCHDA should be connected to 3.3V or 1.5V. If the circuit is designed and configured for I2S VCCHDA should be connected to 1.8V or 3.3V

<Core Design>

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Title: PCH (POWER1)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 21 of 107

PCH STRAP FUNCTIONS

SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU

SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
SMB_ALERT (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

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Title: PCH_(POWER2)

Size: C | Document Number: vHulk | Rev: -1

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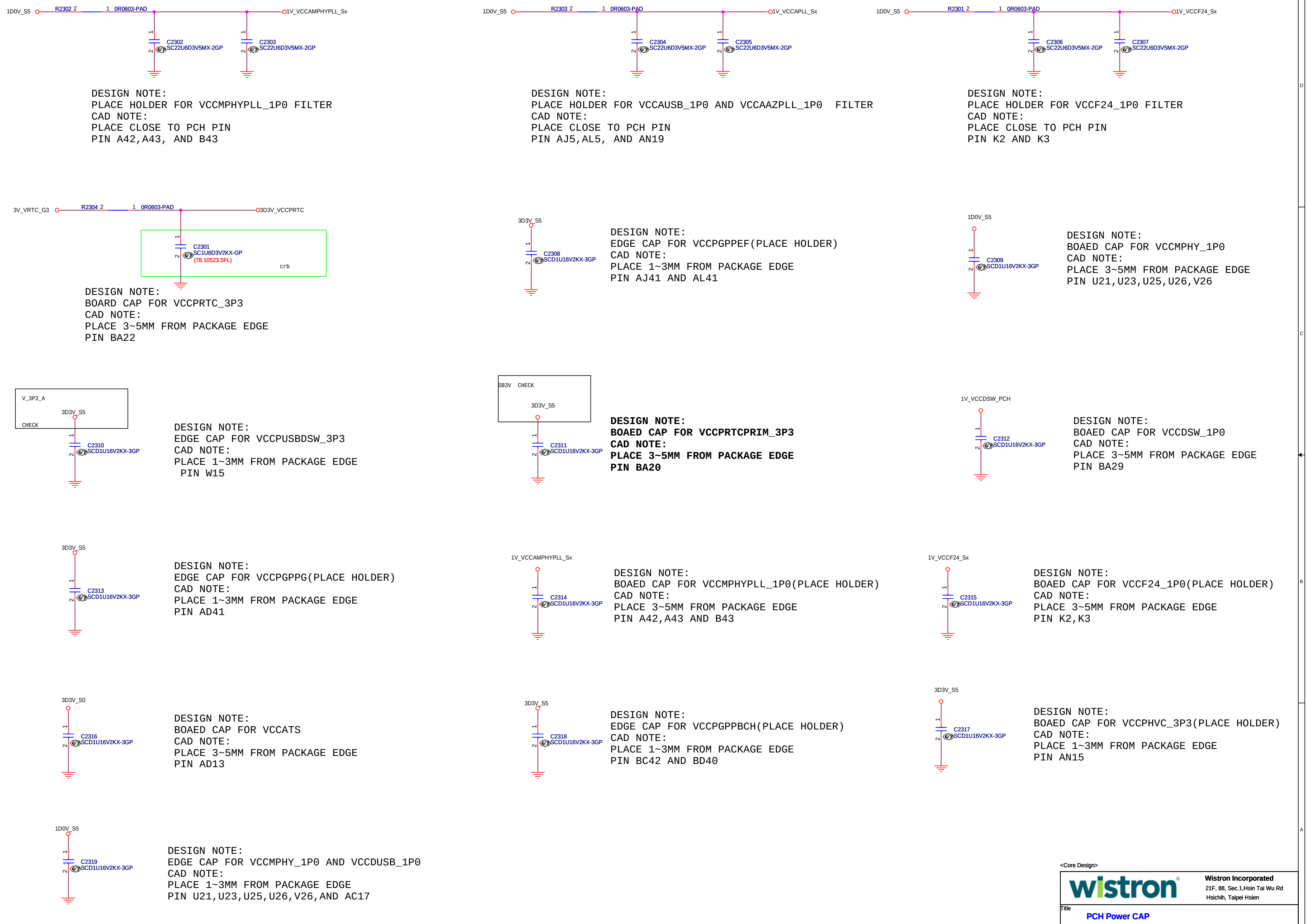

DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43

DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19

DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3

DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22

DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41

DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26

DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN W15

DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20

DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29

DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41

DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43

DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3

DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13

DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40

DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15

DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

<Core Design>

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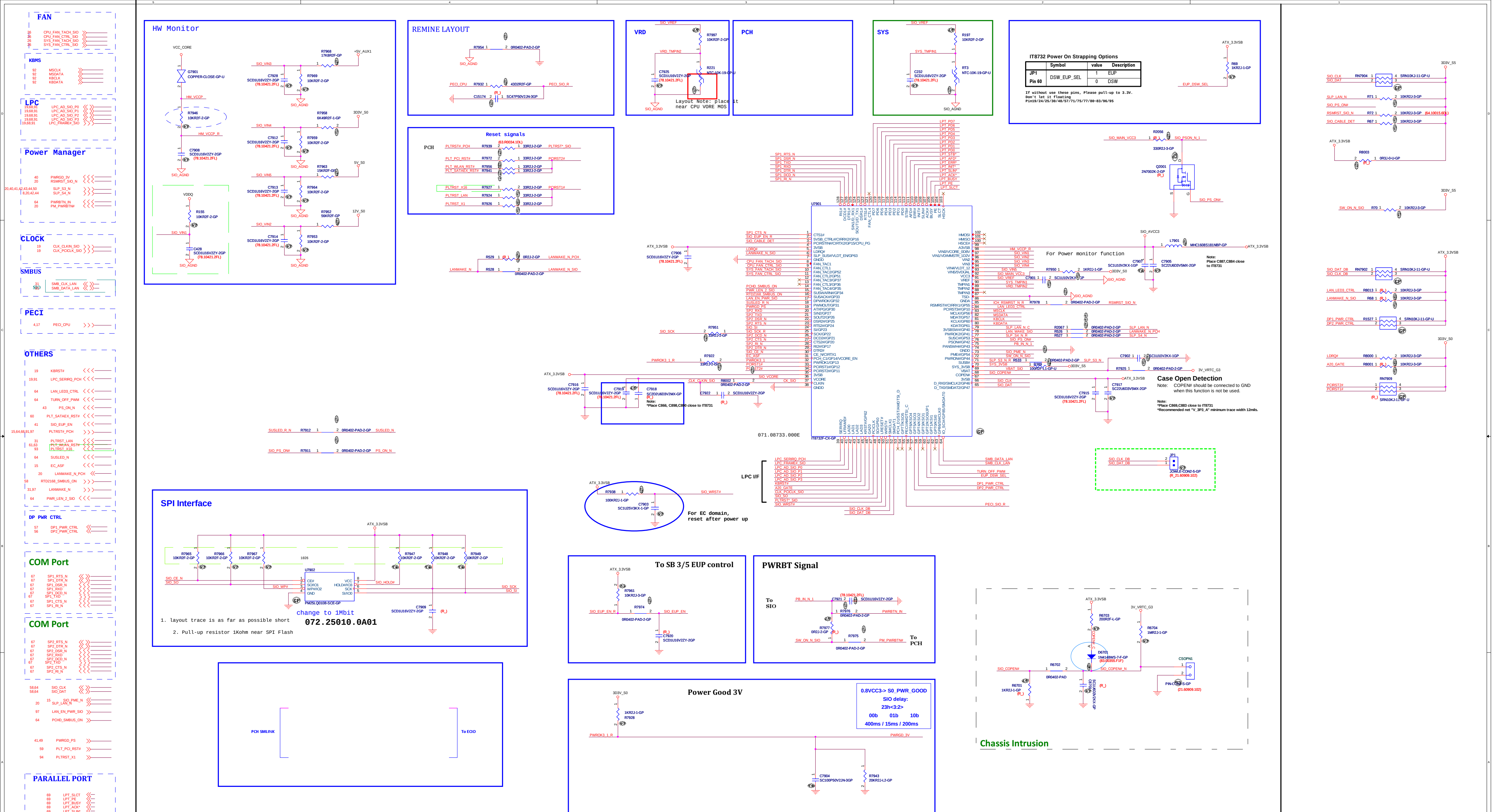
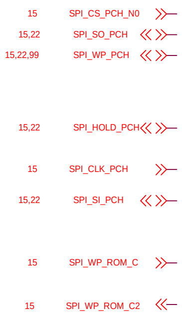
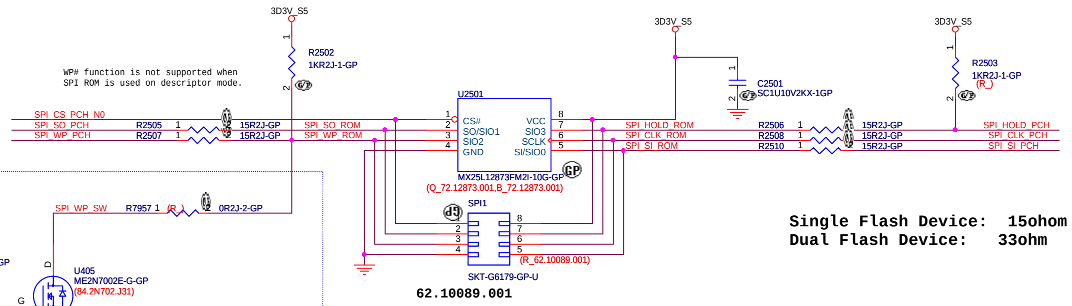
Title: PCH Power CAP		
Size: C	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 23 of 107	

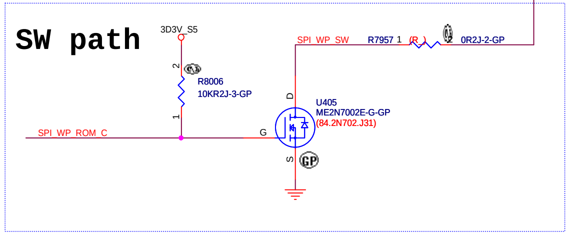

FAN
KBMS
LPC
Power Manager
CLOCK
SMBUS
PECI
OTHERS
DP PWR CTRL
COM Port
COM Port
PARALLEL PORT
HW Monitor
REMINE LAYOUT
Reset signals
VRD
Layout Note: place it near CPU VORE MOS
PCH
SYS
IT8732 Power On Strapping Options
Symbol | value | Description
JP1 Pin 60 | DSW_EUP_SEL | 1 EUP | 0 DSW
If without use these pins, Please pull-up to 3.3V. Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80~83/96/95
For Power monitor function
Case Open Detection
Note: COPEN# should be connected to GND when this function is not be used.
LPC I/F
For EC domain, reset after power up
SPI Interface
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash
change to 1Mbit
072.25010.0A01
071.08733.000E
To SB 3/5 EUP control
PWRBT Signal
To SIO
To PCH
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
PCH SMLINK
To ECIO
Chassis Intrusion

SPI ROM

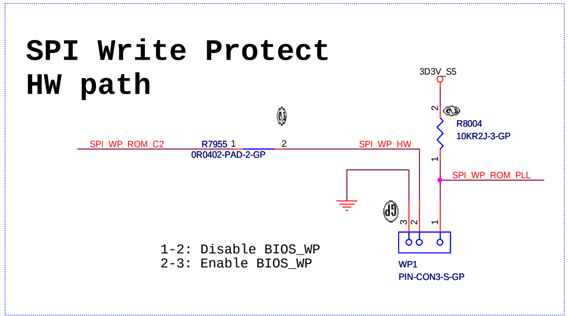




SPI socket mount in SA stage

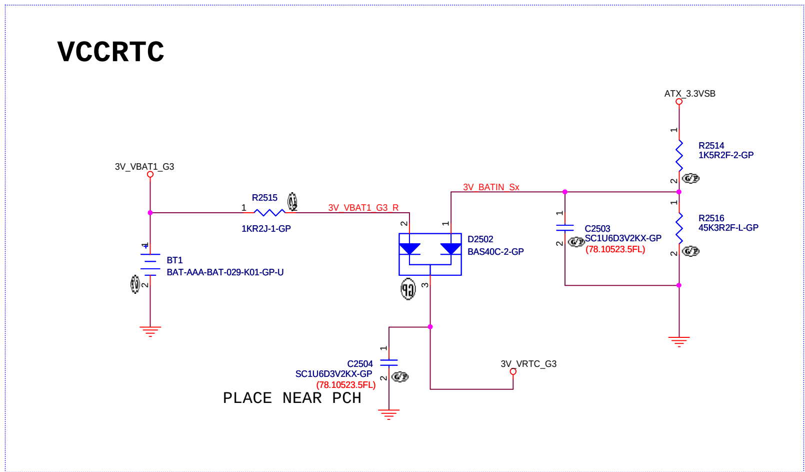


Single Flash Device: 15ohom
Dual Flash Device: 33ohm



SPI ROM TABLE

	Vendor	Package	SA	SB
Q170/B150	MXIC	SOP8 / 16MB	72.12873.001	72.12873.001
	WINBOND	SOP8 / 16MB	72.25128.0E1	72.25128.0E1



SKL Platforms – SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

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Title	Flash&RTC	
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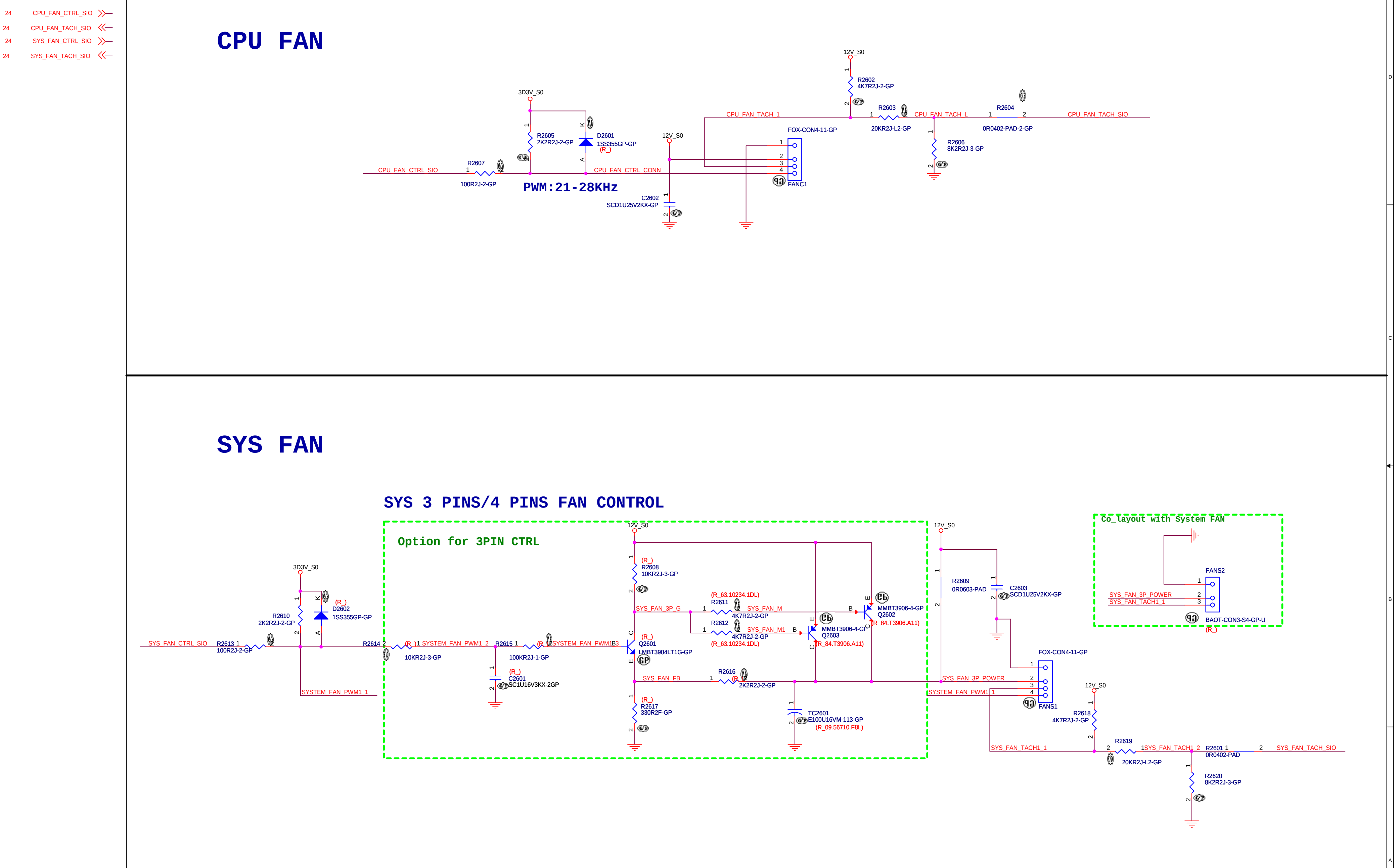

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Title	Thermal & FAN	
Size C	Document Number vHulk	Rev -1
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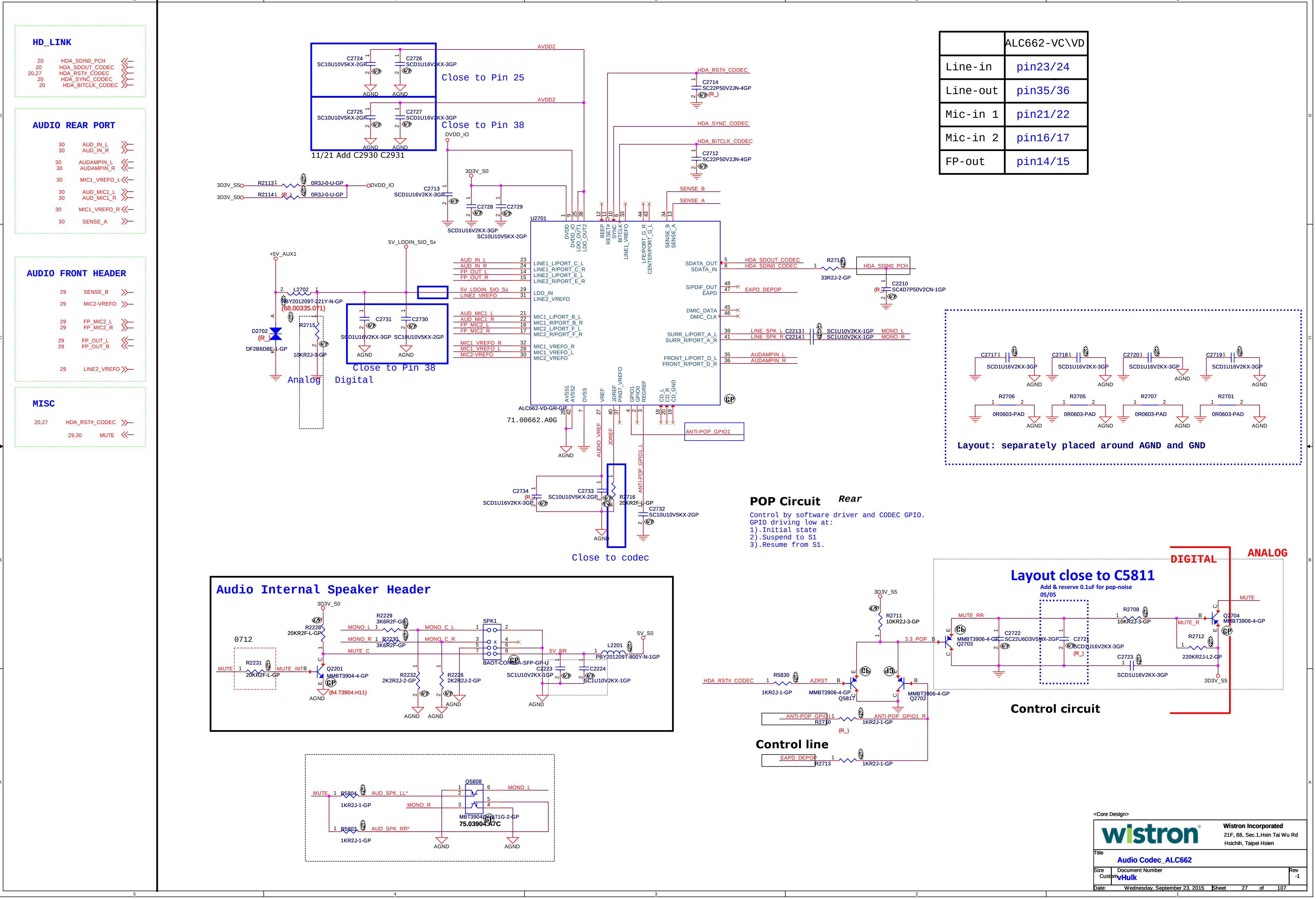

	ALC662-VC\VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
FP-out	pin14/15

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Title: Audio Codec_ALC662

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(R)

<Core Design>

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Title	AMP_(R)	
Size C	Document Number vHulk	Rev -1
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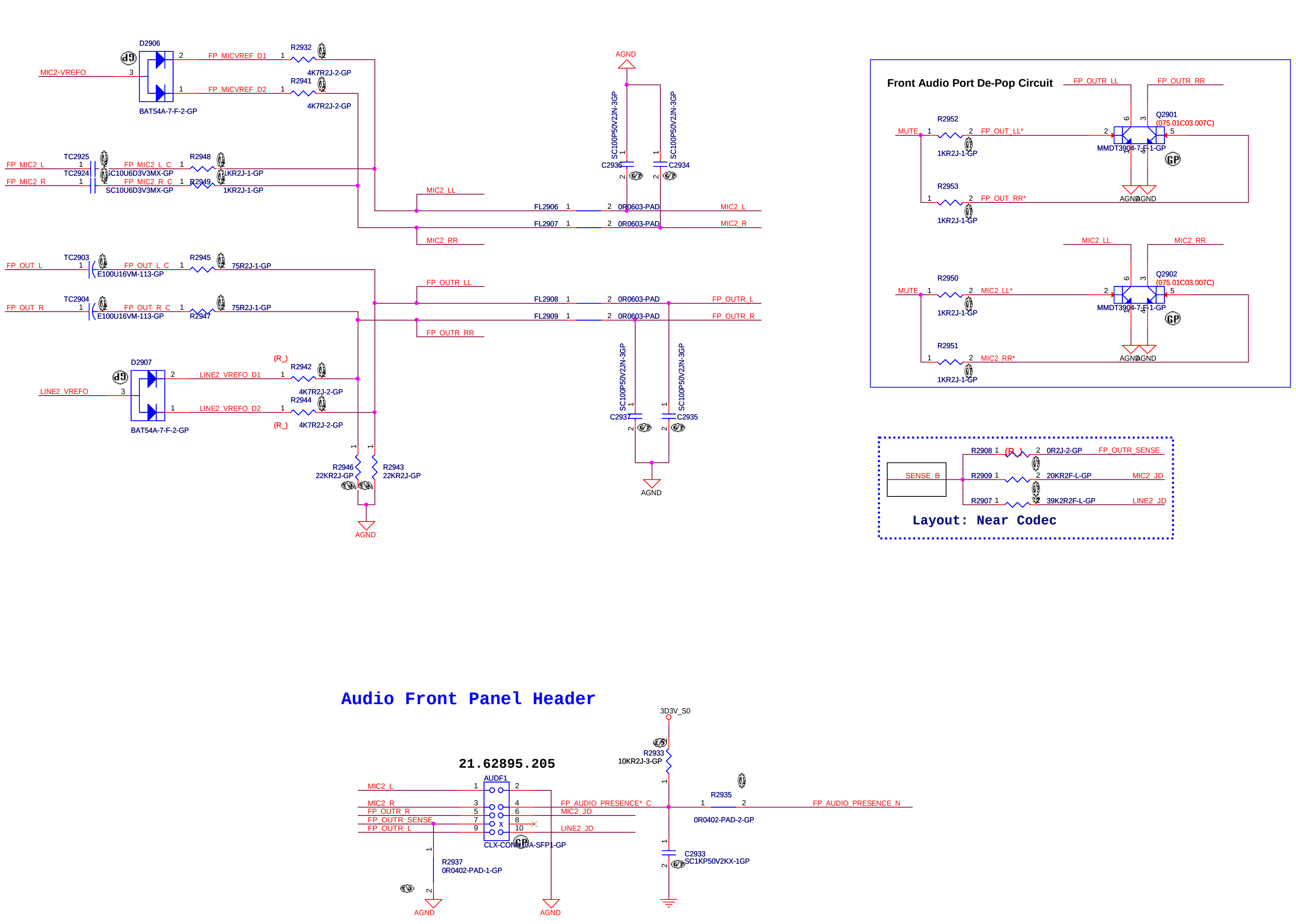
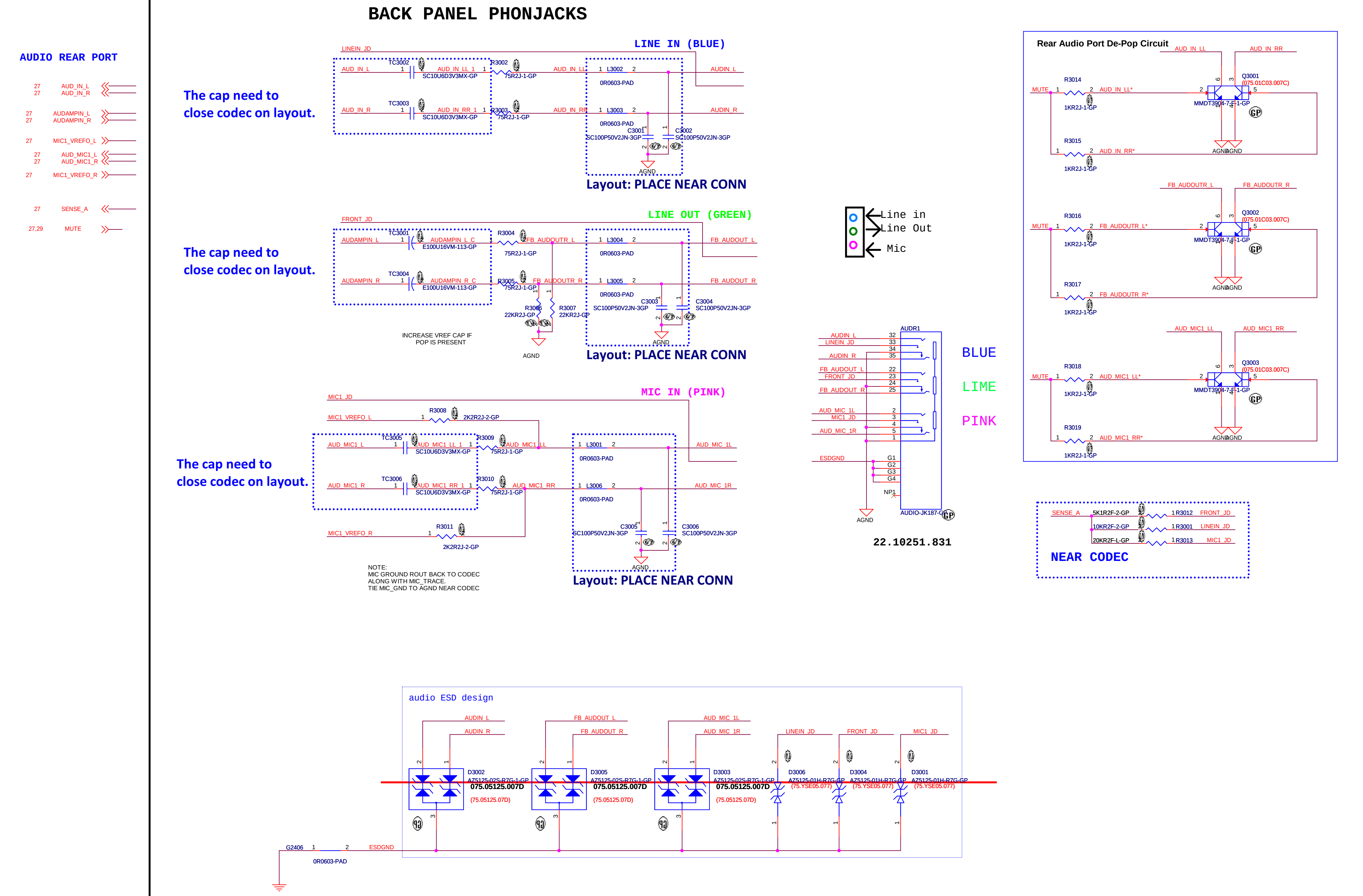


Audio Front Panel Header

BACK PANEL PHONJACKS



<Core Design>

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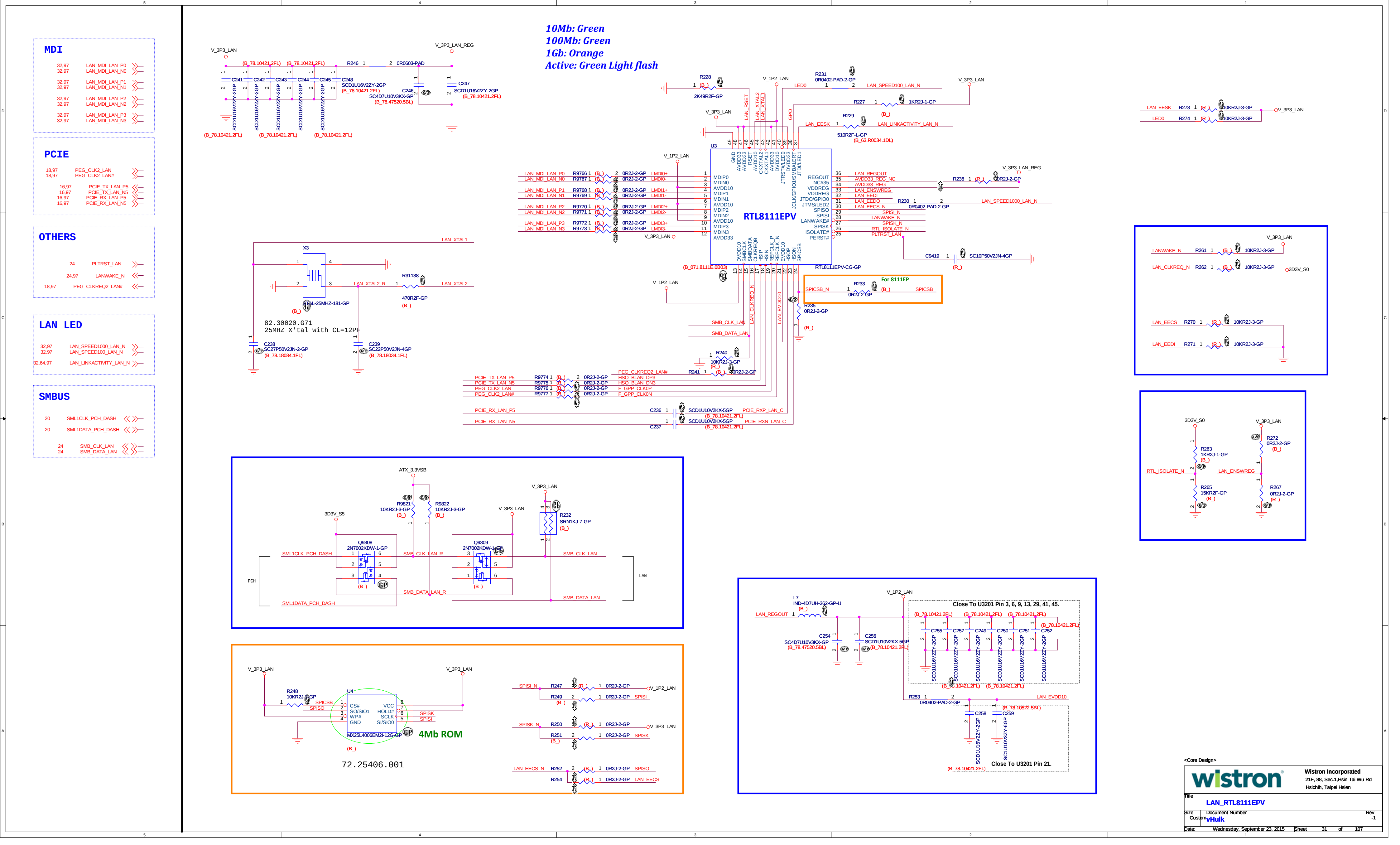
Title	Audio IO_Rear	
Size C	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 30 of 107	



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Title: LAN_RTL8111EPV

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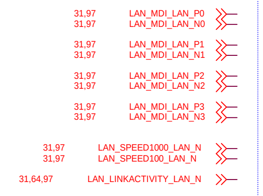
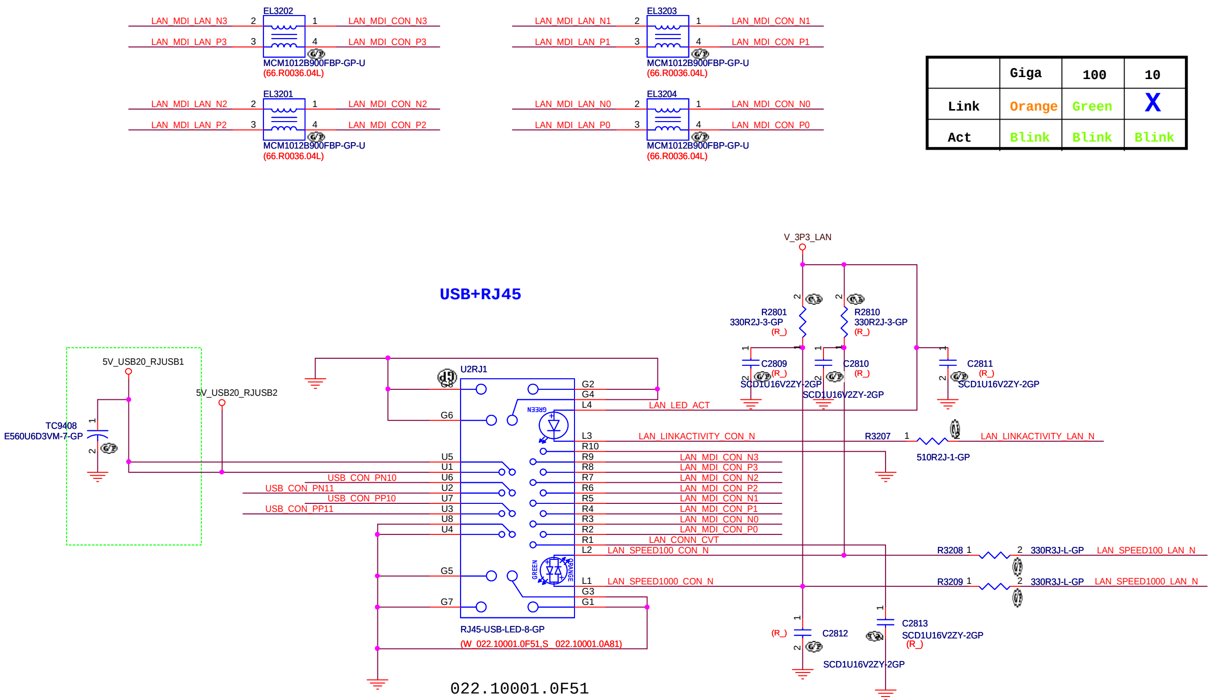
LAN



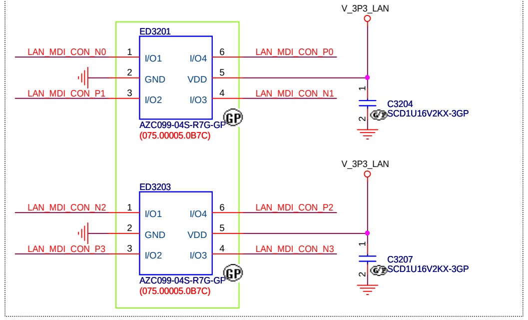
LAN

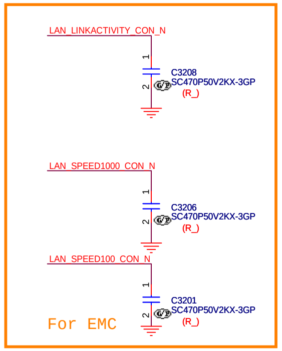
	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

USB+RJ45



ESD





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Title	RJ45&Transformer		
Size C	Document Number vHulk		Rev -1
Date: Wednesday, September 23, 2015	Sheet 32 of 107		

(R)

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Title	Card Reader_(R)	
Size: C	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 33 of 107	

(R)

<Core Design>

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Title	USB Charger_(R)	
Size C	Document Number vHulk	Rev -1
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(R)

<Core Design>

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Title	USB_Redrive_(R)
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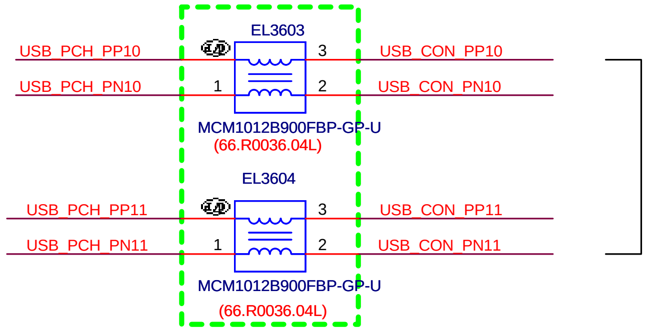
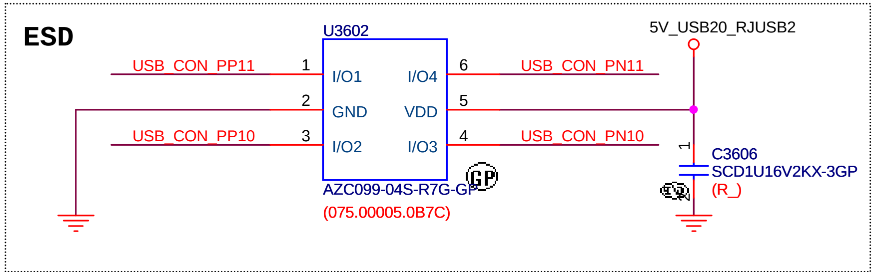
USB 2.0 Rear Signals for RJ45/USB2.0 Stack

16	USB_PCH_PP10	
16	USB_PCH_PN10	
16	USB_PCH_PP11	
16	USB_PCH_PN11	
32	USB_CON_PP10	
32	USB_CON_PN10	
32	USB_CON_PP11	
32	USB_CON_PN11	

USB 2.0 Rear Signals for RJ45/USB2.0 Stack



DESIGN NOTE:
To U2RJ1(U2+RJ45 CONN)
IF SI Concern, Change CMC PN:068.01012.2001



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Title	**USB 20_REAR PORT**	
Size: Custom	Document Number: **vHulk**	Rev: -1
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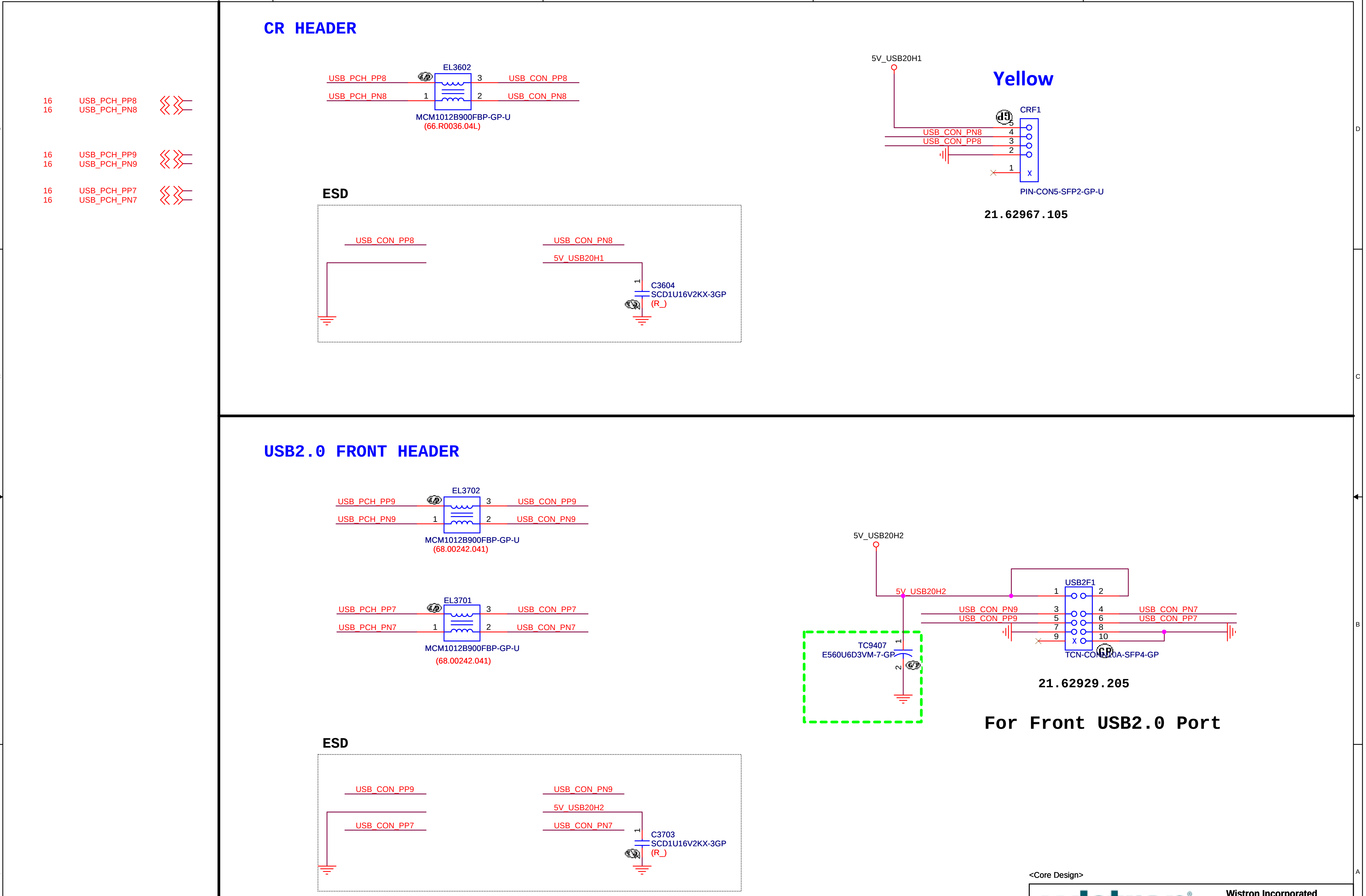

<Core Design>

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Title	USB20_FRONT HEADER	
Size: Custom	Document Number: vHulk	Rev: -1
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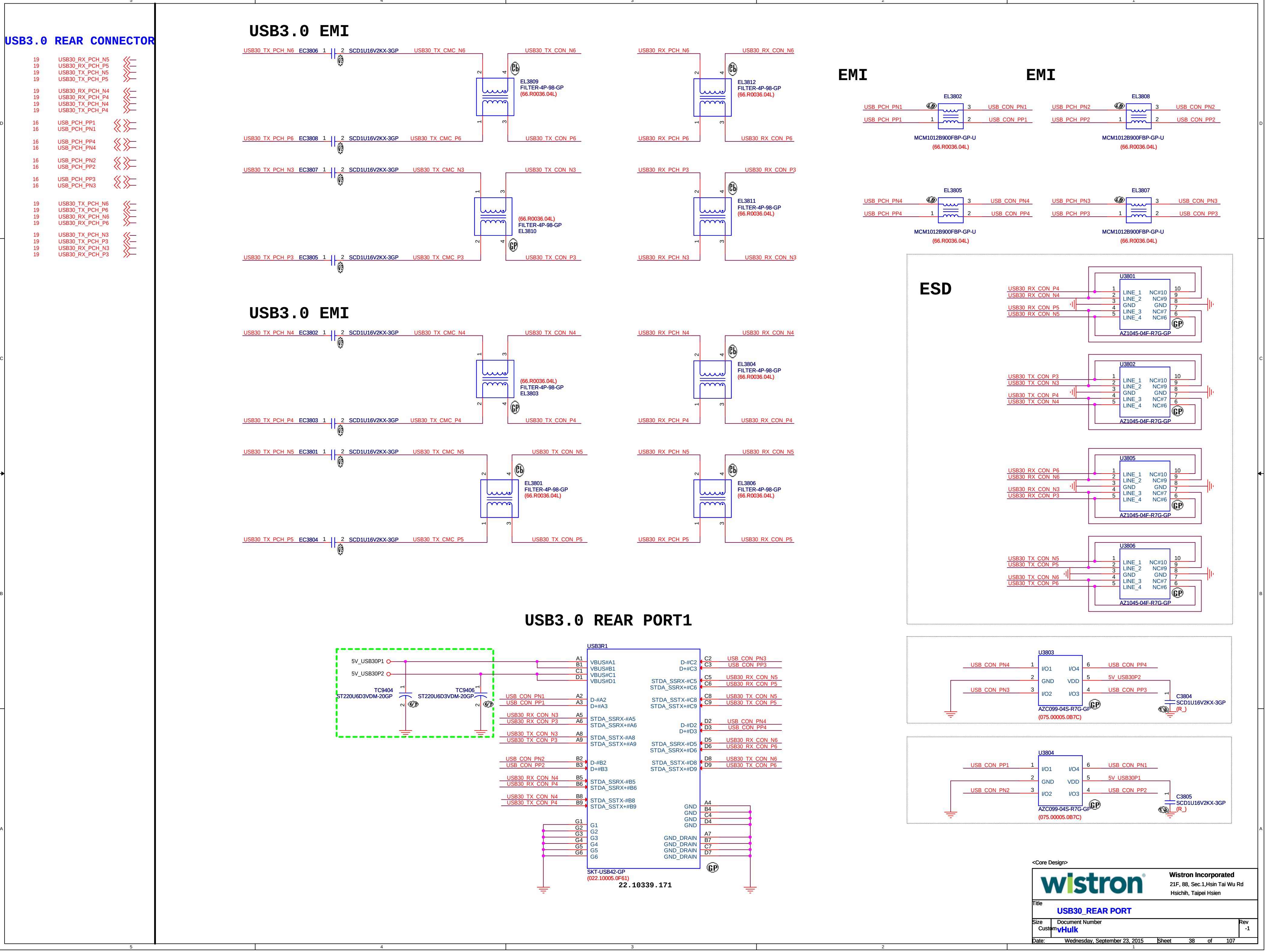
USB3.0 REAR CONNECTOR
19 USB30_RX_PCH_N5
19 USB30_RX_PCH_P5
19 USB30_TX_PCH_N5
19 USB30_TX_PCH_P5
19 USB30_RX_PCH_N4
19 USB30_RX_PCH_P4
19 USB30_TX_PCH_N4
19 USB30_TX_PCH_P4
16 USB_PCH_PP1
16 USB_PCH_PN1
16 USB_PCH_PP4
16 USB_PCH_PN4
16 USB_PCH_PN2
16 USB_PCH_PP2
16 USB_PCH_PP3
16 USB_PCH_PN3
19 USB30_TX_PCH_N6
19 USB30_TX_PCH_P6
19 USB30_RX_PCH_N6
19 USB30_RX_PCH_P6
19 USB30_TX_PCH_N3
19 USB30_TX_PCH_P3
19 USB30_RX_PCH_N3
19 USB30_RX_PCH_P3
USB3.0 EMI
EC3806 SCD1U16V2KX-3GP
EC3808 SCD1U16V2KX-3GP
EC3807 SCD1U16V2KX-3GP
EC3805 SCD1U16V2KX-3GP
EL3809 FILTER-4P-98-GP (66.R0036.04L)
EL3810 FILTER-4P-98-GP (66.R0036.04L)
EL3812 FILTER-4P-98-GP (66.R0036.04L)
EL3811 FILTER-4P-98-GP (66.R0036.04L)
USB30_TX_CMC_N6
USB30_TX_CMC_P6
USB30_TX_CMC_N3
USB30_TX_CMC_P3
USB30_TX_CON_N6
USB30_TX_CON_P6
USB30_TX_CON_N3
USB30_TX_CON_P3
USB30_RX_CON_N6
USB30_RX_CON_P6
USB30_RX_CON_P3
USB30_RX_CON_N3
USB3.0 EMI
EC3802 SCD1U16V2KX-3GP
EC3803 SCD1U16V2KX-3GP
EC3801 SCD1U16V2KX-3GP
EC3804 SCD1U16V2KX-3GP
EL3803 FILTER-4P-98-GP (66.R0036.04L)
EL3801 FILTER-4P-98-GP (66.R0036.04L)
EL3804 FILTER-4P-98-GP (66.R0036.04L)
EL3806 FILTER-4P-98-GP (66.R0036.04L)
USB30_TX_CMC_N4
USB30_TX_CMC_P4
USB30_TX_CMC_N5
USB30_TX_CMC_P5
USB30_TX_CON_N4
USB30_TX_CON_P4
USB30_TX_CON_N5
USB30_TX_CON_P5
USB30_RX_CON_N4
USB30_RX_CON_P4
USB30_RX_CON_N5
USB30_RX_CON_P5
EMI
EL3802 MCM1012B900FBP-GP-U (66.R0036.04L)
USB_CON_PN1
USB_CON_PP1
EL3805 MCM1012B900FBP-GP-U (66.R0036.04L)
USB_CON_PN4
USB_CON_PP4
EMI
EL3808 MCM1012B900FBP-GP-U (66.R0036.04L)
USB_CON_PN2
USB_CON_PP2
EL3807 MCM1012B900FBP-GP-U (66.R0036.04L)
USB_CON_PN3
USB_CON_PP3
ESD
U3801 AZ1045-04F-R7G-GP
U3802 AZ1045-04F-R7G-GP
U3805 AZ1045-04F-R7G-GP
U3806 AZ1045-04F-R7G-GP
LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6
U3803 AZC099-04S-R7G-GP (075.00005.0B7C)
I/O1 GND I/O2 I/O4 VDD I/O3
5V_USB30P2
C3804 SCD1U16V2KX-3GP (R_)
U3804 AZC099-04S-R7G-GP (075.00005.0B7C)
5V_USB30P1
C3805 SCD1U16V2KX-3GP (R_)
USB3.0 REAR PORT1
5V_USB30P1
5V_USB30P2
TC9404 ST220U6D3VDM-20GP
TC9406 ST220U6D3VDM-20GP
USB3R1
VBUS#A1 VBUS#B1 VBUS#C1 VBUS#D1
D-#A2 D+#A3
STDA_SSRX-#A5 STDA_SSRX+#A6
STDA_SSTX-#A8 STDA_SSTX+#A9
D-#B2 D+#B3
STDA_SSRX-#B5 STDA_SSRX+#B6
STDA_SSTX-#B8 STDA_SSTX+#B9
D-#C2 D+#C3
STDA_SSRX-#C5 STDA_SSRX+#C6
STDA_SSTX-#C8 STDA_SSTX+#C9
D-#D2 D+#D3
STDA_SSRX-#D5 STDA_SSRX+#D6
STDA_SSTX-#D8 STDA_SSTX+#D9
GND
GND_DRAIN
G1 G2 G3 G4 G5 G6
SKT-USB42-GP
(022.10005.0F61)
22.10339.171
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Hsichih, Taipei Hsien
Title
USB30_REAR PORT
Size Custom
Document Number vHulk
Rev -1
Date: Wednesday, September 23, 2015
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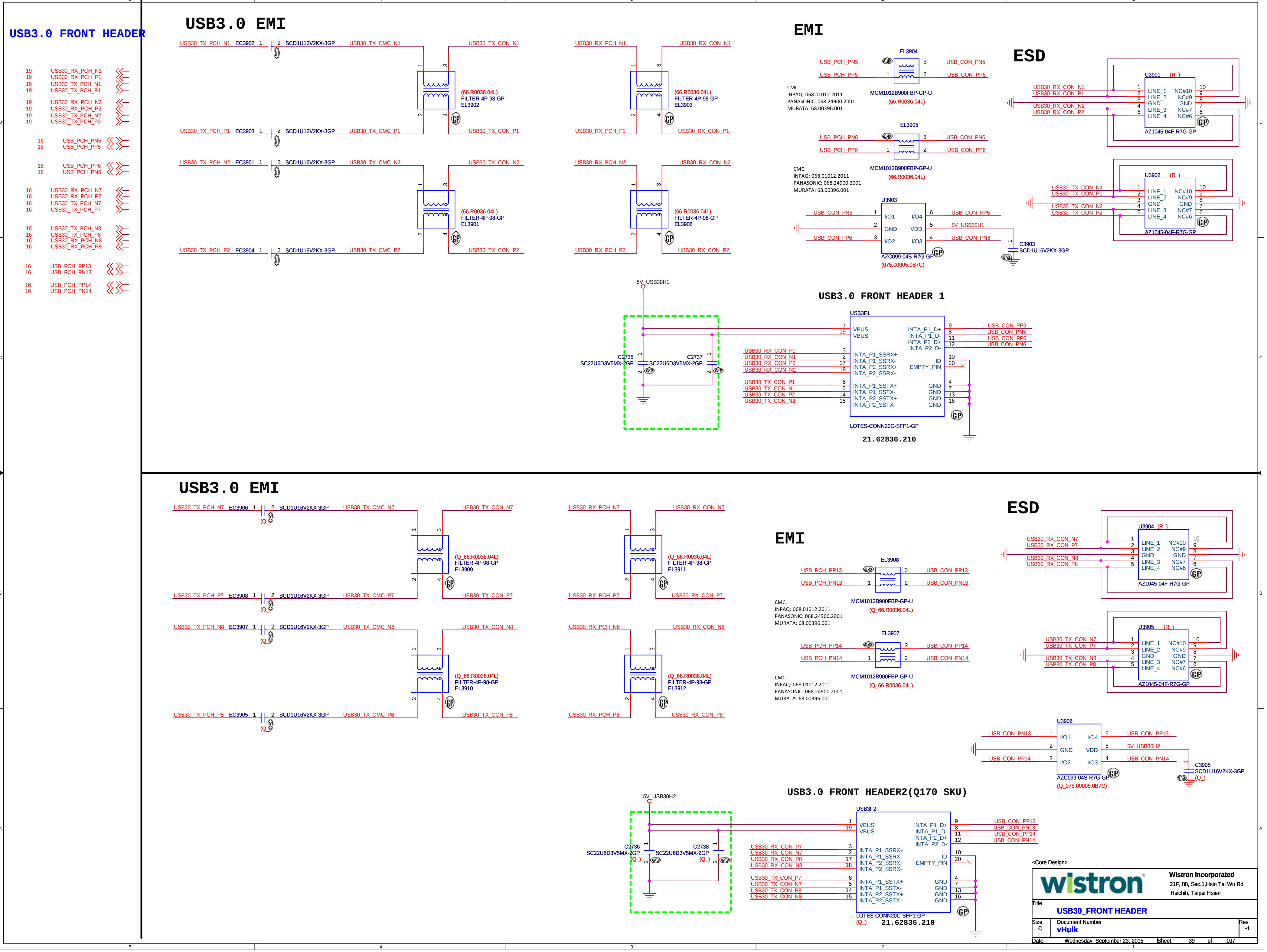

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Title	USB30_FRONT HEADER	
Size C	Document Number vHulk	Rev -1
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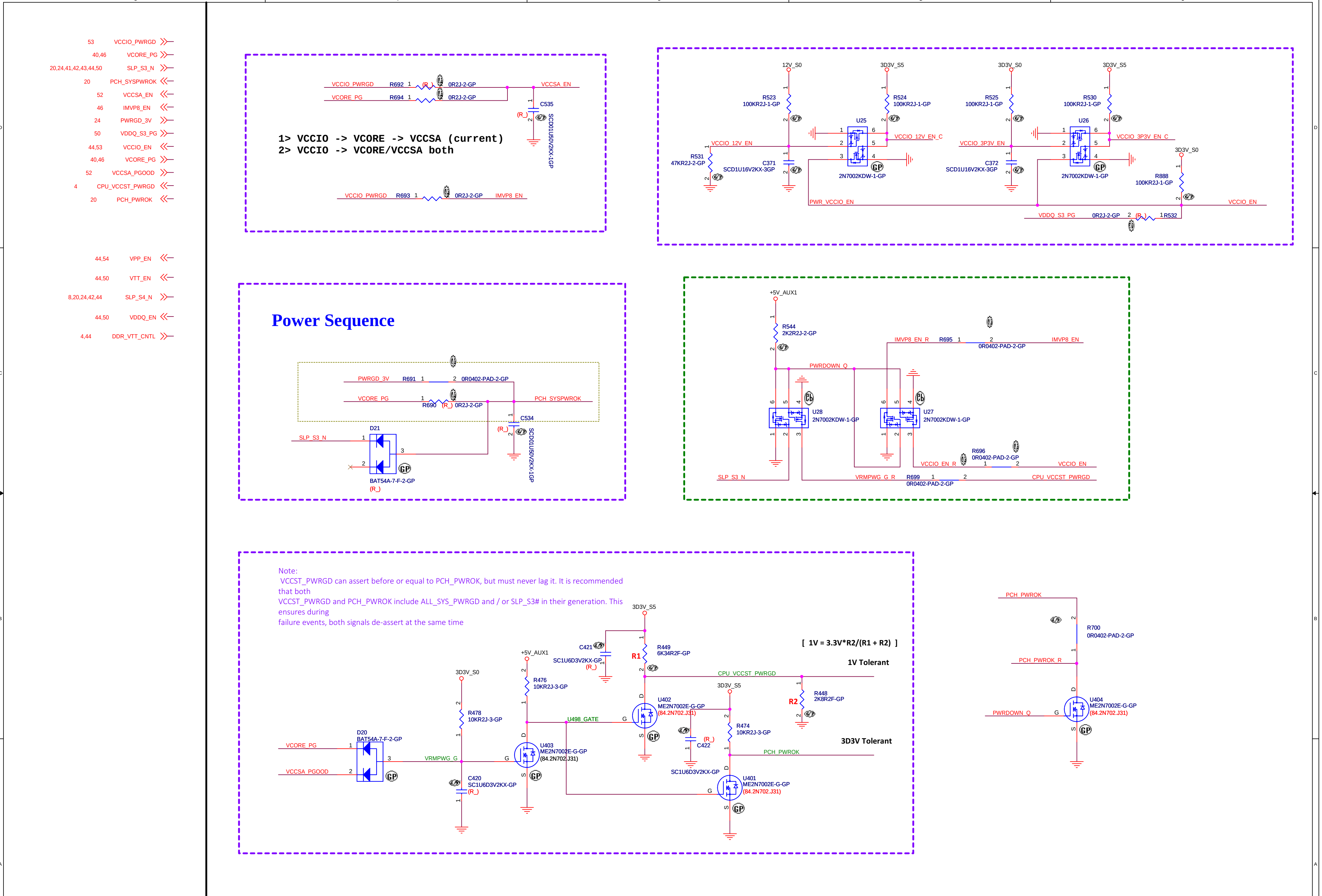

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Title	Power Plane EN Sequence	
Size: C	Document Number: vHulk	Rev: -1
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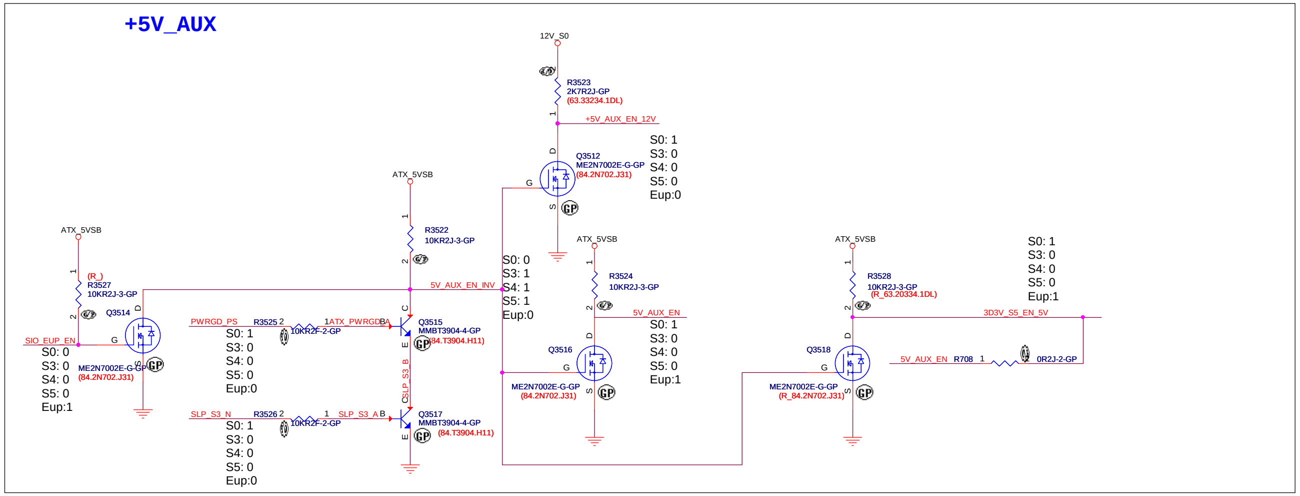
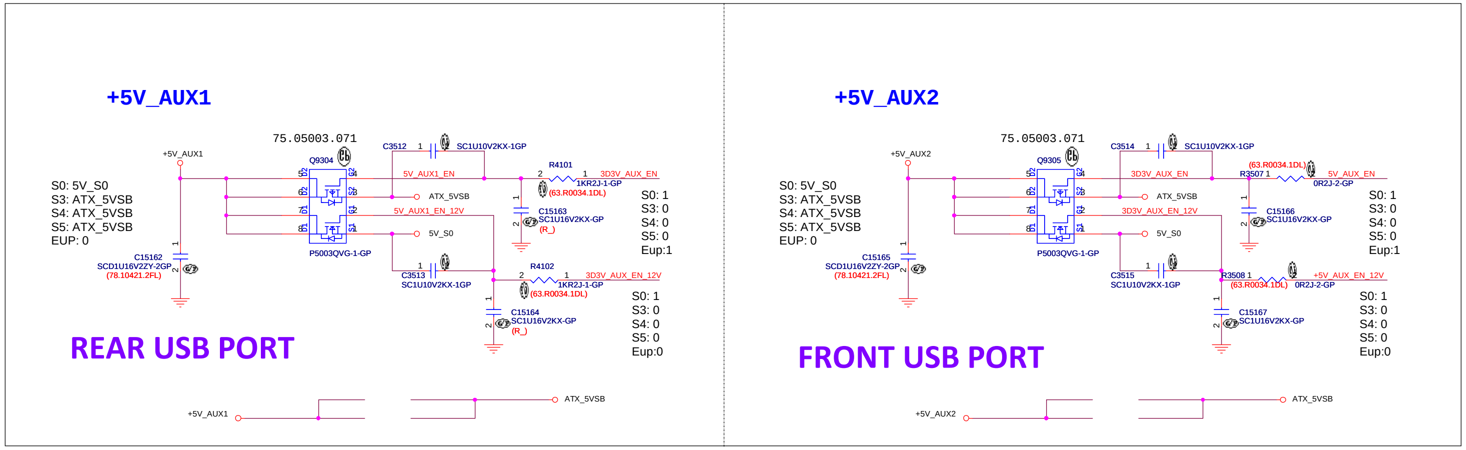
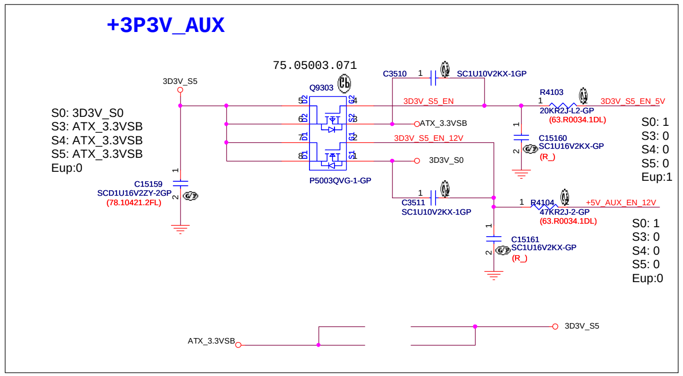
24 SIO_EUP_EN
20,24,40,42,43,44,50 SLP_S3_N
24,49 PWRGD_PS

Dual Power Control

GROUP A POWER(S5_EuP)







	SIO_EUP_EN	SLP_S3_N	+5V_AUX1	+5V_AUX2
S0	0	1	5V_S0	5V_S0
S3	0	0	ATX_5VSB	ATX_5VSB
S4	0	0	ATX_5VSB	ATX_5VSB
S5	0 (EUP Disable)	0	ATX_5VSB	ATX_5VSB
S5	1 (EUP Enable)	0	No Power	No Power

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Title: Dual Power

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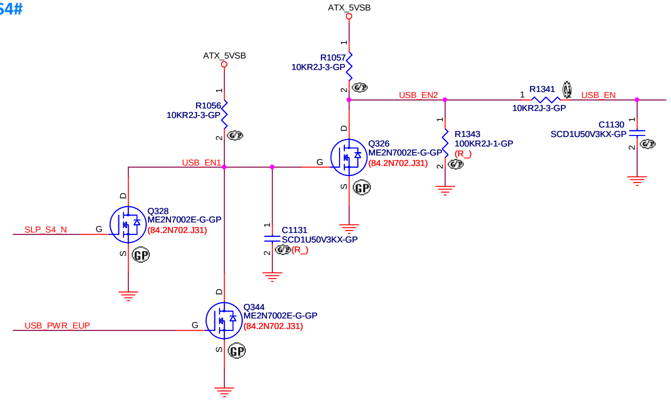
Date: Wednesday, September 23, 2015 | Sheet 41 of 107

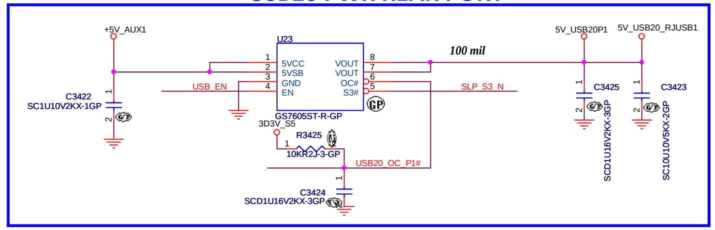
	S5	S4	S3-S0		S5	S4	S3-S0	Status
USB_PWR_SLP	L	L	L	USB_EN	L	L	H	No Support S4 USB wake up
USB_PWR_SLP	L	H	L	USB_EN	L	H	L	Support S4 USB wake up

8,20,24,44 SLP_S4_N
20 USB_PWR_EUP
16 USB30_OC_P1#
16 USB30_OC_P2#
16 USB30_OC_H1#
16 USB30_OC_H2#
16 USB20_OC_P2#
16 USB20_OC_P1#
20,24,40,41,43,44,50 SLP_S3_N

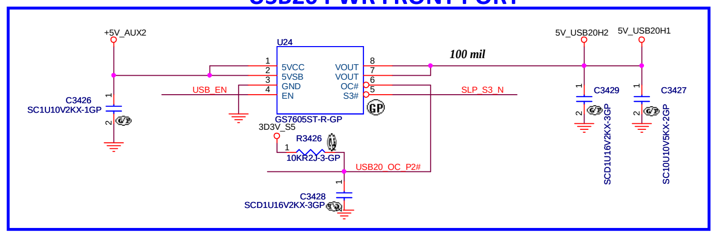
S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#



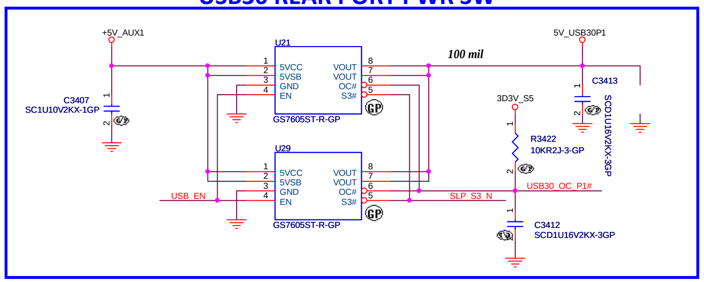
USB20 PWR REAR PORT



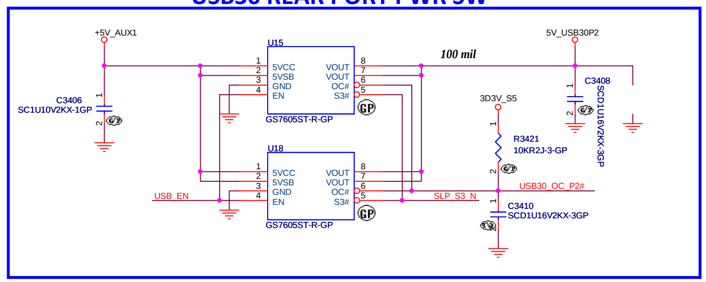
USB20 PWR FRONT PORT



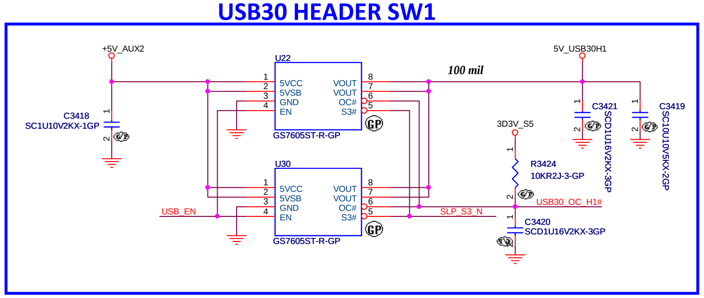
USB30 REAR PORT PWR SW



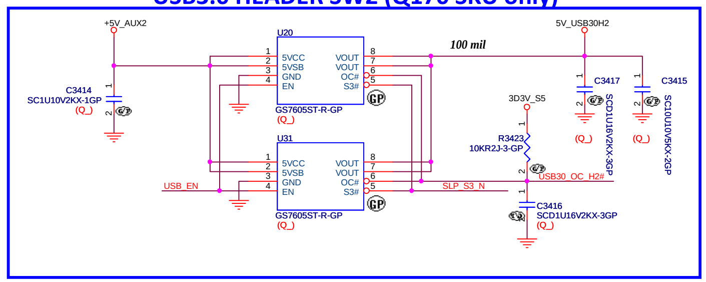
USB30 REAR PORT PWR SW

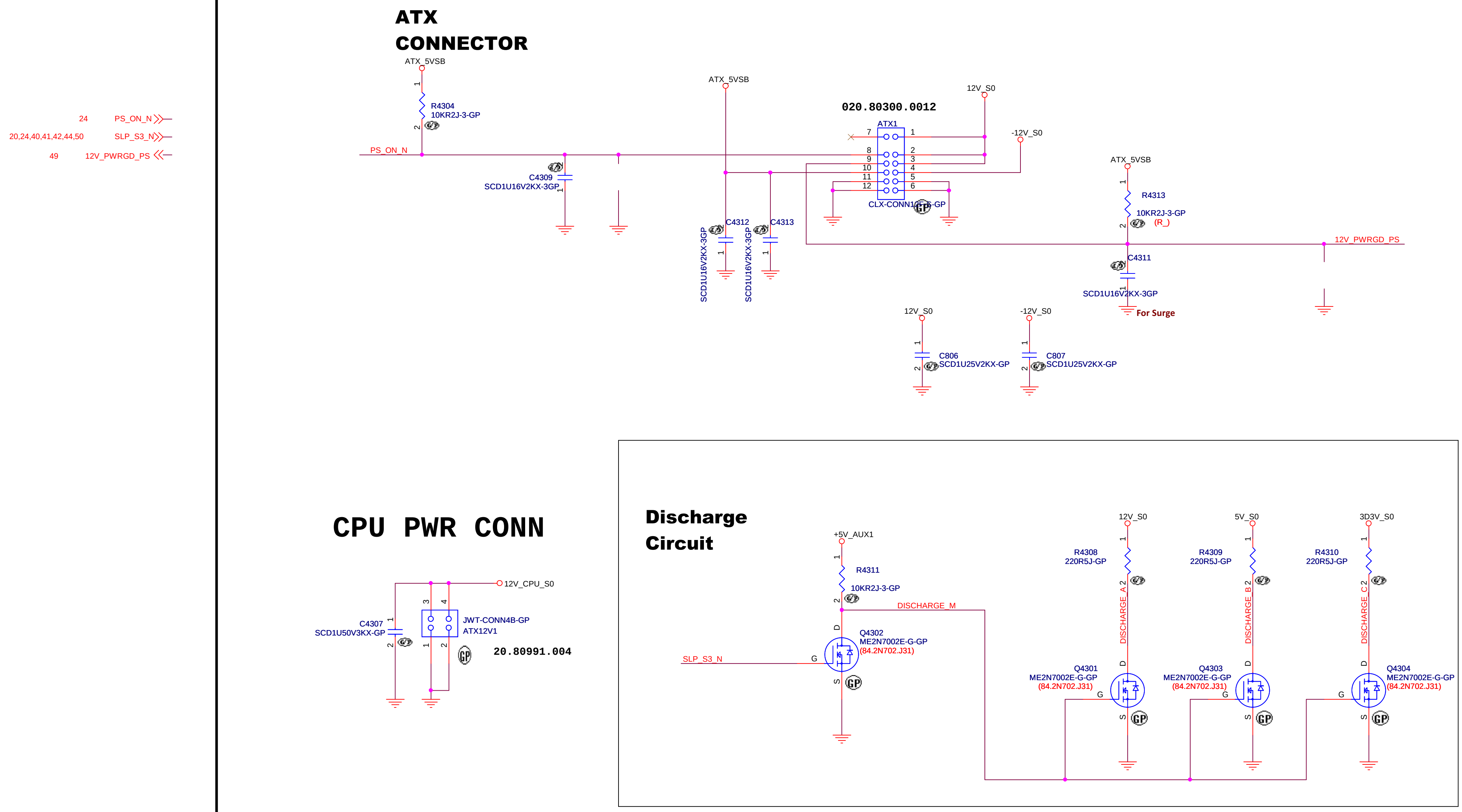


USB30 HEADER SW1



USB3.0 HEADER SW2 (Q170 SKU only)





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Title: ATX

Size: Custom | Document Number: vHulk | Rev: -1

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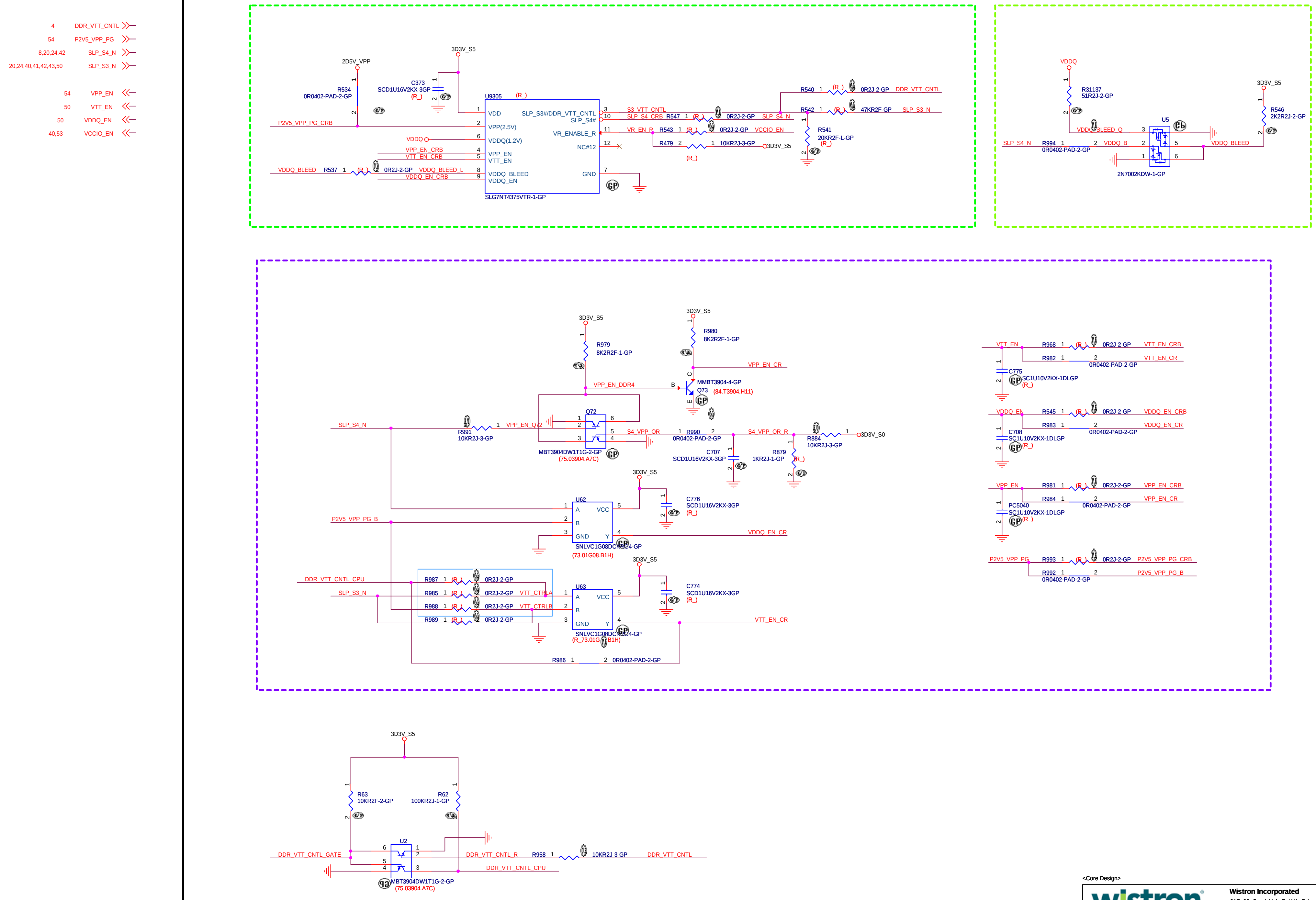

<Core Design>

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Title		
Power Sequence (DDR4)		
Size: C	Document Number: vHulk	Rev: -1
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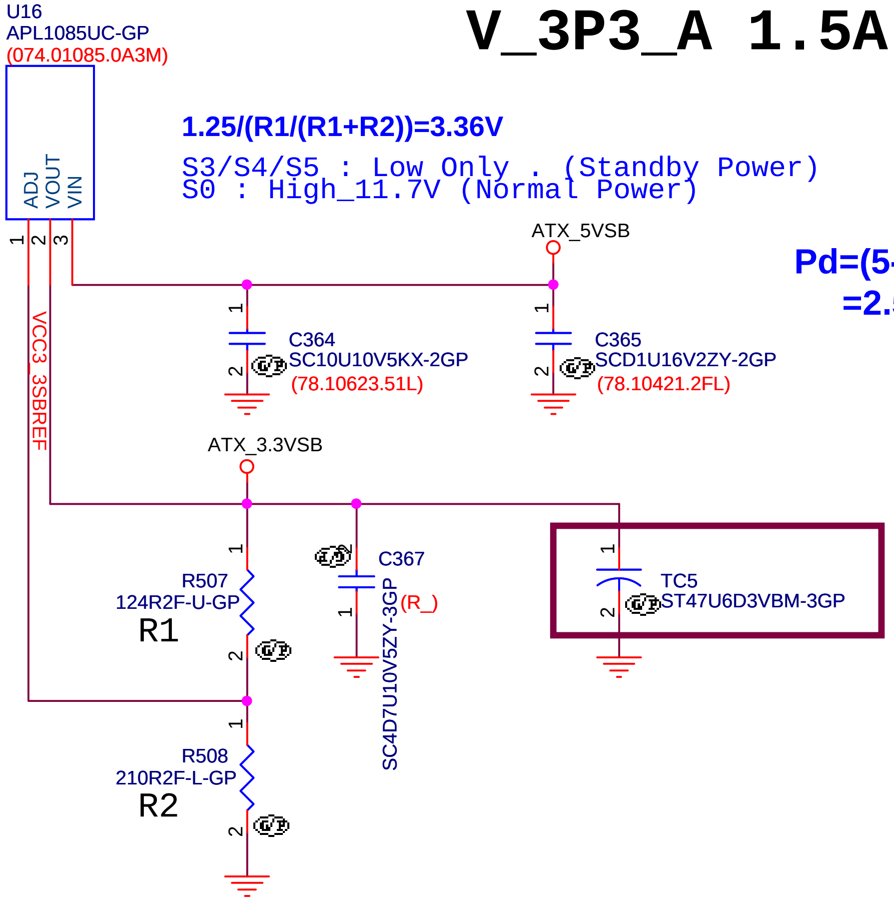
VCC5A/VCC3A

V_3P3_A 1.5A



Pd=(5-3.3)*1.5
=2.55W

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Title	DCDC-3D3V&5V		
Size A	Document Number vHulk		Rev -1
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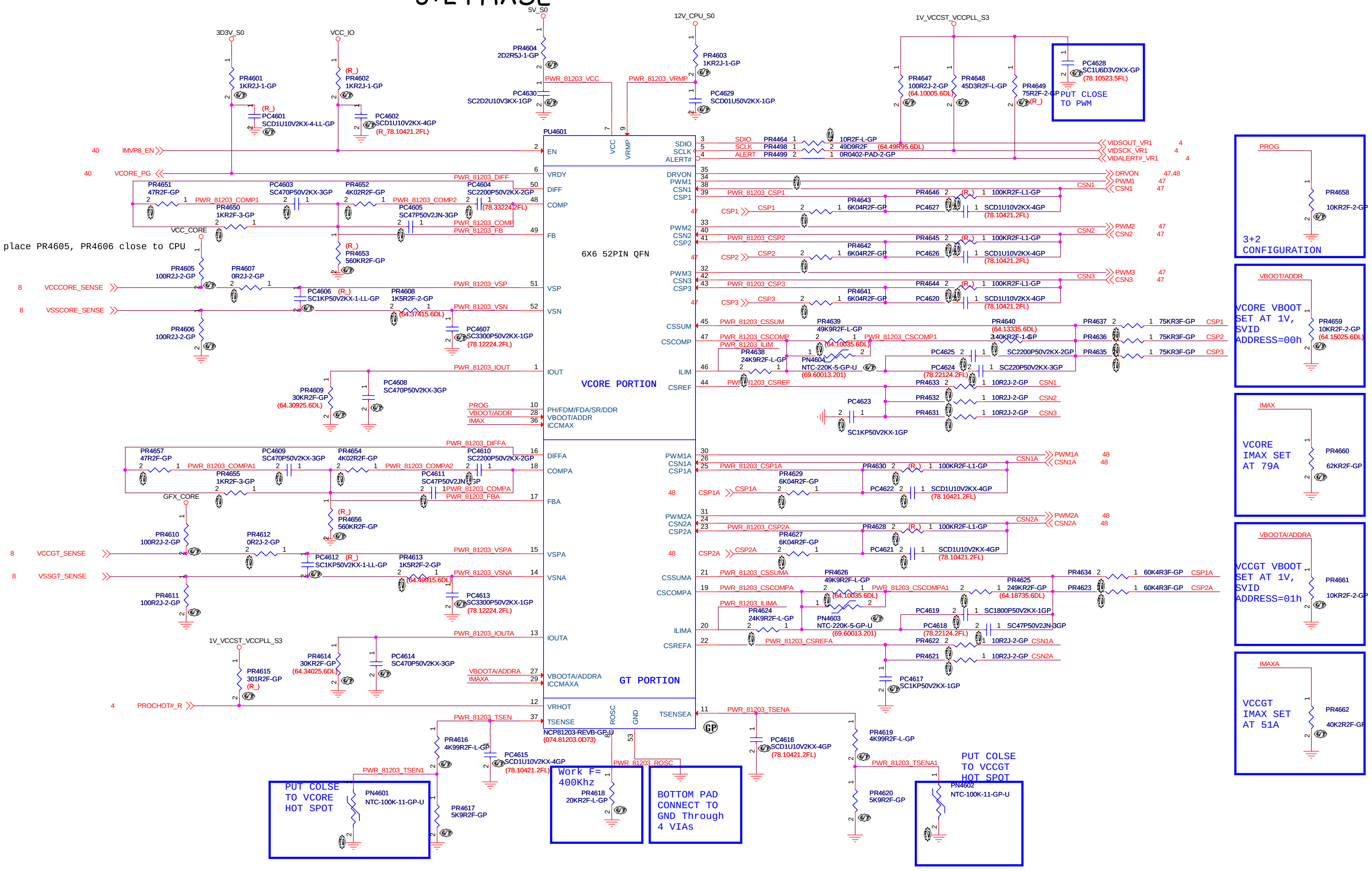
Intel SKYLAKE IMVP8 POWER CKT -
3+2 PHASE



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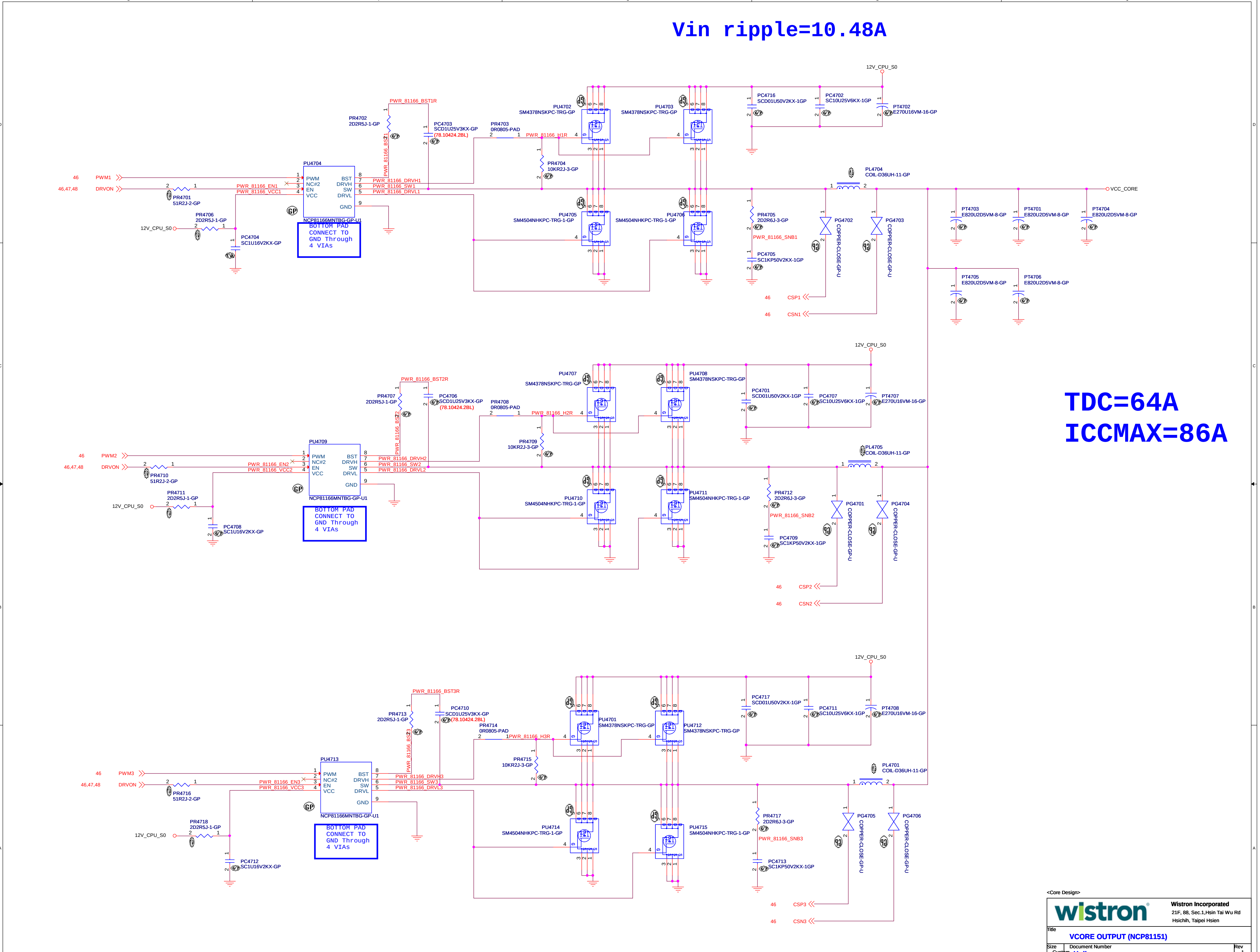
Title	VCORE & V_GT IC(NCP81203)	
Size Custom	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 46 of 107	



<Core Design>

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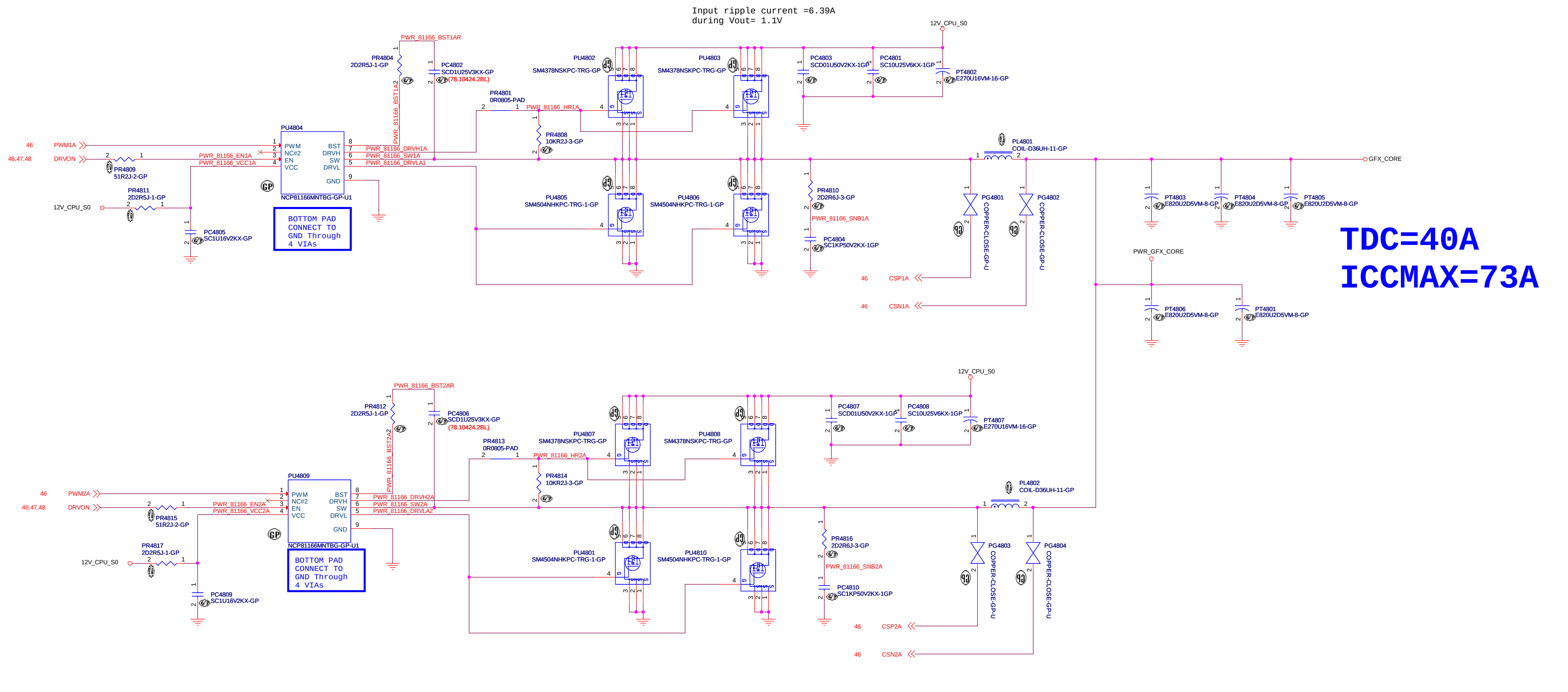
Title: VCORE OUTPUT (NCP81151)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 47 of 107



<Core Design>

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Title: V_GT OUTPUT(NCP81151)

Size: Custom | Document Number: vHulk | Rev: -1

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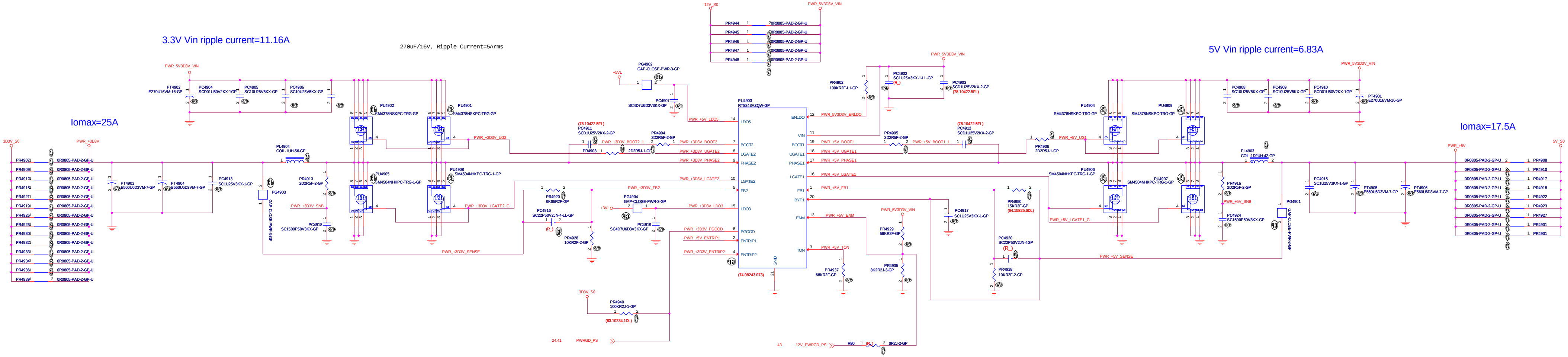
PWR_3D3V/PWR_5V



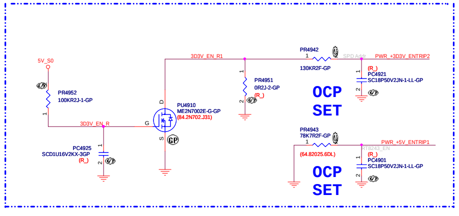


Table 2. Power Up Sequencing(RT8243A)							
ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

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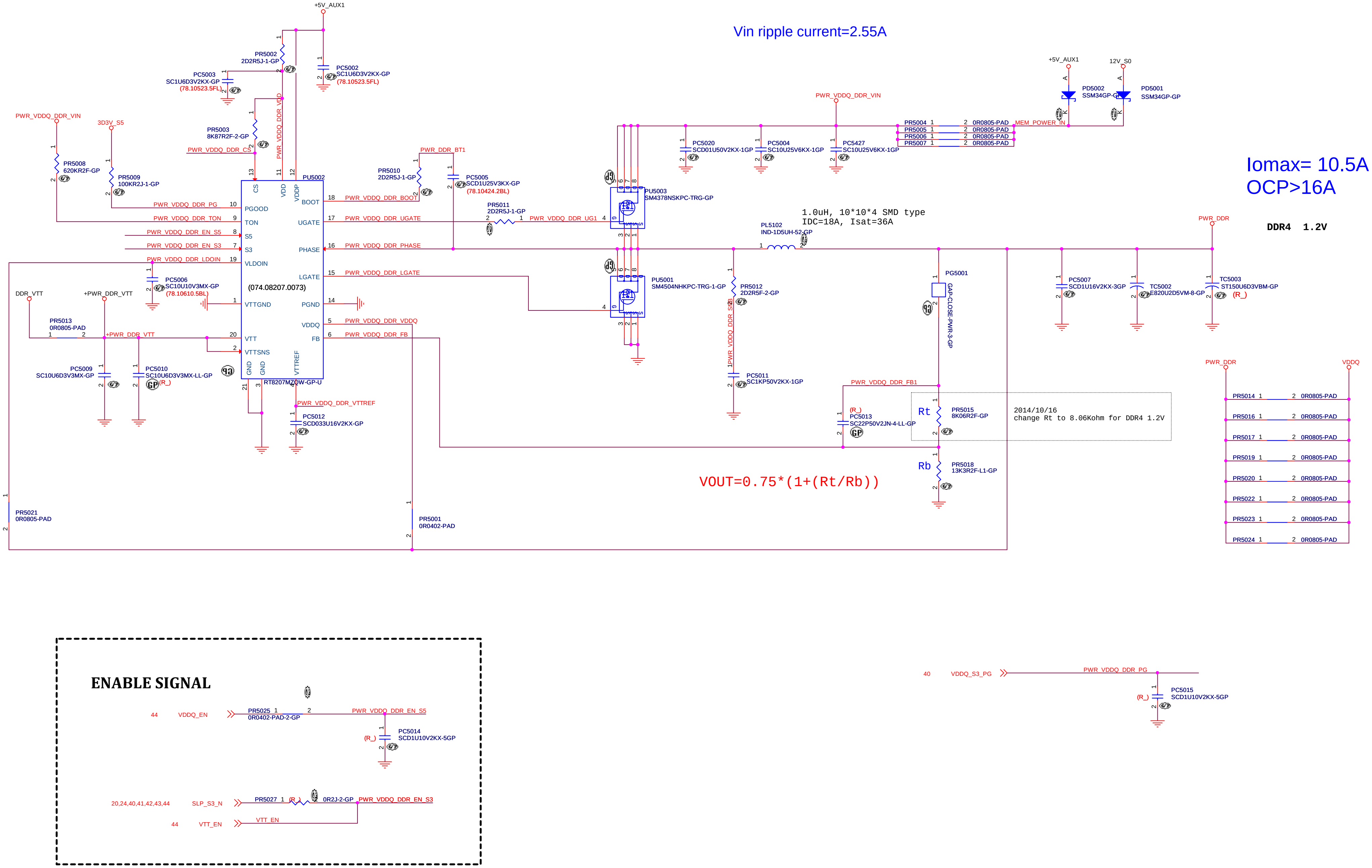
Title: 5V &3.3V(RT8243A)

Size: Custom | Document Number: vHulk | Rev: -1



<Core Design>

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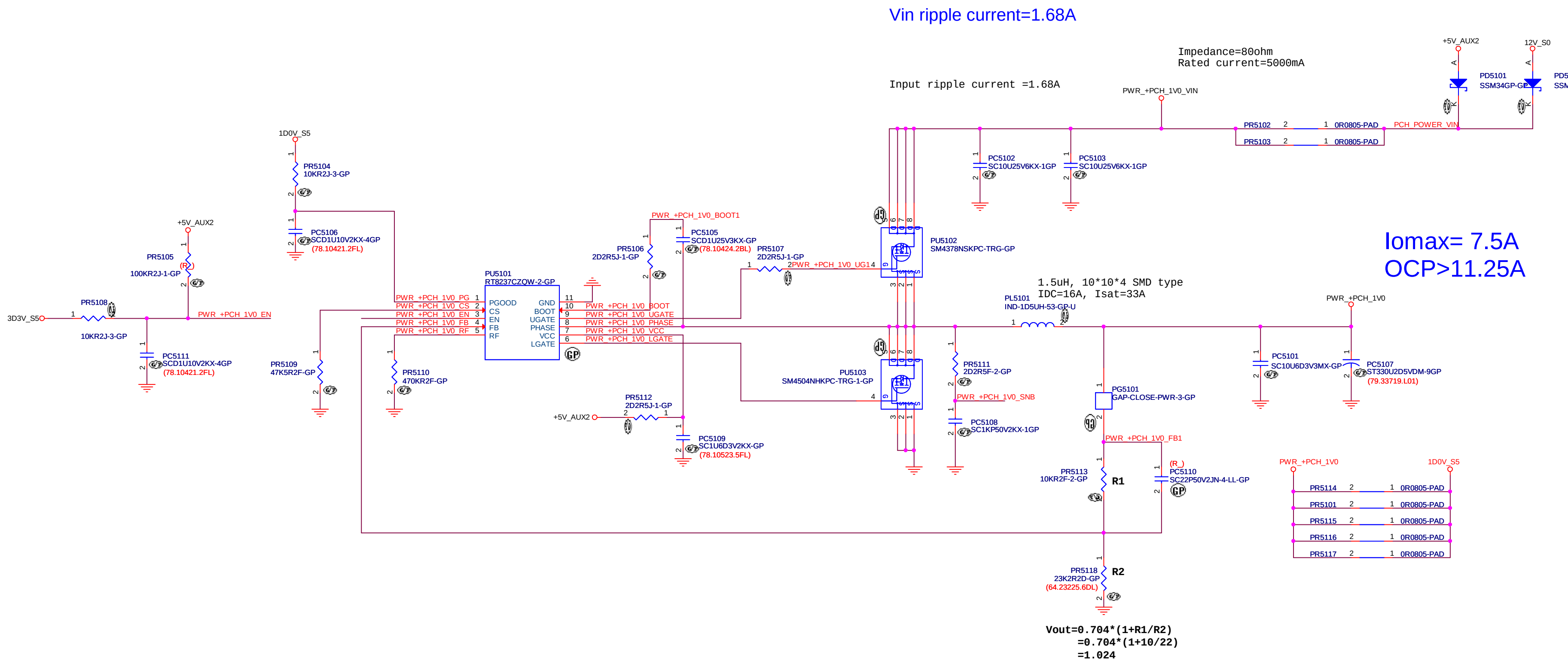
Title	DDR_PWR(RT8207M)	
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 50 of 107	



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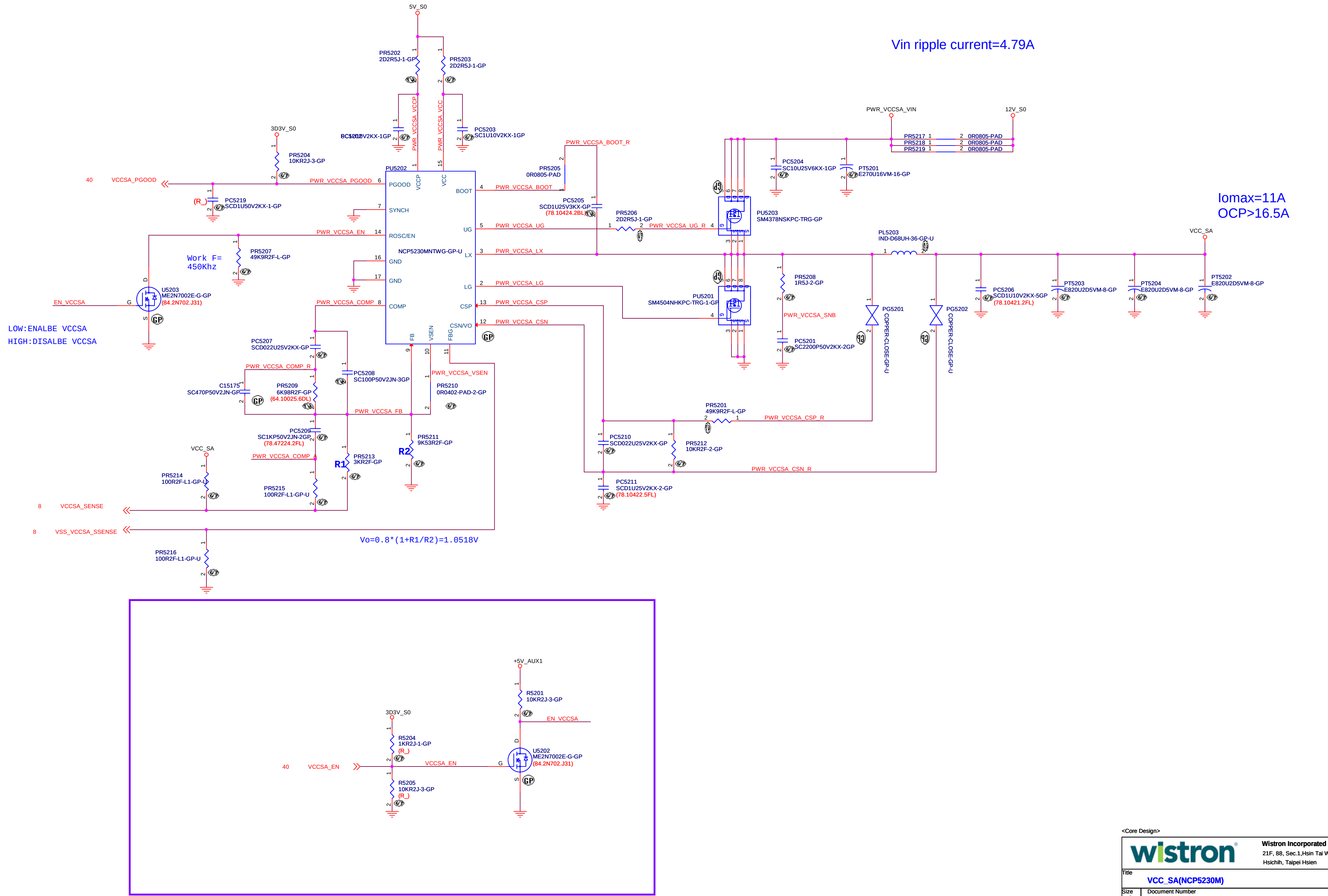
Title: **PCH_1P0V (RT8237C)**

Size	Document Number	Rev
Custom	vHulk	-1

Date: Wednesday, September 23, 2015 Sheet 51 of 107



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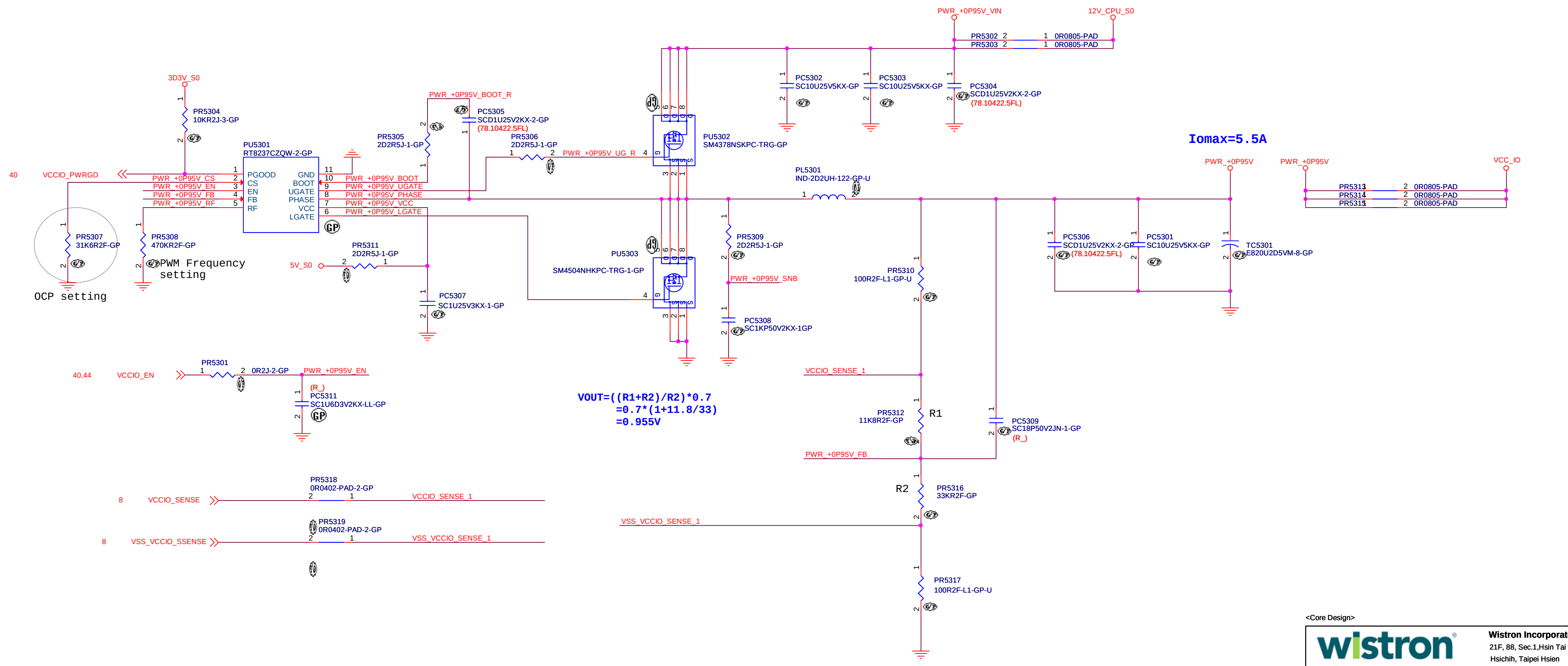
Title		
VCC_SA(NCP5230M)		
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 52 of 107	

VCCIO



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Title: VCC_IO(RT8237C)

Size: Custom | Document Number: vHulk | Rev: -1

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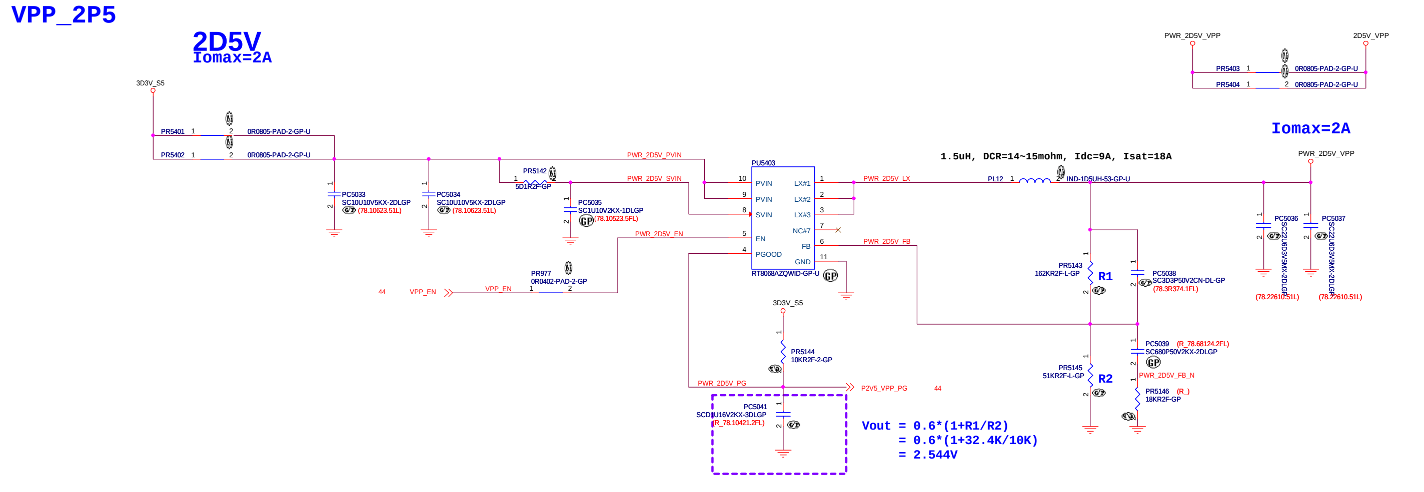
2014/8/26
Del 1D5V_S0



2014/8/26
Del 1D8V_S5

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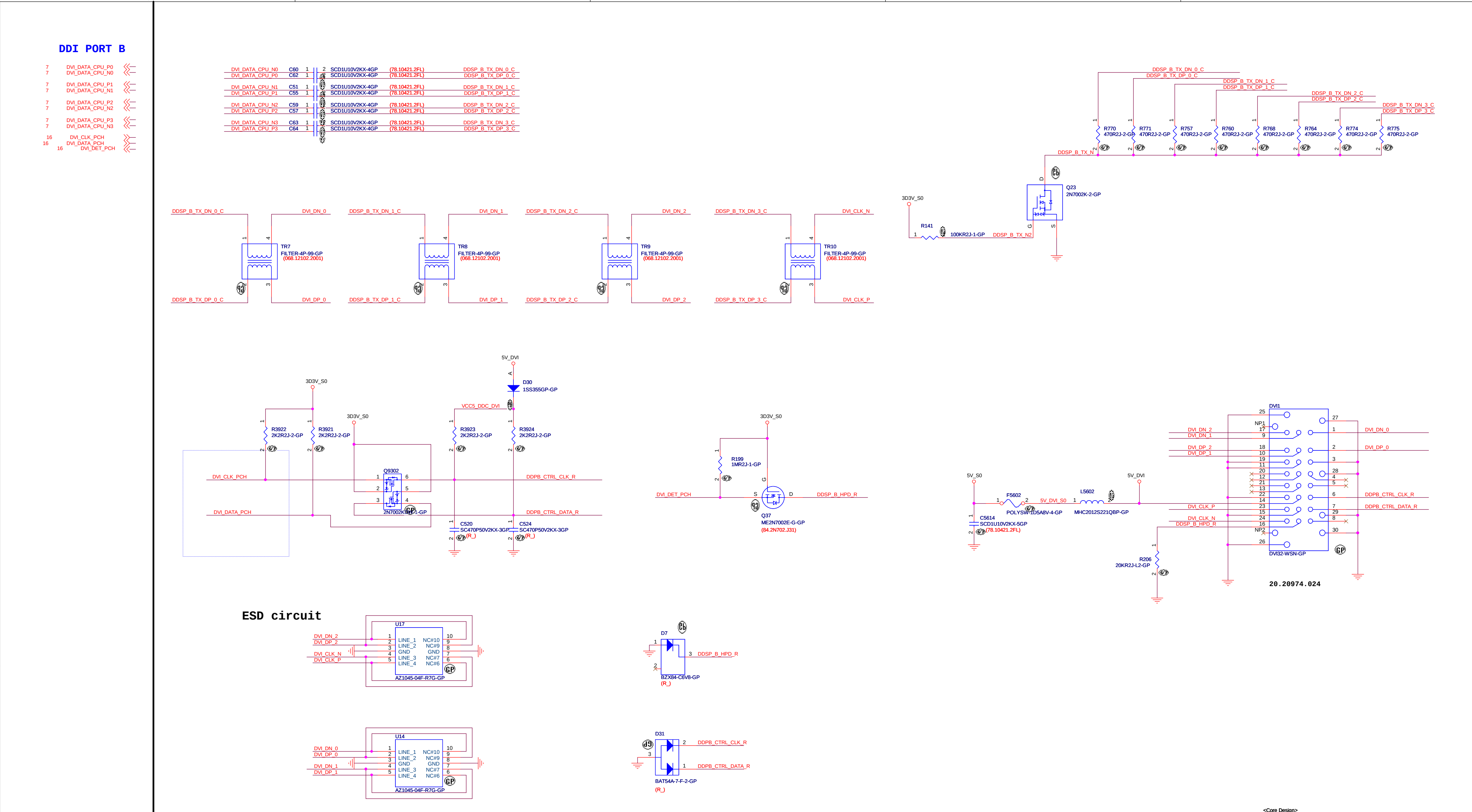
Title	LDO_3P3A_1P5V_1P8V	
Size: Custom	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 54 of 107	



<Core Design>

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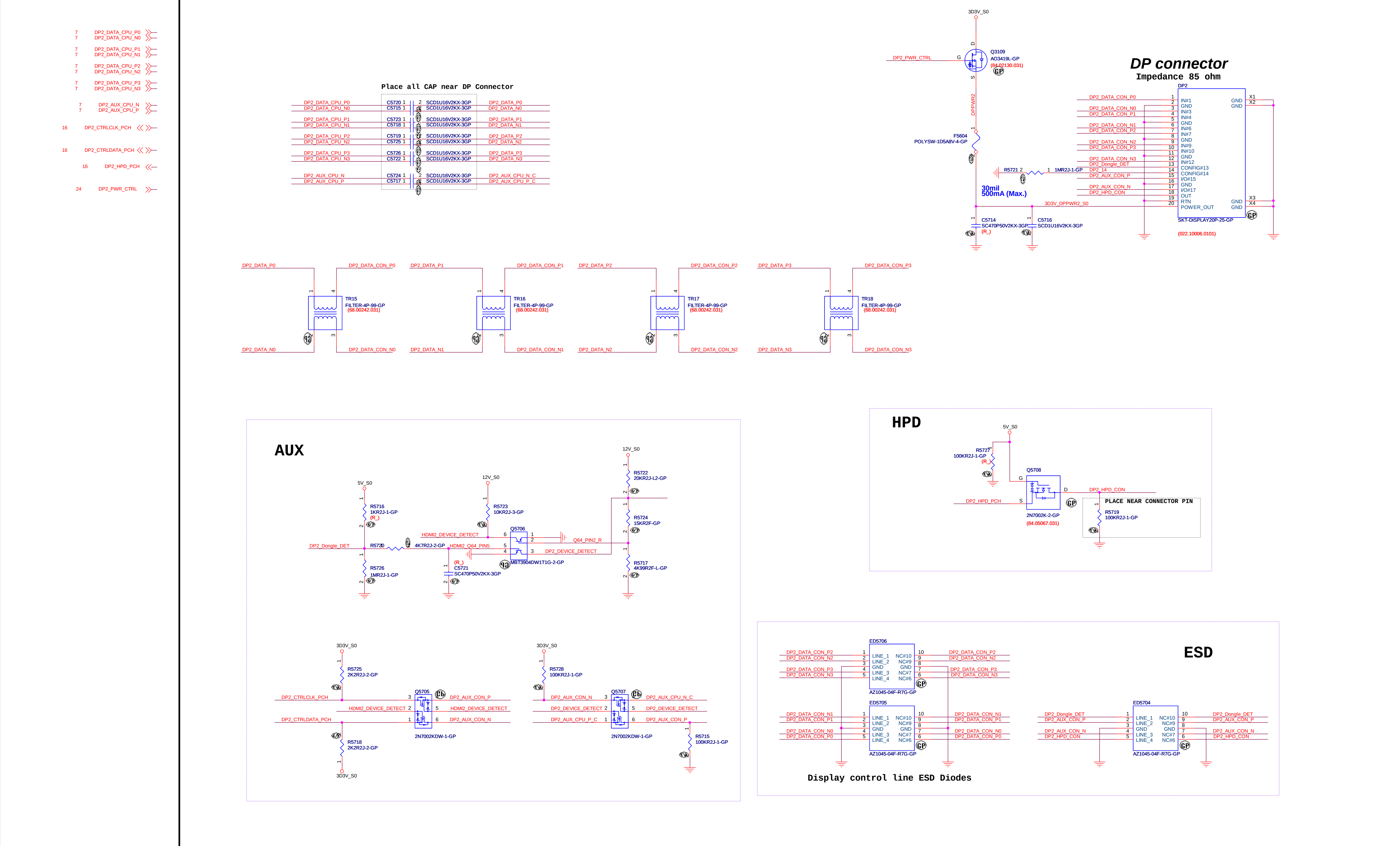
Title	DVI-D	
Size Custom	Document Number vHulk	Rev -1
Date: Wednesday, September 23, 2015	Sheet 55 of 107	



<Core Design>

Wistron Incorporated
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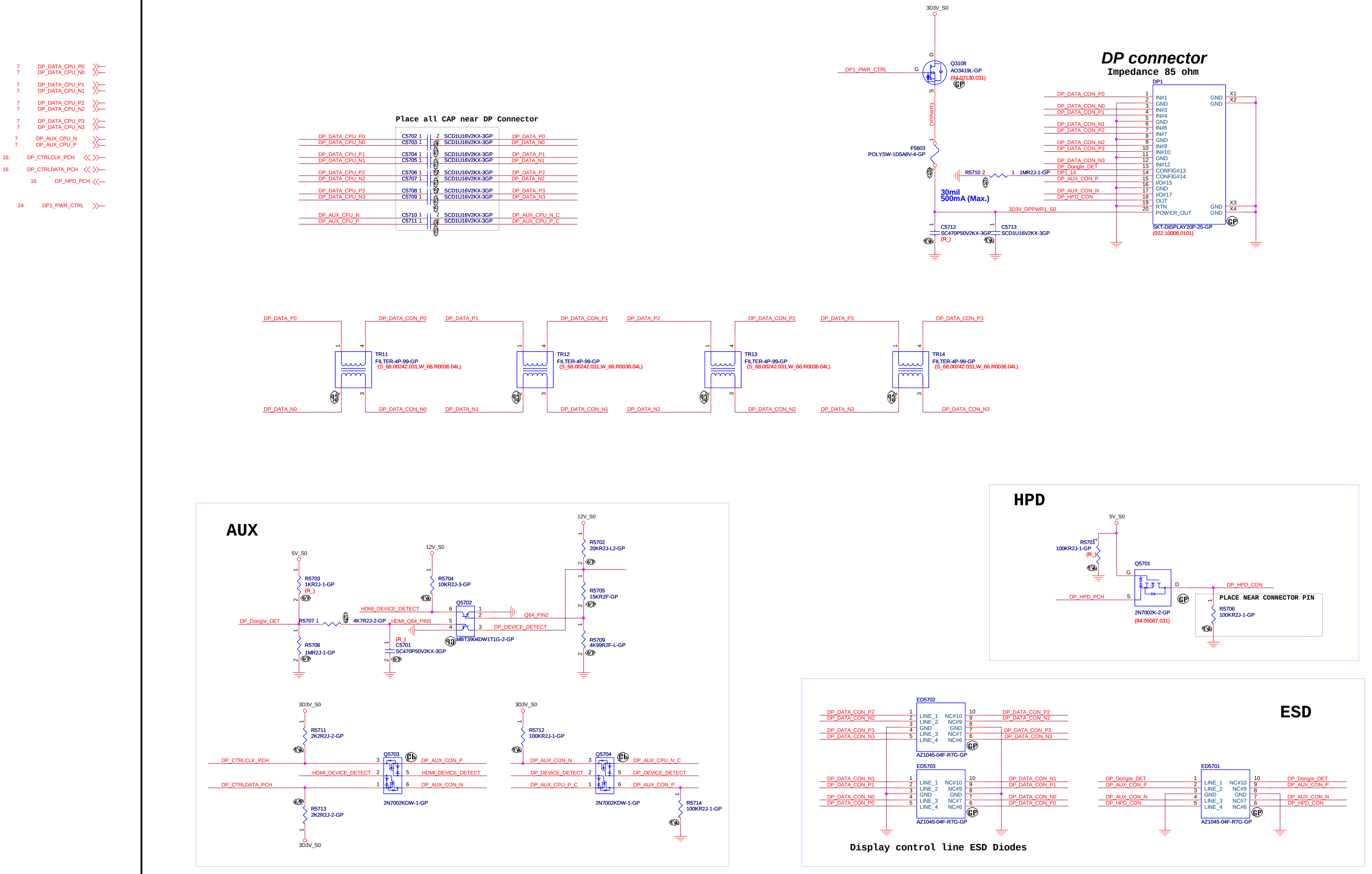
Hsichih, Taipei Hsien

Title	DP2		
Size: Custom	Document Number: vHulk		Rev: -1
Date: Wednesday, September 23, 2015	Sheet 56 of 107		



<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	DP1
Size: Custom	Document Number: vHulk
Rev	-1
Date:	Wednesday, September 23, 2015
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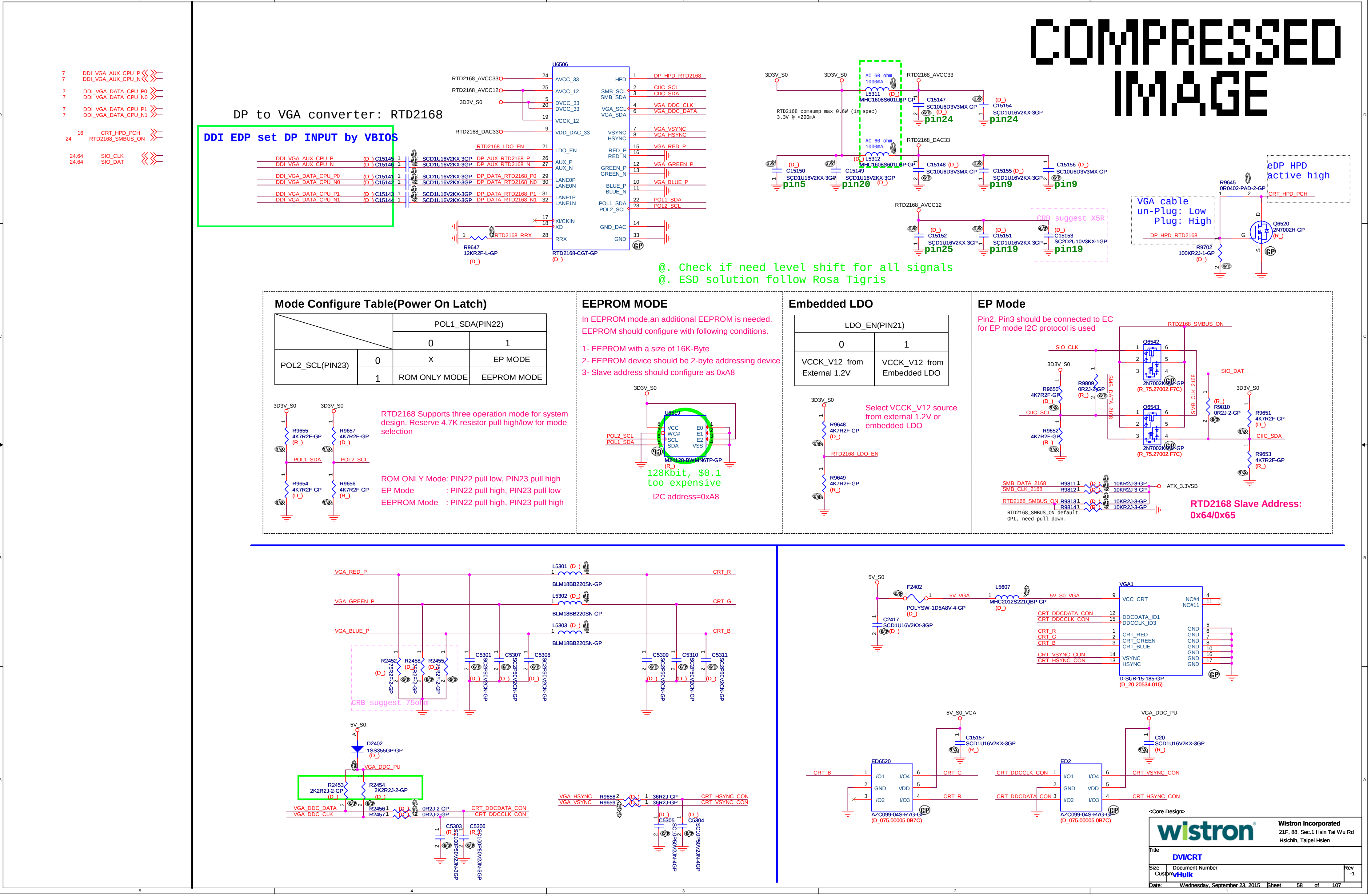

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

EEPROM MODE

In EEPROM mode,an additional EEPROM is needed. EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

EP Mode

<Core Design>
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Title: DVI/CRT
Size: Custom Document Number: vHulk Rev: -1
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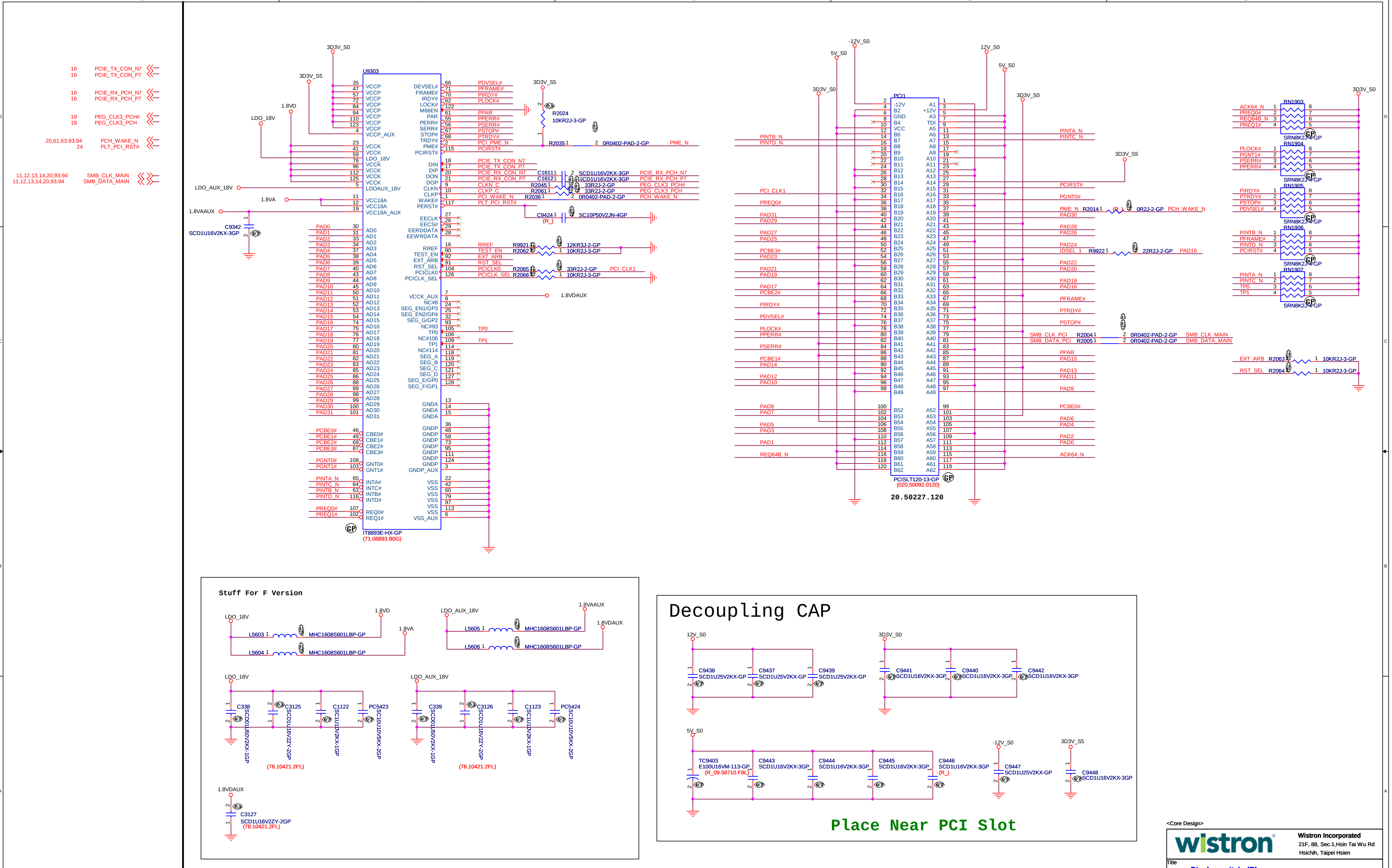

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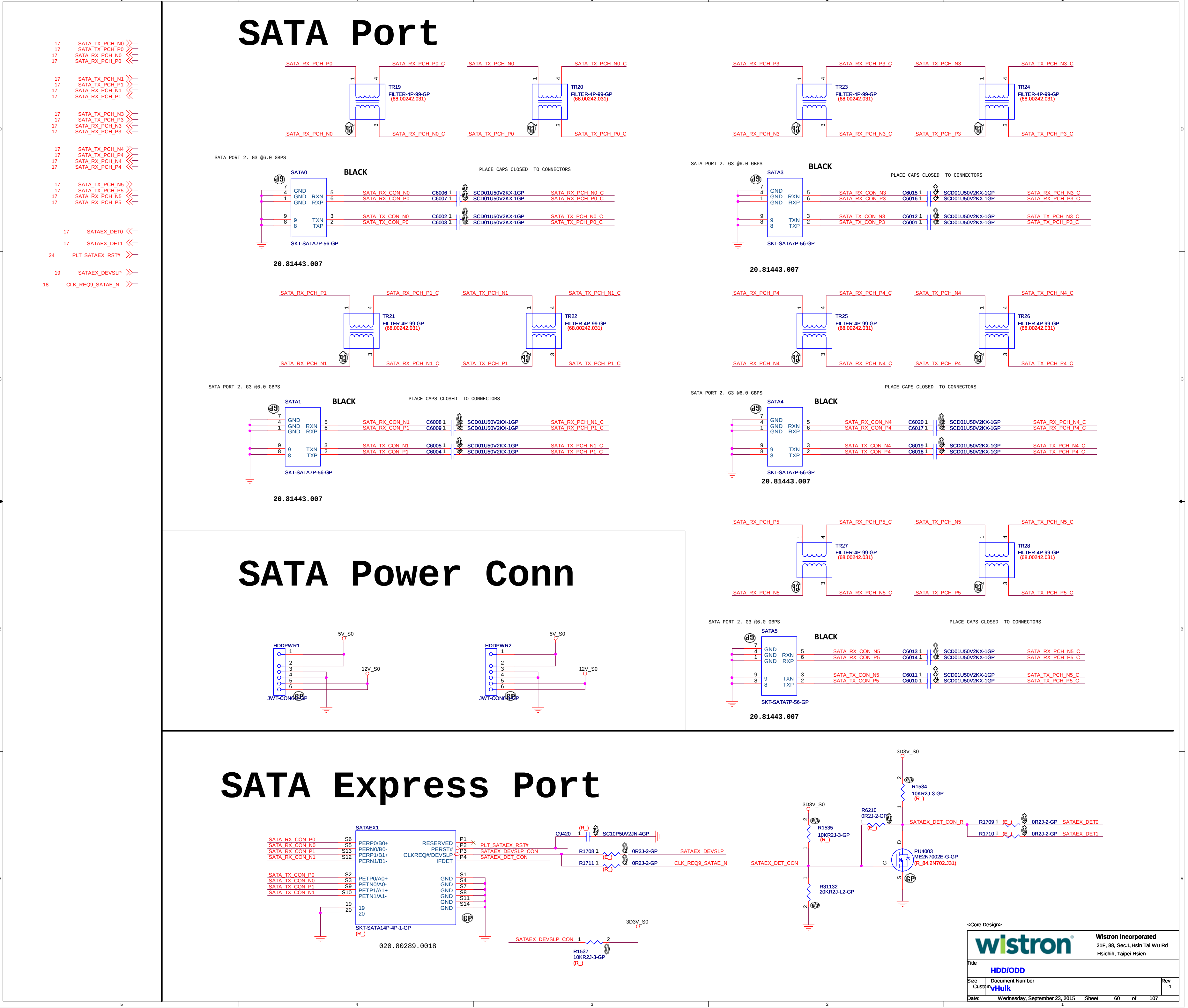
Title: Display switch_(R)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 59 of 107



SATA Port
17 SATA_TX_PCH_N0
17 SATA_TX_PCH_P0
17 SATA_RX_PCH_N0
17 SATA_RX_PCH_P0
17 SATA_TX_PCH_N1
17 SATA_TX_PCH_P1
17 SATA_RX_PCH_N1
17 SATA_RX_PCH_P1
17 SATA_TX_PCH_N3
17 SATA_TX_PCH_P3
17 SATA_RX_PCH_N3
17 SATA_RX_PCH_P3
17 SATA_TX_PCH_N4
17 SATA_TX_PCH_P4
17 SATA_RX_PCH_N4
17 SATA_RX_PCH_P4
17 SATA_TX_PCH_N5
17 SATA_TX_PCH_P5
17 SATA_RX_PCH_N5
17 SATA_RX_PCH_P5
17 SATAEX_DET0
17 SATAEX_DET1
24 PLT_SATAEX_RST#
19 SATAEX_DEVSLP
18 CLK_REQ9_SATAE_N
TR19 FILTER-4P-99-GP (68.00242.031)
TR20 FILTER-4P-99-GP (68.00242.031)
TR21 FILTER-4P-99-GP (68.00242.031)
TR22 FILTER-4P-99-GP (68.00242.031)
TR23 FILTER-4P-99-GP (68.00242.031)
TR24 FILTER-4P-99-GP (68.00242.031)
TR25 FILTER-4P-99-GP (68.00242.031)
TR26 FILTER-4P-99-GP (68.00242.031)
TR27 FILTER-4P-99-GP (68.00242.031)
TR28 FILTER-4P-99-GP (68.00242.031)
SATA PORT 2. G3 @6.0 GBPS
BLACK
PLACE CAPS CLOSED TO CONNECTORS
SATA0
SATA1
SATA3
SATA4
SATA5
SKT-SATA7P-56-GP
SCD01U50V2KX-1GP
20.81443.007
SATA Power Conn
HDDPWR1
HDDPWR2
5V_S0
12V_S0
SATA Express Port
SATAEX1
SKT-SATA14P-4P-1-GP
020.80289.0018
PERP0/B0+
PERN0/B0-
PERP1/B1+
PERN1/B1-
PETP0/A0+
PETN0/A0-
PETP1/A1+
PETN1/A1-
RESERVED
PERST#
CLKREQ#/DEVSLP
IFDET
C9420 SC10P50V2JN-4GP
R1708 0R2J-2-GP
R1711 0R2J-2-GP
R1537 10KR2J-3-GP
3D3V_S0
R1534 10KR2J-3-GP
R1535 10KR2J-3-GP
R6210 0R2J-2-GP
R31132 20KR2J-L2-GP
PU4003 ME2N7002E-G-GP (R_84.2N702.J31)
R1709 0R2J-2-GP SATAEX_DET0
R1710 0R2J-2-GP SATAEX_DET1
SATAEX_DET_CON
SATAEX_DET_CON_R
SATAEX_DEVSLP_CON
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Title
HDD/ODD
Size Custom
Document Number
vHulk
Rev -1
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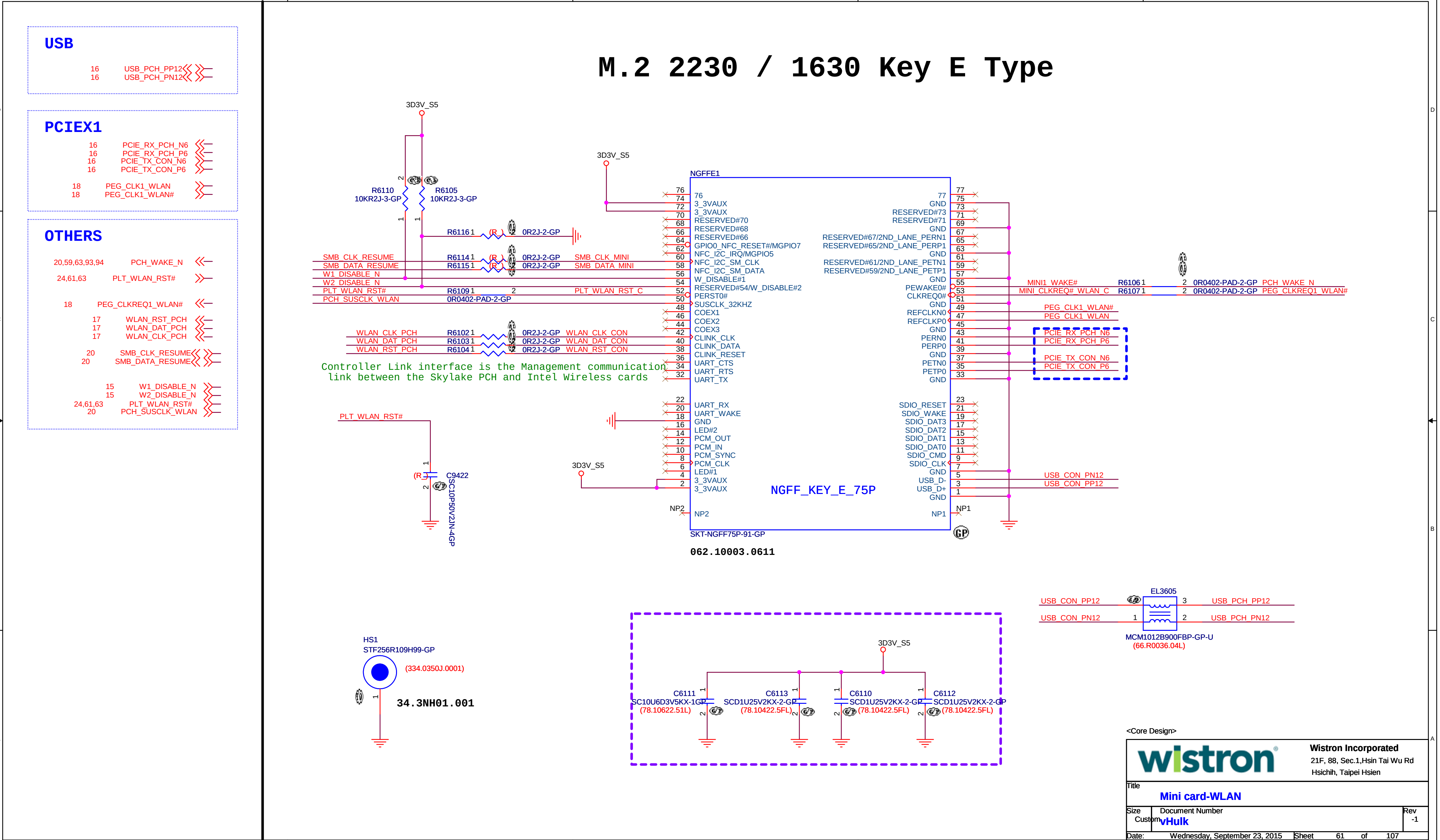
M.2 2230 / 1630 Key E Type
USB
16 USB_PCH_PP12
16 USB_PCH_PN12
PCIEX1
16 PCIE_RX_PCH_N6
16 PCIE_RX_PCH_P6
16 PCIE_TX_CON_N6
16 PCIE_TX_CON_P6
18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#
OTHERS
20,59,63,93,94 PCH_WAKE_N
24,61,63 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH
20 SMB_CLK_RESUME
20 SMB_DATA_RESUME
15 W1_DISABLE_N
15 W2_DISABLE_N
24,61,63 PLT_WLAN_RST#
20 PCH_SUSCLK_WLAN
3D3V_S5
R6110 10KR2J-3-GP
R6105 10KR2J-3-GP
R6116 0R2J-2-GP
R6114 0R2J-2-GP SMB_CLK_MINI
R6115 0R2J-2-GP SMB_DATA_MINI
R6109 PLT_WLAN_RST_C
0R0402-PAD-2-GP
SMB_CLK_RESUME
SMB_DATA_RESUME
W1_DISABLE_N
W2_DISABLE_N
PLT_WLAN_RST#
PCH_SUSCLK_WLAN
WLAN_CLK_PCH R6102 0R2J-2-GP WLAN_CLK_CON
WLAN_DAT_PCH R6103 0R2J-2-GP WLAN_DAT_CON
WLAN_RST_PCH R6104 0R2J-2-GP WLAN_RST_CON
Controller Link interface is the Management communication
link between the Skylake PCH and Intel Wireless cards
PLT_WLAN_RST#
C9422 SC10P50V2JN-4GP
NGFFE1
3_3VAUX
RESERVED#70
RESERVED#68
RESERVED#66
GPIO0_NFC_RESET#/MGPIO7
NFC_I2C_IRQ/MGPIO5
NFC_I2C_SM_CLK
NFC_I2C_SM_DATA
W_DISABLE#1
RESERVED#54/W_DISABLE#2
PERST0#
SUSCLK_32KHZ
COEX1
COEX2
COEX3
CLINK_CLK
CLINK_DATA
CLINK_RESET
UART_CTS
UART_RTS
UART_TX
UART_RX
UART_WAKE
GND
LED#2
PCM_OUT
PCM_IN
PCM_SYNC
PCM_CLK
LED#1
NP2
RESERVED#73
RESERVED#71
RESERVED#67/2ND_LANE_PERN1
RESERVED#65/2ND_LANE_PERP1
RESERVED#61/2ND_LANE_PETN1
RESERVED#59/2ND_LANE_PETP1
PEWAKE0#
CLKREQ0#
REFCLKN0
REFCLKP0
PERN0
PERP0
PETN0
PETP0
SDIO_RESET
SDIO_WAKE
SDIO_DAT3
SDIO_DAT2
SDIO_DAT1
SDIO_DAT0
SDIO_CMD
SDIO_CLK
USB_D-
USB_D+
NP1
NGFF_KEY_E_75P
SKT-NGFF75P-91-GP
062.10003.0611
MINI1_WAKE# R6106 0R0402-PAD-2-GP PCH_WAKE_N
MINI_CLKREQ#_WLAN_C R6107 0R0402-PAD-2-GP PEG_CLKREQ1_WLAN#
PEG_CLK1_WLAN#
PEG_CLK1_WLAN
PCIE_RX_PCH_N6
PCIE_RX_PCH_P6
PCIE_TX_CON_N6
PCIE_TX_CON_P6
USB_CON_PN12
USB_CON_PP12
EL3605
USB_CON_PP12 USB_PCH_PP12
USB_CON_PN12 USB_PCH_PN12
MCM1012B900FBP-GP-U
(66.R0036.04L)
HS1
STF256R109H99-GP
(334.0350J.0001)
34.3NH01.001
C6111 SC10U6D3V5KX-1GP (78.10622.51L)
C6113 SCD1U25V2KX-2-GP (78.10422.5FL)
C6110 SCD1U25V2KX-2-GP (78.10422.5FL)
C6112 SCD1U25V2KX-2-GP (78.10422.5FL)
<Core Design>
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Title
Mini card-WLAN
Size Custom
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Title	Mini card-SSD_(R)	
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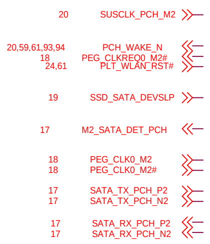
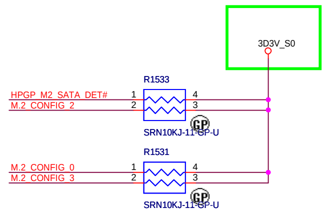
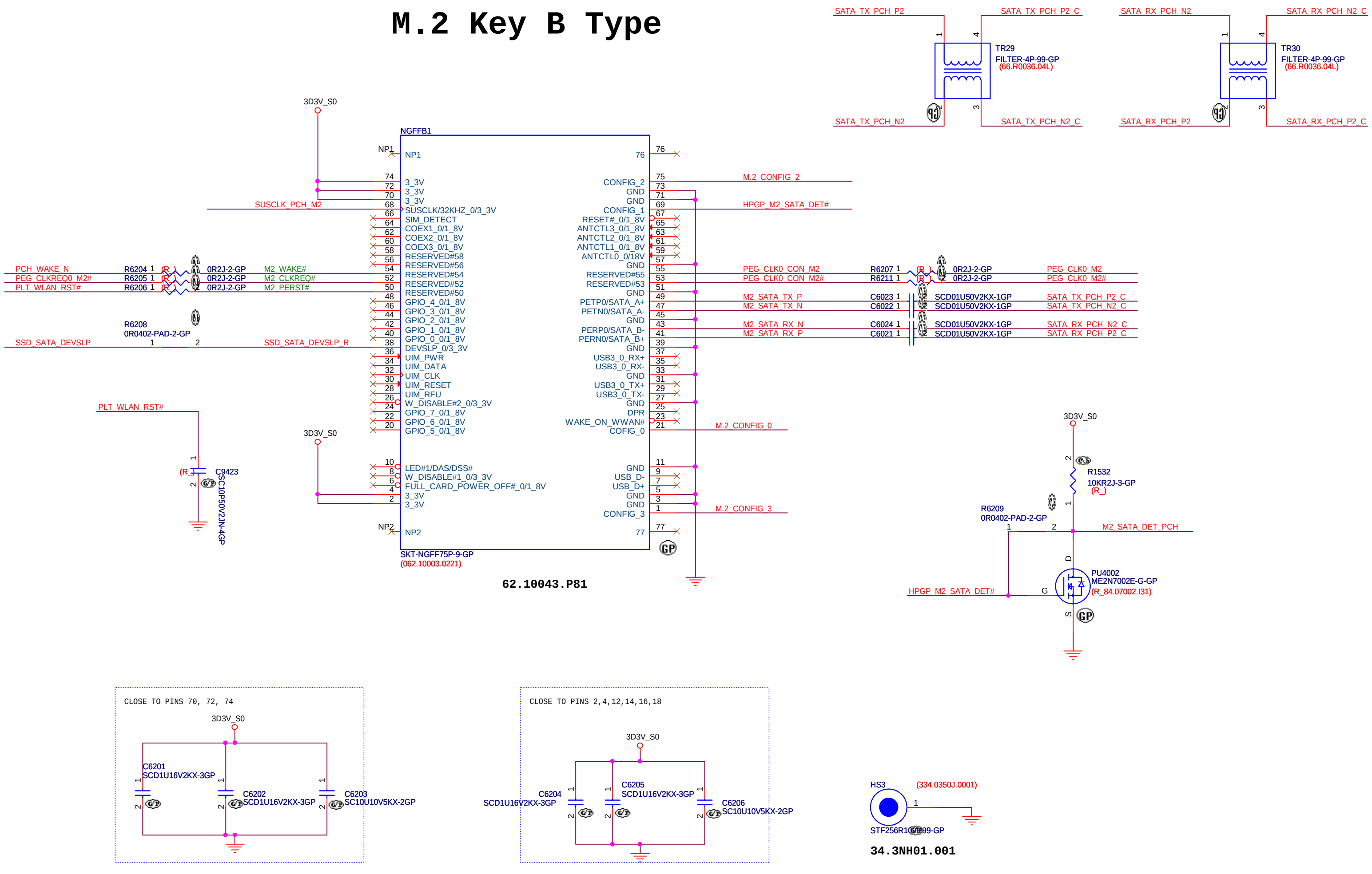


Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A



M.2 Key B Type



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Title: Mini card-NGFF		
Size: C	Document Number: vHulk	Rev: -1
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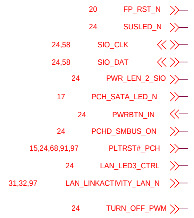
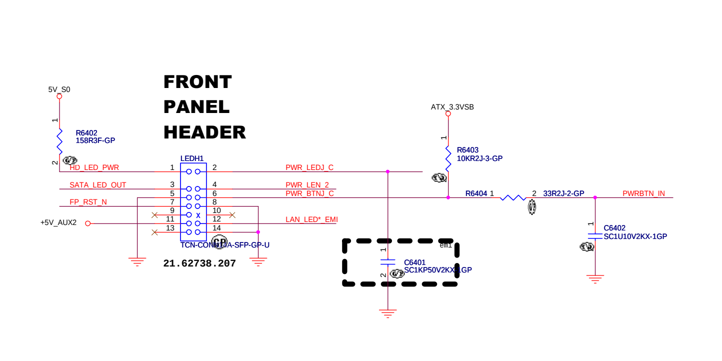
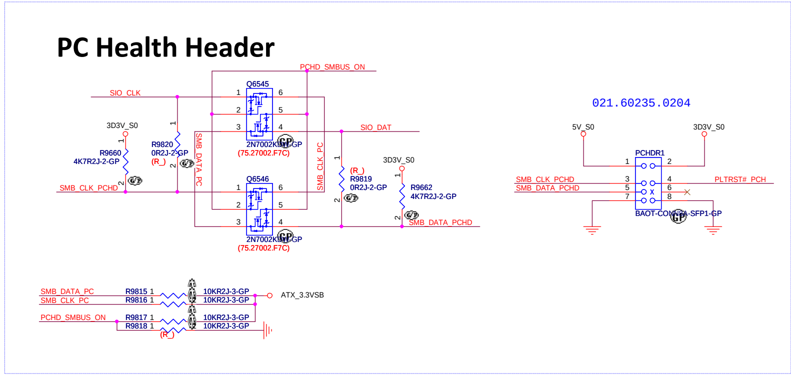
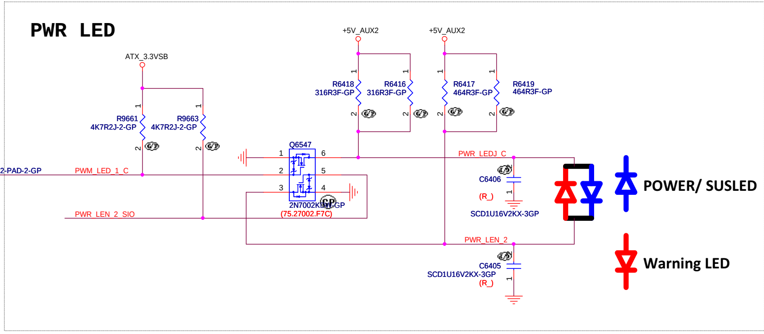


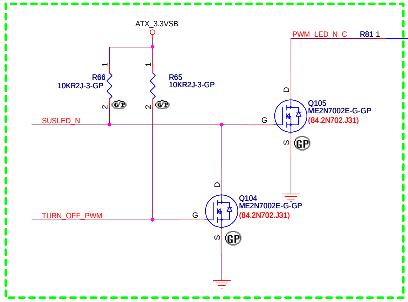


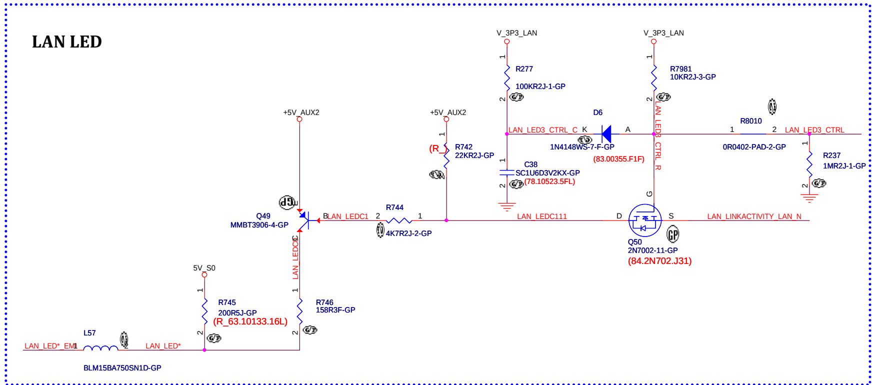


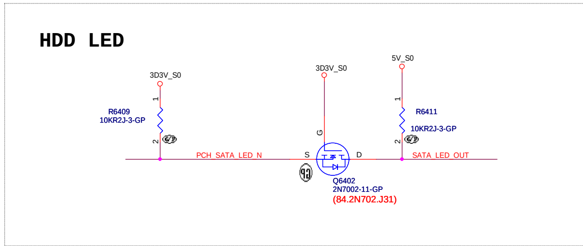
	S0	S0 / Warning	S3	S3 / Warning	S4	S5
SUSLED_N	HIGH	LOW	H & L Circling (Blink)	LOW	HIGH	LOW
PWR_LEN_2_SIO	HIGH	H & L Circling (Blink)	HIGH	H & L Circling (Blink)	LOW	HIGH



System State/Health	Indicator Behavior
S0/ Good★	Blue
S0/ Warning or	Blink Red
S3/ Good★	Blink Blue
S3/ Warning or	Blink Red
S4	No light
S5	No light







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Title: **Front board**

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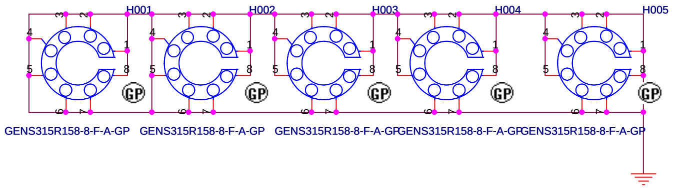
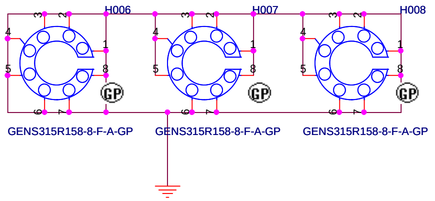




SKYLAKE SOCKET

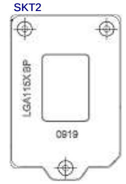
SKT1

Load Plate
(22.78006.001)

Vendor: FOXCONN
P/N: 22.78006.001

Vendor: LOTES
P/N: 22.78005.181

SKT2

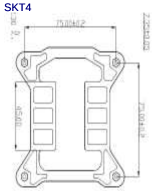


Back Plate
(22.78006.011)

Vendor: FOXCONN
P/N: 22.78006.011
Thickness:2.0mm (with mylar)

Vendor: LOTES
P/N: 022.70001.0121
Thickness: max 2.2mm (with mylar)

SKT4



ASSY BACK PLATE
(60.3EE01.002)

Thermal Component

SKT3

ILMCOVER
(22.78005.281)

Vendor: FOXCONN
P/N: 22.78005.281

Vendor: LOTES
P/N: 22.78005.171

LABEL

LAN ID :
F80F4105EB9A

LBL1
LABEL
(40.3BZ24.011)

W30*H15

Battery Symbol

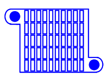
BAT1
BATTERY CR2032
(23.20068.001)

23.20068.001 KTS BBBCR2032BX

23.20023.311 MITSUBISHI CR2032 MITSUBISHI

23.22063.001 JHT CR2032 JHT

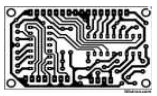
HeatSink Symbol



PCHHS1
HEATSINK
(60.3ET05.001)

Vendor
P/N:
60.3ET05.001
60.3ET05.021

PCB Symbol



PCB
PCB
(348.02802.0011)

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wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	Others
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5 4 3 2 1

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Title	IO Board_(R)
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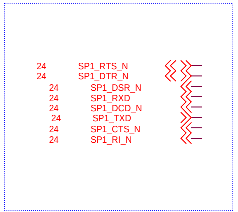
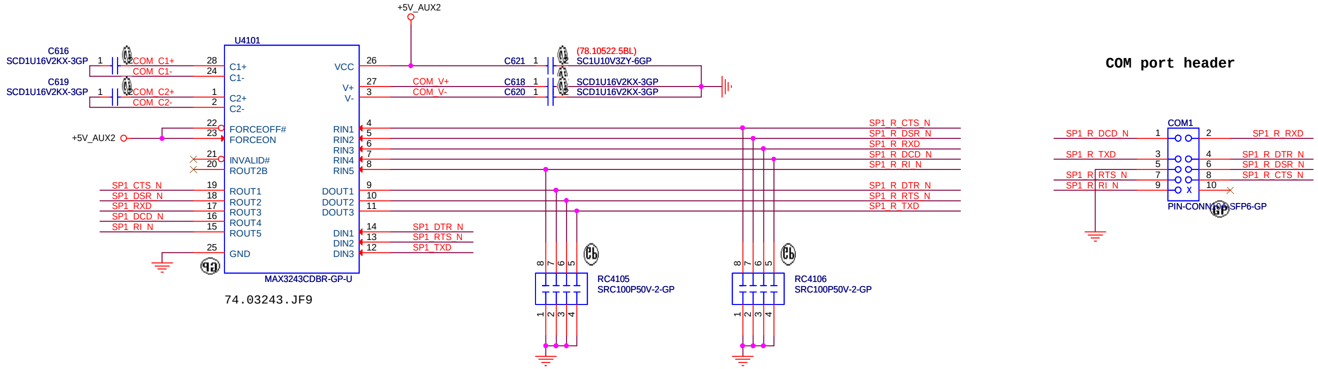
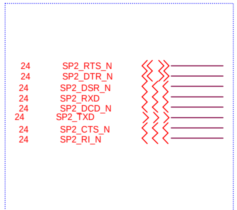
COM1



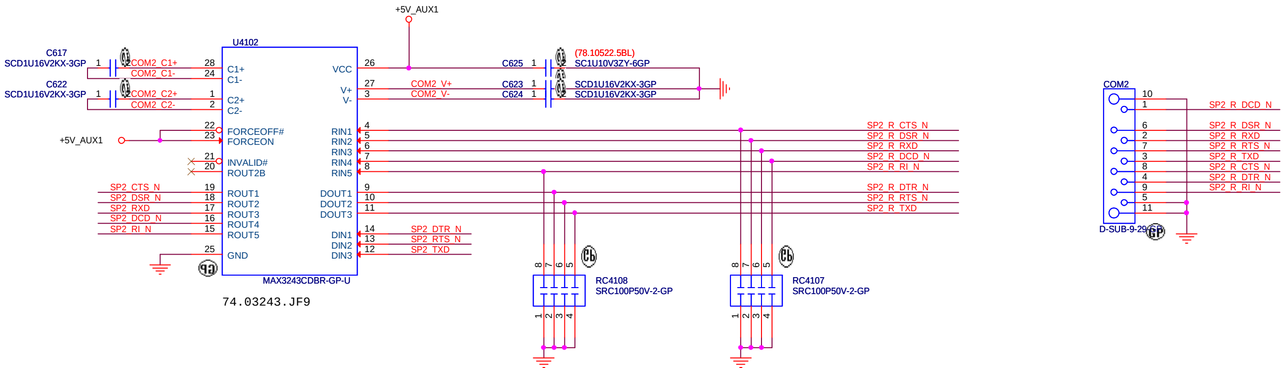
SERIAL PORT



COM2



SERIAL PORT



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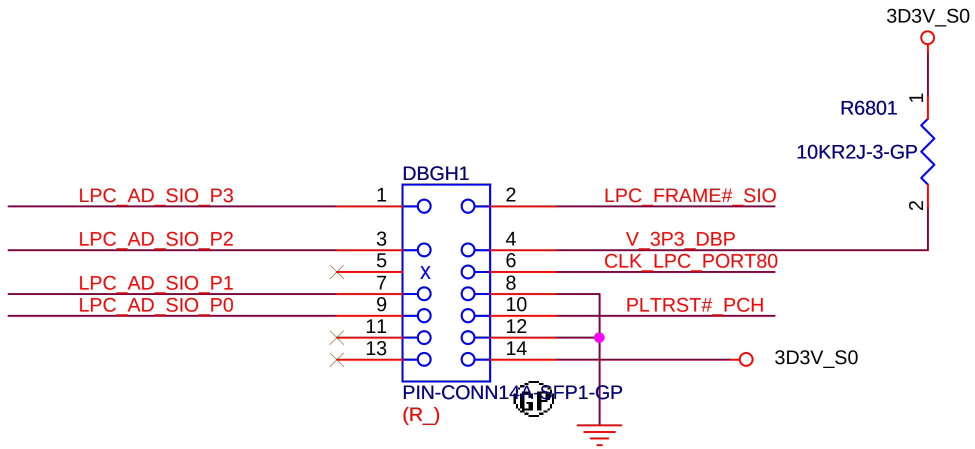
19,24,91 LPC_AD_SIO_P3
19,24,91 LPC_AD_SIO_P2
19,24,91 LPC_AD_SIO_P1
19,24,91 LPC_AD_SIO_P0

19,24,91 LPC_FRAME#_SIO

19,91 CLK_LPC_PORT80
15,24,64,91,97 PLTRST#_PCH

80 port

Layout close to SIO



21.62888.207

Annie pin define

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wistron	**Wistron Incorporated** 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	**Debug**
Size: Custom	Document Number: **vHulk** — Rev: -1
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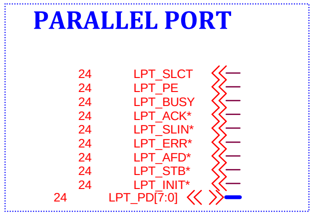

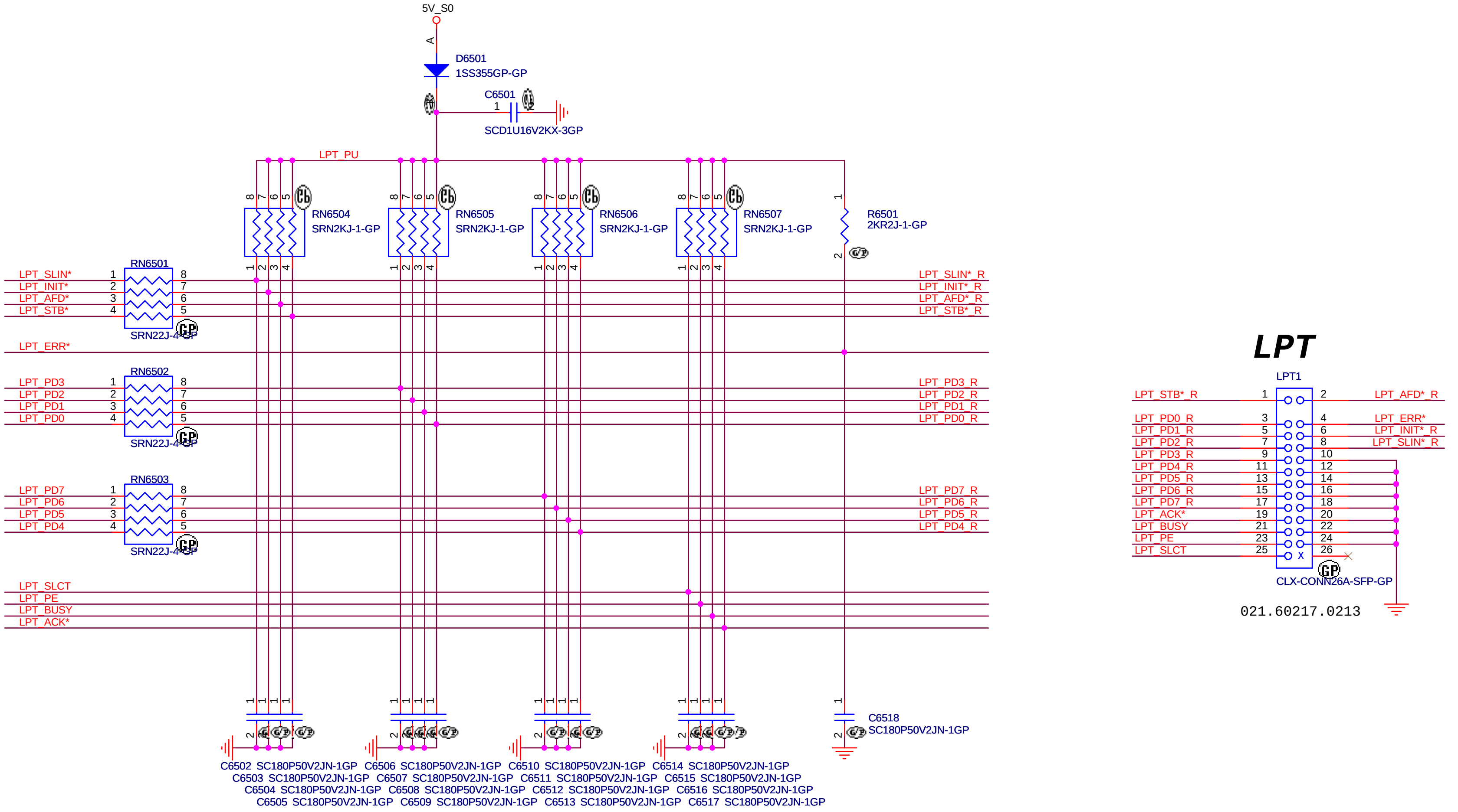

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Title: LPT		
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wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	G sensor_(R)	
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Title	Thunderbolt_(R)	
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Title	**Thunderbolt_(R)**	
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Title	Thunderbolt_(R)	
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Title	Thunderbolt_(R)		
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wistron	**Wistron Incorporated** 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	GPU_(R)
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Title	GPU_(R)	
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Title	GPU_(R)	
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	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
Title: GPU_(R)			
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Title: GPU_(R)		
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Title	GPU VRAM 1&2_(R)	
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wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	GPU VRAM 3&4_(R)	
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Title
GPU VRAM 5&6_(R)

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Title: **GPU CORE_(R)**

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Title: GPU discrete power_(R)		
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wistron	**Wistron Incorporated** 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	GPU Switch_(R)
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Title	GPU Switch_(R)	
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Title	GPU Others_(R)	
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Title	NFC_(R)	
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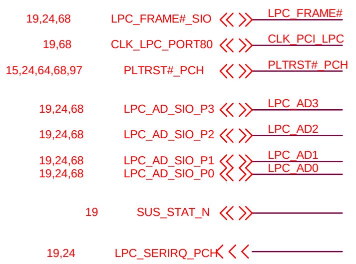
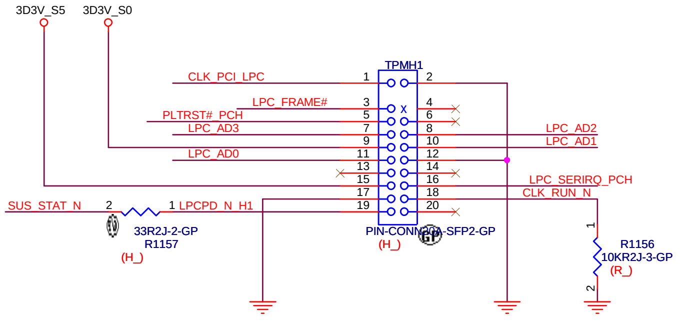
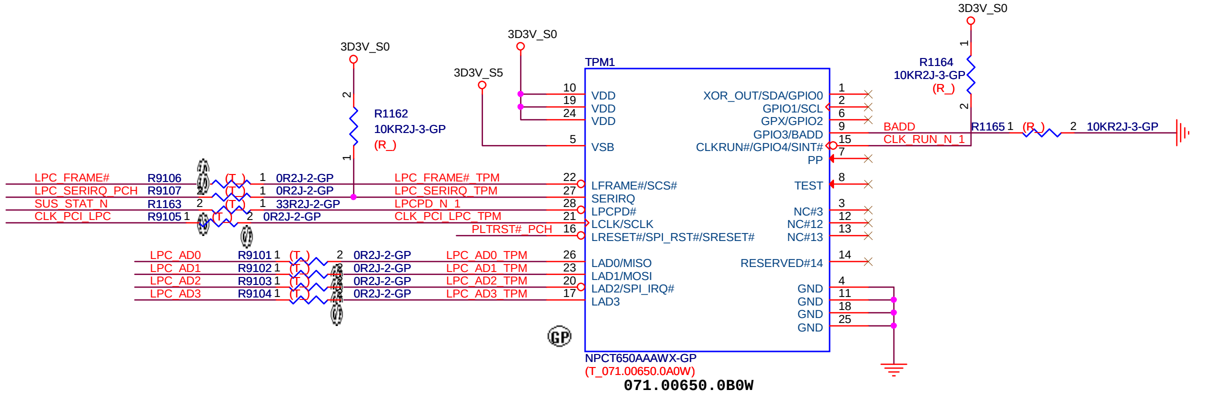
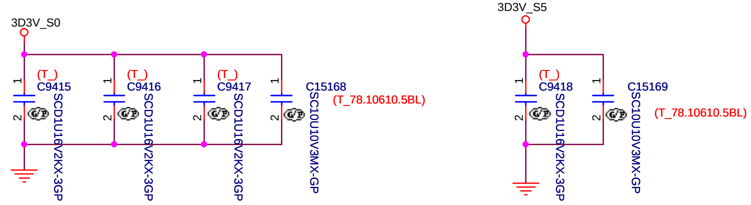


TPM 2.54 pitch Header



TPM onboard chip for Q170





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Title	TPM	
Size Custom	Document Number vHulk	Rev -1
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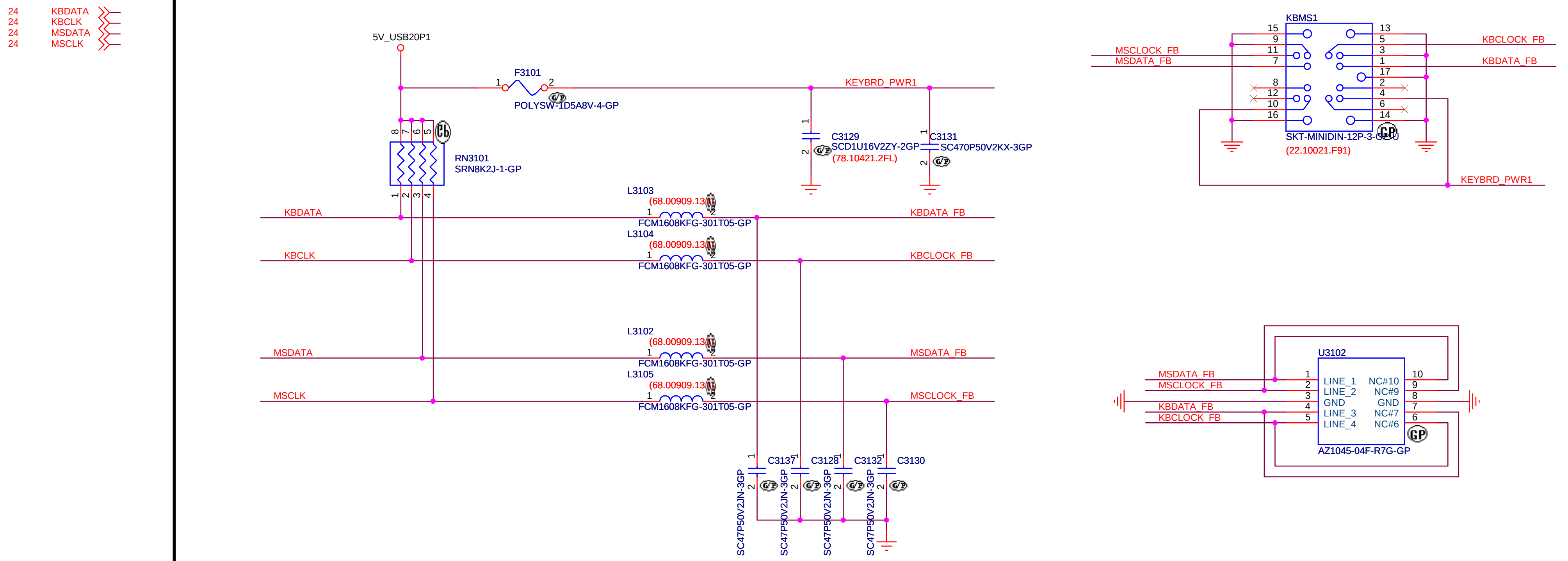

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Title	PS2	
Size: Custom	Document Number: vHulk	Rev: -1
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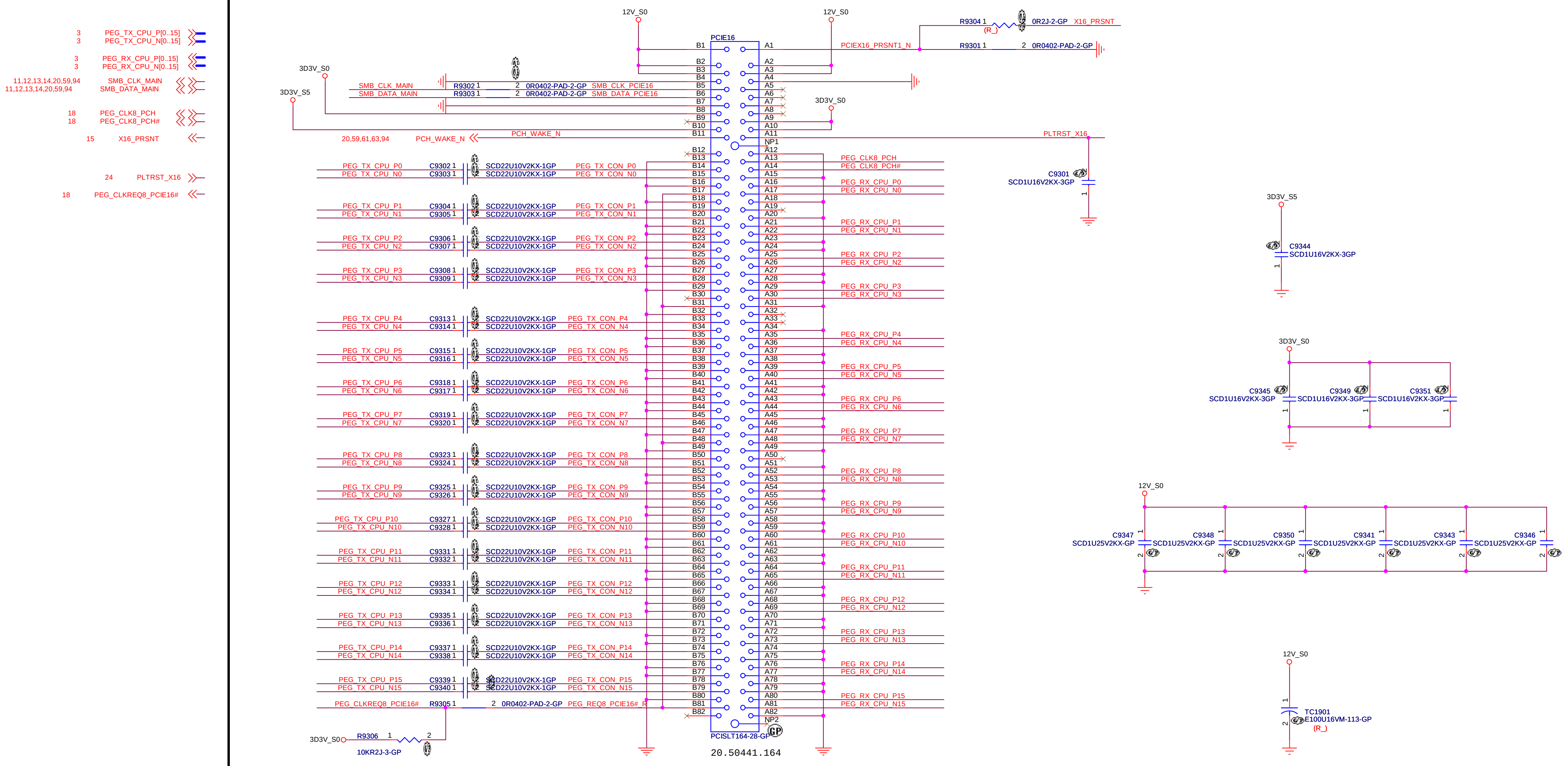

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Title: **Express Card:PCIE X16**

Size	Document Number	Rev
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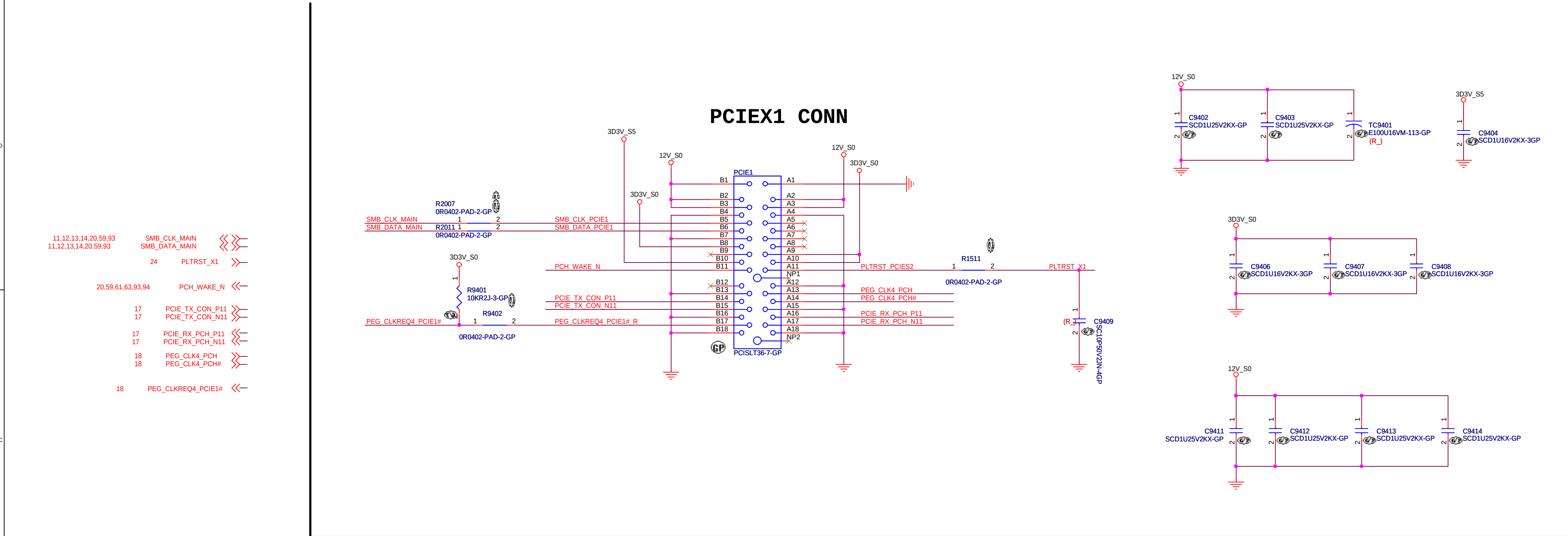

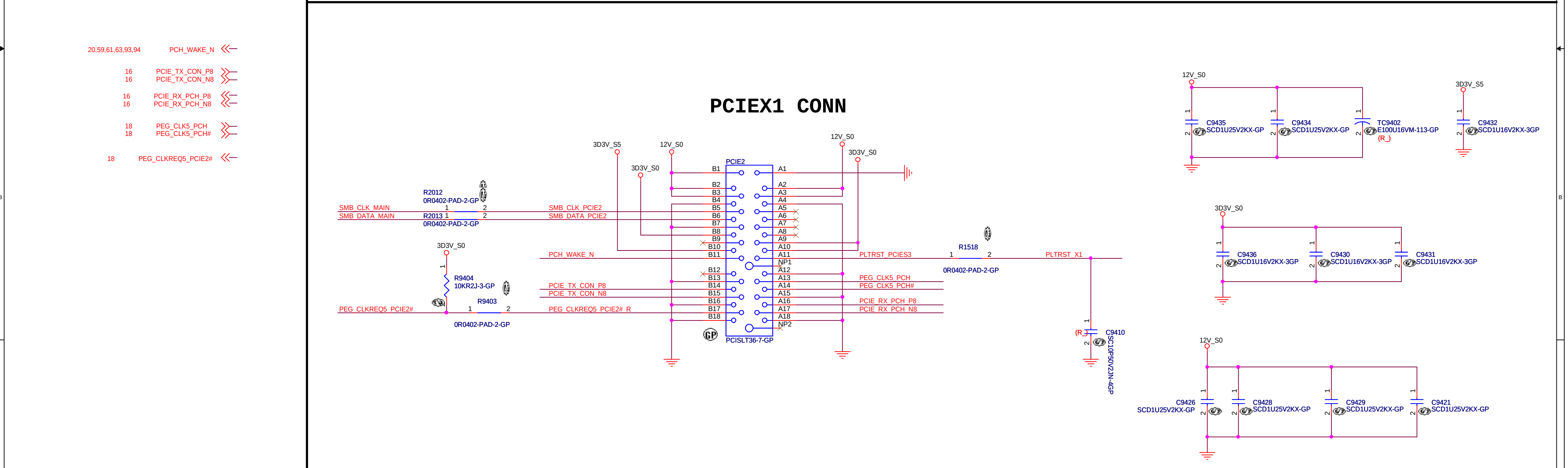

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Title	Smart Card PCIE X1	
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Title	Scalar_(R)	
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Wistron Incorporated
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Title	MCU_(R)	
Size C	Document Number vHulk	Rev -1
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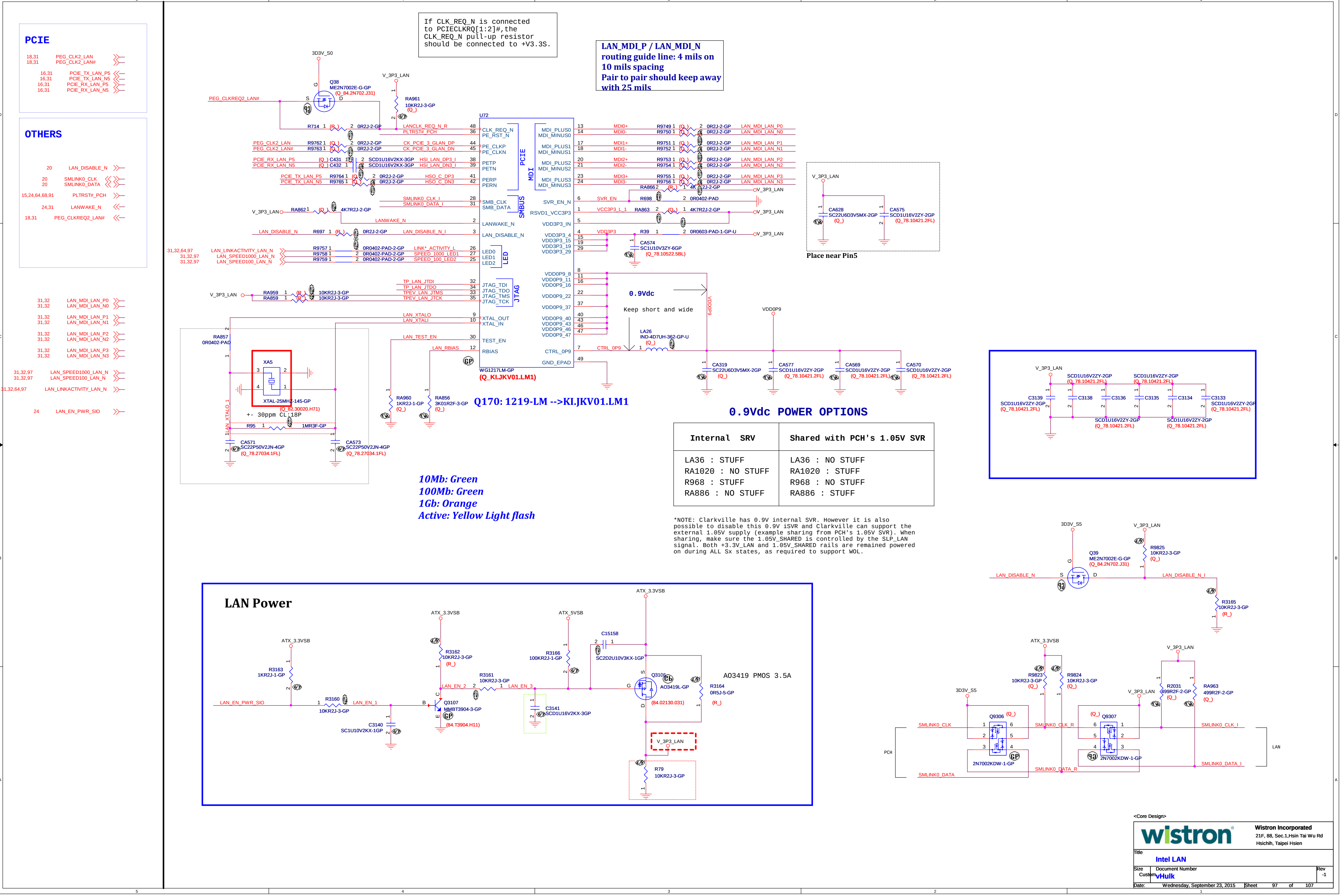

0.9Vdc POWER OPTIONS

Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply (example sharing from PCH's 1.05V SVR). When sharing, make sure the 1.05V_SHARED is controlled by the SLP_LAN signal. Both +3.3V_LAN and 1.05V_SHARED rails are remained powered on during ALL Sx states, as required to support WOL.

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Title: Intel LAN

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Wistron Incorporated
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Title	LAN Switch_(R)	
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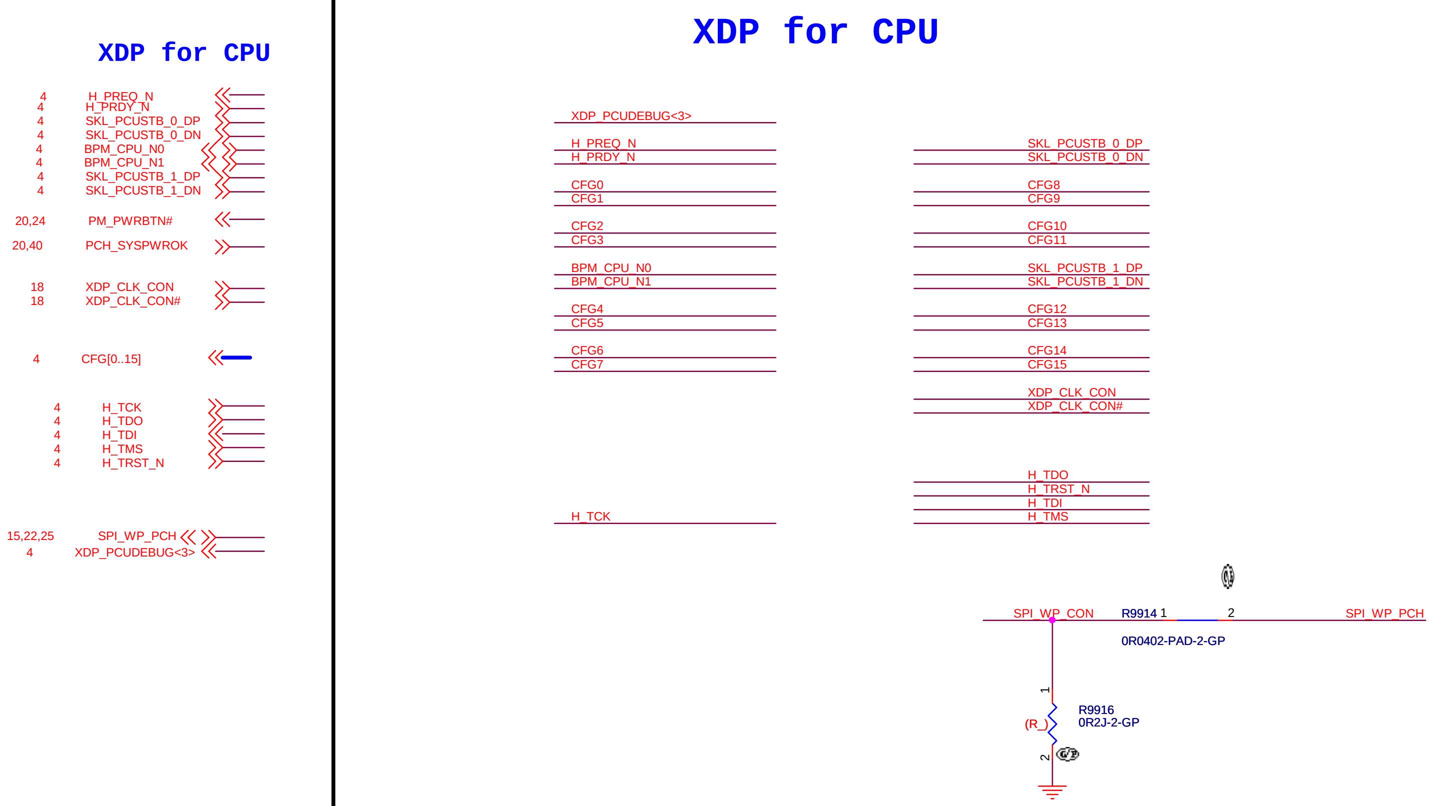

<Core Design>

wistron	Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title	XDP&ITP	
Size Custom	Document Number vHulk	Rev -1
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Title	Table of Content
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wistron	**Wistron Incorporated** 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien
Title	**GPIO table**
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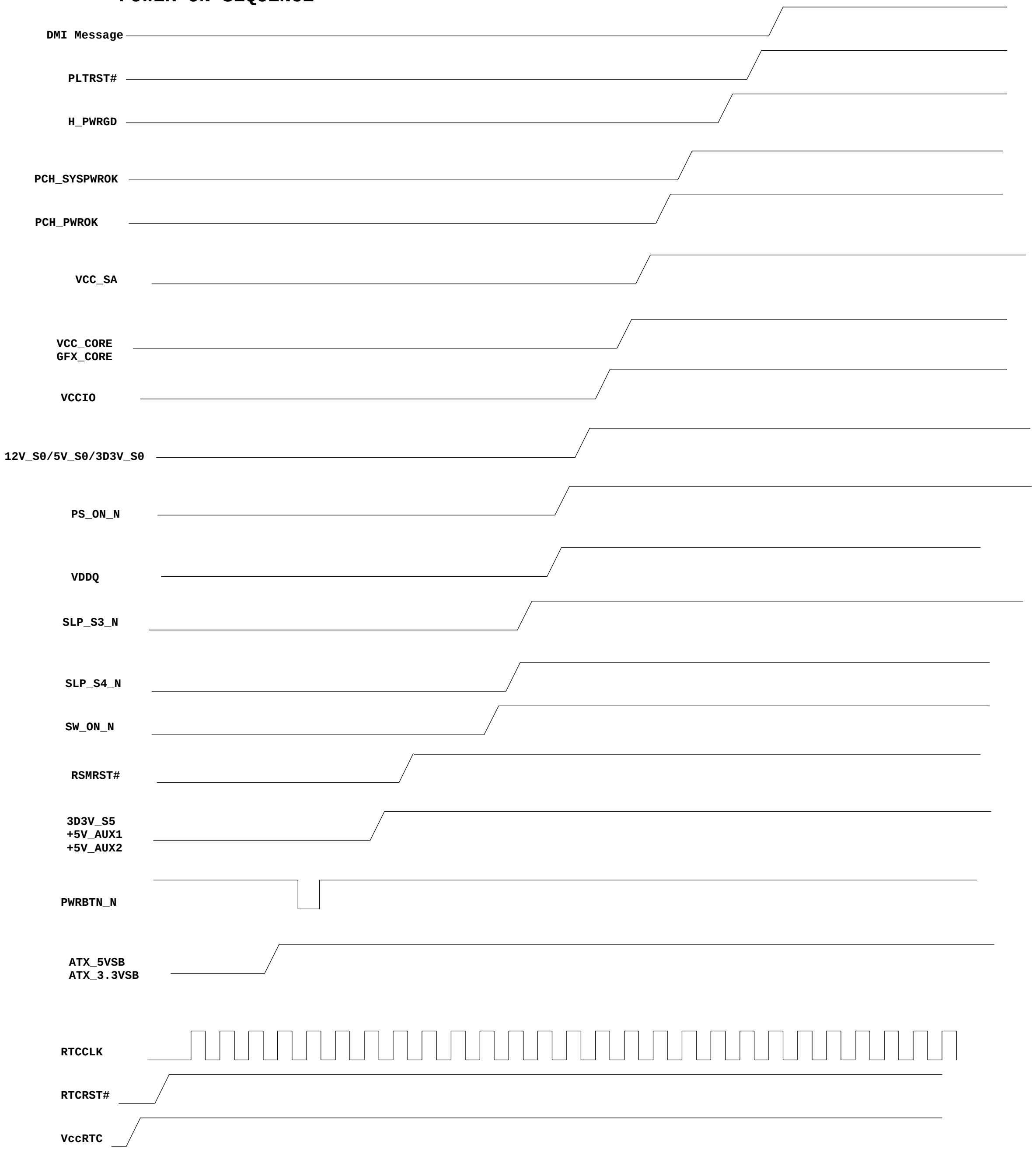
POWER ON SEQUENCE



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Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien		
Title: Power sequence		
Size: Custom	Document Number: vHulk	Rev: -1
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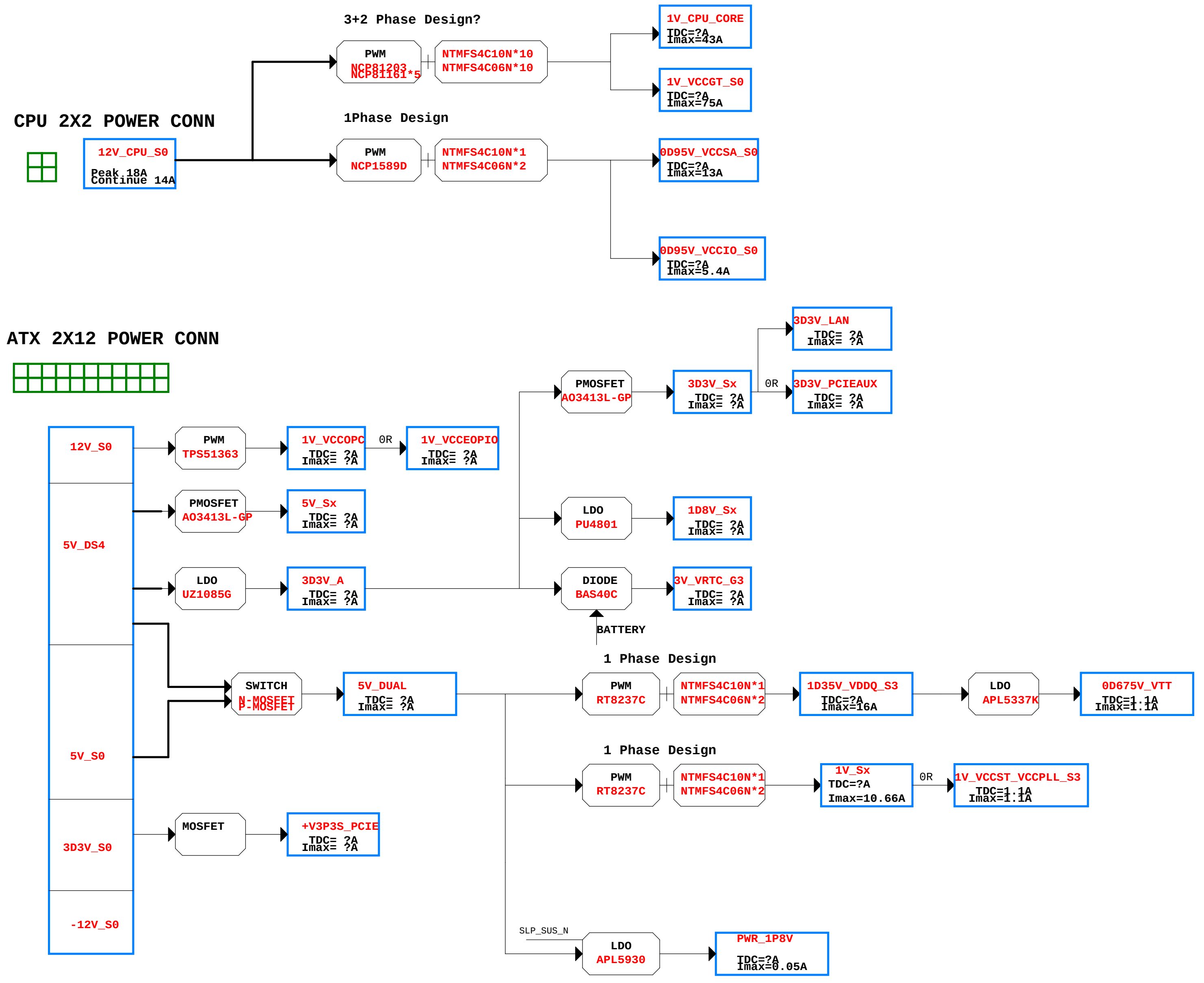

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Title	Power Block Diagram	
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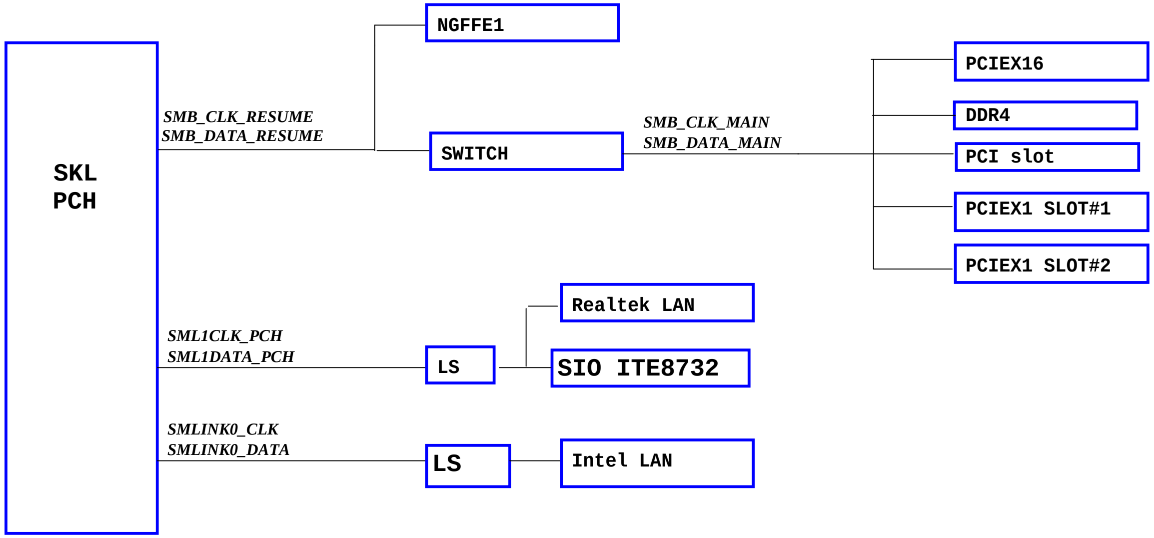

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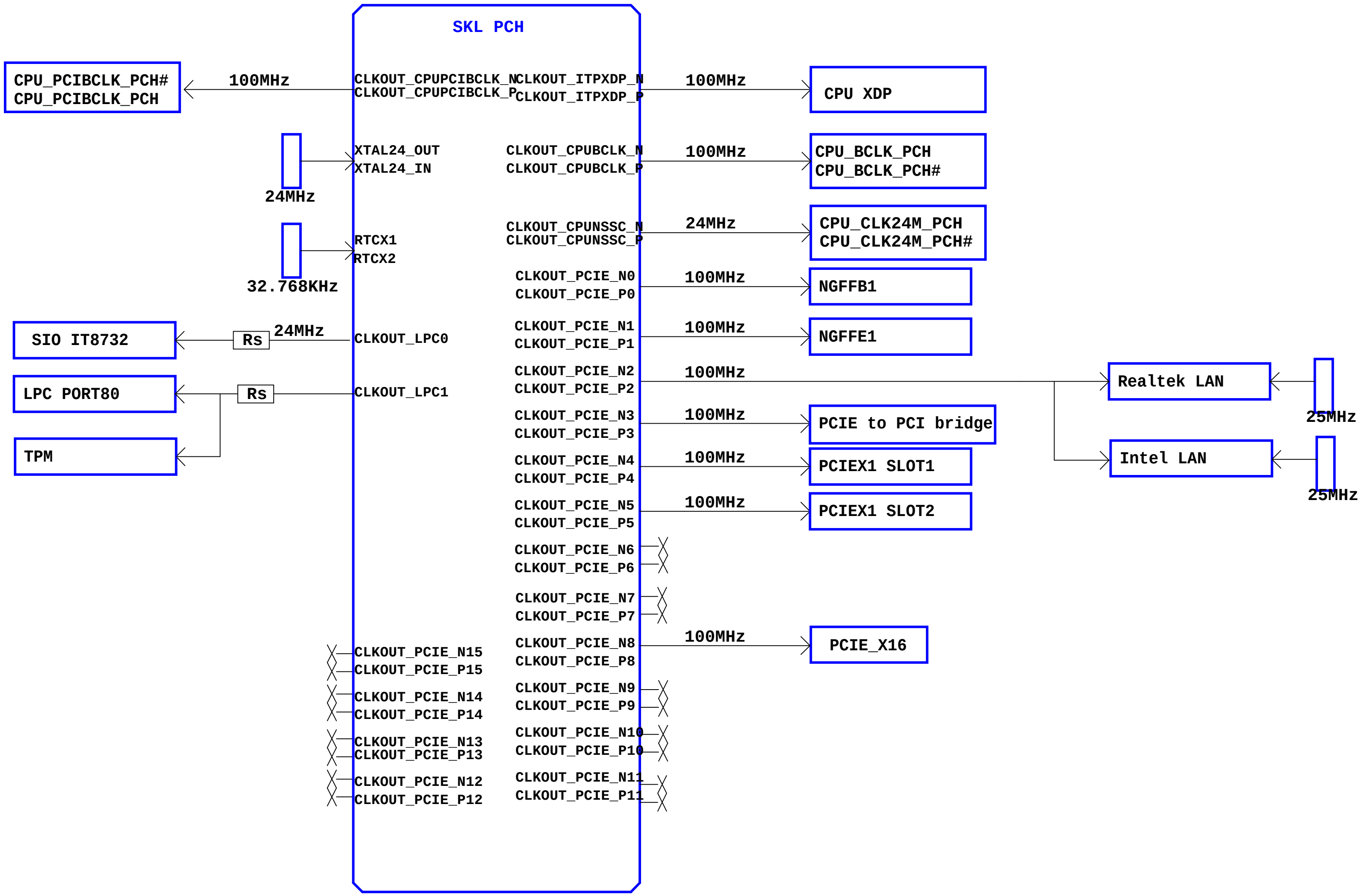
Title: SMBUS Block Diagram		
Size: C	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet 104 of 107	



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Title		
Clock MAP		
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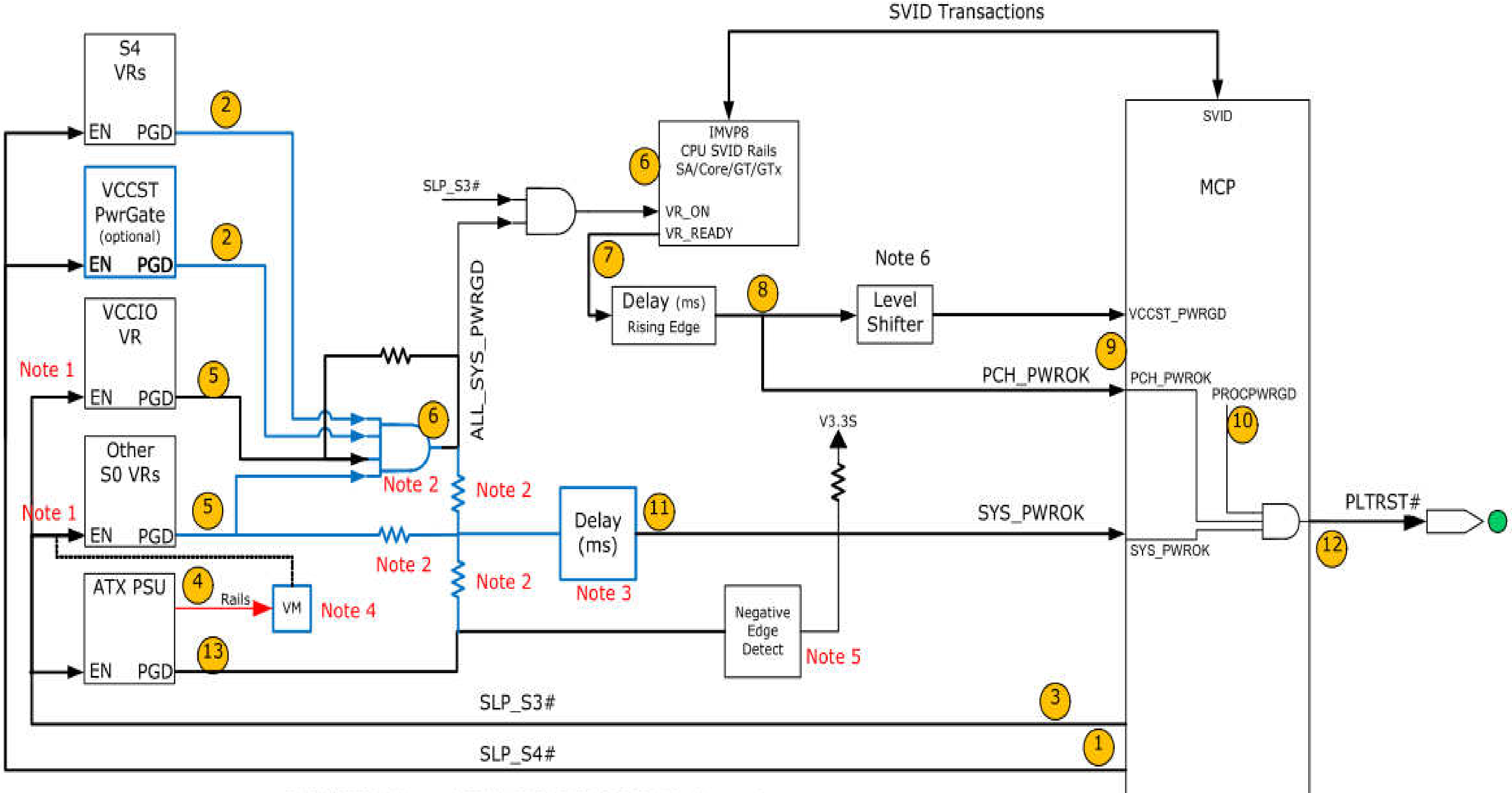

DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown

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Title		
RESET Flow Chart		
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Title	Change History	
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