LCFC Confidential

CG414/CG514 (NMA-851)M/B Schematics Document

Intel Apollolake M-Processor with DDRIIIL + AMD(R16M-M1-30) GPU

2016-07-21

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2014/01/21

Title: *Cover Page*

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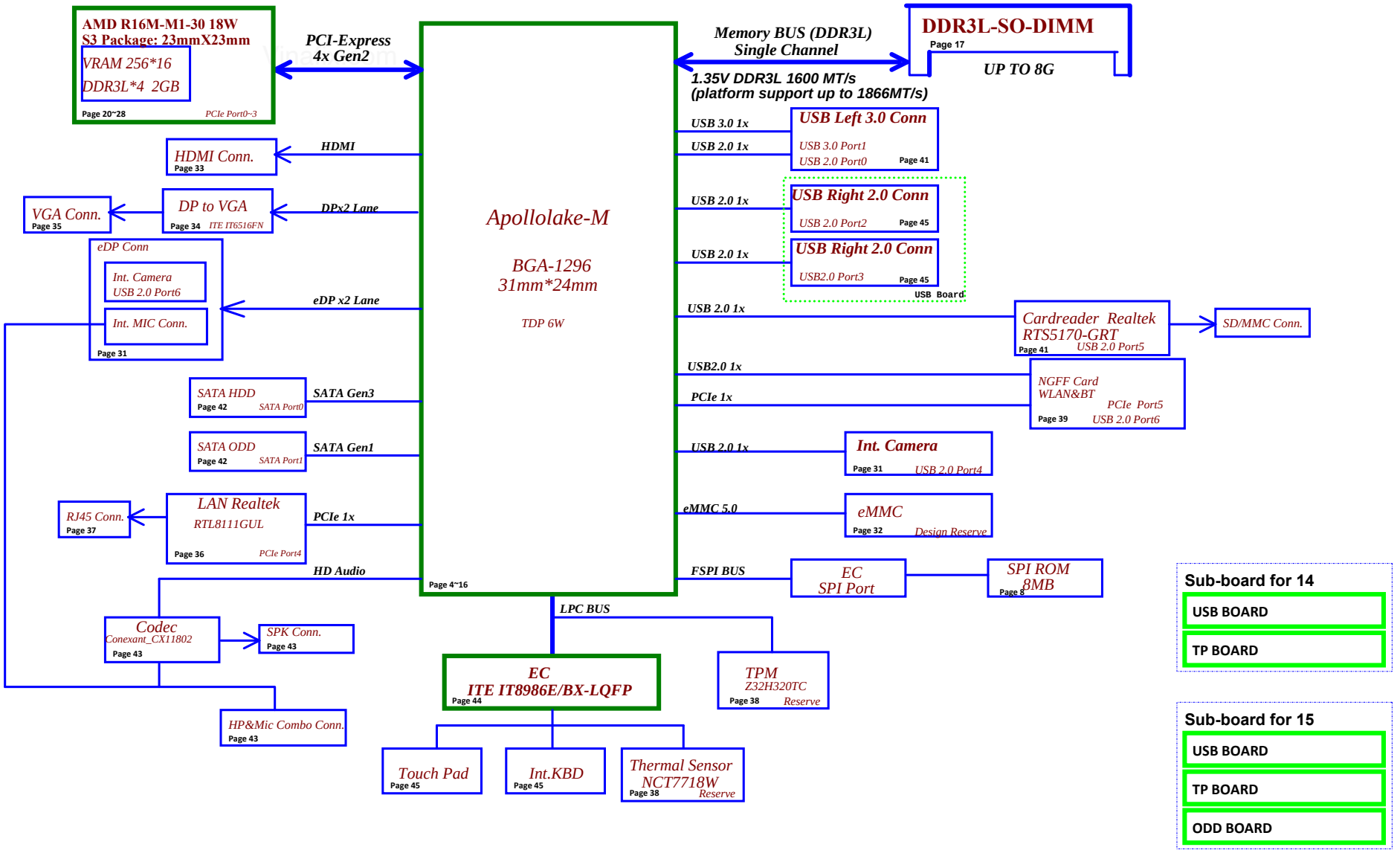
File Name : Toronto



Security Classification	LC Future Center Secret Data		
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Title	Block Diagram		
Size C	Document Number	CG414&CG514	Rev 1.0
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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ Power Plane	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.35V	+5VS +3VS +1.8VS +1.05VS VTT +CPU_CORE +VNN
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

SIGNAL / STATE	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0IX(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	NC
	1	USB3.0(Left Side)
USB 2.0	0	USB3.0(2.0) (Left Side)
	1	NC
	2	RIGHT USB DB (2.0)
	3	RIGHT USB DB (2.0)
	4	CAMERA
	5	CARD READER
	6	NC
	7	BT

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	HDMI
eDP	eDP

PCIE PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
1			
2			
3			
4	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
EMC_14@	EMC 14" part
EMC_USB@	EMC USB TVS part
CD@	Cost Down part
RF@	For RF part
RF_NS@	For RF un-stuff part
RF_PXNS@	For RF GPU un-stuff part
14@	For 14" part
15@	For 15" part
8111GUL@	8111GUL LAN SKU part@
8111H@	8111H LAN SKU part@
PX@	Discrete GPU SKU part
TOPAZ@	TOPAZ dGPU SKU part
EXO@	R16M-M1-30 dGPU SKU part
UMA@	UMA SKU ID part
TMSEN@	Thermal Sensor part
TMSEN_PX@	dGPU Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
NUVOTON@	NOVOTON TPM part
NATIONZ@	NATIONZ TPM part
ICR@	Intel Apollolake Integrated Card Reader
RTSCR@	Realtek RTS5170-GRT Card Reader
EMMC@	EMMC part
UART@	UART debug part
RTCRST@	Clear RTCRST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N3350_B0@	Apollolake N3350 B0 stepping MP CPU part
N3450_B0@	Apollolake N3450 B0 stepping MP CPU part
N4200_B0@	Apollolake N4200 B0 stepping MP CPU part
N3350_B1@	Apollolake N3350 B1 stepping MP CPU part
N3450_B1@	Apollolake N3450 B1 stepping MP CPU part
N4200_B1@	Apollolake N4200 B1 stepping MP CPU part
M4G@	Micron 4Gb(256x16) VRAM part
S4G@	Samsung 4Gb(256x16) VRAM part
H4G@	Hynix 4Gb(256x16) VRAM part
M2GX4@	Micron 2GB(256x16x4) VRAM X76 SKU
S2GX4@	Samsung 2GB(256x16x4) VRAM X76 SKU
H2GX4@	Hynix 2GB(256x16x4) VRAM X76 SKU

EC SM Bus0 address

Device	Address
PMIC	0x68

EC SM Bus1 address

Device	Address
Smart Battery	0x16
Charger	0x12

EC SM Bus2 address

Device	Address
Thermal Sensor	0x98(reserve)
VGA	0x41 (default)

PCH SM Bus address

Device	Address
DDR SO-DIMM	0xA0
Wlan	Rsvd

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Title	Notes List		
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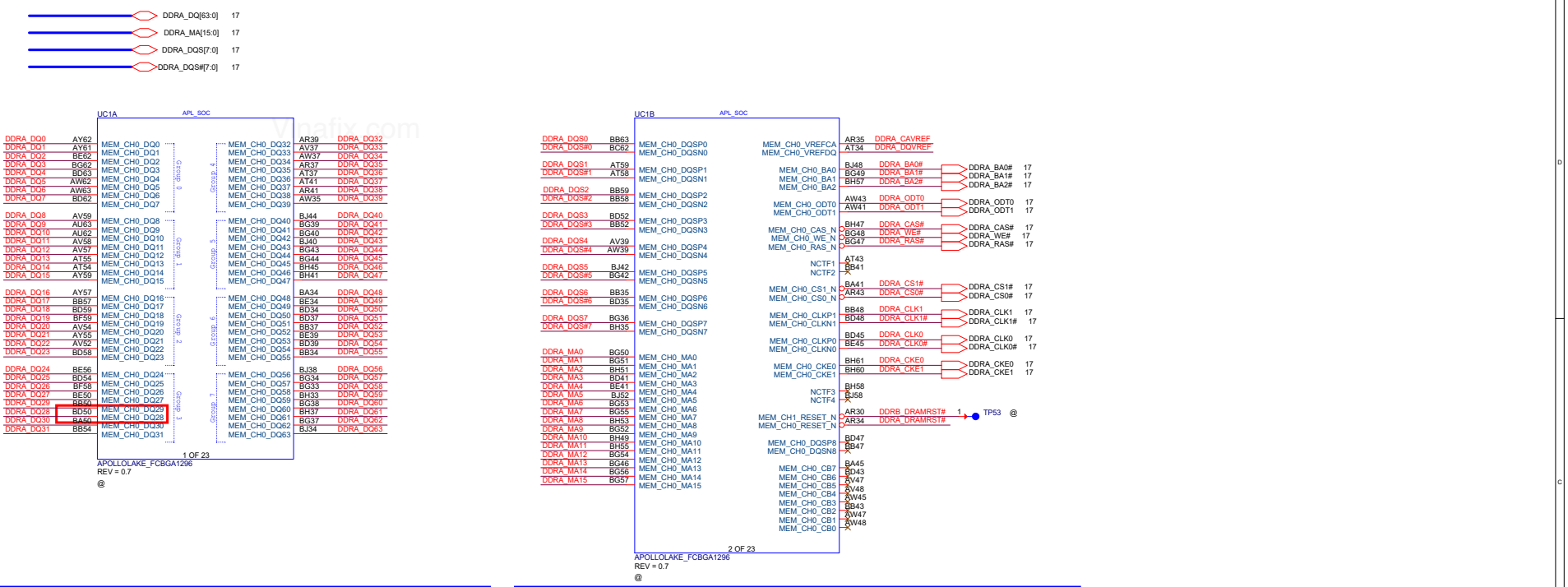
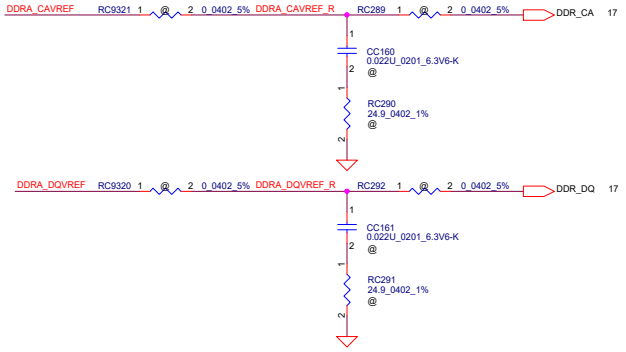


Follow CRB(v1.2): unstuff RC289, CC160, RC290, RC292, CC161, RC291 03/12



Follow CRB(PDG w/o 1k damping resister)
Double confirm with Intel FAE, follow CRB will have low risk

Security Classification	LC Future Center Secret Data		
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Title: SOC (DDR3L CHA)

Size	Document Number	Rev
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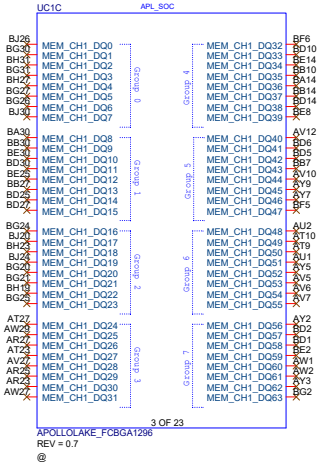

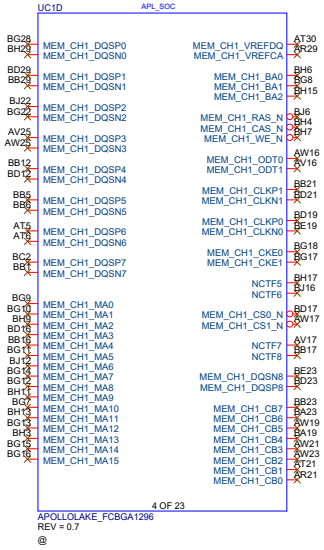

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Issued Date	2013/03/26	Deciphered Date	2014/01/21

Title: SOC (DDR3L CHB)

Size	Document Number	Rev
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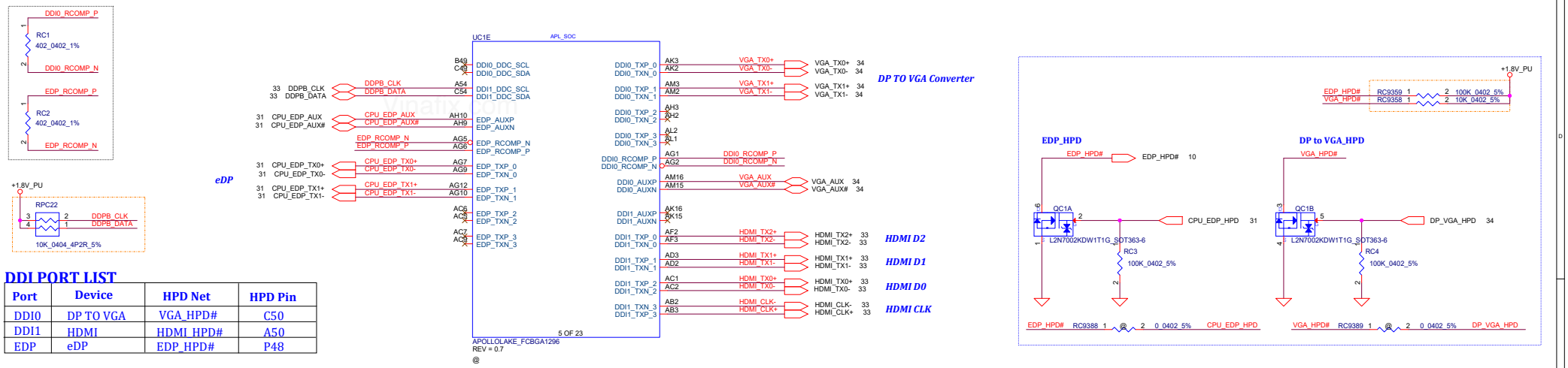

DDI PORT LIST

Port	Device	HPD Net	HPD Pin
DDI0	DP TO VGA	VGA_HPD#	C50
DDI1	HDMI	HDMI_HPD#	A50
EDP	eDP	EDP_HPD#	P48

PCH_LCD_VDDEN_Q VOH min is 1.35V, SY6288C20 VIH min is 1.35V, do NOT use level shift (Follow BMWC1)

PCH_ENBKL can direct connect to EC for costdown

Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2014/01/21

Title	SOC (DDI,EDP,HDMI,MDSI)		
Size	Document Number		Rev
C	CG414&CG514		1.0
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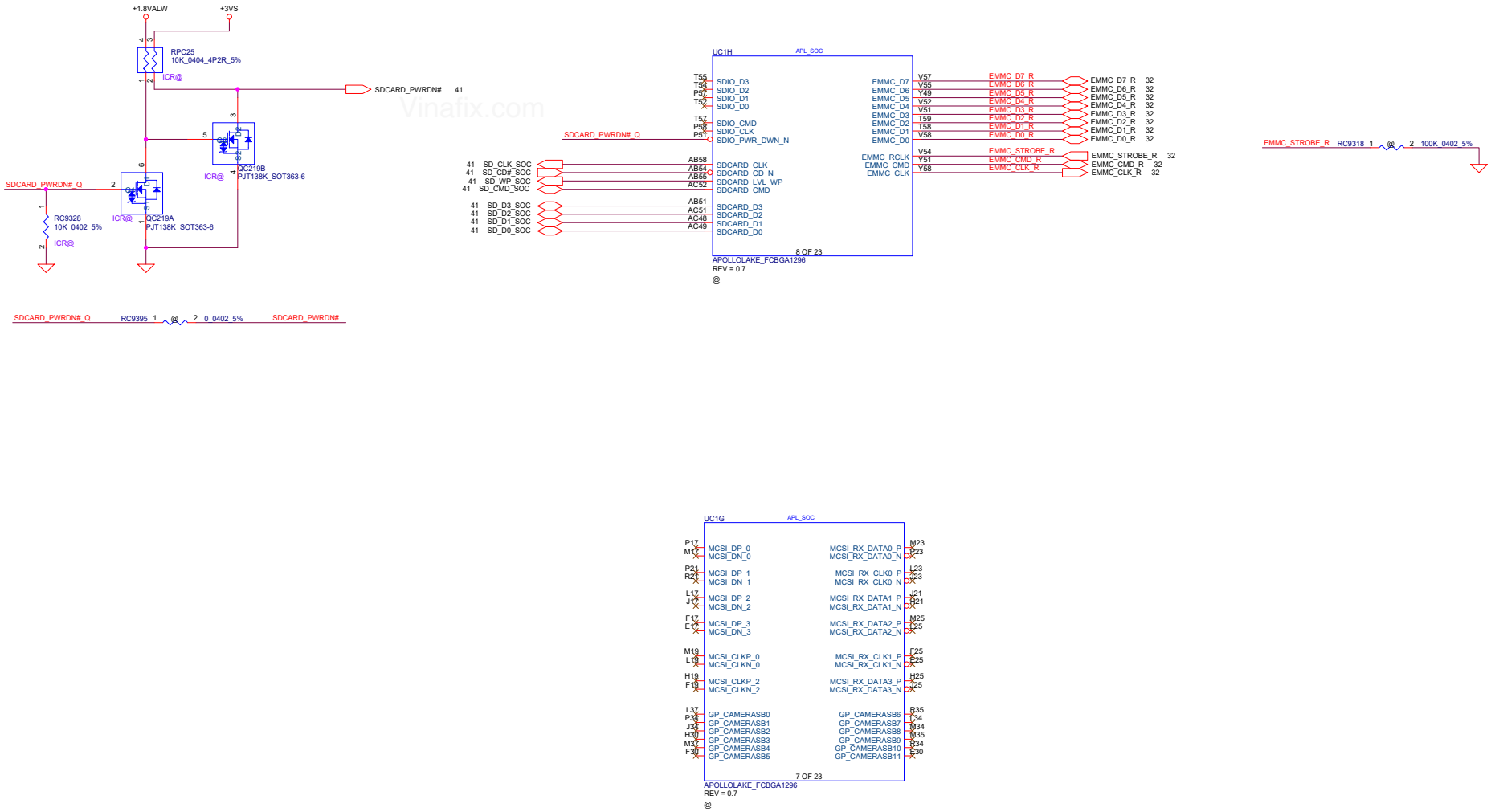

Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2014/01/21

Title: SOC (eMMC,SD,MCSI)

Size	Document Number	Rev
C	CG414&CG514	1.0

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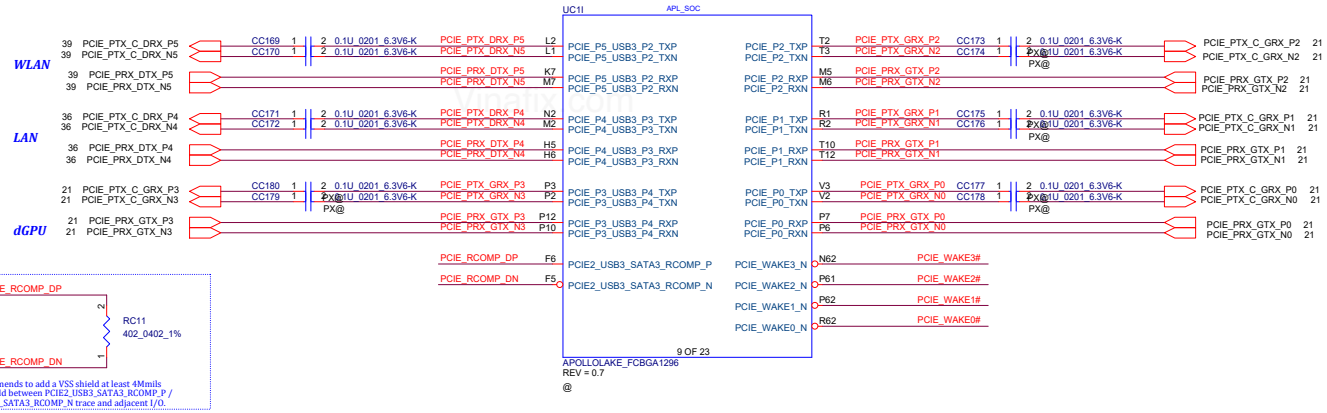
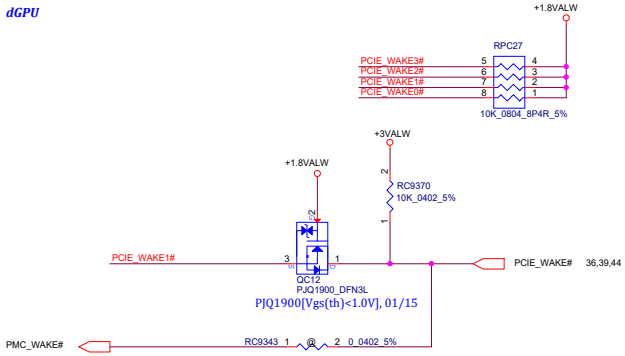
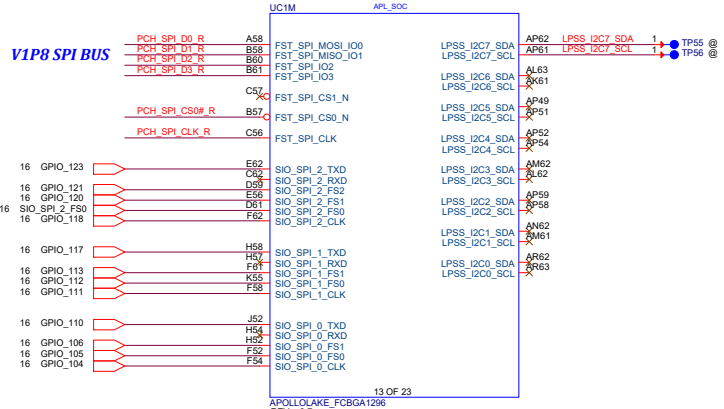
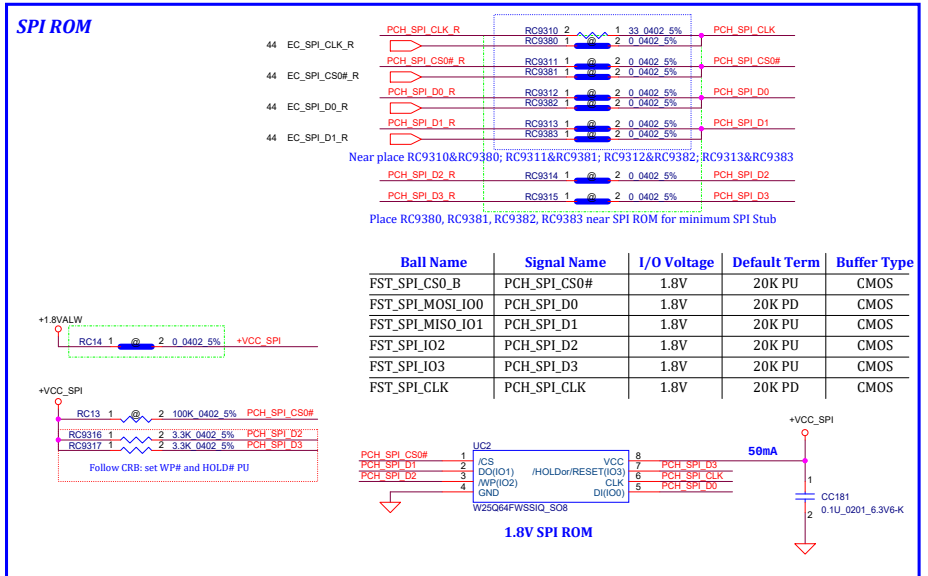
PCIE Configuration

Port	Config	Device	BIOS Device ID Map
P0	X4	dGPU	PCIe1(Func0):Root Port#3
P1			
P2			
P3			
P4	X1	LAN	PCIe0(Func0):Root Port#1
P5	X1	WLAN	PCIe0(Func1):Root Port#2









Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
FST_SPI_CS0_B	PCH_SPI_CS0#	1.8V	20K PU	CMOS
FST_SPI_MOSI_IO0	PCH_SPI_D0	1.8V	20K PD	CMOS
FST_SPI_MISO_IO1	PCH_SPI_D1	1.8V	20K PU	CMOS
FST_SPI_IO2	PCH_SPI_D2	1.8V	20K PU	CMOS
FST_SPI_IO3	PCH_SPI_D3	1.8V	20K PU	CMOS
FST_SPI_CLK	PCH_SPI_CLK	1.8V	20K PD	CMOS

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Title: SOC (PCIE&GPIO&SPI)

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C	CG414&CG6514	1.0

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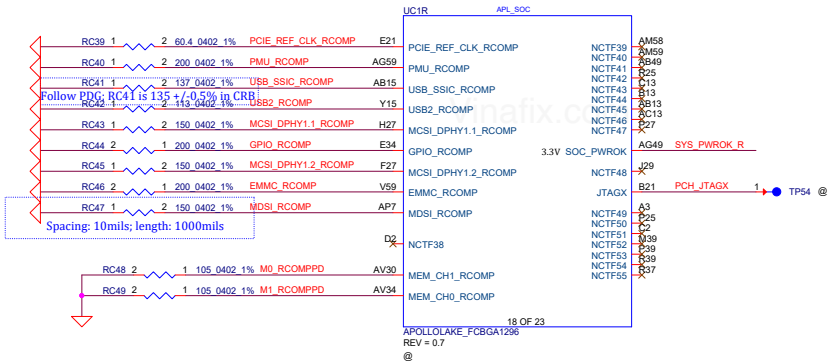
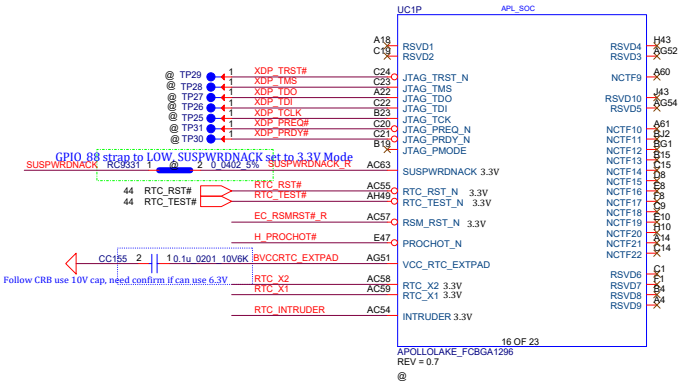
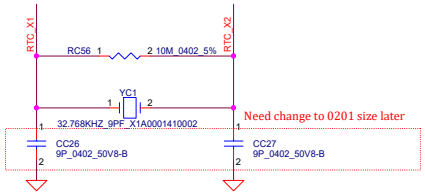




RCOMP RESISTOR REQUIREMENT

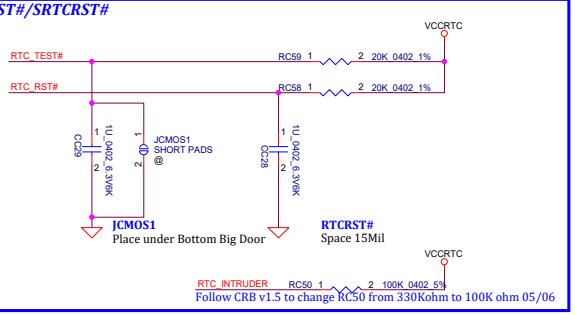
INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
CSI1.1	MCSI_DPHY1.1_RCOMP	RC43	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSI_DPHY1.2_RCOMP	RC45	150 +/-1%
USB2 and 3.3V mode GPIO	USB2_RCOMP	RC42	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	RC39	60.4 +/-1%
modPHY (PCIE, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP_P/N	RC11	402 +/-1%
MDSI	MDSI_RCOMP	RC47	150 +/-1%
SSIC	USB_SSIC_RCOMP	RC41	137 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode SD Card, PMU, LPC, SMBUS.	EMMC_RCOMP GPIO_RCOMP PMU_RCOMP	RC46 RC44 RC40	200 +/-1%
eDP	EDP_RCOMP_P/N	RC2	402 +/-1%
DDI	DDI0_RCOMP_P/N	RC1	402 +/-1%
Memory	MEM_CH0_RCOMP/ MEM_CH1_RCOMP	RC49 RC48	105 +/-1%

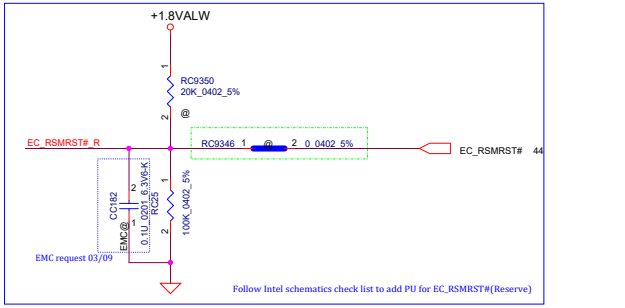


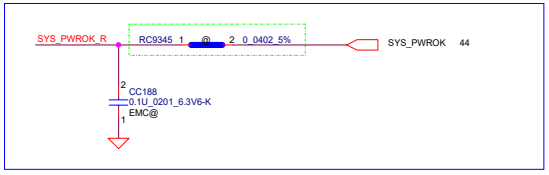
32.768kHz CRYSTAL--EPSON SJ10000IX00

1. Space 15MIL
2. No trace under crystal
3. Place on oppsosit side of MCP for temp influence
4. EDS request X'TAL ESR=50Kohm; +/-20ppm; X1,X2 pin capacitance=15pF

RTCRST#/SRTCRST#







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Title: **SOC (RTC&RCOMP&JTAG)**

Size	Document Number	Rev
C	CG414&CG514	1.0

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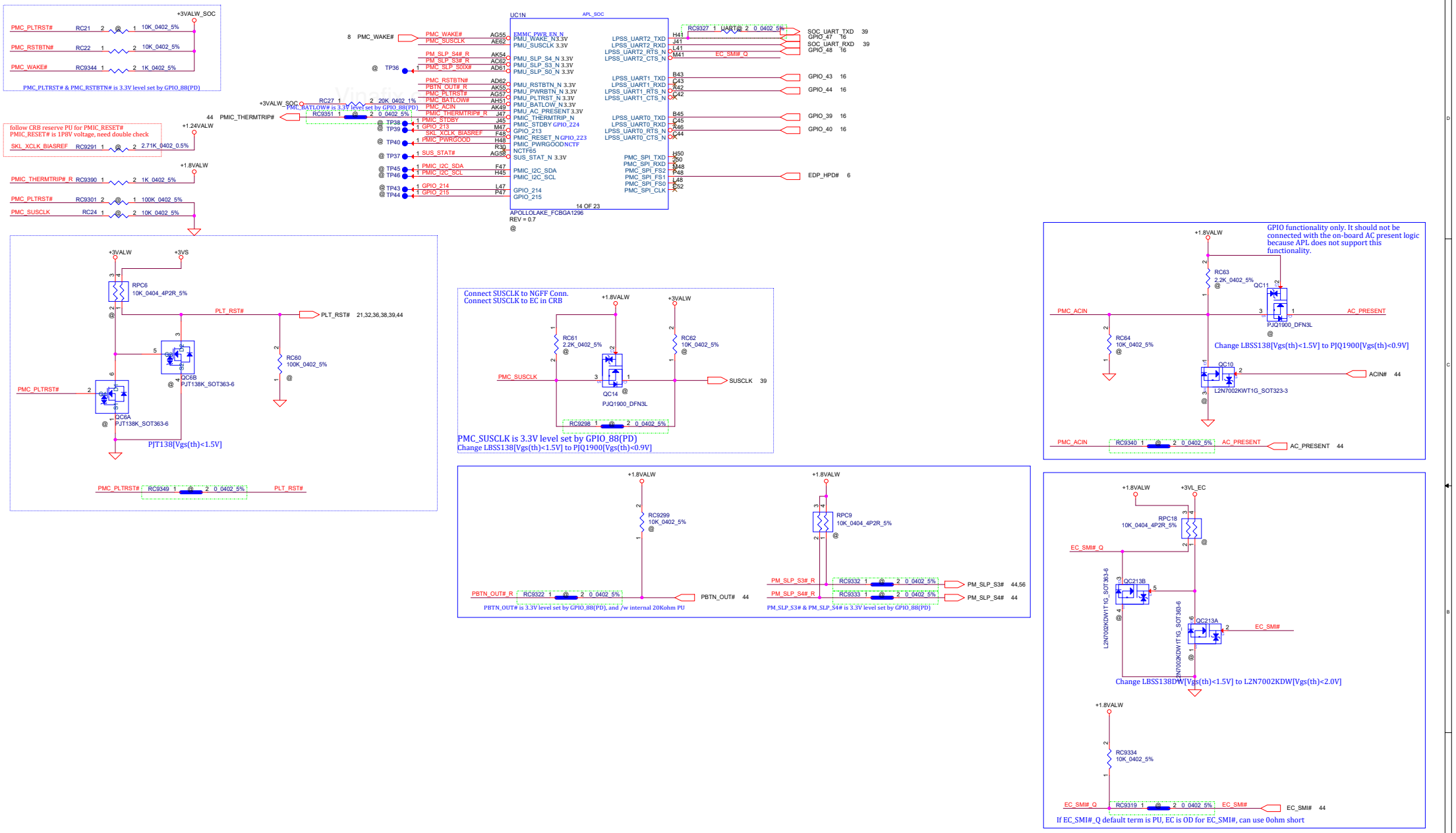

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Title: **SOC (PMU&UART)**

Size	Document Number	Rev
Custom	CG414&CG514	1.0

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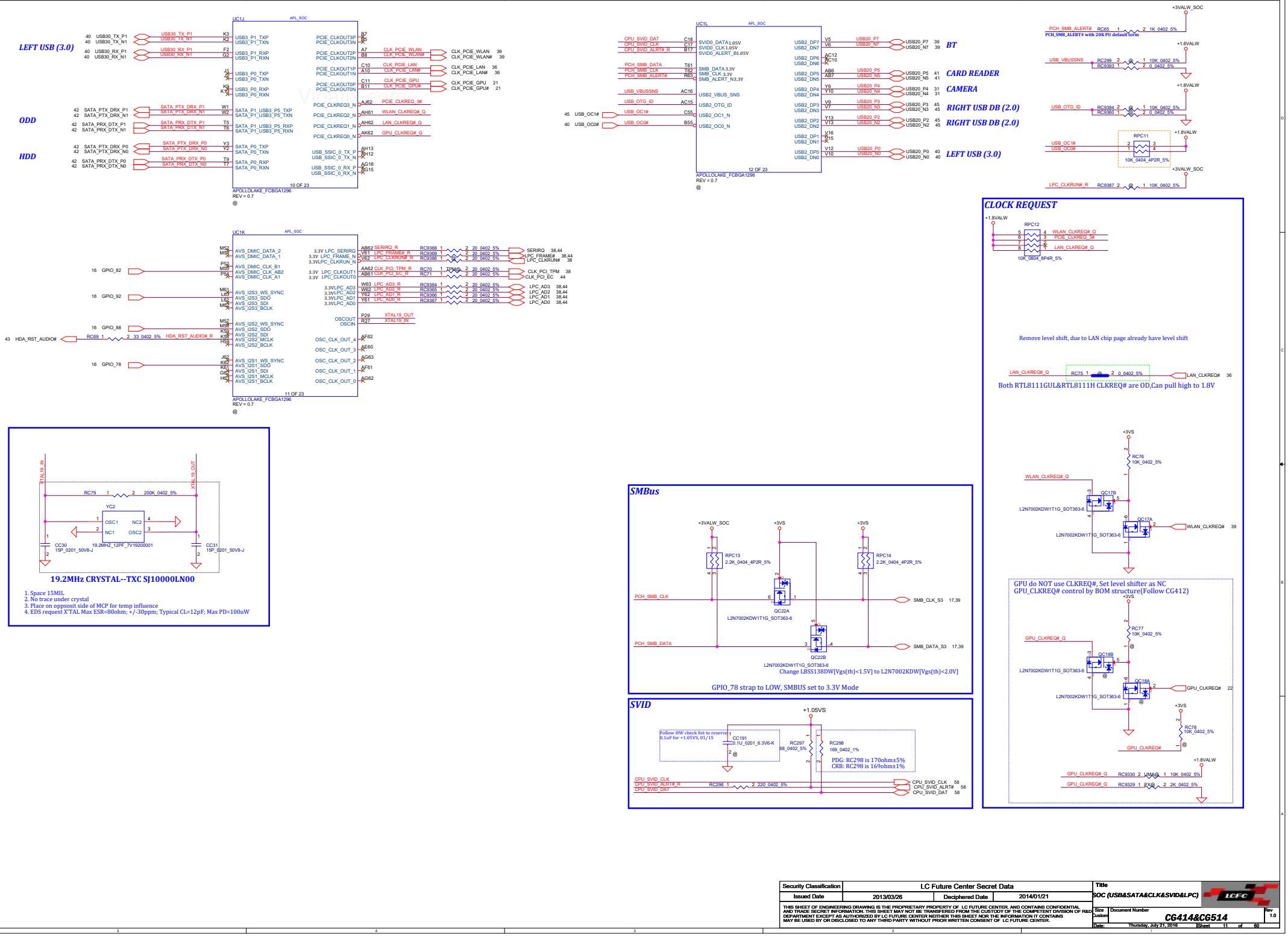

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Title: SOC (USB&SATA&CLK&SVID&LPC)

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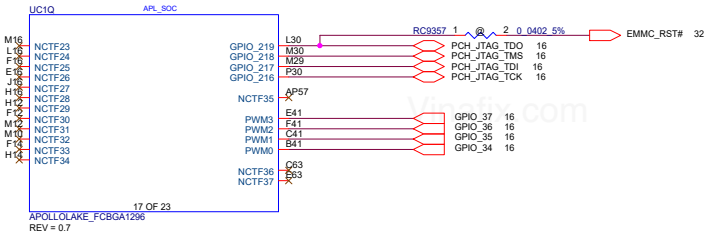
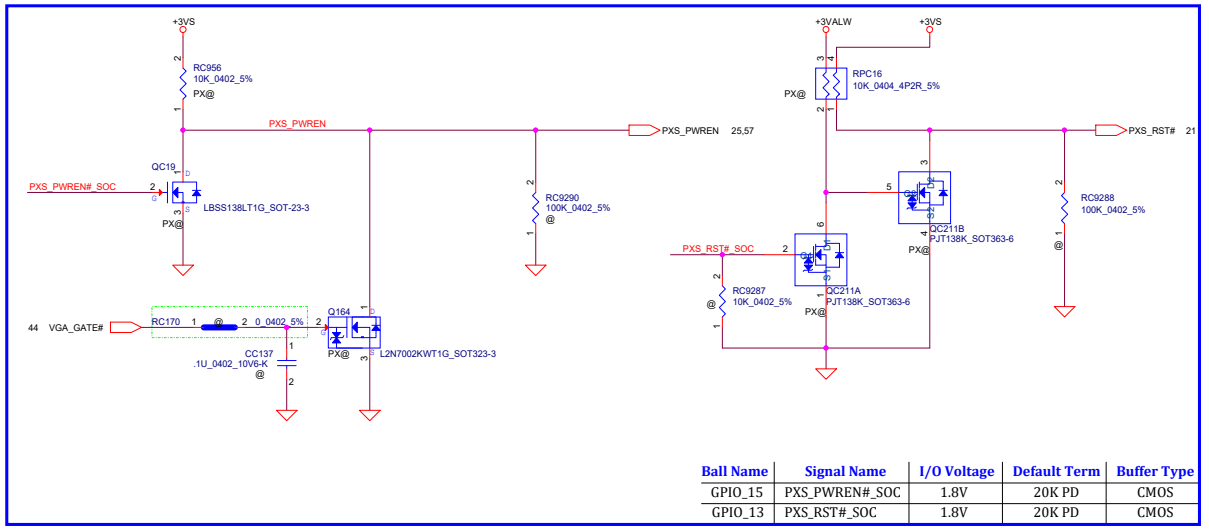
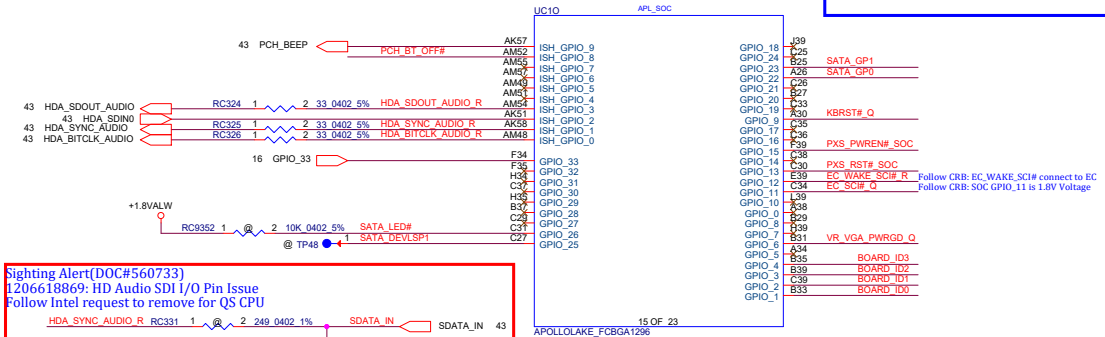
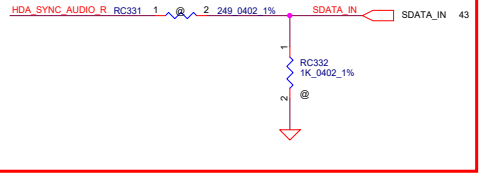


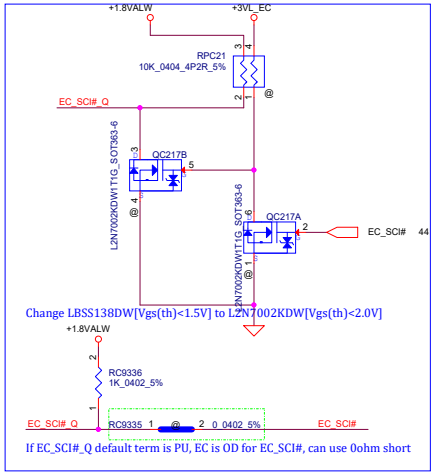


Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
GPIO_15	PXS_PWREN#_SOC	1.8V	20K PD	CMOS
GPIO_13	PXS_RST#_SOC	1.8V	20K PD	CMOS



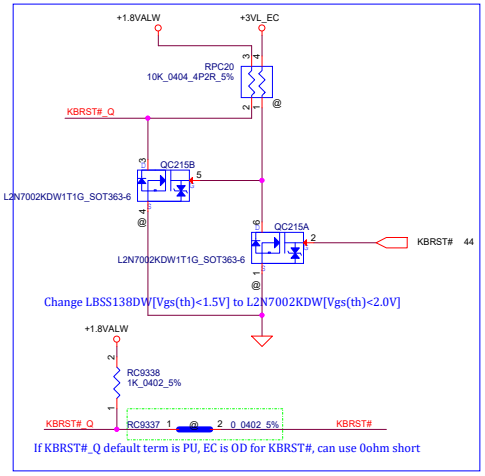
Sighting Alert(DOC#560733)
1206618869: HD Audio SDI I/O Pin Issue
Follow Intel request to remove for QS CPU





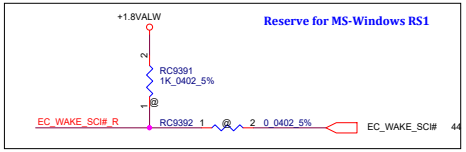
Change LBSS138DW[Vgs(th)<1.5V] to L2N7002KDW[Vgs(th)<2.0V]

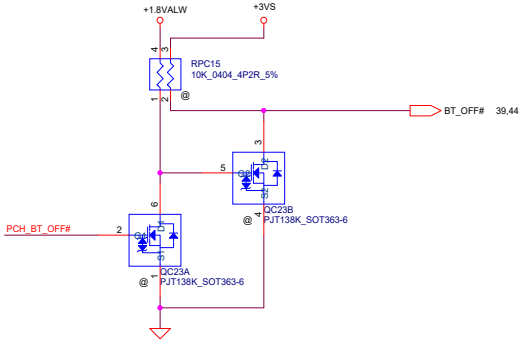
If EC_SCI#_Q default term is PU, EC is OD for EC_SCI#, can use 0ohm short

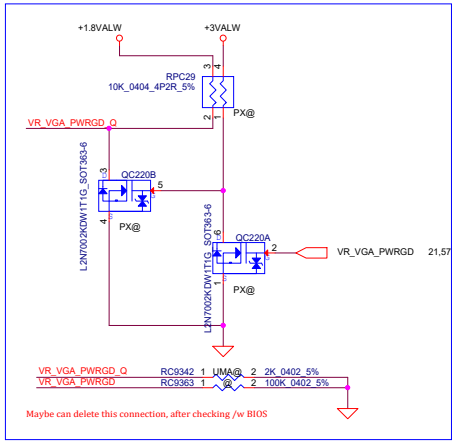


Change LBSS138DW[Vgs(th)<1.5V] to L2N7002KDW[Vgs(th)<2.0V]

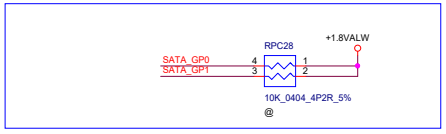
If KBRST#_Q default term is PU, EC is OD for KBRST#, can use 0ohm short



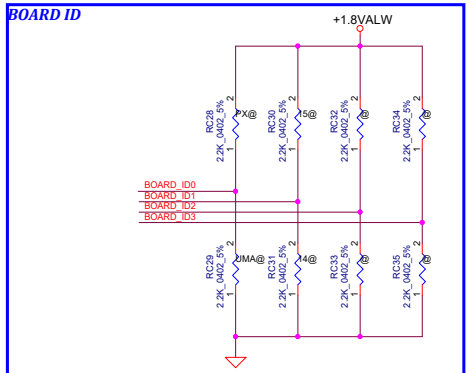




Maybe can delete this connection, after checking /w BIOS



BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description
0		Reserve	Reserve	UMA SKU
1				GPU SKU
	0			14" Panel
	1			15" Panel



Security Classification	LC Future Center Secret Data		
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Title: P12-SOC (GPIO&HDA)

Size	Document Number	Rev
C	CG414&CG514	1.0

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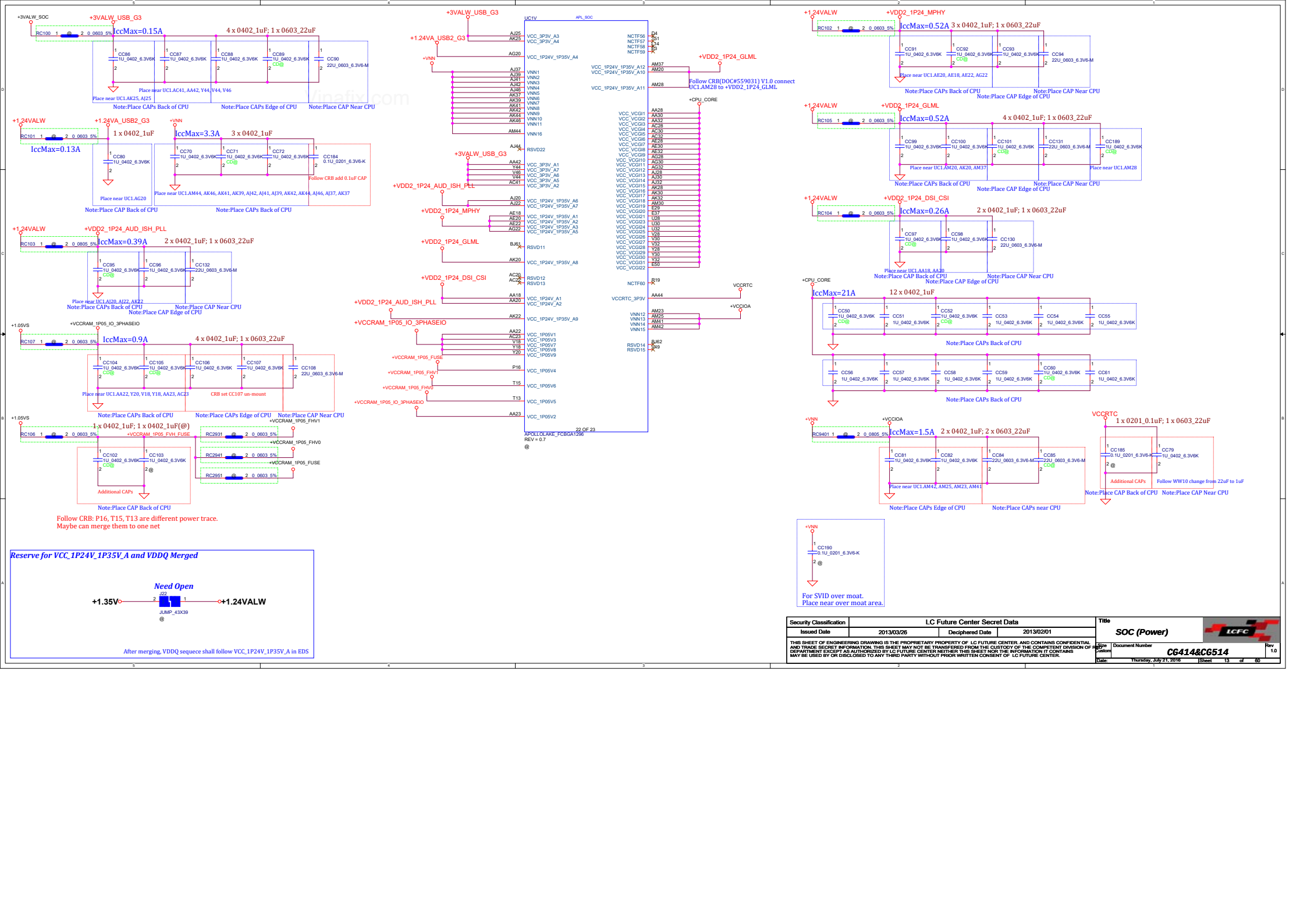
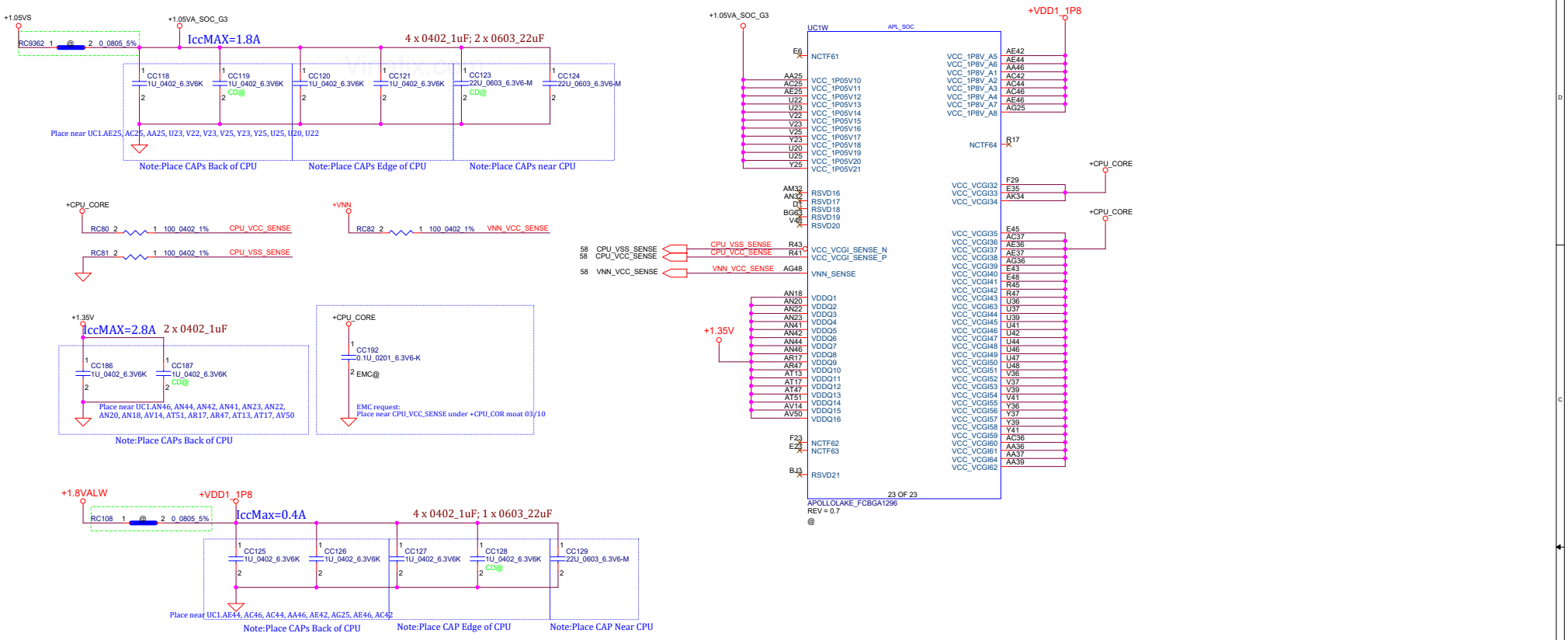


Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

Title	SOC (Power)		
Size: Custom	Document Number	CG414&CG514	Rev 1.0
Date: Thursday, July 21, 2016	Sheet 13 of 60		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

Title	SOC (Power2)		
Size C	Document Number CG414&CG514		Rev 1.0
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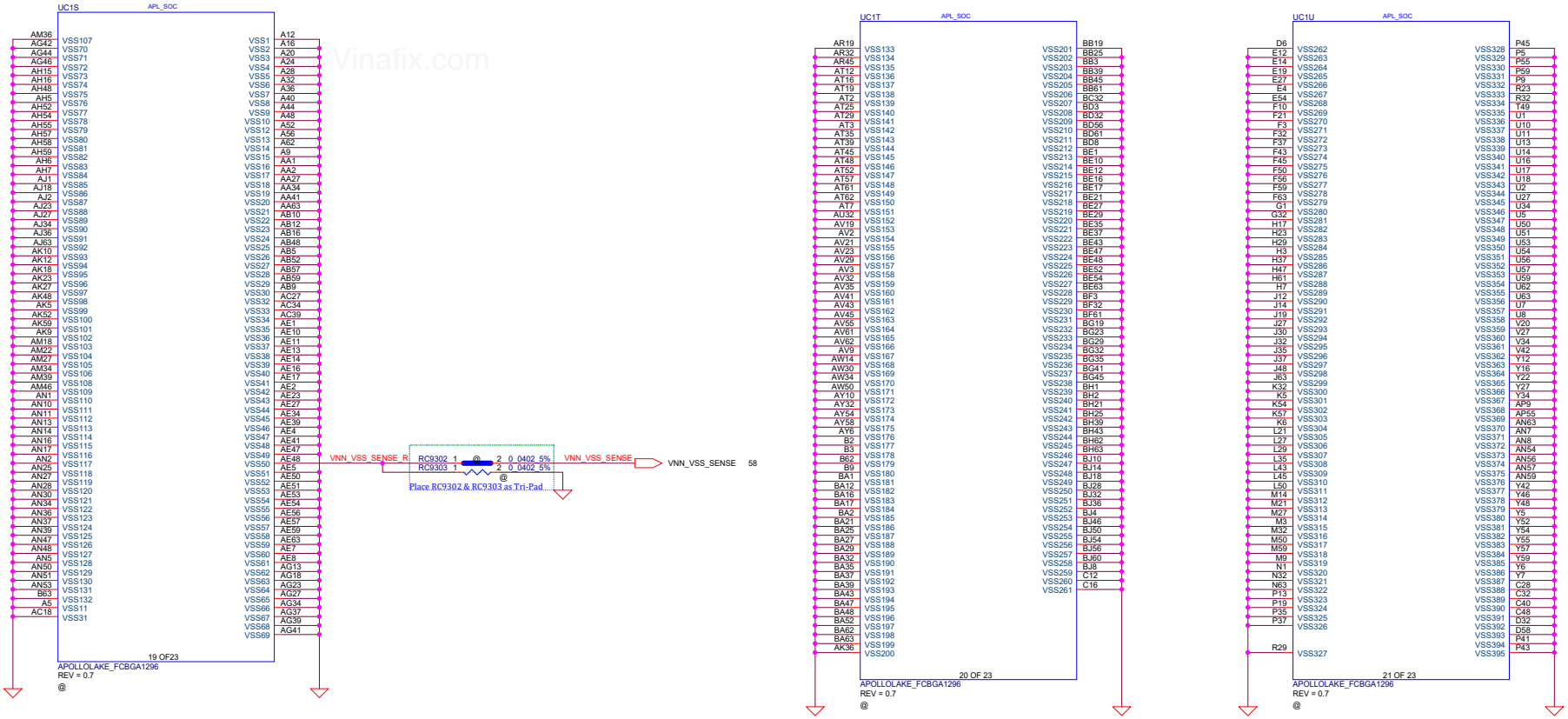

Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

Title: **SOC (VSS)**

Size	Document Number	Rev
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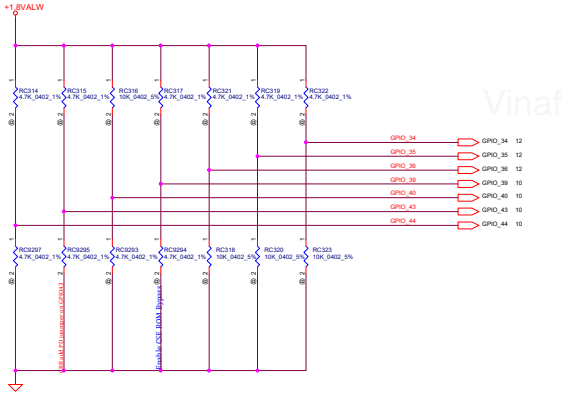
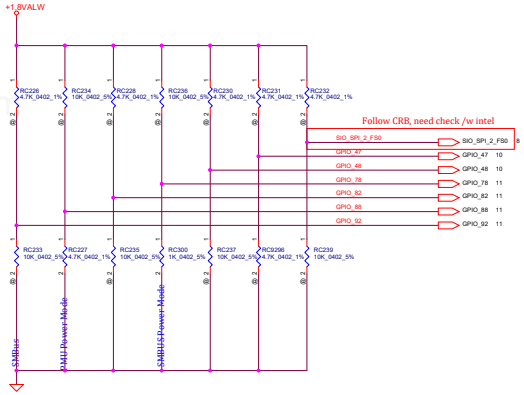
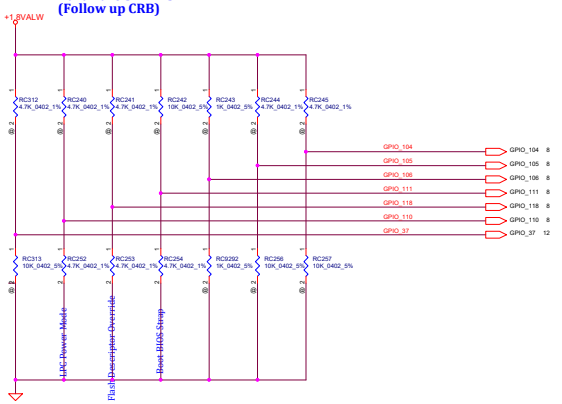
Hardware STRAPS (Follow up CRB)

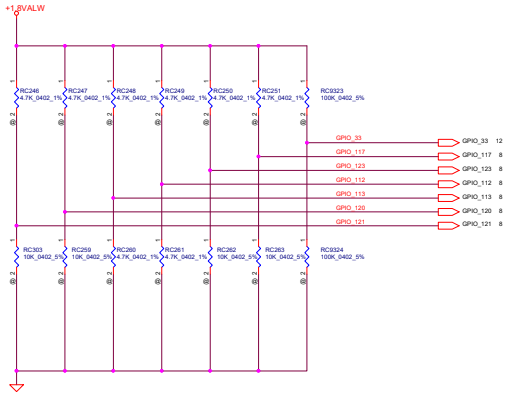




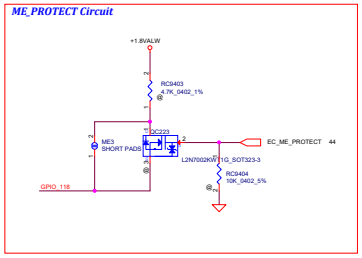
GPIO#	Purpose	Internal Termination	Schematics Setting	Pin usage	Remark
GPIO_33	RSVD	20K PD	Floating	N/A	Follow CRB(DOC#: 561386); EDS(v1.5) P56
GPIO_34	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v1.5) P45 & P56
GPIO_35	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v1.5) P45 & P56
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	Floating	1 = 1.35V 0 = 1.24V(Default)*	EDS(v1.5) P45 & P57
GPIO_37	RSVD	20K PD	Floating	N/A	Follow CRB(DOC#: 561386); EDS(v1.5) P57
GPIO_39	Enable CSE ROM Bypass	20K PU (PDG V1.2 P363)	Floating	1 = Enable bypass 0 = Disable bypass (default)	This strap tells CSE (TXE3.0) to bypass ROM EDS(v1.5) P45&P57
GPIO_40	RSVD	20K PU (PDG V1.2 P363)	Floating	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	EDS(v1.5) P45 & P57
GPIO_43	Allow eMMC as a boot source	20K PU	4.7K PD	1 = Enable(Default) 0 = Disable*	On platforms with both eMMC and SPI flash Device present: GPIO_43 and GPIO_44 are at default--eMMC Boot; GPIO_43 = 0 and GPIO_44 = 1--SPI Boot. PDG(v1.0) P369;EDS(v1.0) P42 & P51
GPIO_44	Allow SPI as a boot source	20K PU	Floating	1 = Enable(Default)* 0 = Disable	
GPIO_47	Force DNX FW Load	20K PU (PDG V1.2 P363)	Floating	1 = Force 0 = Do not force(Default)*	Recovery strap for corrupted FW image PDG(v1.0) P372;EDS(v1.0) P42 & P51
GPIO_48	RSVD	20K PU (PDG V1.2 P363)	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P42 & P51
GPIO_78	SMBus 1.8V/3.3V mode select	20K PD (PDG V1.2 P363)	1K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. SMBus signals are 3.3V mode. EDS(v1.0) P29 & P42 & P48
GPIO_82	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v1.0) P42 & P48
GPIO_88	PMU 1.8V/3.3V mode select	20K PD (PDG V1.2 P363)	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. PMU signals are 3.3V mode. EDS(v1.0) P39 & P42 & P49
GPIO_92	SMBus No Re-Boot	20K PD	Floating	1 = Enable 0 = Disable(Default)*	Should strap this pin LOW. Functionality is handled by the PMC. EDS(v1.0) P43 & P49
GPIO_104	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_105	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_106	RSVD	20K PD (PDG V1.2 P363)	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_110	LPC 1.8V/3.3V mode select	20K PD (PDG V1.2 P363)	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. LPC signals are 3.3V mode. EDS(v1.0)) P41 & P43 & P49
GPIO_111	Boot BIOS Strap (BBS)	20K PD (PDG V1.2 P363)	4.7K PD	1 = Do not boot from SPI (default) 0 = Boot from SPI*	EDS(v1.0) P43 & P49
GPIO_112	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_113	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_117	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P49
GPIO_118	Flash Descriptor Override	20K PD	Floating	0 = No Override (Normal Operation)* 1 = Override	This strap enables the platform to override security features in the SPI. EDS(v1.0) P43 & P49
GPIO_120	Top swap override	20K PD	Floating	1 = Enable 0 = Disable (default)*	This strap enables platform to change different SPI ROM location. ESD(v1.0) P43 & P50
GPIO_121	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43 & P50
GPIO_123	RSVD	20K PD (PDG V1.2 P363)	Floating	Ensure this strap is PU when RSM_RST_N de-asserts for normal platform operation	EDS(v1.0) P43

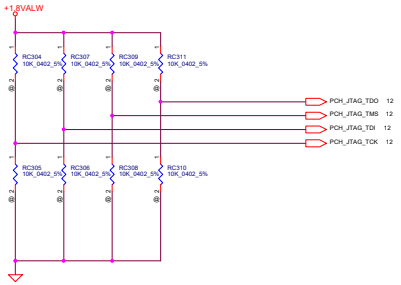
Hardware STRAPS (Follow up CRB)





ME_PROTECT Circuit





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Title	SOC (STRAPS & OTHERS)		
Size: Custom	Document Number: CG414&CG6514		Rev: 1.0
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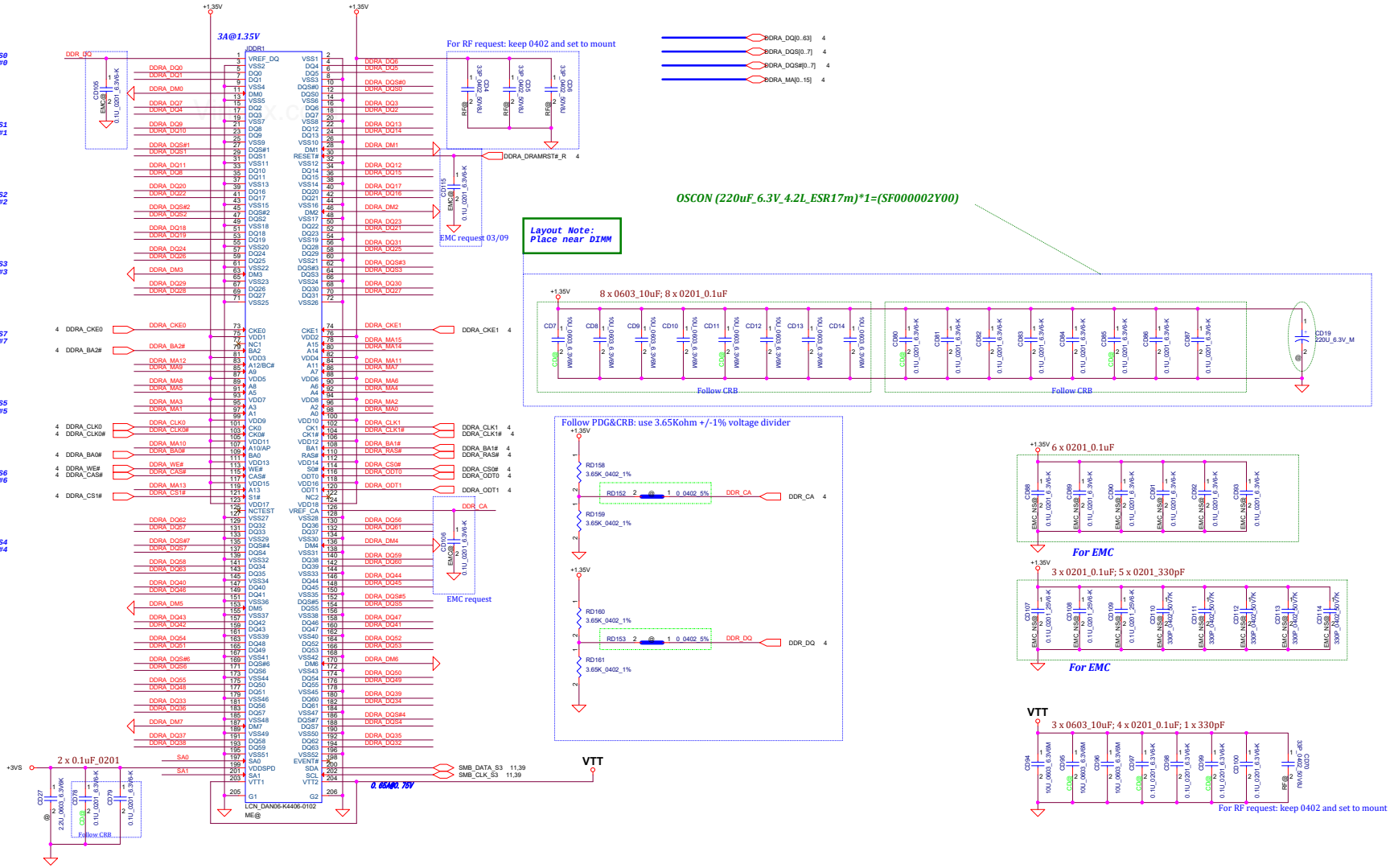
DDR Mapping table

DDRA_DQ0---DQ0		
DDRA_DQ1---DQ1		
DDRA_DQ2---DQ7		
DDRA_DQ3---DQ6	DDRA_DQS0 ---DQS0	
DDRA_DQ4---DQ2	DDRA_DQS0#---DQS#0	
DDRA_DQ5---DQ5		
DDRA_DQ6---DQ4		
DDRA_DQ7---DQ3		
DDRA_DQ8 ---DQ11		
DDRA_DQ9 ---DQ8		
DDRA_DQ10---DQ9		
DDRA_DQ11---DQ10	DDRA_DQS1 ---DQS1	
DDRA_DQ12---DQ14	DDRA_DQS1#---DQS#1	
DDRA_DQ13---DQ12		
DDRA_DQ14---DQ13		
DDRA_DQ15---DQ15		
DDRA_DQ16---DQ21		
DDRA_DQ17---DQ20		
DDRA_DQ18---DQ18		
DDRA_DQ19---DQ19	DDRA_DQS2 ---DQS2	
DDRA_DQ20---DQ16	DDRA_DQS2#---DQS#2	
DDRA_DQ21---DQ23		
DDRA_DQ22---DQ17		
DDRA_DQ23---DQ22		
DDRA_DQ24---DQ24		
DDRA_DQ25---DQ29		
DDRA_DQ26---DQ25		
DDRA_DQ27---DQ31	DDRA_DQS3 ---DQS3	
DDRA_DQ28---DQ27	DDRA_DQS3#---DQS#3	
DDRA_DQ29---DQ26		
DDRA_DQ30---DQ30		
DDRA_DQ31---DQ28		
DDRA_DQ32---DQ63		
DDRA_DQ33---DQ56		
DDRA_DQ34---DQ61		
DDRA_DQ35---DQ62	DDRA_DQS4 ---DQS7	
DDRA_DQ36---DQ57	DDRA_DQS4#---DQS#7	
DDRA_DQ37---DQ58		
DDRA_DQ38---DQ59		
DDRA_DQ39---DQ60		
DDRA_DQ40---DQ40		
DDRA_DQ41---DQ47		
DDRA_DQ42---DQ43		
DDRA_DQ43---DQ42	DDRA_DQS5 ---DQS5	
DDRA_DQ44---DQ46	DDRA_DQS5#---DQS#5	
DDRA_DQ45---DQ45		
DDRA_DQ46---DQ41		
DDRA_DQ47---DQ44		
DDRA_DQ48---DQ51		
DDRA_DQ49---DQ55		
DDRA_DQ50---DQ54		
DDRA_DQ51---DQ49	DDRA_DQS6 ---DQS6	
DDRA_DQ52---DQ52	DDRA_DQS6#---DQS#6	
DDRA_DQ53---DQ53		
DDRA_DQ54---DQ48		
DDRA_DQ55---DQ50		
DDRA_DQ56---DQ36		
DDRA_DQ57---DQ33		
DDRA_DQ58---DQ34		
DDRA_DQ59---DQ38	DDRA_DQS7 ---DQS4	
DDRA_DQ60---DQ39	DDRA_DQS7#---DQS#4	
DDRA_DQ61---DQ37		
DDRA_DQ62---DQ32		
DDRA_DQ63---DQ35		



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Title: DDRIII SO-DIMM A

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Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: Blank

Size: Custom	Document Number: C6414&C6514	Rev: 1.0
Date: Thursday, July 31, 2014	Sheet 18 of 60	

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2014/01/21

Title: ***Blank***

Size	Document Number	Rev
C	CG414&CG514	1.0

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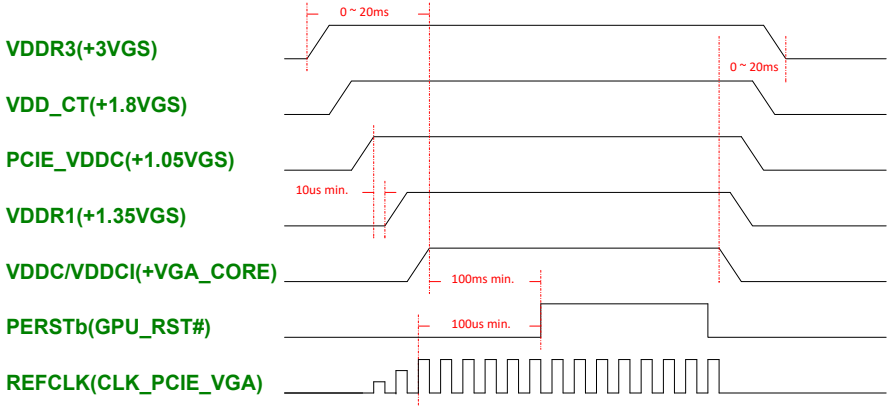
Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µs).
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Title: VGA Notes List

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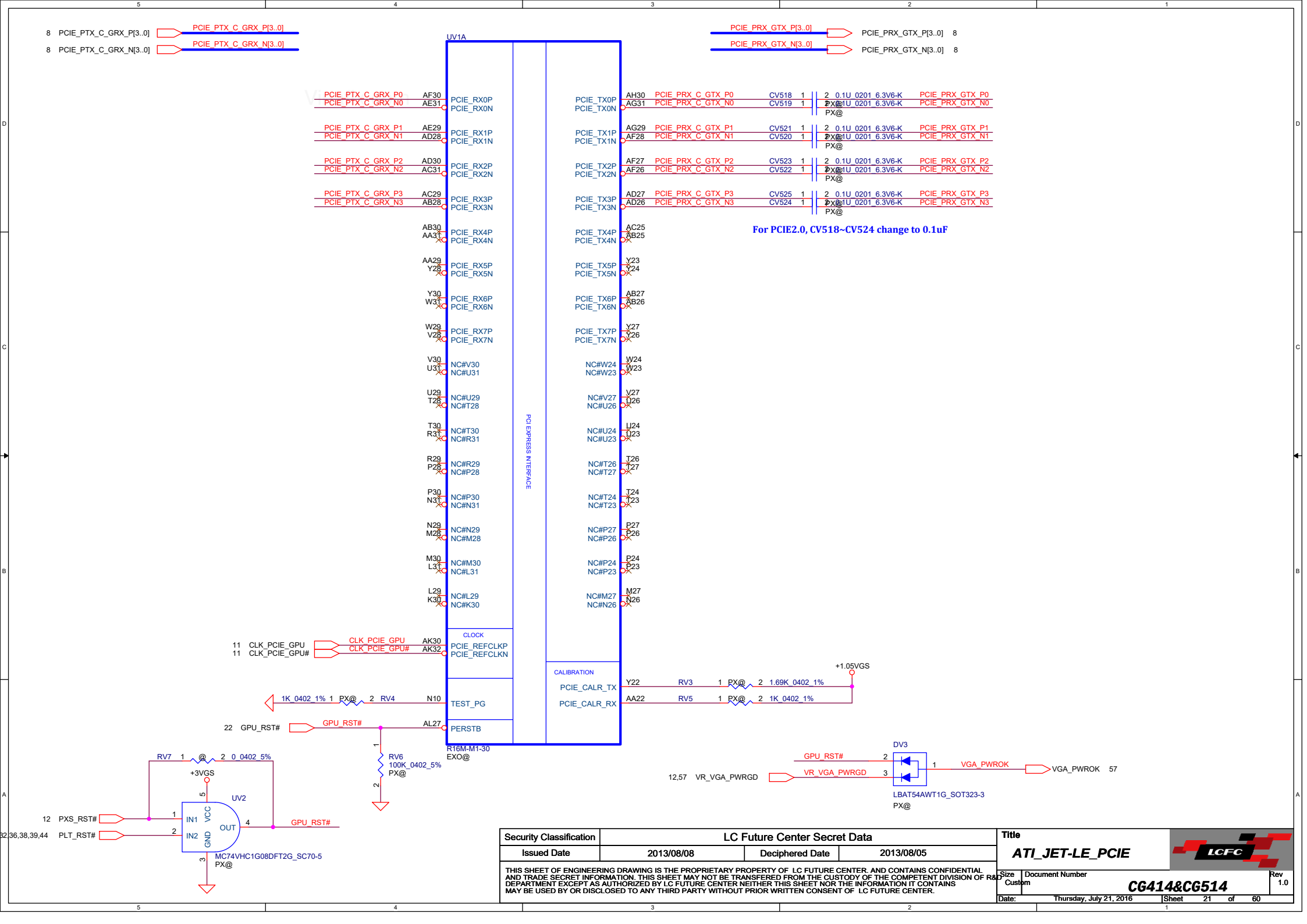

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_PCIE

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Custom	CG414&CG514	1.0

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
N/A = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. 111= No usable endpoints.	11

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu( )	R_pd( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=NC	RV77=4.75K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=X76

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Internal VGA Thermal Sensor

Connect GPIO_28 to 10K pull down to enable MLPS.

no symbol for 8pf cap, PLM has PN,change the PN

(1.8V@20mA TSVDD)

Pull down for none OBFF design

Reserve for Topaz

For Topaz, RV16/RV19 stuff 100ohm
for EXO, RV16/RV19 stuff 0hm.

Delete APU_SHUTDOWN# for AMD Platform

Security Classification	LC Future Center Secret Data		
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Title: ATI_JET-LE_Main_MSIC

Size: Custom | Document Number: CG414&CG514 | Rev: 1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_TMDP

Size: Custom	Document Number: CG414&CG514	Rev: 1.0
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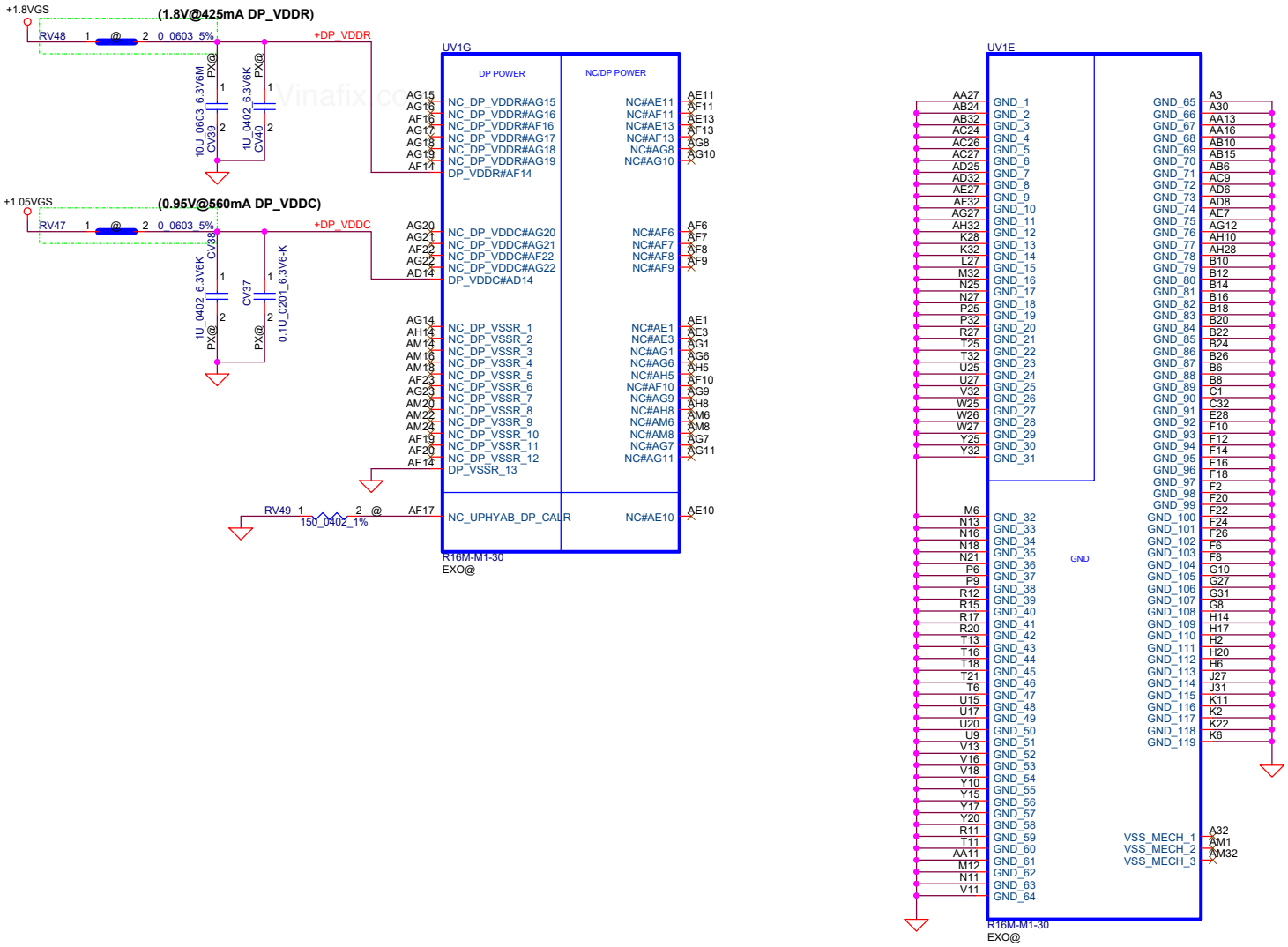

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_DP Power

Size	Document Number	Rev
Custom	CG414&CG514	1.0

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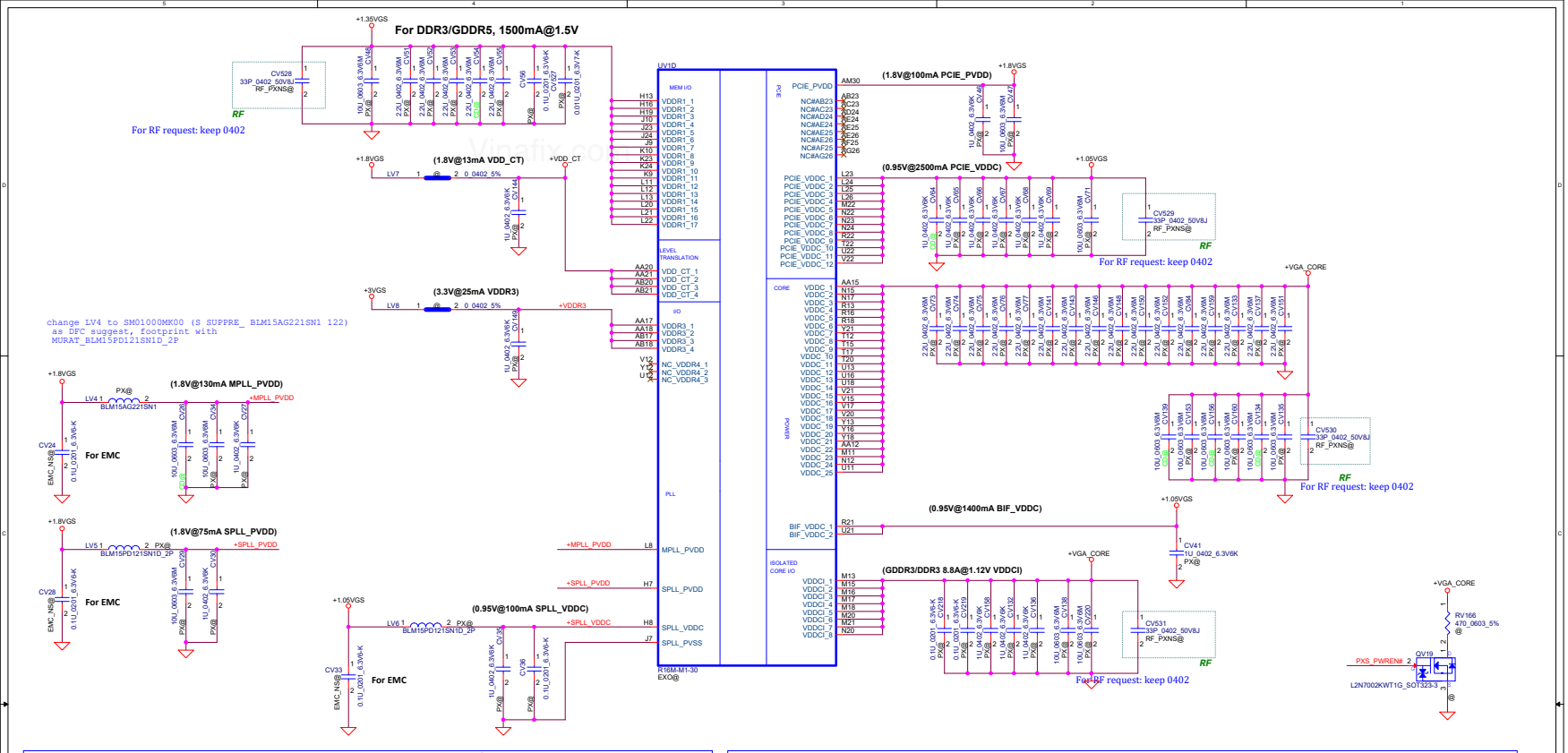

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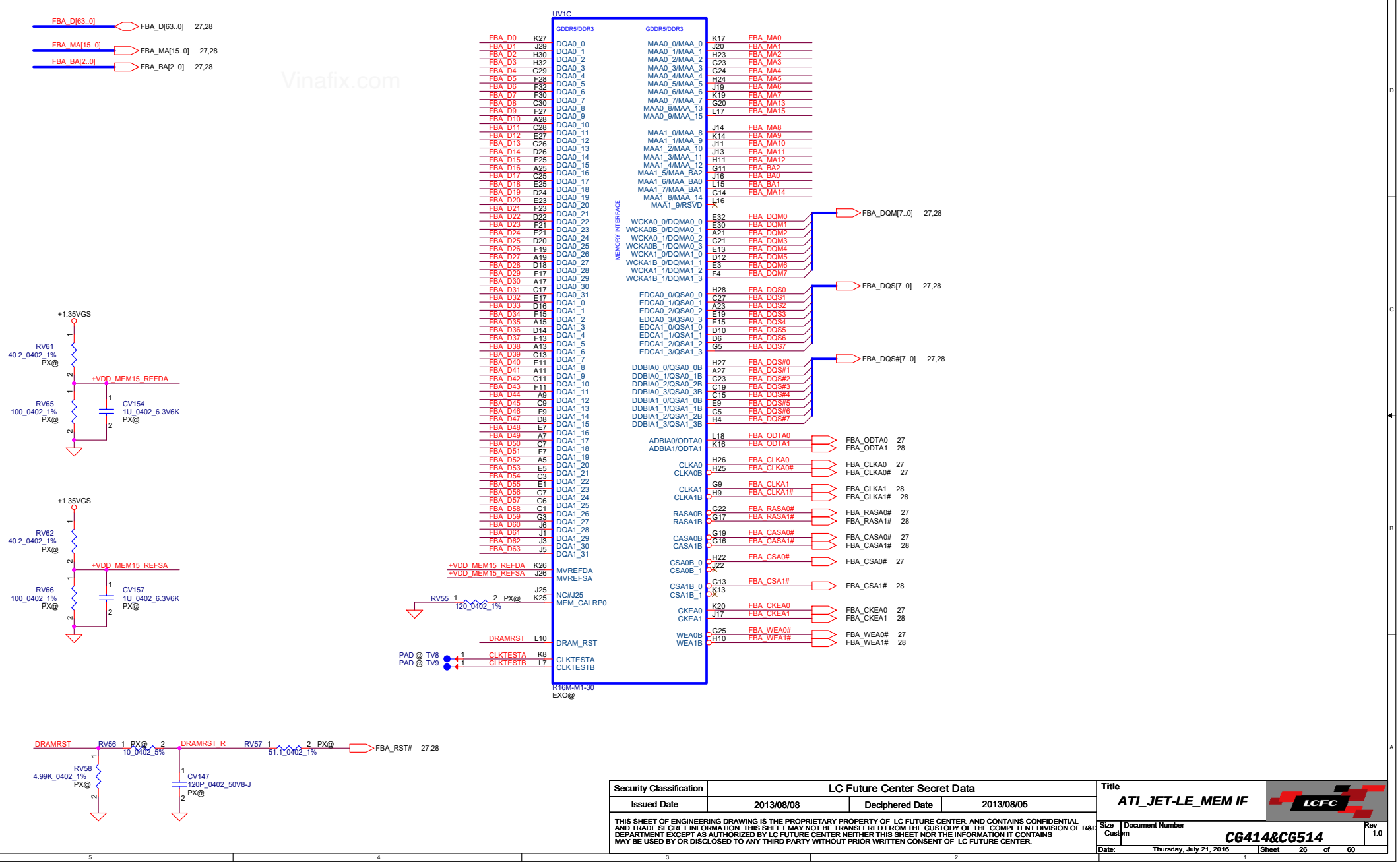

Security Classification	LC Future Center Secret Data		
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Title: ATI_JET-LE_MEM IF

Size	Document Number	Rev
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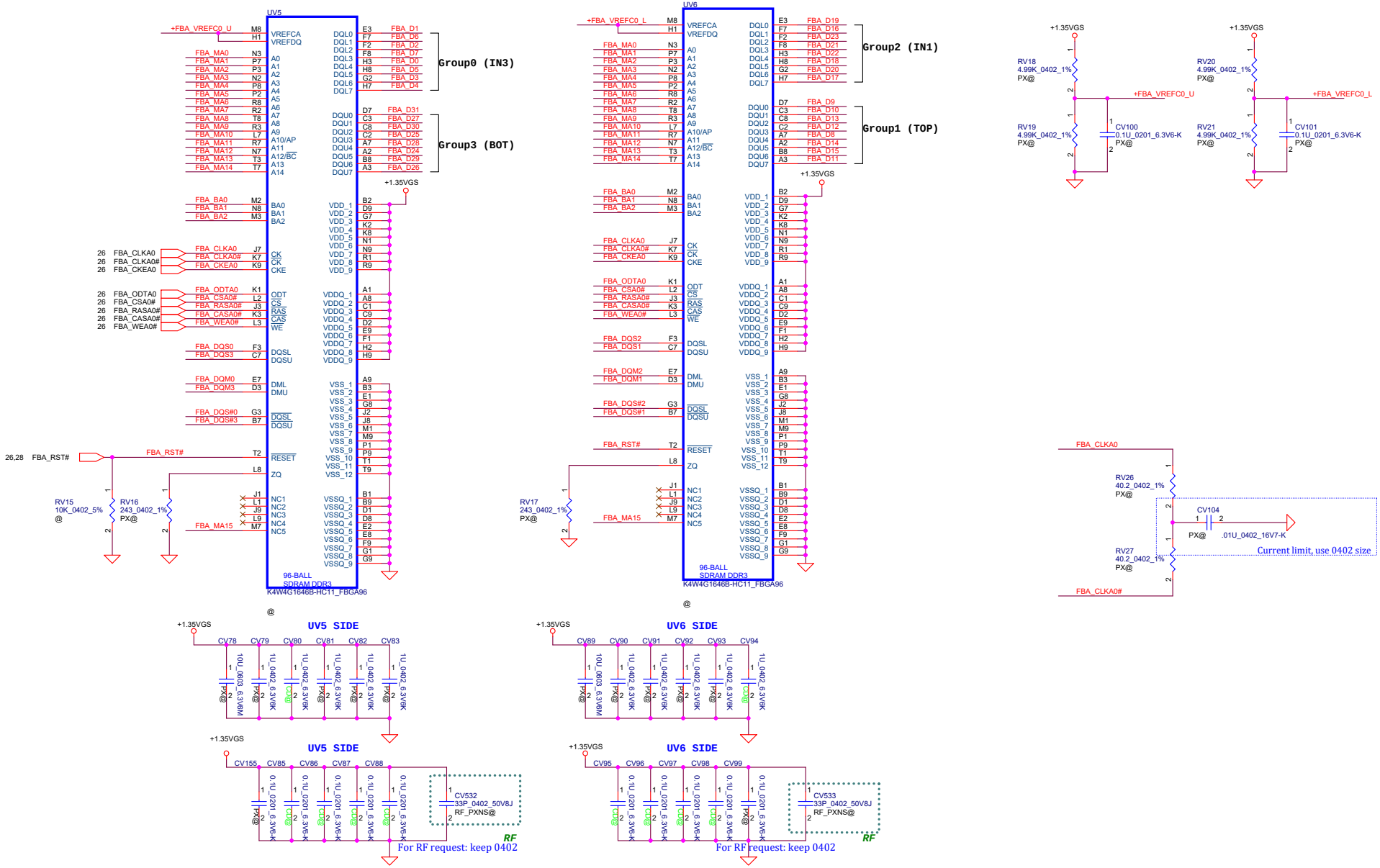
Memory Partition A - Lower 32 bits

FBA_MA[15..0] 26,28
FBA_BA[2..0] 26,28
FBA_DQS[3..0] 26
FBA_DQM[3..0] 26
FBA_DQS#[3..0] 26
FBA_D[31..0] 26



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_A

Size: Custom | Document Number: CG414&CG514 | Rev: 1.0

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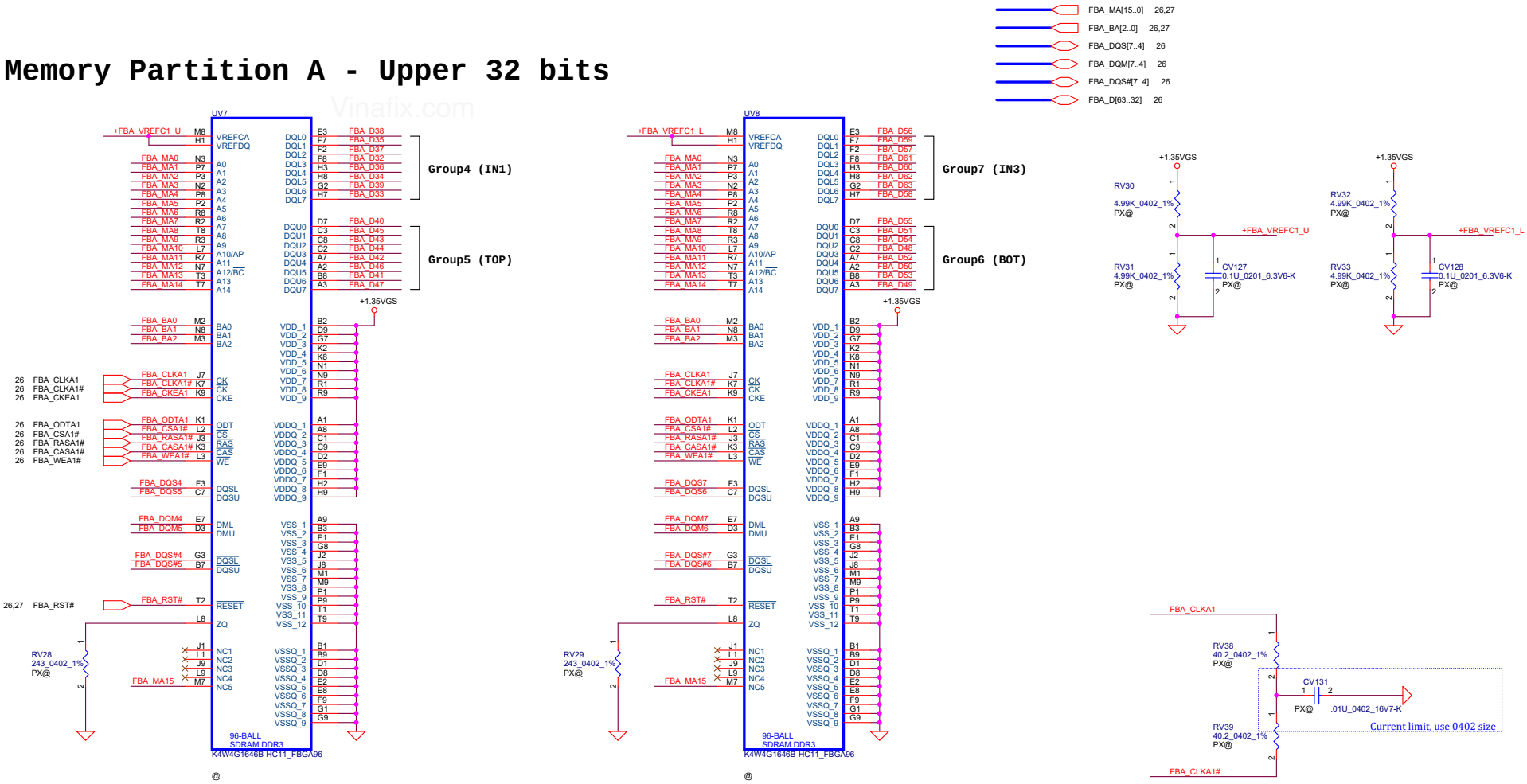
Memory Partition A - Upper 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_B

Size: Custom | Document Number: CG414&CG514 | Rev: 1.0

Date: Thursday, July 21, 2016 | Sheet 28 of 60

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2014/01/21

Title: ***Blank***

Size	Document Number	Rev
C	CG414&CG514	1.0

Date: Thursday, July 21, 2016 | Sheet 29 of 60

Security Classification	LC Future Center Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/11

Title

VGA Notes List

Size	Document Number	Rev
C	***CG414&CG514***	1.0

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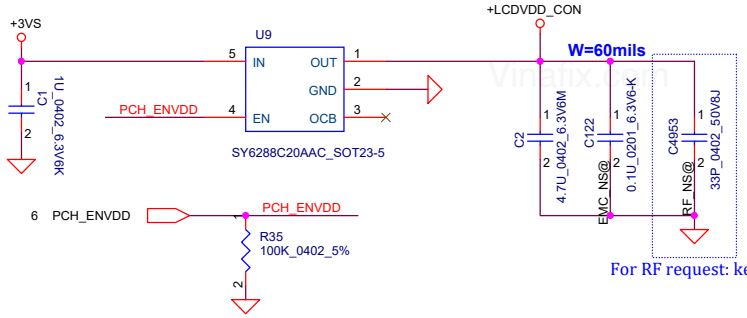
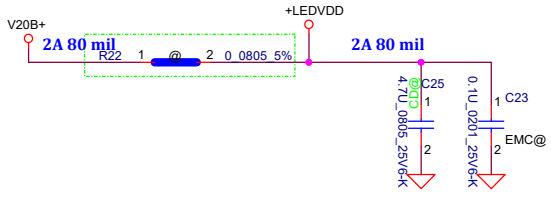
LCD POWER CIRCUIT



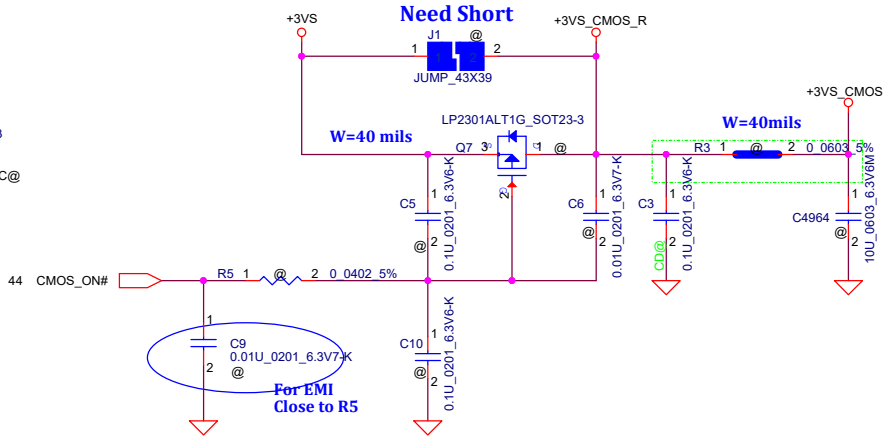
For RF request: keep 0402

B+ to +LEDVDD POWER

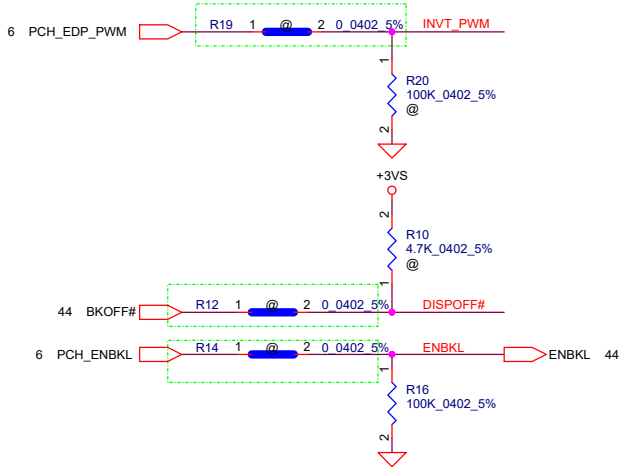


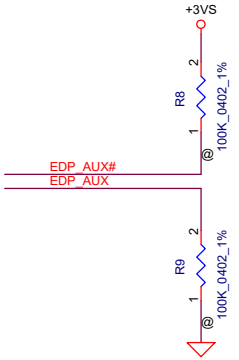
C23 0.1u for G HSW panel blink issue

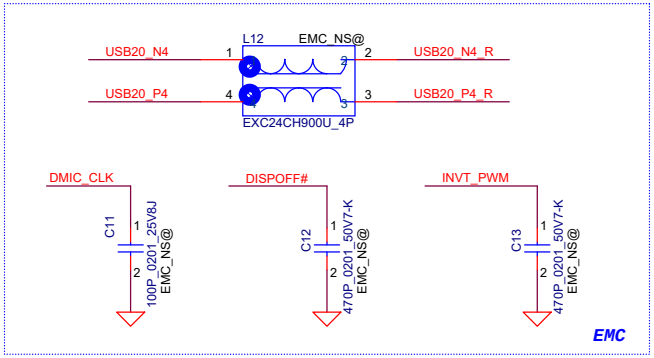
CMOS CAMERA



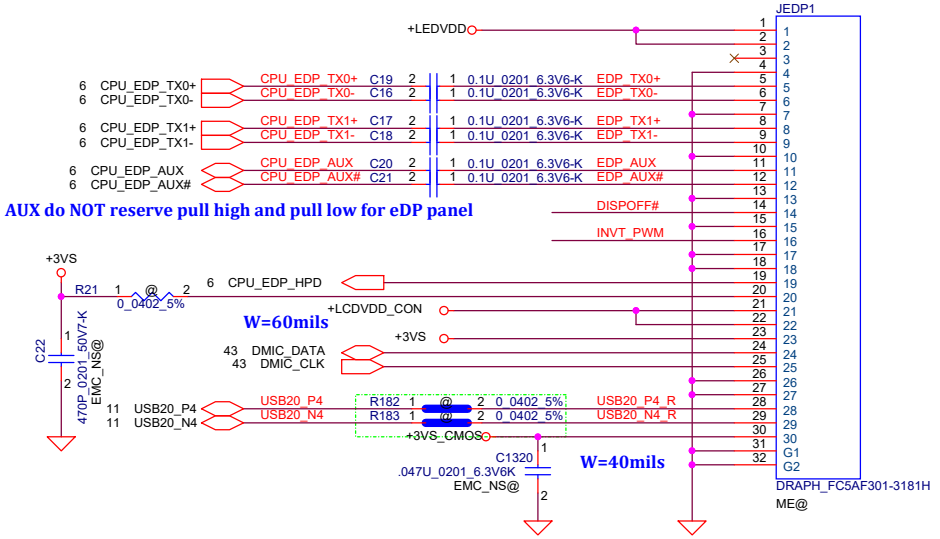
APL SoC output enable Voh min is 1.8V-0.45V=1.35V







EMC



AUX do NOT reserve pull high and pull low for eDP panel

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	eDP/CMOS		
Size	Document Number		Rev
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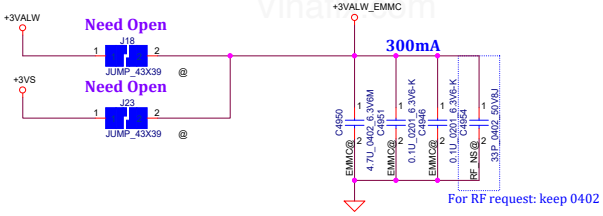
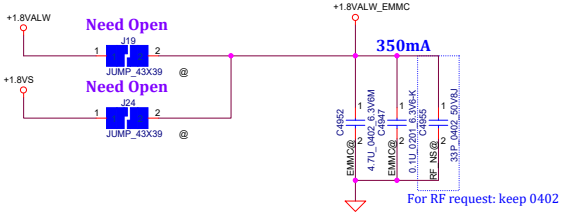
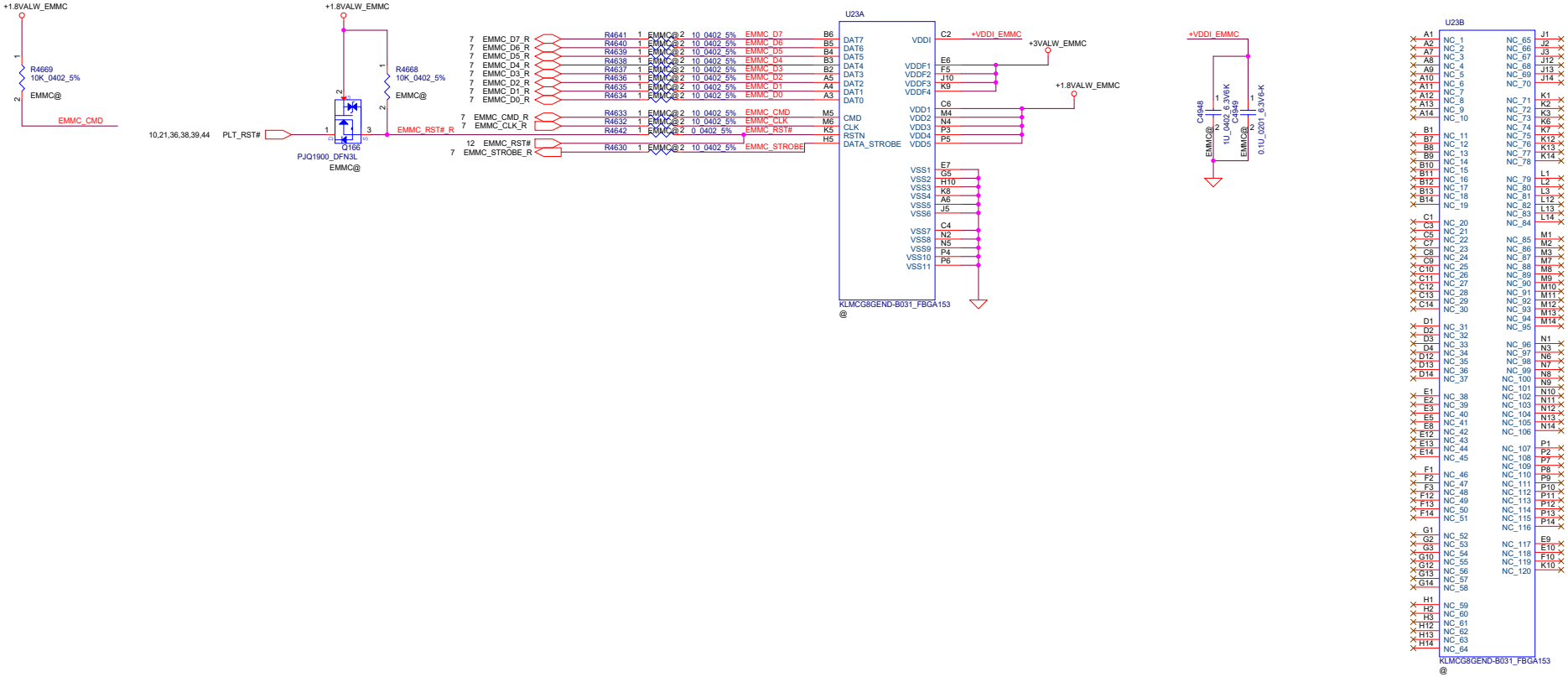
Date:	Thursday, July 21, 2016	Sheet	31 of 60

For Leovo Request: Design Reserved





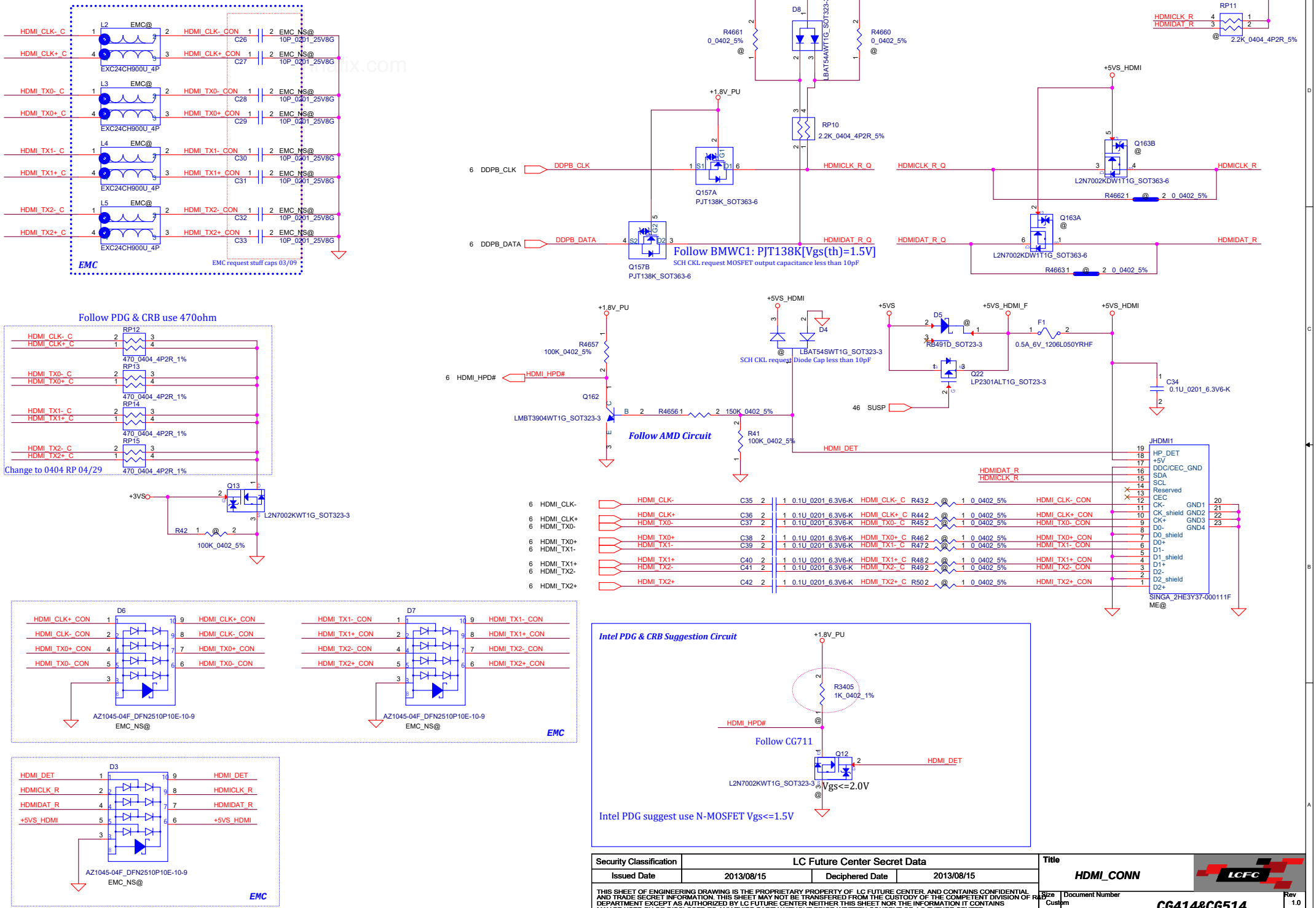


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *eMMC*

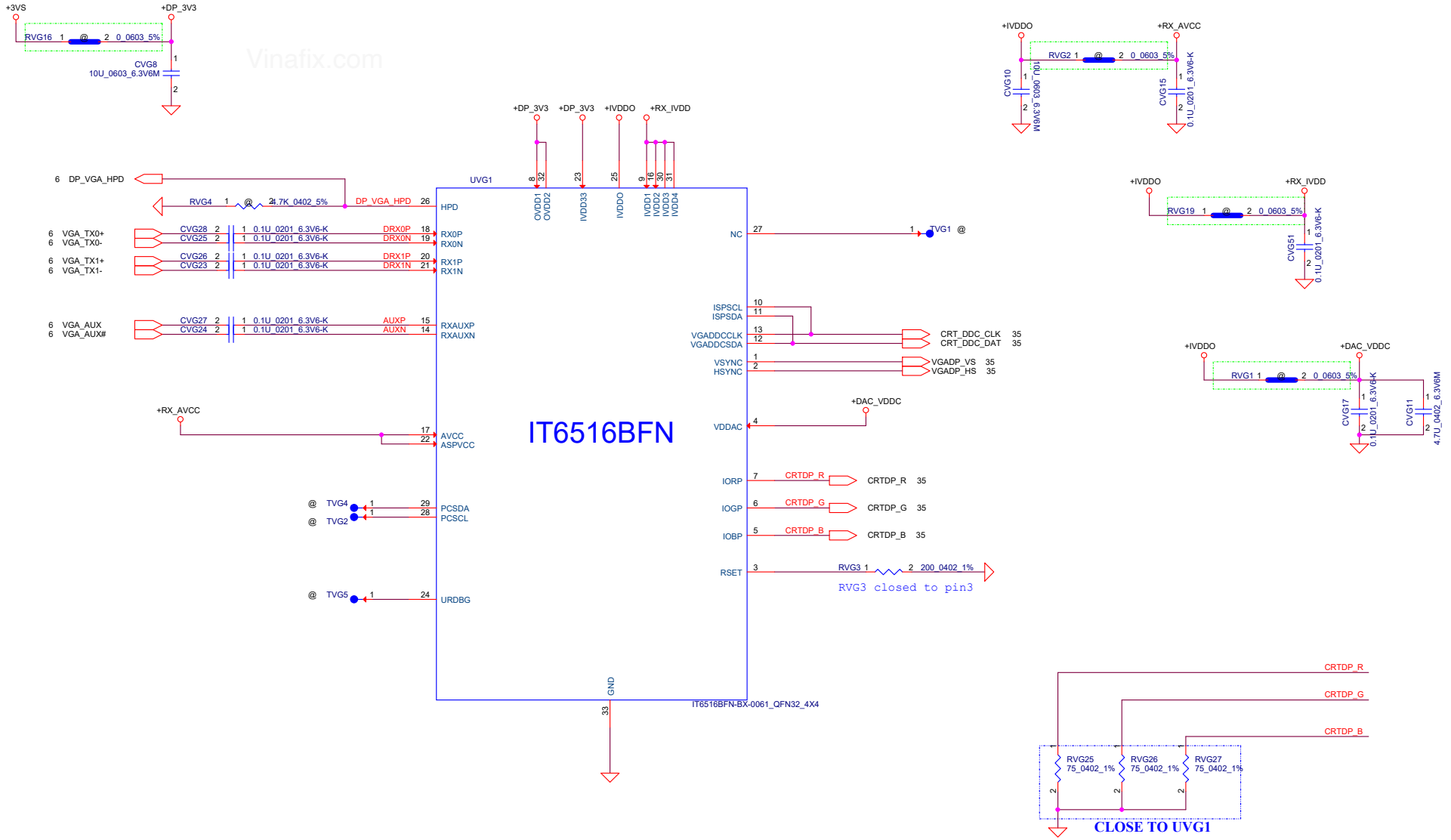
Size	Document Number	Rev
C	CG414&CG514	1.0

Date: Thursday, July 21, 2016 Sheet 32 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	HDMI_CONN		
Size	Document Number		Rev
Custom	CG414&CG514		1.0
Date:	Thursday, July 21, 2016	Sheet	33 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: DP to CRT Convert(IT6515FN)

Size	Document Number	Rev
Custom	CG414&CG514	1.0

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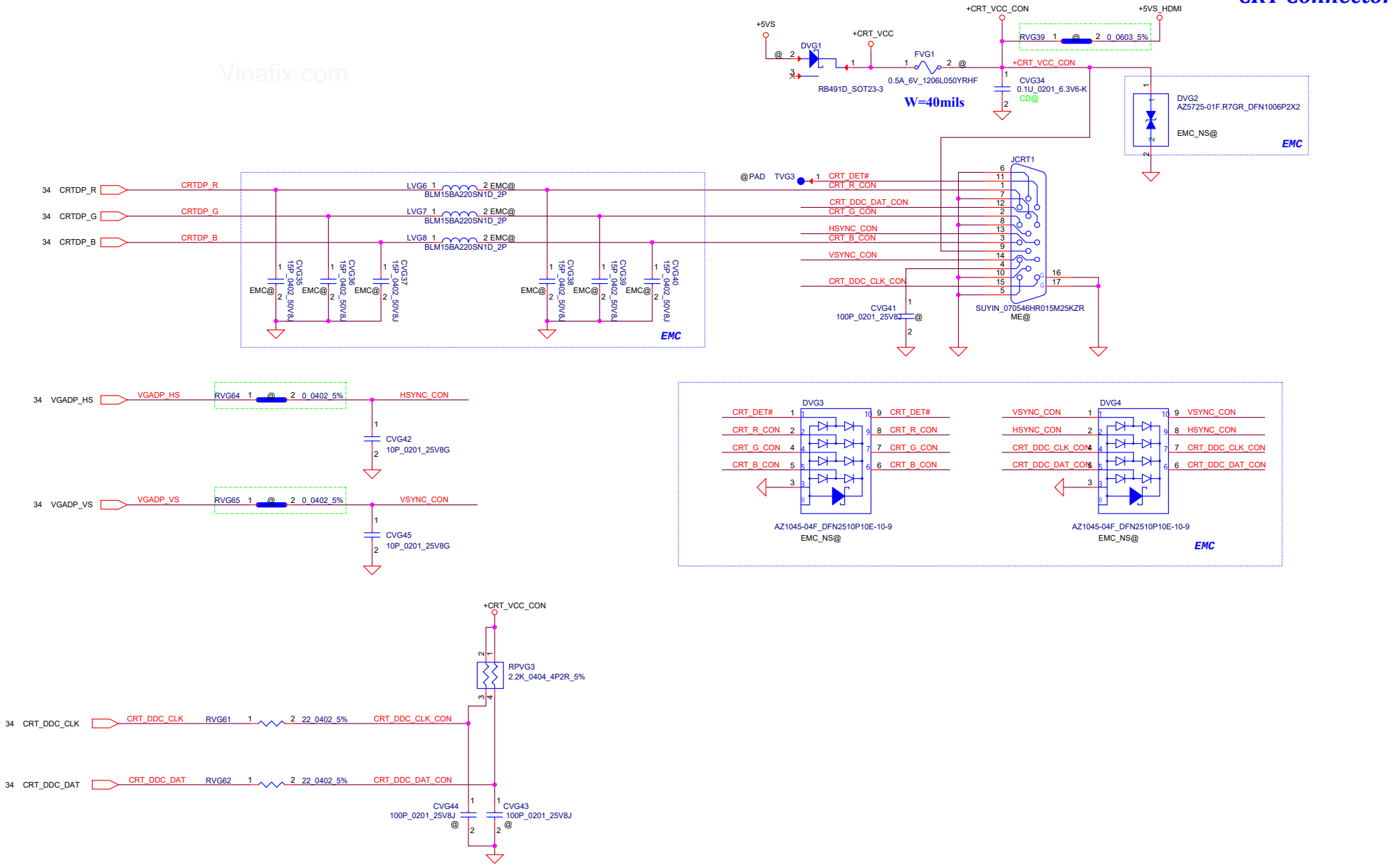
CRT Connector

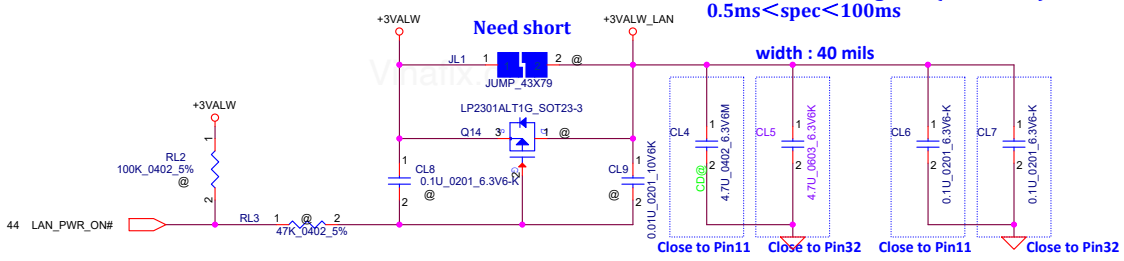


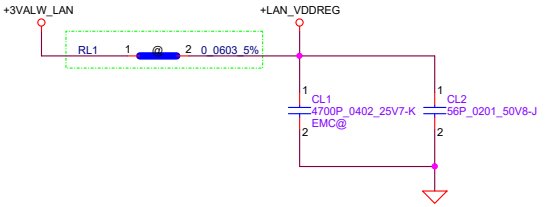
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

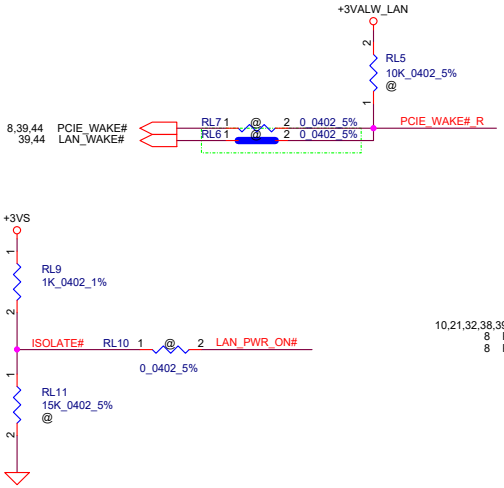
Title	CRT		
Size	Document Number		Rev
Custom	CG414&CG514		1.0
Date:	Thursday, July 21, 2016	Sheet	35 of 60

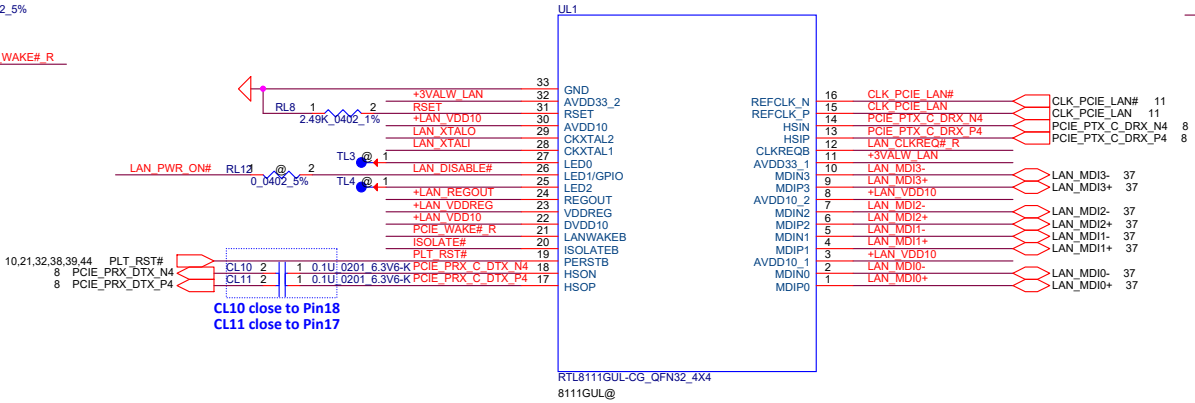
+3VALW TO +3VALW_LAN

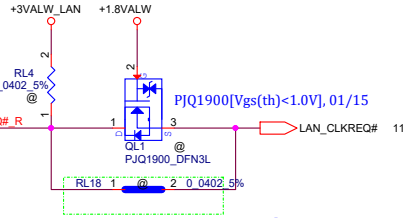
+3VALW_LAN rising time (10%~90%): 0.5ms＜spec＜100ms



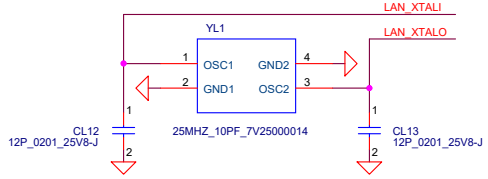








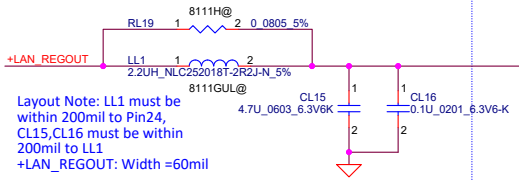
Modify caps for LAN power noise issue:
1. CL17 change from un-mount 0201 0.1uF to 0201 56pF;
2. CL18 Change from 0201 0.1uF to 0201 4.7nF;
3. CL21 change from un-mount 0402 1uF to 0402 1uF;
4. CL5 change from un-mount 0402 4.7uF to 0603 4.7uF;
5. CL1 change from 4.7uF 0402 to 0603 4.7nF;
6. CL2 change from 0201_0.1uF to 0201 56pF.



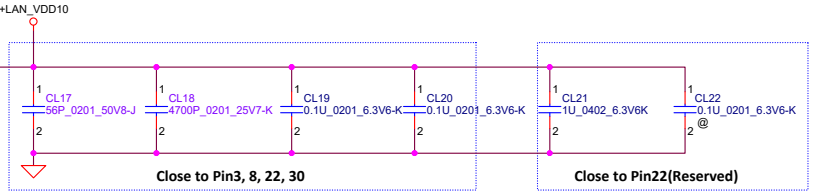
25MHz Crystal--TXC SJ10000G500

Follow common pool change 25MHz X'tal from EPSON to TXC. 03/01

For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuff



Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **LAN_RTL8111GUL**

Size	Document Number	Rev
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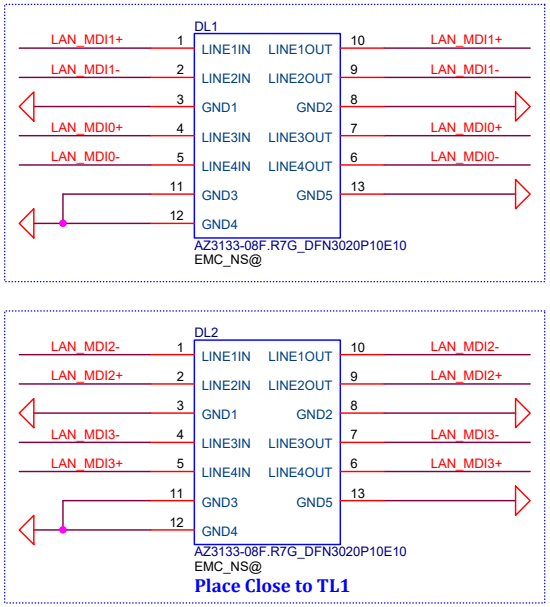
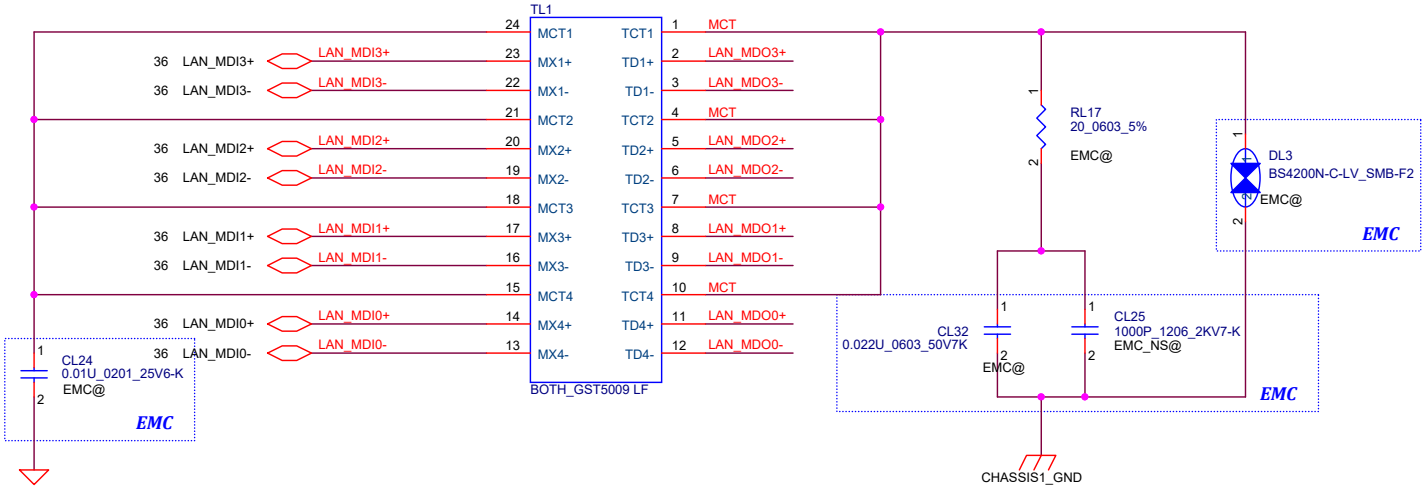
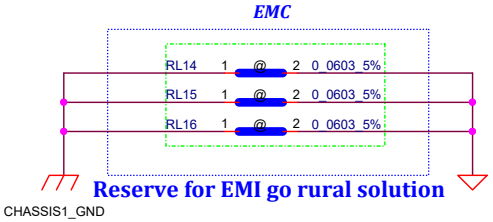
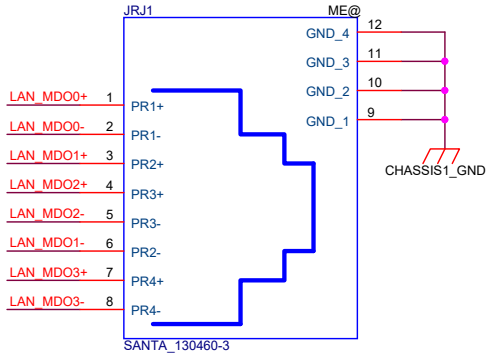
DL1/DL2
1'S PN:SC300004X00









Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_Transformer

Size	Document Number	Rev
B	CG414&CG514	1.0

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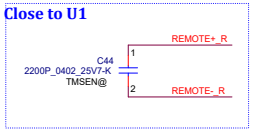
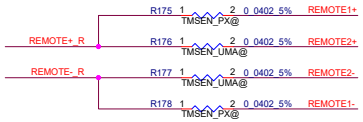
THERMAL SENSOR

Close to U1

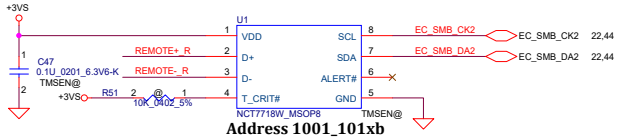


Set Thermal Sensor as a BOM Structure



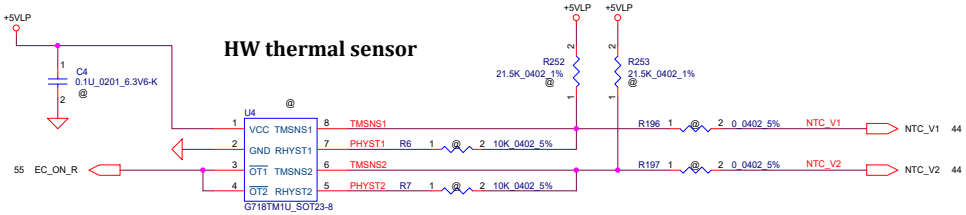
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM



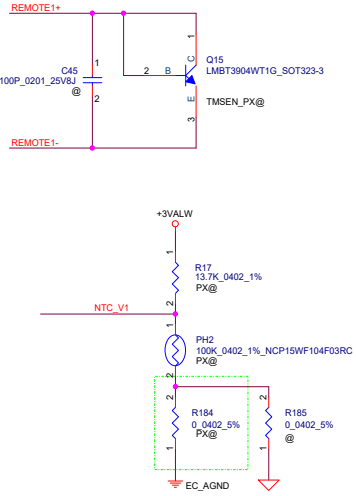
Address 1001_101xb

HW thermal sensor

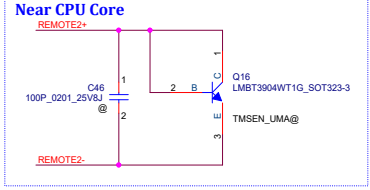


Over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

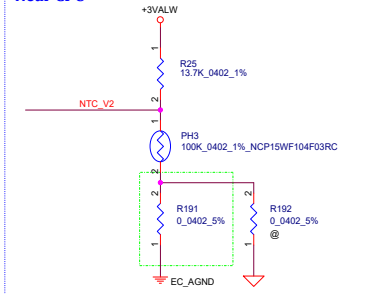
Near GPU&VRAM



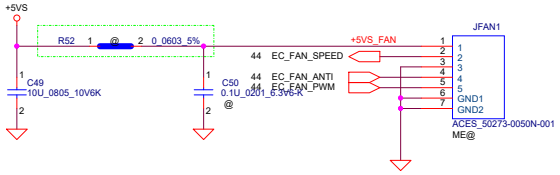
Near CPU Core



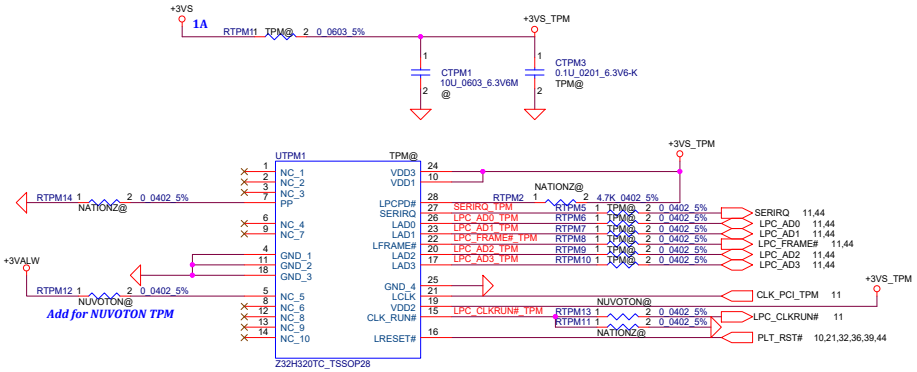
Near CPU



FAN Conn



TPM



Title		
Thermal sensor/FAN CONN/TPM		
Size: C	Document Number: CG414&CG514	Rev: 1.0
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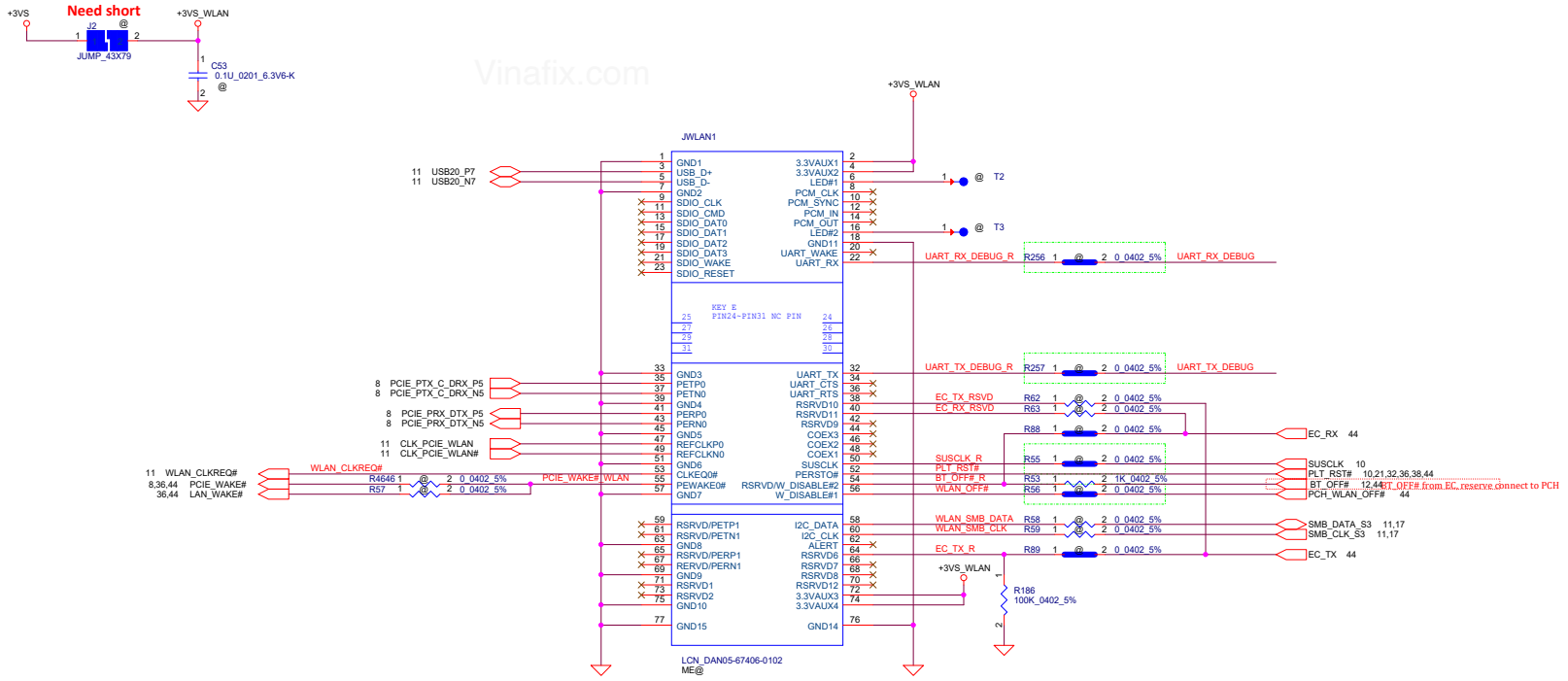
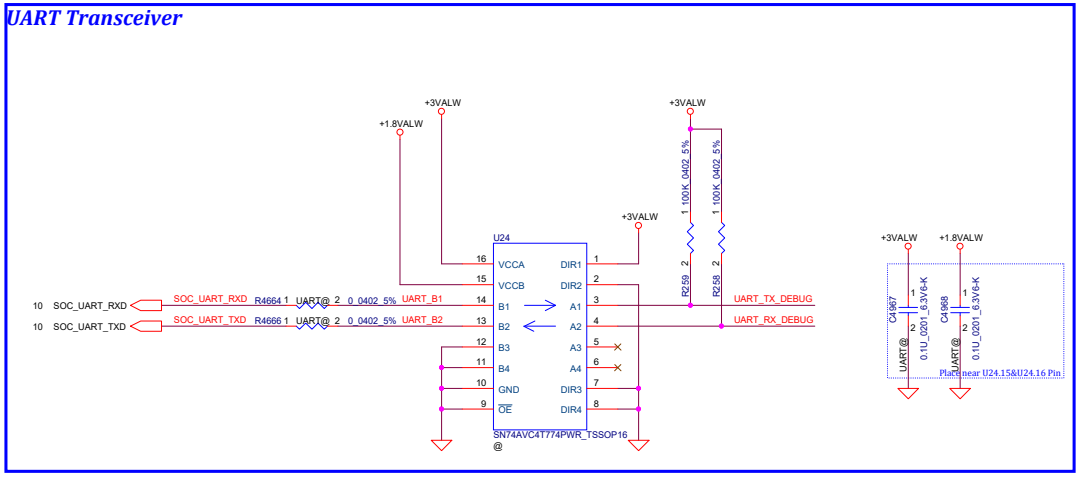
Mini-Express Card(WLAN/WiMAX)



UART Transceiver



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: NGFF WLAN

Size: C | Document Number: CG414&CG514 | Rev: 1.0

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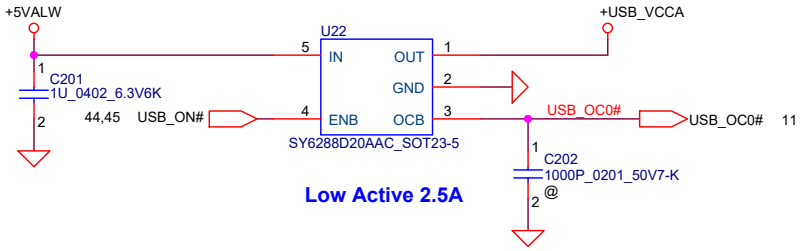
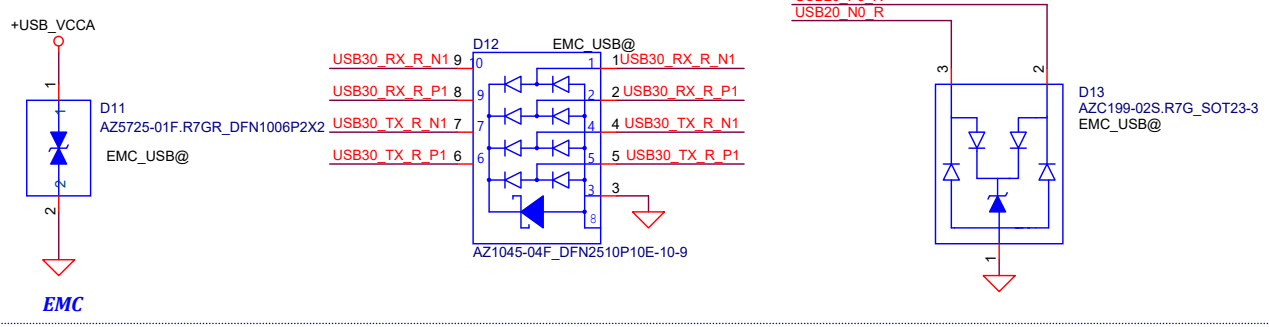
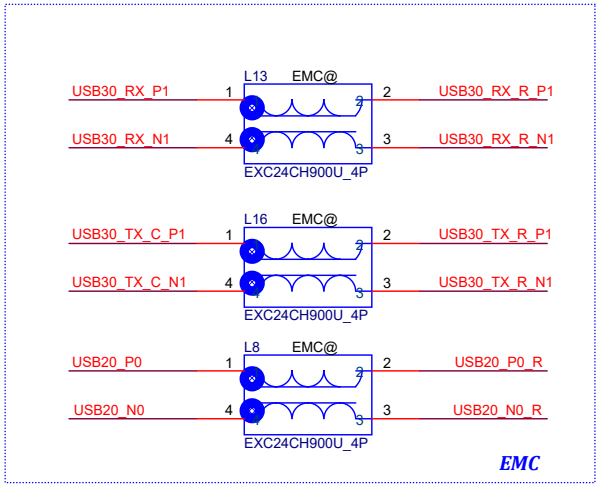
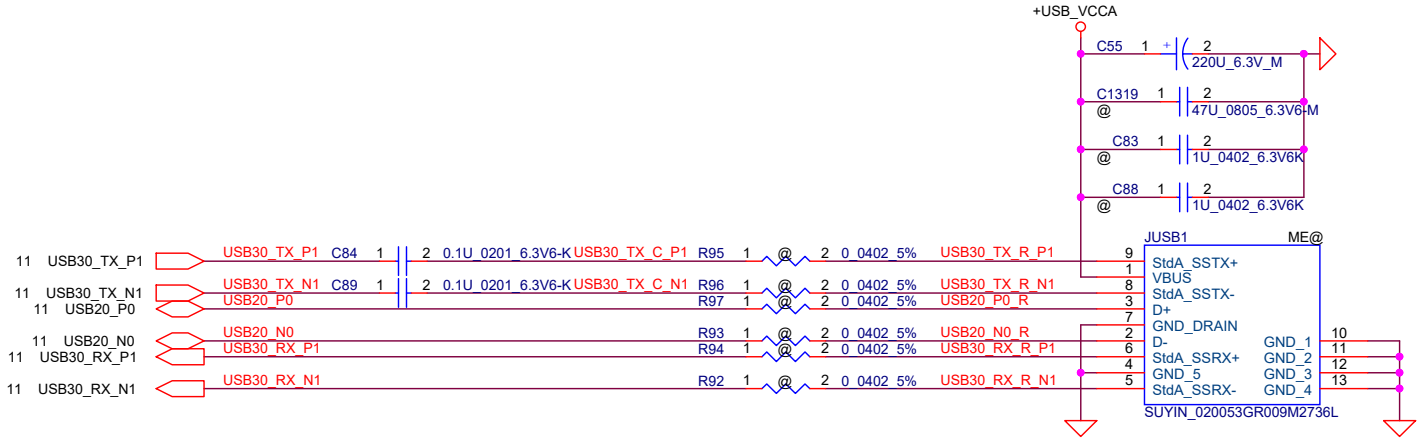
Left Side USB3.0 Port X 1



USB TVS







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **USB PORT (LEFT)**

Size	Document Number	Rev
Custom	CG414&CG514	1.0

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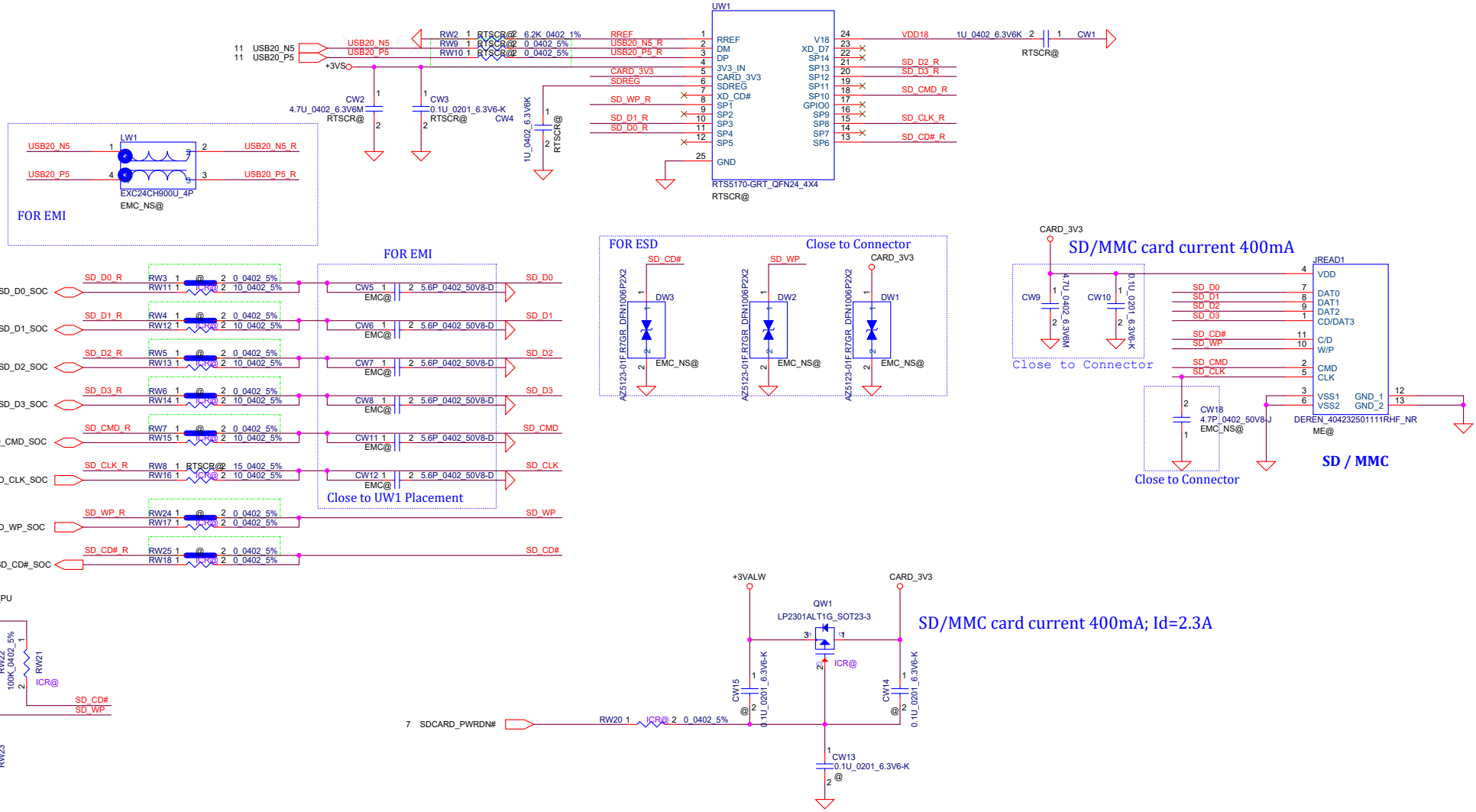
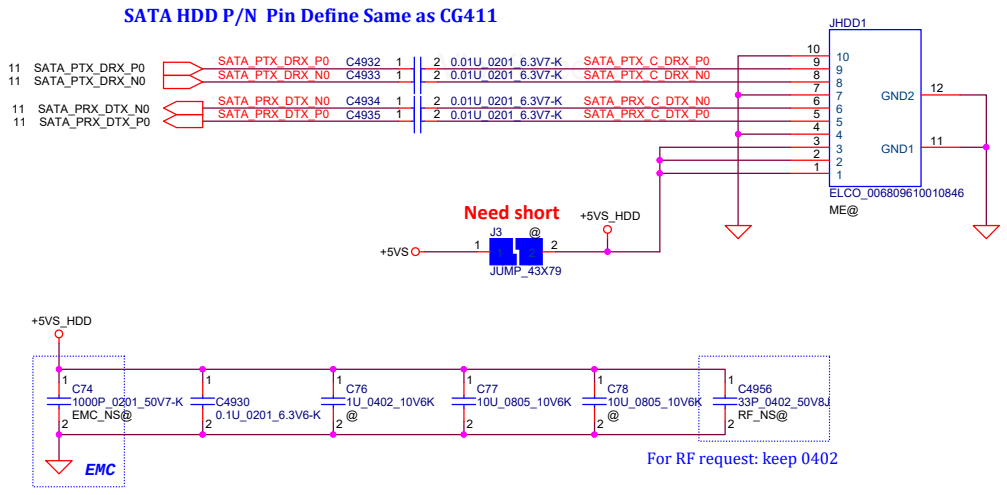
Can't use Intel Internal Card Reader, because change connection to Realtek Card Reader 0ohm to R-short for reduce component count.



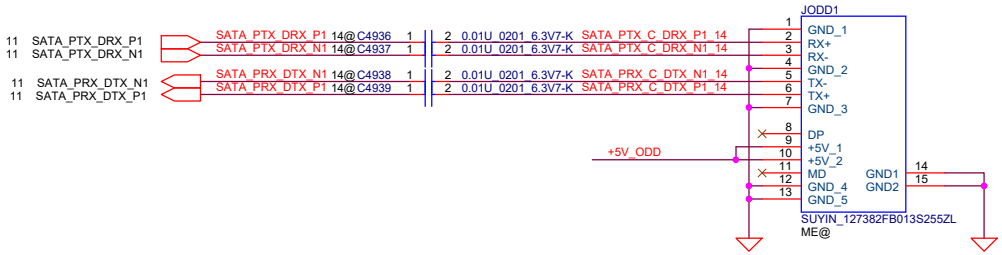
Security Classification	LC Future Center Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/11

Title	Cardreader	
Size: Custom	Document Number: CG414&CG514	Rev: 1.0
Date: Thursday, July 21, 2016	Sheet 41 of 60	

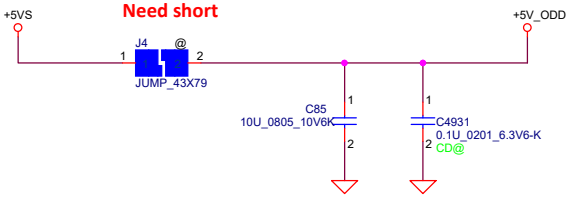
SATA HDD Conn.



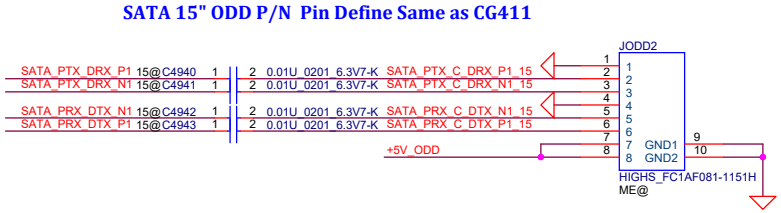
FOR 14" SATA ODD Conn.



+5VS to +5V_ODD



FOR 15" SATA ODD FFC Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: HDD/ODD CONN

Size: Custom | Document Number: CG414&CG514 | Rev: 1.0

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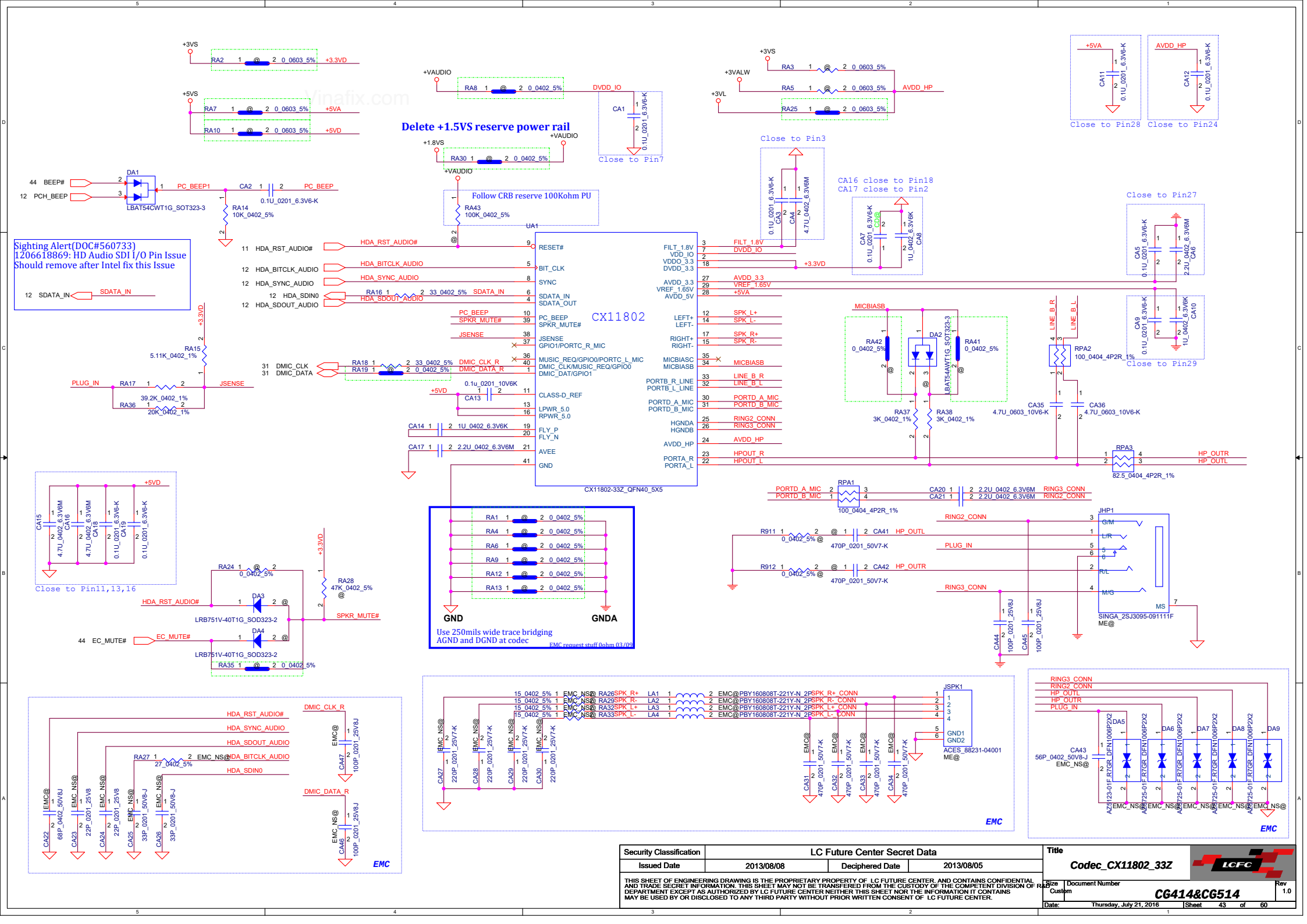
Delete +1.5VS reserve power rail
Sighting Alert(DOC#560733)
1206618869: HD Audio SDI I/O Pin Issue
Should remove after Intel fix this Issue
Follow CRB reserve 100Kohm PU
CX11802
CX11802-33Z_QFN40_5X5
Close to Pin3
Close to Pin7
Close to Pin28
Close to Pin24
Close to Pin27
Close to Pin29
Close to Pin11,13,16
CA16 close to Pin18
CA17 close to Pin2
Use 250mils wide trace bridging
AGND and DGND at codec
GND
GNDA
EMC
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
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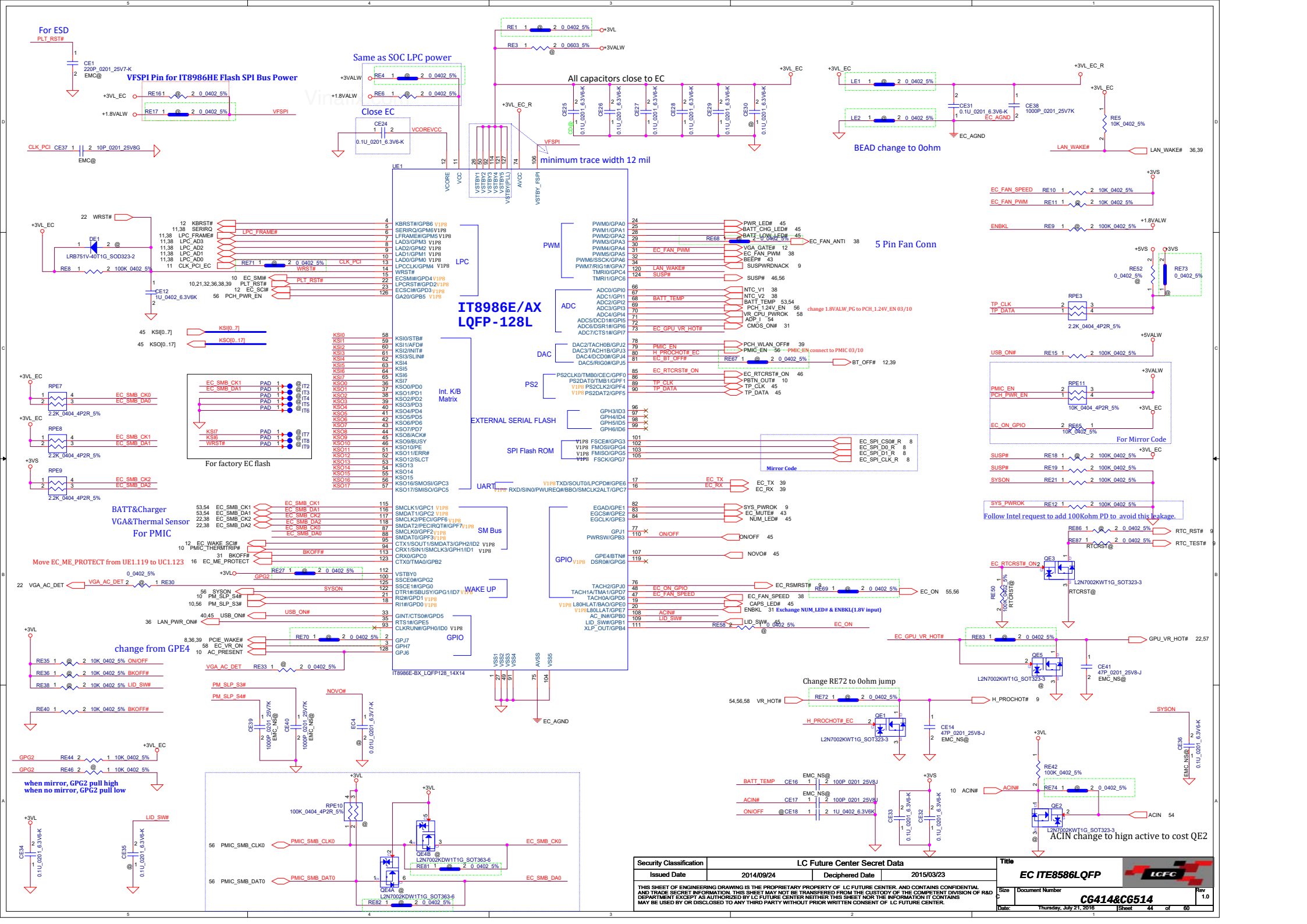
Title
Codec_CX11802_33Z
Size
Custom
Document Number
CG414&CG514
Rev
1.0
Date:
Thursday, July 21, 2016
Sheet
43
of
60


For ESD
PLT_RST#
CE1 220P_0201_25V7-K EMC@
VFSPI Pin for IT8986HE Flash SPI Bus Power
+3VL_EC
+1.8VALW
RE16 1 @ 2 0_0402_5%
RE17 1 @ 2 0_0402_5%
VFSPI
Same as SOC LPC power
+3VALW
RE4 1 @ 2 0_0402_5%
+1.8VALW
RE6 1 @ 2 0_0402_5%
Close EC
CE24 0.1U_0201_6.3V6-K
VCOREVCC
CLK_PCI CE37 1 2 10P_0201_25V8G EMC@
RE1 1 @ 2 0_0402_5% +3VL
RE3 1 @ 2 0_0603_5% +3VALW
All capacitors close to EC
CE25 CE26 CE27 CE28 CE29 CE30 0.1U_0201_6.3V6-K
+3VL_EC_R
VFSPI
minimum trace width 12 mil
UE1
VCORE VCC VSTBY1 VSTBY2 VSTBY3 VSTBY4 VSTBY5 VSTBY(PLL) AVCC VSTBY_FSPI
IT8986E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
Int. K/B Matrix
SM Bus
WAKE UP
GPIO
KBRST# SERIRQ LFRAME# LAD3/GPM3 LAD2/GPM2 LAD1/GPM1 LAD0/GPM0 LPCCLK/GPM4 WRST# ECSMI#/GPD4 LPCRST#/GPD2 ECSCI#/GPD3 GA20/GPB5
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/RIG1#/GPA7 TMRI0/GPC4 TMRI1/GPC6
ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/GPI4 ADC5/DCD1#/GPI5 ADC6/DSR1#/GPI6 ADC7/CTS1#/GPI7
DAC2/TACH0B/GPJ2 DAC3/TACH1B/GPJ3 DAC4/DCD0#/GPJ4 DAC5/RIG0#/GPJ5
PS2CLK0/TMB0/CEC/GPF0 PS2DAT0/TMB1/GPF1 PS2CLK2/GPF4 PS2DAT2/GPF5
GPH3/ID3 GPH4/ID4 GPH5/ID5 GPH6/ID6
V1P8 FSCE#/GPG3 FMOSI/GPG4 FMISO/GPG5 FSCK/GPG7
V1P8 TXD/SOUT0/LPCPD#/GPE6 RXD/SIN0/PWUREQ#/BBO/SMCLK2ALT/GPC7
KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSO16/SMOSI/GPC3 KSO17/SMISO/GPC5
SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/PECI/GPF6 SMDAT2/PECIRQT#/GPF7 SMCLK0/GPF2 SMDAT0/GPF3 CTX1/SOUT1/SMDAT3/GPH2/ID2 CRX1/SIN1/SMCLK3/GPH1/ID1 CRX0/GPC0 CTX0/TMA0/GPB2
VSTBY0 SSCE0#/GPG2 SSCE1#/GPG0 DTR1#/SBUSY/GPG1/ID7 RI2#/GPD1 RI1#/GPD0
GINT/CTS0#/GPD5 RTS1#/GPE5 CLKRUN#/GPH0/ID0
GPJ7 GPH7 GPJ6
EGAD/GPE1 EGCS#/GPE2 EGCLK/GPE3
GPJ1 PWRSW/GPB3
GPE4/BTN# DSR0#/GPG6
TACH2/GPJ0 TACH1A/TMA1/GPD7 TACH0A/GPD6 L80HLAT/BAO/GPE0 L80LLAT/GPE7 AC_IN#/GPB0 LID_SW#/GPB1 XLP_OUT/GPB4
VSS1 VSS2 VSS3 VSS4 AVSS VSS5
IT8986E-BX_LQFP128_14X14
EC_AGND
BEAD change to 0ohm
+3VL_EC_R
LE1 1 @ 2 0_0402_5%
LE2 1 @ 2 0_0402_5%
CE31 0.1U_0201_6.3V6-K EC_AGND
CE38 1000P_0201_25V7K
RE5 10K_0402_5%
LAN_WAKE# LAN_WAKE# 36,39
5 Pin Fan Conn
EC_FAN_SPEED RE10 10K_0402_5%
EC_FAN_PWM RE11 10K_0402_5%
ENBKL RE9 100K_0402_5%
RE68 EC_FAN_ANTI 38
EC_FAN_PWM
VGA_GATE# 12
EC_FAN_PWM 38
BEEP# 43
SUSPWRDNACK 9
LAN_WAKE#
SUSP# SUSP 46,56
change 1.8VALW_PG to PCH_1.24V_EN 03/10
NTC_V1 38
NTC_V2 38
BATT_TEMP BATT_TEMP 53,54
PCH_1.24V_EN 56
VR_CPU_PWROK 58
ADP_I 54
CMOS_ON# 31
EC_GPU_VR_HOT#
PMIC_EN PCH_WLAN_OFF# 39
PMIC_EN 56 PMIC_EN connect to PMIC 03/10
H_PROCHOT# EC
EC_BT_OFF# RE67 0_0402_5% BT_OFF# 12,39
EC_RCTRST#_ON
EC_RCTRST#_ON 46
PBTN_OUT# 10
TP_CLK 45
TP_DATA 45
KSI[0..7]
KSO[0..17]
45 KSI[0..7]
45 KSO[0..17]
EC_SMB_CK1 EC_SMB_DA1 EC_SMB_CK0 EC_SMB_DA0 EC_SMB_CK2 EC_SMB_DA2
2.2K_0404_4P2R_5%
For factory EC flash
Mirror Code
EC_SPI_CS0#_R 8
EC_SPI_D0_R 8
EC_SPI_D1_R 8
EC_SPI_CLK_R 8
EC_TX 39
EC_RX 39
SYS_PWROK 9
EC_MUT# 43
NUM_LED# 45
ON/OFF ON/OFF 45
NOVO# 45
EC_RSMRST# 9
EC_ON_GPIO
EC_FAN_SPEED 38
CAPS_LED# 45
ENBKL 31 Exchange NUM_LED# & ENBKL(1.8V input)
ACIN#
LID_SW# 45
EC_ON
EC_ON 55,56
BATT&Charger
VGA&Thermal Sensor
For PMIC
Move EC_ME_PROTECT from UE1.119 to UC1.123
change from GPE4
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
VGA_AC_DET RE30 SYSON PM_SLP_S3# PM_SLP_S4# USB_ON# LAN_PWR_ON# PCIE_WAKE# EC_VR_ON AC_PRESENT
RE35 RE36 RE38 RE40 ON/OFF BKOFF# LID_SW#
CE39 CE40 1000P_0201_25V7K EMC_NS@
EC4 0.01U_0201_6.3V7-K
RE70 RE27 RE33
PMIC_SMB_CLK0 PMIC_SMB_DAT0 EC_SMB_CK0 EC_SMB_DA0
RPE10 100K_0404_4P2R_5%
QE4A QE4B L2N7002KDW1T1G_SOT363-6
RE81 RE82 2K_0402_5%
CE34 CE35 0.1U_0201_6.3V6-K
LID_SW#
Follow Intel request to add 100Kohm PD to avoid this leakage.
RE86 RE87 RTC_RST# RTC_TEST#
RTCRST@
EC_RTCRST#_ON QE3 L2N7002KWT1G_SOT323-3
RE50 100K_0402_5%
GPU_VR_HOT# 22,57
QE5 L2N7002KWT1G_SOT323-3
CE41 47P_0201_25V8-J EMC_NS@
Change RE72 to 0ohm jump
54,56,58 VR_HOT#
RE72 0_0402_5%
H_PROCHOT# 9
QE1 L2N7002KWT1G_SOT323-3
CE14 47P_0201_25V8-J EMC_NS@
SYSON
CE36 0.1U_0201_6.3V6-K EMC_NS@
BATT_TEMP CE16 100P_0201_25V8J
ACIN# CE17 100P_0201_25V8J
ON/OFF @CE18 1U_0402_6.3V6K
CE33 CE32 0.1U_0201_6.3V6-K
RE42 100K_0402_5%
RE74 0_0402_5%
QE2 L2N7002KWT1G_SOT323-3
ACIN 54
ACIN change to hign active to cost QE2
RPE3 2.2K_0404_4P2R_5%
TP_CLK TP_DATA
RE52 RE73 0_0402_5%
RPE11 10K_0404_4P2R_5%
PMIC_EN PCH_PWR_EN
EC_ON_GPIO RE65 10K_0402_5%
SUSP# SUSP# SYSON SYS_PWROK
RE18 RE19 RE21 RE12 100K_0402_5%
USB_ON# RE15 100K_0402_5%
+3VS +5VS +1.8VALW +5VALW +3VALW +3VL_EC_R
Security Classification LC Future Center Secret Data
Issued Date 2014/09/24 Deciphered Date 2015/03/23
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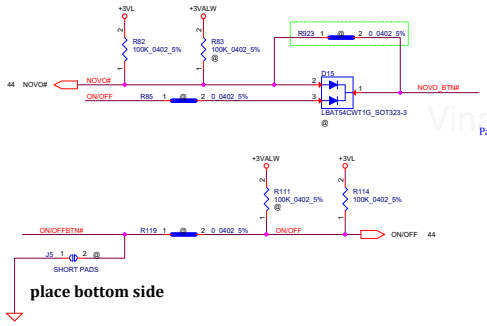
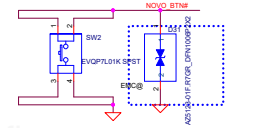
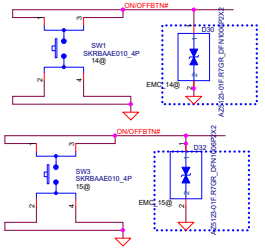
ON/OFF switch



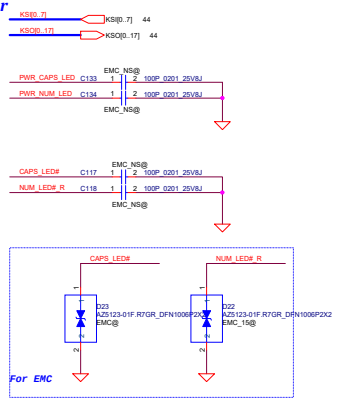
place bottom side

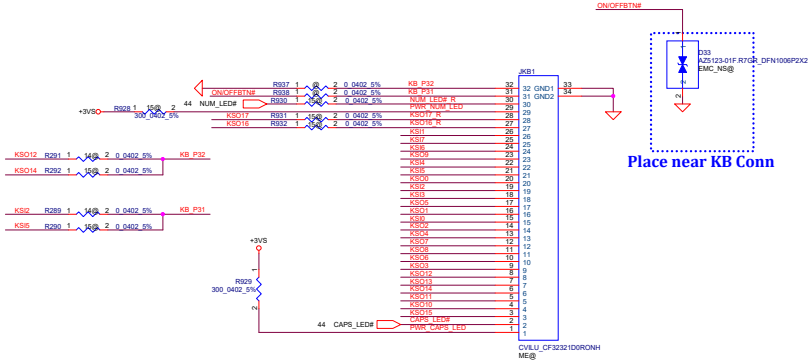


Pay more attention at 14" & 15" Power Button placement



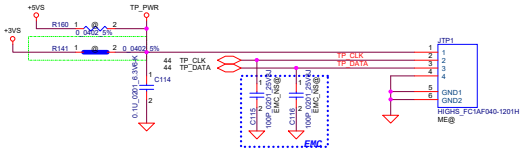
K/B Connector

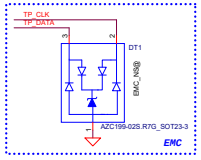




Place near KB Conn

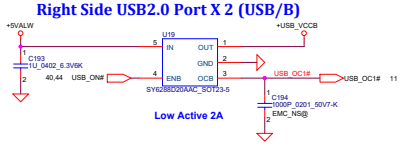
TP/B Connector



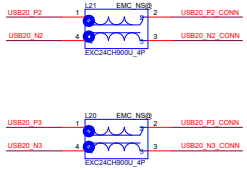


USB DB Connector

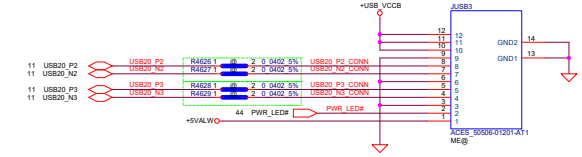
Right Side USB2.0 Port X 2 (USB/B)



Low Active 2A

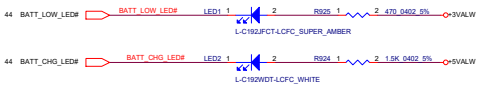


JUSB3 Pin Define Follow CG411

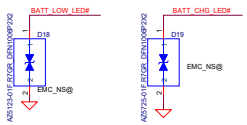


USB I/O Connector for G, USB2.0*2

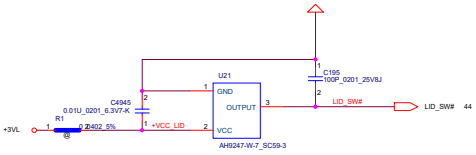
LED



Check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14"/15" 02/26



LID Switch



Delete KBL circuit, due to 310 do NOT support KBL

Security Classification	LC Future Center Secret Data		
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Title: KBD/PWR/IO/LED/TP Conn.

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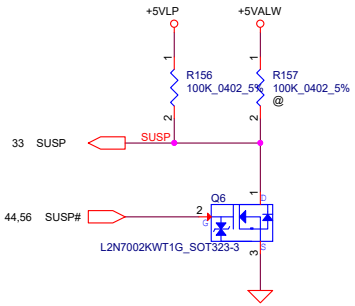
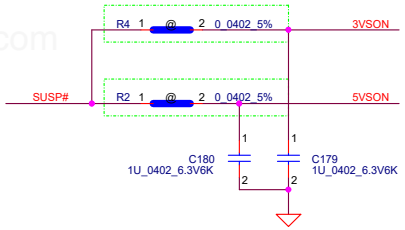
+5VS/+3VS Load Switch



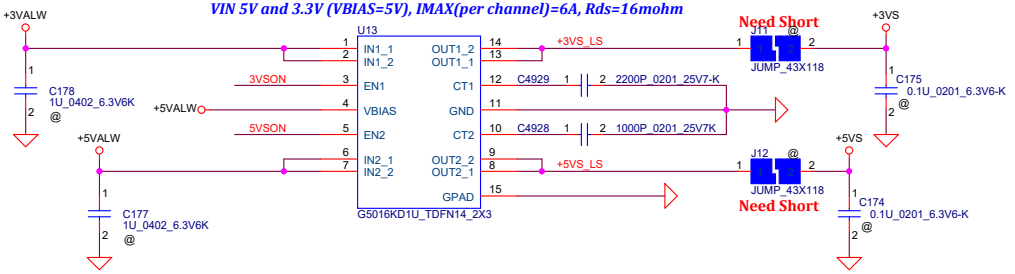


Load Switch
+5VALW To +5VS
+3VALW To +3VS

modify load swtich from APL3523 to G5016KD1U TDFN 14P

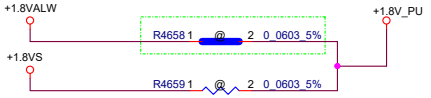
+3VS, C173 --> 2.78ms
+5VS, C176 --> 1.71ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

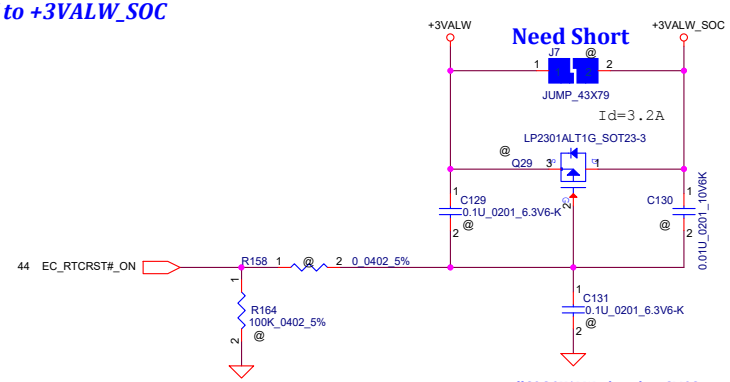


Delete +3.3VALW to +1.5VS

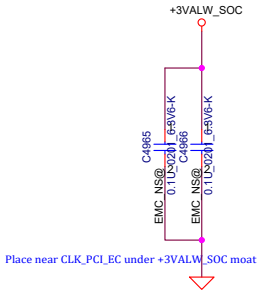
+1.8V_PU Power Rail



+3VALW to +3VALW_SOC

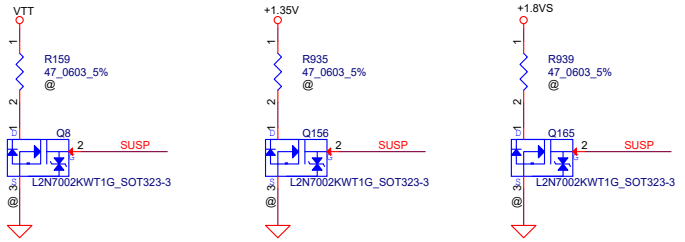


reserve to cut off SOC 3VALW when clear CMOS



Place near CLK_PCI_EC under +3VALW_SOC moat

For DisCharge



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
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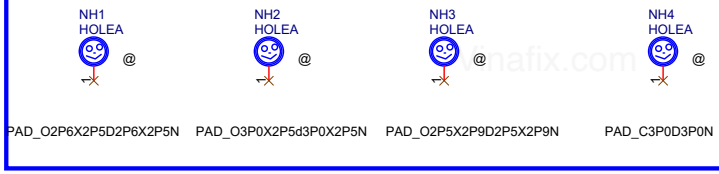
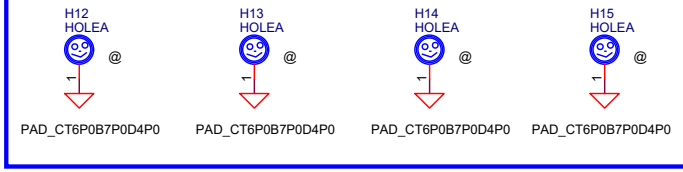
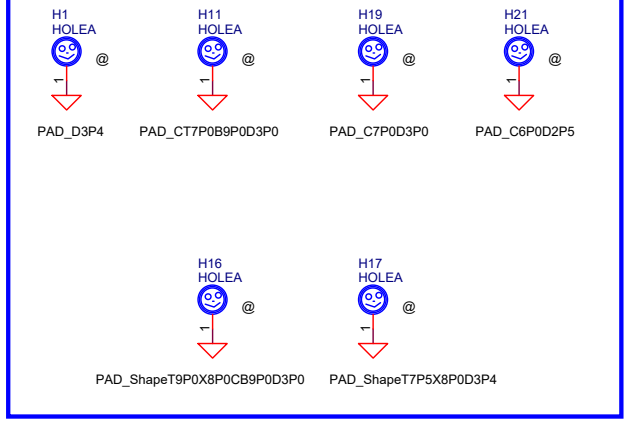
Non-PTH Hole

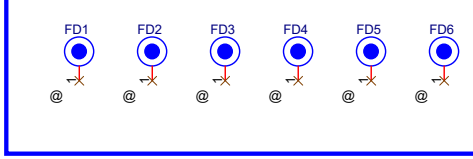


SoC PTH Hole

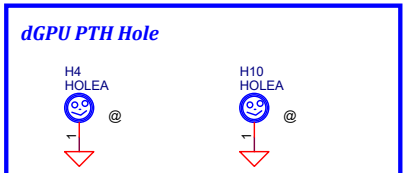




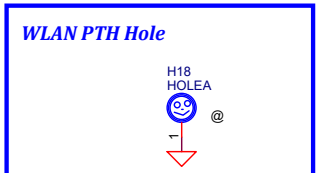
PCB Fedical Mark PAD



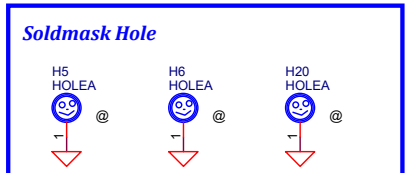
dGPU PTH Hole



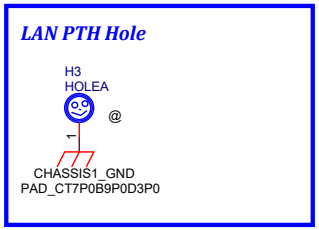
WLAN PTH Hole



Soldmask Hole



LAN PTH Hole



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: Hole

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HDMI Logo

ZZZ1 HDMI@

HDMI Logo
RO00000040J

LAN Chip

UL1

RTL8111H-CG
SA000074W00
8111H@

B0 Stepping CPU

UC1	UC1	UC1
N3350	N3450	N4200
APOLLOLAKE_FCBGA1296	APOLLOLAKE_FCBGA1296	APOLLOLAKE_FCBGA1296
SA000080L20	SA000080M20	SA000080N20
N3350_B0@	N3450_B0@	N4200_B0@

B1 Stepping CPU

UC1	UC1	UC1
N3350	N3450	N4200
APOLLOLAKE_FCBGA1296	APOLLOLAKE_FCBGA1296	APOLLOLAKE_FCBGA1296
SA000080L30	SA000080M30	SA000080N30
N3350_B1@	N3450_B1@	N4200_B1@

eMMC Chip

U23

H26M78103CCR
SA00007T500
EMMC@

Hynix 2GB VRAM

ZZZ3 H2GX4@

HYNIX_2GB_VRAM
X7612312001

UV5 H4G@	UV6 H4G@	UV7 H4G@	UV8 H4G@	RV70 H4G@
H5TC4G63CFR-N0C 4Gb	H5TC4G63CFR-N0C 4Gb	H5TC4G63CFR-N0C 4Gb	H5TC4G63CFR-N0C 4Gb	4.75K_0402_1%
SA00007DU10	SA00007DU10	SA00007DU10	SA00007DU10	SD03447518J

VRAM_Hynix_256M*16 000

Micron 2GB VRAM

ZZZ4 M2GX4@

MICRON_2GB_VRAM
X7612312002

UV5 M4G@	UV6 M4G@	UV7 M4G@	UV8 M4G@	RV63 M4G@	RV70 M4G@
MT41J256M16LY-091G:N	MT41J256M16LY-091G:N	MT41J256M16LY-091G:N	MT41J256M16LY-091G:N	4.53K_0402_1%	2K_0402_1%
SA00007QJ00	SA00007QJ00	SA00007QJ00	SA00007QJ00	SD03445318J	SD03420018J

VRAM_Micron_256M*16 010

Samsung 2GB VRAM

ZZZ5 S2GX4@

SAMSUNG_2GB_VRAM
X7612312003

UV5 S4G@	UV6 S4G@	UV7 S4G@	UV8 S4G@	RV63 S4G@	RV70 S4G@
K4W4G1646E-BC1A 4Gb	K4W4G1646E-BC1A 4Gb	K4W4G1646E-BC1A 4Gb	K4W4G1646E-BC1A 4Gb	8.45K_0402_1%	2K_0402_1%
SA000063F20	SA000063F20	SA000063F20	SA000063F20	SD000011R00	SD03420018J

VRAM_Samsung_256M*16 001

PCB MB

ZZZ2 @

PCB PN
DA600011L10

14"&15" PCB DAZ PN

ZZZ2 14@

PCB PN
DAZ11B00100

ZZZ2 15@

PCB PN
DAZ11C00100

VRAM ID config

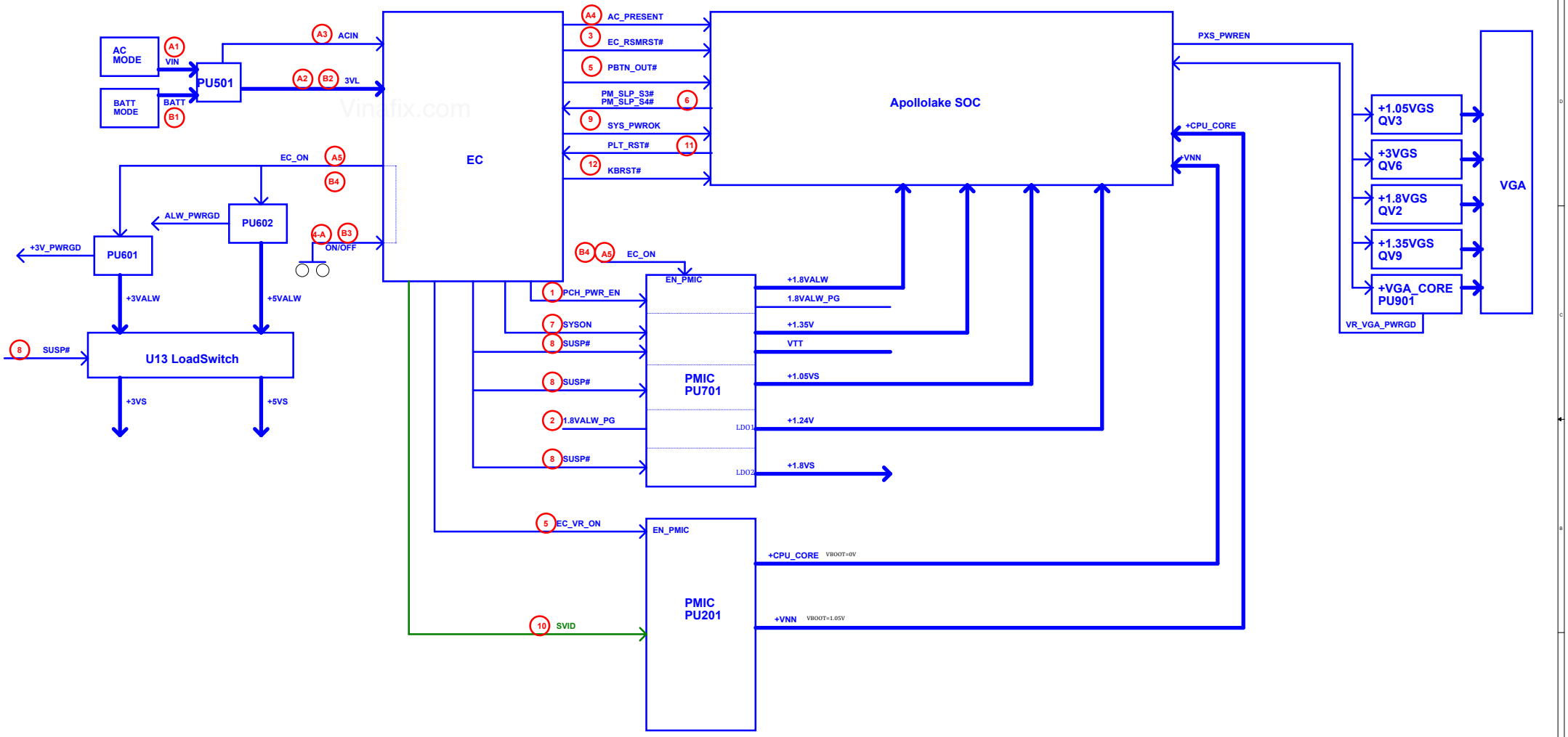
Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *Virtual symbol*

Size	Document Number	Rev
C	CG414&CG514	1.0

Date: Friday, July 22, 2016 Sheet 48 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *Power sequence Block*

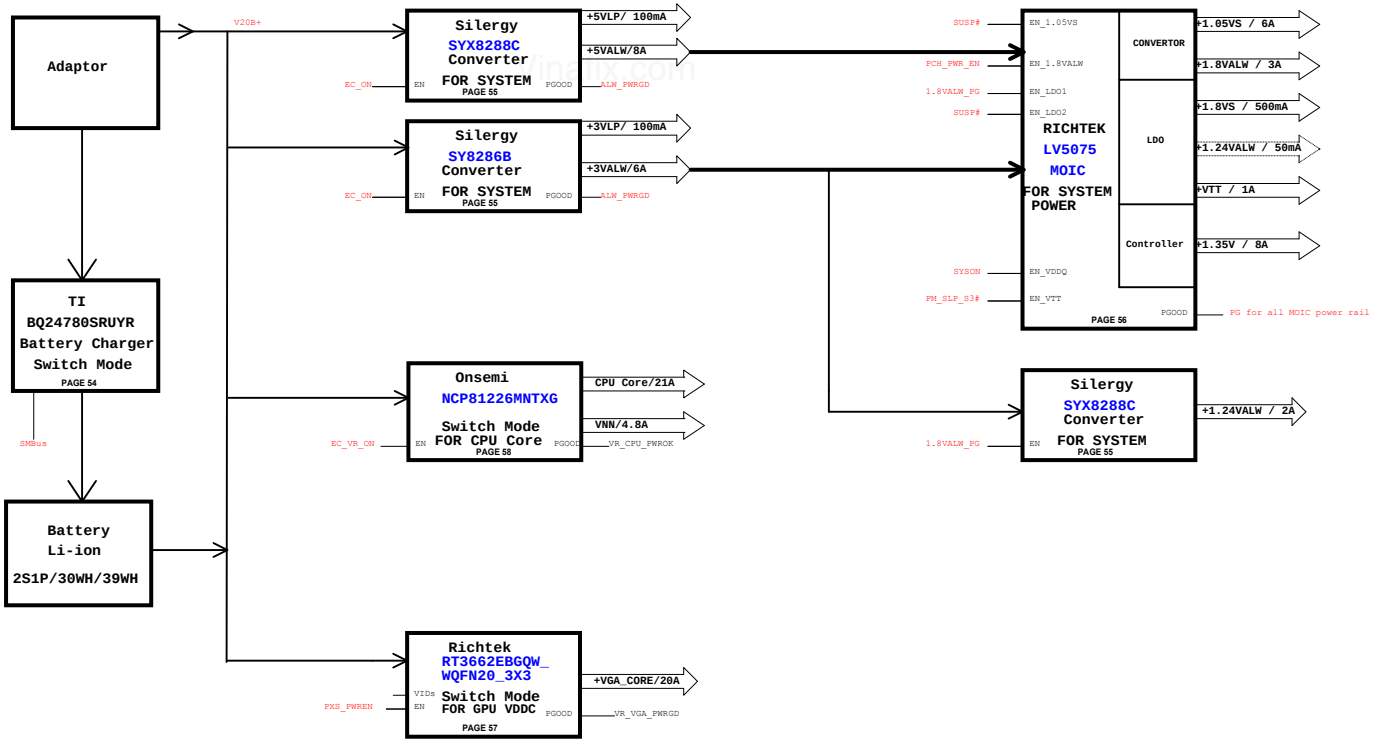
Size: Custom	Document Number: CG414&CG514	Rev: 1.0
Date: Thursday, July 21, 2016	Sheet 49 of 60	

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2014/01/21

Title: ***Blank***

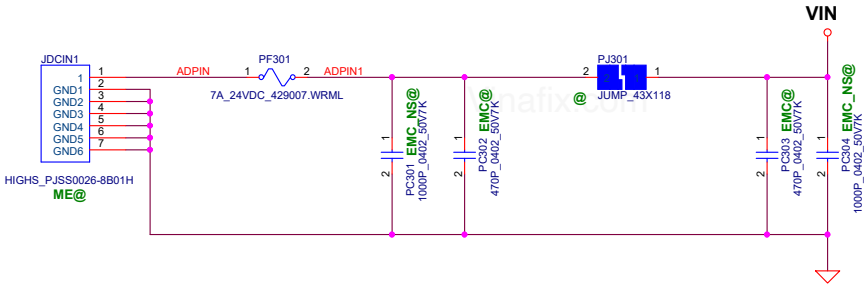
Size	Document Number	Rev
C	CG414&CG514	1.0

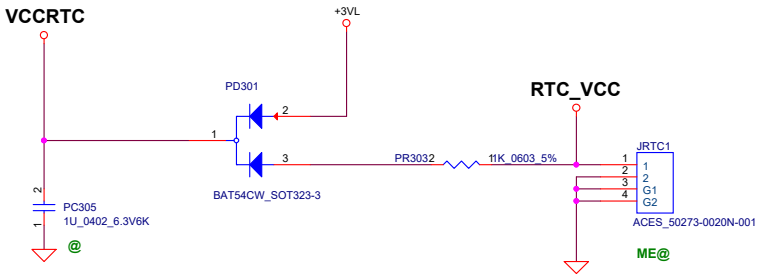
Date: Thursday, July 21, 2016 | Sheet 50 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	Power Diagram		
Size	Document Number		Rev
D	C6414		1.0
Date:	Thursday, July 31, 2014	Sheet	51 of 60



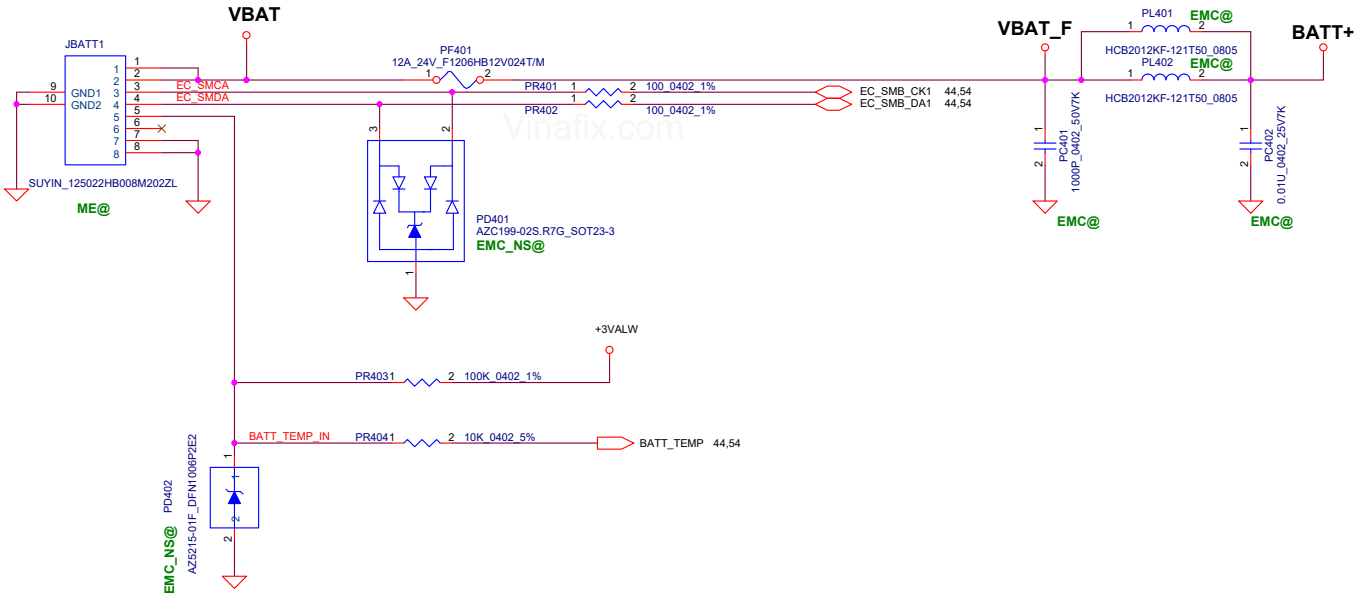


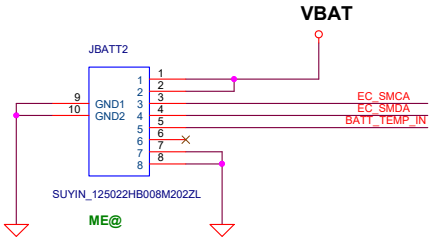
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: *DCIN / RTC*

Size	Document Number	Rev
Custom	CG414	1.0

Date: Thursday, July 21, 2016 Sheet 52 of 6



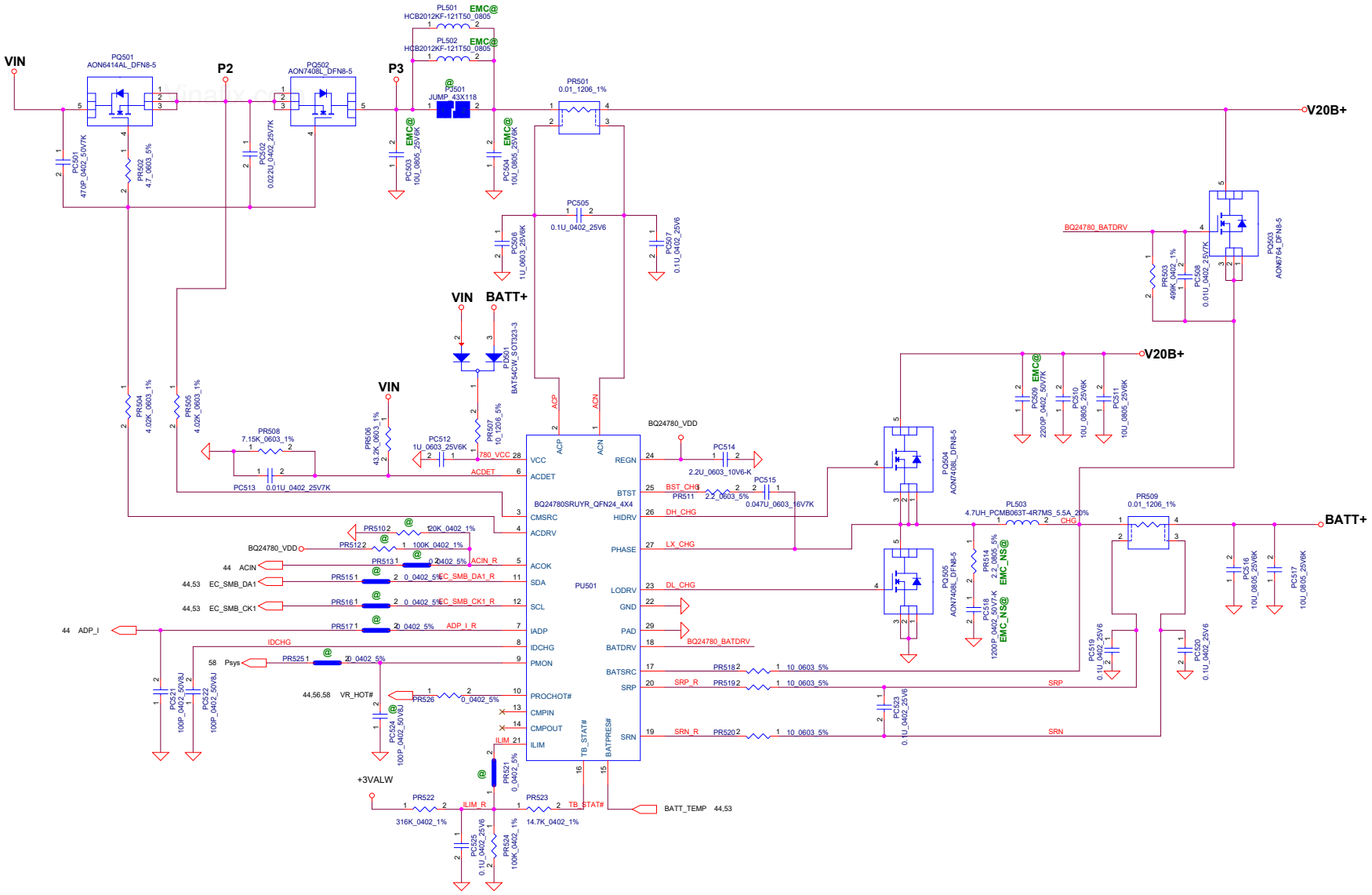


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	CG414	1.0

Date: Thursday, July 21, 2016 Sheet 53 of 6



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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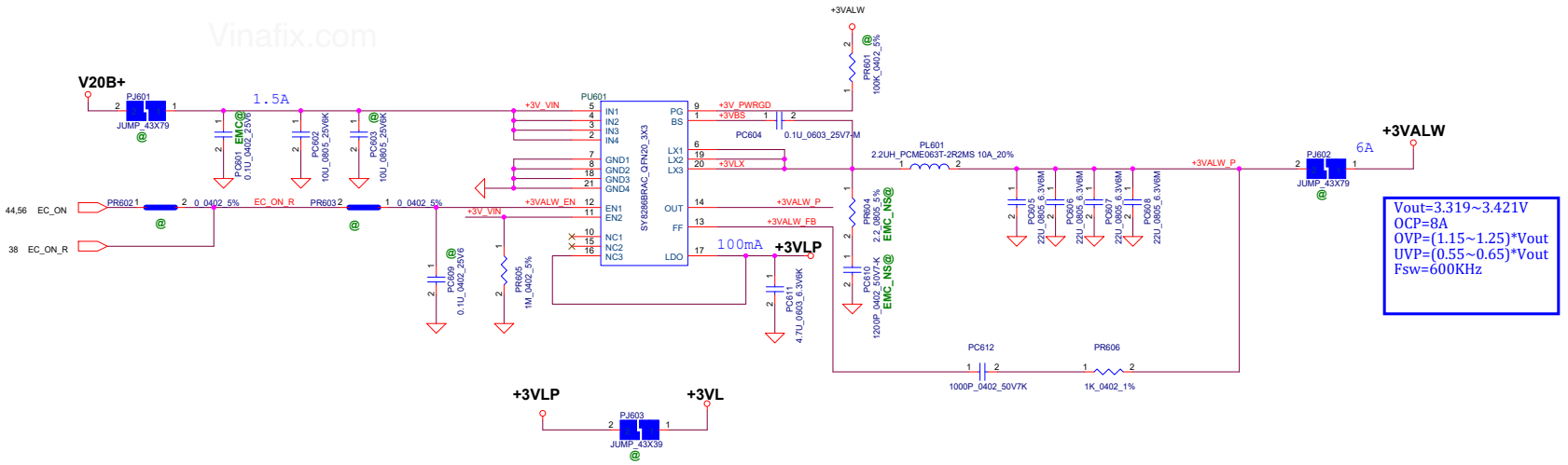
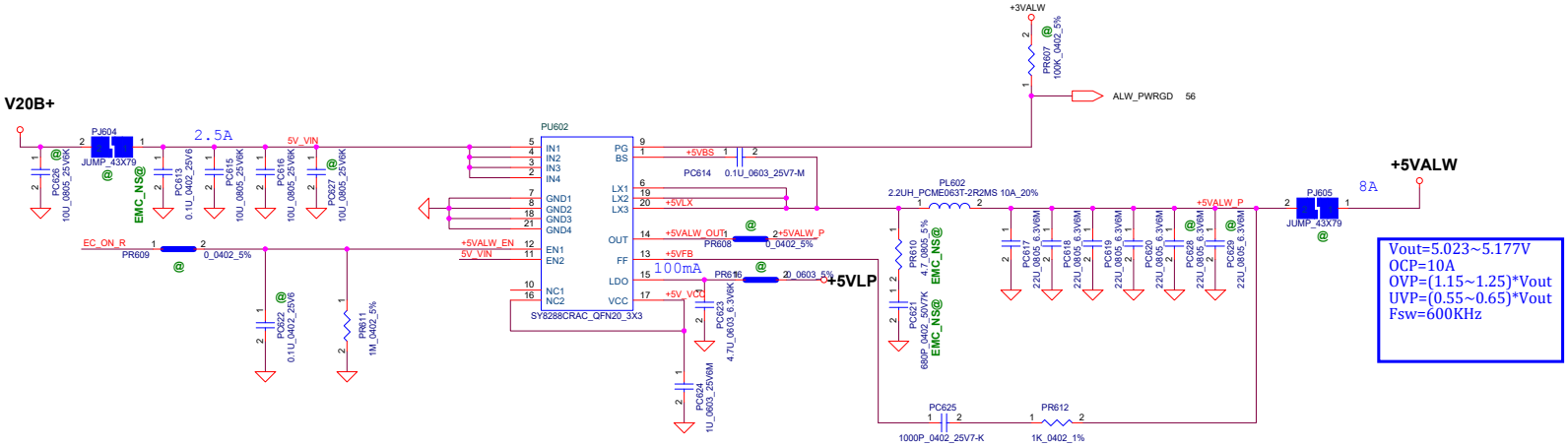
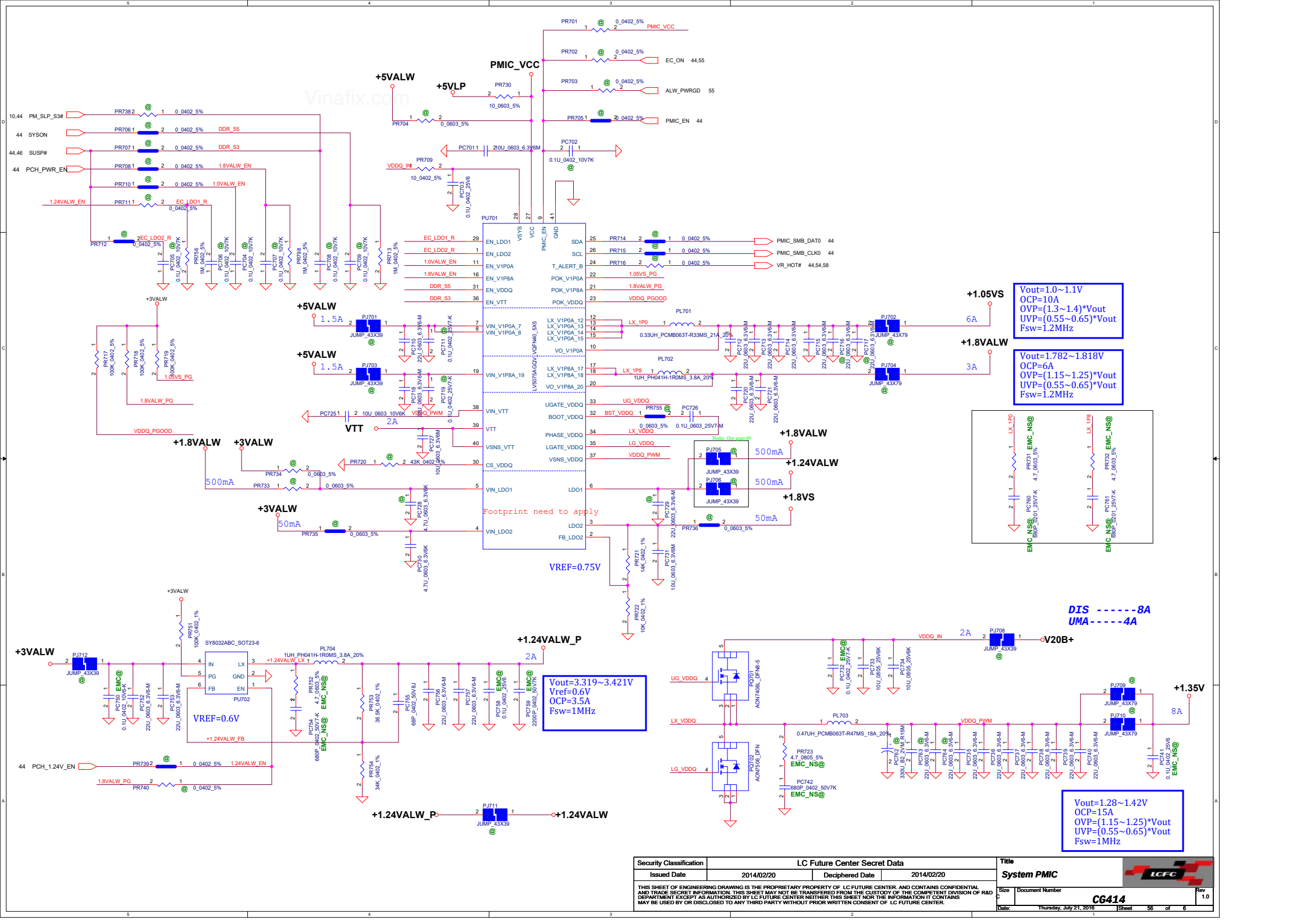
Title	CHARGER		
Size	Document Number		Rev
C	CG414		1.0
Date:	Thursday, July 21, 2016	Sheet	54 of 6





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	CG414		1.0
Date:	Thursday, July 21, 2016	Sheet	55 of 6


PMIC_VCC
+5VALW
+5VLP
+1.05VS
Vout=1.0~1.1V
OCP=10A
OVP=(1.3~1.4)*Vout
UVP=(0.55~0.65)*Vout
Fsw=1.2MHz
+1.8VALW
Vout=1.782~1.818V
OCP=6A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=1.2MHz
VTT
VREF=0.75V
Footprint need to apply
+1.24VALW
+1.8VS
+1.24VALW_P
Vout=3.319~3.421V
Vref=0.6V
OCP=3.5A
Fsw=1MHz
VREF=0.6V
DIS ------8A
UMA-----4A
+1.35V
Vout=1.28~1.42V
OCP=15A
OVP=(1.15~1.25)*Vout
UVP=(0.55~0.65)*Vout
Fsw=1MHz
Security Classification
LC Future Center Secret Data
Issued Date
2014/02/20
Deciphered Date
2014/02/20
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Title
System PMIC
Size
C
Document Number
CG414
Rev
1.0
Date:
Thursday, July 21, 2016
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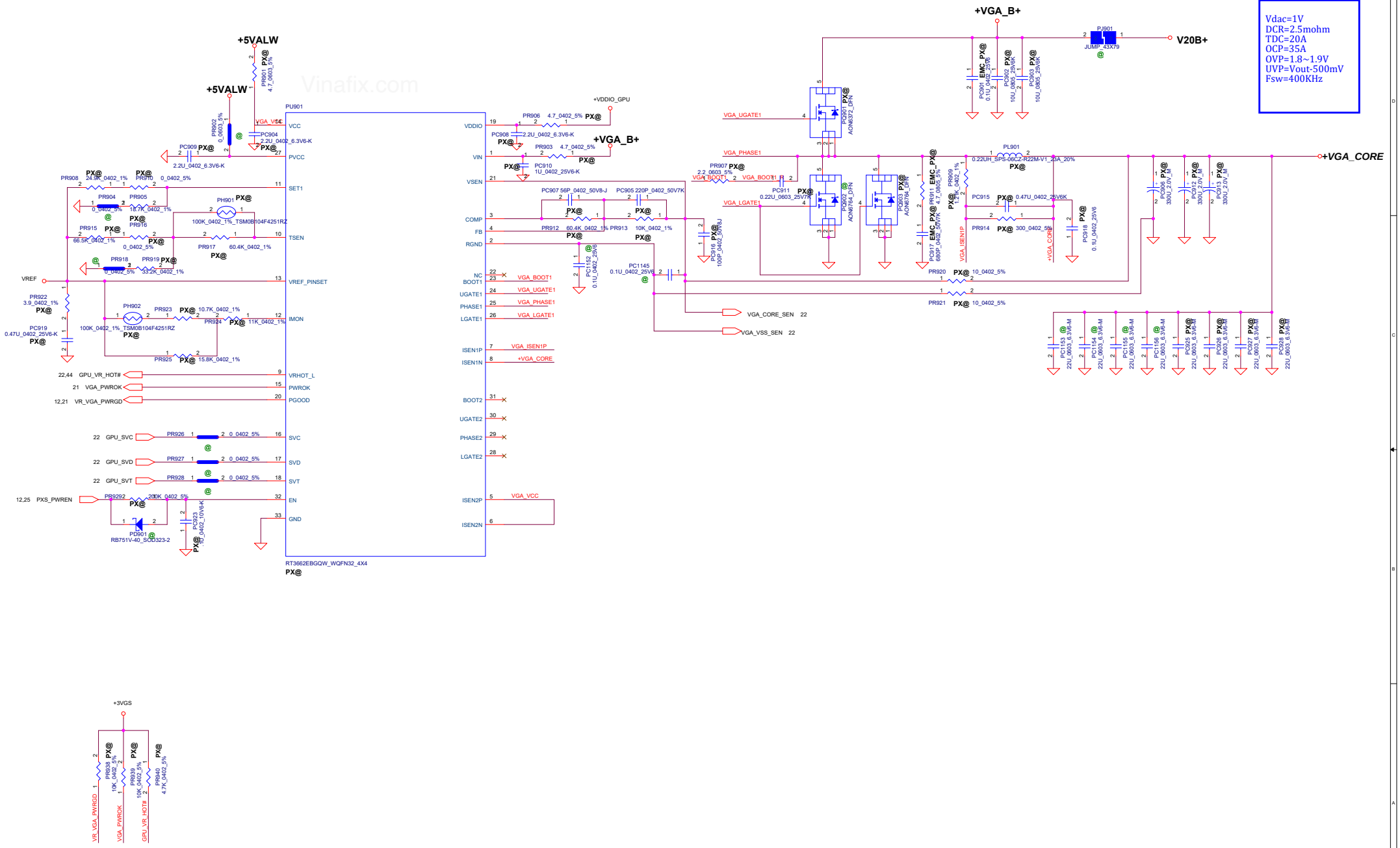
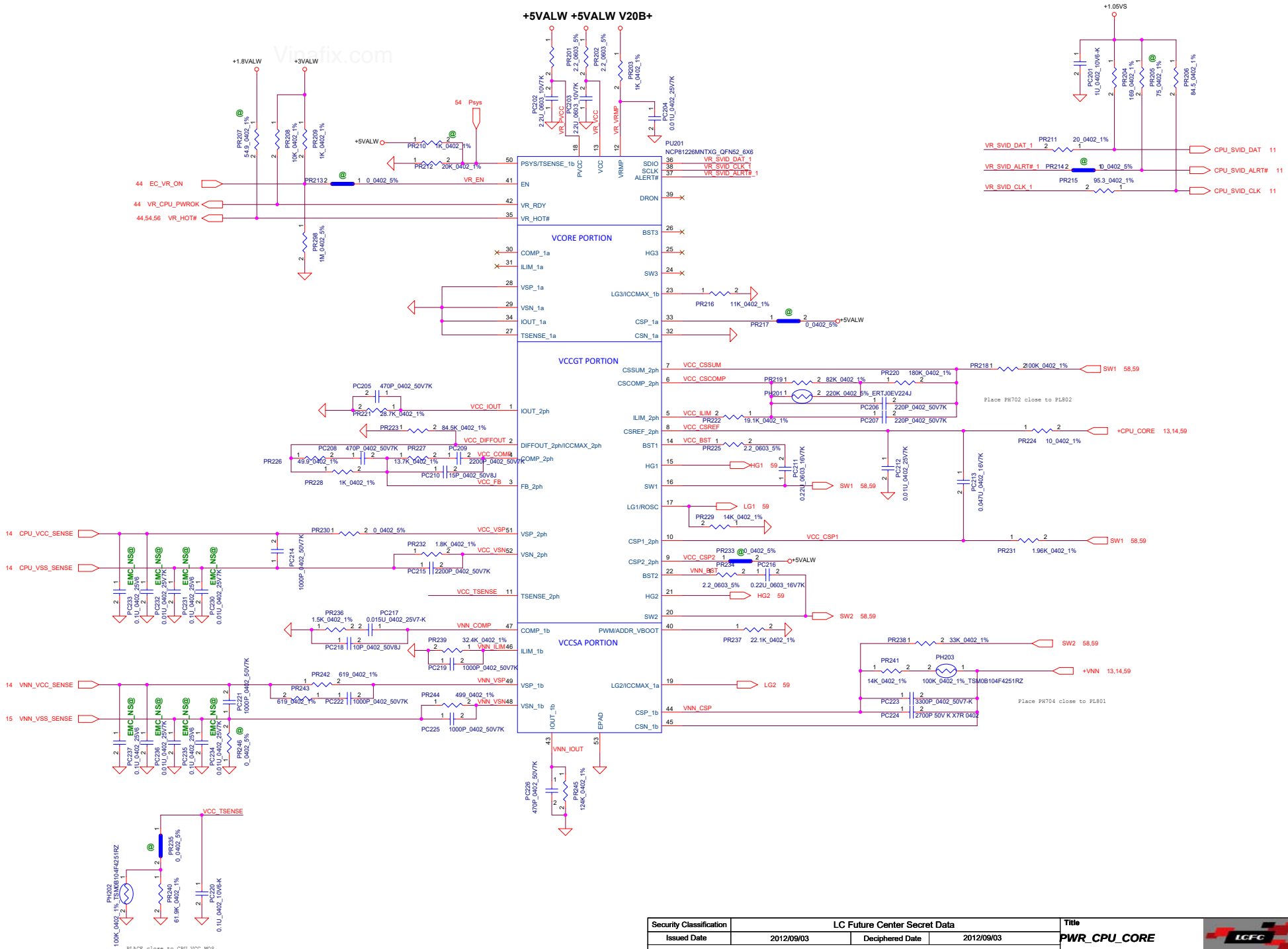


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	+VGA_CORE		
Size: Custom	Document Number: CG414		Rev: 1.0
Date: Thursday, July 21, 2016	Sheet 57 of 60		

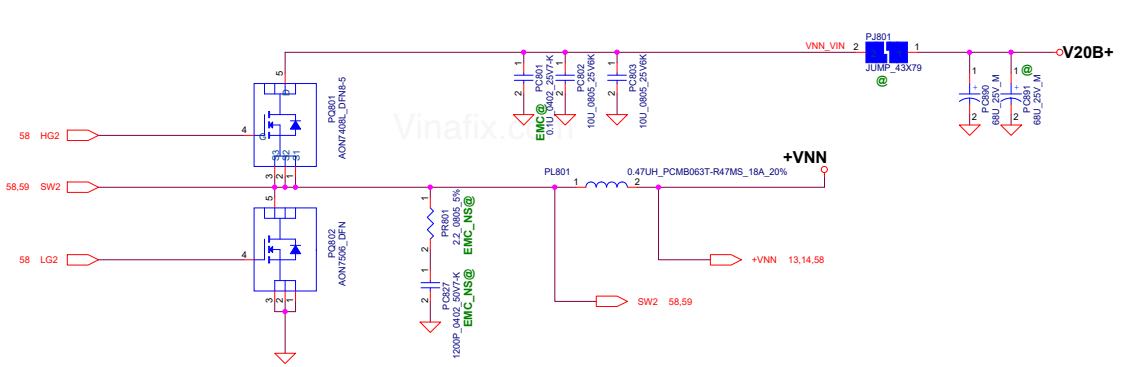


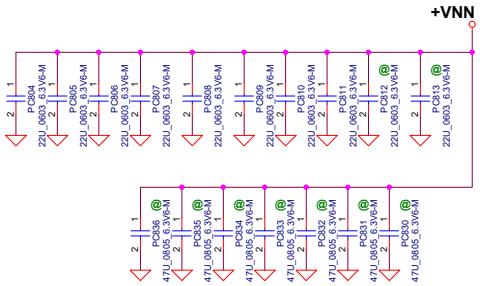
Security Classification	LC Future Center Secret Data		
Issued Date	2012/09/03	Deciphered Date	2012/09/03

Title: PWR_CPU_CORE

Size	Document Number	Rev
C	CG414	1.0

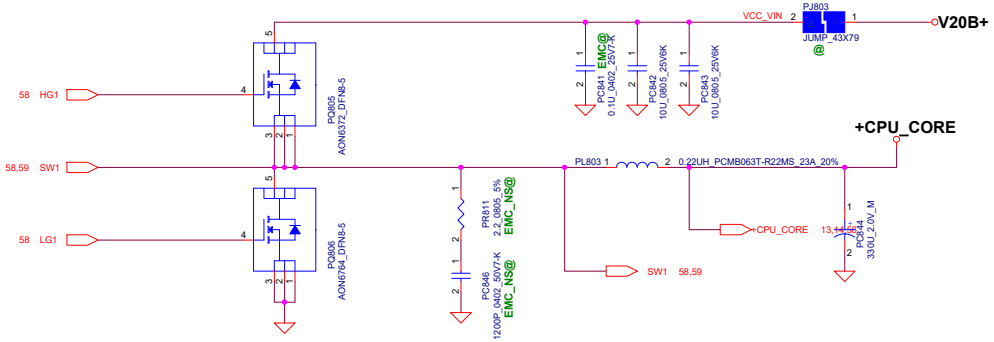
Date: Thursday, July 21, 2016 Sheet 58 of 6

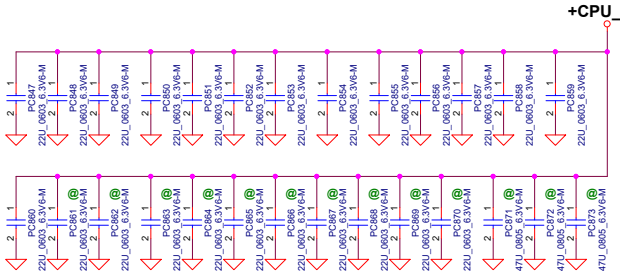




VID1=1.3V
Vboot=1.05V
DCR=4mohm
TDC/Iccmax=4/5A
OCP=12.5A
OVP=Vout+400mV
UVP=Vout-300mV
Fsw=600KHz

VID1=1.3V
Vboot=0V
DCR=2.5mohm
TDC/Iccmax=18/21A
OCP=31.8A
OVP=Vout+400mV
UVP=Vout-300mV
Fsw=600KHz





Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/08	Deciphered Date	2013/11/08

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Title: PWR_CPU_Core

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20160226:
1. P54-PWR-CHARGER: change PR506,PR508,PC513 value for changing ACDET Value
2. P58-PWR_CPU_CORE1: change PR242,PR243, PR239,PR245,PC218,PR221,PR232,PR227value,modify VR transient meet intel spec
3. P58-PWR_CPU_CORE1: change all '+5VS' power port to '+5VALW', solve MB can't boot issue
4. P56-PWR_System PMIC: change PR702,PR705 BOM structure, solve PMIC sequence issue,change PMIC EN from 'EC_ON' to 'PMIC_EN'
20160304:
1. P56-PWR_System PMIC: add PR798 EN PD resistor,solve "1.8ALW" signal glitch
2. P58-PWR_CPU_CORE1:add PR298 EN PD resistor,solve "EC_VR_ON" signal glitch
20160307:
1. P59-PWR_CPU_CORE2:change PC830-836,PC871-873 BOM structure to @, change PC855-860,PC808-811 BOM structure for cost down
20160309:
1. P54-PWR-CHARGER:change PL501,PL502,PC503,PC504 BOM structure to "EMC@" For EMC requirement
2. P58-PWR_CPU_CORE1:add PC230-237 location,For EMC requirement
20160309:
1. P57-PWR-VGA_CORE(RT3662EB):Modify PR940 from 10K_0402_5% to 4.7K_0402_5%, Follow GPU owner request to modify GPU_VR_HOT# PU resistor
20160311:
1. P54-PWR-CHARGER: change PC503,PC504 PN, footprint from '0603' to '0805' for cost down
20160311:
1. P58-PWR_CPU_CORE1: change PR209 BOM structure, stuff PR209(1Kohm_0402), Follow EE requirement
20160509:
1. P56-PWR_System PMIC: change PC712 PN, change PC727 value from 22UF to 10UF
20160510:
1. P54-PWR-CHARGER:change PQ503 PN from AON6414 to AON6764 for palm rest temperature issue
2. P55-PWR_3VALW/5VALW: change PL601,PL602 PN for palm rest temperature issue
20160516:
1. P54-PWR-CHARGER:change PQ503 fuction filed.
2. P55-PWR_3VALW/5VALW: change PL601,PL602fuction filed

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2014/01/21

Title: **Blank**

Size	Document Number	Rev
Custom	CG414	1.0

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