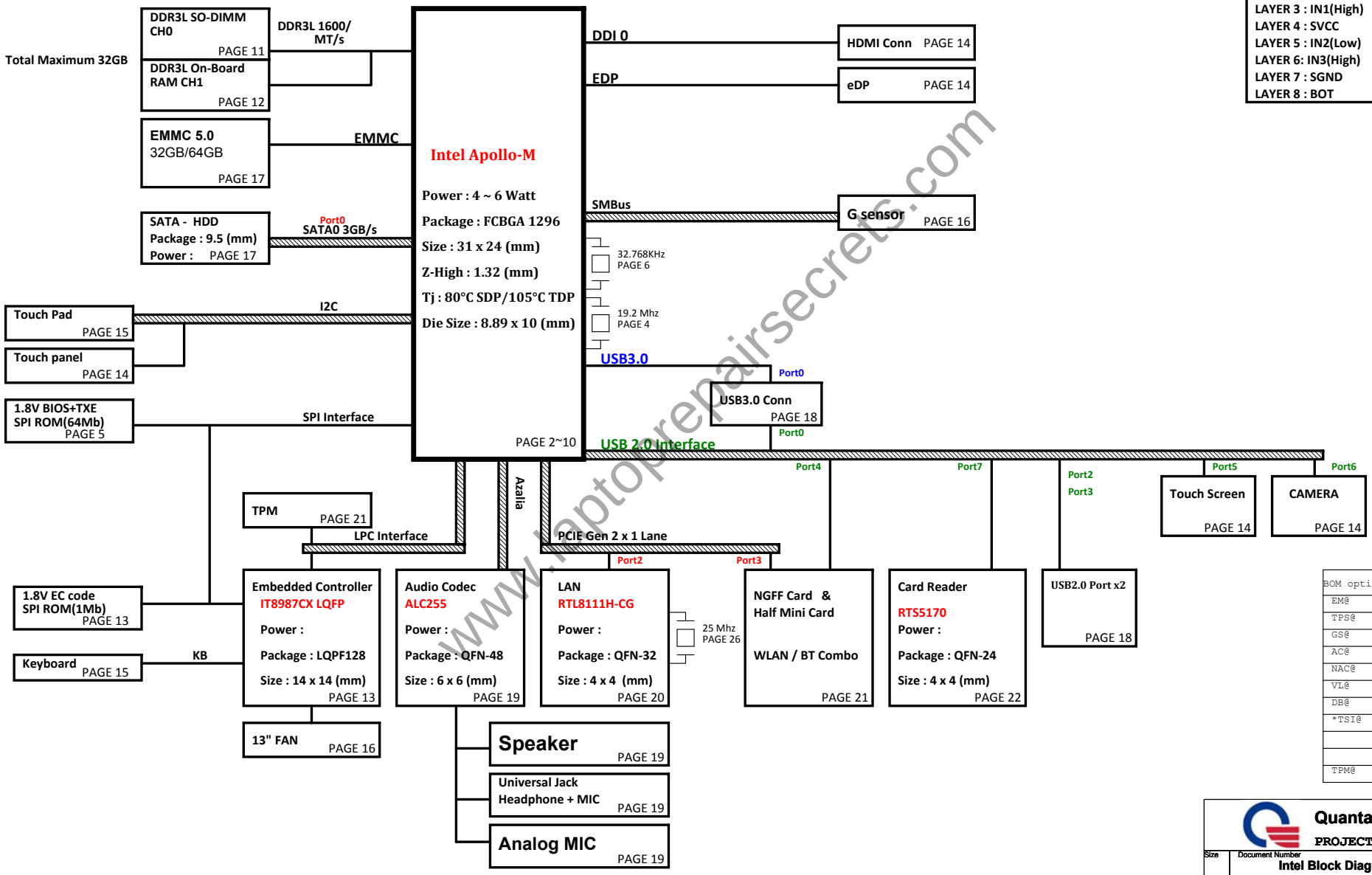
EJ-11/13 ZHP/ZSP (11 and 13")
Intel Apollo Platform Block Diagram

01

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : SVCC
LAYER 5 : IN2(Low)
LAYER 6: IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



BOM option	Note
EM@	EMMC
TPS@	Touch Screen
GS@	G-Sensor
AC@	IOAC
NAC@	Non-IOAC
VL@	LED Backlight
DB@	Debug Conn.
*TSI@	Touch Screen I2C
TPM@	DTPM

Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Tuesday, July 26, 2016 Sheet 1 of 36

+1.35VSUS 3,9,11,12,28

M_A_A[15:0] M_A_A[15:0] 11

M_A_DQ[63:0] M_A_DQ[63:0] 11

U21A BXT_P_SOC_BGA1296

M_A_A0	BG50	DDR3L_CH0_MA0_LPDDR3_CH0_CAB7	DDR3L_CH0_DQ0_LPDDR3_CH0_DQA0	AY62	M_A_DQ0
M_A_A1	BG51	DDR3L_CH0_MA1_LPDDR3_CH0_CAB9	DDR3L_CH0_DQ1_LPDDR3_CH0_DQA1	AY61	M_A_DQ1
M_A_A2	BH51	DDR3L_CH0_MA2_LPDDR3_CH0_CAB5	DDR3L_CH0_DQ2_LPDDR3_CH0_DQA2	BE62	M_A_DQ2
M_A_A3	BD41	DDR3L_CH0_MA3_LPDDR3_NC	DDR3L_CH0_DQ3_LPDDR3_CH0_DQA3	BG62	M_A_DQ3
M_A_A4	BE41	DDR3L_CH0_MA4_LPDDR3_NC	DDR3L_CH0_DQ4_LPDDR3_CH0_DQA4	BD63	M_A_DQ4
M_A_A5	BJ52	DDR3L_CH0_MA5_LPDDR3_CH0_CAA2	DDR3L_CH0_DQ5_LPDDR3_CH0_DQA5	AW62	M_A_DQ5
M_A_A6	BG53	DDR3L_CH0_MA6_LPDDR3_CH0_CAA0	DDR3L_CH0_DQ6_LPDDR3_CH0_DQA6	AW63	M_A_DQ6
M_A_A7	BG55	DDR3L_CH0_MA7_LPDDR3_CH0_CAA3	DDR3L_CH0_DQ7_LPDDR3_CH0_DQA7	BD62	M_A_DQ7
M_A_A8	BH53	DDR3L_CH0_MA8_LPDDR3_CH0_CAA1	DDR3L_CH0_DQ8_LPDDR3_CH0_DQA8	AV59	M_A_DQ8
M_A_A9	BG52	DDR3L_CH0_MA9_LPDDR3_CH0_CAA4	DDR3L_CH0_DQ9_LPDDR3_CH0_DQA9	AU63	M_A_DQ9
M_A_A10	BH49	DDR3L_CH0_MA10_LPDDR3_CH0_CAB6	DDR3L_CH0_DQ10_LPDDR3_CH0_DQA10	AU62	M_A_DQ10
M_A_A11	BH55	DDR3L_CH0_MA11_LPDDR3_CH0_CAA6	DDR3L_CH0_DQ11_LPDDR3_CH0_DQA11	AV58	M_A_DQ11
M_A_A12	BG54	DDR3L_CH0_MA12_LPDDR3_CH0_CAA5	DDR3L_CH0_DQ12_LPDDR3_CH0_DQA12	AV57	M_A_DQ12
M_A_A13	BG46	DDR3L_CH0_MA13_LPDDR3_CH0_CAB0	DDR3L_CH0_DQ13_LPDDR3_CH0_DQA13	AT55	M_A_DQ13
M_A_A14	BG56	DDR3L_CH0_MA14_LPDDR3_CH0_CAA8	DDR3L_CH0_DQ14_LPDDR3_CH0_DQA14	AT54	M_A_DQ14
M_A_A15	BG57	DDR3L_CH0_MA15_LPDDR3_CH0_CAA9	DDR3L_CH0_DQ15_LPDDR3_CH0_DQA15	AY59	M_A_DQ15
			DDR3L_CH0_DQ16_LPDDR3_CH0_DQA16	AY57	M_A_DQ16
11 M_A_BS#0	M_A_BS#0 BJ48	DDR3L_CH0_BA0_LPDDR3_CH0_CAB2	DDR3L_CH0_DQ17_LPDDR3_CH0_DQA17	BB57	M_A_DQ17
11 M_A_BS#1	M_A_BS#1 BG49	DDR3L_CH0_BA1_LPDDR3_CH0_CAB8	DDR3L_CH0_DQ18_LPDDR3_CH0_DQA18	BD59	M_A_DQ18
11 M_A_BS#2	M_A_BS#2 BH57	DDR3L_CH0_BA2_LPDDR3_CH0_CAA7	DDR3L_CH0_DQ19_LPDDR3_CH0_DQA19	BF59	M_A_DQ19
			DDR3L_CH0_DQ20_LPDDR3_CH0_DQA20	AV54	M_A_DQ20
11 M_A_CAS#	M_A_CAS# BH47	DDR3L_CH0_CAS_N_LPDDR3_CH0_CAB1	DDR3L_CH0_DQ21_LPDDR3_CH0_DQA21	AV55	M_A_DQ21
11 M_A_RAS#	M_A_RAS# BG47	DDR3L_CH0_RAS_N_LPDDR3_CH0_CAB3	DDR3L_CH0_DQ22_LPDDR3_CH0_DQA22	AV52	M_A_DQ22
11 M_A_WE#	M_A_WE# BG48	DDR3L_CH0_WE_N_LPDDR3_CH0_CAB4	DDR3L_CH0_DQ23_LPDDR3_CH0_DQA23	BD58	M_A_DQ23
			DDR3L_CH0_DQ24_LPDDR3_CH0_DQA24	BE56	M_A_DQ24
11 M_A_CS#0	M_A_CS#0 AR43	DDR3L_CH0_CS0_N_LPDDR3_CH0_CS0A_N	DDR3L_CH0_DQ25_LPDDR3_CH0_DQA25	BD54	M_A_DQ25
	AT43	DDR3L_NC_LPDDR3_CH0_CS1A_N	DDR3L_CH0_DQ26_LPDDR3_CH0_DQA26	BF58	M_A_DQ26
	BB41	DDR3L_NC_LPDDR3_CH0_CS0B_N	DDR3L_CH0_DQ27_LPDDR3_CH0_DQA27	BE50	M_A_DQ27
11 M_A_CS#1	M_A_CS#1 BA41	DDR3L_CH0_CS1_N_LPDDR3_CH0_CS1B_N	DDR3L_CH0_DQ28_LPDDR3_CH0_DQA28	BD50	M_A_DQ28
			DDR3L_CH0_DQ29_LPDDR3_CH0_DQA29	BB50	M_A_DQ29
11 M_A_CKE0	M_A_CKE0 BH61	DDR3L_CH0_CKE0_LPDDR3_CH0_CKE0A	DDR3L_CH0_DQ30_LPDDR3_CH0_DQA30	BA50	M_A_DQ30
11 M_A_CKE1	M_A_CKE1 BH60	DDR3L_CH0_CKE1_LPDDR3_CH0_CKE1A	DDR3L_CH0_DQ31_LPDDR3_CH0_DQA31	BB54	M_A_DQ31
	BH58	DDR3L_NC_LPDDR3_CH0_CKE0B	DDR3L_CH0_DQ32_LPDDR3_CH0_DQB0	AR39	M_A_DQ32
	BJ58	DDR3L_NC_LPDDR3_CH0_CKE1B	DDR3L_CH0_DQ33_LPDDR3_CH0_DQB1	AV37	M_A_DQ33
			DDR3L_CH0_DQ34_LPDDR3_CH0_DQB2	AW37	M_A_DQ34
11 M_A_ODT0	M_A_ODT0 AW43	DDR3L_CH0_ODT0_LPDDR3_CH0_ODTA	DDR3L_CH0_DQ35_LPDDR3_CH0_DQB3	AR37	M_A_DQ35
11 M_A_ODT1	M_A_ODT1 AW41	DDR3L_CH0_ODT1_LPDDR3_CH0_ODTB	DDR3L_CH0_DQ36_LPDDR3_CH0_DQB4	AT37	M_A_DQ36
			DDR3L_CH0_DQ37_LPDDR3_CH0_DQB5	AT41	M_A_DQ37
11 M_A_VREF_DQ	R271 *0/J_4 MEM_CH0_VREFDQ AT34	MEM_CH0_VREFDQ	DDR3L_CH0_DQ38_LPDDR3_CH0_DQB6	AR41	M_A_DQ38
11 M_A_VREF_CA	R270 *0/J_4 MEM_CH0_VREFCA AR35	MEM_CH0_VREFCA	DDR3L_CH0_DQ39_LPDDR3_CH0_DQB7	AW35	M_A_DQ39
			DDR3L_CH0_DQ40_LPDDR3_CH0_DQB8	BJ44	M_A_DQ40
	R173 105/F_4 DRAM_RCOMP0 AV34	MEM_CH0_RCOMP	DDR3L_CH0_DQ41_LPDDR3_CH0_DQB9	BG39	M_A_DQ41
			DDR3L_CH0_DQ42_LPDDR3_CH0_DQB10	BG40	M_A_DQ42
11 M_A_CLK0	M_A_CLK0 BD45	DDR3L_CH0_CLKP0_LPDDR3_CH0_CLKP_B	DDR3L_CH0_DQ43_LPDDR3_CH0_DQB11	BJ40	M_A_DQ43
11 M_A_CLK0#	M_A_CLK0# BE45	DDR3L_CH0_CLKN0_LPDDR3_CH0_CLKN_B	DDR3L_CH0_DQ44_LPDDR3_CH0_DQB12	BG43	M_A_DQ44
			DDR3L_CH0_DQ45_LPDDR3_CH0_DQB13	BG44	M_A_DQ45
11 M_A_CLK1	M_A_CLK1 BB48	DDR3L_CH0_CLKP1_LPDDR3_CH0_CLKP_A	DDR3L_CH0_DQ46_LPDDR3_CH0_DQB14	BH45	M_A_DQ46
11 M_A_CLK1#	M_A_CLK1# BD48	DDR3L_CH0_CLKN1_LPDDR3_CH0_CLKN_A	DDR3L_CH0_DQ47_LPDDR3_CH0_DQB15	BH41	M_A_DQ47
			DDR3L_CH0_DQ48_LPDDR3_CH0_DQB16	BA34	M_A_DQ48
	M_A_DRAMRST# AR34	DDR3L_CH0_RESET_N_LPDDR3_NC	DDR3L_CH0_DQ49_LPDDR3_CH0_DQB17	BE34	M_A_DQ49
			DDR3L_CH0_DQ50_LPDDR3_CH0_DQB18	BD34	M_A_DQ50
			DDR3L_CH0_DQ51_LPDDR3_CH0_DQB19	BD37	M_A_DQ51
			DDR3L_CH0_DQ52_LPDDR3_CH0_DQB20	BB37	M_A_DQ52
			DDR3L_CH0_DQ53_LPDDR3_CH0_DQB21	BE39	M_A_DQ53
			DDR3L_CH0_DQ54_LPDDR3_CH0_DQB22	BD39	M_A_DQ54
			DDR3L_CH0_DQ55_LPDDR3_CH0_DQB23	BB34	M_A_DQ55
			DDR3L_CH0_DQ56_LPDDR3_CH0_DQB24	BJ38	M_A_DQ56
			DDR3L_CH0_DQ57_LPDDR3_CH0_DQB25	BG34	M_A_DQ57
			DDR3L_CH0_DQ58_LPDDR3_CH0_DQB26	BG33	M_A_DQ58
			DDR3L_CH0_DQ59_LPDDR3_CH0_DQB27	BH33	M_A_DQ59
			DDR3L_CH0_DQ60_LPDDR3_CH0_DQB28	BG38	M_A_DQ60
			DDR3L_CH0_DQ61_LPDDR3_CH0_DQB29	BH37	M_A_DQ61
			DDR3L_CH0_DQ62_LPDDR3_CH0_DQB30	BG37	M_A_DQ62
			DDR3L_CH0_DQ63_LPDDR3_CH0_DQB31	BJ34	M_A_DQ63

			DDR3L_CH0_DQSP0_LPDDR3_CH0_DQSPA0	BB63	M_A_DQS0
			DDR3L_CH0_DQSN0_LPDDR3_CH0_DQSNA0	BC62	M_A_DQS#0
			DDR3L_CH0_DQSP1_LPDDR3_CH0_DQSPA1	AT59	M_A_DQS1
			DDR3L_CH0_DQSN1_LPDDR3_CH0_DQSNA1	AT58	M_A_DQS#1
			DDR3L_CH0_DQSP2_LPDDR3_CH0_DQSPA2	BB59	M_A_DQS2
			DDR3L_CH0_DQSN2_LPDDR3_CH0_DQSNA2	BB58	M_A_DQS#2
			DDR3L_CH0_DQSP3_LPDDR3_CH0_DQSPA3	BD52	M_A_DQS3
			DDR3L_CH0_DQSN3_LPDDR3_CH0_DQSNA3	BB52	M_A_DQS#3
			DDR3L_CH0_DQSP4_LPDDR3_CH0_DQSPB0	AV39	M_A_DQS4
			DDR3L_CH0_DQSN4_LPDDR3_CH0_DQSNB0	AW39	M_A_DQS#4
			DDR3L_CH0_DQSP5_LPDDR3_CH0_DQSPB1	BJ42	M_A_DQS5
			DDR3L_CH0_DQSN5_LPDDR3_CH0_DQSNB1	BG42	M_A_DQS#5
			DDR3L_CH0_DQSP6_LPDDR3_CH0_DQSPB2	BB35	M_A_DQS6
			DDR3L_CH0_DQSN6_LPDDR3_CH0_DQSNB2	BD35	M_A_DQS#6
			DDR3L_CH0_DQSP7_LPDDR3_CH0_DQSPB3	BG36	M_A_DQS7
			DDR3L_CH0_DQSN7_LPDDR3_CH0_DQSNB3	BH35	M_A_DQS#7

Section 1 of 12

AW48	DDR3L_CH0_CB0_LPDDR3_NC
AW47	DDR3L_CH0_CB1_LPDDR3_NC
BB43	DDR3L_CH0_CB2_LPDDR3_NC
AW45	DDR3L_CH0_CB3_LPDDR3_NC
AV48	DDR3L_CH0_CB4_LPDDR3_NC
AV47	DDR3L_CH0_CB5_LPDDR3_NC
BD43	DDR3L_CH0_CB6_LPDDR3_NC
BA45	DDR3L_CH0_CB7_LPDDR3_NC
BD47	DDR3L_CH0_DQSP8_LPDDR3_NC
BB47	DDR3L_CH0_DQSN8_LPDDR3_NC

VREFQD/VREFCA 0 Ohm resistor should be un-stuffed by default. PDG 0.9

10/23 modify it

會缺料

GND

DRAMRST

+1.35VSUS

R323 1K/F_4

12/23 follow Intel PDG 1.0 change R322 to 0 ohm.

CPU M_A_DRAMRST# R322 *short_4 **DRAM** M_A_DRAMRST#_R 11

C252 *0.1u/16V_4

Configuration	Speed (MT/s)	Channels	Raw Card	Maximum Total Capacity (GB)
SODIMM	1333/1600/1867	2	A(2Rx16) C(1Rx16) B(1Rx8) F(2Rx8)	32

Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A

Date: Tuesday, July 26, 2016 Sheet 2 of 36

M_B_A[15:0] — M_B_A[15:0] 12
M_B_DQ[63:0] — M_B_DQ[63:0] 12
+1.35VSUS 2,9,11,12,28

U21B — BXT_P_SOC_BGA1296

M_B_A0	BG9	DDR3L_CH1_MA0_LPDDR3_CH1_CAB7	DDR3L_CH1_DQ0_LPDDR3_CH1_DQA0 BJ26 M_B_DQ0
M_B_A1	BG10	DDR3L_CH1_MA1_LPDDR3_CH1_CAB9	DDR3L_CH1_DQ1_LPDDR3_CH1_DQA1 BG30 M_B_DQ1
M_B_A2	BH9	DDR3L_CH1_MA2_LPDDR3_CH1_CAB5	DDR3L_CH1_DQ2_LPDDR3_CH1_DQA2 BH31 M_B_DQ2
M_B_A3	BD16	DDR3L_CH1_MA3_LPDDR3_NC	DDR3L_CH1_DQ3_LPDDR3_CH1_DQA3 BG31 M_B_DQ3
M_B_A4	BB16	DDR3L_CH1_MA4_LPDDR3_NC	DDR3L_CH1_DQ4_LPDDR3_CH1_DQA4 BH27 M_B_DQ4
M_B_A5	BG11	DDR3L_CH1_MA5_LPDDR3_CH1_CAA2	DDR3L_CH1_DQ5_LPDDR3_CH1_DQA5 BG27 M_B_DQ5
M_B_A6	BJ12	DDR3L_CH1_MA6_LPDDR3_CH1_CAA0	DDR3L_CH1_DQ6_LPDDR3_CH1_DQA6 BG26 M_B_DQ6
M_B_A7	BG14	DDR3L_CH1_MA7_LPDDR3_CH1_CAA3	DDR3L_CH1_DQ7_LPDDR3_CH1_DQA7 BJ30 M_B_DQ7
M_B_A8	BG12	DDR3L_CH1_MA8_LPDDR3_CH1_CAA1	DDR3L_CH1_DQ8_LPDDR3_CH1_DQA8 BA30 M_B_DQ8
M_B_A9	BH11	DDR3L_CH1_MA9_LPDDR3_CH1_CAA4	DDR3L_CH1_DQ9_LPDDR3_CH1_DQA9 BB30 M_B_DQ9
M_B_A10	BG7	DDR3L_CH1_MA10_LPDDR3_CH1_CAB6	DDR3L_CH1_DQ10_LPDDR3_CH1_DQA10 BE30 M_B_DQ10
M_B_A11	BH13	DDR3L_CH1_MA11_LPDDR3_CH1_CAA6	DDR3L_CH1_DQ11_LPDDR3_CH1_DQA11 BD30 M_B_DQ11
M_B_A12	BG13	DDR3L_CH1_MA12_LPDDR3_CH1_CAA5	DDR3L_CH1_DQ12_LPDDR3_CH1_DQA12 BE25 M_B_DQ12
M_B_A13	BH3	DDR3L_CH1_MA13_LPDDR3_CH1_CAB0	DDR3L_CH1_DQ13_LPDDR3_CH1_DQA13 BB27 M_B_DQ13
M_B_A14	BG15	DDR3L_CH1_MA14_LPDDR3_CH1_CAA8	DDR3L_CH1_DQ14_LPDDR3_CH1_DQA14 BD25 M_B_DQ14
M_B_A15	BG16	DDR3L_CH1_MA15_LPDDR3_CH1_CAA9	DDR3L_CH1_DQ15_LPDDR3_CH1_DQA15 BD27 M_B_DQ15
			DDR3L_CH1_DQ16_LPDDR3_CH1_DQA16 BG24 M_B_DQ16
M_B_BS0	BH6	DDR3L_CH1_BA0_LPDDR3_CH1_CAB2	DDR3L_CH1_DQ17_LPDDR3_CH1_DQA17 BJ20 M_B_DQ17
M_B_BS1	BG8	DDR3L_CH1_BA1_LPDDR3_CH1_CAB8	DDR3L_CH1_DQ18_LPDDR3_CH1_DQA18 BH23 M_B_DQ18
M_B_BS2	BH15	DDR3L_CH1_BA2_LPDDR3_CH1_CAA7	DDR3L_CH1_DQ19_LPDDR3_CH1_DQA19 BJ24 M_B_DQ19
			DDR3L_CH1_DQ20_LPDDR3_CH1_DQA20 BG20 M_B_DQ20
M_B_CAS#	BH4	DDR3L_CH1_CAS_N_LPDDR3_CH1_CAB1	DDR3L_CH1_DQ21_LPDDR3_CH1_DQA21 BG21 M_B_DQ21
M_B_RAS#	BJ6	DDR3L_CH1_RAS_N_LPDDR3_CH1_CAB3	DDR3L_CH1_DQ22_LPDDR3_CH1_DQA22 BH19 M_B_DQ22
M_B_WE#	BH7	DDR3L_CH1_WE_N_LPDDR3_CH1_CAB4	DDR3L_CH1_DQ23_LPDDR3_CH1_DQA23 BG25 M_B_DQ23
			DDR3L_CH1_DQ24_LPDDR3_CH1_DQA24 AT27 M_B_DQ24
M_B_CS#0	BD17	DDR3L_CH1_CS0_N_LPDDR3_CH1_CS0A_N	DDR3L_CH1_DQ25_LPDDR3_CH1_DQA25 AW29 M_B_DQ25
	BB17	DDR3L_NC_LPDDR3_CH1_CS1A_N	DDR3L_CH1_DQ26_LPDDR3_CH1_DQA26 AR27 M_B_DQ26
	AV17	DDR3L_NC_LPDDR3_CH1_CS0B_N	DDR3L_CH1_DQ27_LPDDR3_CH1_DQA27 AT23 M_B_DQ27
M_B_CS#1	AW17	DDR3L_CH1_CS1_N_LPDDR3_CH1_CS1B_N	DDR3L_CH1_DQ28_LPDDR3_CH1_DQA28 AV27 M_B_DQ28
			DDR3L_CH1_DQ29_LPDDR3_CH1_DQA29 AR25 M_B_DQ29
M_B_CKE0	BG18	DDR3L_CH1_CKE0_LPDDR3_CH1_CKE0A	DDR3L_CH1_DQ30_LPDDR3_CH1_DQA30 AR23 M_B_DQ30
M_B_CKE1	BG17	DDR3L_CH1_CKE1_LPDDR3_CH1_CKE1A	DDR3L_CH1_DQ31_LPDDR3_CH1_DQA31 AW27 M_B_DQ31
	BH17	DDR3L_NC_LPDDR3_CH1_CKE0B	DDR3L_CH1_DQ32_LPDDR3_CH1_DQB0 BF6 M_B_DQ32
	BJ16	DDR3L_NC_LPDDR3_CH1_CKE1B	DDR3L_CH1_DQ33_LPDDR3_CH1_DQB1 BD10 M_B_DQ33
			DDR3L_CH1_DQ34_LPDDR3_CH1_DQB2 BE14 M_B_DQ34
M_B_ODT0_R	AW16	DDR3L_CH1_ODT0_LPDDR3_CH1_ODTA	DDR3L_CH1_DQ35_LPDDR3_CH1_DQB3 BB10 M_B_DQ35
M_B_ODT1	AV16	DDR3L_CH1_ODT1_LPDDR3_CH1_ODTB	DDR3L_CH1_DQ36_LPDDR3_CH1_DQB4 BA14 M_B_DQ36
			DDR3L_CH1_DQ37_LPDDR3_CH1_DQB5 BB14 M_B_DQ37
MEM_CH1_VREFDQ	AT30	MEM_CH1_VREFDQ	DDR3L_CH1_DQ38_LPDDR3_CH1_DQB6 BD14 M_B_DQ38
MEM_CH1_VREFCA	AR29	MEM_CH1_VREFCA	DDR3L_CH1_DQ39_LPDDR3_CH1_DQB7 BE8 M_B_DQ39
			DDR3L_CH1_DQ40_LPDDR3_CH1_DQB8 AV12 M_B_DQ40
DRAM_RCOMP1	AV30	MEM_CH1_RCOMP	DDR3L_CH1_DQ41_LPDDR3_CH1_DQB9 BD6 M_B_DQ41
			DDR3L_CH1_DQ42_LPDDR3_CH1_DQB10 BD5 M_B_DQ42
M_B_CLKP0	BD19	DDR3L_CH1_CLKP0_LPDDR3_CH1_CLKP_B	DDR3L_CH1_DQ43_LPDDR3_CH1_DQB11 BB7 M_B_DQ43
M_B_CLKN0	BE19	DDR3L_CH1_CLKN0_LPDDR3_CH1_CLKN_B	DDR3L_CH1_DQ44_LPDDR3_CH1_DQB12 AV10 M_B_DQ44
			DDR3L_CH1_DQ45_LPDDR3_CH1_DQB13 AY9 M_B_DQ45
	BB21		DDR3L_CH1_DQ46_LPDDR3_CH1_DQB14 AY7 M_B_DQ46
	BD21	DDR3L_CH1_CLKP1_LPDDR3_CH1_CLKP_A	DDR3L_CH1_DQ47_LPDDR3_CH1_DQB15 BF5 M_B_DQ47
		DDR3L_CH1_CLKN1_LPDDR3_CH1_CLKN_A	DDR3L_CH1_DQ48_LPDDR3_CH1_DQB16 AU2 M_B_DQ48
			DDR3L_CH1_DQ49_LPDDR3_CH1_DQB17 AT10 M_B_DQ49
M_B_DRAMRST#	AR30	DDR3L_CH1_RESET_N_LPDDR3_NC	DDR3L_CH1_DQ50_LPDDR3_CH1_DQB18 AT9 M_B_DQ50
			DDR3L_CH1_DQ51_LPDDR3_CH1_DQB19 AU1 M_B_DQ51
			DDR3L_CH1_DQ52_LPDDR3_CH1_DQB20 AY5 M_B_DQ52
			DDR3L_CH1_DQ53_LPDDR3_CH1_DQB21 AV5 M_B_DQ53
			DDR3L_CH1_DQ54_LPDDR3_CH1_DQB22 AV6 M_B_DQ54
			DDR3L_CH1_DQ55_LPDDR3_CH1_DQB23 AV7 M_B_DQ55
			DDR3L_CH1_DQ56_LPDDR3_CH1_DQB24 AY2 M_B_DQ56
			DDR3L_CH1_DQ57_LPDDR3_CH1_DQB25 BD2 M_B_DQ57
			DDR3L_CH1_DQ58_LPDDR3_CH1_DQB26 BD1 M_B_DQ58
			DDR3L_CH1_DQ59_LPDDR3_CH1_DQB27 BE2 M_B_DQ59
			DDR3L_CH1_DQ60_LPDDR3_CH1_DQB28 AW1 M_B_DQ60
			DDR3L_CH1_DQ61_LPDDR3_CH1_DQB29 AW2 M_B_DQ61
			DDR3L_CH1_DQ62_LPDDR3_CH1_DQB30 AY3 M_B_DQ62
			DDR3L_CH1_DQ63_LPDDR3_CH1_DQB31 BG2 M_B_DQ63

Section 2 of 12

		DDR3L_CH1_DQSP0_LPDDR3_CH1_DQSPA0	BG28 M_B_DQSP0 — M_B_DQSP0 12
		DDR3L_CH1_DQSN0_LPDDR3_CH1_DQSNA0	BH29 M_B_DQSN0 — M_B_DQSN0 12
		DDR3L_CH1_DQSP1_LPDDR3_CH1_DQSPA1	BD29 M_B_DQSP1 — M_B_DQSP1 12
		DDR3L_CH1_DQSN1_LPDDR3_CH1_DQSNA1	BB29 M_B_DQSN1 — M_B_DQSN1 12
		DDR3L_CH1_DQSP2_LPDDR3_CH1_DQSPA2	BJ22 M_B_DQSP2 — M_B_DQSP2 12
		DDR3L_CH1_DQSN2_LPDDR3_CH1_DQSNA2	BG22 M_B_DQSN2 — M_B_DQSN2 12
		DDR3L_CH1_DQSP3_LPDDR3_CH1_DQSPA3	AV25 M_B_DQSP3 — M_B_DQSP3 12
		DDR3L_CH1_DQSN3_LPDDR3_CH1_DQSNA3	AW25 M_B_DQSN3 — M_B_DQSN3 12
		DDR3L_CH1_DQSP4_LPDDR3_CH1_DQSPB0	BB12 M_B_DQSP4 — M_B_DQSP4 12
		DDR3L_CH1_DQSN4_LPDDR3_CH1_DQSNB0	BD12 M_B_DQSN4 — M_B_DQSN4 12
		DDR3L_CH1_DQSP5_LPDDR3_CH1_DQSPB1	BB5 M_B_DQSP5 — M_B_DQSP5 12
		DDR3L_CH1_DQSN5_LPDDR3_CH1_DQSNB1	BB6 M_B_DQSN5 — M_B_DQSN5 12
		DDR3L_CH1_DQSP6_LPDDR3_CH1_DQSPB2	AT5 M_B_DQSP6 — M_B_DQSP6 12
		DDR3L_CH1_DQSN6_LPDDR3_CH1_DQSNB2	AT6 M_B_DQSN6 — M_B_DQSN6 12
		DDR3L_CH1_DQSP7_LPDDR3_CH1_DQSPB3	BC2 M_B_DQSP7 — M_B_DQSP7 12
		DDR3L_CH1_DQSN7_LPDDR3_CH1_DQSNB3	BB1 M_B_DQSN7 — M_B_DQSN7 12
AR21			
AT21		DDR3L_CH1_CB0_LPDDR3_NC	
AW23		DDR3L_CH1_CB1_LPDDR3_NC	
AW21		DDR3L_CH1_CB2_LPDDR3_NC	
BA19		DDR3L_CH1_CB3_LPDDR3_NC	
AW19		DDR3L_CH1_CB4_LPDDR3_NC	
BA23		DDR3L_CH1_CB5_LPDDR3_NC	
BB23		DDR3L_CH1_CB6_LPDDR3_NC	
		DDR3L_CH1_CB7_LPDDR3_NC	
BD23			
BE23		DDR3L_CH1_DQSP8_LPDDR3_NC	
		DDR3L_CH1_DQSN8_LPDDR3_NC	

VREFQD/VREFCA 0 Ohm resistor should be un-stuffed by default. PDG 0.9

12 M_B_CKE0 — TP14 — TP16

Modify it 10/17

12 M_B_ODT0 — R181 *0/J_4 — TP15

12 M_B_VREF_DQ — R260 *0/J_4 — MEM_CH1_VREFDQ AT30
12 M_B_VREF_CA — R261 *0/J_4 — MEM_CH1_VREFCA AR29

10/23 modify it

會缺料

R166 105/F_4 — DRAM_RCOMP1 AV30

GND

12 M_B_CLKP0 — M_B_CLKP0 BD19
12 M_B_CLKN0 — M_B_CLKN0 BE19

DRAMRST

+1.35VSUS — R146 1K/F_4 — M_B_DRAMRST# — R150 *short_4 — M_B_DRAMRST#_R 12

C103 *0.1u/16V_4

12/23 follow Intel PDG 1.0 change R322 to 0 ohm.

CPU — DRAM

DDR3L SODIMM/Memory Down: Populating CH1 only
Note: Not supported on A-step. Only supported on B-step.

Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

Date: Tuesday, July 26, 2016 Sheet 3 of 36

ZHP CPU P/N A-stage
AJ0QKG2VT00 defalut
AJ0QKG3VT00
AJ0QKG4VT00

5,6,11,13,14,16,17,19,20,21,22,23,26,27,28,29,31,32,33 +3V
5,6,8,10,13,14,15,21,23,25,29,31 +1.8V_S5

U21D BXT_P_SOC_BGA1296

HDMI
14 IN_D2
14 IN_D2#
14 IN_D1
14 IN_D1#
14 IN_D0
14 IN_D0#
14 IN_CLK
14 IN_CLK#

R486 402/F_4
SOC_DDI0_RCOMP_P
SOC_DDI0_RCOMP_N
14 HDMI_HPD_CON
DDI0 HPD
DDI1 HPD

eDP
14 INT_EDP_TXP0
14 INT_EDP_TXN0
14 INT_EDP_TXP1
14 INT_EDP_TXN1

R147 402/F_4
EDP_RCOMP_P
EDP_RCOMP_N
14 INT_eDP_AUXP
14 INT_eDP_AUXN

HDMI
14 SDVO_DATA
14 SDVO_CLK

PCH_DISP_ON_C C47
PCH_EDP_BLON_C B47
PCH_DPST_PWM_C C46

XTAL19_OUT P29
XTAL19_IN R27

MDSI_RCOMP AP7 MDSI_RCOMP 150/F_4 R492
MCSI_DPHY1.2_RCOMP F27 MNPH_RCOMP 150/F_4 R104
MCSI_DPHY1.1_RCOMP H27 MCSI_RCOMP 150/F_4 R109

Section 4 of 12

PCH_DISP_ON_C R86 *100K_4
PCH_EDP_BLON_C R85 *100K_4
PCH_DPST_PWM_C R87 *100K_4
+1.8V_S5
follow CRB v1.0

+3V
R35 10K_4
R45 10K_4
PCH_DISP_ON 14
Q3 PJA138K
PCH_DISP_ON_C 2
Q9 PJA138K
GND

+3V
R36 10K_4
R49 10K_4
PCH_EDP_BLON 14
Q4 PJA138K
PCH_EDP_BLON_C 2
Q8 PJA138K
GND

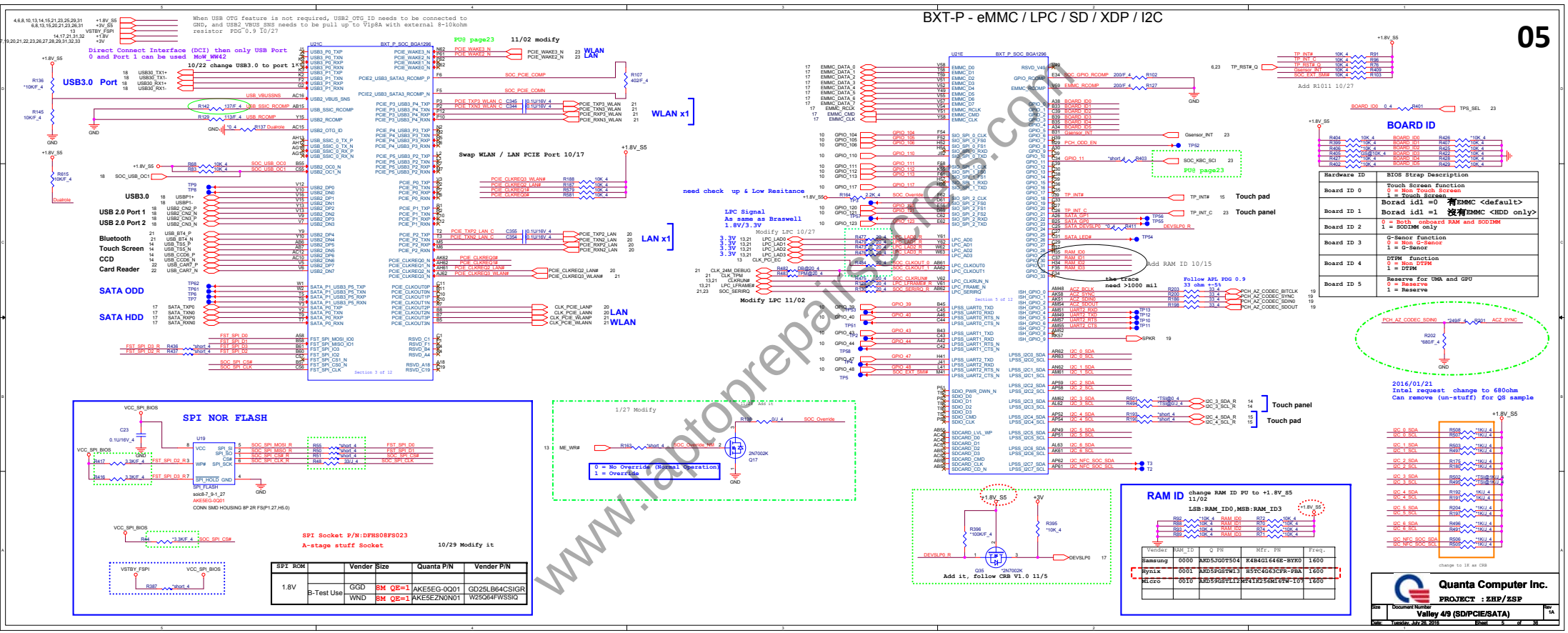
+3V
R30 10K_4
R46 10K_4
PCH_DPST_PWM PCH_DPST_PWM 14
Q5 PJA138K
PCH_DPST_PWM_C 2
Q6 PJA138K
GND

15P/50V_4 C320
XTAL19_OUT
R431 200K/F_4
Y3 19.2MHZ +-20PPM
XTAL19_IN
15P/50V_4 C319
GND

2nd source:BG619200014 (TXC)

Remove barswell hardware strap pin
GP_CAMERASB08/GP_CAMERASB09/GP_CAMERASB11
10/22

Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: Valley 3/9 (Display) | Rev 1A
Date: Tuesday, July 26, 2016 | Sheet 4 of 36


BXT-P - eMMC / LPC / SD / XDP / I2C
05
USB3.0 Port
WLAN x1
LAN x1
SATA ODD
SATA HDD
SPI NOR FLASH
BOARD ID
Touch pad
Touch panel
RAM ID
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Valley 4/9 (SD/PCIE/SATA)
www.laptoprepairforum.com

All PMU can set to 1.8/3.3V
ZHP set to3.3V

Modify 11/14

Pin AG55 is EMMC_PWR_EN_N (CRB 1.0)

12/23 follow Intel PDG 1.0 change R435 to 1K ohm.

10/28 Modify PMU Voltage to 3.3V

Modify 11/04

Touch panel

10/21 change TP_RST to GPIO follow CRB

SMB can set to 3.3V

Unstuff R740 10/17 WoW_WW31

Apollo EDS pin腳有錯 need check

the trace need >1000 mil

Follow CRB 33 ohm +-5%

RTC Clock 32.768KHz

2013/07/25 change package , P/N change from BG332768224 to BG332768453

Add 10p to GND for layout length too long 11/26

Change from +1.0V to +1.05V

可能缺料

SVID_CLK : UP:85 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:170 ohm Series:20 ohm

For Intel MoW04

THERMALTRIP#

Modify it 10/28

AC Present: This input pin indicates when the platform is plugged into AC power.

12/17 Modify

RTC Circuitry(RTC)

20 mils

20MIL

30mils

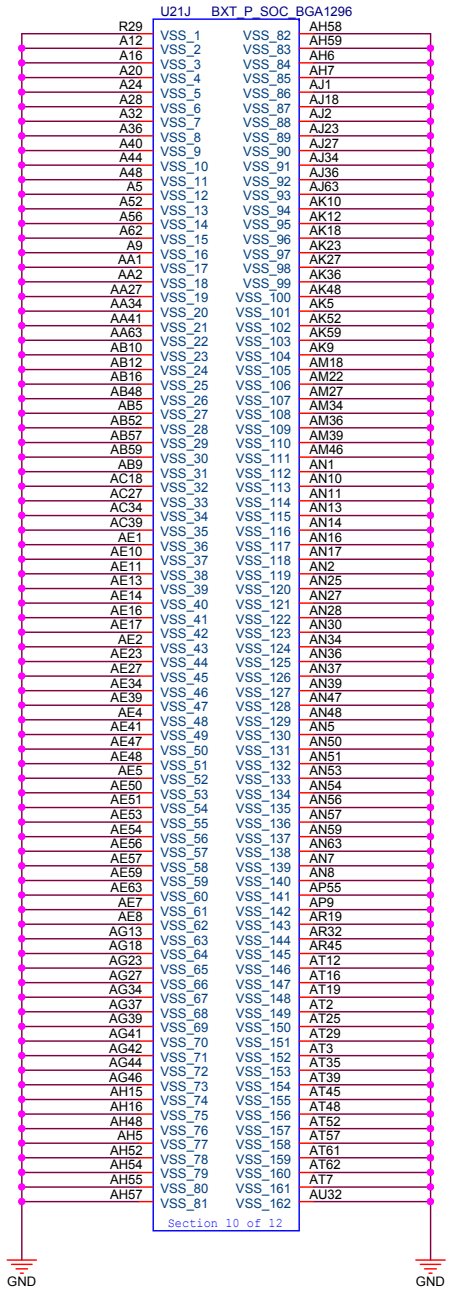
20mils

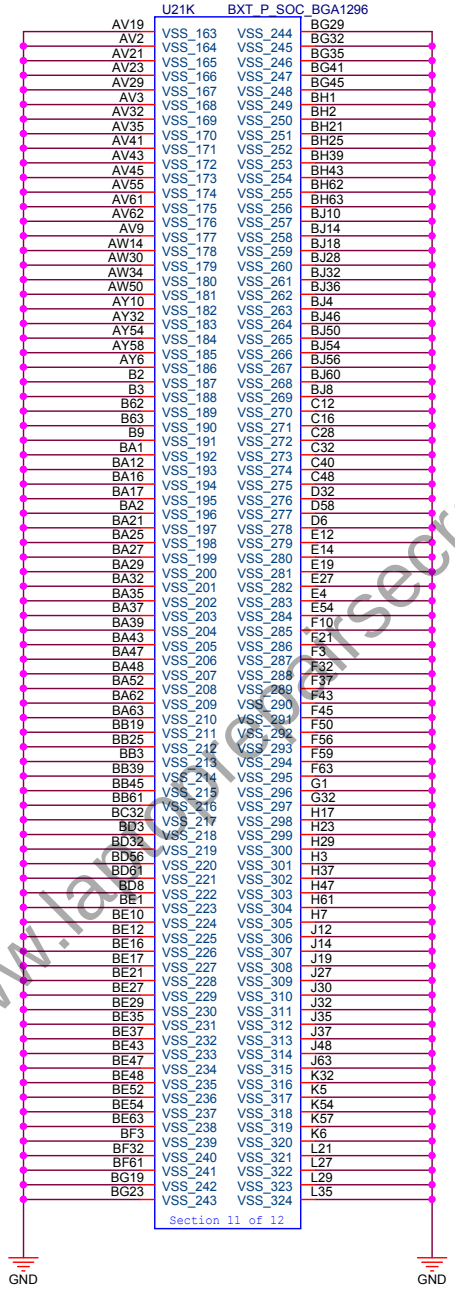
Change G1、G2 footprint from "SOLDERJUMPER-2" to "RC0603-C" for SMT request

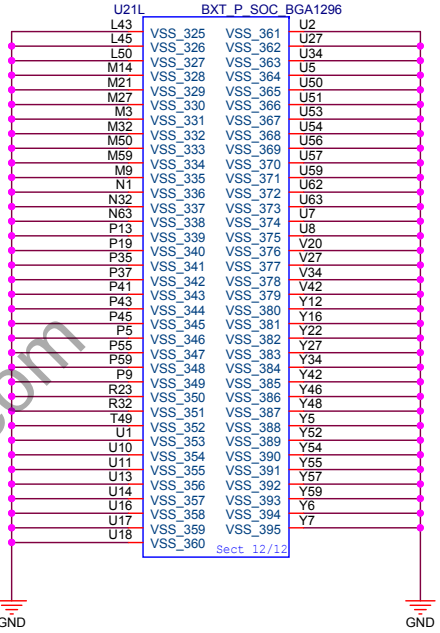
12/25 PE Request change to ML1220

EC RSET RTC

Quanta Computer Inc.
PROJECT : ZHP/ZSP
Valley 6/9 (USB/LPC/I2C)
Size: Document Number: Rev 1A
Date: Tuesday, July 26, 2011 Sheet 6 of 36





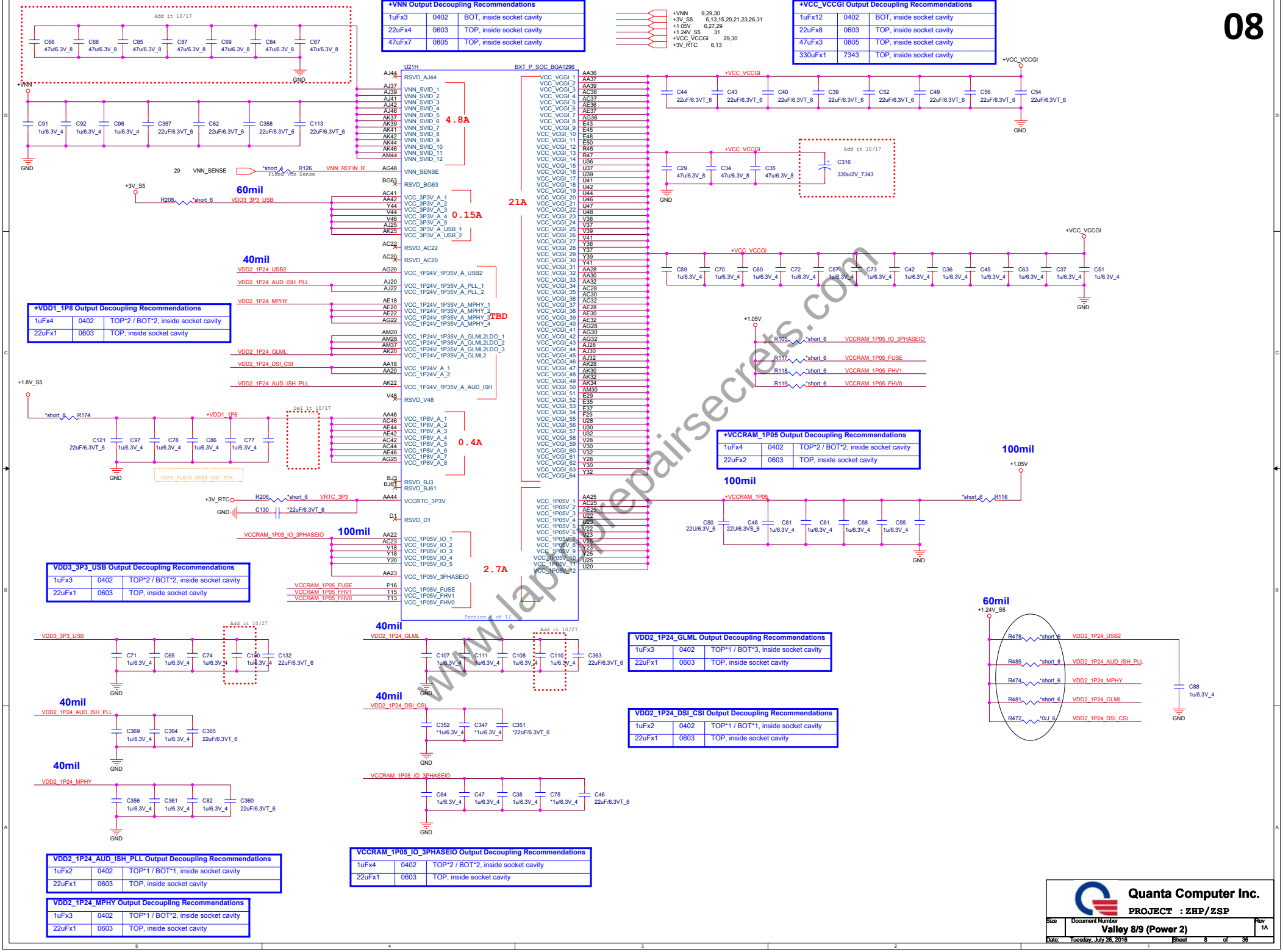


07

Quanta Computer Inc.

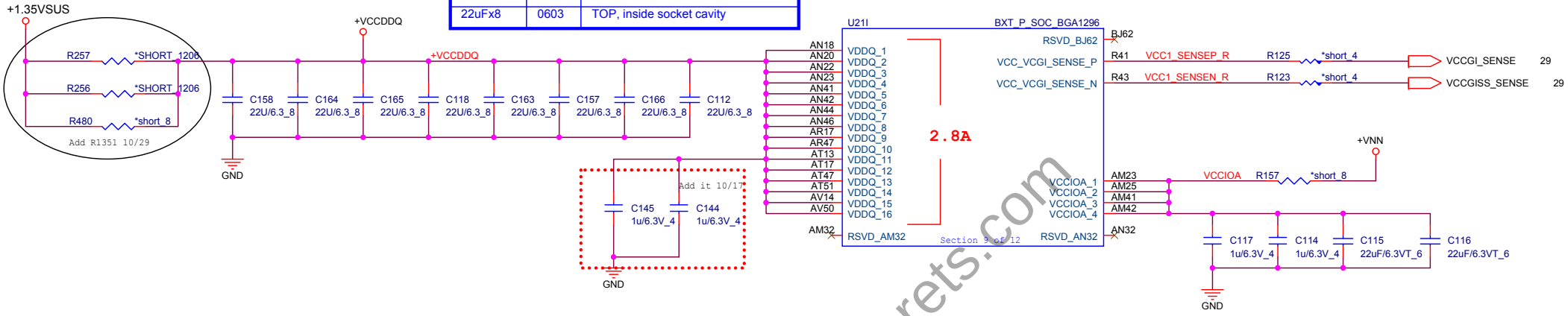
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 7/9 (Power 1)	1A
Date: Tuesday, July 26, 2016	Sheet 7 of 36	

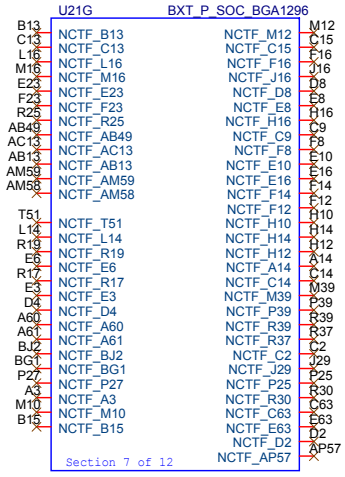


+1.05V 6,8,27,29
+1.35VSUS 2,3,11,12,28
+VNN 8,29,30

+VCCDDQ Output Decoupling Recommendations		
1uFx2	0402	BOT, inside socket cavity
22uFx8	0603	TOP, inside socket cavity



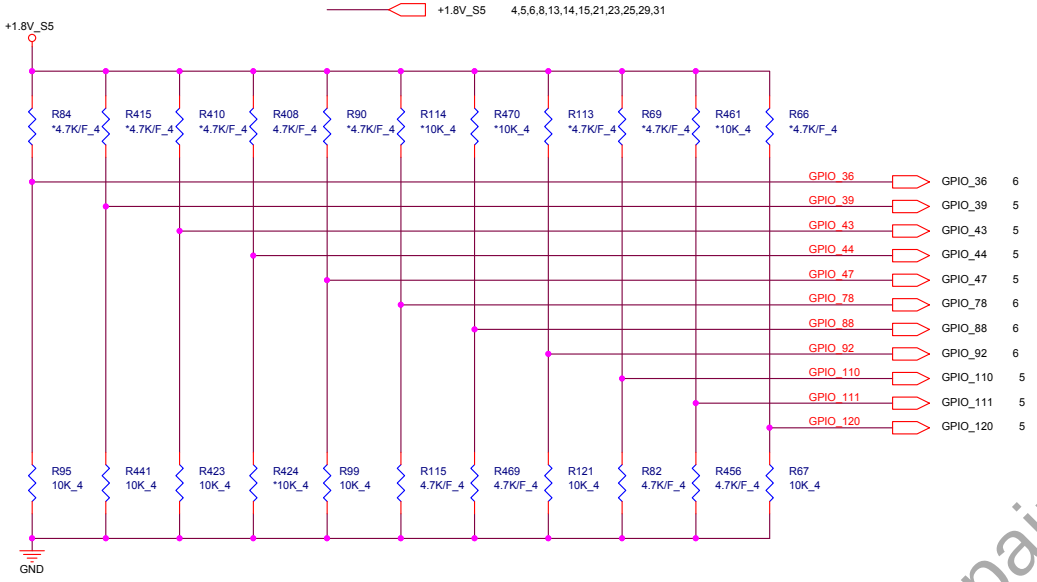
VCCIOA Output Decoupling Recommendations		
1uFx2	0402	TOP, inside socket cavity
22uFx2	0603	TOP, inside socket cavity

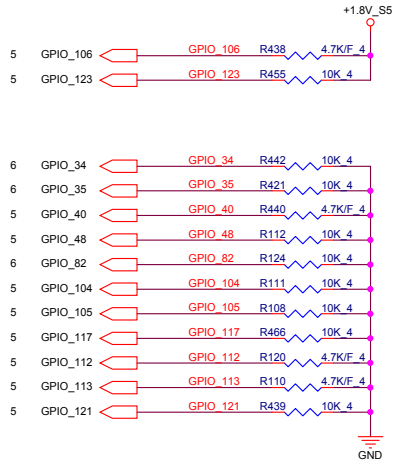


Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Tuesday, July 26, 2016 Sheet 9 of 36





Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = Disable 1 = Enable

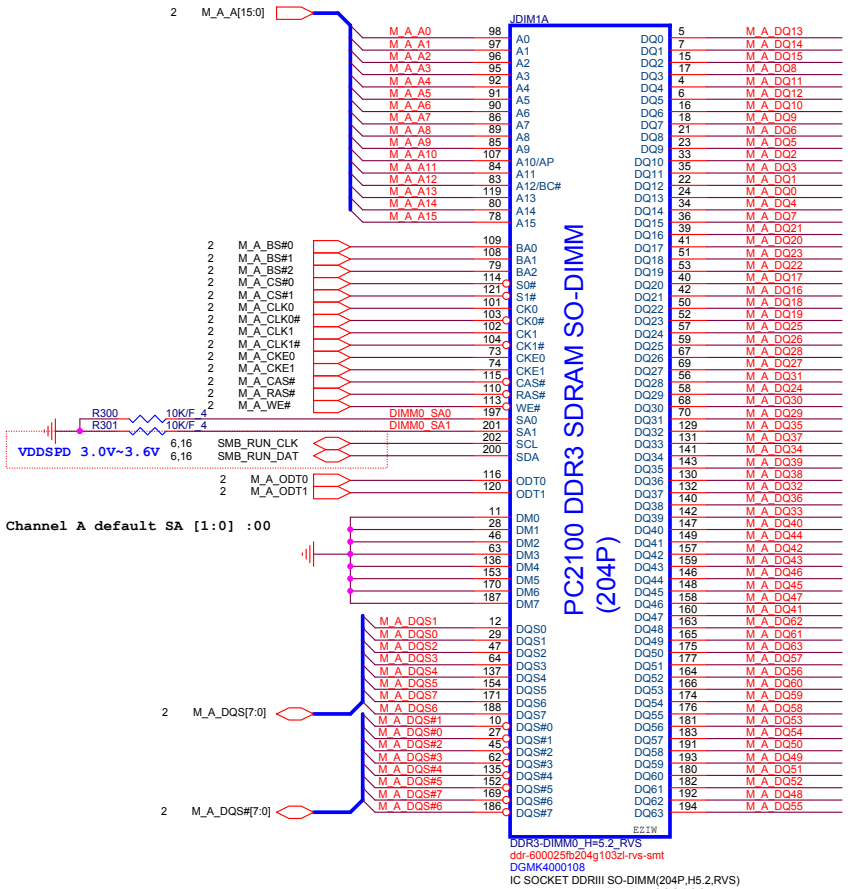
Note: This strap will only be used for B-step.
For A-step this rails should only be set at 1.24V

B Stage change to 3.3V

Hardware Strap to enable boot from SPI
If the platform design wants to have BIOS Boot form SPI then please ensure you have the following setting for hardware strap:
GPIO_43 = 0 [Disable eMMC boot]
GPIO_44 = 1 [Enable SPI Boot]
MoW_WW36

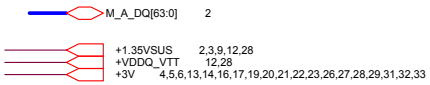
Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_40/GPIO_48/GPIO_104/GPIO_105/GPIO_112/GPIO_113/GPIO_117/GPIO_121 PD
GPIO_106/GPIO_123 PU

Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: Hardware Strap | Rev: 1A
Date: Tuesday, July 26, 2016 | Sheet 10 of 36

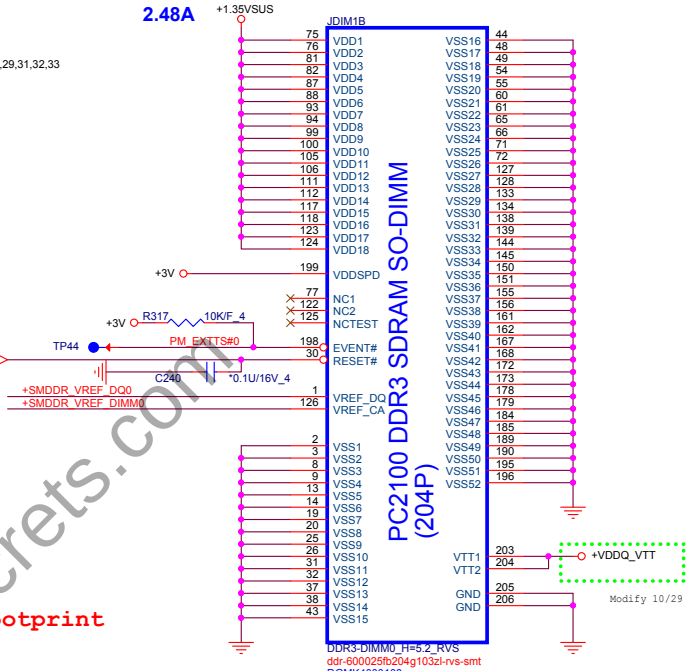


Channel A default SA [1:0] :00

Swap DQ & DQS 10/27

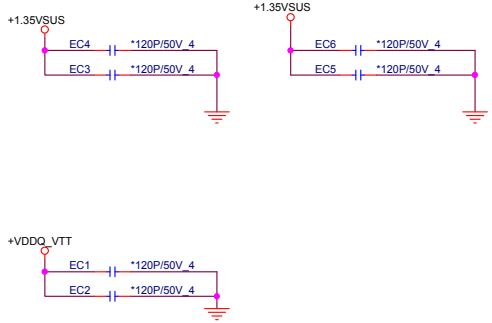


2.48A



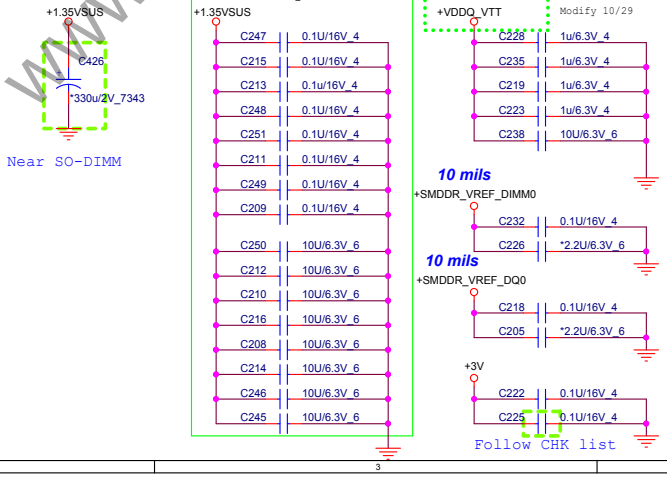
10/16 change to footprint

For EMI RESERVE

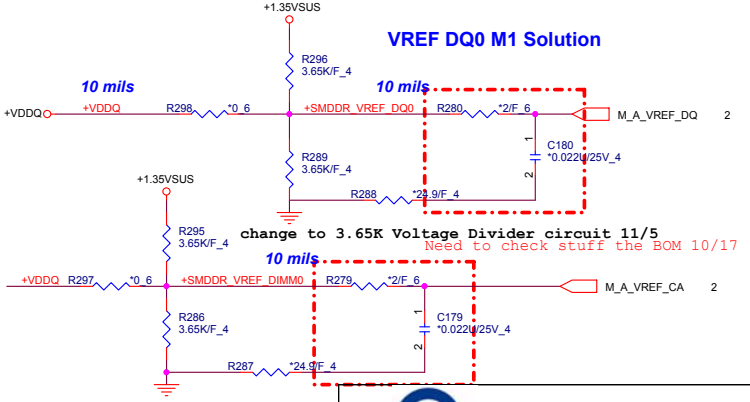


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



Correct CHA VREF_DQ/CA net name 10/29

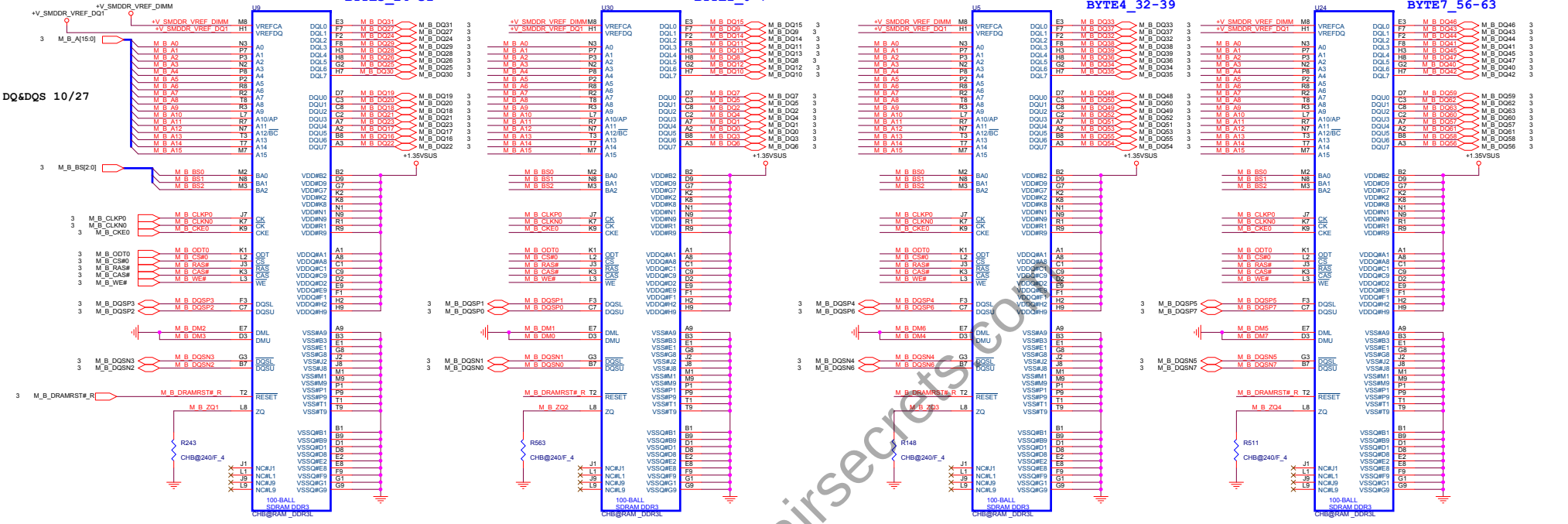
Quanta Computer Inc.		
PROJECT : ZHP/ZSP		
Size	Document Number: DDR3 DIMM0-STD(5.2H)	Rev: 1A
Date: Tuesday, July 26, 2016	Sheet 11 of 36	

On board memory (OBM)

DDR3L MEMORY CHANNEL B

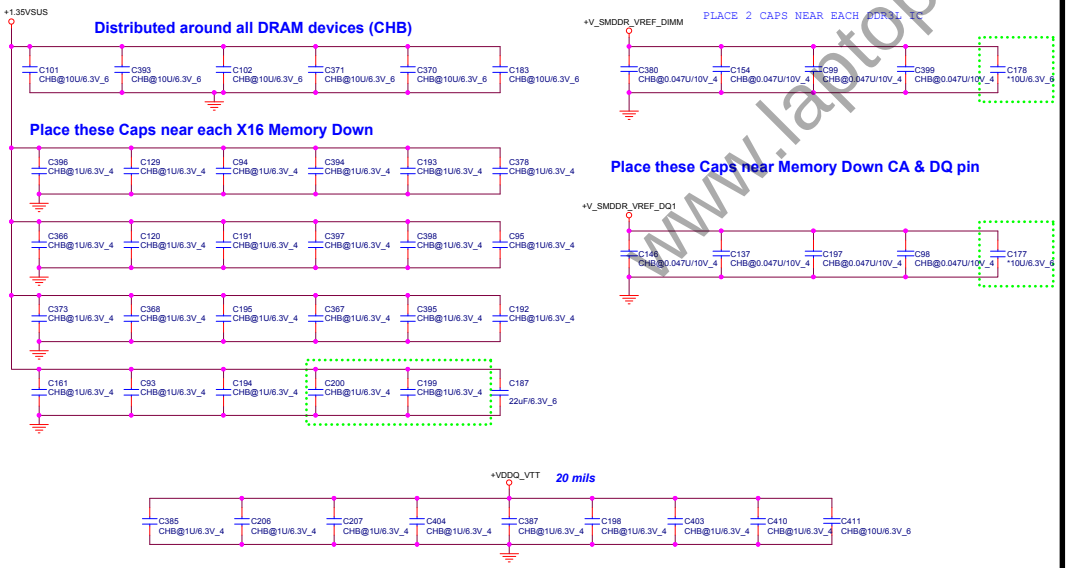
BYTE2_16-23
BYTE3_24-31
BYTE0_8-15
BYTE1_0-7
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63

Swap DQ&DQS 10/27

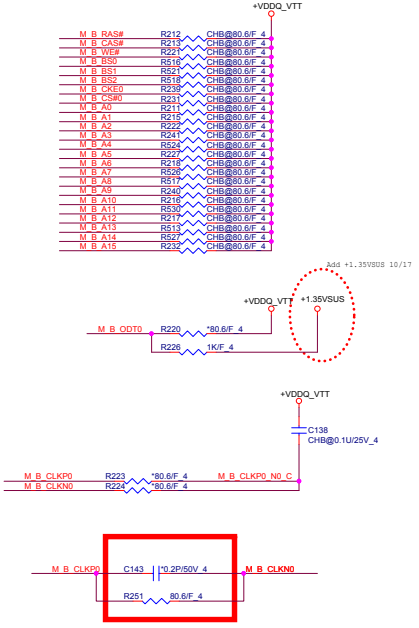


Hynix AKD5JGETW00--H5TC4G63AFR-PBA

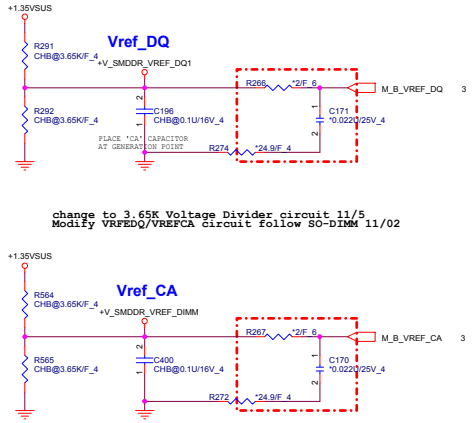
DE-CAPS FOR MEMORY CHANNEL B



VTT TERMINATIONS



VREF_DQ CIRCUIT
VREF_CA_CIRCUIT



Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 CHB	1A
Date: Tuesday, July 26, 2016	Sheet 12 of 36	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

IT8987 LQFP

IT8987E/CX

LPC | GPIO | SM BUS | PS/2 | CIR | PWM | UART port | WAKE UP | EXTERNAL SERIAL FLASH | SPI ENABLE | KBMX | A/D D/A | CLOCK

PIN	PANEL_LED_EN	Active H
GPC0	Only for 2 cell battery	

Sawp TS_EN and CPUFAN# 10/23

The sequence requirement for "VCC 1P05 High (90%) to SOC_PWROK (PCH_PWROK)" assertion timing is minimum of 5mS (Min = 5mS). There is no maximum timing requirement for this sequence. This will be updated in the next revision of Apollo Lake EDS MoW_WW39

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU Thermal
SM Bus 3	
SM Bus 4	

Modify 10/27

開EC對底下SPI ROM的interface

SM BUS PU(KBC)

Change 2nd SMBUS PU to +3V 11/3

Power auto recovery

Modify 12/16 B-Test mount

Battery B/I SW

To battery B/I pin

Battery disable when shell opened

Vgs = 1.5V

Reset Battery

HWID

12/09 EC request ZHP/ZSP ID PD.
ZHP(11" KB)---L (eDP Cable pull-low)
ZHP(13" KB)---H

HWPG(KBC)

Remove SYS_HWPG for HWPG 10/26

SPI NOR FLASH

SPI Socket P/N:DFHS08FS023
A-stage stuff Socket

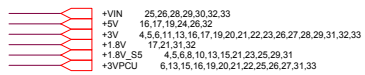
CONN SMD HOUSING 8P 2R FS(P1.27,H5.0)

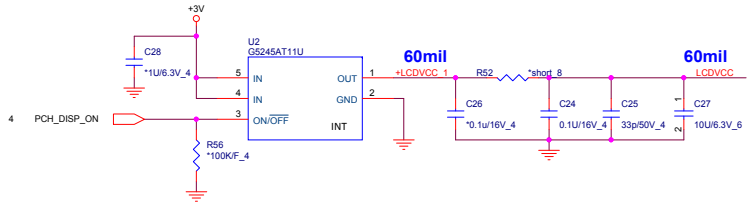
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	1M	AKE5GZP0N00	W25Q80BWSSIG
	EON	1M	AKE5GFN0Q00	EN25S80A-104HIP
	Giga	1M	AKE5GZN0Q00	GD25LQ80BSIGR

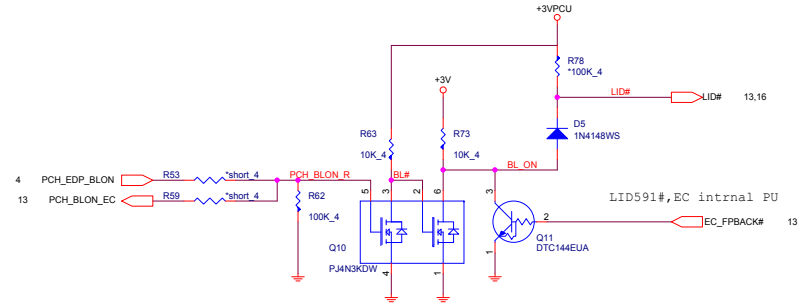
Add SYS_SHDN# 10/27

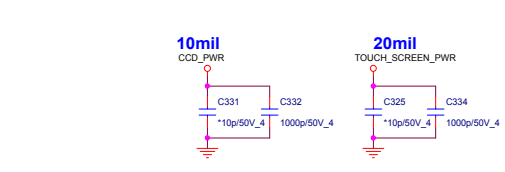
Quanta Computer Inc.
PROJECT : ZHP/ZSP
KBC IT8987CX
Size | Document Number | Rev 1A
Date: Tuesday, July 26, 2016 | Sheet 13 of 36

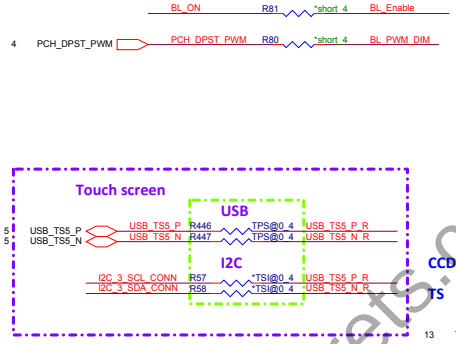
EDP Conn.



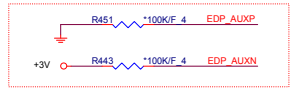




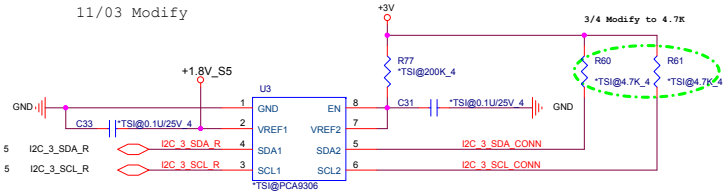


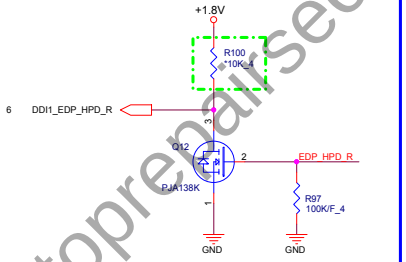


2nd source:DFHS40FS150



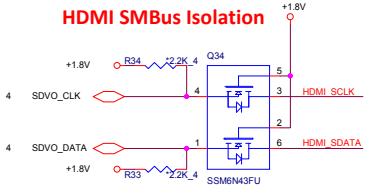
Touch screen level shift I2C(reserve)





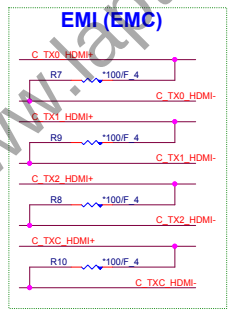
HDMI Conn.

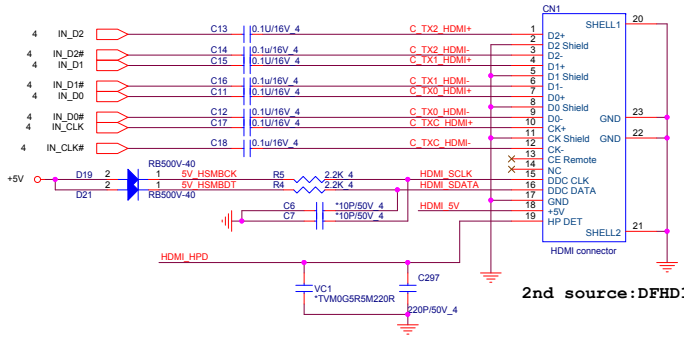
HDMI SMBus Isolation



Intel Requesrt Rds_ON <3.5ohm

EMI (EMC)

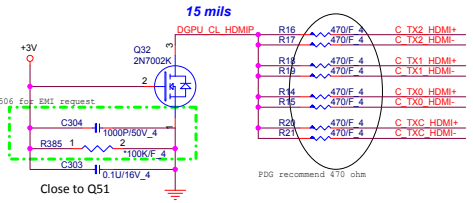




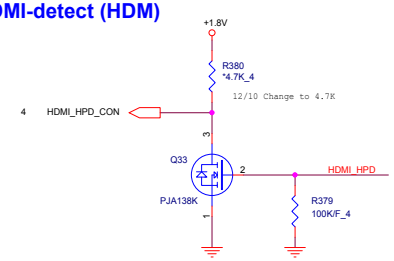
2nd source:DFHD19MRXXX

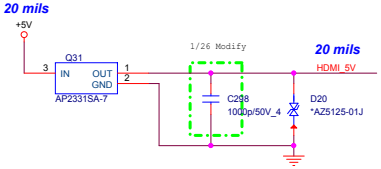
HDMI-Level shift (HDM)

Close to HDMI connector



HDMI-detect (HDM)

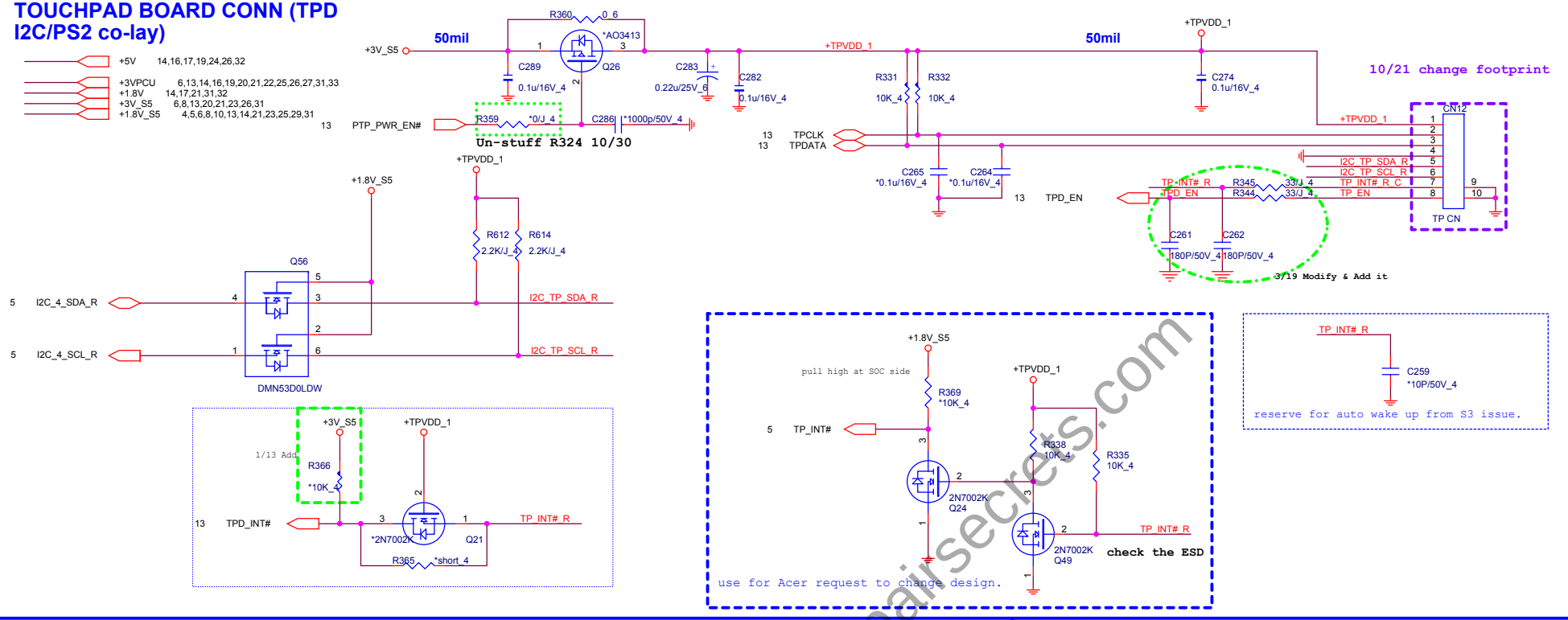




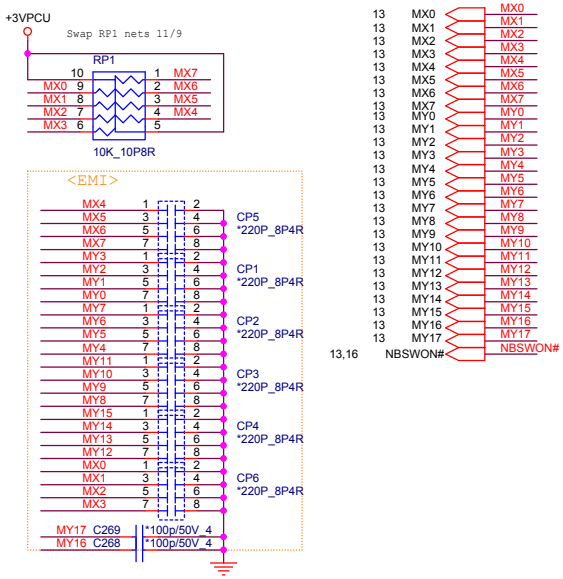
Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	LCD/HDMI/Camera	1A
Date: Tuesday, July 26, 2016	Sheet 14 of 36	

TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

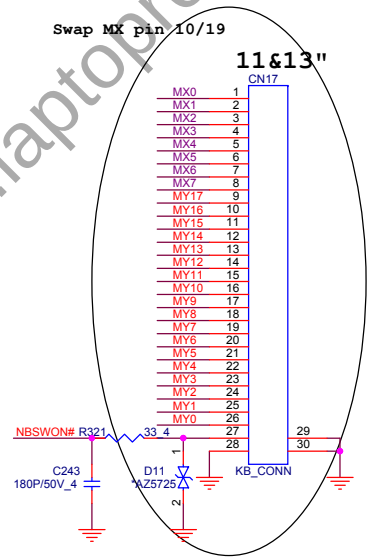


KEYBOARD (KBC)



SWAP KB nets 10/21

Swap MX pin 10/19

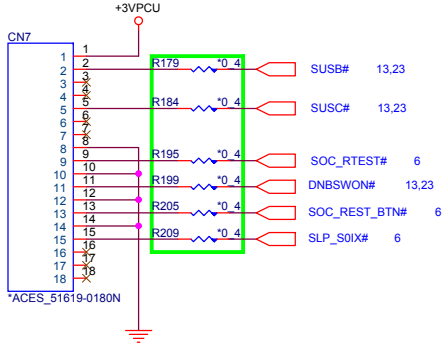


10/13 change KB connector

KB_BL LED (KBC)

Del KB LED 10/19

Intel APS Fixture use

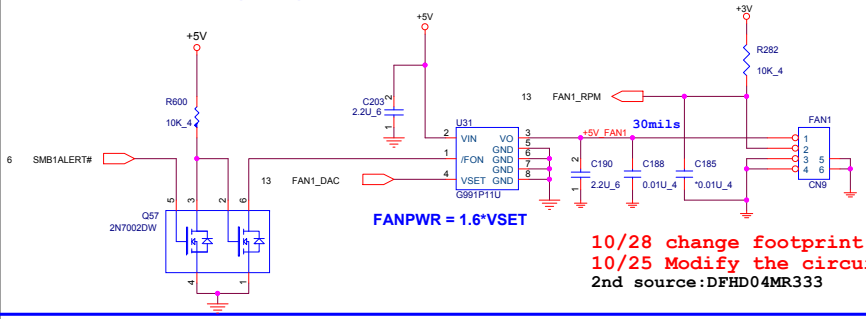


Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A
Date: Tuesday, July 26, 2016	Sheet 15 of 36	

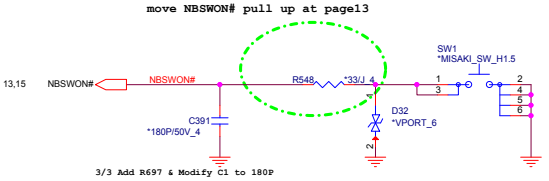
CPU FAN CTRL(THM)



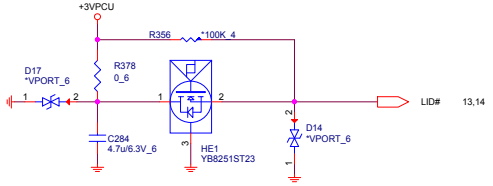
FANPWR = 1.6*VSET

10/28 change footprint
10/25 Modify the circuit
2nd source:DFHD04MR333

Power Switch. (FSW)



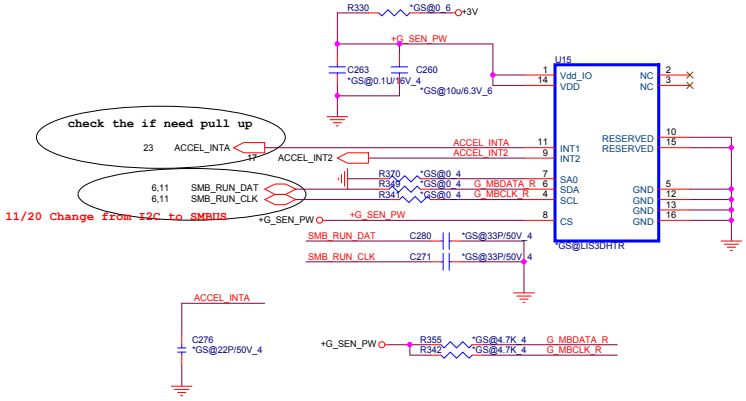
Hall Sensor (HSR)



1st : YB8251000-- YBT
2nd : AL001691000 -- OCS

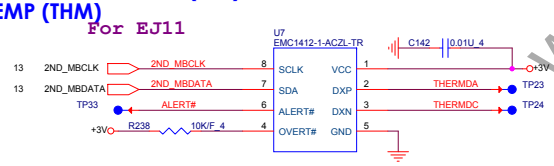
Modify 10/31

G-sensor(GRS)



CPU Thermal sensor(THS) / MB Local TEMP (THM)

For EJ11



Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

Quanta Computer Inc.
PROJECT ZHP/ZSP

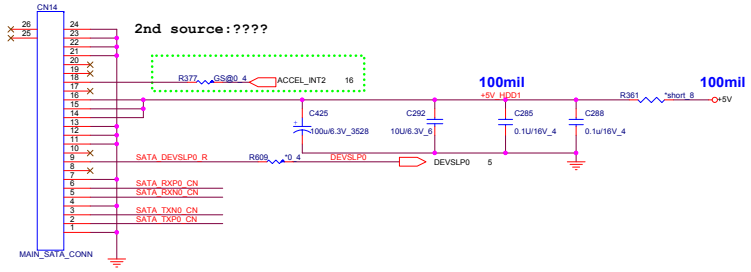
Size	Document Number	Rev
	FAN/BSW/THM/HSR	1A

Date: Tuesday, July 26, 2016 Sheet 16 of 36

SATA HDD

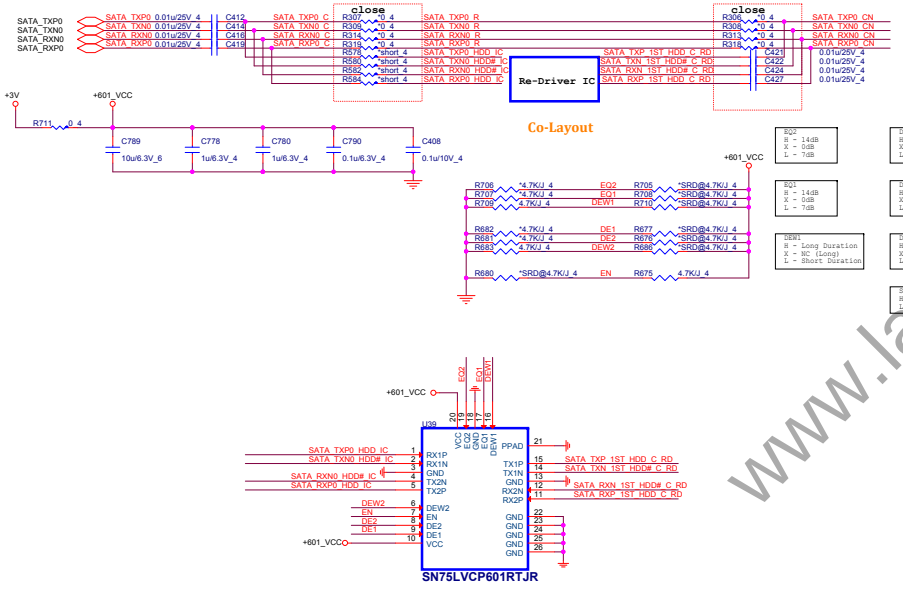
Cable Type
MAIN SATA HDD

10/19 change CN27 Pin define following ZHA/Z09



+5V 14,16,19,24,26,32
+1.8V 14,21,31,32
+3V 4,5,6,11,13,14,16,19,20,21,22,23,26,27,28,29,31,32,33

HDD1 SATA Re-driver

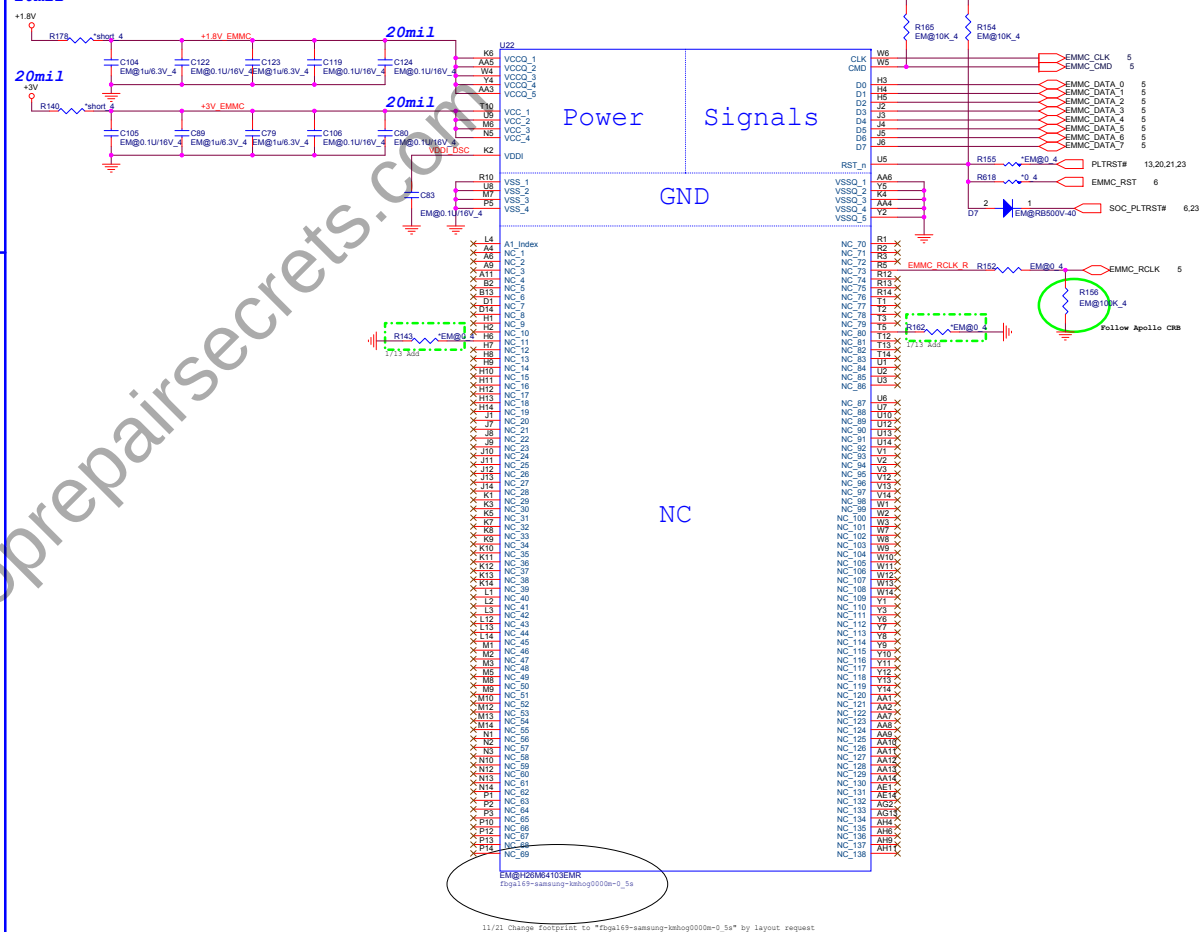


Co-Layout

eMMC

Density	eMMC P/N	Vender
32GB	AKE3SZ-TW09	Hynix
		Kingston
64GB	AKE3TZ-TW00	Hynix
	AKE3UZFT502	Samsung

10 ohm to improve SI
Point to point connection to the corresponding pin at eMMC device.D0-D7/CMD/CLK



11/21 Change footprint to "fbga169-samsung-kmhog0000m-0_5s" by layout request

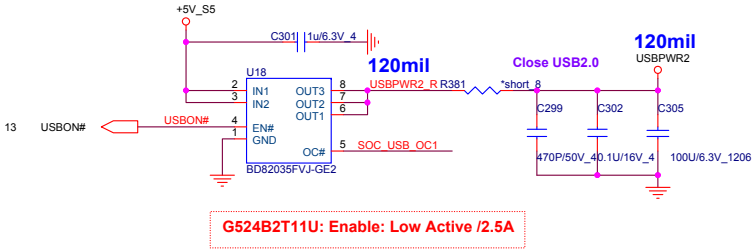
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: SATA HDD/SATA REDRIVER | Rev 1A
Date: Tuesday, July 26, 2016 | Sheet 17 of 36

USB 2.0 X 2

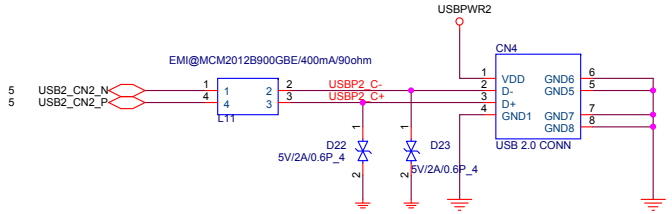
+3V_S5 6,8,13,15,20,21,23,26,31
+3V 4,5,6,11,13,14,16,17,19,20,21,22,23,26,27,28,29,31,32,33
+5V_S5 6,26,28,29,30,33

10/22 change footprint

USB 2.0 Port1

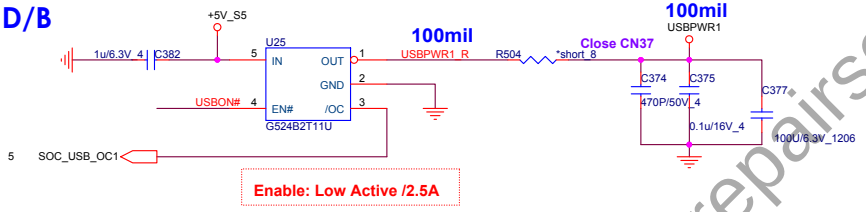


G524B2T11U: Enable: Low Active /2.5A



2nd source:DFHS04FR789

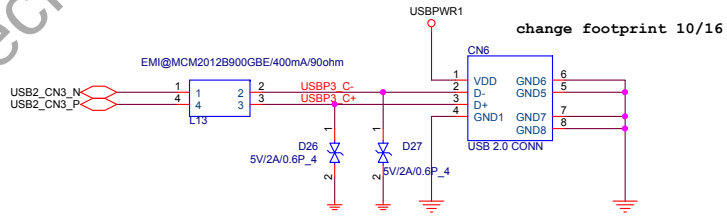
USB IO D/B



Enable: Low Active /2.5A

USB 2.0 Port2

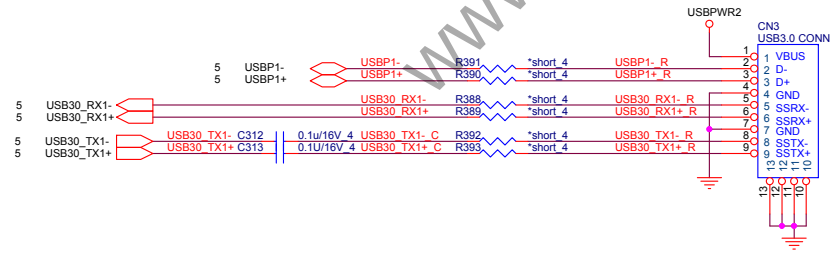
change footprint 10/16



2nd source:DFHD04MR219

10/22 change footprint

USB 3.0 Port1

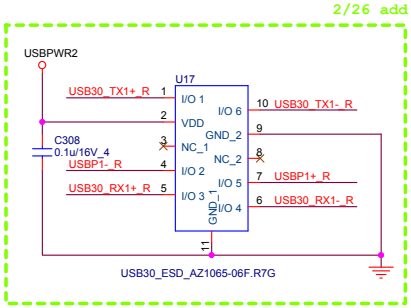


2nd source:DFHS09FR462

10/20 change footprint

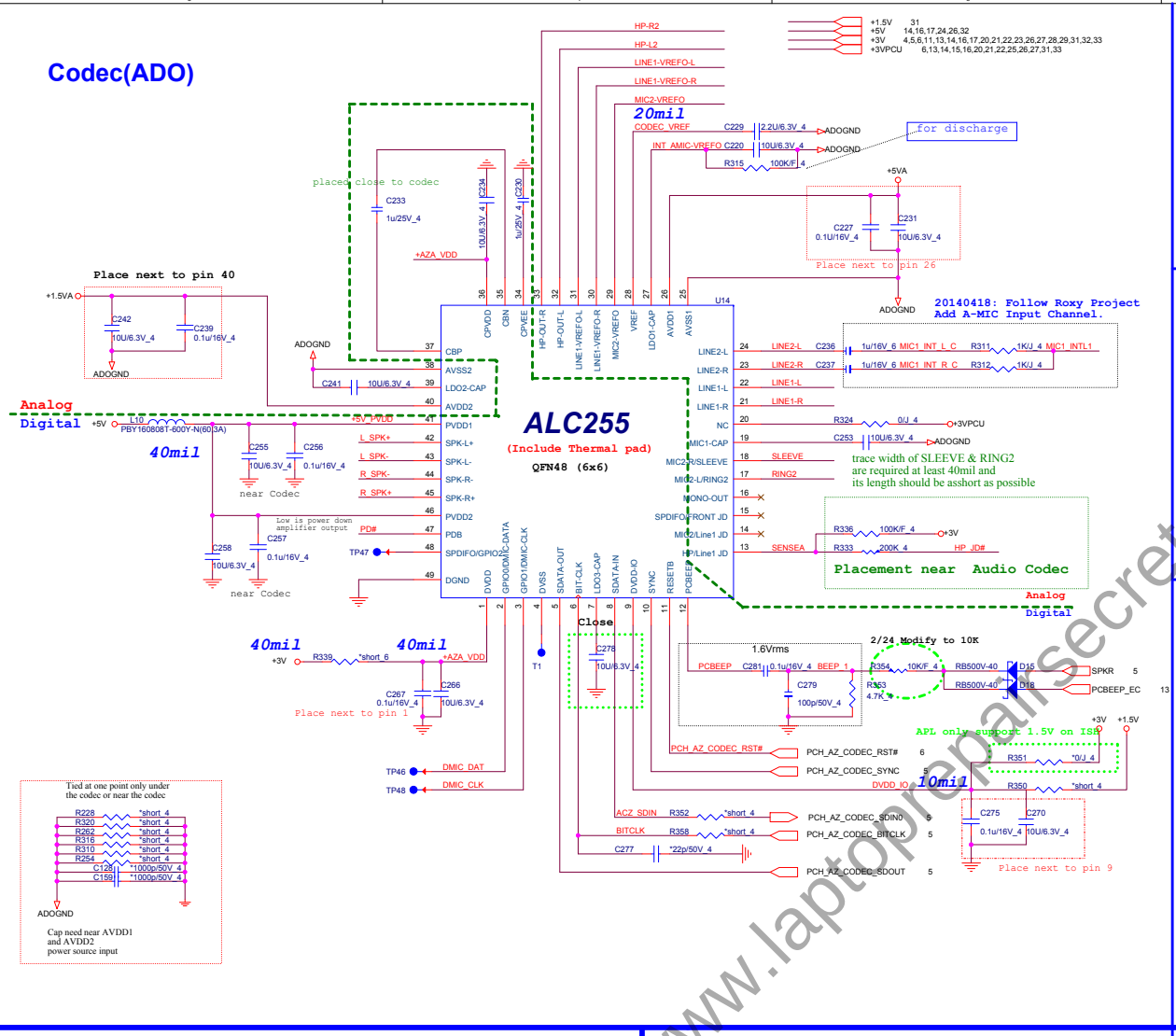
10/22 change to Port 1

2/26 add



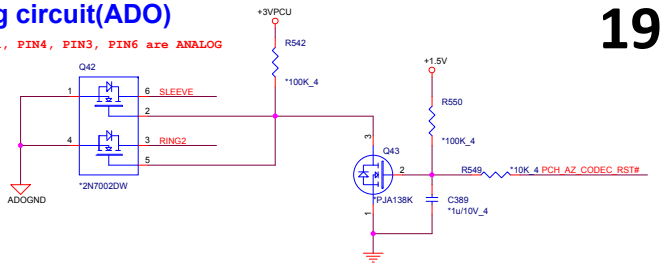
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: USB CONN/USB HUB | Rev 1A
Date: Tuesday, July 26, 2016 | Sheet 18 of 36

Codec(ADO)

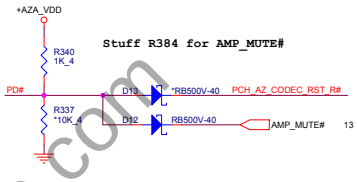


Grounding circuit(ADO)

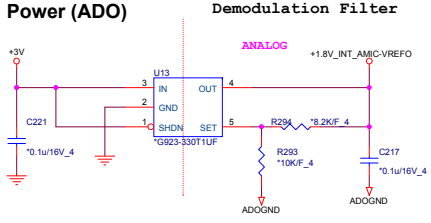
PIN1, PIN4, PIN3, PIN6 are ANALOG



Mute(ADO)



Power (ADO)



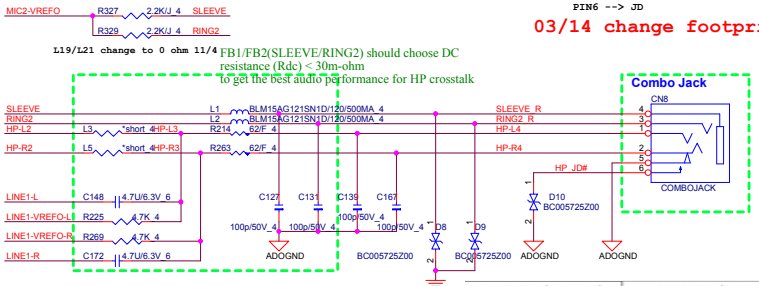
HEADPHONE/MIC/LINE combo (ADO)

Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC(Nokia/iPhone)
PIN4 --> MIC/GND(iPhone/Nokia)
PIN5 --> GND
PIN6 --> JD

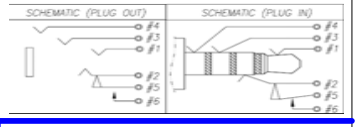
03/14 change footprint

L19/L21 change to 0 ohm 11/4

FB1/FB2(SLEEVE/RING2) should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk

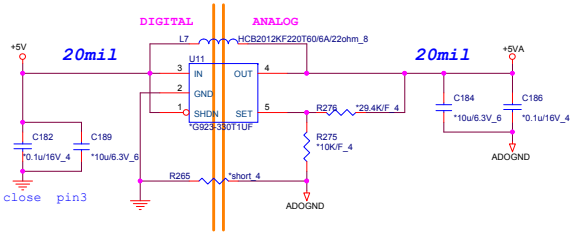


Change R481/R484 value to 62 ohm 12/27

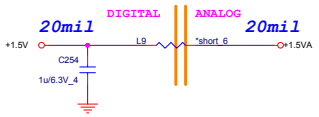


COMPRESSED IMAGE

Codec PWR 5V(ADO)



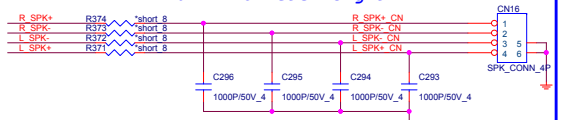
Codec PWR 1.5V(ADO)



Internal Speaker

PE Request CN16 12/25 change footprint

40mil for each signal

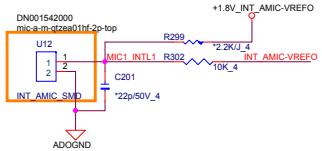


Place these EMI components next to codec 2016/01/19
SMT request change to CH21006JB10

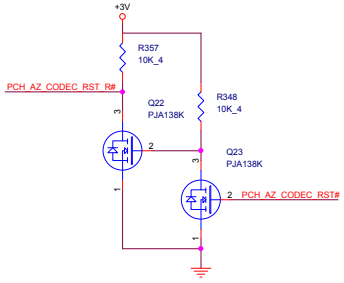
A-Mic

Analog-MIC

8/1 Change CN1 footprint to mic-a-m-qtzea01hf-2p-top .



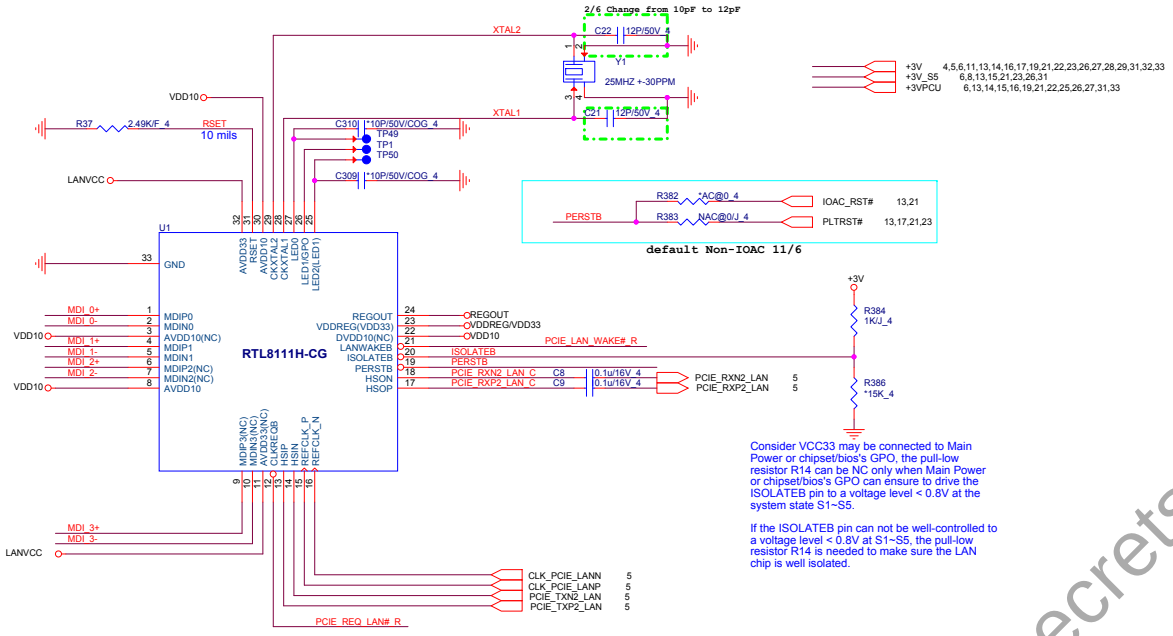
Level shift

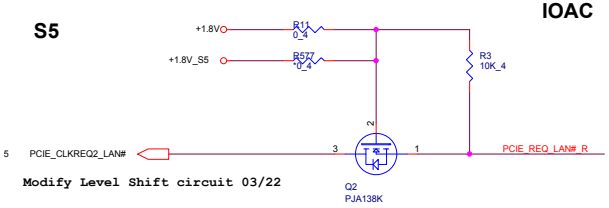


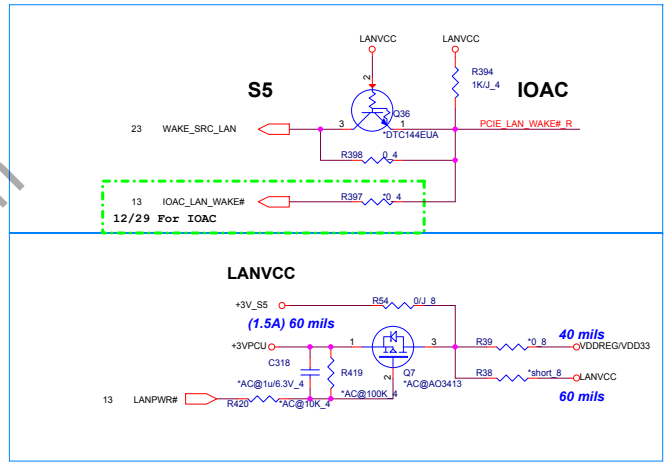
Quanta Computer Inc.
PROJECT : ZHP/ZSP

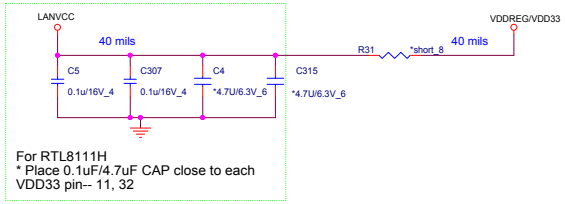
Size	Document Number	Rev
	Codec ALC225	1A
Date: Tuesday, July 26, 2016	Sheet 19 of 36	

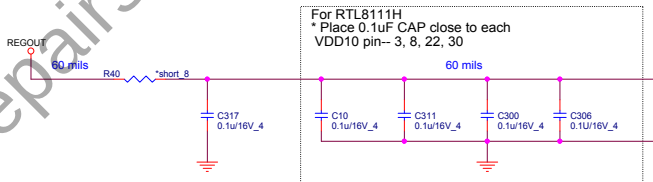
LAN

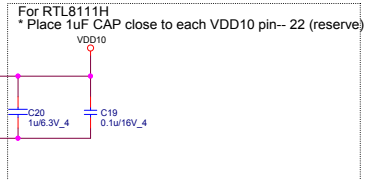




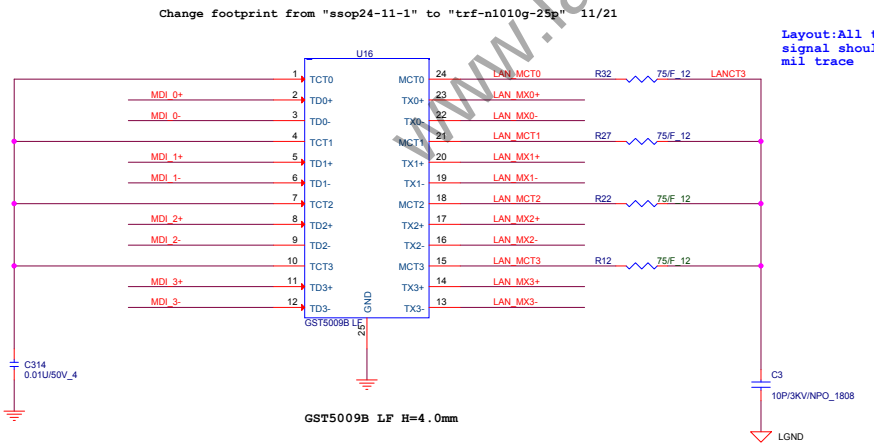






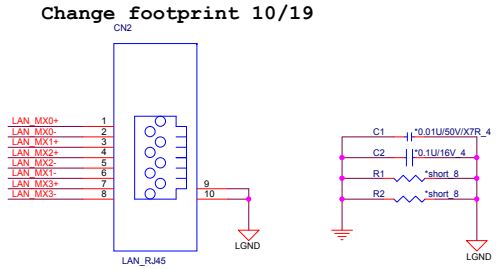


Tramsformer



Layout:All termination signal should have 30 mil trace

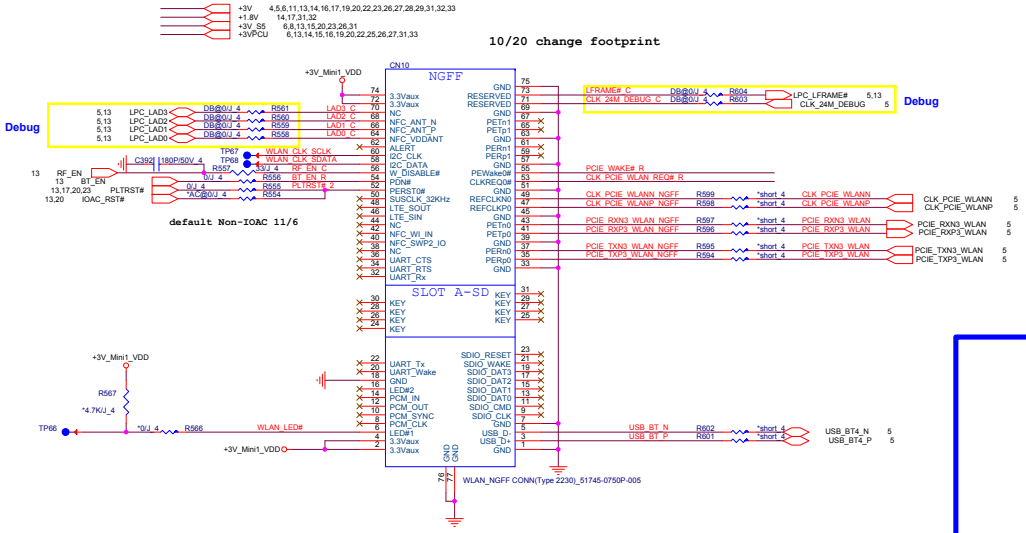
RJ45 Connector

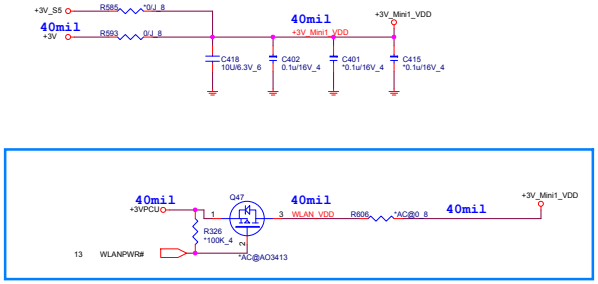


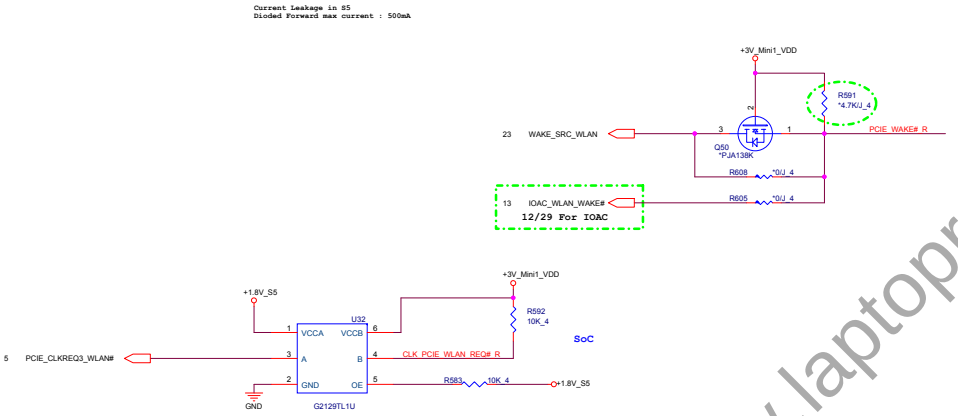
Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	LAN	1A
Date: Tuesday, July 26, 2016	Sheet 20 of 36	

WLAN



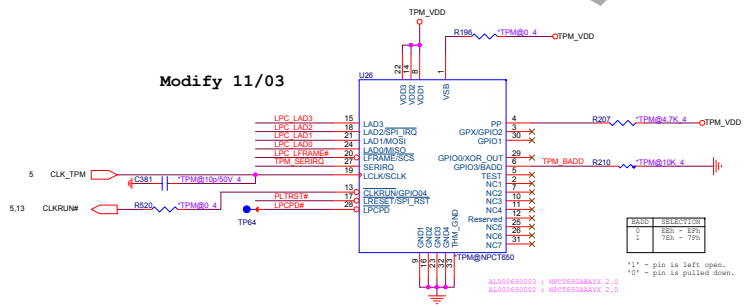


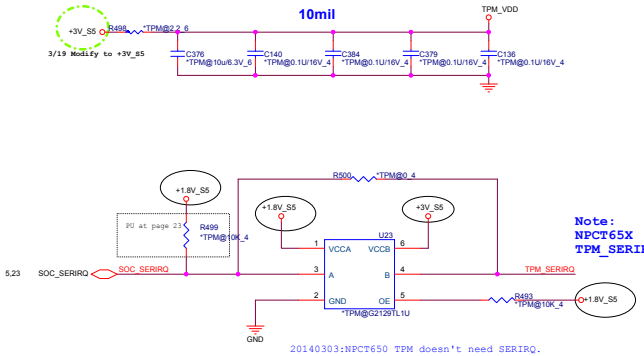


MINI PCI-E

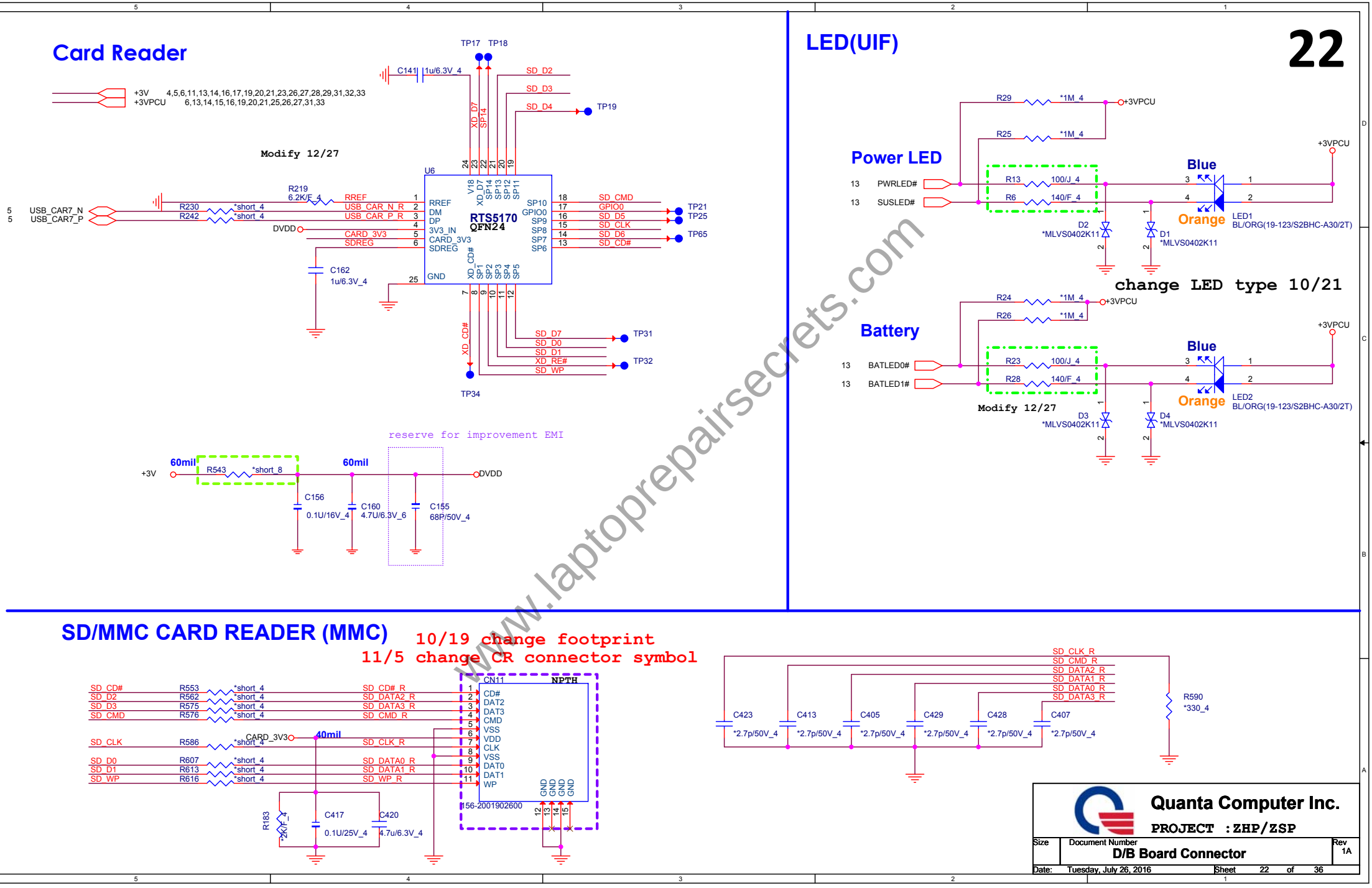
TPM (TPM)

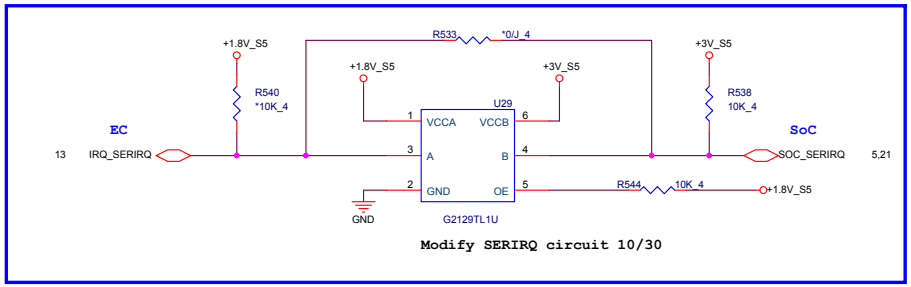
change to QFN type AL000650003
11/03 modify the symbol



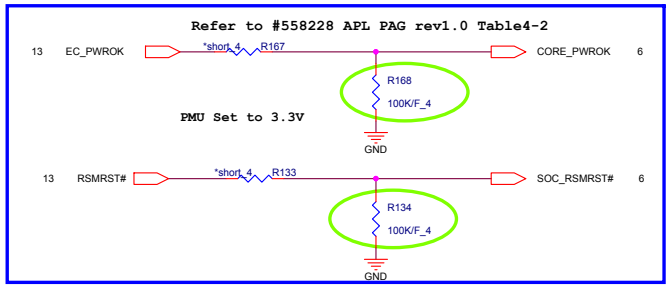


Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: WiFi & BT & TPM | Rev: 1A
Date: Tuesday, July 26, 2016 | Sheet 21 of 36


Card Reader
LED(UIF)
22
SD/MMC CARD READER (MMC)
10/19 change footprint
11/5 change CR connector symbol
Modify 12/27
RTS5170
QFN24
reserve for improvement EMI
Power LED
Battery
Blue
Orange
change LED type 10/21
Modify 12/27
Quanta Computer Inc.
PROJECT : ZHP/ZSP
D/B Board Connector
Tuesday, July 26, 2016
www.laptoprepairsecrets.com

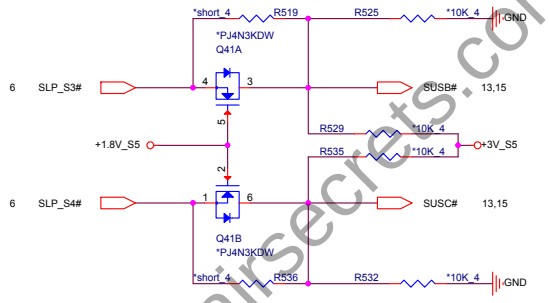


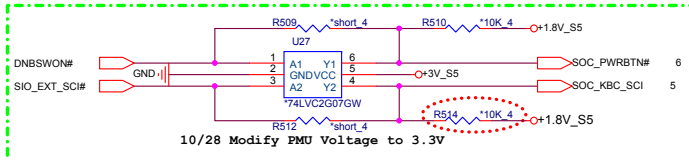
Modify SERIRQ circuit 10/30



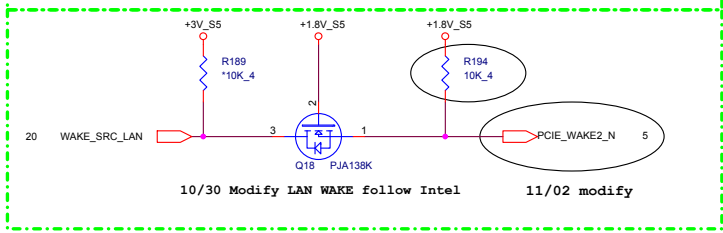
+3V_S5 6,8,13,15,20,21,26,31
+3V 4,5,6,11,13,14,16,17,19,20,21,22,26,27,28,29,31,32,33
+1.8V_S5 4,5,6,8,10,13,14,15,21,25,29,31

Del PCH_SUS_STAT# level shift to EC 10/28

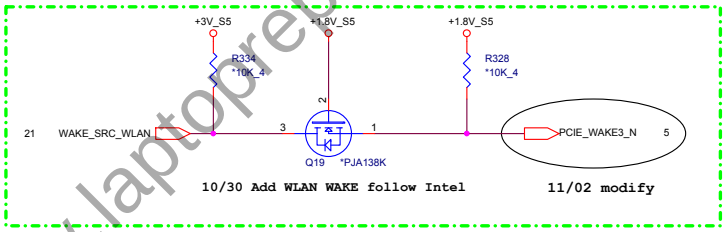




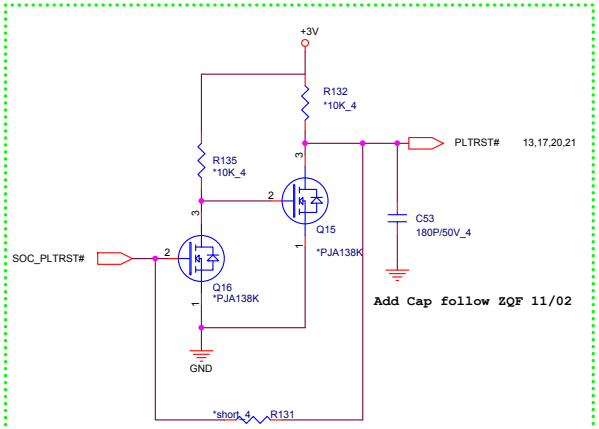
10/28 Modify PMU Voltage to 3.3V



10/30 Modify LAN WAKE follow Intel 11/02 modify



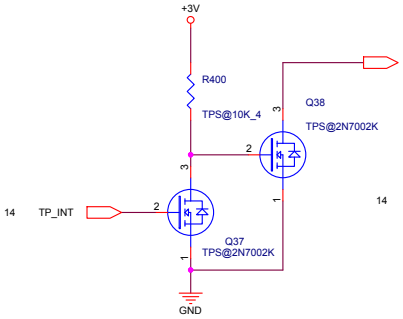
10/30 Add WLAN WAKE follow Intel 11/02 modify



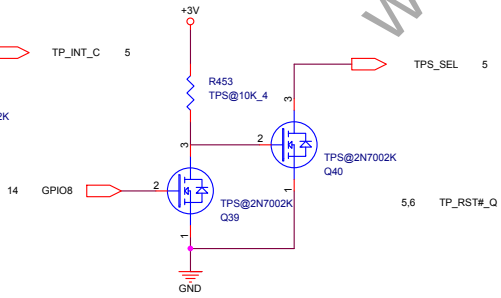
10/28 Modify PMU Voltage to 3.3V

Touch screen INT

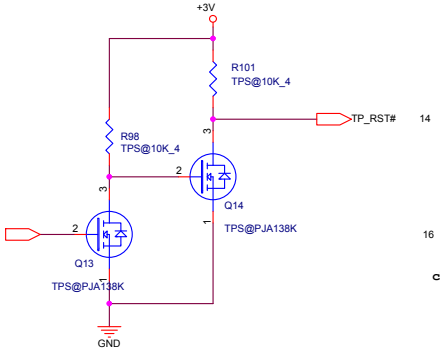
Touch Panel interrupt



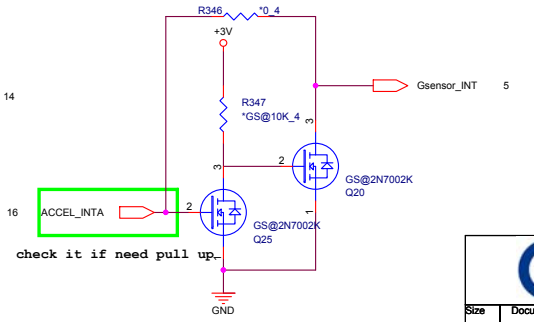
Touch screen detected



Touch screen reset



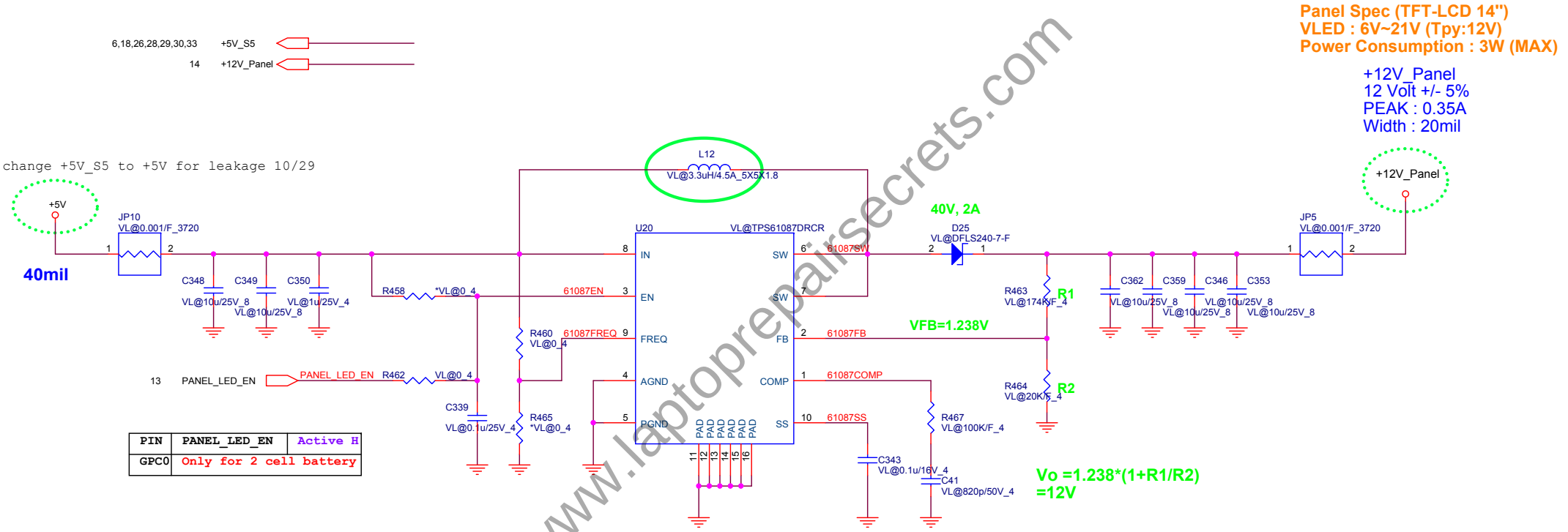
G Sensor INT



check it if need pull up.

Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Level Shift	1A
Date: Tuesday, July 26, 2016	Sheet 23 of 36	



PIN	PANEL_LED_EN	Active H
GPC0	Only for 2 cell battery	

Quanta Computer Inc.

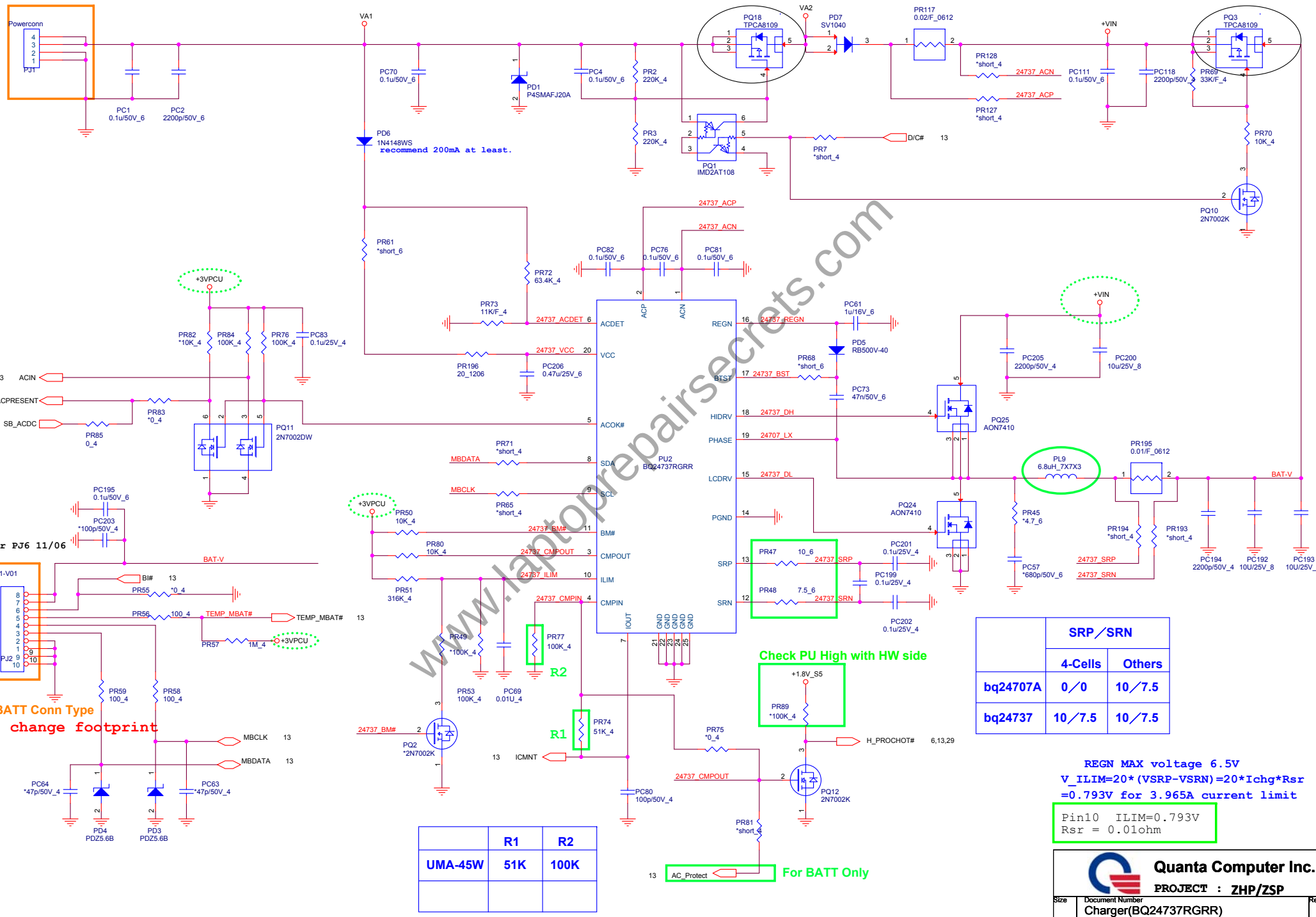
PROJECT :

Size	Document Number	Rev
	DC-DC	1A

Date: Tuesday, July 26, 2016 Sheet 24 of 36

Change ADP-IN Pin define 2016/01/11 by SMT Request.

PQ27 / PQ8 change from BAM14130000 (MOS AOL1413) to BAM81090000 (MOS TPCA8109) 11/06



	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

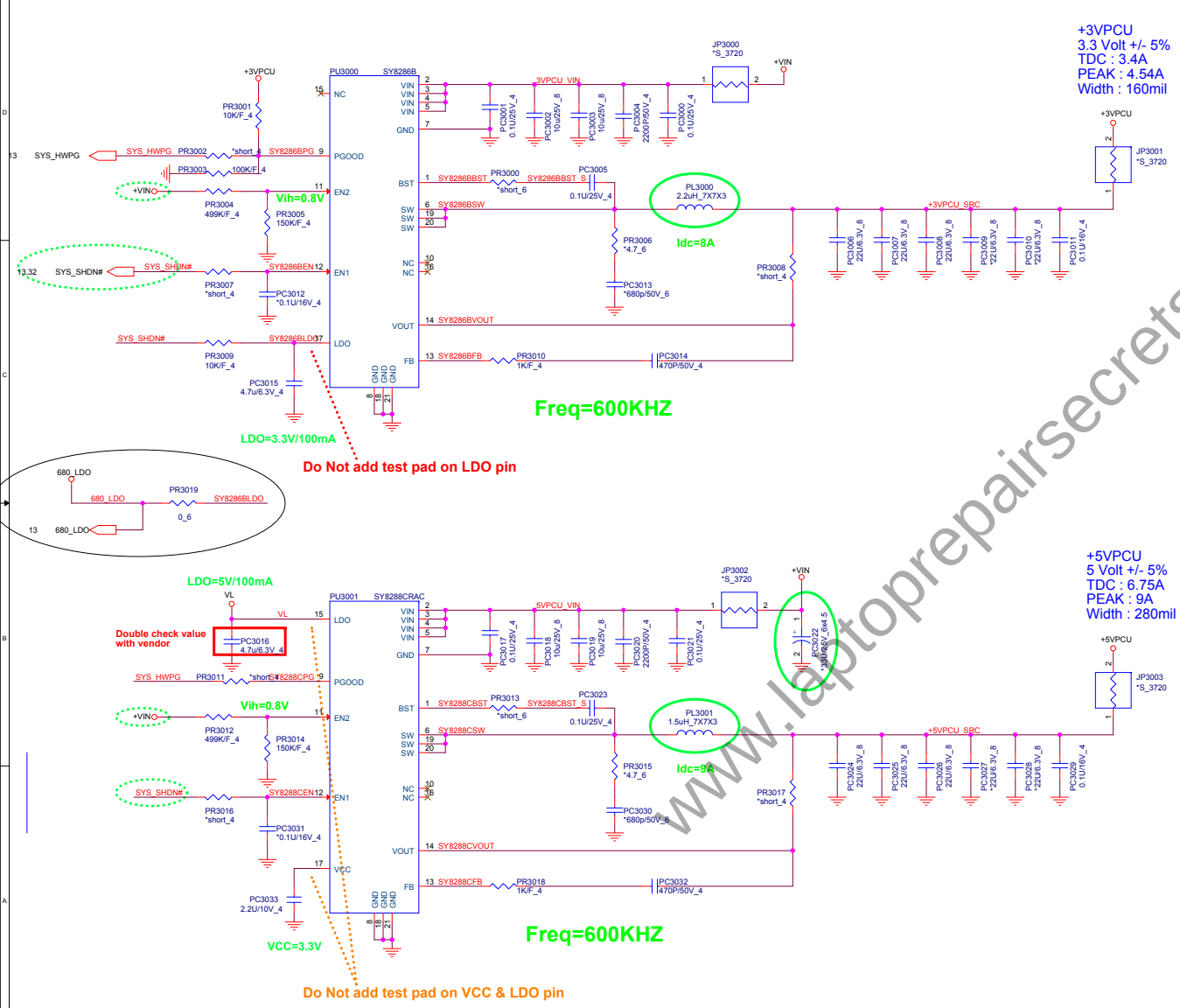
	R1	R2
UMA-45W	51K	100K

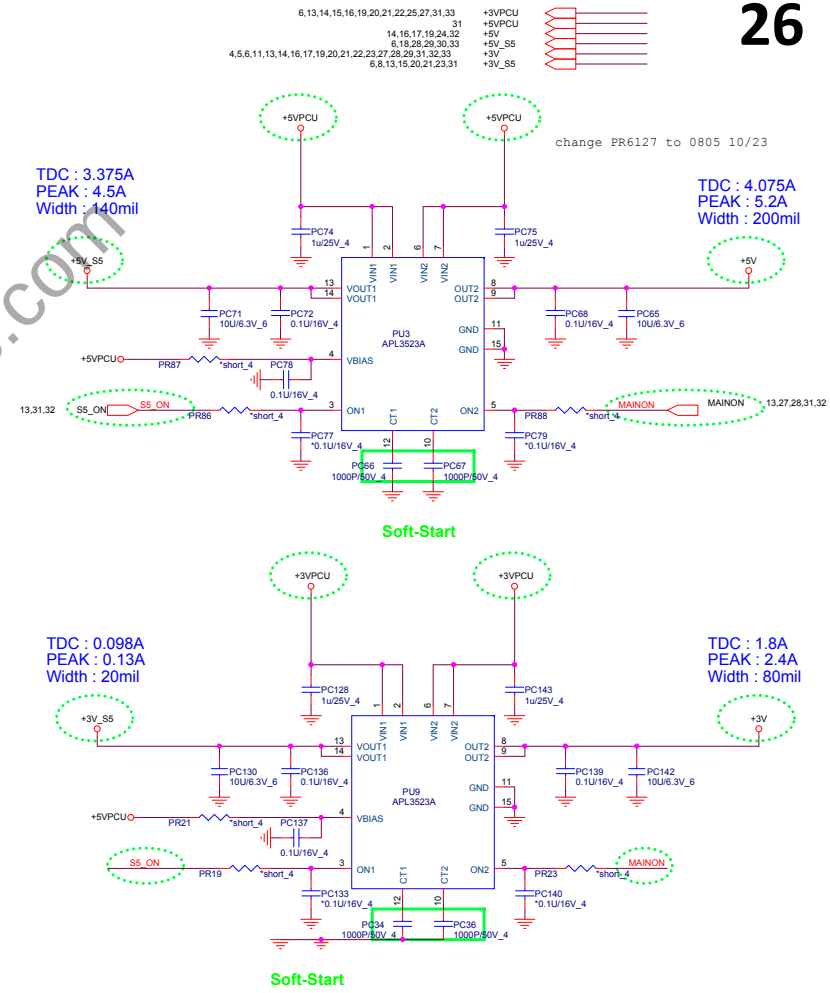
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Charger(BQ24737RGRR)	2A
Date: Tuesday, July 26, 2016	Sheet 25 of 36	





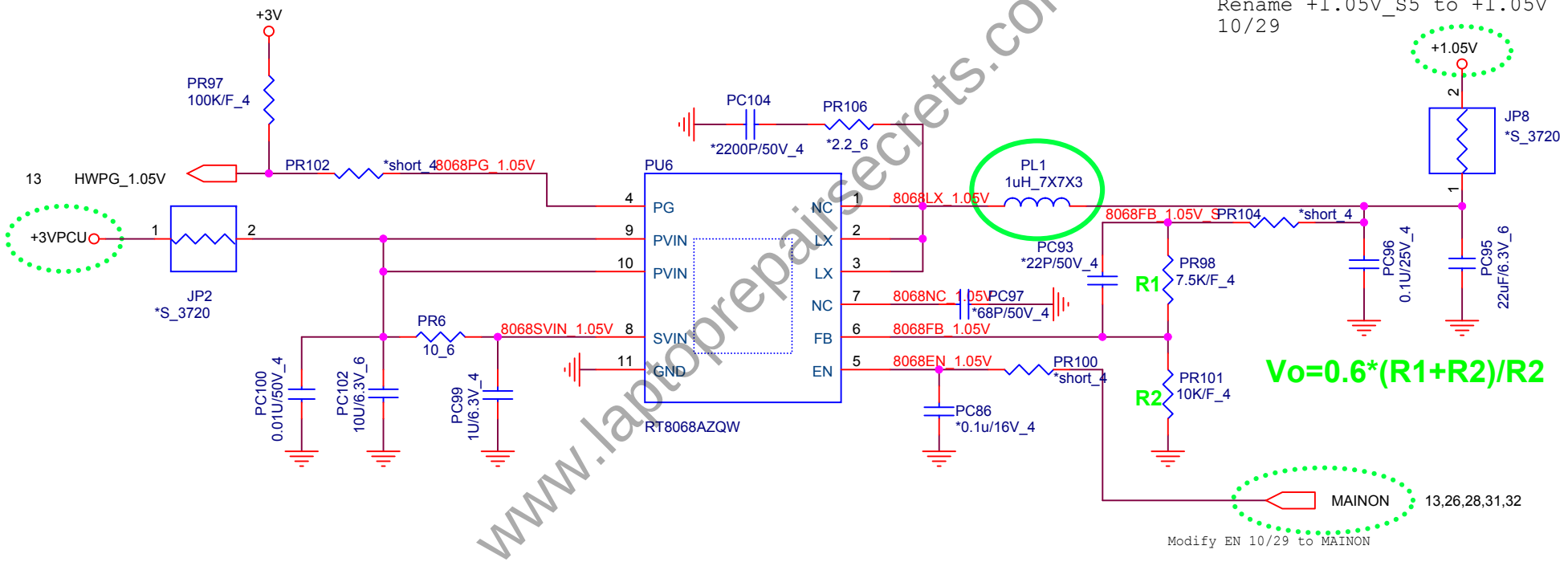
Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	SYSTEM 5V/3V (NB680 & NB679)	1A

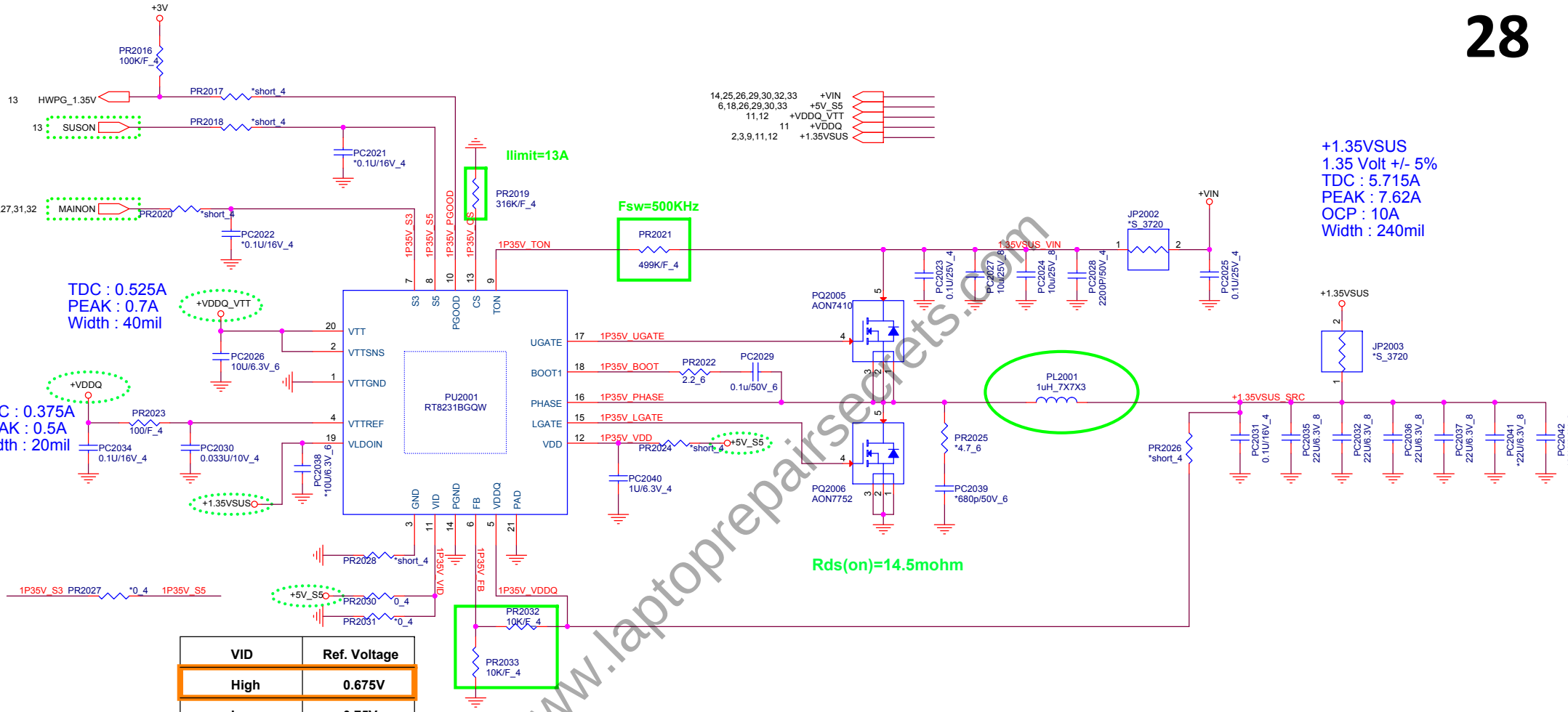
Date: Tuesday, July 26, 2016 Sheet 26 of 36

+1.05V_S5
1.05Volt +/- 5%
TDC : 2.025A
PEAK : 2.7A
Width : 100mil

Rename +1.05V_S5 to +1.05V
10/29



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: +1.05V_S5 (RT8068AZQW)	Rev: 2A
Date: Tuesday, July 26, 2016	Sheet 27 of 36	



VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=10A
L ripple current
=(19-1.35)*1.35/(1u*500k*19)
=2.508A
Vtrip=10-(2.508/2)*14.5mohm
=126.817mV
Rlimit=126.817mV/5uA*10=253.63Kohm

DDR=1.35V
PR2032=10K/F_4
PR2033=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

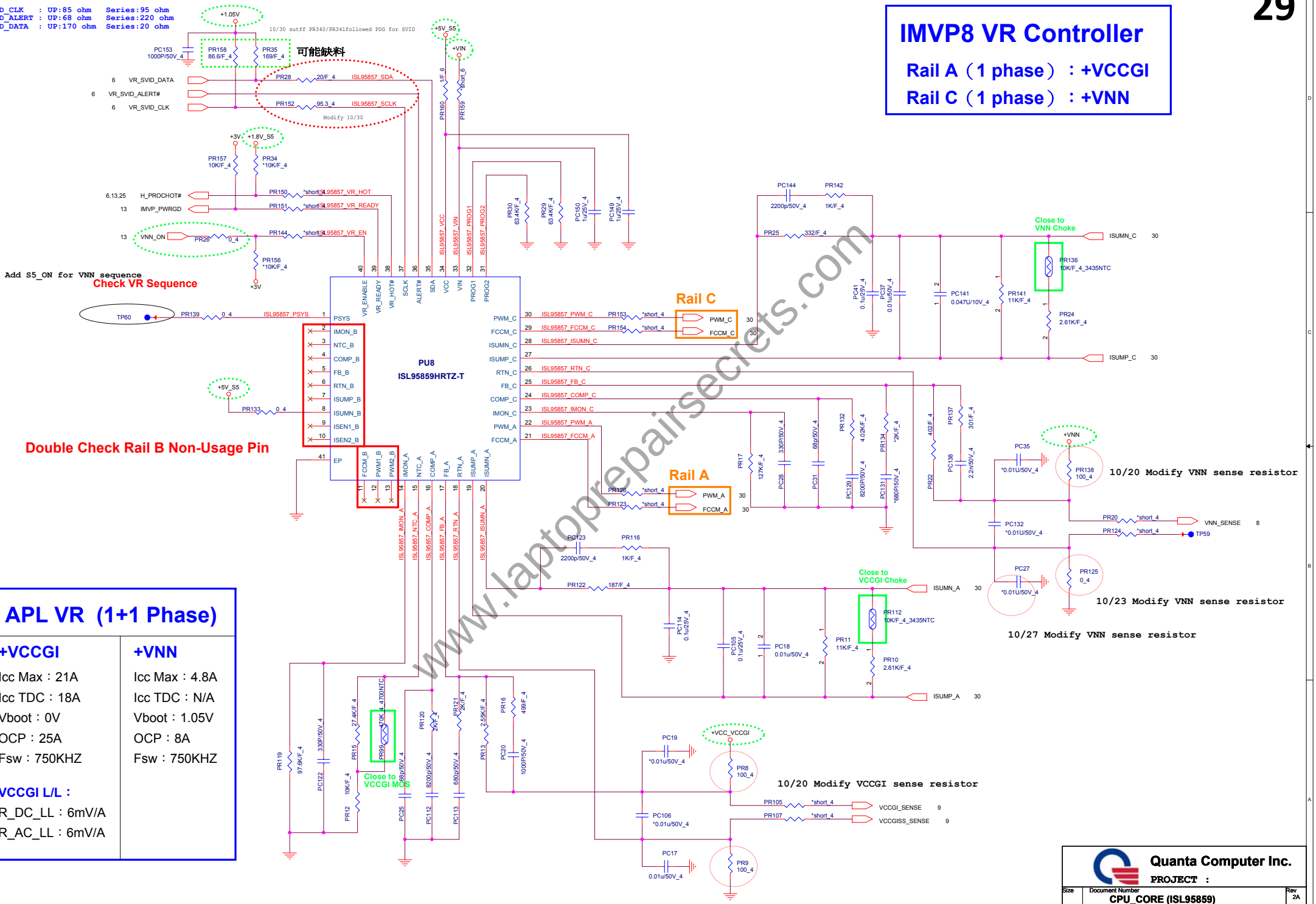
Quanta Computer Inc.
PROJECT :
Size | Document Number: DDR3L (RT8231BGQW) | Rev: 1A
Date: Tuesday, July 26, 2016 | Sheet 28 of 36

Change pull up to +1.05V_S5

SVID_CLK : UP:85 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:170 ohm Series:20 ohm

IMVP8 VR Controller

Rail A（1 phase）：+VCCGI
Rail C（1 phase）：+VNN



APL VR (1+1 Phase)

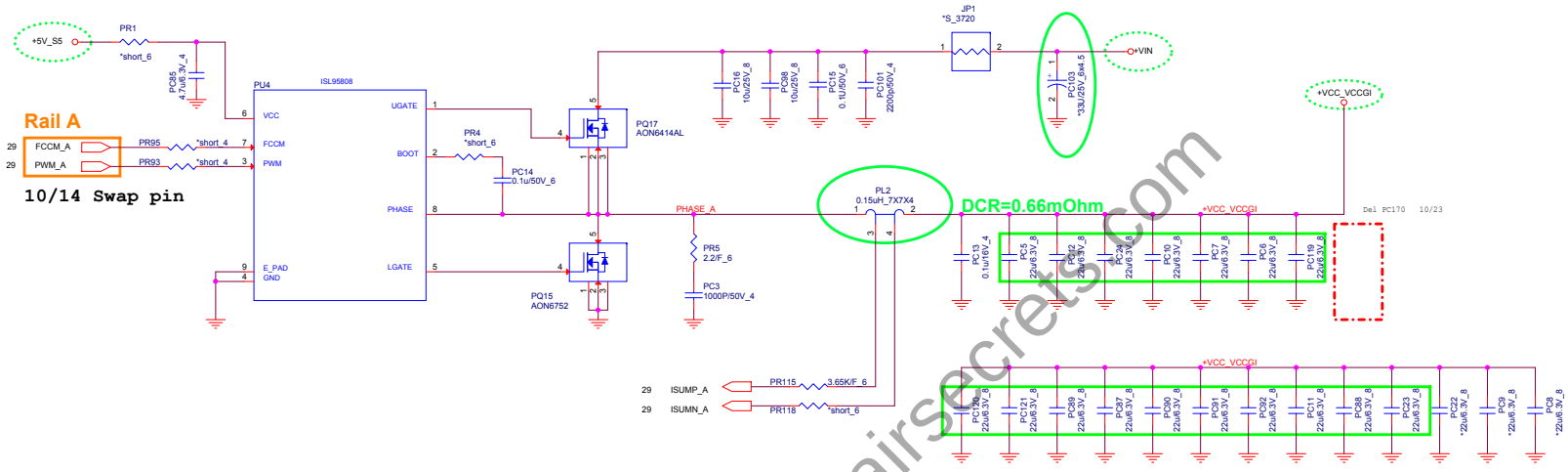
+VCCGI	+VNN
Icc Max：21A	Icc Max：4.8A
Icc TDC：18A	Icc TDC：N/A
Vboot：0V	Vboot：1.05V
OCP：25A	OCP：8A
Fsw：750KHZ	Fsw：750KHZ

VCCGI L/L：
R_DC_LL：6mV/A
R_AC_LL：6mV/A

Quanta Computer Inc.
PROJECT :
Size | Document Number: CPU_CORE (ISL95859) | Rev 2A
Date: Tuesday, July 26, 2016 | Sheet 29 of 36

14,25,26,28,29,32,33 +VIN
8,29 +VCC_VCCGI
8,9,29 +VNN
6,18,26,28,29,33 +5V_S5

VCCGI



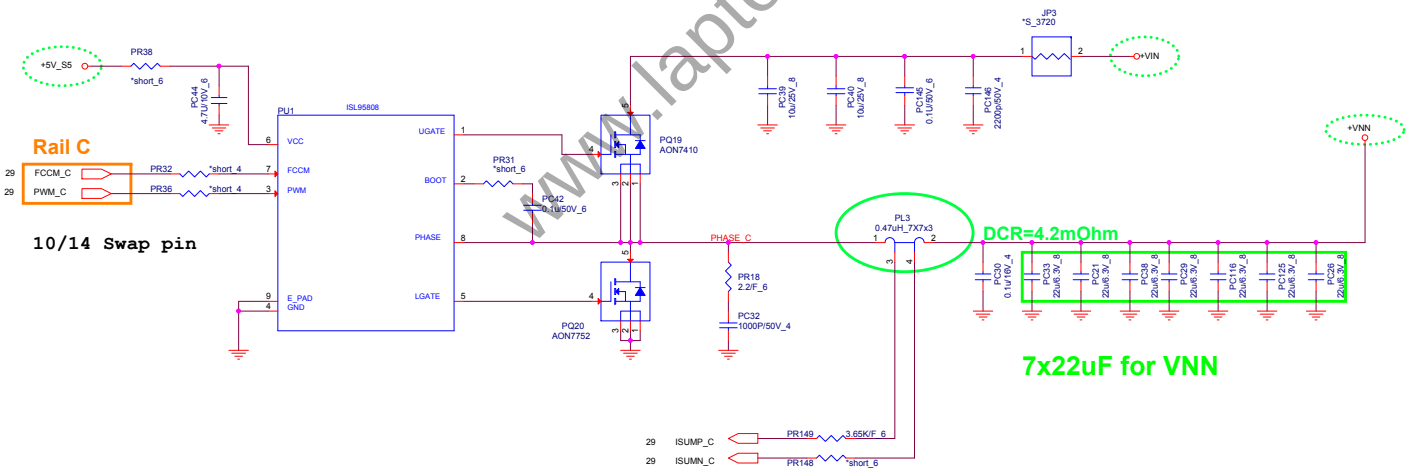
+VCCGI

Icc Max：21A
Icc TDC：18A
Vboot：0V
OCP：25A
Fsw：750KHZ

VCCGI L/L :

R_DC_LL：6mV/A
R_AC_LL：6mV/A

VNN

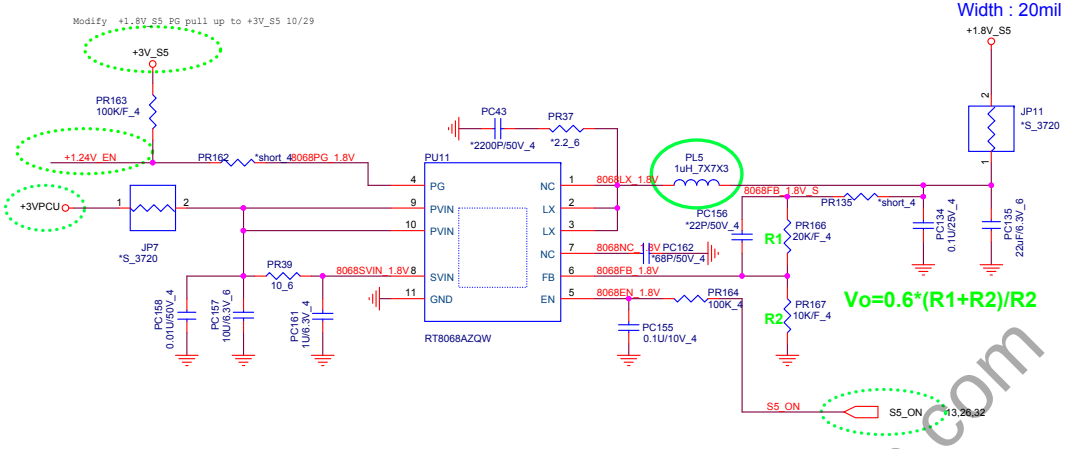


+VNN

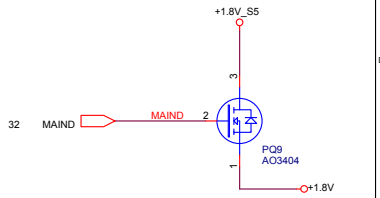
Icc Max：4.8A
Icc TDC：N/A
Vboot：1.05V
OCP：8A
Fsw：750KHZ

Quanta Computer Inc.
PROJECT :
Size | Document Number +VCCGI / +VNN (ISL95859) | Rev 2A
Date: Tuesday, July 26, 2016 | Sheet 30 of 36

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

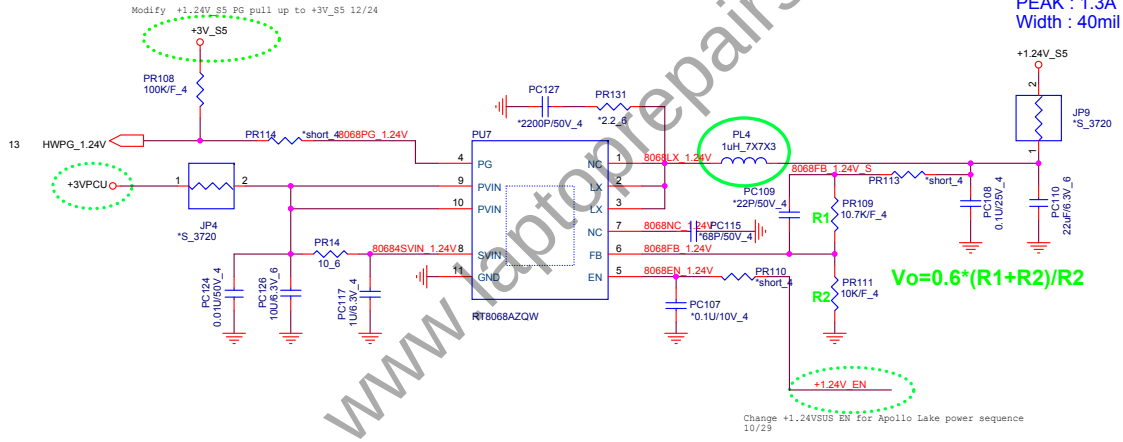


Vo=0.6*(R1+R2)/R2



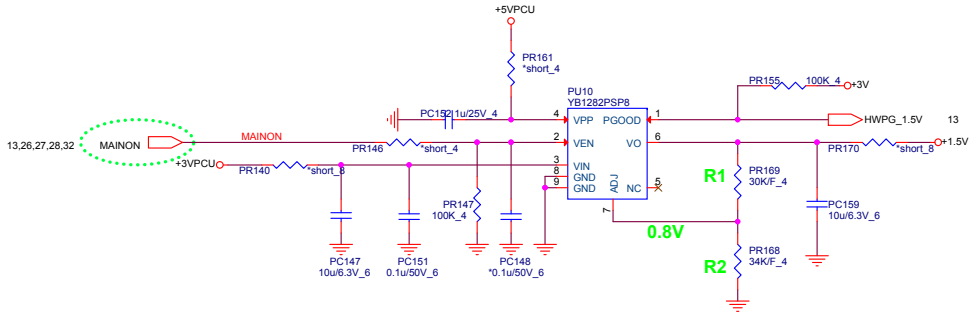
TDC : 0.015A
PEAK : 0.02A
Width : 20mil

+1.24V_S5
1.24Volt +/- 5%
TDC : 0.975A
PEAK : 1.3A
Width : 40mil



Vo=0.6*(R1+R2)/R2

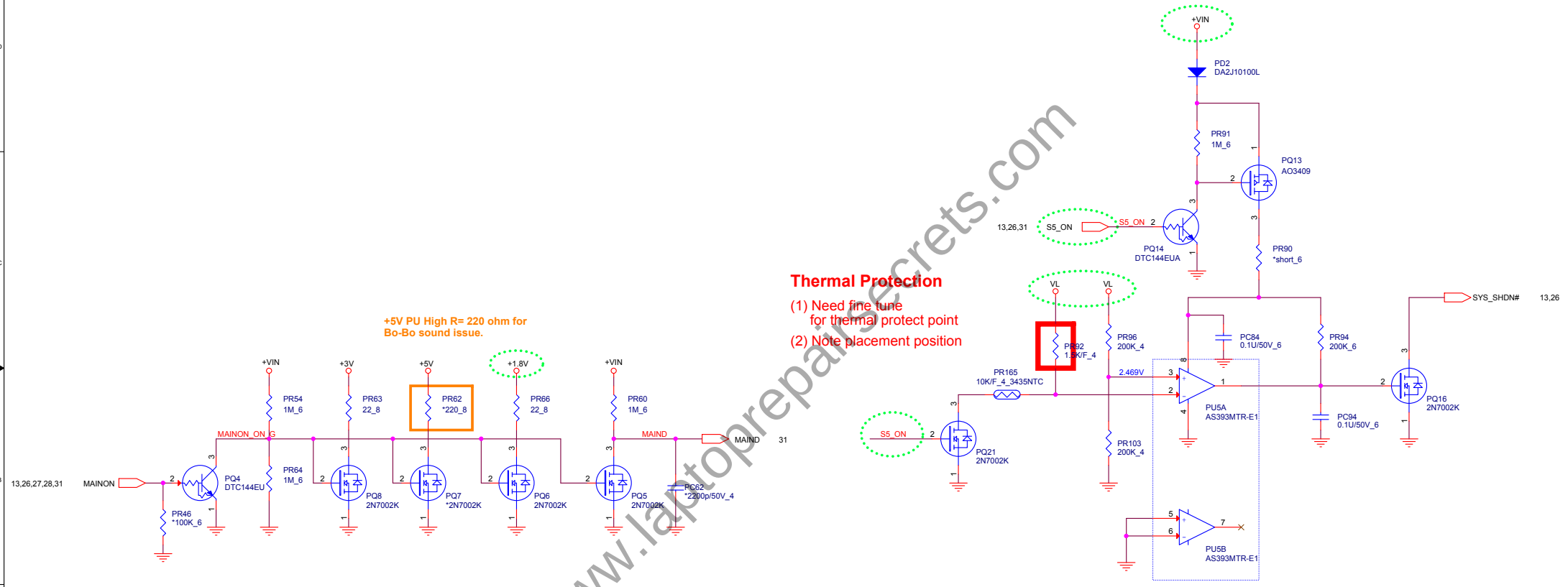
+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil



Vo =0.8(1+R1/R2)
=1.506V

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	+1.8V_S5 / +1.24VSUS / +1.5V	2A
Date: Tuesday, July 26, 2016	Sheet 31 of 36	



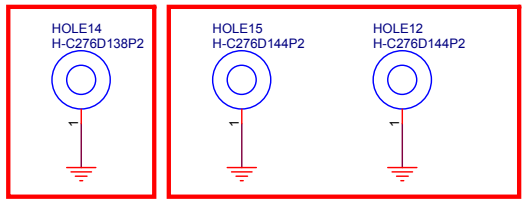
Quanta Computer Inc.
PROJECT :

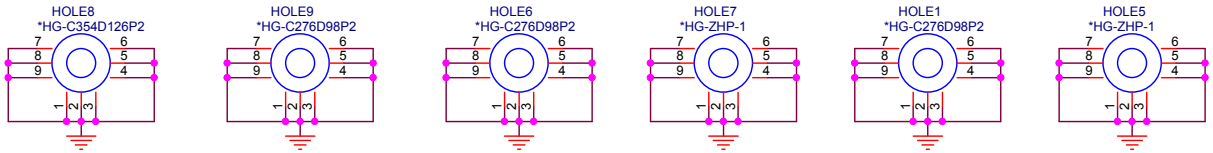
Size	Document Number	Rev
	Thermal / Discharge	1A

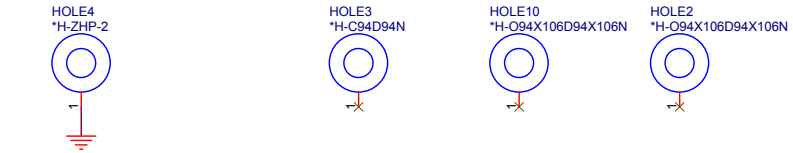
Date: Tuesday, July 26, 2016 Sheet 32 of 36

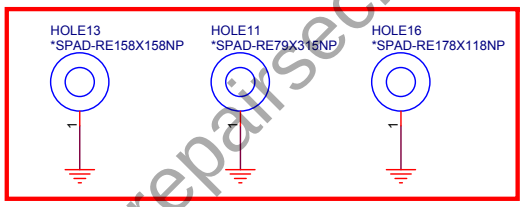
HOLE(OTH)

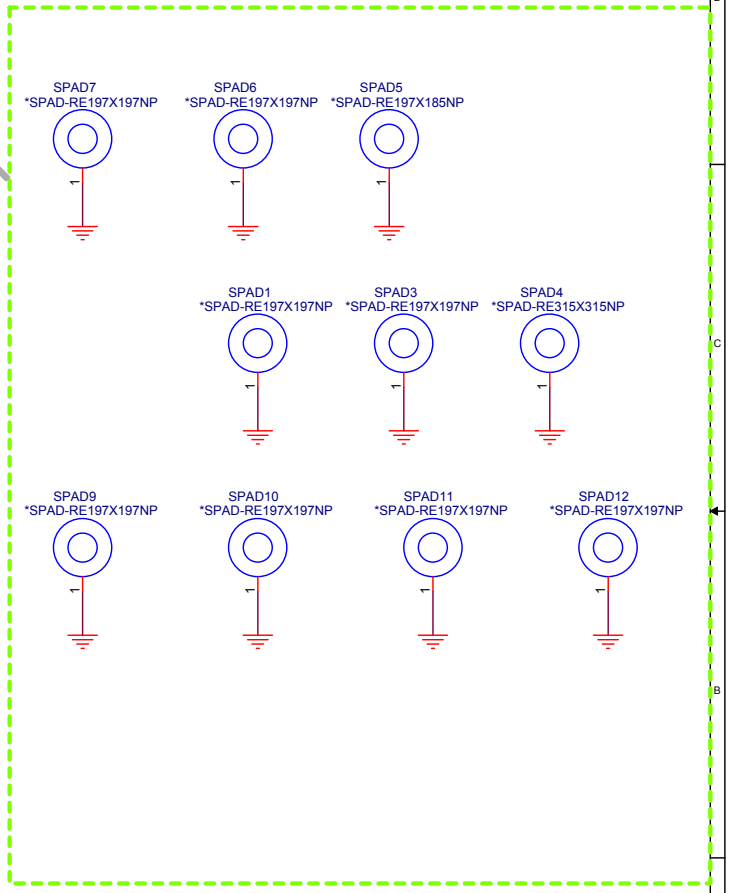
Need to check the nuts 10/27

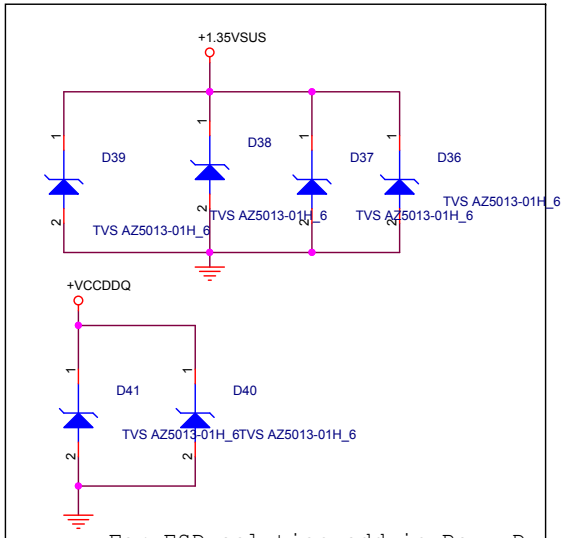


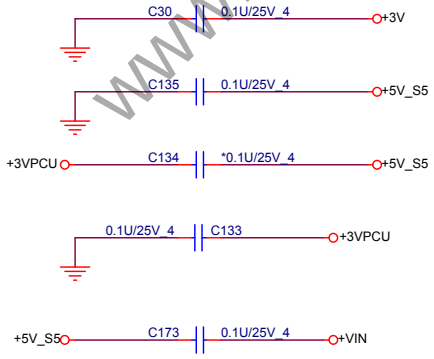


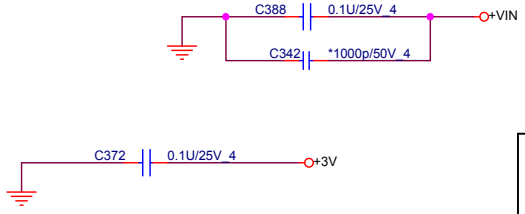










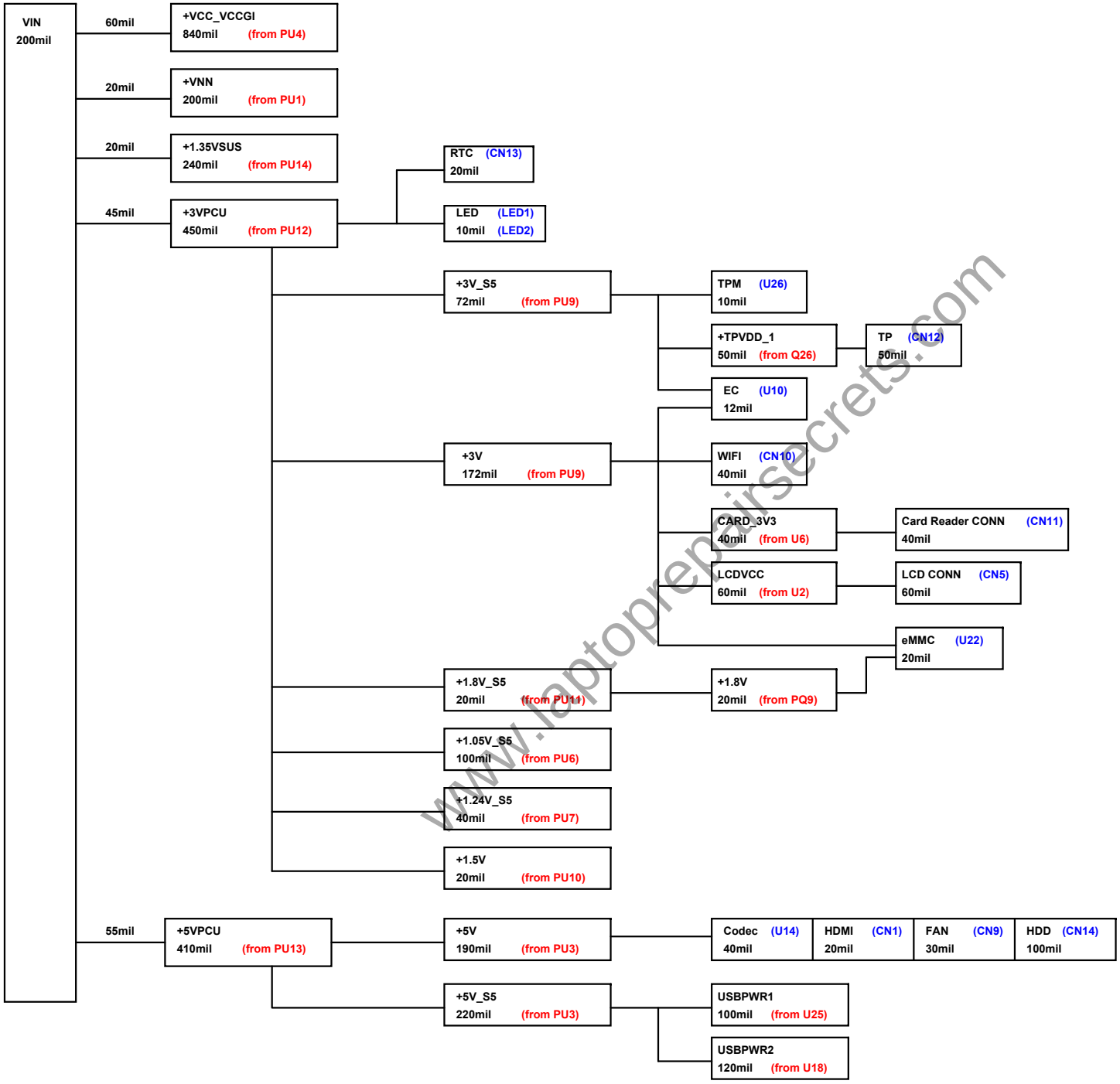


Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	USB BOARD CONN	1A
Date: Tuesday, July 26, 2016	Sheet 33 of 36	

Apollo Power Tree



Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: Power Sequence | Rev: 1A
Date: Tuesday, July 26, 2016 | Sheet 34 of 36

Model	REV	CHANGE LIST	ZHP/ZSP MB

Page	From	To
1		3A
2		3A
3		3A
4		3A
5		3A
6		3A
7		3A
8		3A
9		3A
10		3A
11		3A
12		3A
13		3A
14		3A
15		3A
16		3A
17		3A
18		3A
19		3A
20		3A
21		3A
22		3A
23		3A
24		3A
25		3A
26		3A
27		3A
28		3A
29		3A
30		3A
31		3A
32		3A
33		3A
34		3A
35		3A
36		3A
37		3A
38		3A
39		3A

ZHP/ZSP MB — **REV.A**

1 2015/11/10 REV:A Initial release

1 2015/11/12 R64 (68ohm) change EOD part CS06802FB07 to CS06802JB17
2 2015/11/12 PR152 Change CS09532FB08 to CS09532FB00
3 2015/11/12 Stuff R483
4 2015/11/12 R220 modify value *CHB@80.6/F_4
5 2015/11/12 R266, R274, C171, R267, C170, R272 modify value CHB@
6 2015/11/12 U2 change EOL part AL005243001 to AL005245000
7 2015/11/12 Page 6 add text "Pin AG55 is EMMC_PWR_EN_N (CRB 1.0)"
8 2015/11/12 Correct the value and description of R13, R23
9 2015/11/12 Correct the value and description of R6, R28

1 2015/11/13 R142 change CS11372FB09 to CS11372FB25
2 2015/11/13 PR22 change CS14022FB03 to CS14022FB11
3 2015/11/13 PC18, PC181 change EOD part CH31004KB17 to CH31006KB18
4 2015/11/13 PC96, PC108, PC134, PC182, C138 change EOD part CH41002KB93 to CH4104K1B00
5 2015/11/13 C408, C409, C421, C422 change EOD part CH4102K1B03 to CH4104K1B00
6 2015/11/13 PC152 change EOD part CH5103K9901 to CH5103K1900
7 2015/11/13 PR186 change EOD part CS-2003J932 to CS-2003F900
8 2015/11/13 C112, C118, C157, C158, C163, C164, C165, C166 change EOD part CH6221M9A07 to CH6221M9A01

REV.B

1 2015/12/07 Remove PR27, Add R617 220 ohm for A Can't Power on issue.
2. 2015/12/07 Remove R280/R288/R279/R287/R266/R274/R267/R272/C170/C171/C180/C179/R220, ADD R226 And R251 for memory Down can't work issue.
3. 2015/12/07 remove R75 for can't power on.
4. 2015/12/07 change SW2 to PN: DHPDSA40E00 and Footprint
5. 2015/12/17 change U4 and U33 to Dual 2N7002K for RDC request.
6. 2015/12/17 change C377 from 3528 to 1206 and C27 from 0805 10U to 0603 10U.
7. 2015/12/17 add U21 Pin L30 EMMC Rest to U22
8. 2015/12/25 Change CN13 to support ML1220 for PE Request.
9. 2015/12/25 Change P28 DDR3L Power solution
9. 2016/01/11 Resever 2K for SD-Card VCC
10. 2016/01/11 Change PJ1 ADP-IN Pin define 2016/01/11 by SMT Request.
11. 2016/01/12 R514 remove in B test , for AC/DC change icon issue, Add D35 for Hall IC ESD part by EC side.
12. 2016/01/25 remove R472/C352/C347/C351 int function no need use.
13. 2016/01/25 add EC Pin

REV.C

1.Change Q56 to DMN53D0LDW (Vgs=1.5V)
2.Change Q2 folllow ZRV 雙向.
3.Change PR73 from 10K to 11K by power team request
4.Change PR164 from 63.4K to 100K for power sequence fine tune and PR110 from 4.7K to 0 ohm
5.Add R573 and net "THERMTRIP#" and to conect EC pin4
6.Add R579 and R581 10K PU for PDG 1.2 Request.
7. Remove R136 and R137 , Mount R145 for PDG 1.2 Request.
8. Modify HDMI Q34 to 1.BAM6N430000 for HDMI issue and Remove R34/R33/R380 /R100
9. G_Sensor issue remove R346
10. Core Power OK R171 change from 20K to 100K, R488 change from 2.7K to 10K.
11. CHange C76 and C78 to 15P for RTC clock issue.

REV.D

1.Add R589 for Acer ESD lesson.

REV.E

1.Change R164 from 100K to 2.2K and R138 from 4.7K to 0 ohm for BIOS SOC_Override functiion.
2.Remove R201 and R201 (HDA SDI I/O pin issue) for QS sample .
3.Follow check list V1.5 to change R171 from 100K to 20K
4.Change Q12/Q33 type to PJA138K (Vgs<=1.5V)
5. Unstuff SW1,C391,R548

```
0402: R578,R580,R582,R584,R322,R150,R387,R55,R50,R51,R418,R159,R304,R376,R144,R126,R125,R123,R534,
      R255,R248,R545,R229,R249,R236,R80,R81,R444,R445,R365,R228,R320,R262,R316,R310,R254,R265,
      R352,R358,R350  R601,R602,R594,R595,R596,R597,R598,R599,R242,R230,R553,R562,R575,R576,R586,
      R607,R613,R616,R509,R512,R131,
      R536,R519,R133,R167,R163,PR71,PR65,PR128,PR127,PR194,PR193,PR81,PR7,PR3002,PR3007,PR3011,
     PR3016,PR3017,PR3008,PR87,PR86,PR88,PR21,PR19,PR23,PR102,PR100,PR104,PR2017,PR2018,PR2020,
        PR2028,PR2024,PR2026,PR150,PR151,PR144,PR26,PR126,PR123,PR105,PR107,PR20,PR124,PR153,
    PR154,PR95,PR93,PR32,PR36,PR162,PR114,PR146,PR161,PR110,PR113,PR135,R224,R193/R190/R403
    /R436/R437/R258/R252/R253/R273/R53/R59/L5/L3

0603: R208,R206,R481,R474,R478,R116,R105,R117,R118,R119,R545,L6,PR68,PR61,PR3013,PR3000,
      PR159,PR4,PR31,PR1,PR38,PR118,PR148,PR90,R339


0805: R361,R174,R485,R480,R52,R468,R374,R373,R372,R371,R40,R38,R1,R2,R31,R543,PR130,PR143,PR129,
      PR145,PR67,PR52,PR78,PR79,PR170,PR140

1206:R257,R256,

3720:  JP3000,JP3001,JP3002,JP3003,JP2,JP8,JP2002,JP2003,JP1,JP3,JP11,JP9,JP4
```


Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number: Change List-1 | Rev 1A
Date: Tuesday, July 26, 2016 | Sheet 35 of 38

Model	REV	CHANGE LIST	ZHP/ZSP MB
ZHP/ZSP MB			

Page	From	To
1		3A
2		3A
3		3A
4		3A
5		3A
6		3A
7		3A
8		3A
9		3A
10		3A
11		3A
12		3A
13		3A
14		3A
15		3A
16		3A
17		3A
18		3A
19		3A
20		3A
21		3A
22		3A
23		3A
24		3A
25		3A
26		3A
27		3A
28		3A
29		3A
30		3A
31		3A
32		3A
33		3A
34		3A
35		3A
36		3A
37		3A
38		3A
39		3A

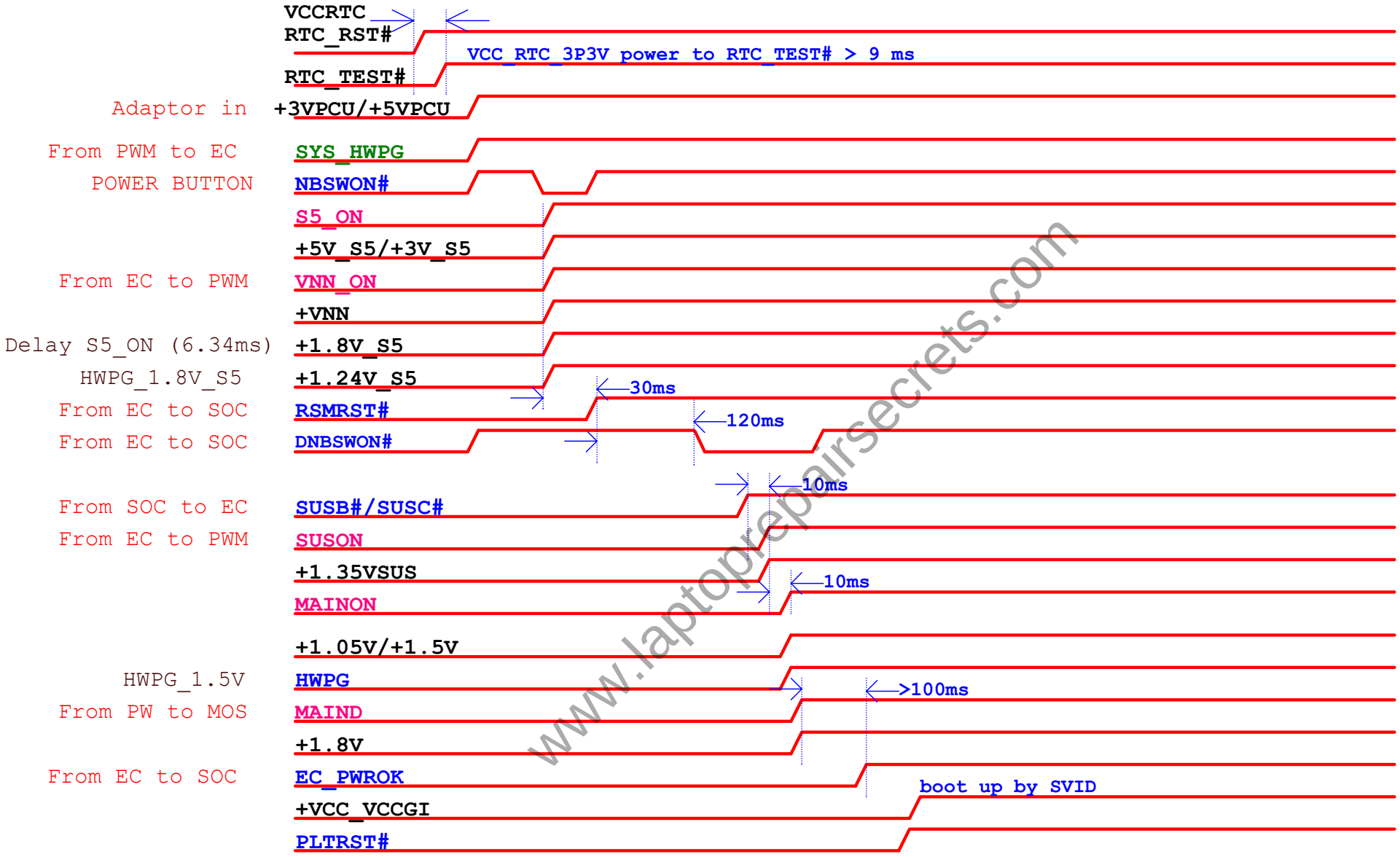
Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Change List-2	1A

Date: Tuesday, July 26, 2016 Sheet 36 of 36

Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF



Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Power Sequence	1A

Date: Tuesday, July 26, 2016 Sheet 38 of 38