MODEL NAME : DDR51(15")/DDR71(17")
PROJECT CODE : ANRDDR5100/ANRDDR7100
PCB NO :
DAC0000E000 : LA-F551P M/B NV G1G2
DAC0000F000 : LA-F552P M/B NV G3
DAB0002I000 : LA-F553P M/B AMD
DA4002AV000 : LS-D751P LOGO_15/B
DA80017I000 : LS-D752P LOGO_17/B
DA4002B000S : LS-D753P PWR_15/B
DA4002AW000 : LS-D754P PWR_17/B
DA80017J000 : LS-D755P IO_12L/B
DA4002ND000 : LS-F551P TRON_LCD_15/B
DA4002NE000 : LS-F552P TRON_REAR_15/B
DA80017K000 : LS-D759P IO_14L/B
DA4002NG000 : LS-F554P TRON_LCD_17/B
DA4002NH000 : LS-F555P TRON_REAR_17/B
DA4002NF000 : LS-F553P TRON_FRONT_15/B
DA4002NI000 : LS-F556P TRON_FRONT_17/B
DA30000W300 : LF-D751P Head_15/B
DA30000W400 : LF-D752P Head_17/B
DA30000W401 : LF-D752P Head_17/B(For LOGO_15/B)
DA300013900 : LF-F551 TRON_15/B
DA300013E00 : LF-F552 TRON_17/B

DDR51
Coffee Lake-H 45W
CNL PCH-H with nVIDIA N17E

REV : 1.0 (A00)
2018.02.06

@ : Nopop Component
EMI@,ESD@,RF@ : EMI/ESD/RF part
CONN@ : Connector Component
@EMI@,@ESD@,@RF@ : Total debug Component

ZZZ PCB@

PCB 26S LA-F552P REV0 M/B NV G3 16

DAC0000F000

ZZZ PCBR1@

PCB 26S LA-F552P REV1 M/B NV G3 16

DAC0000F010

ZZZ PCBR3@

PCB 26S LA-F552P REV1 MB NV TRIP 16 A31!

DAC0000F011

ZZZ DAZR1@

PCB DDR51 LA-F552P LS-D751P-52P/D754P 02

DAZ26S00200

ZZZ DAZR3@

PCB DDR51 LA-F552P LS-D751 02 TRIP A31 !

DAZ26S00201

HDMI@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000003HM	HDMI W/Logo:RO0000003HM

Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1450-06

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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Title: Cover Page

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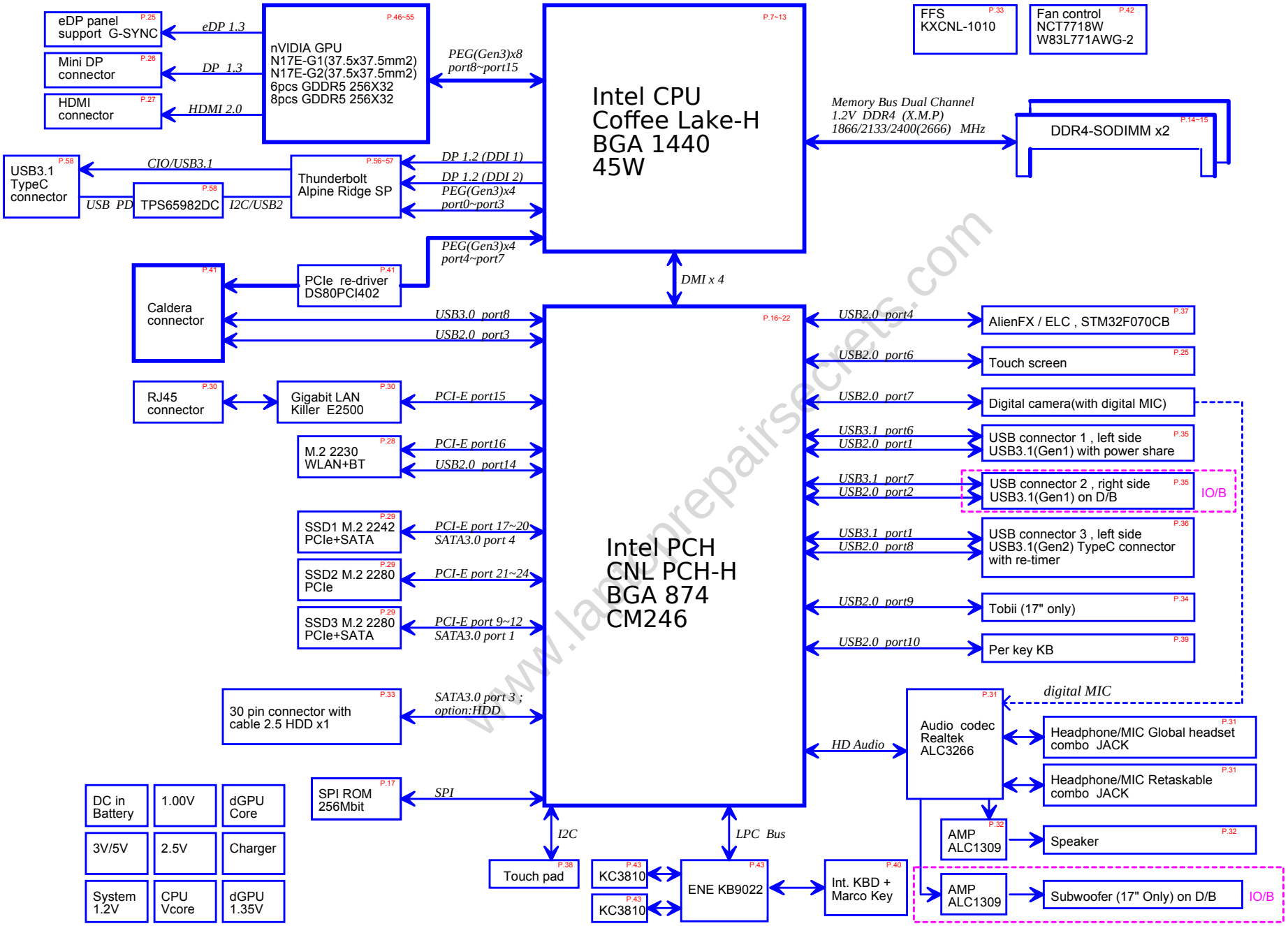
Date: Wednesday, February 21, 2018 | Sheet 1 of 82

Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.	
Title	Block Diagram
Size	Document Number: LA-F551P
Rev	0.3
Date:	Wednesday, February 07, 2018
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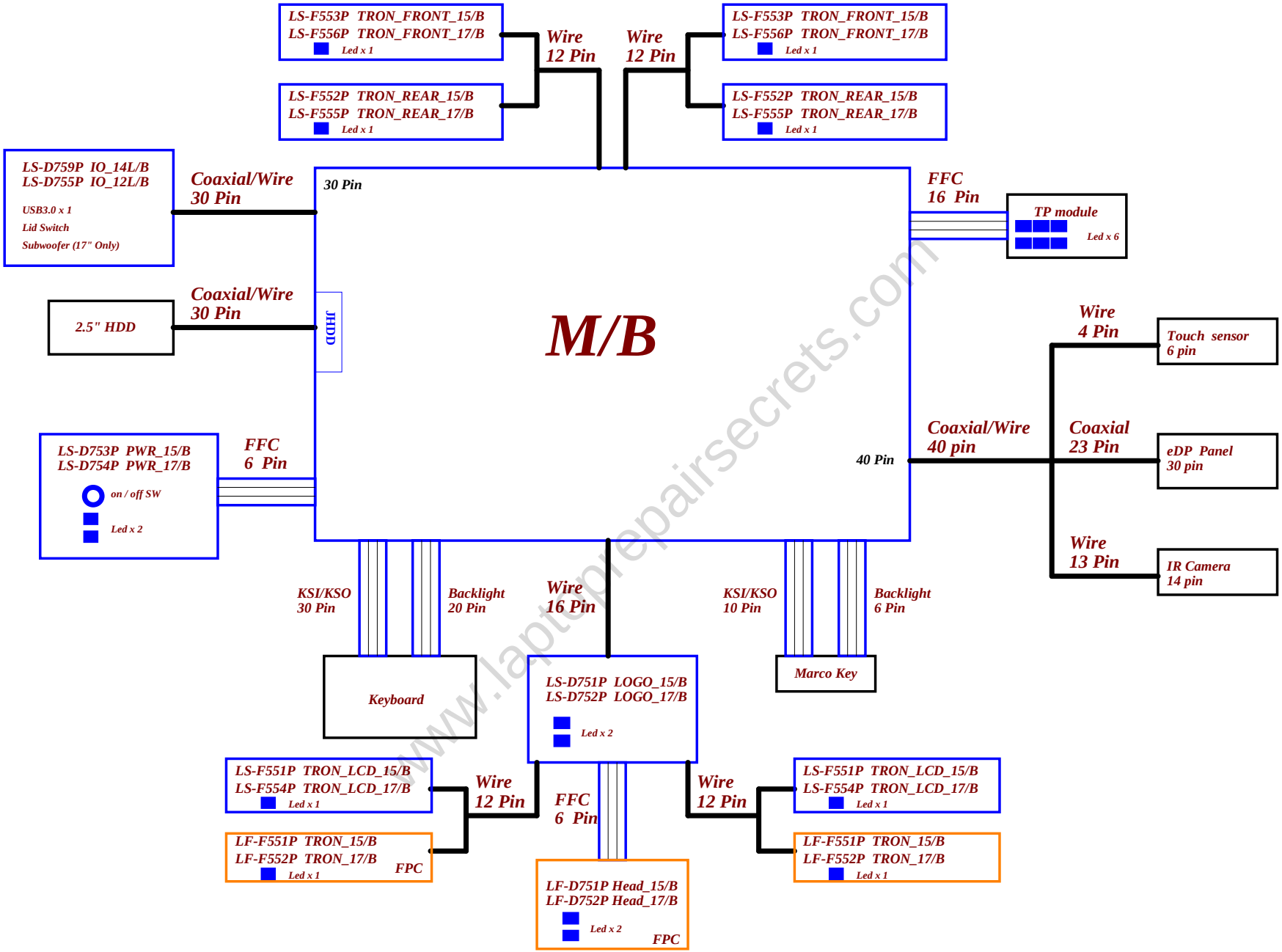

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **Cable Routing Diagram**

Size	Document Number	Rev
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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x13	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A	NVIDIA Graphic
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF	AMD Graphic
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0	
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF	

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID table

NV	AMD	PCB Revision
0	10	EVT-1
1	11	EVT-2
2	12	DVT-1
3	13	DVT-2
4	14	Pilot

PCH-H CM246

HSIO	USB3.1	PCIe	SATA3	Function
0	1			JUSBC2,type C
1	2			
2	3			
3	4			
4	5			
5	6			JUSB1,type A
6	7	1		JIO,IO/B
7	8	2		Caldera
8	9	3		
9	10	4		
10		5		
11		6		
12		7		
13		8		
14		9		JSSD3 , 2280 SATA/PCIe x4
15		10		
16		11	0a	
17		12	1a	
18		13	0b	JSSD4/HDD
19		14	1b	
20		15	2	LAN
21		16	3	WLAN
22		17	4	JSSD1 , 2242 SATA/PCIe x4
23		18	5	
24		19		
25		20		
26		21		JSSD2 , 2280 PCIe x4
27		22		
28		23		
29		24		

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	Per Key
11	Thunderbolt AR
12	
13	
14	Bluetooth

Symbol Note :

Digital Ground

Analog Ground

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Title: Notes List

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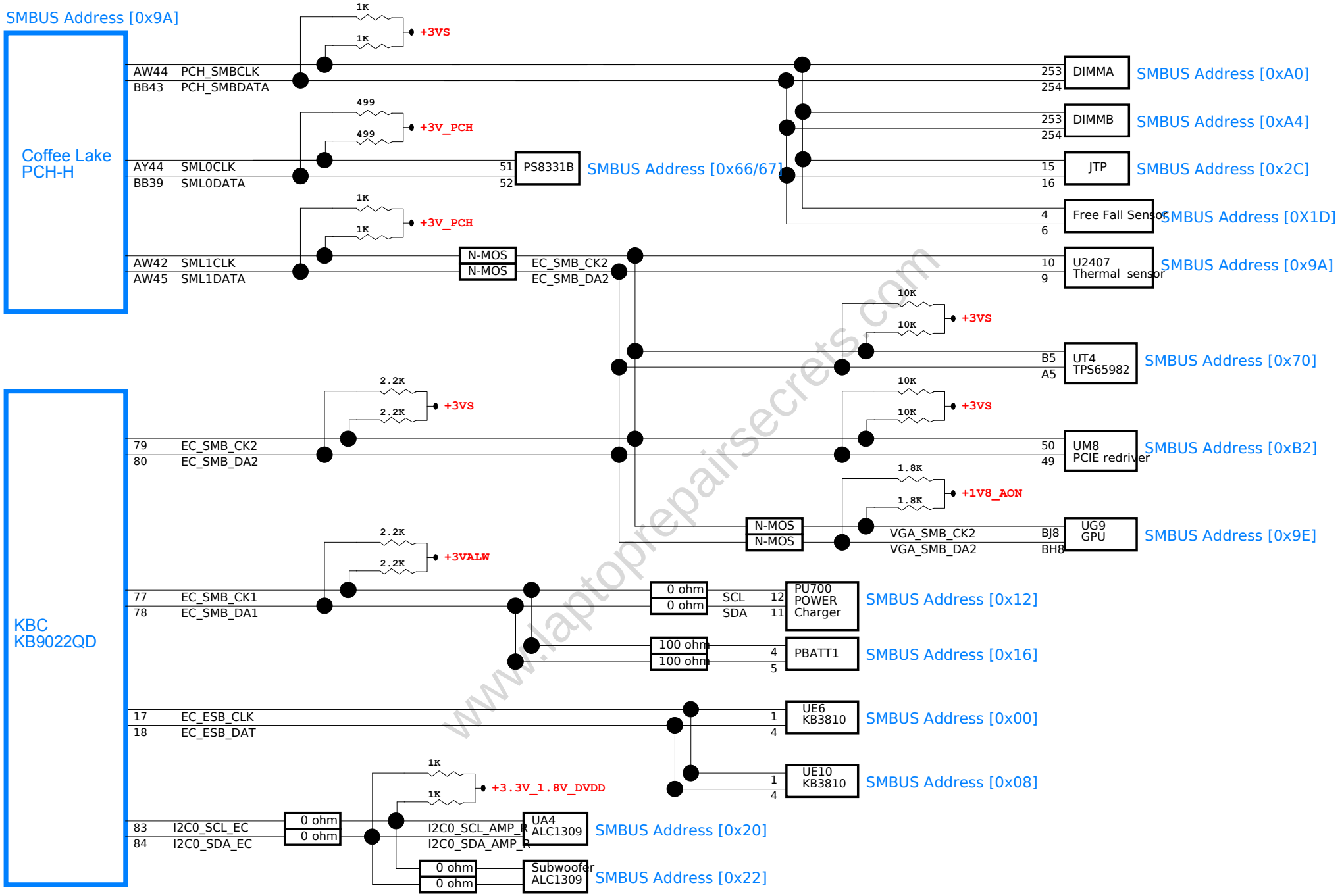


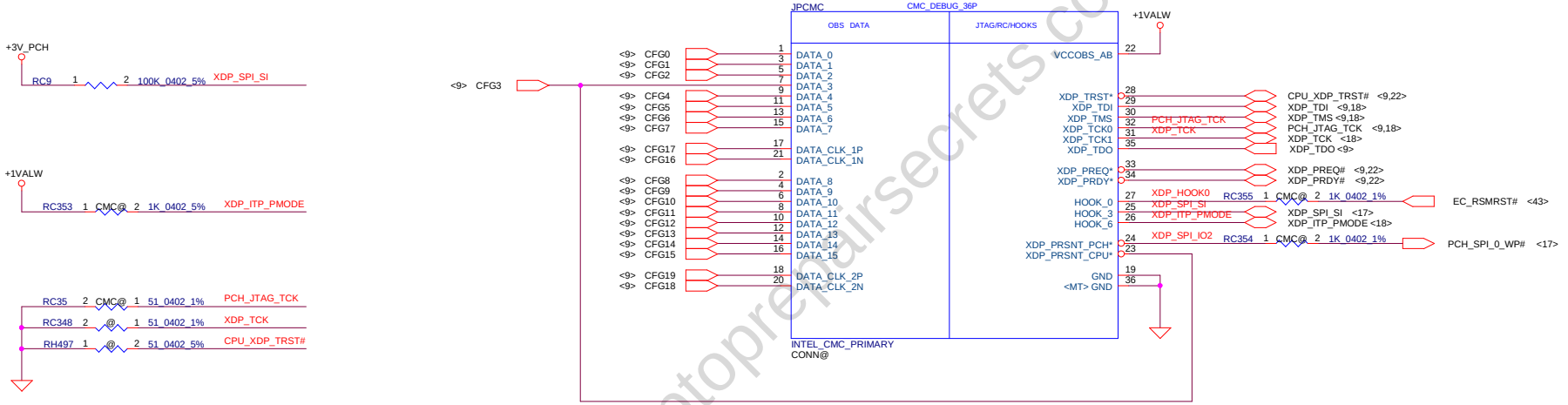
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **SMBus Block Diagram**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 Sheet 5 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CMC Conn**

Size	Document Number	Rev
	LA-F551P	0.3

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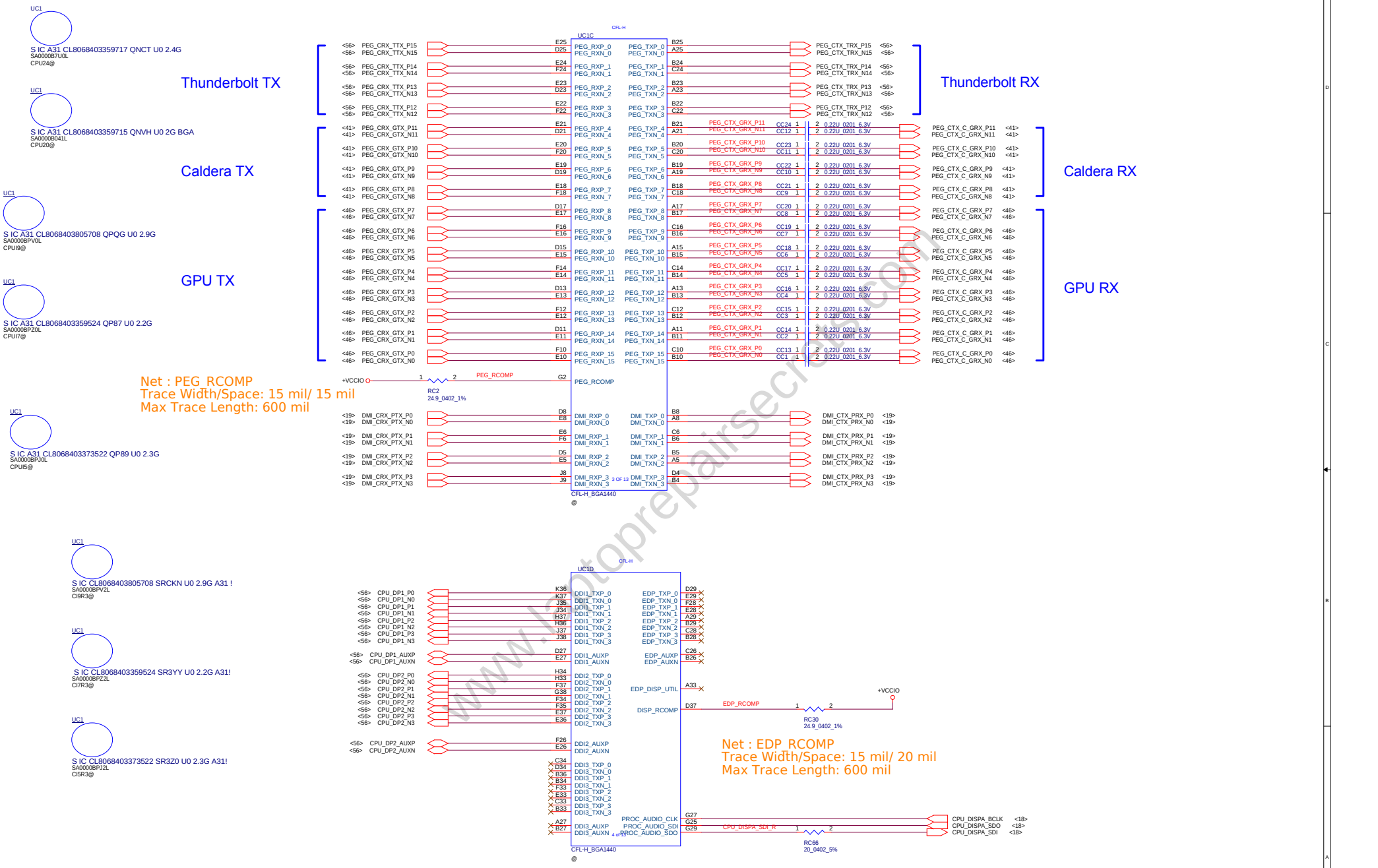

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.	
Title	CPU(1/7) DMI,PEG,DDI,EDP
Size	Document Number: LA-F551P
Rev	0.3
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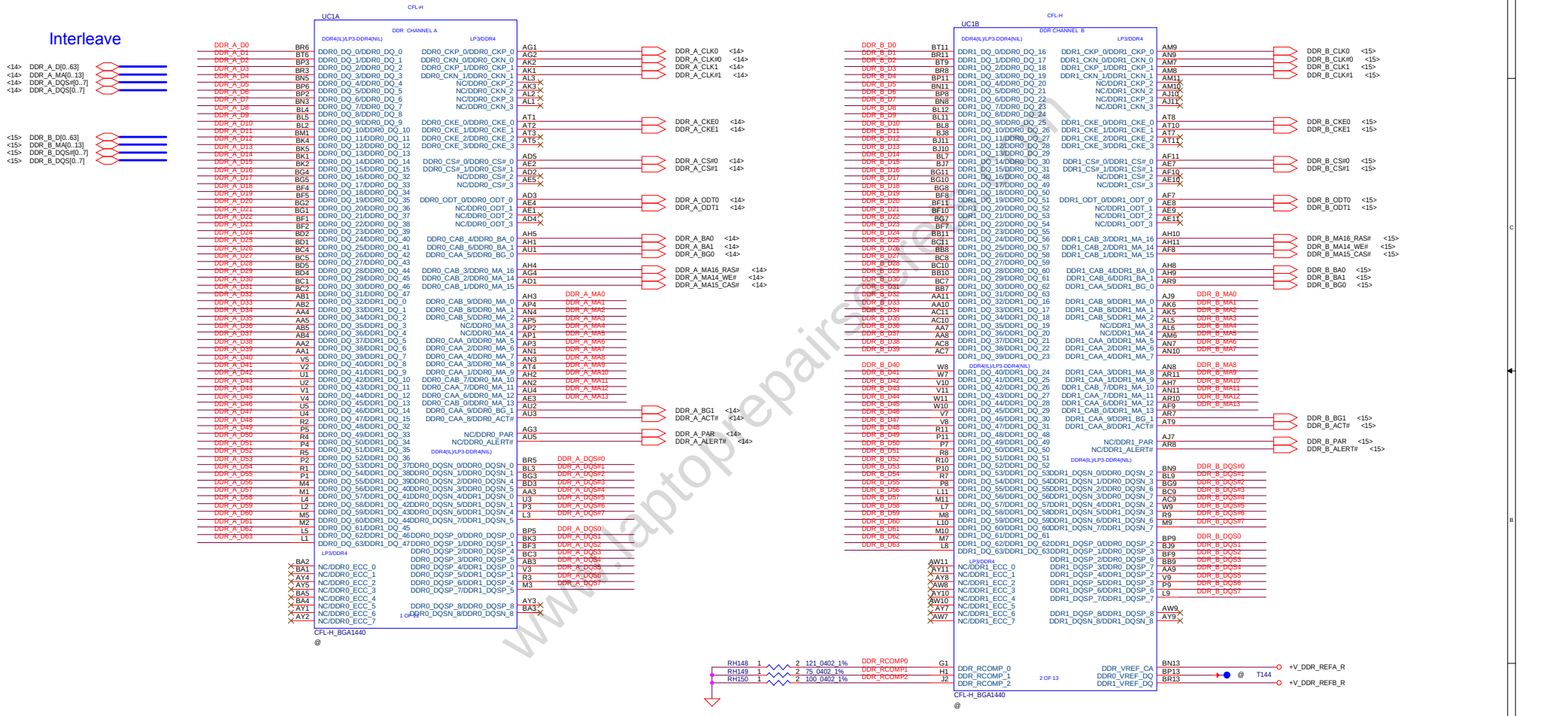

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(2/7) DDR4**

Size	Document Number	Rev
	LA-F551P	0.3

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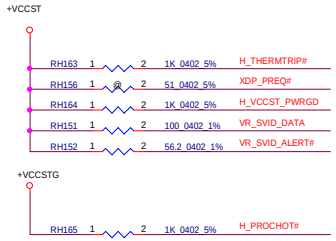
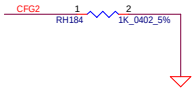
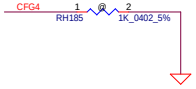


PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

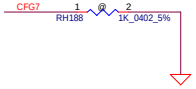


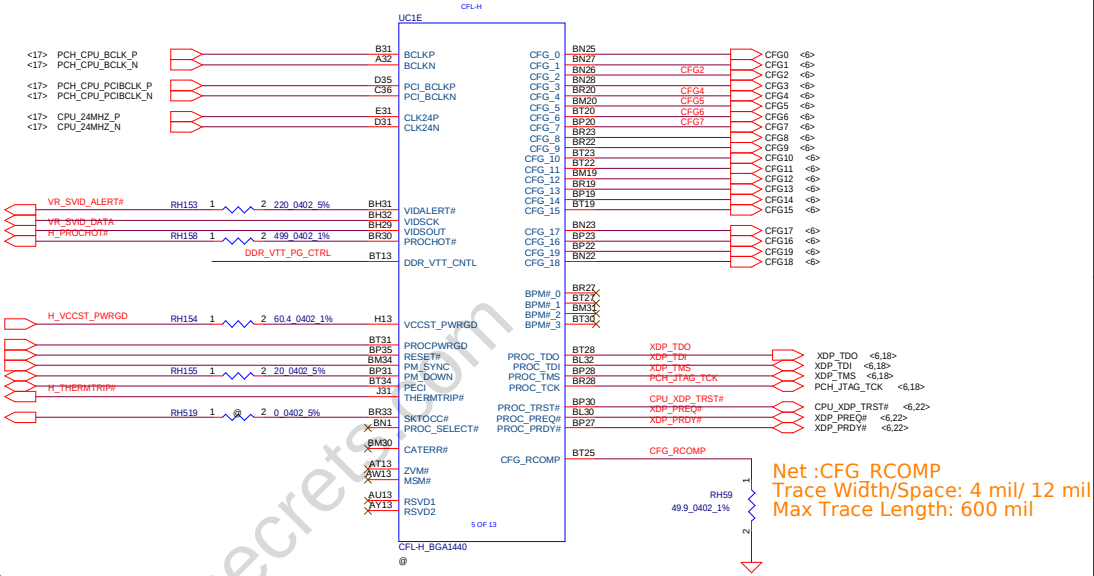
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



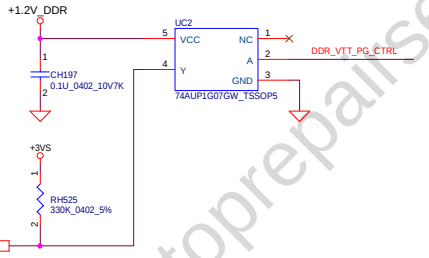
PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) *00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

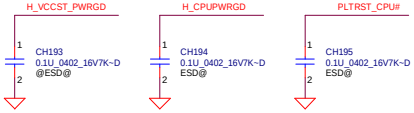
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

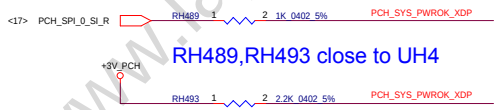




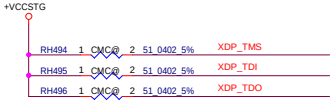
Net :CFG_RCOMP
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil







RH489,RH493 close to UH4



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.	
Title	CPU(3/7) CFG,XDP
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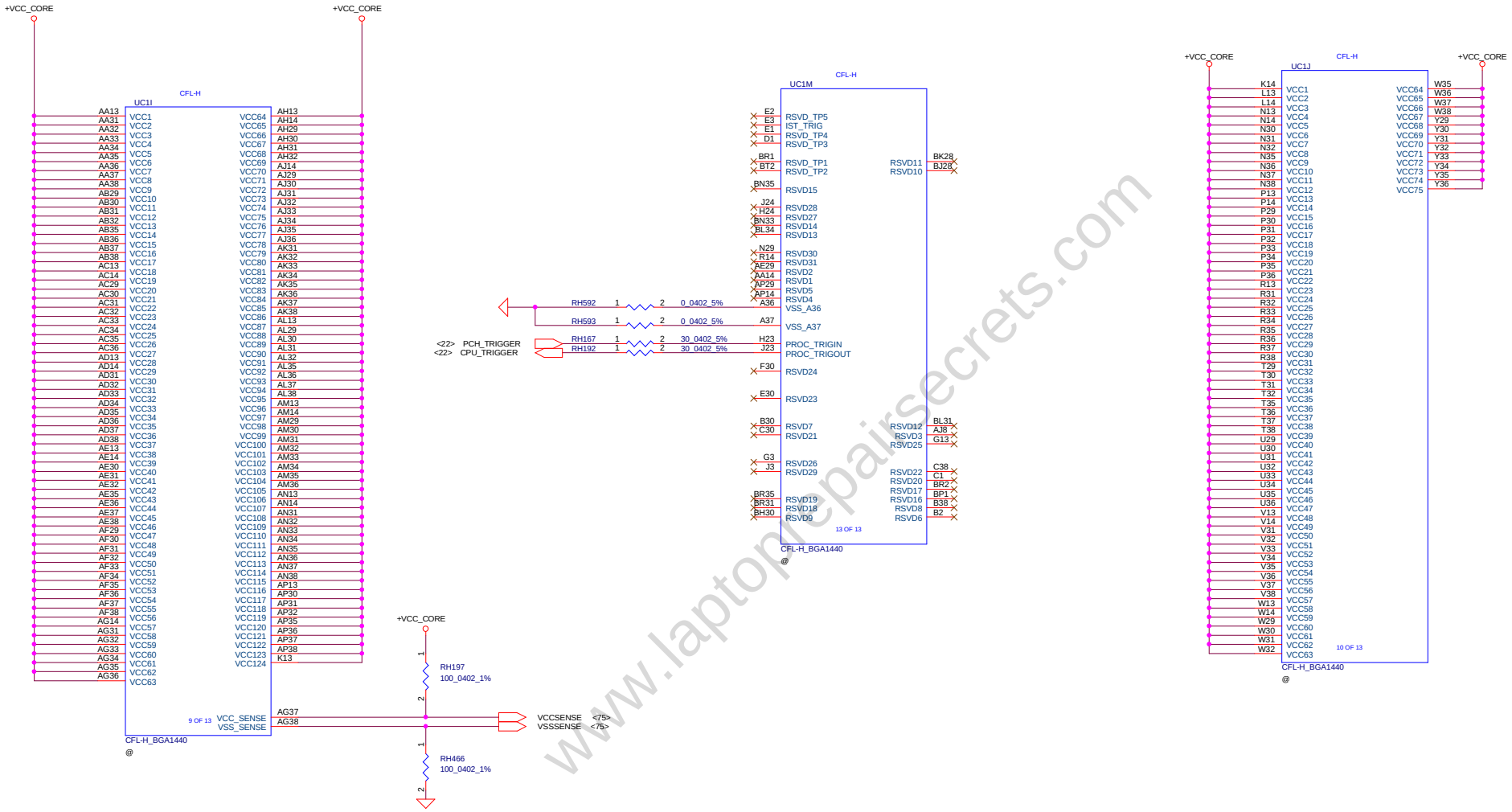

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(4/7) +VCC_CORE,RSVD**

Size	Document Number	Rev
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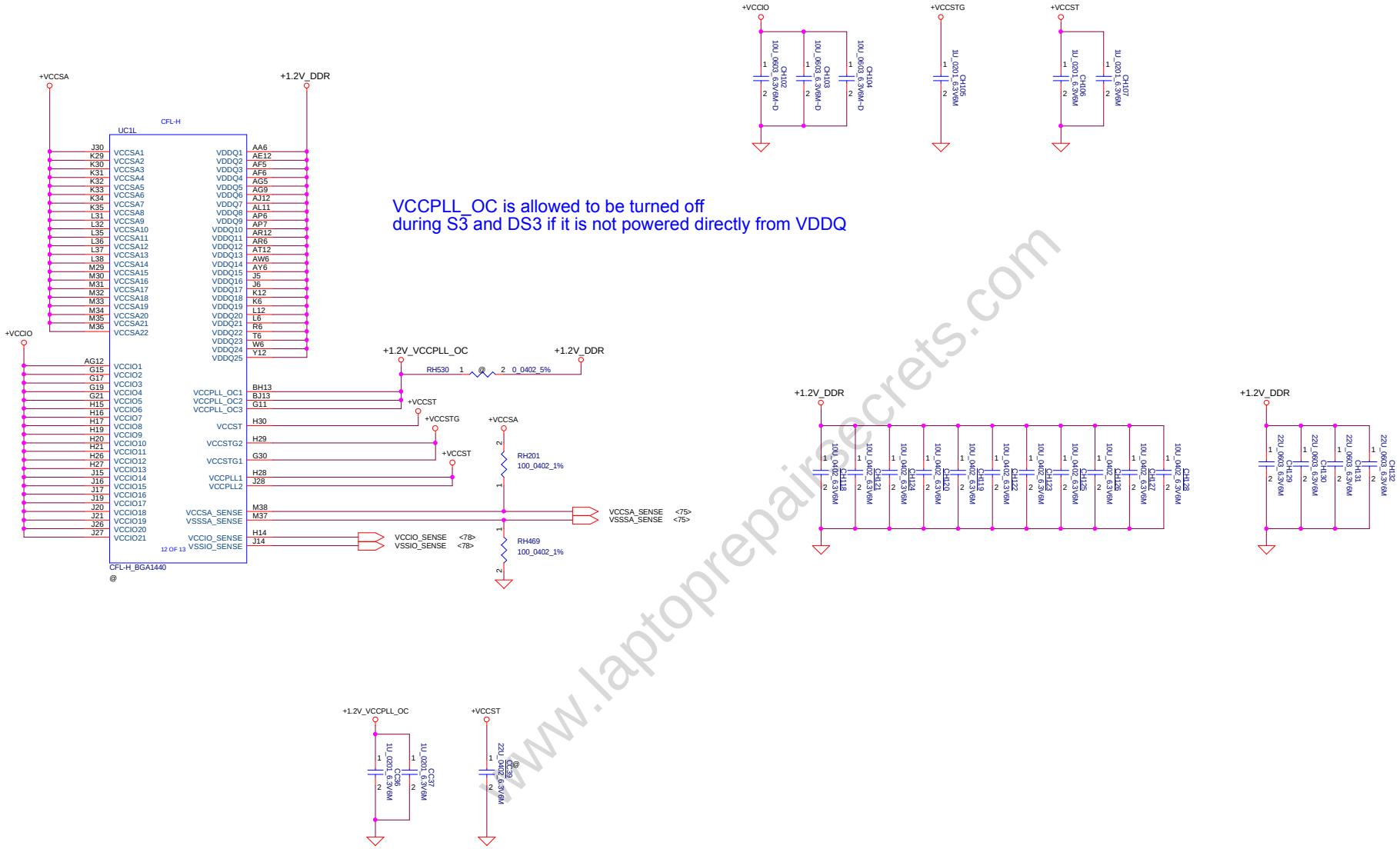

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(5/7) +VCCSA,+VCCIO**

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1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(6/7) +VCCGT**

Size	Document Number	Rev
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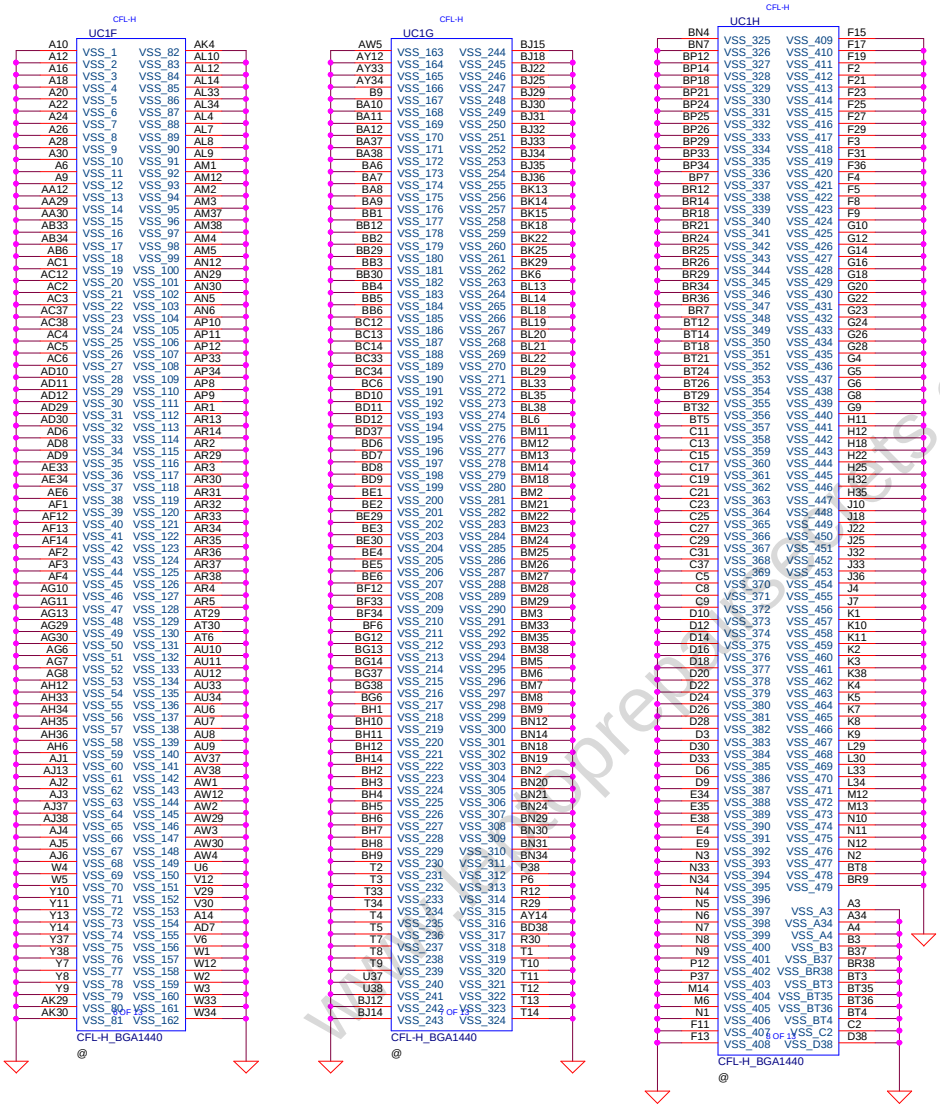

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(7/7) VSS**

Size | Document Number: **LA-F551P** | Rev: 0.3

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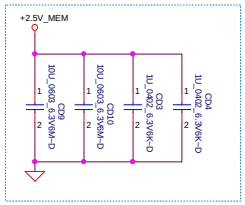
4H , RVS

Layout Note:
Place near JDIMM1.257,259



Layout Note:
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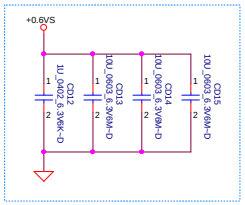

Layout Note:
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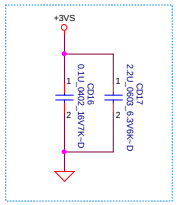
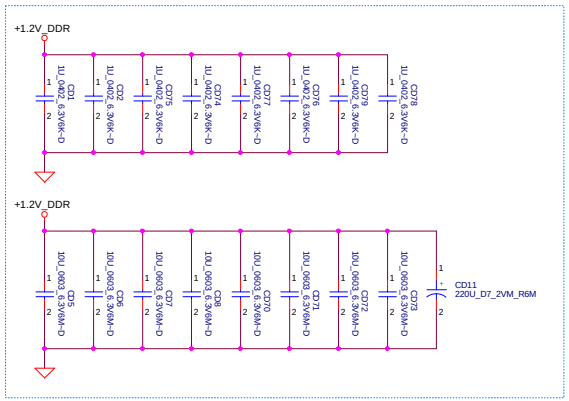
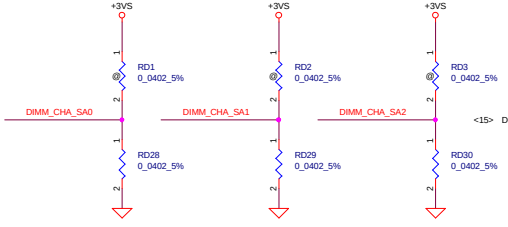
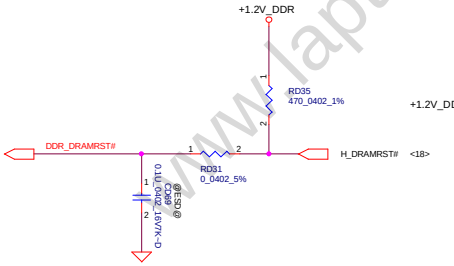


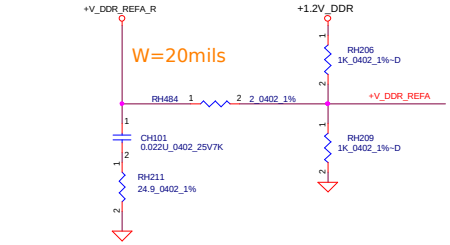
Layout Note:
Place near JDIMM1



<8> DDR_A_D[0..63]
<8> DDR_A_MA[0..13]
<8> DDR_A_DQS#[0..7]
<8> DDR_A_DQS[0..7]







Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **DDR4 DIMMA,RVS**

Size	Document Number	Rev
	LA-F551P	0.3

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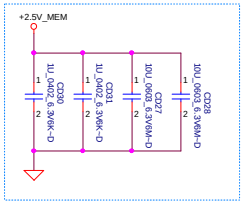
Layout Note:
Place near JDIMM2.257,259



Layout Note:
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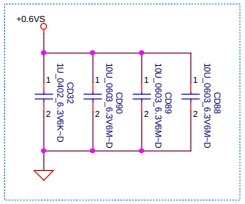

Layout Note:
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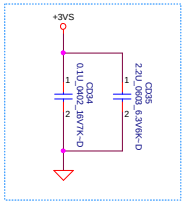
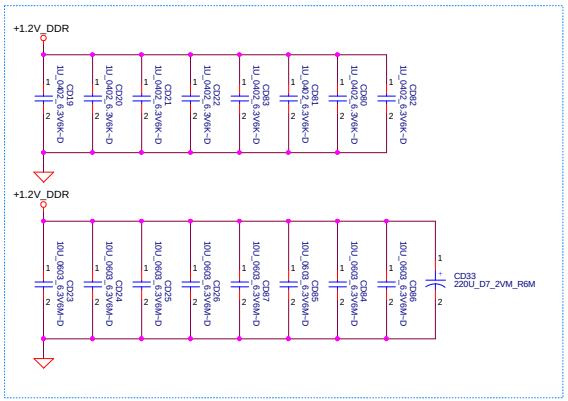
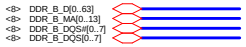
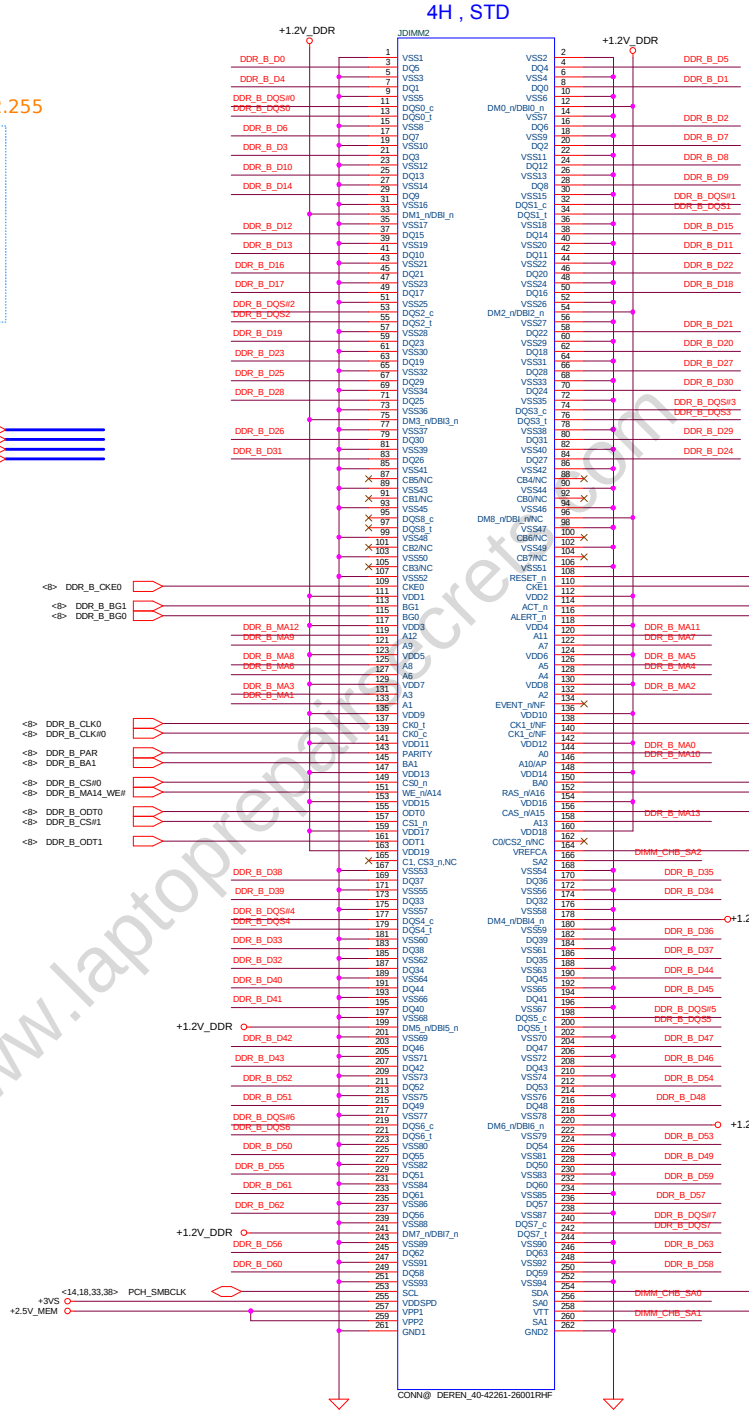


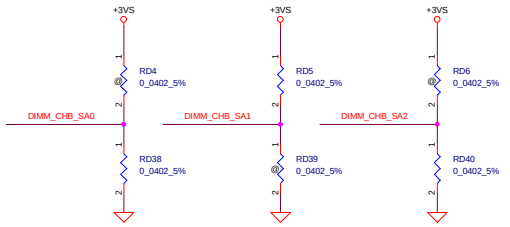
Layout Note:
Place near JDIMM2

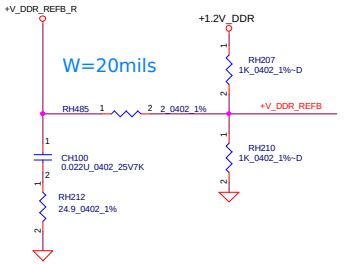




4H , STD







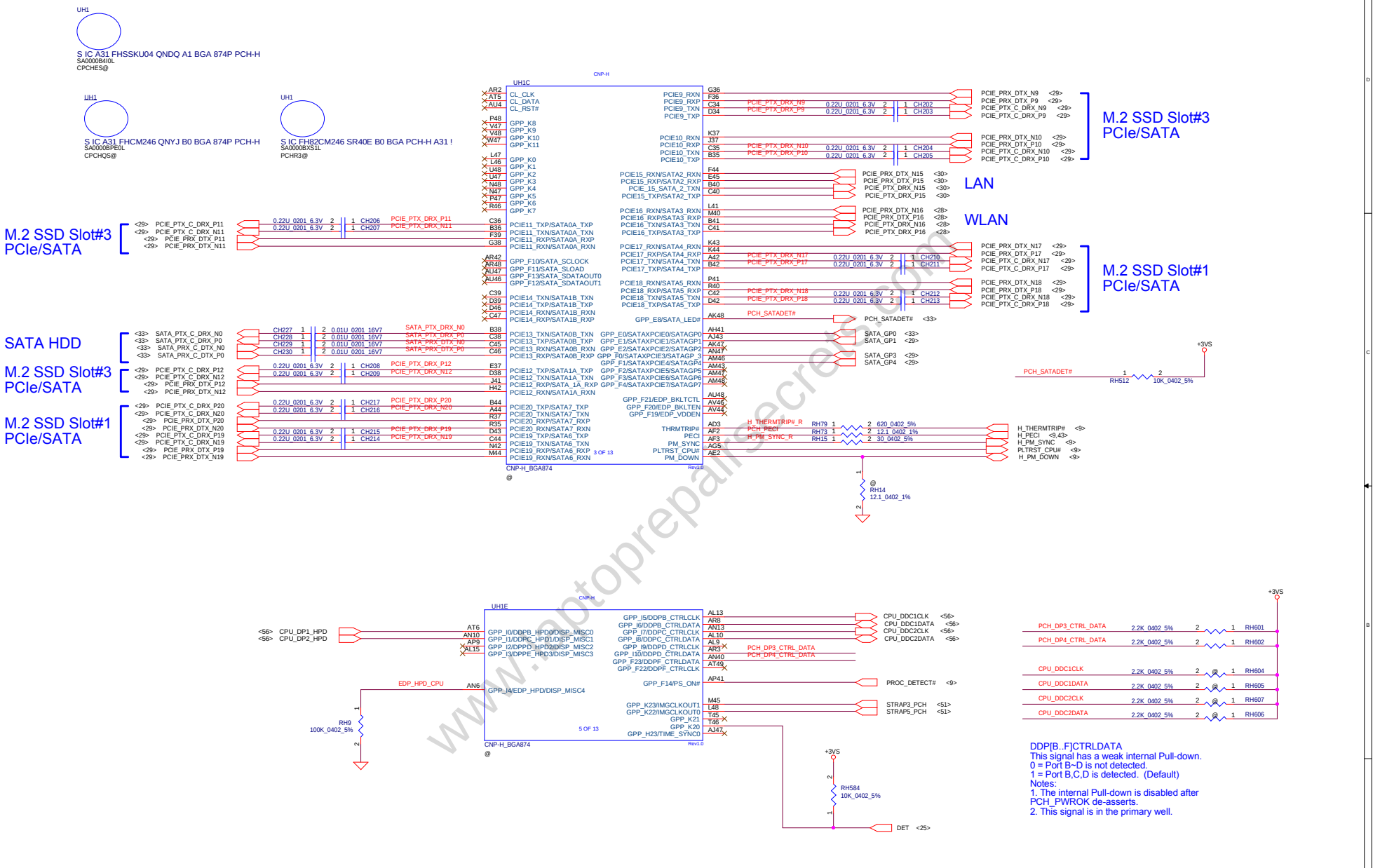
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **DDR4 DIMMB,STD**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 Sheet 15 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title: PCH (1/7) SATA,DDC,PCIE			
Size	Document Number: LA-F551P		Rev: 0.3
Date: Tuesday, March 06, 2018	Sheet 16 of 82		

Net : XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PEG(dGPU)
SSD1
SSD2
Thunderbolt
LAN
WLAN
Caldera
SSD3

#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
571007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

RH1 close to UH4

Internal pull high 20K , if used qual mode need 1K pull high

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to ' 0 ' if t he eSPI or LPC strap is configured to ' 0 '

S IC FL 128M W25Q128JVSIQ SOIC8P SPI ROM

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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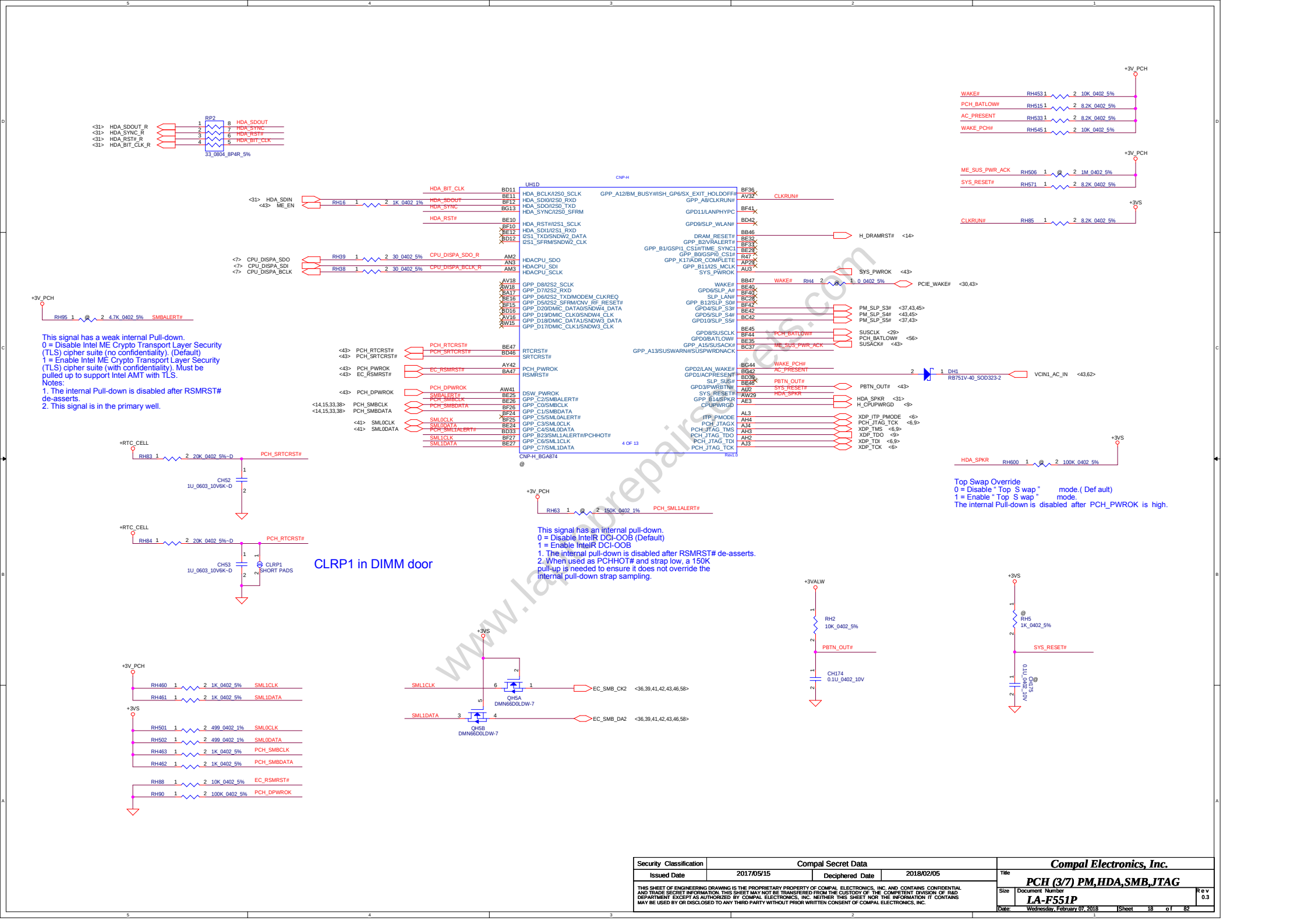
Compal Electronics, Inc.

Title: PCH (2/7) CLK,SPI,PLTRST

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 17 of 82



This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

CLRP1 in DIMM door

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

Top Swap Override
0 = Disable " Top S wap " mode.(Def ault)
1 = Enable " Top S wap " mode.
The internal Pull-down is disabled after PCH_PWROK is high.

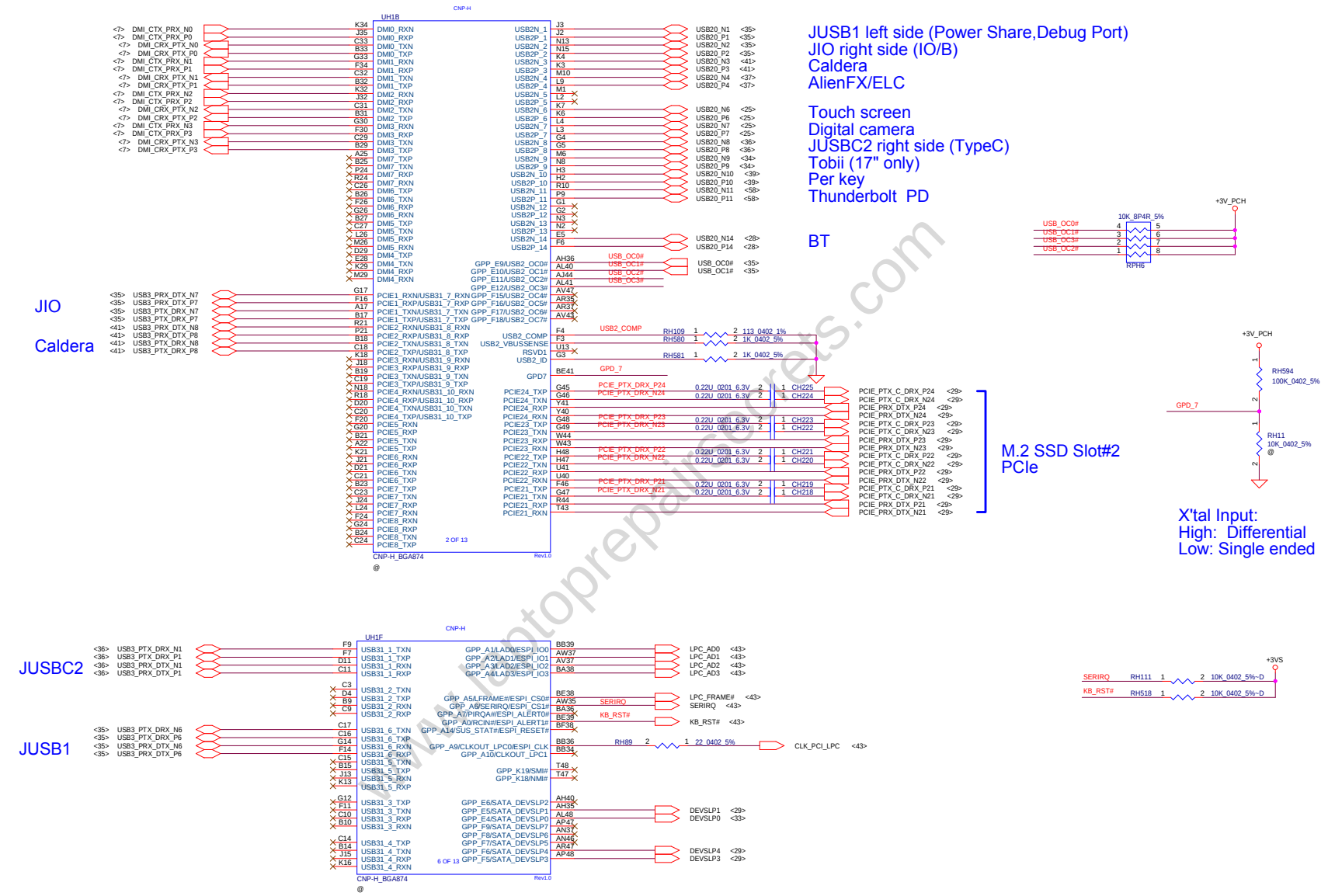
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: PCH (3/7) PM,HDA,SMB,JTAG

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 Sheet 18 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 19 of 82

nVidia GPU_ID	N17_ID1	N17_ID0
N17EG3	H	H
N17EG2	H	L
N17EG1	L	H
N17PG1	L	L

RH25 N17EG3@ — S RES 1/20W 10K +-5% 0201 SD043100280
RH27 N17EG3@ — S RES 1/20W 10K +-5% 0201 SD043100280
RH25 N17EG2@ — S RES 1/20W 10K +-5% 0201 SD043100280
RH28 N17EG2@ — S RES 1/20W 10K +-5% 0201 SD043100280
RH26 N17EG1@ — S RES 1/20W 10K +-5% 0201 SD043100280
RH27 N17EG1@ — S RES 1/20W 10K +-5% 0201 SD043100280

BOARD_ID — RH21 NV@ 10K 0201 5%, RH22 AMD@ 10K 0201 5% — +3V_PCH
N17_ID1 — RH25, RH26 10K 0201 5% — +3V_PCH
N17_ID0 — RH27, RH28 10K 0201 5% — +3V_PCH
GSYNC_ID — RH29 GSYNC@, RH30 NGSYNC@ 10K 0201 5% — +3V_PCH

+3VS
RH517 @ 8.2K 0402 5% BT_OFF#
RH520 @ 8.2K 0402 5% WL_OFF#
RH521 10K 0402 5% EC_SCI#
RC62 49.9K 0402 1% UART_2_PRXD_DTXD
RC63 49.9K 0402 1% UART_2_PTXD_DRXD
RH516 @ 10K 0402 5% DGPU_PWROK
RH588 @ 10K 0402 5% VROM_SEL
RH589 @ 10K 0402 5% VROM_SEL

+5VALW
JWDB — ACES_88266-04001 — CONN@
UART_2_PTXD_DRXD
UART_2_PRXD_DTXD

CNP-H
UH1K — CNP-H_BGA874 — Rev1.0

BBS_BIT0 — BA26 GPP_B22/GSPI1_MOSI
<37> ELC_RESET — BD30 GPP_B21/GSPI1_MISO
<43> EC_SCI# — AU26 GPP_B20/GSPI1_CLK
<51> VROM_SEL — AW26 GPP_B19/GSPI1_CS0#
NRB_BIT — BE30 GPP_B18/GSPI0_MOSI
<37> ELC_BOOT_MODE — BD29 GPP_B17/GSPI0_MISO
<23,46> GC6_FB_EN — BF29 GPP_B16/GSPI0_CLK
<46> GC6_EVENT# — BB26 GPP_B15/GSPI0_CS0#
BB24 GPP_C9/UART0A_TXD
<28> WL_OFF# — BE23 GPP_C8/UART0A_RXD
<28> BT_OFF# — AP24 GPP_C11/UART0A_CTS#
BA24 GPP_C10/UART0A_RTS#
<27> HDMI_HPD_PCH — BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
<26> DP_HPD_PCH — AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD
<56> TBT_CIO_PLUG_EVENT# — AV21 GPP_C23/UART2_CTS#
AW21 GPP_C22/UART2_RTS#
<28> UART_2_PTXD_DRXD — BE20 GPP_C21/UART2_TXD
<28> UART_2_PRXD_DTXD — BD20 GPP_C20/UART2_RXD
<56> RTD3_USB_PWR_EN — BE21 GPP_C19/I2C1_SCL
<56> RTD3_CIO_PWR_EN — BF21 GPP_C18/I2C1_SDA
<38> I2C_0_SCL — BC22 GPP_C17/I2C0_SCL
<38> I2C_0_SDA — BF23 GPP_C16/I2C0_SDA
<38,43> TP_INT# — BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SPI4_IO3
<43> DGPU_PWROK — BE14 GPP_D23/ISH_I2C2_SCL/I2C3_SCL

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# — BA20 — BOARD_ID
GPP_D10/ISH_SPI_CLK/GSPI2_CLK — BB20 — DGPU_HOLD_RST# — DGPU_HOLD_RST# <23,46>
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO — BB16 — DGPU_PWR_EN — DGPU_PWR_EN <23,43,49>
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI — AN18
GPP_D16/ISH_UART0_CTS#/CNV_WCEN — BF14 — N17_ID1
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN — AR18 — N17_ID0
GPP_D14/ISH_UART0_TXD/I2C2_SCL — BF17 — GSYNC_ID
GPP_D13/ISH_UART0_RXD/I2C2_SDA — BE17
GPP_H20/ISH_I2C0_SCL — AG45
GPP_H19/ISH_I2C0_SDA — AH45
GPP_H22/ISH_I2C1_SCL — AH47
GPP_H21/ISH_I2C1_SDA — AH48
GPP_A23/ISH_GP5 — AV34
GPP_A22/ISH_GP4 — AW22
GPP_A21/ISH_GP3 — BA33 — XMP2 <64>, XMP1 <64>
GPP_A20/ISH_GP2 — BE34
GPP_A19/ISH_GP1 — BD34 — CLKDET#
GPP_A18/ISH_GP0 — BF38 — DGPU_PRSNT#
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 — BD38
RH135 @ 10K_0402_5%

+3VS — RPC7 10K_0804_8P4R_5% — I2C_0_SDA, I2C_0_SCL
+3VS — DGPU_PWR_EN — RH537 10K 0201 5%
+3V_PCH — CLKDET# — RH558 @ 10K 0201 5%
+3V_PCH — RH130 @ 4.7K 0402 5%-D — BBS_BIT0

Boot BIOS Strap Bit (internal PD)
HIGH : LPC
LOW(DEFAULT) SPI

+3V_PCH — RH524 @ 4.7K 0402 5%-D — NRB_BIT

NO REBOOT mode (internal PD)
HIGH : Enable
LOW(DEFAULT) Disable

+1.8V_PRIM — RH595 10K 0402 5% — CNV_RGI_PTX_DRX
RH168 @ 10K 0402 5%

M.2 CNV Mode Select
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

+1.8VALW — RH603 4.7K 0402 5% — CNV_BRI_PTX_DRX

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM — RH218 @ 10K 0402 5% — GPP_J9

The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a 1 for the proper functionality of the SPI (Flash) I/Os

CNP-H
UH1M — CNP-H_BGA874 — 13 OF 13 — Rev1.0

GPP_G0/SD_CMD — AW13
GPP_G1/SD_DATA0 — BE9
GPP_G2/SD_DATA1 — BF8
GPP_G3/SD_DATA2 — BF9
GPP_G4/SD_DATA3 — BG8
GPP_G5/SD_CD# — BE8
GPP_G6/SD_CLK — BD8
GPP_G7/SD_WP — AV13
GPP_I11/M2_SKT2_CFG0 — AP3
GPP_I12/M2_SKT2_CFG1 — AP2
GPP_I13/M2_SKT2_CFG2 — AN4
GPP_I14/M2_SKT2_CFG3 — AM7
CPU_VCCIO_PWR_GATE# — GPP_J0/CNV_PA_BLANKING — AV6
GPP_J1/CPU_C10_GATE# — AY3
GPP_J1I/A4WP_PRESENT — AR13
GPP_J10 — AV7
GPP_J_2 — AW3
GPP_J_3 — AT10
CNV_BRI_PTX_DRX — GPP_J4/CNV_BRI_DT/UART0B_RTS# — AV4
CNV_BRI_PRX_DTX — GPP_J5/CNV_BRI_RSP/UART0B_RXD — AY2
CNV_RGI_PTX_DRX — GPP_J6/CNV_RGI_DT/UART0B_TXD — BA4
CNV_RGI_PRX_DTX — GPP_J7/CNV_RGI_RSP/UART0B_CTS# — AV3
GPP_J9 — GPP_J8/CNV_MFUART2_RXD — AW2
GPP_J9/CNV_MFUART2_TXD — AU9

CNV_WR_CLKN — BD4
CNV_WR_CLKP — BE3
CNV_WR_D0N — BB3
CNV_WR_D0P — BB4
CNV_WR_D1N — BA3
CNV_WR_D1P — BA2
CNV_WT_CLKN — BC5
CNV_WT_CLKP — BB6
CNV_WT_D0N — BE6
CNV_WT_D0P — BD7
CNV_WT_D1N — BG6
CNV_WT_D1P — BF6
CNV_WT_RCOMP — BA1 — RH213 150 0402 1%
PCIE_RCOMPN — B12 — RH193 100 0402 1%
PCIE_RCOMPP — A13
PCIE_RCOMPN — BE5 — RH214 200 0402 1%
PCIE_RCOMPP — BE4 — RH215 200 0402 1%
SD_1P8_RCOMP — BD1
SD_3P3_RCOMP — BE1
GPPJ_RCOMP_P1R81 — BE2 — GPPJ_RCOMP_1P8 — RH216 200 0402 1%
GPPJ_RCOMP_P1R82 — Y35
GPPJ_RCOMP_P1R83 — Y36
RSVD2 — BC1
RSVD3 — AL35
RSVD1 — T135 PAD-D @
TP

#571483_CFL_H_RVP_CRB_TDK_Rev0p7
Recommend external test point

+1.8VALW
RH181 20K 0402 1% — CNV_BRI_PRX_DTX
RH182 20K 0402 1% — CNV_RGI_PRX_DTX
RH180 @ 10K 0402 5% — CPU_VCCIO_PWR_GATE#

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

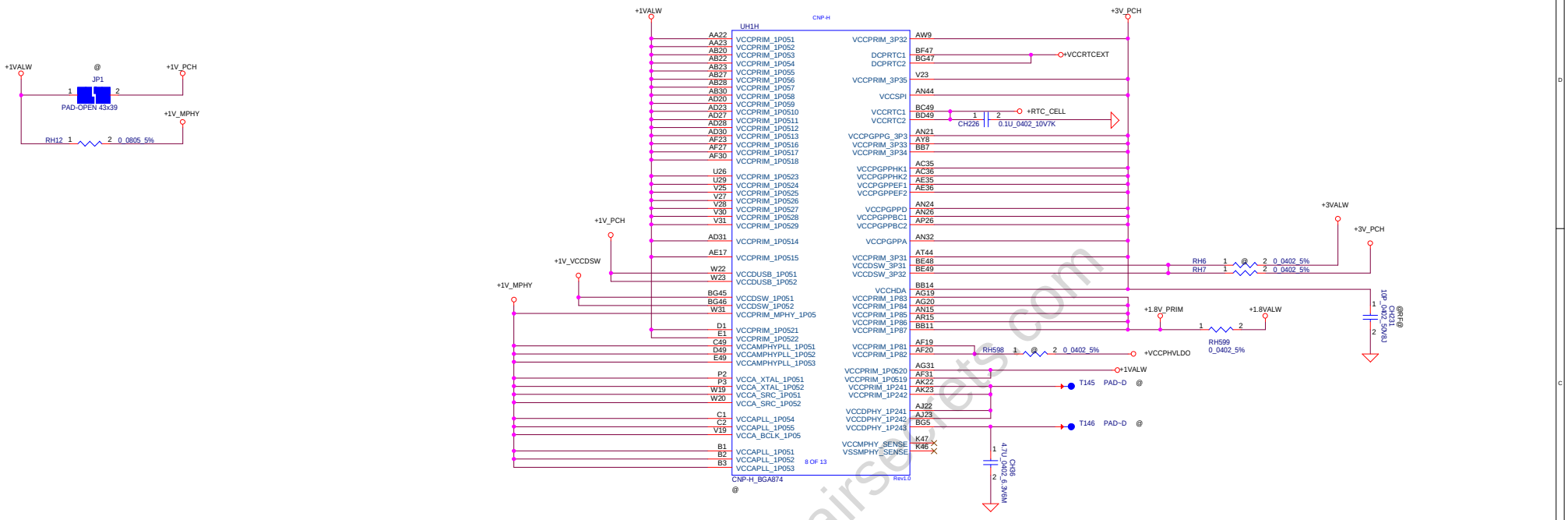
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

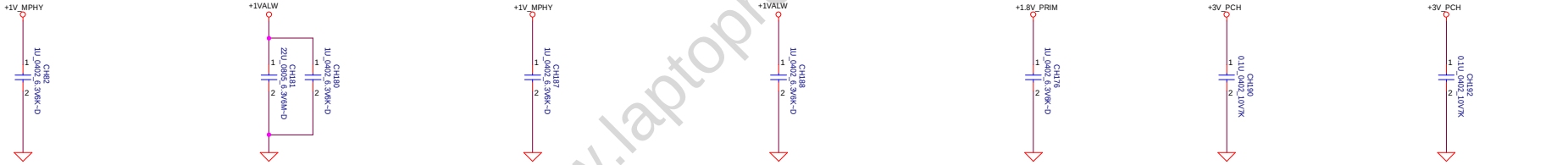
Compal Electronics, Inc.

Title: PCH (5/7) I2C,GPIO

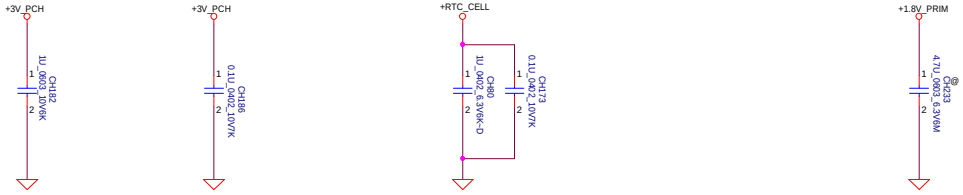
Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 20 of 82





Close to B1,B2,B3,C1,C2 Closeto U26,U29V25,V27,V28,V30,V31 Close to C49,D49,E49 Close to AF31,AG31,AD31,AA22,AA23,AB20,AB22,AB23,AB27,AB28,AB30,AD20,AD23,AD27,AD28,AD30,AF23,AF27,AF30,AE17 Close to AG19,AG20,AR15,AN15,BB11 Close to AE35,AE36 Close to AC35,AC36



Close to AY8,BB7 Close to BE48,BE49 Close to BC49,BD49 Close to AG19,AG20,AR15,AN15,BB11

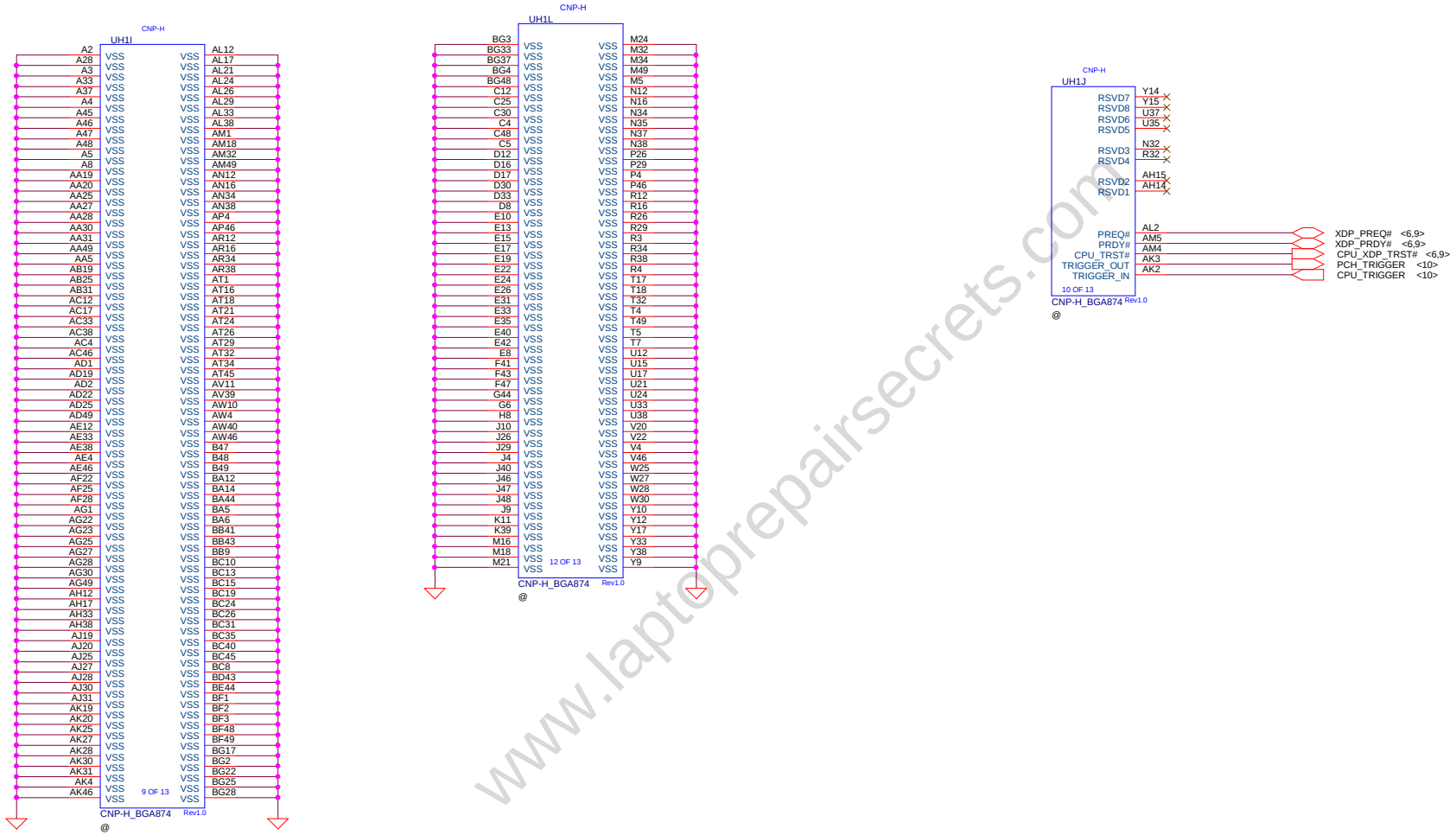
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (6/7) PWR**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 Sheet 21 of 82



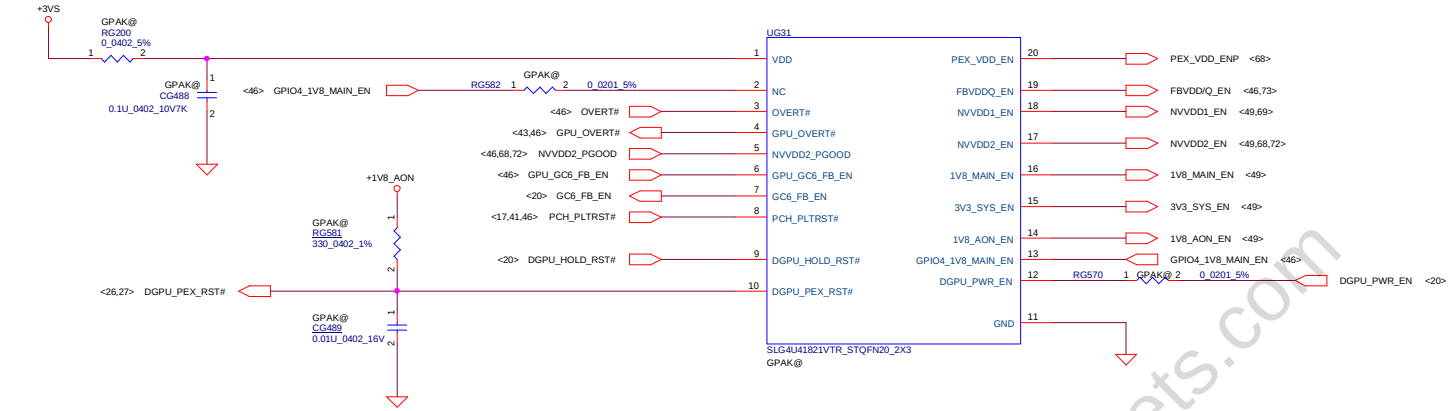
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (7/7) VSS**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 Sheet 22 of 82



PR801
S RES 1/16W 0 +-5% 0402
SD028000080
NGPAK@

PR6408
S RES 1/16W 10K +-1% 0402
SD034100280
GPAK@

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: GPAK SLG4U41821

Size | Document Number: LA-F551P | Rev: 0.3

Date: Thursday, March 01, 2018 | Sheet 23 of 82

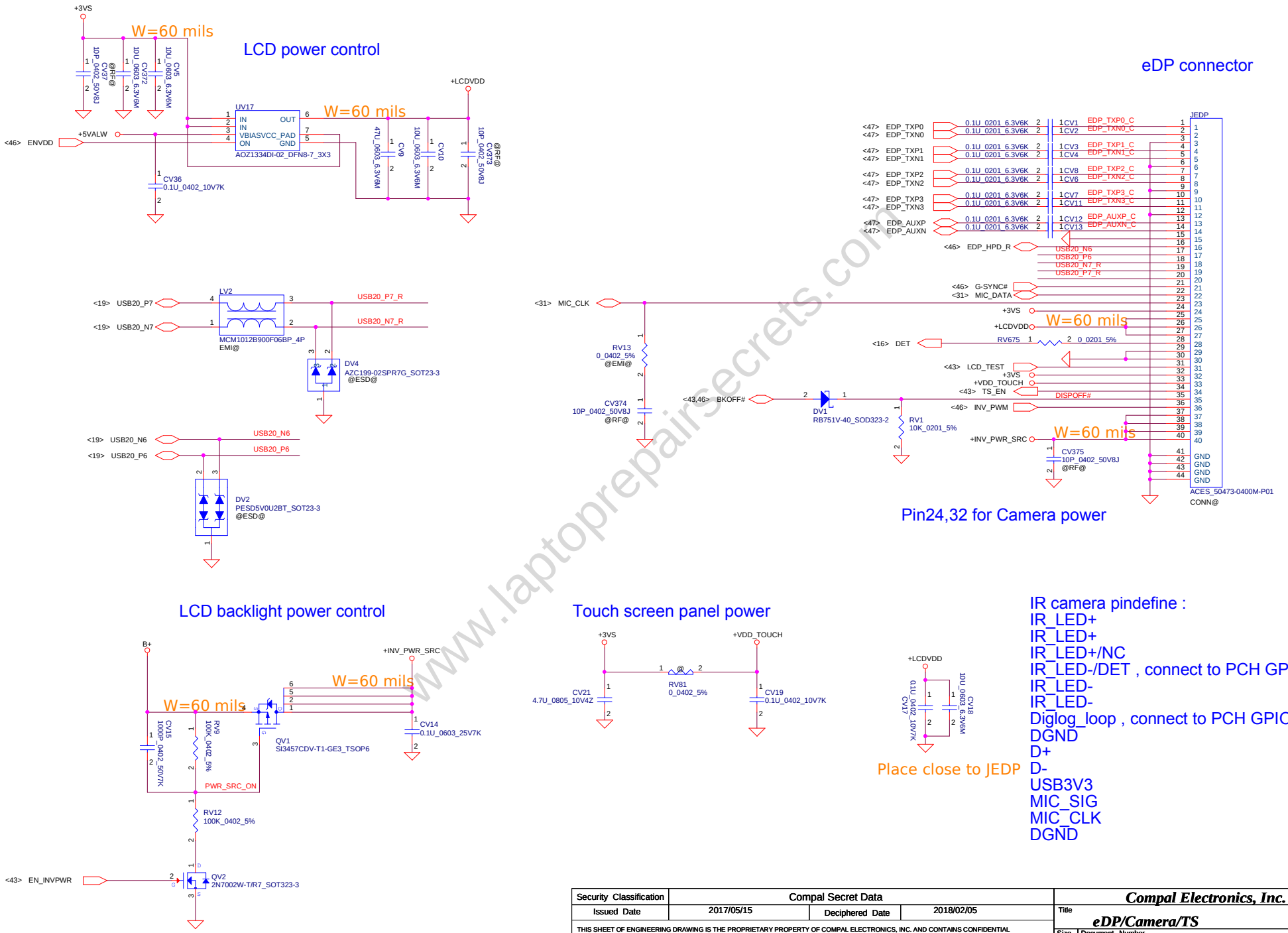
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: ***Reversed***

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 24 of 82



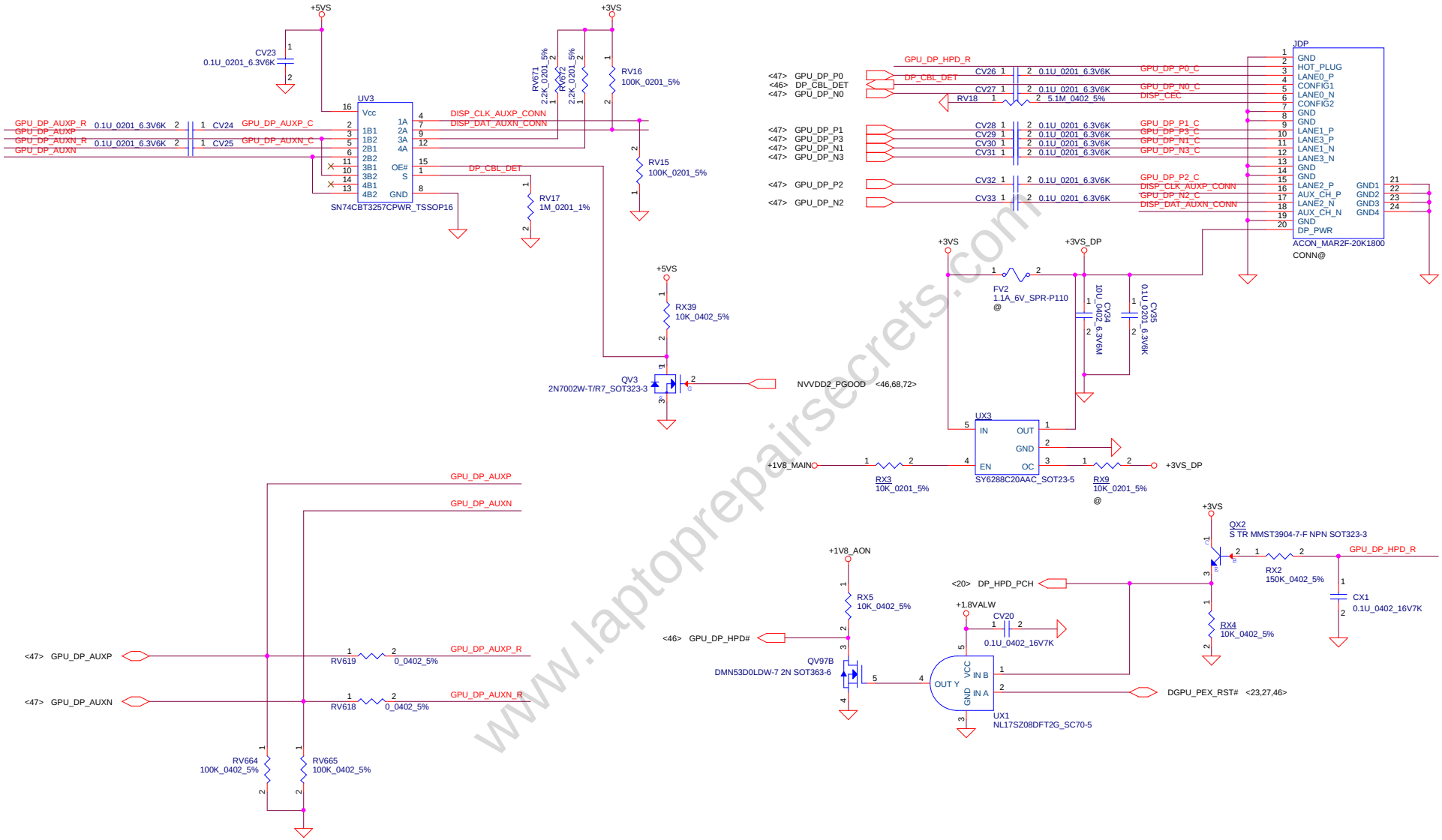
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **eDP/Camera/TS**

Size | Document Number: **LA-F551P** | Rev: 0.3

Date: Wednesday, February 07, 2018 | Sheet 25 of 82



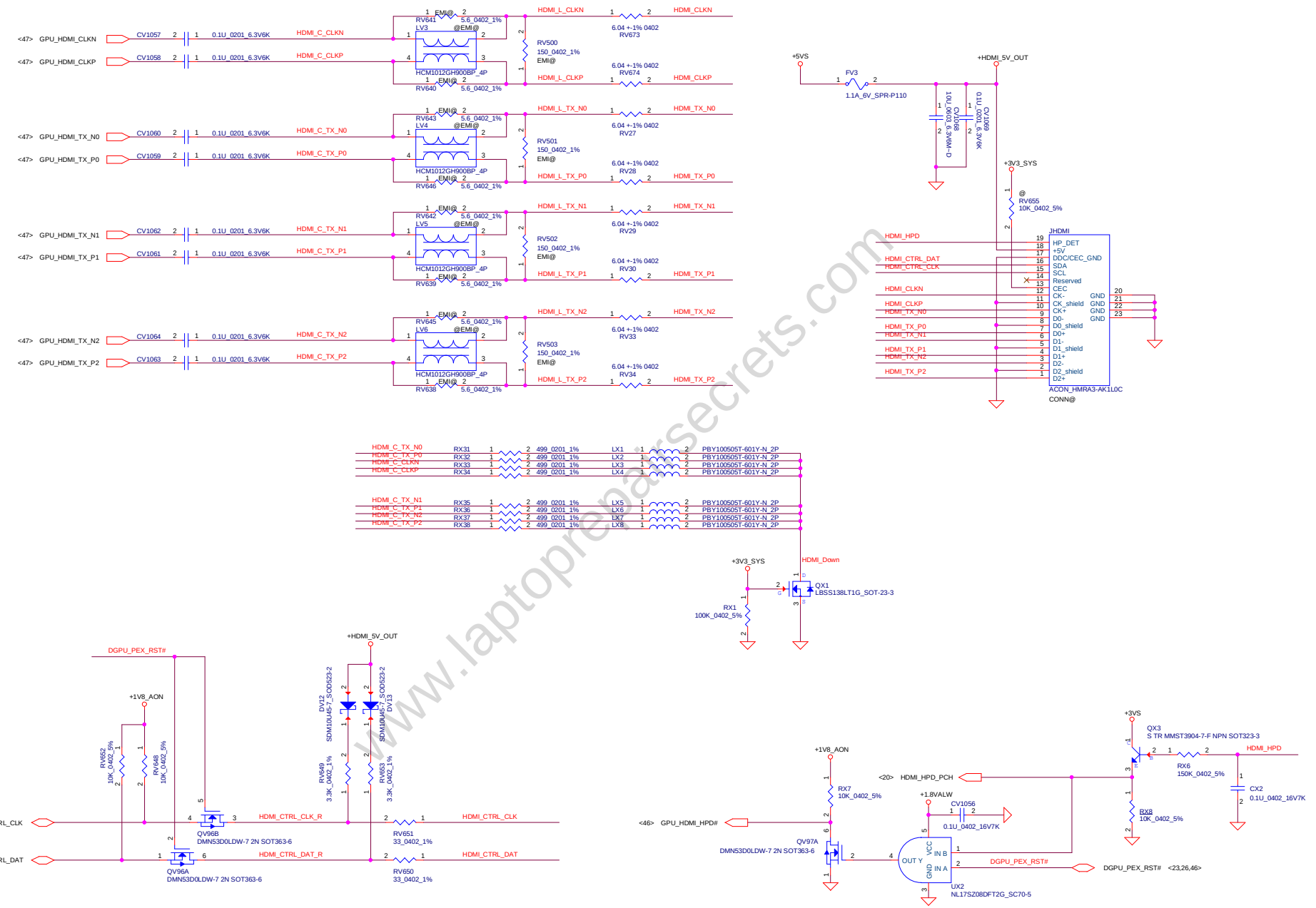
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **Mini DP**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 21, 2018 | Sheet 26 of 82



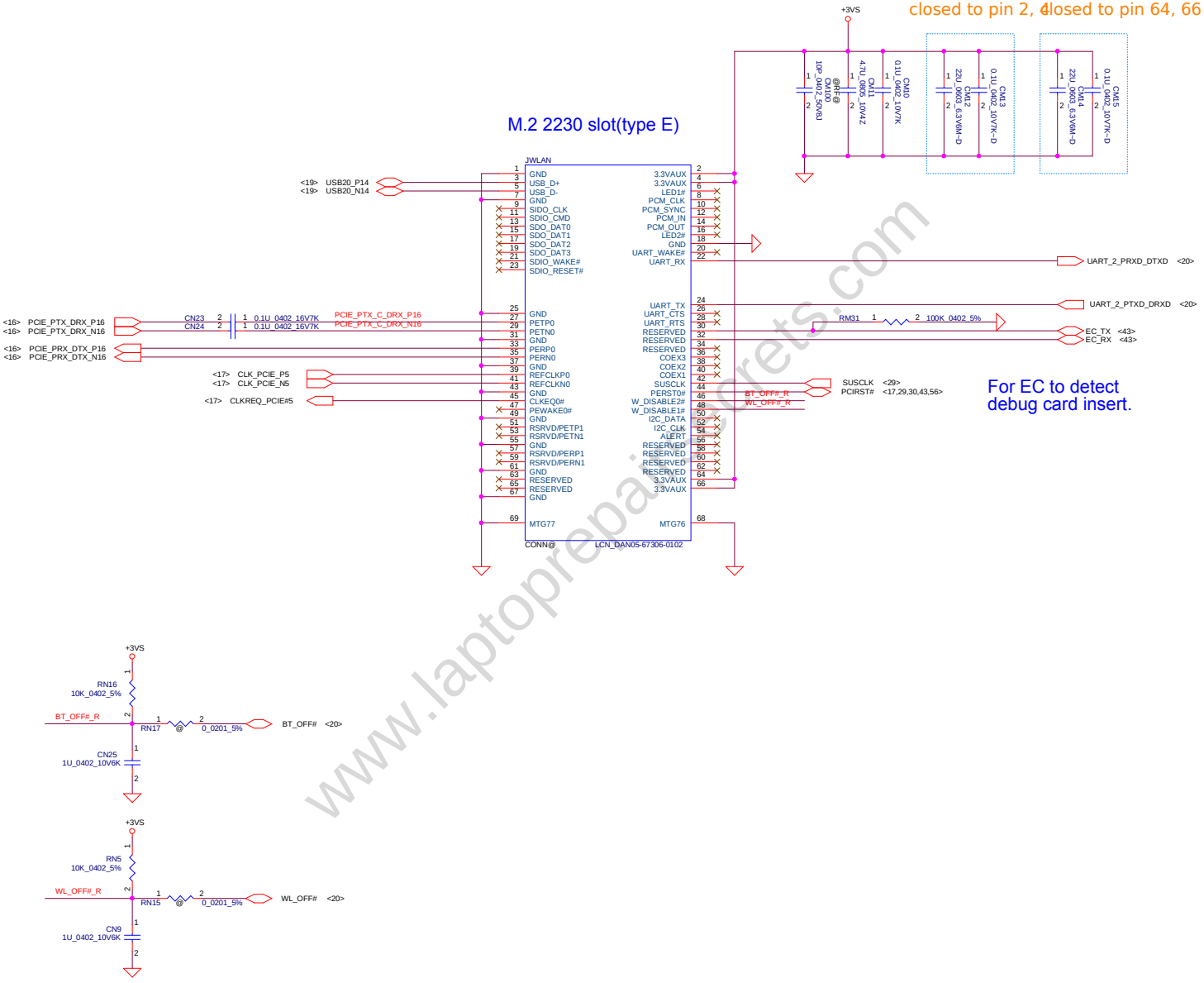
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **HDMI**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 27 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

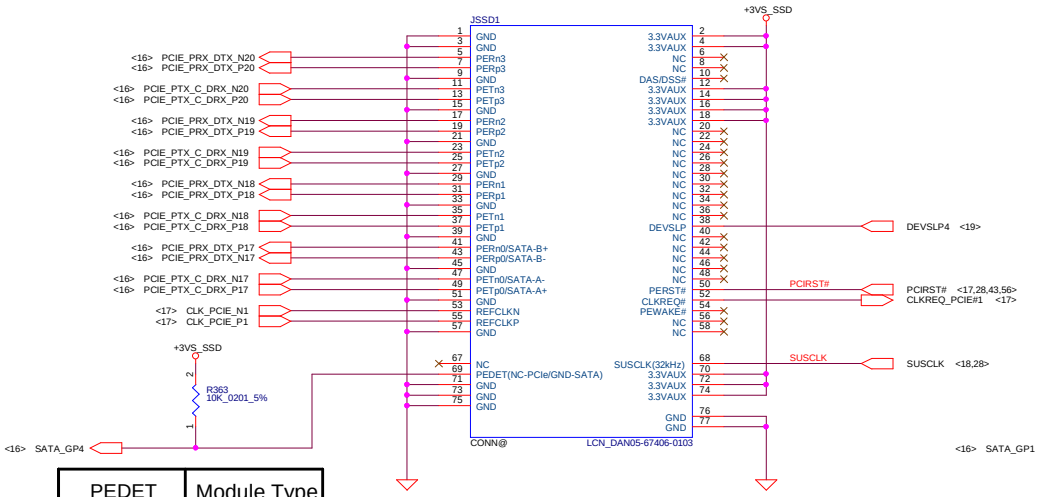
Compal Electronics, Inc.

Title: **NGFF WLAN/BT**

Size	Document Number	Rev
	LA-F551P	0.3

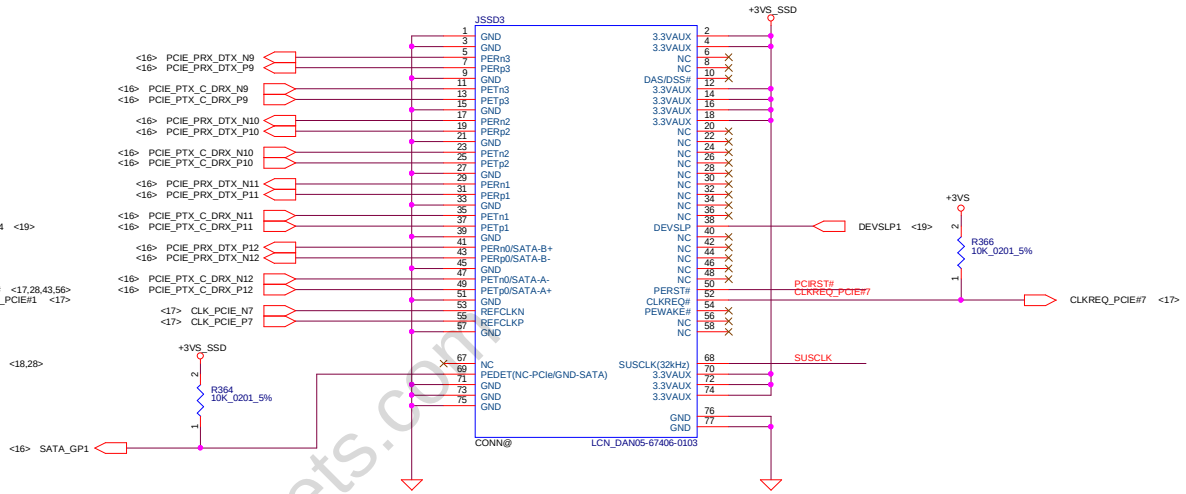
Date: Thursday, February 08, 2018 | Sheet 28 of 82

PCIe / SATA SSD
JSSD1 , 2242

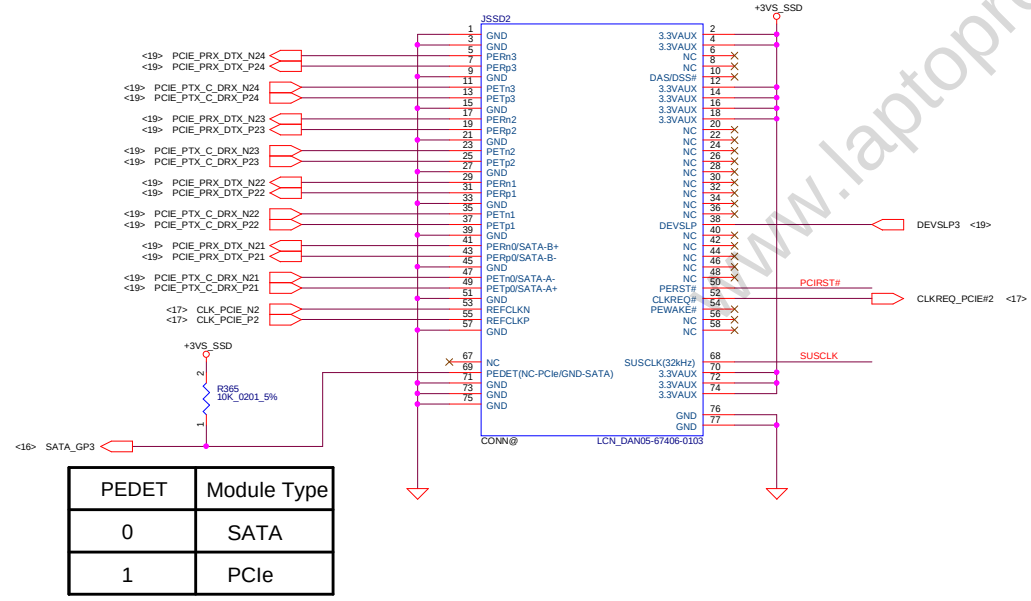


PEDET	Module Type
0	SATA
1	PCIe

PCIe / SATA SSD
JSSD3 , 2280

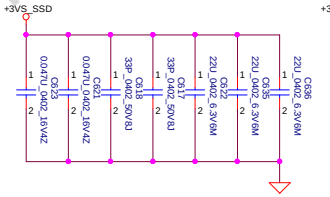


PCIe SSD
JSSD2 , 2280

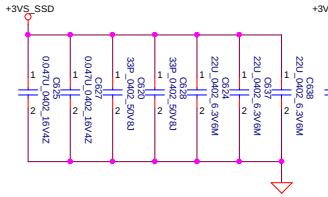


PEDET	Module Type
0	SATA
1	PCIe

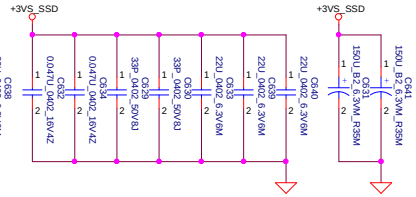
JSSD1

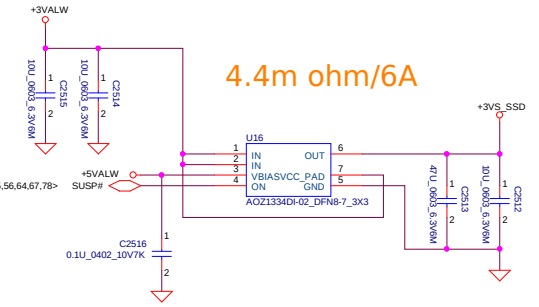


JSSD2



JSSD3





Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **NGFF SSD**

Size: | Document Number: **LA-F551P** | Rev: 0.3

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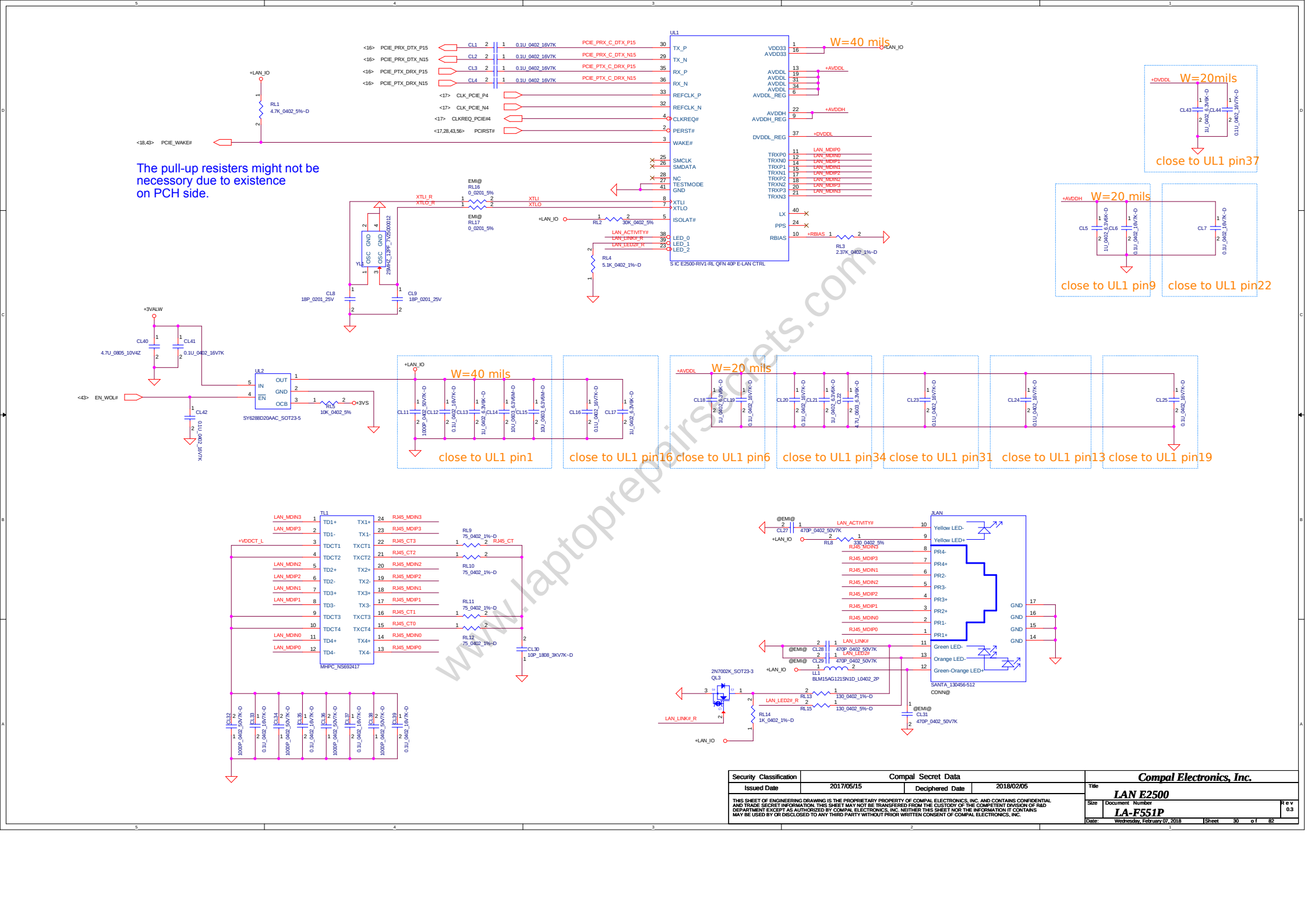
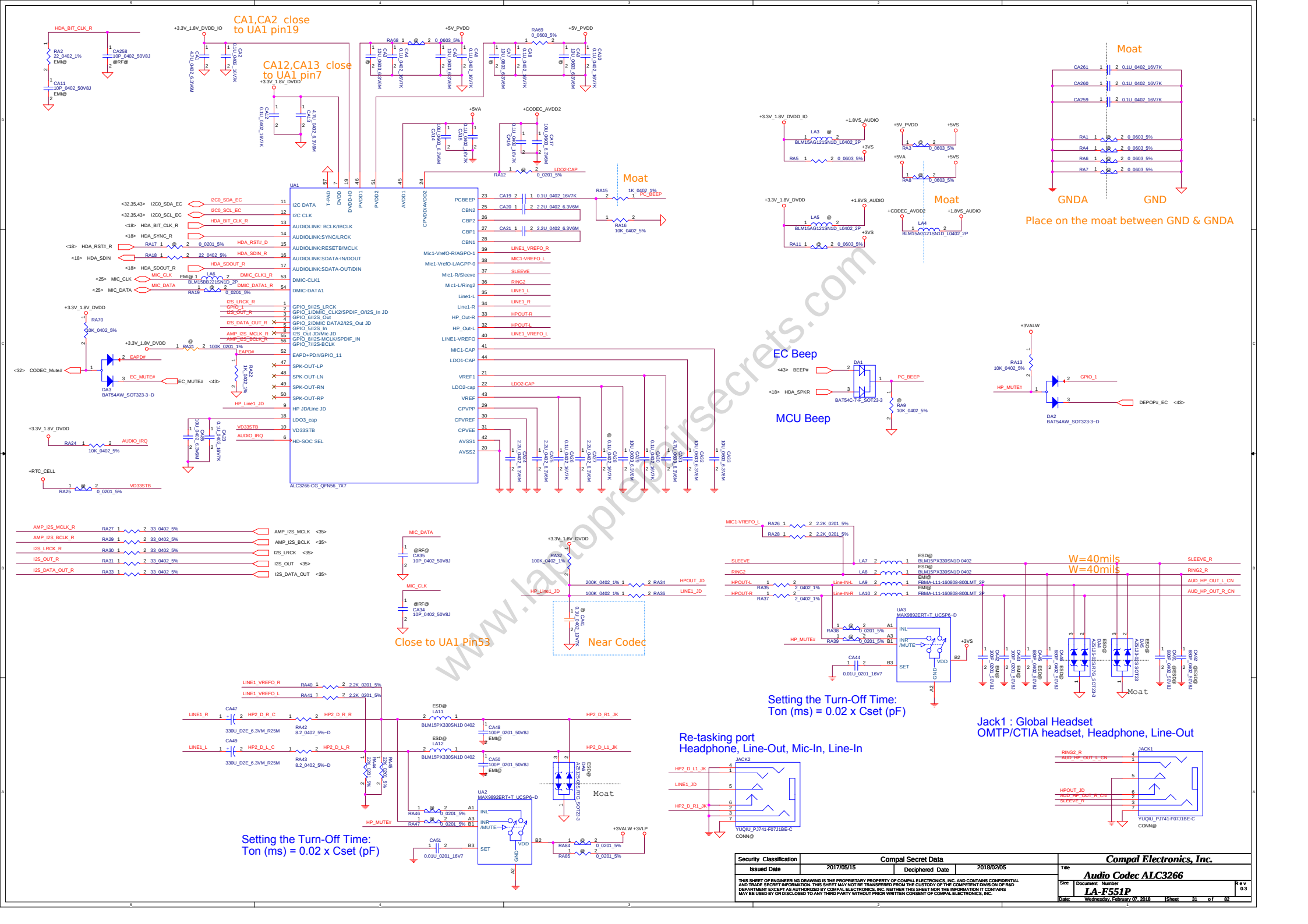
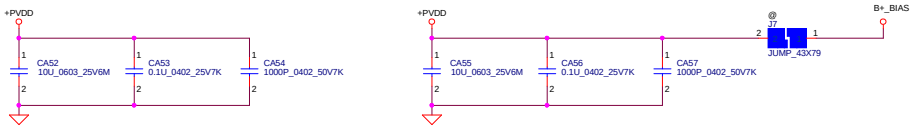
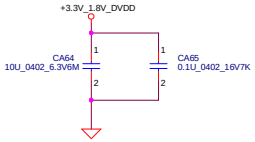




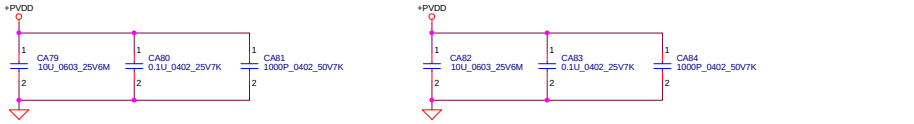


CA52, CA53 and CA54 close to PIN1,56

CA55, CA56 and CA57 close to PIN42,43



CA64, CA65 close to PIN16



CA79, CA80 and CA81 close to PIN51

CA82, CA83 and CA84 close to PIN48

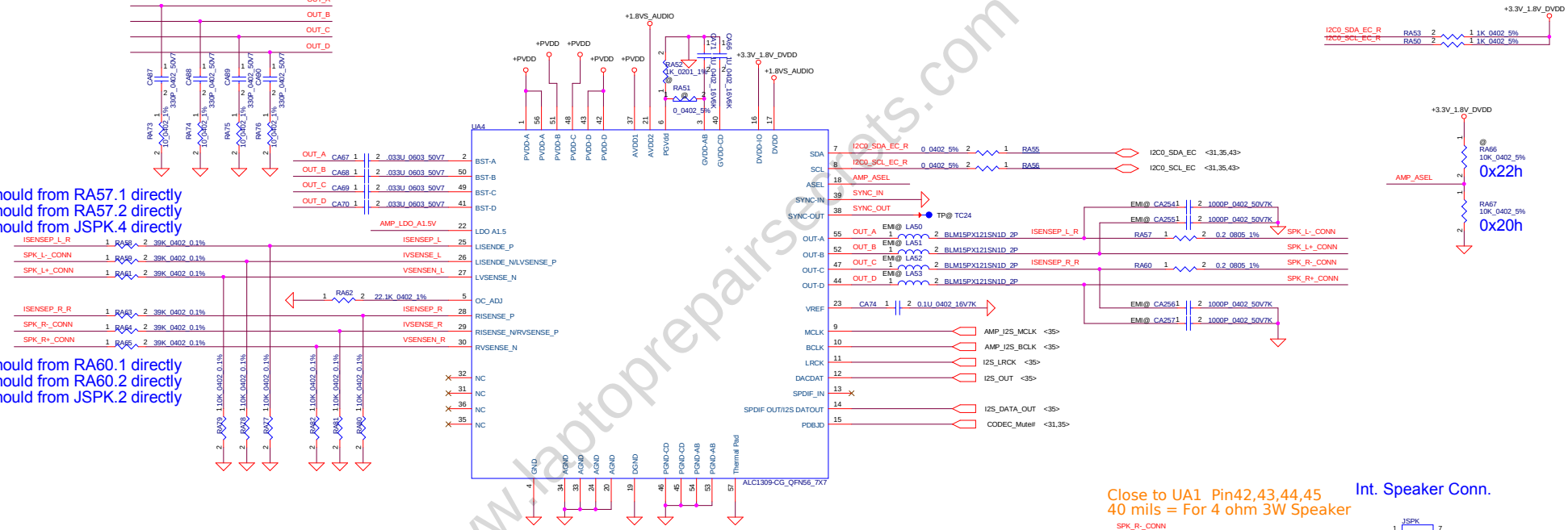
CA58, CA59 close to PIN17

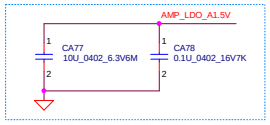
CA60 close to PIN21

CA61, CA62 and CA63 close to PIN37

RA58.1 should from RA57.1 directly
RA59.1 should from RA57.2 directly
RA61.1 should from JSPK.4 directly

RA63.1 should from RA60.1 directly
RA64.1 should from RA60.2 directly
RA65.1 should from JSPK.2 directly

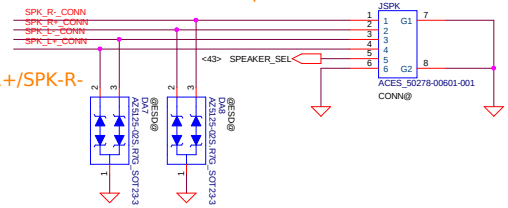




CA77, CA78 close to PIN22

Close to UA1 Pin42,43,44,45
40 mils = For 4 ohm 3W Speaker

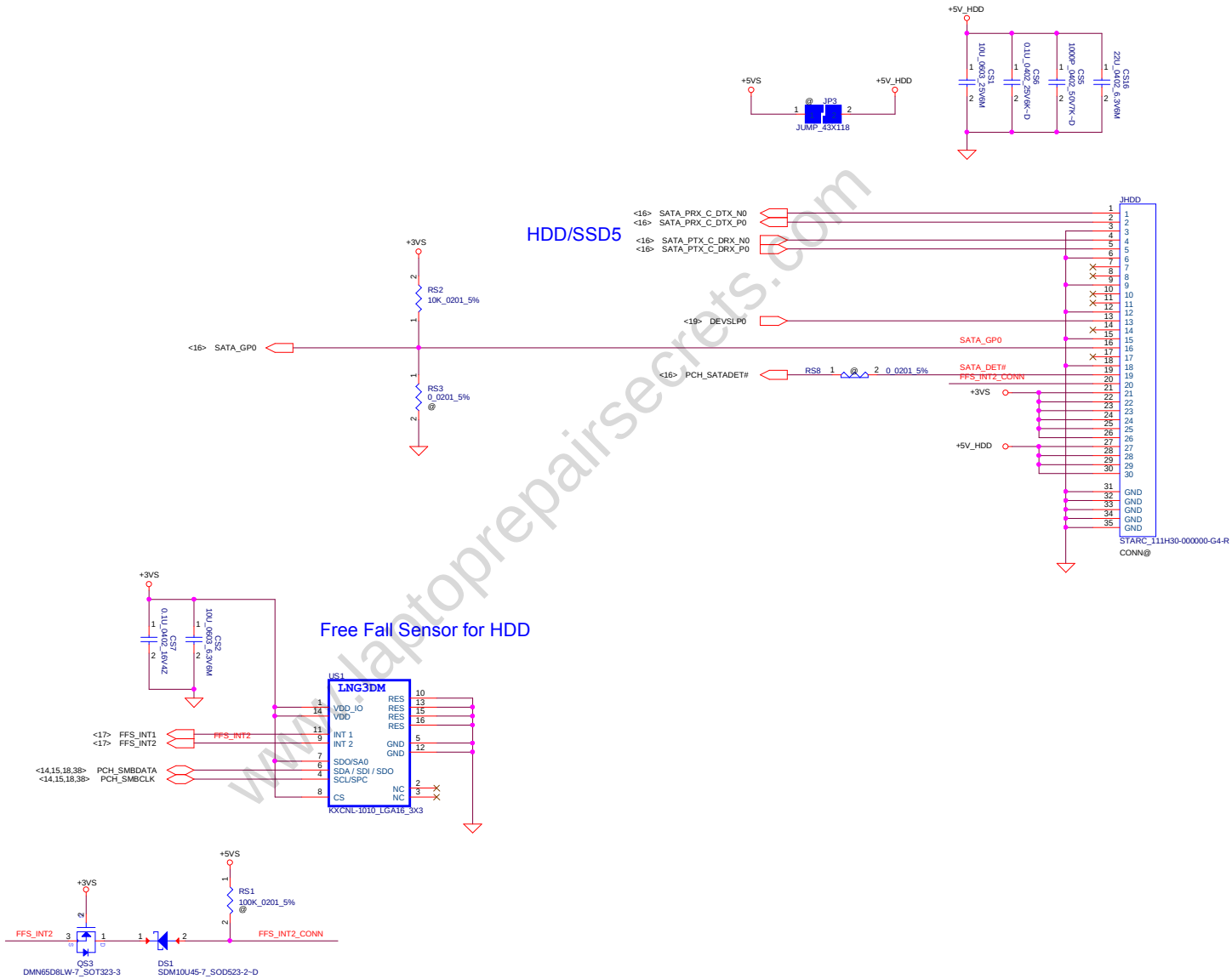
Int. Speaker Conn.



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40 mil
Speaker 8 ohm : 20 mil

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	Audio Amplifier ALC1309		
Size	Document Number		Rev
	LA-F551P		0.3
Date:	Wednesday, February 07, 2018	Sheet	32 of 82



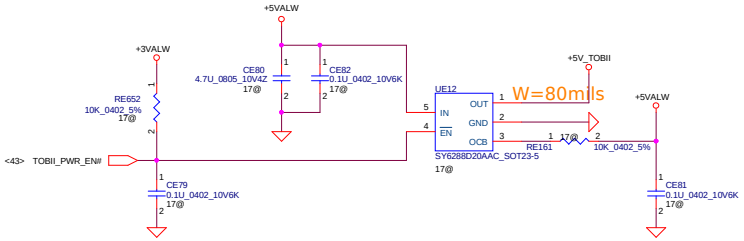
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

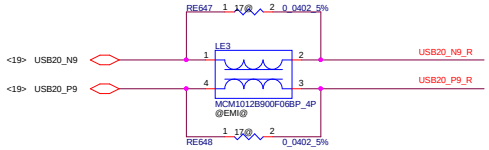
Title: **SATA HDD Connector**

Size	Document Number	Rev
	LA-F551P	0.3

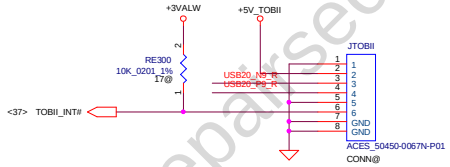
Date: Thursday, February 08, 2018 | Sheet 33 of 82



Near JTOBII



Tobii Conn.



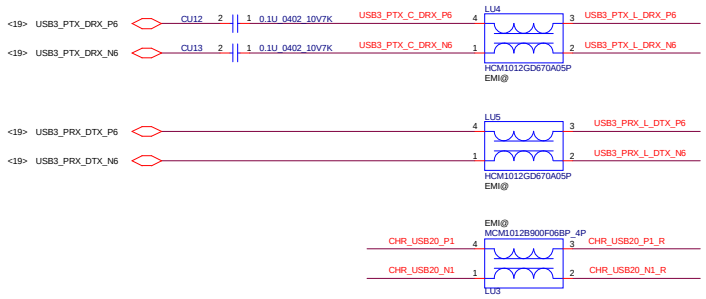
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

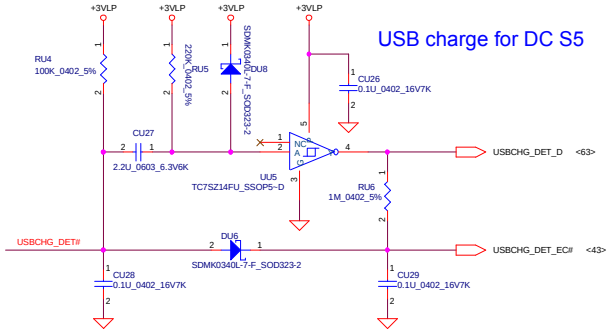
Compal Electronics, Inc.

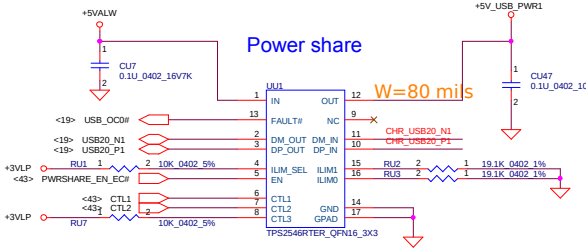
Title: **Tobii (17" Only)**

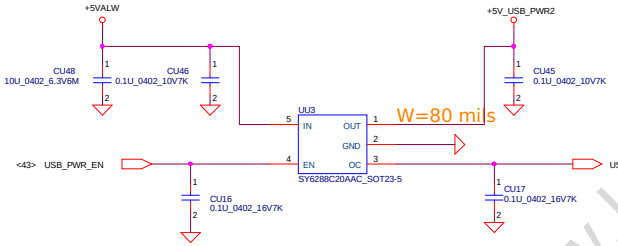
Size | Document Number: **LA-F551P** | Rev: 0.3

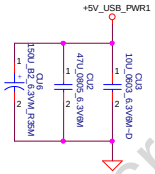
Date: Wednesday, February 21, 2018 | Sheet 34 of 82

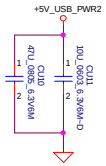


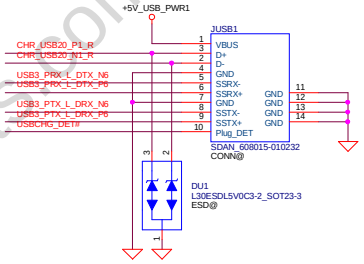


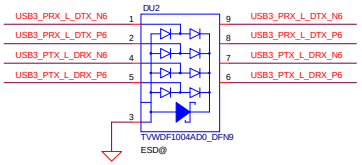


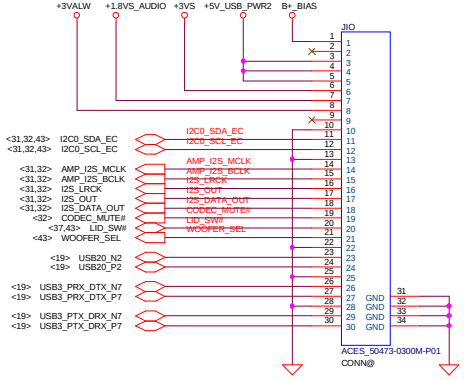












Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	USB3.0/2.0 (TypeA+IO/B)		
Size	Document Number		Rev
	LA-F551P		0.3
Date:	Wednesday, February 07, 2018	Sheet	35 of 82

Add 0.1UF close to pin 18 or 39

DCR max=0.03ohm,1A

DCR max=0.03ohm,1A

Close to Pin2,3,4

W=120 mils

Close to PinA4,A9,B4,B9

USB_SEL0 : 0
USB_SEL1 : 1
I2C ADDRESS : 0x26

Use power switch to delay the 1.8V after 3.3V

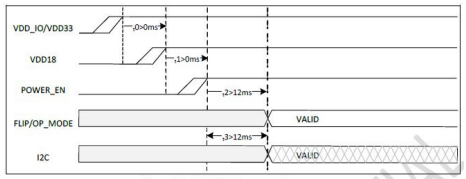


Figure 4-2 ANX7430 Power-on Sequence

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/05
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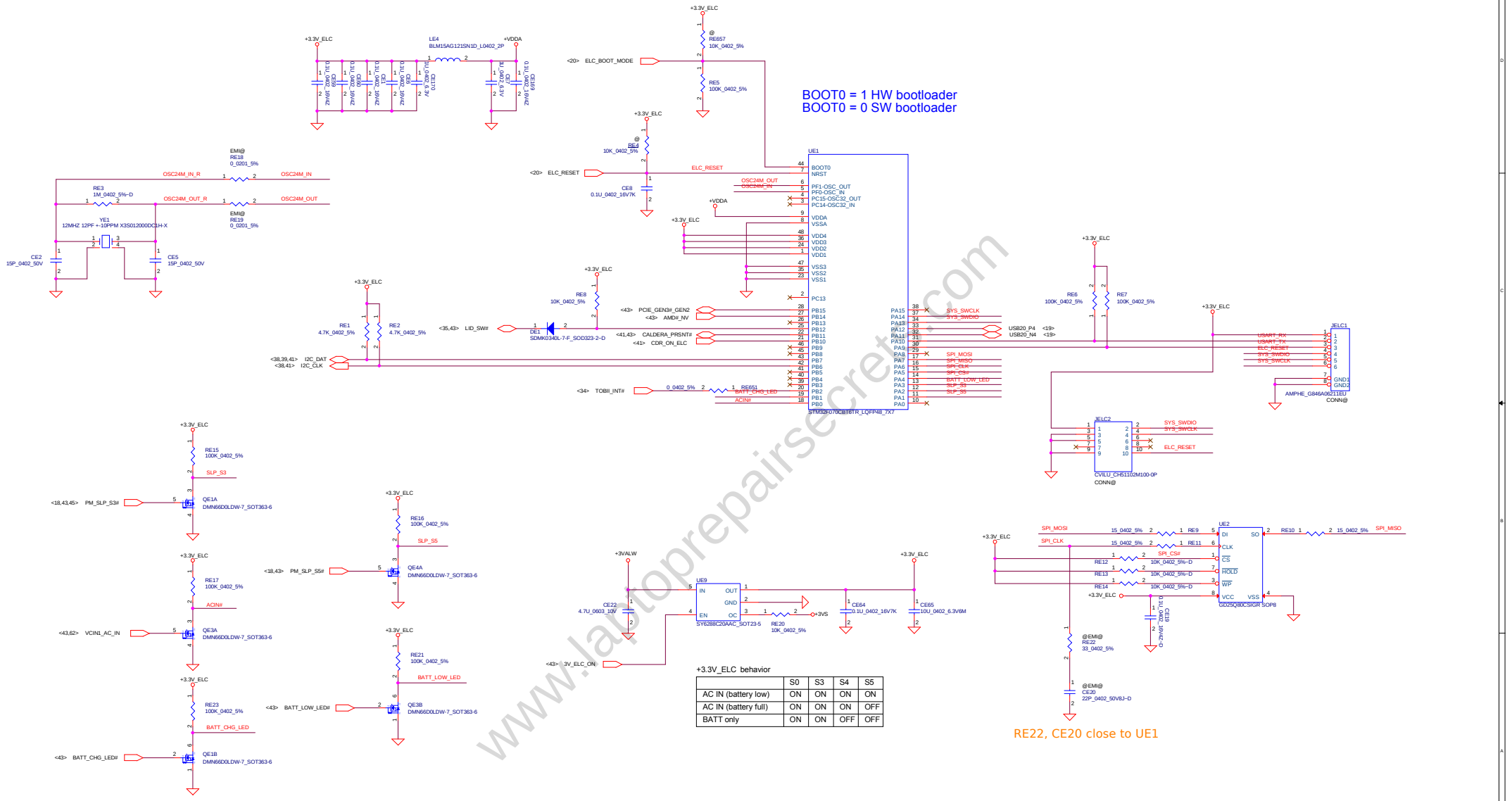
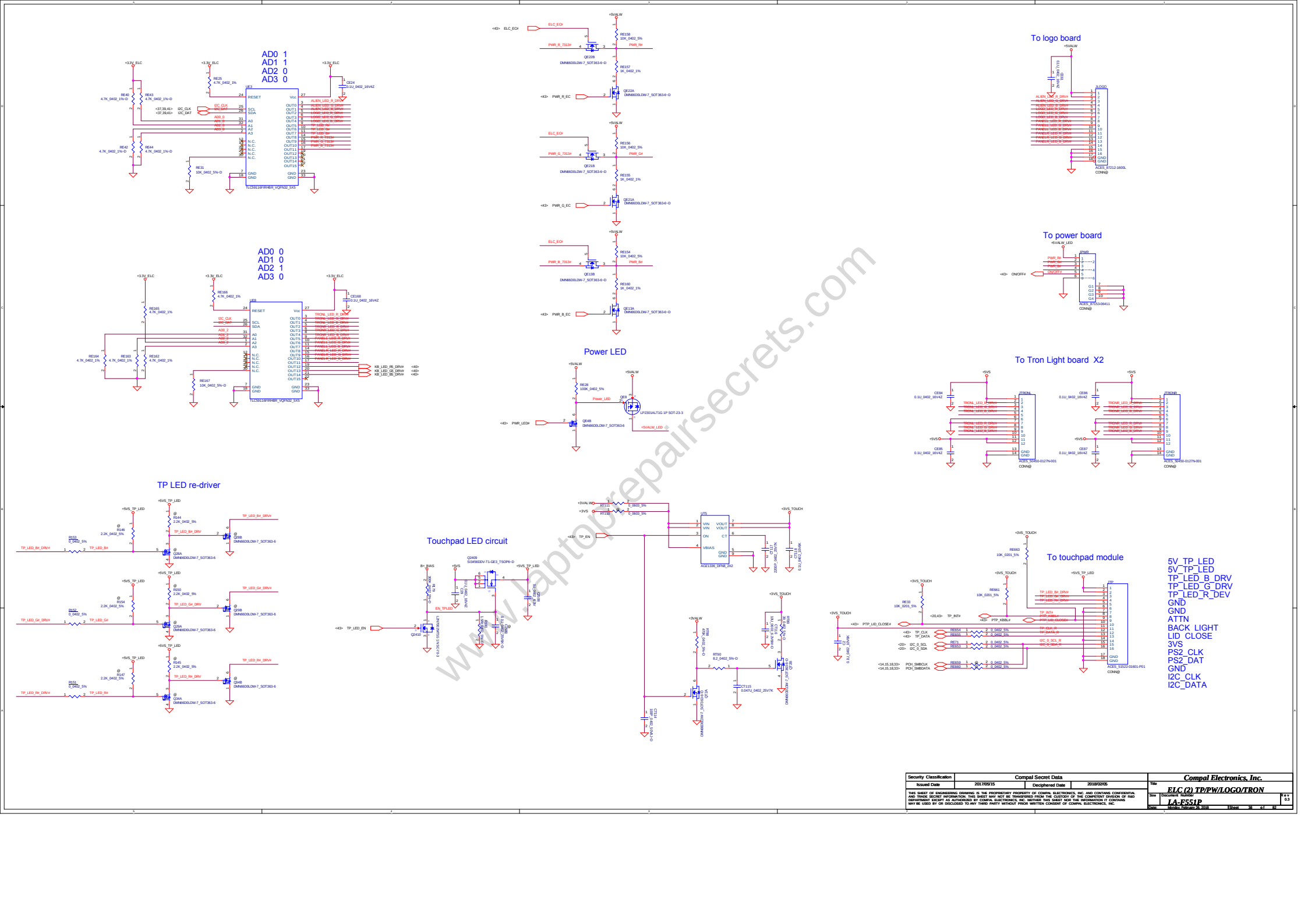
			Size: Document Number: LA-F551P Rev: 0.3
			Date: Wednesday, February 07, 2018 Sheet 36 of 82



	S0	S3	S4	S5
AC IN (battery low)	ON	ON	ON	ON
AC IN (battery full)	ON	ON	ON	OFF
BATT only	ON	ON	OFF	OFF

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.	
Title	ELC (1) STM32F070CB
Size	Document Number: LA-F551P
Rev	0.3
Date:	Tuesday, March 06, 2018
Sheet	37 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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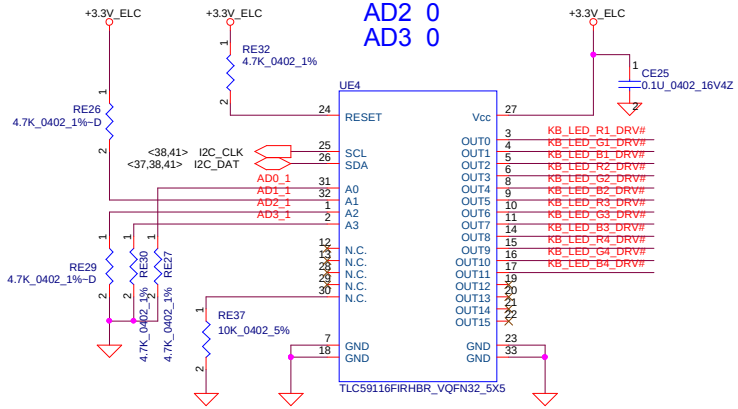
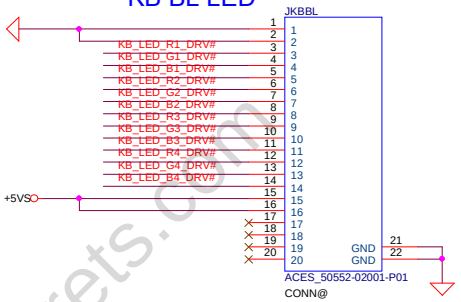
Compal Electronics, Inc.			
Title: ELC (2) TP/PW/LOGO/TRON			
Size:	Document Number: LA-F551P		Rev: 0.3
Date: Monday, February 26, 2018	Sheet 38 of 82		

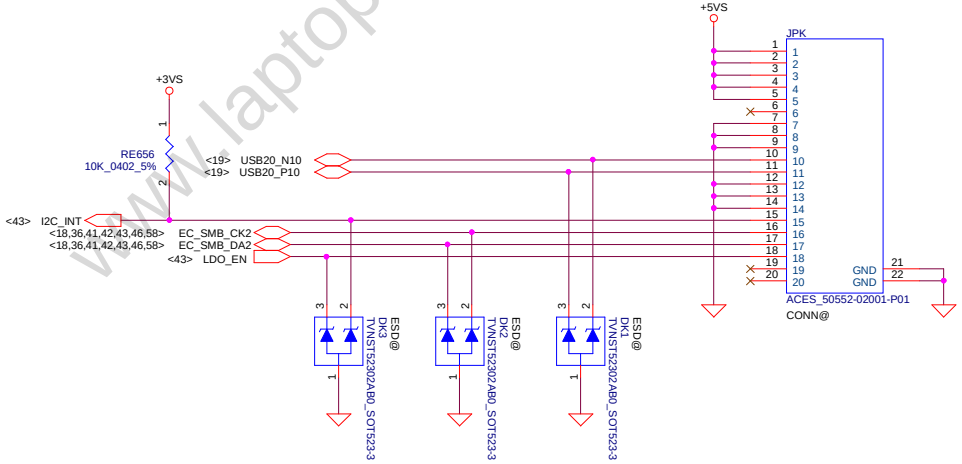
KB Backlight

AD0 0
AD1 1
AD2 0
AD3 0



KB BL LED



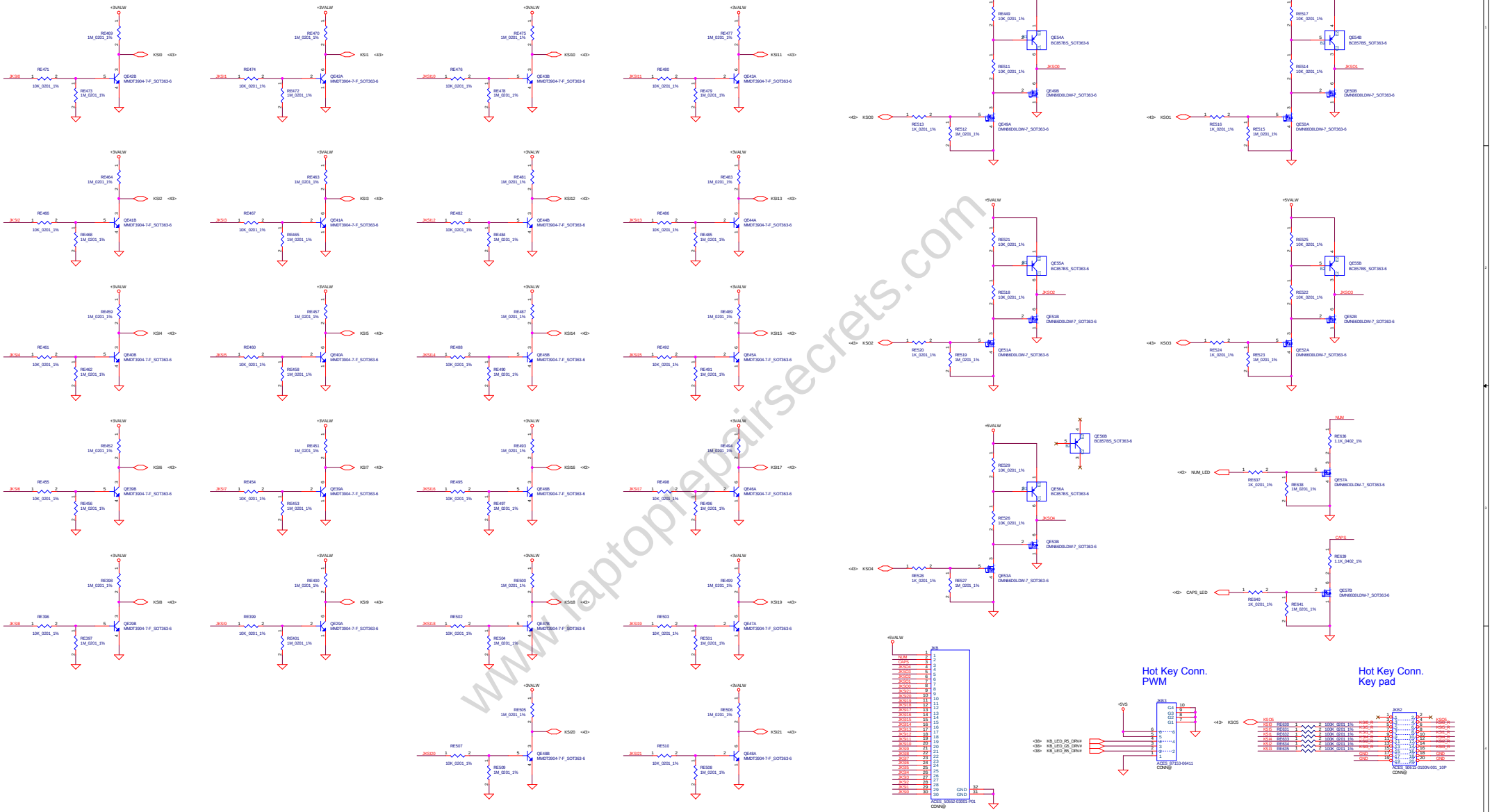


Per Key pin define

Pin1~5	VBUS
Pin6	NC
Pin7~9	GND
Pin10	D-
Pin11	D+
Pin12~14	GND
Pin15	I2C_INT
Pin16	I2C_CLK
Pin17	I2C_DAT
Pin18	LDO_EN
Pin19~20	NC

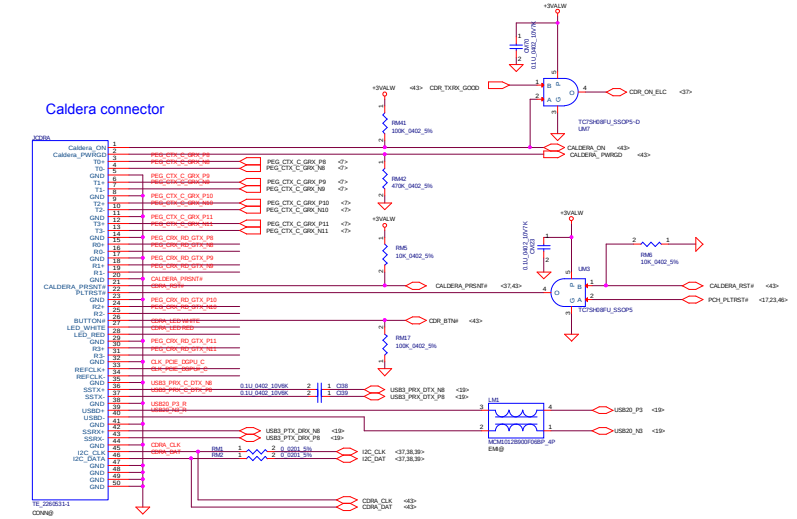
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

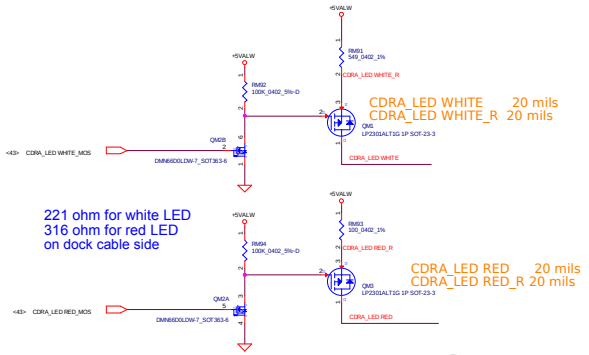
Compal Electronics, Inc.		
Title: ELC (3) KBBL/Per Key		
Size	Document Number: LA-F551P	Rev: 0.3
Date: Wednesday, February 07, 2018	Sheet 39 of 82	



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

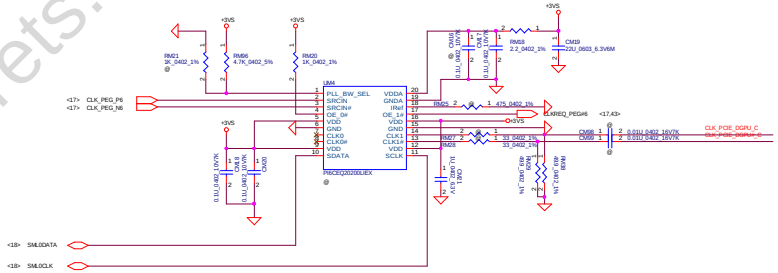
Compal Electronics, Inc.			
Title	ELC (4) NKRO KB		
Size	Document Number		Rev
	LA-F551P		0.3
Date: Wednesday, February 07, 2018	Sheet 40 of 82		

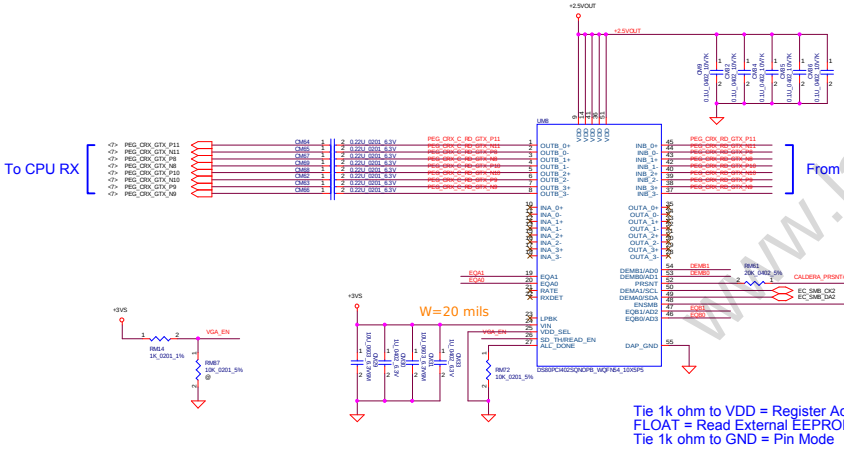


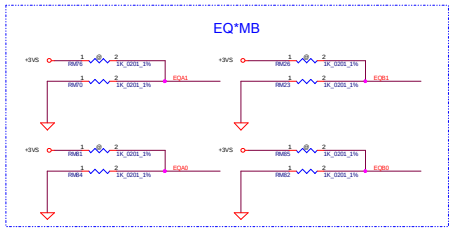


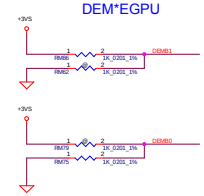
PCIe Clock Buffer	RM25	RM27 / RM28	CM16	CM98 / CM99
Pericom (SA00007J200) X7669431L7S	SD034475080 (475 +-1% 0402)	SD033433080 (33 +-1% 0402)	SE102104K00 (0.1U +-10% 0402)	SE076103K80 (.01U 16V K X7R 0402)
IDT (SA00007ZU00) X7669431L7S	SD034412080 (412 +-1% 0402)	SD000004D80 (27 +-1% 0402)	SE000001L10 (1U +-10% 0402)	SE076104K80 (.1U 16V K X7R 0402)

PCIE_CLK_BUFFER









Tie 1k ohm to VDD = Register Access SMBus Slave mode
FLOAT = Read External EEPROM (Master SMBUS Mode)
Tie 1k ohm to GND = Pin Mode

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	Caldera Docking		
Size	Document Number		Rev
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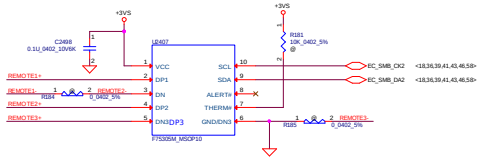
Date: Thursday, February 08, 2018	Sheet 41 of 82		

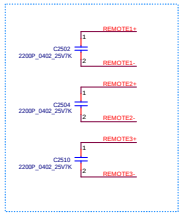
Fintek thermal sensor---> CPU core, DIMM

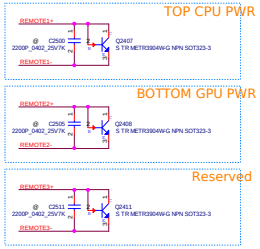


Address 1001_101xb

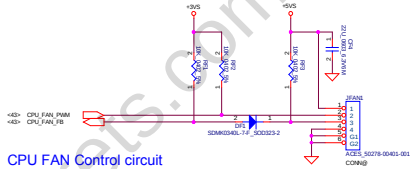
2nd source
SA000029210-->EMC1403-2-AIZL-TR

Close U2407

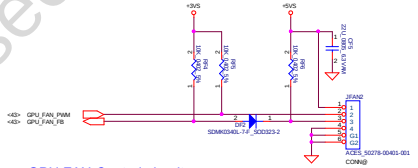




REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



CPU FAN Control circuit



GPU FAN Control circuit

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title	FAN/Thermal		
Size	Document Number		Rev 0.3
	LA-F551P		
Date: Thursday, February 08, 2018	Sheet 42 of 82		

Power ON circuit

Reserve for abnormal shutdown

EVT	00.SD028000080	0_0402_5%
EVT-2	01.SD034120280	12K_0402_1%
DVT-1	02.SD034150280	15K_0402_1%
DVT-2	03.SD028200280	20K_0402_5%
PVT	04.SD034270280	27K_0402_1%
	05.SD034330280	33K_0402_1%
	06.SD034430280	43K_0402_1%
	07.SD034560280	56K_0402_1%
	08.SD034750280	75K_0402_1%
	09.SD034100380	100K_0402_1%
	10.SD034130380	130K_0402_1%
	11.SD034160380	160K_0402_1%
	12.SD034200380	200K_0402_1%
	13.SD000001B80	240K_0402_1%
	14.SD00000G280	270K_0402_1%
	15.SD034330380	330K_0402_1%
	16.SD028430380	430K_0402_5%
	17.SD034560380	560K_0402_1%
	18.SD00000AL80	750K_0402_1%

RES 1/16W 27K +-1% 0402 SD034270280

W=20 mils

W=60 mils

Please close to EC

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

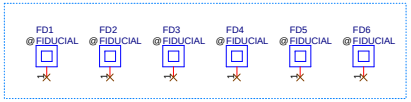
Compal Electronics, Inc.

Title: **EC ENE-KB9022**

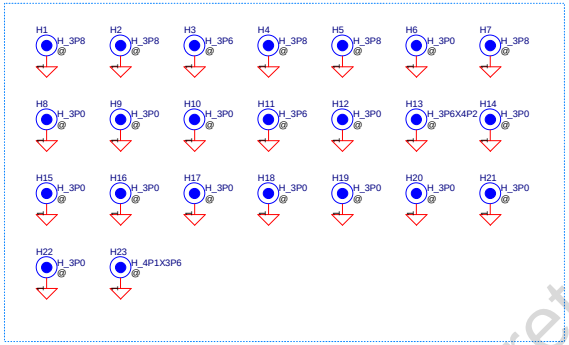
Size: | Document Number: **LA-F551P** | Rev: 0.3

Date: Monday, February 26, 2018 | Sheet 43 of 82

Fiducial Mark



PCB Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

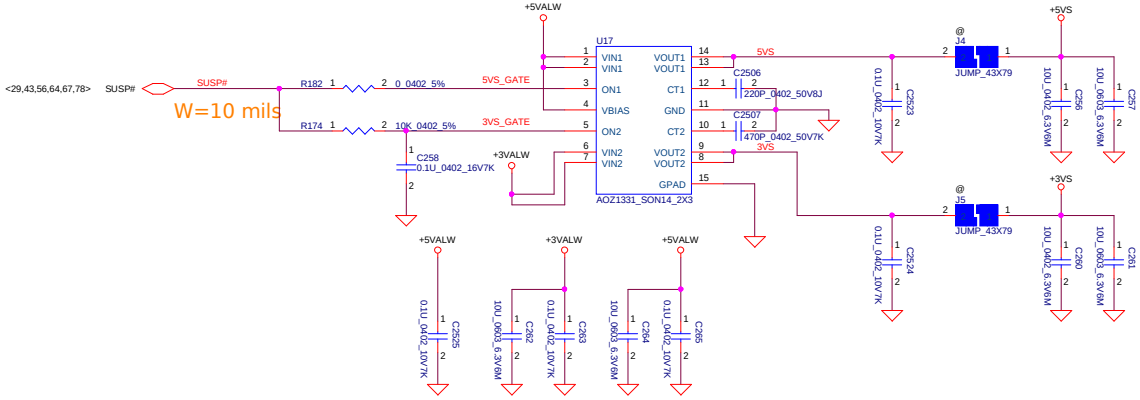
Compal Electronics, Inc.

Title: **Screw Hole**

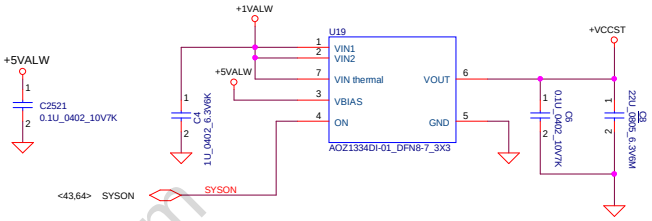
Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 44 of 82

+5VS and +3VS switch
20mohm/6A per channel

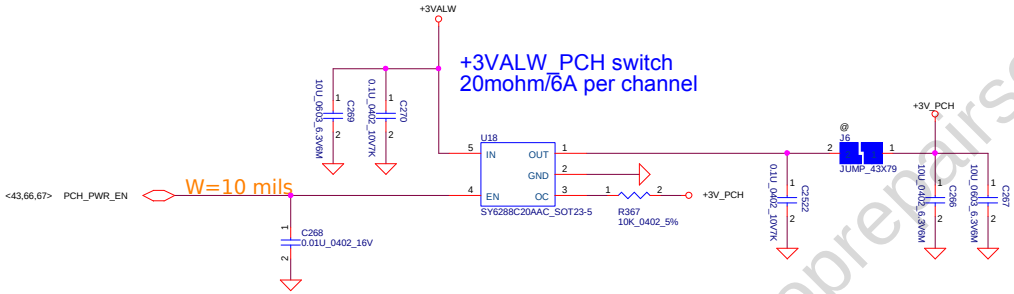


+VCCST switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

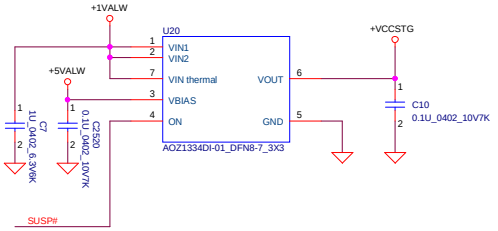


Main source M AOS SA00008A800 M SIMOM1334 MM MOF N 8P SMM M OAM S MM
2nd source M APMM SA00006V300 MSAPM8232 MN3MF N 8P M OAM S MM TM2M
3rd source M M MM SA00008R600 MSIM5201W F N333 8P M OAM S MM TM2M

+3VALW_PCH switch
20mohm/6A per channel



+VCCSTG switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

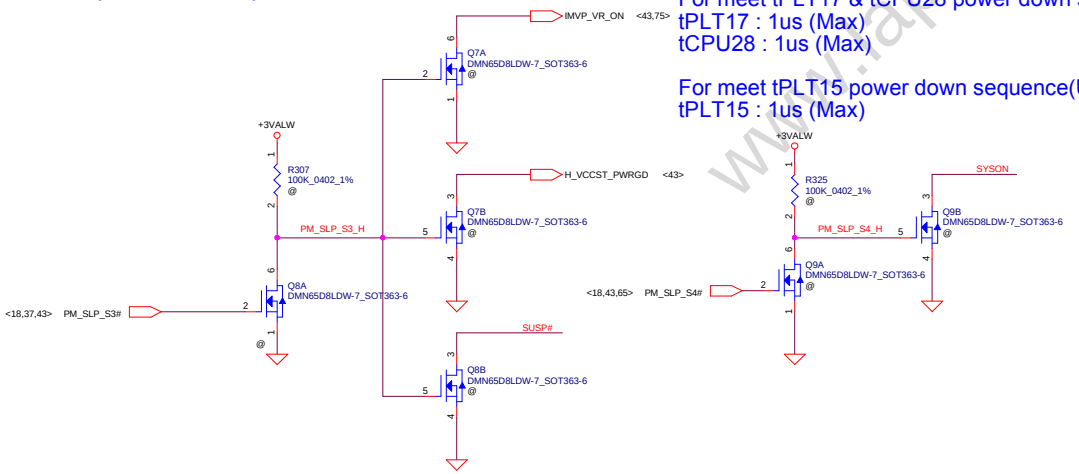


Main source M AOS SA00008A800 M SIMOM1334 MM MOF N 8P SMM M OAM S MM
2nd source M APMM SA00006V300 MSAPM8232 MN3MF N 8P M OAM S MM TM2M
3rd source M M MM SA00008R600 MSIM5201W F N333 8P M OAM S MM TM2M

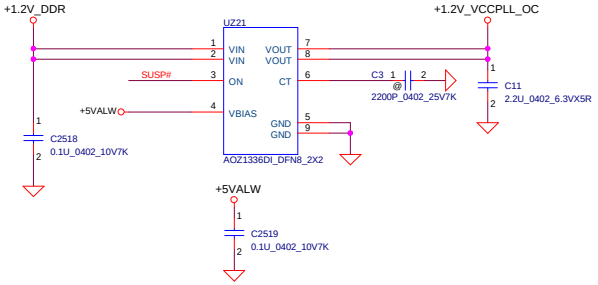
add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuff)
tPLT15 : 1us (Max)



+1.2V_VCCPLL_OC switch
22mohm/4A
TR=520us@Vin=0.8V



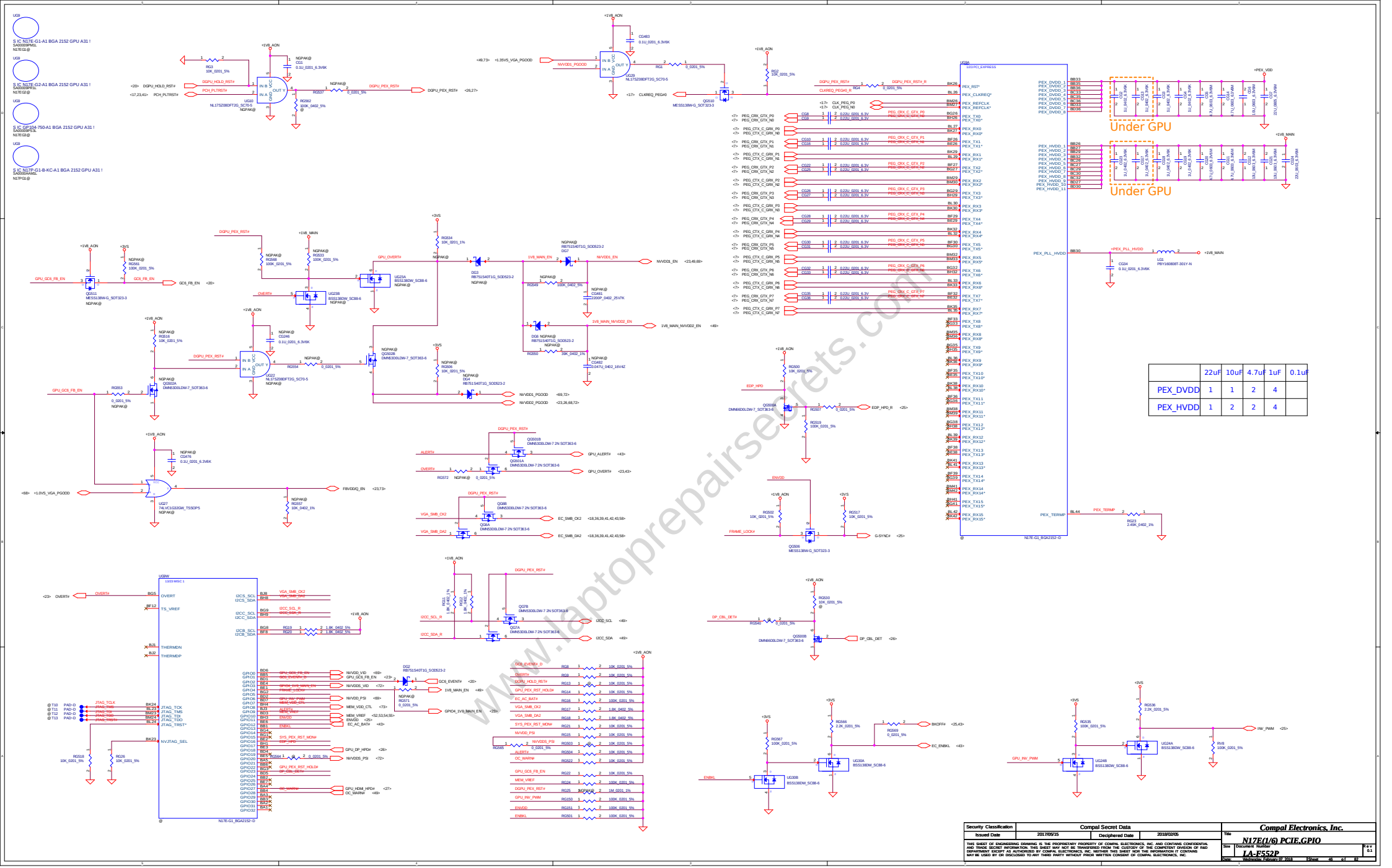
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: DC/DC Interface

Size | Document Number: LA-F551P | Rev: 0.3

Date: Thursday, February 08, 2018 | Sheet 45 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/05/15	Deciphered Date	2018/02/05
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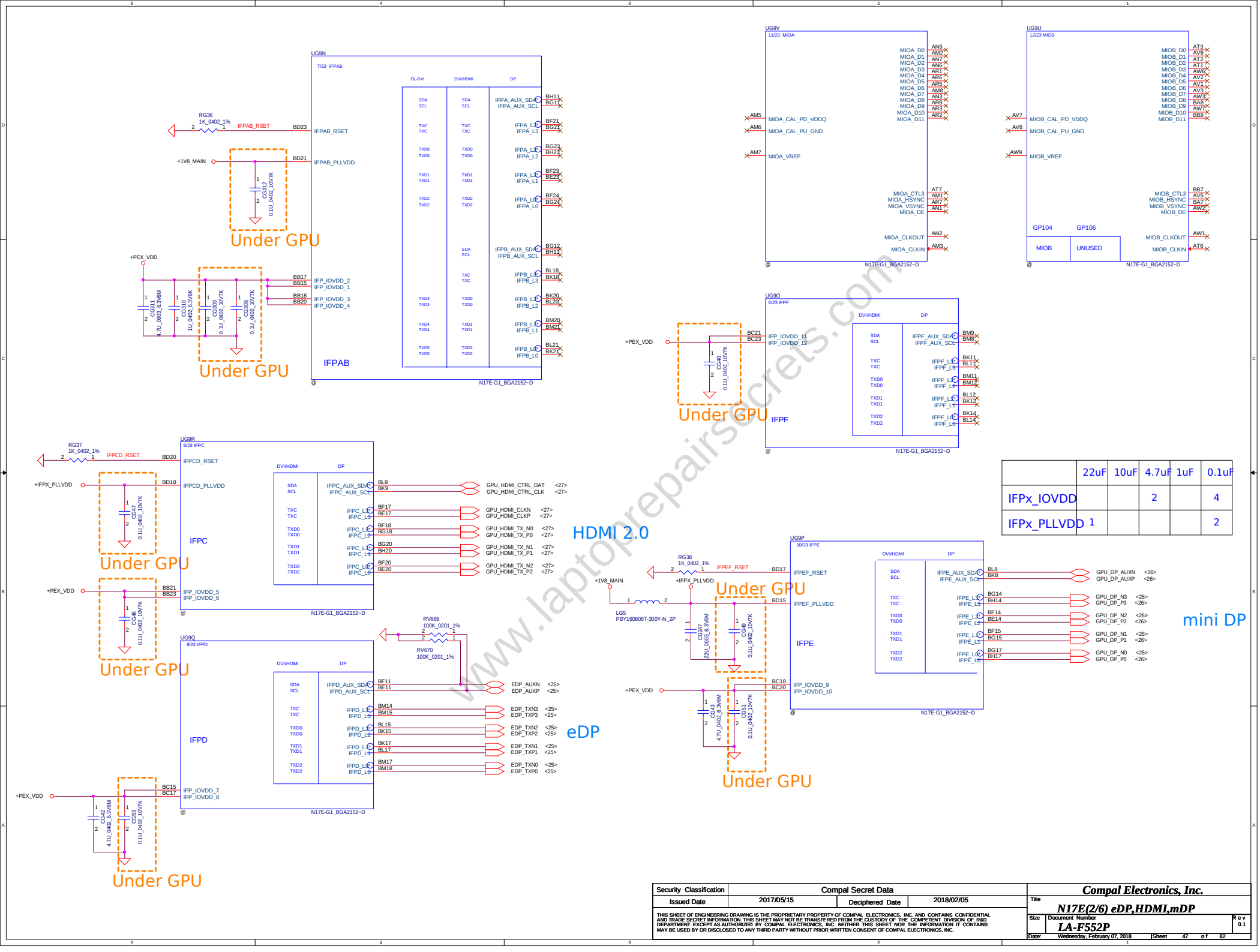
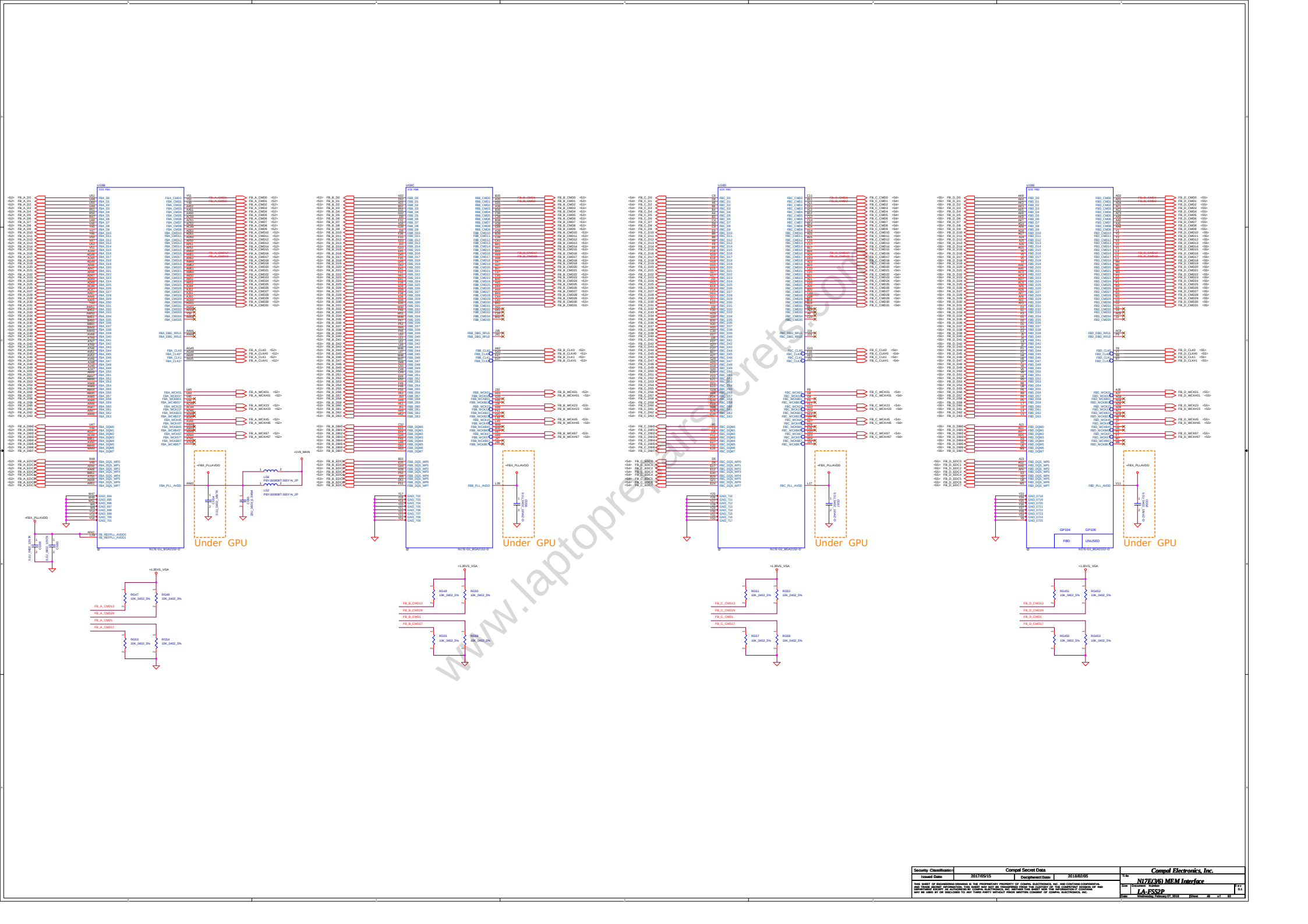
			Size: Document Number: LA-F552P Rev: 0.1
			Date: Wednesday, February 07, 2018 Sheet 46 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			2		4
IFPx_PLLVDD	1				2

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.	
Title	N17E(2/6) eDP,HDMI,mDP
Size	Document Number: LA-F552P
Rev	0.1
Date:	Wednesday, February 07, 2018
Sheet	47 of 82



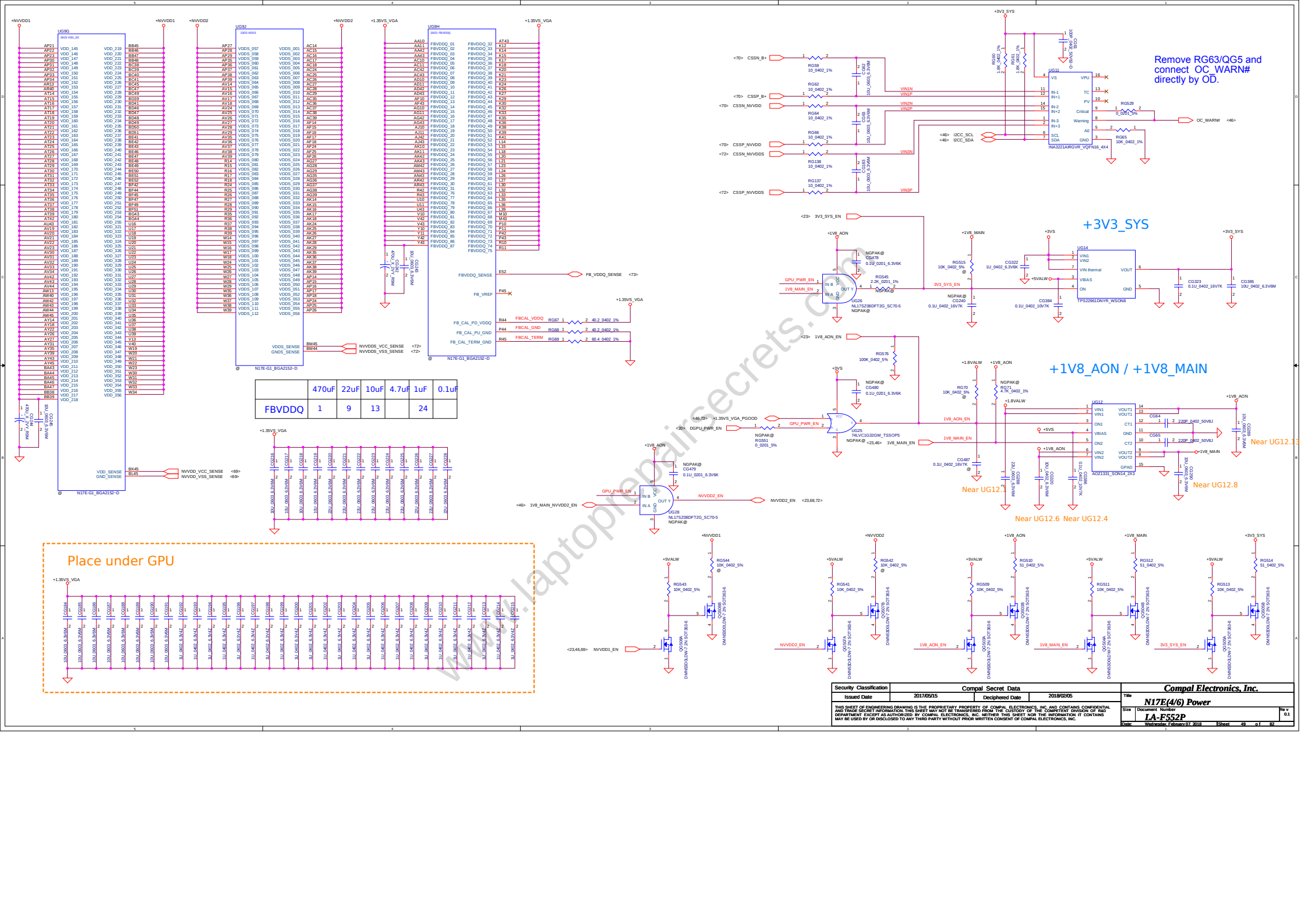
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: N17E(3/6) MEM Interface

Size	Document Number	Rev
	LA-F552P	0.1

Date: Wednesday, February 07, 2018 Sheet 46 of 82



	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ	1	9	13		24	

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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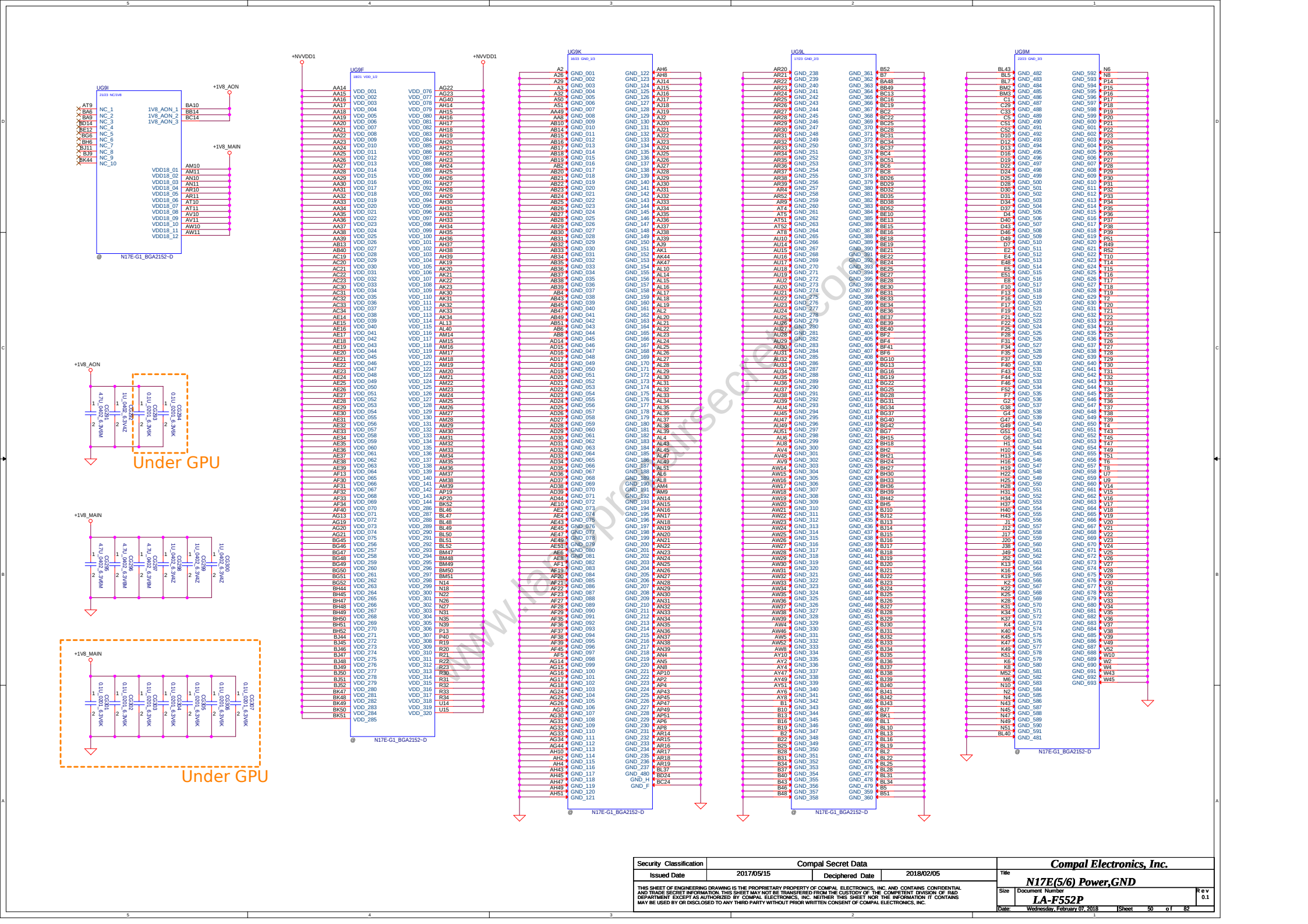
Compal Electronics, Inc.

Title: N17E(4/6) Power

Size: | Document Number: IA-F552P | Rev: 0.1

Date: Wednesday, February 07, 2018 | Sheet 49 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

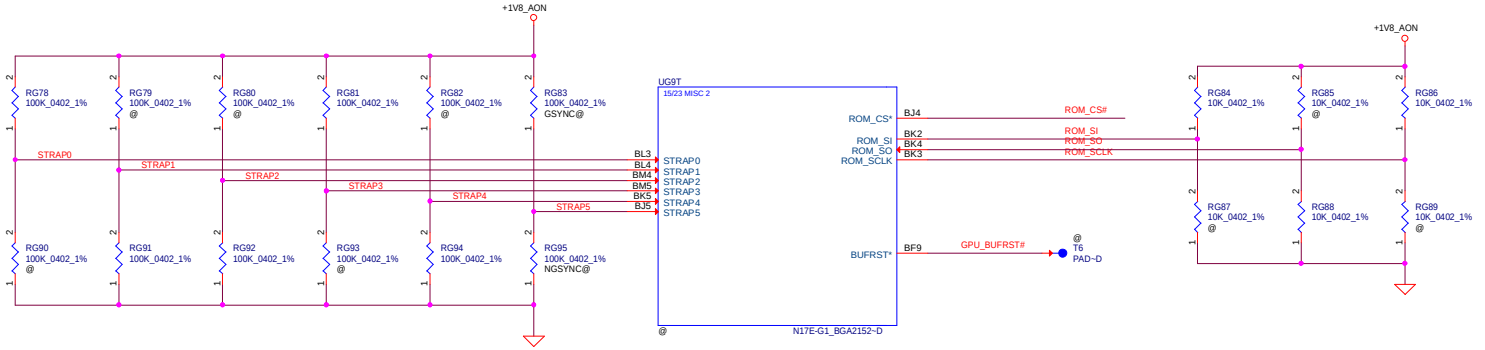
Compal Electronics, Inc.

Title: **N17E(5/6) Power,GND**

Size	Document Number	Rev
	LA-F552P	0.1

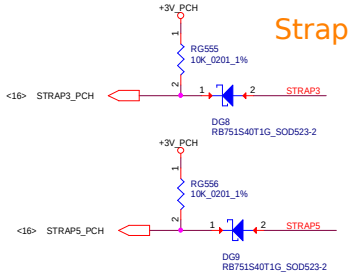
Date: Wednesday, February 07, 2018 | Sheet 50 of 82

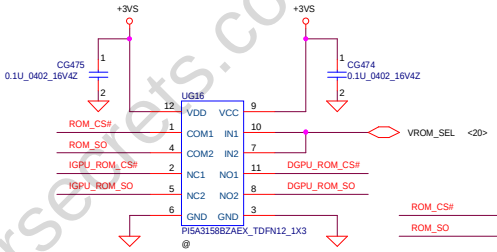
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD GPCPLL_AVDD		1				6



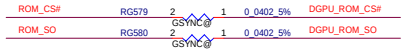
GDDR5x VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
Micron , MT58K256M32JA-100:A	L	L	L	H	L		0
Micron , MT58K256M321JA-100:A	H	L	L	H	L		1

Strap to PCH

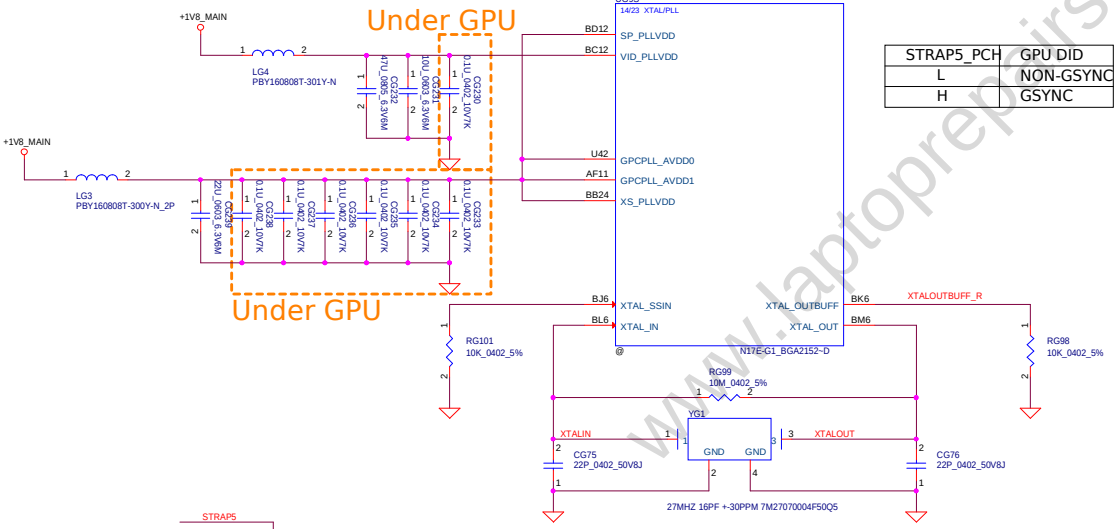




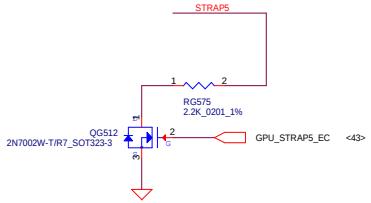
Funct on	VROM_SEL	VBIOS
COM = NC	L	NON-GSYNC
COM = NO	H	GSYNC

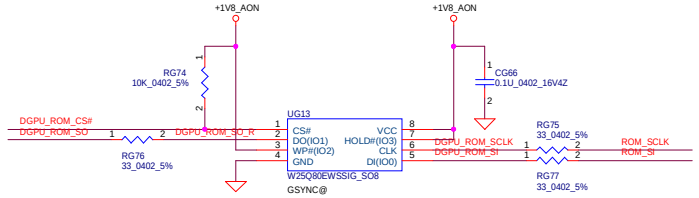


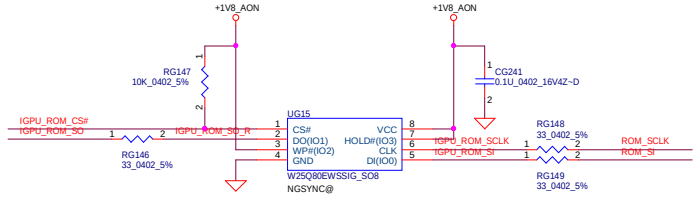
Under GPU



STRAP5_PCH	GPU DID
L	NON-GSYNC
H	GSYNC







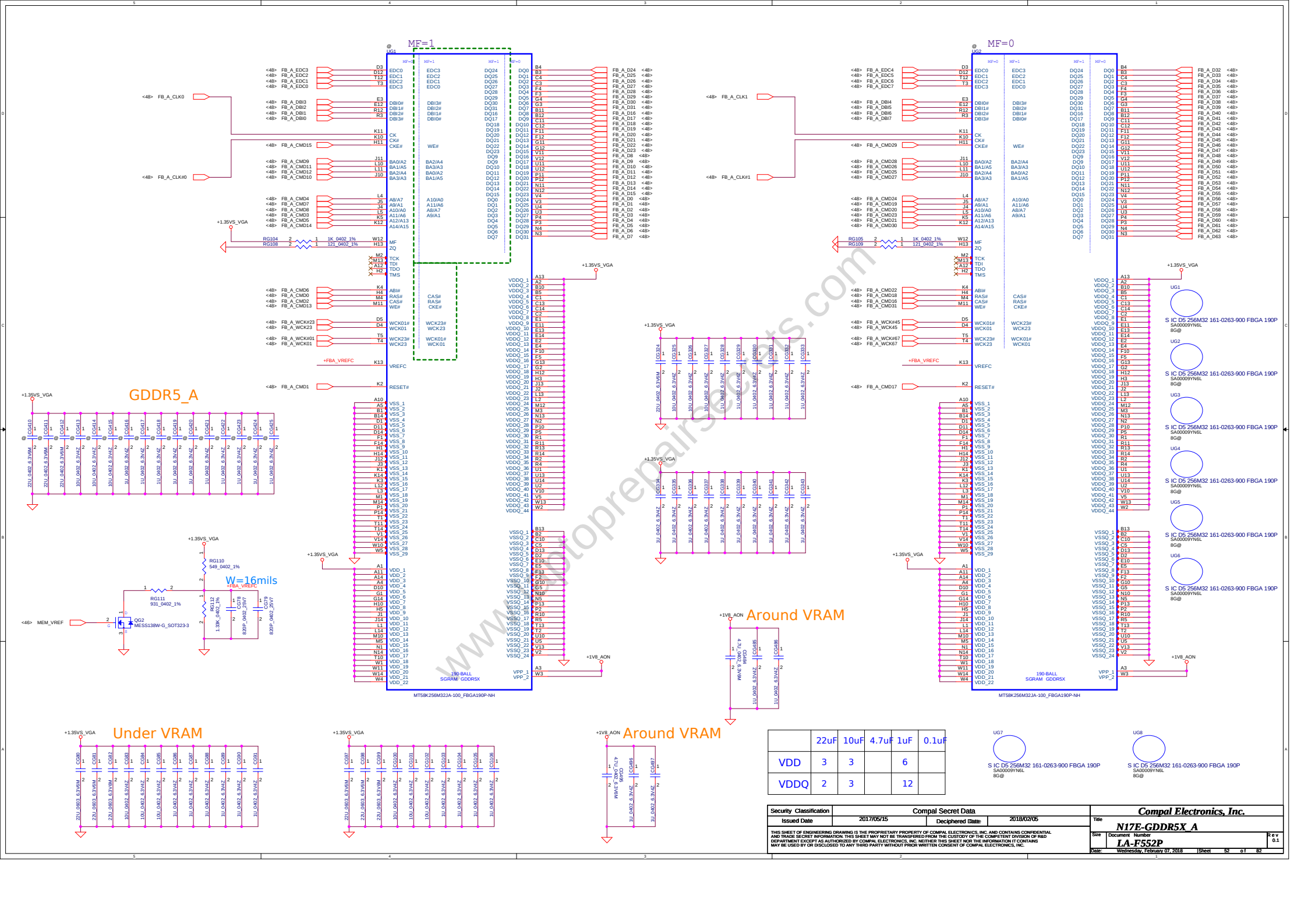
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: N17E(6/6) Strap Pin,ROM

Size	Document Number	Rev
	LA-F552P	0.1

Date: Wednesday, February 07, 2018 Sheet 51 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	2	3		12	

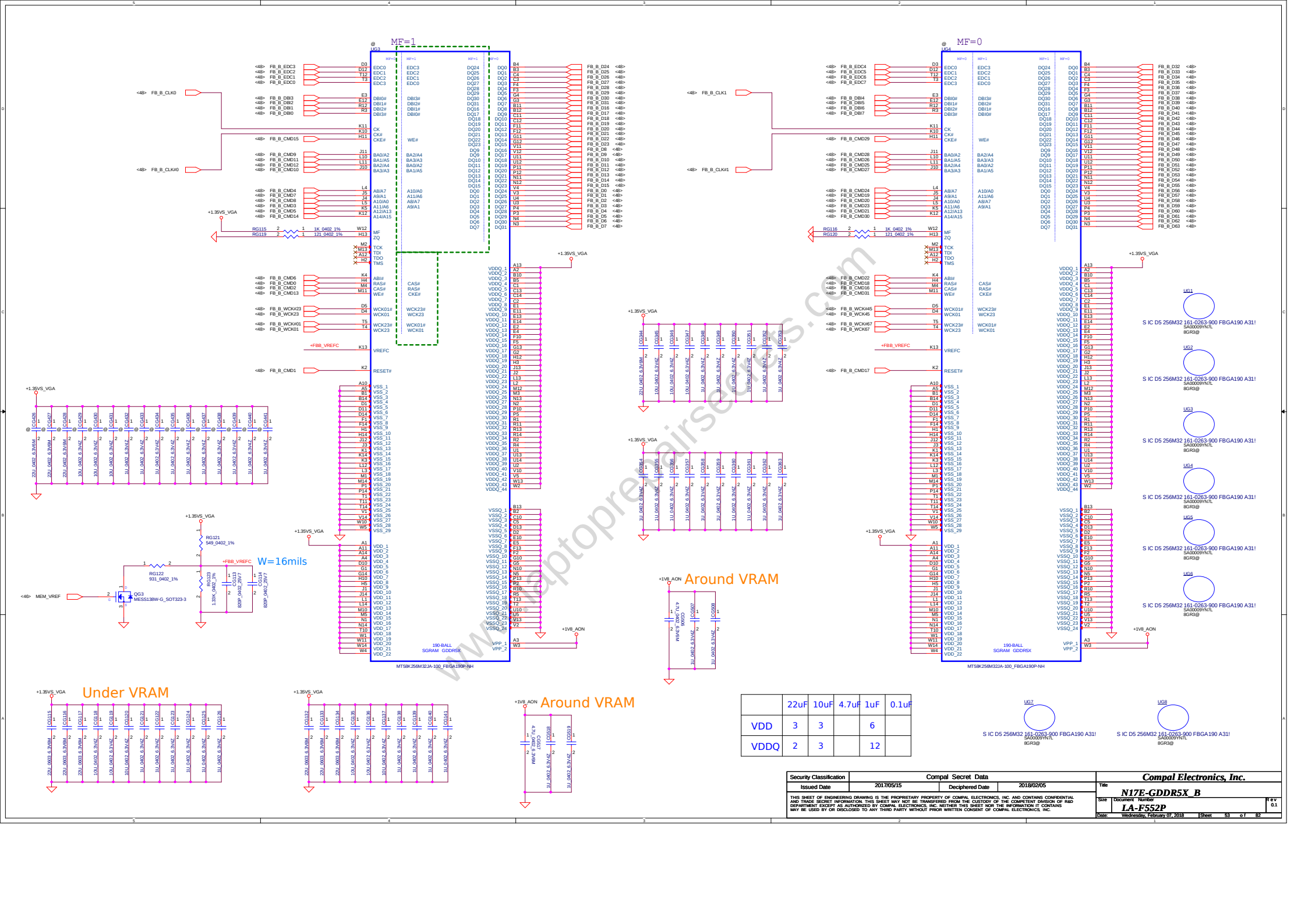
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **N17E-GDDR5X_A**

Size: | Document Number: **LA-F552P** | Rev: 0.1

Date: Wednesday, February 07, 2018 | Sheet 52 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	2	3		12	

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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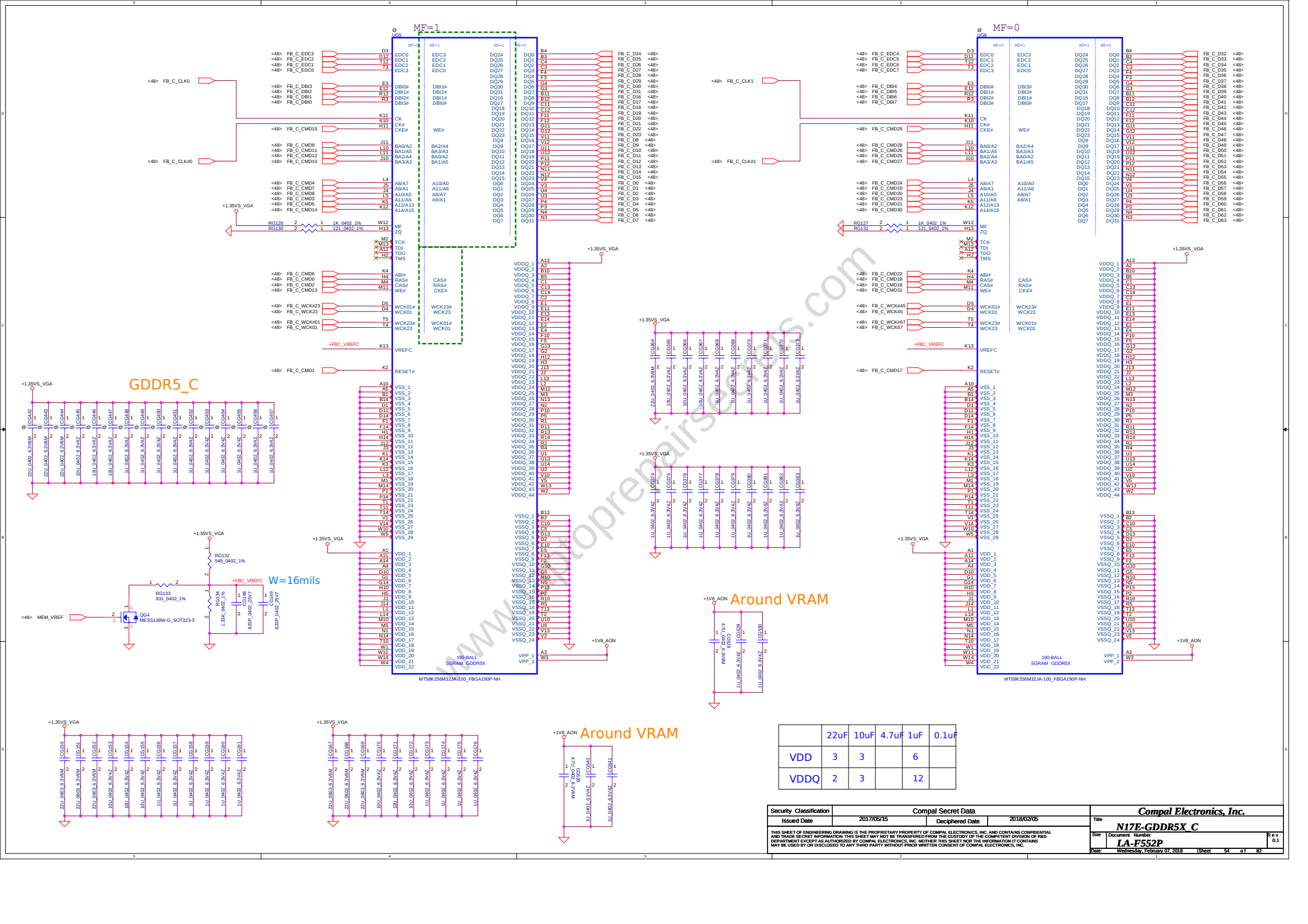
Compal Electronics, Inc.

Title: N17E-GDDR5X_B

Size: | Document Number: LA-F552P | Rev: 0.1

Date: Wednesday, February 07, 2018 | Sheet 53 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	2	3		12	

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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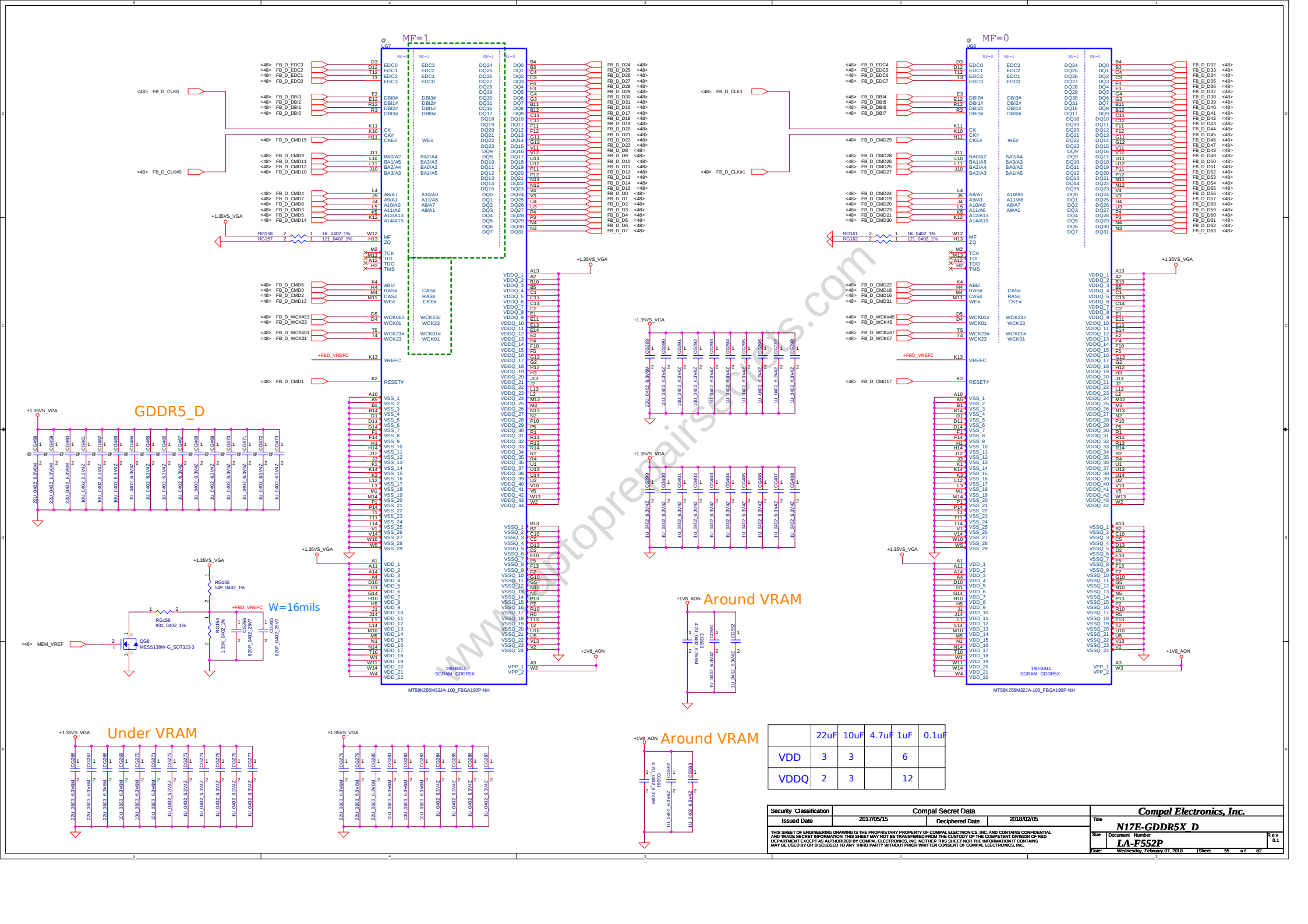
Compal Electronics, Inc.

Title: **N17E-GDDR5X_C**

Size: — Document Number: **LA-F552P** — Rev: 0.1

Date: Wednesday, February 07, 2018 — Sheet 54 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	2	3		12	

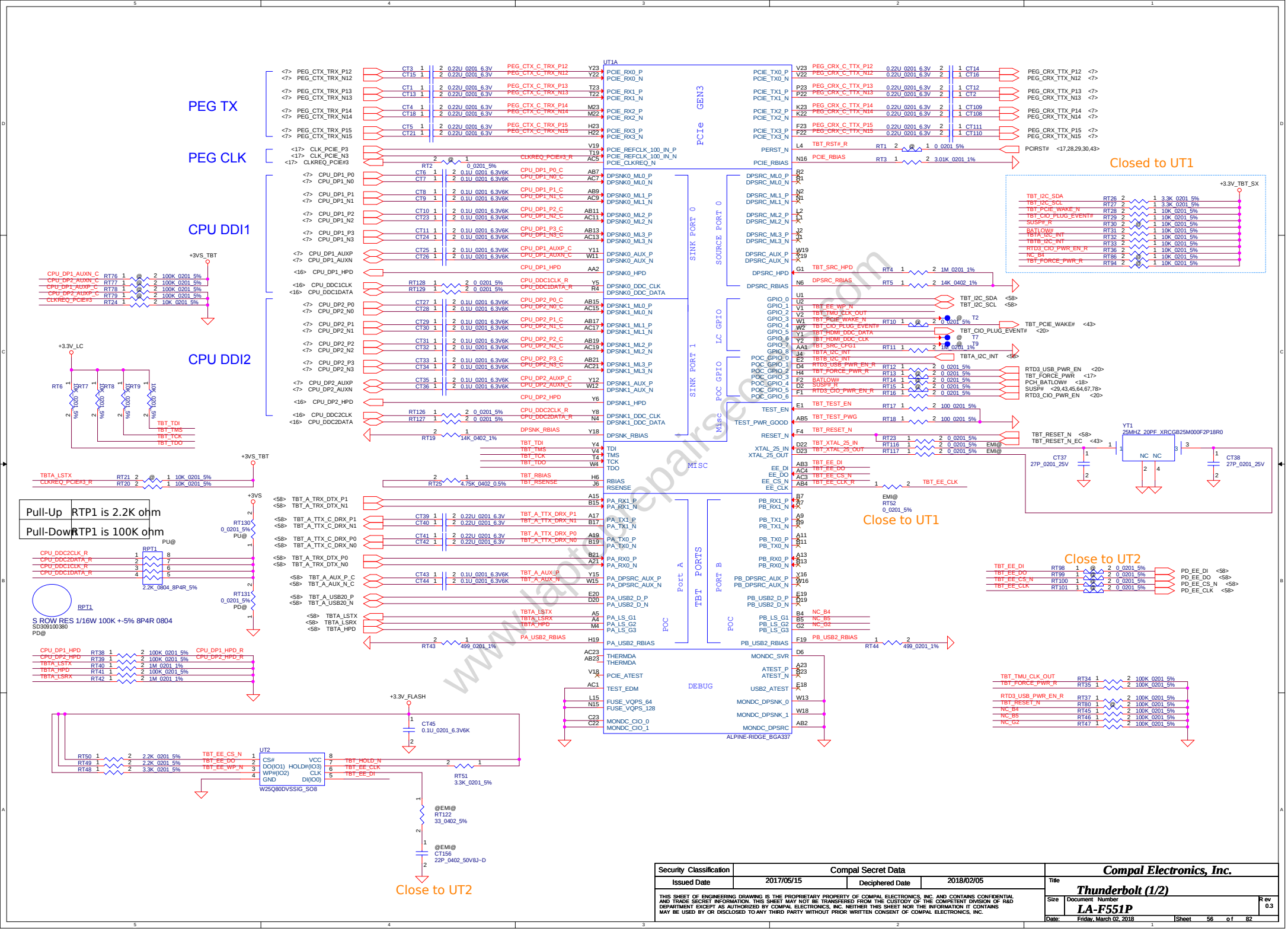
Security Classification	Compal Secret Data	
Issued Date	2017/05/15	Deciphered Date 2018/02/05

Compal Electronics, Inc.

Title: **N17E-GDDR5X_D**

Size: | Document Number: **LA-F552P** | Rev: 0.1

Date: Wednesday, February 07, 2018 | Sheet 55 of 82



Security Classification	Compal Secret Data
Issued Date	2017/05/15
Deciphered Date	2018/02/05

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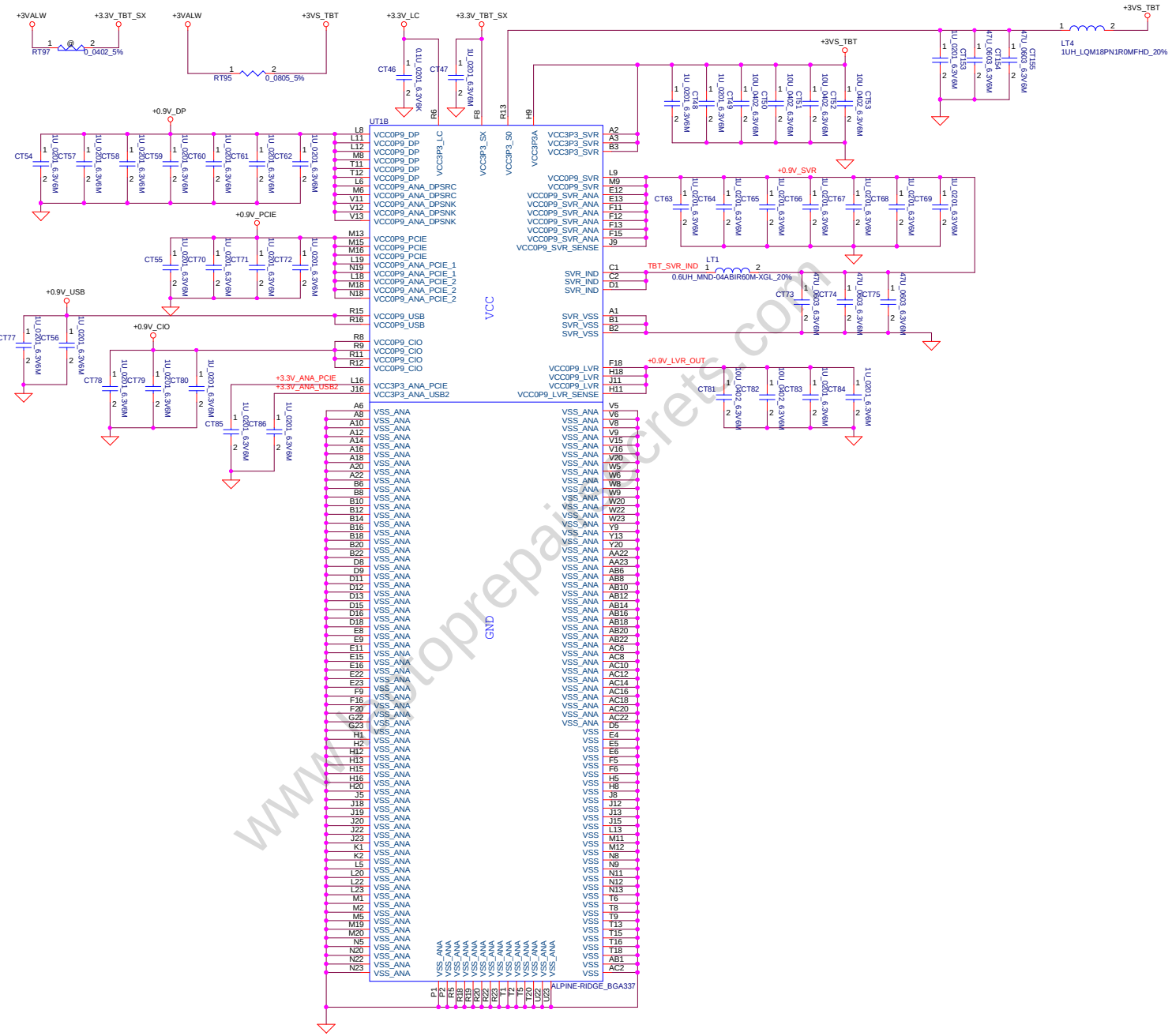
Compal Electronics, Inc.

Title: **Thunderbolt (1/2)**

Size	Document Number	R ev
	LA-F551P	0.3

Date: Friday, March 02, 2018 | Sheet 56 of 82



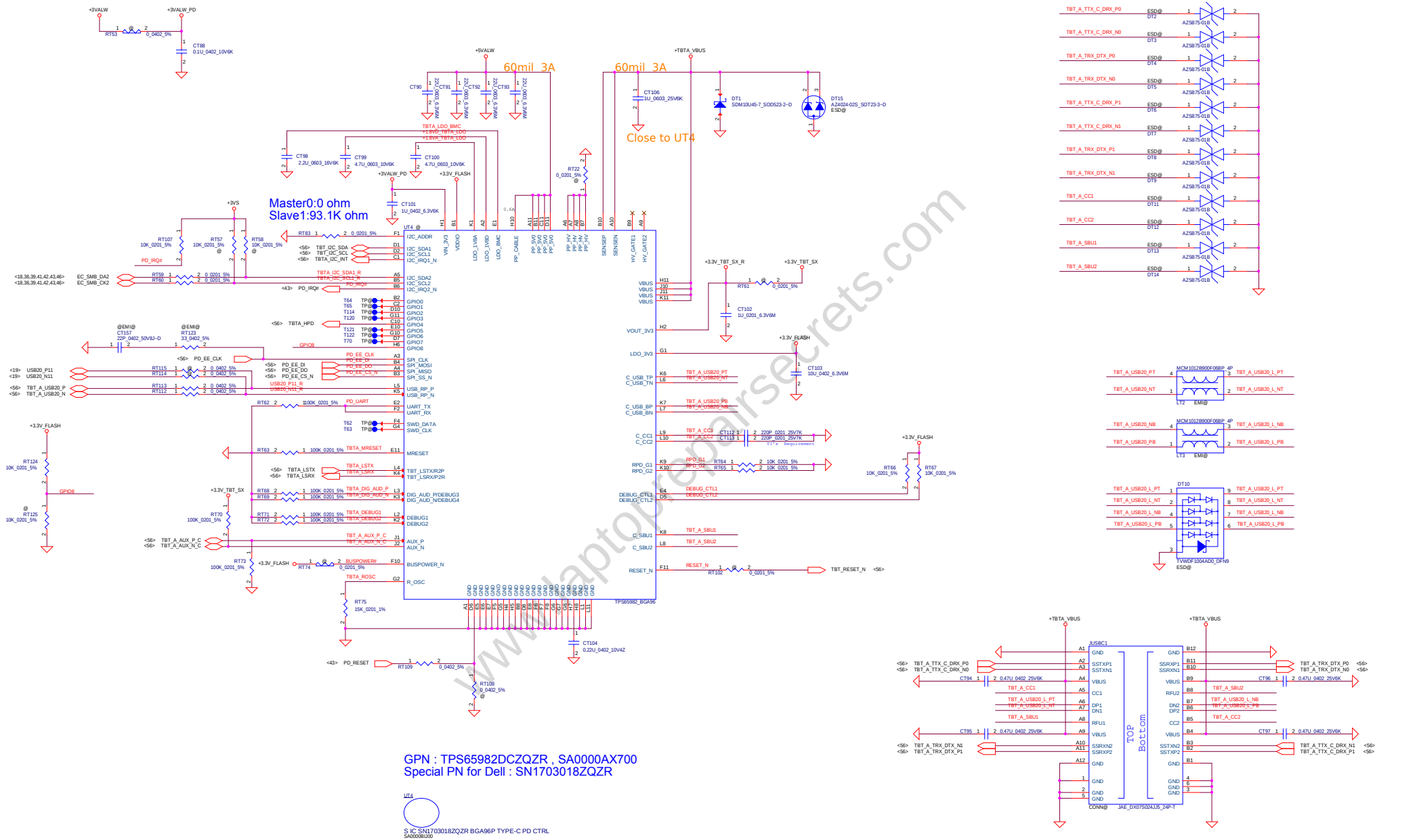
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **Thunderbolt (2/2)**

Size	Document Number	Rev
	LA-F551P	0.3

Date: Wednesday, February 07, 2018 | Sheet 57 of 82

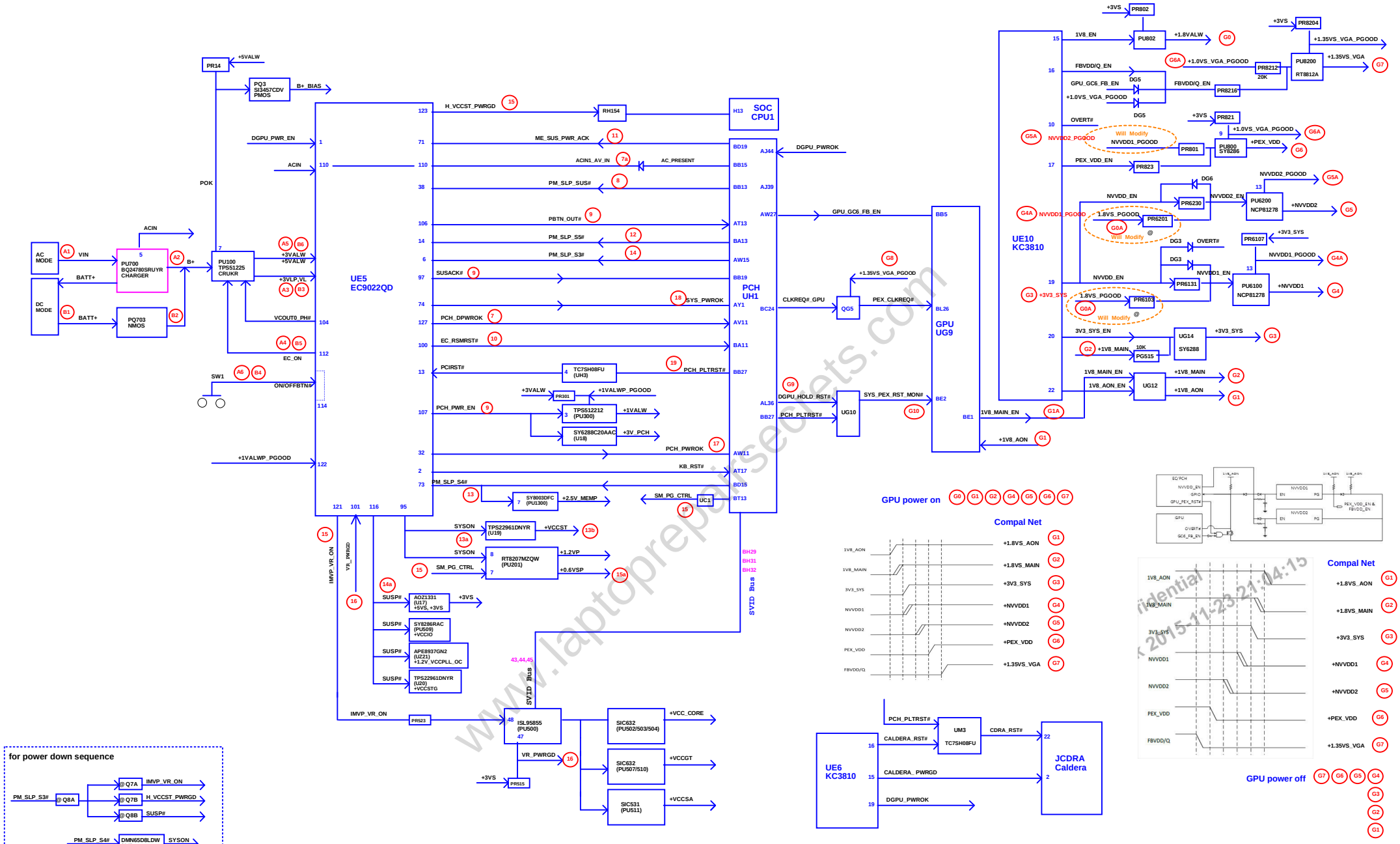


GPN : TPS65982DCZQZR , SA0000AX700
Special PN for Dell : SN1703018ZQZR

UT4

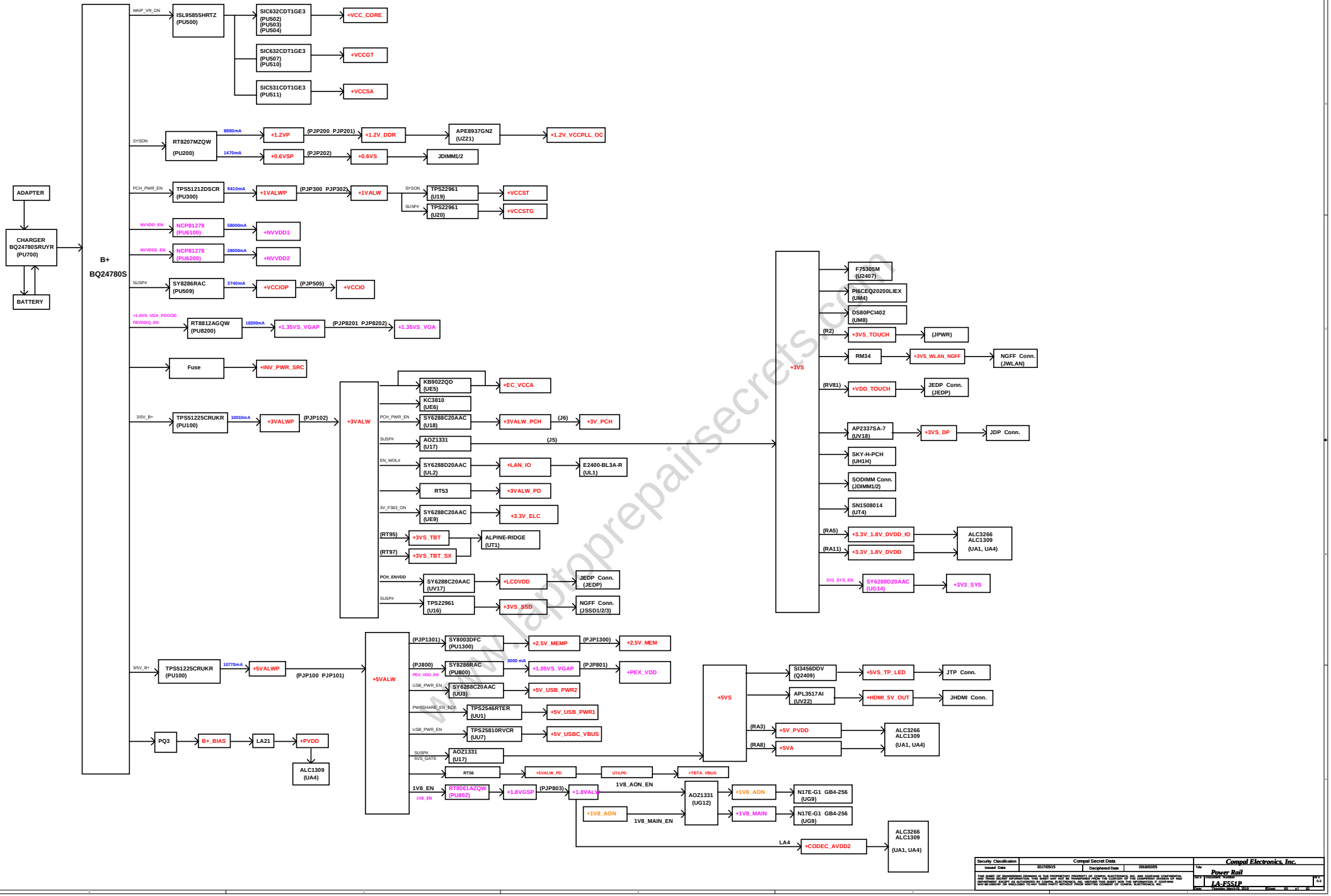
S IC SN1703018ZQZR BGA96P TYPE-C PD CTRL
SA0000BU00
TBTPD@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/05/15	Deciphered Date 2018/02/05	Title: PD+USB3.1 type C
			Size: Document Number: LA-F551P Rev: 0.3
			Date: Thursday, February 08, 2018 Sheet 58 of 82

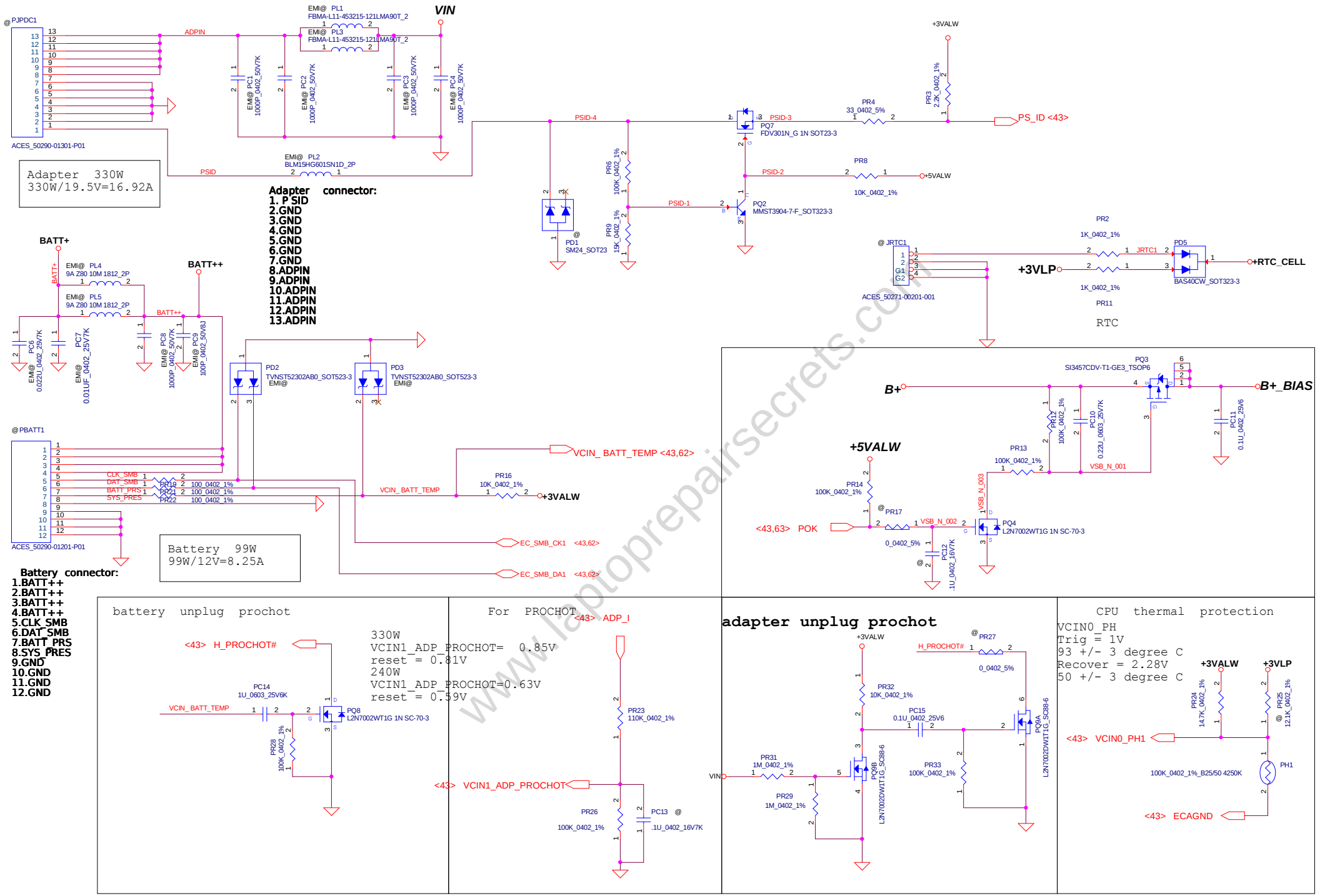


Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title: Power Sequence			
Size	Document Number: LA-F551P		Rev: 0.3
Date: Thursday, March 01, 2018	Sheet 59 of 82		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/05/15	Deciphered Date	2018/02/05
Title	Power Rail		
Size	Document Number		Rev
	LA-F551P		0.3
Date:	Thursday, March 08, 2018	Sheet	66 of 69



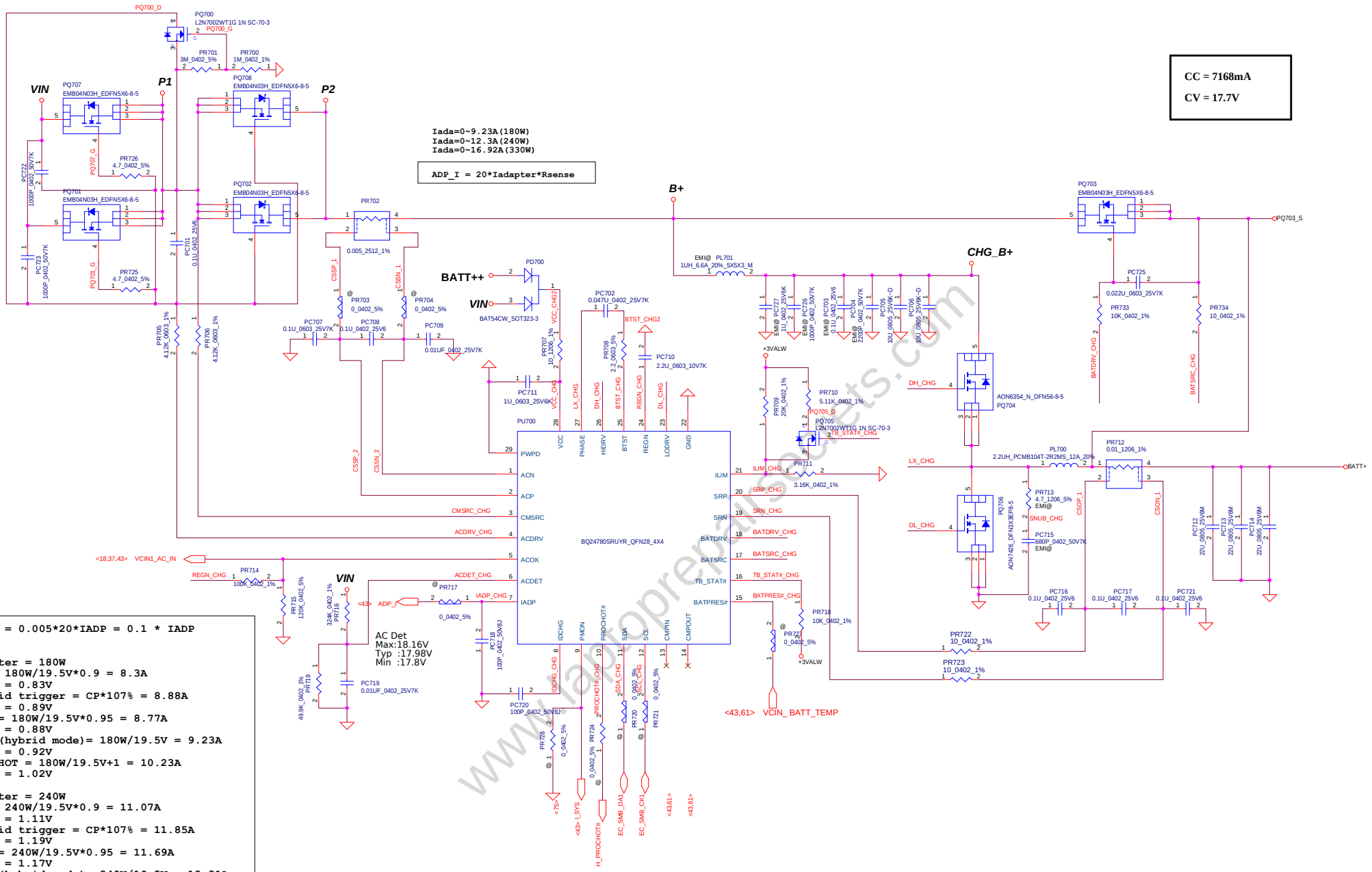
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR-DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 61 of 82

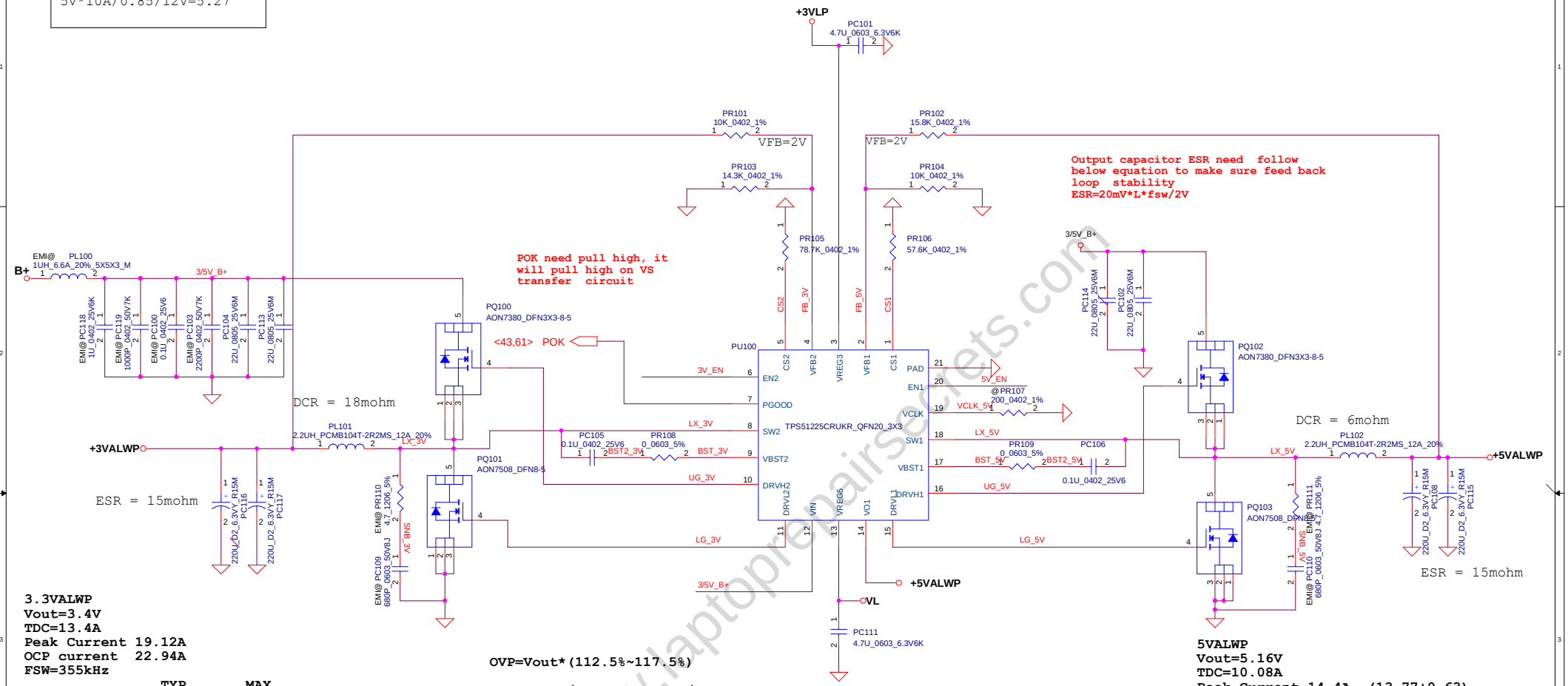



```
ADPI = 0.005*20*IADP = 0.1 * IADP


Adapter = 180W
CP = 180W/19.5V*0.9 = 8.3A
ADPI = 0.83V
Hybrid trigger = CP*107% = 8.88A
ADPI = 0.89V
IPCC= 180W/19.5V*0.95 = 8.77A
ADPI = 0.88V
IPCC(hybrid mode)= 180W/19.5V = 9.23A
ADPI = 0.92V
PROCHOT = 180W/19.5V+1 = 10.23A
ADPI = 1.02V

Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 1.11V
Hybrid trigger = CP*107% = 11.85A
ADPI = 1.19V
IPCC= 240W/19.5V*0.95 = 11.69A
ADPI = 1.17V
IPCC(hybrid mode)= 240W/19.5V = 12.31A
ADPI = 1.23V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 1.33V

Adapter = 330W
CP = 330W/19.5V*0.9 =15.23 A
APDI = 1.52V
Hybrid trigger = CP*107% = 16.3A
ADPI = 1.63V
IPCC = 330W/19.5V*(1*0.95) = 16.08A
ADPI = 1.61V
IPCC(hybrid mode)= 330W/19.5V = 16.92A
ADPI = 1.69V
PROCHOT = 330W/19.5V+1 = 17.92A
ADPI = 1.79V
```


Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR_CHARGER			
Size	Document Number: LA-F551P		Rev: 1.0
Date: Thursday, March 01, 2018	Sheet 62 of 82		

Input Current: 7.5A
3.3V*10A/0.85/12V=2.23
5V*10A/0.85/12V=5.27



3.3VALWP
Vout=3.4V
TDC=13.4A
Peak Current 19.12A
OCP current 22.94A
FSW=355kHz

	TYP	MAX
H/S Rds(on) :	8.2mohm	10.5mohm
L/S Rds(on) :	3.5mohm	4.6mohm

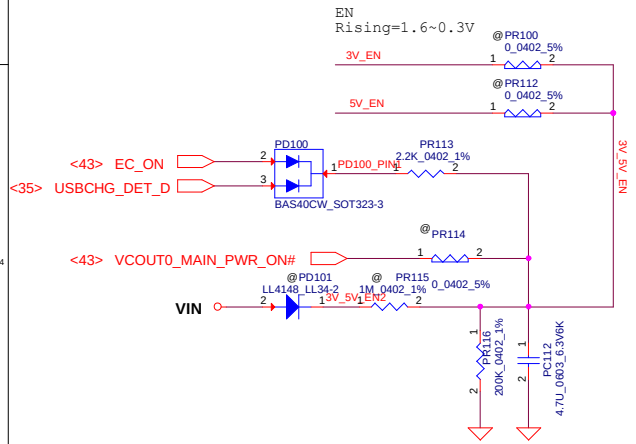
OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

5VALWP
Vout=5.16V
TDC=10.08A
Peak Current 14.4A (13.77+0.63)
OCP current 17.28A
FSW=300kHz

	TYP	MAX
H/S Rds(on) :	8.2mohm	10.5mohm
L/S Rds(on) :	3.5mohm	4.6mohm



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

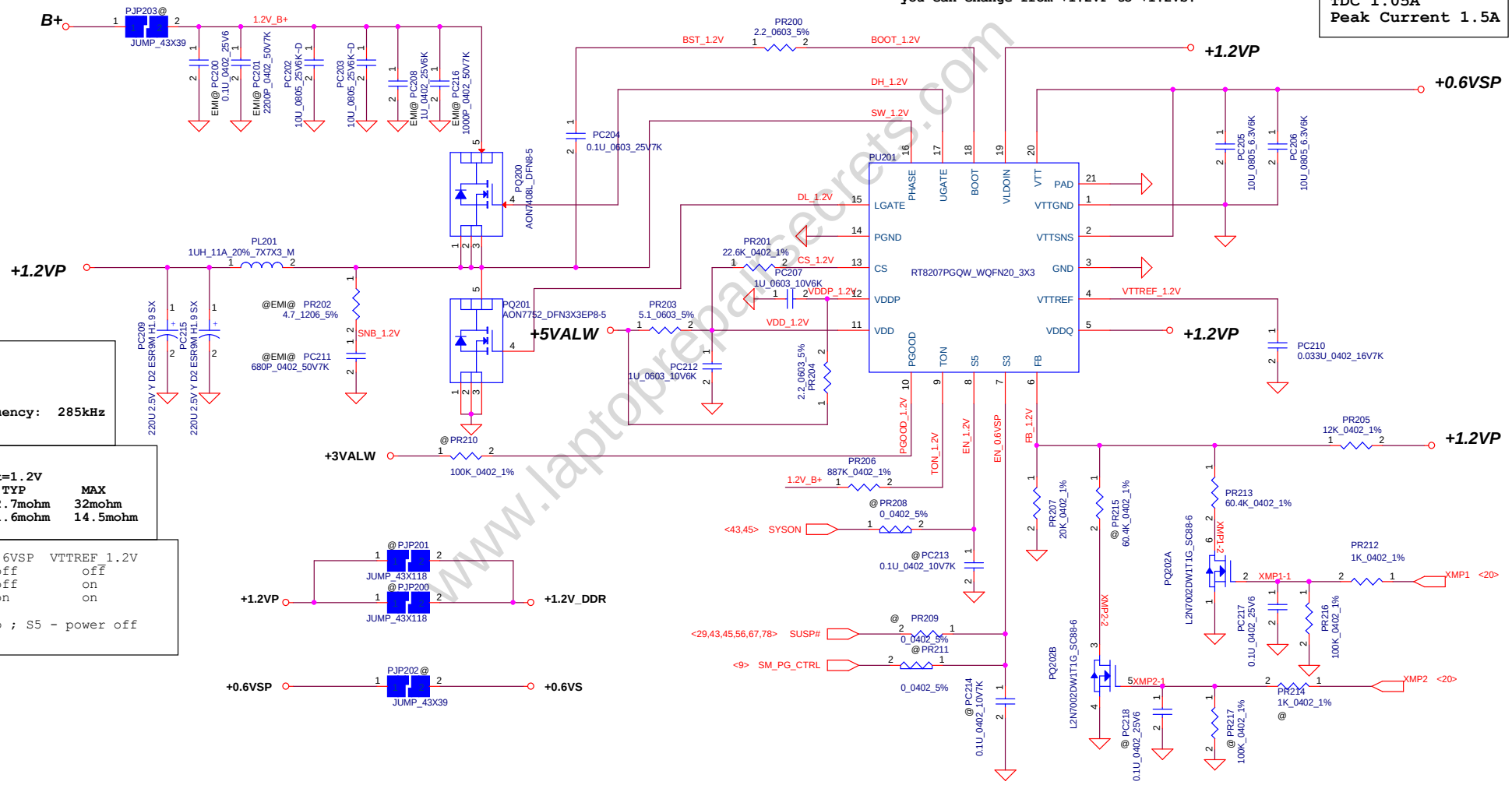
Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 Sheet 63 of 82

Input Current: 1A
1.2V*8.88A/0.85/12V=1

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

+0.6VSP
TDC 1.05A
Peak Current 1.5A



+1.2VP
TDC=9A
Ipeak=12.86A
OCP=15.43A
Switching Frequency: 285kHz

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

	TYP	MAX
H/S Rds(on) :	22.7mohm	32mohm
L/S Rds(on) :	11.6mohm	14.5mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

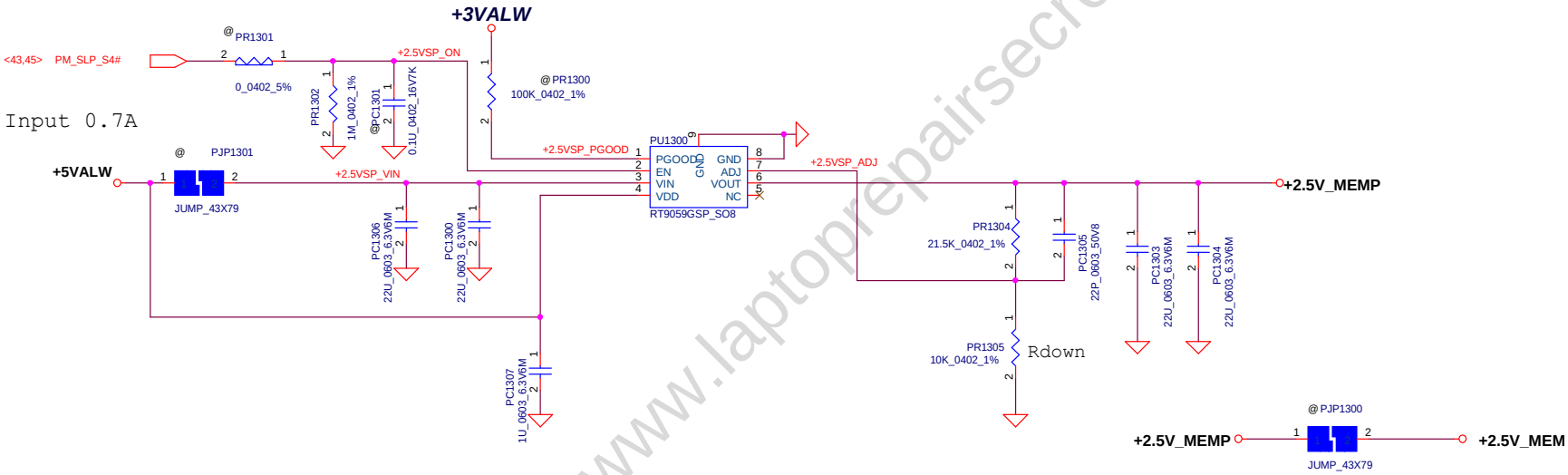
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_1.2VP/0.6VSP

Size | Document Number: LA-F551P | Rev: 1.0

Date: Thursday, March 01, 2018 | Sheet 64 of 82



+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

Vout=0.8V* (1+Rup/Rdown)

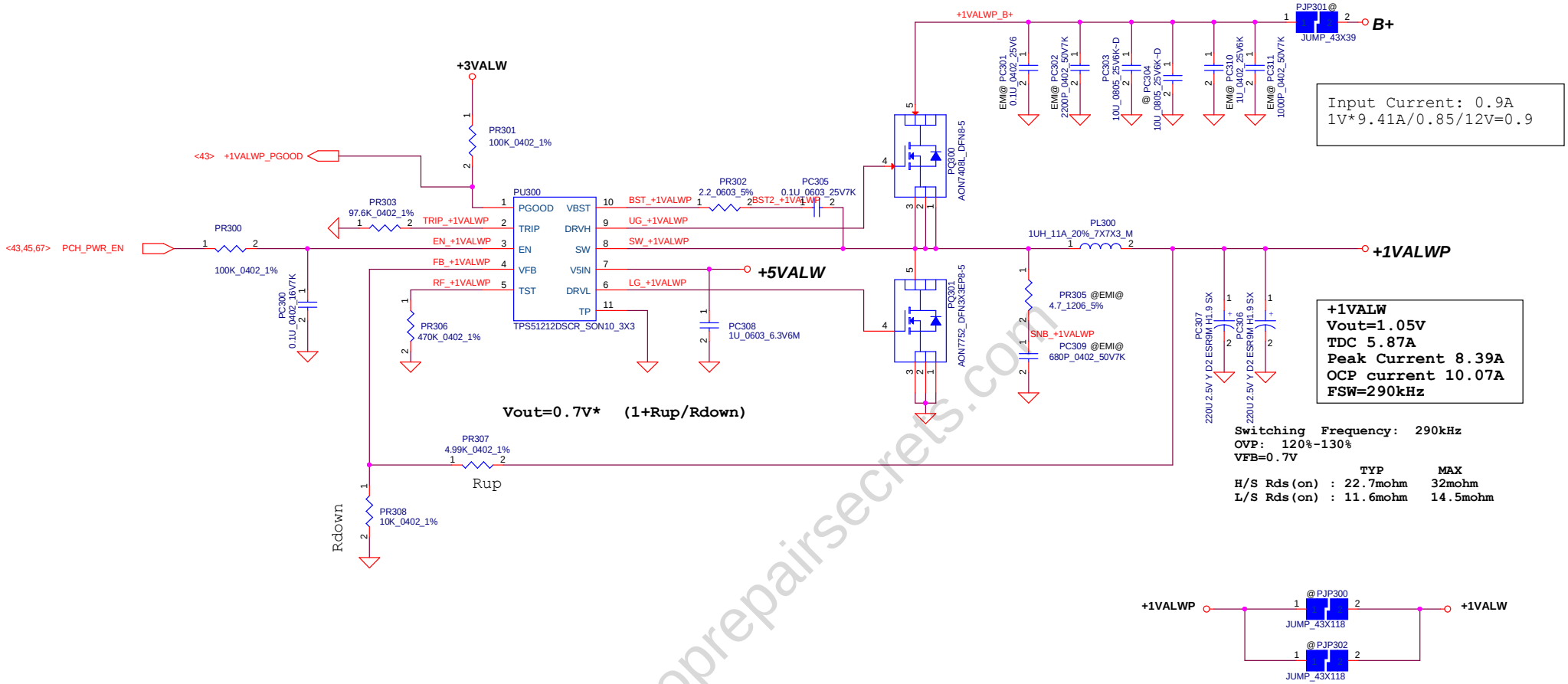
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+2.5V_MEM

Size | Document Number: LA-F551P | Rev 1.0

Date: Thursday, March 01, 2018 | Sheet 65 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+1VALWP**

Size	Document Number	Rev
	LA-F551P	1.0

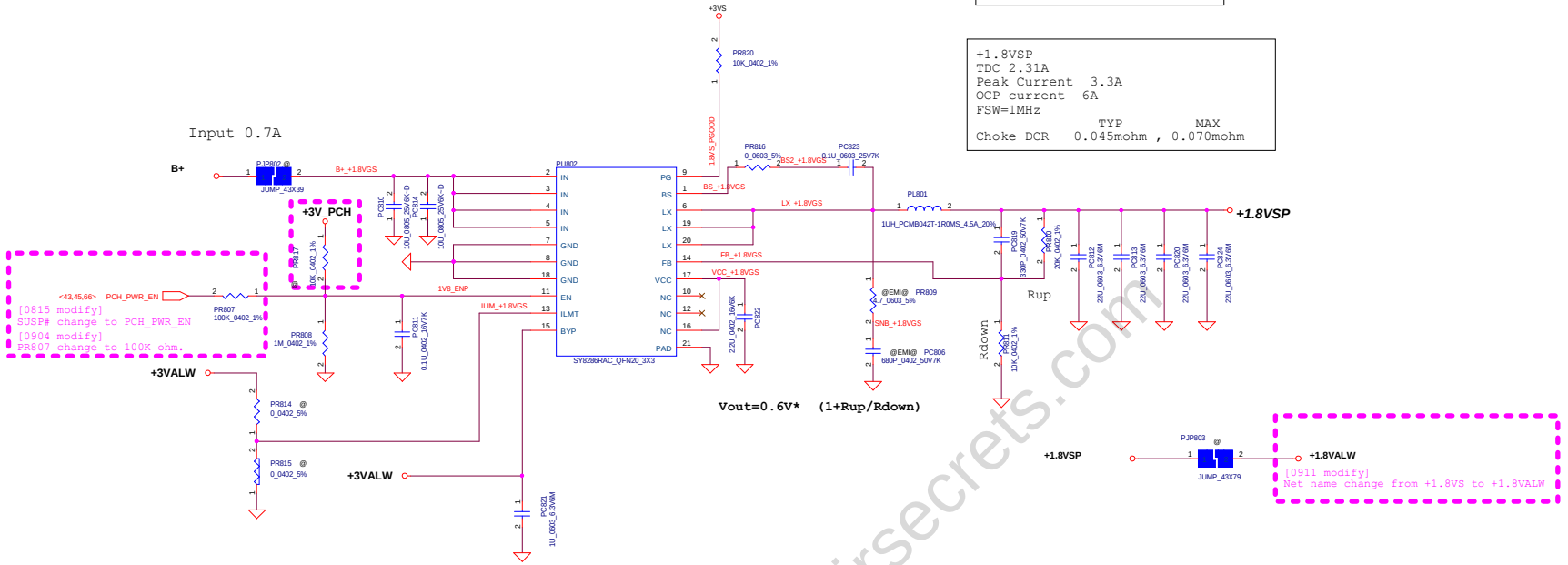
Date: Thursday, March 01, 2018 Sheet 66 of 82

Input Current: 0.407A
1,8V*2,31A/0.85/12V=0.407

+1.8VSP
TDC 2.31A
Peak Current 3.3A
OCP current 6A
FSW=1MHz

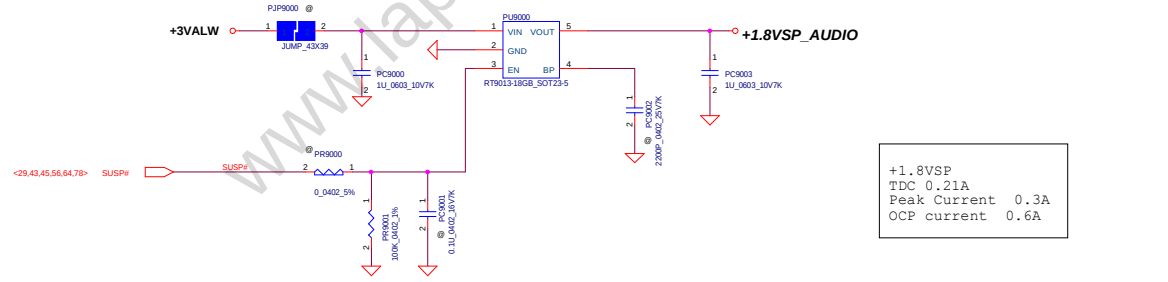
	TYP	MAX
Choke DCR	0.045mohm ,	0.070mohm

Input 0.7A



Vout=0.6V* (1+Rup/Rdown)

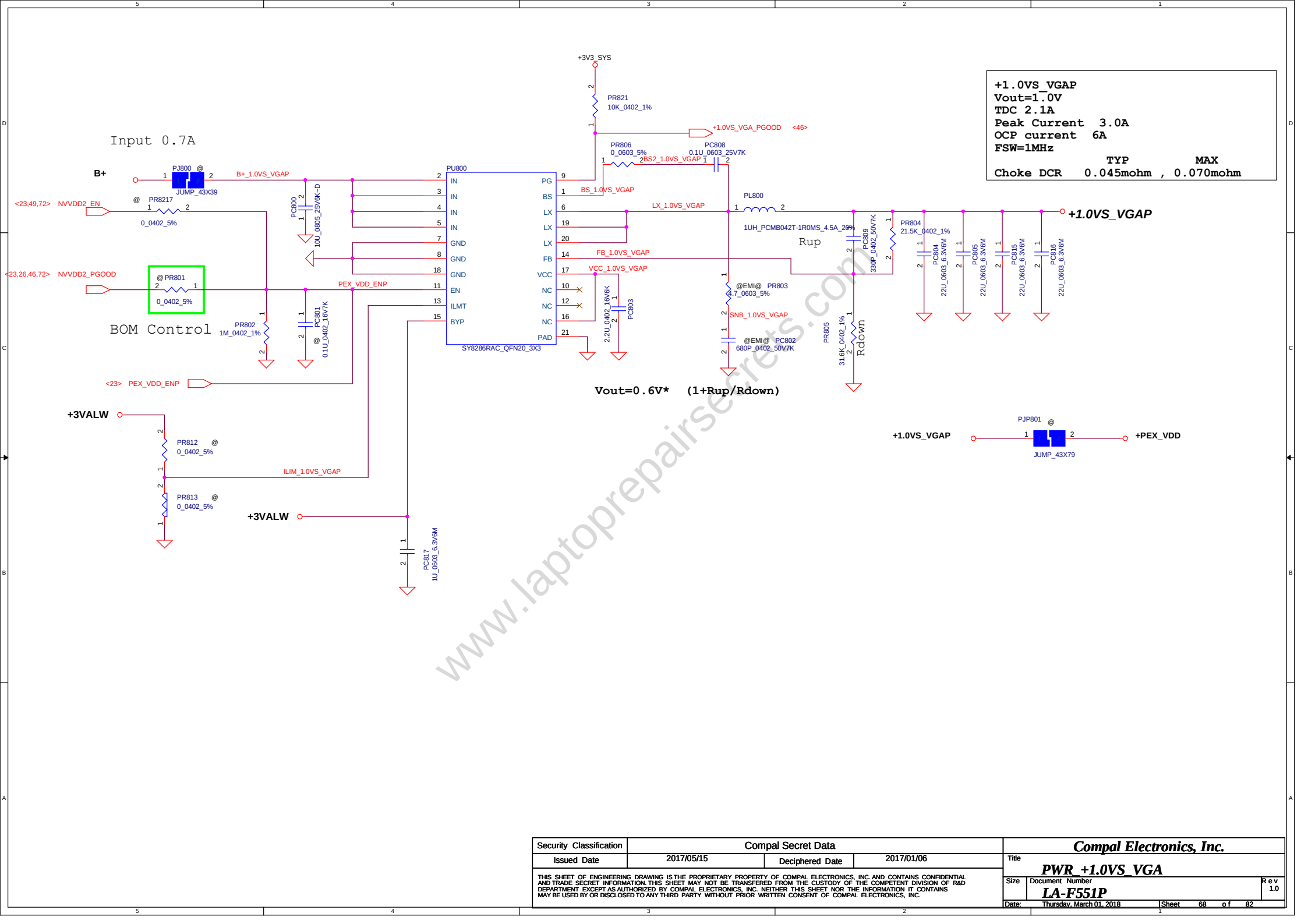
[0814 modify]
Add RT9013 Circuit



+1.8VSP
TDC 0.21A
Peak Current 0.3A
OCP current 0.6A

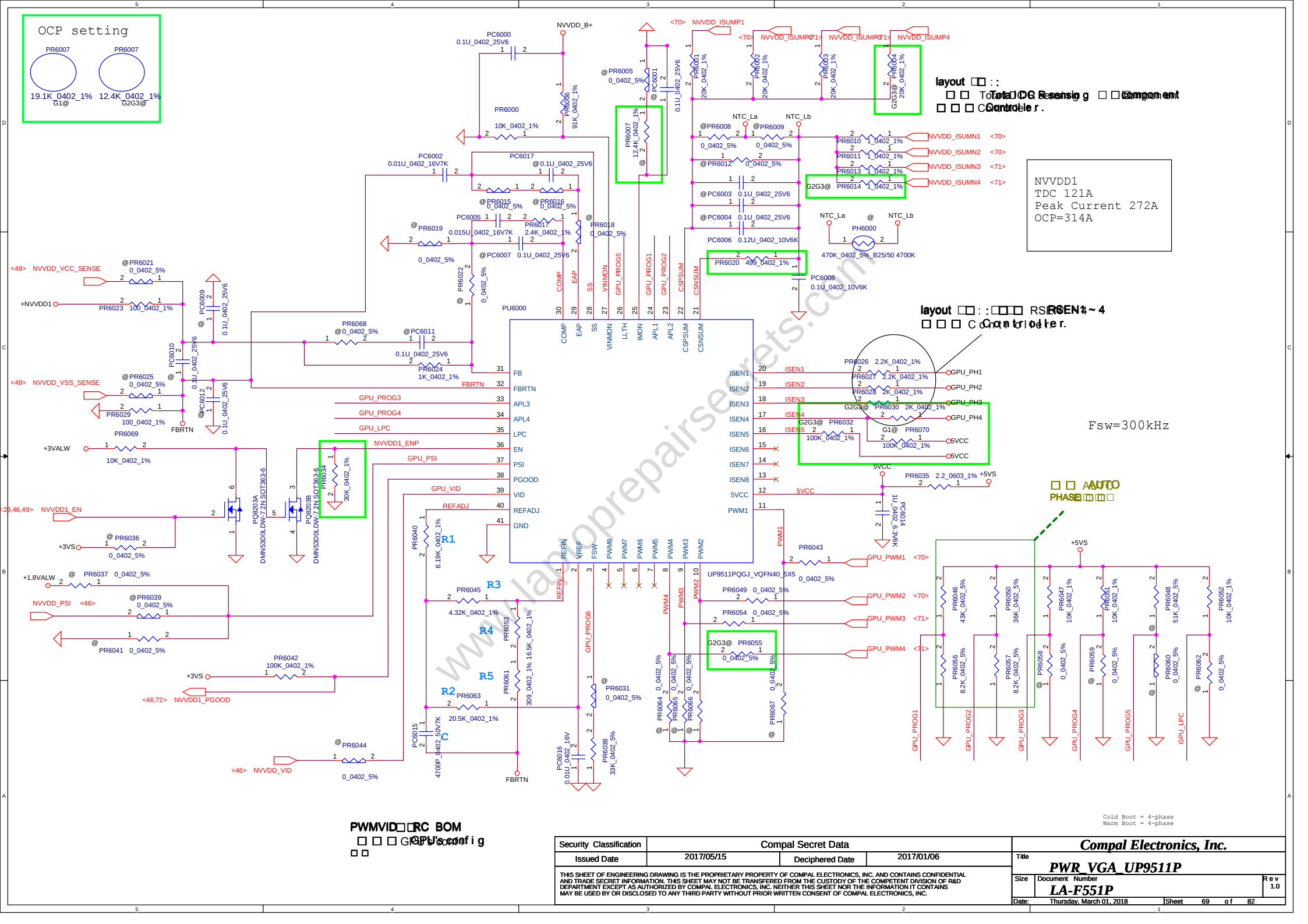
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR_+1.8VSP
Size	Document Number: LA-F551P
Rev	1.0
Date:	Thursday, March 01, 2018
Sheet	67 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: PWR_+1.0VS_VGA			
Size	Document Number: LA-F551P		Rev 1.0
Date: Thursday, March 01, 2018		Sheet 68 of 82	



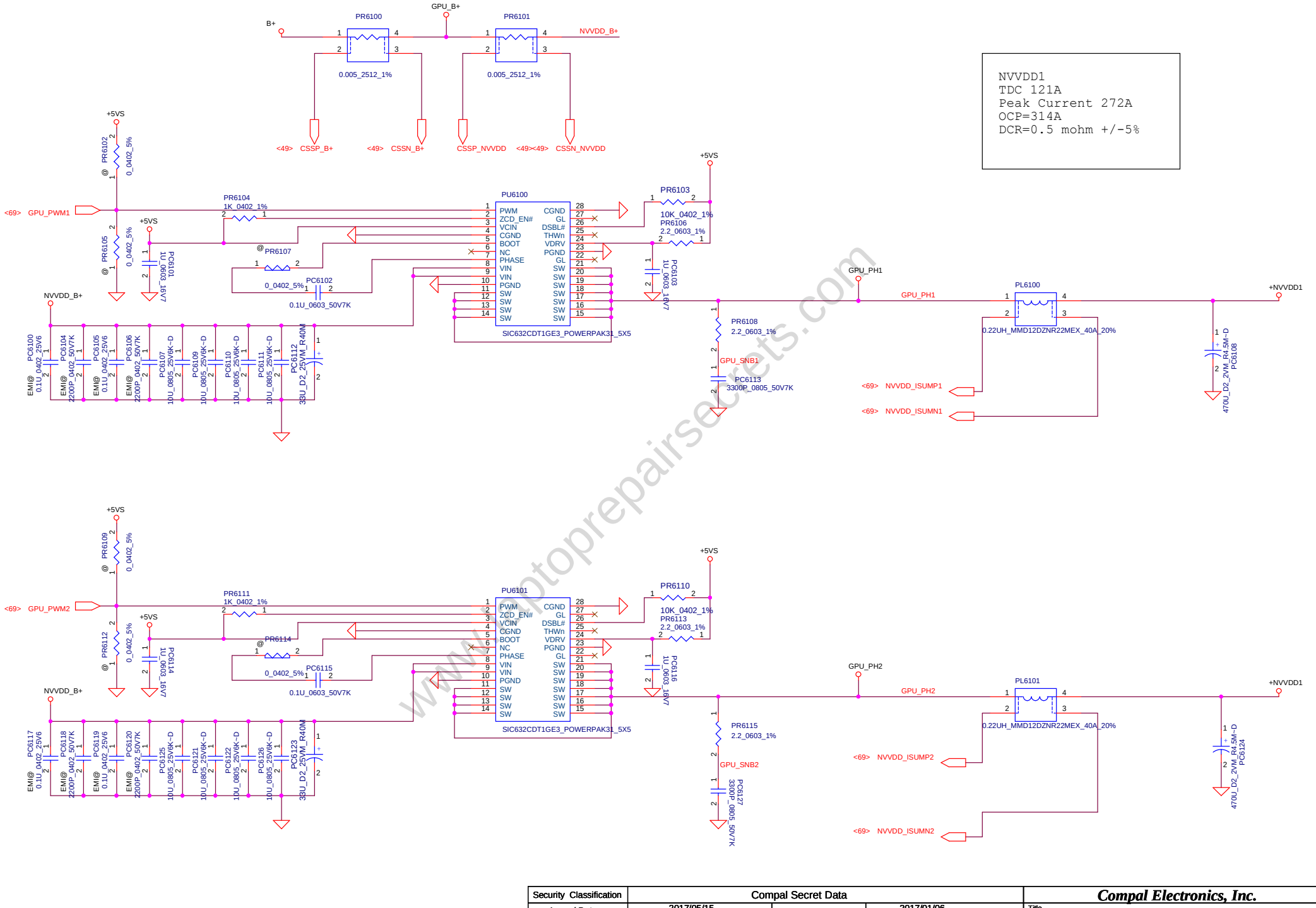
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_VGA_UP9511P

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 69 of 82



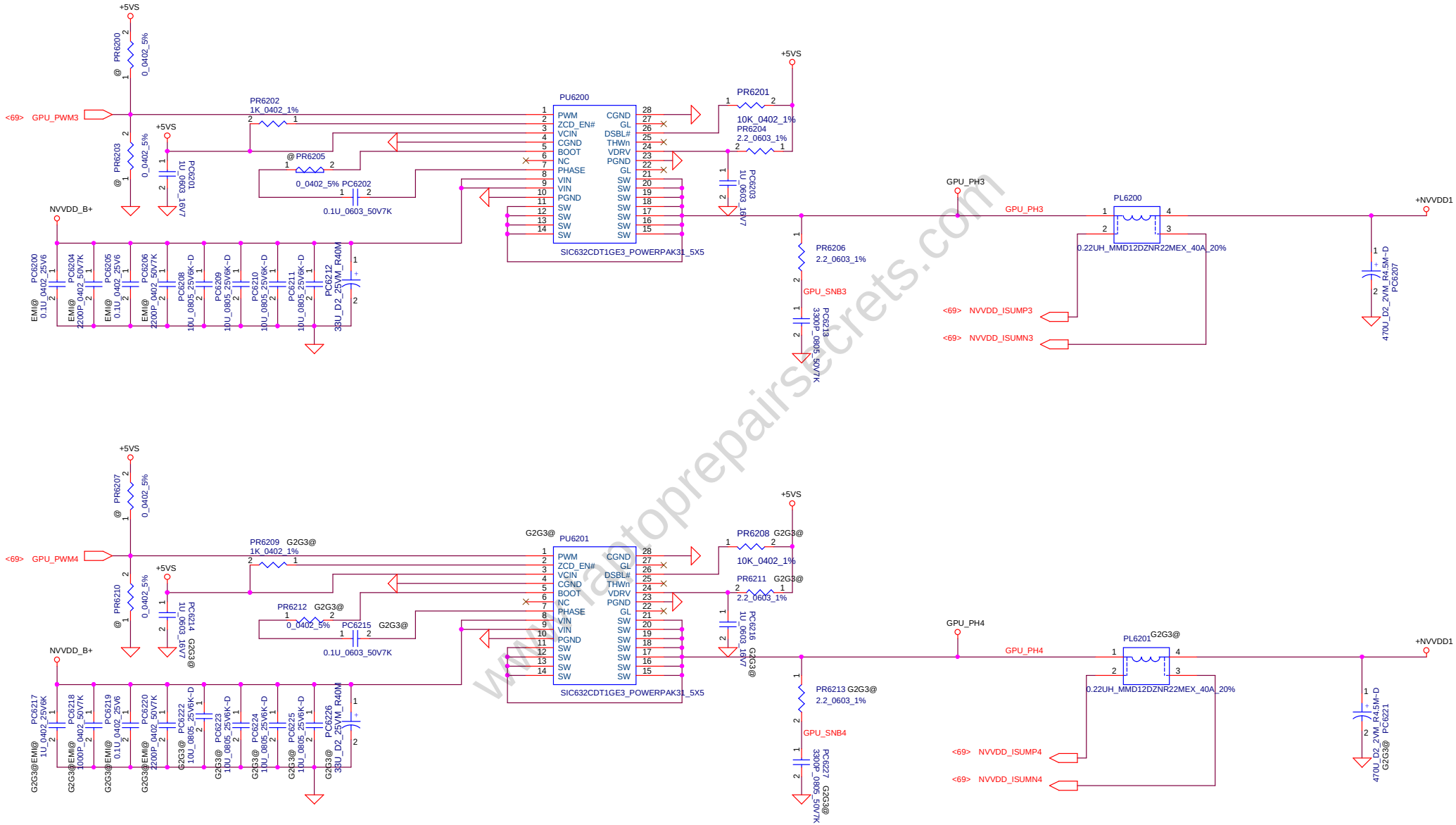
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 70 of 82



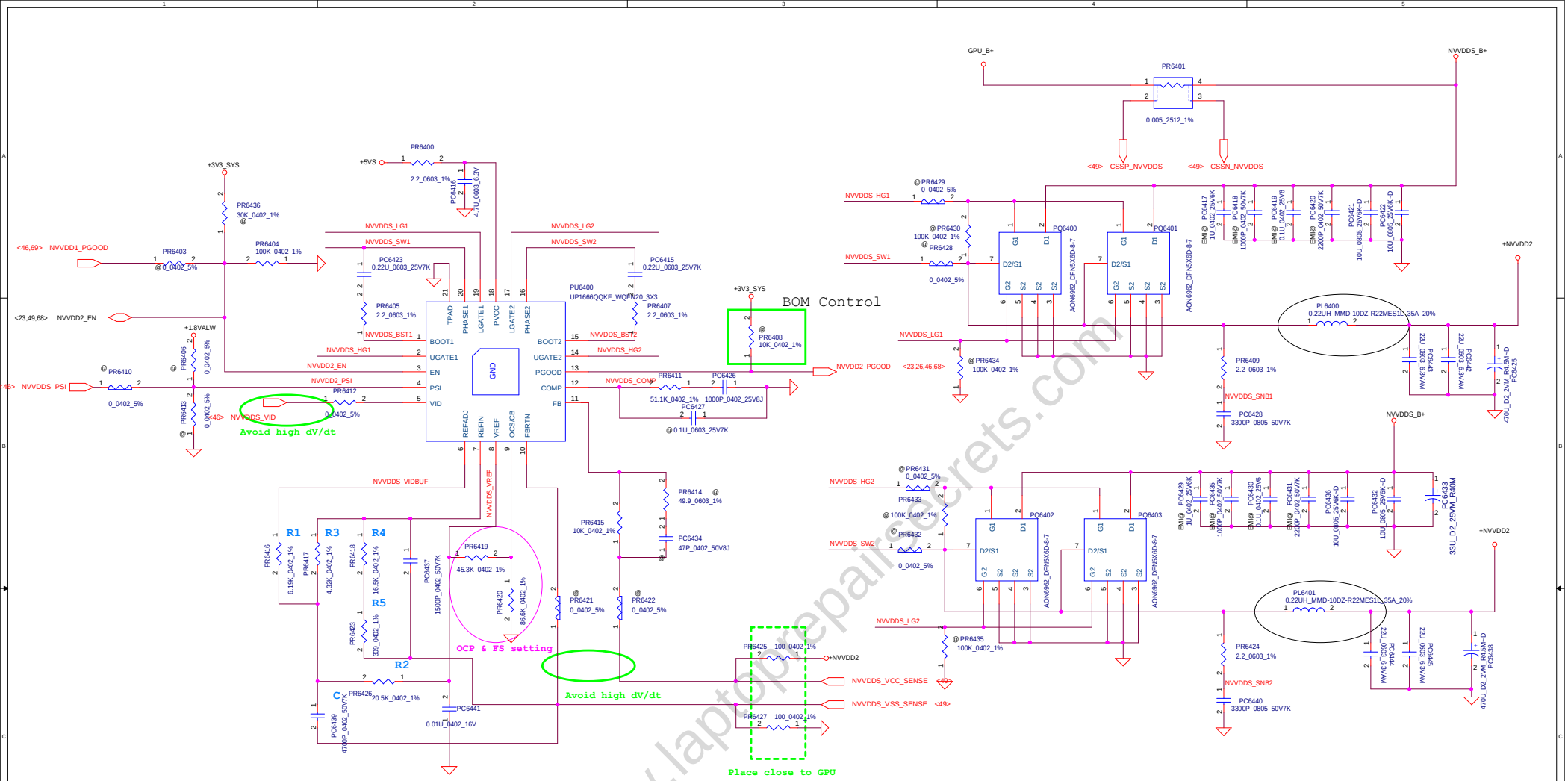
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 71 of 82



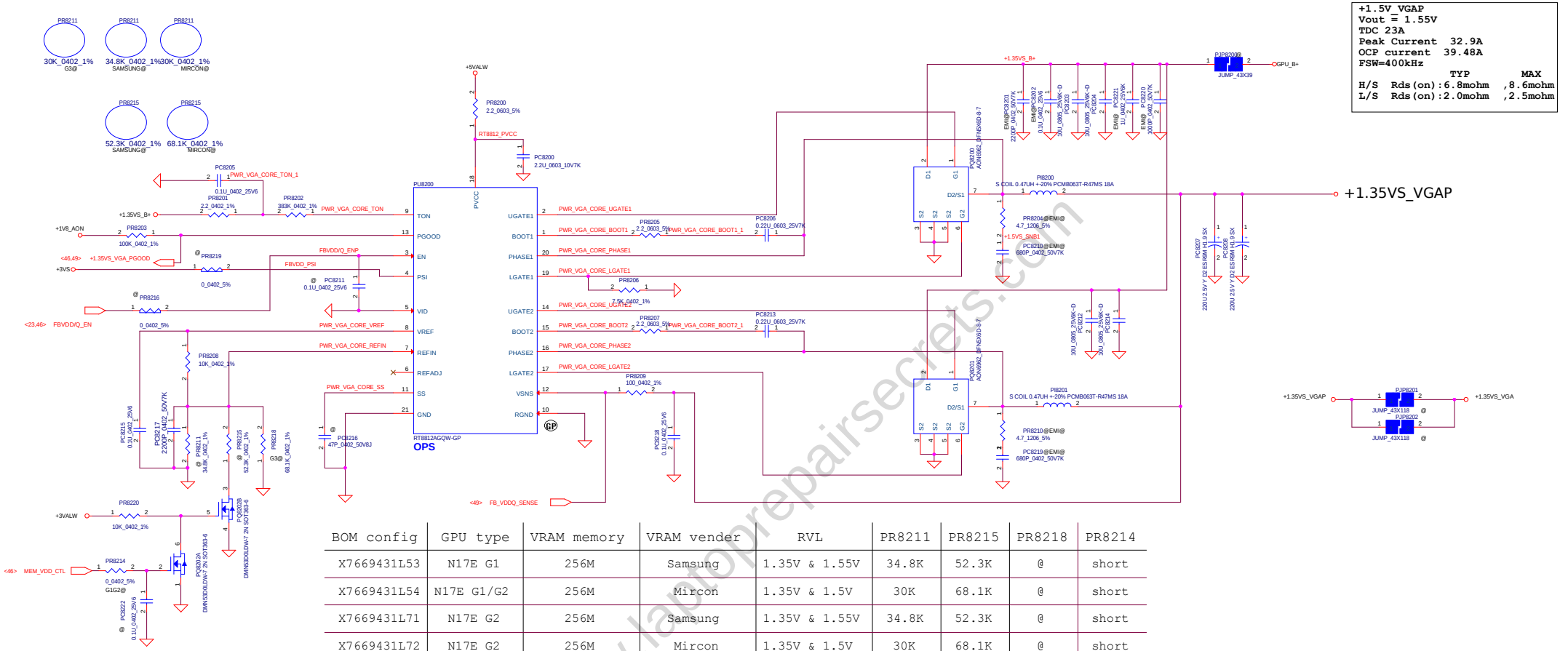
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_+NVVDD2**

Size	Document Number	Rev
	LA-F551P	1.0

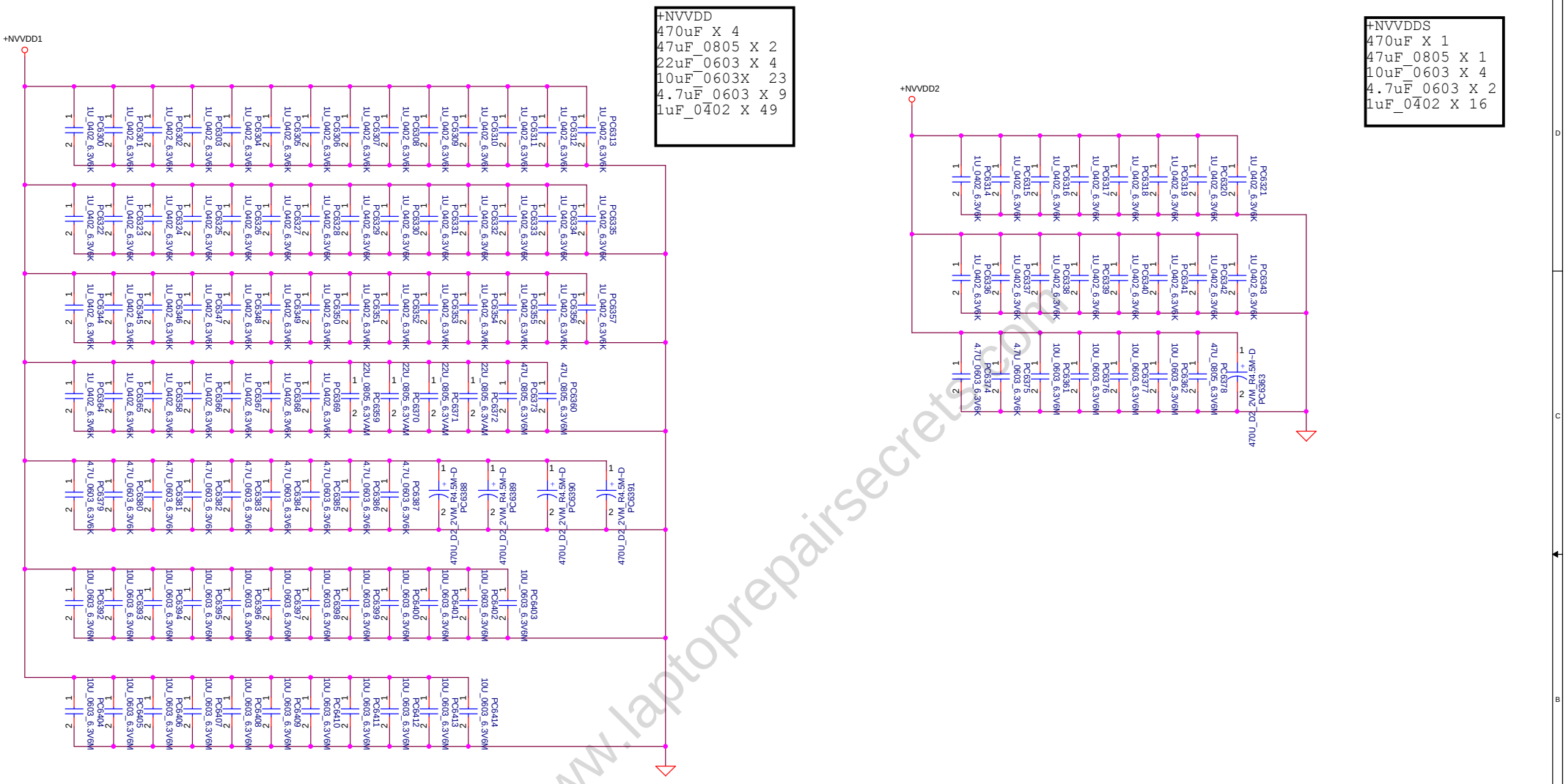
Date: Thursday, March 01, 2018 | Sheet 72 of 82



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PR8211	PR8215	PR8218	PR8214
X7669431L53	N17E G1	256M	Samsung	1.35V & 1.55V	34.8K	52.3K	@	short
X7669431L54	N17E G1/G2	256M	Mircon	1.35V & 1.5V	30K	68.1K	@	short
X7669431L71	N17E G2	256M	Samsung	1.35V & 1.55V	34.8K	52.3K	@	short
X7669431L72	N17E G2	256M	Mircon	1.35V & 1.5V	30K	68.1K	@	short
X7669431L73	N17P G1	128M	Samsung	1.35V & 1.5V	30K	68.1K	@	short
X7669431L74	N17P G1	128M	Hynix	1.35V & 1.5V	30K	68.1K	@	short
X7669431L77	N17E G1	256M	Hynix	1.35V & 1.55V	34.8K	52.3K	@	short
X7669431L78	N17E G2	256M	Hynix	1.35V & 1.55V	34.8K	52.3K	@	short
-	N17E G3		Mircon	1.35V	30K	@	68.1K	@

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR +1.55VRAM		
Size	Document Number LA-F551P		Rev 1.0
Date: Thursday, March 01, 2018	Sheet 73	of	82



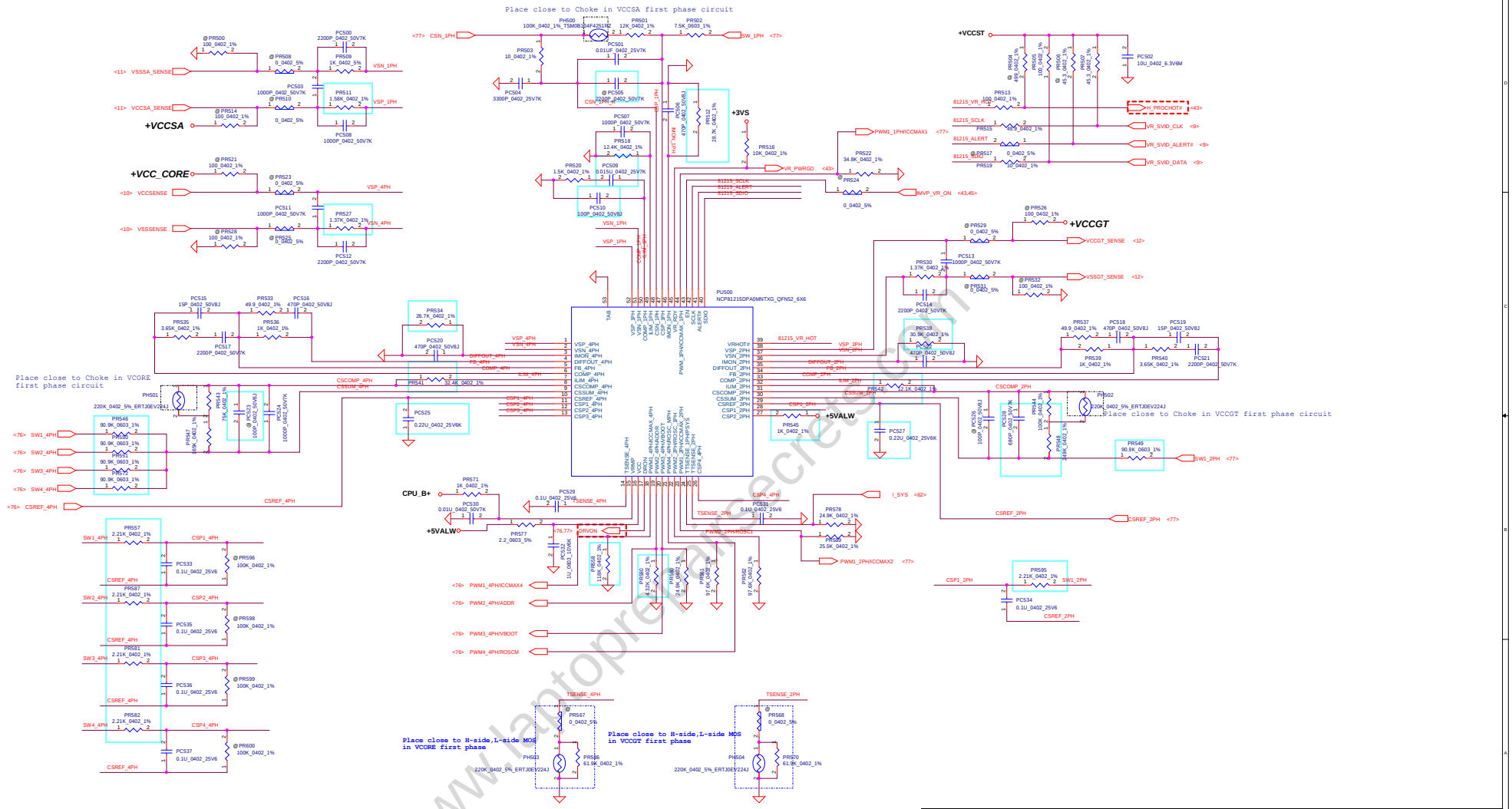
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR_VGA DECOUPLING**

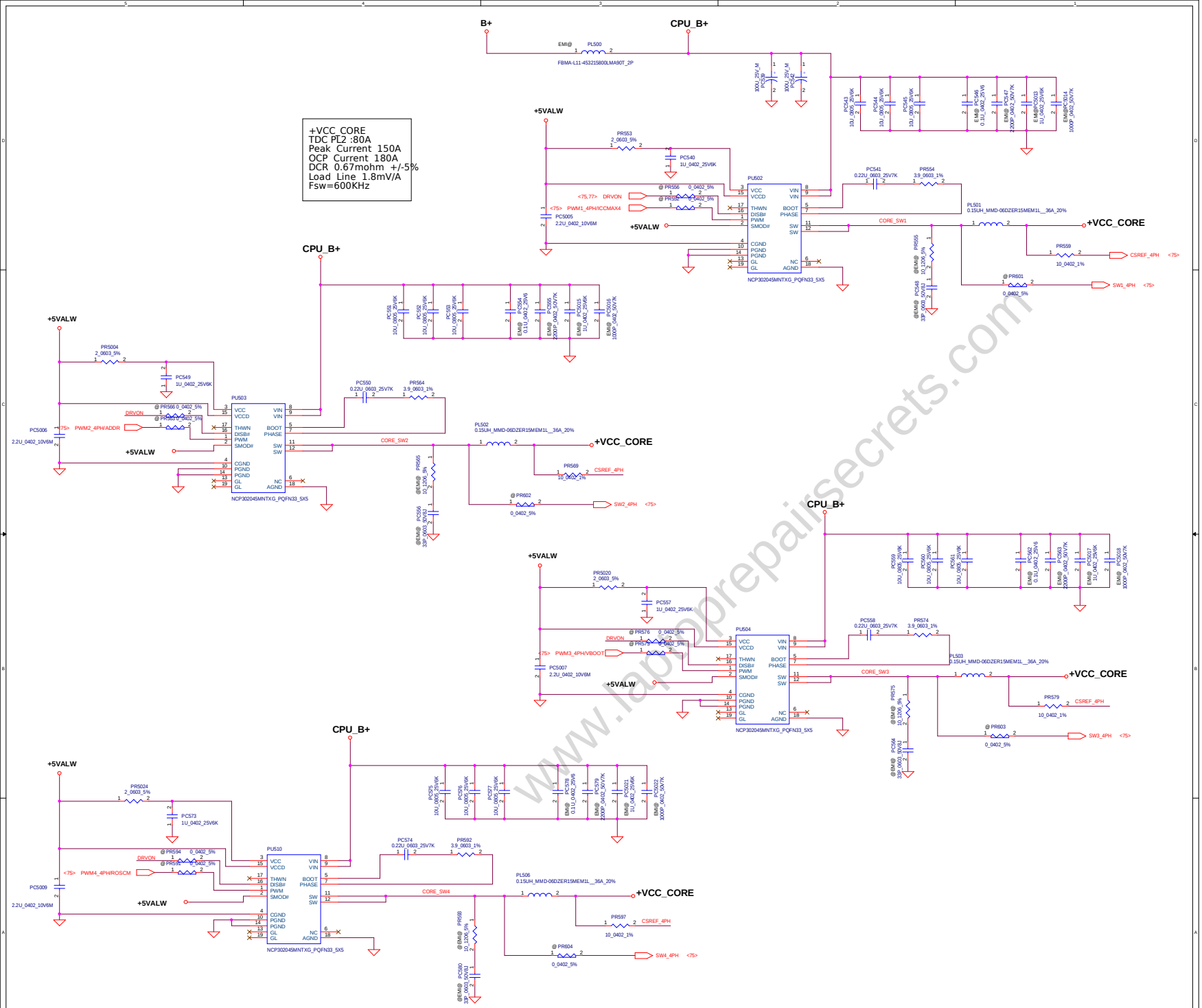
Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 74 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR_VCORE_NCP81215
Size	Document Number: LA-F551P
Rev	1.0
Date: Thursday, March 01, 2018	Sheet 75 of 82



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR_VCORE_+VCC_CORE
Size	Document Number: LA-F551P
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Date:	Thursday, March 01, 2018
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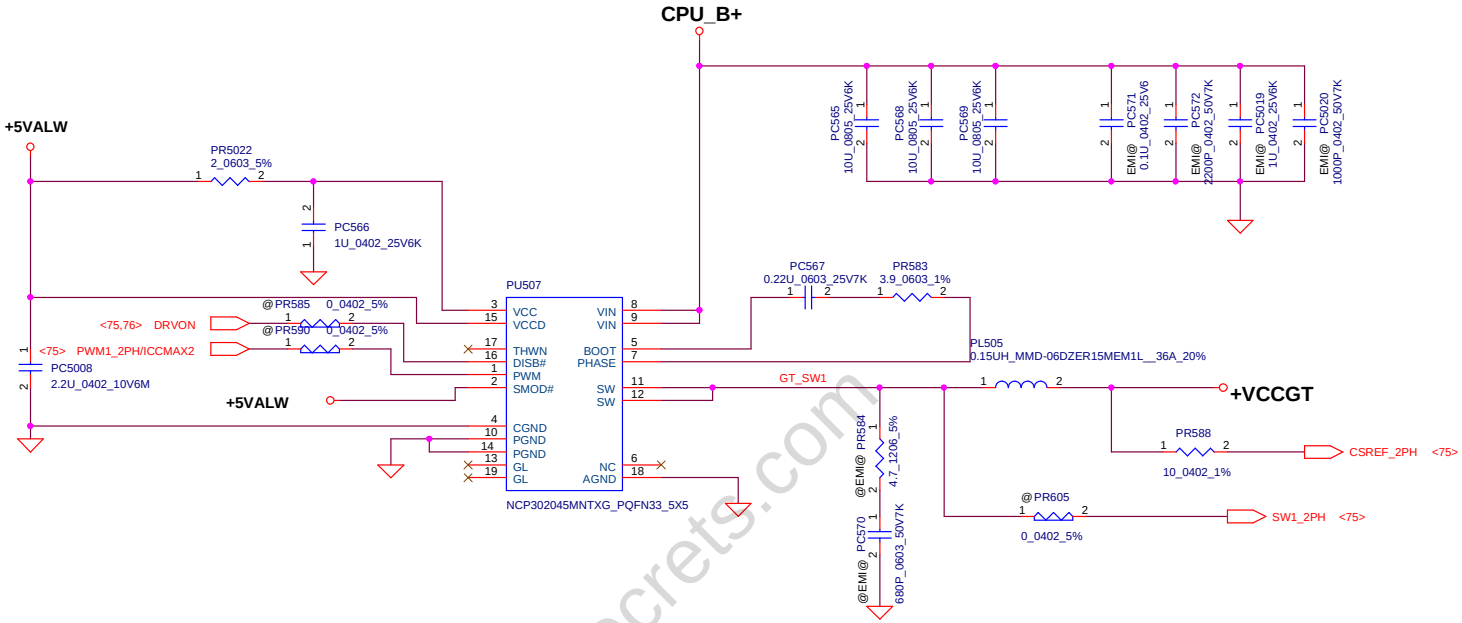
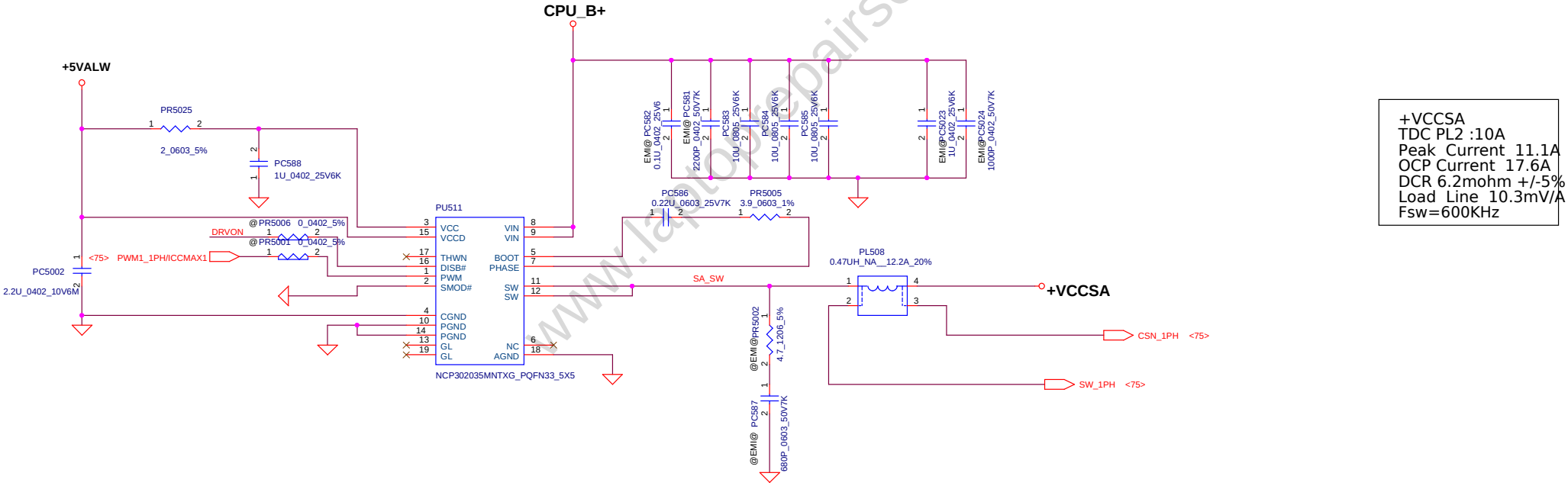
+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 38.4A
DCR 0.67mohm +/-5%
Load Line 2.7mV/A
Fsw=600KHz



+VCCSA
TDC PL2 :10A
Peak Current 11.1A
OCP Current 17.6A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A
Fsw=600KHz



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCCGT/+VCCSA

Size	Document Number	Rev
	LA-F551P	1.0

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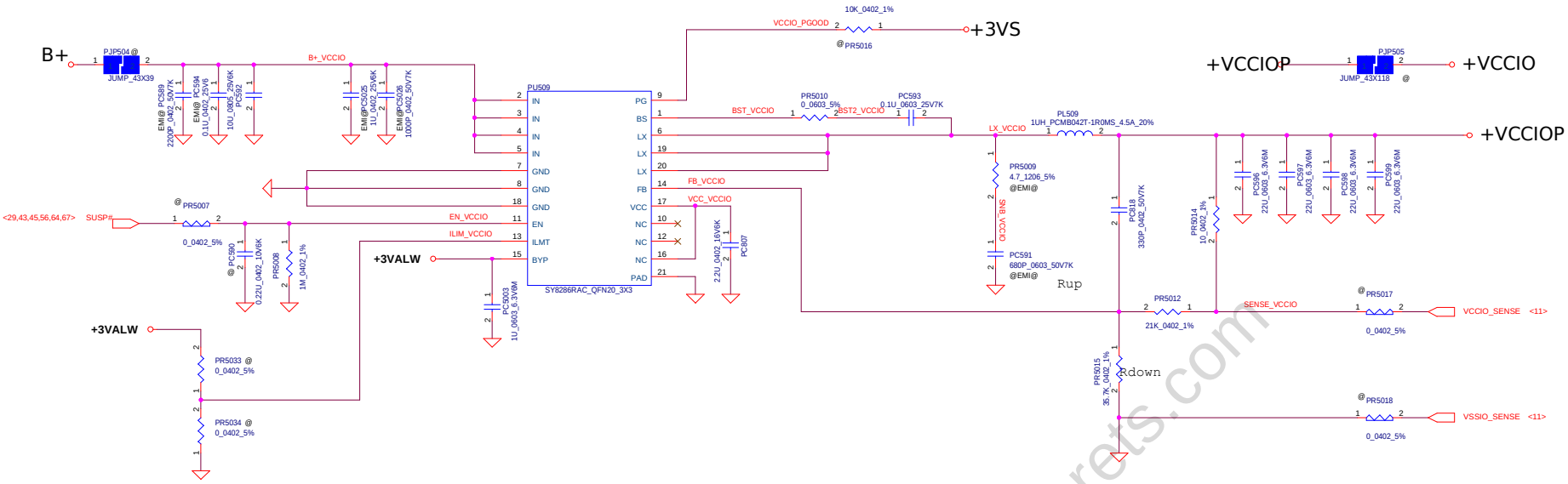

+VCCIOP (0.95V)
TDC 4.48 A
Peak Current 6.4 A
OCP Current 9 A Fix by IC

	TYP	MAX
Choke DCR	24.0mohm , 27.0mohm	

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR_+VCCIO
Size	Document Number: LA-F551P
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Date:	Thursday, March 01, 2018
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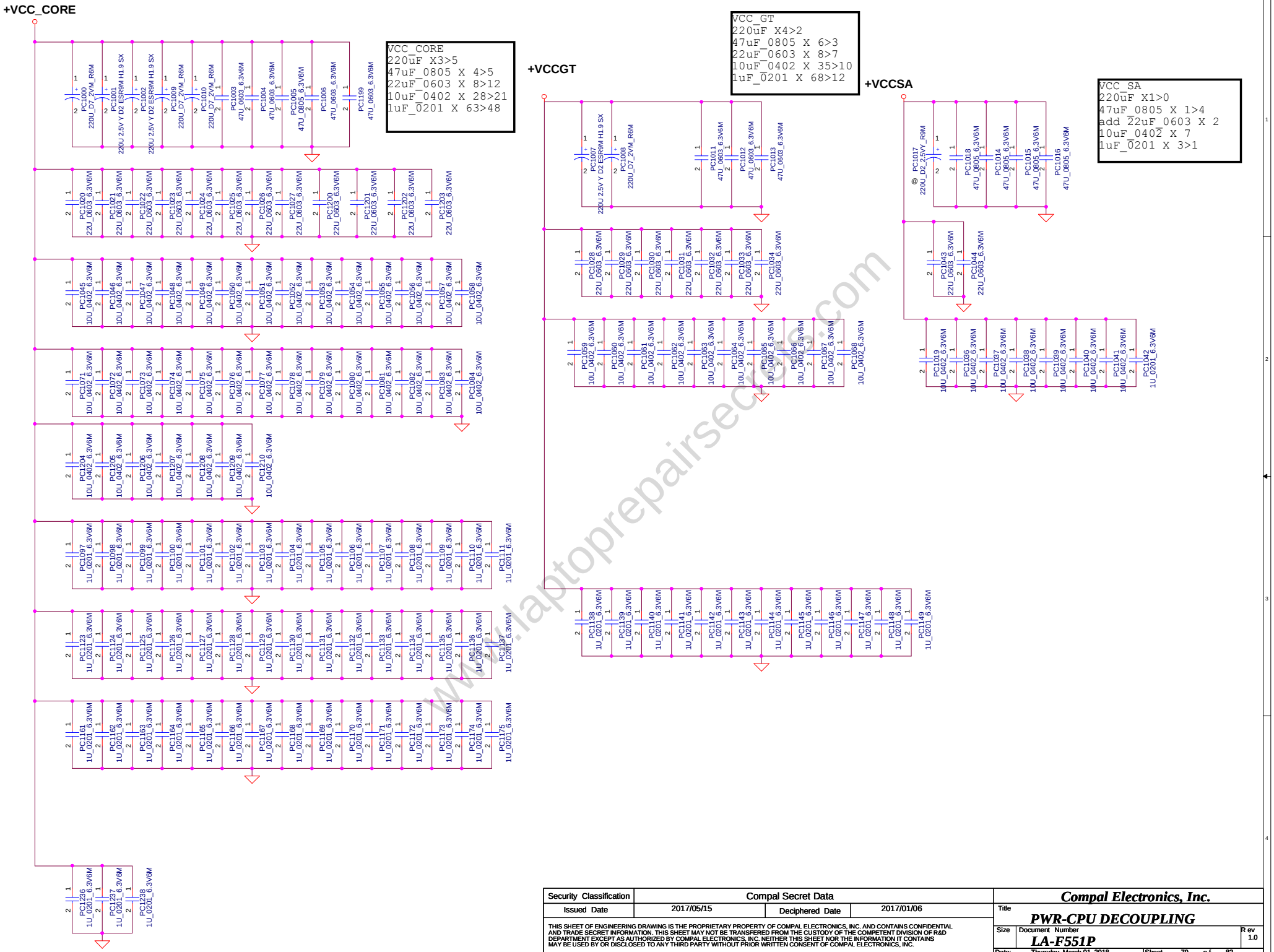


Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

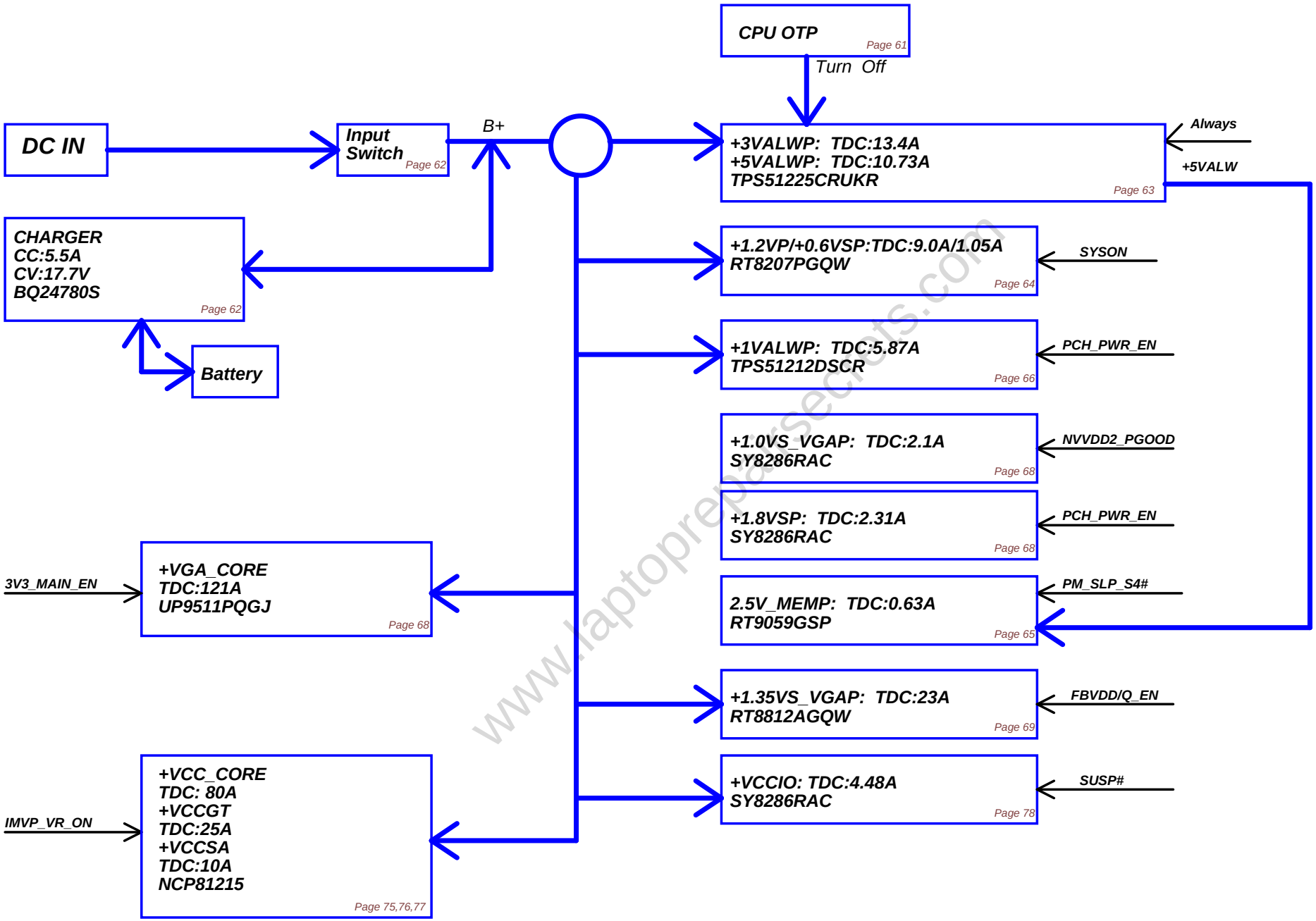
Compal Electronics, Inc.

Title: **PWR-CPU DECOUPLING**

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 | Sheet 79 of 82

Power block



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size	Document Number	Rev
	LA-F551P	1.0

Date: Thursday, March 01, 2018 Sheet 80 of 82

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.1.8VSP enable signal's sequence have wrong. Cause to PM_SLP_S5# pull low.	1.Change 1.8VSP enable signal change from SUSP# to PCH_PWR_EN. 2.Add enable signal pull high 10k ohm to +3VALW 3.PR807/PR808 un-pop.	0.1
2	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.Need another 1.8V supply to audio codec and usb retimer.	1.Add RT9013 LDO Circuit.	0.1
3	P.66	PWR_+1VALWP	2017/08/15	Compal_HW	1.Modify enable signal RC delay.	1.Change PR300 from o ohm to 100K ohm. 2.PC300 0.1uF pop.	0.1
4	P.75	PWR_VCORE_NCP81215	2017/08/17	Compal_PWR	1.PWR and HW side double pull high/down.	1.PR500,PR514,PR521,PR526,PR528,PR531 un-pop.	0.1
5	P.75	PWR_VCORE_NCP81215	2017/08/22	Compal_PWR	1.Modify ICCMAX=150A and OCP=180A.	1.Change PR558 from 100K ohm to 118K ohm. 2.Change PR541 from 27.4K ohm to 32.4K ohm.	0.1
6	P.67	PWR_+1.8VSP/ +1.8VSP_AUDIO	2017/09/04	Compal_HW	1.Modify 1.8VSP enable signal and RC delay time.	1.Delete PR817. 2.Add PR807 100K ohm. 3.Add PC811 0.1uF. 4.Add PR808 1M ohm.	0.1A
7	P.76/77	PWR_VCORE_+VCC_CORE/ +VCC_GT	2017/09/11	Compal_ME	1.CPU choke's height are difference with Cassini. VCORE and VCCGT 's choke height change from 3mm to 4mm.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001DC00 to SH00001EE00	0.2
8	P.67	PWR_+1.8VSP	2017/09/11	Compal_HW	1.Modify 1.8VS net name.	1.Net name +1.8VS change to +1.8VALW.	0.2
9	P.75	PWR_VCORE_NCP81215	2017/09/14	Compal_PWR	1.Change Choke DCR from 0.9mohm to 0.67mohm (+/-5%).Fine tune FB sense and CSCOMP RC value.	1.Change PR546,PR550,PR551,PR572 from 115K to 90.9K ohm. 2.Change PR557,PR587,PR581,PR582,PR595 from 1.62K to 2.21K ohm. 3.Change PR538 from 25.5K to 28.7K ohm. 4.Change PR549 from 100K to 90.9K ohm. 5.Change PC528 from 560pF to 680pF. 6.PC505,PC523 un-pop. 7.Change PC525,PC527 from 0.1uF to 0.22uF. 8.Change PR527 from 1Kohm to 1.37Kohm. 9.Change PR511 from 1.65Kohm to 1.58Kohm. 10.Change PR512 from 31.6Kohm to 28.7Kohm. 11.Change PC509 from 10nF to 15nF. 12.Change PC510 from 56pF to 100pF. 13.Change PR548 from 261Kohm to 249Kohm.	0.2
10	P.73	PWR_+1.55VRAM	2017/09/13	Compal_PW	1.Modify OCP resistor.	1.Change PR8206 from 8.66K ohm to 7.87K ohm.	0.2
11	P.61	DCIN / BATT CONN / OTP	2017/09/14	Compal_PW	1.Unify mos materials.	1.Change PQ9 from SB00000ZU00 to SB00000PV00.	0.2
12	P.61/70/71	DCIN / BATT CONN / OTP PWR_+NVVDD1	2017/09/26	Compal_EMI	1.EMI request to modify VIN beed and capcitor.	1.Change PL1,PL3 from SM01000P500 to SM01000DJ00. 2.Change PC2,PC4 from 100pF to 1000pF. 3.Change PC 6100,PC6117,PC6200 from 1uF to 0.1uF. 4.Change PC6104,PC6118,PC6204 from 1000pF to 2200pF.	0.2

Compal Electronics, Inc.

Title: PWR_PIR1

Size: | Document Number: LA-F551P | Rev: 1.0

Date: Thursday, March 01, 2018 | Sheet 81 of 82

Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
12	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.NCP81215 change PA0 version P/N.	1.Change PU500 from SA0000AQE00 to SA0000BNK10.	0.3
13	P.61	PWR_DCIN / BATT CONN / OTP	2017/12/14	Compal_PWR	1.Main source SB00000Z500 EOL.	1.Change PQ2 from SB00000Z500 to SB000002R00.	0.3
14	P.76/77	PWR_VCORE_+VCC_CORE	2017/12/14	Compal_PWR	1.Cytec choke SH00001DA00 VRTT fail 2.SA choke change common part include SH000015M00 & SH000015P00.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001EE00 to SH00001D800. 2.Change PL508 from SH000015M00 to SH00001ED00.	0.3
15	P.64/66/73	PWR_+1.2VP/+0.6VSP PWR_+1VALWP PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Because of polyma cap non equal substitue, all 220uF H=1.9 polyma cap are unified SGA00009800.	1.Change PC209,PC215,PC306,PC307,PC8207,PC8208 from SGA20221D40 to SGA00009800.	0.3
16	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.VRTT test for IA & GT main and 2nd Choke to fine tune IMON resistor.	1.Change PR534 from 24.9K to 26.7K. 2.Change PR538 from 28.7K to 30.9K.	0.3
17	P.72/73	PWR_+NVVDD2 PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Because thermal derating fail,we change capcitor type.	1.Change PC6442,PC6443,PC6444,PC6445 from SE00000M000 to SE00001CA00. 2.Change PC710,PC8200 from SE000006S80 to SE00000GC00.	0.3
18	P.73	PWR_+1.55VRAM	2017/12/18	Compal_PWR	1.Modify OCP resistor setting for main/2nd mos.	1.Change PR8206 from 7.87K to 7.5K.	0.3
19	all	all	2017/02/07	Compal_PWR	1.Change 0 ohm to short-pad.	1.Change PR100,PR112,PR114,PR1301,PR17,PR208,PR211,PR27,PR5001,PR5006, PR5007,PR5017,PR5018,PR508,PR510,PR517,PR523,PR524,PR525,PR529,PR531, PR552,PR556,PR563,PR566,PR567,PR568,PR573,PR576,PR585,PR590,PR591,PR594, PR6005,PR6015,PR6016,PR6018,PR6019,PR6021,PR6025,PR6031,PR6039,PR6044, PR6060,PR6107,PR6114,PR6205,PR6410,PR6421,PR6422,PR6428,PR6429,PR6431, PR6432,PR703,PR704,PR717,PR720,PR721,PR727,PR813,PR815,PR8216,PR8219, PR9000 from 0 ohm to short-pad.	0.3
20	P.68	P68-PWR_+1.0VS_VGA	2017/02/07	Compal_PWR	1.Bom control for 2nd GPU sequence IC.	1.PR801 0 ohm un-pop.	0.3

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