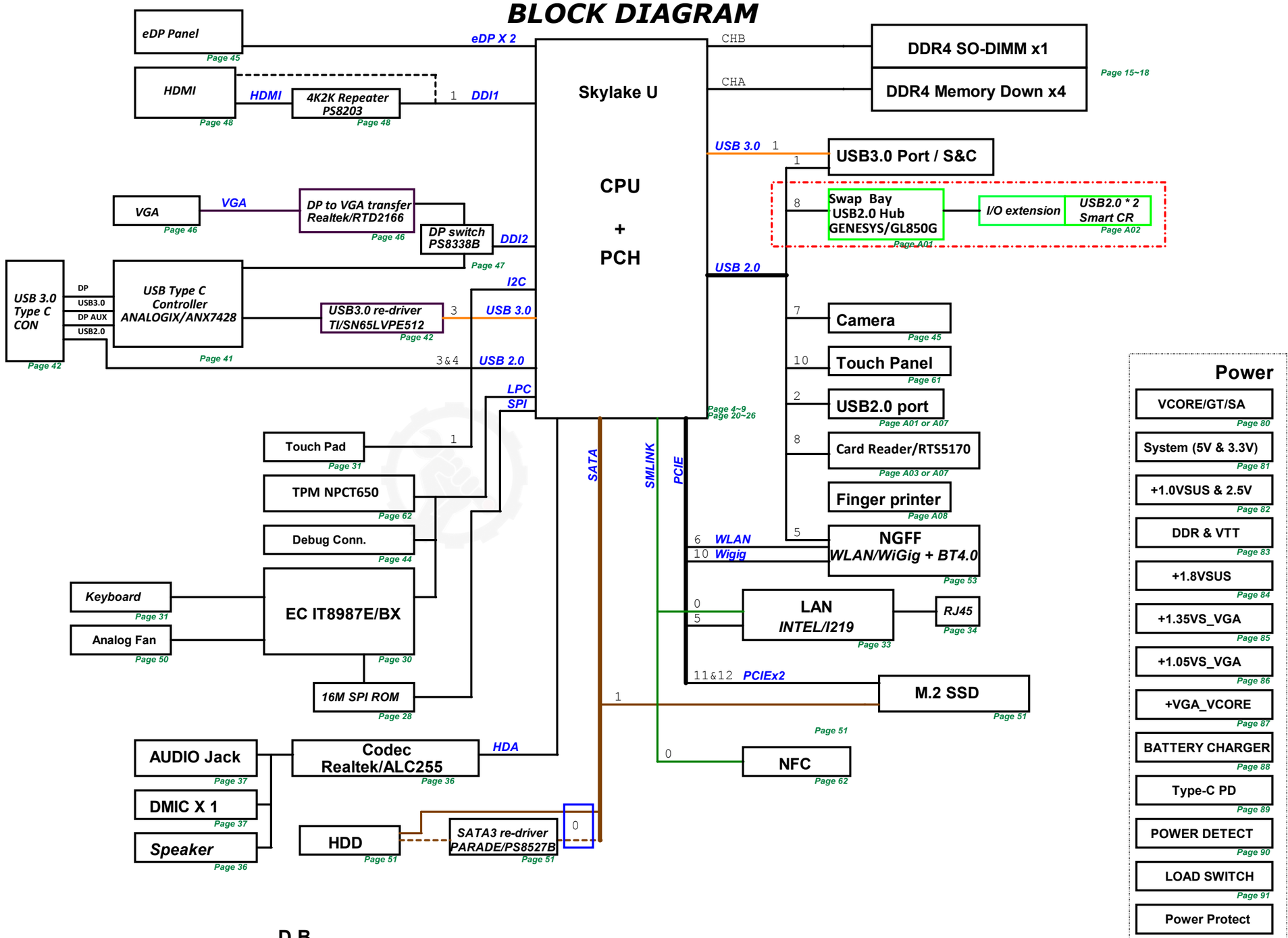
P4 Skylake U (2+2) Rev1.0

SYSTEM PAGE REF.

BLOCK DIAGRAM



Power

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- +1.0VSUS & 2.5V — Page 82
- DDR & VTT — Page 83
- +1.8VSUS — Page 84
- +1.35VS_VGA — Page 85
- +1.05VS_VGA — Page 86
- +VGA_VCORE — Page 87
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- Type-C PD — Page 89
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D.B.

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- LED DB — Page A04
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- KB LED DB — Page A06

<Variant Name>

PEGATRON Title : Block Diagram

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 1 of 108

<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
C	KTU_CSM	1.1

Date: Tuesday, September 06, 2016 Sheet 2 of 108

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

+VCCIO — +VCCIO 7,57,91
+VCCST_CPU — +VCCST_CPU 5,7,9,25
+VCCSTG — +VCCSTG 5,7
+3VS — +3VS 4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

U0301A

DDI Port 1: HDMI

48 HDMI_TXN2 — E55 DDI1_TXN[0]
48 HDMI_TXP2 — F55 DDI1_TXP[0]
48 HDMI_TXN1 — E58 DDI1_TXN[1]
48 HDMI_TXP1 — F58 DDI1_TXP[1]
48 HDMI_TXN0 — F53 DDI1_TXN[2]
48 HDMI_TXP0 — G53 DDI1_TXP[2]
48 HDMI_CLKN — F56 DDI1_TXN[3]
48 HDMI_CLKP — G56 DDI1_TXP[3]

DDI Port 2: DP Switch

47 DP2_TXN0 — C50 DDI2_TXN[0]
47 DP2_TXP0 — D50 DDI2_TXP[0]
47 DP2_TXN1 — C52 DDI2_TXN[1]
47 DP2_TXP1 — D52 DDI2_TXP[1]
47 DP2_TXN2 — A50 DDI2_TXN[2]
47 DP2_TXP2 — B50 DDI2_TXP[2]
47 DP2_TXN3 — D51 DDI2_TXN[3]
47 DP2_TXP3 — C51 DDI2_TXP[3]

DDI

DISPLAY SIDEBANDS

48 HDMI_SCL_PCH — L13 GPP_E18/DDPB_CTRLCLK
48 HDMI_SDA_PCH — HDMI_SDA_PCH — L12 GPP_E19/DDPB_CTRLDATA
DDPC_CTRLDATA — N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22
N12 GPP_E23

+VCCIO — R0301 2 1% 1 24.9Ohm — DP_COMP — E52 eDP_RCOMP

940432
01V010000015

EDP

EDP_TXN[0] C47 — EDP_TXN0 45
EDP_TXP[0] C46 — EDP_TXP0 45
EDP_TXN[1] D46 — EDP_TXN1 45
EDP_TXP[1] C45 — EDP_TXP1 45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

eDP x 2

EDP_AUXN E45 — EDP_AUXN 45
EDP_AUXP F45 — EDP_AUXP 45

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48 — DP2_AUXN 47
DDI2_AUXP F48 — DP2_AUXP 47
RSVD_1 G46
RSVD_2 F46

GPP_E13/DDPB_HPD0 L9 — DPB_HPD 48
GPP_E14/DDPC_HPD1 L7 — DP2_HPD 47
GPP_E15/DDPD_HPD2 L6 — EXT_SMI# R 0302 1 2 0Ohm EXT_SMI# — EXT_SMI# 30,44
GPP_E16/DDPE_HPD3 N9 — EXT_SCI# R 0303 1 2 0Ohm EXT_SCI# — EXT_SCI# 30
GPP_E17/EDP_HPD L10 — eDP_HPD — eDP_HPD 45

Pull down at connector side

eDP_BKLTEN R12 — LCD_BKLTEN_PCH 21,45
eDP_BKLTCTL R11 — LCD_BL_PWM_PCH 45
eDP_VDDEN U13 — EDP_VDD_EN 45

+VCCST_CPU — R0311 1KOhm
+VCCSTG — R0312 1KOhm
H_PROCHOT# — R0314 1 1% 2 499Ohm — 30 H_PECI_EC

+VCCST_CPU — R0313 49.9Ohm 1% @

U0301D

TP_CATERR# R — D63 CATERR#
R0315 1 2 43Ohm — H_PECI — A54 PECI
H_PROCHOT#_R — C65 PROCHOT#
SP0301 — H_THRMTRIP#_R — C63 THERMTRIP#
T0310 — SKTOCC# — A65 SKTOCC#

CPU MISC

C55 BPM#[0]
D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

T0312 — CPU_GP0 — A6 GPP_E3/CPU_GP0
T0311 — CPU_GP1 — A7 GPP_E7/CPU_GP1
T0313 — CPU_GP2 — BA5 GPP_B3/CPU_GP2
T0314 — CPU_GP3 — AY5 GPP_B4/CPU_GP3

R0316 1 1% 2 49.9Ohm — CPU_POPIRCOMP — AT16 PROC_POPIRCOMP
R0317 1 1% 2 49.9Ohm — PCH_POPIRCOMP — AU16 PCH_OPIRCOMP
R0318 1 1% 2 49.9Ohm — EDRAM_OPIO_RCOMP — H66 OPCE_RCOMP
R0319 1 1% 2 49.9Ohm — EOPIO_RCOMP — H65 OPC_RCOMP

JTAG

PROC_TCK — B61 XDP_TCLK 1 — T0315
PROC_TDI — D60 XDP_TDI_CPU 1 — T0316
PROC_TDO — A61 XDP_TDO_CPU 1 — T0317
PROC_TMS — C60 XDP_TMS_CPU 1 — T0318
PROC_TRST# — B59 XDP_TRST_CPU_N 1 — T0319

PCH_JTAG_TCK — B56 PCH_JTAG_TCLK 1 — T0320
PCH_JTAG_TDI — D59 PCH_JTAG_TDI 1 — T0321
PCH_JTAG_TDO — A56 PCH_JTAG_TDO 1 — T0322
PCH_JTAG_TMS — C59 PCH_JTAG_TMS 1 — T0323
PCH_TRST# — C61 PCH_TRST_CPU_N 1 — T0324
JTAGX — A59 XDP_TCLK_JTAGX 1 — T0325

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30 THRO_CPU — Q0301 2N7002 — R0341 2 1 0Ohm — H_PROCHOT#

R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result),預留0ohm是調整空間

88 PROCHOT# — SP0325 N/A 2 1 0Ohm
80 VR_HOT# — R0320 2 @ 1 0Ohm

DDPB_CTRLDATA has pull high at connector side

+3VS
HDMI_SDA_PCH — R0304 1 @ 2 2.2KOhm
DDPC_CTRLDATA — R0321 1 2 2.2KOhm

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
  1 : port is deteccted

+3VS
EXT_SCI# — R0307 1 2 10KOhm
EXT_SMI# — R0308 1 2 10KOhm

Table 5-10. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect

PEGATRON
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Title : CPU(1)_DDI/eDP
BG1/HW3
Engineer: Bill Yang
Size: Custom
Project Name: P4
Rev: 1.0
Date: Tuesday, September 06, 2016
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+1.2V +1.2V 7,15,16,17,18,57,83
+3VSUS +3VSUS 24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+3VS +3VS 3,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

M_A_A[16:0] 15,16
M_A_DQS#[7:0] 16
M_A_DQS[7:0] 16

M_B_A[16:0] 17
M_B_DQS#[7:0] 17
M_B_DQS[7:0] 17

16 M_A_D[63:0]

U0301B

IL Channel A[0..63]

NIL Channel A[0..15]
NIL Channel A[32..47]
NIL Channel B[0..15]
NIL Channel B[32..47]

M_A_D0	AL71	DDR0_DQ[0]	DDR1_DQ[8]
M_A_D1	AL68	DDR0_DQ[1]	DDR1_DQ[9]
M_A_D2	AN68	DDR0_DQ[2]	DDR1_DQ[10]
M_A_D3	AN69	DDR0_DQ[3]	DDR1_DQ[11]
M_A_D4	AL70	DDR0_DQ[4]	DDR1_DQ[12]
M_A_D5	AL69	DDR0_DQ[5]	DDR1_DQ[13]
M_A_D6	AN70	DDR0_DQ[6]	DDR1_DQ[14]
M_A_D7	AN71	DDR0_DQ[7]	DDR1_DQ[15]
M_A_D8	AR70	DDR0_DQ[8]	DDR1_DQ[32]
M_A_D9	AR68	DDR0_DQ[9]	DDR1_DQ[33]
M_A_D10	AU71	DDR0_DQ[10]	DDR1_DQ[34]
M_A_D11	AU68	DDR0_DQ[11]	DDR1_DQ[35]
M_A_D12	AR71	DDR0_DQ[12]	DDR1_DQ[36]
M_A_D13	AR69	DDR0_DQ[13]	DDR1_DQ[37]
M_A_D14	AU70	DDR0_DQ[14]	DDR1_DQ[38]
M_A_D15	AU69	DDR0_DQ[15]	DDR1_DQ[39]
M_A_D16	BB65	DDR0_DQ[16]	DDR0_DQ[32]
M_A_D17	AW65	DDR0_DQ[17]	DDR0_DQ[33]
M_A_D18	AW63	DDR0_DQ[18]	DDR0_DQ[34]
M_A_D19	AY63	DDR0_DQ[19]	DDR0_DQ[35]
M_A_D20	BA65	DDR0_DQ[20]	DDR0_DQ[36]
M_A_D21	AY65	DDR0_DQ[21]	DDR0_DQ[37]
M_A_D22	BA63	DDR0_DQ[22]	DDR0_DQ[38]
M_A_D23	BB63	DDR0_DQ[23]	DDR0_DQ[39]
M_A_D24	BA61	DDR0_DQ[24]	DDR0_DQ[40]
M_A_D25	AW61	DDR0_DQ[25]	DDR0_DQ[41]
M_A_D26	BB59	DDR0_DQ[26]	DDR0_DQ[42]
M_A_D27	AW59	DDR0_DQ[27]	DDR0_DQ[43]
M_A_D28	BB61	DDR0_DQ[28]	DDR0_DQ[44]
M_A_D29	AY61	DDR0_DQ[29]	DDR0_DQ[45]
M_A_D30	BA59	DDR0_DQ[30]	DDR0_DQ[46]
M_A_D31	AY59	DDR0_DQ[31]	DDR0_DQ[47]
M_A_D32	AY39	DDR0_DQ[32]	DDR1_DQ[0]
M_A_D33	AW39	DDR0_DQ[33]	DDR1_DQ[1]
M_A_D34	AY37	DDR0_DQ[34]	DDR1_DQ[2]
M_A_D35	AW37	DDR0_DQ[35]	DDR1_DQ[3]
M_A_D36	BB39	DDR0_DQ[36]	DDR1_DQ[4]
M_A_D37	BA39	DDR0_DQ[37]	DDR1_DQ[5]
M_A_D38	BA37	DDR0_DQ[38]	DDR1_DQ[6]
M_A_D39	BB37	DDR0_DQ[39]	DDR1_DQ[7]
M_A_D40	AY35	DDR0_DQ[40]	DDR1_DQ[8]
M_A_D41	AW35	DDR0_DQ[41]	DDR1_DQ[9]
M_A_D42	AY33	DDR0_DQ[42]	DDR1_DQ[10]
M_A_D43	AW33	DDR0_DQ[43]	DDR1_DQ[11]
M_A_D44	BB35	DDR0_DQ[44]	DDR1_DQ[12]
M_A_D45	BA35	DDR0_DQ[45]	DDR1_DQ[13]
M_A_D46	BA33	DDR0_DQ[46]	DDR1_DQ[14]
M_A_D47	BB33	DDR0_DQ[47]	DDR1_DQ[15]
M_A_D48	AY31	DDR0_DQ[48]	DDR1_DQ[32]
M_A_D49	AW31	DDR0_DQ[49]	DDR1_DQ[33]
M_A_D50	AY29	DDR0_DQ[50]	DDR1_DQ[34]
M_A_D51	AW29	DDR0_DQ[51]	DDR1_DQ[35]
M_A_D52	BB31	DDR0_DQ[52]	DDR1_DQ[36]
M_A_D53	BA31	DDR0_DQ[53]	DDR1_DQ[37]
M_A_D54	BA29	DDR0_DQ[54]	DDR1_DQ[38]
M_A_D55	BB29	DDR0_DQ[55]	DDR1_DQ[39]
M_A_D56	AY27	DDR0_DQ[56]	DDR1_DQ[40]
M_A_D57	AW27	DDR0_DQ[57]	DDR1_DQ[41]
M_A_D58	AY25	DDR0_DQ[58]	DDR1_DQ[42]
M_A_D59	AW25	DDR0_DQ[59]	DDR1_DQ[43]
M_A_D60	BB27	DDR0_DQ[60]	DDR1_DQ[44]
M_A_D61	BA27	DDR0_DQ[61]	DDR1_DQ[45]
M_A_D62	BA25	DDR0_DQ[62]	DDR1_DQ[46]
M_A_D63	BB25	DDR0_DQ[63]	DDR1_DQ[47]

DDR0_CKN[0]	AU53		
DDR0_CKP[0]	AT53		M_A_DIM0_CLK#0 15,16
DDR0_CKN[1]	AU55		M_A_DIM0_CLK0 15,16
DDR0_CKP[1]	AT55		
DDR0_CKE[0]	BA56		
DDR0_CKE[1]	BB56		M_A_DIM0_CKE0 15,16
DDR0_CKE[2]	AW56		
DDR0_CKE[3]	AY56		
DDR0_CS#[0]	AU45		
DDR0_CS#[1]	AU43		M_A_DIM0_CS#0 15,16
DDR0_ODT[0]	AT45		M_A_DIM0_ODT0 15,16
DDR0_ODT[1]	AT43		
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BA51	M_A_A5	
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BB54	M_A_A9	
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	BA52	M_A_A6	
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AY52	M_A_A8	
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AW52	M_A_A7	
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AY55		M_A_BG0 15,16
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	AW54	M_A_A12	
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA54	M_A_A11	
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	BA55		M_A_ACT# 15,16
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]	AY54		M_A_BG1 15,16
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU46	M_A_A13	
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_A15	
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_A14	
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_A16	
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52		M_A_BA0 15,16
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_A2	
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48		M_A_BA1 15,16
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_A10	
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	BB50	M_A_A1	
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_A0	
DDR0_MA[3]	BA50	M_A_A3	
DDR0_MA[4]	BB52	M_A_A4	

DDR0_DQSN[0]	AM70	M_A_DQS#0	
DDR0_DQSP[0]	AM69	M_A_DQS0	
DDR0_DQSN[1]	AT69	M_A_DQS#1	
DDR0_DQSP[1]	AT70	M_A_DQS1	
DDR0_DQSN[2]	BA64	M_A_DQS#2	
DDR0_DQSP[2]	AY64	M_A_DQS2	
DDR0_DQSN[3]	AY60	M_A_DQS#3	
DDR0_DQSP[3]	BA60	M_A_DQS3	
DDR0_DQSN[4]	BA38	M_A_DQS#4	
DDR0_DQSP[4]	AY38	M_A_DQS4	
DDR0_DQSN[5]	AY34	M_A_DQS#5	
DDR0_DQSP[5]	BA34	M_A_DQS5	
DDR0_DQSN[6]	BA30	M_A_DQS#6	
DDR0_DQSP[6]	AY30	M_A_DQS6	
DDR0_DQSN[7]	AY26	M_A_DQS#7	
DDR0_DQSP[7]	BA26	M_A_DQS7	

IL Channel A DQS[0..7]
NIL Channel A DQS[0,1,4,5]
NIL Channel B DQS[0,1,4,5]
DDR CH - A

DDR0_ALERT#	AW50		M_A_ALERT# 15,16
DDR0_PAR	AT52		M_A_PAR 15,16
DDR_VREF_CA	AY67		DIMM0_VREF_CA 18
DDR0_VREF_DQ	AY68	DDR0_VREF_DQ 1 T0401	
DDR1_VREF_DQ	BA67		DIMM1_VREF_DQ 18
DDR_VTT_CNTL	AW67	DDR_PG_CTRL_S	

940432

17 M_B_D[63:0]

U0301C

SKL_ULT

IL Channel B[0..63]

NIL Channel A[16..31]
NIL Channel A[48..63]
NIL Channel B[16..31]
NIL Channel B[48..63]

M_B_D0	AF65	DDR1_DQ[0]	DDR0_DQ[16]
M_B_D1	AF64	DDR1_DQ[1]	DDR0_DQ[17]
M_B_D2	AK65	DDR1_DQ[2]	DDR0_DQ[18]
M_B_D3	AK64	DDR1_DQ[3]	DDR0_DQ[19]
M_B_D4	AF66	DDR1_DQ[4]	DDR0_DQ[20]
M_B_D5	AF67	DDR1_DQ[5]	DDR0_DQ[21]
M_B_D6	AK67	DDR1_DQ[6]	DDR0_DQ[22]
M_B_D7	AK66	DDR1_DQ[7]	DDR0_DQ[23]
M_B_D8	AF70	DDR1_DQ[8]	DDR0_DQ[24]
M_B_D9	AF68	DDR1_DQ[9]	DDR0_DQ[25]
M_B_D10	AH71	DDR1_DQ[10]	DDR0_DQ[26]
M_B_D11	AH68	DDR1_DQ[11]	DDR0_DQ[27]
M_B_D12	AF71	DDR1_DQ[12]	DDR0_DQ[28]
M_B_D13	AF69	DDR1_DQ[13]	DDR0_DQ[29]
M_B_D14	AH70	DDR1_DQ[14]	DDR0_DQ[30]
M_B_D15	AH69	DDR1_DQ[15]	DDR0_DQ[31]
M_B_D16	AT66	DDR1_DQ[16]	DDR0_DQ[48]
M_B_D17	AU66	DDR1_DQ[17]	DDR0_DQ[49]
M_B_D18	AP65	DDR1_DQ[18]	DDR0_DQ[50]
M_B_D19	AN65	DDR1_DQ[19]	DDR0_DQ[51]
M_B_D20	AN66	DDR1_DQ[20]	DDR0_DQ[52]
M_B_D21	AP66	DDR1_DQ[21]	DDR0_DQ[53]
M_B_D22	AT65	DDR1_DQ[22]	DDR0_DQ[54]
M_B_D23	AU65	DDR1_DQ[23]	DDR0_DQ[55]
M_B_D24	AT61	DDR1_DQ[24]	DDR0_DQ[56]
M_B_D25	AU61	DDR1_DQ[25]	DDR0_DQ[57]
M_B_D26	AP60	DDR1_DQ[26]	DDR0_DQ[58]
M_B_D27	AN60	DDR1_DQ[27]	DDR0_DQ[59]
M_B_D28	AN61	DDR1_DQ[28]	DDR0_DQ[60]
M_B_D29	AP61	DDR1_DQ[29]	DDR0_DQ[61]
M_B_D30	AT60	DDR1_DQ[30]	DDR0_DQ[62]
M_B_D31	AU60	DDR1_DQ[31]	DDR0_DQ[63]
M_B_D32	AU40	DDR1_DQ[32]	DDR1_DQ[16]
M_B_D33	AT40	DDR1_DQ[33]	DDR1_DQ[17]
M_B_D34	AT37	DDR1_DQ[34]	DDR1_DQ[18]
M_B_D35	AU37	DDR1_DQ[35]	DDR1_DQ[19]
M_B_D36	AR40	DDR1_DQ[36]	DDR1_DQ[20]
M_B_D37	AP40	DDR1_DQ[37]	DDR1_DQ[21]
M_B_D38	AP37	DDR1_DQ[38]	DDR1_DQ[22]
M_B_D39	AR37	DDR1_DQ[39]	DDR1_DQ[23]
M_B_D40	AT33	DDR1_DQ[40]	DDR1_DQ[24]
M_B_D41	AU33	DDR1_DQ[41]	DDR1_DQ[25]
M_B_D42	AU30	DDR1_DQ[42]	DDR1_DQ[26]
M_B_D43	AT30	DDR1_DQ[43]	DDR1_DQ[27]
M_B_D44	AR33	DDR1_DQ[44]	DDR1_DQ[28]
M_B_D45	AP33	DDR1_DQ[45]	DDR1_DQ[29]
M_B_D46	AR30	DDR1_DQ[46]	DDR1_DQ[30]
M_B_D47	AP30	DDR1_DQ[47]	DDR1_DQ[31]
M_B_D48	AU27	DDR1_DQ[48]	
M_B_D49	AT27	DDR1_DQ[49]	
M_B_D50	AT25	DDR1_DQ[50]	
M_B_D51	AU25	DDR1_DQ[51]	
M_B_D52	AP27	DDR1_DQ[52]	
M_B_D53	AN27	DDR1_DQ[53]	
M_B_D54	AN25	DDR1_DQ[54]	
M_B_D55	AP25	DDR1_DQ[55]	
M_B_D56	AT22	DDR1_DQ[56]	
M_B_D57	AU22	DDR1_DQ[57]	
M_B_D58	AU21	DDR1_DQ[58]	
M_B_D59	AT21	DDR1_DQ[59]	
M_B_D60	AN22	DDR1_DQ[60]	
M_B_D61	AP22	DDR1_DQ[61]	
M_B_D62	AP21	DDR1_DQ[62]	
M_B_D63	AN21	DDR1_DQ[63]	

DDR1_CKN[0]	AN45		
DDR1_CKN[1]	AN46	M_B_DIM0_CLK#1	M_B_DIM0_CLK#0 17
DDR1_CKP[0]	AP45		M_B_DIM0_CLK#1 17
DDR1_CKP[1]	AP46	M_B_DIM0_CLK1	M_B_DIM0_CLK0 17
DDR1_CKE[0]	AN56		M_B_DIM0_CLK1 17
DDR1_CKE[1]	AP55		M_B_DIM0_CKE0 17
DDR1_CKE[2]	AN55		M_B_DIM0_CKE1 17
DDR1_CKE[3]	AP53		
DDR1_CS#[0]	BB42		
DDR1_CS#[1]	AY42		M_B_DIM0_CS#0 17
DDR1_ODT[0]	BA42		M_B_DIM0_CS#1 17
DDR1_ODT[1]	AW42		M_B_DIM0_ODT0 17
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AY48	M_B_A5	M_B_DIM0_ODT1 17
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	AP50	M_B_A9	
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	BA48	M_B_A6	
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	BB48	M_B_A8	
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AP48	M_B_A7	
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AP52		M_B_BG0 17
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AN50	M_B_A12	
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AN48	M_B_A11	
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AN53		M_B_ACT# 17
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	AN52		M_B_BG1 17
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	BA43	M_B_A13	
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AY43	M_B_A15	
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AY44	M_B_A14	
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AW44	M_B_A16	
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	BB44		
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AY47	M_B_A2	M_B_BA0 17
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	BA44		M_B_BA1 17
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AW46	M_B_A10	
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AY46	M_B_A1	
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	BA46	M_B_A0	
DDR1_MA[3]	BB46	M_B_A3	
DDR1_MA[4]	BA47	M_B_A4	

DDR1_DQSN[0]/DDR0_DQSN[2]	AH66	M_B_DQS#0	
DDR1_DQSP[0]/DDR0_DQSP[2]	AH65	M_B_DQS0	
DDR1_DQSN[1]/DDR0_DQSN[3]	AG69	M_B_DQS#1	
DDR1_DQSP[1]/DDR0_DQSP[3]	AG70	M_B_DQS1	
DDR1_DQSN[2]/DDR0_DQSN[6]	AR66	M_B_DQS#2	
DDR1_DQSP[2]/DDR0_DQSP[6]	AR65	M_B_DQS2	
DDR1_DQSN[3]/DDR0_DQSN[7]	AR61	M_B_DQS#3	
DDR1_DQSP[3]/DDR0_DQSP[7]	AR60	M_B_DQS3	
DDR1_DQSN[4]/DDR1_DQSN[2]	AT38	M_B_DQS#4	
DDR1_DQSP[4]/DDR1_DQSP[2]	AR38	M_B_DQS4	
DDR1_DQSN[5]/DDR1_DQSN[3]	AT32	M_B_DQS#5	
DDR1_DQSP[5]/DDR1_DQSP[3]	AR32	M_B_DQS5	
DDR1_DQSN[6]	AR25	M_B_DQS#6	
DDR1_DQSP[6]	AR27	M_B_DQS6	
DDR1_DQSN[7]	AR22	M_B_DQS#7	
DDR1_DQSP[7]	AR21	M_B_DQS7	

NIL Channel A DQS[2,3,6,7]
NIL Channel B DQS[2,3,6,7]
DDR CH - B

DDR1_ALERT#	AN43		M_B_ALERT# 17
DDR1_PAR	AP43		M_B_PAR 17
DRAM_RESET#	AT13	CPUDRAMRST#	
DDR_RCOMP[0]	AR18	SM_RCOMP_0	R0402 1 1% 2 121OHM
DDR_RCOMP[1]	AT18	SM_RCOMP_1	R0403 1 1% 2 80.6Ohm
DDR_RCOMP[2]	AU18	SM_RCOMP_2	R0404 1 1% 2 100Ohm

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If Mixed SO-DIMM and Memory Down, RCOMP[0] should be 121 Ohm.

+1.2V
R0405 470Ohm
R0401 0Ohm
DDR4_DRAMRST# 16,17
C0402 0.1UF/16V

U0401
74AUP1G07GW
C0401 0.1UF/16V
+3VS
R0407 220KOhm 1%
+3VSUS
R0408 220KOhm @1%
R0411 2MOHM @
DDR_PG_CTRL 83

DDR_VTT_CNTL to VTT power ready < 35us (tCPU18)

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Title : CPU(2)_DDR3L
BG1/HW3
Engineer: Bill Yang
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+VCORE +VCORE 57,80
+VCCSTG +VCCSTG 3,7
+VCCST_CPU +VCCST_CPU 3,7,9,25

+VCORE

U0301L

CPU POWER 1 OF 4

A30	VCC_1	VCC_19	G32
A34	VCC_2	VCC_20	G33
A39	VCC_3	VCC_21	G35
A44	VCC_4	VCC_22	G37
AK33	VCC_5	VCC_23	G38
AK35	VCC_6	VCC_24	G40
AK37	VCC_7	VCC_25	G42
AK38	VCC_8	VCC_26	J30
AK40	VCC_9	VCC_27	J33
AL33	VCC_10	VCC_28	J37
AL37	VCC_11	VCC_29	J40
AL40	VCC_12	VCC_30	K33
AM32	VCC_13	VCC_31	K35
AM33	VCC_14	VCC_32	K37
AM35	VCC_15	VCC_33	K38
AM37	VCC_16	VCC_34	K40
AM38	VCC_17	VCC_35	K42
G30	VCC_18	VCC_36	K43
K32	RSVD_3	VCC_SENSE	E32
AK32	RSVD_4	VSS_SENSE	E33
AB62	VCCOPC_1	VIDALERT#	B63
P62	VCCOPC_2	VIDSCK	A63
V62	VCCOPC_3	VIDSOUT	D64
H63	VCC_OPC_1P8_1	VCCSTG	G20
G61	VCC_OPC_1P8_2		
AC63	VCCOPC_SENSE		
AE63	VSSOPC_SENSE		
AE62	VCCEOPIO_1		
AG62	VCCEOPIO_2		
AL63	VCCEOPIO_SENSE		
AJ62	VSSEOPIO_SENSE		

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01V010000015

CPU side | VR side

VCORE_VCCSENSE 80
VCORE_VSSSENSE 80

VIDALERT# R0517 1 1% 2 220Ohm
VIDSCK R0518 2 1 0Ohm
VIDSOUT R0519 2 1 0Ohm

+VCCFUSEPRG SP0505 1 2
NB_R0402_20MIL_SMALL

+VCCSTG

+VCCST_CPU
R0520 56Ohm 1%

+VCCST_CPU
R0521 100Ohm 1%

+VCCST_CPU
R0523 100Ohm 1%

+VCCST_CPU
R0522 45.3Ohm 1%
C0505 0.1UF/16V @

R0524 2 1 0Ohm VR_SVID_ALERT# 80

VIDALERT# R
VIDSCK_R

R0525 1 1% 2 51Ohm VR_SVID_CLK 80

VIDSOUT_R

R0526 1 1% 2 10Ohm VR_SVID_DATA 80

+VCORE
R0540 100Ohm 1%
VCORE_VCCSENSE
VCORE_VSSSENSE
R0541 100Ohm 1%

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Title : CPU(3)_+VCCCORE

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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+VCCGT

+VCCGT +VCCGT 57,80

U0301M

CPU POWER 2 OF 4

A48	VCCGT_1		VCCGT_56	N70	+VCCGT
A53	VCCGT_2		VCCGT_57	N71	
A58	VCCGT_3		VCCGT_58	R63	
A62	VCCGT_4		VCCGT_59	R64	
A66	VCCGT_5		VCCGT_60	R65	
AA63	VCCGT_6		VCCGT_61	R66	
AA64	VCCGT_7		VCCGT_62	R67	
AA66	VCCGT_8		VCCGT_63	R68	
AA67	VCCGT_9		VCCGT_64	R69	
AA69	VCCGT_10		VCCGT_65	R70	
AA70	VCCGT_11		VCCGT_66	R71	
AA71	VCCGT_12		VCCGT_67	T62	
AC64	VCCGT_13		VCCGT_68	U65	
AC65	VCCGT_14		VCCGT_69	U68	
AC66	VCCGT_15		VCCGT_70	U71	
AC67	VCCGT_16		VCCGT_71	W63	
AC68	VCCGT_17		VCCGT_72	W64	
AC69	VCCGT_18		VCCGT_73	W65	
AC70	VCCGT_19		VCCGT_74	W66	
AC71	VCCGT_20		VCCGT_75	W67	
J43	VCCGT_21		VCCGT_76	W68	
J45	VCCGT_22		VCCGT_77	W69	
J46	VCCGT_23		VCCGT_78	W70	
J48	VCCGT_24		VCCGT_79	W71	
J50	VCCGT_25		VCCGT_80	Y62	
J52	VCCGT_26				
J53	VCCGT_27		VccGTx_1	AK42	
J55	VCCGT_28		VccGTx_2	AK43	
J56	VCCGT_29		VccGTx_3	AK45	
J58	VCCGT_30		VccGTx_4	AK46	
J60	VCCGT_31		VccGTx_5	AK48	
K48	VCCGT_32		VccGTx_6	AK50	
K50	VCCGT_33		VccGTx_7	AK52	
K52	VCCGT_34		VccGTx_8	AK53	
K53	VCCGT_35		VccGTx_9	AK55	
K55	VCCGT_36		VccGTx_10	AK56	
K56	VCCGT_37		VccGTx_11	AK58	
K58	VCCGT_38		VccGTx_12	AK60	
K60	VCCGT_39		VccGTx_13	AK70	
L62	VCCGT_40		VccGTx_14	AL43	
L63	VCCGT_41		VccGTx_15	AL46	
L64	VCCGT_42		VccGTx_16	AL50	
L65	VCCGT_43		VccGTx_17	AL53	
L66	VCCGT_44		VccGTx_18	AL56	
L67	VCCGT_45		VccGTx_19	AL60	
L68	VCCGT_46		VccGTx_20	AM48	
L69	VCCGT_47		VccGTx_21	AM50	
L70	VCCGT_48		VccGTx_22	AM52	
L71	VCCGT_49		VccGTx_23	AM53	
M62	VCCGT_50		VccGTx_24	AM56	
N63	VCCGT_51		VccGTx_25	AM58	
N64	VCCGT_52		VccGTx_26	AU58	
N66	VCCGT_53		VccGTx_27	AU63	
N67	VCCGT_54		VccGTx_28	BB57	
N69	VCCGT_55		VccGTx_29	BB66	
VCCGT_VCCSENSE J70	VCCGT_SENSE		VCCGTx_SENSE	AK62	
VCCGT_VSSSENSE J69	VSSGT_SENSE		VSSGTx_SENSE	AL61	

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01V010000015

+VCCGT

R0611
100Ohm
1%

80 VCCGT_VCCSENSE
80 VCCGT_VSSSENSE

VCCGT_VCCSENSE
VCCGT_VSSSENSE

R0610
100Ohm
1%

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Title : CPU(4)_+VCCGT

BG1/HW3

Engineer: Bill Yang

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Custom	P4	1.0

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+1.2V — +1.2V 4,15,16,17,18,57,83

+VCCST_CPU — +VCCST_CPU 3,5,9,25

+VCCSTG — +VCCSTG 3,5

+VCCIO — +VCCIO 3,57,91

+VCCSA — +VCCSA 57,80

+5VSUS — +5VSUS 41,42,52,56,67,81

+12VSUS — +12VSUS 81,91

+1.0V — +1.0V 57,91

+1.2V — JP0701 (1 2) — 3MM_OPEN_5MIL — +VDDQ_CPU

C0701 - C0704 : Near by package
C0705 - C0710 : Underneath the package

2.8A

C0701 10UF/6.3V
C0702 10UF/6.3V
C0703 10UF/6.3V
C0704 10UF/6.3V
C0705 10UF/6.3V
C0706 10UF/6.3V
C0707 1UF/6.3V
C0708 1UF/6.3V
C0709 1UF/6.3V
C0710 1UF/6.3V

U0301N
CPU POWER 3 OF 4

VDDQ_1 AU23
VDDQ_2 AU28
VDDQ_3 AU35
VDDQ_4 AU42
VDDQ_5 BB23
VDDQ_6 BB32
VDDQ_7 BB41
VDDQ_8 BB47
VDDQ_9 BB51

+VDDQ_CPU — R0701 1 — 2 0Ohm — +VDDQ_CPU_CLK

Decoupling cap for internal power

VDDQC AM40
C0711 0.1UF/16V

VCCST A18
+VCCST_CPU
C0712 1UF/6.3V

VCCSTG A22
+VCCSTG
C0713 1UF/6.3V

0.1A
VCCPLL_OC AL23
+VCCSFR_OC
C0714 0.1UF/16V

VccPLL_1 K20
VccPLL_2 K21
+VCCSFR
C0715 0.1UF/16V
C0716 0.1UF/16V

940432
01V010000015

VCCIO_1 AK28
VCCIO_2 AK30
VCCIO_3 AL30
VCCIO_4 AL42
VCCIO_5 AM28
VCCIO_6 AM30
VCCIO_7 AM42

+VCCIO
C0717 1UF/6.3V
C0718 1UF/6.3V
C0719 1UF/6.3V
C0720 1UF/6.3V

VCCSA_1 AK23
VCCSA_2 AK25
VCCSA_3 G23
VCCSA_4 G25
VCCSA_5 G27
VCCSA_6 G28
VCCSA_7 J22
VCCSA_8 J23
VCCSA_9 J27
VCCSA_10 K23
VCCSA_11 K25
VCCSA_12 K27
VCCSA_13 K28
VCCSA_14 K30

4.5A

+VCCSA

VCCIO_SENSE AM23 VCCIO_VR_FB
VSSIO_SENSE AM22 VSSIO_VR_FB

VSSSA_SENSE H21 — VCCSA_VSSSENSE 80
VCCSA_SENSE H20 — VCCSA_VCCSENSE 80

+VCCIO
R0714 1KOhm @
R0715 1KOhm @

Reserved PH/PD

+VCCSA
R0720 100Ohm 1%
VCCSA_VCCSENSE
VCCSA_VSSSENSE
R0721 100Ohm 1%

+1.0V — 0.24A — R0710 1 — 2 0Ohm — 0.24A — +VCCST_CPU
RES 0 OHM 1/10W (0603) JUMP

+1.0V — 0.24A — R0711 1 — 2 0Ohm — 0.24A — +VCCSFR
RES 0 OHM 1/10W (0603) JUMP

+1.2V — R0709 1 — 2 0Ohm — +VCCSFR_OC
Refer to CRB 0.53
RES 0 OHM 1/10W (0603) JUMP

+VCCIO — 0.12A — R0713 1 — 2 0Ohm — 0.12A — +VCCSTG
RES 0 OHM 1/10W (0603) JUMP

PEGATRON
Title: CPU(5)_+VDDQ/IO/SA
BG1/HW3
Engineer: Bill Yang
Size: Custom
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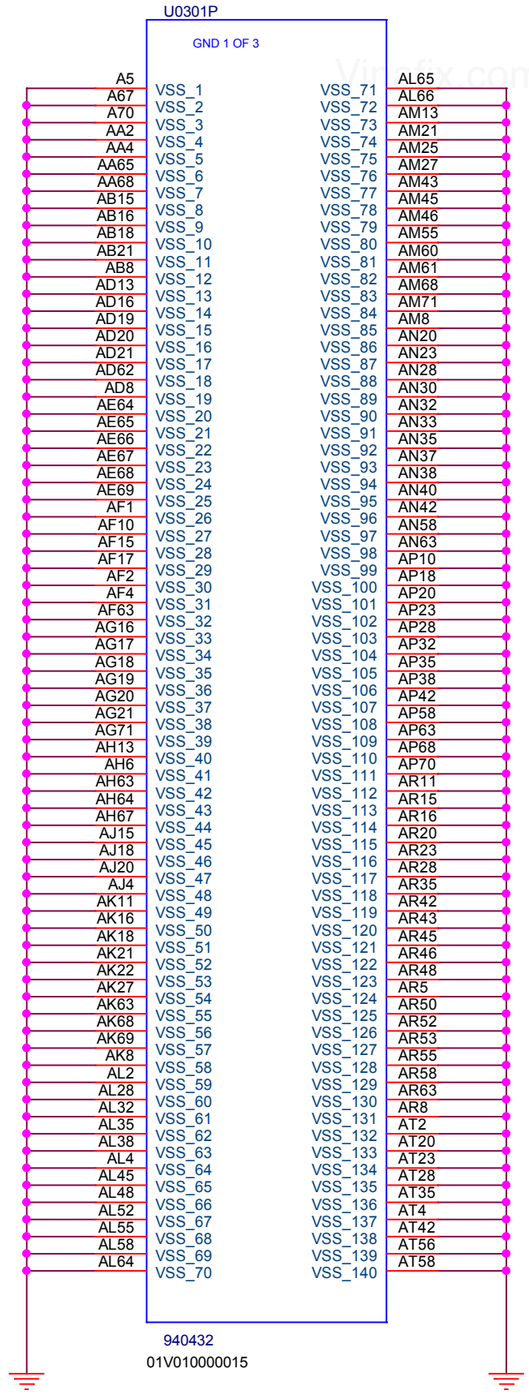

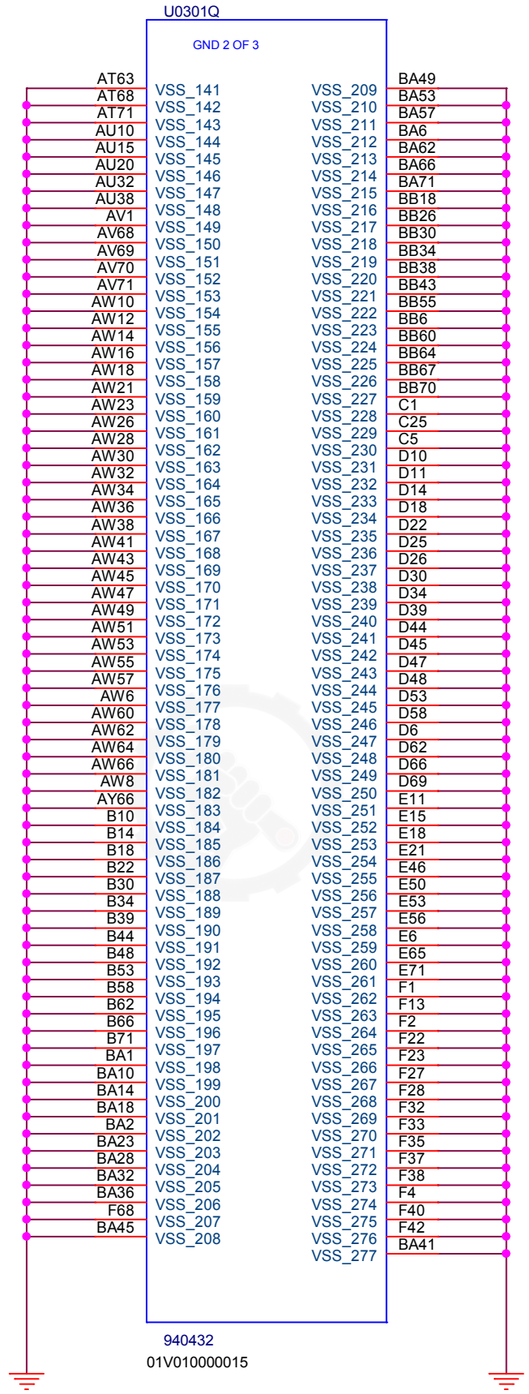

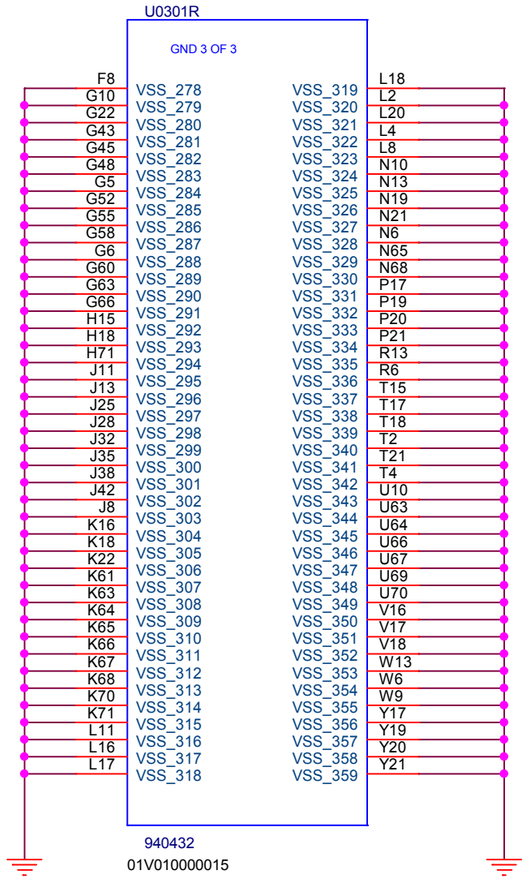

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Title : CPU(6)_CPU GND

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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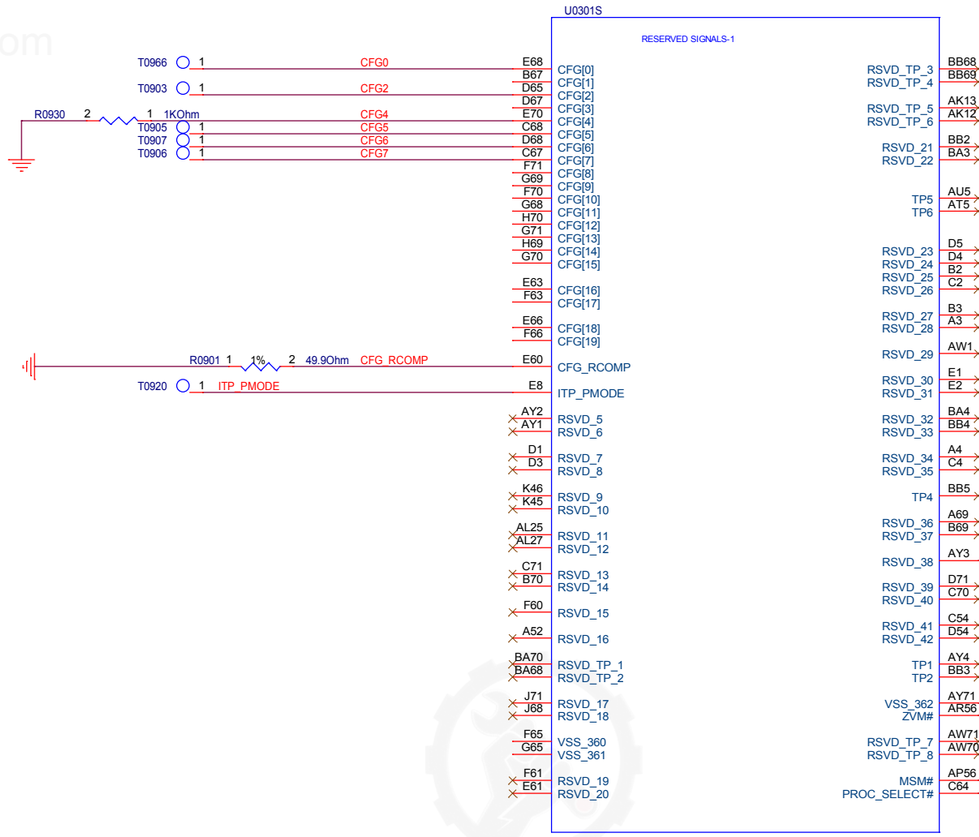
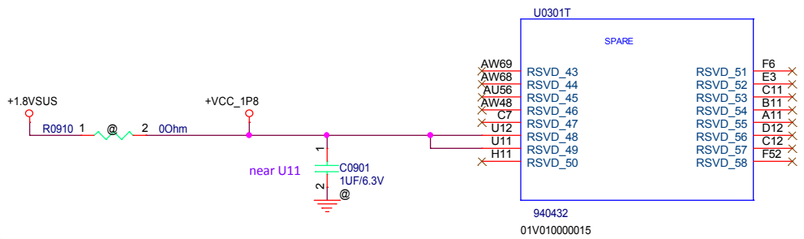
6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.





1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (IBP#543016).

Table 52-8 – Decoupling and Power Connection Requirement for Skylake-U PCH

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.8A	VccPGPPF	AF16	-	-	-	-	-
	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
	Vcc_1P8	U11, U12	1 uF	0402	1	E (<10 mm)	U11, U12 (Note 1 & 5)

PEGATRON Title :CPU(7)_CFG/RSVD

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
		1.1
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<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
C	KTU_CSM	1.1

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Size A	Document Number <Doc>
Rev	<RevCode>
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Size A	Document Number <Doc>
Rev	<RevCode>
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<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
C	KTU_CSM	1.1

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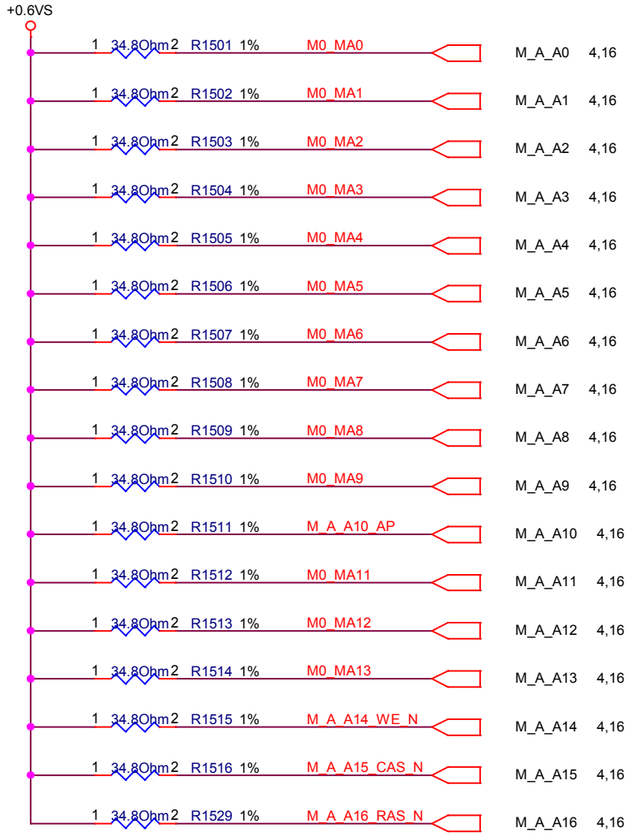
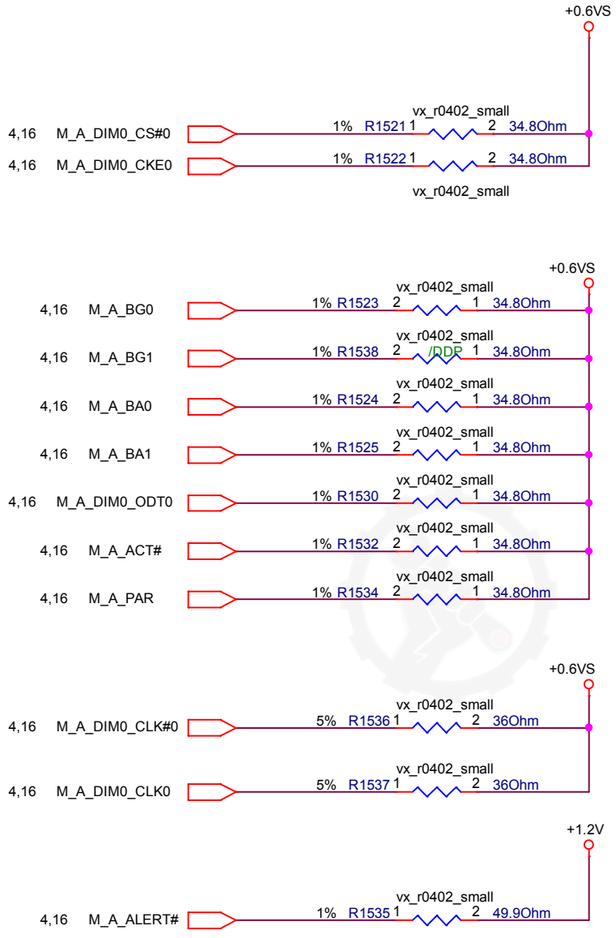
DDR4(0)_Termination

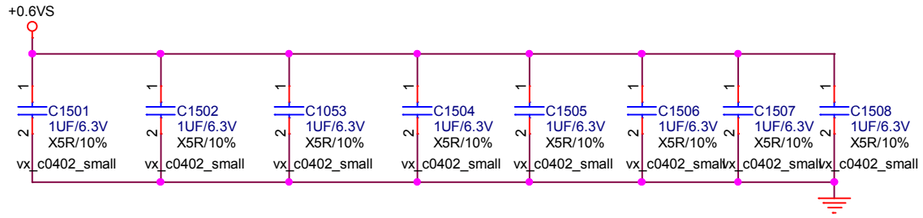
+0.6VS — +0.6VS 17,57,83

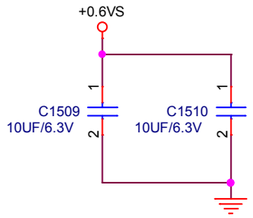
+1.2V — +1.2V 4,7,16,17,18,57,83





Average placed close to +VDDQ_VTT power plane





PEGATRON Title : DDR4(1)_Termination

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 15 of 96

M_A_A[16:0] 4,15
M_A_D[63:0] 4

+1.2V 4,7,15,17,18,57,83
+2P5VPP 17,57,82

Close to U1601

Byte 0: 0~7

Byte 1: 8~15

Byte 2: 16~23

Byte 3: 24~31

Close to U1602

Change to 0402 size for layout

Around the DRAM devices

Close to U1603

Byte 4: 32~39

Byte 5: 40~47

Byte 6: 48~55

Byte 7: 56~63

Close to U1604

Colay

MT40A1G16HBA-083E:A
03V150000100

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :DDR4(1)_MEMORY DOWN
BG1/HW3
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 16 of 104

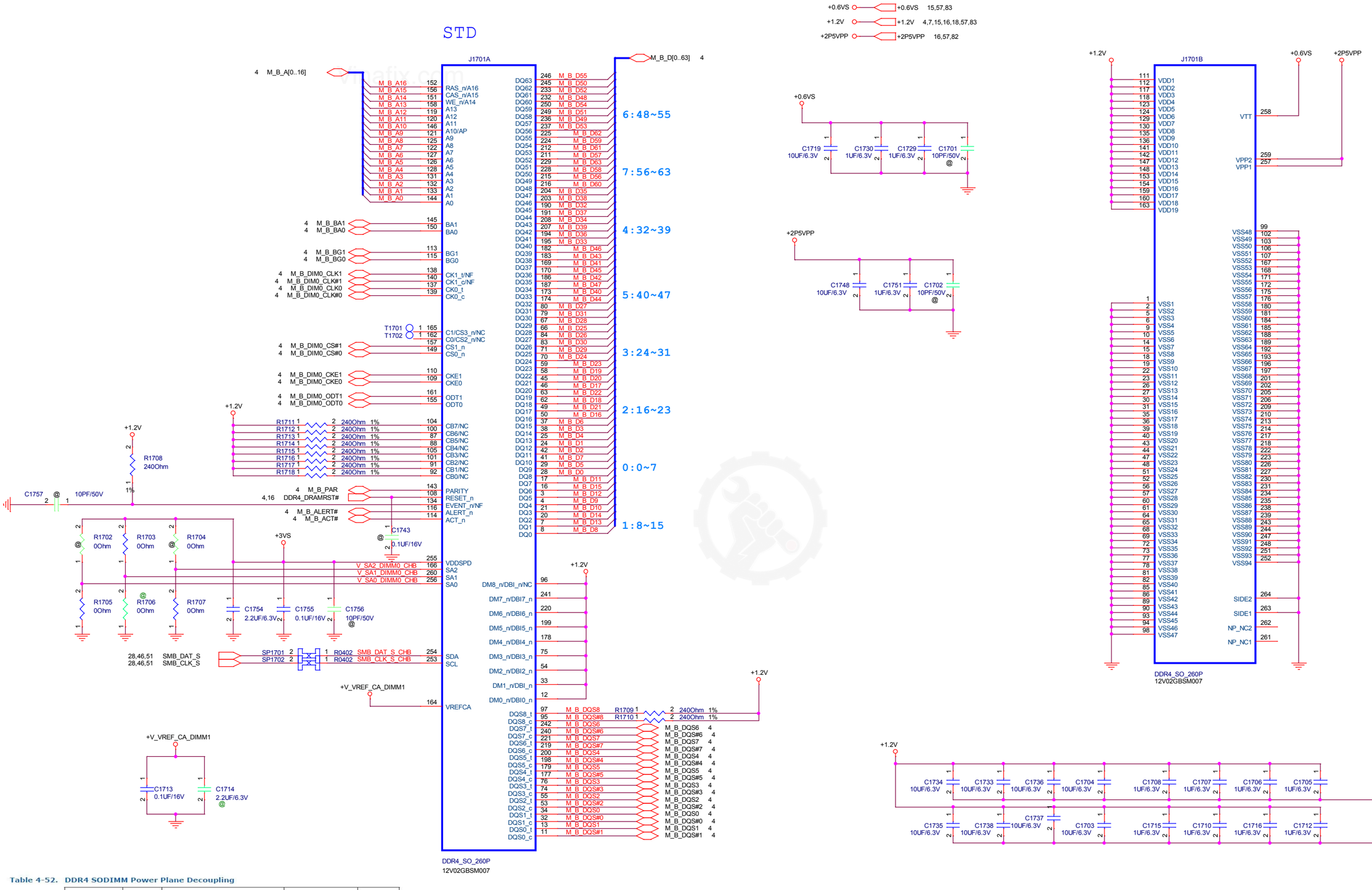


Table 4-52. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: DDR4(1)_SO-DIMM

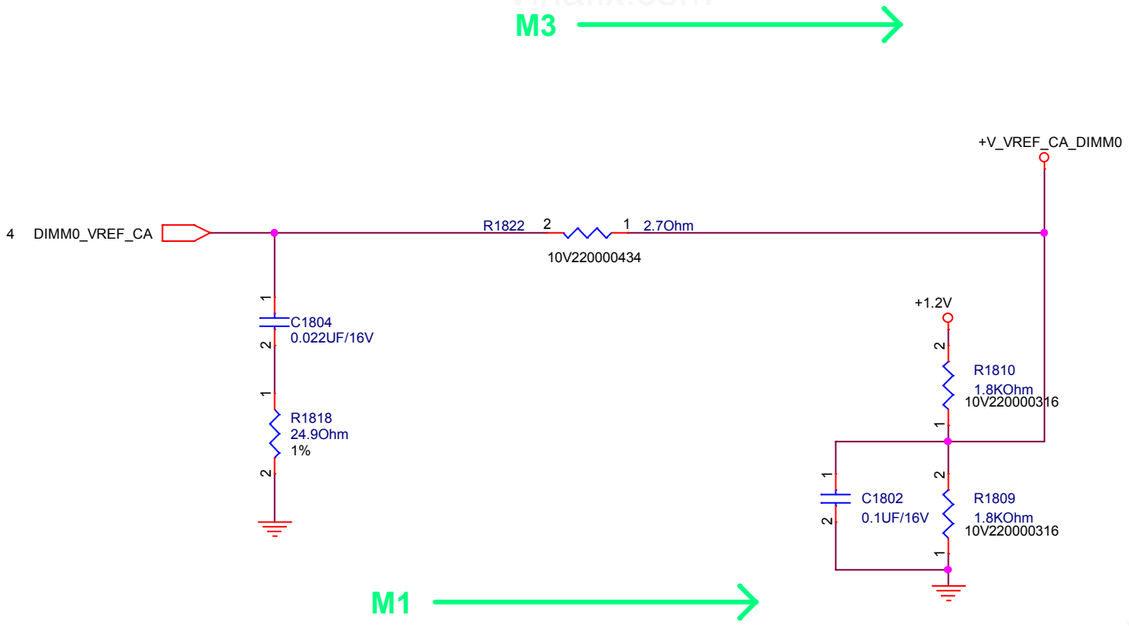
BG1/HW3

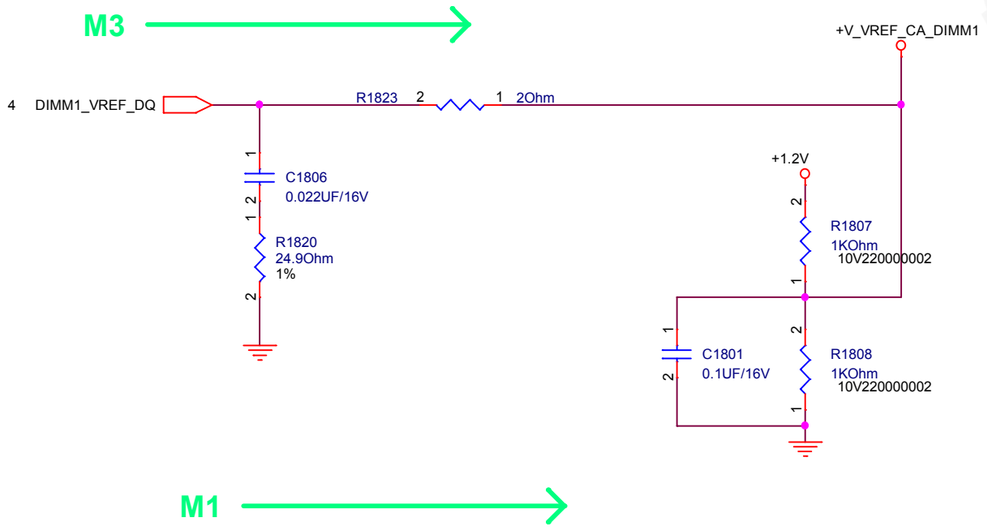
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 17 of 108

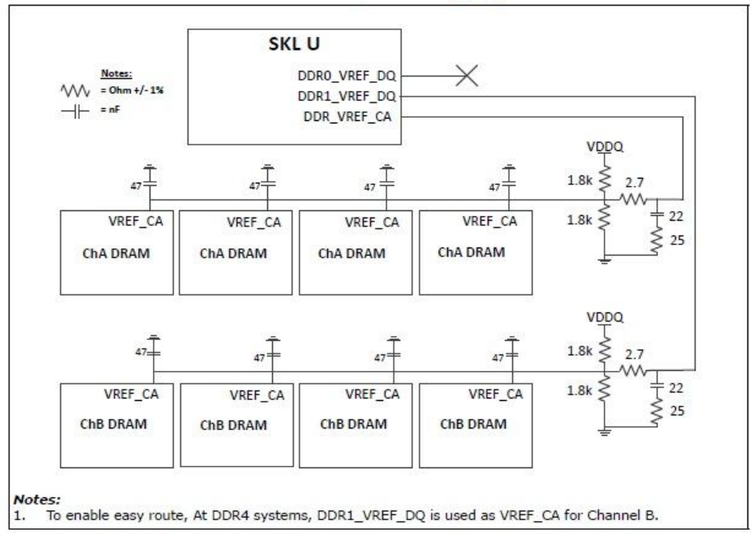
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off





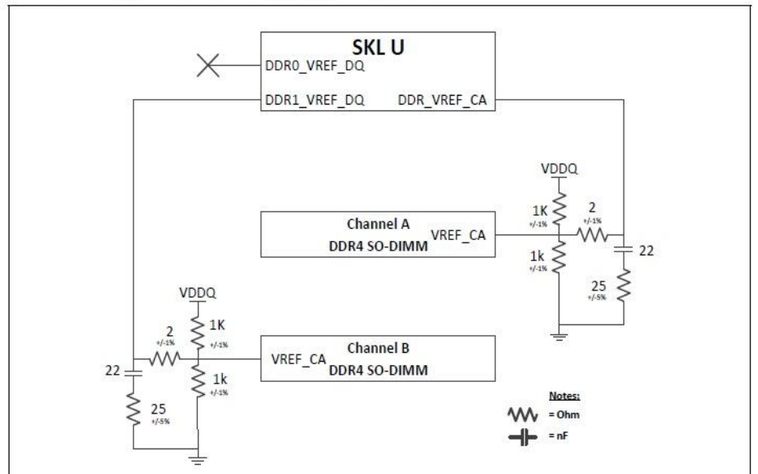
+1.2V — +1.2V 4,7,15,16,17,57,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 16
+V_VREF_CA_DIMM1 — +V_VREF_CA_DIMM1 17

Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :DDR4(3)_CA/DQ Voltage

Engineer: *Bill Yang*

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 18 of 108

<Variant Name>

PEGATRON Title :

Engineer:

Size	Project Name	Rev
C	KTU3_DSW	1.1

Date: Tuesday, September 06, 2016 Sheet 19 of 108

+3VS — +3VS 3,4,17,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+3VSUS_ORG — +3VSUS_ORG 21,22,23,25,26

U0301E

SPI - FLASH

28,30 SPI_CLK — AV2 SPI0_CLK
28,30 SPI_SO — AW3 SPI0_MISO
28,30 SPI_SI — AV3 SPI0_MOSI
28 SPI_WP#_IO2 — AW2 SPI0_IO2
28 SPI_HOLD#_IO3 — AU4 SPI0_IO3
28,30 SPI_CS#0 — AU3 SPI0_CS0#
T2001 1 — SPI_CS2# — AU2 SPI0_CS1#
AU1 SPI0_CS2#

SPI - TOUCH

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK

53 CL_CLK — G3 CL_CLK
53 CL_DAT — G2 CL_DATA
53 CL_RST# — G1 CL_RST#

30 RCIN# — AW13 GPP_A0/RCIN#
30,44,62 INT_SERIRQ — AY11 GPP_A6/SERIRQ

940432
01V010000015

SMBUS, SMLINK

GPP_C0/SMBCLK — R7
GPP_C1/SMBDATA — R8
GPP_C2/SMBALERT# — R10 SMB_ALERT#

SMB_CLK 28 — GPP_C0/SMBCLK
SMB_DAT 28 — GPP_C1/SMBDATA

GPP_C3/SML0CLK — R9 SML0_CLK
GPP_C4/SML0DATA — W2 SML0_DAT
GPP_C5/SML0ALERT# — W1 SML0_ALERT#

SML0_CLK 33,62 — GPP_C3/SML0CLK
SML0_DAT 33,62 — GPP_C4/SML0DATA

GPP_C6/SML1CLK — W3 SML1_CLK — 1 T2017
GPP_C7/SML1DATA — V3 SML1_DAT — 1 T2018
GPP_B23/SML1ALERT#/PCHHOT# — AM7 SML1_ALERT#

LPC

GPP_A1/LAD0/ESPI_IO0 — AY13
GPP_A2/LAD1/ESPI_IO1 — BA13
GPP_A3/LAD2/ESPI_IO2 — BB13
GPP_A4/LAD3/ESPI_IO3 — AY12
GPP_A5/LFRAME#/ESPI_CS# — BA12
GPP_A14/SUS_STAT#/ESPI_RESET# — BA11

LPC_AD0 30,44,62 — GPP_A1/LAD0/ESPI_IO0
LPC_AD1 30,44,62 — GPP_A2/LAD1/ESPI_IO1
LPC_AD2 30,44,62 — GPP_A3/LAD2/ESPI_IO2
LPC_AD3 30,44,62 — GPP_A4/LAD3/ESPI_IO3
LPC_FRAME# 30,44,62 — GPP_A5/LFRAME#/ESPI_CS#
PM_SUS_STAT# 62 — GPP_A14/SUS_STAT#/ESPI_RESET#

GPP_A9/CLKOUT_LPC0/ESPI_CLK — AW9 CLK_KBCPCI_PCH_R
GPP_A10/CLKOUT_LPC1 — AY9 CLK_DEBUG_R
GPP_A8/CLKRUN# — AW11 PM_CLKRUN# 30,62

CLK_KBCPCI_PCH_R — R2001 1 — 2 22Ohm — /Debug — CLK_KBCPCI_PCH 30
CLK_DEBUG_R — R2002 1 — 2 22Ohm — /Debug — CLK_DEBUG 44
R2022 1 — 2 22Ohm — /TPM — LPCCLK_TPM 62

C2001 10PF/50V @ — GND
C2002 10PF/50V @ — GND

DIMM/TouchPad

Intel LAN/NFC

+3VSUS_ORG

R2021 1 @ 2 20KOhm SML0_ALERT# R2020 1 @ 2 4.7KOhm — GND

SML0ALERT# - Internal weak pull down
0 : LPC EC (default)
1 : eSPI EC

+3VSUS_ORG

R2004 1 @ 2 20KOhm SMB_ALERT# R2003 1 /vpro 2 2.2KOhm — GND

SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

PDG Page.836 (#543016)

SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

+3VS

INT_SERIRQ — R2009 1 — 2 10KOhm
PM_CLKRUN# — R2013 1 — 2 10KOhm

10VH40000005

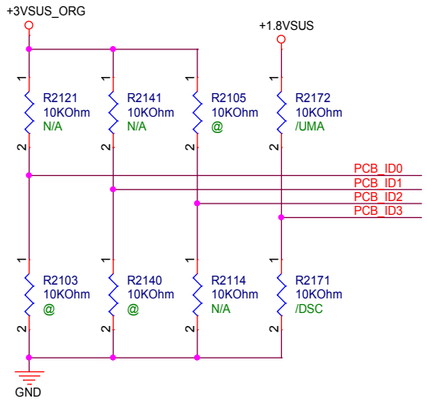
SMB_CLK — 10KOhm 3 — 4 RN2001B
SMB_DAT — 10KOhm 1 — 2 RN2001A

SML1_DAT — 2.2KOhm 3 — 4 RN2002B
SML1_CLK — 2.2KOhm 1 — 2 RN2002A
SML1_ALERT# — R2012 1 — 2 150KOhm

vx_r0402_small

<Variant Name>

PEGATRON Title : PCH(1)_SMB,LPC
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
BG1/HW3
Size Custom | Project Name P4 | Rev 1.0
Date: Tuesday, September 06, 2016 | Sheet 20 of 108

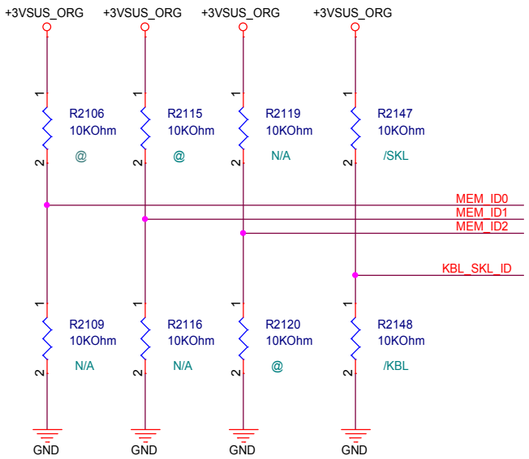


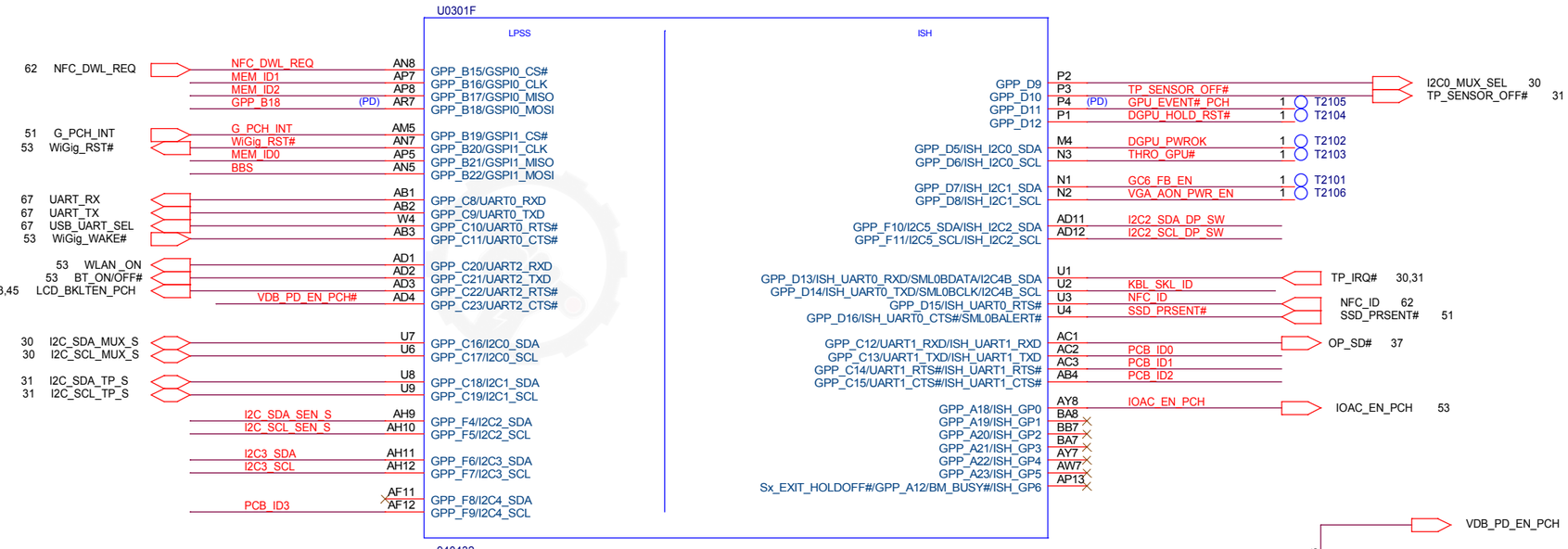
ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R2.0
0	1	1	R2.1
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

MEM_ID0	MEM_ID1	MEM_ID2	Memory Setting
0	0	0	SAMSUNG/K4A4G165WD-BCPB 4Gb 256Mb*16 0315-01C70PB
1	0	0	HYNIX/H5AN4G6NAFR-UHC 4G 256Mb*16 b0315-01EK0PB
0	1	0	SAMSUNG/K4A8G165WB-BCPB 8Gb 512Mb*16 0315-01HF0PB
1	1	0	HYNIX 8G
0	0	1	SAMSUNG/K4A8G165WB-BCRC 2400 512Mb*16 0315-01C80PB
1	0	1	SK HYNIX/H5AN8G6NAFR-UHC 2400 512Mb*16 0315-01W60PB
0	1	1	MICRON/MT40A512M16JY-083E:B 2400 512Mb*16 0315-01W90PB
1	1	1	MICRON/MT40A1G16WBU-083E:B 2400 1Gb*16 0315-01YC0PB

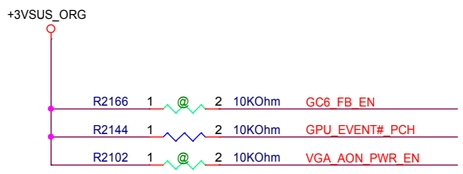
+3VS 3,4,17,20,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+3VSUS_ORG +3VSUS_ORG 20,22,23,25,26
+1.8VSUS +1.8VSUS 9,24,26,84

KBL_ID	SSD_PRSENT#	NFC_ID	PCB_ID3
1: SKL 0: KBL	1: No SSD 0: SSD	1: No NFC 0: NFC	1: UMA 0: DSC

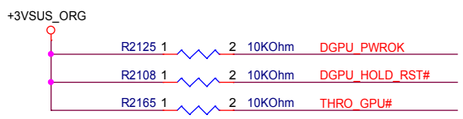


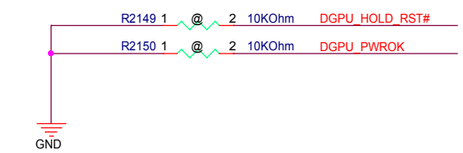


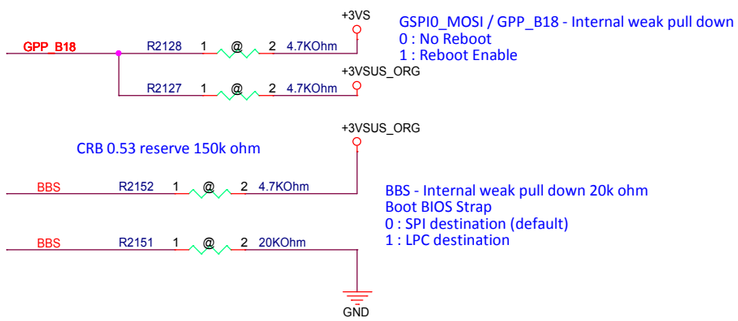
G Sensor

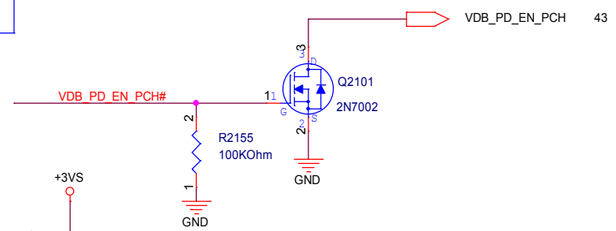


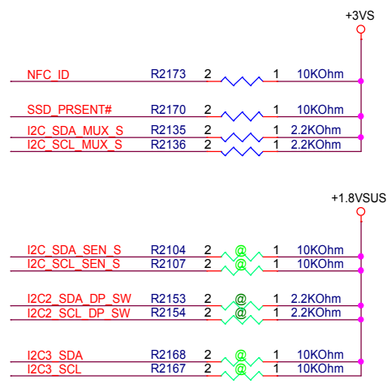
GPIO need to pull high to power with 10Kohm if unused











<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(2) LPSS,ISH

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 21 of 108

+3VS — +3VS 3,4,17,20,21,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+3VSUS_ORG — +3VSUS_ORG 20,21,23,25,26

HDA_BCLK_R
HDA_SDO_R
C2201 22PF/25V
C2202 22PF/25V
GND

RF request

U0301G

AUDIO

36	HDA_SYNC	R2219 33Ohm	HDA_SYNC_R	BA22	HDA_SYNC/I2S0_SFRM
36	HDA_BCLK	R2216 33Ohm	HDA_BCLK_R	AY22	HDA_BLK/I2S0_SCLK
36	HDA_SDO	R2215 33Ohm	HDA_SDO_R	BB22	HDA_SDO/I2S0_TXD
36	HDA_SDI0	R2220 33Ohm	HDA_SDI0_R	BA21	HDA_SDI0/I2S0_RXD
		T2230 1	SNN_HDA_SDI1	AY21	HDA_SDI1/I2S1_RXD
36,37	HDA_RST#	R2217 33Ohm	HDA_RST#_R	AW22	HDA_RST#/I2S1_SCLK
		T2202 1	PCH_GPP_D23	J5	GPP_D23/I2S_MCLK
				AY20	I2S1_SFRM
				AW20	I2S1_TXD
				AK7	GPP_F1/I2S2_SFRM
				AK6	GPP_F0/I2S2_SCLK
				AK9	GPP_F2/I2S2_TXD
				AK10	GPP_F3/I2S2_RXD
				H5	GPP_D19/DMIC_CLK0
				D7	GPP_D20/DMIC_DATA0
				D8	GPP_D17/DMIC_CLK1
				C8	GPP_D18/DMIC_DATA1
36	HDA_SPKR	HDA_SPKR		AW5	GPP_B14/SPKR

SDIO/SDXC

GPP_G0/SD_CMD	AB11
GPP_G1/SD_DATA0	AB13
GPP_G2/SD_DATA1	AB12
GPP_G3/SD_DATA2	W12
GPP_G4/SD_DATA3	W11
GPP_G5/SD_CD#	W10
GPP_G6/SD_CLK	W8
GPP_G7/SD_WP	W7
GPP_A17/SD_PWR_EN#/ISH_GP7	BA9
GPP_A16/SD_1P8_SEL	BB9
SD_RCOMP	AB7 — 2 200Ohm 1 R2201 1% 10V220000034 — GND
GPP_F23	AF13 — RTC_IN# 24

940432
01V010000015

R2202 1 @ 2 20KOhm — HDA_SPKR — R2209 1 @ 2 4.7KOhm — +3VS
GND
R2210 1 @ 2 4.7KOhm — +3VSUS_ORG

SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG

HDA_SDO_R 1KOhm 1 @ 2 R2203 — +VCCPAZIO
RB751V-40 2 — 1 D2210 — PCH_FLASH_DESCRIPTOR 30

HDA_SDO - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable
1 : Disable

<Variant Name>

PEGATRON Title : PCH(3),HDA,SDIO
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 22 of 108

+3VS — +3VS 3,4,17,20,21,22,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+3VSUS_ORG — +3VSUS_ORG 20,21,22,25,26

U0301H

PCIE/USB3/SATA

H13	PCIE1_RXN/USB3_5_RXN	
G13	PCIE1_RXP/USB3_5_RXP	
B17	PCIE1_TXN/USB3_5_TXN	
A17	PCIE1_TXP/USB3_5_TXP	
G11	PCIE2_RXN/USB3_6_RXN	
F11	PCIE2_RXP/USB3_6_RXP	
D16	PCIE2_TXN/USB3_6_TXN	
C16	PCIE2_TXP/USB3_6_TXP	
H16	PCIE3_RXN	
G16	PCIE3_RXP	
D17	PCIE3_TXN	
C17	PCIE3_TXP	
G15	PCIE4_RXN	
F15	PCIE4_RXP	
B19	PCIE4_TXN	
A19	PCIE4_TXP	
F16	PCIE5_RXN	LAN: 33 PCIE_RXN_LAN
E16	PCIE5_RXP	33 PCIE_RXP_LAN
C19	PCIE5_TXN	33 PCIE_TXN_LAN — 0.1UF/16V 1 2 C2320 PCIE_TXN_LAN_C
D19	PCIE5_TXP	33 PCIE_TXP_LAN — 0.1UF/16V 1 2 C2321 PCIE_TXP_LAN_C
G18	PCIE6_RXN	WLAN: 53 PCIE_RXN_WLAN
F18	PCIE6_RXP	53 PCIE_RXP_WLAN
D20	PCIE6_TXN	53 PCIE_TXN_WLAN — 0.1UF/16V 1 2 C2322 PCIE_TXN_WLAN_C
C20	PCIE6_TXP	53 PCIE_TXP_WLAN — 0.1UF/16V 1 2 C2323 PCIE_TXP_WLAN_C
F20	PCIE7_RXN/SATA0_RXN	HDD: 51 SATA_RXN0 — SATA_RXN0
E20	PCIE7_RXP/SATA0_RXP	51 SATA_RXP0 — SATA_RXP0
B21	PCIE7_TXN/SATA0_TXN	51 SATA_TXN0 — SATA_TXN0
A21	PCIE7_TXP/SATA0_TXP	51 SATA_TXP0 — SATA_TXP0
G21	PCIE8_RXN/SATA1A_RXN	
F21	PCIE8_RXP/SATA1A_RXP	
D21	PCIE8_TXN/SATA1A_TXN	
C21	PCIE8_TXP/SATA1A_TXP	
E22	PCIE9_RXN	
E23	PCIE9_RXP	
B23	PCIE9_TXN	
A23	PCIE9_TXP	
F25	PCIE10_RXN	WIGIG: 53 PCIE_RXN_WIGIG
E25	PCIE10_RXP	53 PCIE_RXP_WIGIG
C23	PCIE10_TXN	53 PCIE_TXN_WIGIG — 0.1UF/16V 1 2 C2301 PCIE_TXN_WIGIG_C
D23	PCIE10_TXP	53 PCIE_TXP_WIGIG — 0.1UF/16V 1 2 C2302 PCIE_TXP_WIGIG_C
F5	PCIE_RCOMPN	R2301 1 2 100Ohm 1% PCIE_RCOMPN
E5	PCIE_RCOMPP	PCIE_RCOMPP
D56	PROC_PRDY#	
D61	PROC_PREQ#	
BB11	GPP_A7/PIRQA#	PIRQA#
E28	PCIE11_RXN/SATA1B_RXN	SSD: 51 PCIE_SATA_RXN11_SSD
E27	PCIE11_RXP/SATA1B_RXP	51 PCIE_SATA_RXP11_SSD
D24	PCIE11_TXN/SATA1B_TXN	51 PCIE_SATA_TXN11_SSD
C24	PCIE11_TXP/SATA1B_TXP	51 PCIE_SATA_TXP11_SSD
E30	PCIE12_RXN/SATA2_RXN	51 PCIE_RXN12_SSD
F30	PCIE12_RXP/SATA2_RXP	51 PCIE_RXP12_SSD
A25	PCIE12_TXN/SATA2_TXN	51 PCIE_TXN12_SSD
B25	PCIE12_TXP/SATA2_TXP	51 PCIE_TXP12_SSD

SSIC / USB3

H8	USB3_1_RXN	USB3_RXN1 52
G8	USB3_1_RXP	USB3_RXP1 52
C13	USB3_1_TXN	USB3_TXN1 52
D13	USB3_1_TXP	USB3_TXP1 52
J6	USB3_2_RXN/SSIC_RXN	
H6	USB3_2_RXP/SSIC_RXP	
B13	USB3_2_TXN/SSIC_TXN	
A13	USB3_2_TXP/SSIC_TXP	
J10	USB3_3_RXN	USB3_RXN3 42
H10	USB3_3_RXP	USB3_RXP3 42
B15	USB3_3_TXN	USB3_TXN3 42
A15	USB3_3_TXP	USB3_TXP3 42
E10	USB3_4_RXN	
F10	USB3_4_RXP	
C15	USB3_4_TXN	
D15	USB3_4_TXP	

on MLB USB3.0

on MLB Type-C

USB2

AB9	USB2N_1	USB_PN1 52
AB10	USB2P_1	USB_PP1 52
AD6	USB2N_2	USB_PN2 67
AD7	USB2P_2	USB_PP2 67
AH3	USB2N_3	USB_PN3 42
AJ3	USB2P_3	USB_PP3 42
AD9	USB2N_4	USB_PN4 42
AD10	USB2P_4	USB_PP4 42
AJ1	USB2N_5	USB_PN5 53
AJ2	USB2P_5	USB_PP5 53
AF6	USB2N_6	USB_PN6 31
AF7	USB2P_6	USB_PP6 31
AH1	USB2N_7	USB_PN7 45
AH2	USB2P_7	USB_PP7 45
AF8	USB2N_8	USB_PN8 67
AF9	USB2P_8	USB_PP8 67
AG1	USB2N_9	
AG2	USB2P_9	
AH7	USB2N_10	USB_PN10 45
AH8	USB2P_10	USB_PP10 45

on MLB USB2.0

ON Swap Bay HUB/ IO U2

on MLB Type-C

on MLB Type-C

M.2 BT

Finger Printer

Normal Camera

SD

Touch Panel

AB6	USB2_COMP	R2302 1 2 113Ohm 1% GND
AG3	USB2_ID	USB2_ID_OTG R2310 1 2 1KOhm GND
AG4	USB2_VBUSSENSE	USB2_VBUSSENSE_OTG R2330 1 2 1KOhm

A9	GPP_E9/USB2_OC0#	USB_OC0# PCH → USB_OC0#_PCH 52
C9	GPP_E10/USB2_OC1#	USB_OC1# PCH → USB_OC1#_PCH 67
D9	GPP_E11/USB2_OC2#	USB_OC2# PCH → USB_OC2#_PCH 42
B9	GPP_E12/USB2_OC3#	NFC_IRQ → NFC_IRQ 62

USB3.0 with USB charge

USB2.0

Type-C

J1	GPP_E4/DEVSLP0	NFC_RESET 62
J2	GPP_E5/DEVSLP1	DEVSLP1 51
J3	GPP_E6/DEVSLP2	
H2	GPP_E0/SATAXPCIE0/SATAGP0	SATAGP0
H3	GPP_E1/SATAXPCIE1/SATAGP1	SATA_SSD_PEDET 51
G4	GPP_E2/SATAXPCIE2/SATAGP2	SATA_ODD_PRSNT#
H1	GPP_E8/SATALED#	

+3VSUS_ORG

USB_OC0# PCH 1 10KOhm 2 RN2310A

USB_OC1# PCH 3 10KOhm 4 RN2310B

USB_OC2# PCH R2329 1 2 10KOhm

+3VS

DEVSLP1 R2324 1 @ 2 10KOhm

+3VS

SATAGP0 R2320 1 @ 2 10KOhm

SATA_ODD_PRSNT# R2305 1 @ 2 10KOhm

PIRQA# R2318 1 2 10KOhm

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3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

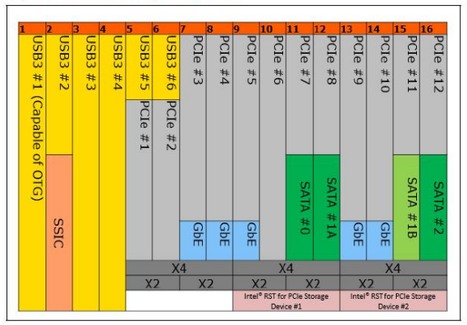

Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

<Variant Name>

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Title : PCH(4) _PCIE,SATA,US

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 23 of 108

+VCCF24NS_1P0 → +VCCF24NS_1P0 26
+VCC_RTC → +VCC_RTC 25,26,36,60
+AC_BAT_SYS → +AC_BAT_SYS 43,45,80,81,82,83,88
+3VS → +3VS 3,4,17,20,21,22,23,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+3VA → +3VA 30,31,36,41,43,53,56,57,67,81,88,93

U0301I

CSI-2

A36	CSI2_DN0	CSI2_CLKN0	C37
B36	CSI2_DP0	CSI2_CLKP0	D37
C38	CSI2_DN1	CSI2_CLKN1	C32
D38	CSI2_DP1	CSI2_CLKP1	D32
C36	CSI2_DN2	CSI2_CLKN2	C29
D36	CSI2_DP2	CSI2_CLKP2	D29
A38	CSI2_DN3	CSI2_CLKP3	B26
B38	CSI2_DP3		A26
C31	CSI2_DN4	CSI2_COMP	E13
D31	CSI2_DP4	GPP_D4/FLASHTRIG	B7
C33	CSI2_DN5		
D33	CSI2_DP5		
A31	CSI2_DN6		
B31	CSI2_DP6		
A33	CSI2_DN7		
B33	CSI2_DP7		
A29	CSI2_DN8		
B29	CSI2_DP8		
C28	CSI2_DN9		
D28	CSI2_DP9		
A27	CSI2_DN10		
B27	CSI2_DP10		
C27	CSI2_DN11		
D27	CSI2_DP11		

EMMC

GPP_F13/EMMC_DATA0	AP2	
GPP_F14/EMMC_DATA1	AP1	
GPP_F15/EMMC_DATA2	AP3	
GPP_F16/EMMC_DATA3	AN3	
GPP_F17/EMMC_DATA4	AN1	
GPP_F18/EMMC_DATA5	AN2	
GPP_F19/EMMC_DATA6	AM4	
GPP_F20/EMMC_DATA7	AM1	
GPP_F21/EMMC_RCLK	AM2	
GPP_F22/EMMC_CLK	AM3	
GPP_F12/EMMC_CMD	AP4	
EMMC_RCOMP	AT1	

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CSI2_COMP R2418 1 2 100Ohm 1% → GND
GPP_D4 → 1 T2417
EMMC_RCOMP R2419 1 2 200Ohm 1% → GND

24MHz signal 需包GND

U0301J

CLOCK SIGNALS

CLKOUT_PCIE_N0	D42	
CLKOUT_PCIE_P0	C42	
GPP_B5/SRCCLKREQ0#	AR10	
CLKOUT_PCIE_N1	B42	CLK_PCIE_WIGIG#
CLKOUT_PCIE_P1	A42	CLK_PCIE_WIGIG
GPP_B6/SRCCLKREQ1#	AT7	CLK_REQ_WIGIG#
CLKOUT_PCIE_N2	D41	CLK_PCIE_WLAN#
CLKOUT_PCIE_P2	C41	CLK_PCIE_WLAN
GPP_B7/SRCCLKREQ2#	AT8	CLK_WLAN_REQ#
CLKOUT_PCIE_N3	D40	CLK_PCIE_LAN#
CLKOUT_PCIE_P3	C40	CLK_PCIE_LAN
GPP_B8/SRCCLKREQ3#	AT10	CLK_REQ_LAN#
CLKOUT_PCIE_N4	B40	CLK_PCIE_SSD#
CLKOUT_PCIE_P4	A40	CLK_PCIE_SSD
GPP_B9/SRCCLKREQ4#	AU8	CLK_REQ_SSD#
CLKOUT_PCIE_N5	E40	
CLKOUT_PCIE_P5	E38	
GPP_B10/SRCCLKREQ5#	AU7	CLK_REQ5#

SP2420 2 1 CLKOUT_PCIE_N1 B42
SP2421 2 1 CLKOUT_PCIE_P1 A42
SP2419 2 1 CLK_REQ1# AT7
SP2416 2 1 CLKOUT_PCIE_N2 D41
SP2418 2 1 CLKOUT_PCIE_P2 C41
SP2417 2 1 CLK_REQ2# AT8
SP2401 2 1 CLKOUT_PCIE_N3 D40
2 1 CLKOUT_PCIE_P3 C40
SP2403 2 1 CLK_REQ3# AT10
SP2404 2 1 CLKOUT_PCIE_N4 B40
SP2405 2 1 CLKOUT_PCIE_P4 A40
SP2406 2 1 CLK_REQ4# AU8

CLKOUT_ITPXDP_N	F43	
CLKOUT_ITPXDP_P	E43	
GPD8/SUSCLK	BA17	SUS_CLK
XTAL24_IN	E37	XTAL_24M_IN
XTAL24_OUT	E35	XTAL_24M_OUT
XCLK_BIASREF	E42	XCLK_BIASREF
RTCX1	AM18	XTAL_32K_X1
RTCX2	AM20	XTAL_32K_X2
SRTCRST#	AN18	SRTC_RST#
RTCRST#	AM16	RTC_RST#

SUS_CLK → 1 T2401
+VCCF24NS_1P0
XCLK_BIASREF R2417 1 2 2.71Kohm 0.5%
PDG 0.9 - 2.7k +-1%

C2401 1 2 10PF/50V 5% → GND
R2401 1MOhm
X2401 24MHZ
C2402 1 2 10PF/50V 5% → GND
C2403 1 2 15PF/50V → GND
R2402 10MOhm
X2402 32.768KHZ 07V080000064
C2404 1 2 15PF/50V → GND

+VCC_RTC
R2403 1 2 20KOhm
JRST2001 0Ohm @ → GND
C2405 1UF/6.3V → GND
R2404 1 2 20KOhm
JRST2002 0Ohm @ → GND
C2406 1UF/6.3V → GND

CLK_REQ1# /NON_IOAC R2405 1 2 10KOhm → +3VS
CLK_REQ3# R2406 1 2 10KOhm → +3VS

A 10 K ±5% external pull-up resistor required to core rail, but the corresponding CLKREQ# function can be disabled by means of the IntelR ME FW.

CLK_REQ2# /NON_IOAC R2430 1 2 10KOhm → +3VS
CLK_REQ4# R2435 1 2 10KOhm → +3VS
CLK_REQ5# R2431 1 2 10KOhm @ → +3VS

CLK_REQ1# R2408 1 2 10KOhm @
CLK_REQ2# R2434 1 2 10KOhm @
CLK_REQ3# R2409 1 2 10KOhm @
CLK_REQ4# R2432 1 2 10KOhm @
CLK_REQ5# R2440 1 2 10KOhm @
SUS_CLK R2437 1 2 1KOhm 5% @ → GND

If CLKREQ# control is not needed, say for a free running clock, do not pulldown signal to GND. This will increase leakage in Sx states.

CLK_REQ1# /IOAC R2442 1 2 10KOhm → +3VSUS
CLK_REQ2# /IOAC R2441 1 2 10KOhm → +3VSUS

+3VA
R2425 0Ohm
R2423 1.5KOhm 1% @
+RTC_AC
R2424 45.3KOhm 1% @
+VCC_RTC
R2420 1KOhm @
D2401 0.8V/0.2mA
C2407 1UF/6.3V
+RTC_BAT
R9306 1 2 1KOhm
+RTCBAT
J2401 SIDE2 2 1 SIDE1
WtoB_CON_2P
12V17AISM015
GND

EC reset
CMOS feature

30 SW_RTCRST
R2407 10KOhm
Q2401 2N7002
GND

RTC Detect

+RTCBAT
+1.8VSUS
R2438 100KOhm @
RTC_IN# 22
Q2402 2N7002
R2439 10MOhm @
GND

<Variant Name>

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Title: CLK,RTC,HDA,SDIO
Engineer: Bill Yang
BG1/HW3
Size: Custom
Project Name: P4
Rev: 1.0
Date: Tuesday, September 06, 2016
Sheet 24 of 108

+3VSUS
+VCCDSW
+3VSUS_ORG
+3V
+VCC_RTC
+VCCST_CPU

+3VSUS +3VSUS 4,24,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+VCCDSW +VCCDSW 26,30
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,26
+3V +3V 31,44,57,67,82,91
+VCC_RTC +VCC_RTC 24,26,36,60
+VCCST_CPU +VCCST_CPU 3,5,7,9

+3VSUS_ORG
R2501 10KOhm
SYS_RESET#
R2502 1KOhm @
GND

U0301K
SYSTEM POWER MANAGEMENT
940432
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30 PM_RSMRST# — R2543 — PLT_RST# — SYS_RESET# — PM_RSMRST_R — GPP_B13/PLTRST# SYS_RESET# RSMRST#
T2501 — H_CPUPWRGD_TP — R2503 1KOhm — H_CPUPWRGD — H_VCCST_PWRGD_MCP — PROCPWRGD VCCST_PWRGD
30,68 SYS_PWROK — R2504 0Ohm — SYS_PWROK_R — SYS_PWROK PCH_PWROK DSW_PWROK
PM_PWROK — R2505 0Ohm — PM_PCH_PWROK_R
PM_RSMRST_R — R2506 0Ohm — PCH_DPWROK
ALL_SYS_PWRGD delay 99 ms from EC
30 SUSWARN#/SUSPWRDNACK — R2508 /SBA 0Ohm — SUS_PWR_ACK_R — GPP_A13/SUSWARN#/SUSPWRDNACK GPP_A15/SUSACK#
30 SUSACK# — R2509 0Ohm — SUSACK# R
53 PCIE_WAKE# — R2510 @ 0Ohm — WAKE#
33 LAN_WAKE# — LAN_WAKE# — GPD2/LAN_WAKE#
33 LAN_DISABLE# — T2508 — GPD11 — GPD11/LANPHYPC
EC_WAKE_DSW# — GPD7/RSVD

GPP_B12/SLP_S0# — AT11 SLP_S0# — T2514 — NB_R0402_20MIL_SMALL — PM_SUSB# 30,68
GPD4/SLP_S3# — AP15 SLP_S3# R — R2545 — PM_SUSC# 30,68
GPD5/SLP_S4# — BA16 SLP_S4# R — R2544
GPD10/SLP_S5# — AY16 SLP_S5# — T2504 — NB_R0402_20MIL_SMALL
SLP_SUS# — AN15 SLP_SUS# — T2503
SLP_LAN# — AW15
GPD9/SLP_WLAN# — BB17 SLP_WLAN# — T2515 — SLP_LAN# 33
GPD6/SLP_A# — AN16 ME_PM_SLP_A# R — R2536 /SBA 0Ohm — ME_PM_SLP_A# 30
GPD3/PWRBTN# — BA15
GPD1/ACPRESENT — AY15 AC_PRESENT_R — R2532 0Ohm — PM_PWRBTN# 30
GPD0/BATLOW# — AU13 BATLOW# — ME_AC_PRESENT 30
GPP_A11/PME# — AU11 PME# — T2513 internal pull high
INTRUDER# — AP16 INTRUDER# — R2513 1MOhm — +VCC_RTC
GPP_B11/EXT_PWR_GATE# — AM10 EXT_PWR_GATE# — SP2508 — MPHY_EXT_PWR_GATEB 26
GPP_B2/VRALERT# — AM11 VR_ALERT#

+3VSUS_ORG
R2514 10KOhm internal pull high

+3V
U2501 @ SN74LVC1G08DCKR
PLT_RST# — BUF_PLT_RST# 30,32,33,51,53,62
C2502 100PF/50V @ — R2515 0Ohm — C2503 100PF/50V @ — R2516 10KOhm
GND

Set to GPI — VR_ALERT# — R2528 @ 10KOhm — +3VSUS_ORG

+VCCDSW
BATLOW# — R2522 10KOhm
LAN_WAKE# — R2523 10KOhm
PCIE_WAKE# — R2525 1KOhm
AC_PRESENT_R — R2526 10KOhm
EC_WAKE_DSW# — R2524 @ 10KOhm

+3VSUS
ALL_SYSTEM_PWRGD — R2531 @ 0Ohm — ALL_SYSTEM_PWRGD_PMOK
DELAY_ALL_SYSTEM_PWRGD — SP2506
80,92 VRM_PWRGD — D2506 RB751V-40
PLT_RST# — D2507 RB751V-40
U2502 Vcc=2~5.5 — PM_PWROK — R2519 10KOhm
R2517 @ 0Ohm
GND

EC delay ALL_SYSTEM_PWRGD 2ms
30 DELAY_ALL_SYSTEM_PWRGD — R2529 0Ohm — H_VCCST_PWRGD_L
30,92 ALL_SYSTEM_PWRGD — R2530 @ 0Ohm
U2503 74AUP1G07GW 06V030000021
+3VSUS — 0.1UF/16V C2504
+VCCST_CPU — R2520 1KOhm
H_VCCST_PWRGD_R — R2521 1% 60.4Ohm — H_VCCST_PWRGD_MCP
0.1UF/16V C2505
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title PCH(6)_SYS PWR
Engineer: Bill Yang
BG1/HW3
Size Custom | Project Name P4 | Rev 1.0
Date: Tuesday, September 06, 2016 | Sheet 25 of 108

+1.0VSUS +1.0VSUS 82
+VCCPRIM_CORE +VCCPRIM_CORE 82
+VCCDSW +VCCDSW 25,30
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,25
+1.8VSUS +1.8VSUS 9,21,24,84

+VCCPAZIO +VCCPAZIO 22
+VCC_RTC +VCC_RTC 24,25,36,60
+VCCF24NS_1P0 +VCCF24NS_1P0 24
+3VSUS +3VSUS 4,24,25,28,30,31,33,41,42,51,53,62,67,68,81,92

+1.0VSUS R2601 0Ohm +VCCPRIM_1P0 C2601 1UF/6.3V @ near AB19
+VCCPRIM_CORE C2602 1UF/6.3V @ near AF18
+1.0VSUS R2603 0Ohm +VCCMPHYAON_1P0 C2603 1UF/6.3V near K17
+VCCMPHYGTAON_1P0_LS_SIP C2616 22UF/6.3V @ C2605 22UF/6.3V @ C2606 1UF/6.3V near N15 near N15 near N15
+1.0VSUS R2604 0Ohm +VCCAPLL_1P0 C2608 47UF/6.3V @ C2636 0.1UF/16V +V1.00A_SIP
+VCCAMPHYPLL_1P0 C2607 1UF/6.3V @ near K15
+1.0VSUS R2605 0Ohm +VCCPDSW_3P3
+VCCDSW R2606 @ 0Ohm +VCCPAZIO C2609 1UF/6.3V @ near AJ19 C2637 0.1UF/16V
+3VSUS_ORG R2611 0Ohm +VCCPRIM_3P3 C2611 1UF/6.3V @ near V19
+1.0VSUS R2612 0Ohm +VCCFHV
+VCCAPLLEBB_1P0 C2612 1UF/6.3V near N18
+VCCSRAM_1P0 +VCCPSPI C2610 1UF/6.3V @ near AF20
+VCCDSW +VCCPDSW_3P3

U0301O
CPU POWER 4 OF 4

0.696A	AB19	VCCPRIM_1P0_1	
	AB20	VCCPRIM_1P0_2	
	P18	VCCPRIM_1P0_3	
2.574A	AF18	VCCPRIM_CORE_1	
	AF19	VCCPRIM_CORE_2	
	V20	VCCPRIM_CORE_3	
	V21	VCCPRIM_CORE_4	
	AL1	DCPDSW_1p0	
0.022A	K17	VCCMPHYAON_1P0_1	
	L1	VCCMPHYAON_1P0_2	
0.727A	N15	VCCMPHYGT_1P0_1	
	N16	VCCMPHYGT_1P0_2	
	N17	VCCMPHYGT_1P0_3	
	P15	VCCMPHYGT_1P0_4	
	P16	VCCMPHYGT_1P0_5	
0.088A	K15	VCCAMPHYPLL_1P0_1	
	L15	VCCAMPHYPLL_1P0_2	
0.026A	V15	VCCAPLL_1P0	
0.696A	AB17	VCCPRIM_1P0_4	
	Y18	VCCPRIM_1P0_5	
0.118A	AD17	VCCDSW_3p3_1	
	AD18	VCCDSW_3p3_2	
	AJ17	VCCDSW_3p3_3	
0.068A	AJ19	VCCHDA	
0.011A	AJ16	VCCSPI	
0.642A	AF20	VCCSRAM_1P0_1	
	AF21	VCCSRAM_1P0_2	
	T19	VCCSRAM_1P0_3	
	T20	VCCSRAM_1P0_4	
0.075A	AJ21	VCCPRIM_3p3_1	
0.696A	AK20	VCCPRIM_1P0_6	
0.033A	N18	VCCAPLLEBB_1P0	

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Decoupling cap for internal power

0.02A	AK15	VCCPGPPA	
0.004A	AG15	VCCPGPPB	
0.006A	Y16	VCCPGPPC	
0.008A	Y15	VCCPGPPD	
0.006A	T16	VCCPGPPE	
0.161A	AF16	VCCPGPPF	
0.056A	AD15	VCCPGPPG	
0.075A	V19	VCCPRIM_3p3_2	
0.696A	T1	VCCPRIM_1P0_7	
0.006A	AA1	VCCATS_1p8	
0.001A	AK17	VCCRTCPRIM_3p3	
	AK19	VCCRTC_1	
	BB14	VCCRTC_2	
	BB10	DCPRTC	
0.035A	A14	VCCCLK1	
0.029A	K19	VCCCLK2	
0.024A	L21	VCCCLK3	
0.033A	N20	VCCCLK4	
0.004A	L19	VCCCLK5	
0.01A	A10	VCCCLK6	
	AN11	GPP_B0/CORE_VID0	
	AN13	GPP_B1/CORE_VID1	

GND 0.1UF/16V 2C2634 near AK19 +VCCPRTC_3P3 R2626 +VCC_RTC
VCCRTCEXT 0.1UF/16V 2C2620 near BB10 GND
C2619 0Ohm 1 2 1UF/6.3V GND near AK19

R2646 1KOhm R2647 1KOhm
Intel confirm pull down 1k

+VCCDTS_1P0 R2623 0Ohm +1.0VSUS
+V1.8A_SIP C2615 1UF/6.3V near AA1 R2624 0Ohm +1.8VSUS
+VCCPRIM_3P3
+VCCPRTCPRIM_3P3 C2617 0.1UF/16V near AK17 C2618 1UF/6.3V near AK17 R2625 0Ohm +3VSUS_ORG

+VCC19P2_1P0 R2627 0Ohm +1.0VSUS
+VCCF100_1P0 R2628 0Ohm +1.0VSUS
+VCCF135_1P0 R2629 0Ohm +1.0VSUS
+VCCF100OC_1P0 R2630 0Ohm +1.0VSUS
+VCCF24NS_1P0 R2631 0Ohm +1.0VSUS
+VCC24TBT_1P0 R2632 0Ohm +1.0VSUS
C2624 1UF/6.3V @ near A10

+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)

+3VSUS JP2601 +3VSUS_ORG
0.358A 2 2 1 1 0.358A
2MM_OPEN_5MIL

w/o DSW
+3VSUS_ORG R2633 vx_r0805_0ohm_h24_small 0Ohm +VCCDSW

+3VSUS_ORG R2607 1 2 0Ohm +VCCPAZIO

+3VSUS_ORG R2610 0Ohm +VCCPSPI

+VCCDSW
R2652 1 @ 2 0Ohm +VCCPDSW_3P3
Q2602
N/A
SI2301CDS-T1-GE3
07V040000124

N/A
Q2601
BC856BS
07V020000007

N/A R2648 100KOhm
N/A R2649 100KOhm

+1.0VSUS +VCCMPHYGTAON_1P0_LS
R2650 1 @ 2 0Ohm vx_r0805_0ohm_h24_small
+VCCMPHYGTAON_1P0_LS_P
R2651 1 2 0Ohm vx_r0805_0ohm_h24_small
+VCCMPHYGTAON_1P0_LS_SIP 0.727A
R2636 1 2 0Ohm vx_r0805_0ohm_h24_small +VCCSRAM_1P0
0.642A
R2637 1 2 0Ohm vx_r0805_0ohm_h24_small +VCCAMPHYPLL_1P0
0.088A
R2638 1 2 0Ohm +VCCAPLLEBB_1P0
0.033A
R2639 1 2 0Ohm

GPIO power Rail

+3VSUS_ORG R2613 0Ohm +VCCPGPPA
+3VSUS_ORG R2617 0Ohm +VCCPGPPD
+3VSUS_ORG R2615 0Ohm +VCCPGPPB C2635 1UF/6.3V @ near AG15
+3VSUS_ORG R2619 0Ohm +VCCPGPPE C2614 1UF/6.3V @ near T16
+3VSUS_ORG R2616 0Ohm +VCCPGPPC C2613 1UF/6.3V @ near Y16
+1.8VSUS R2620 0Ohm +VCCPGPPF
+3VSUS_ORG R2621 0Ohm +VCCPGPPG

MPHY_EXT_PWR_GATEB should pull high at A0 chip
25 MPHY_EXT_PWR_GATEB R2644 1 2 0Ohm C2629 0.033UF/16V @

+5VO +1.0VSUS
Rdson = 15m OHM
U2601
TPS22966DPUR 06V290000053
C2632 1UF/6.3V C2630 1UF/6.3V C2633 1UF/10V
C2627 220PF/25V C2628 220PF/25V
C2631 0.1UF/16V C2626 0.1UF/16V
T2601 TPC26T
Iout =2.12A / ICC_Max 2.12A _CRB 0.53/TPCH17 TR<200us
+VCCMPHYGTAON_1P0_LS_P

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :PCH(7)_POWER
BG1/HW3
Engineer: Bill Yang
Size Custom | Project Name P4 | Rev 1.0
Date: Tuesday, September 06, 2016 | Sheet 26 of 108

<Variant Name>

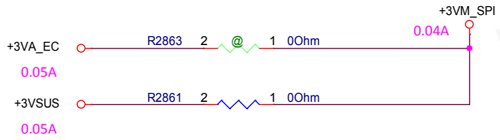
PEGATRON Title :

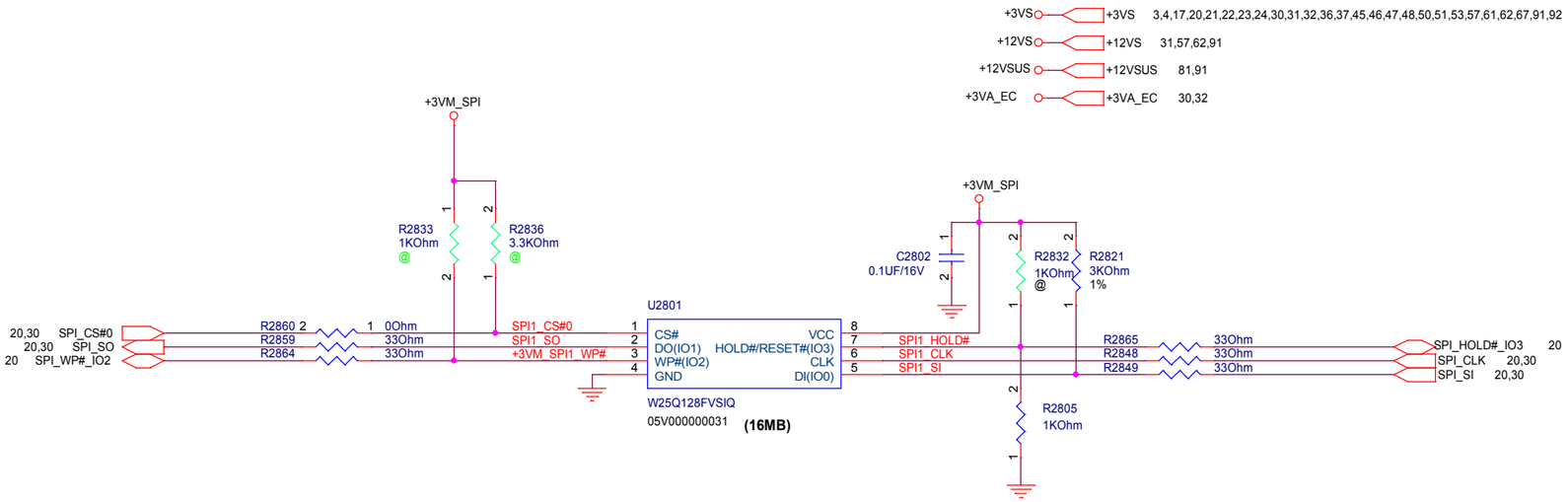
Engineer:

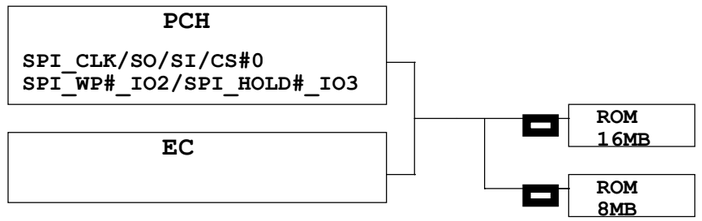
Size	Project Name	Rev
C	KTU_CSM	1.1

Date: Tuesday, September 06, 2016 Sheet 27 of 108

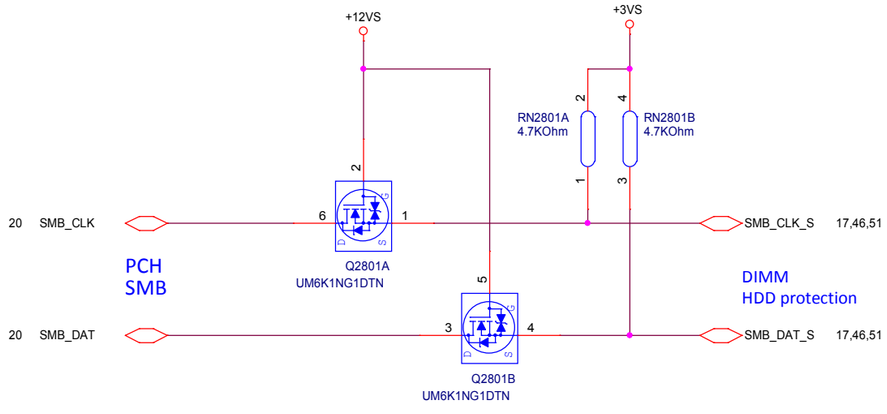
PCH SPI ROM







PCH SMBus



PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title :PCH(8)_SPI,SMB

BG1/HW3 Engineer: Bill Yang

Size Custom | Project Name P4 | Rev 1.0

Date: Tuesday, September 06, 2016 | Sheet 28 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 29 of 108

+3VA_EC +3VA_EC 28,32
+3VS +3VS 3,4,17,20,21,22,23,24,28,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+3VSUS +3VSUS 4,24,25,26,28,31,33,41,42,51,53,62,67,68,81,92
+3VA +3VA 24,31,36,41,43,53,56,57,67,81,88,93
+1.8VSUS +1.8VSUS 9,21,24,26,84
+VCCDSW +VCCDSW 25,26

U3001

42 PD_VBUS_OFF_EC# — PD_VBUS_OFF_EC# — 3 GPH7
+3VAPLL — 127 VSTBY(PLL)
114 VSTBY5
92 VSTBY4
50 VSTBY3
+3VA_EC — 26 VSTBY2
VSTBY1
+3VACC — 74 AVCC
+3VS — R3023 1 2 0Ohm EC_VCC 11 VCC

20,44,62 LPC_AD0 — SP3001 1 2 LAD0 10 — LAD0/GPM0
20,44,62 LPC_AD1 — SP3002 1 2 LAD1 9 — LAD1/GPM1
20,44,62 LPC_AD2 — SP3003 1 2 LAD2 8 — LAD2/GPM2
20,44,62 LPC_AD3 — SP3004 1 2 LAD3 7 — LAD3/GPM3
20 CLK_KBCPCI_PCH — SP3005 1 2 CLK_KBCPCI_EC 13 — LPCCLK/GPM4
20,44,62 LPC_FRAME# — 6 LFRAME#/GPM5
25,32,33,51,53,62 BUF_PLT_RST# — SP3026 1 2 LPCRST#_EC 22 — LPCRST#/GPD2
20,44,62 INT_SERIRQ — 5 SERIRQ/GPM6
3,44 EXT_SMI# — SP3006 1 2 EXT_SMI#_EC 15 — ECSMI#/GPD4
3 EXT_SCI# — SP3007 1 2 EXT_SCI#_EC 23 — ECSCI#/GPD3
T3001 1 A20GATE 126 — GA20/GPB5
20 RCIN# — RCIN# 4 — KBRST#/GPB6
32 EC_RST# — 14 WRST#

31 KSI0 — 58 KSI0/STB#
31 KSI1 — 59 KSI1/AFD#
31 KSI2 — 60 KSI2/INIT#
31 KSI3 — 61 KSI3/SLIN#
31 KSI4 — 62 KSI4
31 KSI5 — 63 KSI5
31 KSI6 — 64 KSI6
31 KSI7 — 65 KSI7
31 KSO0 — 36 KSO0/PD0
31 KSO1 — 37 KSO1/PD1
31 KSO2 — 38 KSO2/PD2
31 KSO3 — 39 KSO3/PD3
31 KSO4 — 40 KSO4/PD4
31 KSO5 — 41 KSO5/PD5
31 KSO6 — 42 KSO6/PD6
31 KSO7 — 43 KSO7/PD7
31 KSO8 — 44 KSO8/ACK#
31 KSO9 — 45 KSO9/BUSY
31 KSO10 — 46 KSO10/PE
31 KSO11 — 51 KSO11/ERR#
31 KSO12 — 52 KSO12/SLCT
31 KSO13 — 53 KSO13
31 KSO14 — 54 KSO14
31 KSO15 — 55 KSO15

31 PTP_PWR_EN — 119 DSR0#/GPG6
3 THRO_CPU — 123 CTX0/TMA0/GPB2

88 BAT_LEARN — 85 PS2CLK0/TMB0/CEC/GPF0
53 WLAN_RST#_EC — 86 PS2DAT0/TMB1/GPF1
25 PM_PWRBTN# — PM_PWRBTN# 87 PS2CLK1/DTR0#/GPF2
25 SUSACK# — R3072 2 @ 1 0Ohm — 88 PS2DAT1/RTS0#/GPF3
37 OP_SD#_EC — R3073 2 @ 1 0Ohm — 89 PS2CLK2/GPF4
31 TP_PS2_DAT — TP_PS2_DAT 90 PS2DAT2/GPF5
31 TP_PS2_CLK — TP_PS2_CLK
41,46,60,88 SMB0_CLK — SMB0_CLK 110 SMCLK0/GPB3
41,46,60,88 SMB0_DAT — SMB0_DAT 111 SMDAT0/GPB4
SMB1_CLK 115 SMCLK1/GPC1
SMB1_DAT 116 SMDAT1/GPC2
3 H_PECI_EC — 117 SMCLK2/PECI/GPF6
45 LCD_BKLTEN_EC — 118 SMDAT2/PECIRQT#/GPF7

41 PD_RST#_EC — PD_RST#_EC 81 DAC5/RIG0#/GPJ5
67 USBP01_EN — USBP01_EN 80 DAC4/DCD0#/GPJ4
52,81 USB_CPW_EN — 79 DAC3/TACH1B/GPJ3
IOAC_CB2 78 DAC2/TACH0B/GPJ2
T3033 1 GPJ1 77 GPJ1
T3032 1 GPJ0 76 TACH2/GPJ0

24 SW_RTCRST — 128 GPJ6
22 PCH_FLASH_DESCRIPTOR — 2 GPJ7

20,28 SPI_CS#0 — 101 FSCE#/GPG3
20,28 SPI_CLK — 105 FSCK/GPG7
20,28 SPI_SI — 102 FMOSI/GPG4
20,28 SPI_SO — 103 FMISO/GPG5

C3008 10PF/50V @ — GND

IT8987E/BX

ADC0/GPI0 66 — AD_IINP 88
ADC1/GPI1 67 — SUS_PWRGD 81,82,92
ADC2/GPI2 69 — ALL_SYSTEM_PWRGD 25,92
ADC3/GPI3 70 POA_AUTH_ERR — ME_PM_SLP_A# 25
ADC4/GPI4 71 PD_CAB_DET_EC — POA_AUTH_ERR 31
ADC5/DCD1#/GPI5 72 — PD_CAB_DET_EC 41
ADC6/DSR1#/GPI6 73 POA_POWERREQ — WLAN_WAKE# 53
ADC7/CTS1#/GPI7 — POA_POWERREQ 31

PWM0/GPA0 24 — PWR_BLUE_LED# 56
PWM1/GPA1 25 — CHG_BLUE_LED# 56
PWM2/GPA2 28 — CHG_ORG_LED# 56
PWM3/GPA3 29 — PWR_ORG_LED# 56
PWM4/GPA4 30 — FAN0_PWM 50
PWM5/GPA5 31 GPA5 — T3031
PWM6/SSCK/GPA6 32 — EC_SPKR 36
PWM7/RIG1#/GPA7 34 — KEYBOARD_LED# 31

RXD/SIN0/GPB0 108 NUM_LED# — NUM_LED# 56
TXD/SOUT0/GPB1 109 CAP_LED# — CAP_LED# 56
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 112 PM_RSMRST# — PM_RSMRST# 25

KSO16/SMOSI/GPC3 56 — KSO16 31
TMRI0/GPC4 120 AC_IN_OC_EC — SP3008 1 2 AC_IN_OC — AC_IN_OC 88
KSO17/SMISO/GPC5 57 — KSO17 31
TMRI1/GPC6 124 BAT1_IN_OC# — BAT1_IN_OC# 90
PWUREQ#/BBO/SMCLK2ALT/GPC7 16 — ME_AC_PRESENT 25

RI1#/GPD0 18 PM_SUBS# — PM_SUBS# 25,68
RI2#/GPD1 21 PM_SUSC# — PM_SUSC# 25,68
GINT/CTS0#/GPD5 33 SYS_PWROK_EC_R — R3067 1 @ 2 0Ohm — SYS_PWROK 25,68
TACH0A/GPD6 47 FAN0_TACH — SP3010 1 2 — SYS_PWROK_EC 68
TACH1A/TMA1/GPD7 48 GPD7 — T3030
SP3009 1 2 VSUS_ON — VSUS_ON 81,82,84,93
19 VSUS_ON_EC — R3063 1 @ 2 0Ohm — SUSC_EC# 57,68,91
L80HLAT/BAO/GPE0 82 SUSC_EC# — R3064 1 @ 2 0Ohm — SUSB_EC# 57,68,91,92
EGA/GPE1 83 SUSB_EC# — R3048 1 2 0Ohm — DE_ALL_SYS_PGD_EC 68
EGCS#/GPE2 84 DE_ALL_SYS_PGD_EC — R3065 1 @ 2 0Ohm — DE_ALL_SYS_PGD_S — R3049 1 2 0Ohm — DELAY_ALL_SYSTEM_PWRGD 25
EGCLK/GPE3 125 BT_ON/OFF#_EC — R3066 1 @ 2 0Ohm — CPU_VRON 80
SSCE1#/GPG0 35 ILIM_SEL — DE_ALL_SYS_PGD_HW 68
RTS1#/GPE5 17 LID_SW# — BT_ON/OFF#_EC 53
LPCPD#/GPE6 20 POA_PWR_INT# — ILIM_SEL 52
L80LLAT/GPE7 — LID_SW# 31,45,56,61
POA_PWR_INT# 31 — T3002 T3003

VSTBY_FSPI 106 — +3VAPLL
PWRSW/GPE4 107 PWR_SW# — PWR_SW# 31
SSCE0#/GPG2 100 TP_OFF#_EC — TP_OFF#_EC 31
VSS5 104 — GND

CLKRUN#/GPH0/ID0 93 — PM_CLKRUN# 20,62
CRX1/SIN1/SMCLK3/GPH1/ID1 94 — CHGCB0 52
CTX1/SOUT1/SMDAT3/GPH2/ID2 95 — CHGCB1 52
GPH3/ID3 96 POA_EN# — POA_EN# 31
GPH4/ID4 97 POA_FP_PWREN — POA_FP_PWREN 31
GPH5/ID5 98 USB_SW_EN — USB_SW_EN 31
GPH6/ID6 99 PD_PWR_EN_EC — PD_PWR_EN_EC 41

VSS1 1 — GND — C3012 1 2 0.1UF/16V — GND
VCORE 12
VSS2 27
VSS3 49
VSS4 91
CRX0/GPC0 113 — SUSWARN#/SUSPWRDNACK 25
DTR1#/SBUSY/GPG1/ID7 122 — R3038 1 2 0Ohm — TP_IRQ# 21,31
AVSS 75 — EC_AGND

Battery / Charger
GPU

52 CHGCB2 — R3096 2 @ 1 0Ohm — IOAC_CB2
53 IOAC_EN — R3097 2 @ 1 0Ohm

+3VA_EC — R3093 0Ohm — +3VA_I2C_MUX — C3015 0.1UF/16V — GND
R3091 1 @ 2 0Ohm
R3092 1 @ 2 0Ohm
R3095 0Ohm
21 I2C0_MUX_SEL — I2C0_MUX_SEL_R
41 SMB1_CLK_CFG
41 SMB1_DAT_CFG
U3003 NX3DV221GM
S D+ D- OE# VCC GND 1D+ 1D- 2D+ 2D-
SMB1_CLK — SMB1_CLK
SMB1_DAT — SMB1_DAT
I2C_SCL_MUX_S 21
I2C_SDA_MUX_S 21
R3094 10KOhm — GND
VCC: 2.3V~3.6V
Ig:Max 30uA
Ishut-down: Max 2uA
Active Low:<0.25*VCC

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

For EC Power

+3VA — B3001 1 2 120Ohm/100Mhz — +3VA_EC
+3VDB_EC — B3003 1 @ 2 120Ohm/100Mhz

+3VA_EC — C3001 10UF/6.3V — C3002 0.1UF/16V — C3003 0.1UF/16V — GND

+3VA_EC — C3004 10UF/6.3V — GND
SP3012 1 2 NB_R0402_20MIL_SMALL — +3VAPLL — C3005 0.1UF/16V — GND
For +3VPLL Nearby pin 127

SP3011 1 2 NB_R0402_20MIL_SMALL — GND — EC_AGND

+3VS — C3006 0.1UF/16V — GND
SP3013 1 2 NB_R0402_20MIL_SMALL — +3VACC — C3007 0.1UF/16V — EC_AGND

For PU / PD

+3VA_EC — R3001 1 N/A 2 47KOhm BAT1_IN_OC#
R3002 1 @ 2 10KOhm AC_IN_OC
RN3001A 1 2 4.7KOhm SMB0_CLK
RN3001B 3 4 4.7KOhm SMB0_DAT

+3VA_EC — R3014 1 2 10KOhm LID_SW#

+3VA_EC — RN3001D 7 8 4.7KOhm SMB1_DAT
RN3001C 5 6 4.7KOhm SMB1_CLK

+3VS — RN3002A 1 2 4.7KOhm TP_PS2_CLK
RN3002B 3 4 4.7KOhm TP_PS2_DAT

PM_SUBS# — R3003 1 2 100KOhm
PM_SUSC# — R3004 1 2 100KOhm
PM_RSMRST# — R3006 1 2 10KOhm
BAT1_IN_OC# — R3050 1 @ 2 100KOhm — GND

RN3003A 1 @ 2 4.7KOhm SUSC_EC#
RN3003B 3 @ 4 4.7KOhm SUSB_EC#
GND

+3VS — R3017 1 @ 2 10KOhm A20GATE
R3018 1 2 10KOhm RCIN#
R3019 1 2 10KOhm FAN0_TACH

141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)
TP_OFF#_EC — R3010 1 @ 2 10KOhm — GND

+3VA_EC — N/A — R3011 1 2 10KOhm VSUS_ON
R3012 1 N/A 2 10KOhm TP_OFF#_EC
HW STRAP PIN??need PU
+3VSUS — R3013 1 @ 2 100KOhm VSUS_ON

+VCCDSW — R3020 1 2 10KOhm PM_PWRBTN#

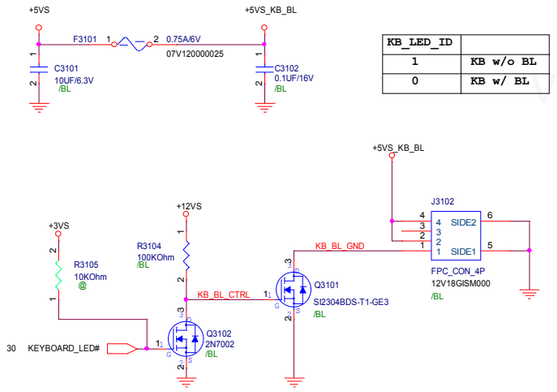
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in

Reserved for IT8587E/FX
AD_IINP R3055 1 @ 2 0Ohm
SUS_PWRGD R3056 1 @ 2 0Ohm
ALL_SYSTEM_PWRGD R3057 1 @ 2 0Ohm
WLAN_WAKE# R3060 1 @ 2 0Ohm
GND

<Variant Name>

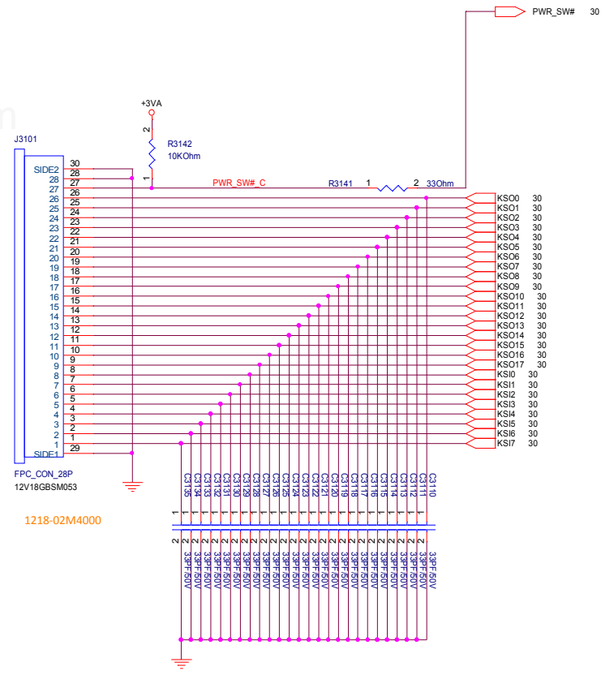
PEGATRON Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1AHW3 Engineer: Bill Yang
Size Custom | Project Name P4 | Rev 1.0
Date: Tuesday, September 06, 2016 | Sheet 30 of 99

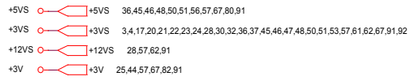
Keyboard LED



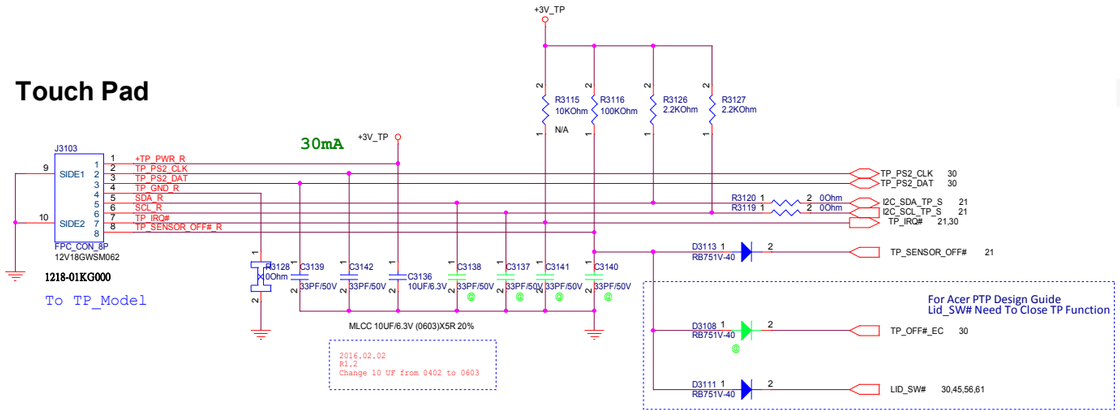
KB_LED_ID	
1	KB w/o BL
0	KB w/ BL

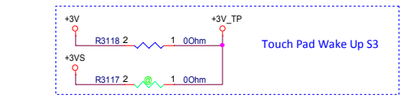
Keyboard

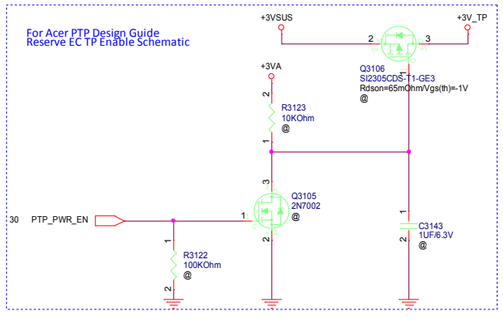




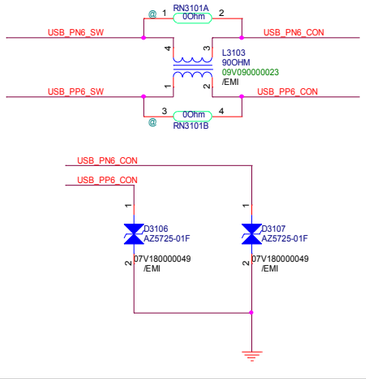
Touch Pad

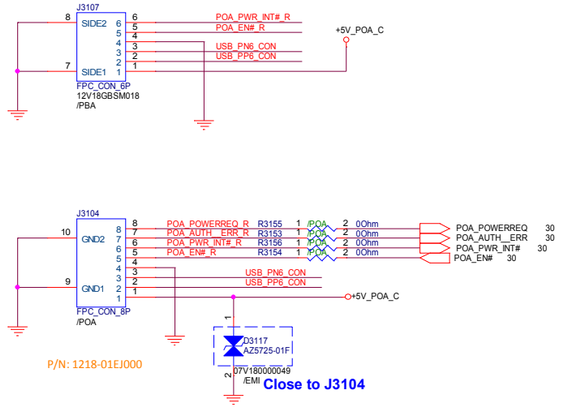


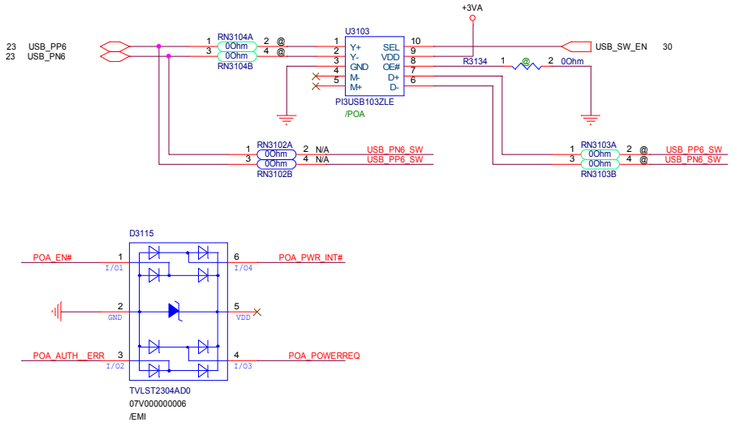


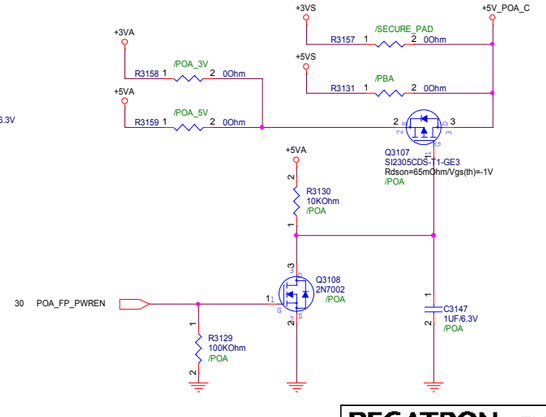


Finger Print









PEGATRON PROPRIETARY AND CONFIDENTIAL

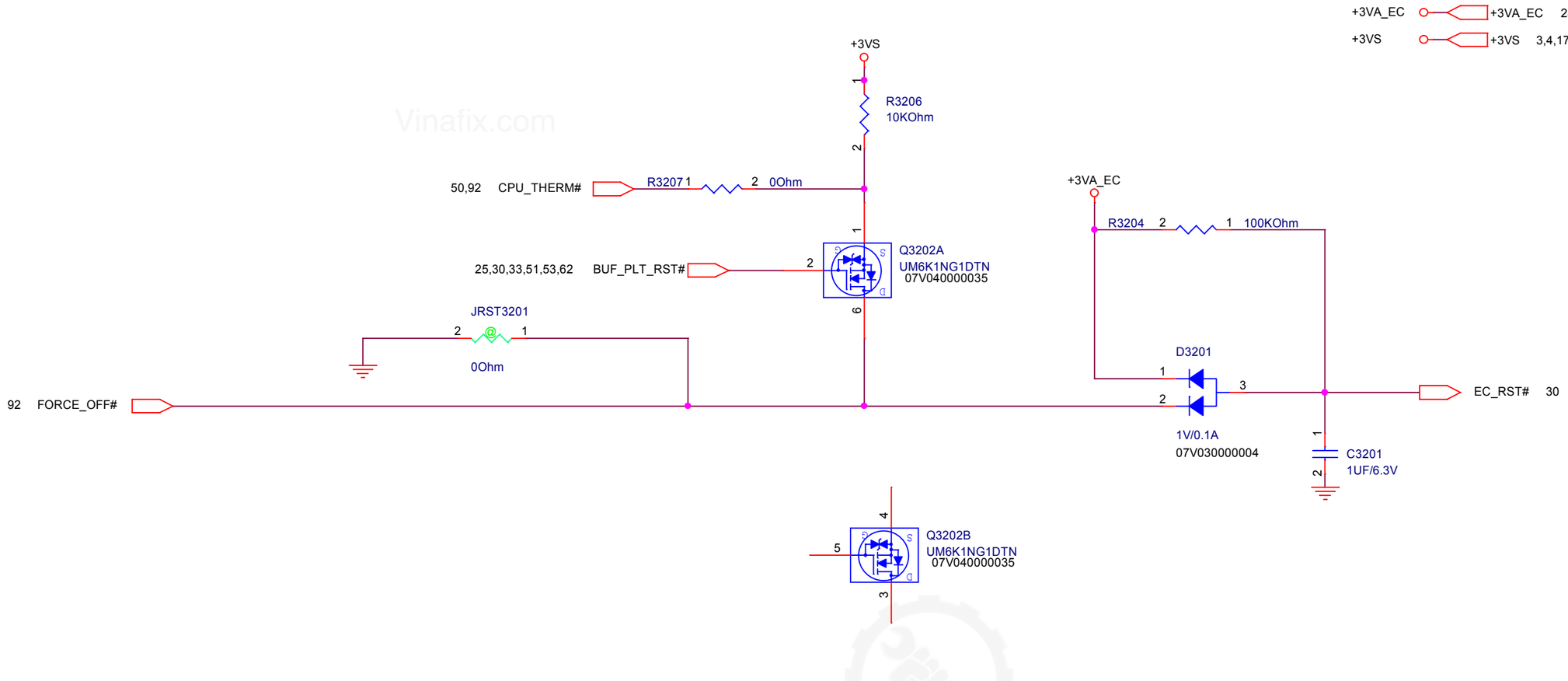
Title : TP / KB / FP

Engineer: Bill Yang

BG1A-W3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 31 of 108



Remove 10s RTC reset

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON	Title : RST_Reset Circuit		
BG1/HW3	Engineer: Bill Yang		
Size: Custom	Project Name: P4		Rev: 1.0
Date: Tuesday, September 06, 2016	Sheet 32 of 108		

+3VSUS_LAN

C3312 22UF/6.3V

C3305 1UF/6.3V

C3311 0.1UF/16V

GND

U3301A

VDD3P3_IN 5
VDD3P3_1 4
VDD3P3_2 15
VDD3P3_3 19
VDD3P3_4 29

MDI_PLUS[0] 13 — LAN_MDI0P 34
MDI_MINUS[0] 14 — LAN_MDI0N 34
MDI_PLUS[1] 17 — LAN_MDI1P 34
MDI_MINUS[1] 18 — LAN_MDI1N 34
MDI_PLUS[2] 20 — LAN_MDI2P 34
MDI_MINUS[2] 21 — LAN_MDI2N 34
MDI_PLUS[3] 23 — LAN_MDI3P 34
MDI_MINUS[3] 24 — LAN_MDI3N 34

4.7UH Irat=1.2A 1 L3301 2

C3308 22UF/6.3V

C3307 10UF/6.3V @

C3306 0.1UF/16V

GND

CTRL0P9 7

VDD0P9_1 8
VDD0P9_11 11
VDD0P9_2 16
VDD0P9_3 22
VDD0P9_4 37
VDD0P9_5 40
VDD0P9_6 43
VDD0P9_7 46
VDD0P9_8 47

Keep short and wide

LED2 25
LED1 27
LED0 26

+3VSUS_LAN

R3309 4.7KOhm

R3303 10KOhm @

R3302 4.7KOhm

RSVD1_VCC3P3 1
LANWAKE_N 2 LAN_WAKE#

LAN_WAKE# 25

LAN_DISABLE_N 3 LAN_DISABLE# _R

0Ohm R3310 2

LAN_DISABLE# 25

LAN_DISABLE does not require pull-up.It is no-stuff default (for testing purpose).

SVR_EN_N 6

R3308 0Ohm

GND

24 CLK_REQ_LAN# — CLK_REQ_N 48

25,30,32,51,53,62 BUF_PLT_RST# — PE_RST_N 36

24 CLK_PCIE_LAN — PE_CLKP 44
24 CLK_PCIE_LAN# — PE_CLKN 45

23 PCIE_RXP_LAN — 0.1UF/16V C3302 — PCIE_RXP_LAN_C — PETp 38
23 PCIE_RXN_LAN — 0.1UF/16V C3301 — PCIE_RXN_LAN_C — PETn 39

23 PCIE_TXP_LAN — PERp 41
23 PCIE_TXN_LAN — PERn 42

JTAG_TCK 35 — T3301
JTAG_TMS 33 — T3302
JTAG_TDI 32 — T3303
JTAG_TDO 34 — T3304

SML0_CLK 28 — SMB_CLK
SML0_DAT 31 — SMB_DATA

XTAL_IN 10 — XTAL_IN
XTAL_OUT 9 — XTAL_OUT

TEST_EN 30
RBIAS 12
GND 49

R3307 3.01KOHM 1%

R3306 1KOhm

GND

WGI219LM
02V000000025

If LAN is the only device on SMBUS, the SMBUS pull-up can be on +3.3V_LAN.

+3.3V_A is always on during G3->S5, S0, Sx, and DeepSx states.

+3VSUS_LAN

R3304 499Ohm

R3305 499Ohm

20,62 SML0_CLK
20,62 SML0_DAT

CPU

25 SLP_LAN#

+3VSUS_LAN

0.165A

R3315 1 2 0Ohm

R3314 1 @ 2 0Ohm +3VSUS_LAN_OUT

R3312 1 0Ohm @ 2 SLP_LAN#_R

U3302
OUT IN
GND
EN DSG
G5244T11U @

R3311 150Ohm @

+3VSUS

+3VSUS_LAN_OUT

C3309 4.7UF/6.3V @

C3310 1UF/6.3V @

U3301B

GND1 50
GND2 51
GND3 52
GND4 53
GND5 54
GND6 55
GND7 56
GND8 57

WGI219LM
02V000000025

GND

XTAL_IN

XTAL_OUT

X3301 25MHZ

C3303 10PF/50V 5%

C3304 10PF/50V 5%

GND GND GND

PEGATRON

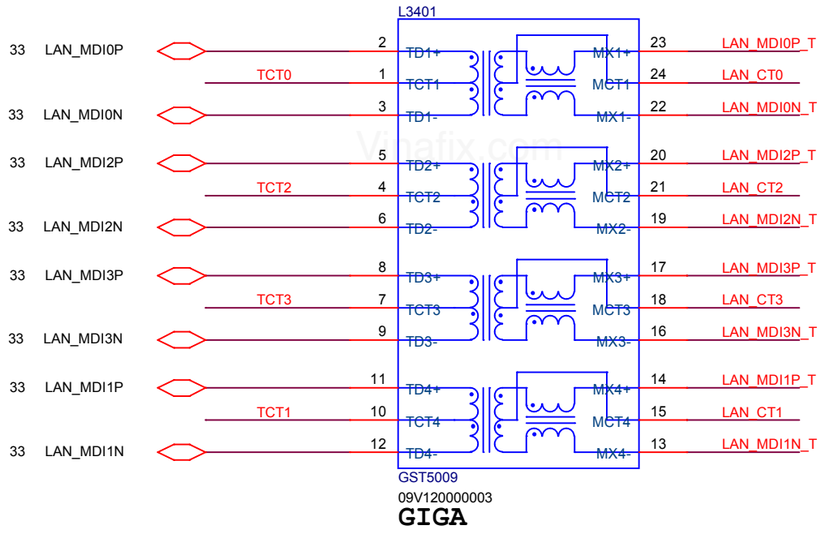
Title : Intel/I219

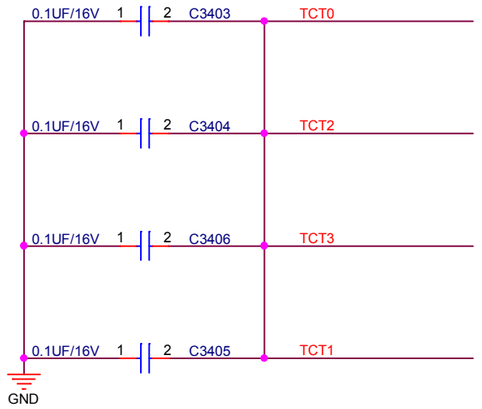
BG1\HW3

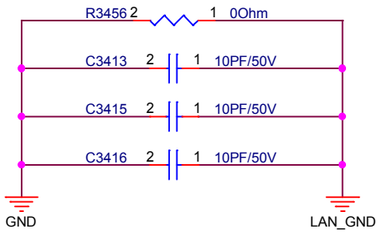
Engineer: Bill Yang

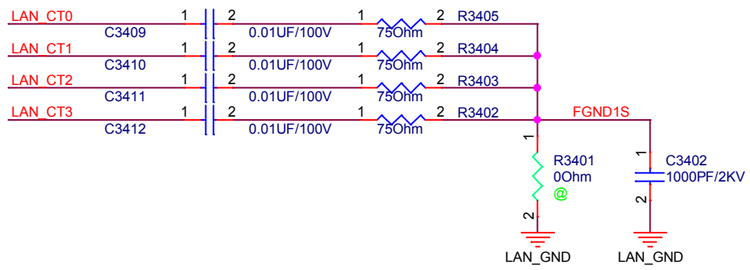
Size	Project Name	Rev
Custom	P4	1.0
	P/N	

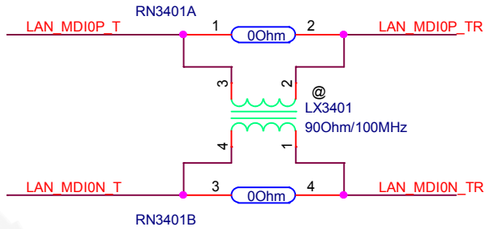
Date: Tuesday, September 06, 2016 Sheet 33 of 108

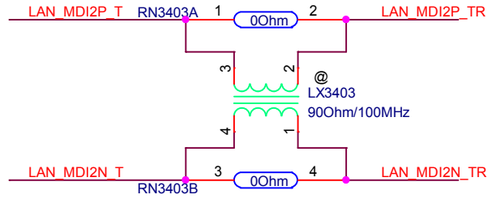


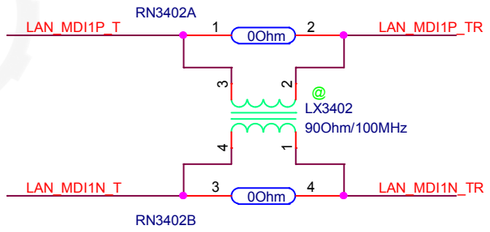


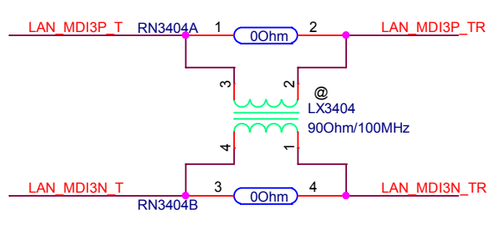


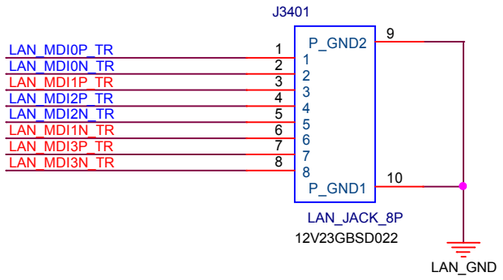


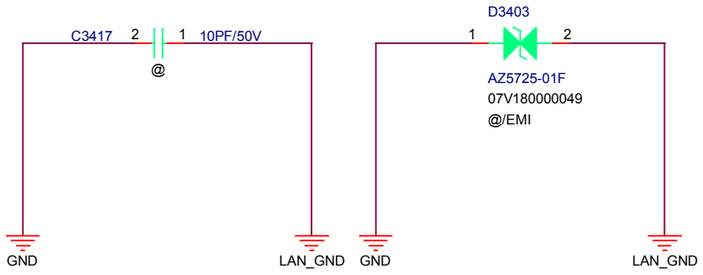


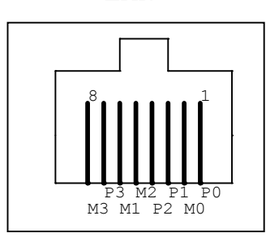












Place near chassis GND

PEGATRON

Title : RJ45

BG1\HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0
	P/N	

Date: Tuesday, September 06, 2016 Sheet 34 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 35 of 108

AUD_ALC255

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+5VS +5VS 31,45,46,48,50,51,56,57,67,80,91

AC_HP_R
AC_HP_L
LINE1_VREFO_L
LINE1_VREFO_R
MIC2_VREFO

U3601B
GND9 58
GND8 57
GND7 56
GND6 55
GND5 54
GND4 53
GND3 52
GND2 51
GND1 50
GND
ALC255-CGT

H_SPKL- R3628 0Ohm AMP_SPK_LN
H_SPKL+ R3627 0Ohm AMP_SPK_LP
H_SPKR- R3626 0Ohm AMP_SPK_RN
H_SPKR+ R3653 0Ohm AMP_SPK_RP

J3602
GND2 6
GND1 5
WTOB_CON_4P
12V17ABSM000

C3640 100PF/50V
C3641 100PF/50V
C3621 100PF/50V
C3642 100PF/50V

Analog
Digital

+1.5VS
L3601 120Ohm/100Mhz
C3612 10UF/6.3V
+5VS_PVDD_AVD
10UF/6.3V C3611

U3601A
CBP
AVSS2
LDO2-CAP
AVDD2
PVDD1
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R-
SPK-OUT-R+
PVDD2
PDB
SPDIF-OUT/GPIO2
GND
H_SPKL+
H_SPKL-
H_SPKR-
H_SPKR+
37 MUTE_AMP#
PDB

+3VS_AUDIO
C3638 10UF/6.3V
C3617 1UF/6.3V
C3616 1UF/6.3V
C3615 2.2UF/6.3V
C3609 10UF/6.3V
R3635 100KOhm
+5VS_AUDIO
C3604 0.1UF/16V
C3637 10UF/6.3V
Place close to Pin 26

CPVDD
CBN
CPVEE
HPOUT-R(PORT-I-R)
HPOUT-L(PORT-I-L)
LINE1-VREFO-L
LINE1-VREFO-R
MIC2-VREF
VREF
LDO1-CAP
AVDD1
AVSS1

LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
VD33_STB
MIC_CAP
MIC2-R(PORT-F-R)/SLEEVE
MIC2-L(PORT-F-L)/RING
MONO-OUT
SPDIFO/FRONT_JD(JD3)/GPIO3
MIC2/LINE2_JD(JD2)
HP/LINE1_JD(JD1)

+3VA
R3637 0Ohm
Digital
Analog

LINE1_L 37
LINE1_R 37
C3614 10UF/6.3V
SLEEVE 37
RING2 37
+3VS_AUDIO
R3604 100KOhm
R3603 200KOhm
HP_JD# 37

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

Place close audio codec

DVDD
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
DC_DET
SDATA-OUT
BCLK
LDO3-CAP
SDATA-IN
DVDD-IO
SYNC
RESETB
PCBEEP
ALC255-CGT

Analog
Digital

PC_BEEP
HDA_RST# 22,37
HDA_SYNC 22
HDA_SDI0 22
HDA_BCLK 22
HDA_SDO 22

+3VS_AUDIO
C3605 10UF/6.3V
C3606 0.1UF/16V
Place close to pin 1

DMIC_DAT_C
DMIC_CLK_C
HDA_BCLK_C
HDA_SDO_C
C3607 10UF/6.3V

37 DMIC_DAT
37 DMIC_CLK
R3614 0Ohm
R3615 22Ohm
C3629 33PF/50V
C3624 33PF/50V

R3621 22Ohm
R3620 22Ohm
C3613 22PF/50V
MLCC 22PF/50V (0402) NPO 5%

+3VS_AUDIO
C3618 0.1UF/16V
C3625 10UF/6.3V

PC_BEEP C3602 0.1UF/16V
PCBEEP
R3605 22KOhm
C3626 100PF/50V
R3618 4.7KOhm

R3638 0Ohm
R3639 0Ohm
D3603 1V/0.2A
HDA_SPKR 22
EC_SPKR 30

2016.02.04
R1.2
EMC/Ricky changes 10 pF to 33 pF

2016.02.02
R1.2
Change 22 pF from 0201 to 0402

+3VS 5mA +3VS_AUDIO
R3636 0Ohm

1.05A
+5VS Digital Analog +5VS_AUDIO
D3602
AZ5725-01F
/EMI
L3603
120Ohm/100Mhz
C3628 10UF/6.3V
Moat
GND A_GND

In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.

2015.12.07
R1.1
EMI build confirm

Add this Filter to avoid other components/chips be influenced

+5VS L3602 600Ohm/100Mhz +5VS_PVDD_AVD
C3622 0.1UF/16V
C3623 10UF/6.3V
C3619 10UF/6.3V
C3601 0.1UF/16V
Close PIN 45
C3620 10UF/6.3V
C3603 0.1UF/16V
Close PIN 46

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Grounding circuit for combo jack SLEEVE pin

+3VS_AUDIO +VCC_RTC +3VA
R3634 100KOhm @
R3633 100KOhm @
R3631 100KOhm @
SLEEVE
Q3601 2N7002 @
HDA_RST# R3619 0Ohm
Q3603 2N7002 @
C3627 1UF/6.3V @
RING2
Q3602 2N7002 @
A_GND

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

20160413 EMI 建議

U3602
GND 1
VC 2
AZ5725-01F
07V180000029
@/EMI
R3625 0Ohm
R3624 0Ohm
R3623 0Ohm
C3635 100PF/50V
C3633 1000PF/50V
C3634 1000PF/50V
GND A_GND

PEGATRON Title : AUD_ALC255
BG1-NB4 Engineer: Bill Yang
Size Custom | Project Name P4 | Rev 1.0
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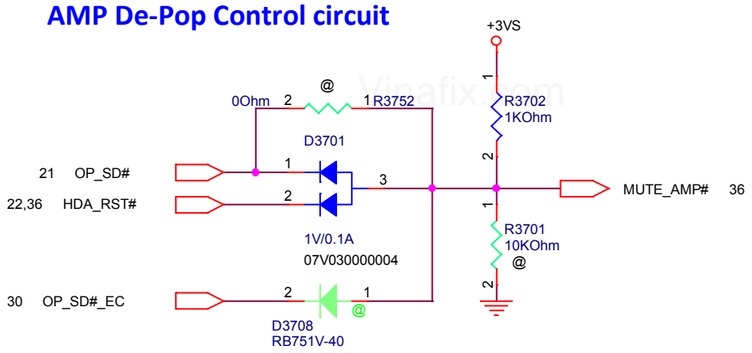
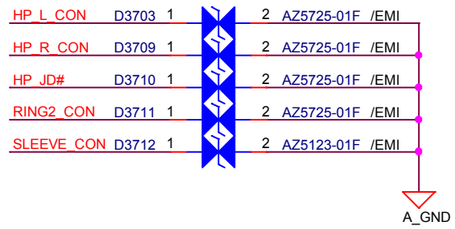
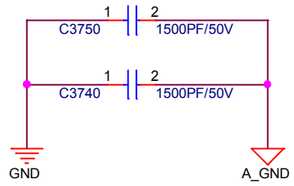
+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,45,46,47,48,50,51,53,57,61,62,67,91,92

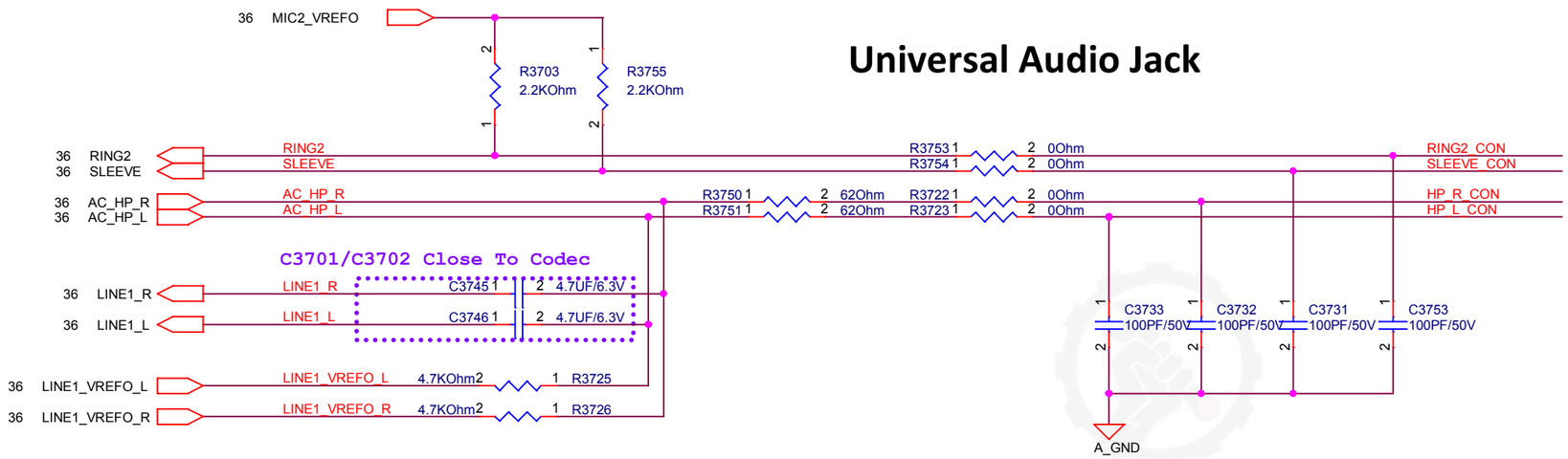
AMP De-Pop Control circuit

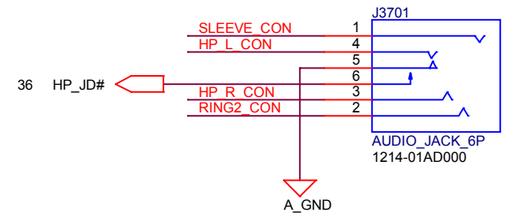




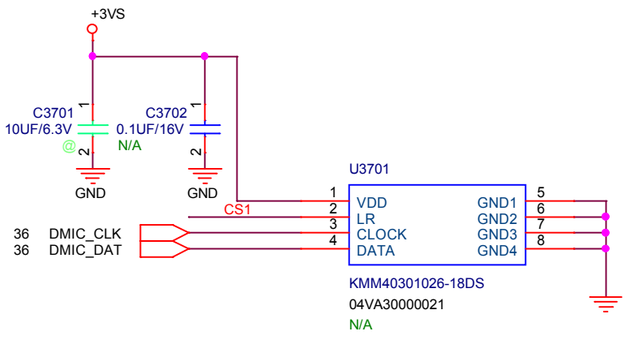


Universal Audio Jack

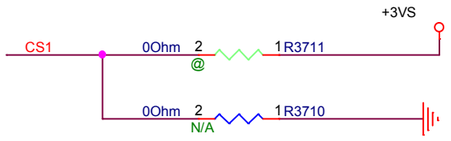


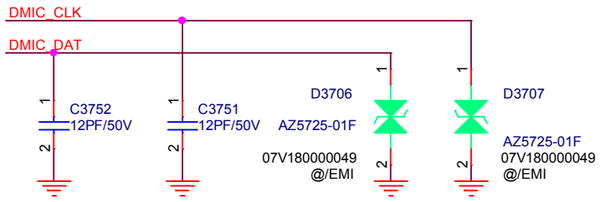


DMIC



Single MIC	Left Channel	Right Channel
CS Pin	Pull Down	Pull Up





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :COMBO_JACK

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 37 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 38 of 108

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 39 of 108

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	40 of 108

ANX7428

R4123, R4124 close to U4701

R4138, R4139 close to U4100

+3VA_PD
R4123 100KOHM vx_r0402_small — DPC_S1_AUXN
R4124 100KOHM vx_r0402_small — DPC_S1_AUXP

+3VA_PD
R4139 100KOHM vx_r0402_small — DPC_S1_AUXN_C
R4138 100KOHM vx_r0402_small — DPC_S1_AUXP_C

+V5_VCONN — C4126 10UF/6.3V @

+3VDB_PD — R4134 0Ohm vx_r0402_0ohm_small — +3VA_PD
+3VSUS — R4130 0Ohm vx_r0402_0ohm_small @ — +3VA
+3VA — R4126 0Ohm vx_r0402_0ohm_small @ — +5VSUS
+5VSUS — R4129 0Ohm vx_r0402_0ohm_small — +V5_VCONN

+VBUS_USB_TYPE_C	+VBUS_USB_TYPE_C	42,43
+3VA	+3VA	24,30,31,36,43,53,56,57,67,81,88,93
+3VA_PD	+3VA_PD	42
+3VSUS	+3VSUS	4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+3VDB_PD	+3VDB_PD	43

DPC_S1_HPD — R4137 100KOhm

The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.

+3VA_PD — C4101 1UF/16V vx_c0402_small — C4102 0.1UF/16V — C4100 1000PF/50V vx_c0402_small
+3VA_PD — C4104 1UF/16V vx_c0402_small — C4105 0.1UF/16V — C4103 1000PF/50V vx_c0402_small

U4100A

Connect to DP Source

47	DDI2_S1_TXP0	C4118 0.1UF/16V	DDI2_S1_TXP0_C	1 DP_LN_0P
47	DDI2_S1_TXN0	C4119 0.1UF/16V	DDI2_S1_TXN0_C	2 DP_LN_0N
47	DDI2_S1_TXP1	C4120 0.1UF/16V	DDI2_S1_TXP1_C	7 DP_LN_1P
47	DDI2_S1_TXN1	C4121 0.1UF/16V	DDI2_S1_TXN1_C	8 DP_LN_1N
47	DDI2_S1_TXP2	C4122 0.1UF/16V	DDI2_S1_TXP2_C	9 DP_LN_2P
47	DDI2_S1_TXN2	C4123 0.1UF/16V	DDI2_S1_TXN2_C	10 DP_LN_2N
47	DDI2_S1_TXP3	C4124 0.1UF/16V	DDI2_S1_TXP3_C	3 DP_LN_3P
47	DDI2_S1_TXN3	C4125 0.1UF/16V	DDI2_S1_TXN3_C	4 DP_LN_3N
47	DPC_S1_AUXP	C4128 0.1UF/16V	DPC_S1_AUXP_C	16 AUXP
47	DPC_S1_AUXN	C4127 0.1UF/16V	DPC_S1_AUXN_C	17 AUXN
47	DPC_S1_HPD	DPC_S1_HPD	PD_HPD (F.P)	37 HPD

AVDD33_1, AVDD33_2: 3.14V~3.3V~3.46V
DVDD_IO: 1.7V~3.3V~3.63V

Connect to USB3.0 signals

42	USB3_RE_TXN	11 SSTX_N
42	USB3_RE_TXP	12 SSTX_P
42	USB3_RE_RXN	5 SSRX_N
42	USB3_RE_RXP	6 SSRX_P

30 PD_RST#_EC (From EC:) — R4125 100KOhm — 33 RESET_N
23 NC

R4133 vx_r0402_0ohm_small: 30 SMB1_DAT_CFG — CFG_SDA
R4132 vx_r0402_0ohm_small: 30 SMB1_CLK_CFG — CFG_SCL
R4127 vx_r0402_0ohm_small: 30,46,60,88 SMB0_DAT — SMB_DAT_PD — 38 CFG_SDA
R4128 vx_r0402_0ohm_small: 30,46,60,88 SMB0_CLK — SMB_CLK_PD — 39 CFG_SCL
43 M_SCL/GPIO_4
42 M_SDA/GPIO_5

+3VA_PD — R4135 1.8KOHM — R4136 1.8KOHM — CFG_SDA / CFG_SCL
42,89 PD_VBUS_CTRL
+3VA_PD — R4120 4.7KOhm vx_r0402_small @

M_SDA/GPIO_5 pin:
Connect to AP/CPU/Charge IC
as a charge mode indicator.

Logic 0: Fast Charger Mode,
charge voltage > 5V or
charge current >= 1.5A.

Logic 1: Normal Charger Mode,
charge voltage = 5V and
charge current <1.5A.

+3VA_PD — R4109 4.7KOhm vx_r0402_small — DRP_EN — 28 DRP_EN
R4112 4.7KOhm vx_r0402_small @

DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.

34 TEST_EN

I2C_ADR_0 — Int. PD 47 — Int. PD 48 — I2C_ADR_1 — I2C_ADR_0/VBUS_Discharge_CTRL — GND — DVSS
ANX7428QN-AD-R
06V500000024

Change to 0650-007L000

I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

R4118 0Ohm vx_r0402_0ohm_small — VBUS_DISCHARGE_CTRL 42

I2C_ADR_0/INTP_IN/GPIO_2:
Connect to AP or CPU to control the discharge of VBUS.
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.

U4100B
50 GND_1
51 GND_2
52 GND_3
53 GND_4
54 GND_5
55 GND_6
56 GND_7
57 GND_8
ANX7428QN-AD-R
06V500000024

I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1,
these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

V5_VCONN is the power source for
VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate
Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required.
It might be necessary to add a diode to
protect the power supply.

Requirement of Q3:
1) Id >= 500mA (Vgs = - 4.5V).
2) Ron < 120 mOhm (Vgs = - 4.5V).
3) Max Vds >= -10V

Connect to USB Type-C connector

SSTXP1	25	UTC_A2_SSTXp1 42
SSTXN1	26	UTC_A3_SSTXn1 42
SSRXN2	35	UTC_A10_SSRXn2 42
SSRXP2	36	UTC_A11_SSRXp2 42
SSTXP2	30	UTC_B2_SSTXp2 42
SSTXN2	29	UTC_B3_SSTXn2 42
SSRXN1	32	UTC_B10_SSRXn1 42
SSRXP1	31	UTC_B11_SSRXp1 42
SBU1	19	UTC_A8_SBU1_AUX 42
SBU2	18	UTC_B8_SBU2_AUX 42

CC1 — 21 CHIP_CC1 — R4102 0Ohm vx_r0402_0ohm_small — UTC_A5_CC1 42
VCONN1_EN — 45 VCONN1_EN
CC_CAP — 22 CC_CAP — C4106 1000PF/50V @
CC2 — 20 CHIP_CC2 — R4105 0Ohm vx_r0402_0ohm_small — UTC_B5_CC2 42
VCONN2_EN — 44 VCONN2_EN

+V5_VCONN — R4103 100KOHM vx_r0402_small — U4101 TPS2041BDBVR (IN, EN#, OUT, GND, OC#)
+V5_VCONN — R4121 100KOHM vx_r0402_small — U4102 TPS2041BDBVR (IN, EN#, OUT, GND, OC#)

0629-007K000
VIN: 2.7V~5.5V
Iq:Max 190uA
Ishut-down: Max 1uA
Active Low:<0.6V
ILMIT:0.6A~0.8A~1.0A

+VBUS_USB_TYPE_C — R4107 750KOhm — VBUS_DIV6 — 15 VBUS_DIV6 — R4110 150KOhm vx_r0402_small 1%

INTP_OUT — 41 (Default: O.D) — PD_INT# — T4101

CABLE_DET — 14 — R4113 0Ohm vx_r0402_0ohm_small — PD_CAB_DET_EC 30
PWR_EN — 27

INTP_OUT pin: interrupt output.
Connect to AP or CPU.

If AP or GPU's interrupt is low level
triggered, set R16 = 4.7K, leave R22
not installed;
else if is high level triggered, set R22
=4.7K, leave R16 not installed.

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

Note:
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse
in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

PD_PWR_EN_EC 30 — R4122 100KOhm

PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

<Variant Name>

PEGATRON Title : POWER_FLOWCHART
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang

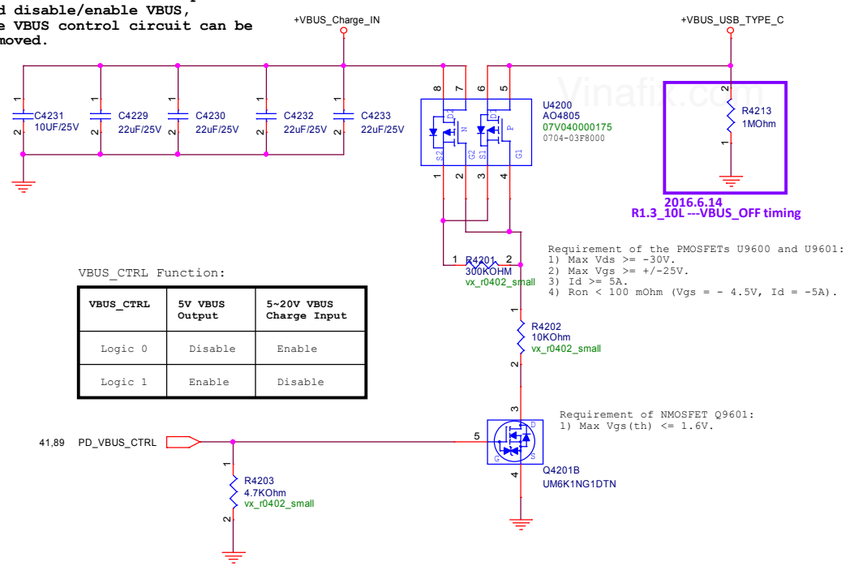
Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 41 of 97

VBUS Control

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS, the VBUS control circuit can be removed.

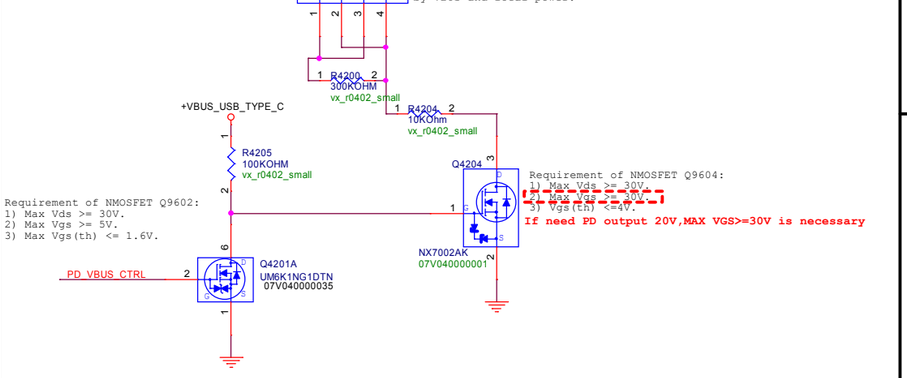
5V VBUS Output Control



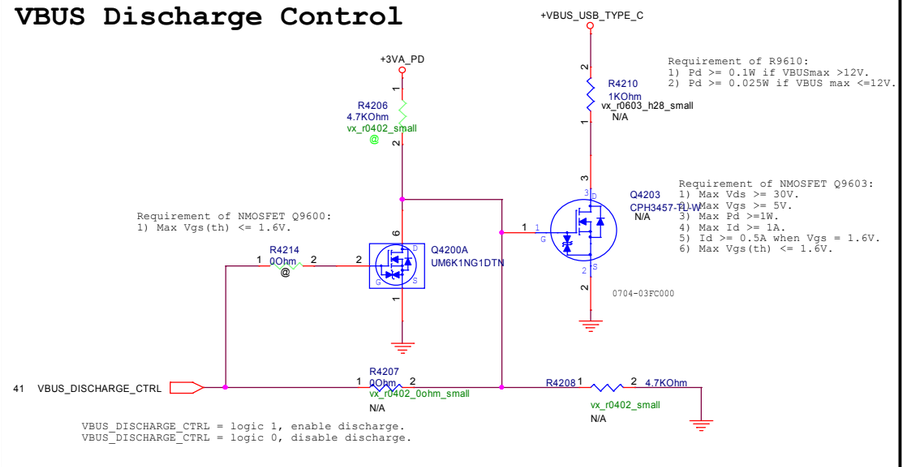
VBUS_CTRL Function:

VBUS_CTRL	5V VBUS Output	5~20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

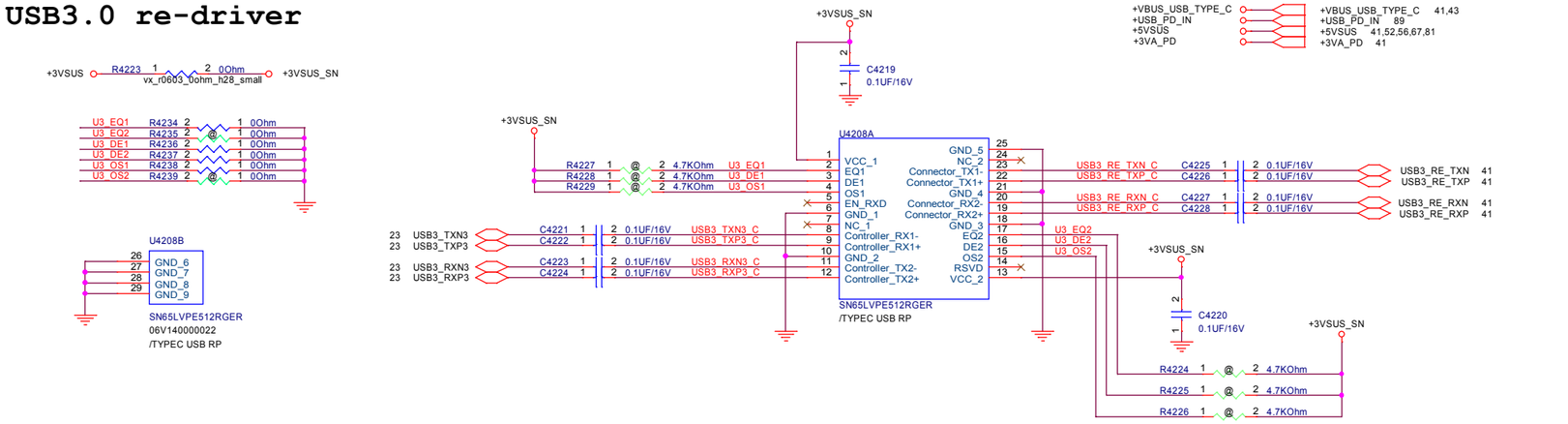
5~20V VBUS Charge Input Control



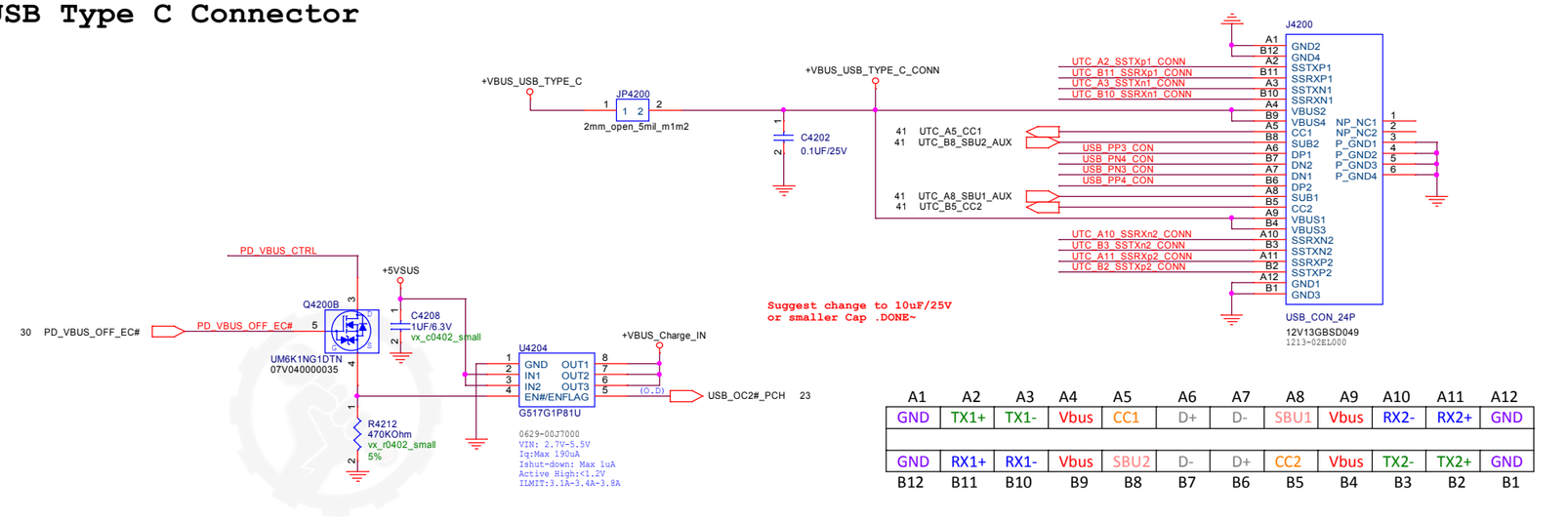
VBUS Discharge Control



USB3.0 re-driver

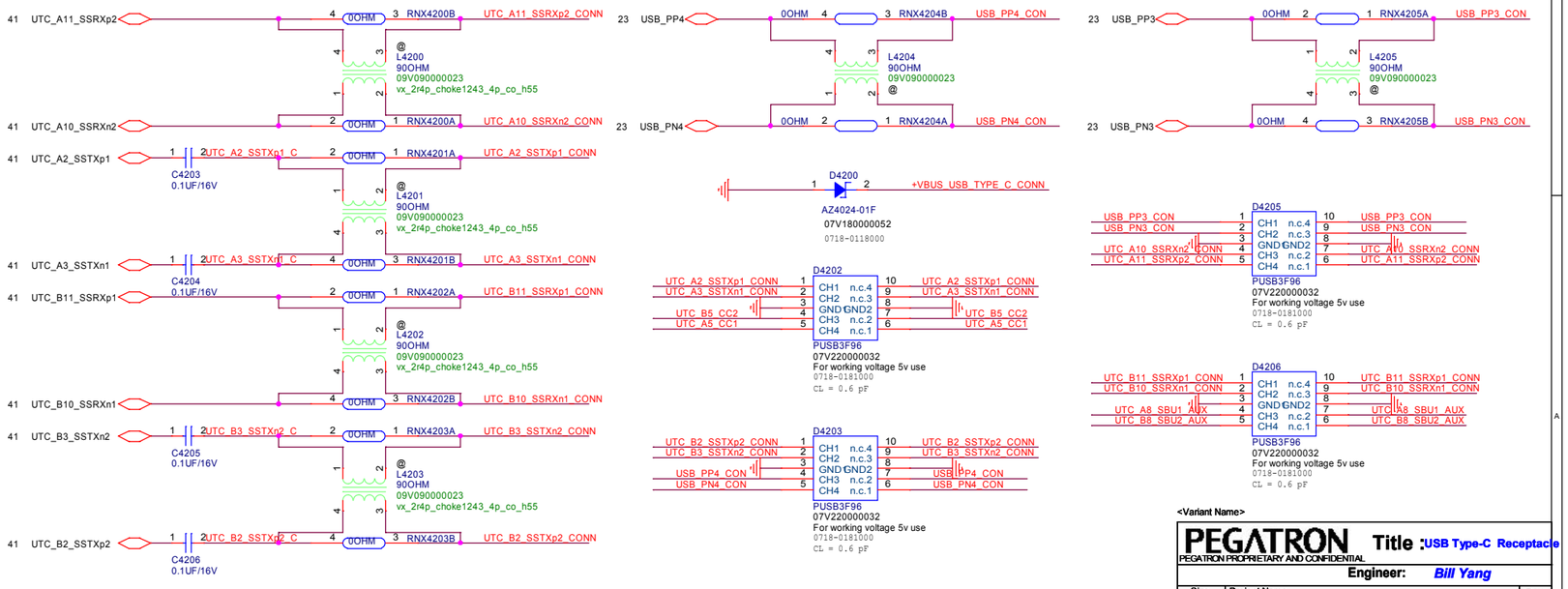


USB Type C Connector



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

ESD



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB Type-C Receptacle

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

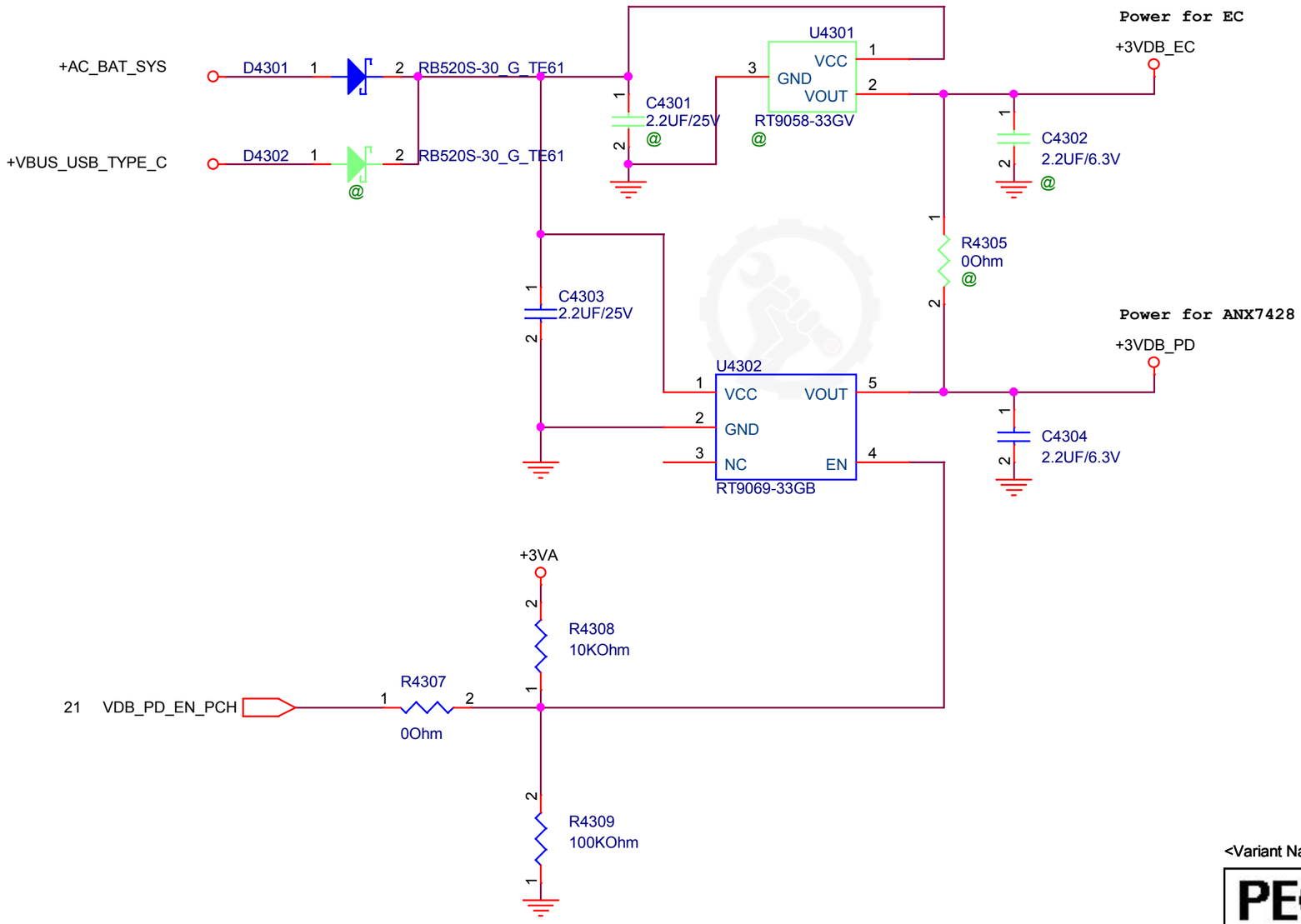
Date: Tuesday, September 06, 2016 Sheet 42 of 108

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

+VBUS_USB_TYPE_C — +VBUS_USB_TYPE_C 41,42
+AC_BAT_SYS — +AC_BAT_SYS 45,80,81,82,83,88
+3VDB_EC — +3VDB_EC 30
+3VDB_PD — +3VDB_PD 41
+3VA — +3VA 24,30,31,36,41,53,56,57,67,81,88,93

Requirement of U1:
1) Vin range: 4V-30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.



<Variant Name>

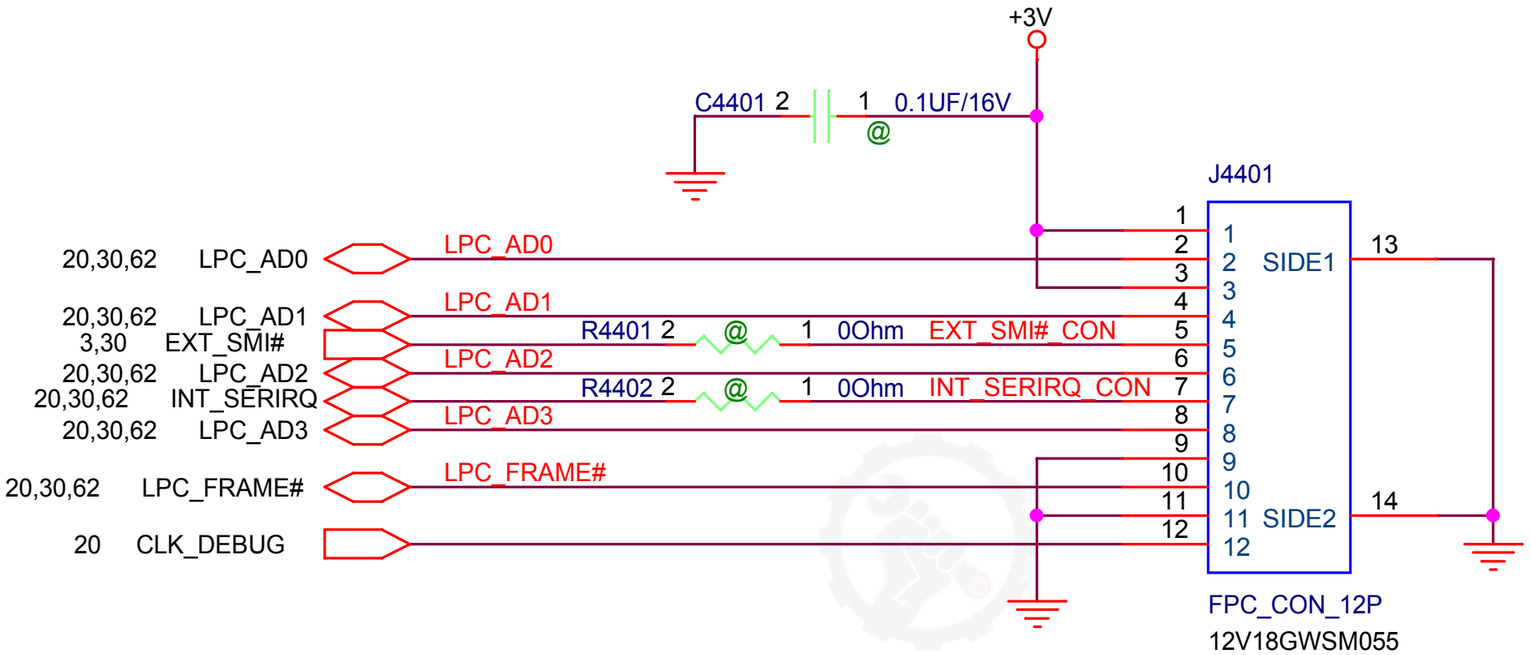
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 43 of 97

+3V +3V 25,31,57,67,82,91



<Variant Name>

PEGATRON Title : BUG_Debug

PEGATRON PROPRIETARY AND CONFIDENTIAL

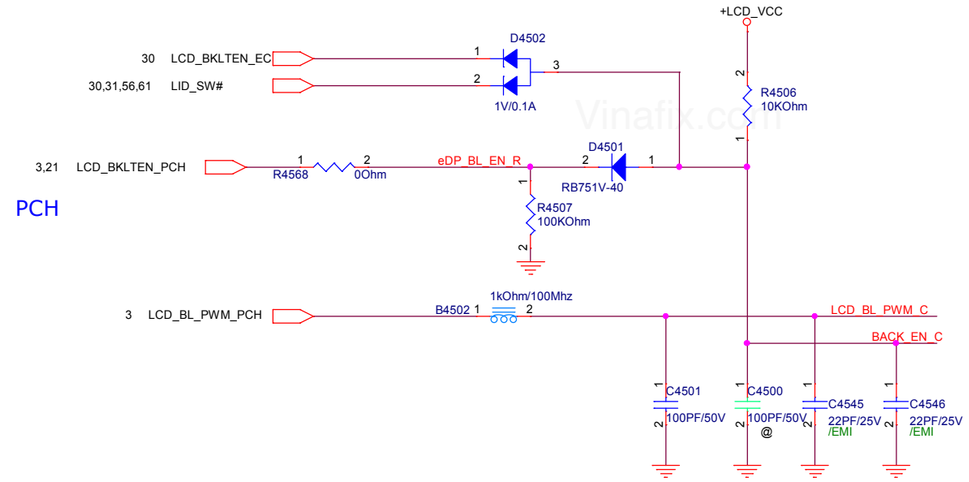
Engineer: Bill Yang

BG1/HW3

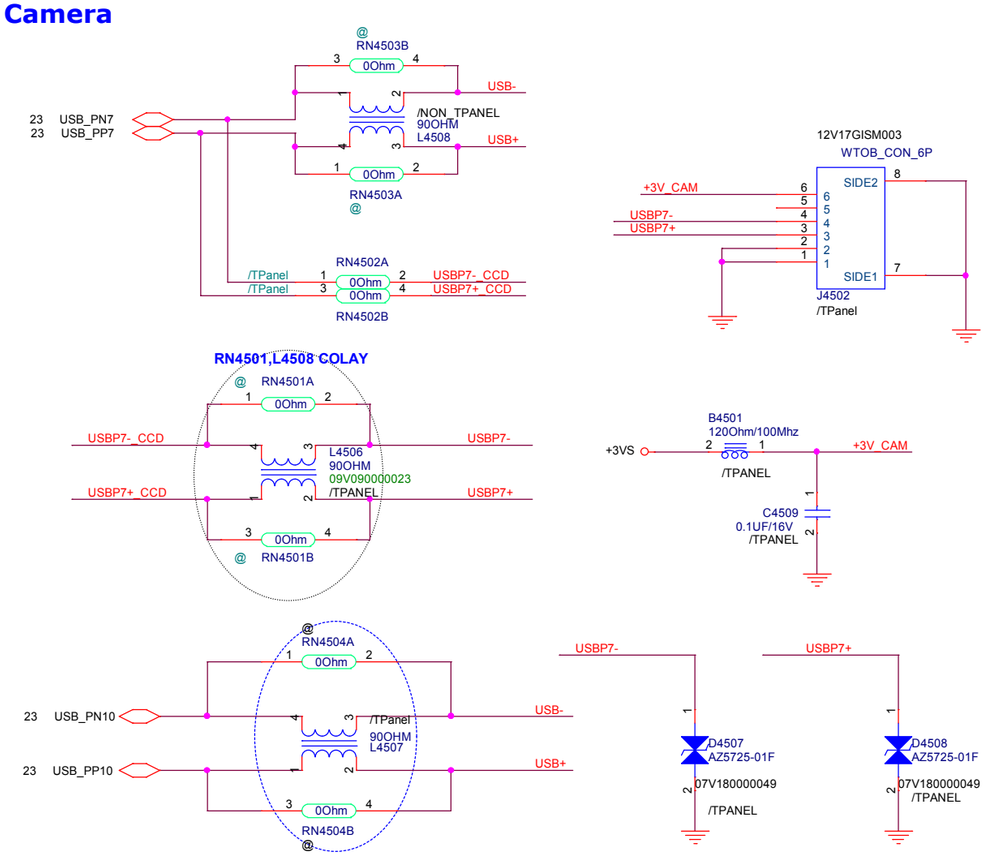
Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 44 of 108

Controller circuit

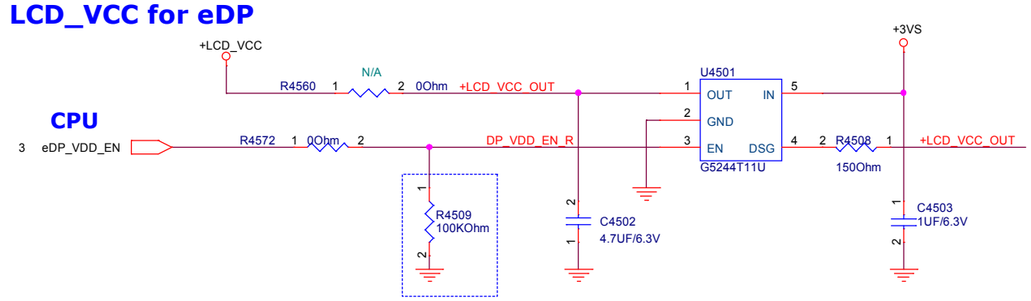


Camera

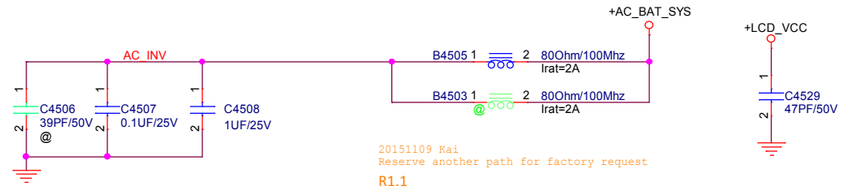


eDP HPD

LCD_VCC for eDP

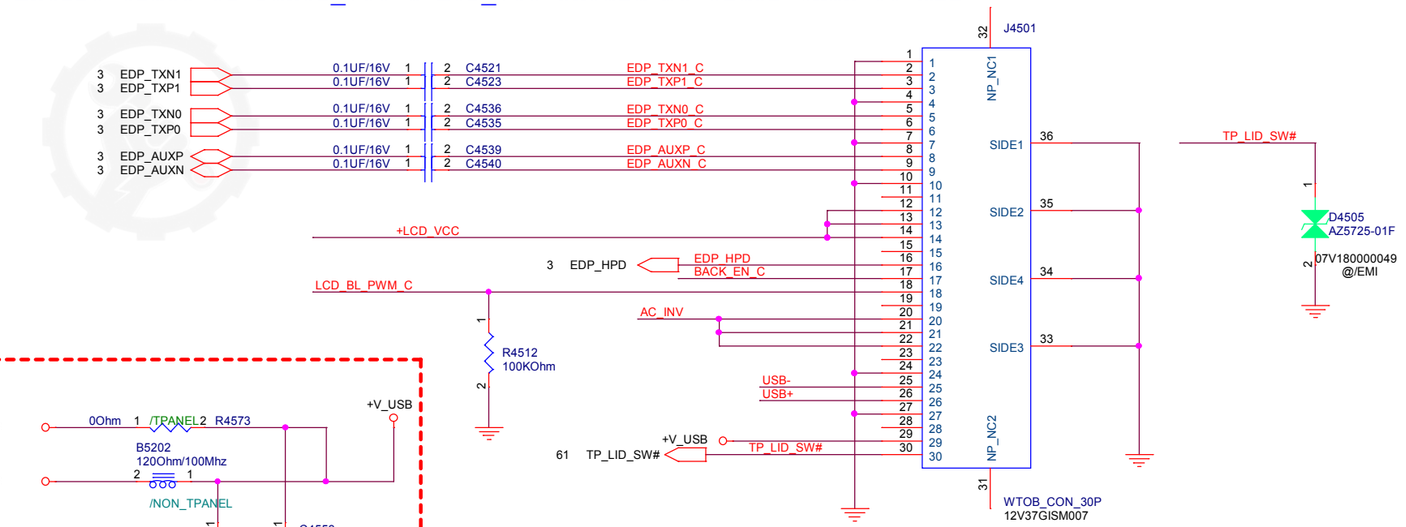


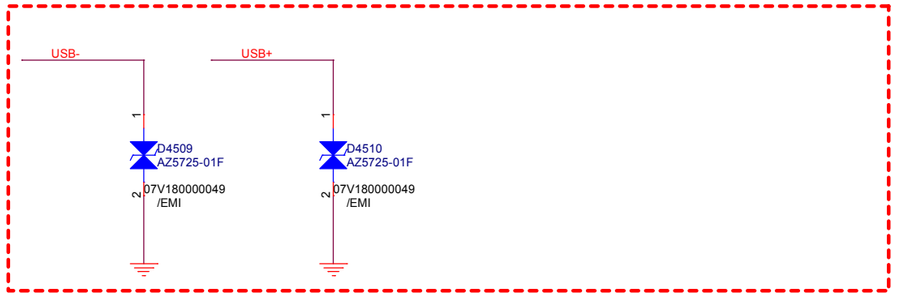
Check PCH/FCH or CPU PD

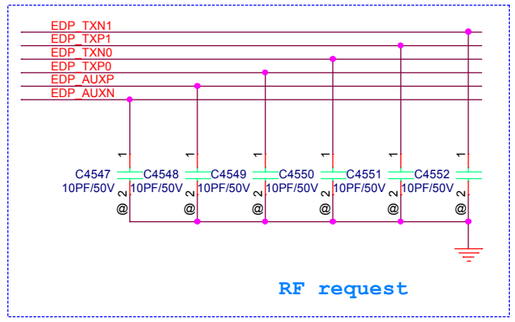


eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LVDS Out

BG1\HW3

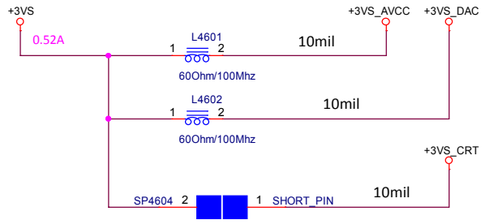
Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 45 of 108

DP2VGA Realtek RTD2166

Power



Rom / Flash Mode :

		POL1 (Pin10)	
		0	1
POL2 (Pin9)	0	No Use	No Use
	1	**(V) Rom mode**	Ext Flash mode

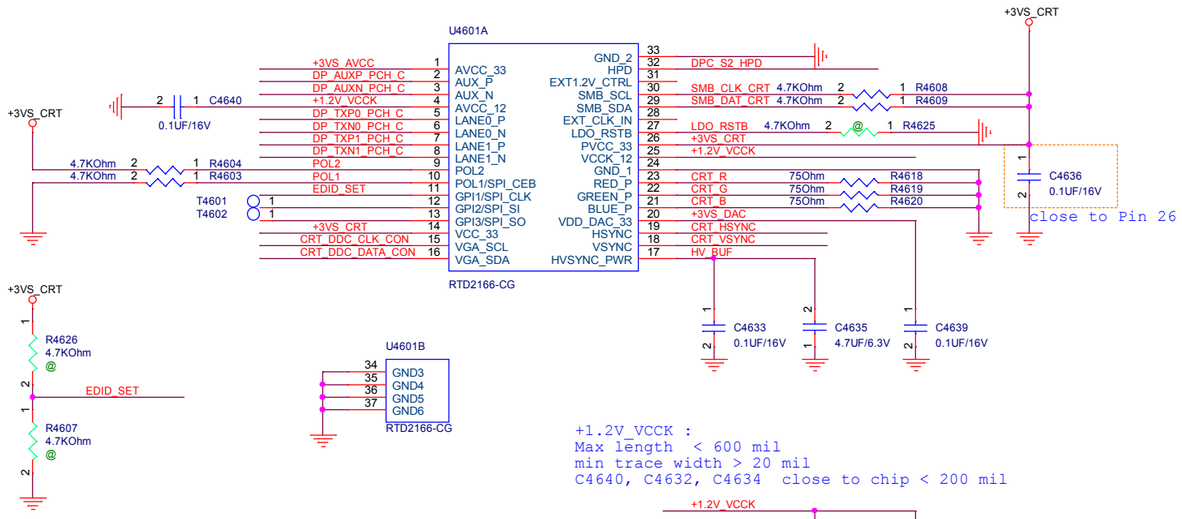
Embedded EDID setting :

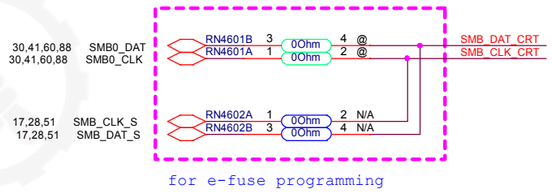
EDID_SET (Pin11)	Mode
0 or NC	**(V) Disable RTD2166 Embedded EDID**
1	Enable RTD2166 Embedded EDID

LDO Mode :

LDO_RSTB (Pin27)	Mode
1 or NC	**(V) embedded LD0 Mode**
0	External 1.2V Mode

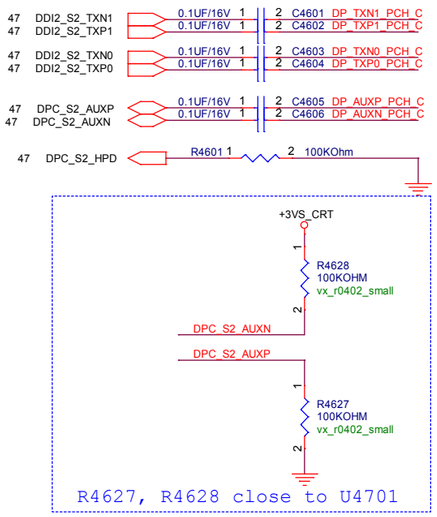
1: Pull High 0: Pull Down



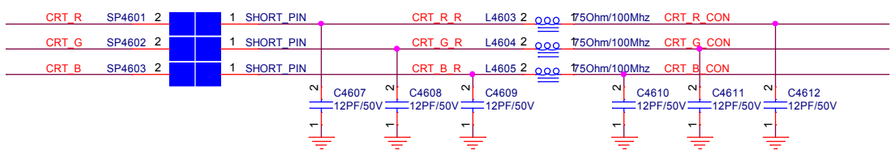


CPU Interface

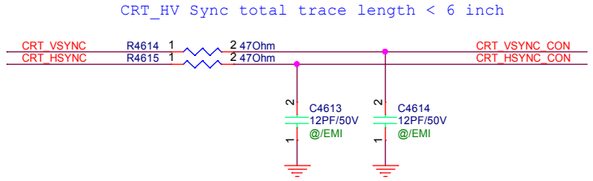
DP main link total length < 8 inch
VIA < 2

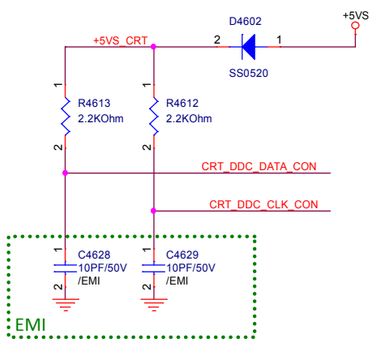


Max mismatch between RGB signal < 200 mil,
total trace length < 6 inch

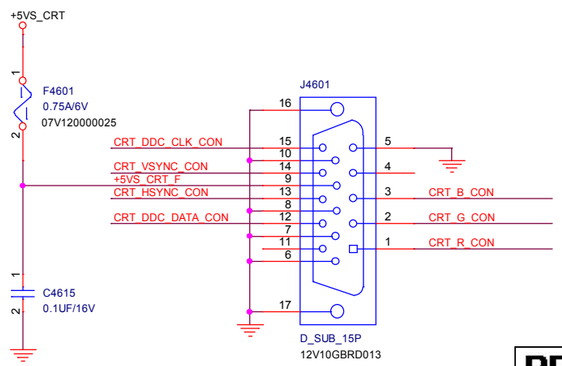


CRT_HV Sync total trace length < 6 inch





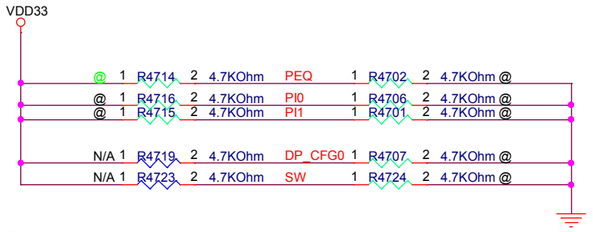
D-SUB Connector



PEGATRON Title : CRT RTD2166
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Bill Yang
<OrgName>
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 46 of 104

+1.5VS +1.5VS 36,57,85

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,48,50,51,53,57,61,62,67,91,92



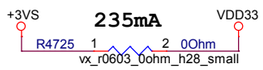
CFG0: operational mode configuration;
L: Control switching mode (default) int PD
H: Automatic switching mode

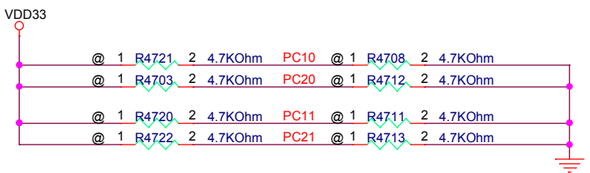
SW: Port switching control or priority configuration;
L: Port1 is selected or with higher priority (default) Int PD
H: Port2 is selected or with higher priority

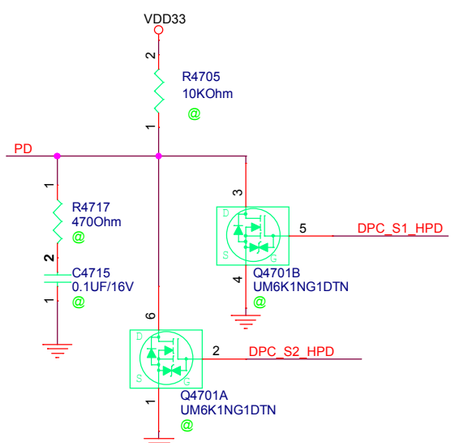
If Type C DP and VGA plug at the same time.
Only VGA have output.

PEQ:
Programmable input equalization levels;
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2 Int PD
H: HEQ, compensate channel loss up to 14.5dB @ HBR2

PI0:
Automatic EQ disable;
L: Automatic EQ enable (default) Int PD
H: Automatic EQ disable
PI1:
Auto test enable;
L: Auto test disable & input offset cancellation enable (default) Int PD
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable







PD:
PD = L: Normal operation
PD = H: Power down

PD	S1	S2
H	L	L
L	H	L
L	L	H
L	H	H

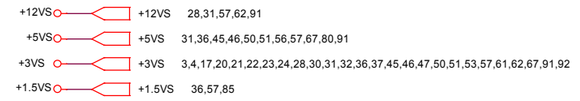
PC10,PC20
AUX interception disable for Port y (y = 1, 2).
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

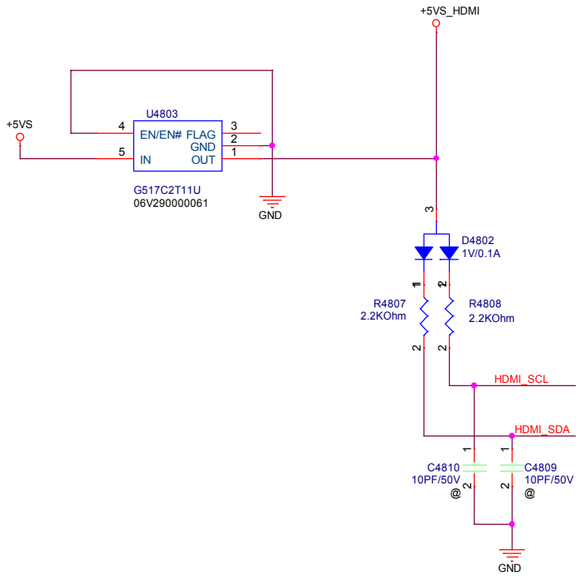
PC11,PC21
Output swing adjustment for Port y (y = 1, 2).
L: default
H: +20%
M: -16.7%

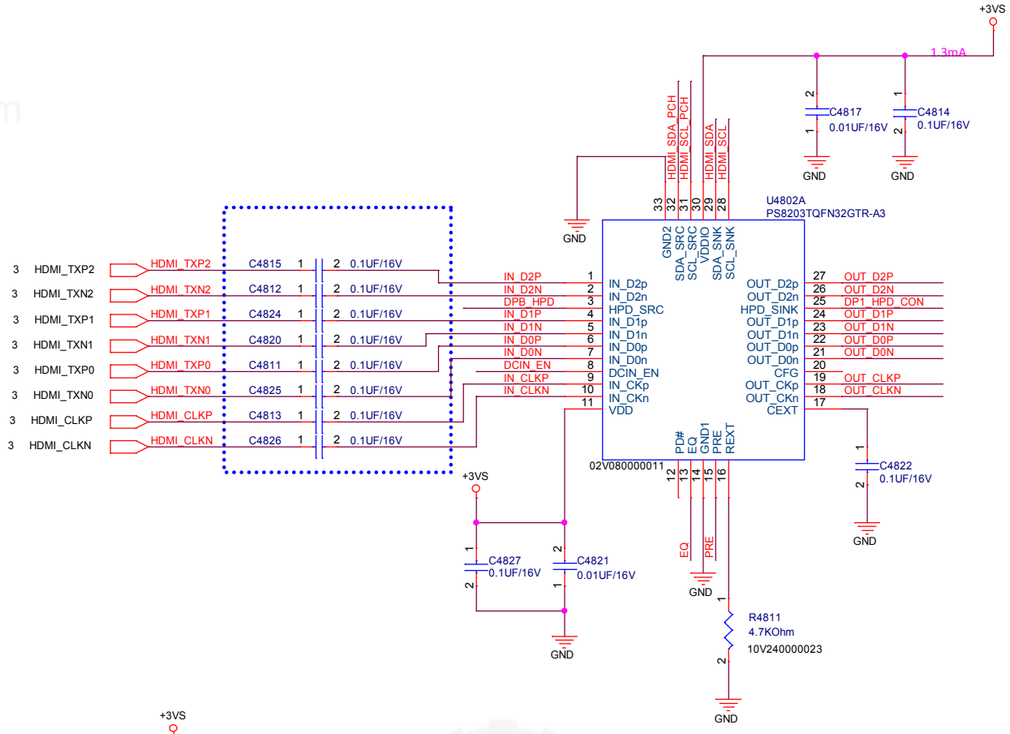
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

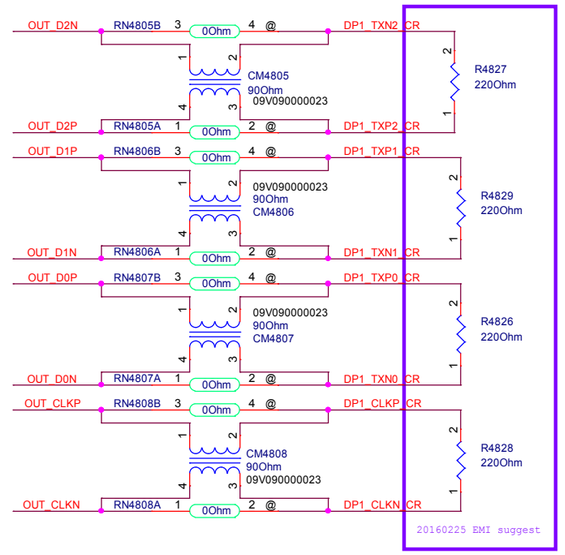
Title : DP_SWITCH
Engineer: Bill Yang
BG1/HW3
Size: Custom | Project Name: P4 | Rev: 1.0
Date: Tuesday, September 06, 2016 | Sheet 47 of 108

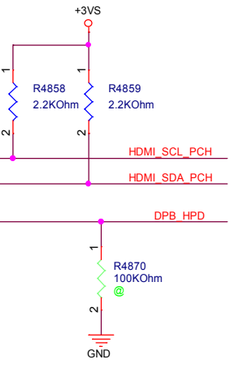
HDMI

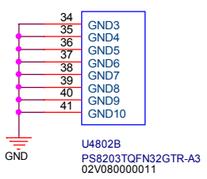


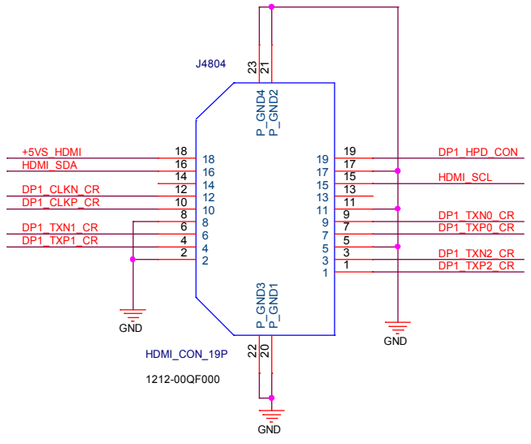




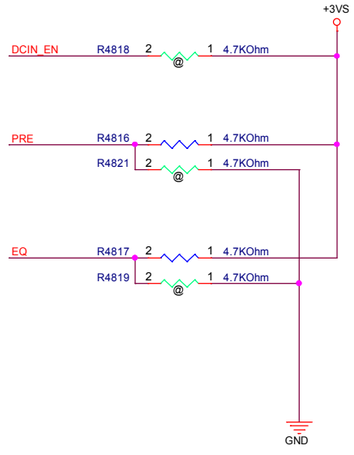









```
DCIN_EN : DC cou;ing enable; Internal pull down at ~150k次, 3.3V I/O.
   L: default, AC coupling input
   H: DC coupling input
PRE : Output pre-emphasis setting; Internal pull down at ~150k次, 3.3V
I/O.
   L: no pre-emphasis
   H: 2.5dB pre-emphasis
EQ : Receiver equalization setting; Internal pull down at ~150k次, 3.3V
I/O.
   L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
   H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
   M: programmable EQ for channel loss up to 8.6dB @ 3Gbps
```



<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

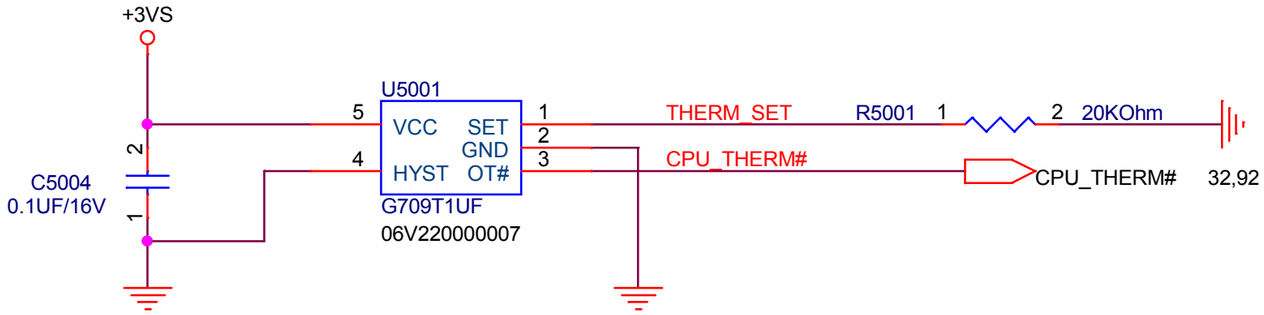
<Title> Engineer:

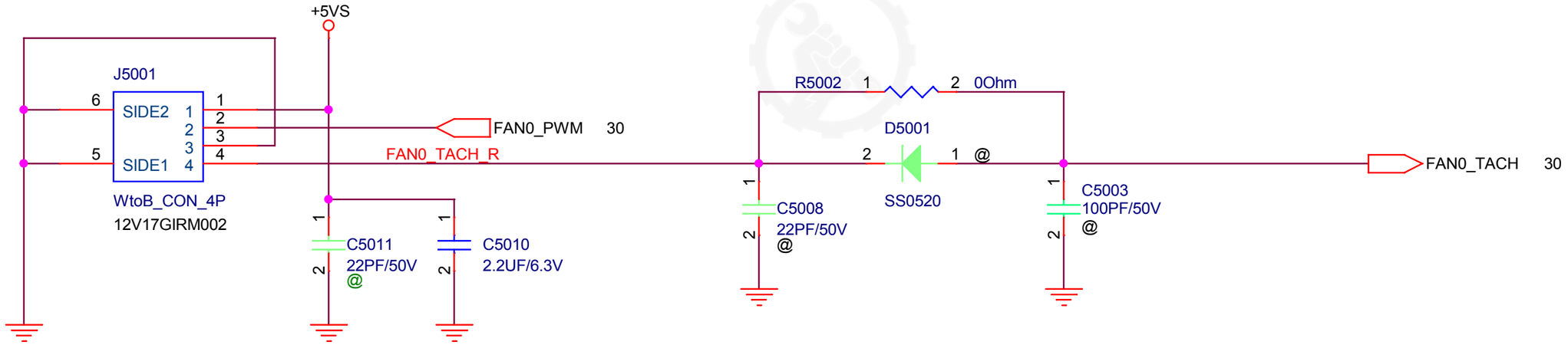
Size	Project Name	Rev
C	KTKUG_25W	1.1

Date: Tuesday, September 06, 2016 Sheet 49 of 108

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,51,53,57,61,62,67,91,92

+5VS +5VS 31,36,45,46,48,51,56,57,67,80,91





PEGATRON Title THERMAL/ FAN

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: *Bill Yang*

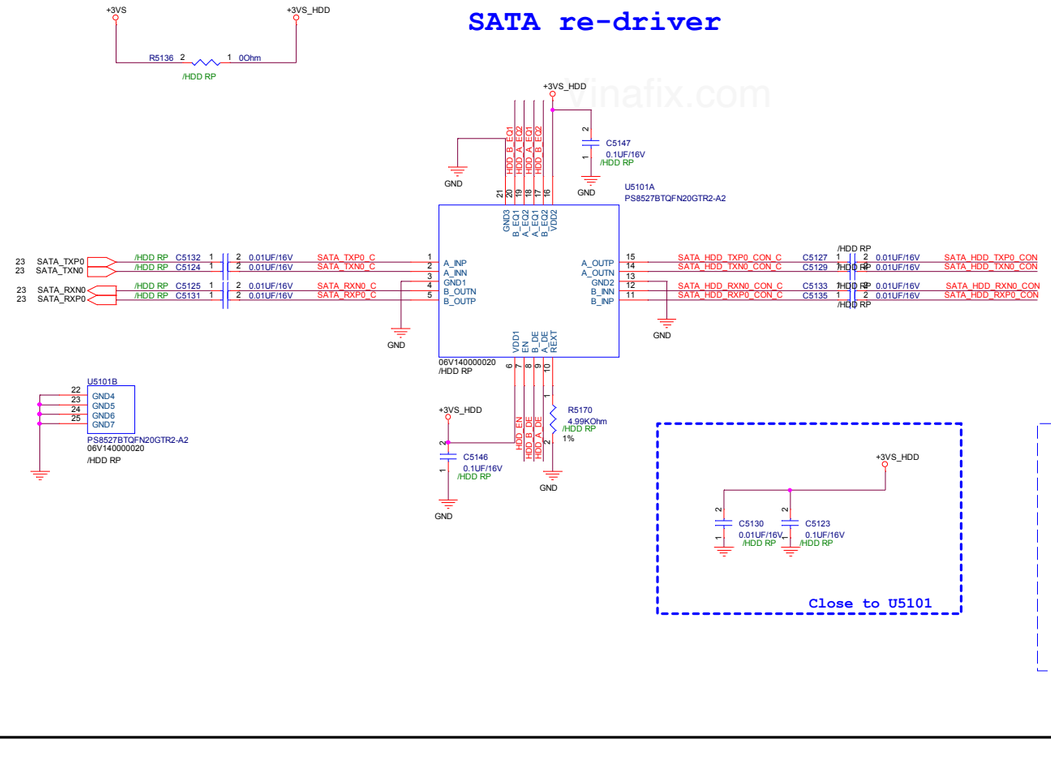
BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 50 of 108

HDD

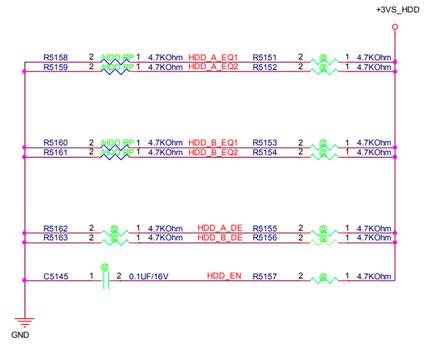
SATA re-driver



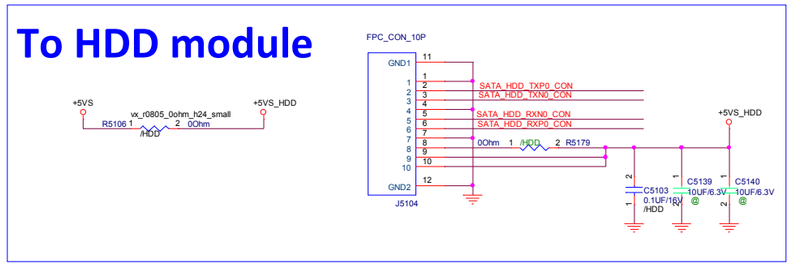
Close to U5101

Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/M: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/M: for channel loss up to 12.2dB (Default)
M/L: for channel loss up to 9.4dB
M/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

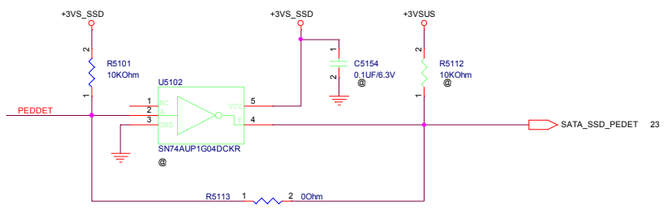
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB (Default)
L: 0dB
H: -6dB



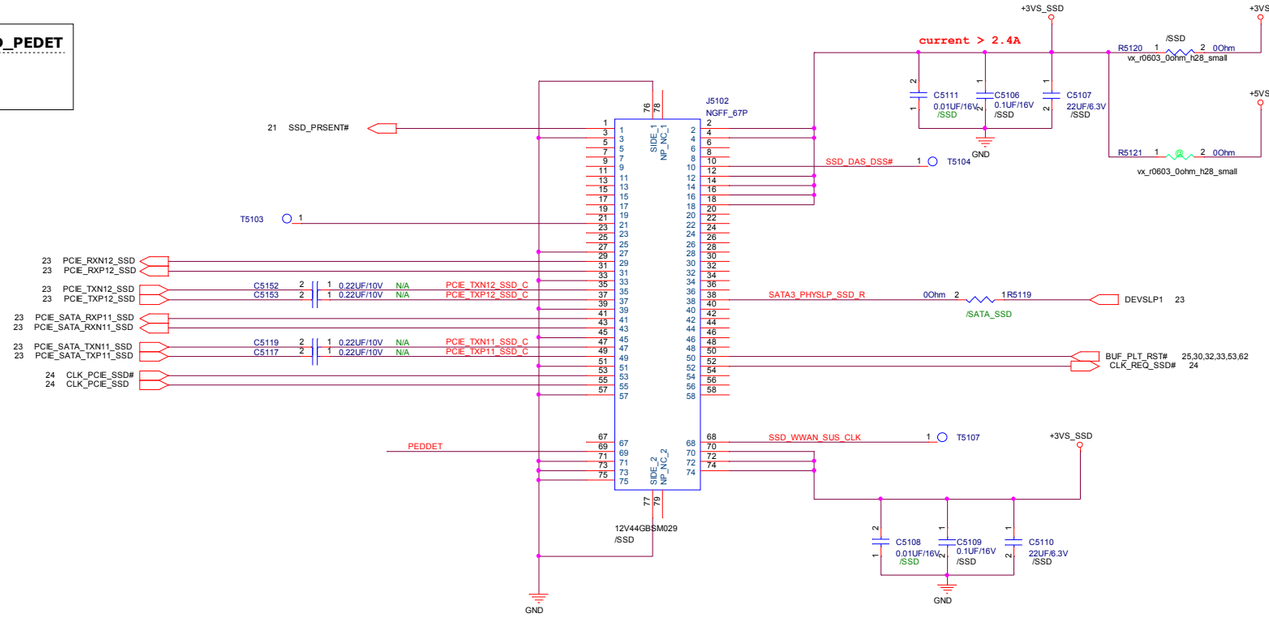
To HDD module



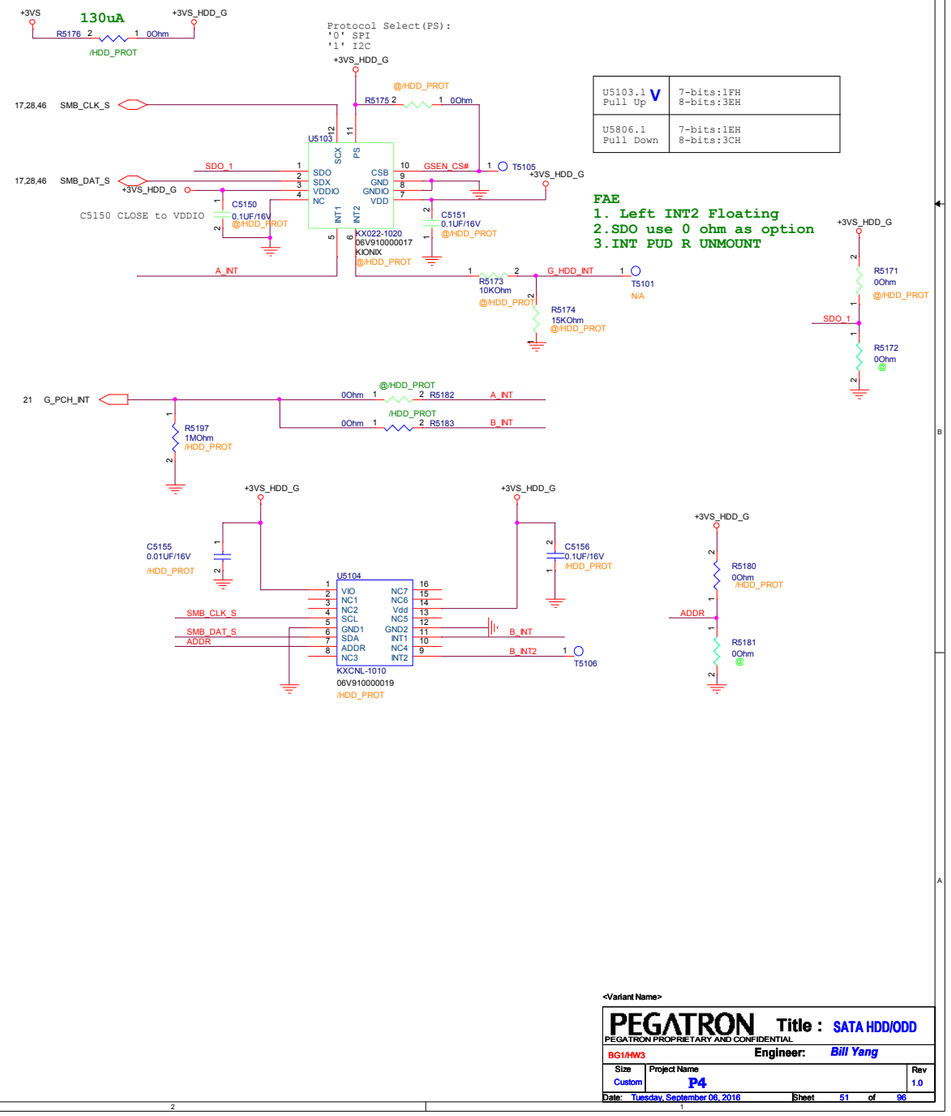
SSD(SATA/PCIE x2) NGFF socket (M-key)



SATA_SSD_PEDET
0: SATA
1: PCIE



HDD G-Sensor



U5103.1 V Pull Up	7-bits:1FH 8-bits:3EH
U5806.1 Pull Down	7-bits:1EH 8-bits:3CH

FAE
1. Left INT2 Floating
2.SDO use 0 ohm as option
3.INT PUD R UNMOUNT

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SATA HDD/ODD

BG1/MW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 51 of 96

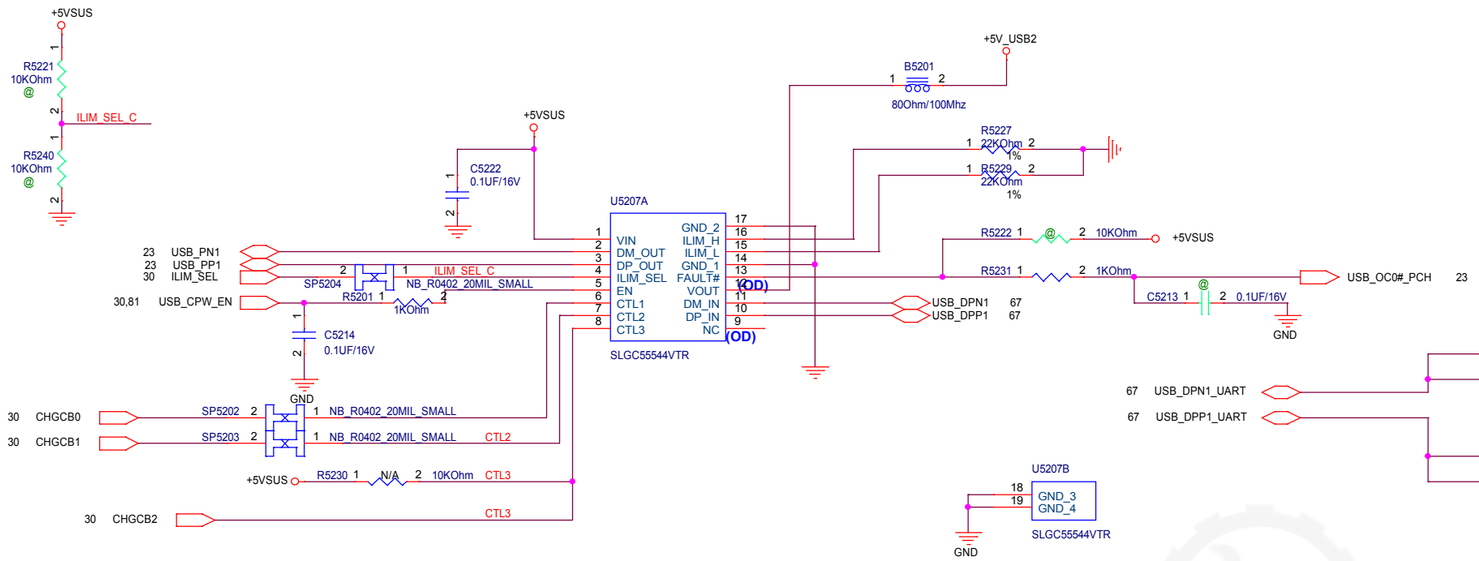
USB 3.0 ports x 1 with Sleep & Charge Left_Down

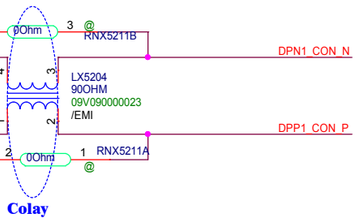
TPS2544 Device True Table

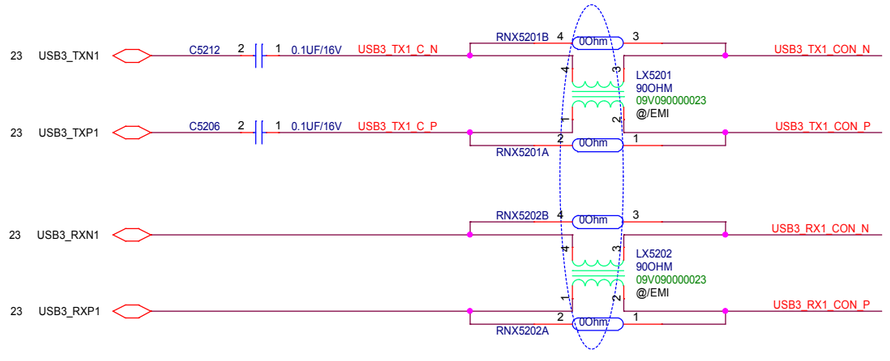
+5VSUS → +5VSUS 41,42,56,67,81

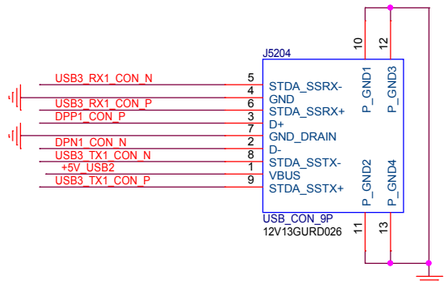
+3VSUS → +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92

22k is to set current limit at 2.2A in DCP and CDP
47k is to set current limit at 1A in SDP

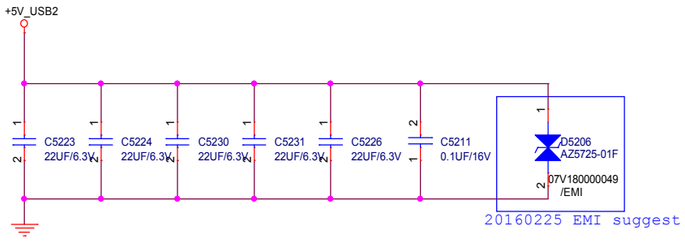




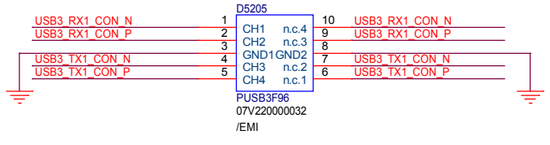


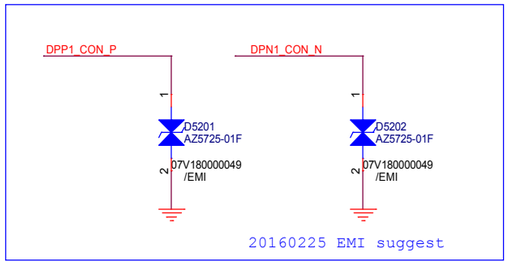


System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



PLACE ESD Diodes near USB Connector



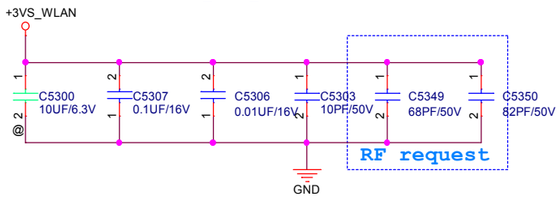


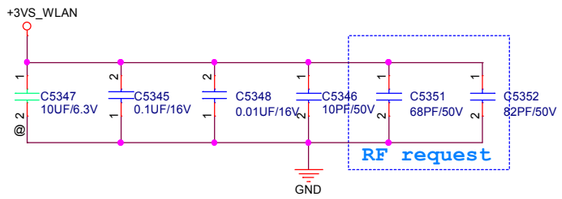
PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : USB JACK		
BG1/HW3	Engineer: Bill Yang		
Size: Custom	Project Name: P4		Rev: 1.0
Date: Tuesday, September 06, 2016	Sheet 52 of 108		

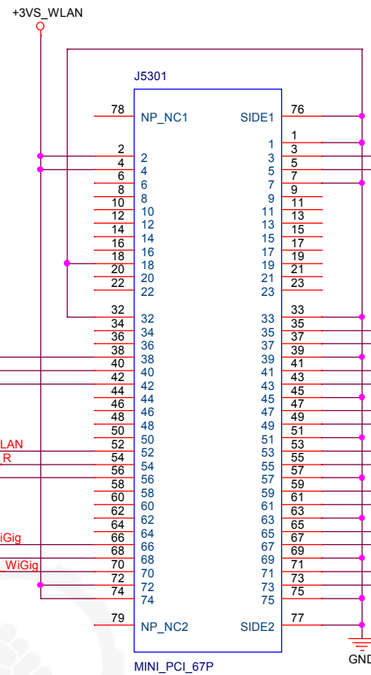
WLAN/ WiGig / BT

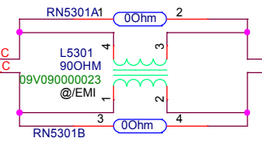
+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 2,4
Place 10UF near +3V_WLAN_WP1 source side.

+3V_WLAN_WP1 bypass capactor:
Place 0.1UF near pin 72,74.
Place 10UF near +3V_WLAN_WP1 source side.

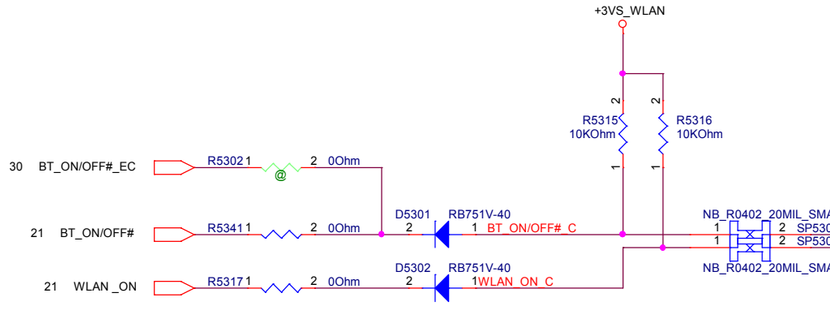


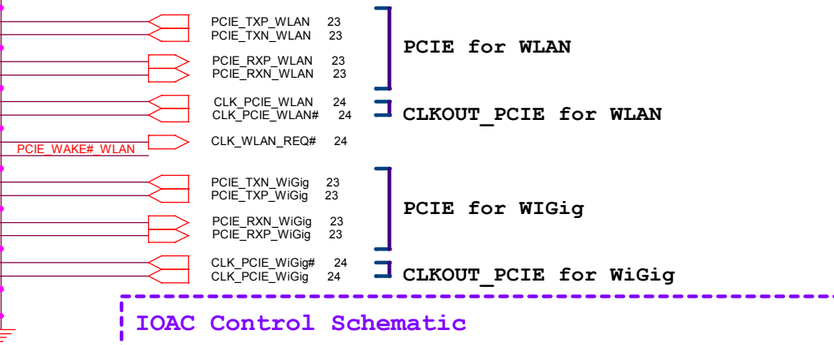






USB2.0 for BT



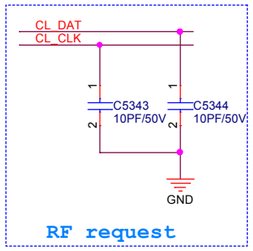


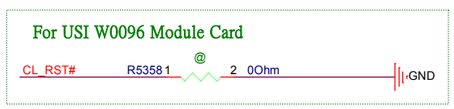
PCIE for WLAN

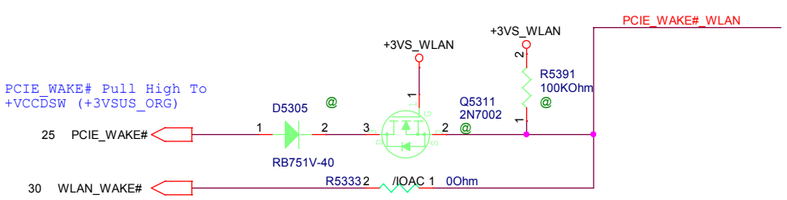
CLKOUT_PCIE for WLAN

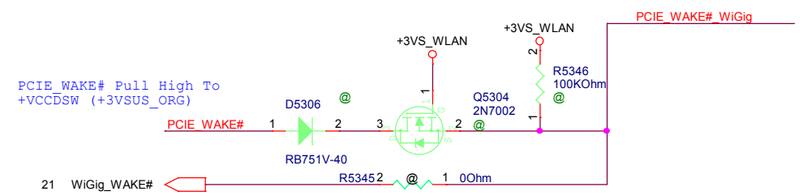
PCIE for WIGig

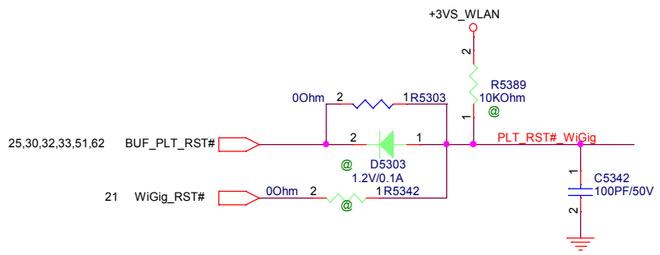
CLKOUT_PCIE for WiGig

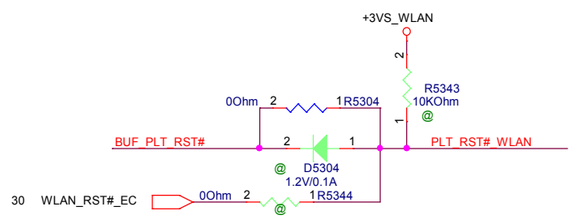


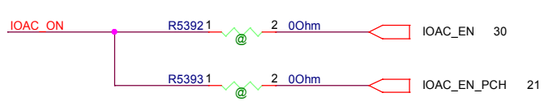






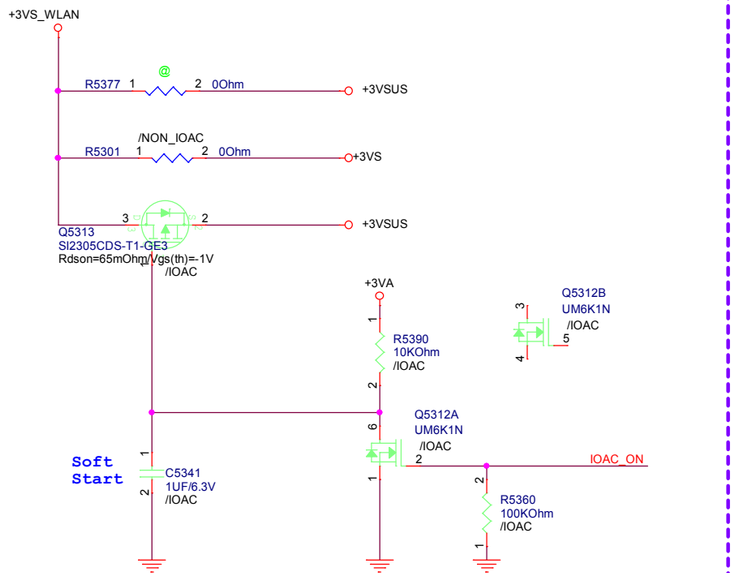






IOAC Control Schematic

500mA



<Variant Name>

PEGATRON Title : WLAN/ WiGig / BT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW4 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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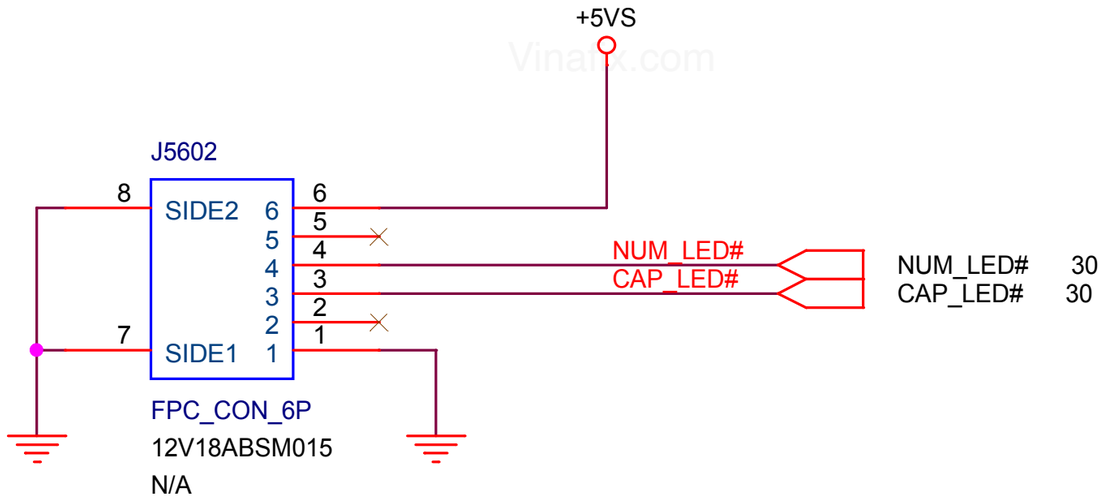
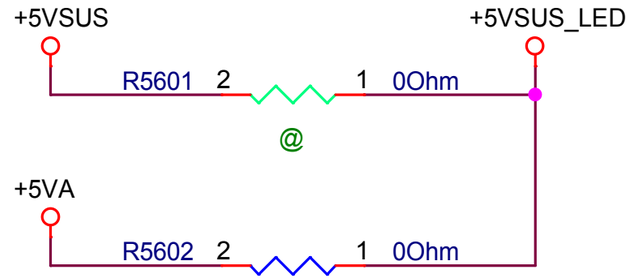
Title	<Title>
Size: A	Document Number: KTKUG_25W
Rev: 1.1	
Date: Tuesday, September 06, 2016	Sheet 55 of 108

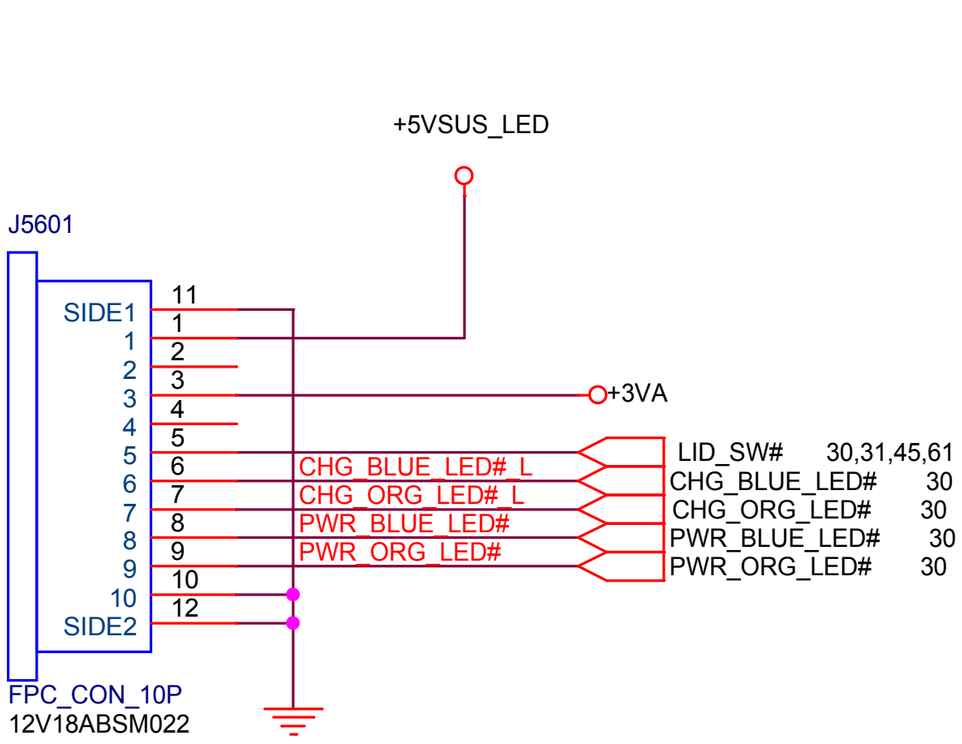
+5VS +5VS 31,36,45,46,48,50,51,57,67,80,91

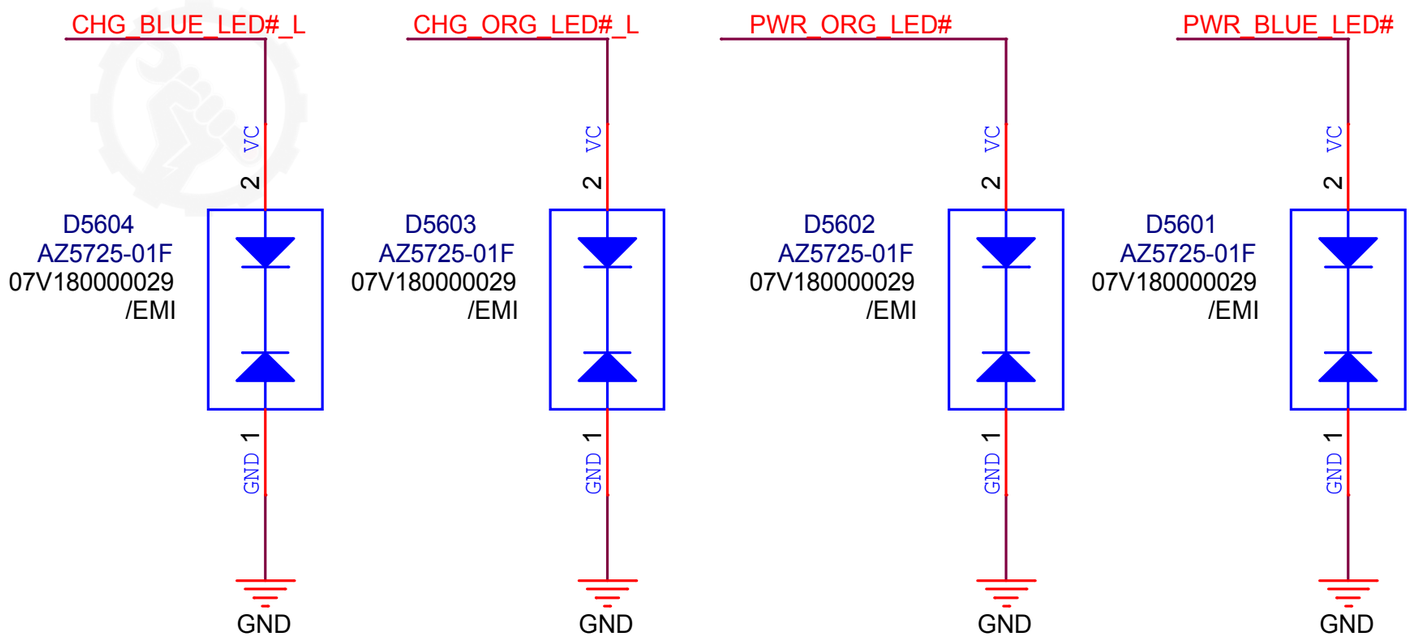
+5VSUS +5VSUS 41,42,52,67,81

+3VA +3VA 24,30,31,36,41,43,53,57,67,81,88,93









PEGATRON Title : LED

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.0

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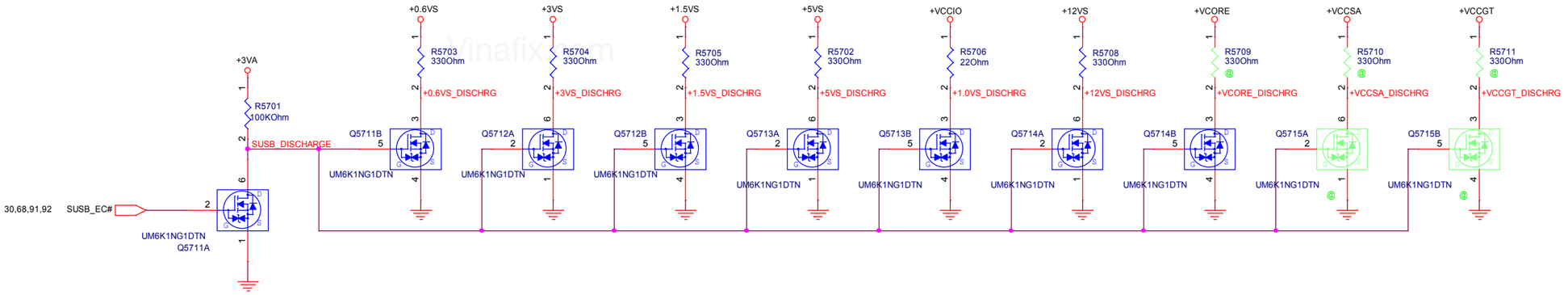

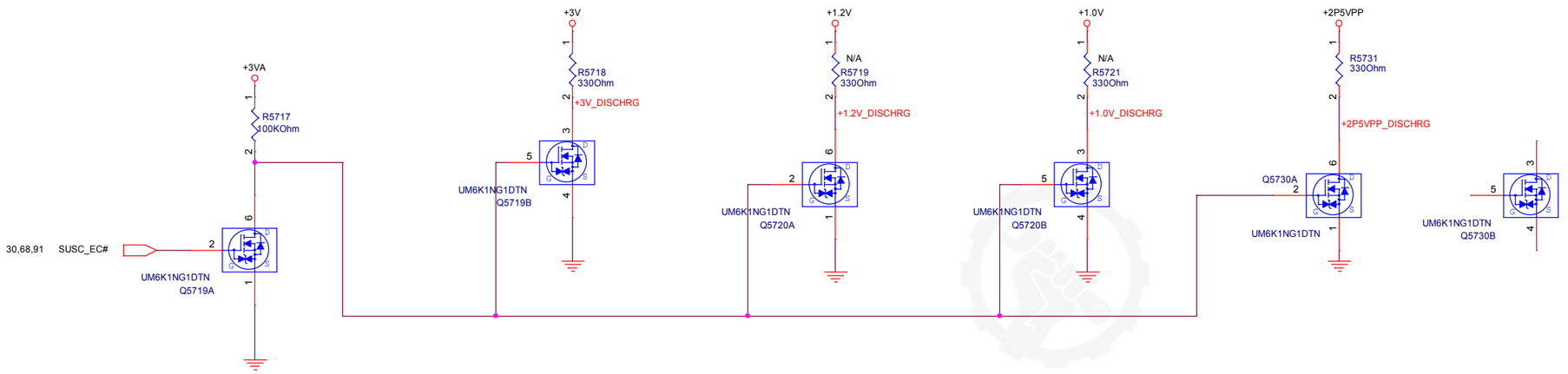

+3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,61,62,67,91,92
+3VA 24,30,31,36,41,43,53,56,67,81,88,93
+0.6VS 15,17,83
+1.5VS 36,85
+5VS 31,36,45,46,48,50,51,56,67,80,91
+VCCIO 3,7,91
+12VS 28,31,62,91
+VCORE 5,80
+VCCSA 7,80
+VCCGT 6,80
+3V 25,31,44,67,82,91
+1.2V 4,7,15,16,17,18,83
+1.0V 7,91
+2P5VPP 16,17,82

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :DSG_Discharge

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 57 of 108

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	Rev
C	KTKUG_25W	1.1

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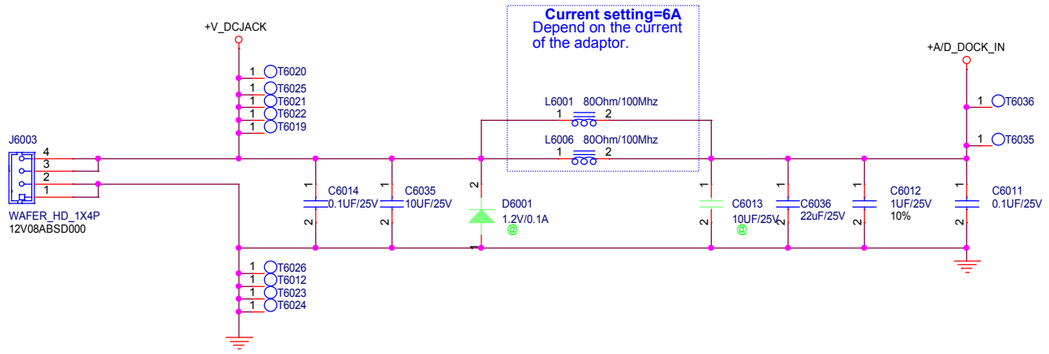
60

DC_BAT_CONN

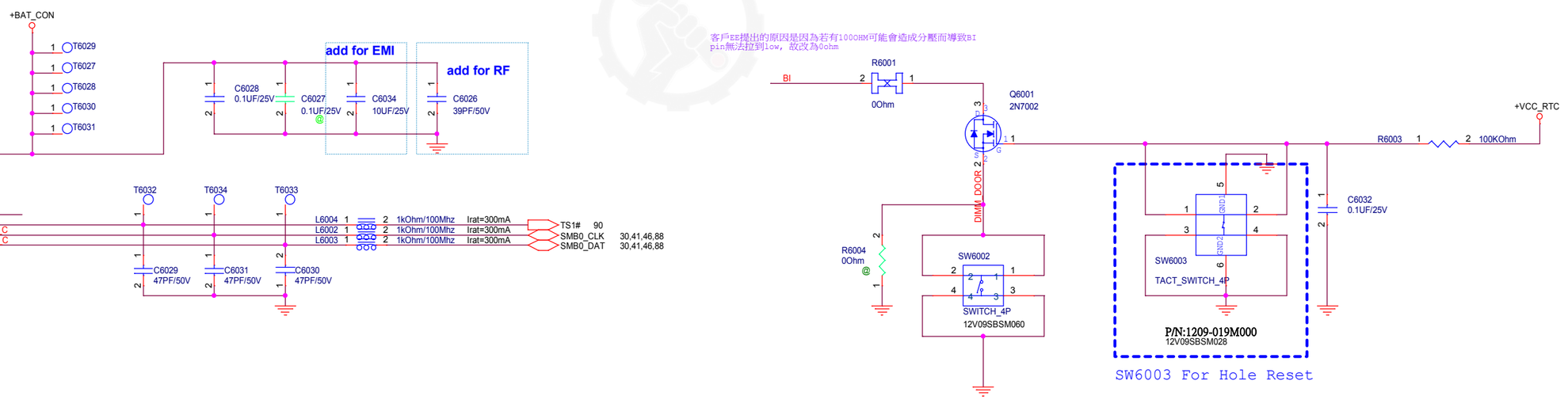
DC Jack WTB CONN



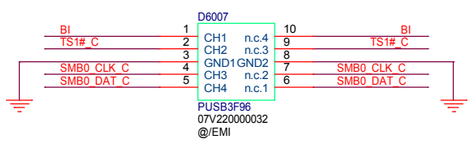
+VCC_RTC — +VCC_RTC 24,25,26,36
+3VA_EC — +3VA_EC 28,30,32
+3VA — +3VA 24,30,31,36,41,43,53,56,57,67,81,88,93
+5VA — +5VA 31,56,81
+1.0VSUS — +1.0VSUS 26,82
+1.8VSUS — +1.8VSUS 9,21,24,26,84
+3VSUS — +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+5VSUS — +5VSUS 41,42,52,56,67,81
+12VSUS — +12VSUS 81,91
+3V — +3V 25,31,44,57,67,82,91
+12V — +12V 91

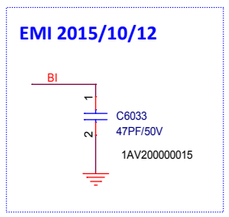
+3VS — +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+5VS — +5VS 31,36,45,46,48,50,51,56,57,67,80,91
+12VS — +12VS 28,31,57,62,91
+AC_BAT_SYS — +AC_BAT_SYS 43,45,80,81,82,83,88
+A/D_DOCK_IN — +A/D_DOCK_IN 89
+BAT_CON — +BAT_CON 88
+VCORE — +VCORE 5,57,80
+VCCGT — +VCCGT 6,57,80
+VCCSA — +VCCSA 7,57,80
+VCCIO — +VCCIO 3,7,57,91
+RTCBAT — +RTCBAT 24

Battery Connector



客戶EE提出的原因是因為若有100OHM可能會造成分壓而導致BI pin無法拉到low，故改為0ohm





PEGATRON Title : DC_BAT_CONN
BG1-HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 60 of 108

+5VS — +5VS 31,36,45,46,48,50,51,56,57,67,80,91

+3VS — +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,62,67,91,92

+3VS

R6101
10KOhm
@/TPANEL

30,31,45,56 LID_SW# — 2 — 1 D6101 RB751V-40 /TPANEL — 2 — TP_LID_SW# — TP_LID_SW# 45

<Variant Name>

PEGATRON Title : Touch Panel Conn

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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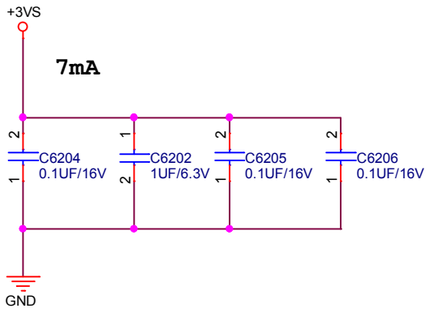
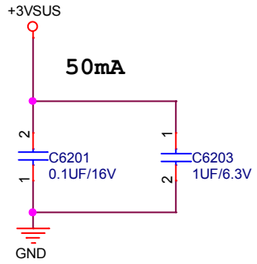
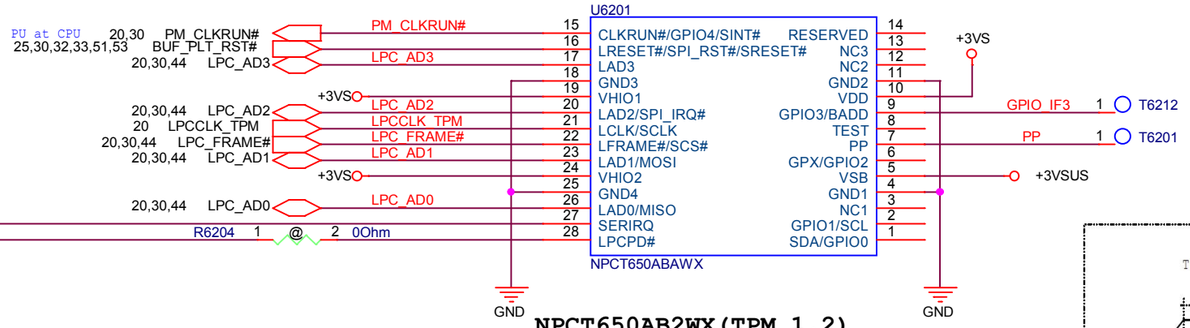
TPM

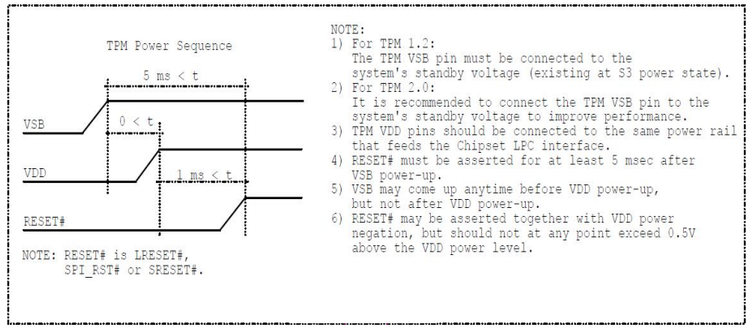




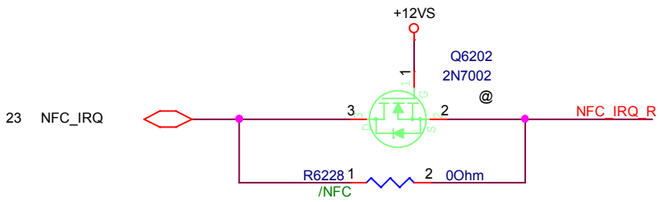
Slave address is for I2C interface,
and is selected by BADD

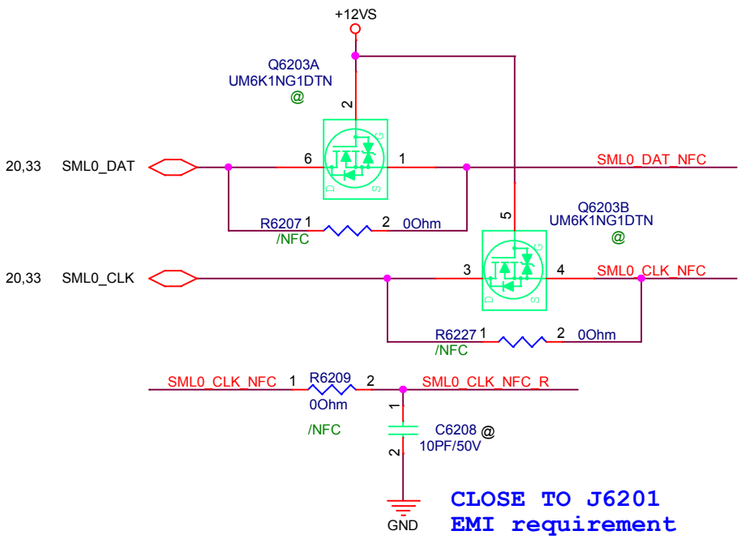


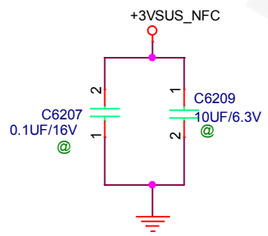
NPCT650AB2WX(TPM 1.2)
NPCT650ABAWX(TPM 2.0)

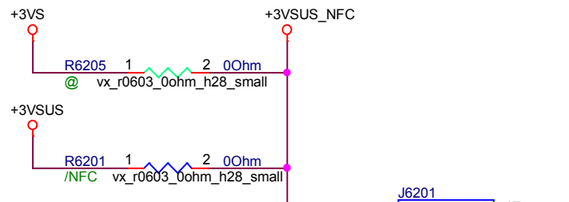


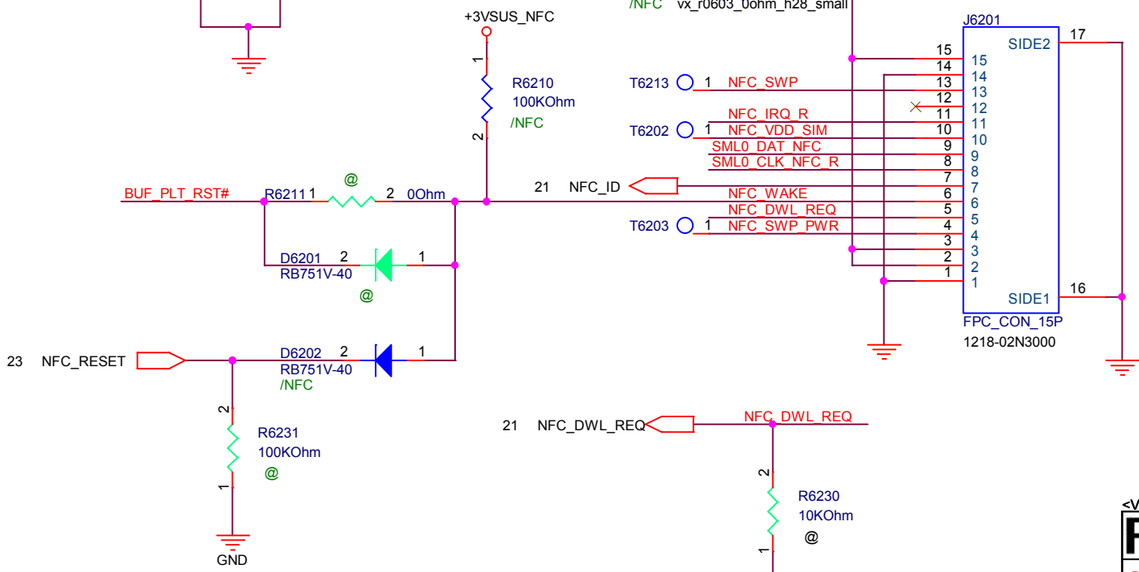
NFC

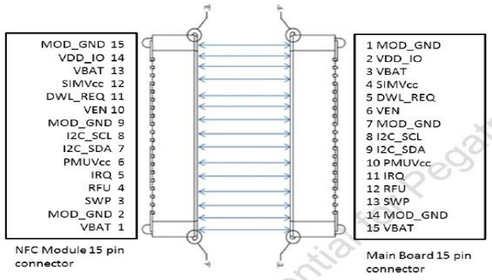












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PEGATRON Title : TPM CONN

BG1/HW3 Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

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Title	<Title>
Size: A	Document Number: KTKUG_25W
Rev: 1.1	
Date: Tuesday, September 06, 2016	Sheet 63 of 108

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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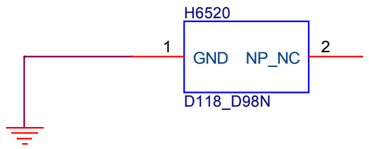
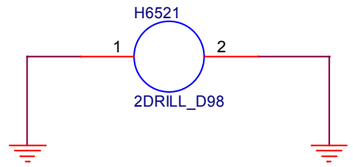
A



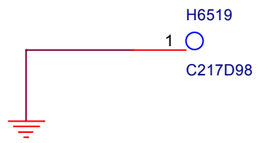
B

C



E

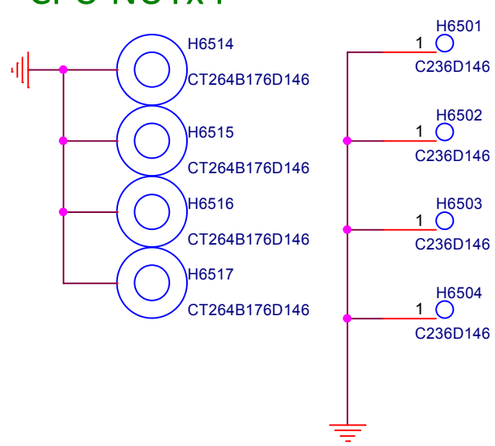
F

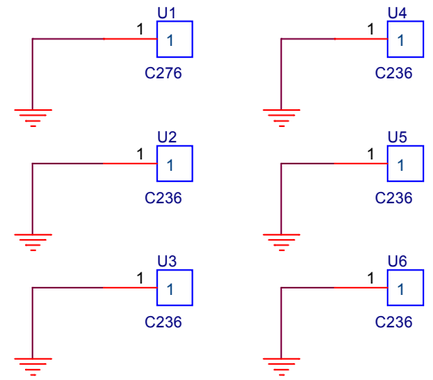


BGA

CPU NUTx4

D





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PEGATRON

Title: ME_CONN,Skew Hole

Engineer: *Bill Yang*

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 65 of 108

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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+5VSUS — +5VSUS 41,42,52,56,81

+3V — +3V 25,31,44,57,82,91

+3VS — +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,91,92

+3VS

R6708 49.9KOhm 1% vx_r0402_small /UART

R6707 49.9KOhm 1% vx_r0402_small /UART

21 UART_RX

21 UART_TX

/NON_UART

2 0Ohm 1 R6709 USB_PN1_N

2 0Ohm 1 R6710 USB_PP1_N

0Ohm /NON_UART /UART

52 USB_DPN1

52 USB_DPP1

2 0Ohm 1 R6703 USB_PN1_U

2 0Ohm 1 R6704 USB_PP1_U

0Ohm /UART

Pin 2 Colay

U6702

HSD2- HSD2+ HSD1+ HSD1- GND OE# VCC S D- D+

USB_PN1_C

USB_PP1_C

1 0Ohm 2 R6711

1 0Ohm 2 R6712

0Ohm /NON_UART /UART

1 0Ohm 2 R6705

1 0Ohm 2 R6706

0Ohm /UART

/NON_UART

Pin 2 Colay

USB_DPN1_UART 52

USB_DPP1_UART 52

+3VA

C6704 0.1UF/16V /UART

+3VA

+3VSUS

R6715 10KOhm /UART

21 USB_UART_SEL

/UART

2N7002

Q6777

NX3DV42GU

06V150000026

/UART

20150417

For layout limitation

23 USB_PN2

23 USB_PP2

2 0Ohm 1 RNX6709A @

/EMI 09V090000023 90OHM LX6706

RNX6709B @ 4 0Ohm 3

DPN2_CON_N

DPP2_CON_P

23 USB_PN8

23 USB_PP8

2 0Ohm 1 RNX6708A @

/EMI 09V090000023 90OHM LX6708

RNX6708B 4 0Ohm 3 @

DPN8_CON_N

DPP8_CON_P

SD

Swaybay Hub

J6701

DPP8_CON_P

DPN8_CON_N

DPP2_CON_P

DPN2_CON_N

23 USB_OC1#_PCH

30 USBP01_EN

USB_OC1#_PCH

USBP01_EN

+3VS

+3V

+5VSUS

+5VSUS

+5VS

10 SIDE1

21 SIDE2

31

32

FPC_CON_30P

12V18ABSM028

/W SB

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

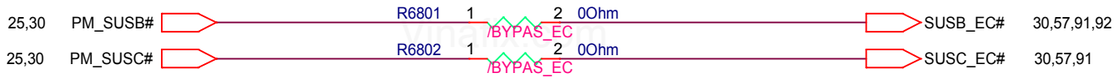
Title : MLB to IO

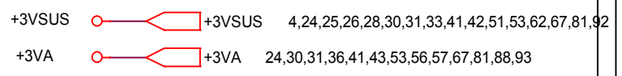
Engineer: Bill Yang

BG1/HW3

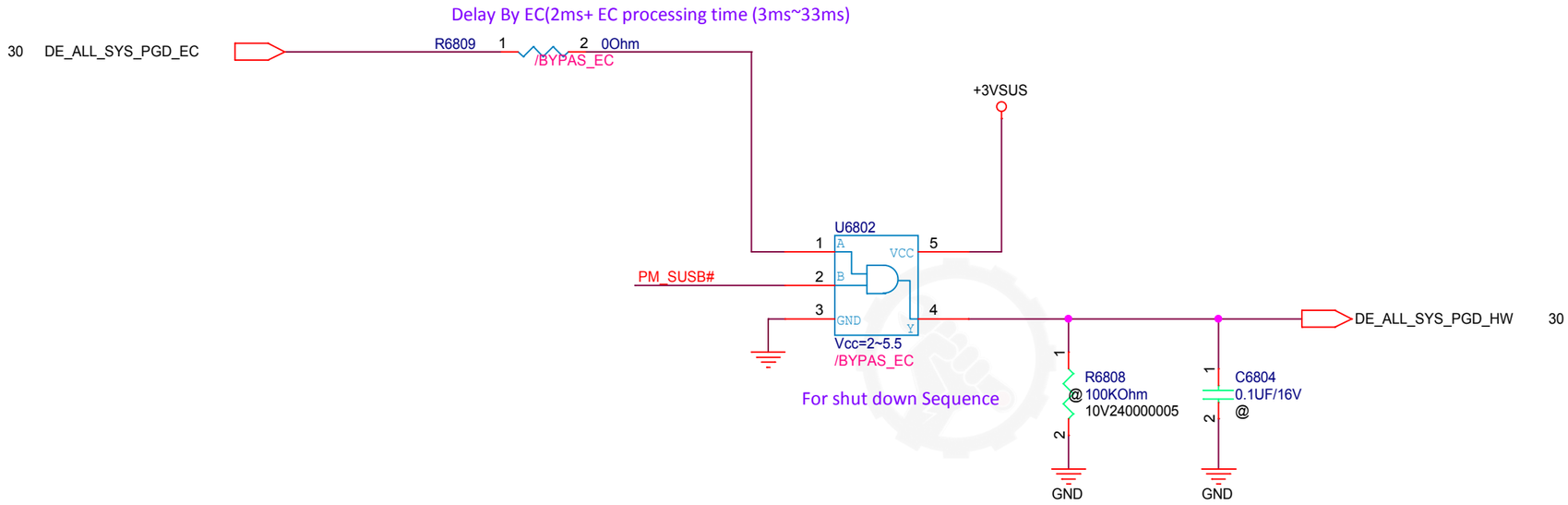
Size Custom | Project Name P4 | Rev 1.0

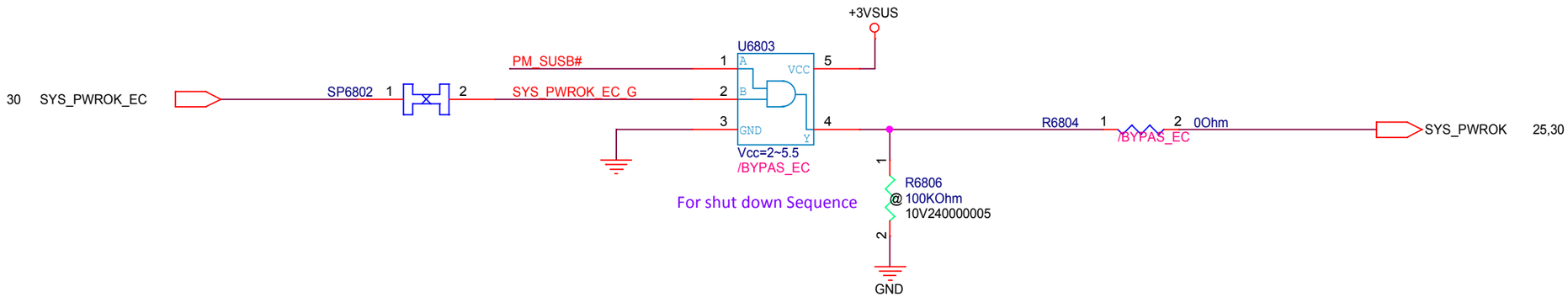
Date: Tuesday, September 06, 2016 | Sheet 67 of 108





For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms





<Variant Name>

PEGATRON

Title : BYPASS EC SEQUENCE

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 68 of 108

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
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PEGATRON Title : GPU(1)

PEGATRON PROPRIETARY AND CONFIDENTIAL

BSMMS

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 70 of 108

PEGATRON

Title : GPU(1)

BSTHW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 71 of 108

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : GPU(1)

BSTHW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 72 of 108

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : GPU(1)

BSTHW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 73 of 108

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG nHW3

Title : GPU(1)

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 74 of 108

PEGATRON Title : GPU(1)

BSTHW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0

Date: Tuesday, September 06, 2016 Sheet 75 of 108

PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : GPU-MEM CHA		
BSTMWS Engineer: Raly Hsieh		
Size: Custom	Project Name: KTKUG_25W	Rev: 2.0
Date: Tuesday, September 06, 2016	Sheet 76 of 108	

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, September 06, 2016
Sheet	77 of 108

PEGATRON Title : ****

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: *Raly Hsieh*

Size	Project Name	Rev
A	KTKUG_25W	1.0

Date: Tuesday, September 06, 2016 Sheet 78 of 99

PEGATRON Title : ****

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: *Raly Hsieh*

Size	Project Name	Rev
A	KTKUG_25W	1.0

Date: Tuesday, September 06, 2016 Sheet 79 of 99

VCORE & VCCGT & VCCSA POWER SUPPLY

VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 29A
PL2 TDC=21A
LL=2.4mV/A
OCP=43.5A

VCCGT
VID1 : 0.9V
Vboot : 0V
Iccmax = 31A
PL2 TDC =18A
LL=3.1mV/A
OCP=46.5A

VCCSA
VID1 : 0.9V
VBoot : 1.05V
Iccmax = 4.5A
PL2 TDC = 4A
LL=10.3mV/A
OCP=6.75A

Iin=3.25A
Iin=2.6A
Iin=0.9A
Iccmax=6A

U8002A SIC631CD-T1-GE3
U8003A SIC631CD-T1-GE3
U8000A ISL95859HRTZ
U8000B ISL95859HRTZ
U8002B SIC631CD-T1-GE3
U8003B SIC631CD-T1-GE3
U8005 ISL95808HRZ

The R8042 closes to L8001 for VCCGT
The R8043 closes to L8002 for VCCSA
The R8041 closes to L8000 for Vcore

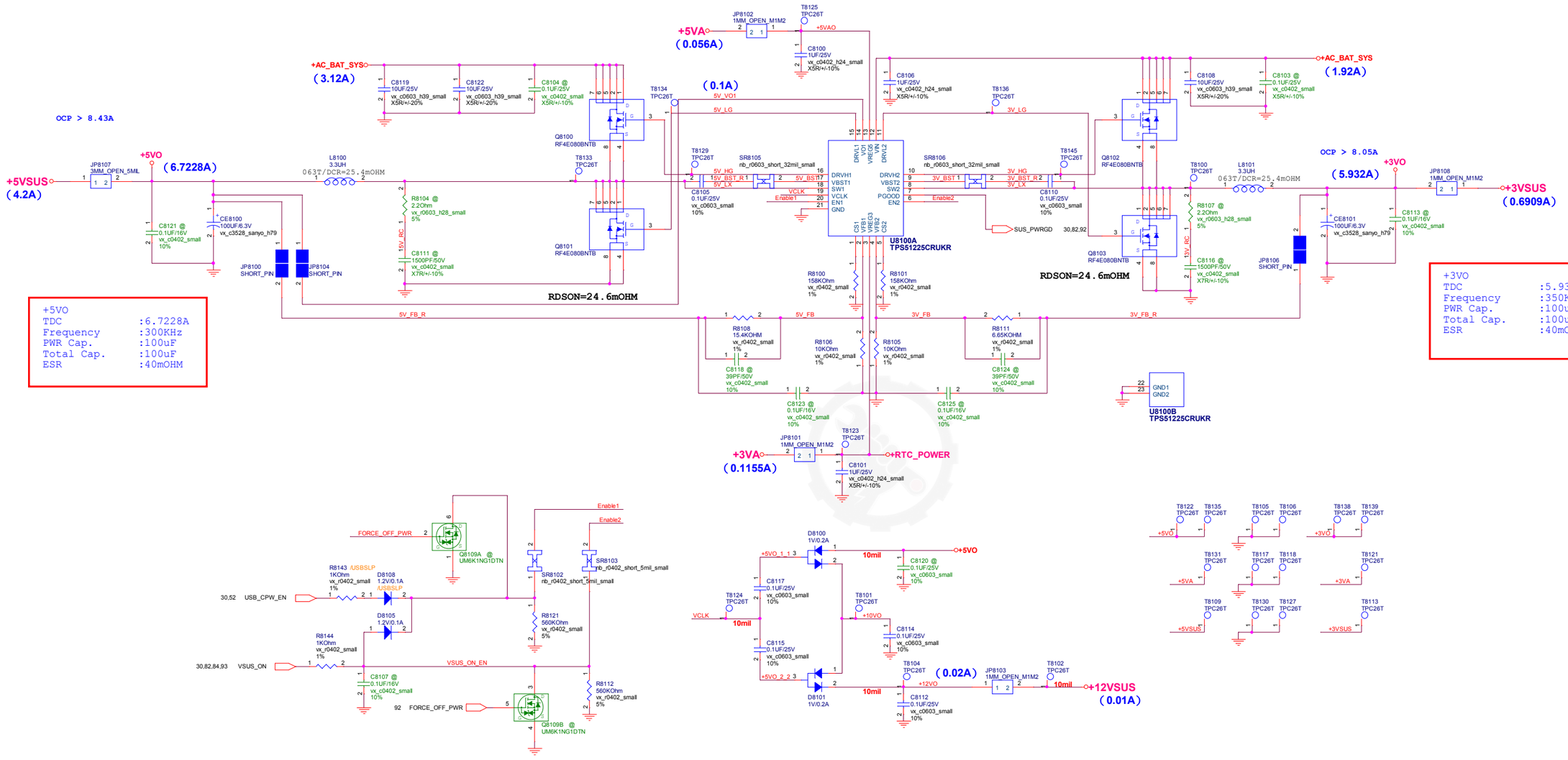
EE side : 10uF * 6

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_VCORE
Engineer: Adams Lin
Size: Custom | Project Name: P4 | Rev: 2.1
Date: Tuesday, September 06, 2016 | Sheet 80 of 94

5VO & 3VO POWER SUPPLY



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SYSTEM

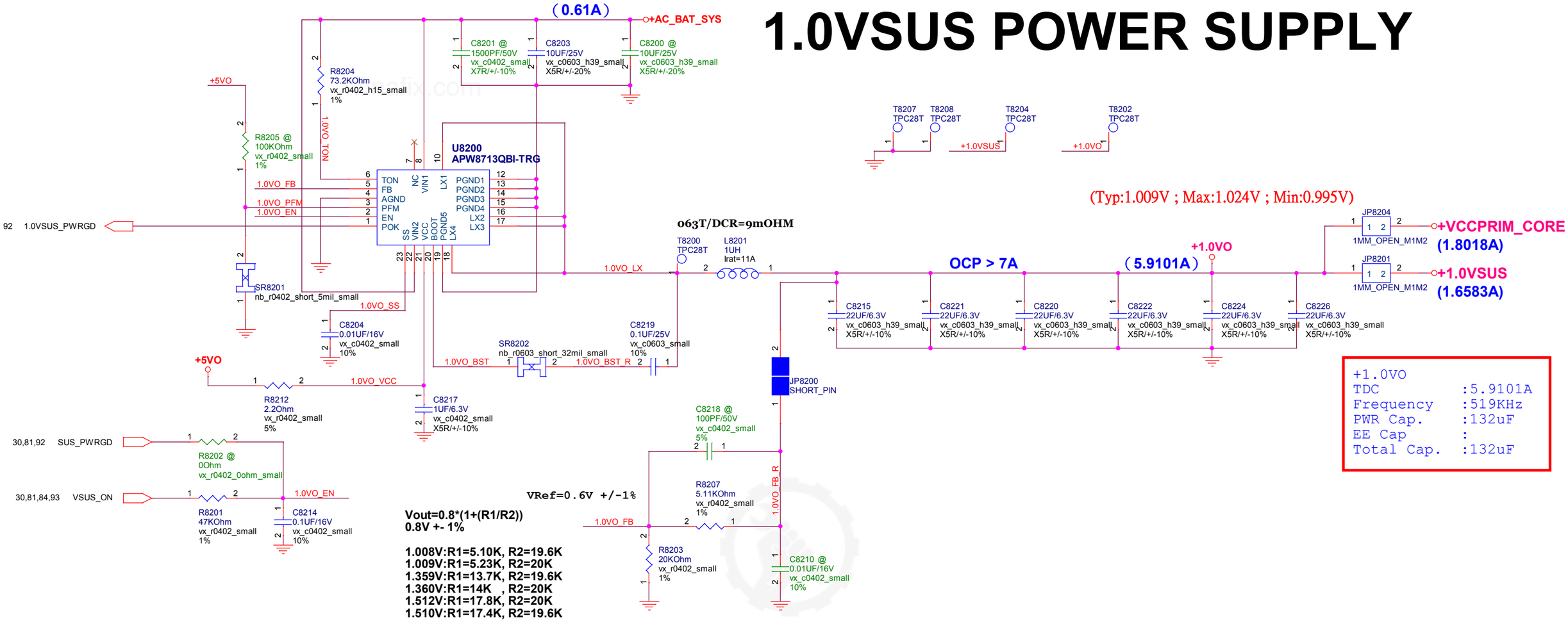
Engineer: Adams Lin

BGI-POWER

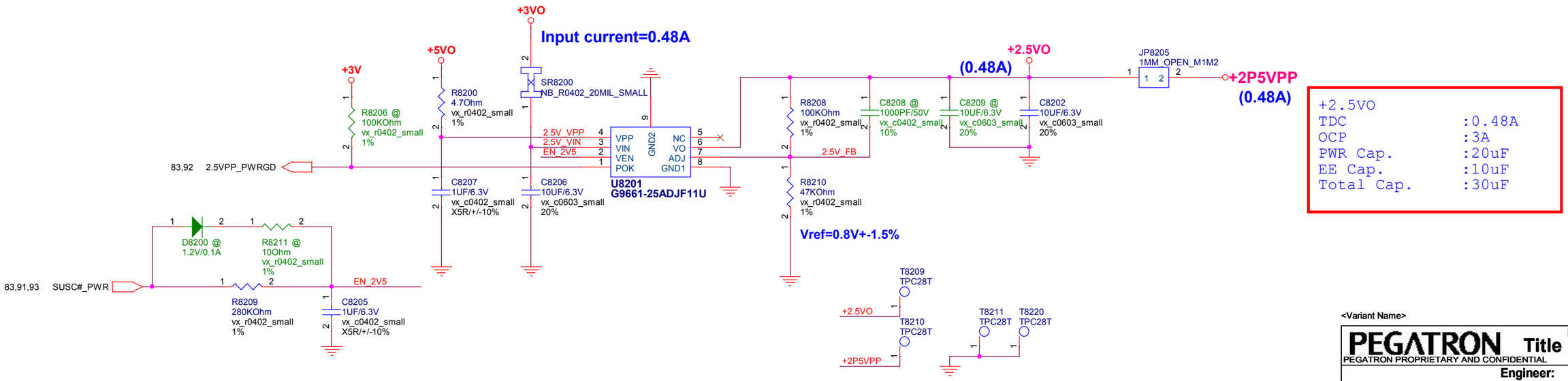
Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 81 of 94

1.0VSUS POWER SUPPLY



2.5V POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

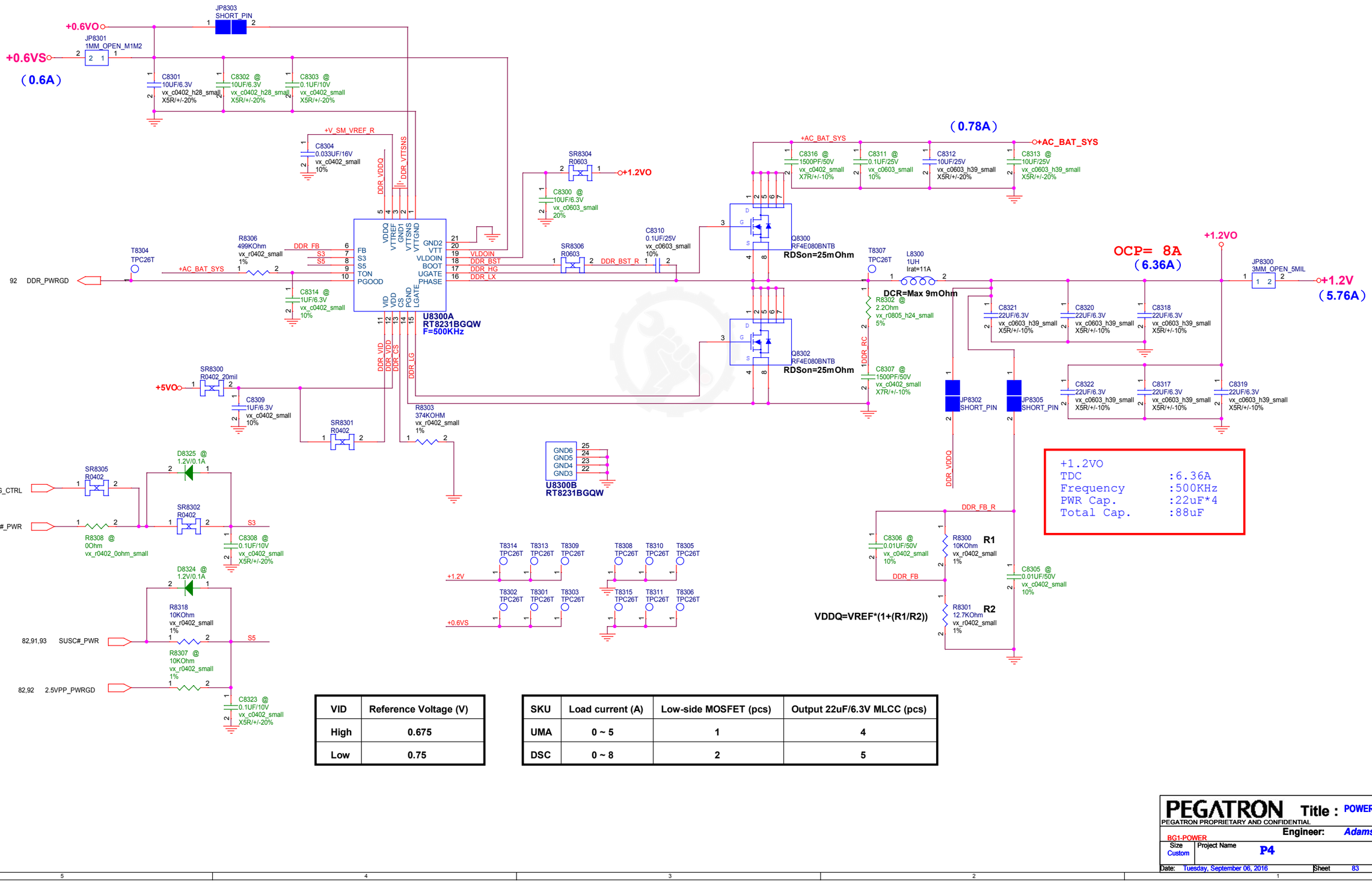
Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 82 of 94

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON Title : POWER_DDR & VTT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

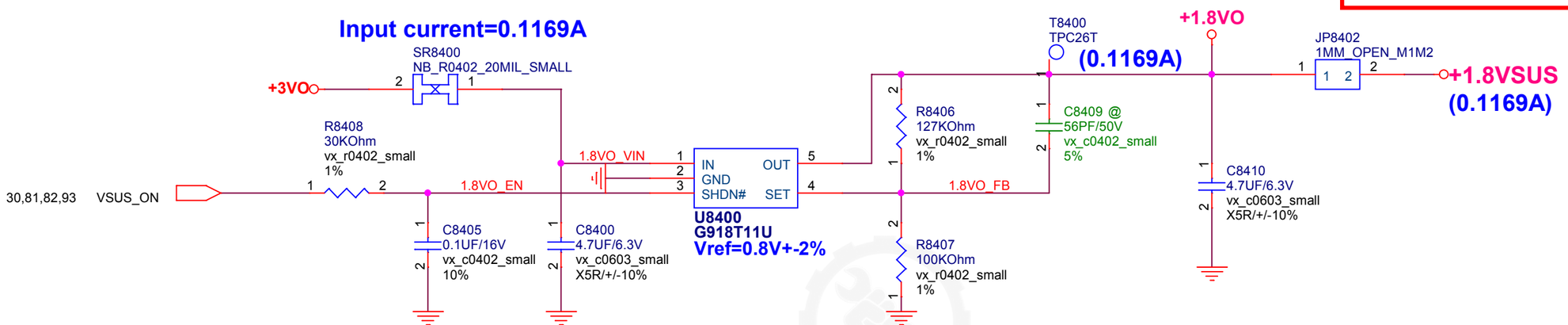
BG1-POWER

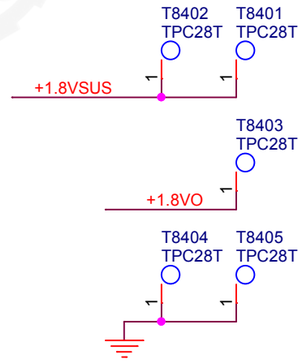
Size: Custom | Project Name: P4 | Rev: 2.1

Date: Tuesday, September 06, 2016 | Sheet 83 of 94

1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF





<Variant Name>

PEGATRON Title : POWER_+1.8VSUS

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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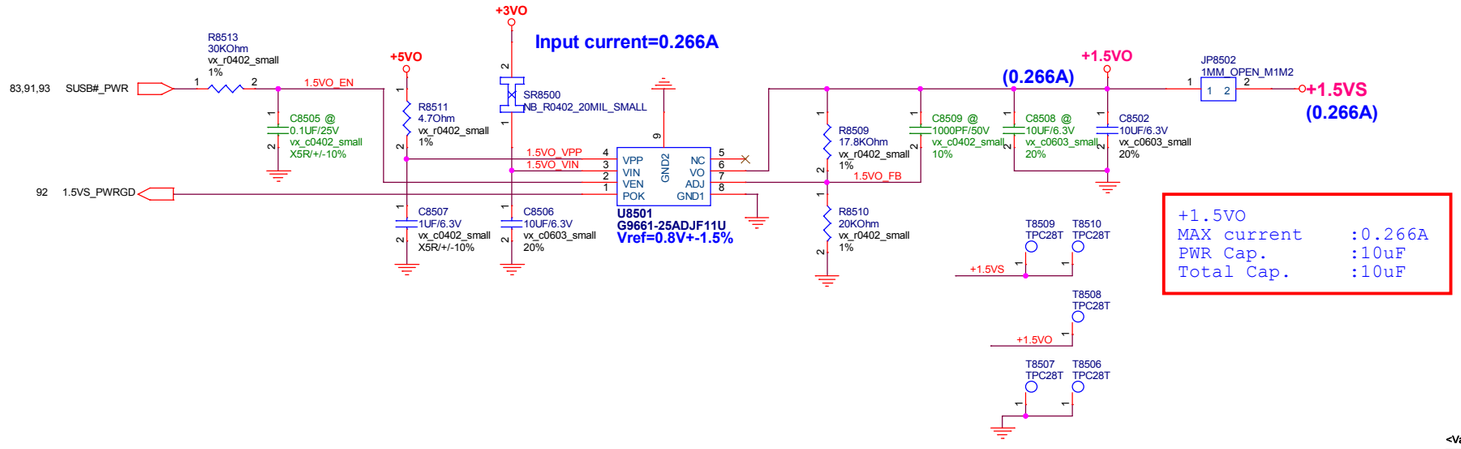
1.5VS POWER SUPPLY



+1.5VO
MAX current :0.266A
PWR Cap. :10uF
Total Cap. :10uF

<Variant Name>

PEGATRON Title : POWER_+1.5VS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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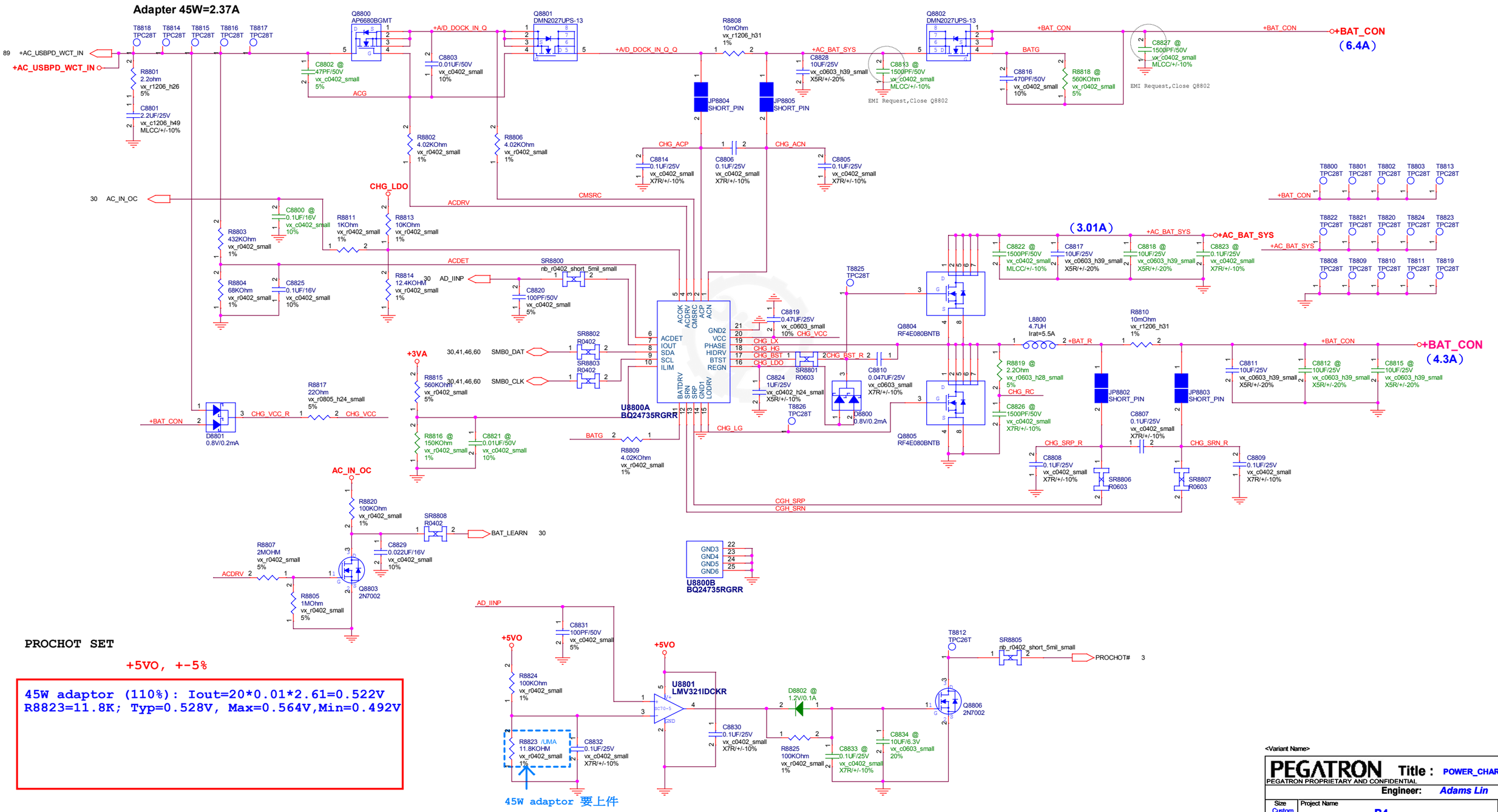
BATTERY CHARGER



PROCHOT SET

+5VO, +-5%

45W adaptor (110%): Iout=20*0.01*2.61=0.522V
R8823=11.8K; Typ=0.528V, Max=0.564V,Min=0.492V

<Variant Name>

PEGATRON Title : POWER_CHARGER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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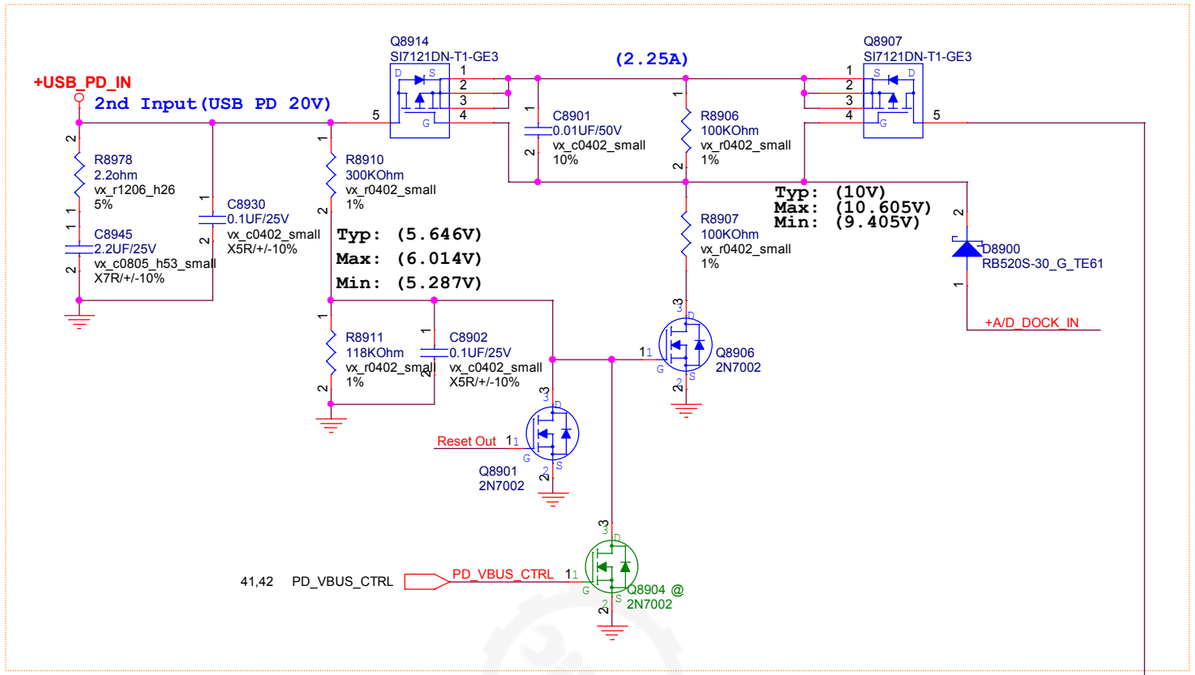
2 Input switch Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

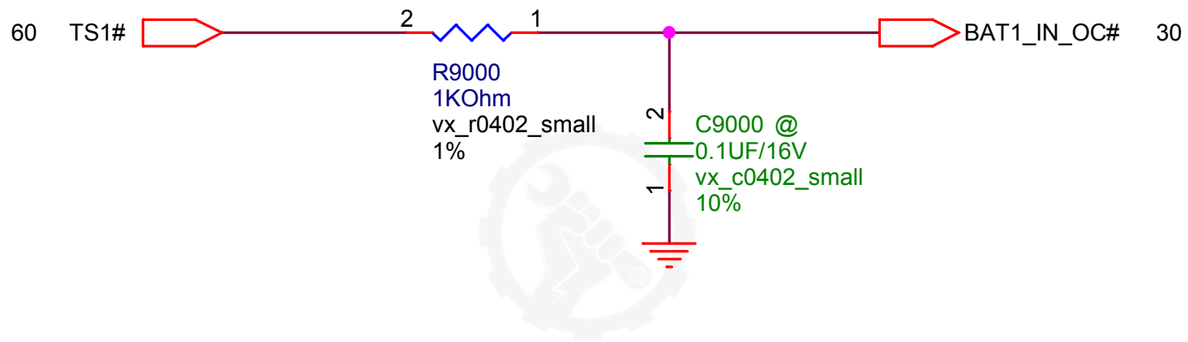
Title : AC&PD S.W.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016 Sheet 89 of 94

BATTERY IN DETECT



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DETECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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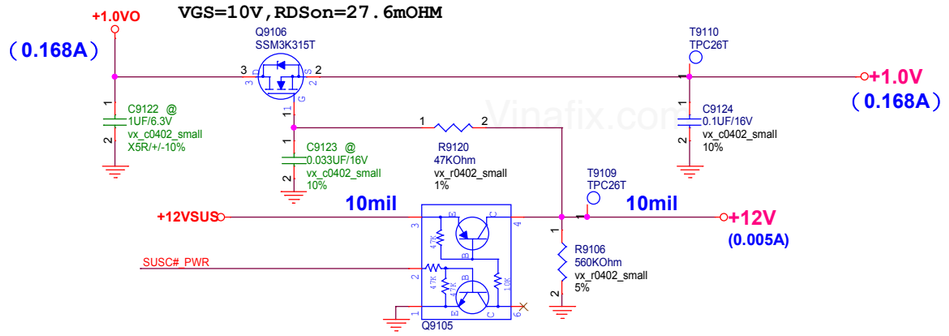
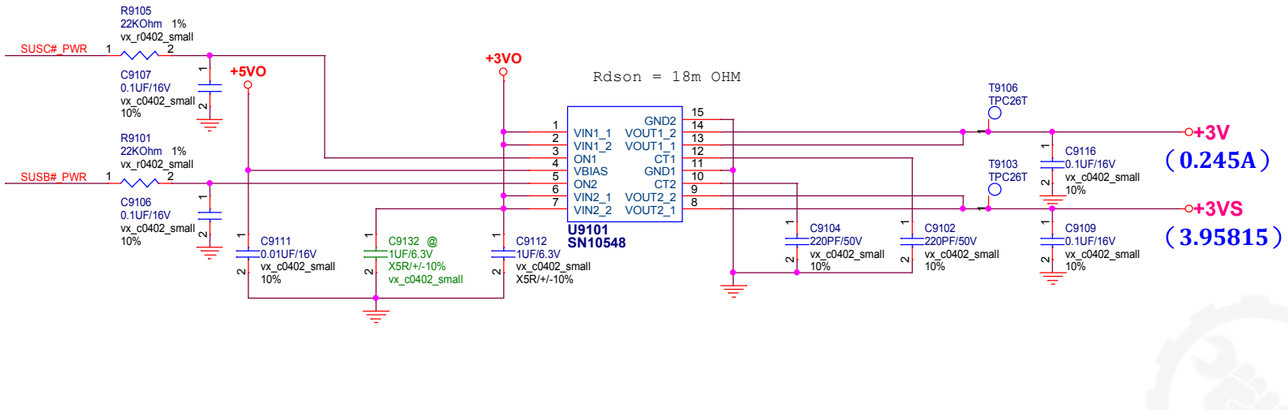
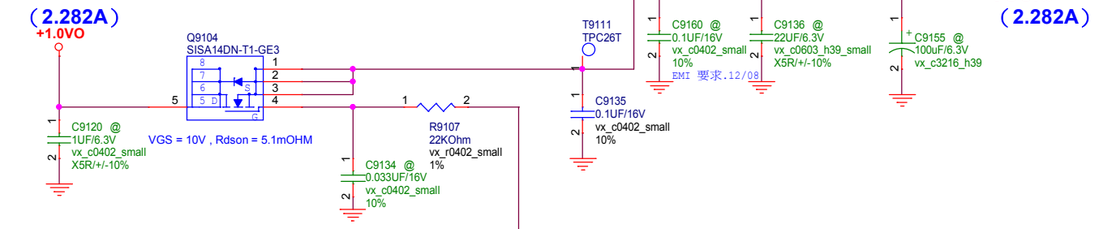
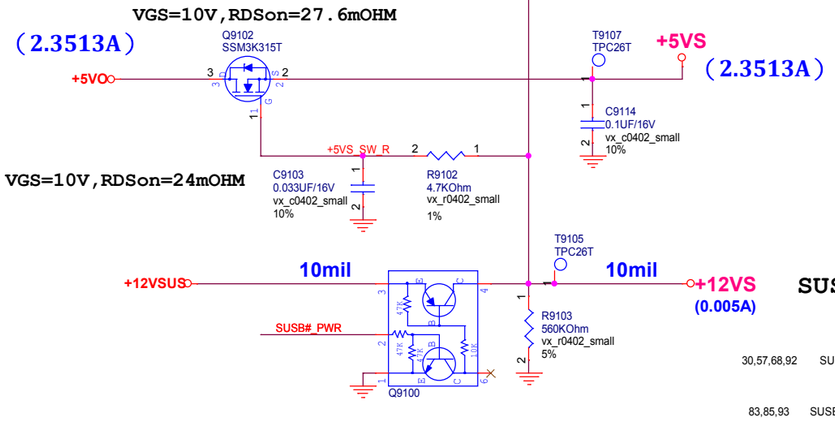
SUSC#_PWR POWER　　SUSB#_PWR POWER

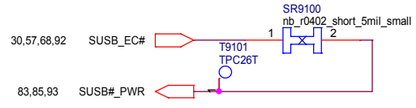




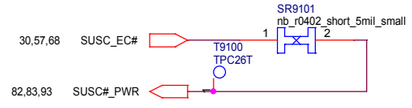




SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

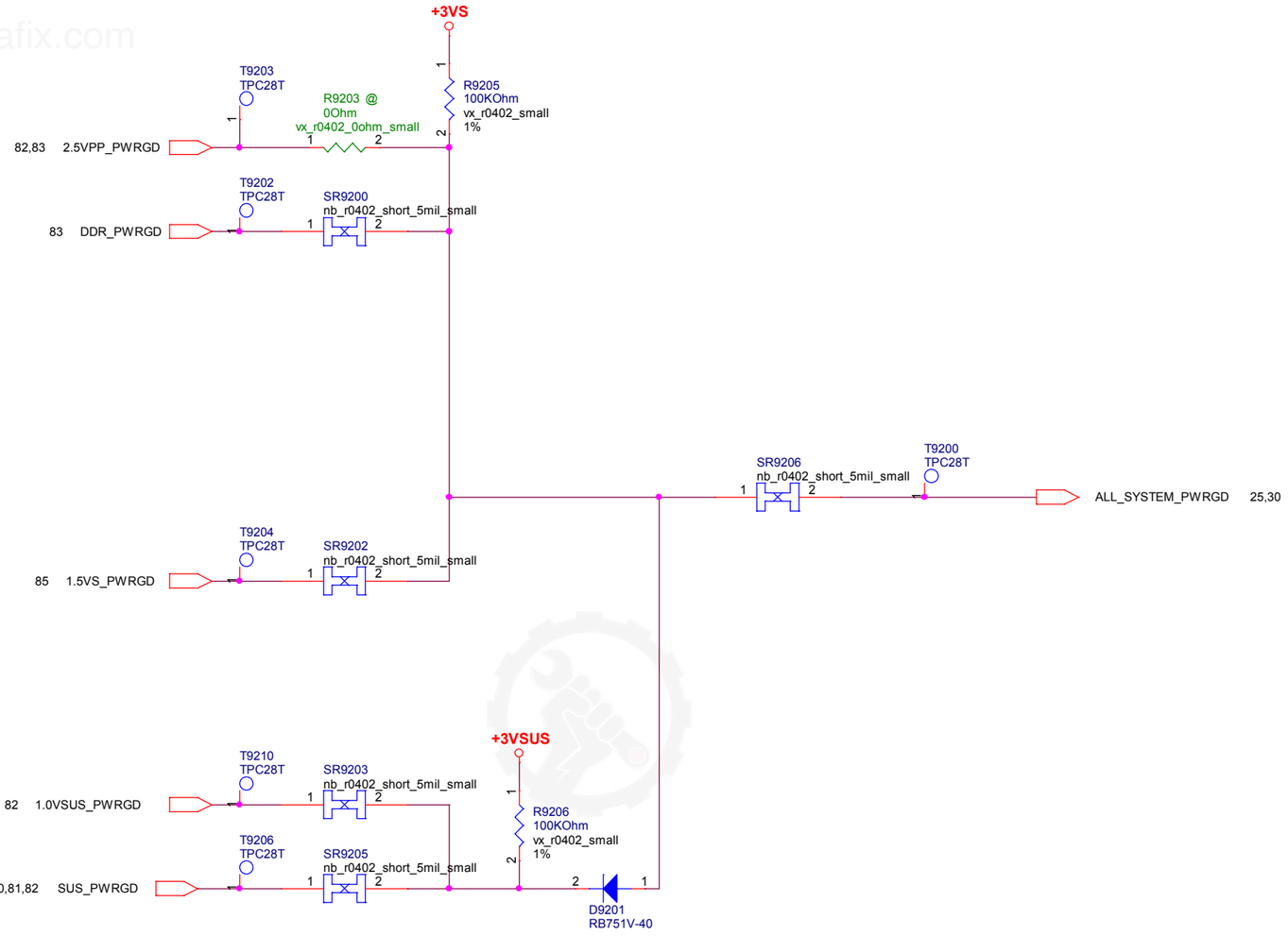
PEGATRON PROPRIETARY AND CONFIDENTIAL

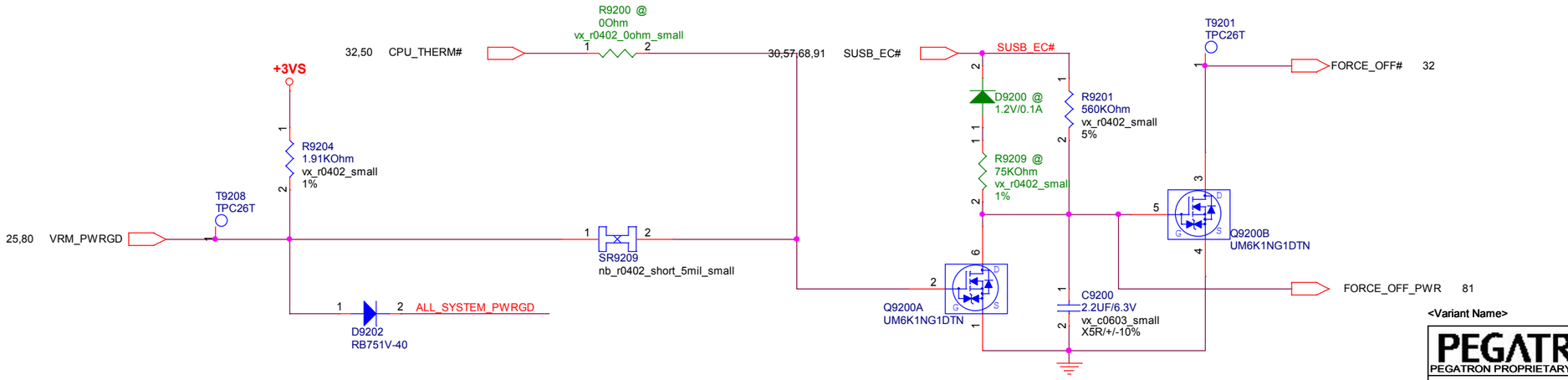
Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

Date: Tuesday, September 06, 2016　Sheet 91 of 94

POWER GOOD DETECTER





<Variant Name>

PEGATRON Title : POWER_PROTECT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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+USB_PD_IN — +USB_PD_IN 42,89
+A/D_DOCK_IN — +A/D_DOCK_IN 60,89
+AC_USBPD_WCT_IN — +AC_USBPD_WCT_IN 88,89
+AC_BAT_SYS — +AC_BAT_SYS 43,45,80,81,82,83,88
+BAT_CON — +BAT_CON 60,88
+RTC_POWER — +RTC_POWER 81

+5VA — +5VA 31,56,81
+3VA — +3VA 24,30,31,36,41,43,53,56,57,67,81,88

+5VO — +5VO 26,81,82,83,85,88,91
+3VO — +3VO 81,82,84,85,91
+2.5VO — +2.5VO 82
+1.8VO — +1.8VO 84
+1.5VO — +1.5VO 85

+1.2VO — +1.2VO 83

+1.0VO — +1.0VO 82,91
+0.6VO — +0.6VO 83

+12VSUS — +12VSUS 81,91
+5VSUS — +5VSUS 41,42,52,56,67,81
+3VSUS — +3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+1.8VSUS — +1.8VSUS 9,21,24,26,84
+1.0VSUS — +1.0VSUS 26,82

+12V — +12V 91
+2P5VPP — +2P5VPP 16,17,57,82
+1.2V — +1.2V 4,7,15,16,17,18,57,83
+1.0V — +1.0V 7,57,91

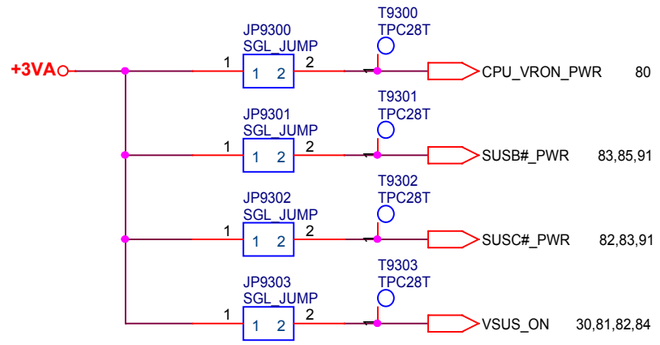
+12VS — +12VS 28,31,57,62,91
+5VS — +5VS 31,36,45,46,48,50,51,56,57,67,80,91
+3VS — +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92

+1.5VS — +1.5VS 36,57,85

+0.6VS — +0.6VS 15,17,57,83

+VCORE — +VCORE 5,57,80
+VCCGT — +VCCGT 6,57,80
+VCCSA — +VCCSA 7,57,80
+VCCIO — +VCCIO 3,7,57,91
+VCCPRIM_CORE — +VCCPRIM_CORE 26,82

FOR POWER TEST



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SIGNAL

BG1-POWER

Engineer: Adams Lin

Size	Project Name	Rev
B	P4	2.1

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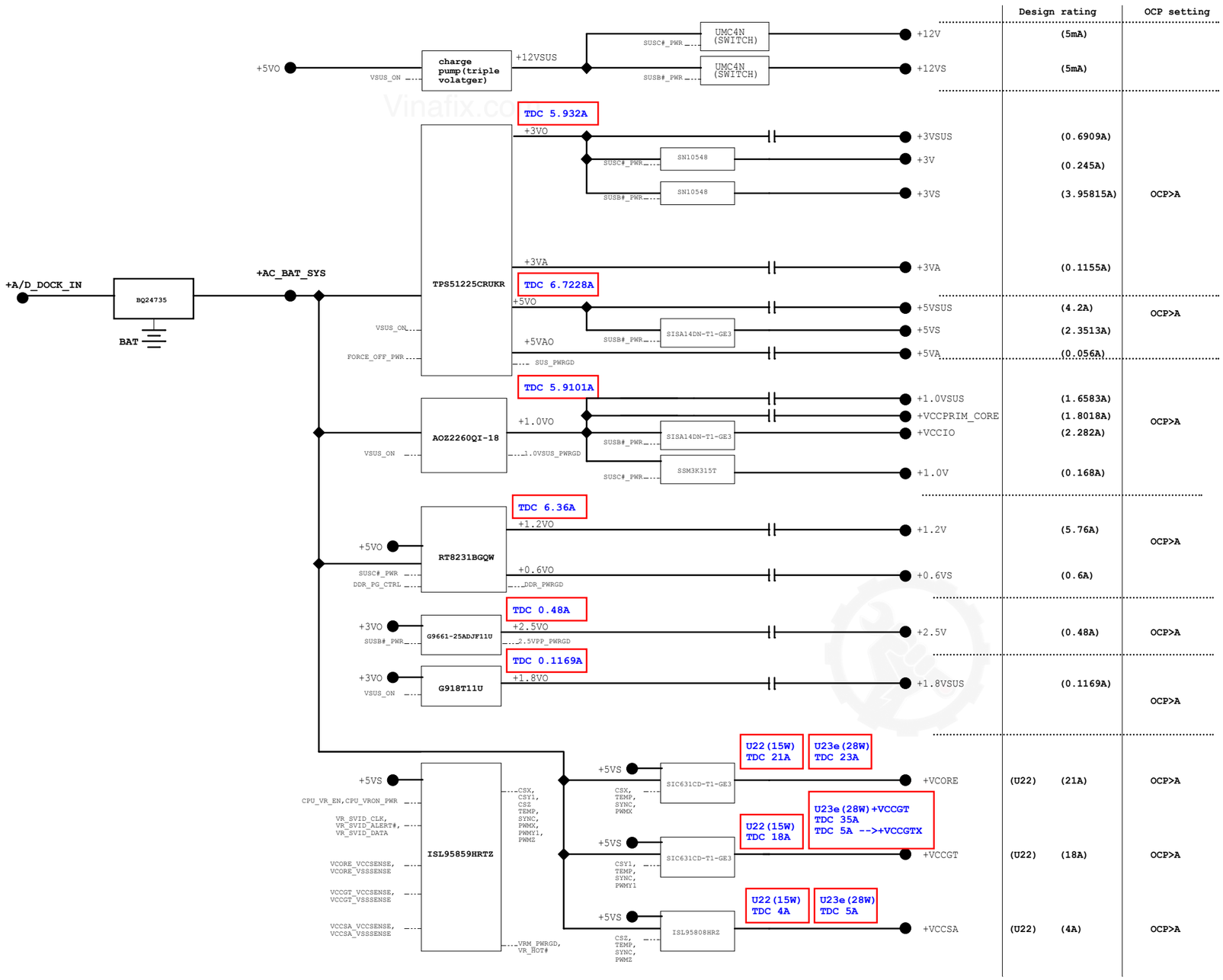

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_FLOWCHART

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P4	2.1

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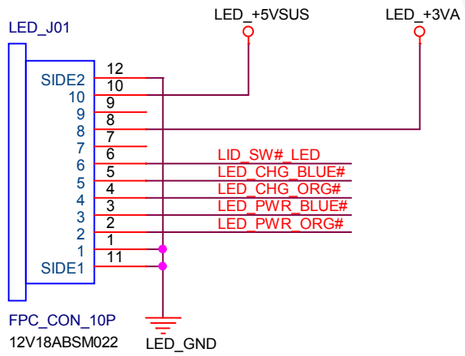
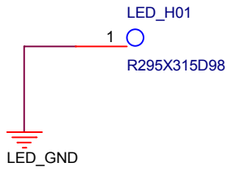
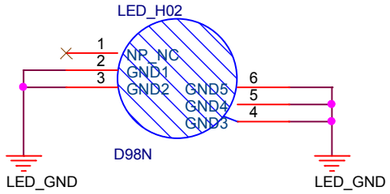
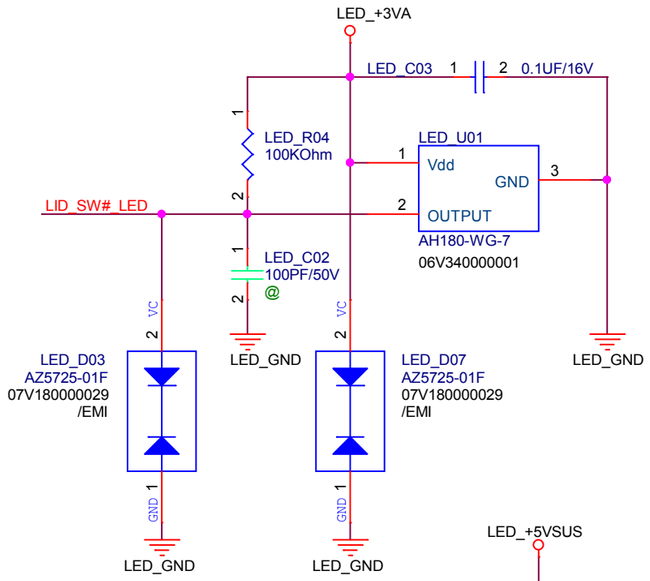
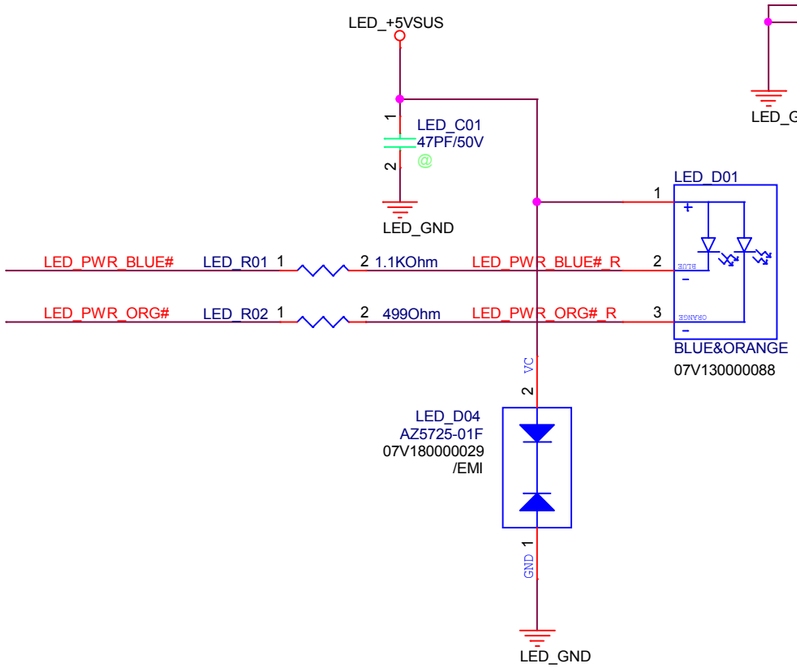
P4_LED BRD

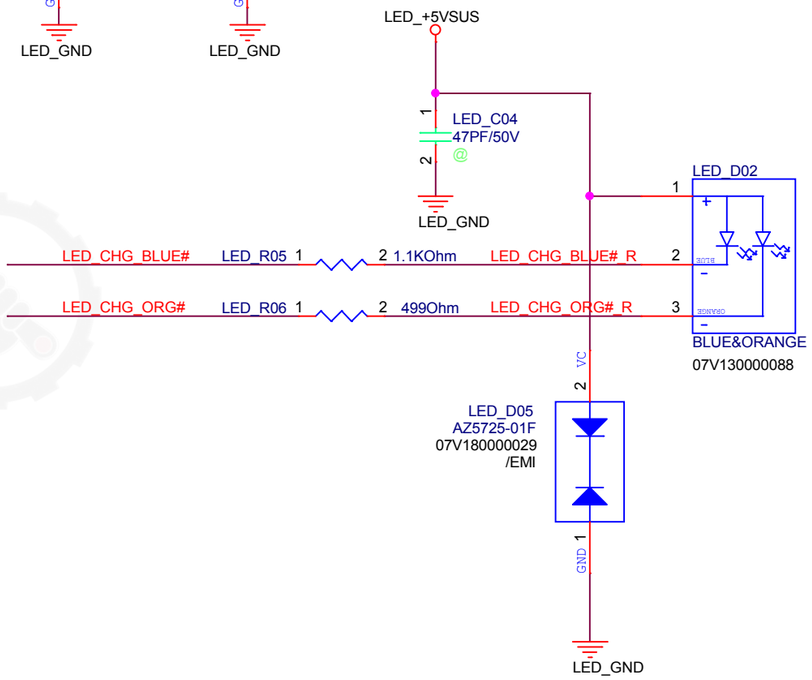












PEGATRON

Title : P4_LED BRD

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0
	P/N	

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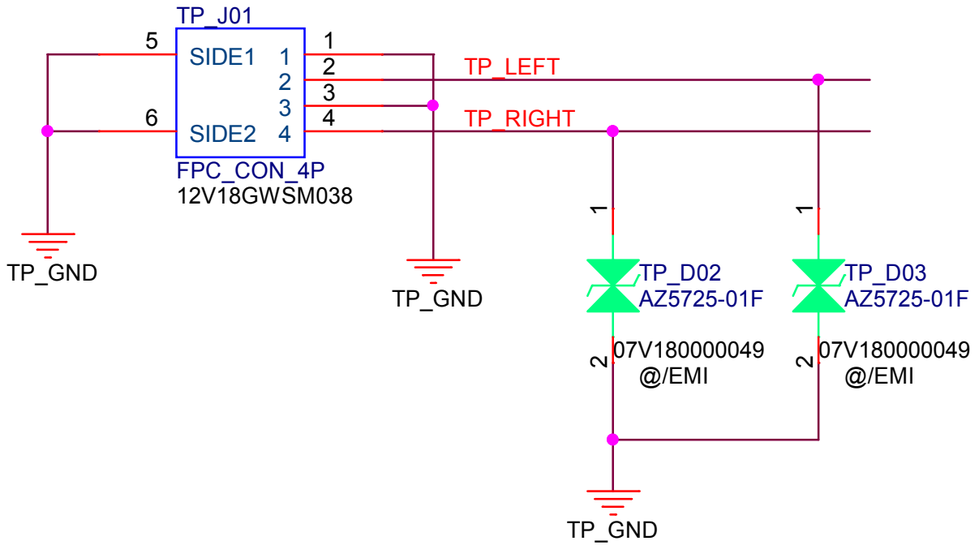
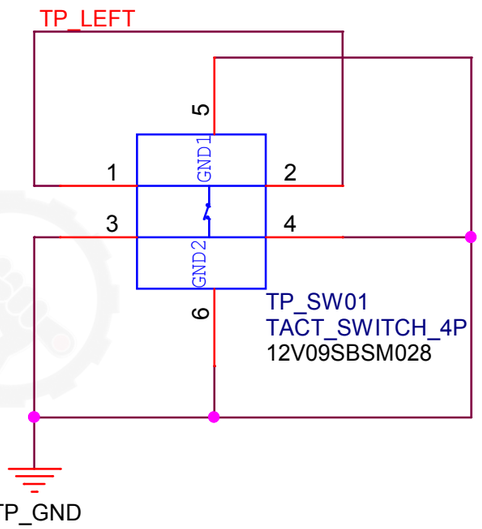
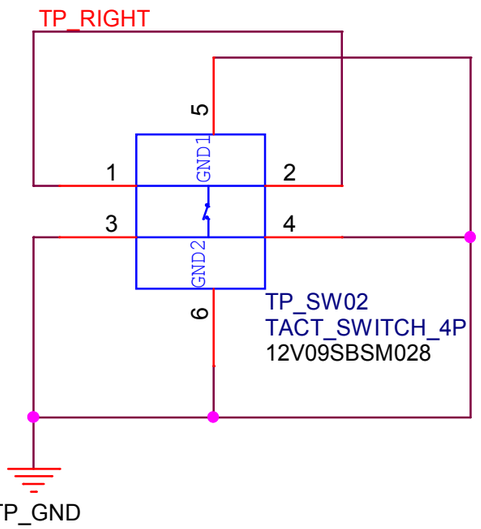
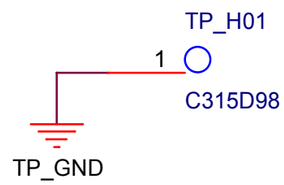
P4_TP-button BRD

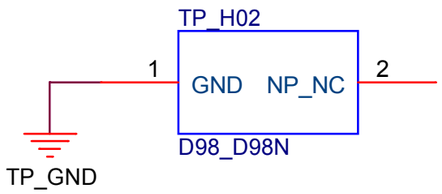
TP_BRD to TP_Model

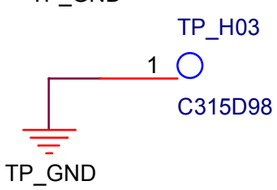


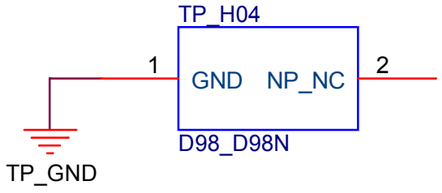












PEGATRON

Title : P4_TP-button BRD

BG1/HW3

Engineer: Bill Yang

Size	Project Name	Rev
Custom	P4	1.0
	P/N	

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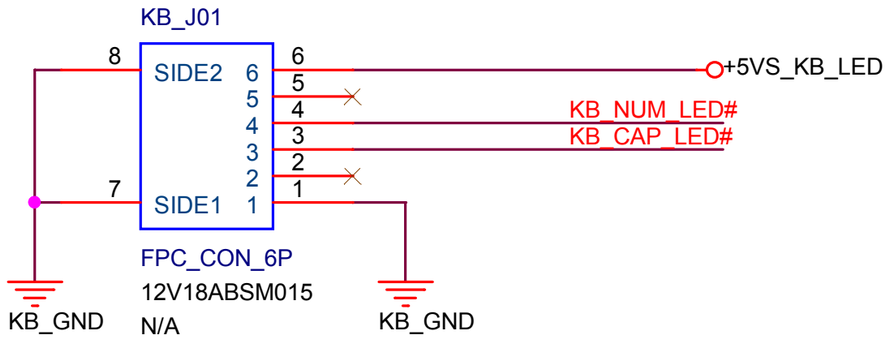

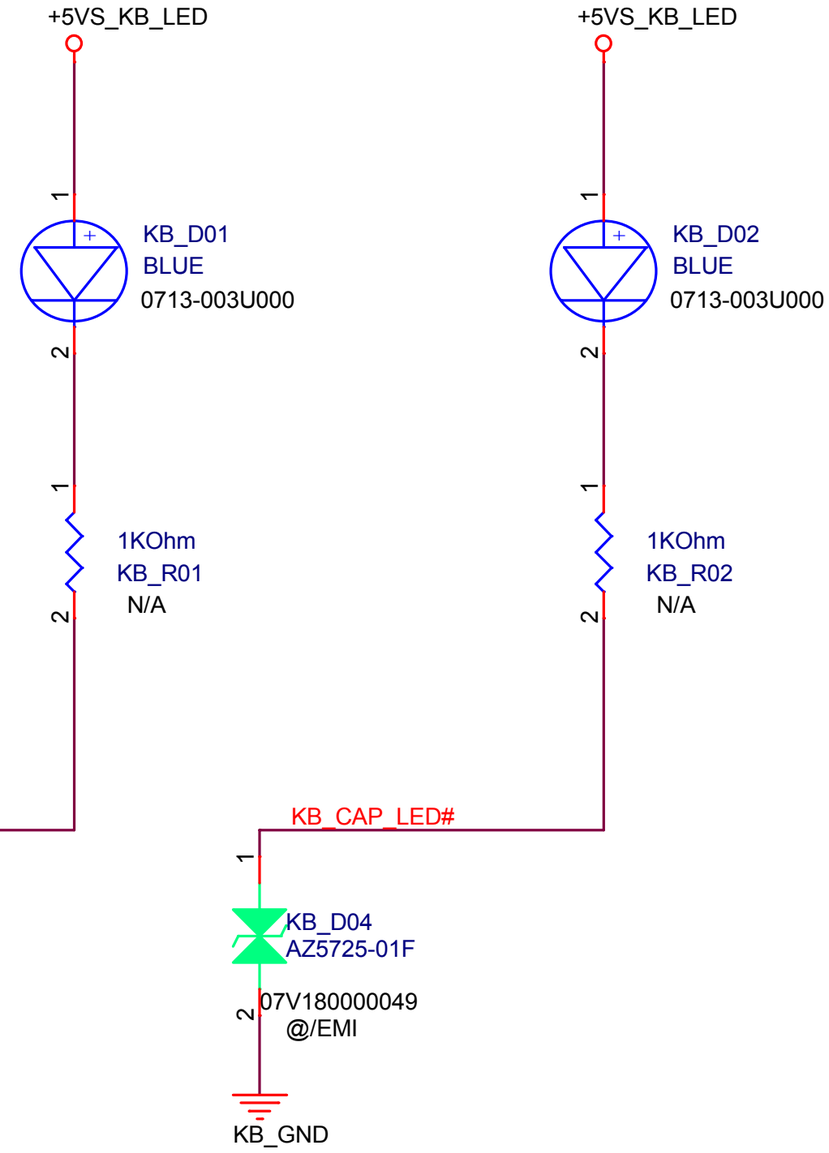

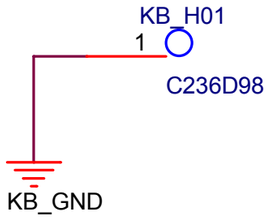

PEGATRON

Title : P4_KB LED

Engineer: Bill Yang

BG1/HW3

Size	Project Name	Rev
Custom	P4	1.1

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