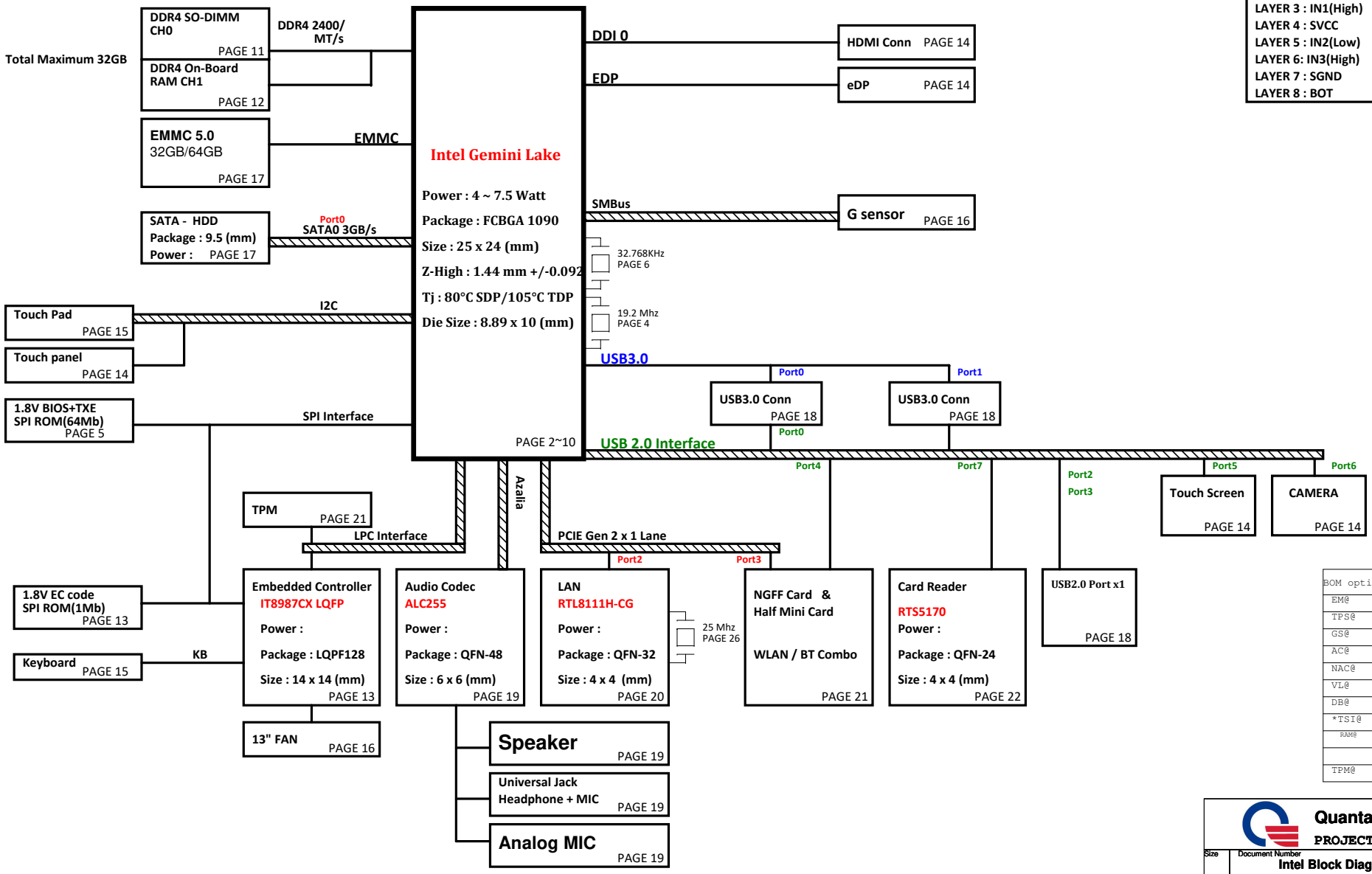
EJ-11 ZHE 11"

Intel Gemini Lake Block Diagram

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : SVCC
LAYER 5 : IN2(Low)
LAYER 6: IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



BOM option	Note
EM@	EMMC
TPS@	Touch Screen
GS@	G-Sensor
AC@	IOAC
NAC@	Non-IOAC
VL@	LED Backlight
DB@	Debug Conn.
*TSI@	Touch Screen I2C
RAM@	On Board RAM use
TPM@	DTPM

Quanta Computer Inc.

PROJECT : ZHE/ZSG

Size | Document Number: Intel Block Diagram | Rev 1A

Date: Wednesday, December 27, 2017 | Sheet 1 of 37

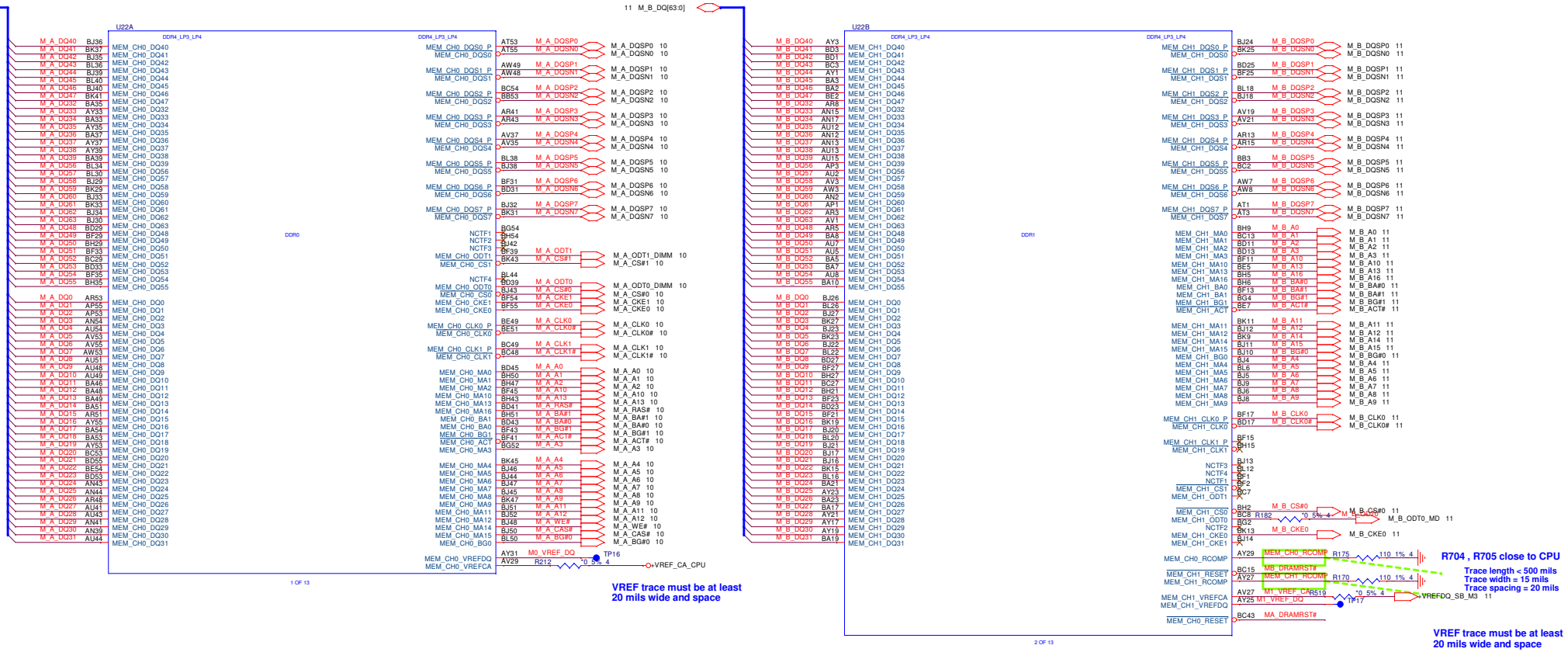
GLK ULT (DDR4)

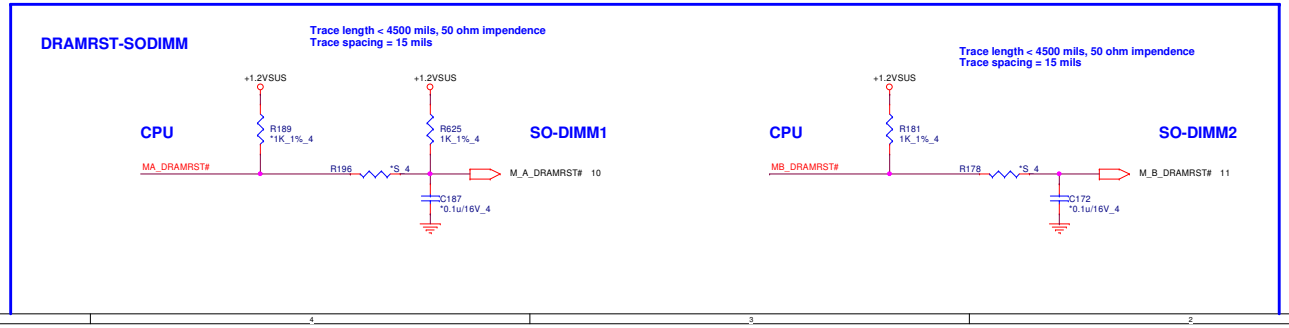
02

10,28 +VDDQ
7,10,11,28,33 +1.2VSUS

10 M_A_DQ[63:0]

11 M_B_DQ[63:0]





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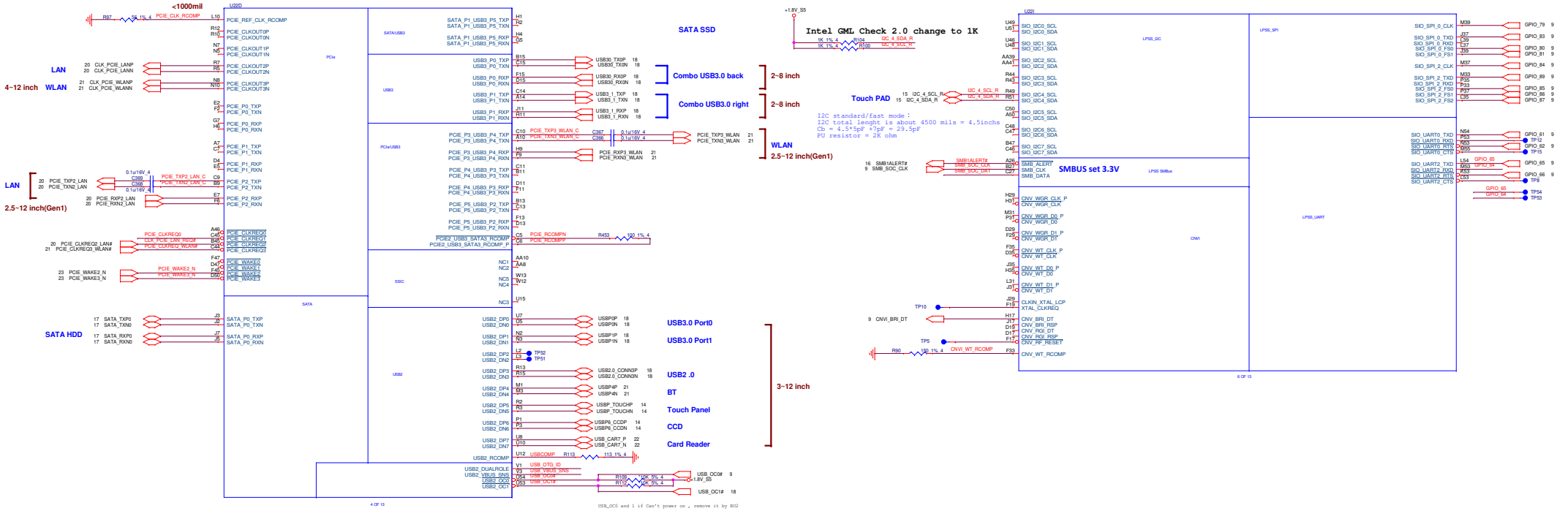
PROJECT : ZHE/ZSG

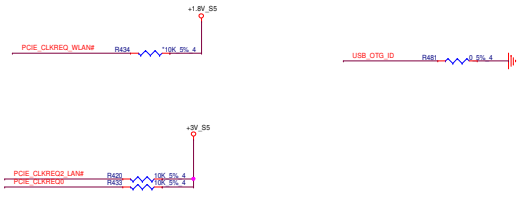
Size	Document Number	Rev
	GLK(MEMORY)	1A

Date: Wednesday, December 27, 2017 Sheet 2 of 37

Gemini lake (SATA , ODD, CLK ,USB,PCIE)

03





Quanta Computer Inc.			
PROJECT : ZHE/ZSG			
Size	Document Number		Rev
	GLK(PCIE/USB/SATA/CNVI)		1A
Date: Wednesday, December 27, 2017	Sheet 3	of 37	

Gemini lake (DISPLAY,eDP)

04

3,5,6,7,9,13,15,20,21,23,25,29,31 +1.8V_S5
14,17,20,31,32 +1.8V
3,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,30,31,32,33 +3V

U22C

Max 7.5 inch **HDMI**

14 INT_HDMITX2P — AH1 DDI0_TXP_0
14 INT_HDMITX2N — AH3 DDI0_TXN_0
14 INT_HDMITX1P — AE2 DDI0_TXP_1
14 INT_HDMITX1N — AE3 DDI0_TXN_1
14 INT_HDMITX0P — AJ2 DDI0_TXP_2
14 INT_HDMITX0N — AJ3 DDI0_TXN_2
14 INT_HDMICLK+ — AG2 DDI0_TXP_3
14 INT_HDMICLK- — AG3 DDI0_TXN_3
AC12 DDI0_AUXP
AC10 DDI0_AUXN

DDI0/DDI_B

HDMI_HPD

14 INT_HDMI_HPD# — C39 DDI0_HPD
14 HDMI_DDCCLK_SW — B43 DDI0_DDC_SCL
14 HDMI_DDCDATA_SW — C43 DDI0_DDC_SDA

AA2 DDI1_TXP_0
AA3 DDI1_TXN_0
Y3 DDI1_TXP_1
Y1 DDI1_TXN_1
AD1 DDI1_TXP_2
AD3 DDI1_TXN_2
AC2 DDI1_TXP_3
AC3 DDI1_TXN_3
AC7 DDI1_AUXP
AC5 DDI1_AUXN
C42 DDI1_DDC_SCL
A42 DDI1_DDC_SDA
C38 DDI1_HPD

DDI1/DDI_C

MDSI

MDSI_A_CLKP AL2
MDSI_A_CLKN AM3
MDSI_C_CLKP AG13
MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5
MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15
MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7
MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10
MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15
MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8
MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7
MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15
MDSI_C_DN_3 AE17

MIPI_I2C_SCL R53
MIPI_I2C_SDA R54

MDSI_C_TE T53
MDSI_A_TE T55
SOC_OVRIDE — GPIO_43 9

GPIO_42 HW Strap

MDSI_RCOMP AL5
MDSI_RCOMP — R507 150_1%_4

eDP Panel
<10000 mil

14 EDP_TXP0 — AE12 EDP_TXP_0
14 EDP_TXN0 — AE13 EDP_TXN_0
14 EDP_TXP1 — AC15 EDP_TXP_1
14 EDP_TXN1 — AC17 EDP_TXN_1
14 EDP_TXP2 — AE10 EDP_TXP_2
14 EDP_TXN2 — AE8 EDP_TXN_2
14 EDP_TXP3 — AE5 EDP_TXP_3
14 EDP_TXN3 — AE7 EDP_TXN_3
14 EDP_AUXP — W17 EDP_AUXP
14 EDP_AUXN — W15 EDP_AUXN
14 INT_EDP_HPD# — INT_EDP_HPD# B39 EDP_HPD

eDP/DDI_A

PCH_BKLTCTL B41 PNL0_BKLCTL
PCH_BKLTEN C40 PNL0_BKLTEN
PCH_VDDEN C41 PNL0_VDDEN

R114 100_1%_4 — EDP_RCOMP_P AA5 EDP_RCOMP_P
EDP_RCOMP_N AA7 EDP_RCOMP

3 OF 13

+3V — R82 *10K_5%_4 — PCH_VDDEN — R620 *S_4 — EDP_VDD_EN 14

+3V — R115 *10K_5%_4 — PCH_BKLTEN — R621 *S_4 — PCH_BLON 14

+3V — R86 *10K_5%_4 — PCH_BKLTCTL — R622 *S_4 — PCH_BRIGHT 14

Override

Flash Descriptor Override (SOC_OVRIDE)
0 = Normal Override(Normal operation)
1 = Override

+1.8V_S5 — R483 2.2K_5%_4 — SOC_OVRIDE

13 ME_WR# — 2 — Q33 2N7002K

Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	GLK (HDMI/eDP)	1A
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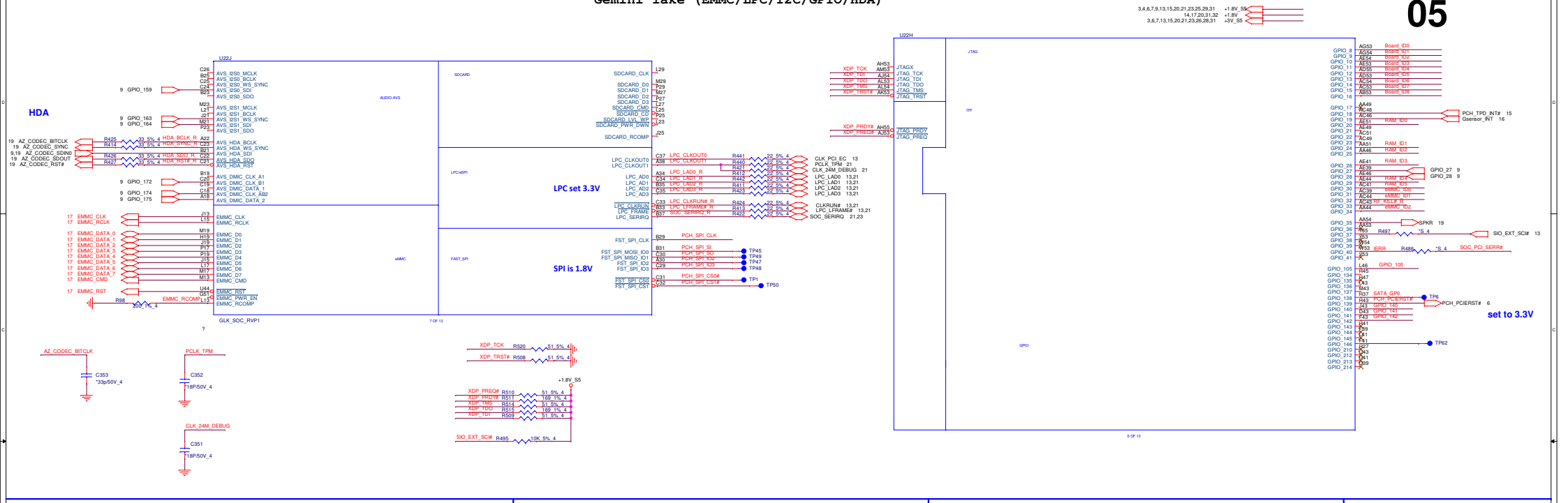
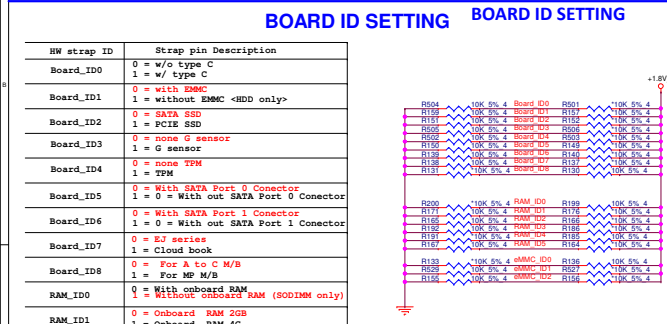
Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

05

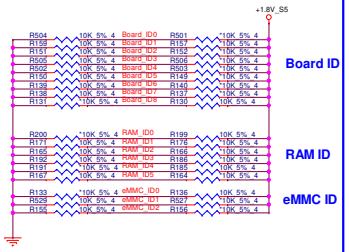




BOARD ID SETTING

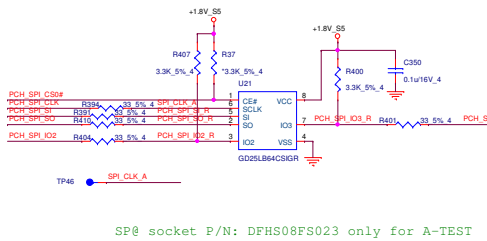
HW strap ID	Strap pin Description
Board_ID0	0 = w/o type C 1 = w/ type C
Board_ID1	0 = with EMMC 1 = without EMMC <HDD only>
Board_ID2	0 = SATA SSD 1 = PCIE SSD
Board_ID3	0 = none G sensor 1 = G sensor
Board_ID4	0 = none TPM 1 = TPM
Board_ID5	0 = With SATA Port 0 Conector 1 = 0 = With out SATA Port 0 Conector
Board_ID6	0 = With SATA Port 1 Conector 1 = 0 = With out SATA Port 1 Conector
Board_ID7	0 = EJ series 1 = Cloud book
RAM_ID0	0 = For A to C M/B 1 = For MP M/B
RAM_ID1	0 = With onboard RAM 1 = Without onboard RAM (SODIMM only)
RAM_ID2	0 = Onboard RAM 2GB 1 = Onboard RAM 4G
	(Reserved)

BOARD ID SETTING

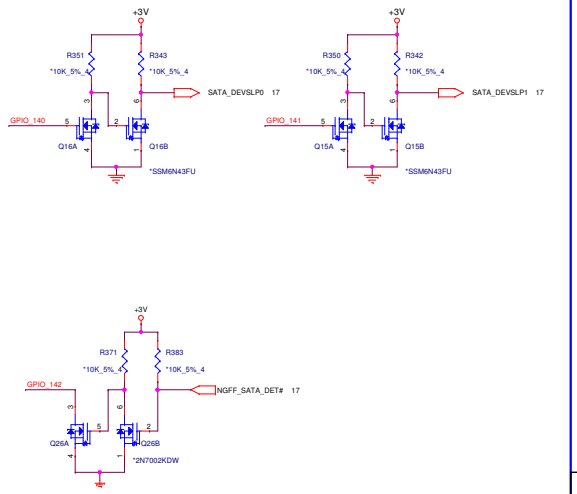


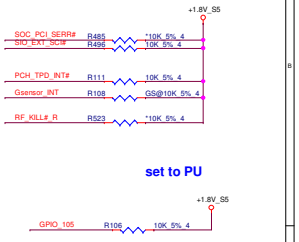
RAM_ID5	RAM_ID4	RAM_ID3	Vender	Quanta PN	Description
0	0	0	Micron-8Gb	AR05QGST118	IC SDRAM(96P)MT40A512M16JY-083E:B STNBSQ
0	0	1	Hynix-8Gb	AR05QGST905	IC SDRAM(96P)H5AN8G6NAFR-UHC(FBGA)STNBSQ
0	1	0	Samsung-8Gb	AR05Q20T504	IC SDRAM(96P)K4A8G165WB-BCRC STNBSQ
0	1	1			

eMMC_ID1	eMMC_ID0	eMMC_ID0	Vender	Quanta PN
0	0	0	Samsung 32/64GB	
0	0	1	Hynix 32/64GB	AR2HXXR1001--HYNIX 32G AR0ISSER1000--HYNIX 64G
0	1	0	Kingston 32/64GB	
0	1	1	Sandisk 32G/64GB	AR02KXR1000--Sandisk 32G AR02KXR1001--Sandisk 64G
1	1	1	Toshiba 128GB	



SP@ socket P/N: DFHS08FS023 only for A-TEST





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PROJECT : ZHE/ZSG

Size	Document Number	Rev
	GLK (GPIO/LPC/I2C/HDA)	1A
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Gemini lake (PMU/PMIC/RTC)

06

PMU set to 3.3V

check list use 20k

RTC is 3.3V

1.8V

PMU set 3.3V

EC reset RTC

RTC Circuitry (RTC)

RTC Clock 32.768KHz (CPU)

Trace width = 20 mils

Trace length < 1000 mils

ML1220 Coin type
AHL03001031 [VDE] 17mAH
AHL03001057 [DBV] 17mAH

Quanta Computer Inc.
PROJECT : ZHE/ZSG
GLK (PMU/PMIC/SMB/RTC)
Rev 1A
Date: Wednesday, December 27, 2017 Sheet 6 of 37

EDGE DECAPS
FOR EXPOSED POWER PLANES

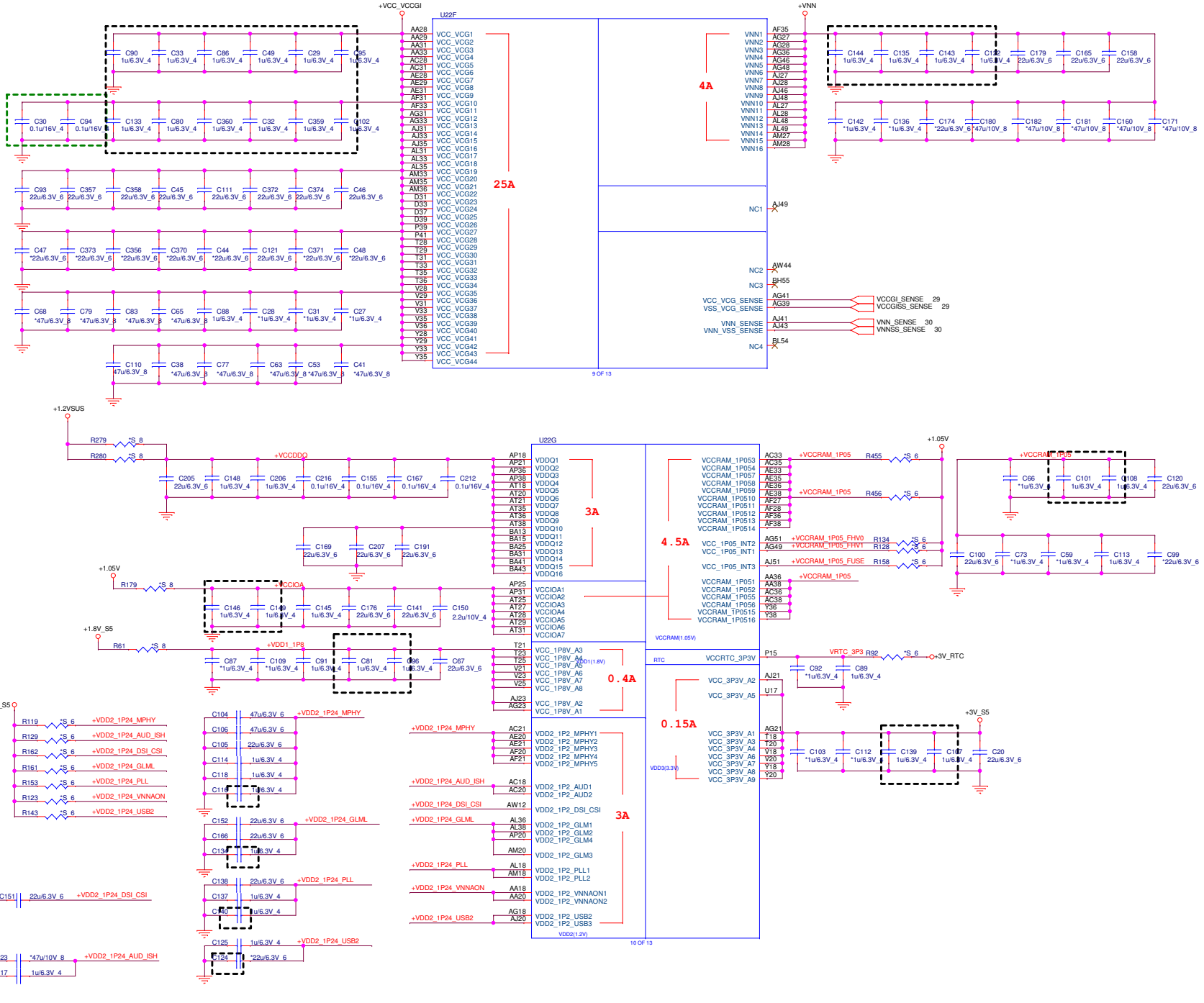
BACK side cap

Gemini (POWER)

07

3,6,13,15,20,21,23,26,28,31 +3V_S5
31 +1.24V_S5
3,4,5,6,9,13,15,20,21,23,25,29,31 +1.8V_S5
6,13 +3V_RTC

30 +VNN
29 +VCC_VCCGI
6,27,29,30 +1.05V
10,28 +VDDQ



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PROJECT : ZHE/ZSG

Size	Document Number	Rev
	GLK (POWER)	1A
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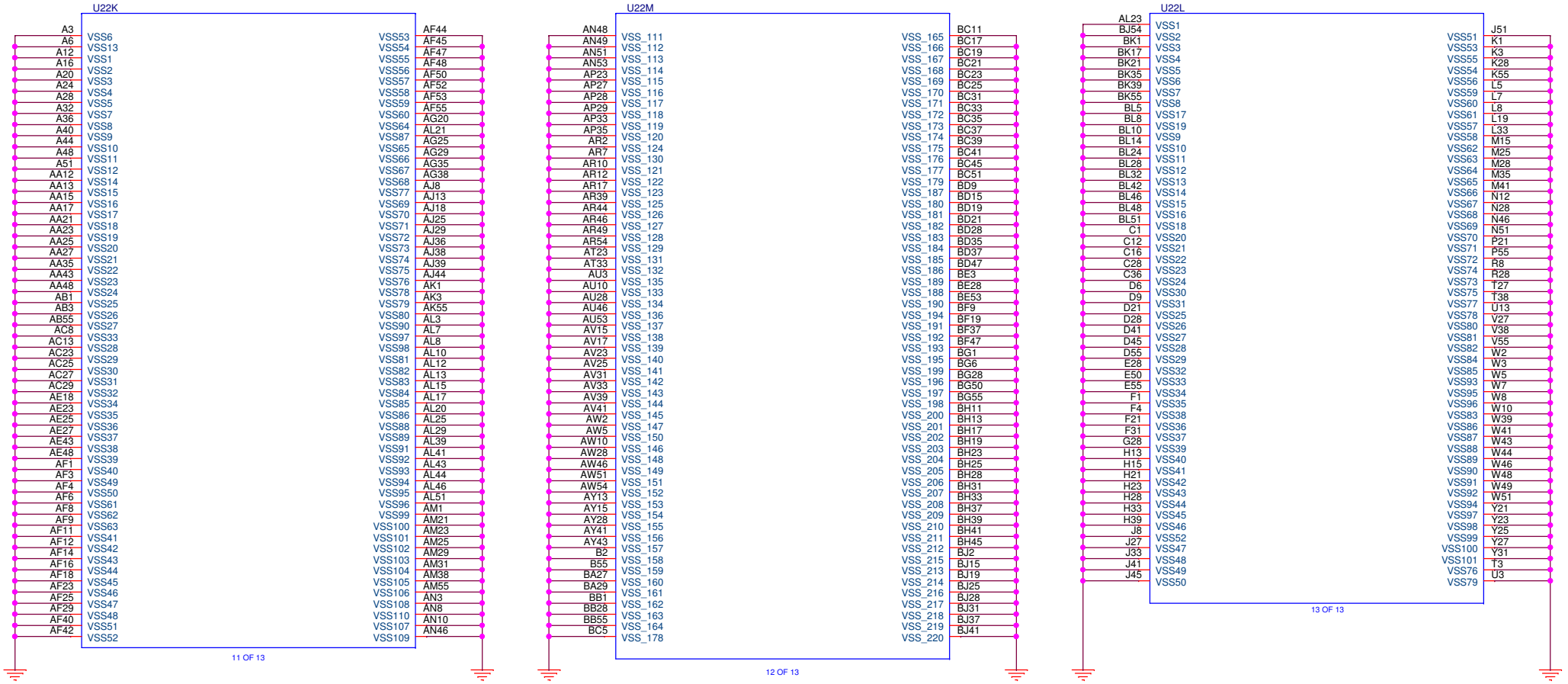
GLK ULT (GND)

08



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PROJECT : ZHE/ZSG

Size	Document Number	Rev
	GLK (GND)	1A
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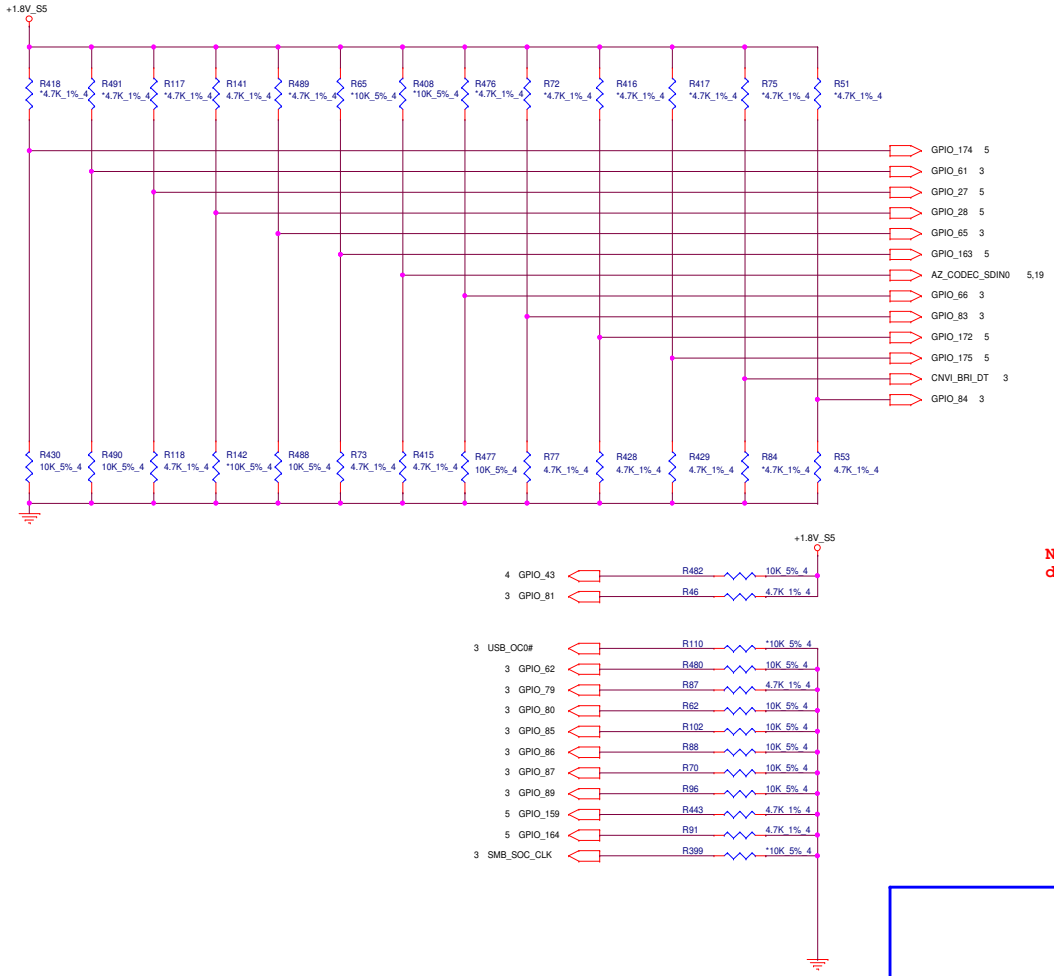
HARDWARE STRAPS



Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.

Note: The default for A0 will be eSPI due to a bug on LPC.

Hardware Strap	Strap Description	Value
GPIO_174	VDD2 1.24V vs.1.20V select 0 = 1.2V(default) 1 = 1.24V	0
GPIO_61	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_27	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_28	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_65	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_163	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
AZ_CODEC_SDIN0	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_66	LPC No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_83	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
		0
GPIO_172	SMbus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_42	Top swap override 0 = Disable 1 = Enable	0
GPIO_175	eSPI vs. LPC 0 = LPC mode (default) 1 = eSPI mode	0
CNVI_BRI_DT	eSPI Flash Sharing Mode: 0 = master attached flash sharing (MAFS; default) 1 = slave attached flash sharing (SAFS)	0
GPIO_84	Allow SPI as a boot source 0 = Enable (default) 1 = Disable	0

P/N and F/P

JDIM1A — DDR4 SODIMM 260 PIN (260P) — D4AR0-26001-1P52

JDIM1B — DDR4 SODIMM 260 PIN (260P) — D4AR0-26001-1P52

RVS

DFHSR0FR043	FOX	AS0A821-H2RB-7H
DFHSR0FR045	LTK	D4AR0-26001-1P52
DFHSR0FR078	LTS	ADDR0208-P035A

2250mA

0.5A

600mA

12/4 Change for +3.3V to +3V

12/21 Change JDIM2 footprint to "ddr4-d4as0-26001-1p52-std-smt " for SMT requset

VREF DQ0 M1 Solution

Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

28	+VDDQ	
11,28	+2.5V_SUS	
2,7,11,28,33	+1.2VSUS	
11,28	+VDDQ_VTT	
2	+VREF_CA_CPU	
3,4,5,6,13,14,16,17,19,20,21,22,26,27,28,29,30,31,32,33	+3V	

Quanta Computer Inc.

PROJECT : ZHE/ZSG

Size	Document Number	Rev
	DDR4 DIMM-STD 4H (CH. A)	1A

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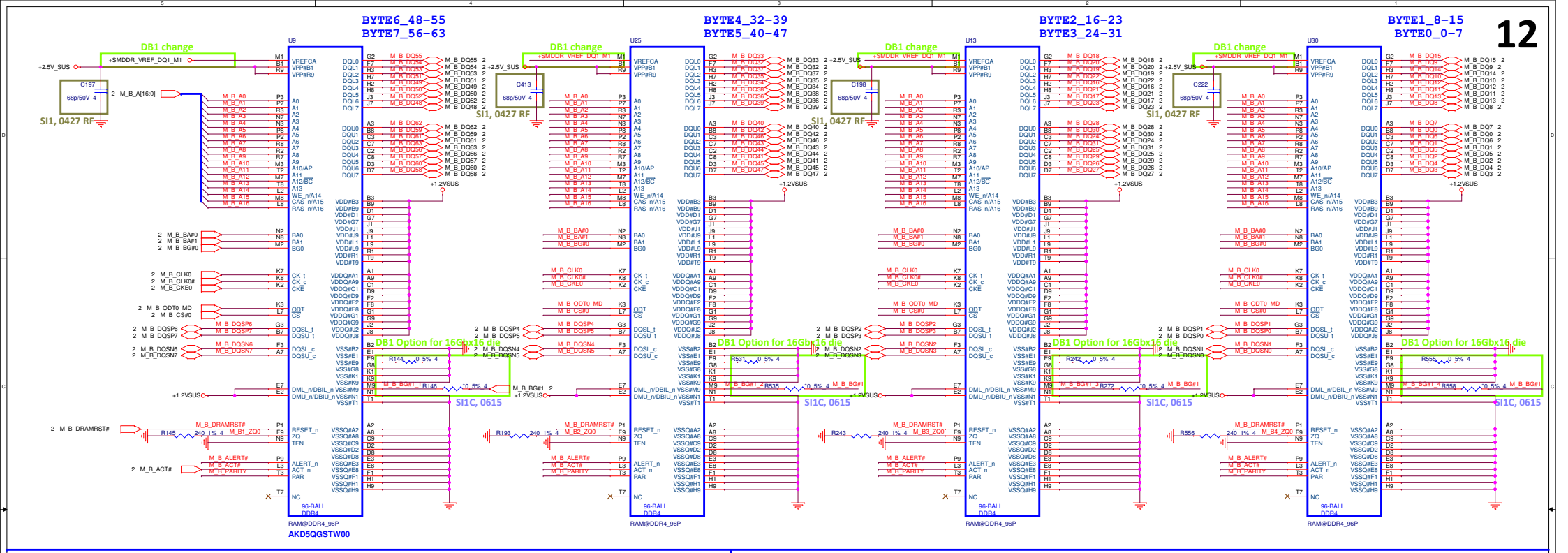


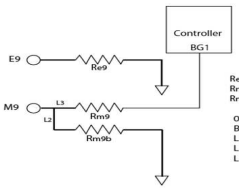
Vendor	P/N	Vendor P/N
MIC 16G	AKD5EG0TL00	MT40A1G16HBA-083E:A
Elpida		
SAMSUNG		

DB1 Option for 16Gbx16 die
Close DDR ball

DB1 12/11, close memory

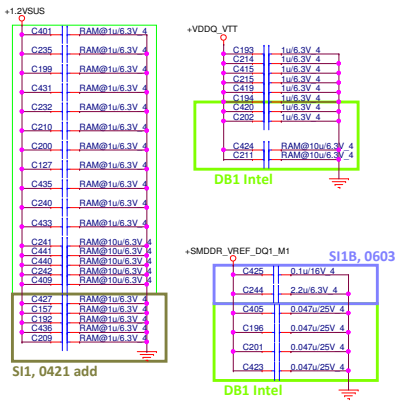
In the middle of CPU and Double-2

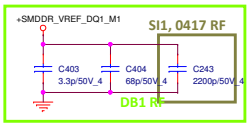
Memory 8G & Memory 16G TABLE		
	Memory 8G	Memory 16G
R278	0Ω CS00002JB38	240Ω CS12402FB03
R279	0Ω CS00002JB38	240Ω CS12402FB03
R280	0Ω CS00002JB38	240Ω CS12402FB03
R281	0Ω CS00002JB38	240Ω CS12402FB03
R282	UNINSTAL	INSTAL
R283	UNINSTAL	INSTAL
R284	UNINSTAL	INSTAL
R285	UNINSTAL	INSTAL
R290	INSTAL	UNINSTAL
R291	INSTAL	UNINSTAL
R292	INSTAL	UNINSTAL
R293	INSTAL	UNINSTAL

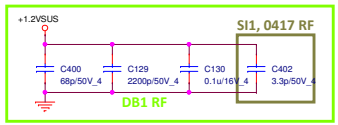


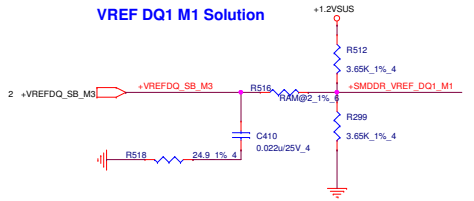
Place these Caps near Channel B

1uF/10uF 4pcs on each side of connector









Quanta Computer Inc.
PROJECT : ZHE/ZSG
Size
Document Number
DDR4 Memory Down (CH. B)
Rev 1A
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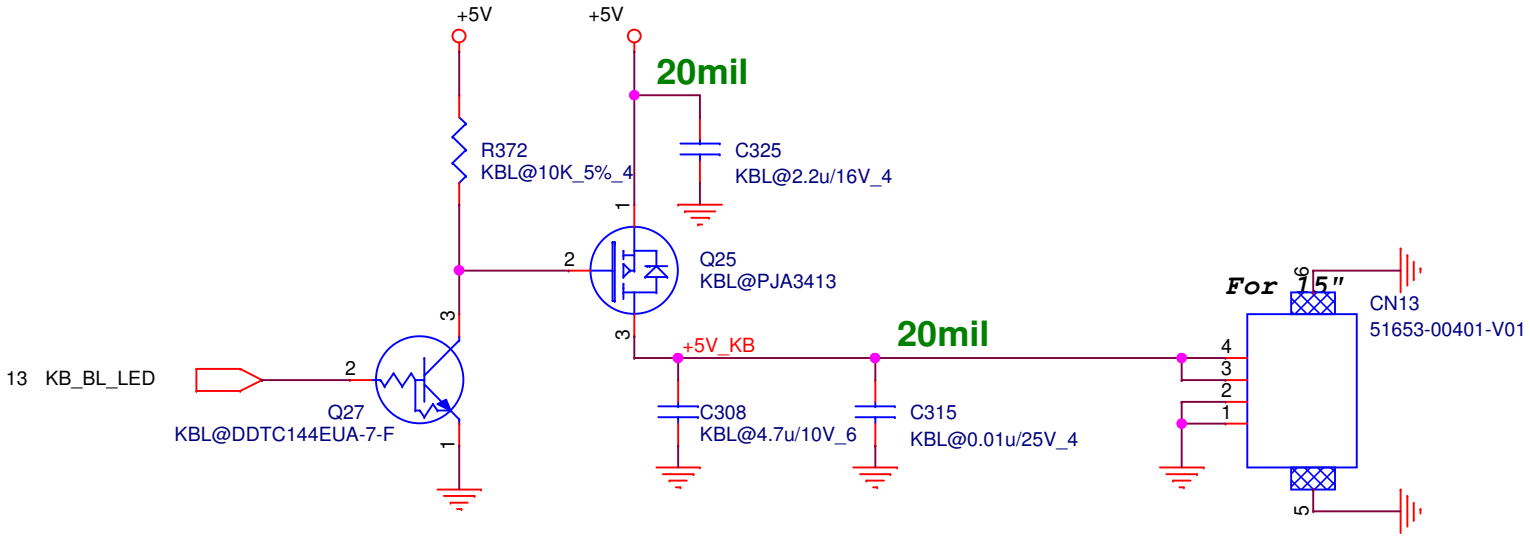

Quanta Computer Inc.

PROJECT : ZHE/ZSG

Size	Document Number	Rev
	Change List-2	1A
Date: Wednesday, December 27, 2017	Sheet 12 of 37	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

L7 BLM15AG121SN1D

+3VPCU

VSTBY_FSPI

C257 0.1u/16V_4

ECAGND

R256

C245 0.1u/16V_4 C271 0.1u/16V_4 C228 0.1u/16V_4 C226 0.1u/16V_4 C429 0.1u/16V_4 C428 0.1u/16V_4

+3V_LDO_EC

R214 2.2_5%_6

+3VPCU_EC

2.2_5%_6

C217 0.1u/16V_4

+3V

R285 2.2_5%_6

+3V_S5

R286 2.2_5%_6

10/29 Modify it

+3V_EC

C229 0.1u/16V_4

12 mils

+3VPCU_ECPLL

L4 BLM15AG121SN1D

+3VPCU_EC

(For PLL Power)

C221 0.1u/16V_4

11/11 swap to pin 125

+1.8V_S5 3,4,5,6,7,9,15,20,21,23,25,29,31
+3V 3,4,5,6,10,14,16,17,19,20,21,22,26,27,28,29,30,31,32,33
+3VPCU 6,14,15,16,19,20,21,22,25,26,31,33
+3V_S5 3,6,7,15,20,21,23,26,28,31

U14 IT8987E/BX

IT8987

LPC

5,21 LPC_LAD0 → LAD0 10
5,21 LPC_LAD1 → LAD1 9
5,21 LPC_LAD2 → LAD2 8
5,21 LPC_LAD3 → LAD3 7
6,17,20,21 PLTRST# → PLTRST# 22
5 CLK_PCI_EC → LPCCLK/GPM4 13
5,21 LPC_LFRAME# → LFRAME#/GPM5 6
PROCHOT_EC → LPCPD#/GPE6 17

GPIO

DDR4_SUSON_2V5 → GA20/GPB5 126
IRQ_SERIRQ → SERIRQ/GPM6 5
PCH_SUSPWRDNACK → ECSMI#/GPD4 23
SIO_EXT_SCI# → ECSCI#/GPD3 4
WRST# → WRST# 16
IOAC_WLAN_WAKE# → KBRST#/GPB6
PWUREQ#/BBO/GPC7

PS/2

PS2DAT0/TMB1/GPF1
PS2CLK0/TMB0/CEC/GPF0
PS2DAT1/RTS0#/GPF3
PS2CLK1/DTR0#/GPF2
PS2DAT2/GPF5
PS2CLK2/GPF4

UART

DSR0#/GPG6
GINT/CTS0#/GPD5
RXD/SIN0/GPB0
TXD/SOUT0/GPB1

FLASH

SSCE1#/GPG0
FSCK/GPG7
FMISO/GPG5
FMOSI/GPG4
SSCE0#/GPG2

KBMX

KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7

CLOCK

GPJ6
GPJ7

SM_BUS

EGCLK/GPE3 → PCH_ACPRESENT → TP63
EGCS#/GPE2 → VCCDSW → R290 → TP33
EGAD/GPE1 → BT_EN → BT_EN 21
KSO16/SMOSI/GPC3 → MY16 15
KSO17/SMISO/GPC5 → MY17 15
L80HLAT/BAO/GPE0 → GPE0 → TP35
L80LLAT/GPE7 → GPE7 → TP36
DTR1/SBUSY/GPG1/ID7 → HWPG_1.05V_EC# → *S_4 → R225 → THERMTRIP# 6
GPH6/ID6 → GPH6 → TP26 → *S_4 → USBON# 18
GPH5/ID5 → GPH5 → R274 → *S_4 → TPD_EN 15
GPH4/ID4 → GPH4 → TP29
GPH3/ID3 → GPH3
CTX1/SOUT1/SMDAT3/GPH2/ID2 → GPH2 → TP30
CRX1/SIN1/SMCLK3/GPH1/ID1 → GPH1 → TP31
CLKRUN#/GPH0/ID0 → GPH0 → R282 → *S_4 → CLKRUN# 5,21
GPH7

SMCLK2/PECI/GPF6 → GPF6 → TP24
SMDAT2/PECIRQ7#/GPF7 → LIDF_H → R549 → 33_5%_4 → LID# 14,16
SMCLK0/GPB3 → MBCLK → MBCLK 25
SMDAT0/GPB4 → MBDATA → MBDATA 25
SMCLK1/GPC1 → 2ND_MBCLK → 2ND_MBCLK 16
SMDAT1/GPC2 → 2ND_MBDATA → 2ND_MBDATA 16
D40 180P/50V_4
D40 Change 180P

PWM

PWM0/GPA0 → PWRLED# 22
PWM1/GPA1 → BATLED1# 22
PWM2/GPA2 → SUSLED# 22
PWM3/GPA3 → BATLED0# 22
PWM4/GPA4 → MAINON 26,27,28,31,32
PWM5/GPA5 → GPA5 → TP58
PWM6/SSCK/GPA6 → TS_EN → TS_EN 14
PWM7/RIG1#/GPA7 → PCBEEP_EC → PCBEEP_EC 19
1/20 Swap with pin 79
TACH0A/GPD6 → FAN1_RPM → TP40 → FAN1_RPM 16
TACH1A/TMA1/GPD7

WAKE UP

GPJ1 → R300 → *S_4 → SYS_HWPG 26
TACH2/GPJ0 → VNN_ON → VNN_ON 29,30
TMR0/GPC4 → SUSON → SUSON 28
TMR1/GPC6 → GPC6 14
PWRSW/GPE4 → NBSWON# → NBSWON# 15,16
R14/GPD0 → R296 → *S_4 → SUSC# → SUSC# 6,15
RI2#/GPD1 → HWPG
RTS1#/GPE5 → WLANPWR# → WLANPWR# 21
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 → RSMRST# → RSMRST# 23

A/D D/A

ADC0/GPI0 → RF_EN → RF_EN 21
ADC1/GPI1 → ICMNT → ICMNT 25
ADC2/GPI2 → GPI2 → VRON 29
ADC3/GPI3 → SS_ON_R → R312 → *S_4 → S5_ON → S5_ON 26,30,31
ADC4/GPI4 → LANPWR# → LANPWR# 20
ADC5/DCD1#/GPI5 → ODD_POWER → TP38
ADC6/DSR1#/GPI6 → ACIN → ACIN 25
ADC7/CTS1#/GPI7 → TEMP_MBAT# → TEMP_MBAT# 25

DAC5/RIG2#/GPJ5 → FAN1_DAC → *0_5%_4 → TP54 → FAN1_DAC 16
DAC4/DCD0#/GPJ4 → NUMLED# → R292 → *0_5%_4 → TP55
DAC3/TACH1B/GPJ3 → GPJ3 → R294 → 0_5%_4 → CLR_CMOS 6
DAC2/TACH0B/GPJ2
R297 → 100K_5%_4 → Add CLR_CMOS PD 10/30
PANEL_LED_EN → PANEL_LED_EN 24

VSS_2 VSS_27 VSS_51 VSS_104 AVSS VCORE_75 VCORE_12

ECAGND

C231 0.1u/16V_4

L8 BLM15AG121SN1D

ICMNT C261 10u/6.3V_6 ECAGND

Add SYS_SHDN# 10/27

Sawp TS_EN and CPUFAN# 10/23

PIN	PANEL_LED_EN	Active H
GPC0	Only for 2 cell battery	

The sequence requirement for "VCC_1P05 High (90%) to SOC_PWROK (PCH_PWROK)" assertion timing is minimum of 5mS (Min = 5mS). There is no maximum timing requirement for this sequence. This will be updated in the next revision of Apollo Lake EDS MoW_WW39

8987BX: AJ089870F01
8987CX: AJ089870F02

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU Thermal
SM Bus 3	
SM Bus 4	

HWID

+3V R221 200K_5%_6 GPC6 R248 *200K_5%_6 GND

12/09 EC request ZHP/ZSP ID PD.
ZHP(11" KB)---L (eDP Cable pull-low)
ZHP(13" KB)---H

HWPG(KBC)

Remove SYS_HWPG for HWPG 10/26

+3V R302 10K_5%_4 HWPG

30	IMVP_PWRGD_VNN	D8	*RB500V-40
28	HWPG_1.2VSUS	D18	RB500V-40
27	HWPG_1.05V	D11	RB500V-40
29	IMVP_PWRGD	D10	*RB500V-40
28	HWPG_2.5V	D22	*RB500V-40
31	HWPG_1.24V_S5	D14	*RB500V-40
31	HWPG_1.8V_S5	D9	*RB500V-40
31	HWPG_1.5V	D21	*RB500V-40

SPI NOR FLASH

15 mil

VCC_SPI C426 0.1u/16V_4

U29 W25X10CLSNIG

R547 3.3K_1%_4 SPI_WP#
R541 3.3K_1%_4 SPI_Hold#
GND

PCH_SPI_SI_EC → TP60
PCH_SPI_SO_EC → TP58
SPI_CS0#_UR_ME → TP57
PCH_SPI_CLK_EC → TP59

SPI Socket P/N:DFHS08FS023
A-stage stuff Socket

VCC_SPI R538 3.3K_1%_4 SPI_CS0#_UR_ME
PCH_SPI_SI_EC R546 *10K_5%_4
PCH_SPI_SO_EC R543 *10K_5%_4

VSTBY_FSPI R542 *S_4 VCC_SPI

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
3.3V	WND	128K	AKE35ZN0N00	W25X10CLSNIG
	GGD	128K	AKE5BY00000	GD25D10BTIGR
	MAX	128K	AKE35FN0Z02	MX25L1006EMI-10G

Modify 10/27

NBSWON# R258 10K_5%_4
S5_ON R268 *10K_5%_4
SPIVCC_ON R259 10K_5%_4
+3V_LDO_EC

開EC對底下SPI ROM的interface

MAINON R314 100K_5%_4
SUSON R550 100K_5%_4
S5_ON R275 10K_5%_4

SM BUS PU(KBC)

+3V_LDO_EC
MBCLK R250 4.7K_5%_4
MBDATA R267 4.7K_5%_4
+3V
2ND_MBCLK R234 4.7K_5%_4
2ND_MBDATA R262 4.7K_5%_4

Change 2nd SMBUS PU to +3V 11/3

H_PROCHOT# 6,25,29,30
PROCHOT_EC
Q34 2N7002K
R295 100K_5%_4

Power auto recovery

+3V_LDO_EC
+3VPCU R273 *0_5%_4
3V_LDO R266 0_5%_4

+3V_LDO_EC
VSTBY_FSPI
+1.8V_S5 R247 0_5%_4
1.8V_LDO R257 *0_5%_4
R232 *0_5%_4

680_LDO R254 *S_4 3V_LDO

Modify 12/16 B-Test mount

680_LDO
20 mils
U12
VIN VOUT GND EN NC
1.8V_LDO
SPIVCC_ON R271 0_5%_4
R276 *0_5%_4
S5_ON
C208 *G9090-180T11U 2.2u/6.3V_4
C223 1u/6.3V_4

Battery B/I SW

To battery B/I pin

25 BI#

Battery disable wher shell opened

NDT016-G1A-KKKT SW2

+3V_RTC +3VPCU
R367 *0_5%_4 R368 *0_5%_4
R382 *10K_5%_4
C324 *0.1u/16V_4
WRST#
R356 100K_5%_4
BI_GATE
Q24 PJA138K
C313 0.1u/25V_4
SW3 TME-533B-Q-T/R
Q23A Q23B PJ4N3KDW
Reset Battery

Vgs = 1.5V
Vgs = 1.5V

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KBC IT8987CX
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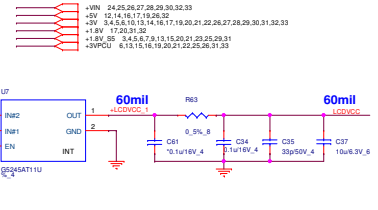
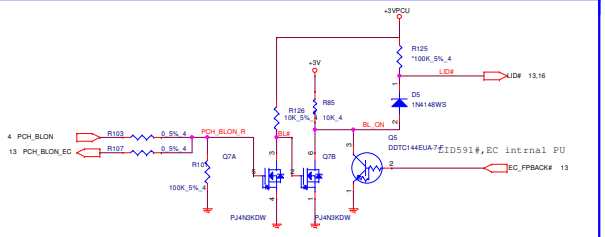
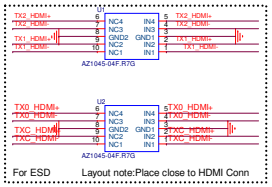
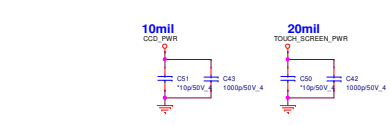
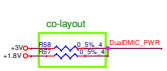
EDP Conn.





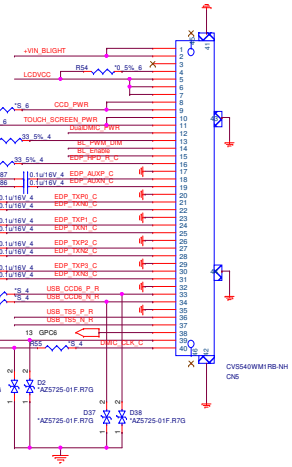


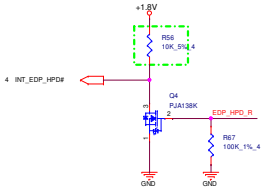


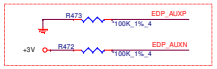


Touch screen

CCD



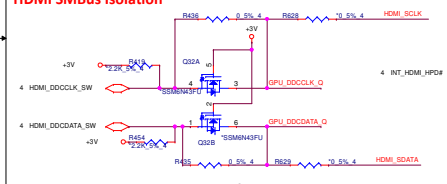




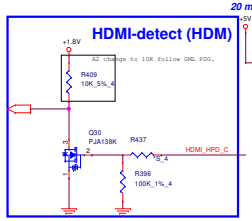
2nd source:DFHS40FS150

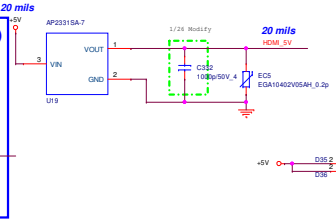
HDMI Conn.

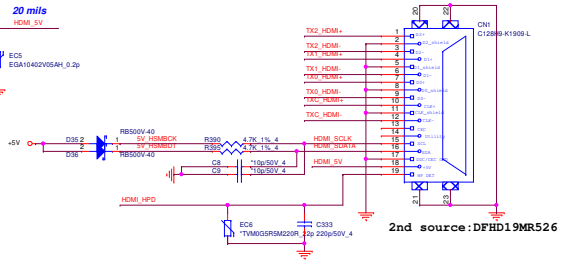
HDMI SMBus Isolation



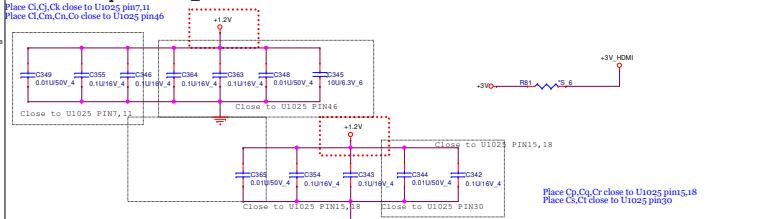
Intel Requesrt Rds_ON <3.5ohm

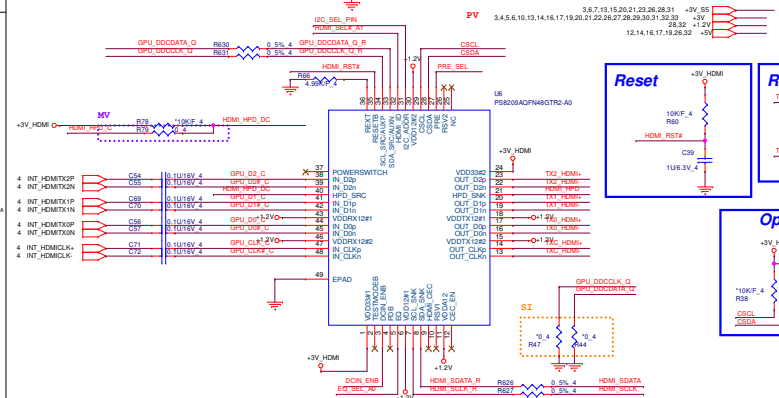


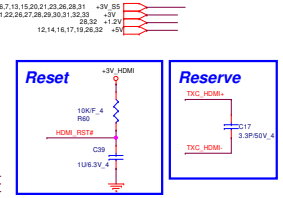


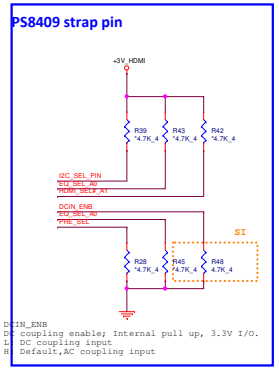


2nd source:DFHD19MR526









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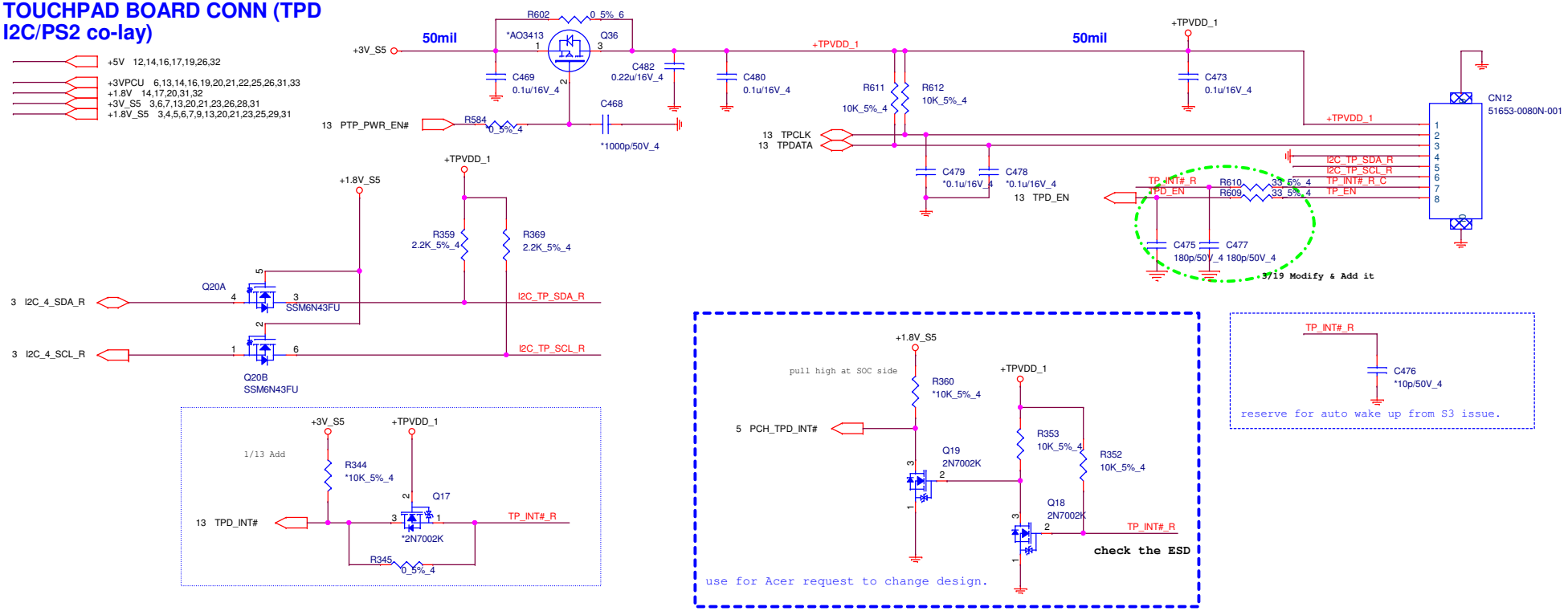
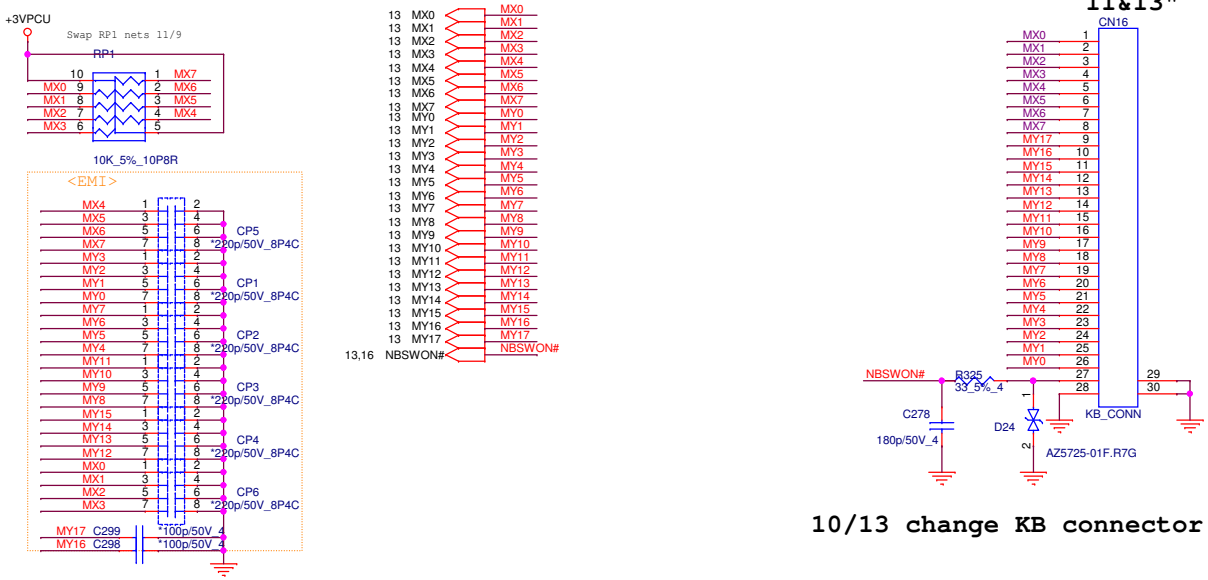
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



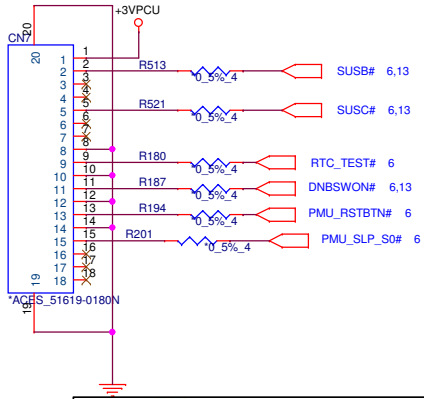
KEYBOARD (KBC)



SWAP KB nets 10/21

10/13 change KB connector

Intel APS Fixture use



Quanta Computer Inc.

PROJECT : ZHE/ZSG

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A
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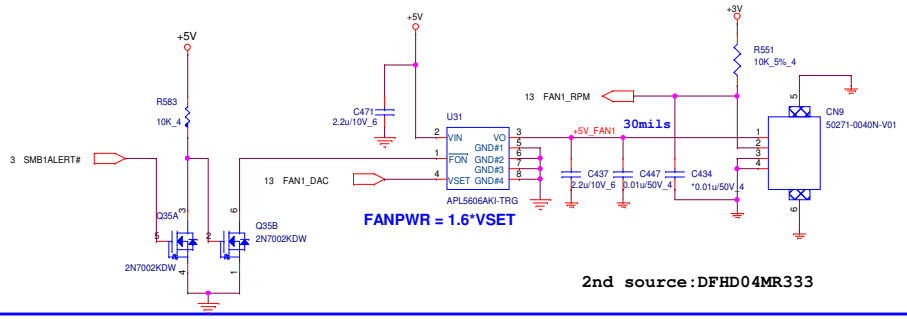
CPU FAN CTRL(THM)

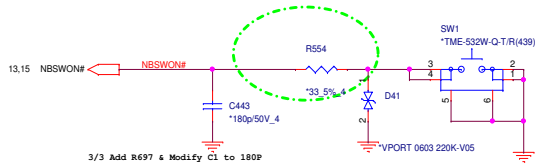


FANPWR = 1.6*VSET

2nd source:DFHD04MR333

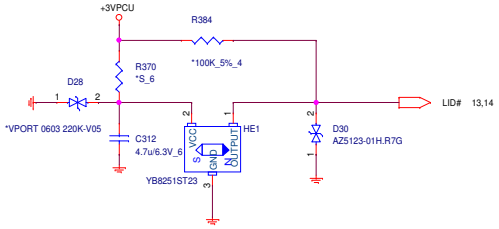
Power Switch. (FSW)

move NBSWON# pull up at page13



3/3 Add R697 & Modify C1 to 180P

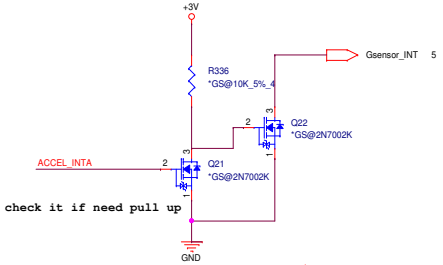
Hall Sensor (HSR)



1st : AL008251007-- YBT
2nd : AL008251000 -- YBT
3rd: AAL008132004- ANC

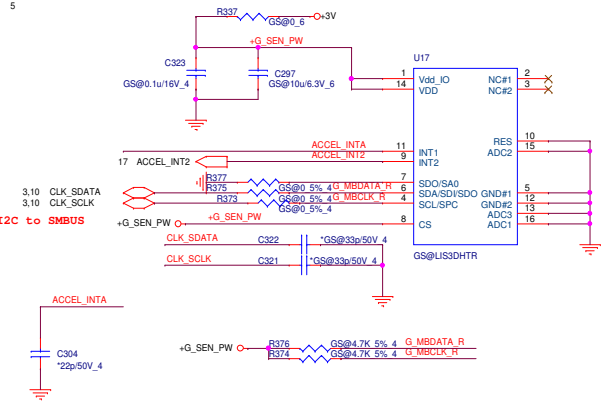
G-sensor(GRS)

G Sensor INT



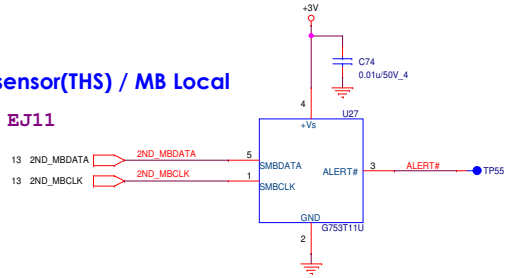
check it if need pull up

11/20 Change from I2C to SMBUS



CPU Thermal sensor(THS) / MB Local TEMP (THM)

For EJ11



Quanta Computer Inc.
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	FAN/BSW/THM/HSR	1A
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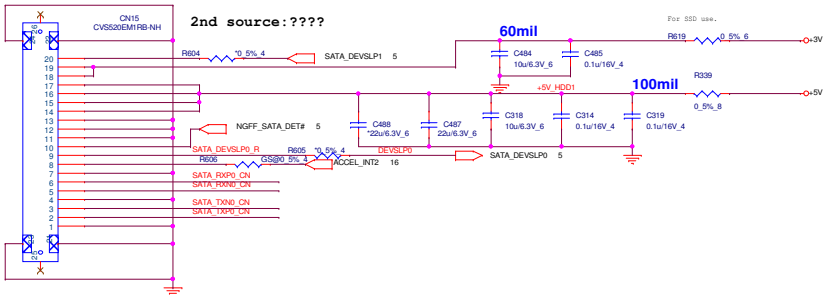
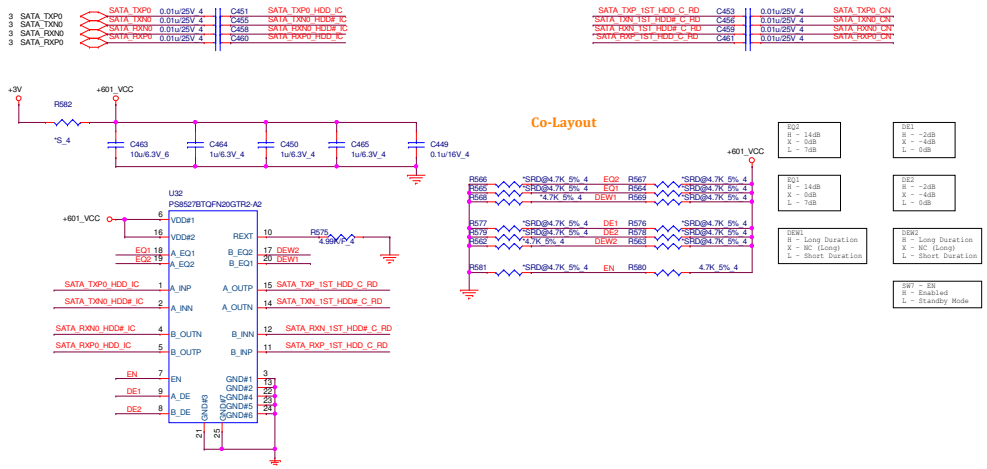
SATA HDD

Cable Type
MAIN SATA HDD



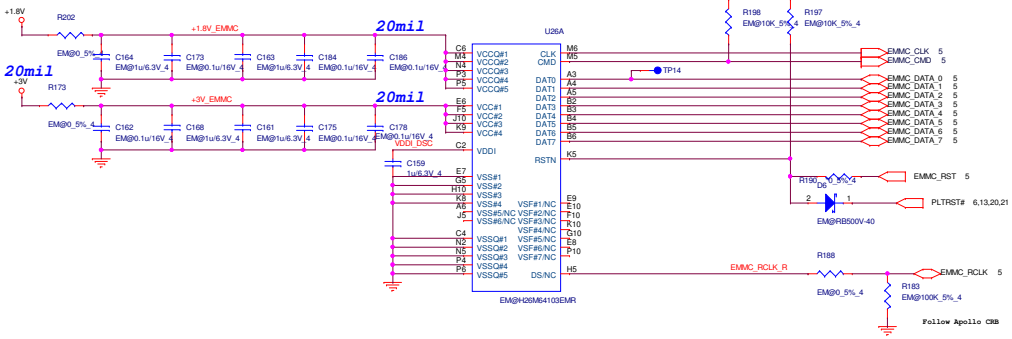
HDD1 SATA Re-driver

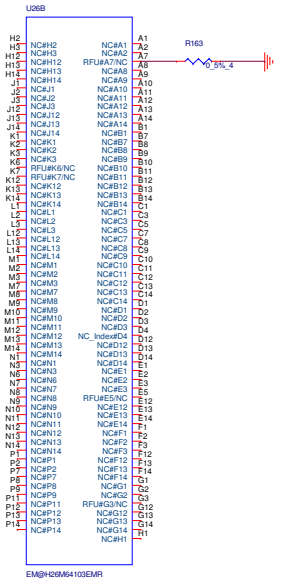


eMMC

Density	eMMC P/N	Vender
32GB	AKE3SZ-TW09	Hynix
		Samsung
64GB	AKE3TZ-TW00	Hynix
	AKE3UZFT502	Samsung

20mil





Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	SATA HDD/SATA REDRIVER	1A

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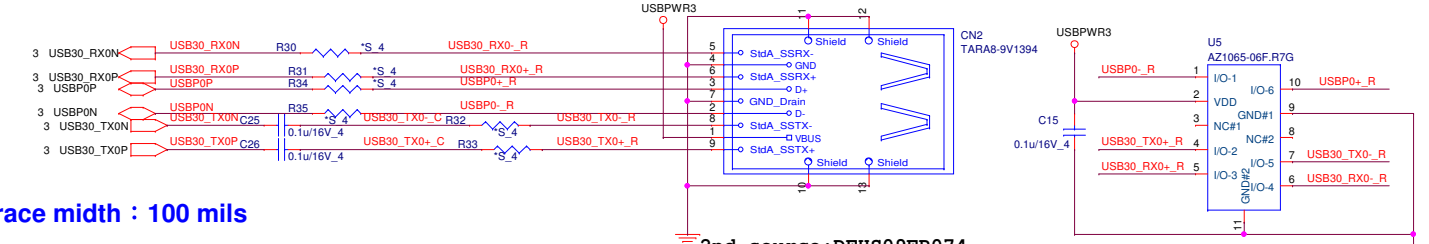
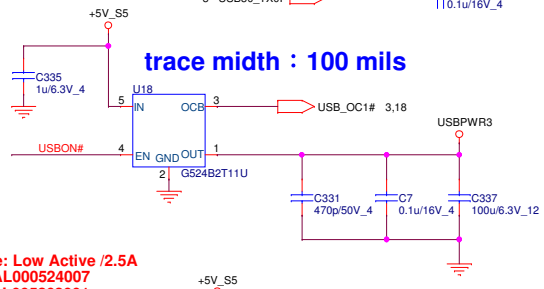
+3V_S5 3,6,7,13,15,20,21,23,26,28,31
+3V 3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,30,31,32,33
+5V_S5 6,24,26,28,29,30,33

Back

10/22 change footprint

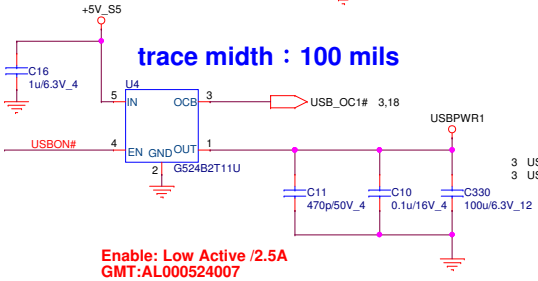


2nd source:DFHS09FR074



trace midth：100 mils

Enable: Low Active /2.5A
GMT:AL000524007
EMS:AL005203001

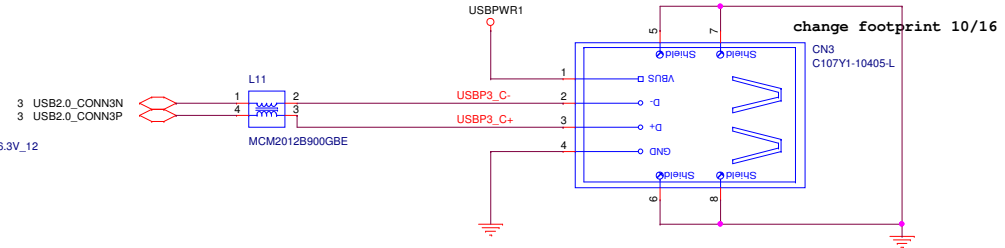


trace midth：100 mils

Enable: Low Active /2.5A
GMT:AL000524007
YBT:AL001901007

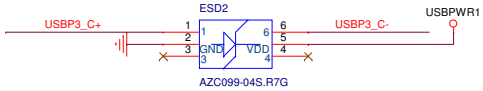
USB 2.0 Port0

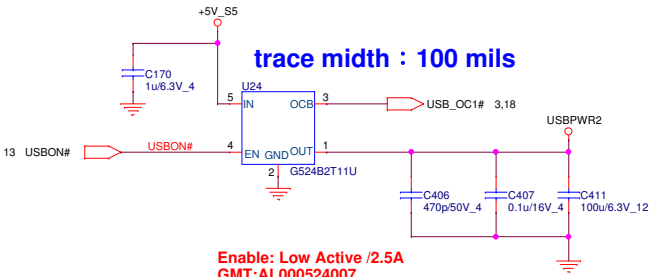
change footprint 10/16



2nd sourceDFHS04FR789

10/22 change footprint

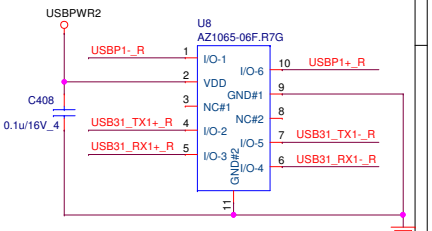




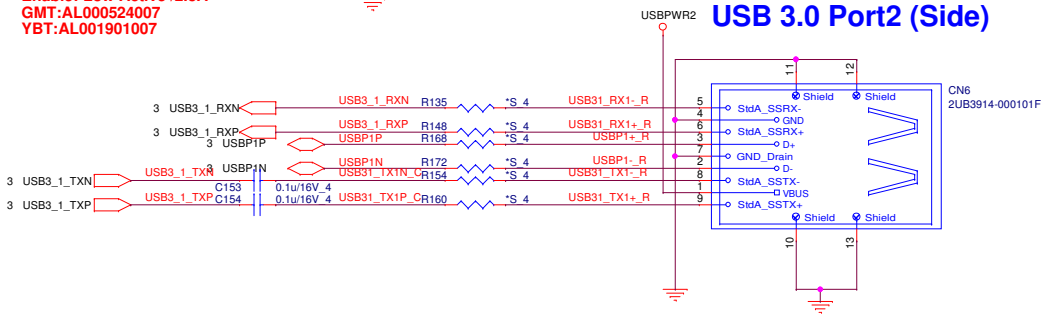
trace midth：100 mils

Enable: Low Active /2.5A
GMT:AL000524007
YBT:AL001901007

USB 3.0 Port1



USB 3.0 Port2 (Side)



2nd source:DDFHS09FR920

Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	USB CONN/USB HUB	1A
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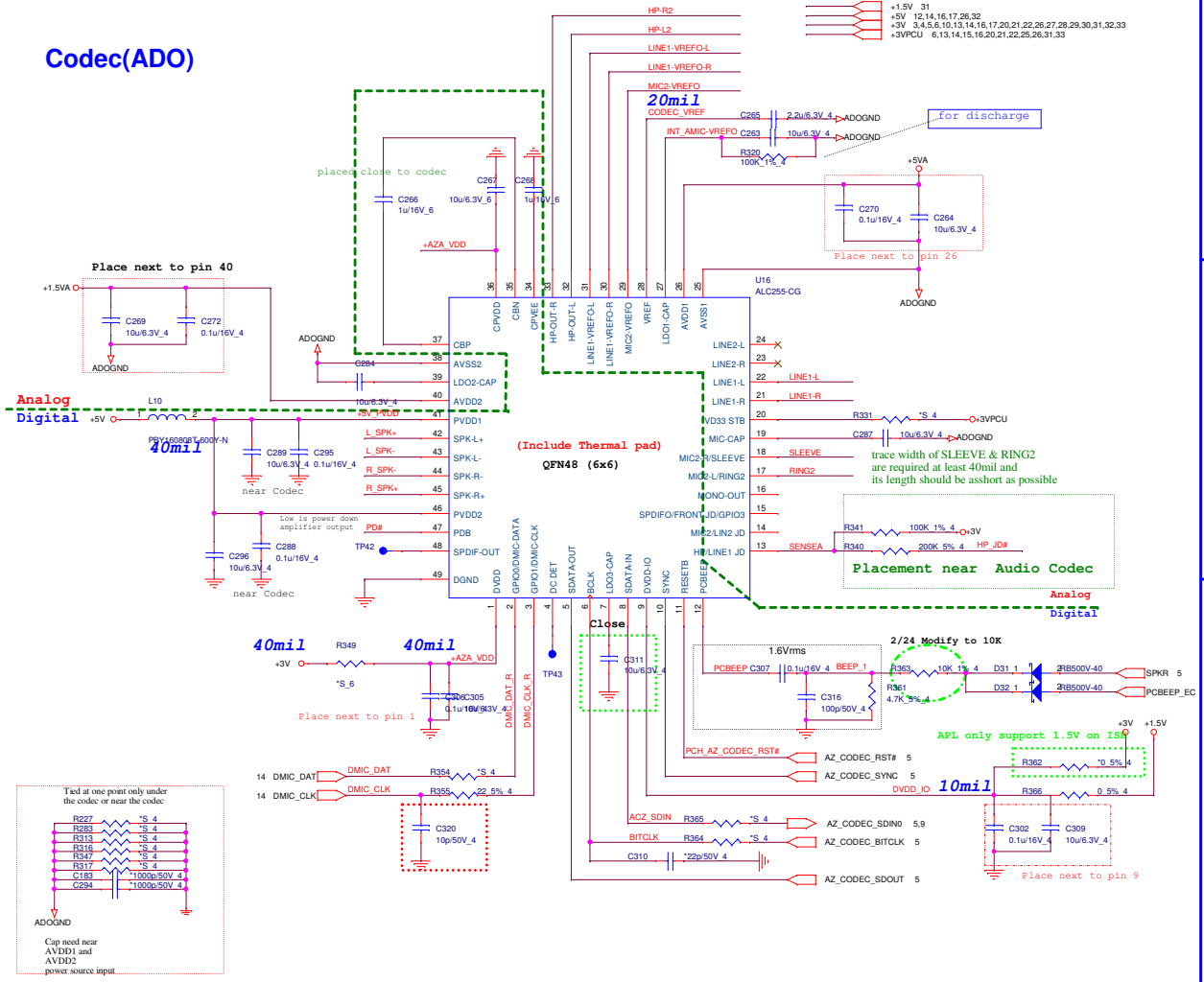
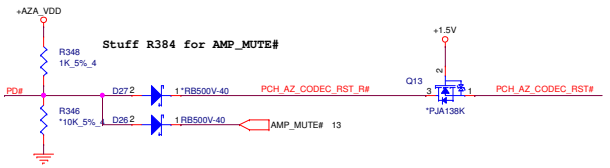
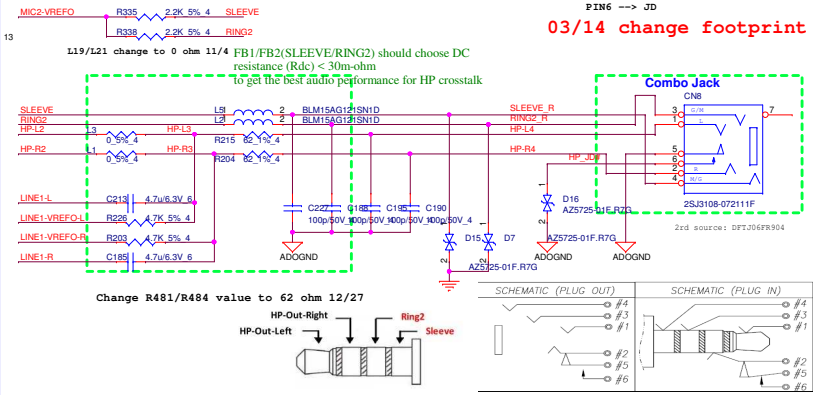
Codec(ADO)



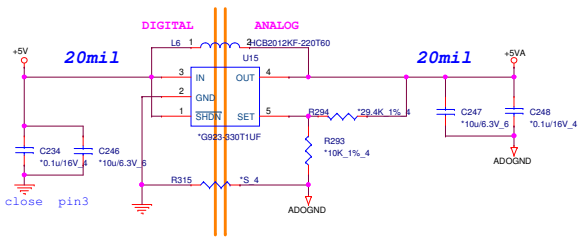
Mute(ADO)



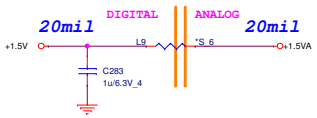
HEADPHONE/MIC/LINE combo (ADO)



Codec PWR 5V(ADO)



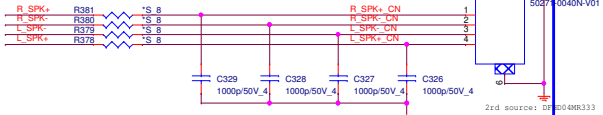
Codec PWR 1.5V(ADO)



Internal Speaker

PE Request CN16 12/25 change footprint

40mil for each signal



Place these EMI components next to codec
2016/01/19 SMT request change to CH21006JB10

A-Mic

Quanta Computer Inc.

PROJECT : ZHE/ZSG

Size	Document Number	Rev
	Codec ALC225	1A

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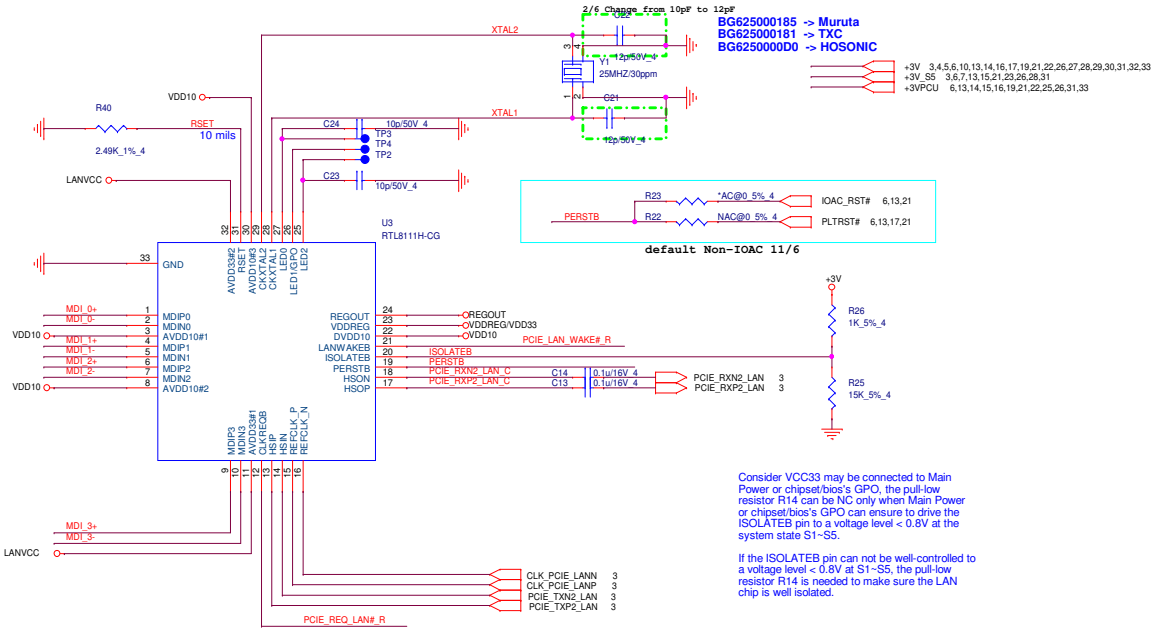
LAN

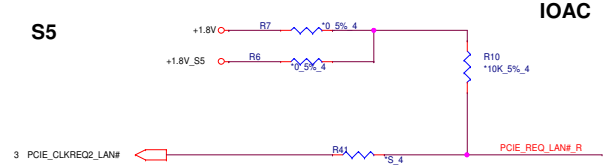


default Non-IOAC 11/6

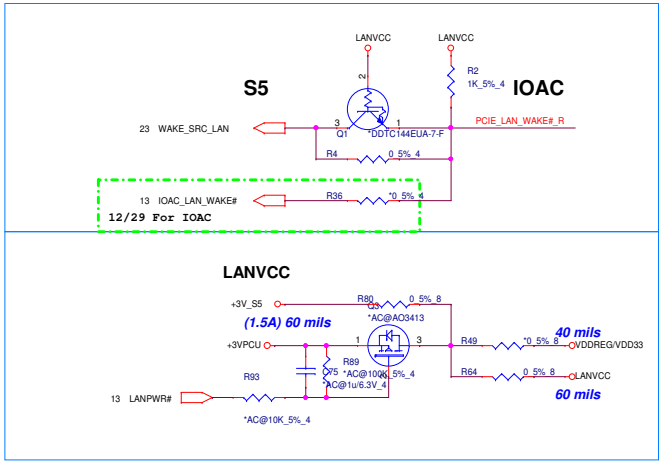
Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

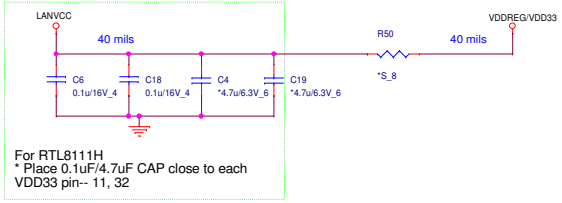
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

S5

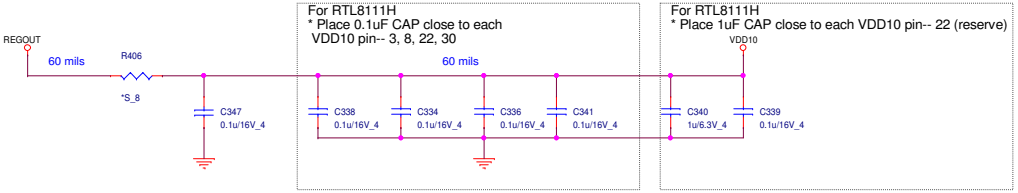


Modify Level Shift circuit 03/22



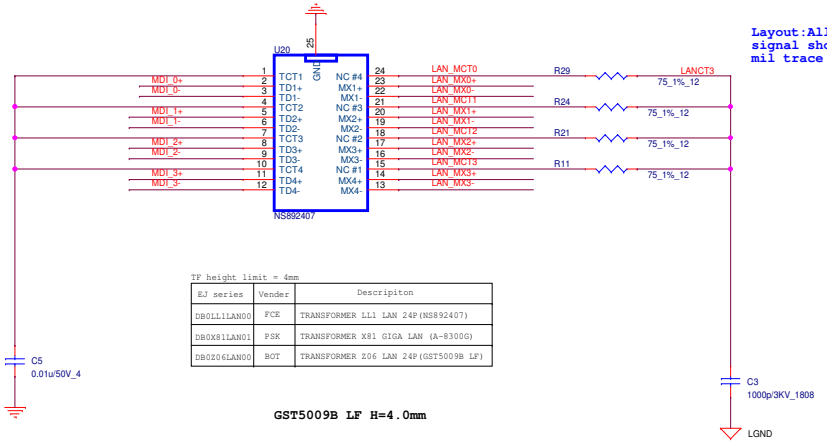


For RTL8111H
* Place 0.1uF/4.7uF CAP close to each VDD33 pin-- 11, 32



Tramsformer

Change footprint from "ssop24-11-1" to "trf-n1010g-25p" 11/21



Layout:All termination signal should have 30 mil trace

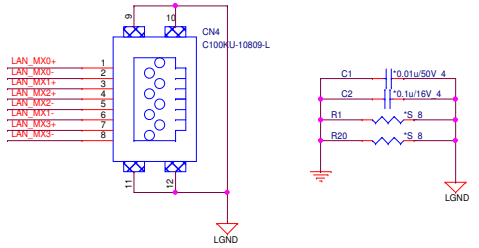
TF height limit = 4mm

EJ series	Vender	Descripiton
DB0LL1LAN00	FCE	TRANSFORMER LL1 LAN 24P(NS892407)
DB0X81LAN01	PSK	TRANSFORMER X81 GIGA LAN (A-8300G)
DB0Z06LAN00	BOT	TRANSFORMER Z06 LAN 24P(GST5009B LF)

GST5009B LF H=4.0mm

RJ45 Connector

Change footprint 10/19



Quanta Computer Inc.		
PROJECT : ZHE/ZSG		
Size	Document Number: LAN	Rev: 1A
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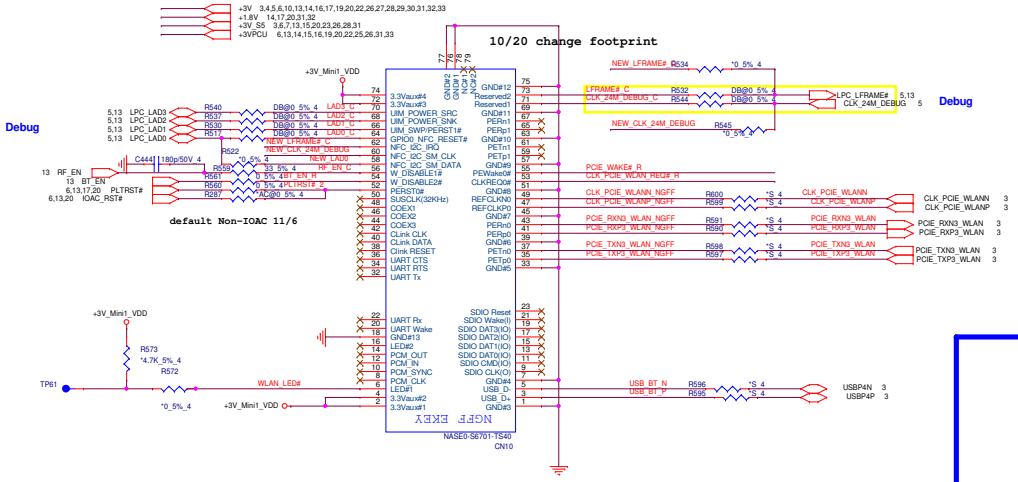
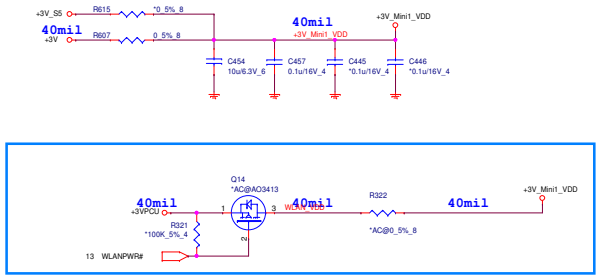
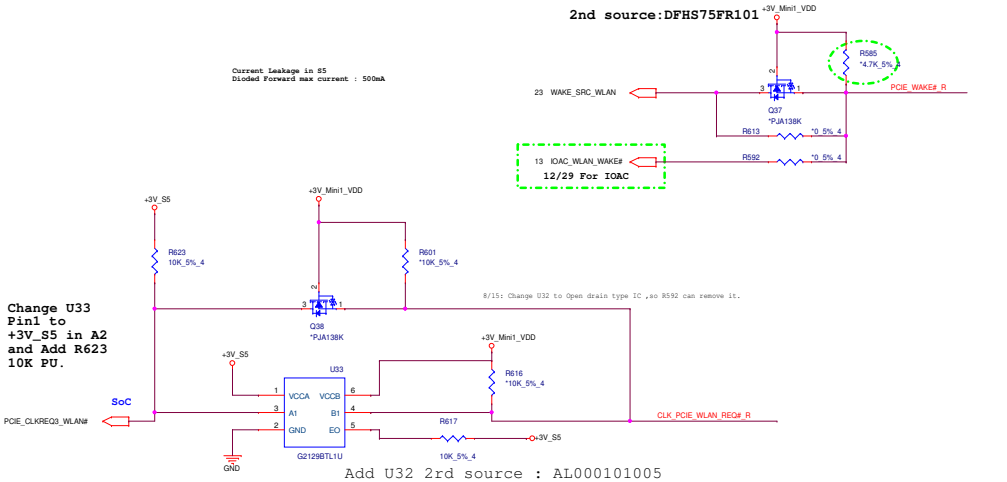
WLAN

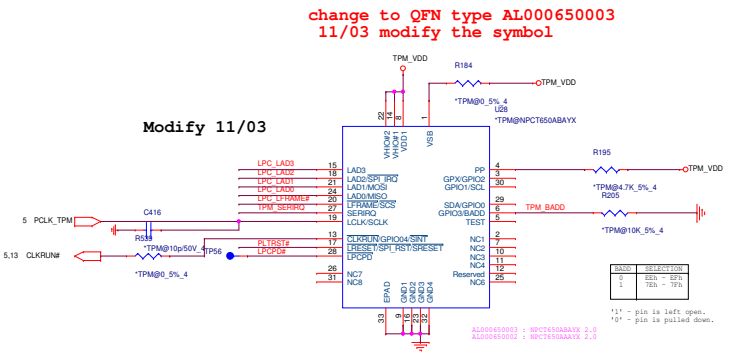


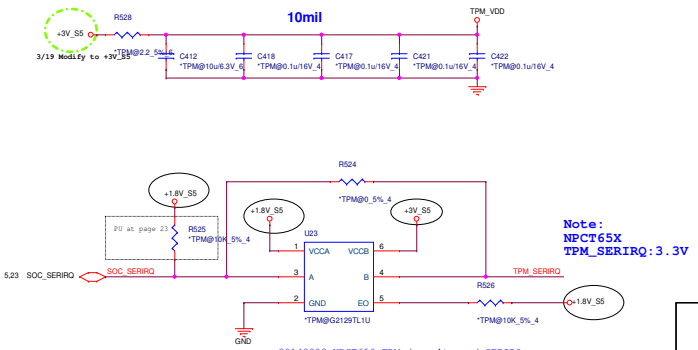


MINI PCI-E



TPM (TPM)





Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	WiFi & BT & TPM	1A
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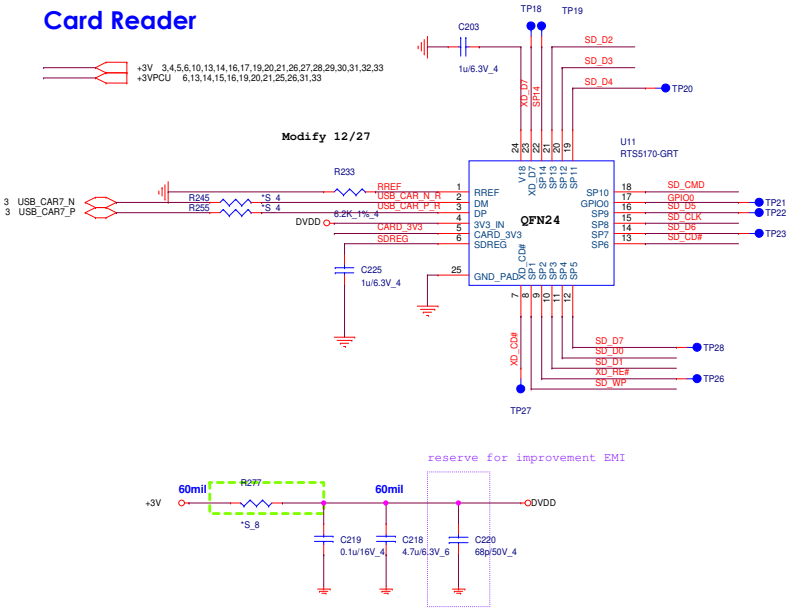
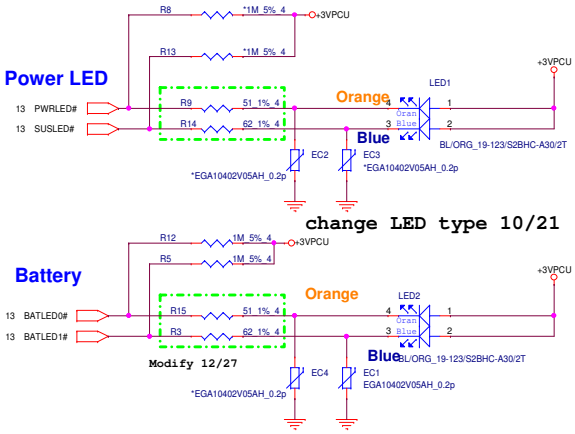
Card Reader

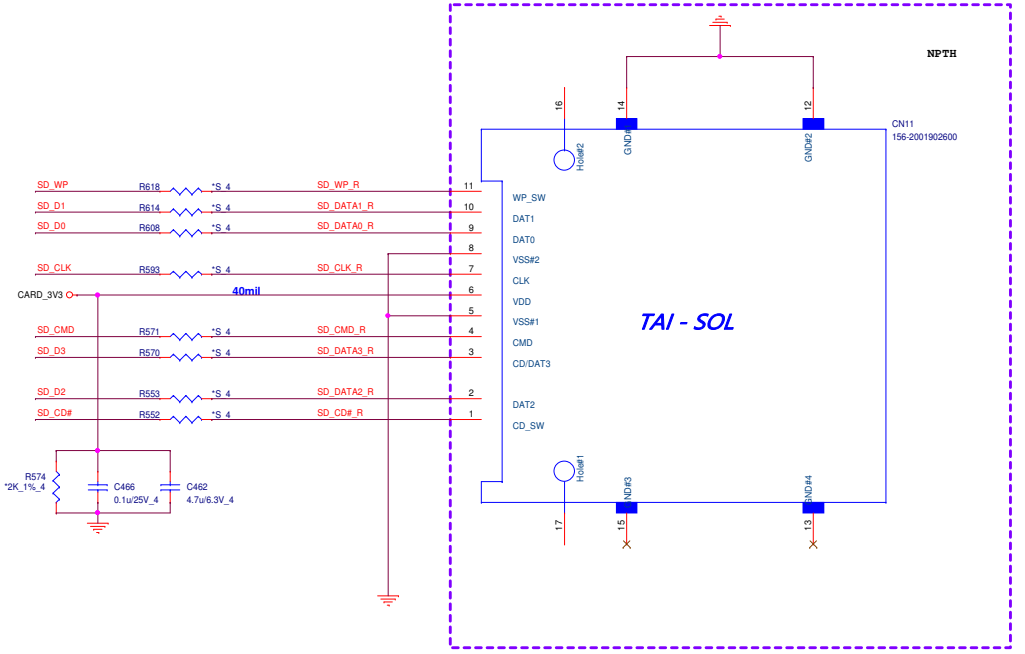


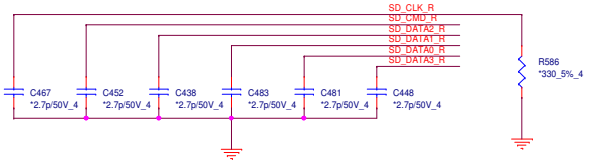
LED(UIF)



SD/MMC CARD READER (MMC)

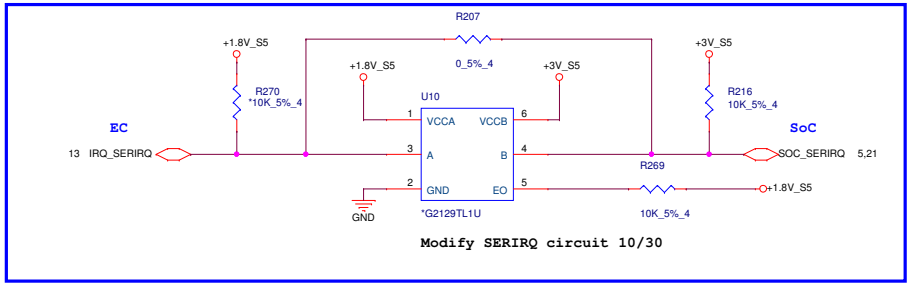
10/19 change footprint
11/5 change CR connector symbol

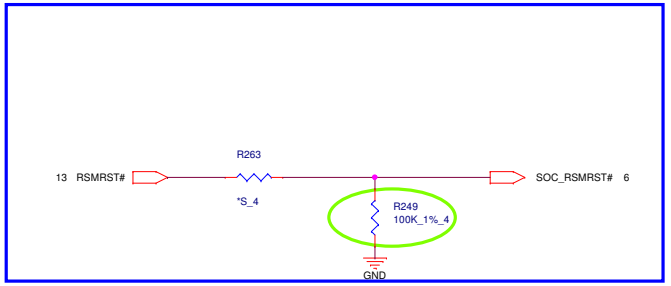




Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	D/B Board Connector	1A
Date: Wednesday, December 27, 2017	Sheet 22 of 37	

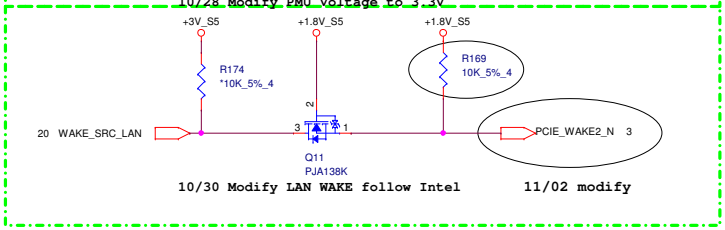


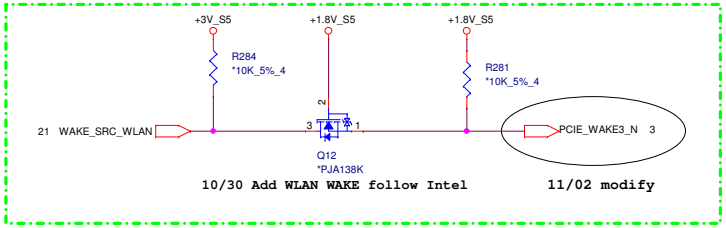


+3V_S5 3,6,7,13,15,20,21,26,28,31
+3V 3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,30,31,32,33
+1.8V_S5 3,4,5,6,7,9,13,15,20,21,25,29,31

Del PCH_SUS_STAT# level shift to EC 10/28

10/28 Modify PMU Voltage to 3.3V





Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	Level Shift	1A

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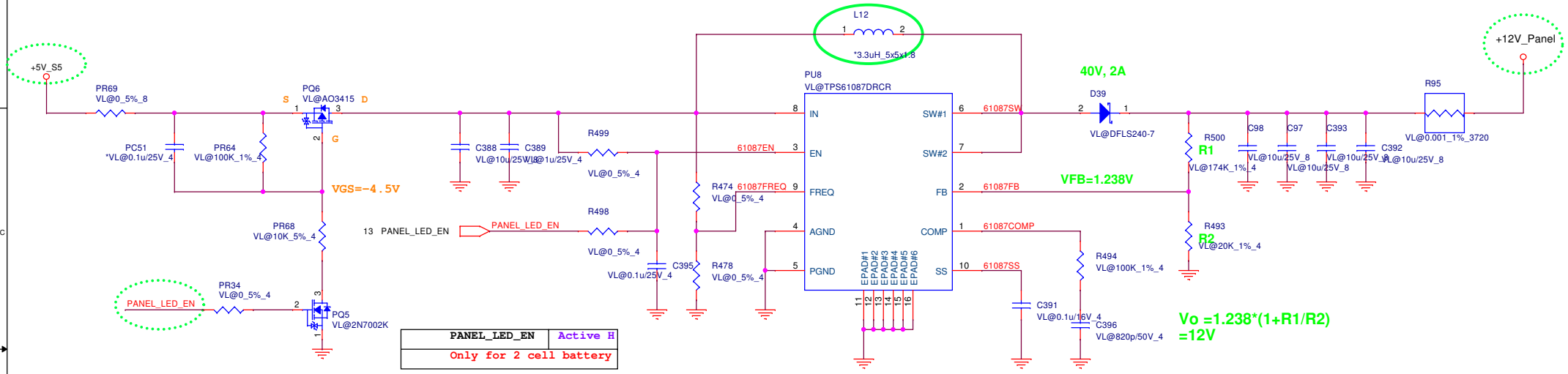
Panel Spec (TFT-LCD 14")
VLED : 6V~21V (Tpy:12V)
Power Consumption : 3W (MAX)

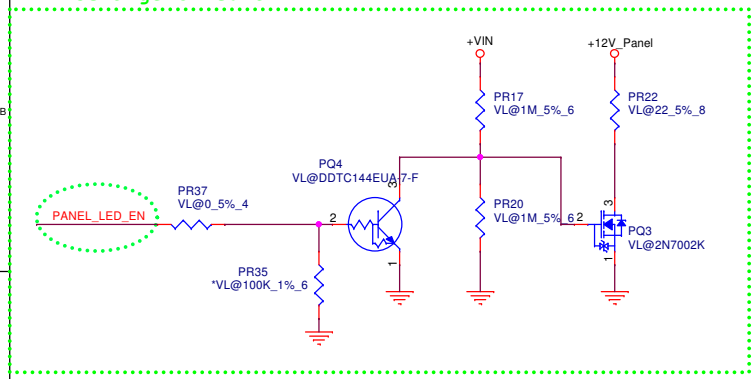
+12V_Panel
12 Volt +/- 5%
PEAK : 0.35A
Width : 20mil

6,18,26,28,29,30,33 +5V_S5
14 +12V_Panel



PANEL_LED_EN	Active H
Only for 2 cell battery	

BL Discharge Circuit

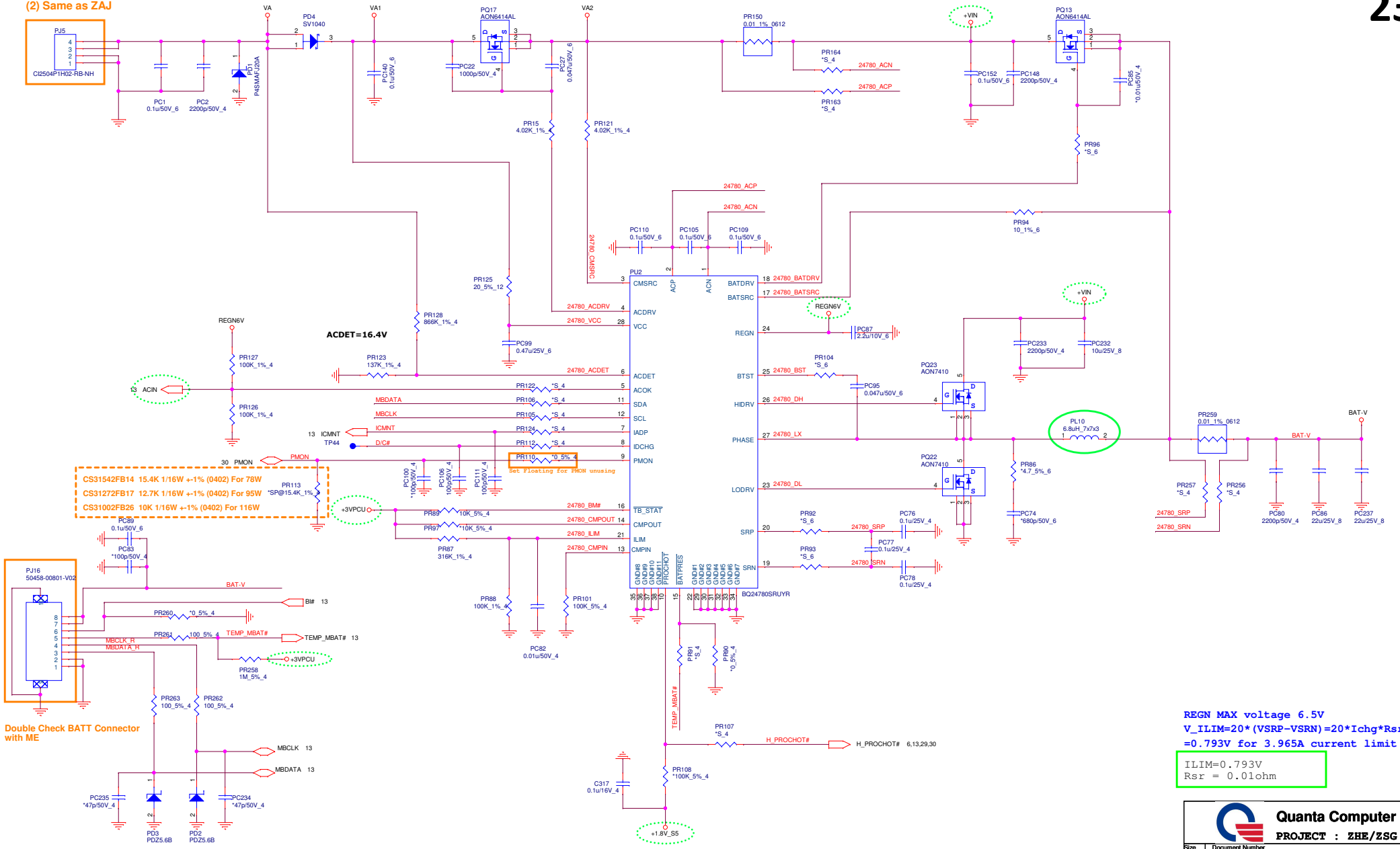


Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	DC-DC	1A
Date: Wednesday, December 27, 2017	Sheet 24 of 37	

(1) Double Check ADP-IN Connector with ME

(2) Same as ZAJ



REGN MAX voltage 6.5V

V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr

=0.793V for 3.965A current limit

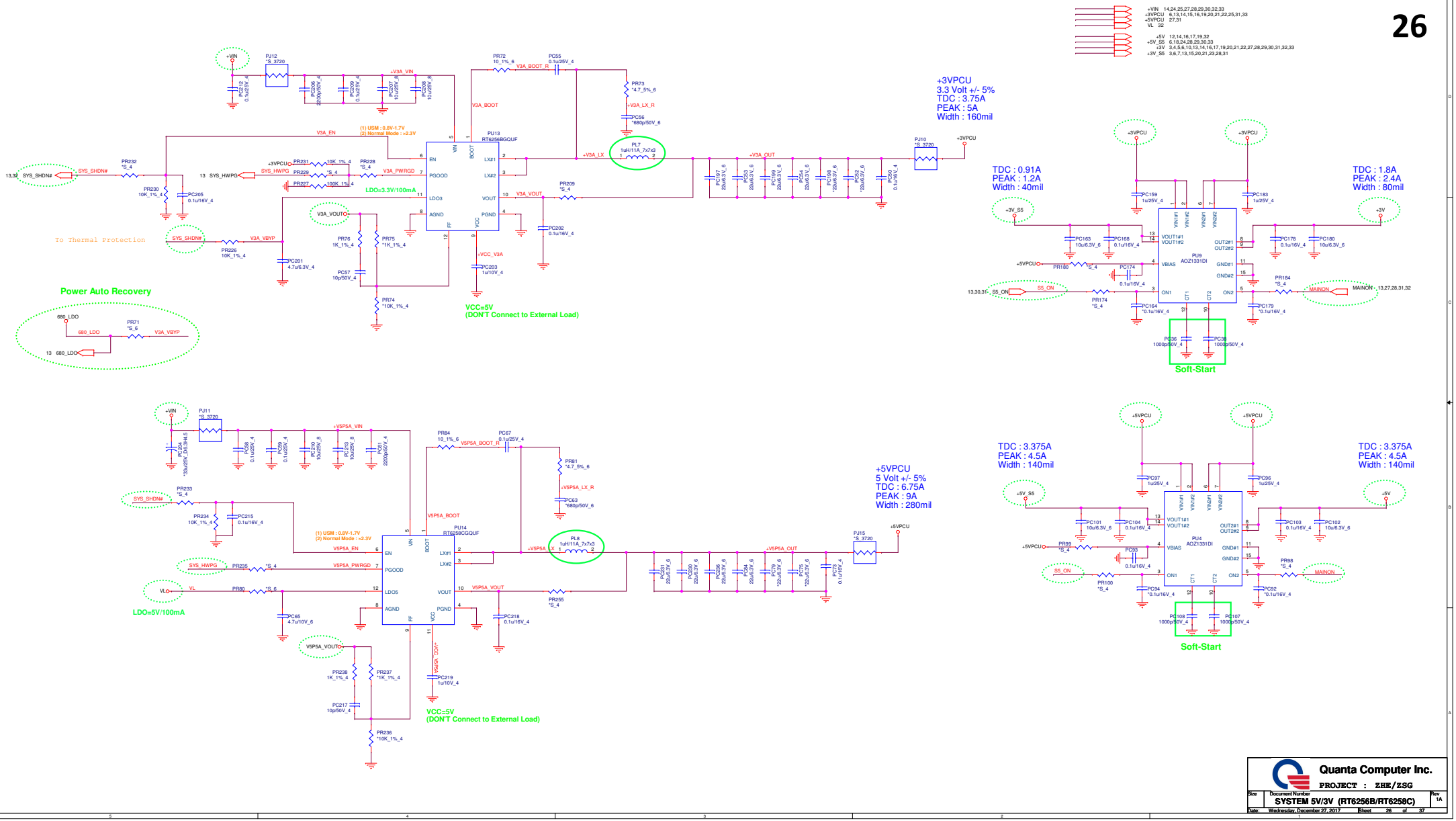
ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.

PROJECT : ZHE/ZSG

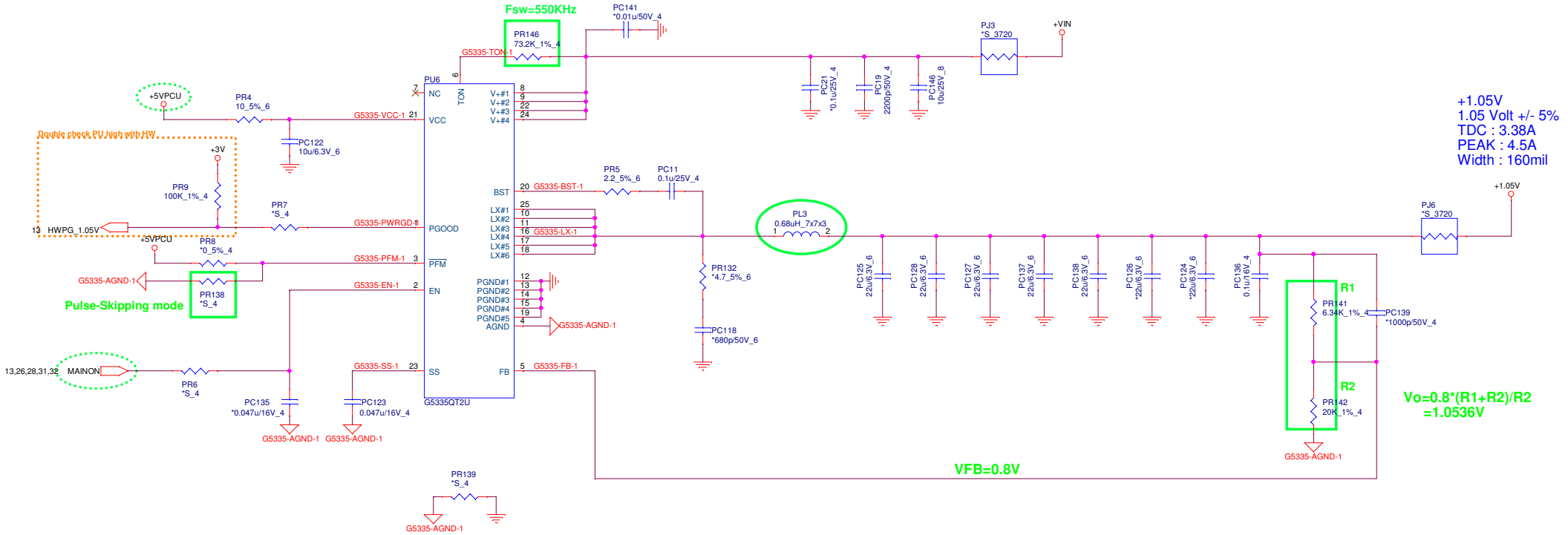
Size	Document Number	Rev
	Charger (BQ24780S)	1A

Date: Wednesday, December 27, 2017 Sheet 25 of 37



Quanta Computer Inc.			
PROJECT : ZHE/ZSG			
Size	Document Number		Rev
	SYSTEM 5V/3V (RT6256B/RT6258C)		1A
Date: Wednesday, December 27, 2017	Sheet 26 of 37		

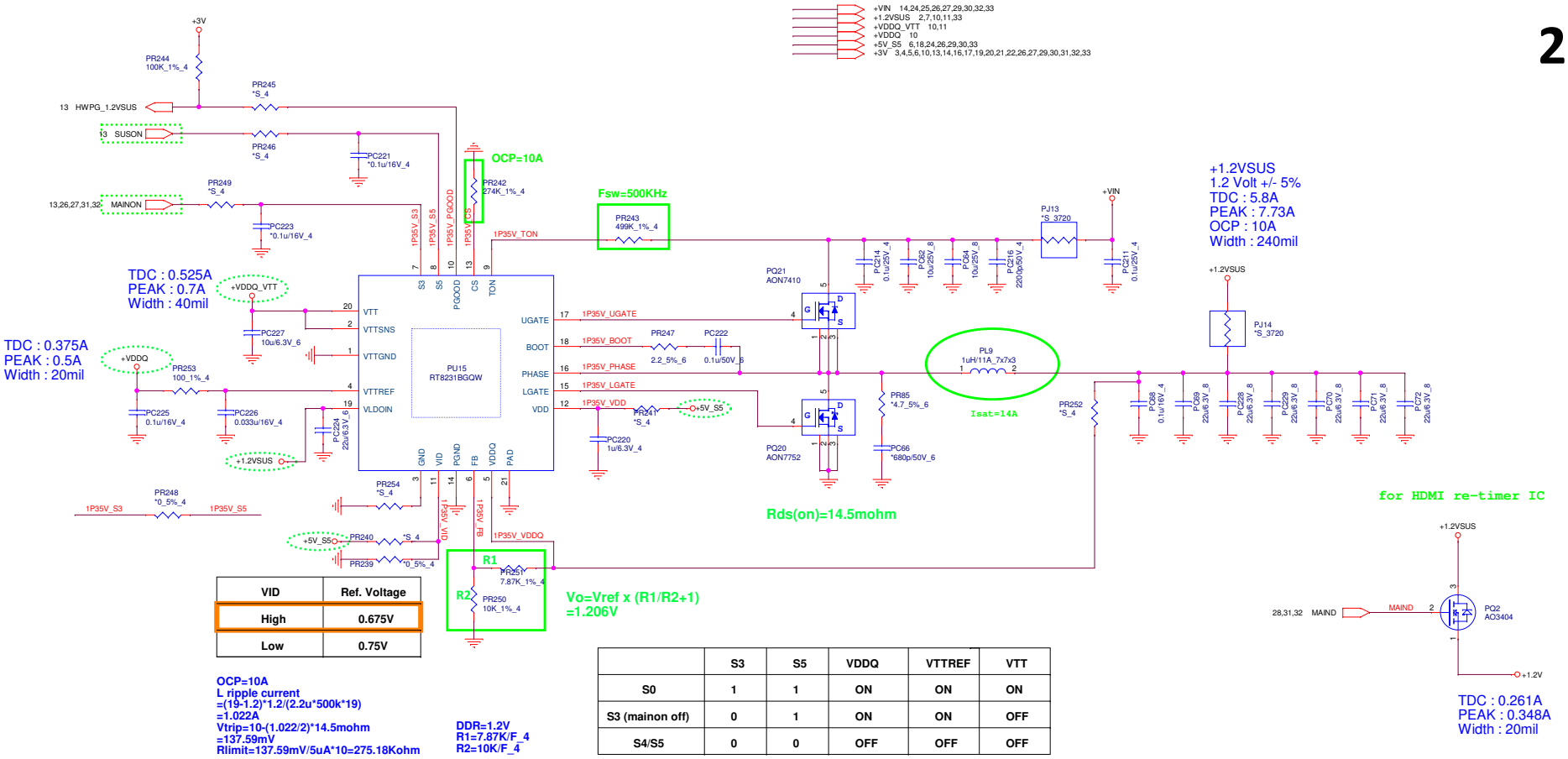
+VIN 14,24,25,26,28,29,30,32,33
+1.05V 6,7,29,30
+5VPCU 26,31
+3V 3,4,5,6,10,13,14,16,17,19,20,21,22,26,28,29,30,31,32,33



+1.05V
1.05 Volt +/- 5%
TDC : 3.38A
PEAK : 4.5A
Width : 160mil

Quanta Computer Inc.
PROJECT : ZHE/ZSG

Size	Document Number	Rev
	+1.05V (G5335QT2U)	1A
Date: Wednesday, December 27, 2017	Sheet 27 of 37	



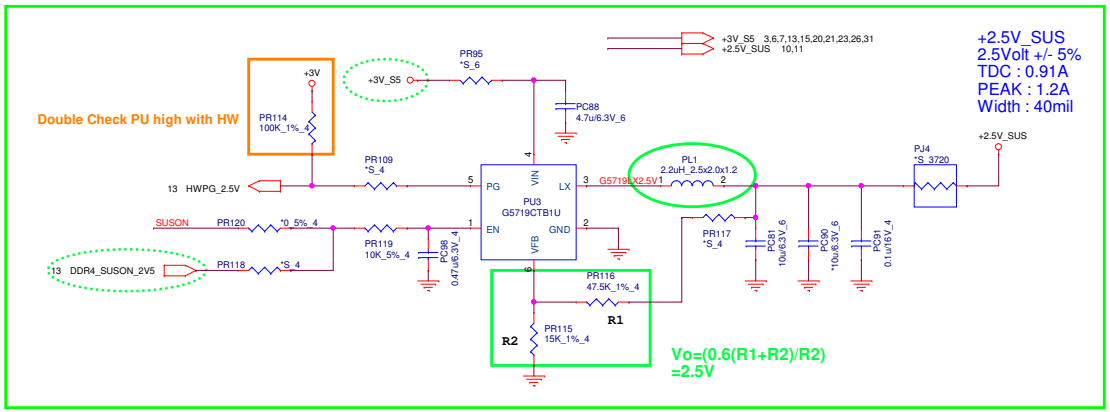
VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

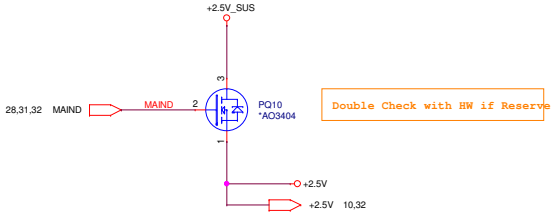
OCP=10A
L ripple current
=(19-1.2)*1.2/(2.2u*500k*19)
=1.022A
Vtrip=10-(1.022/2)*14.5mohm
=137.59mV
Rlimit=137.59mV/5uA*10=275.18Kohm

DDR=1.2V
R1=7.87K/F_4
R2=10K/F_4

+2.5VSUS Power Rail For DDR4

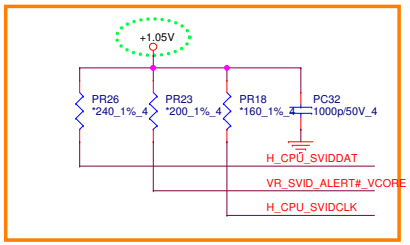


Reserve +2.5V for DDR4 VDDSPD



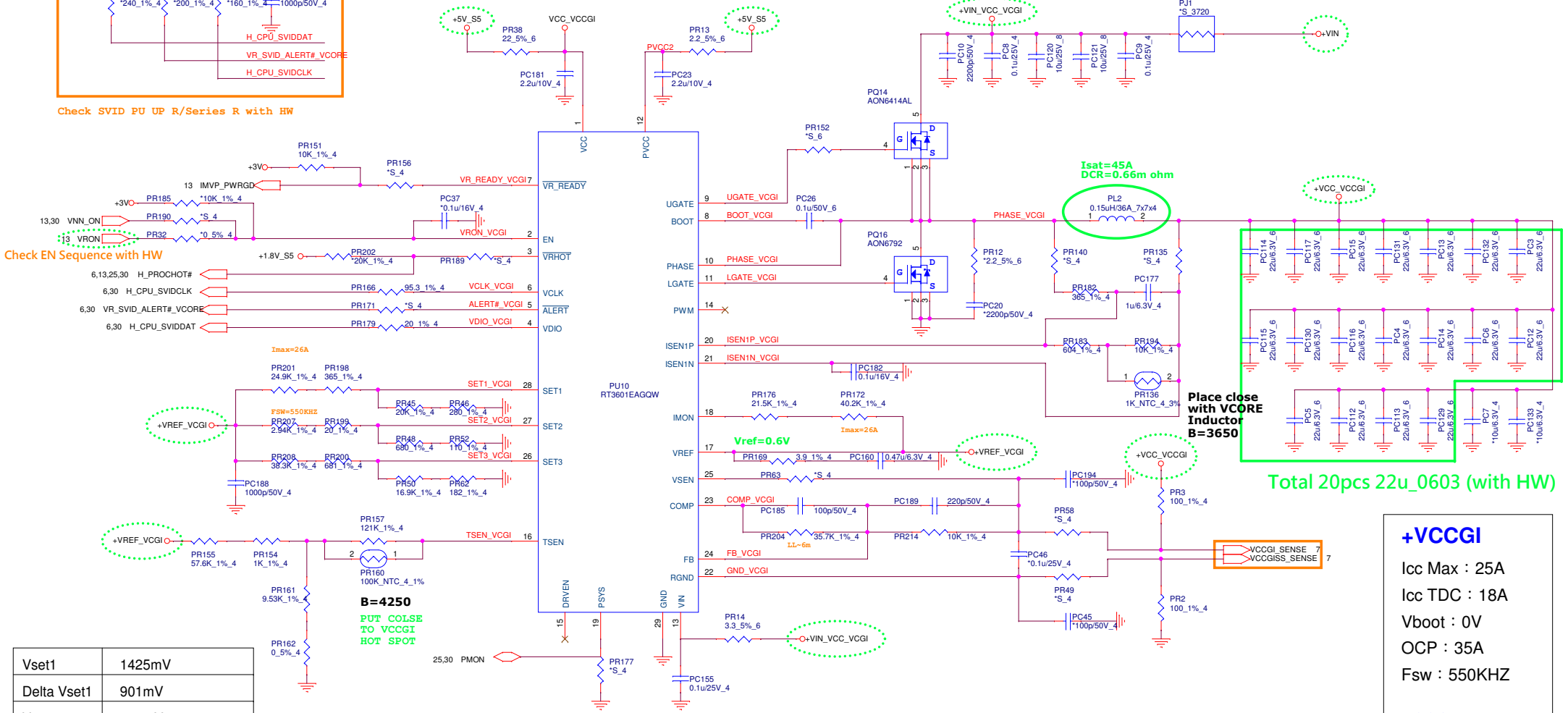
Quanta Computer Inc.				
PROJECT : ZHE/ZSG				
Size	Document Number			Rev
	DDR4 (RT8231BGQW)			1A
Date: Wednesday, December 27, 2017		Sheet 28 of 37		

SVID_CLK : UP:324 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:475 ohm Series:20 ohm



Check SVID PU UP R/Series R with HW

+VIN 14,24,25,26,27,28,30,32,33
+VCC_VCCGI 7
+3V 3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,30,31,32,33
+5V_S5 6,18,24,26,28,30,33
+1.8V_S5 3,4,5,6,7,9,13,15,20,21,23,25,31
+1.05V 6,7,27,30



Total 20pcs 22u_0603 (with HW)

Vset1	1425mV
Delta Vset1	901mV
Vset2	675mV
Delta Vset2	49.8mV
Vset3	974mV
Delta Vset3	950mV
VTsen	448mV

+VCCGI

Icc Max：25A
Icc TDC：18A
Vboot：0V
OCP：35A
Fsw：550KHZ

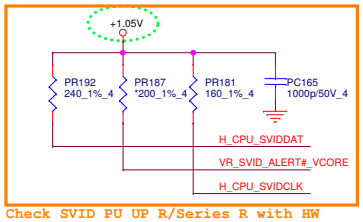
VCCGI L/L :
R_DC_LL：6mV/A
R_AC_LL：6mV/A

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	+VCC_VCCGI (RT3601EAGQW)	1A

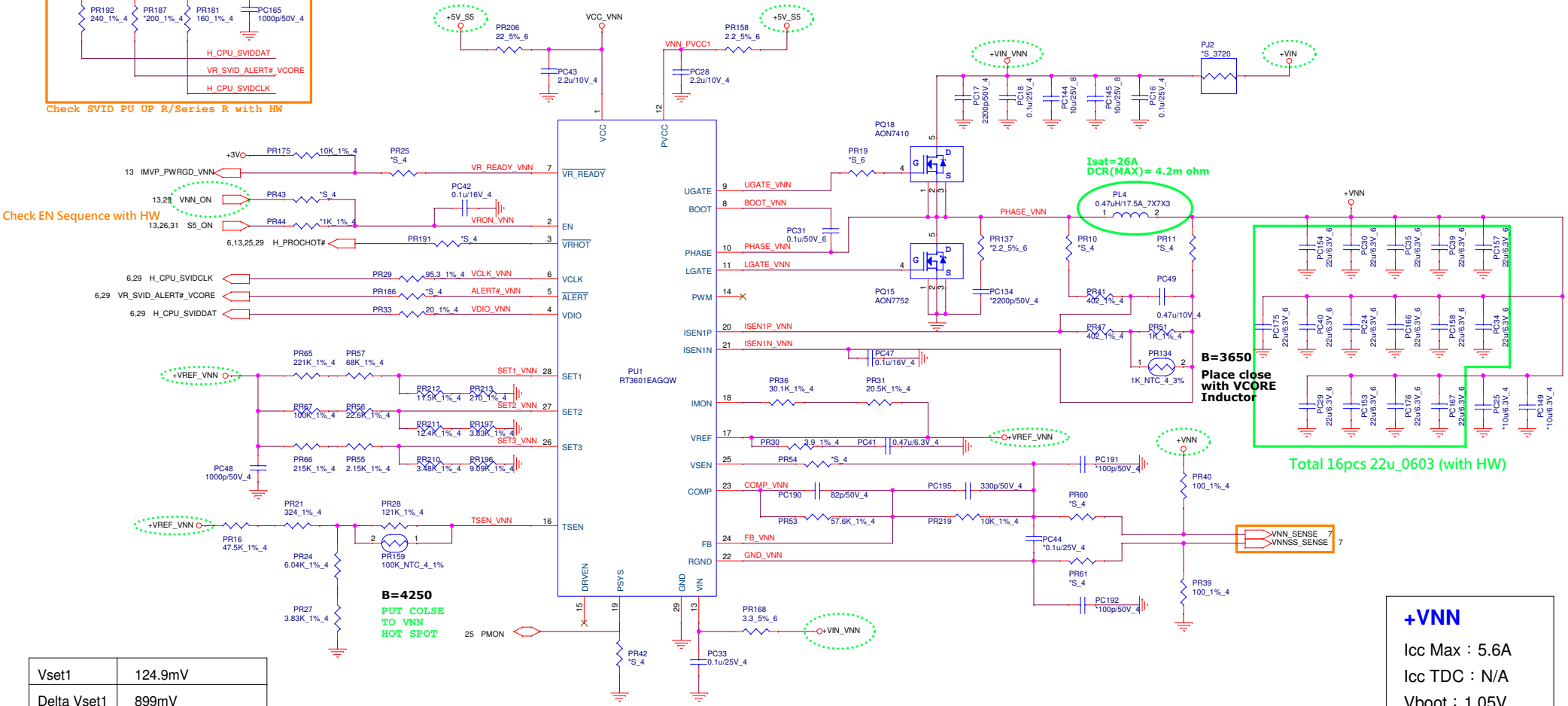
Date: Wednesday, December 27, 2017 Sheet 29 of 37

SVID_CLK : UP:324 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:475 ohm Series:20 ohm



Check SVID PU UP R/Series R with HW

+VIN 14,24,25,26,27,28,29,32,33
+VNN 7
+5V_S5 6,18,24,26,28,29,33
+1.05V 6,7,27,29
+3V 3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,31,32,33



Vset1	124.9mV
Delta Vset1	899mV
Vset2	373.4mV
Delta Vset2	1.14V
Vset3	176mV
Delta Vset3	950mV
VTsen	548mV

+VNN

Icc Max：5.6A
Icc TDC：N/A
Vboot：1.05V
OCP：10A
Fsw：600KHZ

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6,13,14,15,16,19,20,21,22,25,26,33 +3VPCU
3,4,5,6,7,9,13,15,20,21,23,25,29 +1.8V_S5
7 +1.24V_S5
14,17,20,32 +1.8V
19 +1.5V

3,6,7,13,15,20,21,23,26,28 +3V_S5
26,27 +5VPCU
3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,30,32,33 +3V

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.85A
PEAK : 1.13A
Width : 40mil

ZHP change +1.8V_S5 PG pull up to +3V_S5

+3V_S5 +3VPCU PR205 *S_6 PC193 4.7u/6.3V_4
PR220 100K_1%_4
PR215 *S_4
13 HWPG_1.8V_S5
13,26,30 S5_ON
PR173 110K_5%_4 PC173 0.1u/16V_4
PU11 G5719CTB1U PG VIN LX EN GND VFB
G5719LX_1.8V PL6 2.2uH_2.5x2.0x1.2
PR221 *S_4
PC172 10u/6.3V_6 PC171 *10u/6.3V_6 PC170 0.1u/16V_4
PJ9 *S_3720 +1.8V_S5

Check RC delay time with HW
(follow ZHE RC dealy time)

R1 PR217 30K_1%_4
R2 PR216 15K_1%_4

Vo=(0.6(R1+R2)/R2
=1.8V

28,32 MAIND MAIND PQ19 AO3404 +1.8V_S5 +1.8V

TDC : 0.173A
PEAK : 0.23A
Width : 20mil

+1.24V_S5
1.24Volt +/- 5%
TDC : 1.875A
PEAK : 2.5A
Width : 80mil

Check PU High Sequence with HW

+3V_S5 PR143 100K_1%_4
PR147 *S_4
13 HWPG_1.24V_S5
5671PG_1.24V
+3VPCU PJ8 *S_3720
PC161 *2200p/50V_4 PR170 *2.2_5%_6
PU7 M5671RE1U POK VIN#1 VIN#2 VCC GND NC#1 SW#1 SW#2 NC#2 FB EN
PL5 1uH_7x7x3
5671LX_1.24V
5671FB_1.24V_S
PC143 *22p/50V_4
5671NC_1.24V PC150 *68p/50V_4
5671FB_1.24V
5671EN_1.24V PR148 *S_4
PC142 *0.1u/16V_4
PR167 10_5%_6
5671SVIN_1.24V
PC162 0.01u/50V_4 PC156 10u/6.3V_6 PC151 1u/6.3V_4
PR144 *S_4
PC147 0.1u/25V_4 PC169 22u/6.3V_6
+1.24V_S5 PJ7 *S_3720
R1 PR145 10K_1%_4
R2 PR149 10K_1%_4
HWPG_1.8V_S5

Vo=0.6*(R1+R2)/R2
=1.24V

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

+3VPCU PR178 *S_8 PC187 10u/6.3V_6 PC194 0.1u/50V_6
13,26,27,28,32 MAINON MAINON PR188 *S_4
PR195 100K_5%_4 PC186 *0.1u/50V_6
PU12 G9661MF11U VIN NC VO VEN VPP POK ADJ GND#1 GND#2
PR225 *S_8 +1.5V
+5VPCU PR222 *S_4 PC196 1u/25V_4
13 HWPG_1.5V +3V PR218 100K_5%_4
PC200 10u/6.3V_6
R1 PR224 30K_1%_4
Vref=0.8V
Vo =0.8(1+R1/R2)
=1.506V
R2 PR223 34K_1%_4

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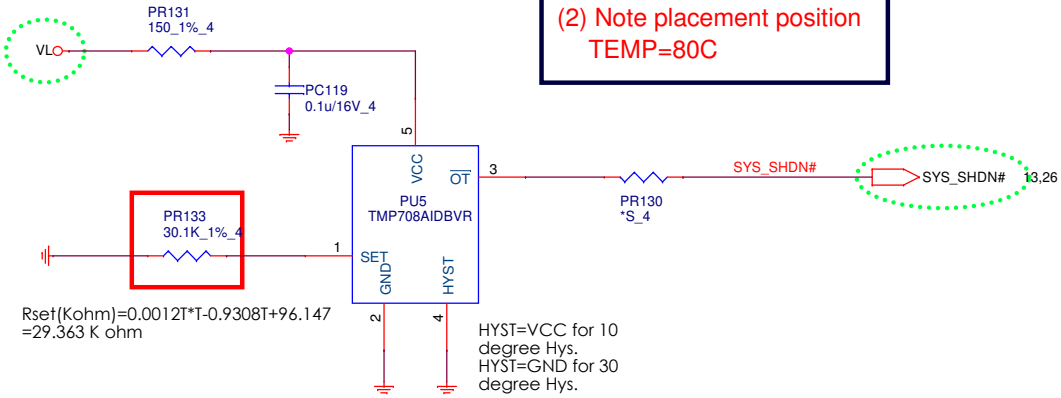
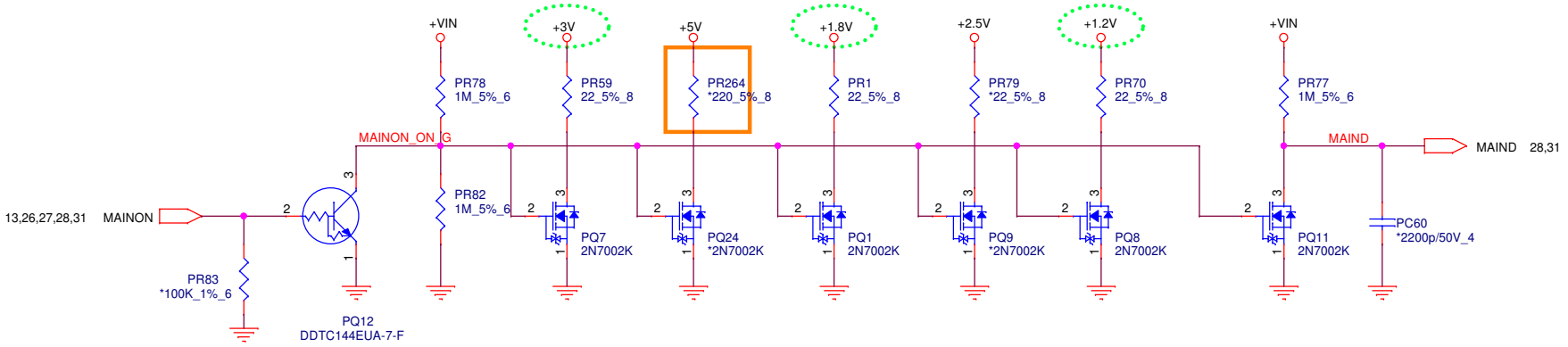
26 VL
14,24,25,26,27,28,29,30,33 +VIN
3,4,5,6,10,13,14,16,17,19,20,21,22,26,27,28,29,30,31,33 +3V
12,14,16,17,19,26 +5V
14,17,20,31 +1.8V
10,28 +2.5V

Thermal Protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C



+5V PU High R= 220 ohm for Bo-Bo sound issue.



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	Thermal / Discharge	1A

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HOLE(OTH)

HOLE15
H-C276D138P2

HOLE16
H-C276D144P2

HOLE13
H-C276D144P2

HOLE7
h-c126d126n

NGFF nuts

CPU Thermal nuts

HOLE8
*HG-C354D126P2

HOLE10
*HG-C276D98P2

HOLE6
*HG-C276D98P2

HOLE9
*HG-ZHP-1

HOLE1
*HG-C276D98P2

HOLE5
*HG-ZHP-1

HOLE4
*H-ZHP-2

HOLE3
*H-C94D94N

HOLE11
*H-O94X106D94X106N

HOLE2
*H-O94X106D94X106N

HOLE14
*SPAD-RE158X158NP

HOLE12
*SPAD-RE79X315NP

HOLE17
*SPAD-RE178X118NP

SPAD10
*SPAD-RE197X197NP

SPAD8
*SPAD-RE197X197NP

SPAD9
*SPAD-RE197X185NP

SPAD1
*SPAD-RE197X197NP

SPAD5
*SPAD-RE197X197NP

SPAD6
*SPAD-RE315X315NP

SPAD7
*SPAD-RE197X197NP

SPAD3
*SPAD-RE197X197NP

SPAD4
*SPAD-RE197X197NP

SPAD2
*SPAD-RE197X197NP

+1.2VSUS

D19 *AZ5725-01F.R7G

D20 *AZ5725-01F.R7G

D13 *AZ5725-01F.R7G

D12 *AZ5725-01F.R7G

+1.2VSUS

D23 *AZ5725-01F.R7G

D25 *AZ5725-01F.R7G

C156 0.1u/25V_4 +3V

C12 0.1u/25V_4 +5V_S5

+3VPCU C126 *0.1u/25V_4 +5V_S5

C147 *0.1u/25V_4 +3VPCU

+5V_S5 C177 *0.1u/25V_4 +VIN

C62 0.1u/25V_4 +VIN

C60 *1000p/50V_4

C58 0.1u/25V_4 +3V

For ESD solution add in Rev: D

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	USB BOARD CONN	1A
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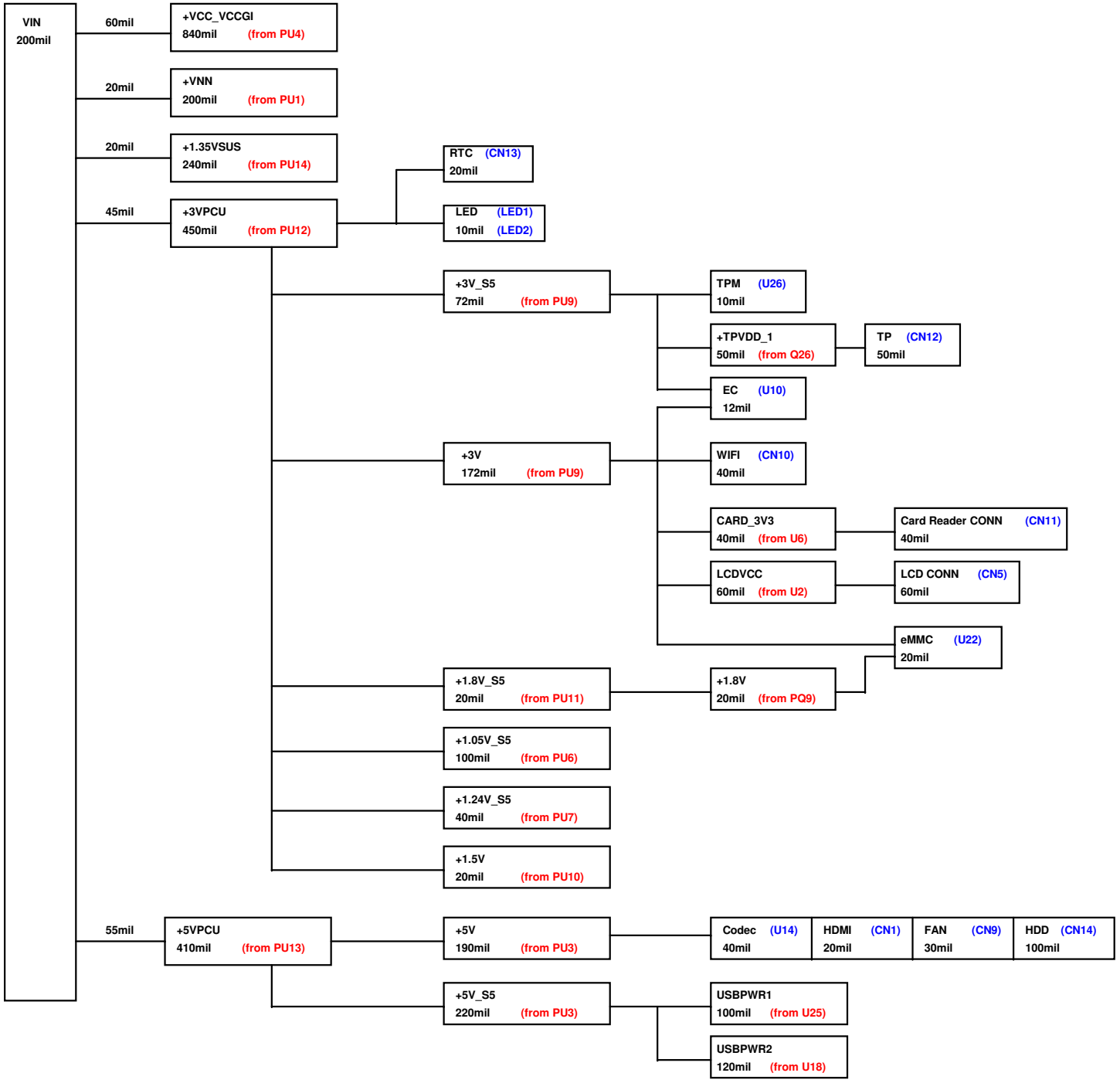
Apollo Power Tree



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Model	REV	CHANGE LIST	ZHP/ZSP MB
ZHE/ZSG MB	REV.A	1 2017/8/15 REV:A Initial release	
	REV.B	1 Page 8 Vender test crystal change C361/C362t o 18P 2 Page 3 Intel suggest R109/R112. 3 Page 6 AC_PRESENT SCH (GML support is, Remove in B) 4 Page 4 BIOS Change Panel GPIO to +3V , so remove Q6/Q8/Q9/R76/R83/R105, add R620/R621/R622 5 Page 11 Memory Vender suggest M_B_PARITY need PU, So remove R177 , mout R206. 6 Page 28 PL9 Change from CV-2280MZ15 2.2U to CV-10B0MZ13 1U. PR65 Change from CS42202FB01 220K to CS42212FB22 221K. 7 PR173 Change from CS41002JB20 100K to CS41102FB13 110K. 8 Page 6 C78/C119/R633/R634 for Intel ESD.	
	REV. C	1. Remove below 0 ohm , change to Short Pad. R178,R196,R620,R621,R622,R486,R497,R68,R438,R61,R92,R119,R123,R128,R129,R134,R143,R153,R158,R161,R162,R179,R279 R280,R455,R456,R236,R251,R254,R261,R278,R290,R296,R300,R312,R542,R548,R71,R437,R455,R451,R464,R465,R466,R467,R370 R582,R30,R31,R32,R33,R34,R35,R115,R148,R154,R160,R168,R172,19,R227,R283,R313,R315,R316,R317,R331,R347,R349,R364,R365 R378,R379,R380,R381,R1,R30,R50,R406,R590,R591,R595,R596,R597,R598,R599,R601,R245,R255,R277,R552,R553,R570,R571,R593 R608,R614,R618,R263,PR91,PR92,PR93,PR96,PR104,PR105,PR106,PR107,PR112,PR122,PR124,PR163,PR164,PR256,PR257,PJ10,PJ11,PJ12 PJ15,PR71,PR80,PR98,PR99,PR100,PR102,PR103,PR111,PR129,PR153,PR165,PR174,PR180,PR184,PR193,PR203,PR209,PR226,PR229,PR232 PR233,PR235,PR255,PJ3,PJ6,PR6,PR7,PR138,PR139,PJ4,PJ13,PJ14,PR95,PR109,PR117,PR118,PR240,PR241,PR245,PR246,PR249,PR252,PR254 PJ1,PR49,PR58,PR63,PR135,PR140,PR152,PR156,PR171,PR177,PR189,PR190,PJ2,PR10,PR11,PR19,PR25,PR42,PR43,PR54,PR60,PR6,PR186 PR191,PJ7,PJ8,PJ9,PR144,PR147,PR148,PR178,PR188,PR205,PR215,PR221,PR222,PR225,PR150 2. Page 14 Add R16,R17,R18,R19 ,C17 and remove R419,R454 for HDMI issue. 3. Mount R177 0 ohm ,Remove R222 for 60 OD RAM issue.	

Page	From	To
1		3A
2		3A
3		3A
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38		3A
39		3A

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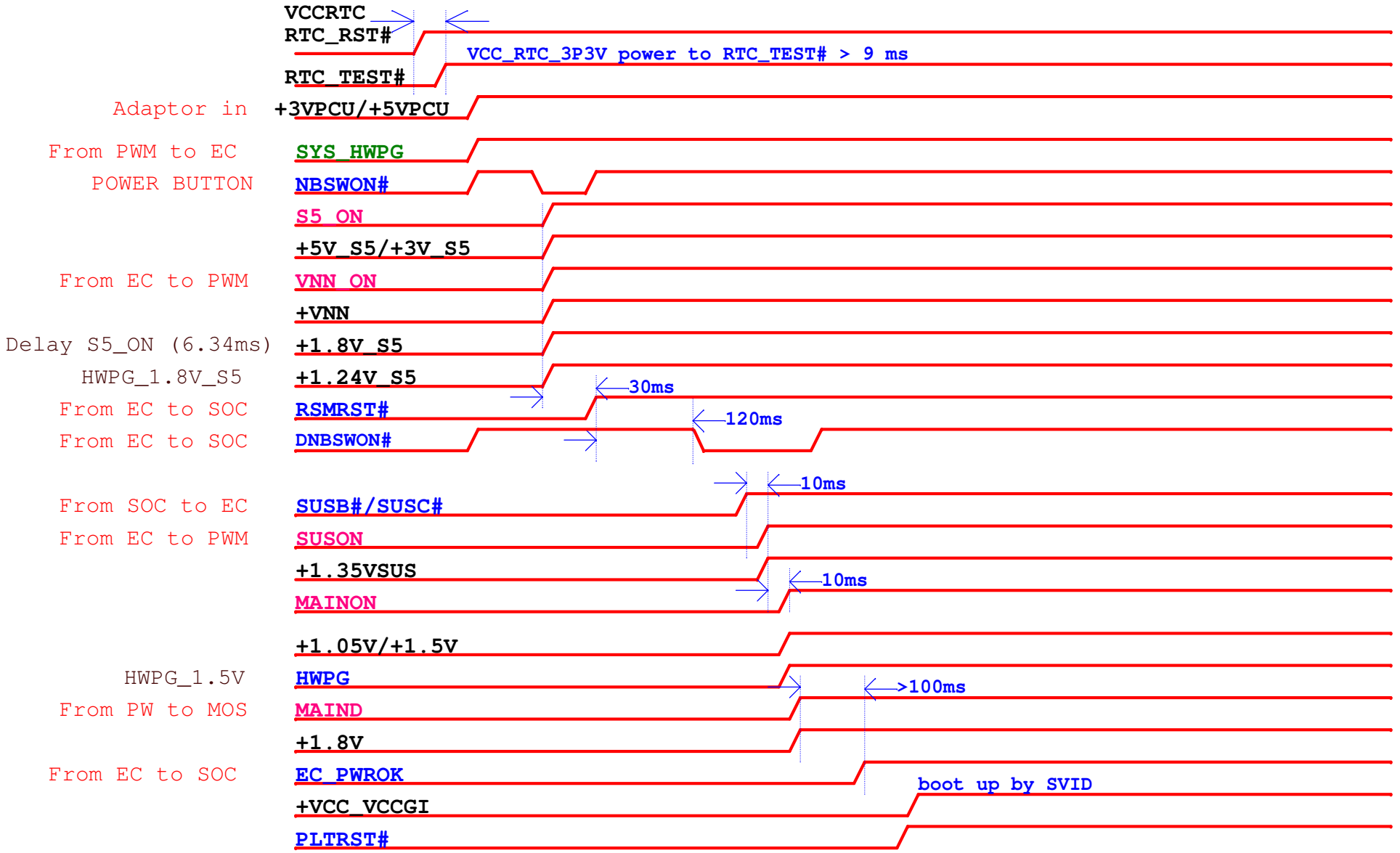
Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF



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