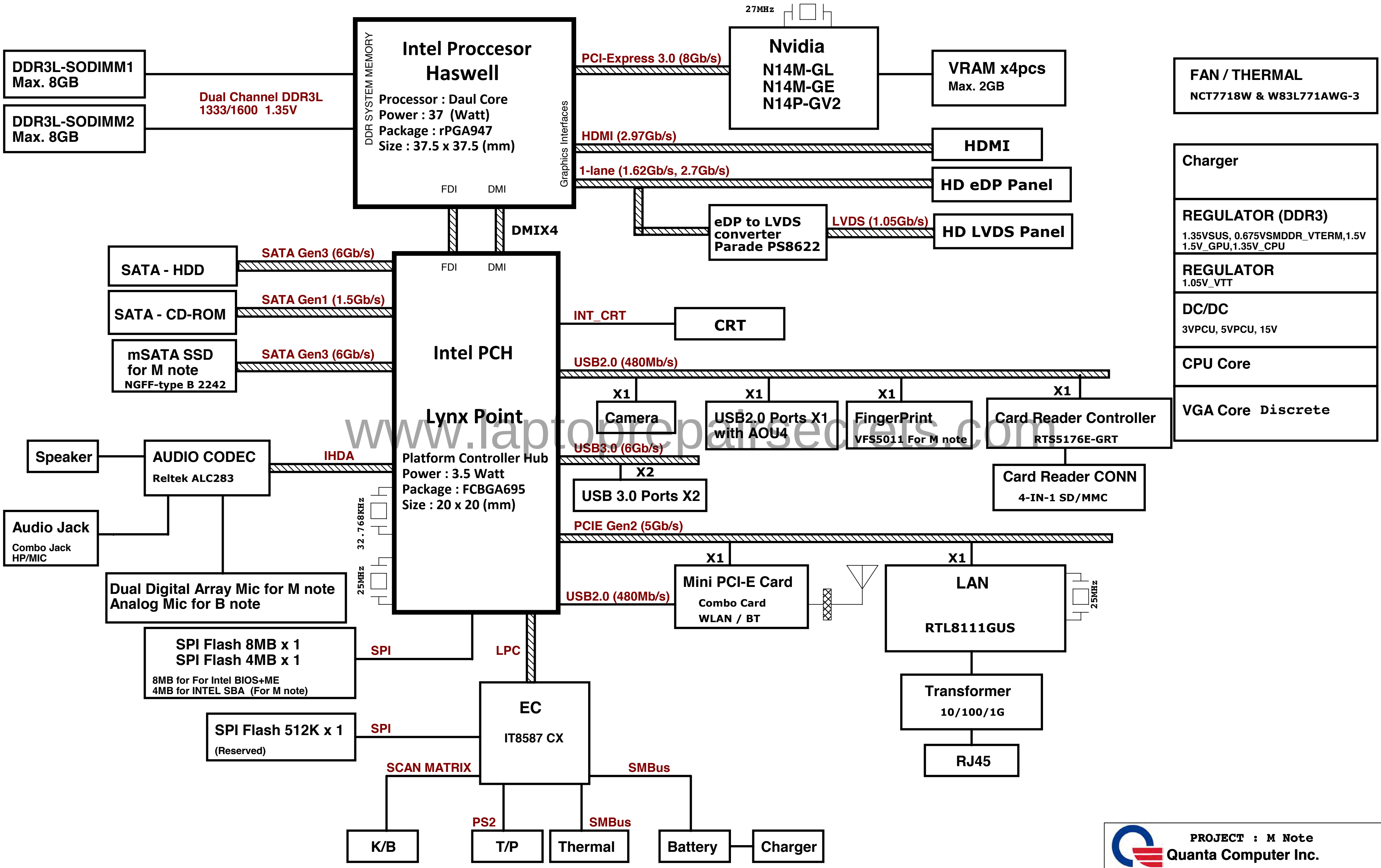
M/B Note Intel Shark Bay Platform (Optimus) Block Diagram



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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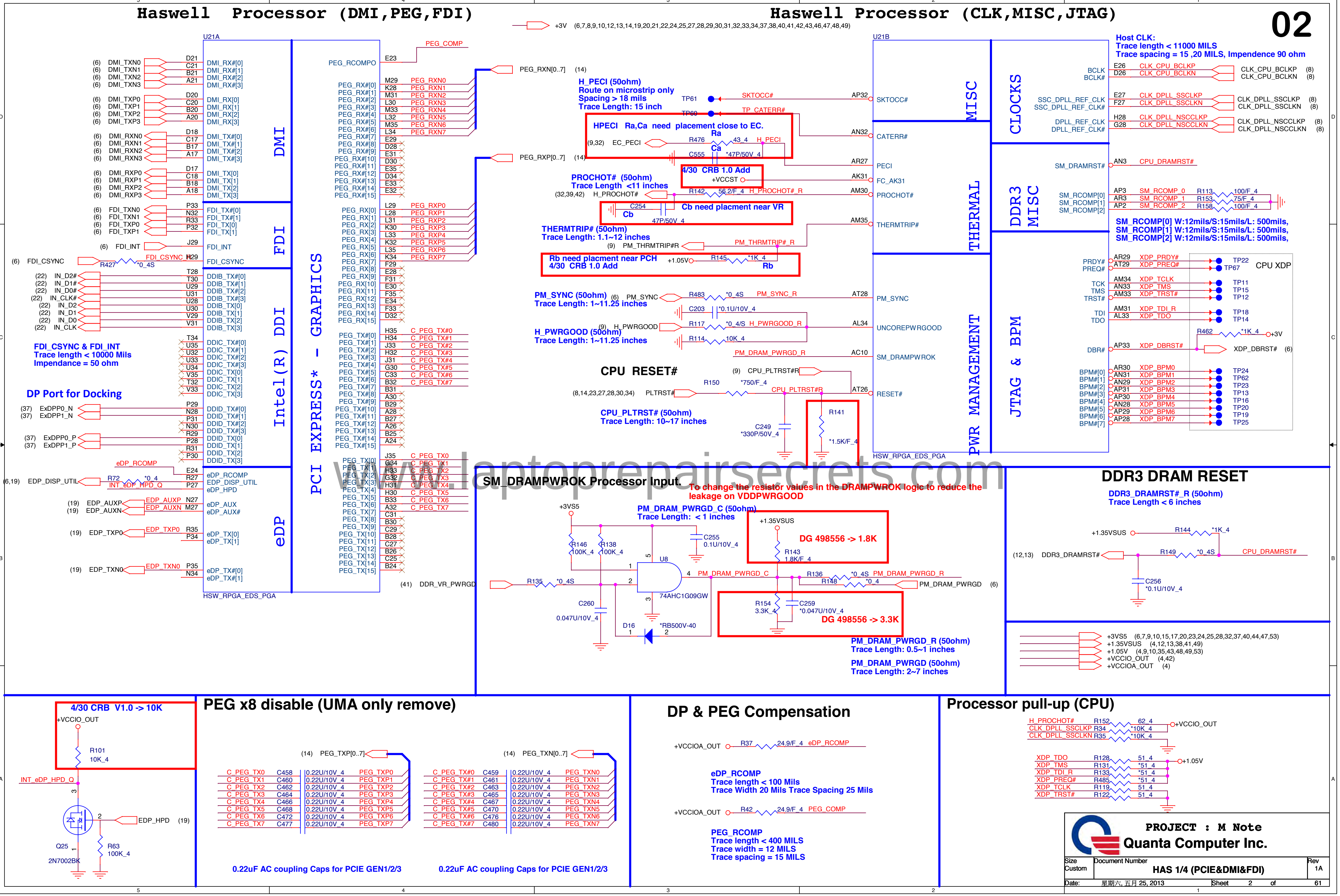

02
Haswell Processor (DMI,PEG,FDI)
Haswell Processor (CLK,MISC,JTAG)
+3V (6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
U21A
U21B
DMI
FDI
Intel(R) DDI
PCI EXPRESS* - GRAPHICS
eDP
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
HSW_RPGA_EDS_PGA
FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm
DP Port for Docking
Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm
H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch
HPECI Ra,Ca need placement close to EC.
4/30 CRB 1.0 Add
PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR
THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH
4/30 CRB 1.0 Add
SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,
CPU XDP
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
CPU RESET#
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
SM_DRAMPWROK Processor Input.
To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
DG 498556 -> 1.8K
DG 498556 -> 3.3K
74AHC1G09GW
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
DDR3 DRAM RESET
DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
+3VS5 (6,7,9,10,15,17,20,23,24,25,28,32,37,40,44,47,53)
+1.35VSUS (4,12,13,38,41,49)
+1.05V (4,9,10,35,43,48,49,53)
+VCCIO_OUT (4,42)
+VCCIOA_OUT (4)
4/30 CRB V1.0 -> 10K
PEG x8 disable (UMA only remove)
0.22uF AC coupling Caps for PCIE GEN1/2/3
0.22uF AC coupling Caps for PCIE GEN1/2/3
DP & PEG Compensation
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS
Processor pull-up (CPU)
PROJECT : M Note
Quanta Computer Inc.
Size Custom
Document Number HAS 1/4 (PCIE&DMI&FDI)
Rev 1A
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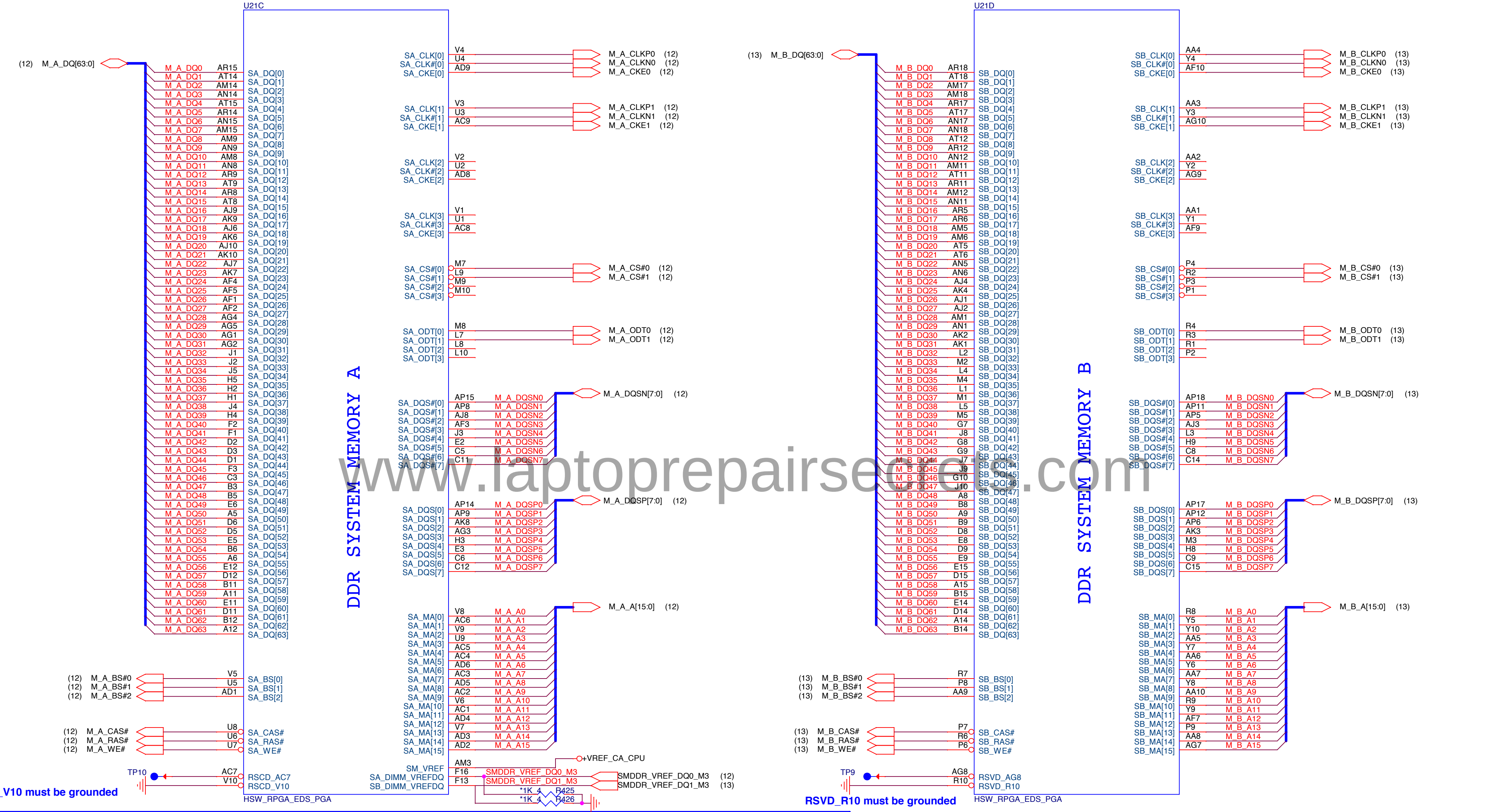
Haswell Processor (DDR3)

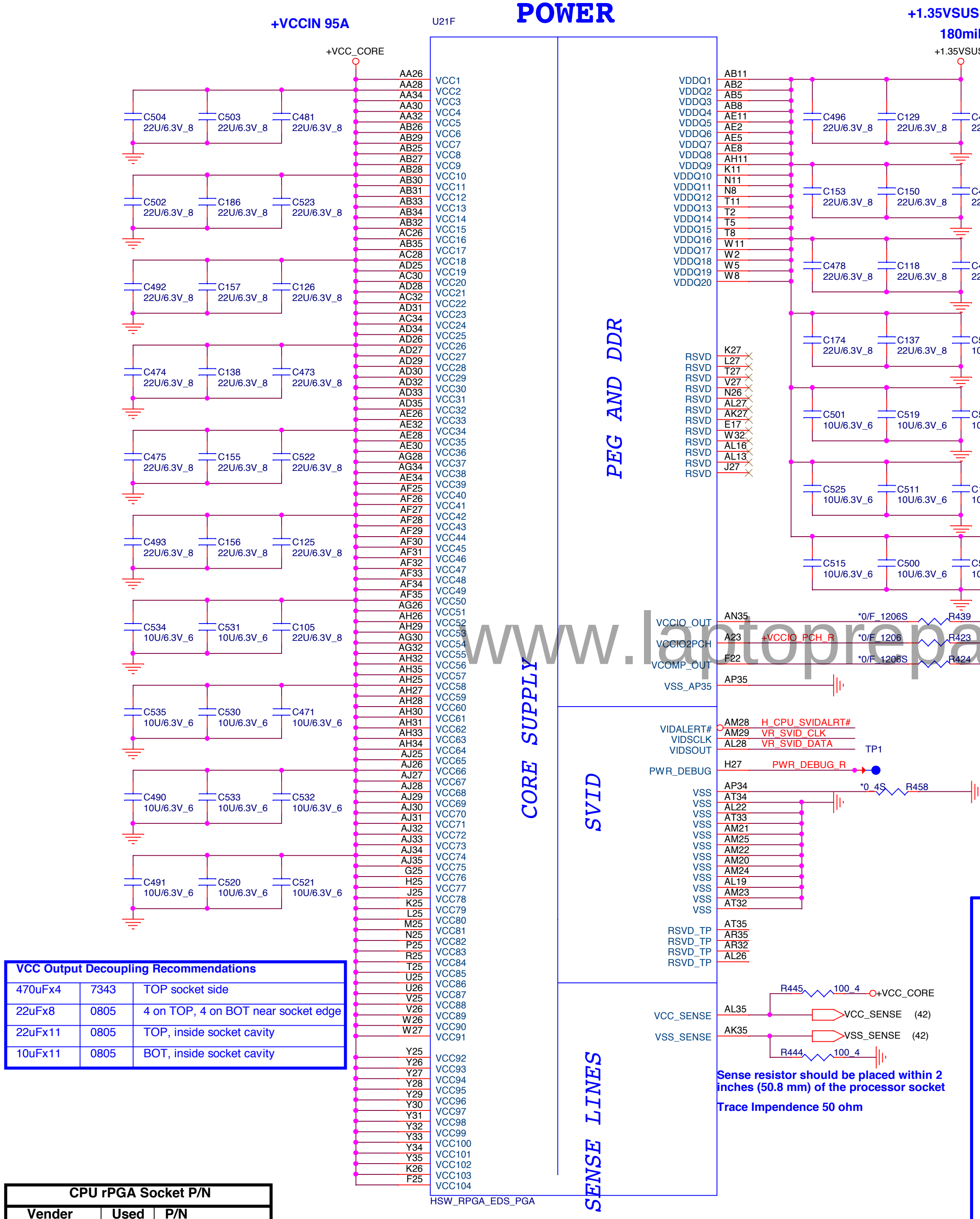


CPU SM_VREF

+VREF_CA_CPU (12)

Haswell Processor (POWER)

04



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

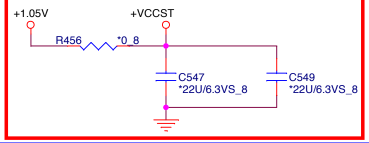
VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

CPU rPGA Socket P/N

Vender	Used	P/N
LTS	V	DGG^7000001
FOX		DGG^9000058

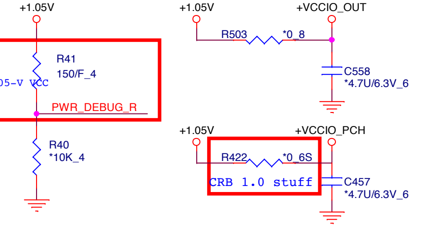
CRB 1.0 add



Power Test Propose

DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP



CPU VDDQ

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

SVID DATA

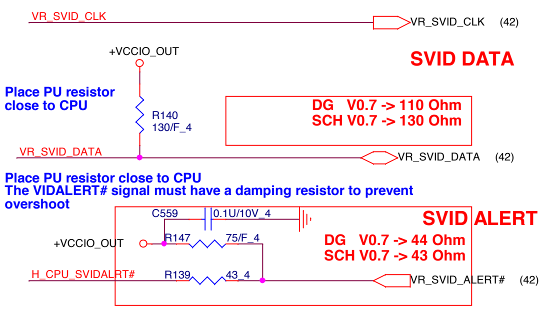
Place PU resistor close to CPU

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm



PROJECT : M Note

Quanta Computer Inc.

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Custom	HAS 3/4 (POWER)	1A

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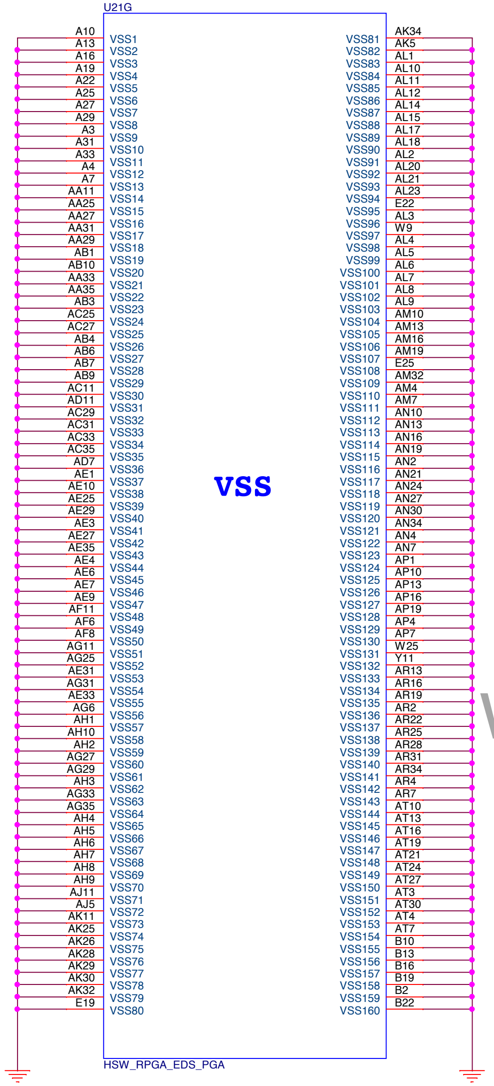
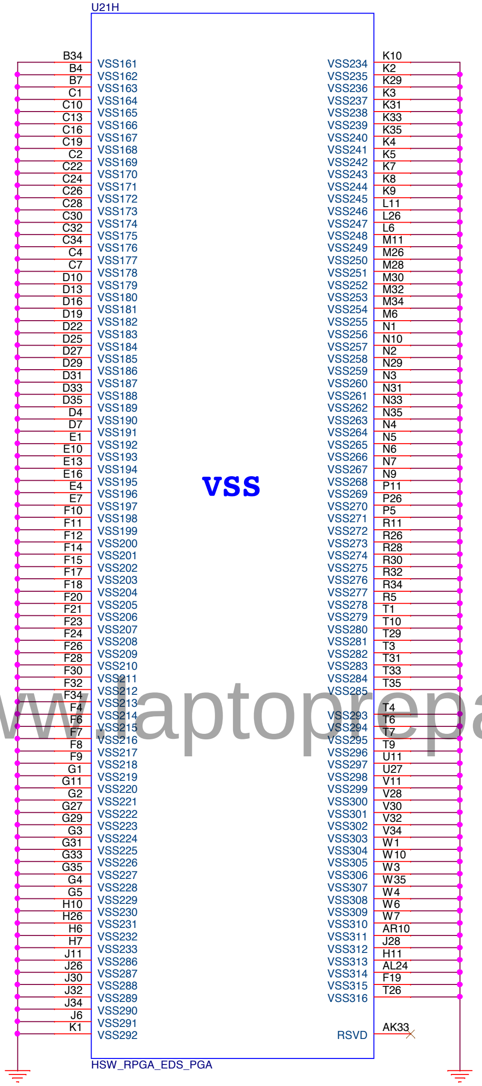
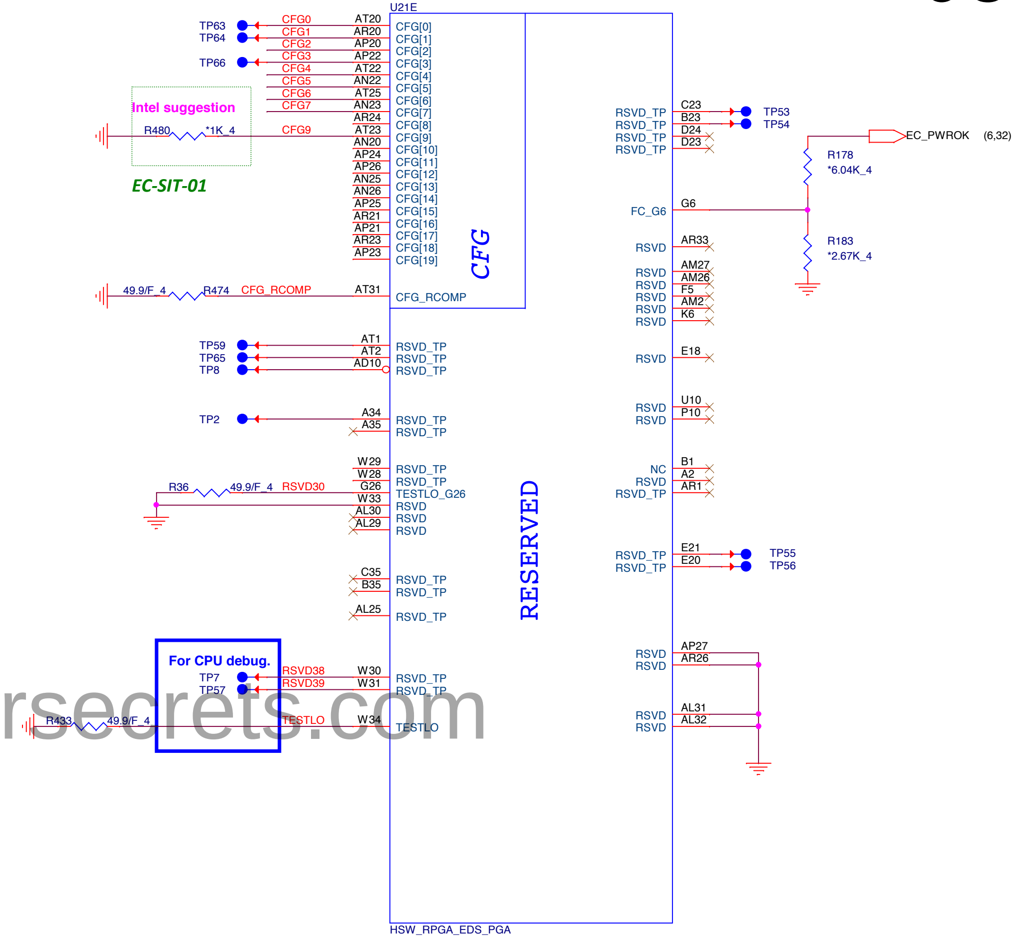
Haswell Processor (GND)





Haswell Processor (RESERVED, CFG)



CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R481 *1K_4

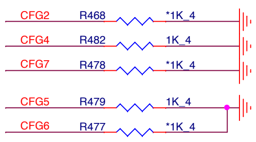
CFG[6:5] (PCIE Port Bifurcation Straps)

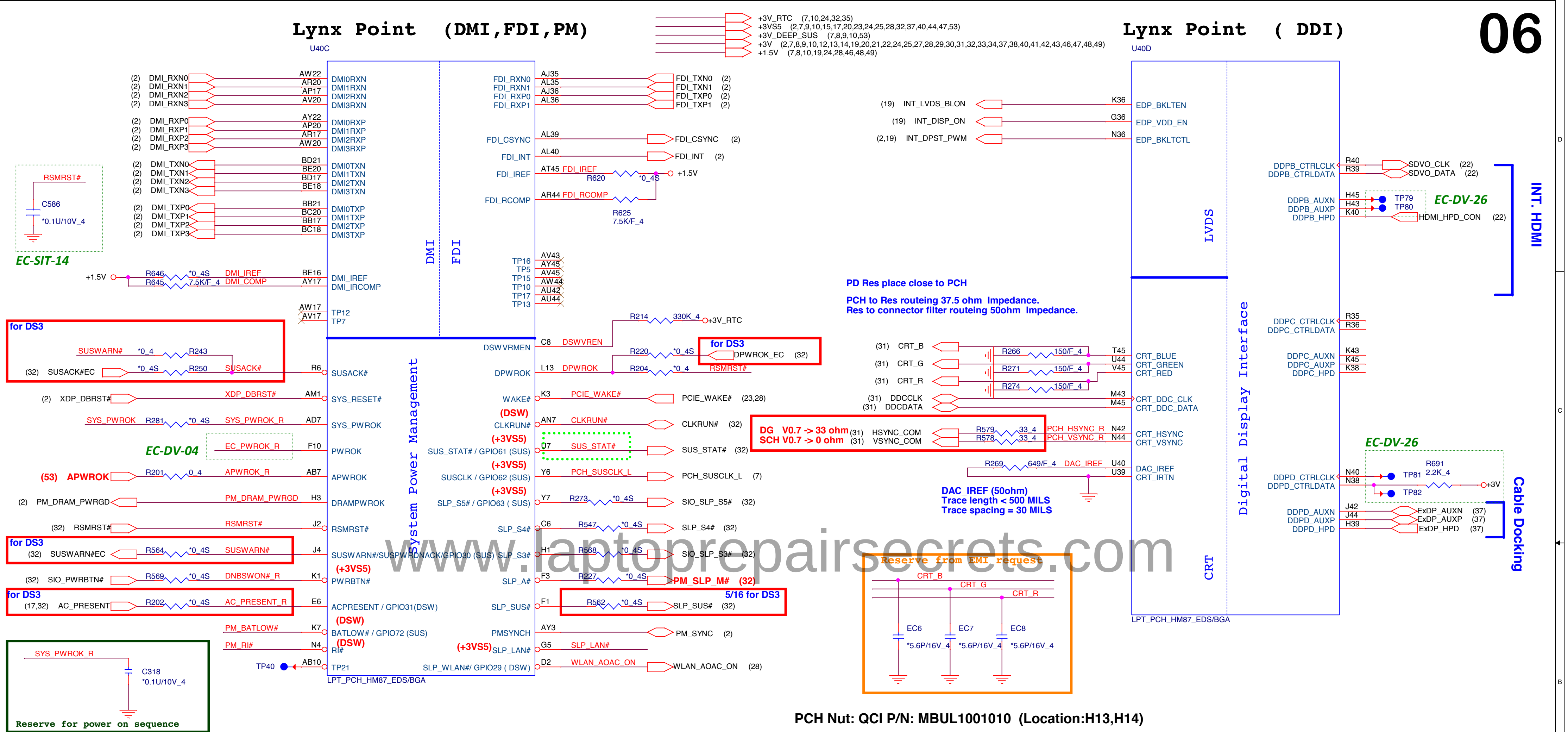
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

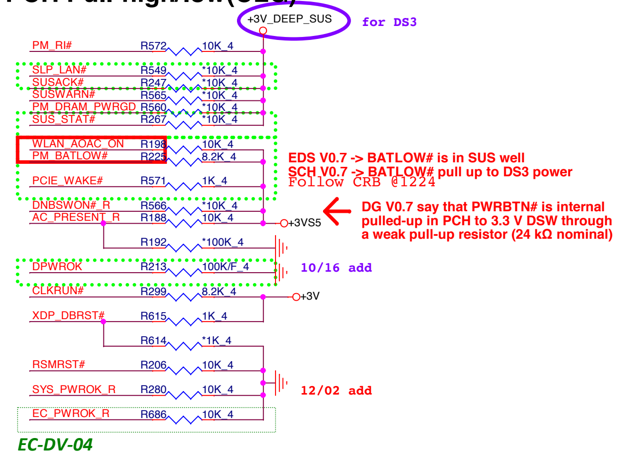
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

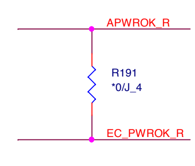




PCH Pull-high/low(CLG)

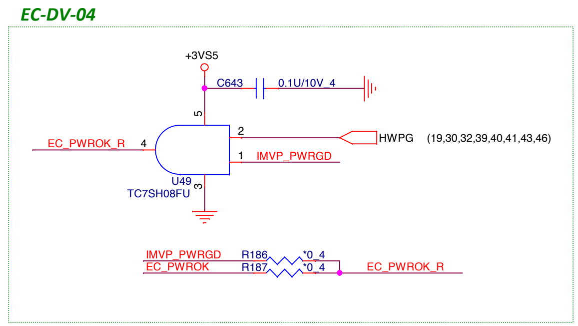


SBA Support



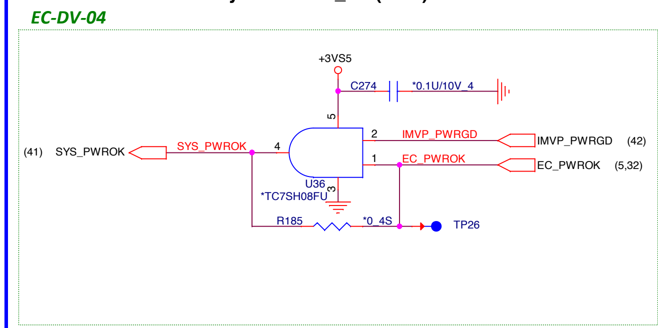
	R	Status
Non-SBA	R191/Stuff,R201/Un-Stuff	
SBA	R191/Un-Stuff,R201/Stuff	

PCH_PWROK_OK(CLG)



Follow Intel schematic review suggestion

System PWR_OK(CLG)



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
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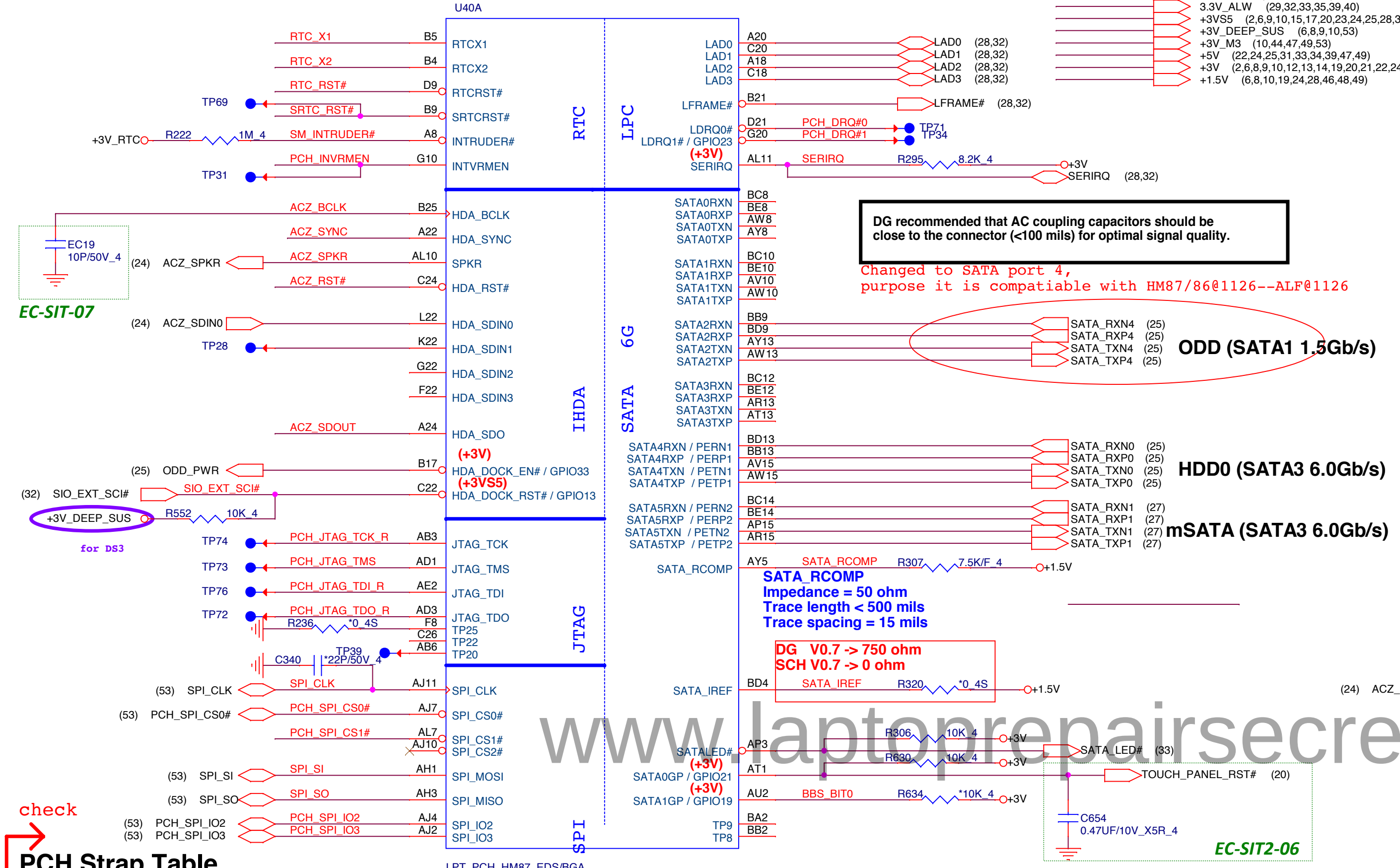
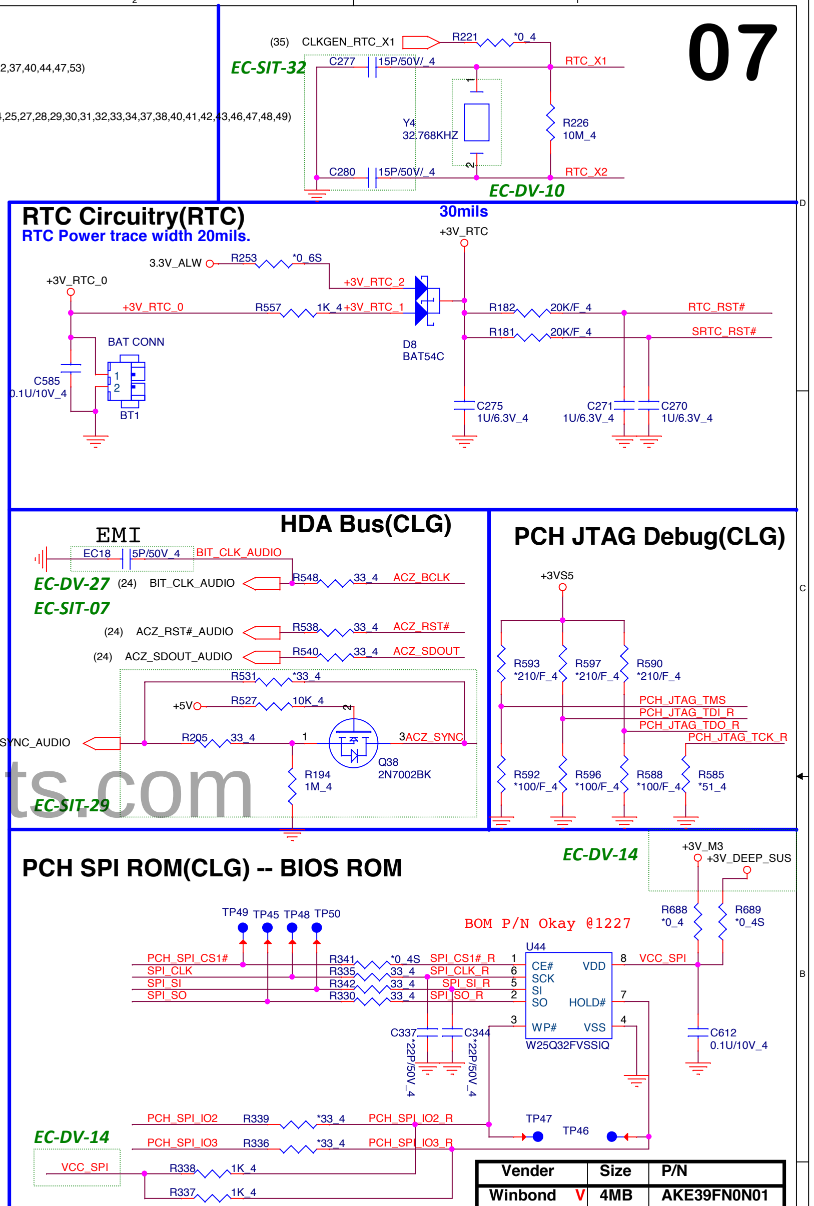
Lynx Point (HDA,JTAG,SATA)

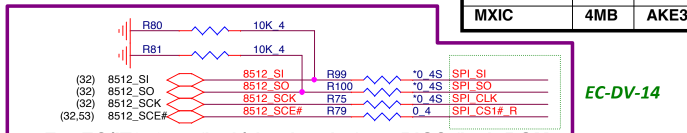




PCH Strap Table

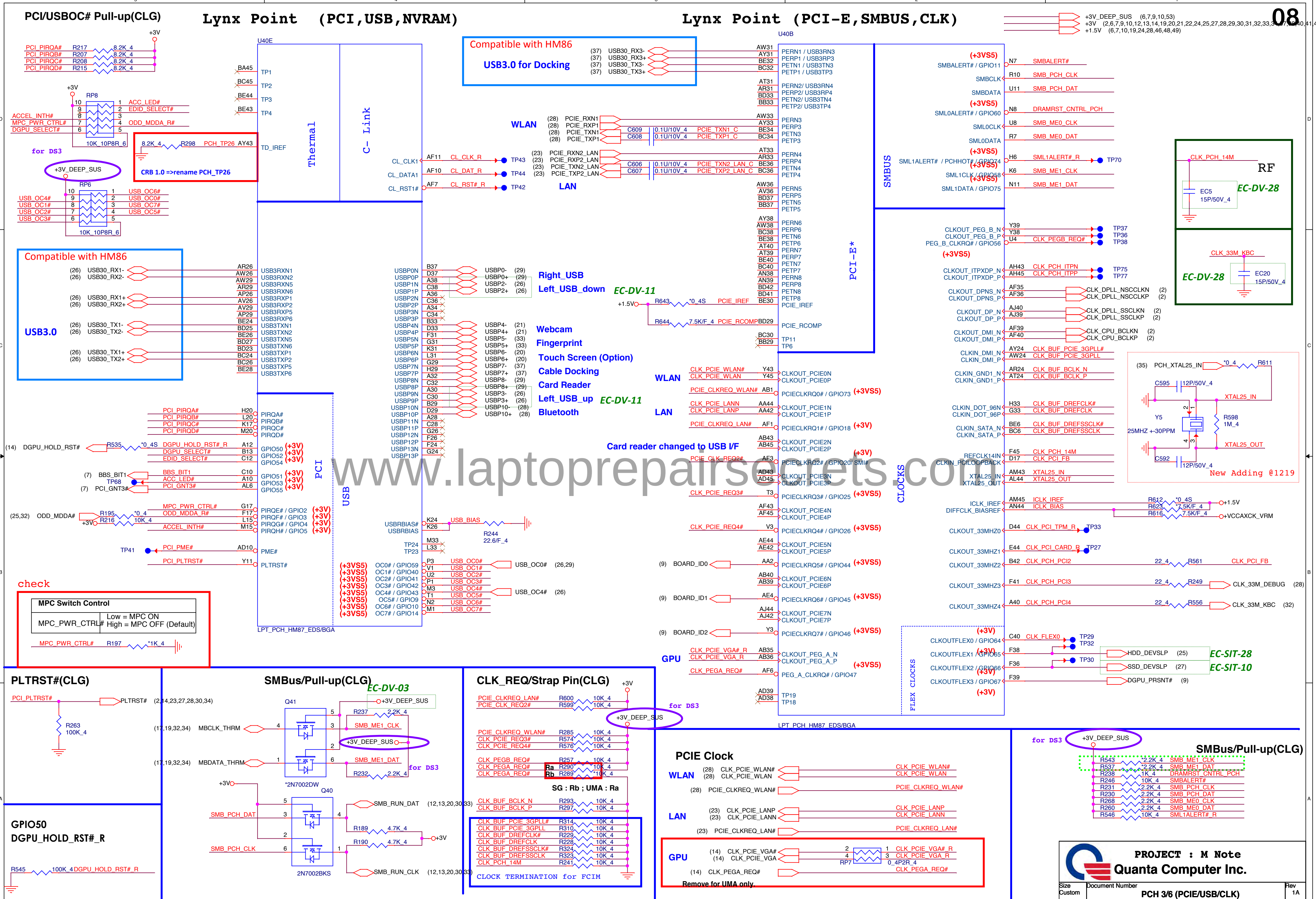
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R292 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R286 *1K_4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R240 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI; 0 / 0 / LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# BBS_BIT0 R633 *1K_4 R550 *1K_4 BBS_BIT1 (8)
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R539 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	ACZ_SDOUT R551 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R583 *1K_4 BT_OFF# (9,28)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R577 *1K_4 PLL_ODVR_EN (9)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	SPI_SI R291 *1K_4 +3V
SUSCLK / GPIO62	On-die PLL Voltage Regulator	PWROK	0 = Disable 1 = Enable (Int PU)	(6) PCH_SUSCLK_L R256 *1K_4 R262 *1K_4 +3V

Vender		Size	P/N
Winbond	V	4MB	AKE39FN0N01
MXIC		4MB	AKE39ZN0Z01



For EC(IT8587 e-flash) load code from BIOS flash ROM

BIOS = 4MB_CS1 ME = 8MB_CS0	R	Status
Un-SBA	R79	Un-Stuff
SBA	R79	Stuff



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A
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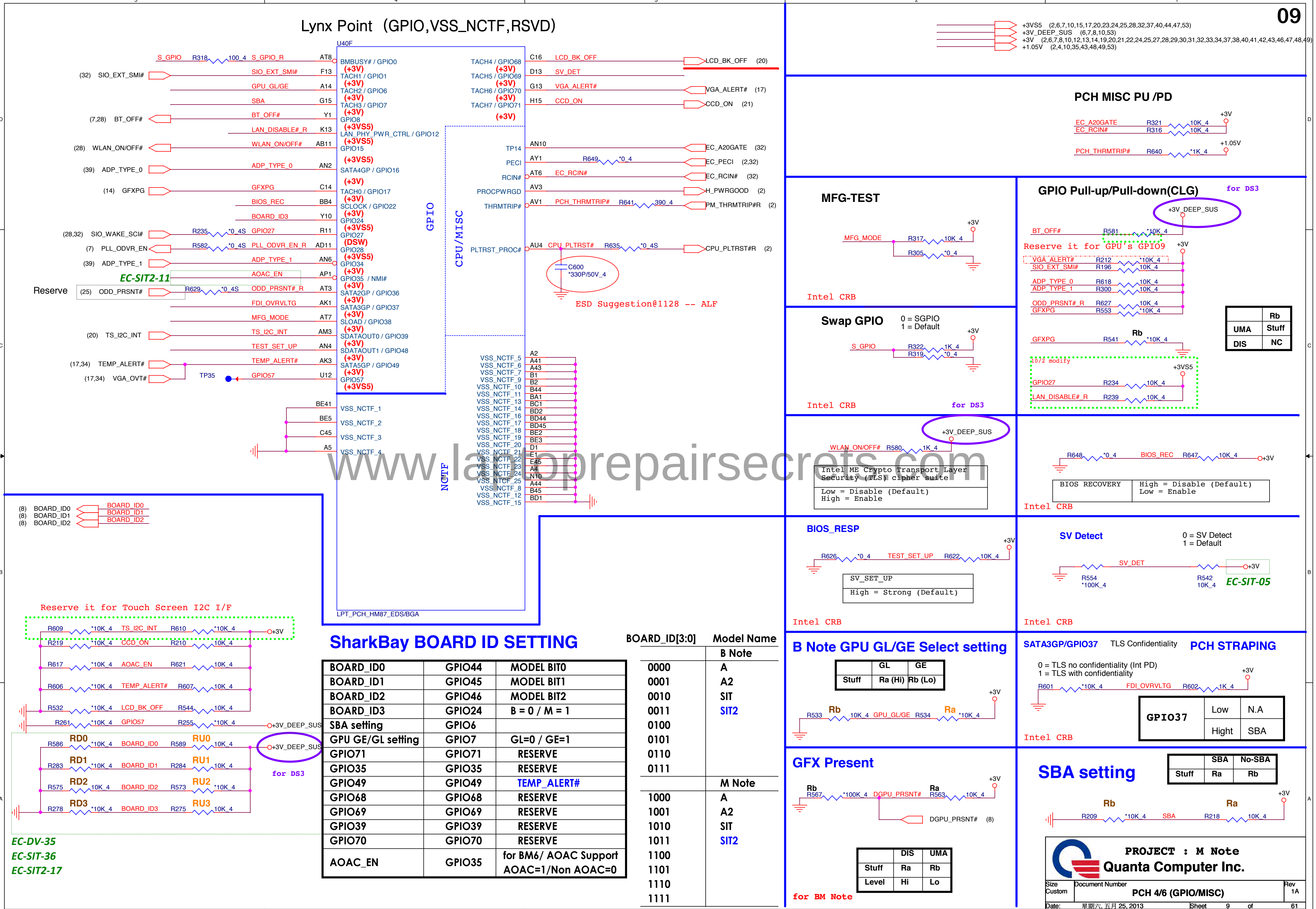
Lynx Point (GPIO,VSS_NCTF,RSVD)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

	Rb
UMA	Stuff
DIS	NC

SharkBay BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO24	B = 0 / M = 1
SBA setting	GPIO6	
GPU GE/GL setting	GPIO7	GL=0 / GE=1
GPIO71	GPIO71	RESERVE
GPIO35	GPIO35	RESERVE
GPIO49	GPIO49	TEMP_ALERT#
GPIO68	GPIO68	RESERVE
GPIO69	GPIO69	RESERVE
GPIO39	GPIO39	RESERVE
GPIO70	GPIO70	RESERVE
AOAC_EN	GPIO35	for BM6/ AOAC Support AOAC=1/Non AOAC=0

BOARD_ID[3:0]	Model Name
	B Note
0000	A
0001	A2
0010	SIT
0011	SIT2
0100	
0101	
0110	
0111	
	M Note
1000	A
1001	A2
1010	SIT
1011	SIT2
1100	
1101	
1110	
1111	

	GL	GE
Stuff	Ra (Hi)	Rb (Lo)

GPIO37	Low	N.A
	Hight	SBA

	SBA	No-SBA
Stuff	Ra	Rb

	DIS	UMA
Stuff	Ra	Rb
Level	Hi	Lo

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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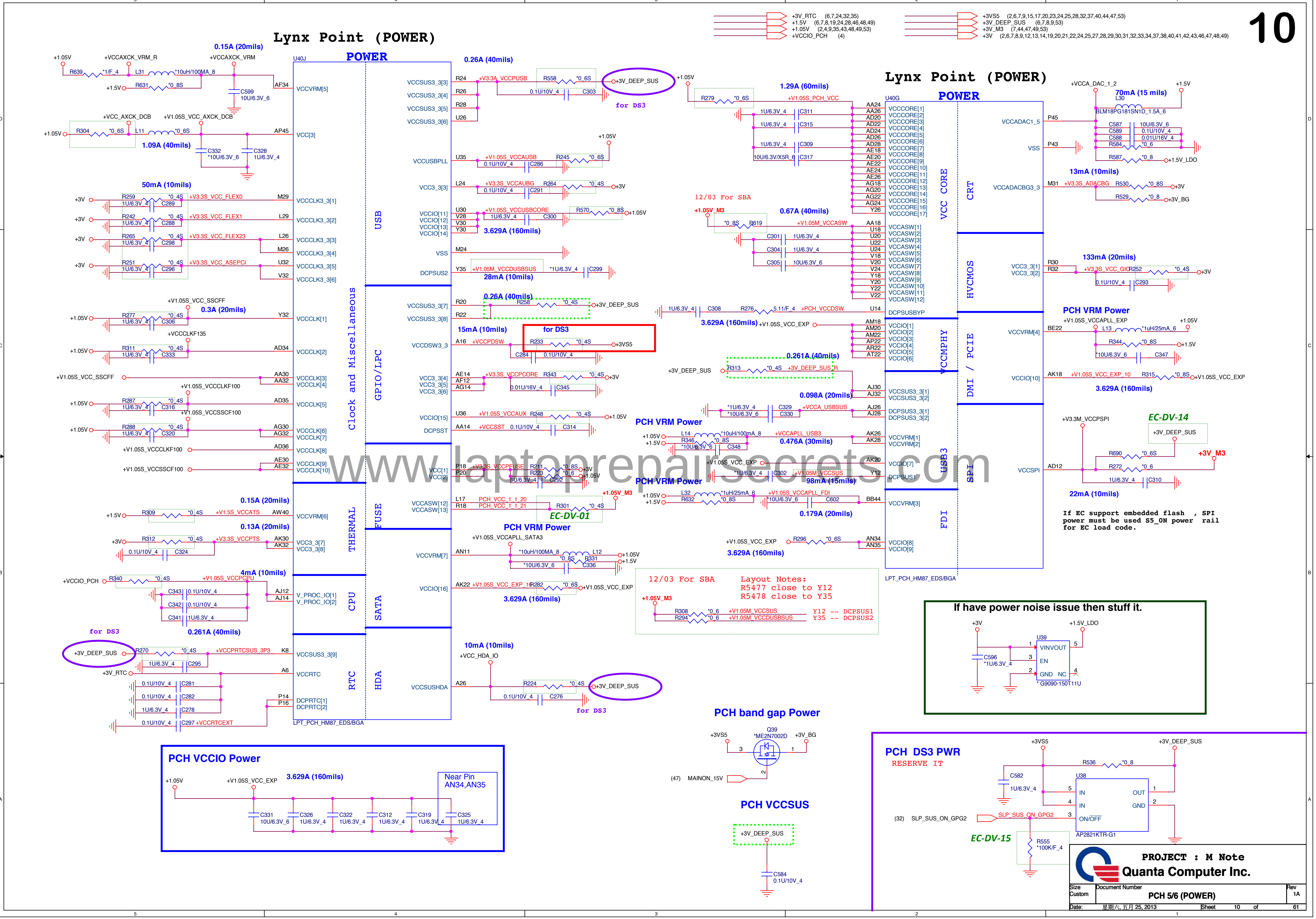
10
Lynx Point (POWER)
POWER
+3V_RTC (6,7,24,32,35)
+1.5V (6,7,8,19,24,28,46,48,49)
+1.05V (2,4,9,35,43,48,49,53)
+VCCIO_PCH (4)
+3VS5 (2,6,7,9,15,17,20,23,24,25,28,32,37,40,44,47,53)
+3V_DEEP_SUS (6,7,8,9,53)
+3V_M3 (7,44,47,49,53)
+3V (2,6,7,8,9,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
0.15A (20mils)
1.09A (40mils)
50mA (10mils)
0.3A (20mils)
0.15A (20mils)
0.13A (20mils)
4mA (10mils)
0.261A (40mils)
0.26A (40mils)
3.629A (160mils)
28mA (10mils)
15mA (10mils)
for DS3
EC-DV-01
PCH VRM Power
10mA (10mils)
1.29A (60mils)
0.67A (40mils)
12/03 For SBA
0.098A (20mils)
0.476A (30mils)
98mA (15mils)
0.179A (20mils)
70mA (15 mils)
13mA (10mils)
133mA (20mils)
22mA (10mils)
EC-DV-14
If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.
Layout Notes:
R5477 close to Y12
R5478 close to Y35
Y12 -- DCPSUS1
Y35 -- DCPSUS2
If have power noise issue then stuff it.
PCH VCCIO Power
Near Pin AN34,AN35
PCH band gap Power
PCH VCCSUS
PCH DS3 PWR
RESERVE IT
EC-DV-15
LPT_PCH_HM87_EDS/BGA
www.laptoprepairsecrets.com
PROJECT : M Note
Quanta Computer Inc.
Document Number
PCH 5/6 (POWER)
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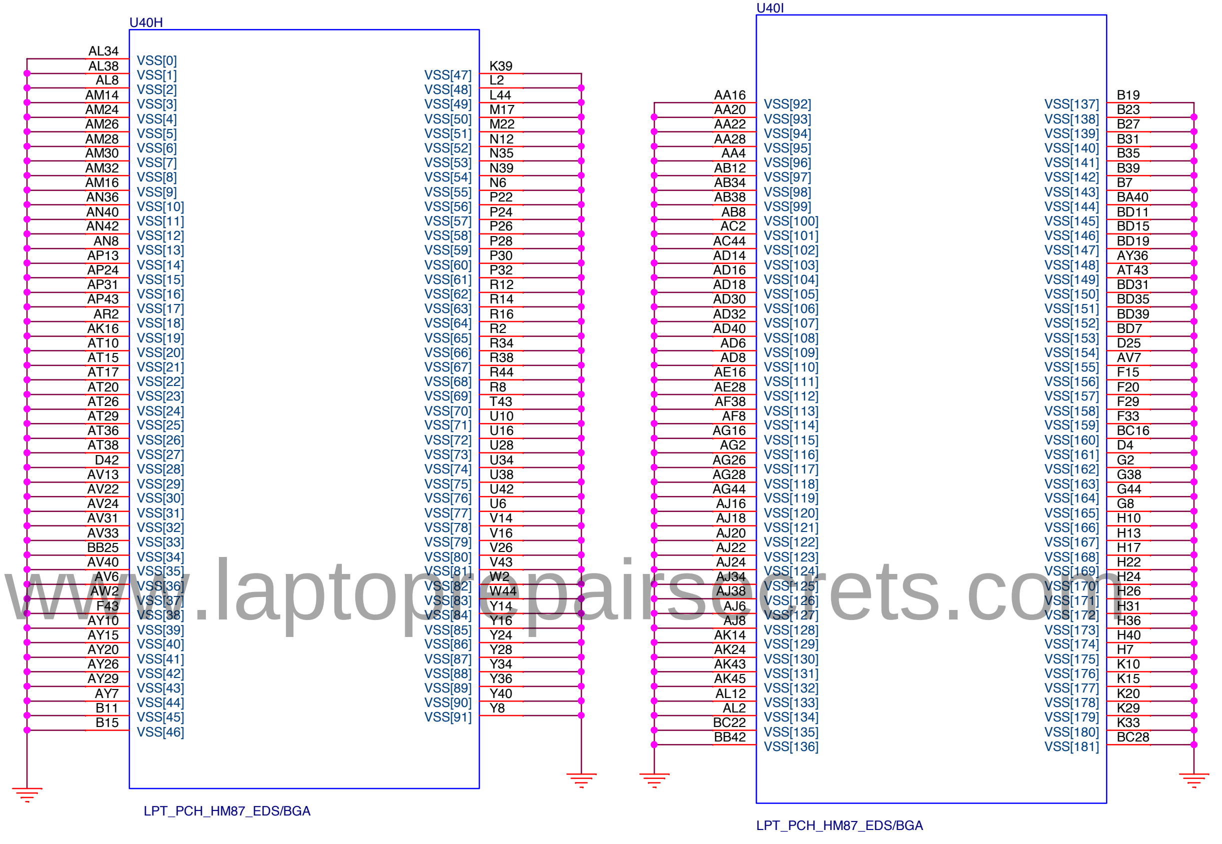
Lynx Point (GND)



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
B	PCH 6/6 (GND)	1A
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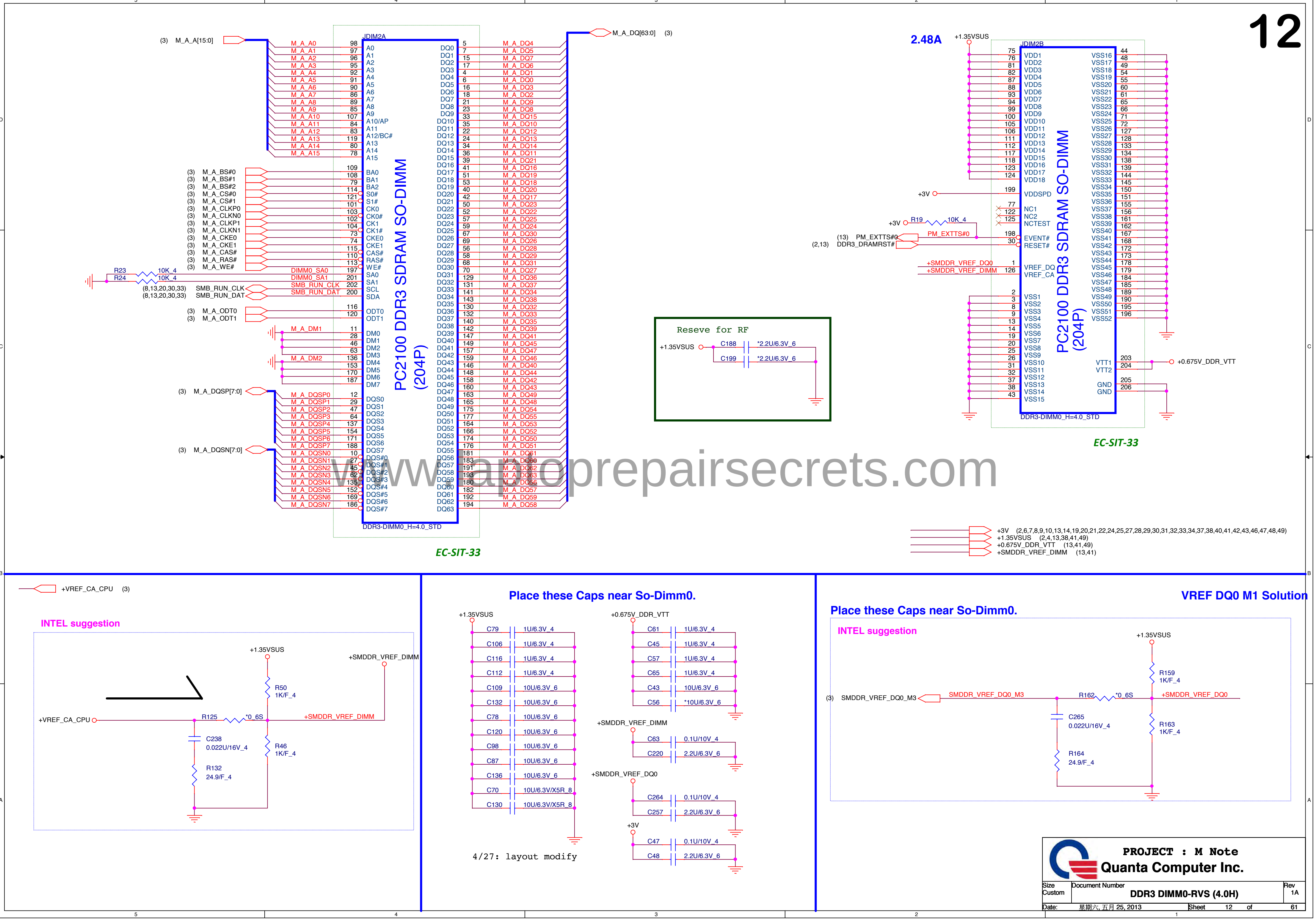
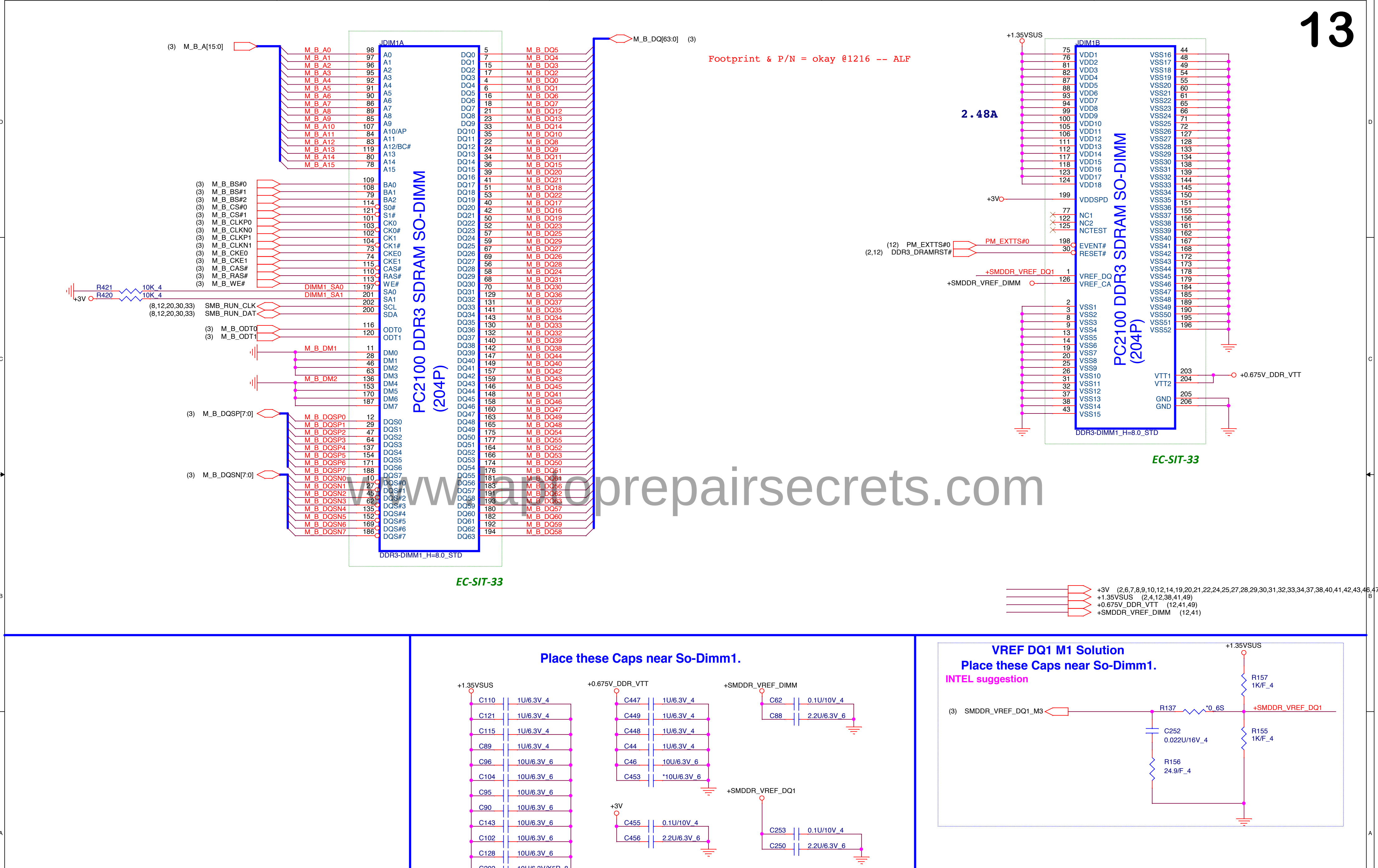
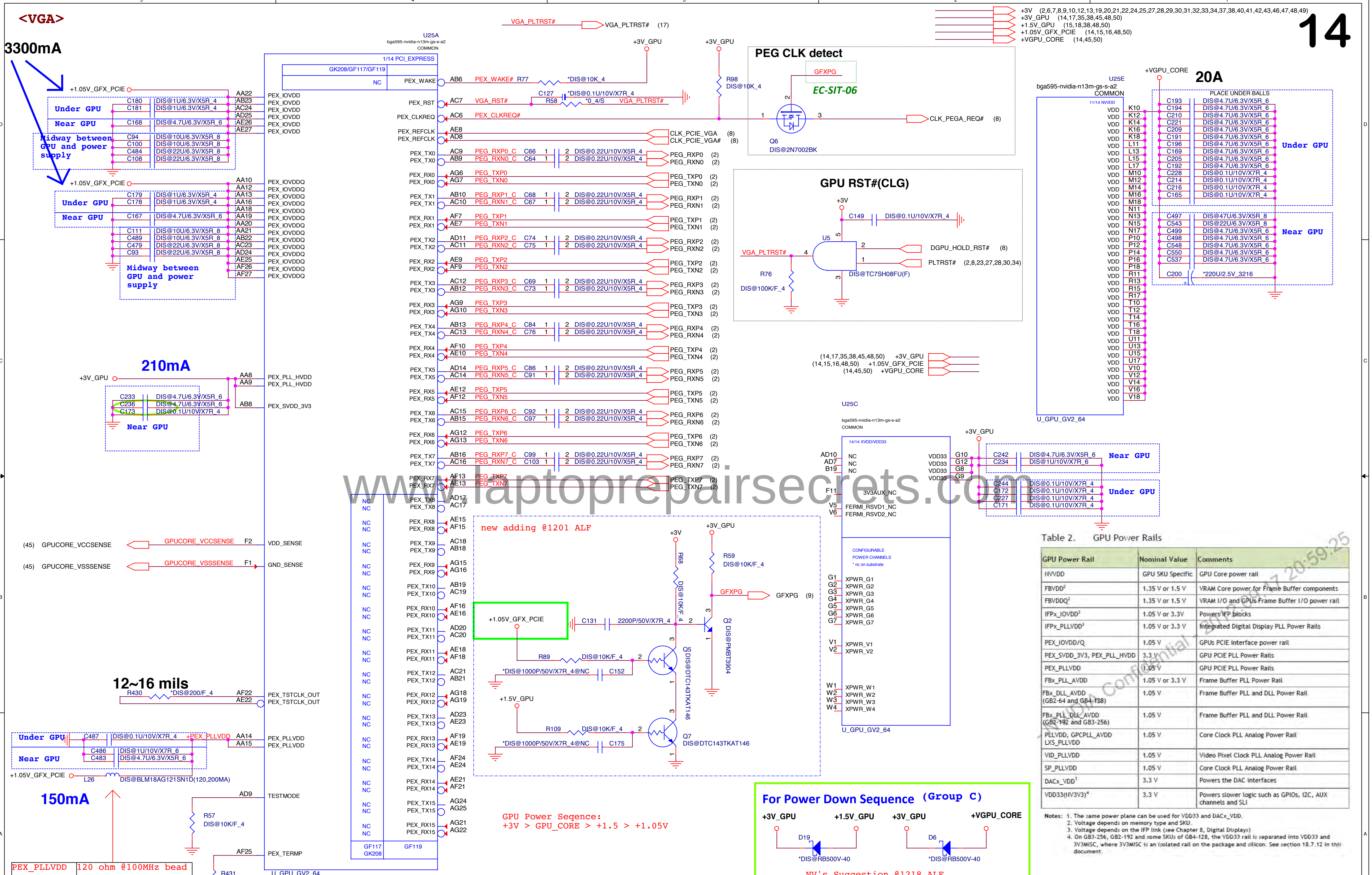

12
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4.0_STD
EC-SIT-33
(3) M_A_A[15:0]
M_A_A0 ... M_A_A15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15
(3) M_A_BS#0
(3) M_A_BS#1
(3) M_A_BS#2
(3) M_A_CS#0
(3) M_A_CS#1
(3) M_A_CLKP0
(3) M_A_CLKN0
(3) M_A_CLKP1
(3) M_A_CLKN1
(3) M_A_CKE0
(3) M_A_CKE1
(3) M_A_CAS#
(3) M_A_RAS#
(3) M_A_WE#
BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE# SA0 SA1 SCL SDA
R23 10K_4
R24 10K_4
DIMM0_SA0
DIMM0_SA1
(8,13,20,30,33) SMB_RUN_CLK
(8,13,20,30,33) SMB_RUN_DAT
(3) M_A_ODT0
(3) M_A_ODT1
ODT0 ODT1
M_A_DM1
M_A_DM2
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
(3) M_A_DQSP[7:0]
M_A_DQSP0 ... M_A_DQSP7
DQS0 ... DQS7
(3) M_A_DQSN[7:0]
M_A_DQSN0 ... M_A_DQSN7
DQS#0 ... DQS#7
DQ0 ... DQ63
M_A_DQ[63:0] (3)
JDIM2B
2.48A
+1.35VSUS
VDD1 ... VDD18
VSS1 ... VSS52
+3V VDDSPD
NC1 NC2 NCTEST
+3V R19 10K_4
(13) PM_EXTTS#0
(2,13) DDR3_DRAMRST#
PM_EXTTS#0
EVENT# RESET#
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
VREF_DQ VREF_CA
VTT1 VTT2
GND GND
+0.675V_DDR_VTT
Reseve for RF
+1.35VSUS
C188 *2.2U/6.3V_6
C199 *2.2U/6.3V_6
+3V (2,6,7,8,9,10,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
+1.35VSUS (2,4,13,38,41,49)
+0.675V_DDR_VTT (13,41,49)
+SMDDR_VREF_DIMM (13,41)
+VREF_CA_CPU (3)
INTEL suggestion
+1.35VSUS
+SMDDR_VREF_DIMM
R50 1K/F_4
+VREF_CA_CPU
R125 *0_6S
C238 0.022U/16V_4
R46 1K/F_4
R132 24.9/F_4
Place these Caps near So-Dimm0.
+1.35VSUS
C79 1U/6.3V_4
C106 1U/6.3V_4
C116 1U/6.3V_4
C112 1U/6.3V_4
C109 10U/6.3V_6
C132 10U/6.3V_6
C78 10U/6.3V_6
C120 10U/6.3V_6
C98 10U/6.3V_6
C87 10U/6.3V_6
C136 10U/6.3V_6
C70 10U/6.3V/X5R_8
C130 10U/6.3V/X5R_8
+0.675V_DDR_VTT
C61 1U/6.3V_4
C45 1U/6.3V_4
C57 1U/6.3V_4
C65 1U/6.3V_4
C43 10U/6.3V_6
C56 *10U/6.3V_6
+SMDDR_VREF_DIMM
C63 0.1U/10V_4
C220 2.2U/6.3V_6
+SMDDR_VREF_DQ0
C264 0.1U/10V_4
C257 2.2U/6.3V_6
+3V
C47 0.1U/10V_4
C48 2.2U/6.3V_6
4/27: layout modify
VREF DQ0 M1 Solution
Place these Caps near So-Dimm0.
INTEL suggestion
+1.35VSUS
R159 1K/F_4
(3) SMDDR_VREF_DQ0_M3
SMDDR_VREF_DQ0_M3
R162 *0_6S
+SMDDR_VREF_DQ0
C265 0.022U/16V_4
R163 1K/F_4
R164 24.9/F_4
PROJECT : M Note
Quanta Computer Inc.
Size Custom
Document Number DDR3 DIMM0-RVS (4.0H)
Rev 1A
Date: 星期六, 五月 25, 2013
Sheet 12 of 61



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (8.0H)	1A
Date: 星期六, 五月 25, 2013	Sheet 13 of 61	



PEX_PLLVDD	120 ohm @100MHz bead
N14P-GV2	0 ohm
N14M-GE	Stuff
N14M-GL	Stuff

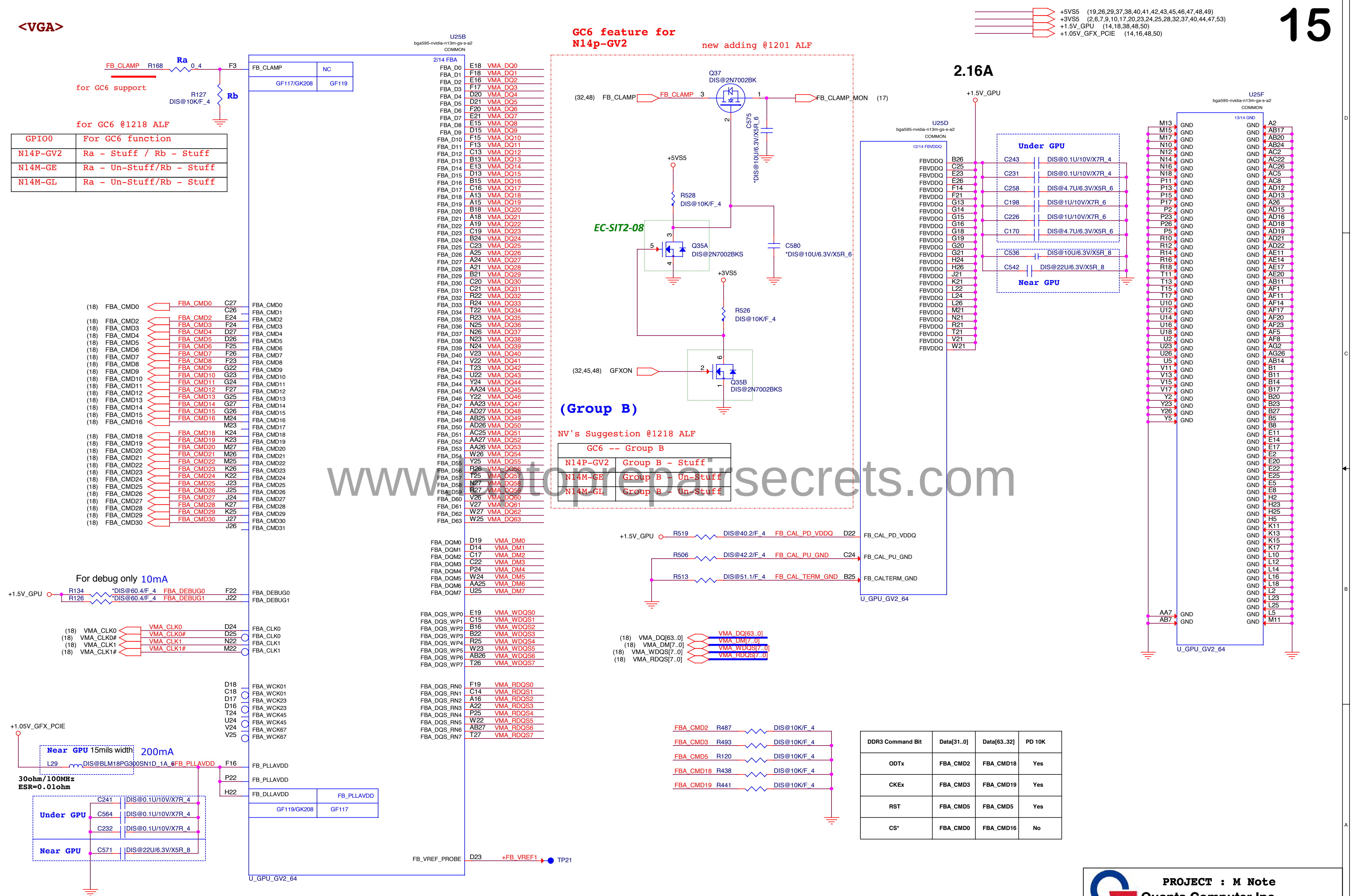
	Group C
N14P-GV2	Group C - Un-Stuff
N14M-GE	Group C - Stuff
N14M-GL	Group C - Stuff

Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
NVVDD	GPU SKU Specific	GPU Core power rail
FBVDD[2]	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ[2]	1.35 V or 1.5 V	VRAM I/O and GPUs Frame Buffer I/O power rail
IFPx_IOVDD[3]	1.05 V or 3.3V	Powers IFP blocks
IFPx_PLLVDD[3]	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX_IOVDD/Q	1.05 V	GPUs PCIE interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD	3.3 V	GPU PCIE PLL Power Rails
PEX_PLLVDD	1.05 V	GPU PCIE PLL Power Rails
FBx_PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FBx_DLL_AVDD (GB2-64 and GB4-128)	1.05 V	Frame Buffer PLL and DLL Power Rail
FBx_PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVDD, GPCPLL_AVDD LXS_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVDD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DACx_VDD[1]	3.3 V	Powers the DAC interfaces
VDD33(NV3V3)[4]	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes:
1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

<VGA>



for GC6 @1218 ALF

GPIO0	For GC6 function
N14P-GV2	Ra - Stuff / Rb - Stuff
N14M-GE	Ra - Un-Stuff/Rb - Stuff
N14M-GL	Ra - Un-Stuff/Rb - Stuff

NV's Suggestion @1218 ALF

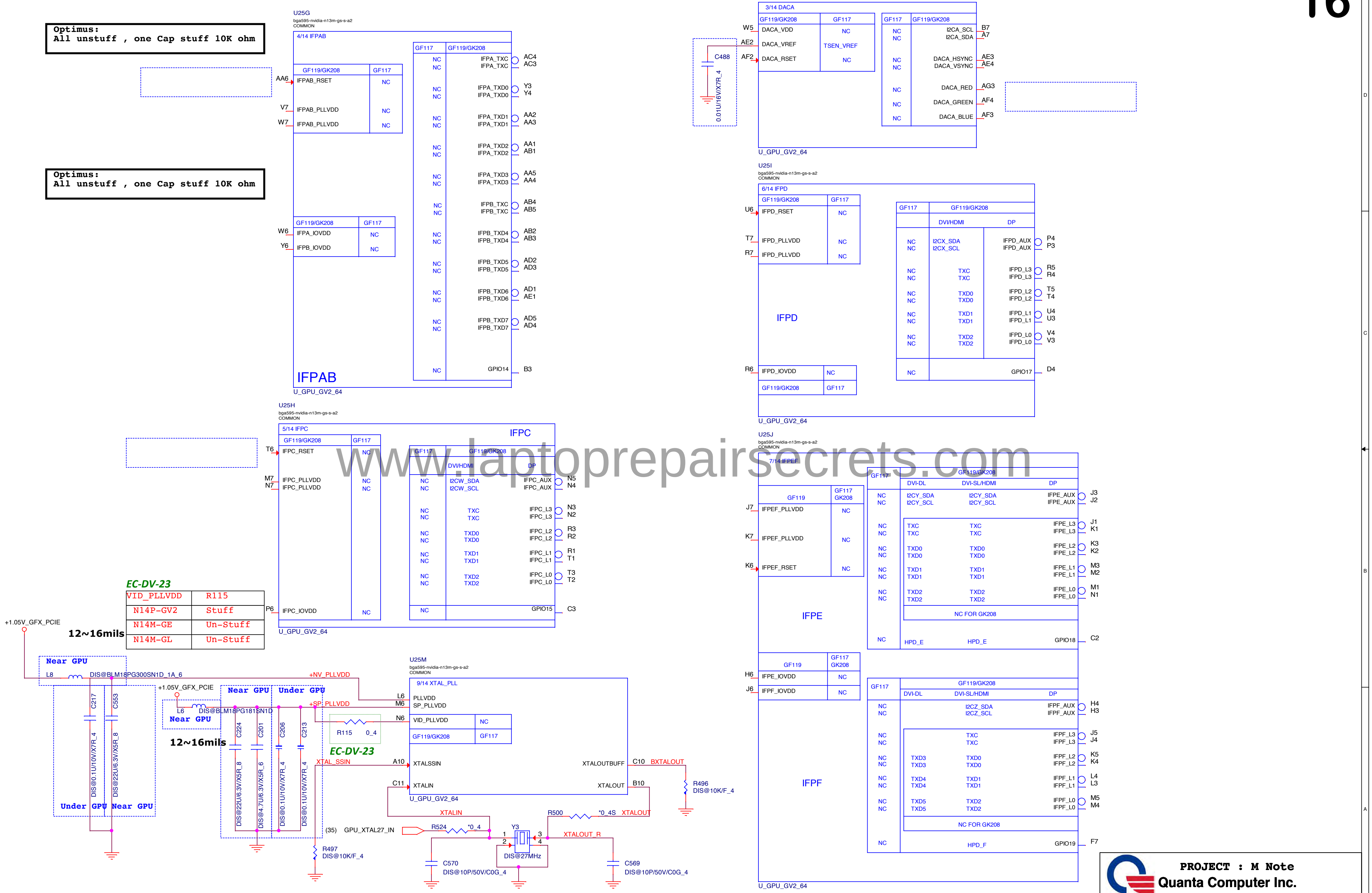
GC6 -- Group B	
N14P-GV2	Group B - Stuff
N14M-GE	Group B - Un-Stuff
N14M-GL	Group B - Un-Stuff

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

<VGA> <HDM> <CRT>

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm



EC-DV-23

VID_PLLVDD	R115
N14P-GV2	Stuff
N14M-GE	Un-Stuff
N14M-GL	Un-Stuff

PROJECT : M Note
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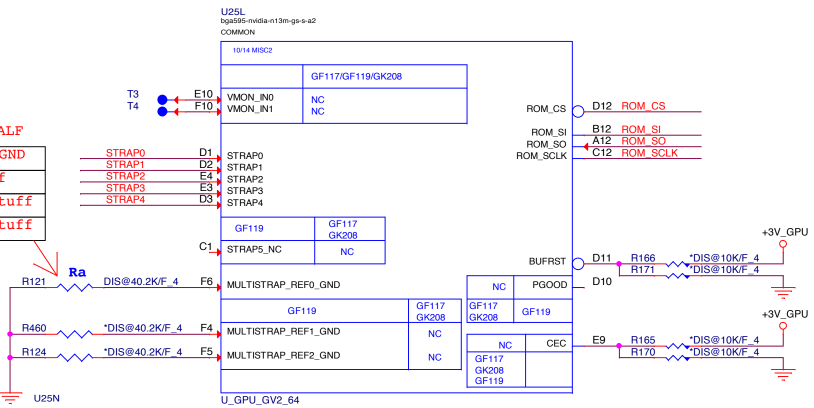
Custom	N14M-GL (DISPLAY) 3/5	1A

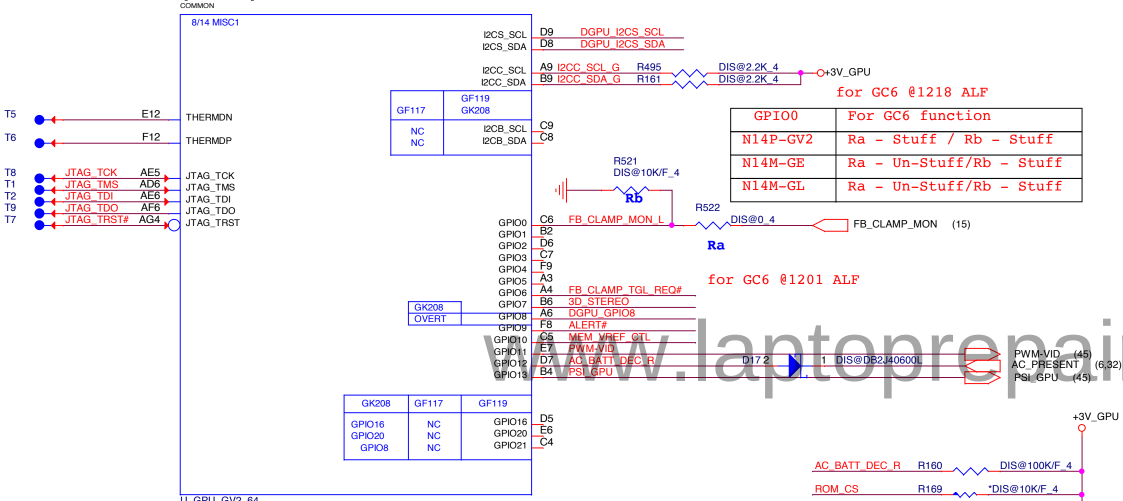
<VGA>

+3VS5 (2,6,7,9,10,15,20,23,24,25,28,32,37,40,44,47,53)
+3V_GPU (14,35,38,45,48,50)

NV's Suggestion @1218 ALF

MULTI_STRAP_REF0_GND	
N14P-GV2	Ra - Stuff
N14M-GE	Ra - Un-Stuff
N14M-GL	Ra - Un-Stuff

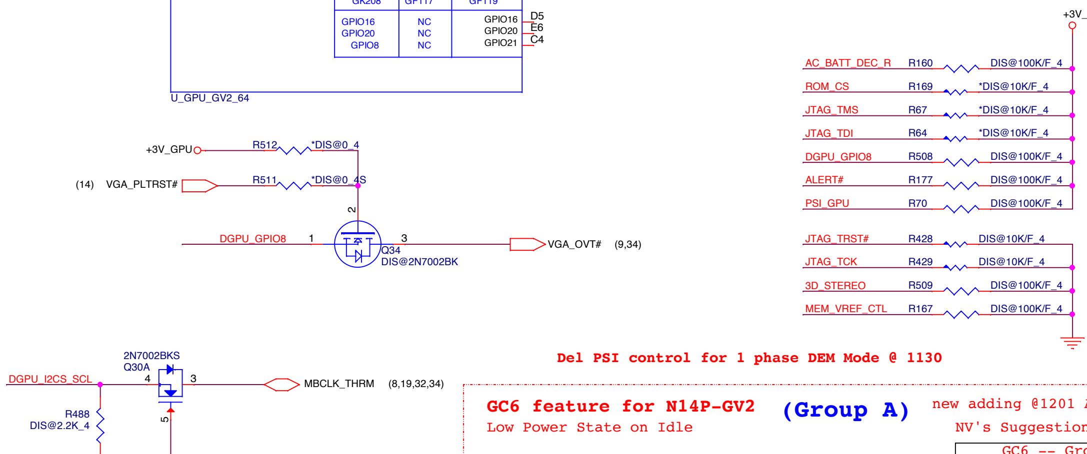


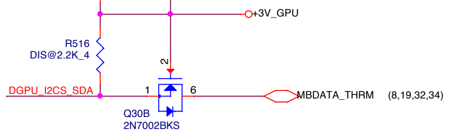


for GC6 @1218 ALF

GPIO0	For GC6 function
N14P-GV2	Ra - Stuff / Rb - Stuff
N14M-GE	Ra - Un-Stuff/Rb - Stuff
N14M-GL	Ra - Un-Stuff/Rb - Stuff

for GC6 @1201 ALF

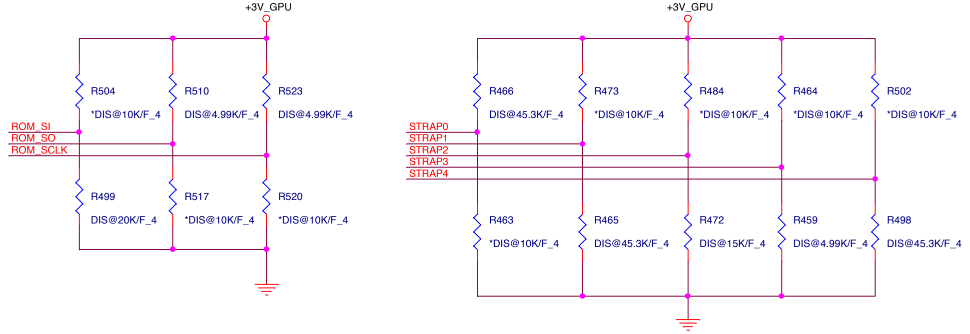




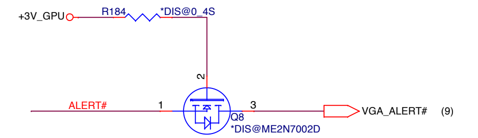
Del PSI control for 1 phase DEM Mode @ 1130

DDR3 RAM_CFG

GPU SKU	GPU	VRAM Vendor	Type		Config	VRAM P/N	Max Speed CLI	D/C Mini	RAM_CFG	Strap 3	Strap 2	Strap 1	Strap 0
GF117	N14M-GE/GL	Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1150	0x1	PD 10K	PD 10K	PD 10K	PU 10K
						MT41K256M16HA-107G:E	900Mhz						
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x5	PD 10K	PU 10K	PD 10K	PU 10K
						K4W2G1646E-BC11	900Mhz						
		Hynix	DDR3	1.5V/1.5V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 10K	PU 10K	PU 10K	PD 10K
						H5TQ2G63DFR-11C	900Mhz						
		Samsung	DDR3	1.5V/1.5V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0xB	PU 10K	PD 10K	PU 10K	PU 10K
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0xD	PU 10K	PU 10K	PD 10K	PU 10K
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63MFR-11C	900Mhz	NA	0x3	PD 10K	PD 10K	PU 10K	PU 10K
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63AFR-11C	900Mhz	NA	0x4	PD 10K	PU 10K	PD 10K	PD 10K



Reserve it for GPIO9 @1222 ALF



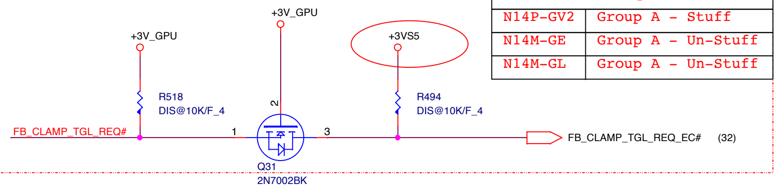
GF117 SKU

Item	N14M-GL-B-A2
Device ID	0x1140
Package	GB4-128
Internal P/N	GF117, 28nm
ROM_SI	10kohm pull down
ROM_SO	10kohm pull down
ROM_SCLK	10kohm pull down
Strap0	Refer to N14x_RAM_Straps table
Strap1	
Strap2	
Strap3	
Strap4	10kohm pull down
NVVDD Boot Voltage	0.9V

GC6 feature for N14P-GV2 (Group A)
Low Power State on Idle

new adding @1201 ALF
NV's Suggestion @1218 ALF

GC6 -- Group A	
N14P-GV2	Group A - Stuff
N14M-GE	Group A - Un-Stuff
N14M-GL	Group A - Un-Stuff



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GL (GPIO/STRAPS) 4/5	1A
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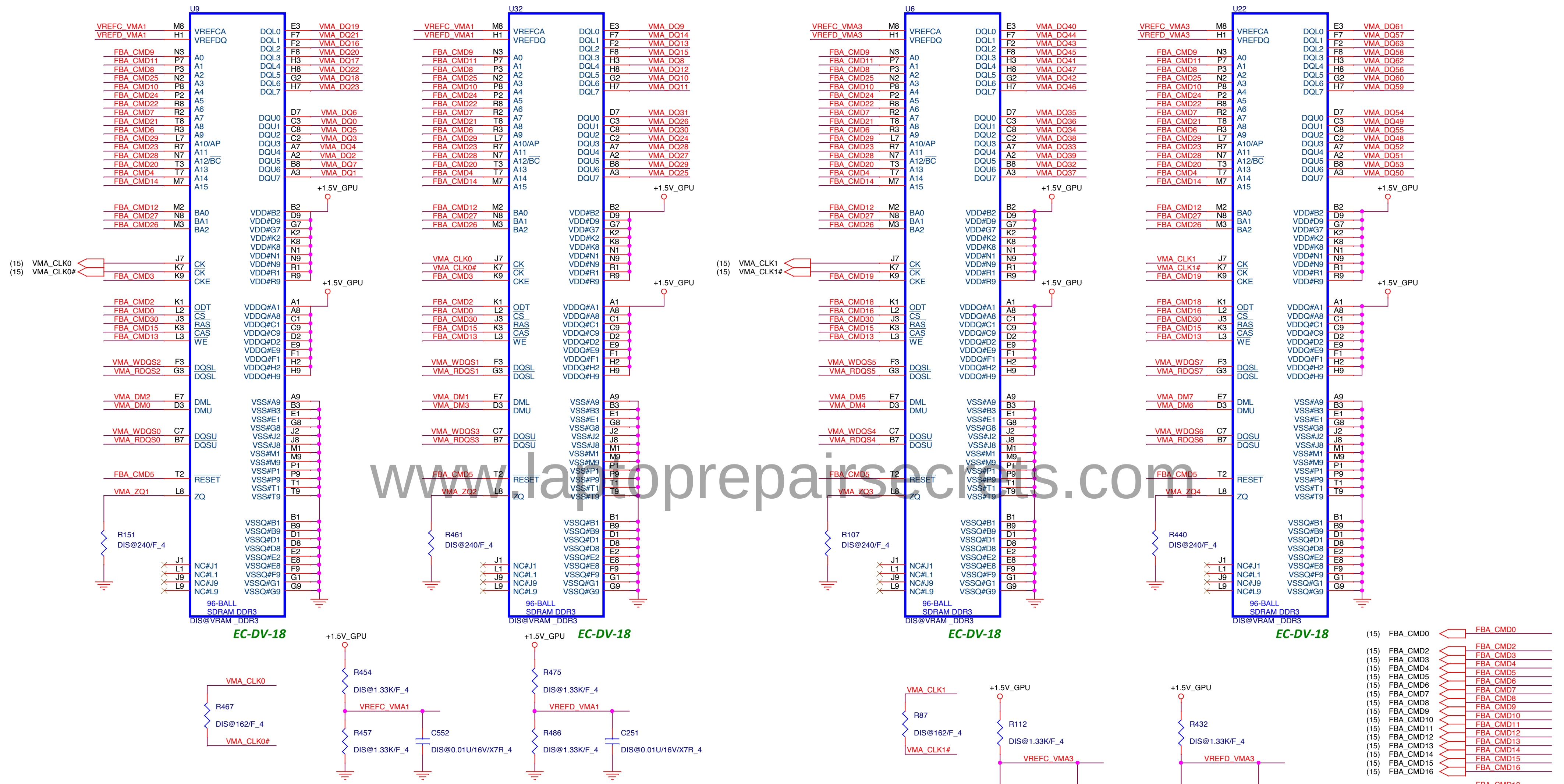
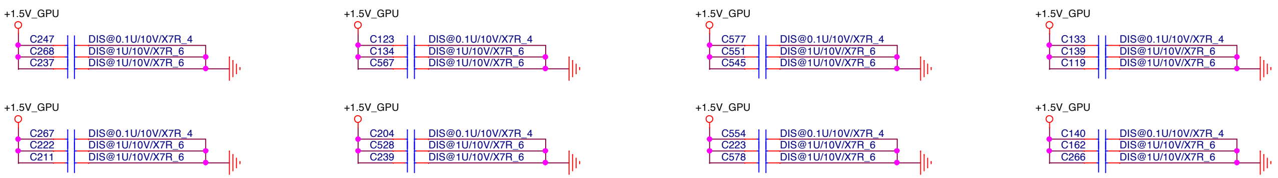
<VGA>

18

CHANNEL A: DDR3 4Gb x4 = 2GB
Double T Topology for DDR3 Memory



REV-00 change R3086 and R3091 from 240/F_4 to160 Ohms



Close to DRAM

PROJECT : M Note
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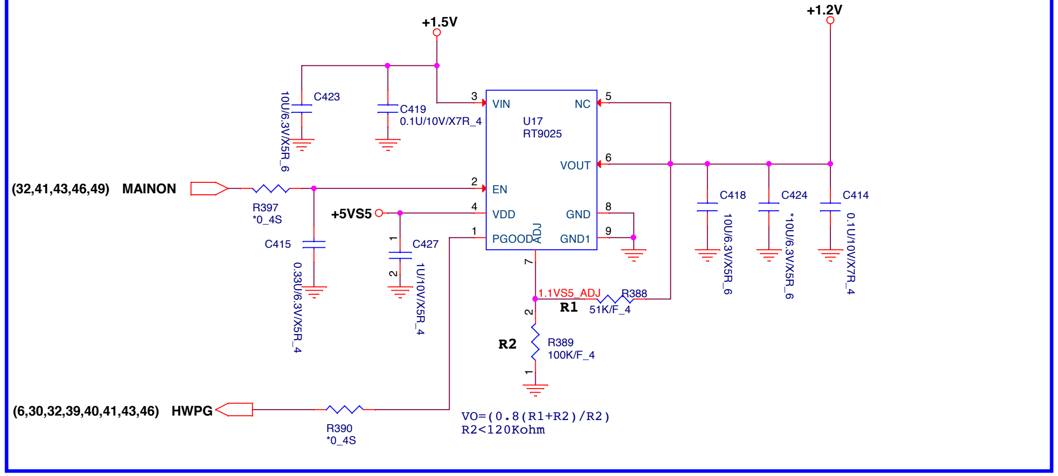
Size	Document Number	Rev
Custom	DDR3 VRAM (BGA96) 5/5	1A

Date: 星期六, 五月 25, 2013 Sheet 18 of 61

+5VS5 (15,26,29,37,38,40,41,42,43,45,46,47,48,49)
+3V (2,6,7,8,9,10,12,13,14,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
+1.5V (6,7,8,10,24,28,46,48,49)
+1.2V

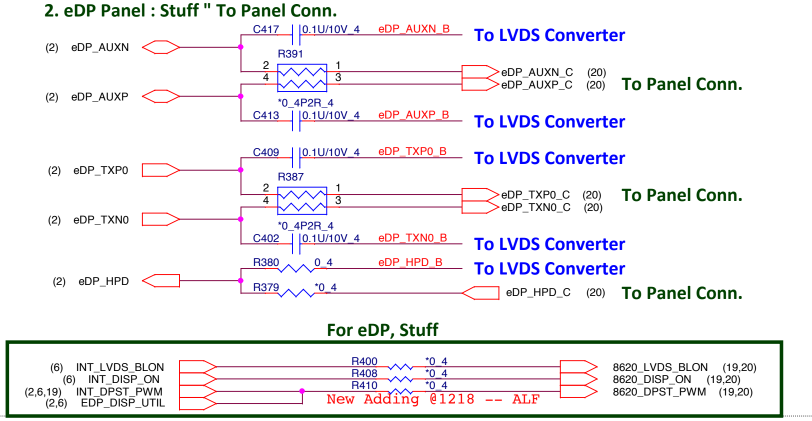
1.2V Power Source

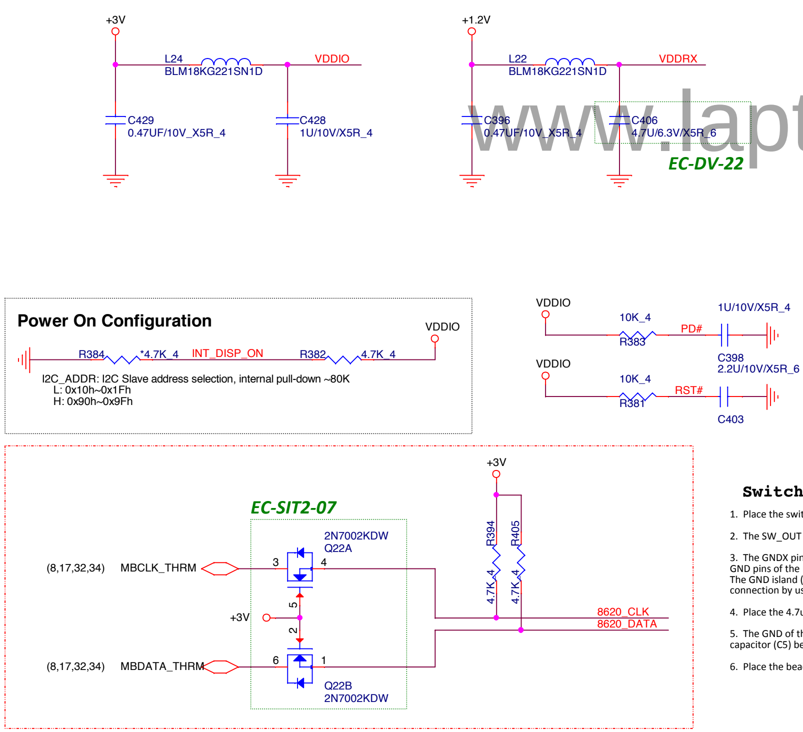
1.2 V +/- 5%
TDC:0.3A(max)

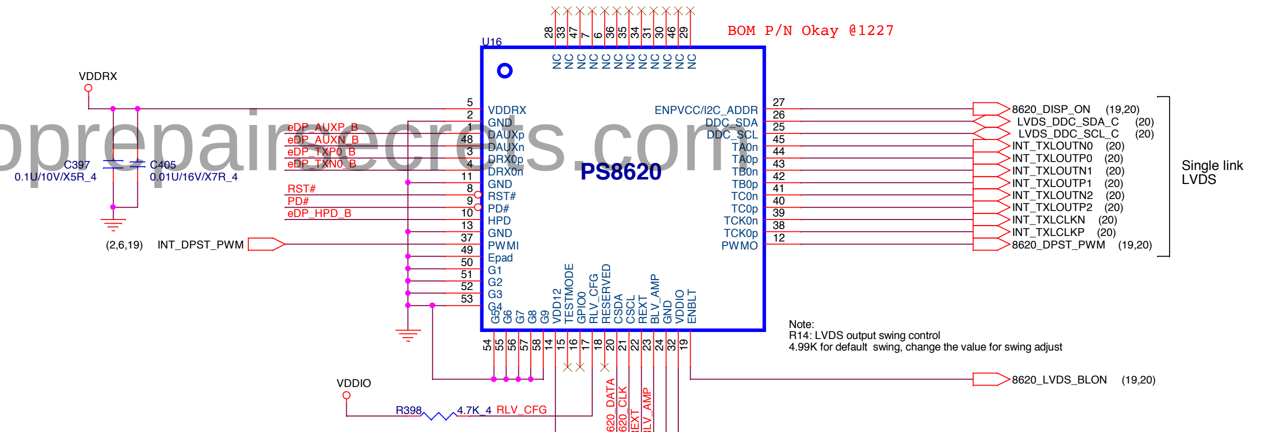


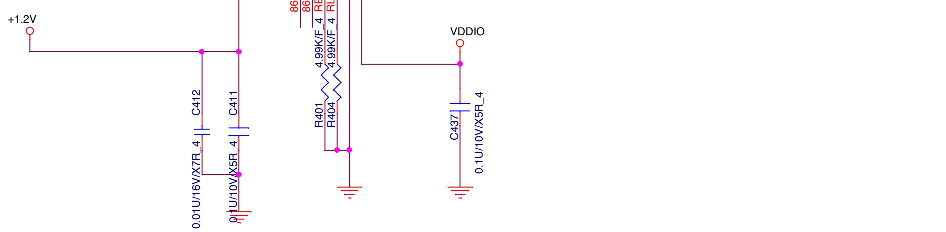
New Adding for eDP and LVDS Panel @1128 -- ALF

For BOM Control:
1. LVDS Panel : Stuff "To LVDS Converter. (Default)
2. eDP Panel : Stuff " To Panel Conn.









Switching Regulator Layout Guideline

1. Place the switching regulator inductor (L3) close to SW_OUT Pin (Pin13).
2. The SW_OUT output traces should be as wide as possible.
3. The GNDX pin (Pin14) should be connected to the main PCB ground plane, with the device GND pins of the PS8622 connected to separate GND island (GNDA) for the device. The GND island (GNDA) should be connected to the main GND plane (GND) with a single-point connection by use of a wide PCB trace.
4. Place the 4.7uF decoupling Capacitor (C4) for VDDIOX close to VDDIOX pin.
5. The GND of the 4.7uF capacitor (C4) should be placed close to the GND of 4.7uF capacitor (C5) behind Inductor.
6. Place the bead (L2) for VDDIOX close to PS8622.

PROJECT : M Note
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Size	Document Number	Rev
Custom	PS8620	1A
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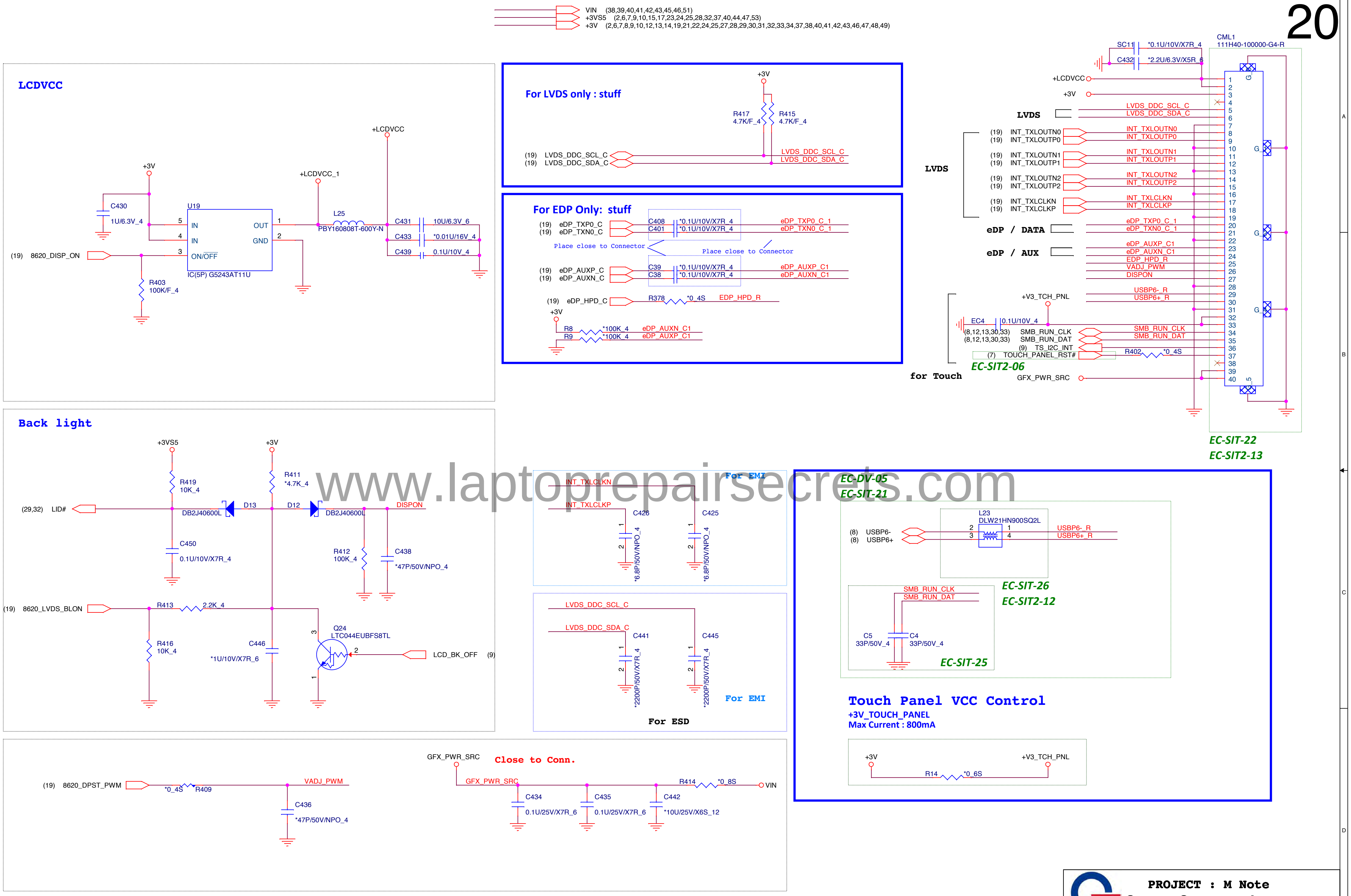

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN / Touch Panel	1A
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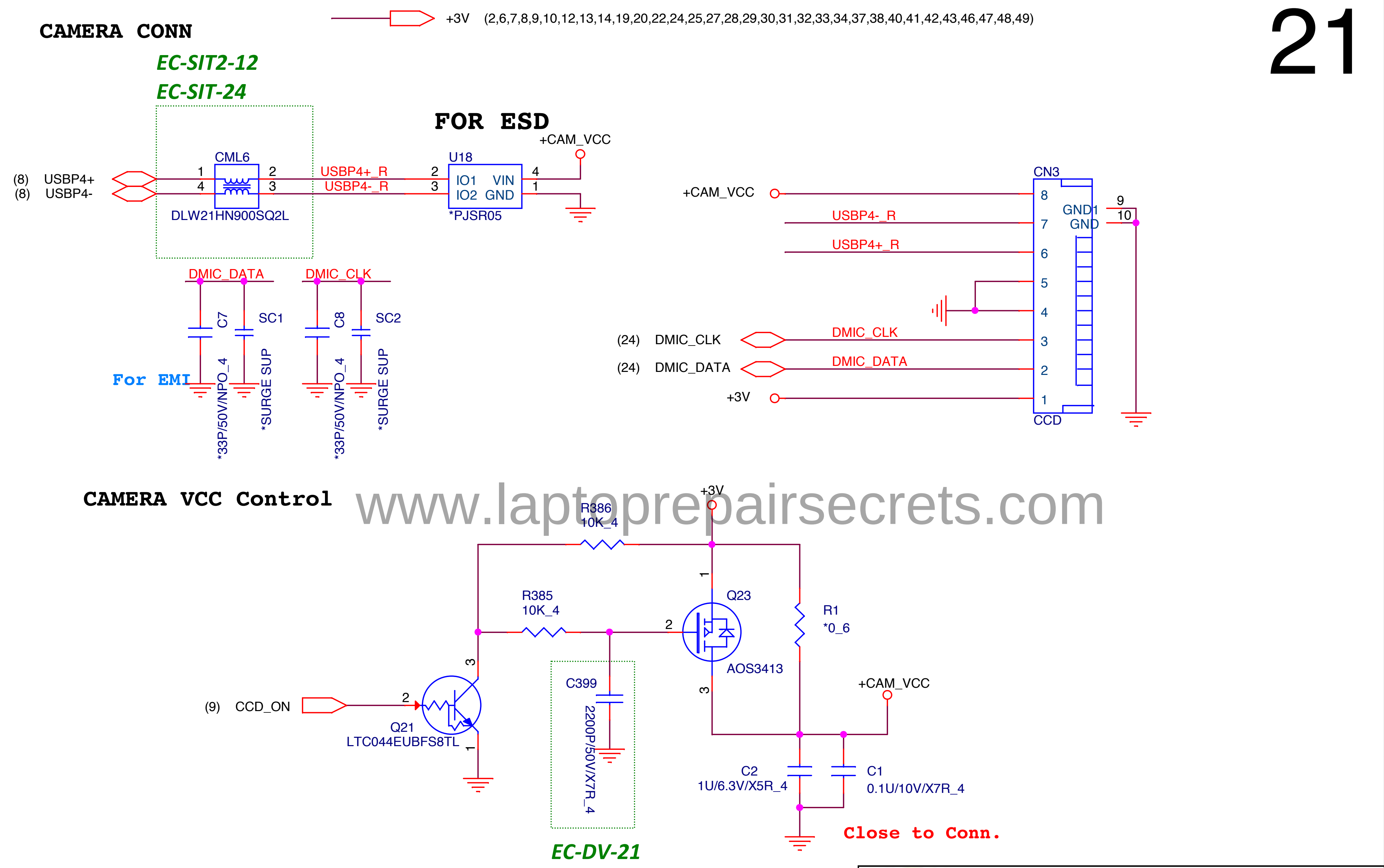

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
A	CAMERA	1A

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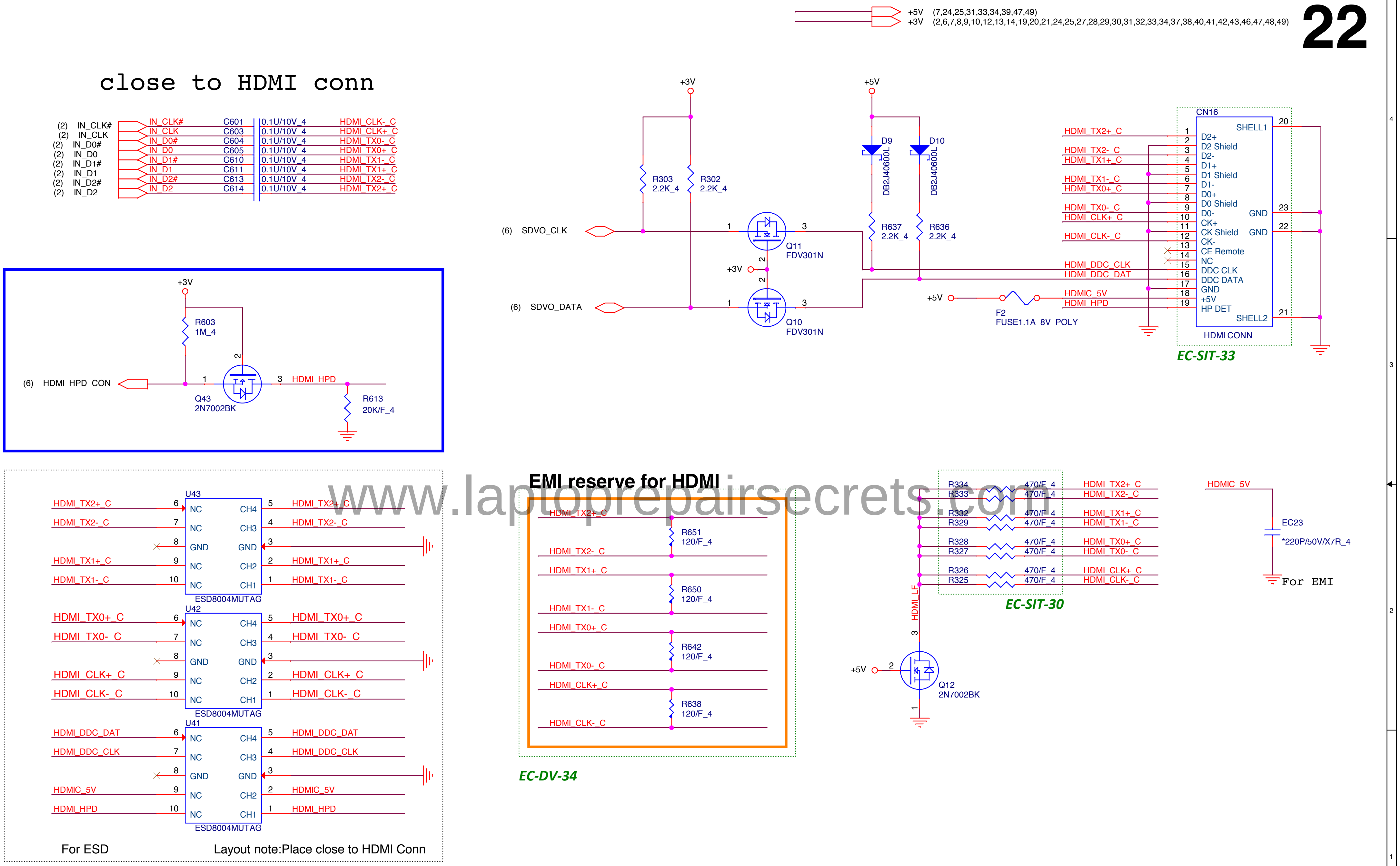

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A
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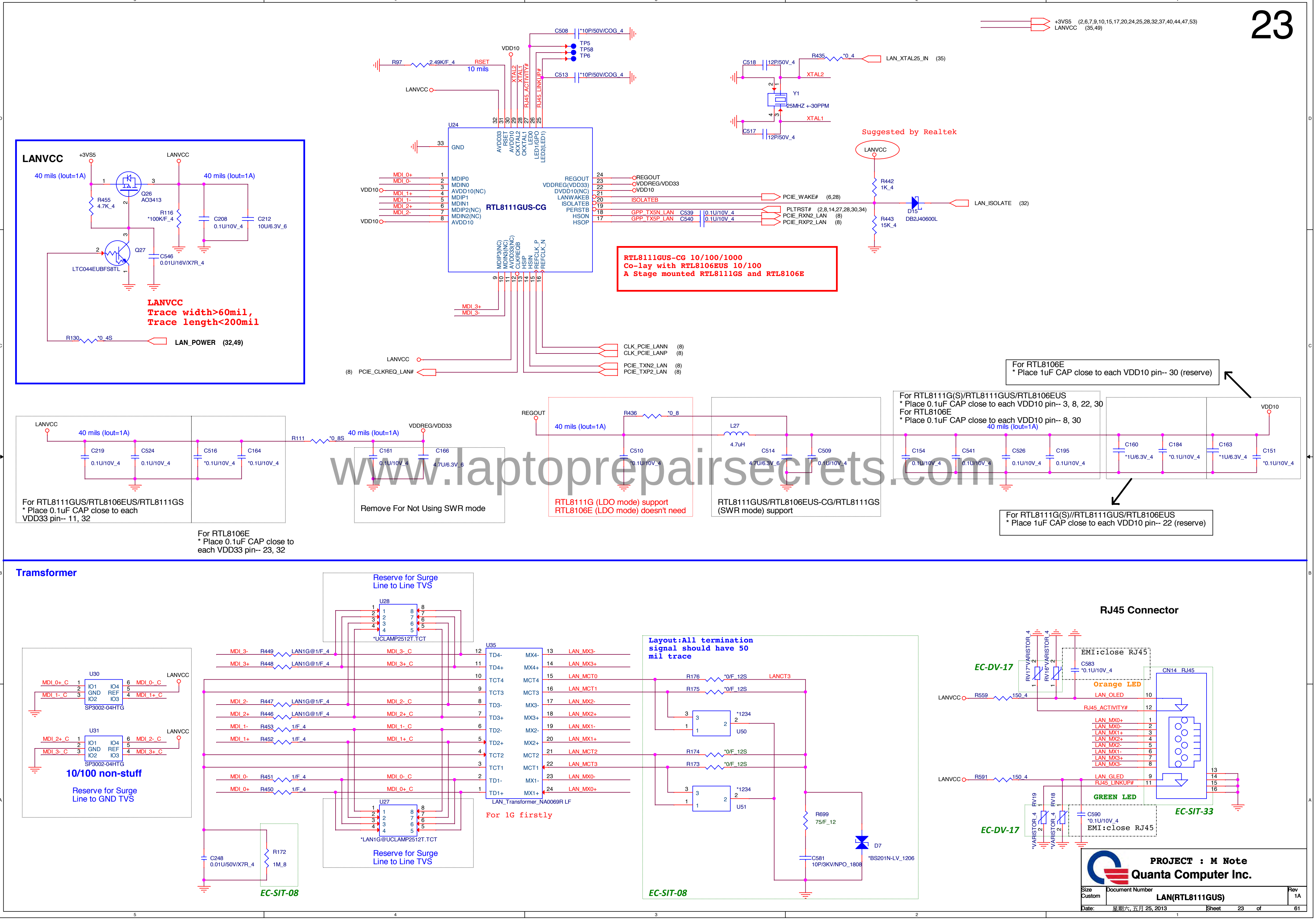
LANVCC
+3VSS
40 mils (Iout=1A)
Q26 AO3413
R455 4.7K_4
R116 *100K/F_4
C208 0.1U/10V_4
C212 10U/6.3V_6
Q27 LTC044EUBFS8TL
C546 0.01U/16V/X7R_4
LANVCC
Trace width>60mil,
Trace length<200mil
R130 *0_4S
LAN_POWER (32,49)
U24
RTL8111GUS-CG
R97 2.49K/F_4 RSET 10 mils
VDD10
C508 *10P/50V/COG_4
TP5 TP58 TP6
C513 *10P/50V/COG_4
XTAL2 XTAL1 RJ45_ACTIVITY# RJ45_LINKUP#
GND
MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10
REGOUT VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP
AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2(LED1)
MDIP3(NC) MDIN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N
MDI_0+ MDI_0- MDI_1+ MDI_1- MDI_2+ MDI_2- MDI_3+ MDI_3-
ISOLATEB
PCIE_WAKE# (6,28)
PLTRST# (2,8,14,27,28,30,34)
GPP_TXSN_LAN C539 0.1U/10V_4 PCIE_RXN2_LAN (8)
GPP_TXSP_LAN C540 0.1U/10V_4 PCIE_RXP2_LAN (8)
CLK_PCIE_LANN (8)
CLK_PCIE_LANP (8)
PCIE_TXN2_LAN (8)
PCIE_TXP2_LAN (8)
(8) PCIE_CLKREQ_LAN#
RTL8111GUS-CG 10/100/1000
Co-lay with RTL8106EUS 10/100
A Stage mounted RTL8111GS and RTL8106E
+3VSS (2,6,7,9,10,15,17,20,24,25,28,32,37,40,44,47,53)
LANVCC (35,49)
C518 12P/50V_4
R435 *0_4
LAN_XTAL25_IN (35)
XTAL2
Y1 25MHZ +-30PPM
XTAL1
C517 12P/50V_4
Suggested by Realtek
R442 1K_4
R443 15K_4
D15 DB2J40600L
LAN_ISOLATE (32)
For RTL8106E
* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)
C219 0.1U/10V_4
C524 0.1U/10V_4
C516 *0.1U/10V_4
C164 *0.1U/10V_4
R111 *0_8S
VDDREG/VDD33
C161 0.1U/10V_4
C166 4.7U/6.3V_6
REGOUT
R436 *0_8
C510 *0.1U/10V_4
L27 4.7uH
C514 4.7U/6.3V_6
C509 0.1U/10V_4
For RTL8111G(S)/RTL8111GUS/RTL8106EUS
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30
For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
C154 0.1U/10V_4
C541 0.1U/10V_4
C526 0.1U/10V_4
C195 0.1U/10V_4
C160 *1U/6.3V_4
C184 *0.1U/10V_4
C163 *1U/6.3V_4
C151 *0.1U/10V_4
For RTL8111GUS/RTL8106EUS/RTL8111GS
* Place 0.1uF CAP close to each
VDD33 pin-- 11, 32
For RTL8106E
* Place 0.1uF CAP close to
each VDD33 pin-- 23, 32
Remove For Not Using SWR mode
RTL8111G (LDO mode) support
RTL8106E (LDO mode) doesn't need
RTL8111GUS/RTL8106EUS-CG/RTL8111GS
(SWR mode) support
For RTL8111G(S)//RTL8111GUS/RTL8106EUS
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)
Tramsformer
U30 SP3002-04HTG
U31 SP3002-04HTG
10/100 non-stuff
Reserve for Surge
Line to GND TVS
Reserve for Surge
Line to Line TVS
U28 *UCLAMP2512T.TCT
U27 *LAN1G@UCLAMP2512T.TCT
U35 LAN_Transformer_NA0069R LF
TD4- TD4+ TCT4 TCT3 TD3- TD3+ TD2- TD2+ TCT2 TCT1 TD1- TD1+
MX4- MX4+ MCT4 MCT3 MX3- MX3+ MX2- MX2+ MCT2 MCT1 MX1- MX1+
R449 R448 R447 R446 LAN1G@1/F_4
R453 R452 R451 R450 1/F_4
LAN_MX3- LAN_MX3+ LAN_MCT0 LAN_MCT1 LAN_MX2- LAN_MX2+ LAN_MX1- LAN_MX1+ LAN_MCT2 LAN_MCT3 LAN_MX0- LAN_MX0+
For 1G firstly
C248 0.01U/50V/X7R_4
R172 1M_8
EC-SIT-08
Layout:All termination
signal should have 50
mil trace
R176 *0/F_12S LANCT3
R175 *0/F_12S
R174 *0/F_12S
R173 *0/F_12S
U50 *1234
U51 *1234
R699 75/F_12
C581 10P/3KV/NPO_1808
D7 *BS201N-LV_1206
EC-SIT-08
RJ45 Connector
EC-DV-17
RV17 *VARISTOR_4
RV16 *VARISTOR_4
EMI:close RJ45
C583 *0.1U/10V_4
CN14 RJ45
Orange LED
R559 150_4
LAN_OLED
RJ45_ACTIVITY#
LAN_GLED
RJ45_LINKUP#
R591 150_4
GREEN LED
RV19 RV18 *VARISTOR_4
C590 *0.1U/10V_4
EMI:close RJ45
EC-DV-17
EC-SIT-33
PROJECT : M Note
Quanta Computer Inc.
Size Custom
Document Number
LAN(RTL8111GUS)
Rev 1A
Date: 星期六, 五月 25, 2013
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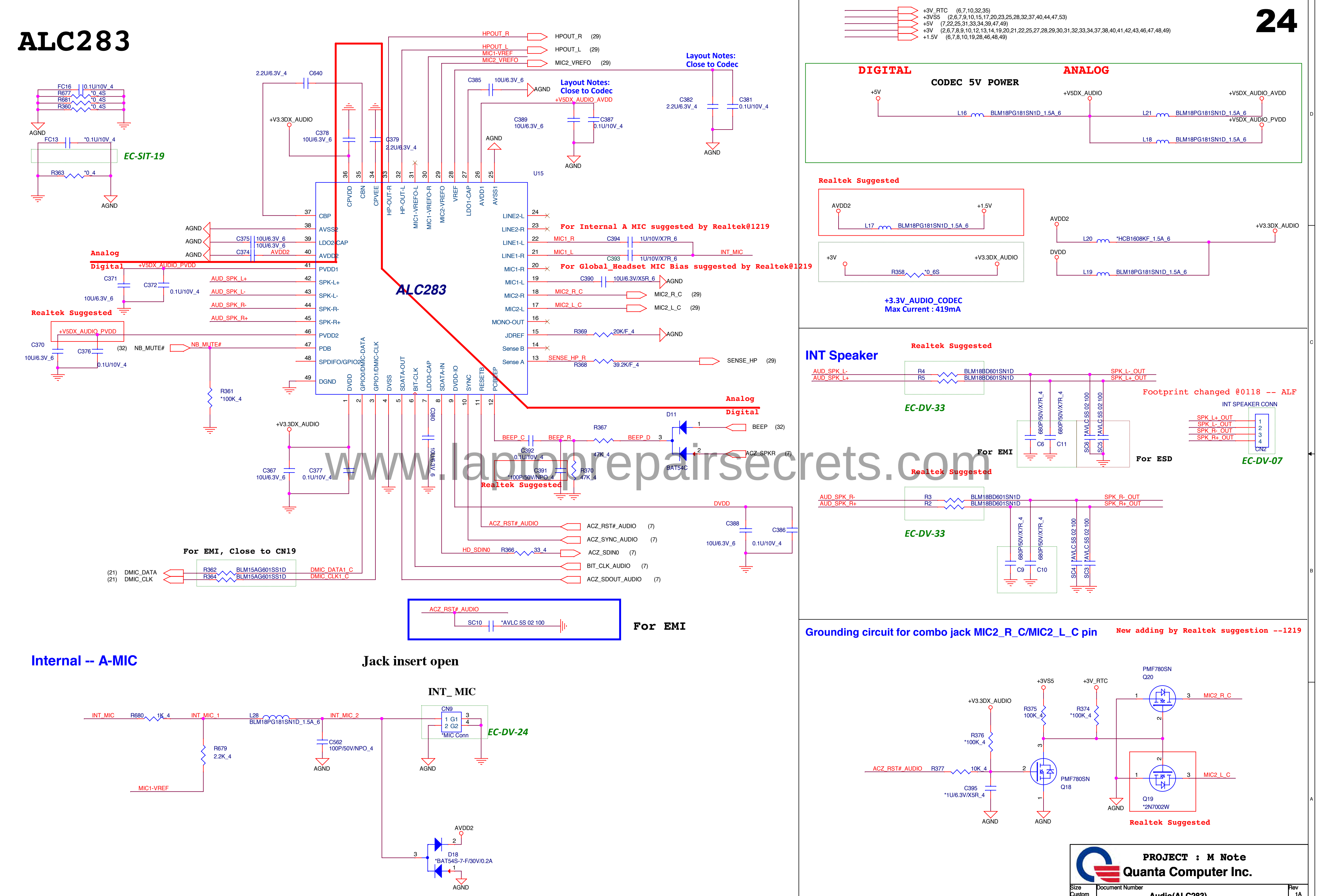
ALC283



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio(ALC283)	1A

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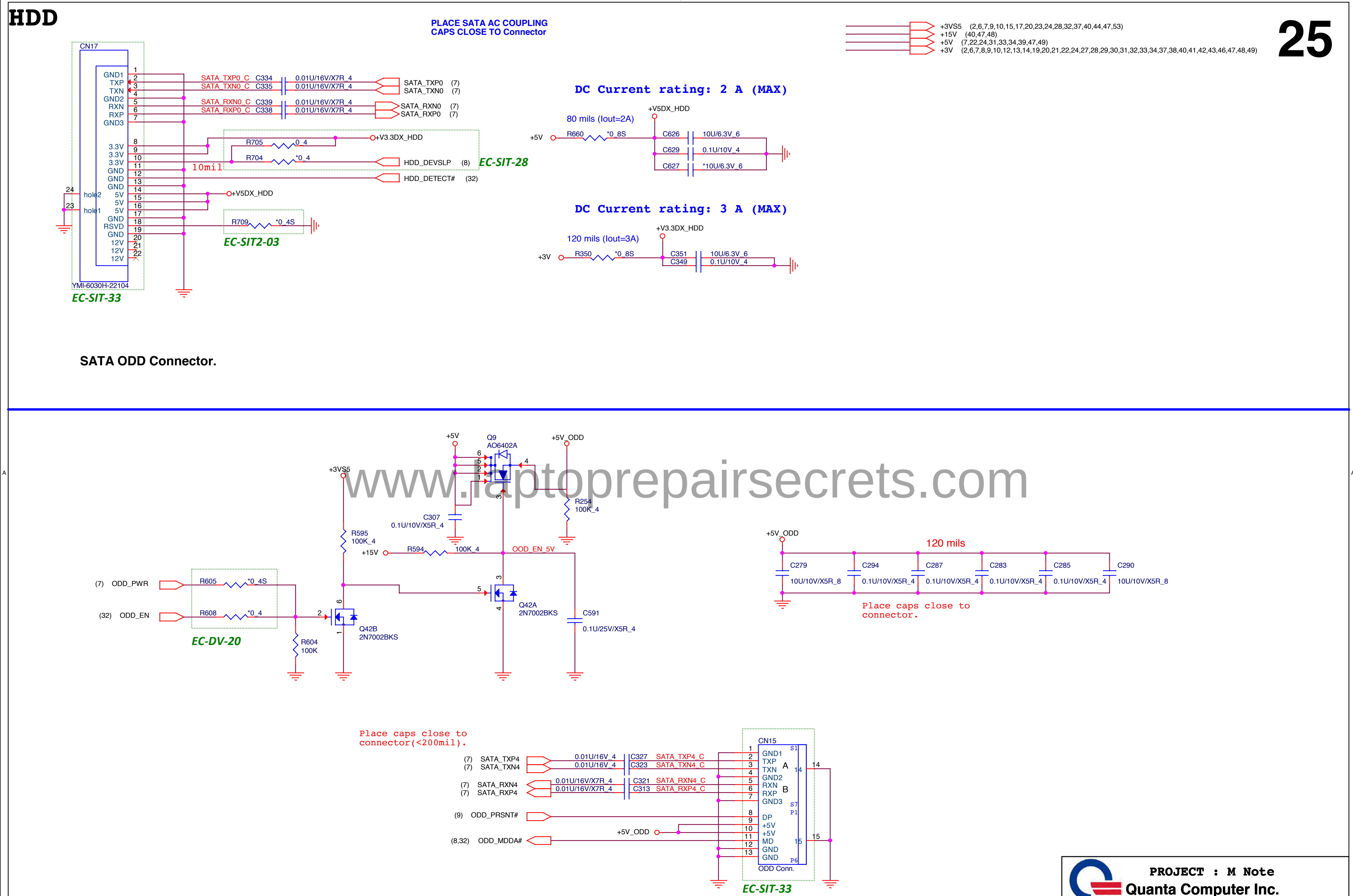
HDD



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA-HDD	1A

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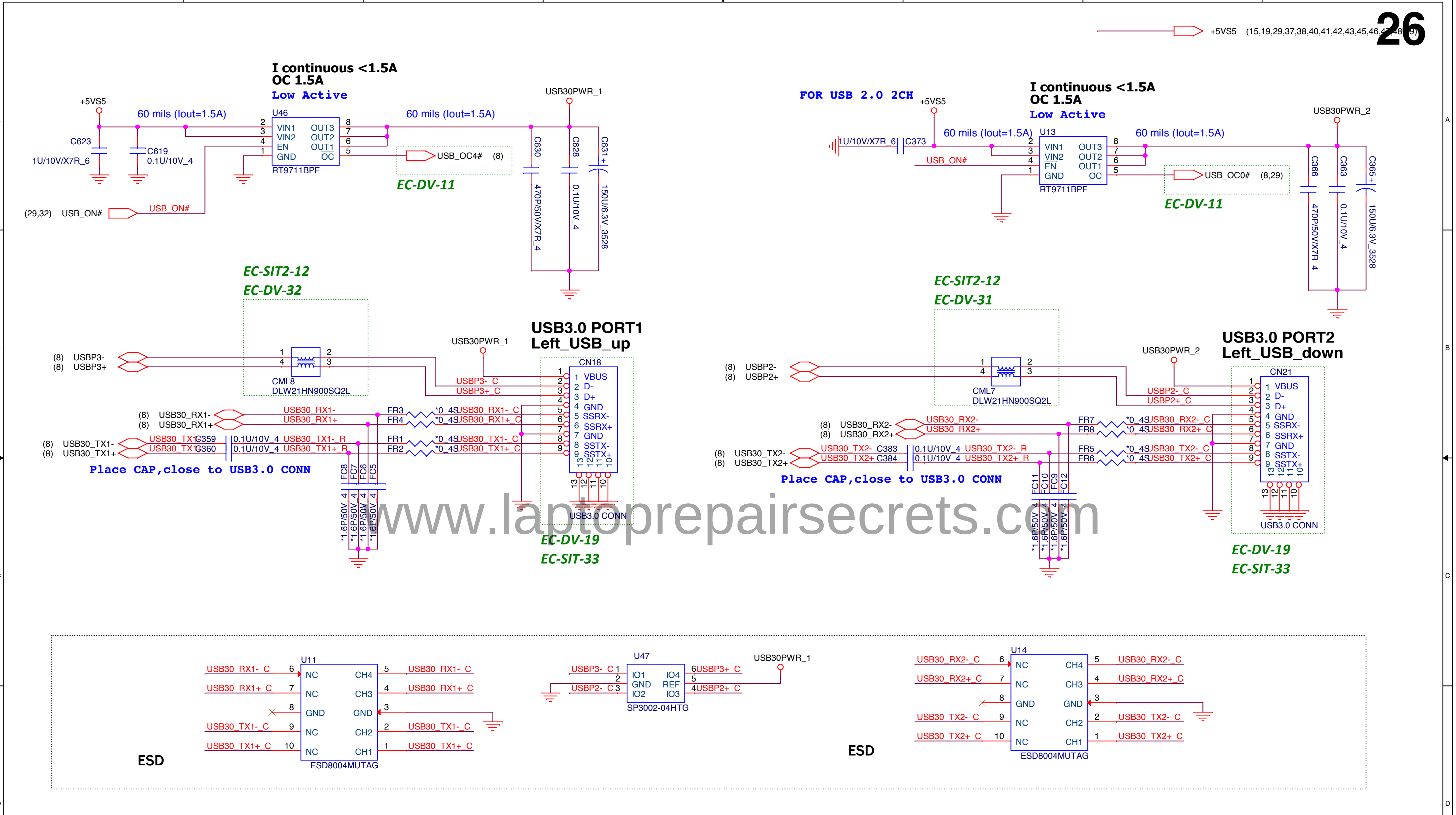

PROJECT : M Note

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Size	Document Number	Rev
B	USB3.0 x2	1A

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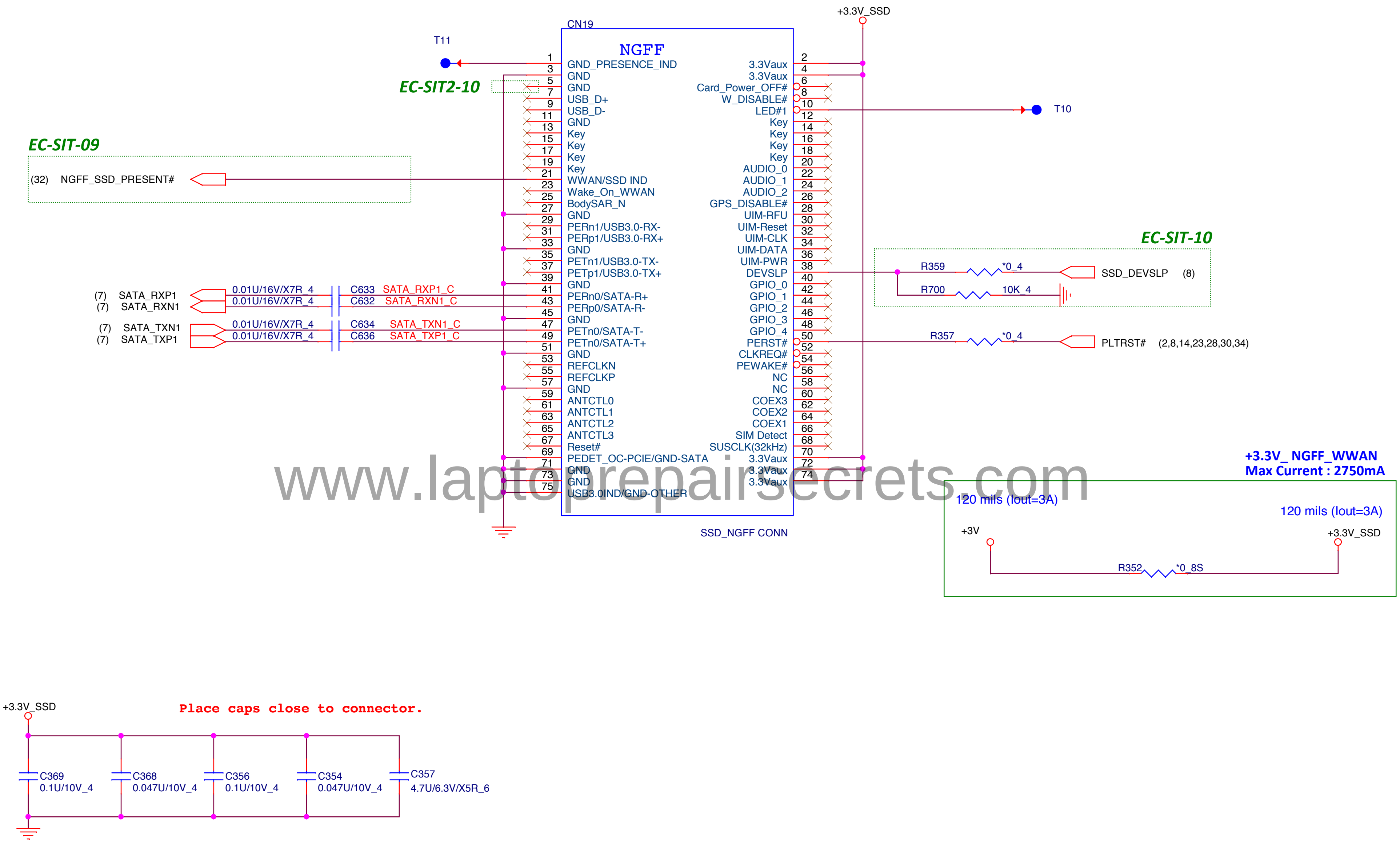
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

NGFF SSD connector

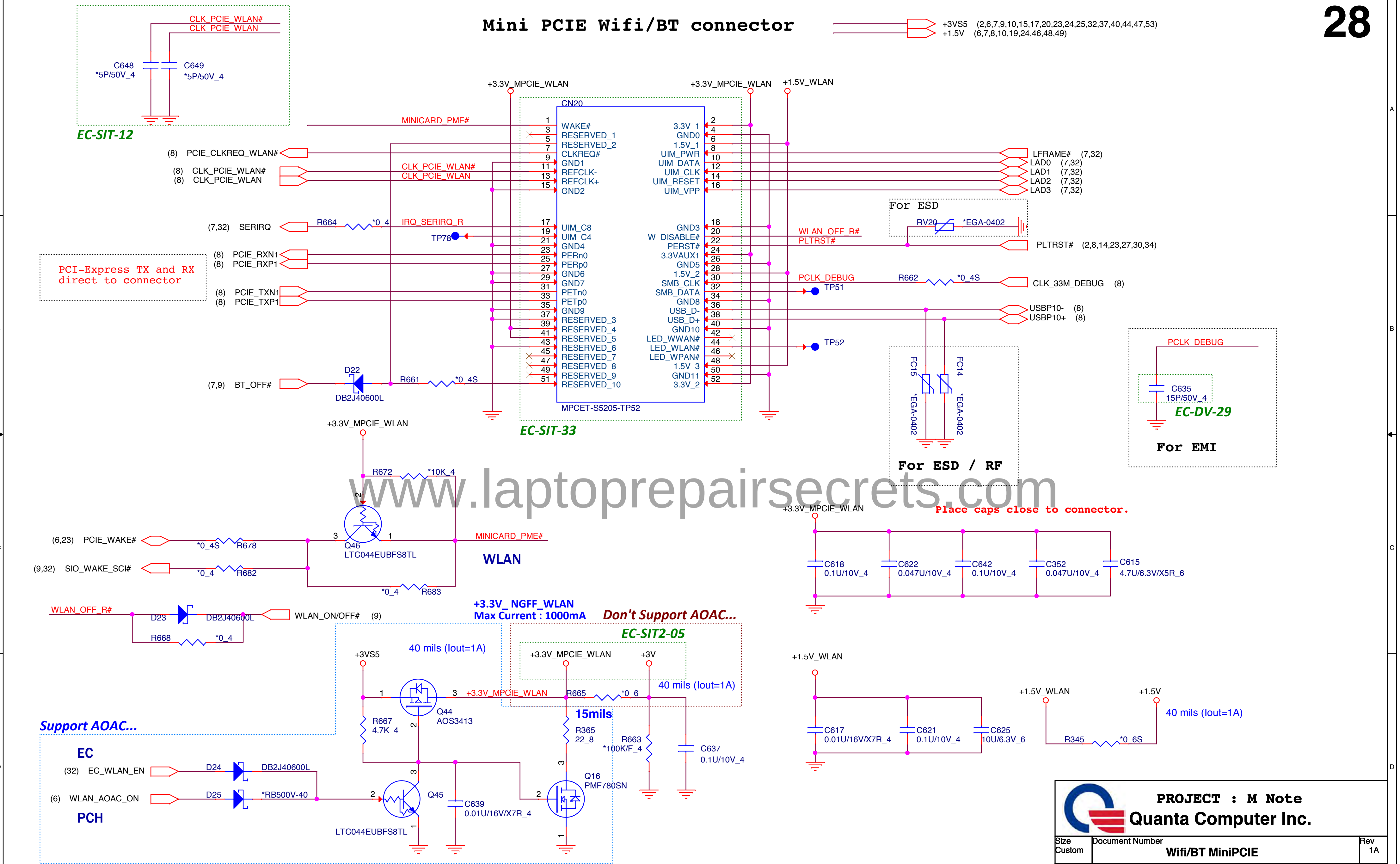


PROJECT : M Note

Quanta Computer Inc.

Size Custom	Document Number SSD NGFF	Rev 1A
Date: 星期六, 五月 25, 2013	Sheet 27 of 61	

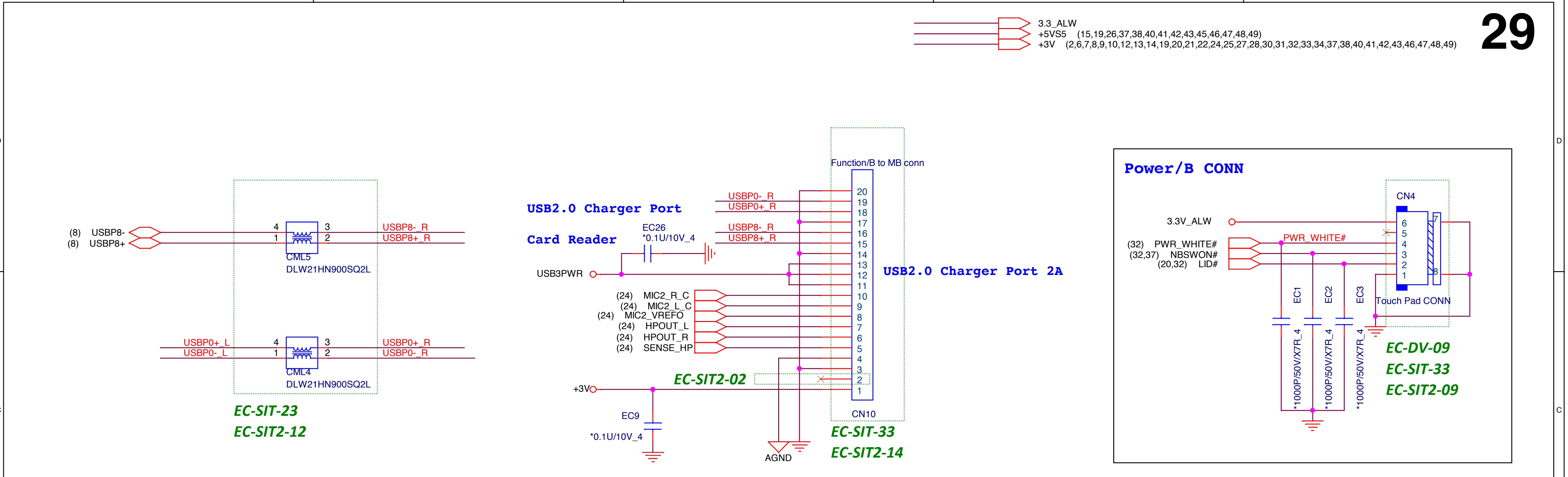
Mini PCIE Wifi/BT connector

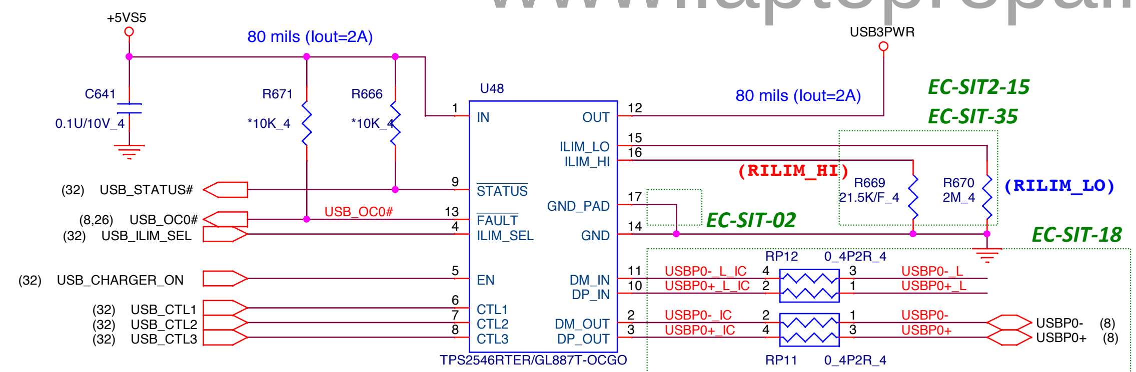


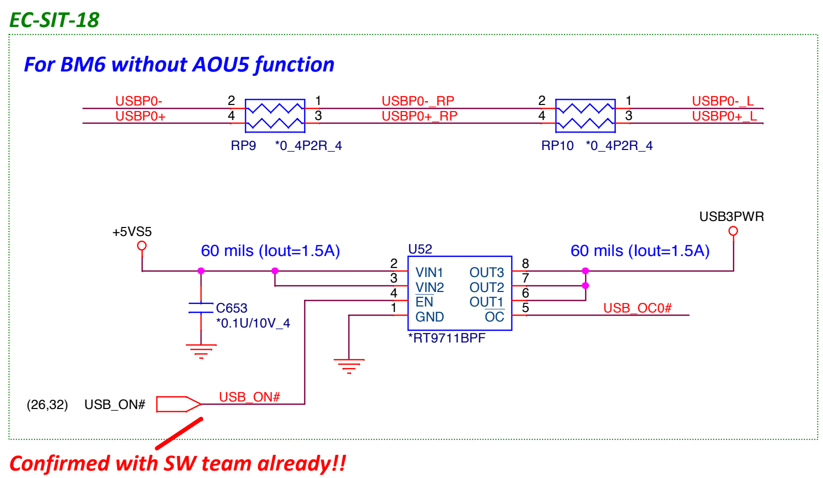
PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Wifi/BT MiniPCIE	1A
Date: 星期六, 五月 25, 2013	Sheet 28 of 61	







RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use
RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

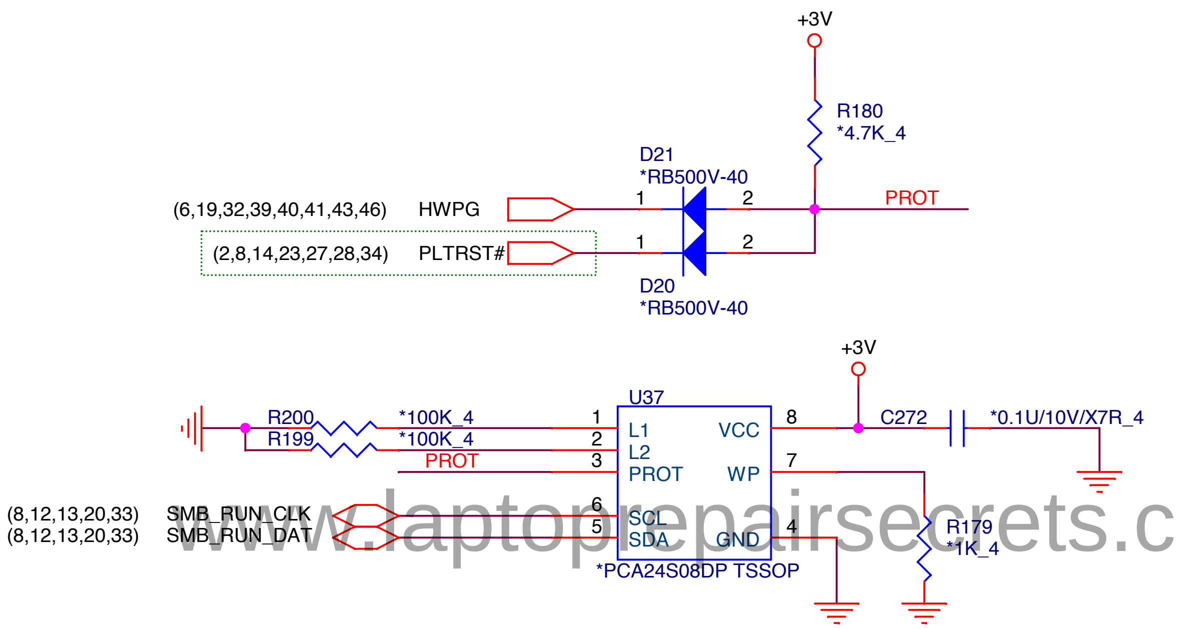
$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0--Audio Jack Conn	1A
Date: 星期六, 五月 25, 2013	Sheet 29 of 61	

RFID

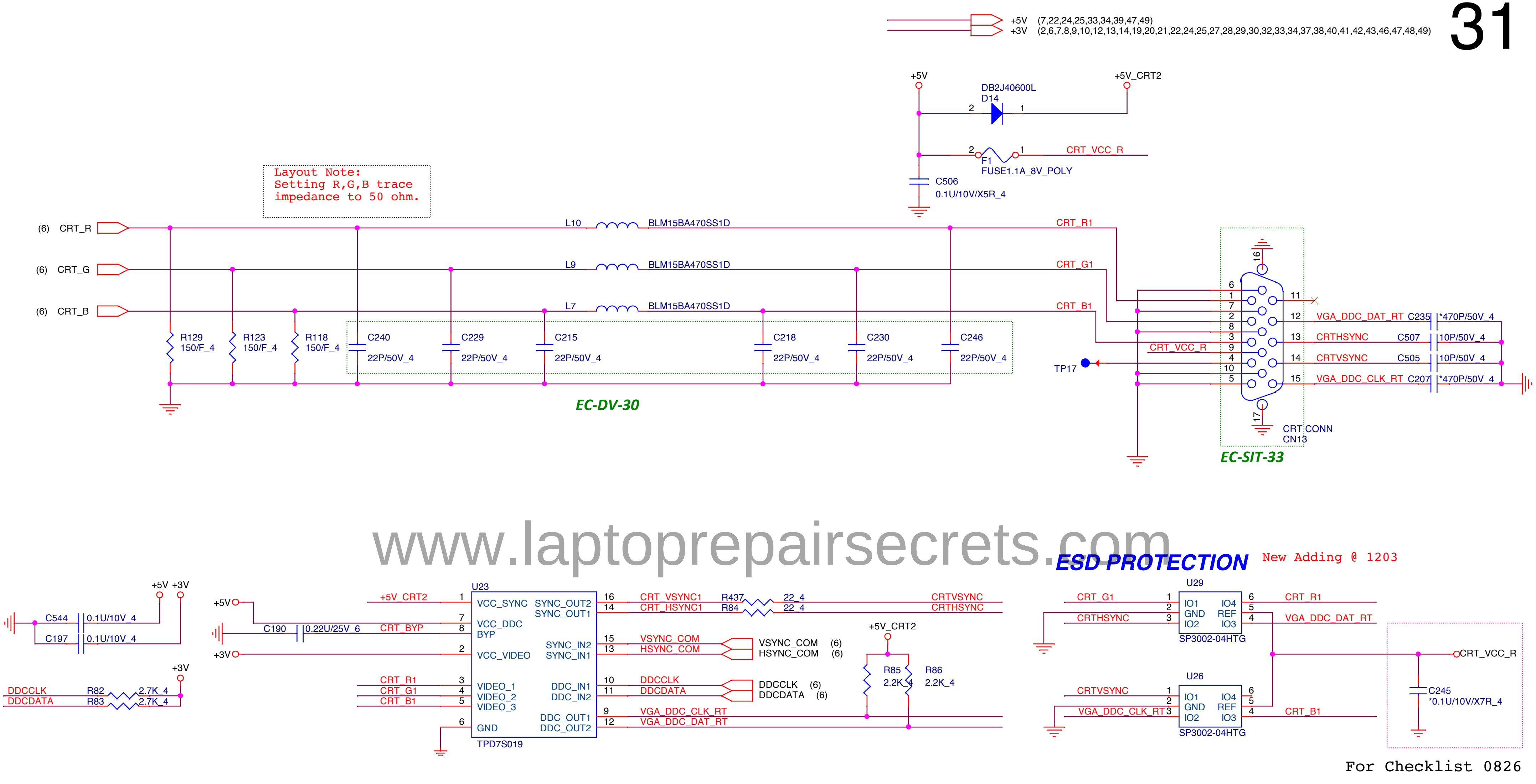
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,31,32,33,34,37,38,40,41,42,43,46,47,48,49)



PROJECT : M Note

Quanta Computer Inc.

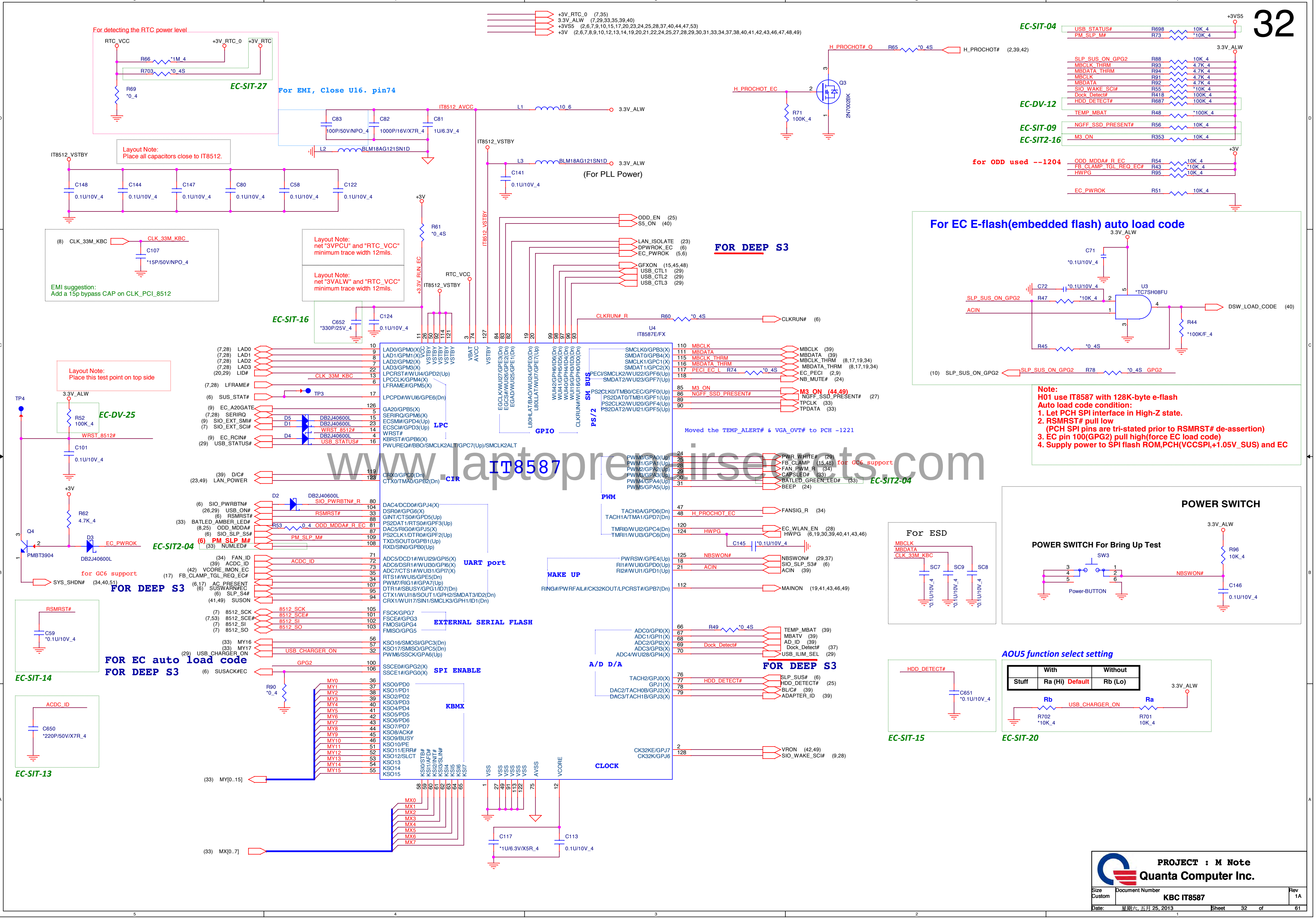
Size	Document Number	Rev
A	RFID	1A
Date: 星期六, 五月 25, 2013	Sheet 30 of 61	



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
B	CRT	1A

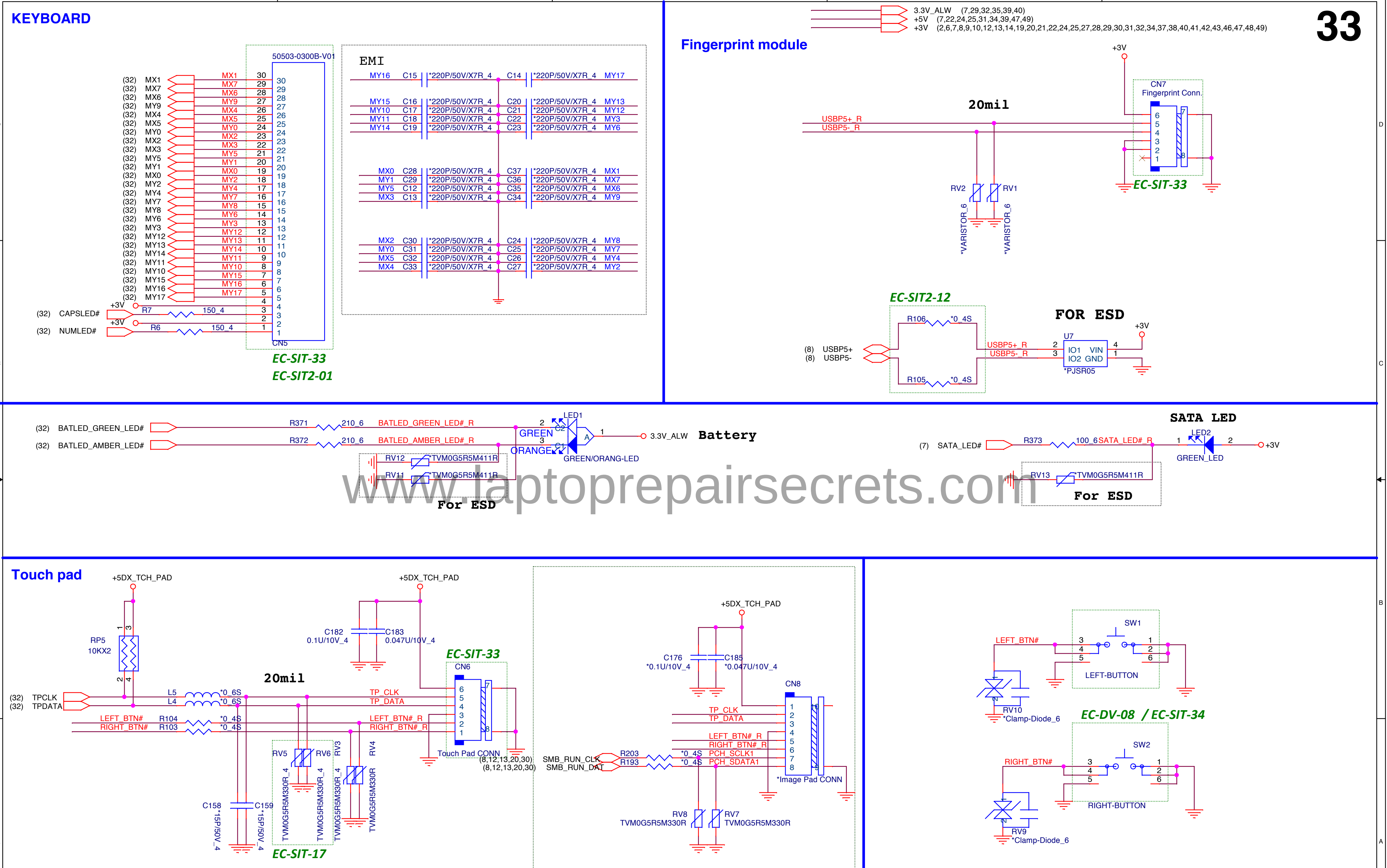
Date: 星期六, 五月 25, 2013 Sheet 31 of 61



	With	Without
Stuff	Ra (Hi) Default	Rb (Lo)

PROJECT : M Note
Quanta Computer Inc.

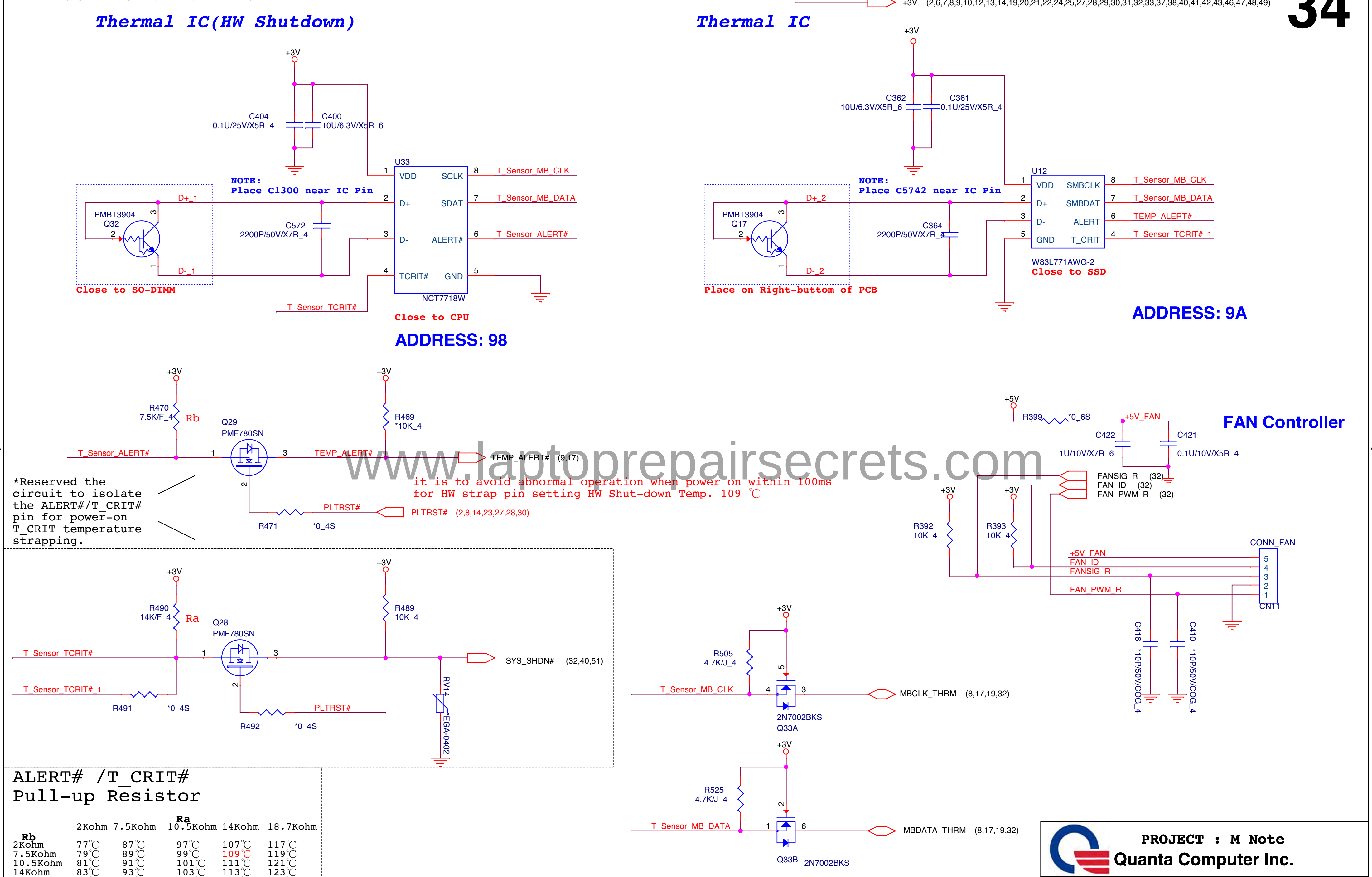
Size: Custom | Document Number: KBC IT8587 | Rev: 1A



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/TP/LID	1A
Date: 星期六, 五月 25, 2013	Sheet 33 of 61	

FAN CONTROL & Thermal IC



ALERT# /T_CRIT# Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

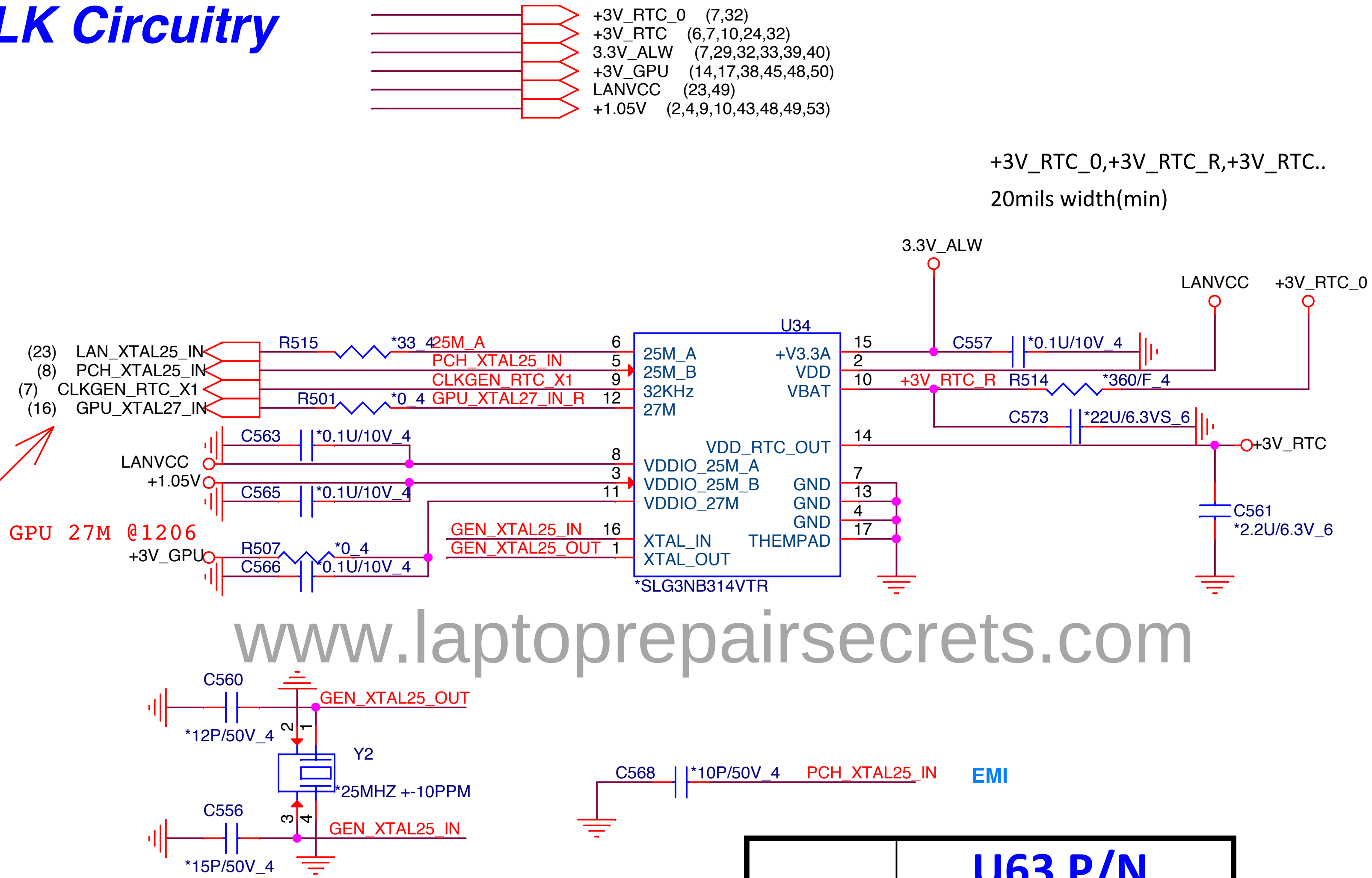
PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN/Thermal	1A

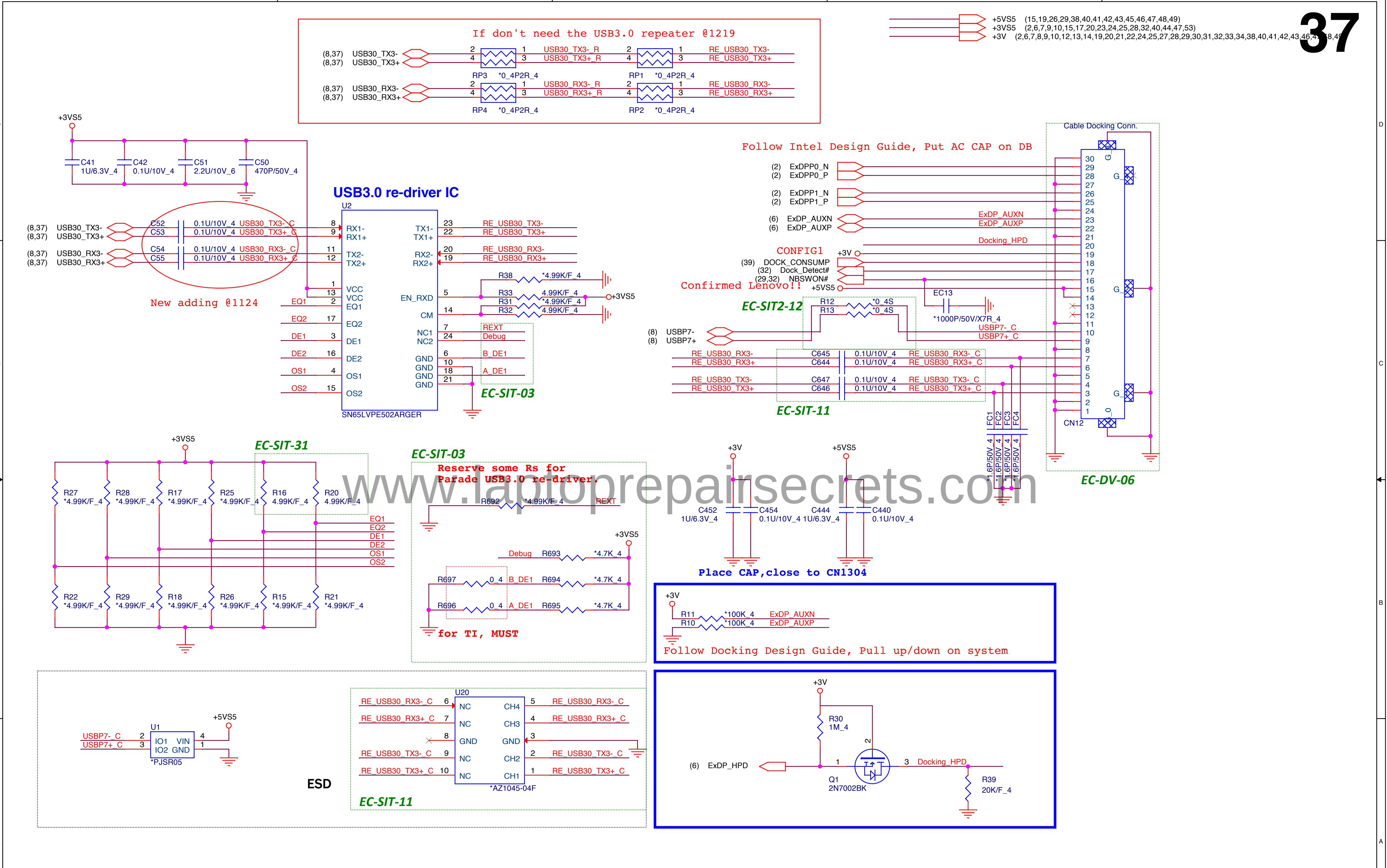
Date: 星期六, 五月 25, 2013 Sheet 34 of 61

Green CLK Circuitry



	U63 P/N
DIS	AL000314000
UMA	AL3NB244000

DIS
32Kx1+25M*2+27Mx1
UMA
32Kx1+25M*2

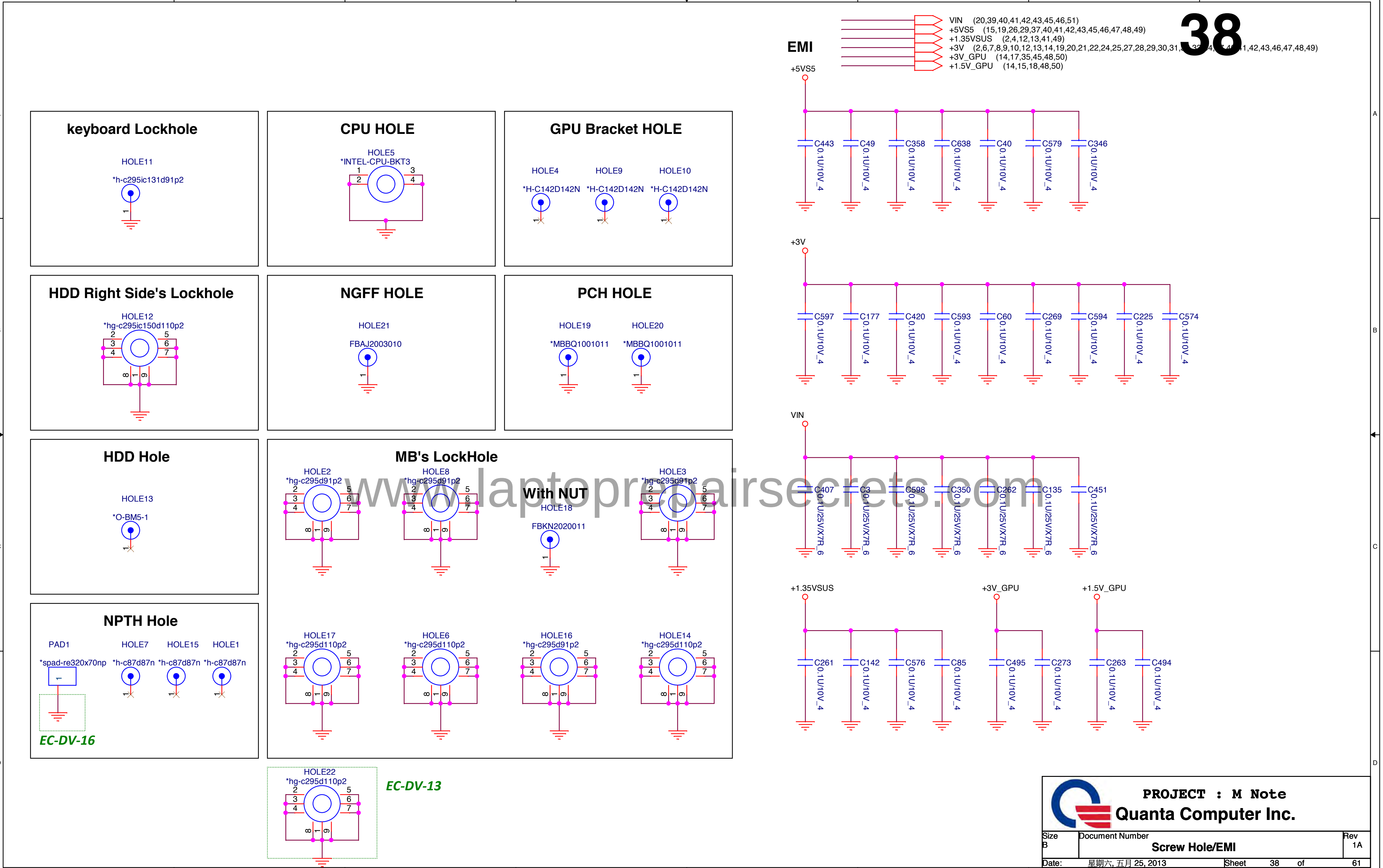


PROJECT : M Note

Quanta Computer Inc.

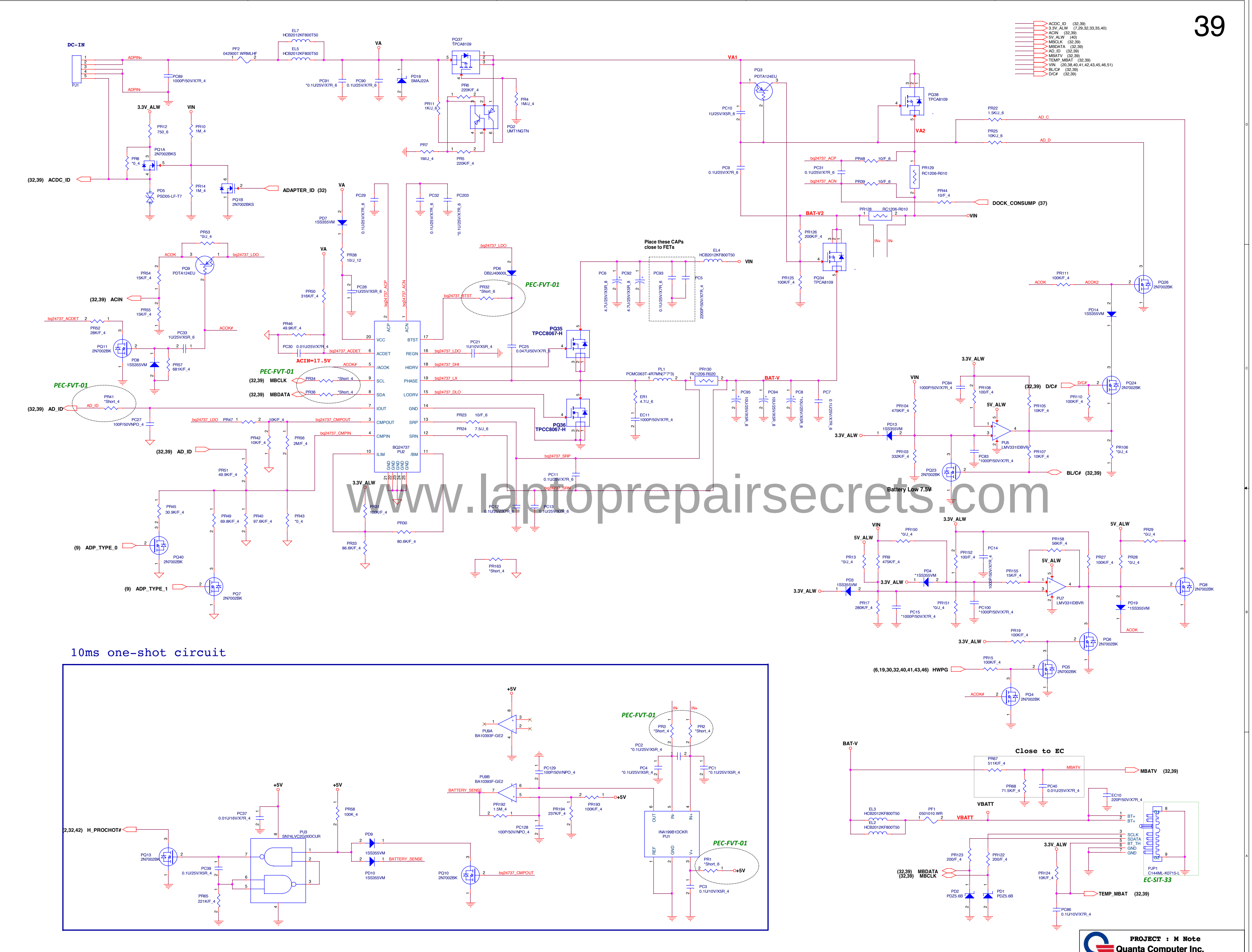
Size	Document Number	Rev
Custom	Cable Docking	1A

Date: 星期六, 五月 25, 2013 Sheet 37 of 61



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
B	Screw Hole/EMI	1A
Date: 星期六, 五月 25, 2013	Sheet 38 of 61	



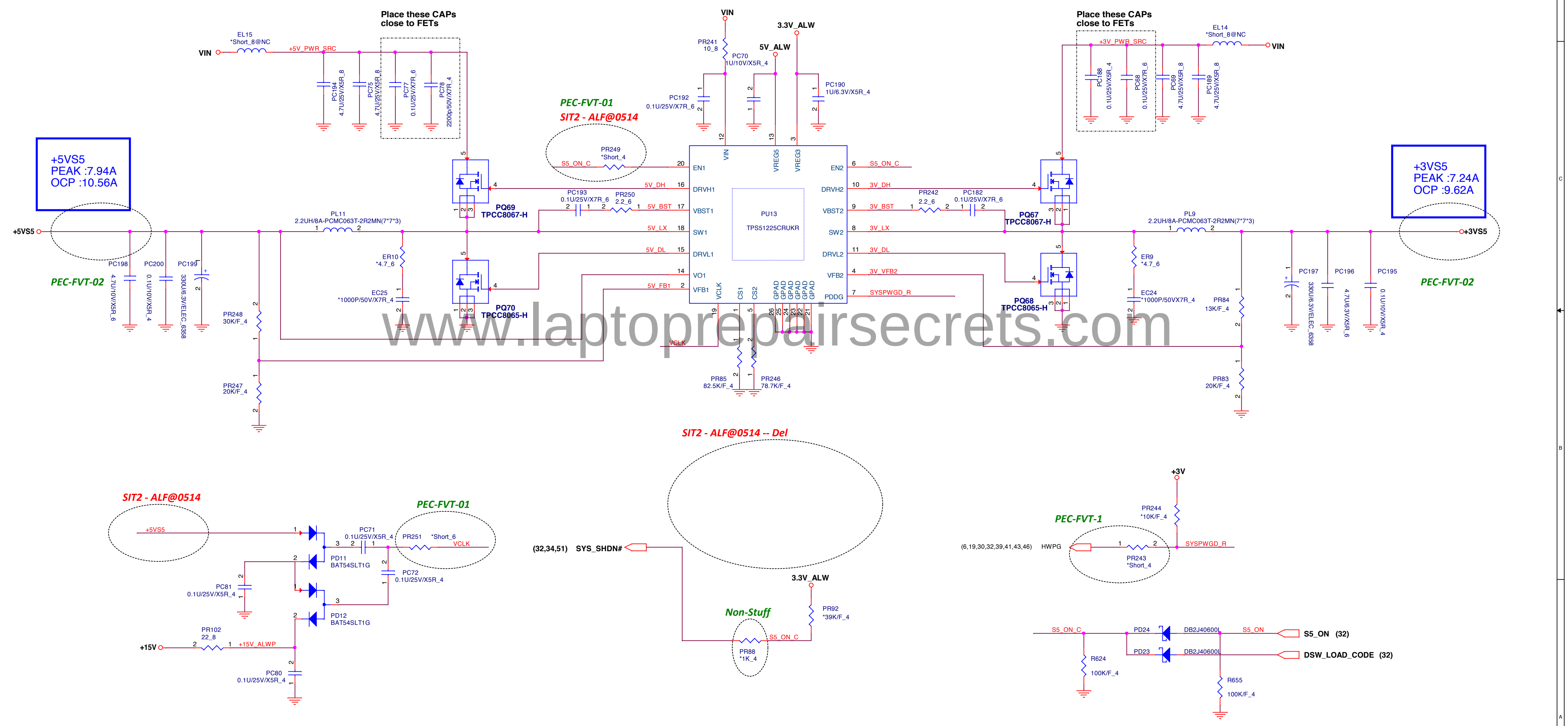
www.laptoprepairsecrets.com

PROJECT : M Note

Quanta Computer Inc.

Size: Custom | Document Number: Charger (BQ24737) | Rev: 1A

Date: 星期六, 五月 25, 2013 | Sheet 39 of 61



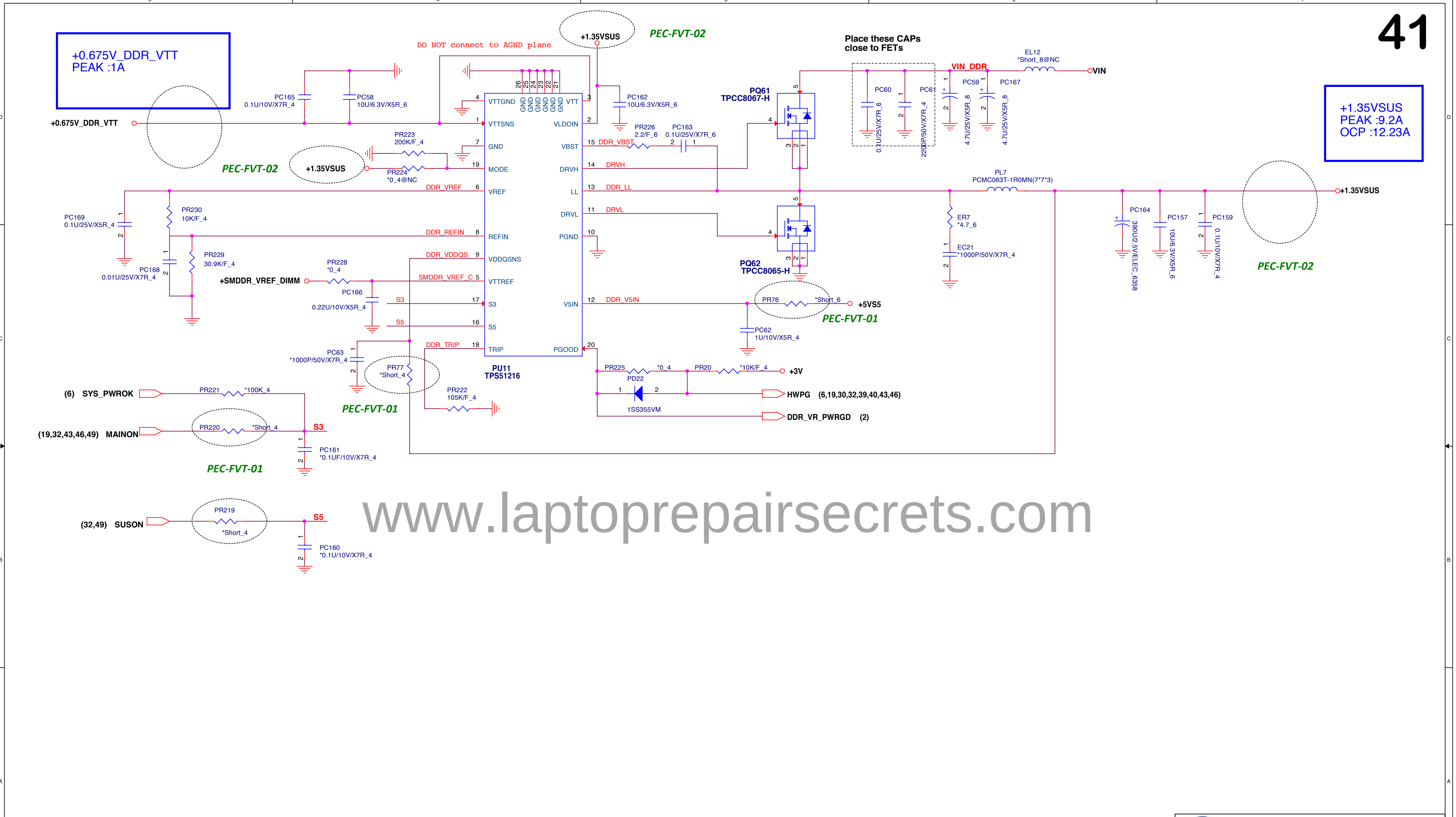
www.laptoprepairsecrets.com

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Power(TPS51225)	1A

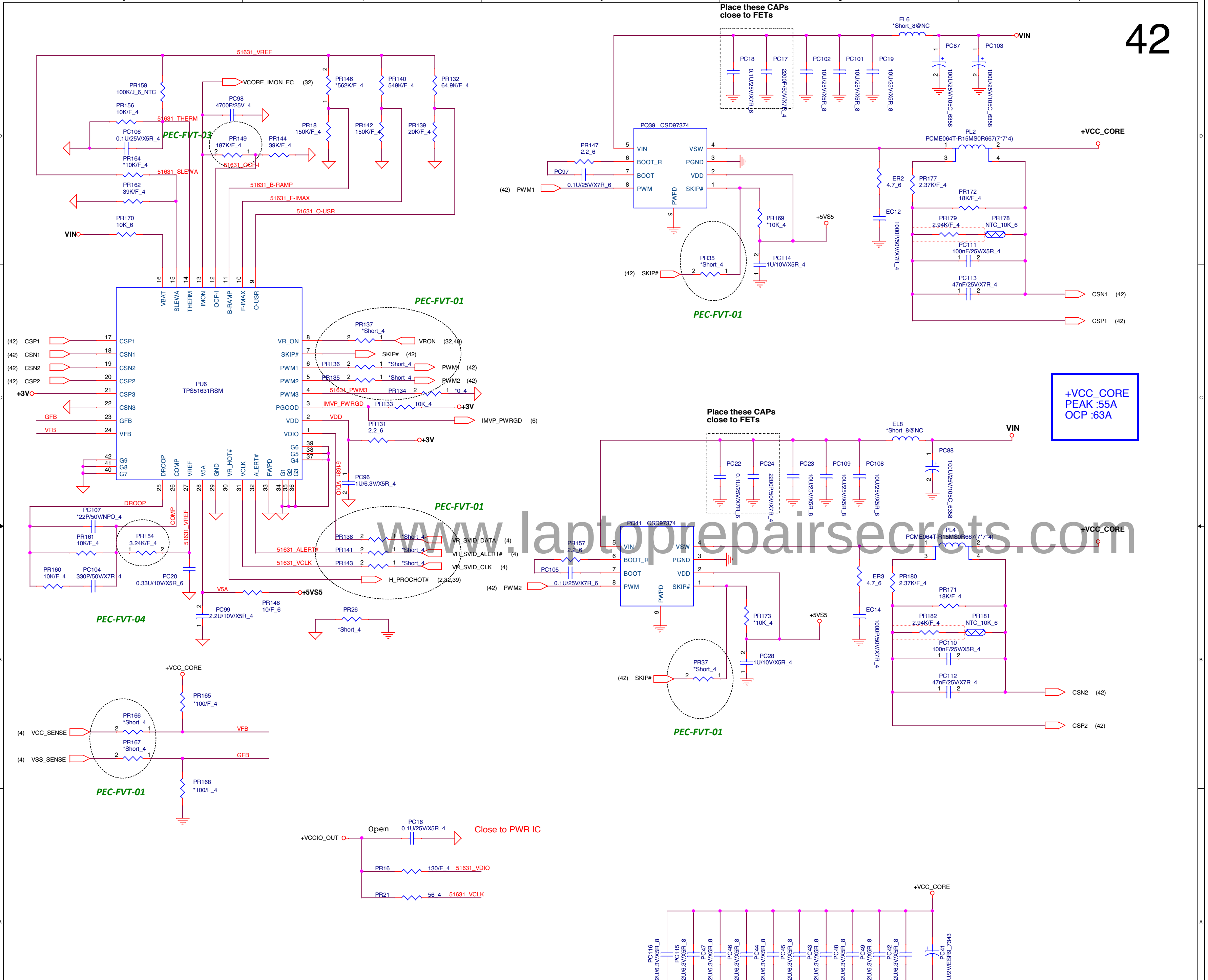
Date: 星期六, 五月 25, 2013 Sheet 40 of 61



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR Power (TPS51216)	1A
Date: 星期六, 五月 25, 2013	Sheet 41 of 61	

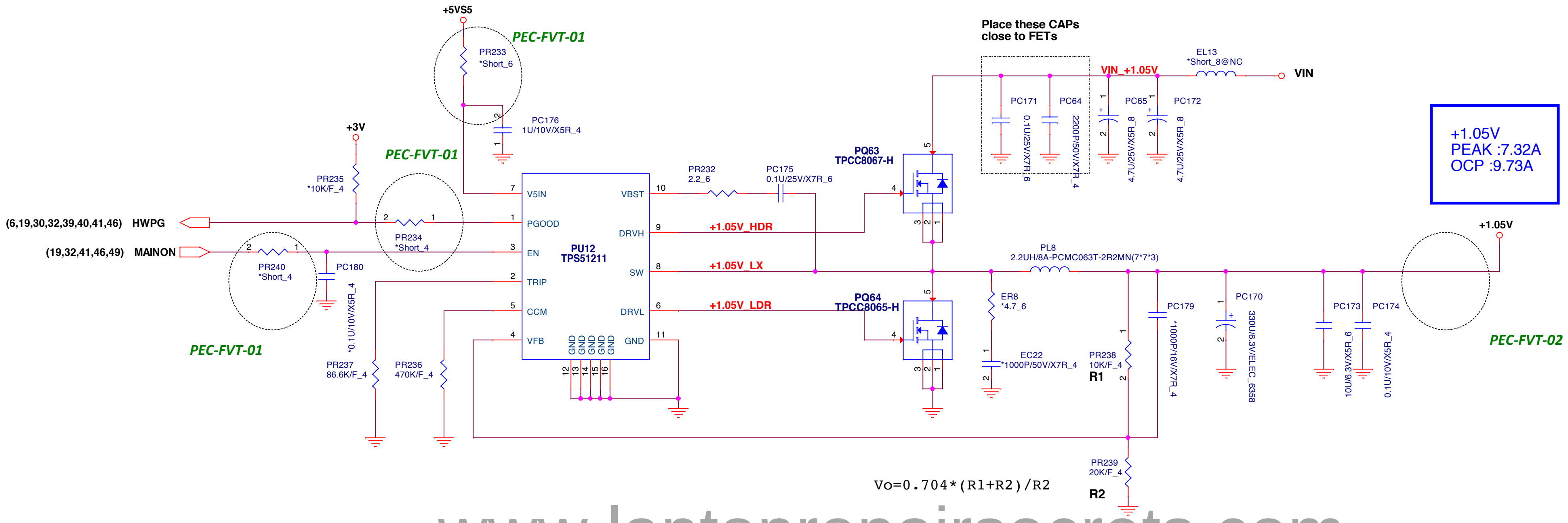


PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCC_CORE(TPS51631RSM)	1A

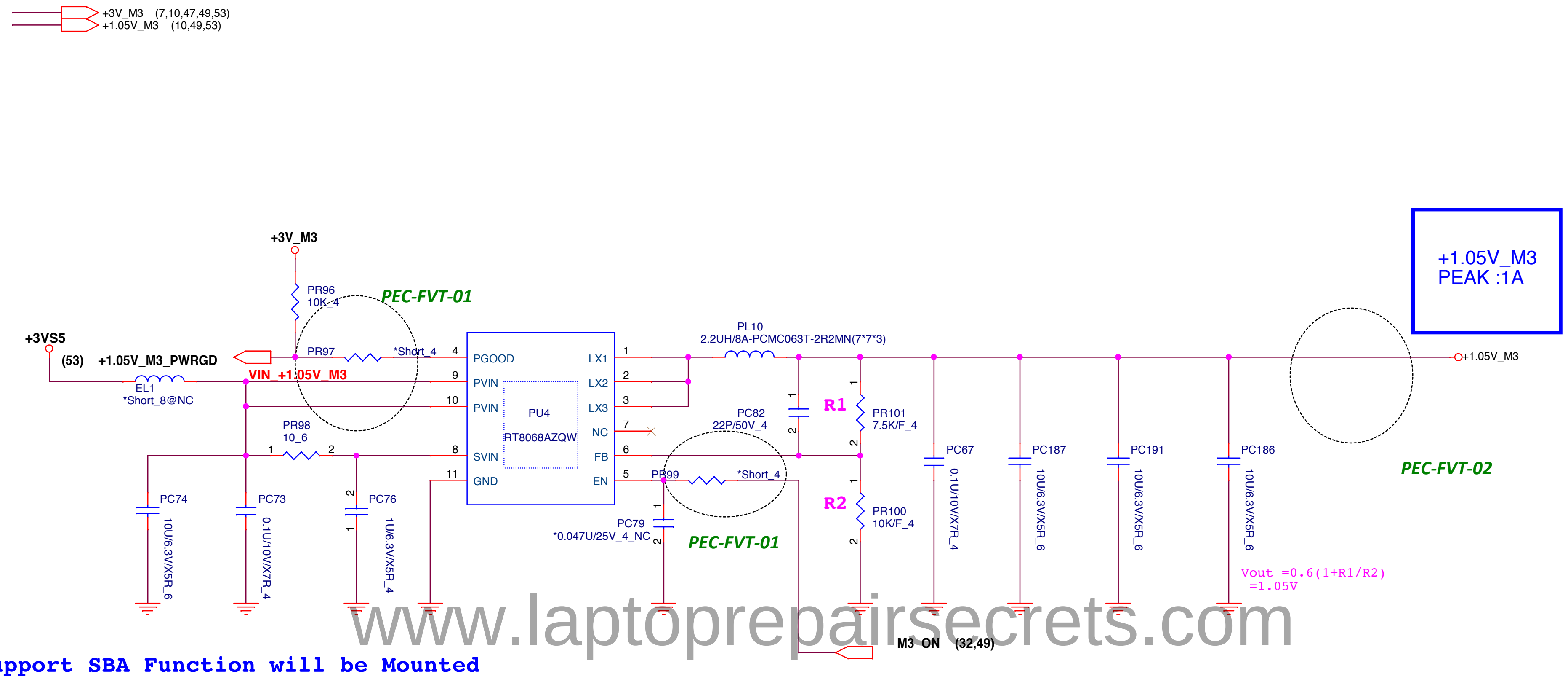
Date: 星期六, 五月 25, 2013 Sheet 42 of 61



PROJECT : M Note
Quanta Computer Inc.

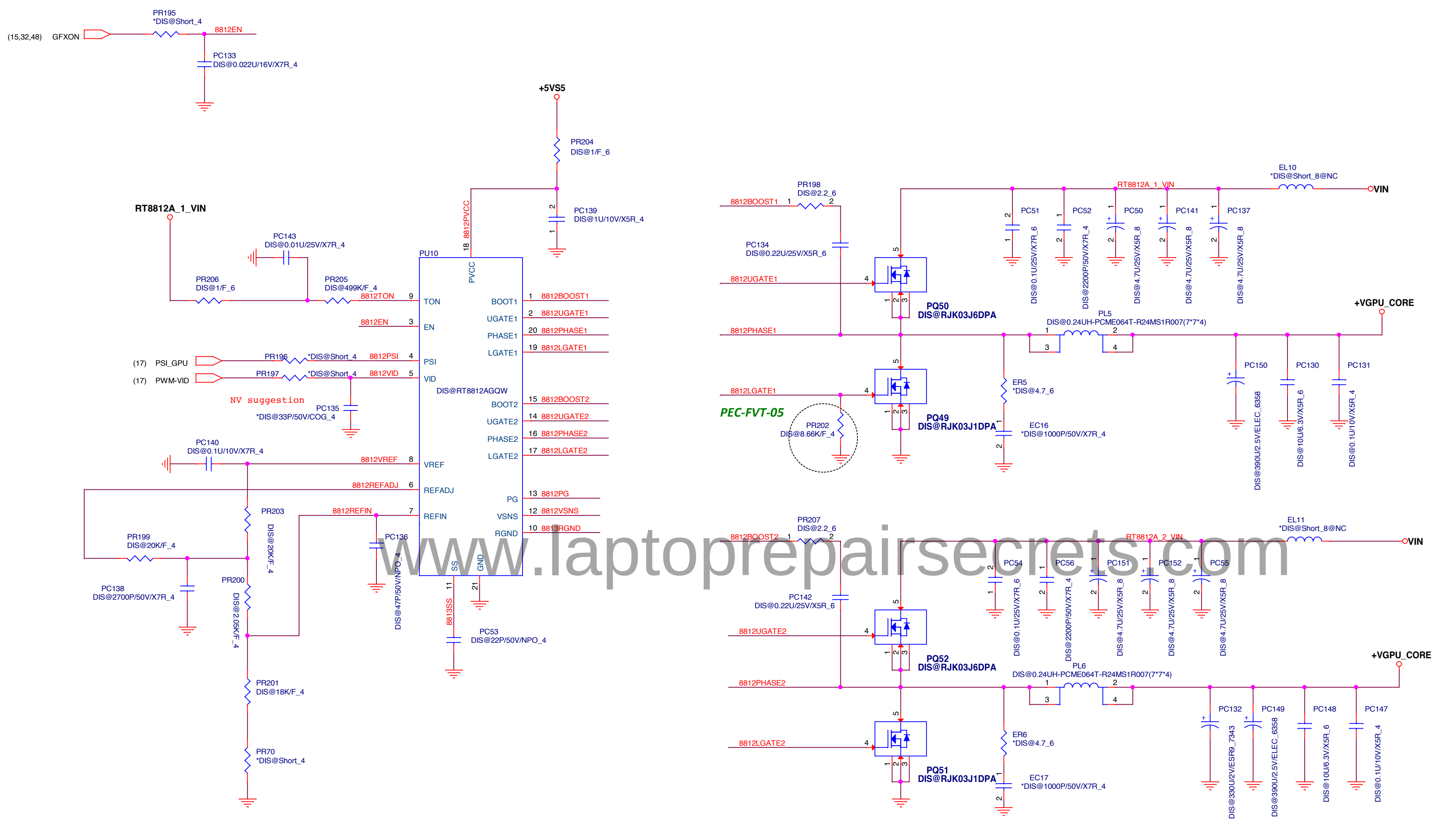
Size	Document Number	Rev
Custom	+1.05V(TPS51211)	1A

Date: 星期六, 五月 25, 2013 Sheet 43 of 61



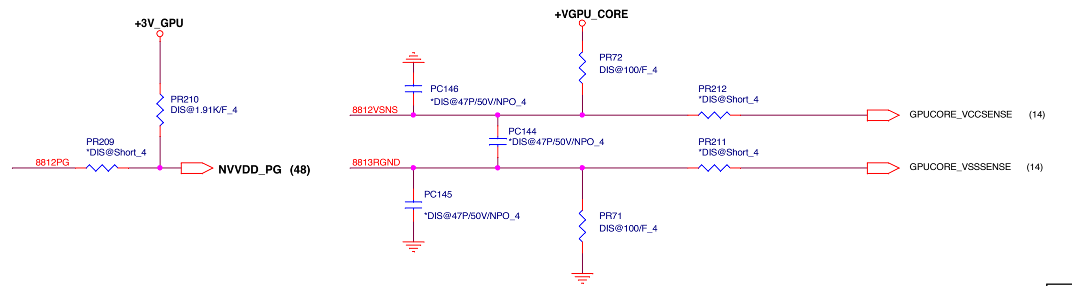
Support SBA Function will be Mounted

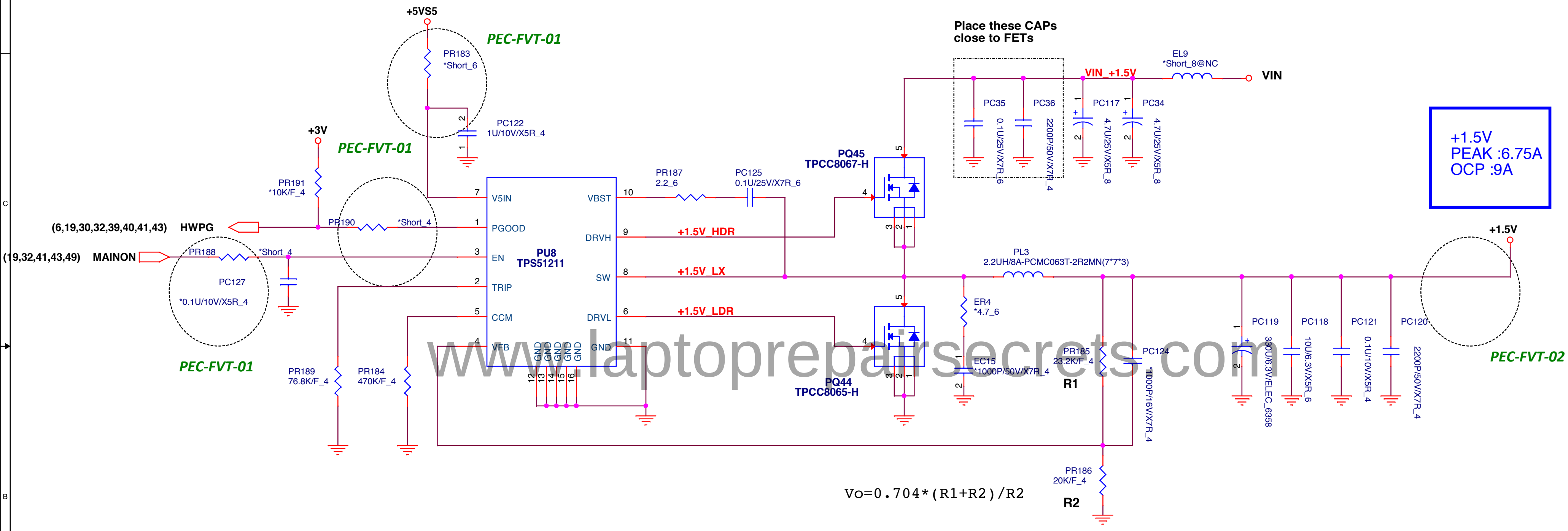
PROJECT : M Note		
Quanta Computer Inc.		
Size: B	Document Number: M3 Power(RT8068A)	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 44 of 61	



+VGPU_CORE
EDP-C: 35A
EDP-Peak: 55A
OCP: 60A

Nvidia	N14P-GV2 (Config B)	N14M-GL N14M-GE (Config C)
PR199	20KΩ	39KΩ
PR203	20KΩ	30KΩ
PR200	2.05KΩ	3KΩ
PR201	18KΩ	27KΩ
PR70	0Ω	0Ω
PC138	2.7nF	1.8nF





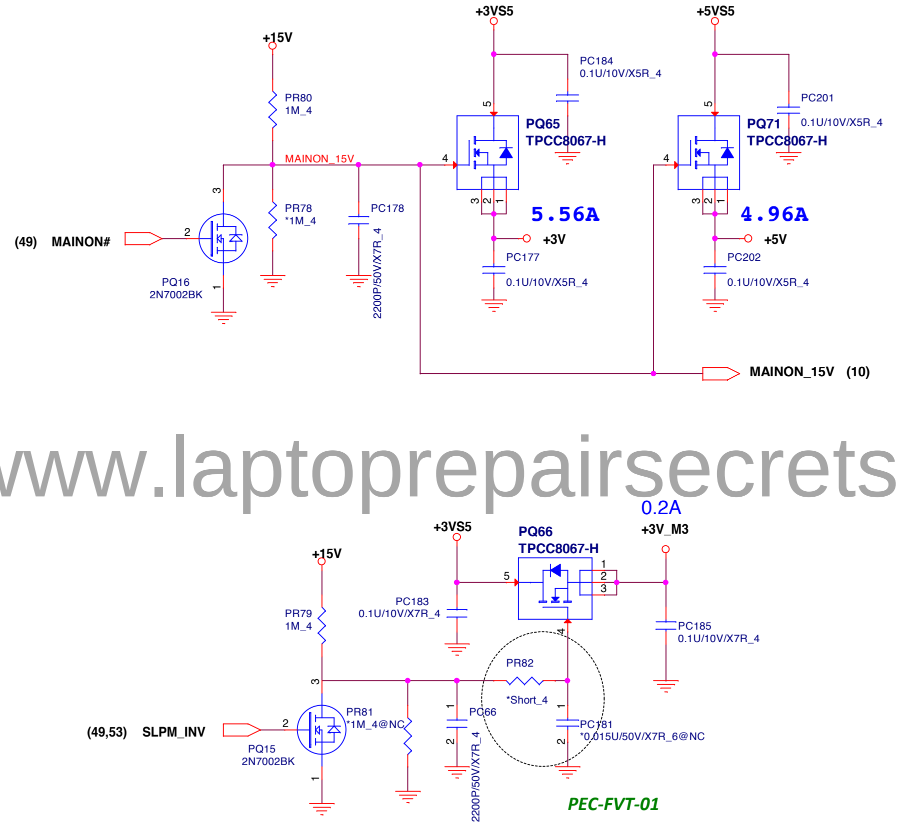
PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5V	1A

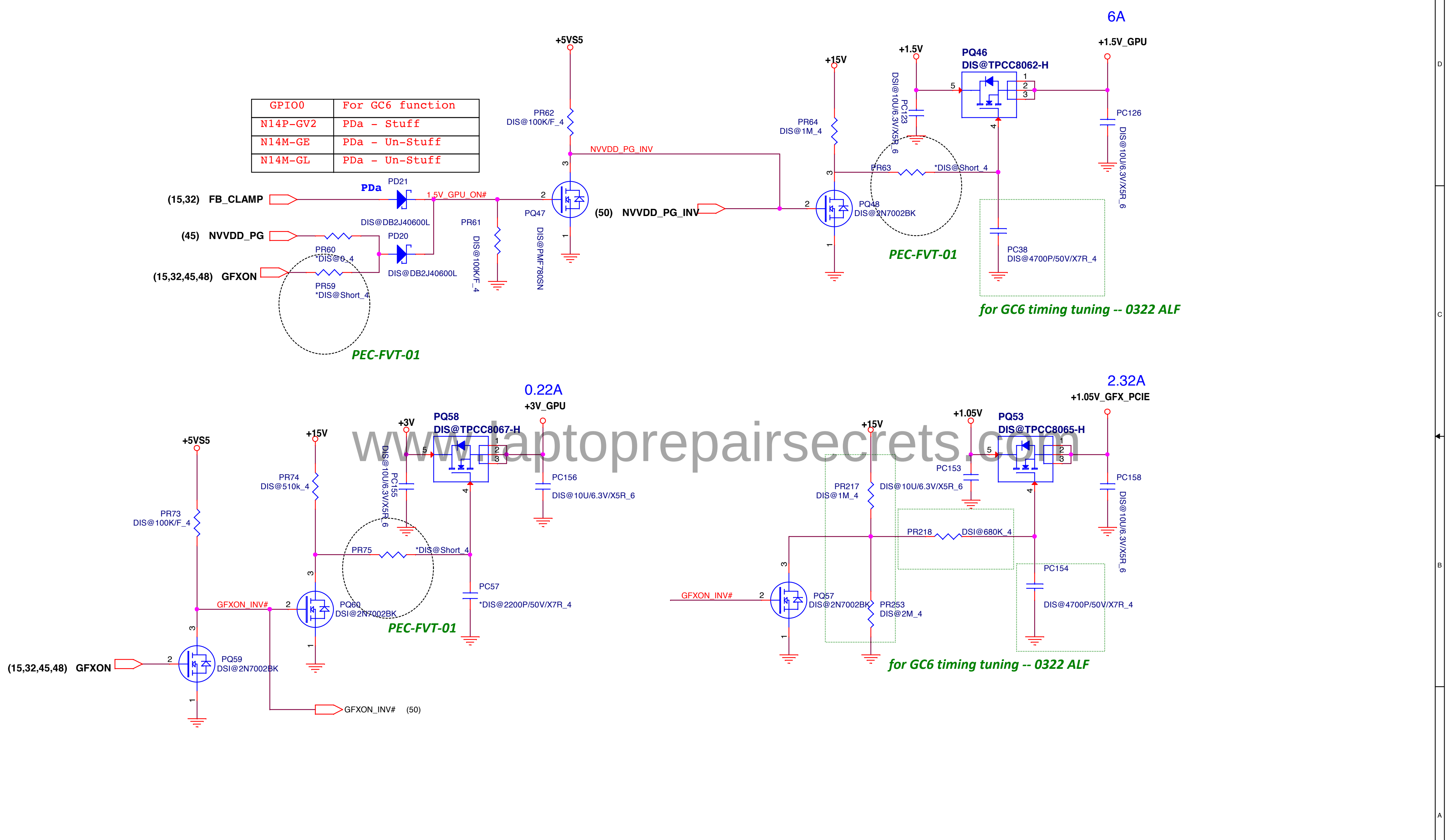
Date: 星期六, 五月 25, 2013 Sheet 46 of 61

+3V, +5V

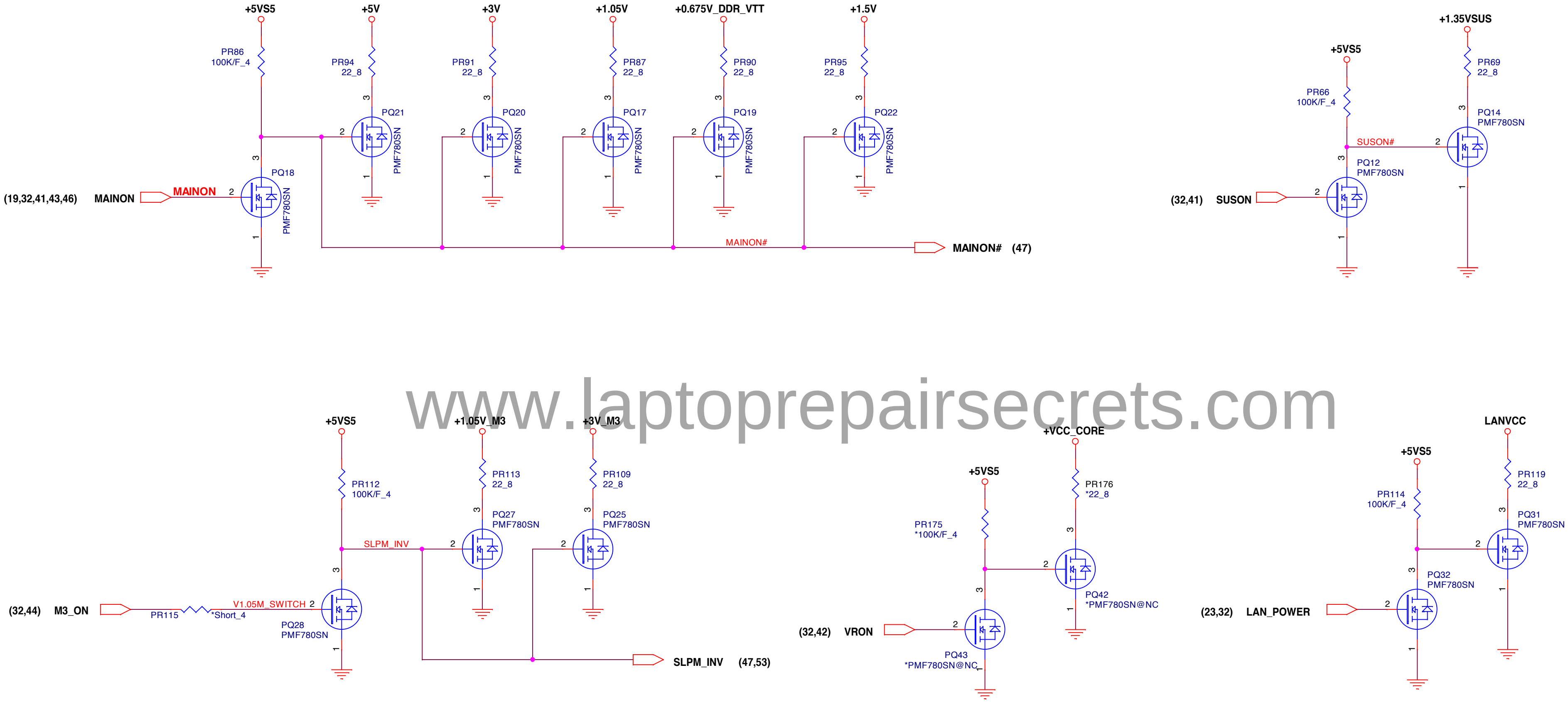


Support SBA Function will be Mounted

GPIO0	For GC6 function
N14P-GV2	PDa - Stuff
N14M-GE	PDa - Un-Stuff
N14M-GL	PDa - Un-Stuff



DISCHARGE



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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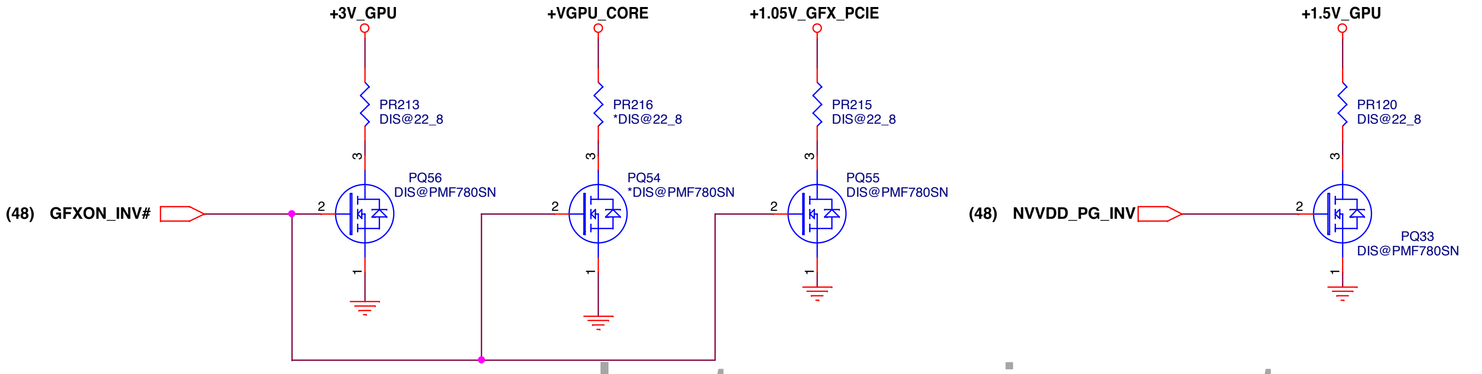
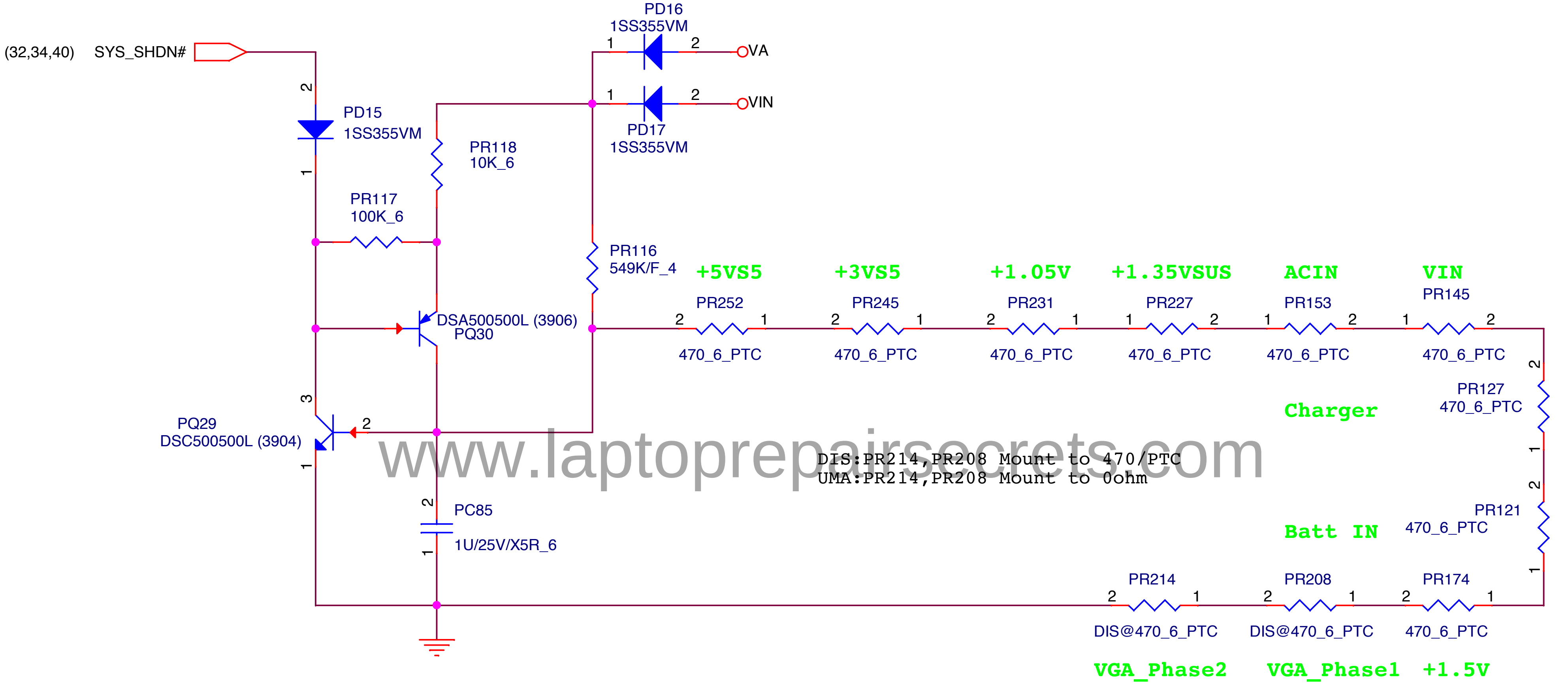
Discrete only



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
B	Discrete Discharge	1A

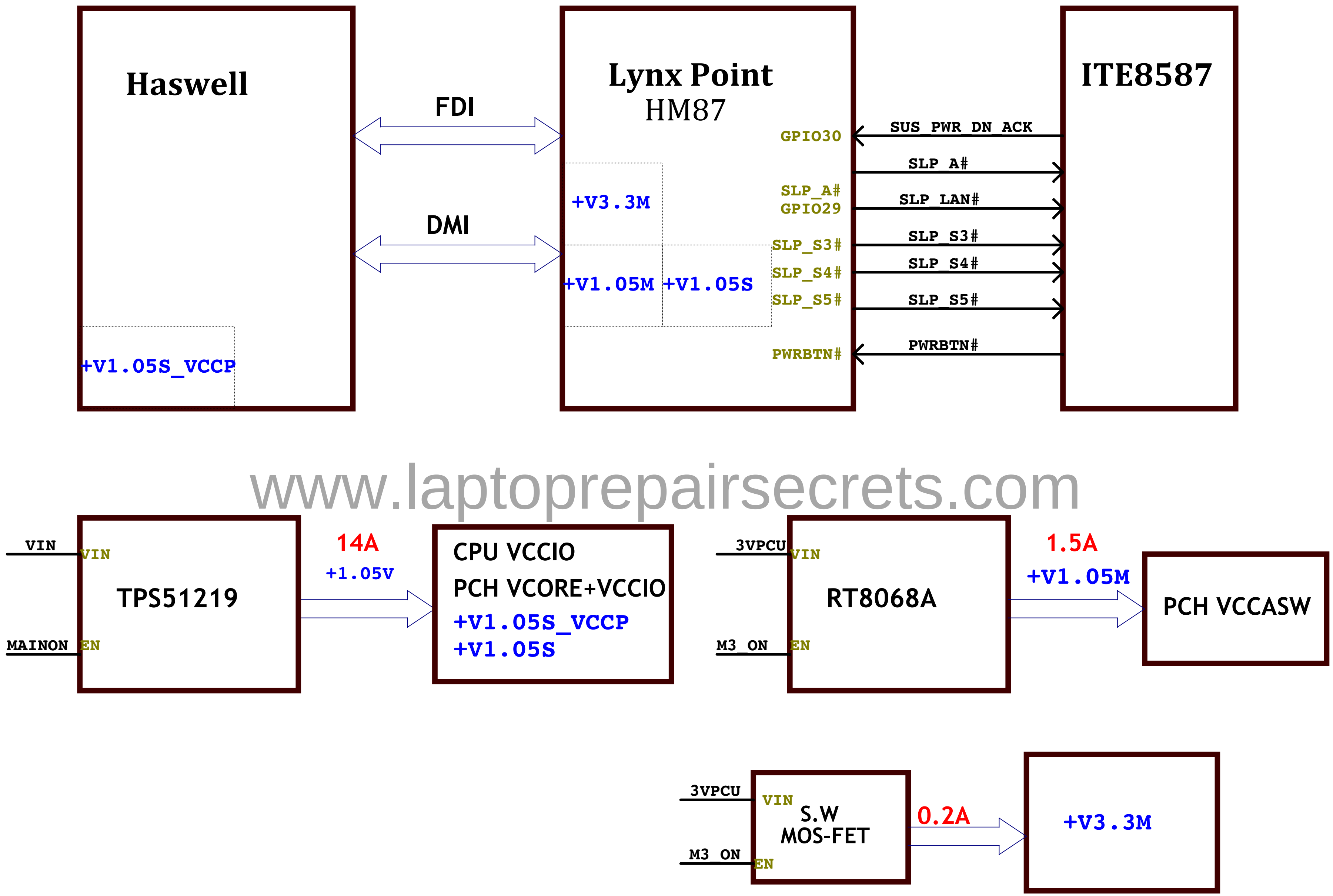
Date: 星期六, 五月 25, 2013 Sheet 50 of 61



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
A	PTC Circuit	1A
Date: 星期六, 五月 25, 2013	Sheet 51 of 61	

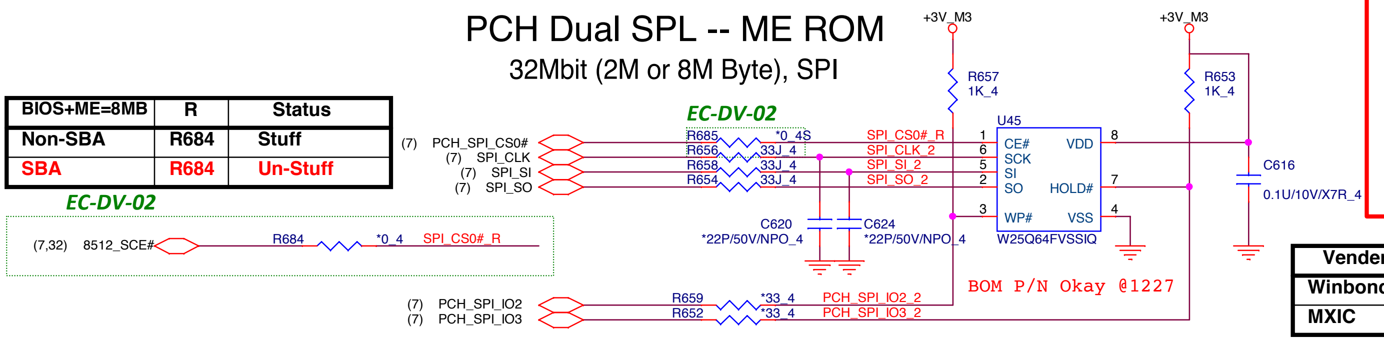

Haswell
+V1.05S_VCCP
FDI
DMI
Lynx Point
HM87
+V3.3M
+V1.05M
+V1.05S
GPIO30
SLP_A#
GPIO29
SLP_S3#
SLP_S4#
SLP_S5#
PWRBTN#
SUS_PWR_DN_ACK
SLP_A#
SLP_LAN#
SLP_S3#
SLP_S4#
SLP_S5#
PWRBTN#
ITE8587
VIN
VIN
MAINON
EN
TPS51219
14A
+1.05V
CPU VCCIO
PCH VCORE+VCCIO
+V1.05S_VCCP
+V1.05S
3VPCU
VIN
M3_ON
EN
RT8068A
1.5A
+V1.05M
PCH VCCASW
3VPCU
VIN
S.W
MOS-FET
M3_ON
EN
0.2A
+V3.3M

+3VS5 (2,6,7,9,10,15,17,20,23,24,25,28,32,37,40,44,47)
+3V_M3 (7,10,44,47,49)
+3V_DEEP_SUS (6,7,8,9,10)
+1.05V_M3 (10,44,49)
+1.05V (2,4,9,10,35,43,48,49)

PCH Dual SPL -- ME ROM

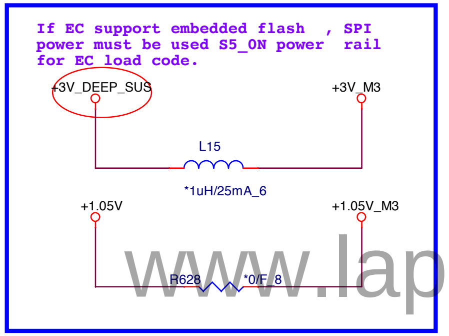
32Mbit (2M or 8M Byte), SPI

BIOS+ME=8MB	R	Status
Non-SBA	R684	Stuff
SBA	R684	Un-Stuff

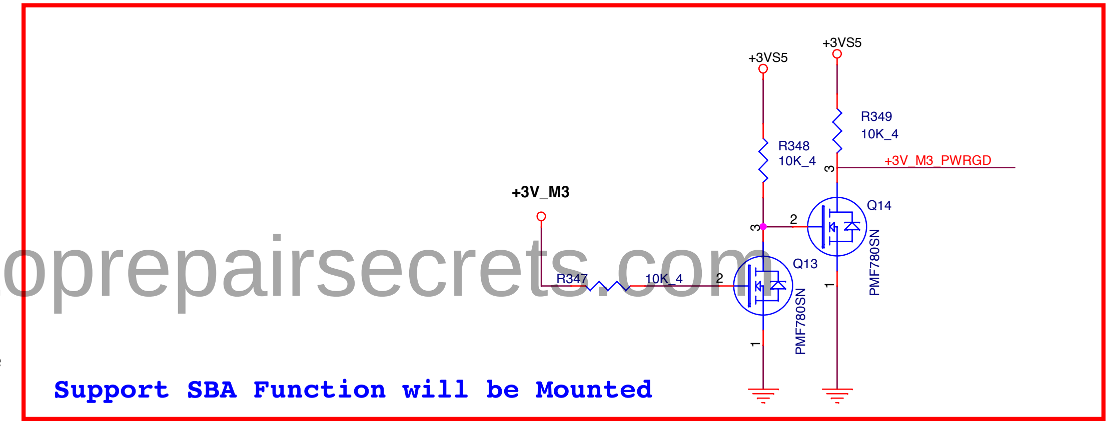


Vender		Size	P/N
Winbond	V	8MB	AKE3EFP0N07
MXIC		8MB	AKE3EZN0Z00

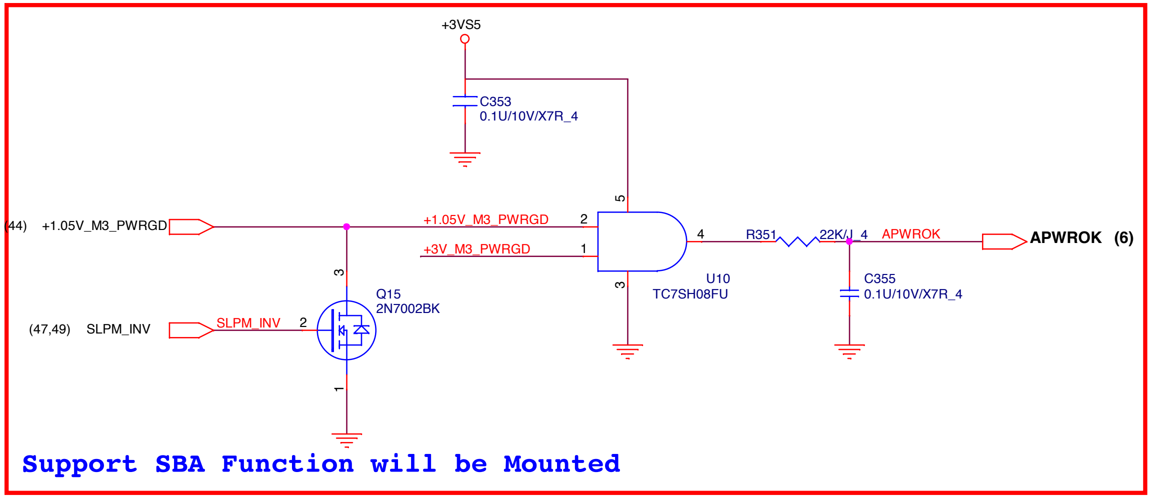
SBA POWERGD/SBA Power select



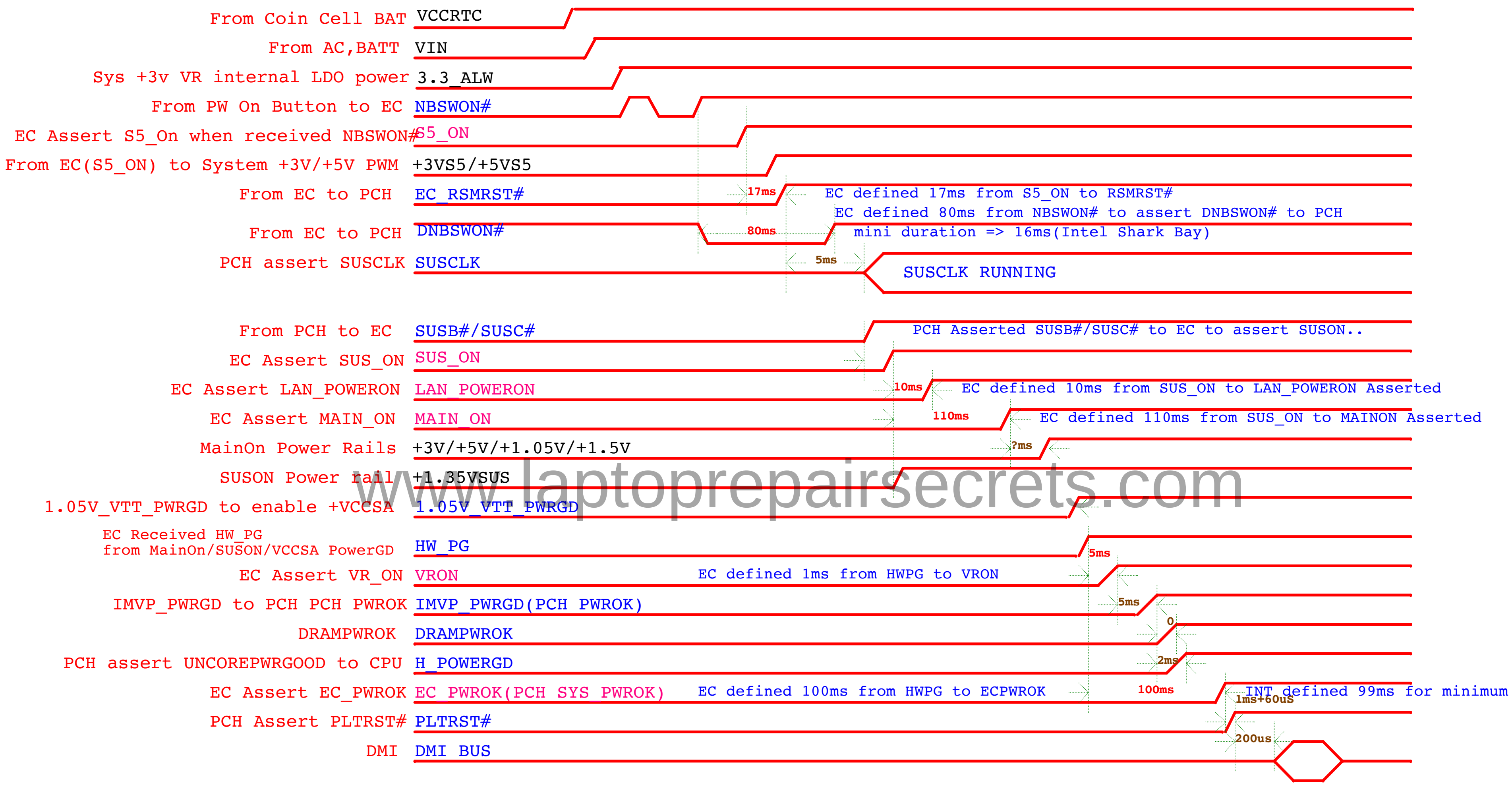
Without SBA Function will be Mounted



SBA LOGIC



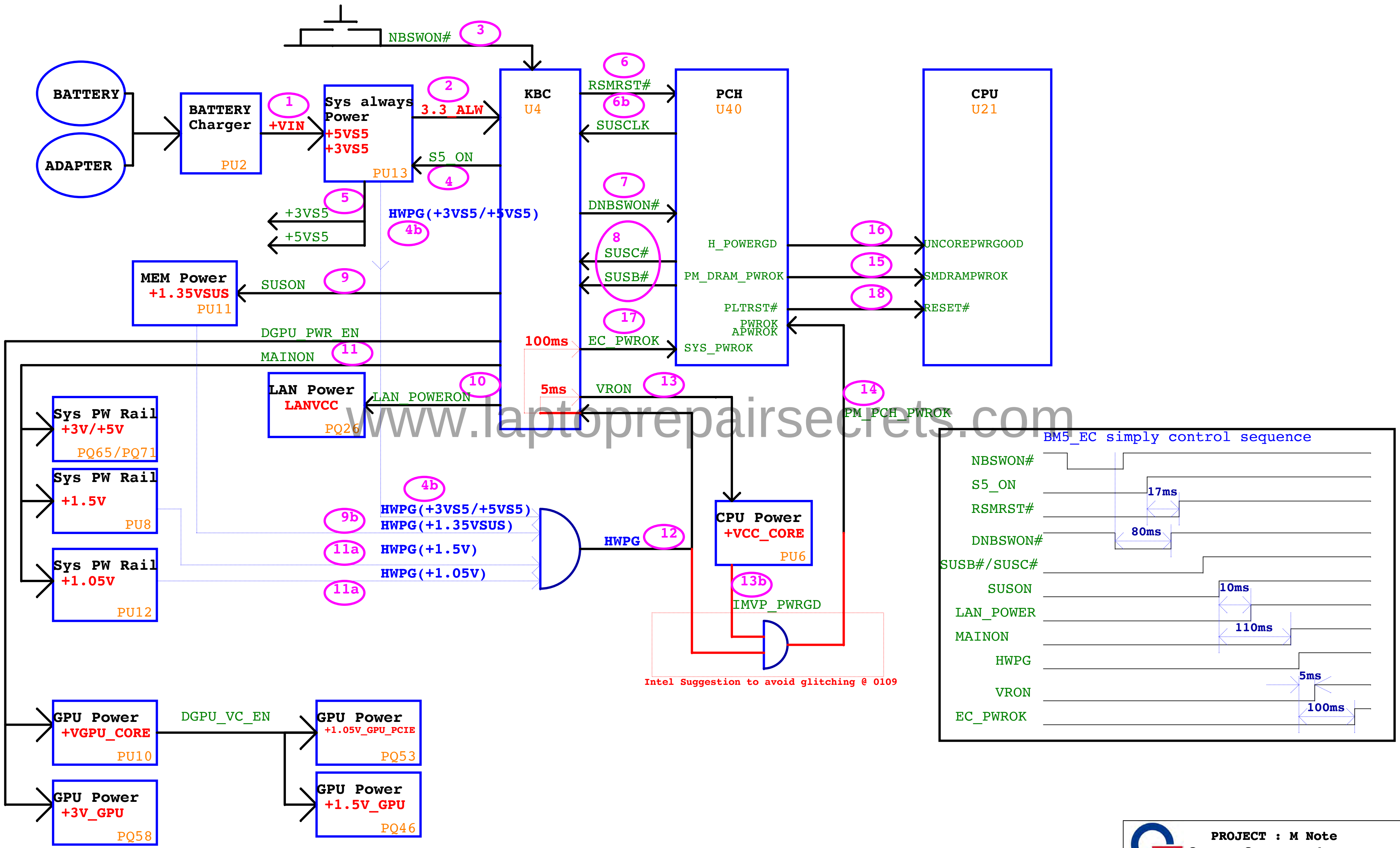
BM5/6 -- Intel Shark Bay mainly Power On Sequence(G3 to S0)



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power On Sequence CDP ROF	1A
Date: 星期六, 五月 25, 2013	Sheet 54 of 61	

BM5/6 -- Intel Shark Bay mainly Power On Sequence(G3 to S0)



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Control Procesure CDP ROF	1A

Date: 星期六, 五月 25, 2013 Sheet 55 of 61

BM5/6 Schematic EC Tracking Record DV (for DV) Jan. 18, 2013

EC #	Page	Description	Part Affected
EC-DV-01	10	Change component to "Stuff" to supply the power for VCCASW.	R301
EC-DV-02	53	Add one CS0# for SPI ROM for suppoted non-SBA function. BIOS+ME at one 8MB SPI ROM.	R685,R684
EC-DV-03	8	Changed the Power Rail to +3V_DEEP_SUS following CRB	Q41
EC-DV-04	6	Follow up Intel suggestion to meet the power up sequence for Shark Bay Platform	R686,R187,U49,C643,U36,R185,C274
EC-DV-05	21	Changed the Touch Screen CONN footprint and swap Pin Define.	CN1
EC-DV-06	37	Changed the internal docking CONN footprint and swap Pin Define.	CN21
EC-DV-07	24	Modify Speaker CONN footprint	CN2
EC-DV-08	33	Modify SW1 & SW2 Switch footprint	SW1,SW2
EC-DV-09	29	Changed the Power/B CONN footprint	CN4
EC-DV-10	7	Changed the 32.768KHz part for single source issue	Y4
EC-DV-11	8	Moved the USB2+/- from port 2 to port 1and USB3+/- from port 3 to port 9 for BIOS debug function.	
EC-DV-12	32	Add HDD_DETECT# pull up 100K ohm to 3.3_ALW	R687
EC-DV-13	38	Modify HOLE 22 footprint	HOLE 22
EC-DV-14	7,10	Separate the BIOS SPI & PCH SPI I/F power from +3V_M3, and adding a +3V_DEEP_SUS power	R688,R689
EC-DV-14	7	Modify the layout routing for EC auto load function to support CS0# (SBA) & CS1#(non-SBA)	
EC-DV-15	10	Un-Stuff the 100K ohm on SLP_SUS_ON_GPG2 for voltage-divider issue	R555
EC-DV-16	38	Add a GND signal suggesded by ESD team	PAD1
EC-DV-17	23	Modify the component footprint suggestion by ESD team	RV15,RV16,RV17,RV18,RV19
EC-DV-18	18	Modify the VRAM footprint, to add the silkscreen for different VRAM package of 2Gb & 4Gb	U9,U32,U6,U22
EC-DV-19	26	Changed the USB3.0 footprint.	CN18,CN21
EC-DV-20	25	Changed the ODD Power control GPIO from EC to PCH by customer request	R605,R608
EC-DV-21	20	Modify the component footprint	C399
EC-DV-22	23	Modify the component footprint	C406
EC-DV-23	16	For install GPU-GV2 driver issue, to stuff to supply power for VID_PLLVDD.	R115
EC-DV-24	24	Swap the Pin define to solve the recorder issue of internal MIC.	CN9
EC-DV-25	32	Change the R vaule to 100K ohm	R52
EC-DV-26	6	Reserver TPs for DDI Port debug, And adding pull-up a R to +3V for Enable DDI Port.	TP79,TP80,TP81,TP82, R691
EC-DV-27	7	EMI Suggestion, stuff 15pF for 24MHz Harmonic	EC18
EC-DV-28	8	EMI Suggestion, stuff 15pF for 33MHz SSC issue	EC5,EC20
EC-DV-29	28	EMI Suggestion, stuff 15pF for 33MHz SSC issue	C635

BM5/6 Schematic EC Tracking Record DV (for DV) Jan. 18, 2013

EC #	Page	Description	Part Affected
EC-DV-30	31	EMI Suggestion, stuff 22pF for CRT EMI issue	C215,C218,C229,C230,C240,C246,
EC-DV-31	26	EMI Sugestion, stuff 90 ohm common choke for USB2.0 port.	CML7,R673,R674
EC-DV-32	26	EMI Sugestion, stuff 90 ohm common choke for USB2.0 port.	CML8,R675,R676
EC-DV-33	24	EMI Sugestion, stuff 600 ohm bead for Speaker port.	R2,R3,R4,R5
EC-DV-34	22	EMI Sugestion, stuff 120 ohm R for HDMI port.	R638,R642,R650,R651
EC-DV-35	09	Board ID for BM5 / BM6 A2 stage	R586,R589,R283,R284,R575,R573,R278,R275

BM5/6 Schematic POWER EC Tracking Record DV (for DV) Jan. 18, 2013

EC #	Page	Description	Part Affected
PEC-DV-01	5	Follow Intel schematic review suggestion	C487,C92,C93,C512,C478

BM5/6 Schematic EC Tracking Record SIT (for SIT) Mar. 21, 2013

EC #	Page	Description	Part Affected
EC-SIT-01	05	Intel's Suggestion, to remove 1K ohm on CFG9	R480
EC-SIT-02	29	Added Thermal Pad to GND	U48
EC-SIT-03	37	Reserve design for Parade USB3.0 re-driver IC	U2,R692,R693,R694,R695,R696,R697
EC-SIT-04	32	Added 10K ohm to pull-up the +3VS5 rail on USB_STATUS#	R698
EC-SIT-05	09	Changed the power rail of "SV_DET" to +3V	R542
EC-SIT-06	14	Changed the GPU's enable signal of CLK_REGA_REQ# to "GFXPG"	Q6
EC-SIT-07	07	EMI suggestion to change the capacitor value	EC18,EC19
EC-SIT-08	23	Modify the LAN Surge protected circuit from EMI suggestion	R172,RV15,R699,R173,R174,R175,R176,U50,U51
EC-SIT-09	27,32	Removed the "NGFF_SSD_PRESENT#" to Pin21, and changed to 3.3V_ALW. Lenovo suggestion	CN19
EC-SIT-10	08,27	Added one GPIO controlled by PCH and pull down 10K ohm	R700,CN19,R359
EC-SIT-11	37	Added 4pcs AC Cap at RX/TX for docking USB3.0 function. Lenovo suggestion	C644,C645,C646,C647,CN12,U2,U20
EC-SIT-12	28	Reserve 2pcs Cap on WLAN PCIE Clock 100MHz.	C648,C649
EC-SIT-13	32	Reserve 220pF on ACDC_ID signal	C650
EC-SIT-14	06,32	Non-stuff the parts, ESD suggestion	C59,C586
EC-SIT-15	32	Reserve 0.1uF on "HDD_DETECT# signal	C651
EC-SIT-16	32	Reserve 330pF on +3.3V_RUN_EC power rail	C652
EC-SIT-17	33	Stuff the parts, ESD suggestion	RV5,RV6
EC-SIT-18	29	Reserve without AOU5 circuit	RP9,PR10,RP11,RP12,U52,U48,C653
EC-SIT-19	24	Delete R359 to increase space for circuit of w/o AOU5	R359
EC-SIT-20	32	Added 2 resistances to select AOU5 function	R701,R702
EC-SIT-21	20	Changed the Touch Screen solution, so deleted the CN1 Conn.	CN1
EC-SIT-22	20	Changed the LVDS Conn type to 40Pin for adding touch function	CML1,R402
EC-SIT-23	29	Stuff the parts, EMI suggestion	CML4,CML5,R355,R356,R354,R353
EC-SIT-24	21	Stuff the parts, EMI suggestion	CML6,R395,R396
EC-SIT-25	20	Stuff the parts, EMI suggestion	C4,C5
EC-SIT-26	20	Stuff the parts, EMI suggestion	L23,R406,R407
EC-SIT-27	32	Added on 0 ohm from +3V_RTC rail to RTC_VCC rail	R703
EC-SIT-28	08,25	Reserve HDD_DEVSLP function at HDD device	R704,R705
EC-SIT-29	07	Stuff the some components for preventing the leakage on +3V power rail	Q38,R205,R194,R527,R
EC-SIT-30	22	Changed the R value from 680 to 470 of Cost Reduced Level Shifter for HDMI eye diagram test	R325,R326,R327,R328,R329,R332,R333,R334

BM5/6 Schematic EC Tracking Record SIT (for SIT) Mar. 21, 2013

EC #	Page	Description	Part Affected
EC-SIT-31	37	Added the pull-up R on EQ1 & EQ2 for USB3.0 SI of RX test	R16,R20
EC-SIT-32	07	Changed the Cap Value for fine-tuning the crystal's accuracy	C277,C280
EC-SIT-33		Changed the Conn. to ECSL parts	JDIM2,JDIM1,CN15,CN17, PJP1,CN13,CN14,CN16,CN18,CN21,CN5,CN6 CN7,CN10,CN4,CN20
EC-SIT-34	33	Changed the parts of click pad switch by ME requirement	SW1,SW2
EC-SIT-35	29	Setting the AOU5 RILIM_Hi & RILIM_Lo to current 2.3A & 1.5A	R669,R670
EC-SIT-36	09	Board ID for BM5 / BM6 SIT Stage	R586,R589,R283,R284,R575,R573,R278,R275

BM5/6 Schematic EC Tracking Record SIT2 (for SIT2) May. 24, 2013

EC #	Page	Description	Part Affected
EC-SIT2-01	33	Changed the CN5 Footprint	CN5
EC-SIT2-02	29	Delete the CN10 Pin 2 +3V for assembly line issue	CN10
EC-SIT2-03	25	Directly connect HDD Conn Pin18 to GND. Lenovo suggestion	CN17
EC-SIT2-04	32	Swap the GPIO Pin on 108 & 30 to support the breathing effect	U4
EC-SIT2-05	28	Add a circuit to don't support AOAC function	R665
EC-SIT2-06	07,20	Added 1 GPIO21 of PCH to control the Touch Panel RST Pin and 1 Cap 0.47u for timing fine tune	U40,R630, C654
EC-SIT2-07	19	Stuff the parts for linking the eDP to LVDS converter IC via SMBus	Q22
EC-SIT2-08	15	Modify the part's footprint	Q35
EC-SIT2-09	29	Changed the CN4 Footprint from 0.5 pitch to 1.0 pitch for assembly line issue	CN4
EC-SIT2-10	27	Delete the GND Pin on Pin5 of NGFF Connector as Vendor's PCR	CN19
EC-SIT2-11	09	Just modify the signal neme to AOAC_EN	U40
EC-SIT2-12		Delete the 0 ohm or common chock on all USB ports	R353,R354,R355,R356,R673,R674,R675,R676,R395,R396,R406,R407,CML2,3
EC-SIT2-13	20	Modify the part's footprint	CML1
EC-SIT2-14	29	Modify the part's footprint	CN10
EC-SIT2-15	29	Modify the ILIM LO R value from 68K ohm to 2M ohm	R670
EC-SIT2-16	32	Added M3_ON pull up 10K ohm with 3.3V_ALW for Auto load code issue	R353
EC-SIT2-17	09	Board ID for BM5 / BM6 SIT2 Stage	R586,R589,R283,R284,R575,R573,R278,R275