Compal Confidential

DH53F MB Schematic Document

LA-F991P

Rev : 1.C

2018.02.13

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: DH53F M/B LA-F991P	Rev: 1.A
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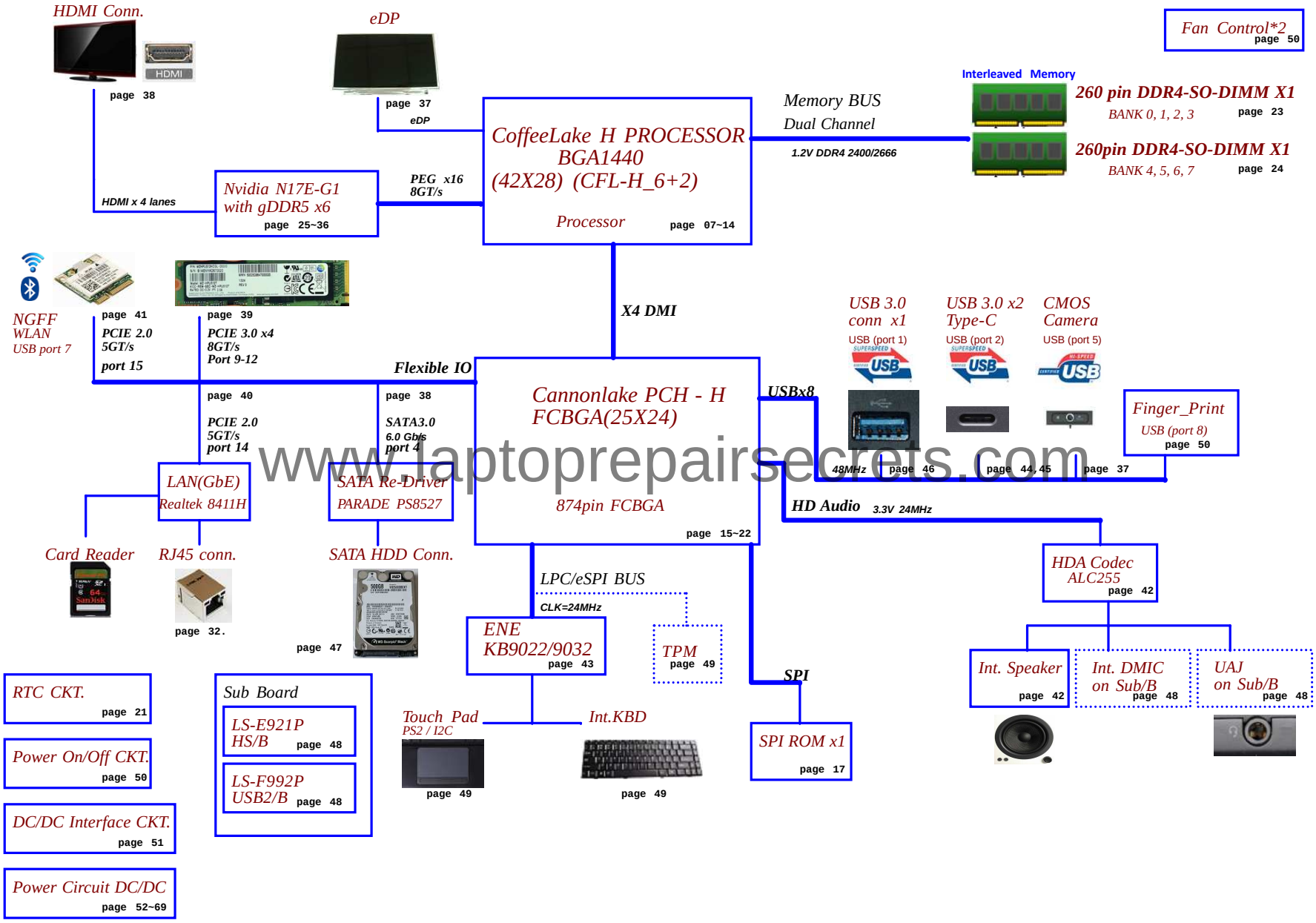

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Title	Block Diagrams		
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 / 28P
1	0.2 / 28P
2	1.0 / 28P
3	1.C / 28P
10	0.1 / 32P
11	0.2 / 32P
12	1.0 / 32P
13	1.C / 32P

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17E-G1 (VGA)	0x9E		
	EC			
	CC controller 179F			
	TMS			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
UMA only	UMA@
CMC	CMC@
dGPU	VGA@
DIS only	DIS@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
28P keyboard connector	28P@
32P keyboard connector	32P@
Finger Print	FP@
Finger Print for ESD	FPESD@
PBA	PBA@
Thermal sensor	TMS@
LAN LDO mode	LDO@
LAN Switch mode	SWR@
G-Sensor	GSEN@
EMI requirement	EMI@
EMI require reserve	@EMI@
ESD requirement	ESD@
EMI require reserve	@ESD@
CNVI	CNVI@
UART debug	UART@
Codec ALC255	255@
Codec ALC256	256@
Codec ALC256 for ESD	256ESD@
Codec ALC256 for EMI	256EMI@
G-PAK for GPU sequence	GPK@
DIS for GPU sequence	NGPK@
W/ SATA re-driver	SATARD@
W/O SATA re-driver	NORD@
PCH	PCH@
CPU	i5@/i7@

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BOM table

43 Level	Description	BOM Structure
431AB2BOL05~08		
431AB2BOL53_54		
431AB1BOL67		
X4EAB2BO001		
X4EAB2BO051		
X76730BOL56	ALT. GROUP PARTS N17E6G SAM 256M32 DH7VF	
X76730BOL57	ALT. GROUP PARTS N17E6G HYN 256M32 DH7VF	
X76730BOL58	ALT. GROUP PARTS N17E6G MIC 256M32 DH7VF	

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Title: Notes List

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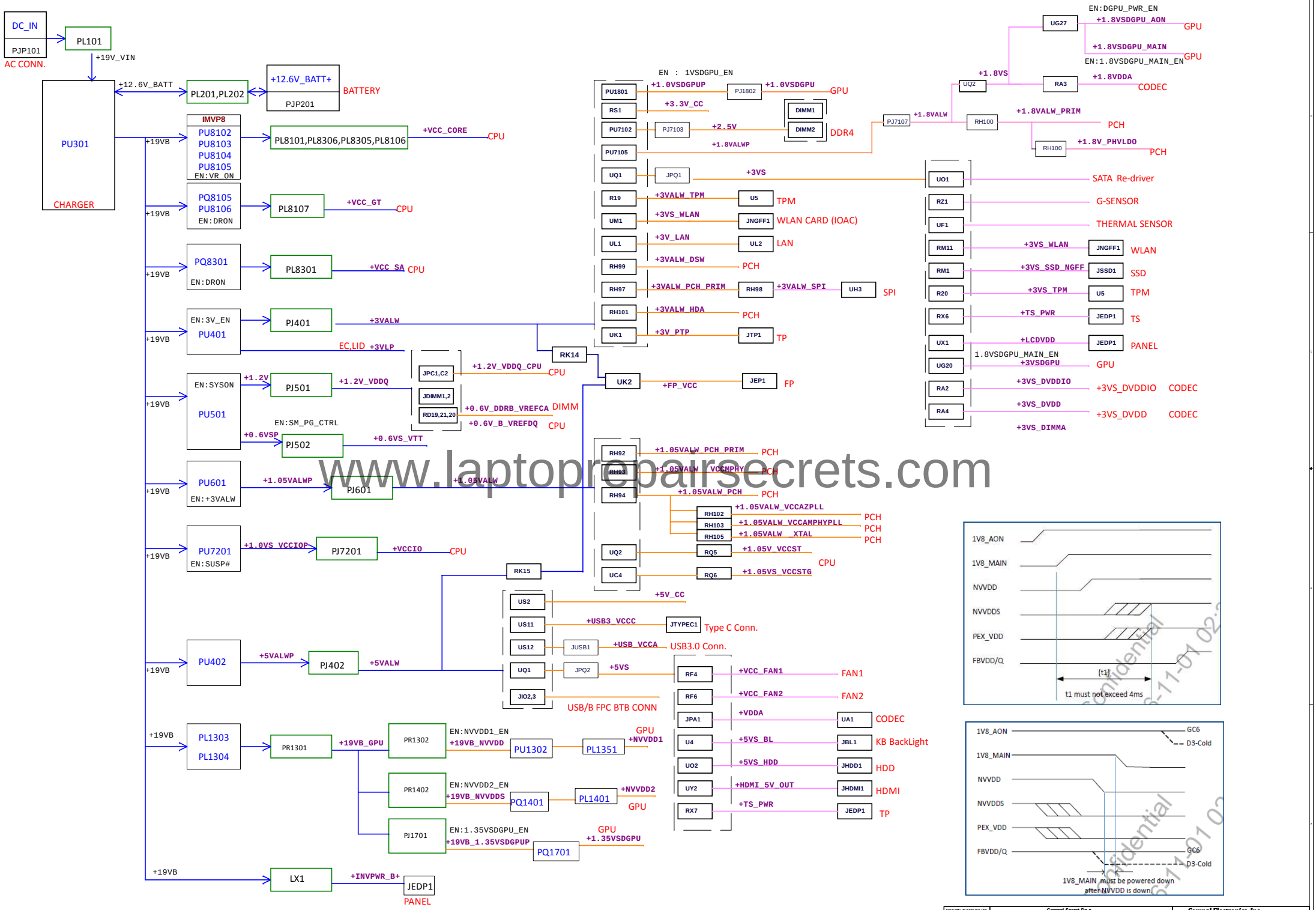


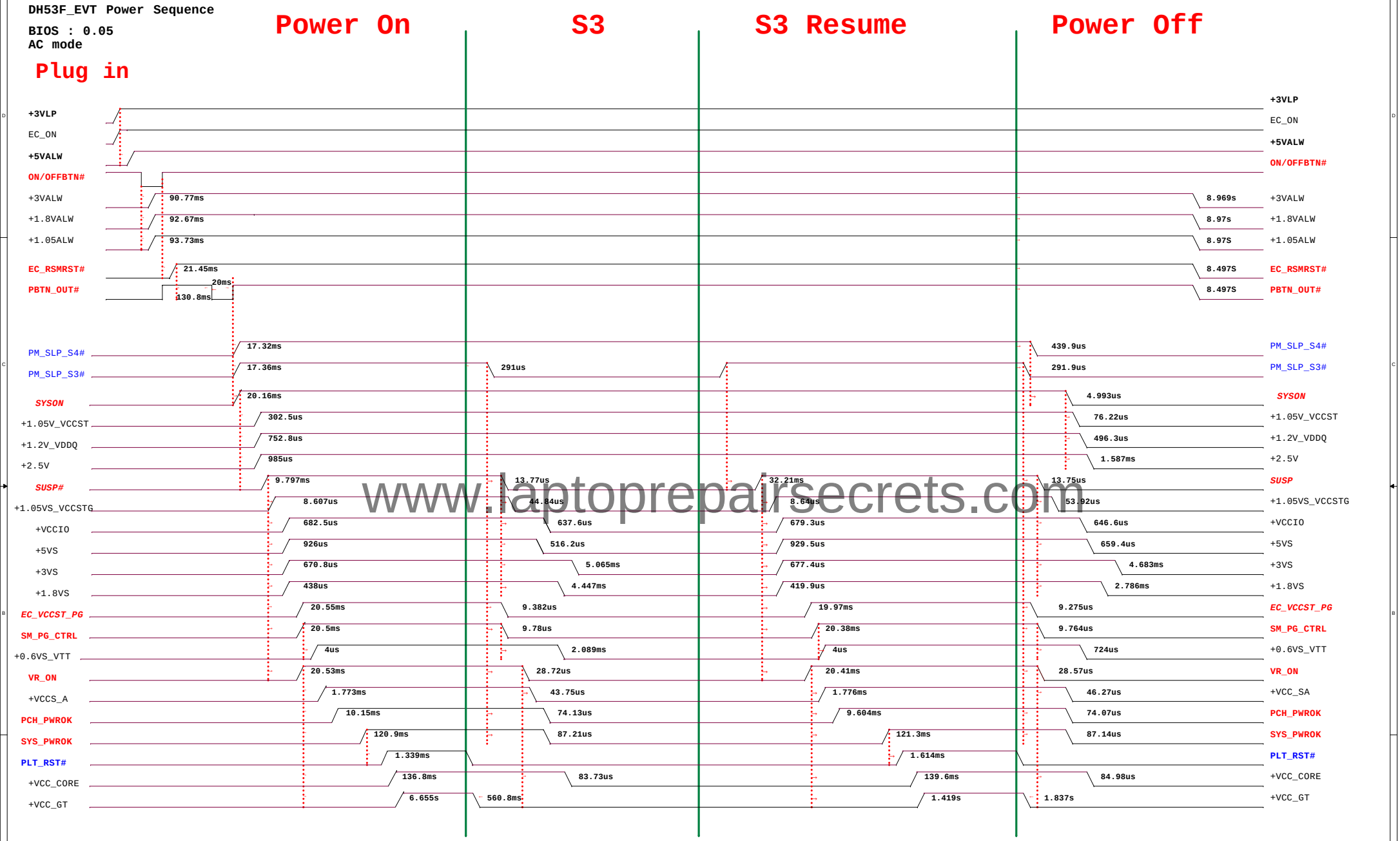
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	20 7 07 20	Deciphered Date 20 8 07 20	Power Map
			DA53F M/B LA-F991P

DH53F_EVT Power Sequence

BIOS : 0.05

AC mode

Plug in



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Compal Electronics, Inc.

Title: Power Map

Size	Document Number	Rev
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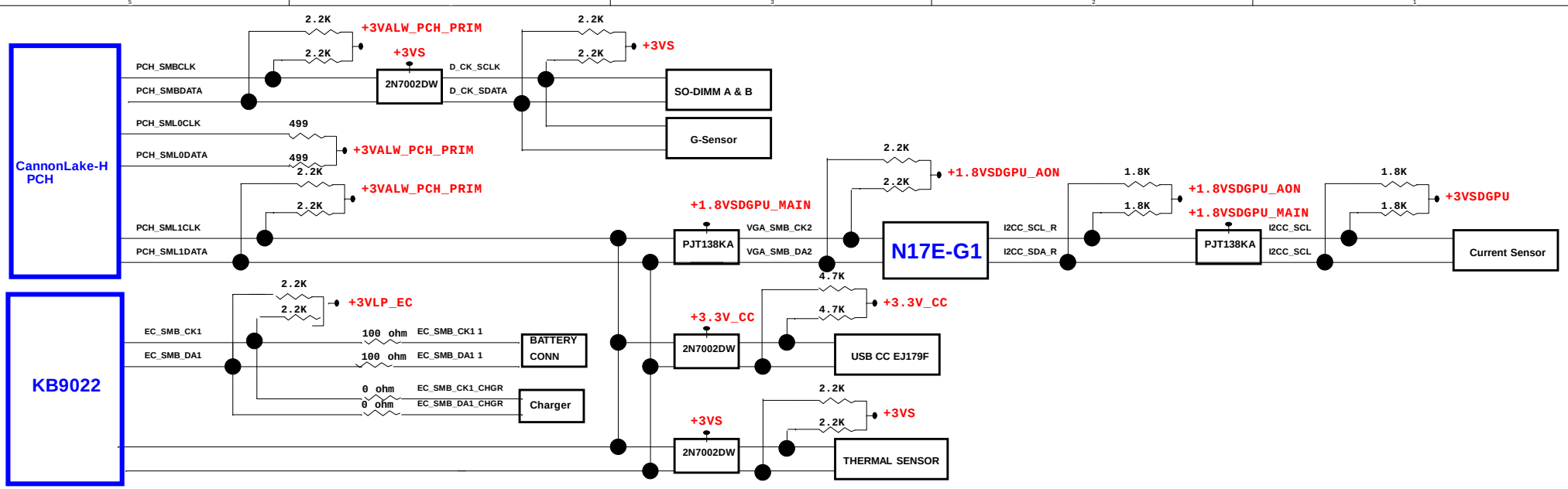

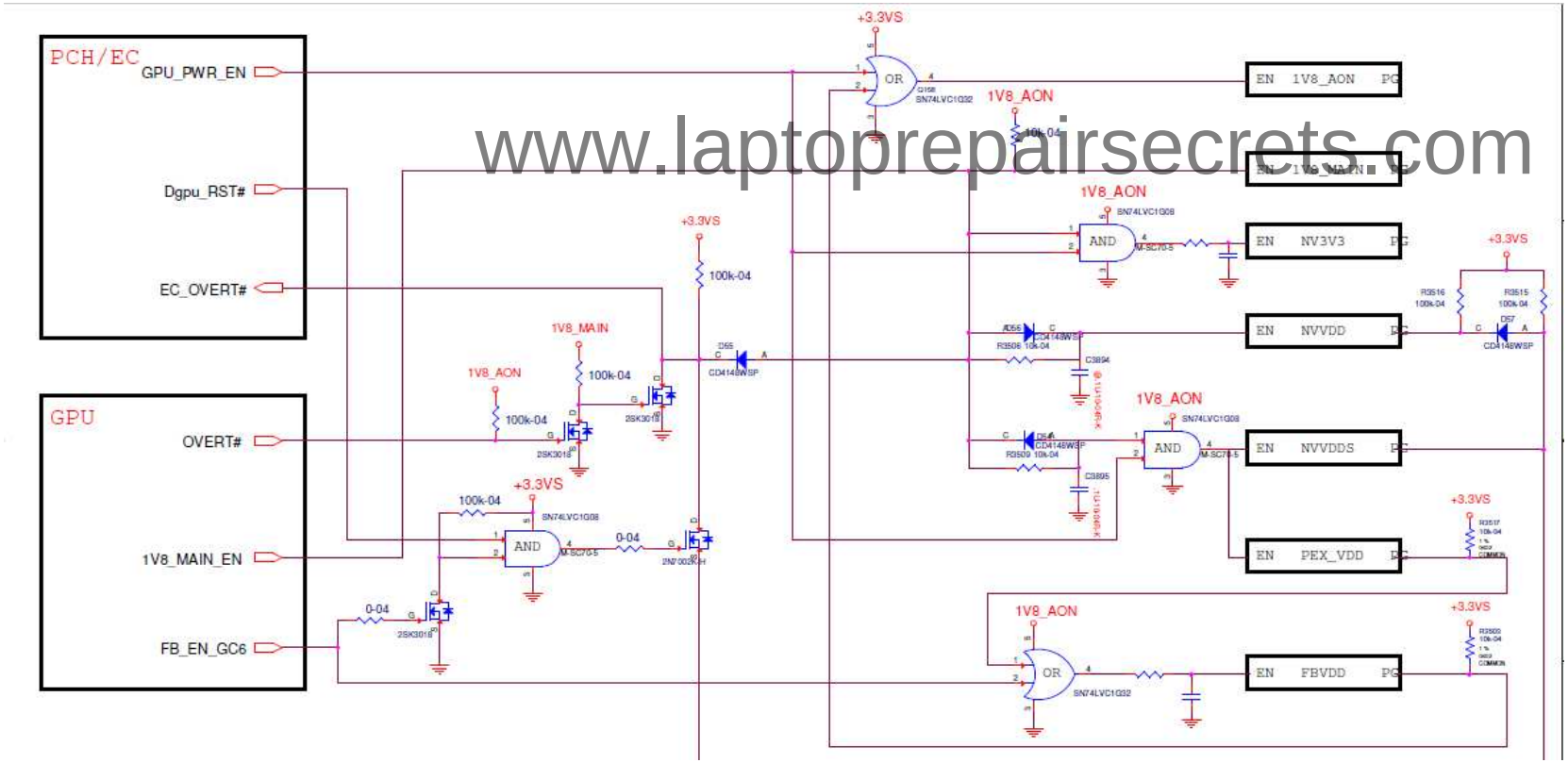

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	N17E-GDDR5_D
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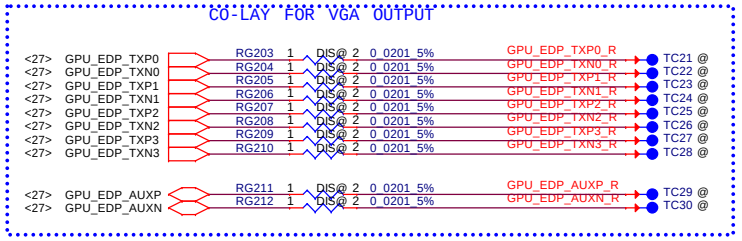

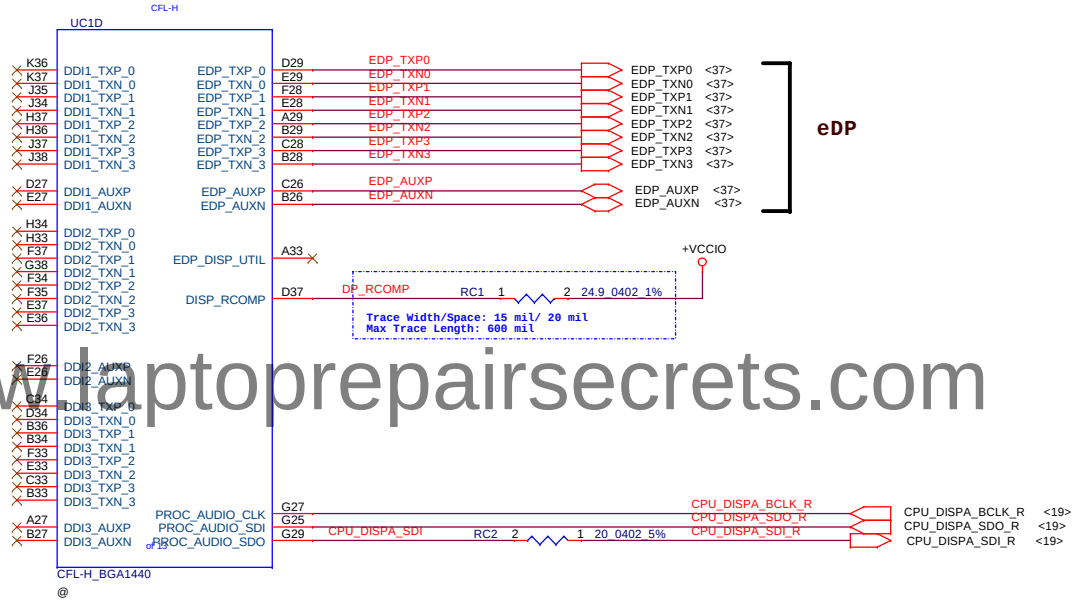

ZZZ

PCB@ DAZ29000103

PCB DH53F LA-F991P LS-F992P/E921P

Coffee Lake-H CPU SKU

UC1

CFL-H_BGA1440

S IC CL8068403373522 SR3Z0 U0 2.3G ABO!

SA0000BPJ40

5@

UC1

CFL-H_BGA1440

S IC CL8068403359524 SR3YY U0 2.2G ABO!

SA0000BPZ40

i7@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CFL-H(1/8)DDI/eDP

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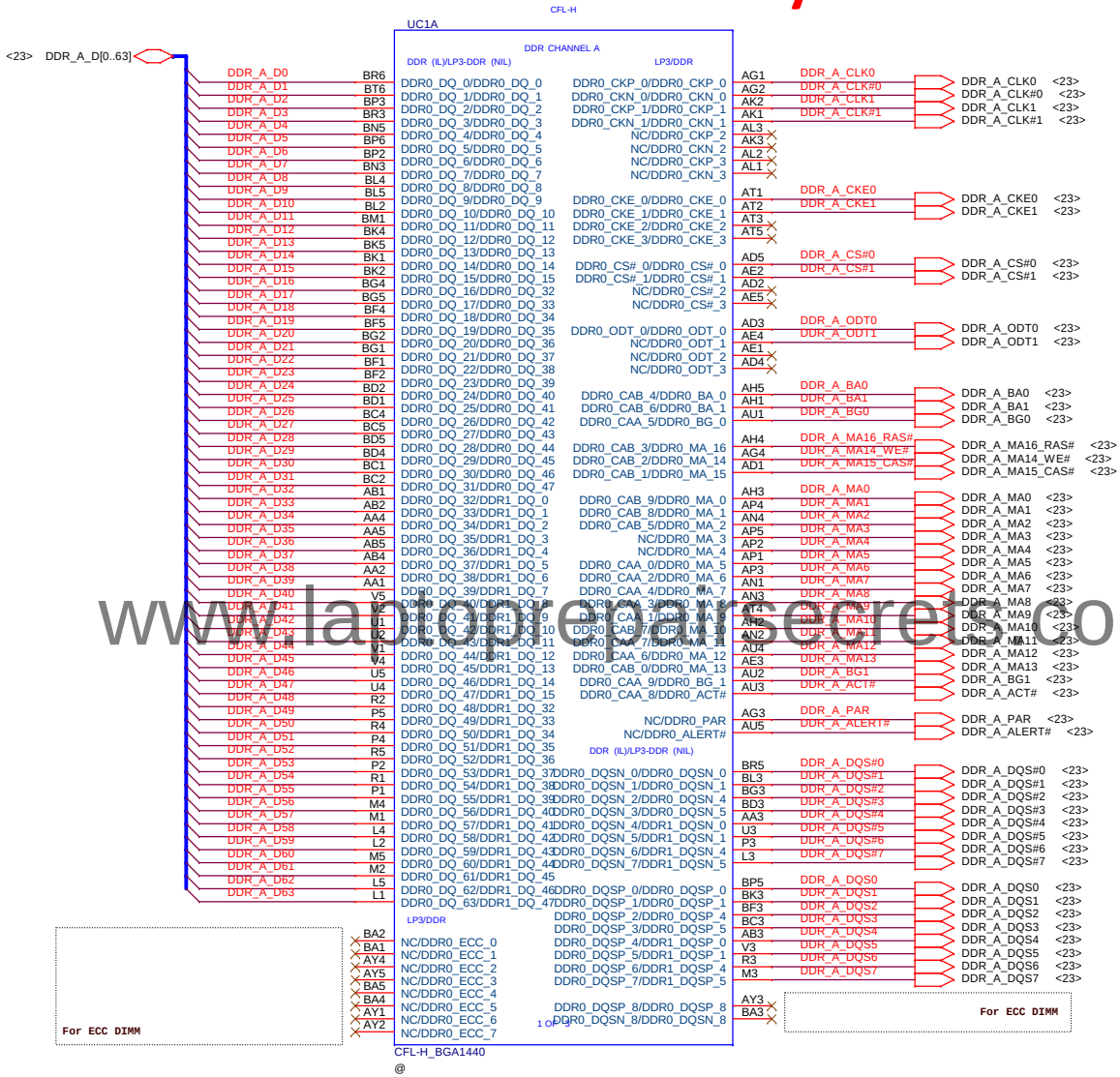
CHANNEL-A

Interleaved Memory



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Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	CFL-H(2/8)DIMMA		
Size	Document Number		Rev
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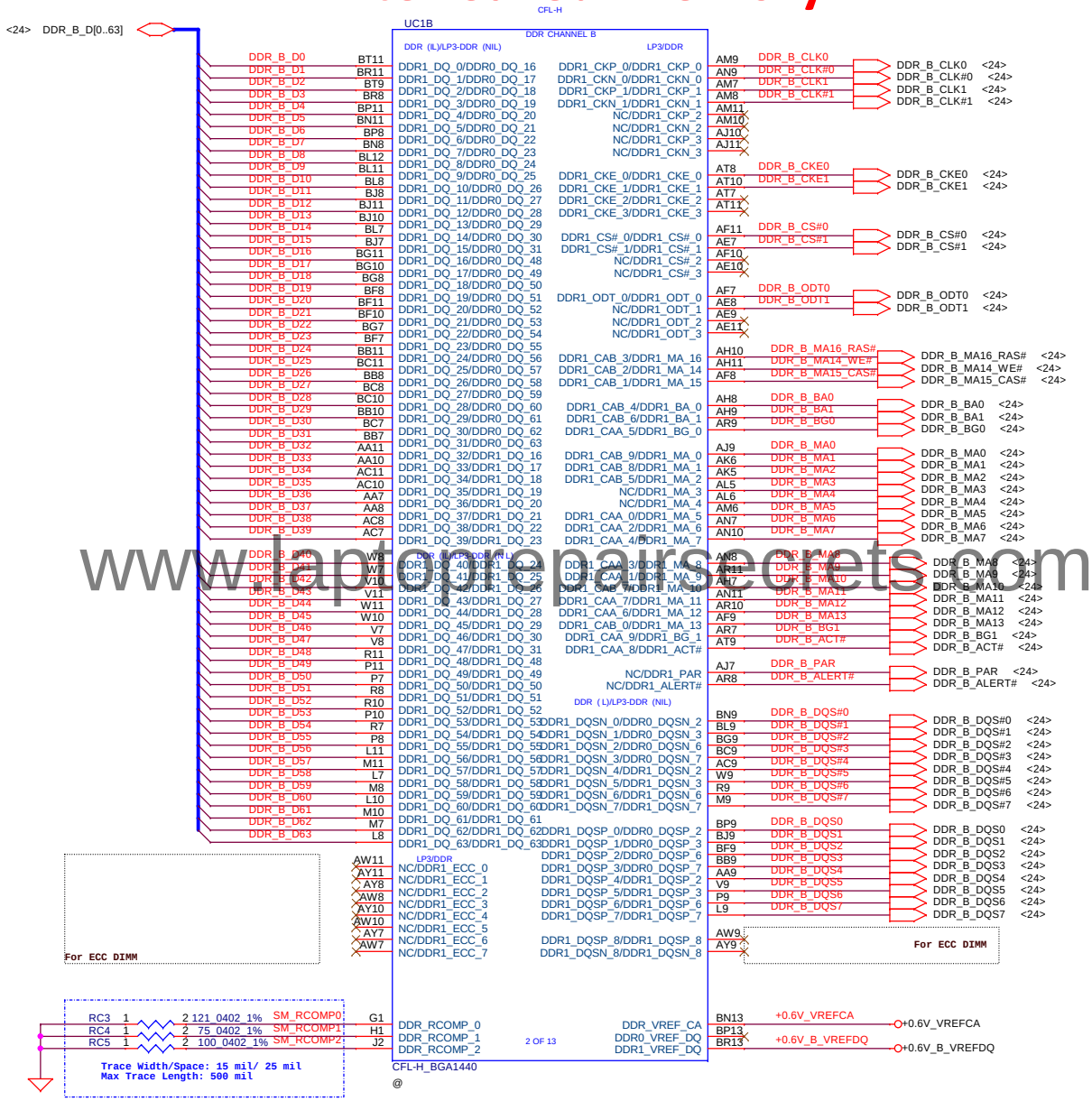
CHANNEL - B

Interleaved Memory



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Compal Electronics, Inc.			
Title	CFL-H(3/8)DIMMB		
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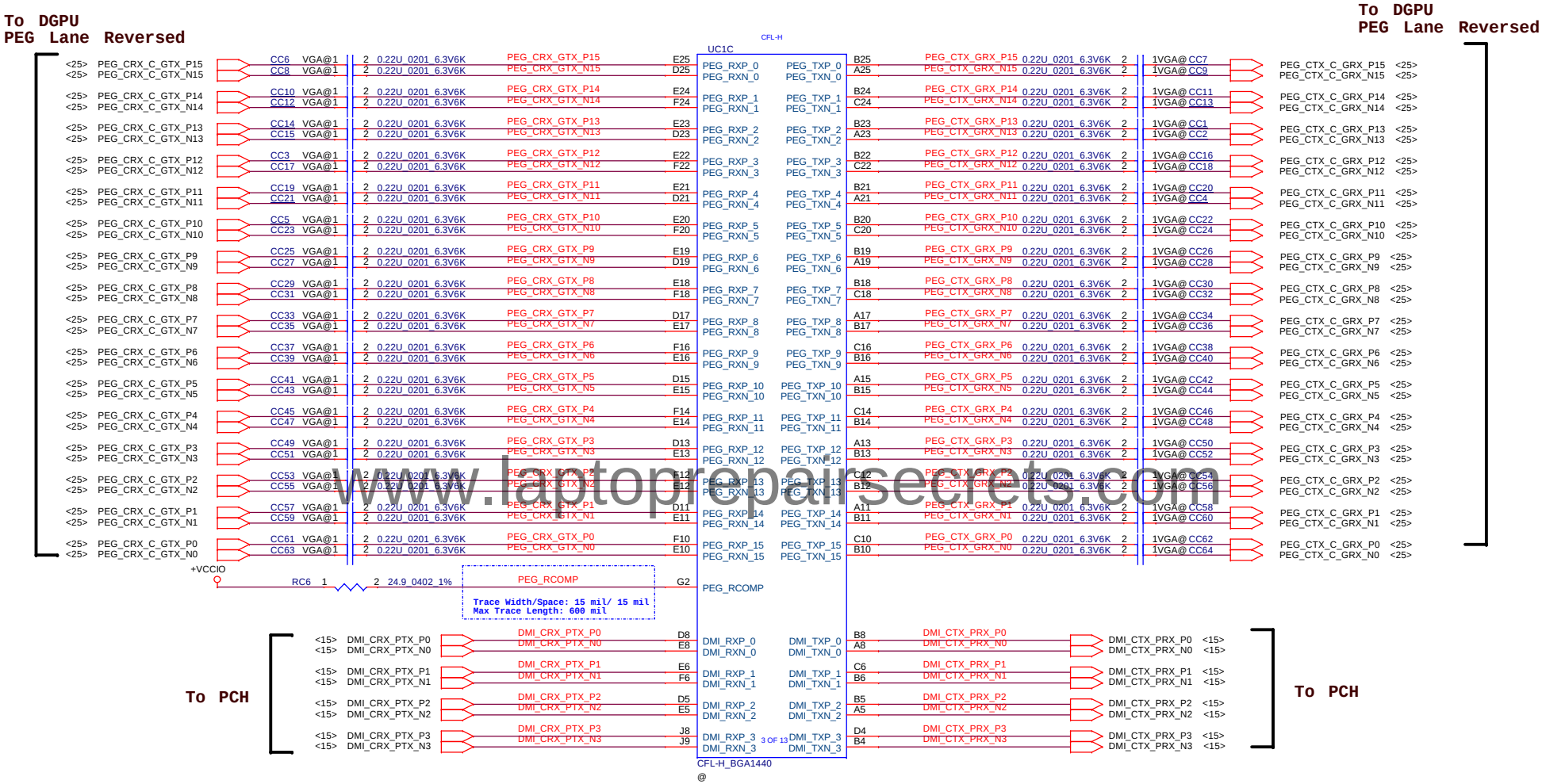
PEG&DMI



Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	PEG/DMI		
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
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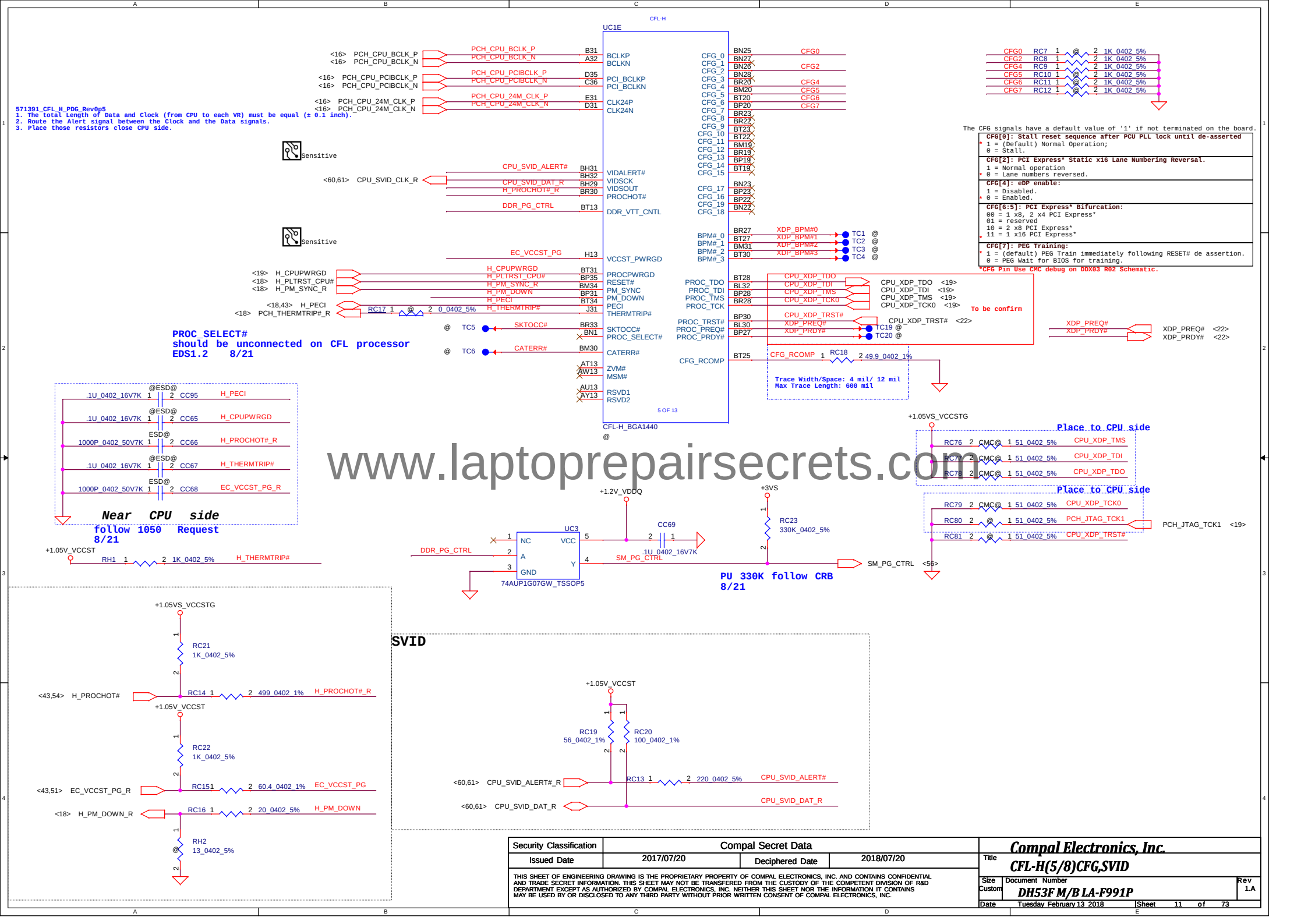
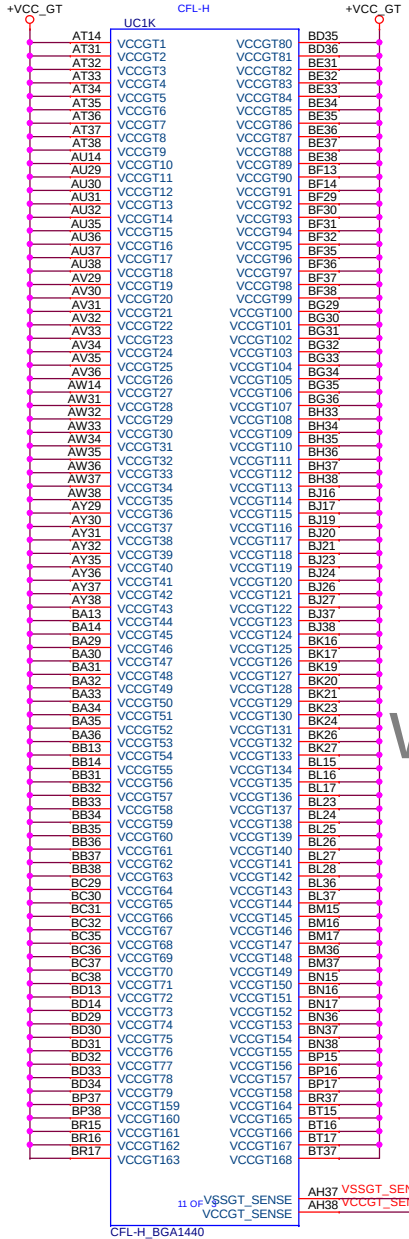
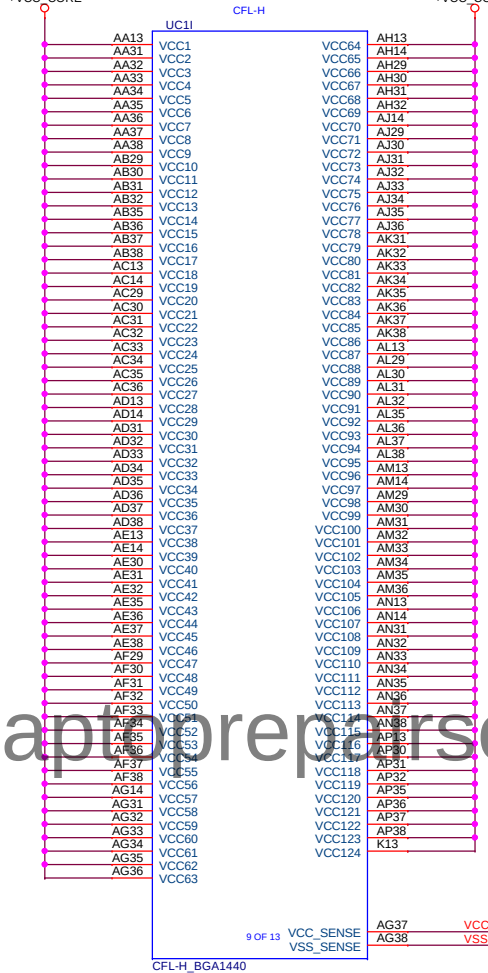


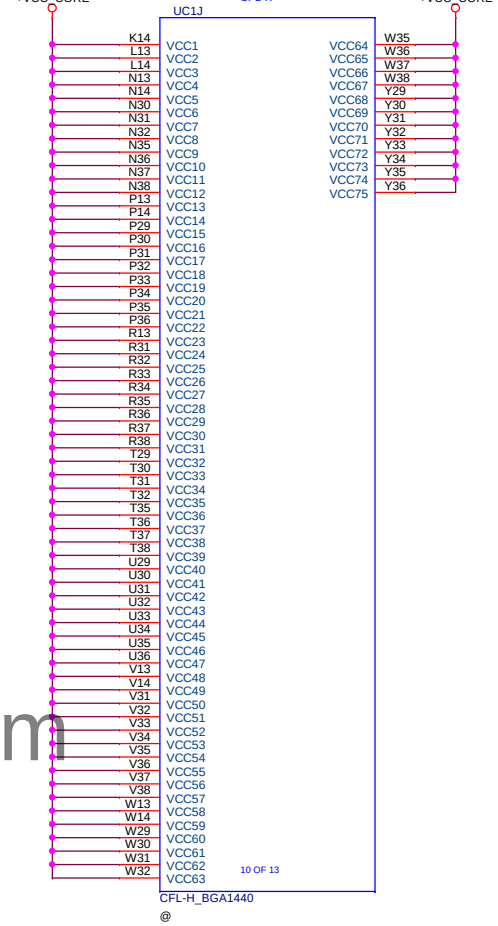
GT
32000mA(Hexa Core GT2)



1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

128000mA(Hexa Core GT2)





1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

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Title: CFL-H(6/8)VCC CORE/GT

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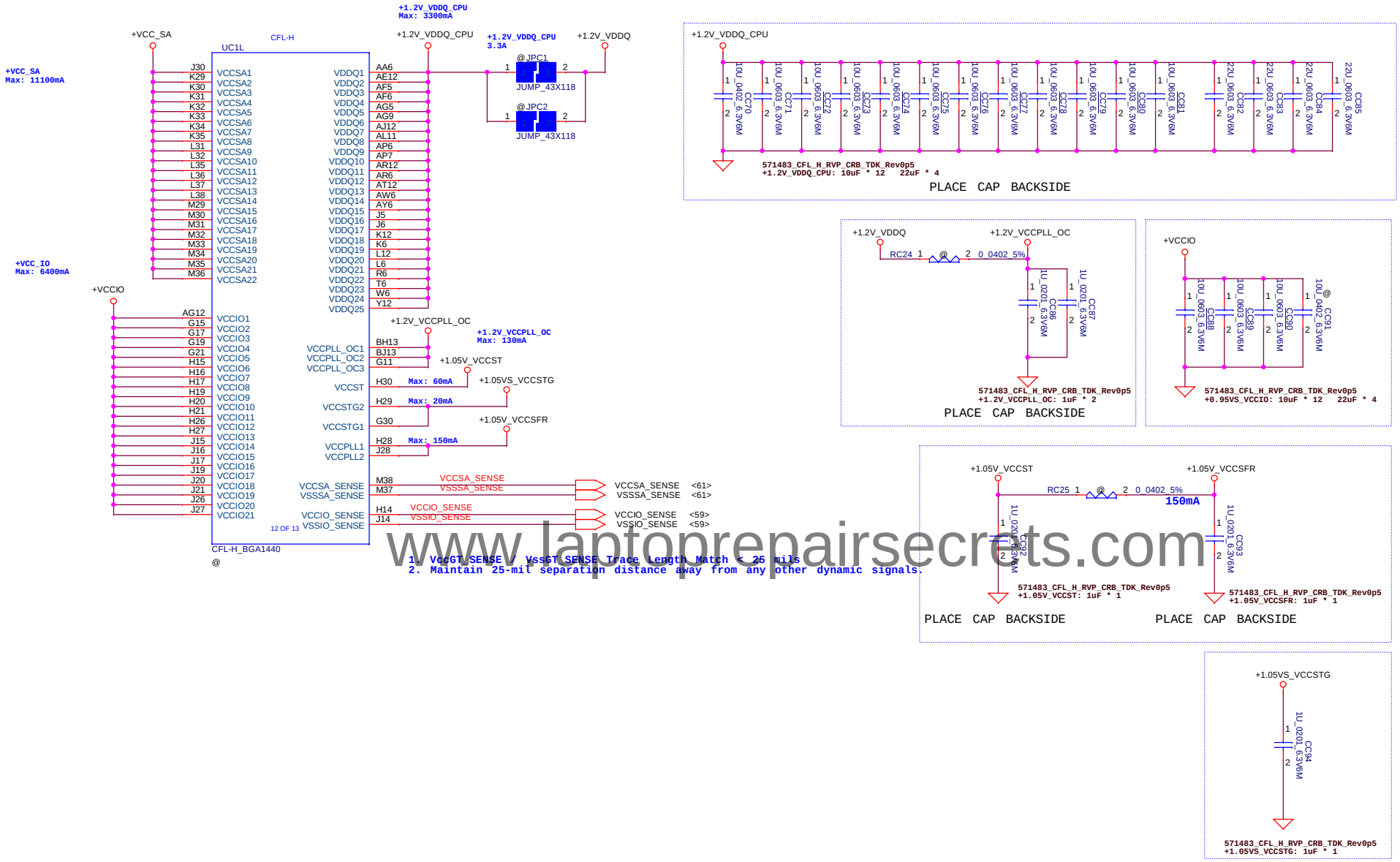

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Compal Electronics, Inc.			
Title	CFL-H(7/8)VCCSA/VCCIO/VDDQ		
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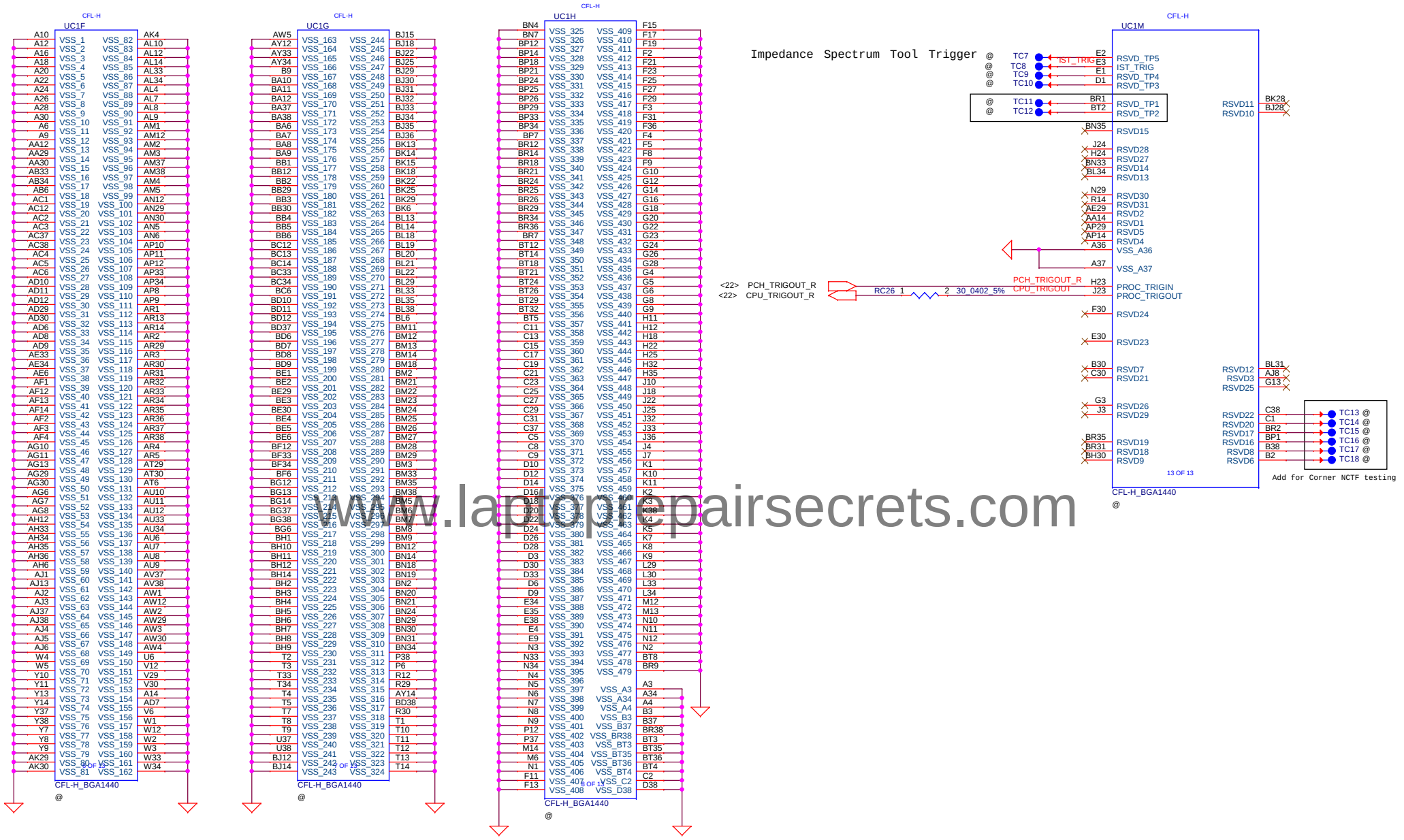

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: CFL-H(8/8)GND/RSVD

Size	Document Number	Rev
Custom	DH53F M/B LA-F991P	1.A
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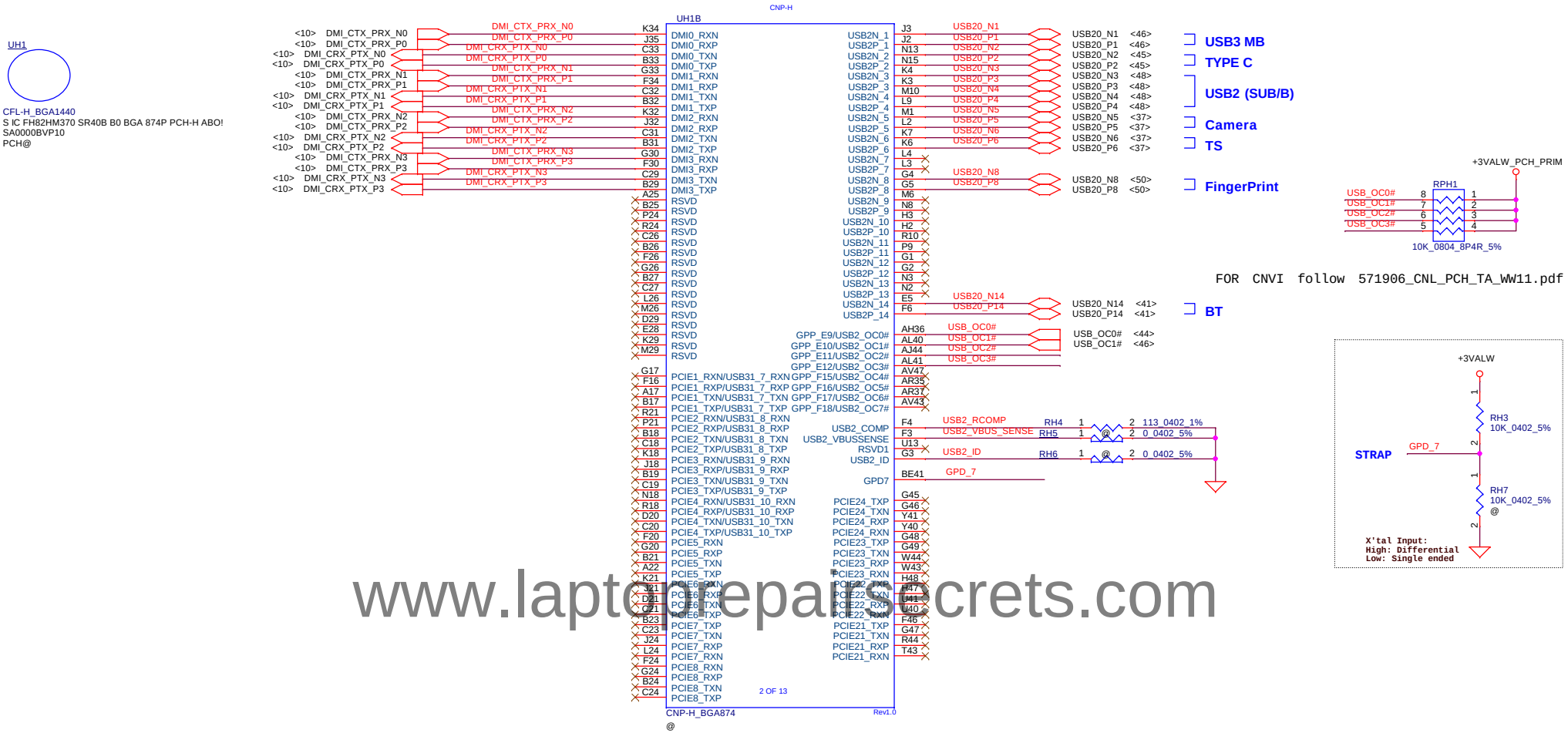

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5 / GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 / GbE	PCIe* #10	PCIe* #11 / SATA 0a	PCIe* #12 / SATA 1a / GbE	PCIe* #13 / SATA 0b / GbE	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

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Title: PCH(1/8)DMI/PCIE/USB2

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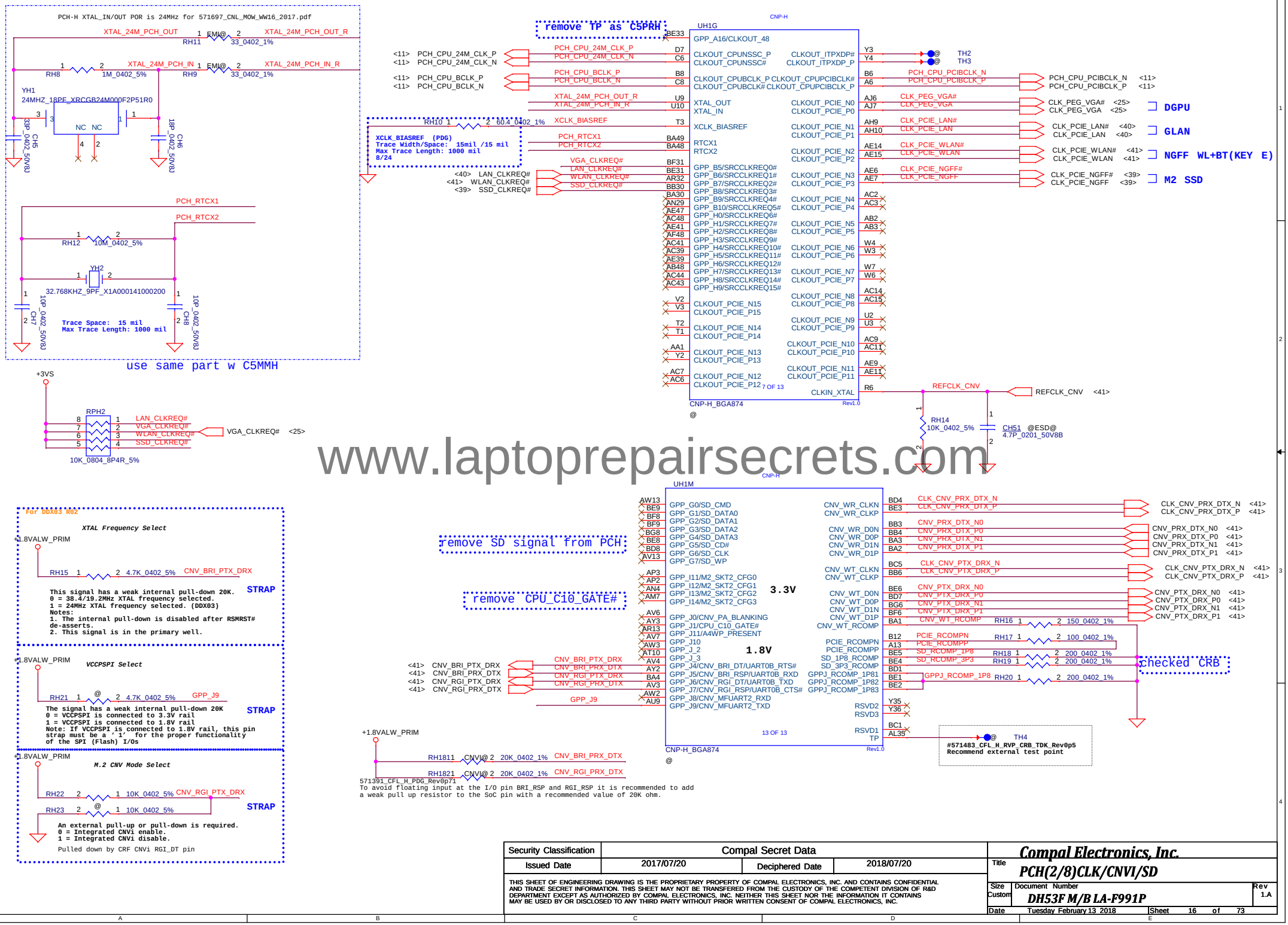

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PCH(2/8)CLK/CNVI/SD		
Size Custom	Document Number DH53F M/B LA-F991P		Rev 1.A
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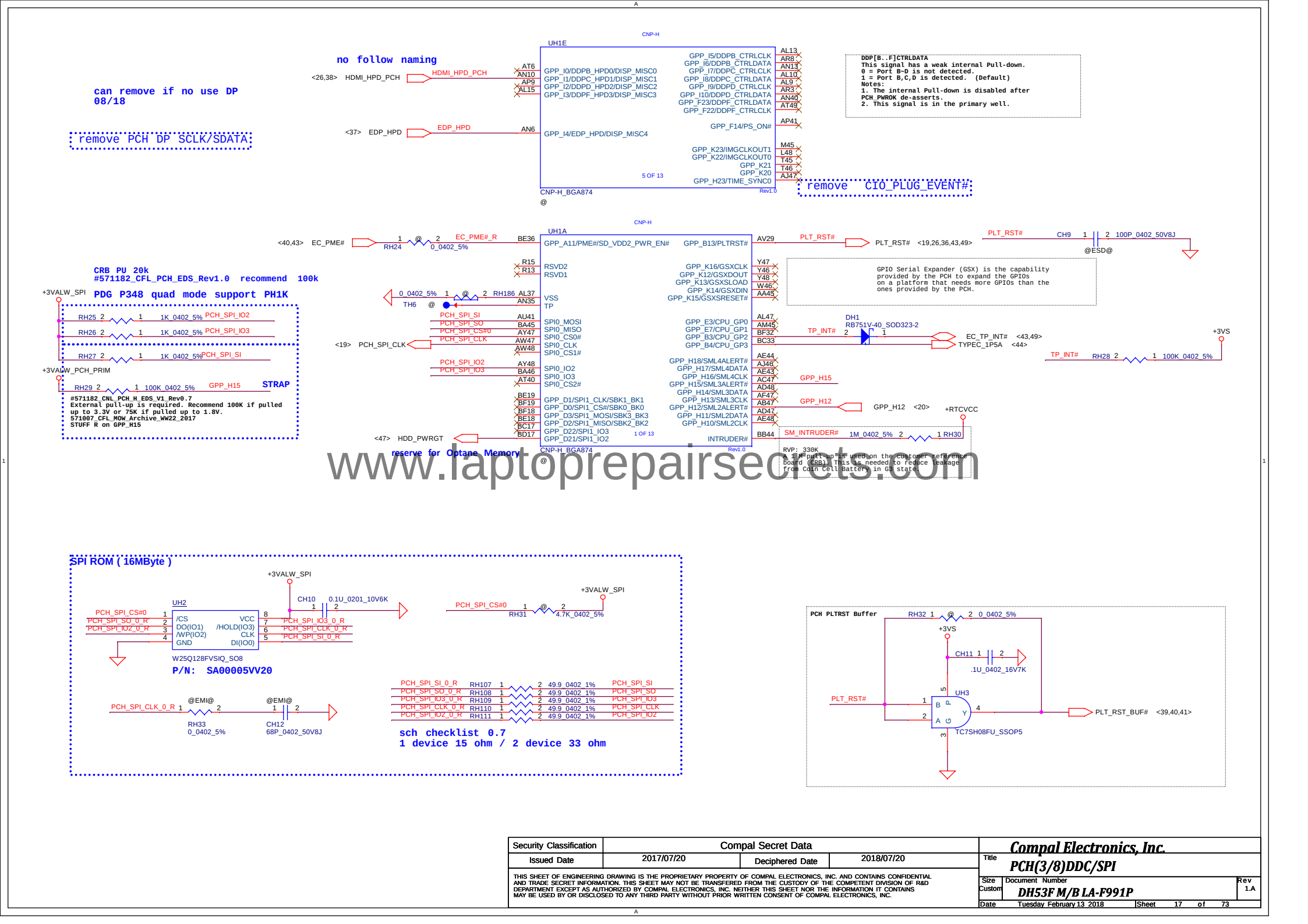

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PCH(3/8)DDC/SPI		
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#571391_CFL_H_PDG_Rev0p5
• eSPI clock and eSPI data mismatched: <500 mils.
• eSPI clock and eSPI chip select mismatched: <500 mils.
• eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.
CNP-H
UH1F
USB3 MB
USB3_PTX_DRX_N1
USB3_PTX_DRX_P1
USB3_PRX_DTX_N1
USB3_PRX_DTX_P1
USB3 Type C
USB3_PTX_DRX_N2
USB3_PTX_DRX_P2
USB3_PRX_DTX_N2
USB3_PRX_DTX_P2
USB3 SUB
USB3_PTX_DRX_N5
USB3_PTX_DRX_P5
USB3_PRX_DTX_N5
USB3_PRX_DTX_P5
USB3 Type C
USB3_PTX_DRX_P3
USB3_PTX_DRX_N3
USB3_PRX_DTX_P3
USB3_PRX_DTX_N3
USB3 SUB
USB3_PTX_DRX_P4
USB3_PTX_DRX_N4
USB3_PRX_DTX_P4
USB3_PRX_DTX_N4
USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN
1.8V (eSPI)
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
6 OF 13
CNP-H_BGA874
Rev1.0
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3
LPC Bus
LPC : +3.3V
check straps
LPC_FRAME# <43,49>
TPM_SERIRQ <43,49>
LPC_PIRQA#
ESPI_RST# <43>
CLK_LPC
CLK_LPC_TPM
RH35 22_0402_5%
RH36 22_0402_5%
TPM@
CLK_LPC_R <43>
CLK_LPC_TPM_R <49>
SSD_DEVSLP1 <39>
+3VS
TPM_SERIRQ RH37 10K_0402_5%
LPC_PIRQA# RH38 10K_0402_5%
UH1C
For Intel CLINK
TH10 @
TH11 @
TH12 @
CL_CLK
CL_DATA
CL_RST#
GPP_K8
GPP_K9
GPP_K10
GPP_K11
GPP_K0
GPP_K1
GPP_K2
GPP_K3
GPP_K4
GPP_K5
GPP_K6
GPP_K7
M.2 SSD PCIE L1
PCIE_PTX_DRX_P11
PCIE_PTX_DRX_N11
PCIE_PRX_DTX_P11
PCIE_PRX_DTX_N11
PCIE11_TXP/SATA0A_TXP
PCIE11_TXN/SATA0A_TXN
PCIE11_RXP/SATA0A_RXP
PCIE11_RXN/SATA0A_RXN
DGPU_PRSNT#
GPP_F10/SATA_SCLOCK
GPP_F11/SATA_SLOAD
GPP_F13/SATA_SDATAOUT0
GPP_F12/SATA_SDATAOUT1
GLAN
PCIE_PTX_C_DRX_N14
PCIE_PTX_C_DRX_P14
PCIE_PRX_DTX_N14
PCIE_PRX_DTX_P14
CH3 .1U_0402_16V7K
CH4 .1U_0402_16V7K
PCIE14_TXN/SATA1B_TXN
PCIE14_TXP/SATA1B_TXP
PCIE14_RXN/SATA1B_RXN
PCIE14_RXP/SATA1B_RXP
PCIE13_TXN/SATA0B_TXN
PCIE13_TXP/SATA0B_TXP
PCIE13_RXN/SATA0B_RXN
PCIE13_RXP/SATA0B_RXP
M.2 SSD PCIE L0
PCIE_PTX_DRX_P12
PCIE_PTX_DRX_N12
PCIE_PRX_DTX_P12
PCIE_PRX_DTX_N12
PCIE12_TXP/SATA1A_TXP
PCIE12_TXN/SATA1A_TXN
PCIE12_RXP/SATA_1A_RXP
PCIE12_RXN/SATA1A_RXN
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
3 OF 13
CNP-H_BGA874
PCIE9_RXN PCIE9_RXP PCIE9_TXN PCIE9_TXP
PCIE_PRX_DTX_N9 PCIE_PRX_DTX_P9 PCIE_PTX_DRX_N9 PCIE_PTX_DRX_P9
M.2 SSD PCIE L3
PCIE10_RXN PCIE10_RXP PCIE10_TXN PCIE10_TXP
PCIE_PRX_DTX_N10 PCIE_PRX_DTX_P10 PCIE_PTX_DRX_N10 PCIE_PTX_DRX_P10
M.2 SSD PCIE L2
PCIE15_RXN/SATA2_RXN
PCIE15_RXP/SATA2_RXP
PCIE15_SATA2_TXN
PCIE15_TXP/SATA2_TXP
PCIE_PRX_DTX_N15 PCIE_PRX_DTX_P15 PCIE_PTX_C_DRX_N15 PCIE_PTX_C_DRX_P15
CH1 .1U_0402_16V7K
CH2 .1U_0402_16V7K
NGFF WL+BT(KEY E)
PCIE16_RXN/SATA3_RXN
PCIE16_RXP/SATA3_RXP
PCIE16_TXN/SATA3_TXN
PCIE16_TXP/SATA3_TXP
PCIE17_RXN/SATA4_RXN
PCIE17_RXP/SATA4_RXP
PCIE17_TXN/SATA4_TXN
PCIE17_TXP/SATA4_TXP
SATA_PRX_DTX_N4 SATA_PRX_DTX_P4 SATA_PTX_DRX_N4 SATA_PTX_DRX_P4
HDD
PCIE18_RXN/SATA5_RXN
PCIE18_RXP/SATA5_RXP
PCIE18_TXN/SATA5_TXN
PCIE18_TXP/SATA5_TXP
GPP_E8/SATA_LED#
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_F0/SATAXPCIE3/SATAGP_3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7
SATA_GP1 <39>
RH187 PBA@ 1K_0402_5%
TH13
SATA_GP5
+3VS
SATA_GP1 RH39 10K_0402_5%
M.2 SSD PCIE/SATA select pin
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN
PCH_BKL_PWM <26,37>
ENBKL <26,43>
PCH_ENVDD <26,37>
THRMTRIP#
PECI
PM_SYNC
PLTRST_CPU#
PM_DOWN
#571391_CFL_H_PDG_Rev0p5.pdf
RH40 620_0402_5%
RH41 13_0402_5%
RH42 30_0402_5%
PCH_THERMTRIP#_R <11>
H_PECI <11,43>
H_PM_SYNC_R <11>
H_PLTRST_CPU# <11>
H_PM_DOWN_R <11>
+3VALW_PCH_PRIM
RH43 10K_0402_5% UMA@
DGPU_PRSNT#
RH44 10K_0402_5% VGA@

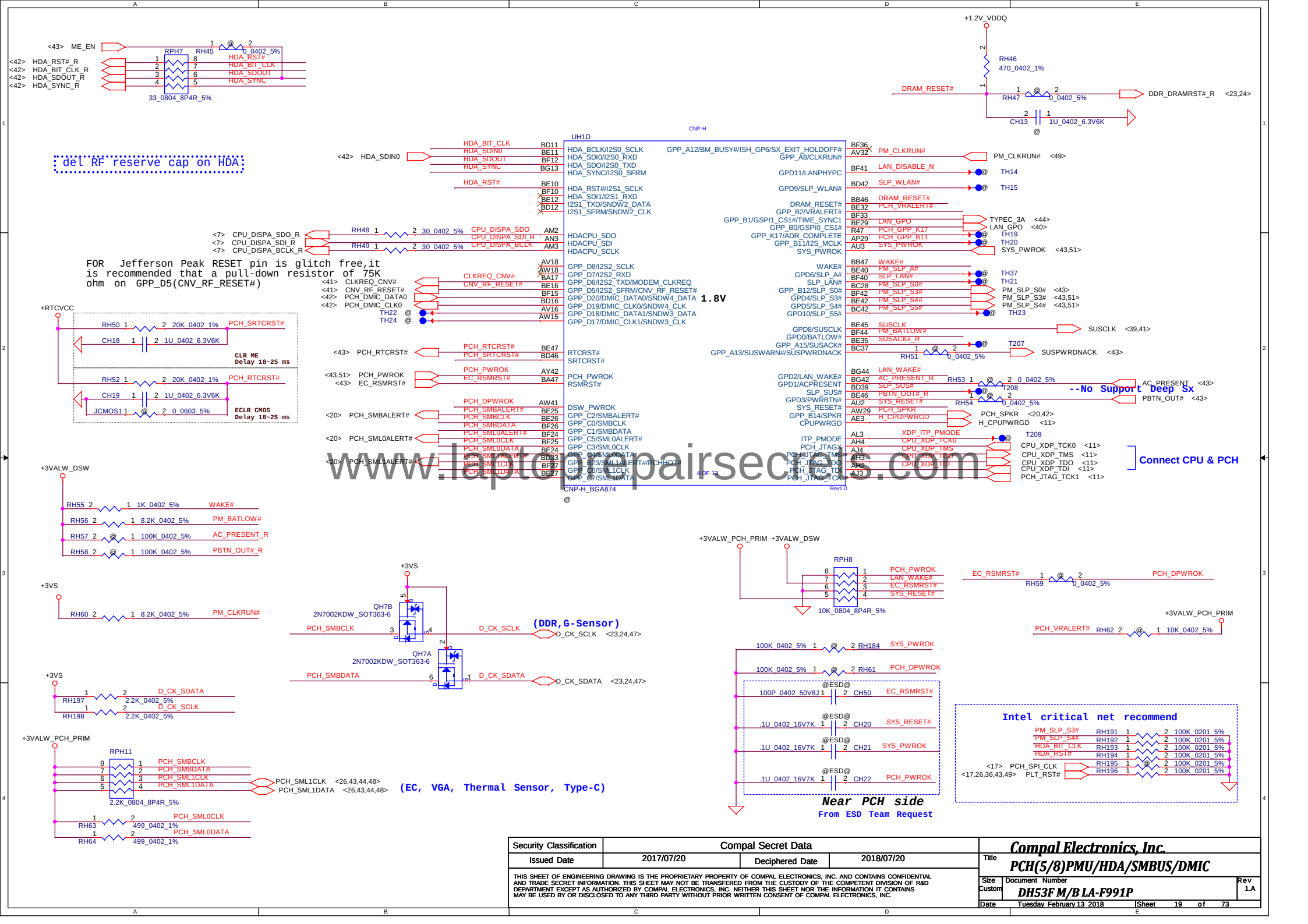
	GPP_F13
	DGPU PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: **PCIE/SATA/USB3/eSPI**

Size: Custom — Document Number: **DH53F M/B LA-F991P** — Rev 1.A



Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

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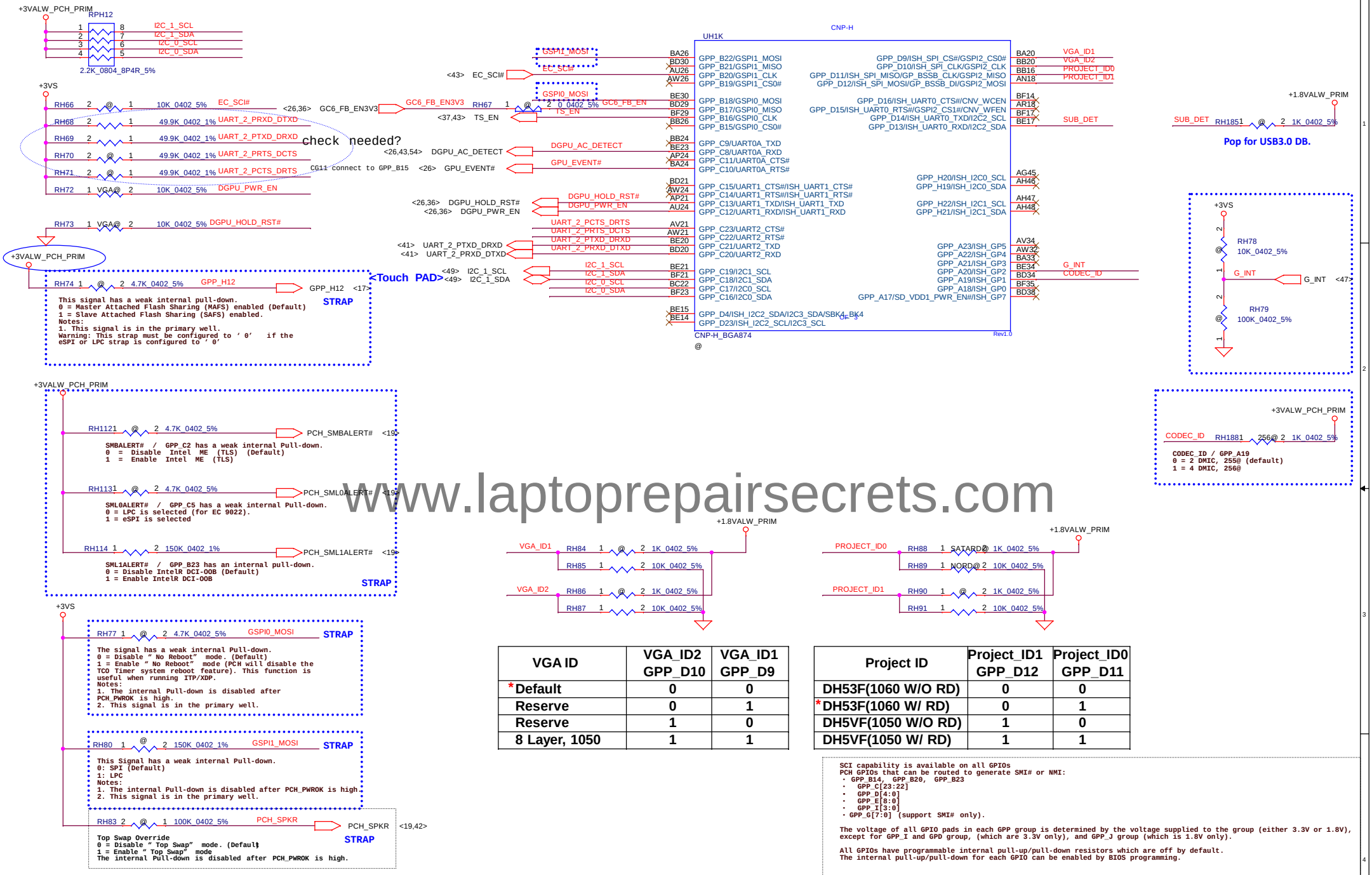
Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS/DMIC

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 19 of 73



VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
*Default	0	0
Reserve	0	1
Reserve	1	0
8 Layer, 1050	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
DH53F(1060 W/O RD)	0	0
*DH53F(1060 W/ RD)	0	1
DH5VF(1050 W/O RD)	1	0
DH5VF(1050 W/ RD)	1	1

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

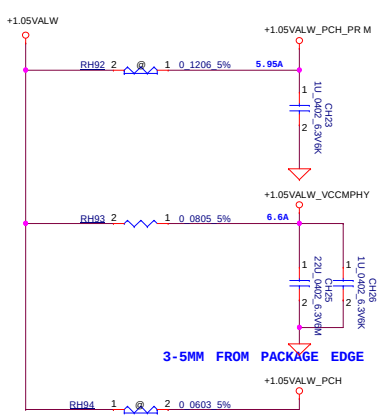
Compal Electronics, Inc.

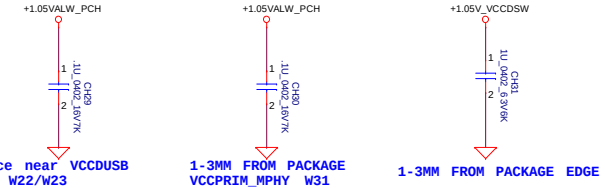
Title: PCH(6/8)GPIO/I2C/UART/STRAP

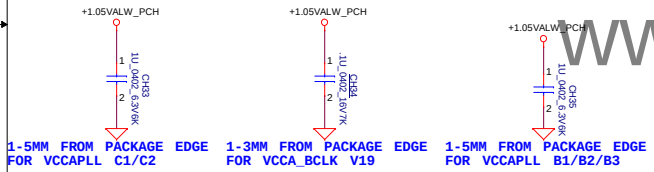
Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

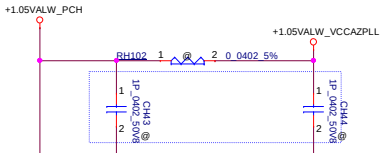
Date: Tuesday, February 13, 2018 | Sheet 20 of 73

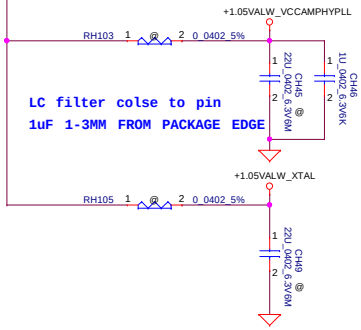
GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

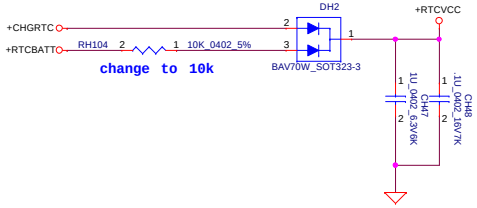


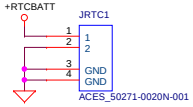


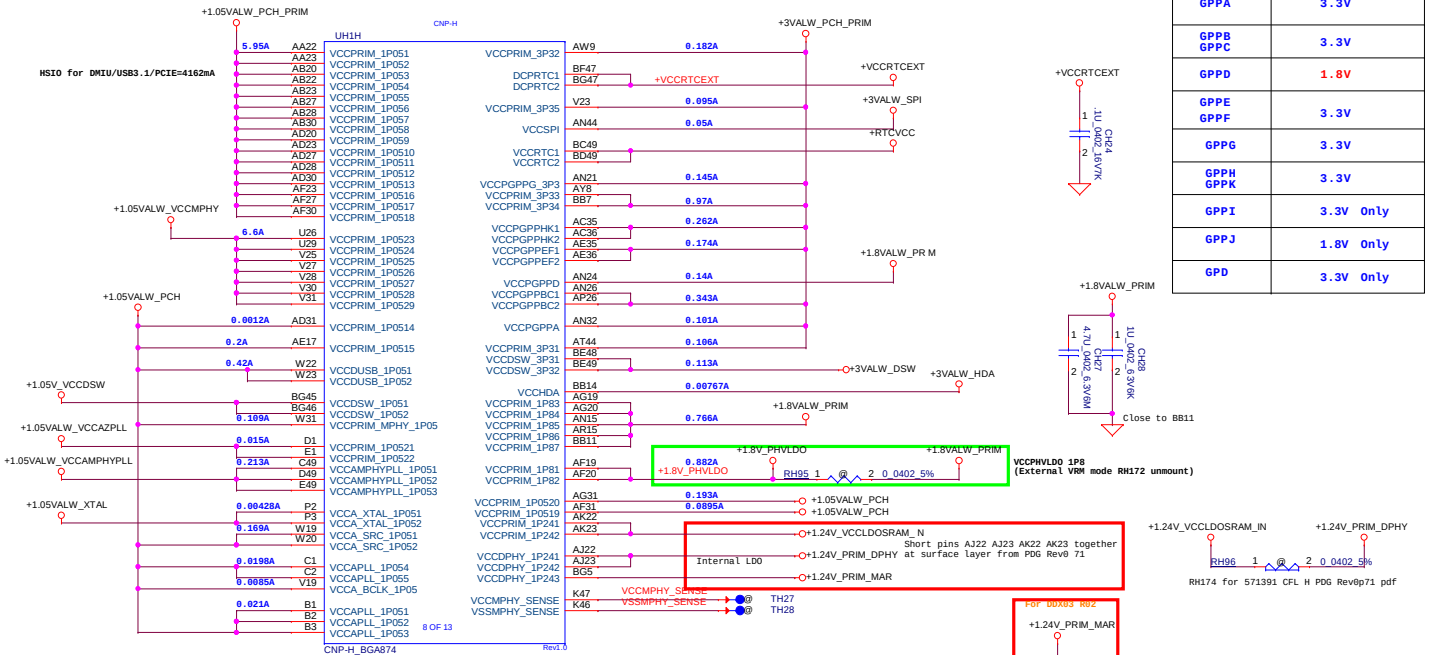


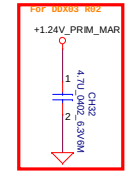


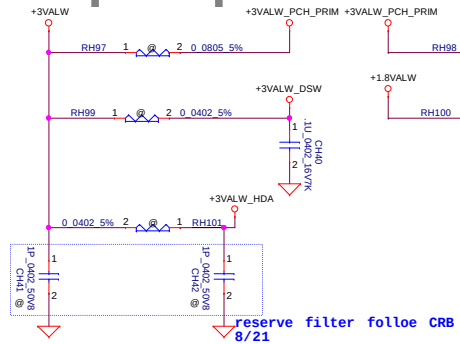


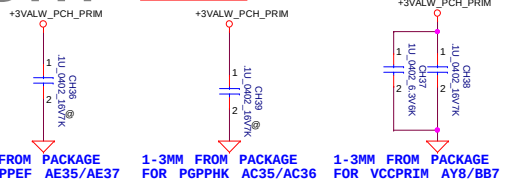












Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Title	Compal Electronics, Inc.		
	PCH(7/8)Power		
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
Date: Tuesday, February 13, 2018	Sheet: 21	of: 73	

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

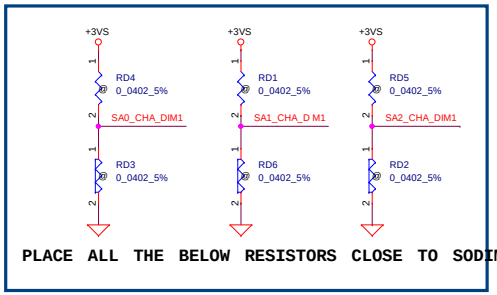
Compal Electronics, Inc.		
Title	PCH(8/8)GND/RSVD	
Size: Custom	Document Number: DH53F M/B LA-F991P	Rev: 1.A
Date: Tuesday, February 13, 2018	Sheet 22 of 73	

CHANNEL-A

BOT REVERSE TYPE (4 mm)

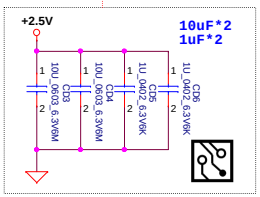
Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM



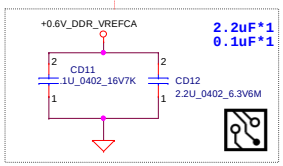
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

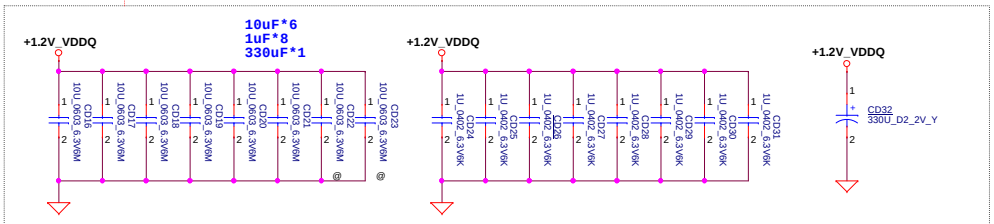


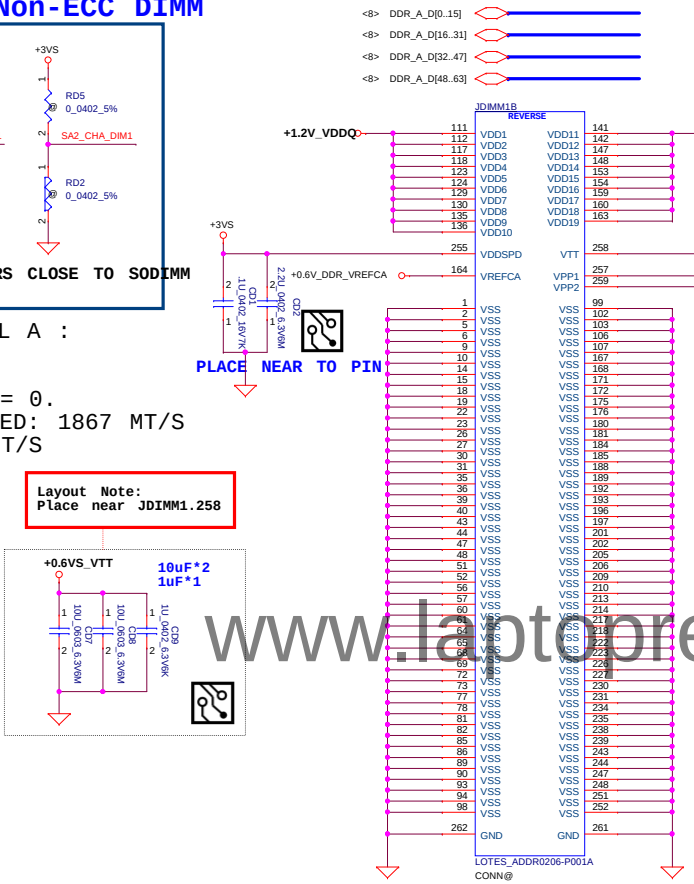
Layout Note:
Place near JDIMM1.258

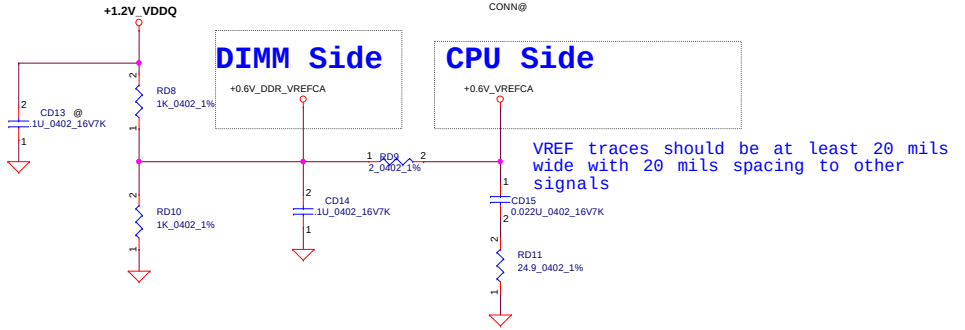
Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1





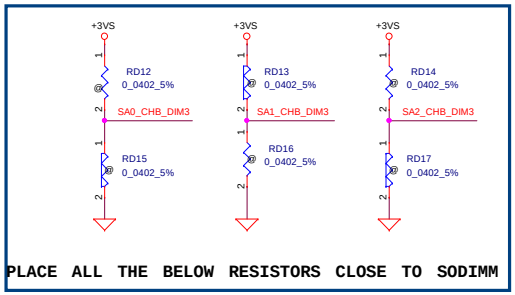


Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.		
Title	DDRIV_CHA: DIMM0	
Size	Document Number: DH53F M/B LA-F991P	Rev: 1.A
Date: Tuesday, February 13, 2018	Sheet 23 of 73	

CHANNEL-B

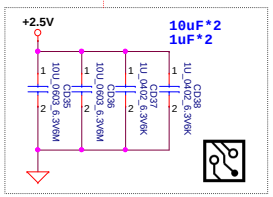
TOP: JDIMM3 CONN Non-ECC DIMM



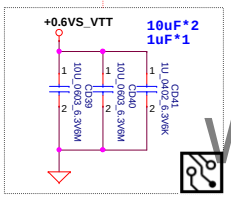
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

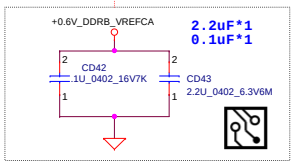
Layout Note:
Place near JDIMM3.257,259



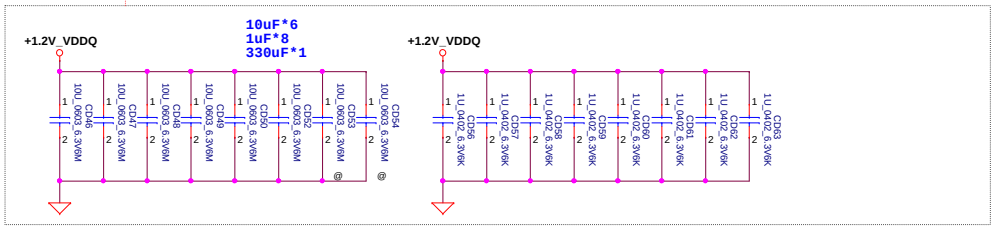
Layout Note:
Place near JDIMM3.258



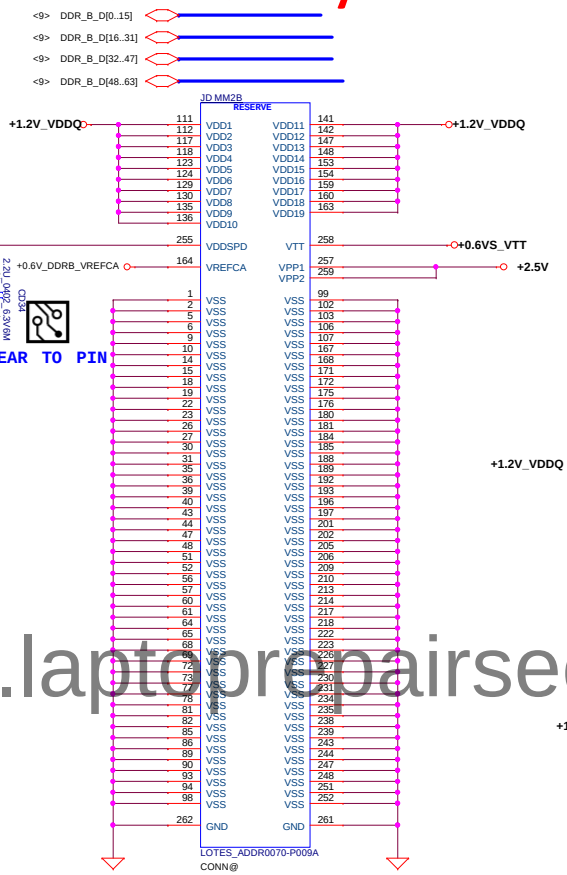
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



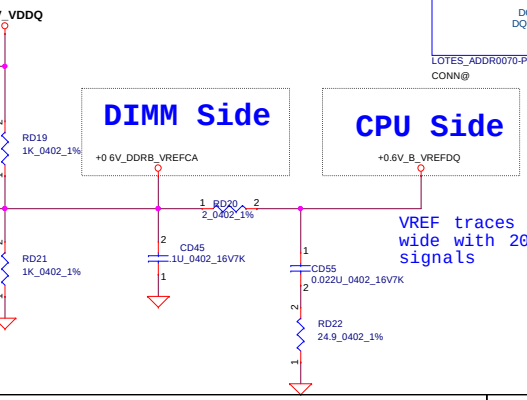
Layout Note:
Place near JDIMM3



Interleaved Memory



BOT REVERSE TYPE (8 mm)



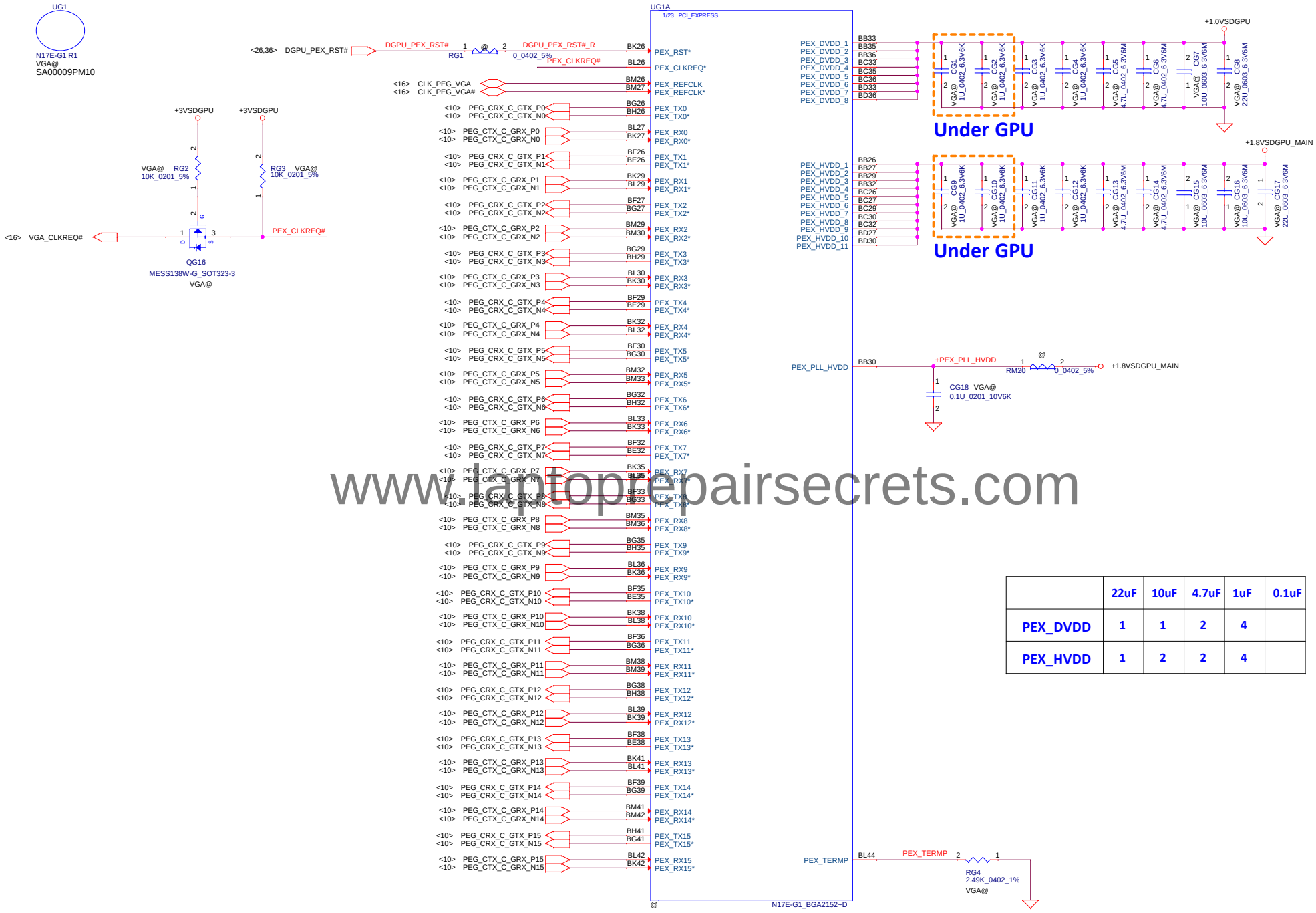
Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 24 of 73



	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

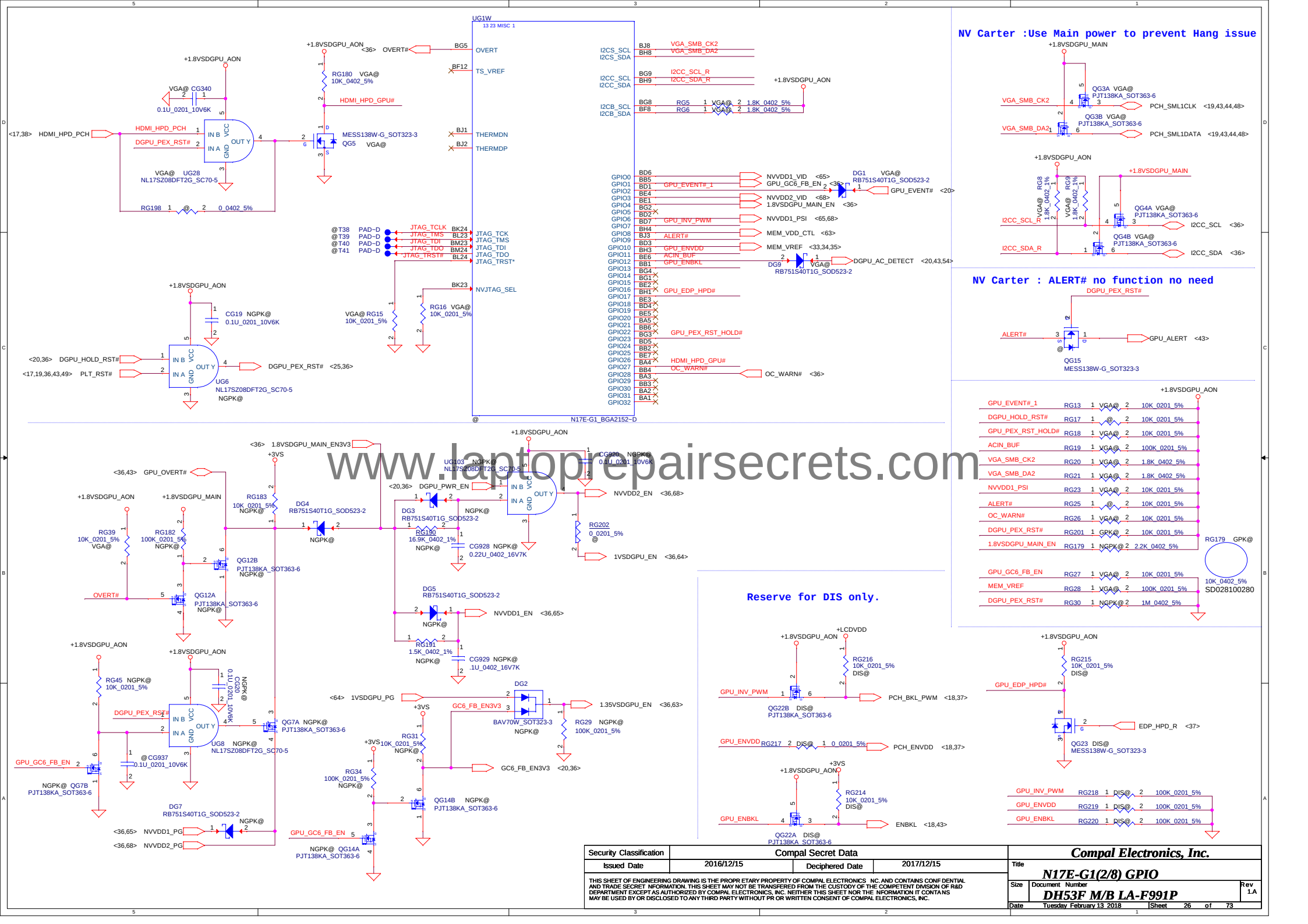
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(1/8) PCIE**

Size: | Document Number: **DH53F M/B LA-F991P** | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 25 of 73



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(2/8) GPIO**

Size: | Document Number: **DH53F M/B LA-F991P** | Rev: 1.A

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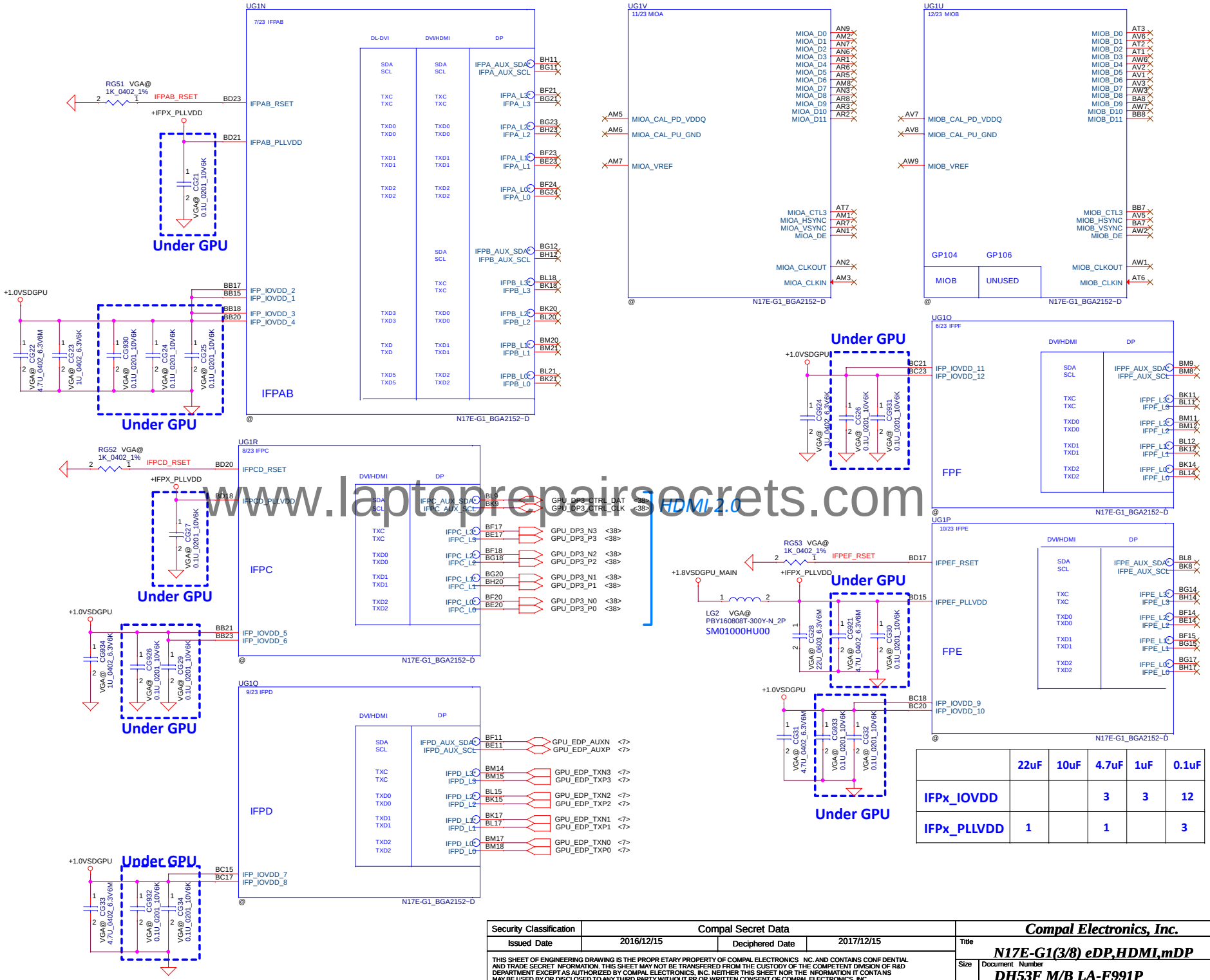


	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	3	12
IFPx_PLLVDD	1		1		3

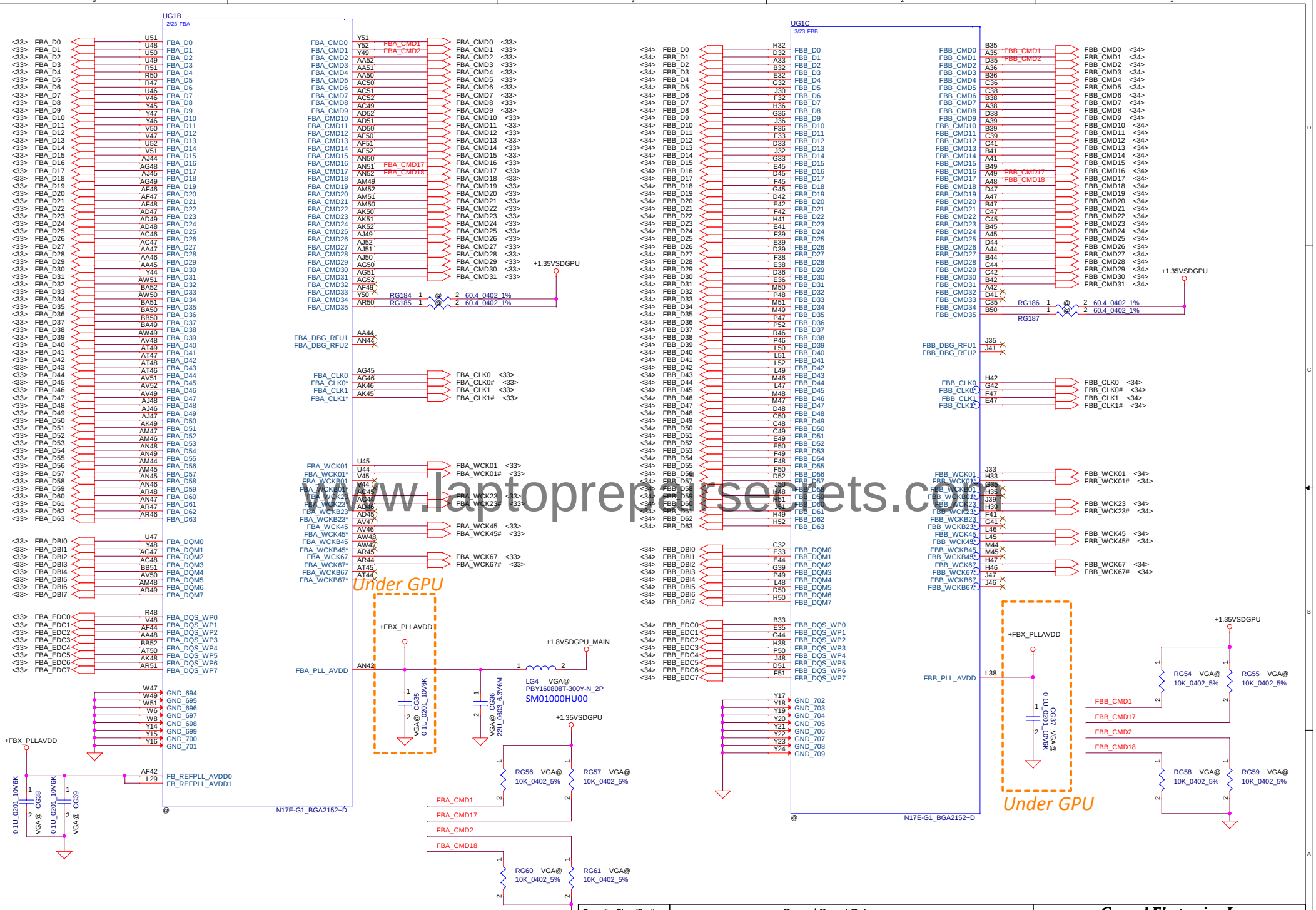
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: N17E-G1(3/8) eDP,HDMI,mDP

Size: | Document Number: DH53F M/B LA-F991P | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 27 of 73



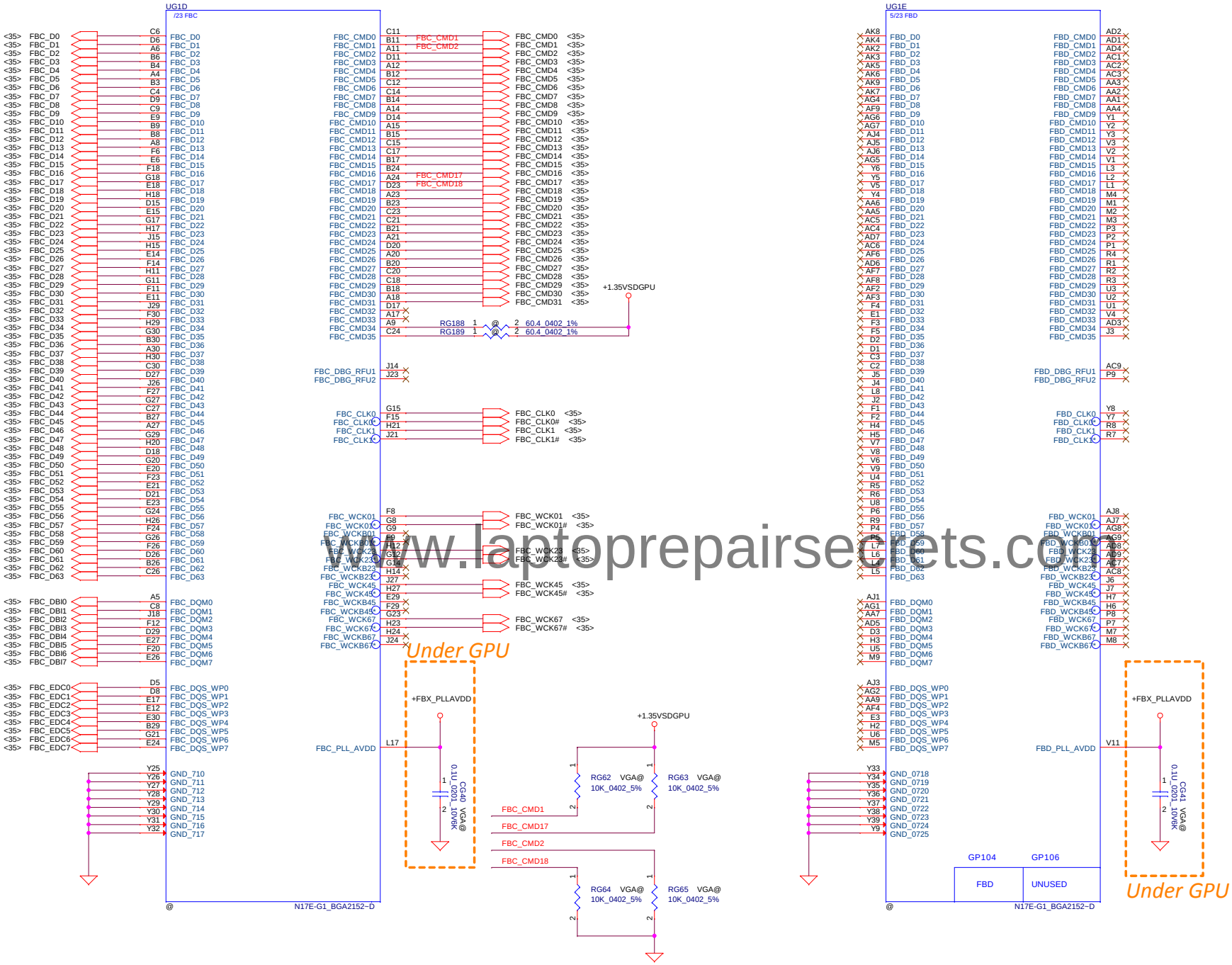
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(4/8) MEM Interface**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 28 of 73



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(5/8) MEM Interface**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A
Date: Tuesday, February 13, 2018	Sheet 29 of 73	

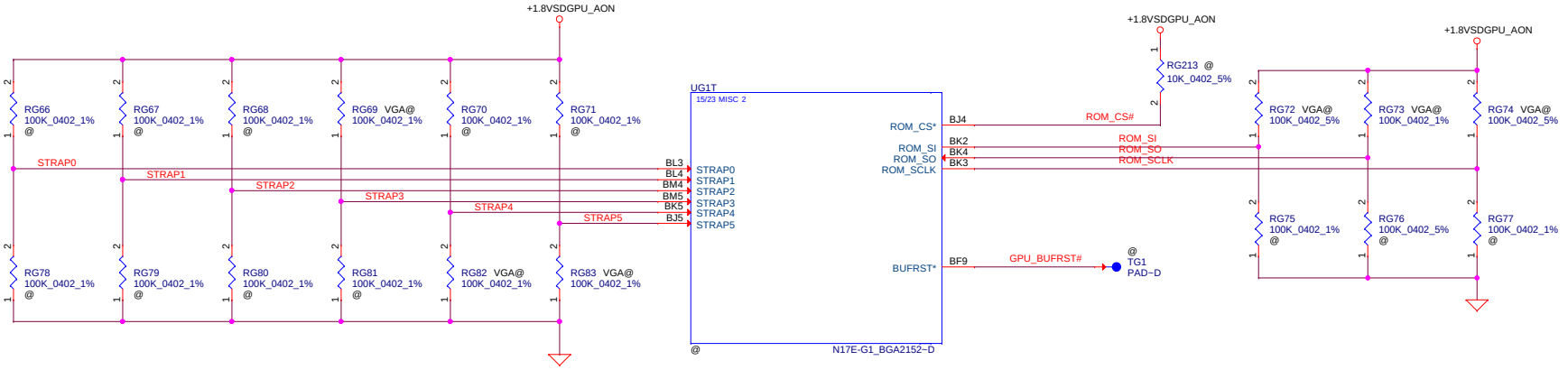


Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready
		1.35V and 1.55V[2]	Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.55V[2]	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	Full	Post production ready

Notes:
1. For N17E-G1, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-G1 runs WCLK up to 3000 MHz with FBVDD = 1.35V. DVS is required to run WCLK > 3000 MHz.

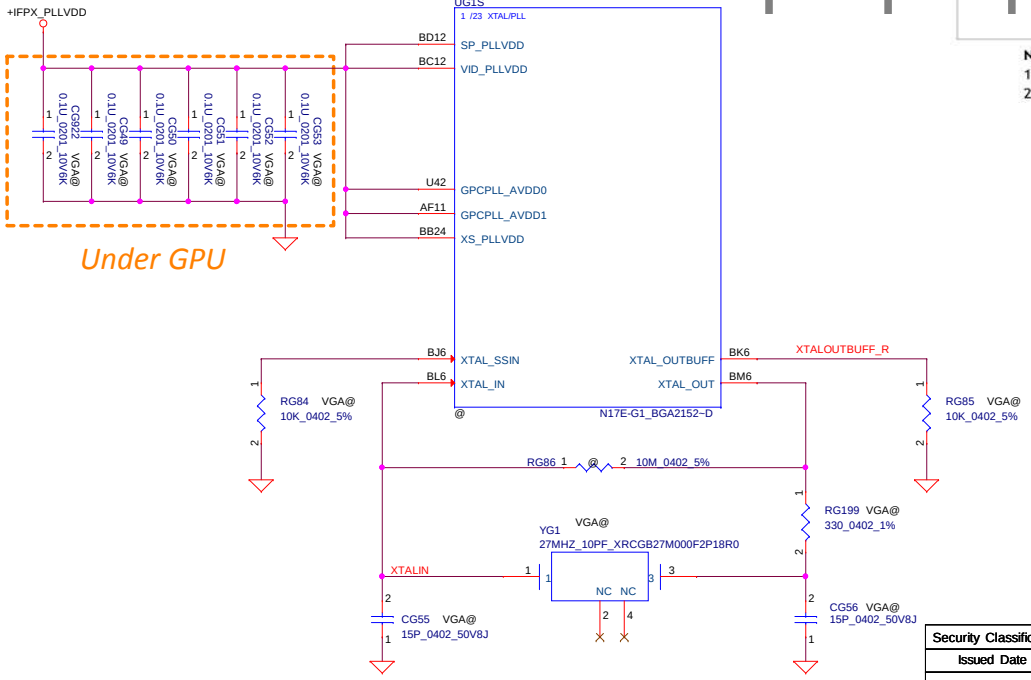


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)

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Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: N17E-G1(6/8) Strap Pin,ROM

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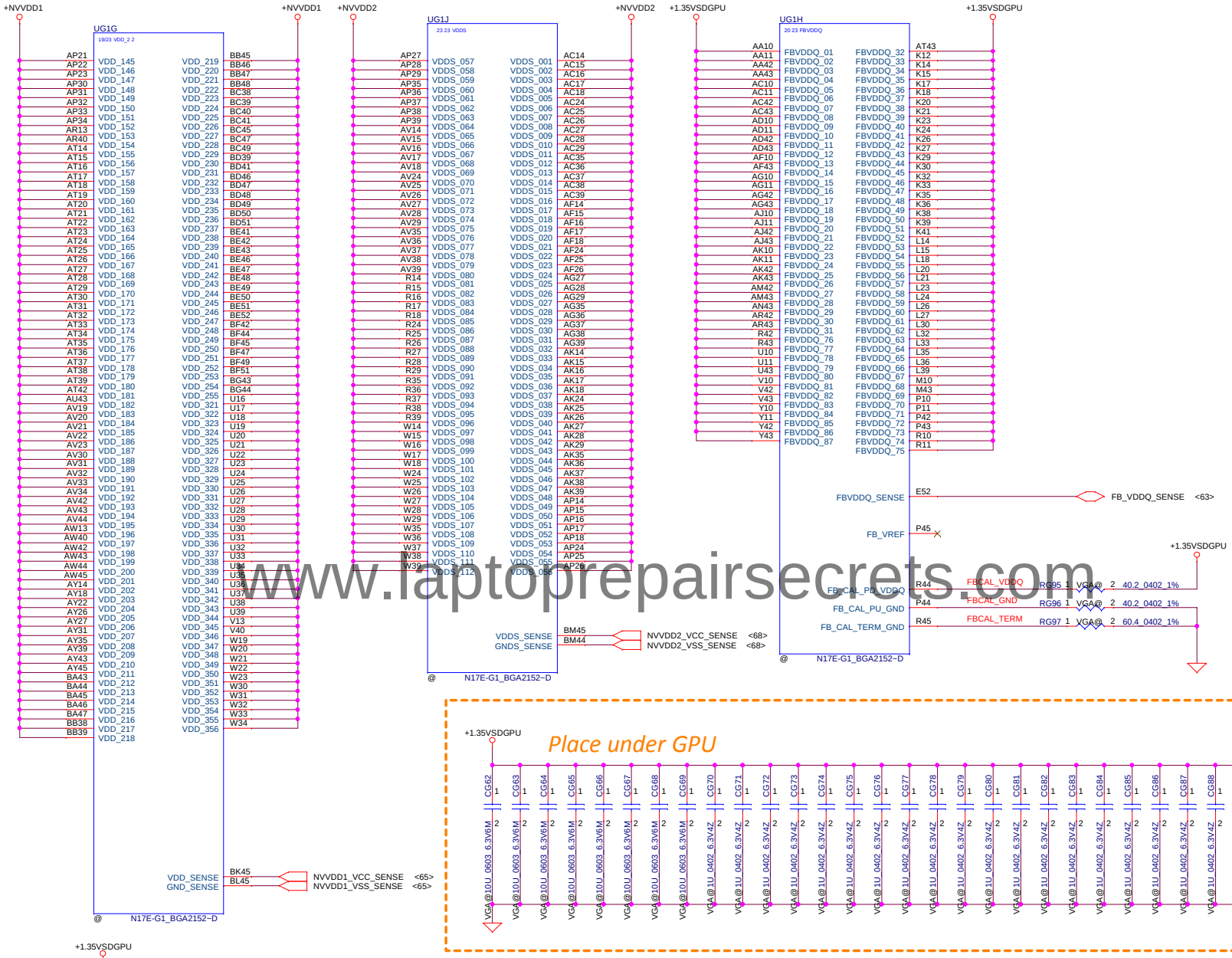

	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ	1	9	13		24	

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(7/8) Power**

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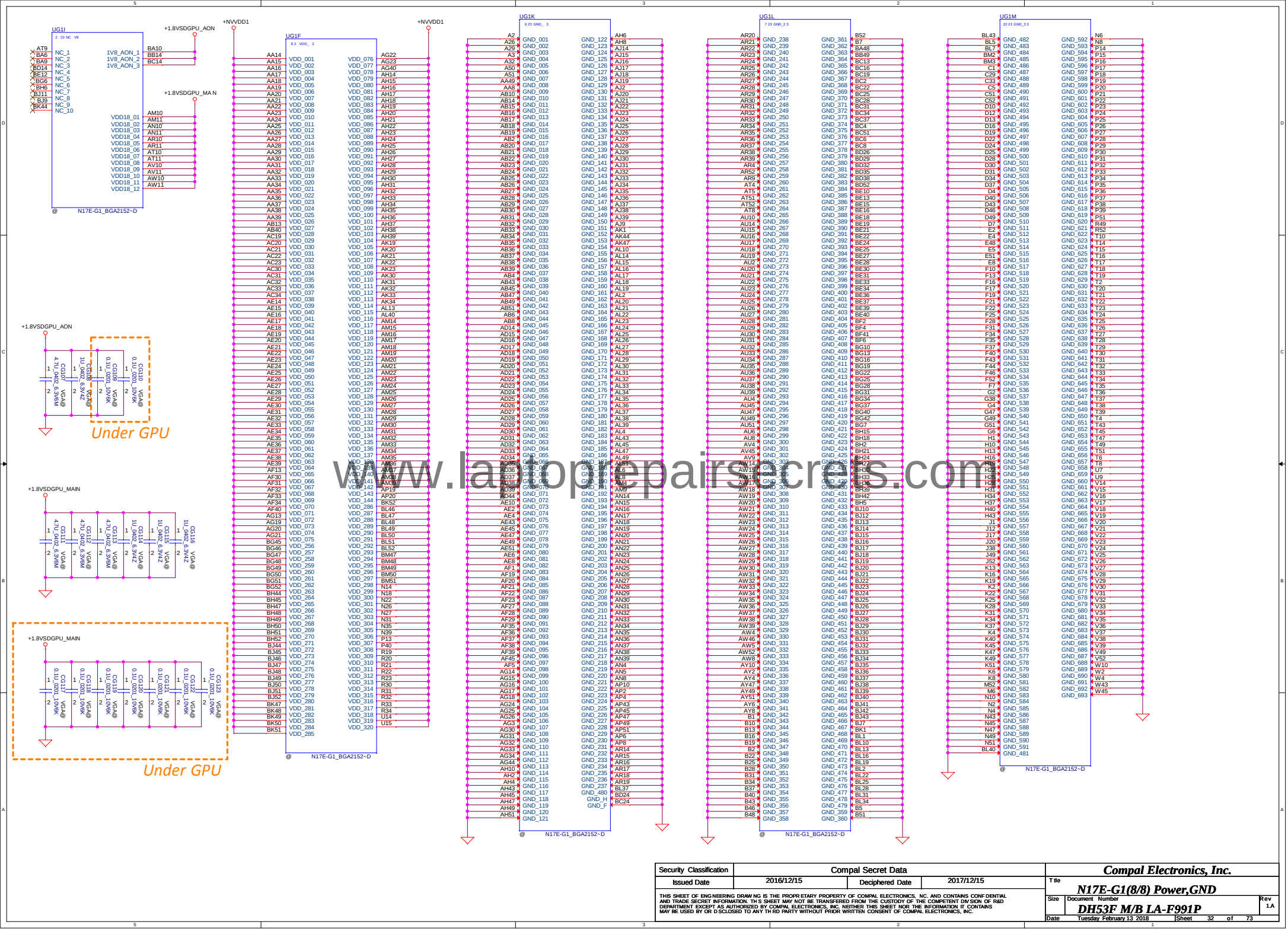

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(8/8) Power,GND**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A

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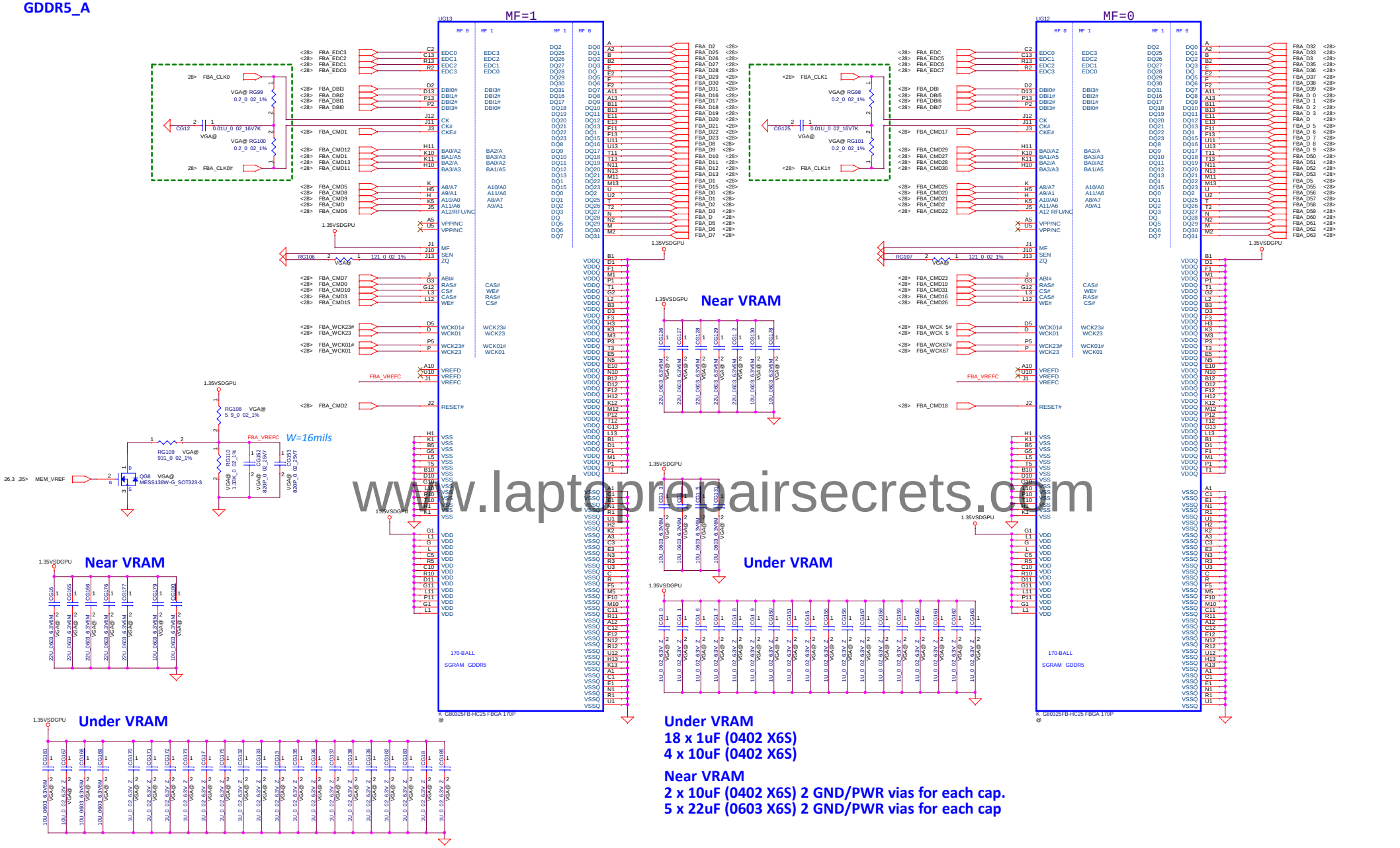
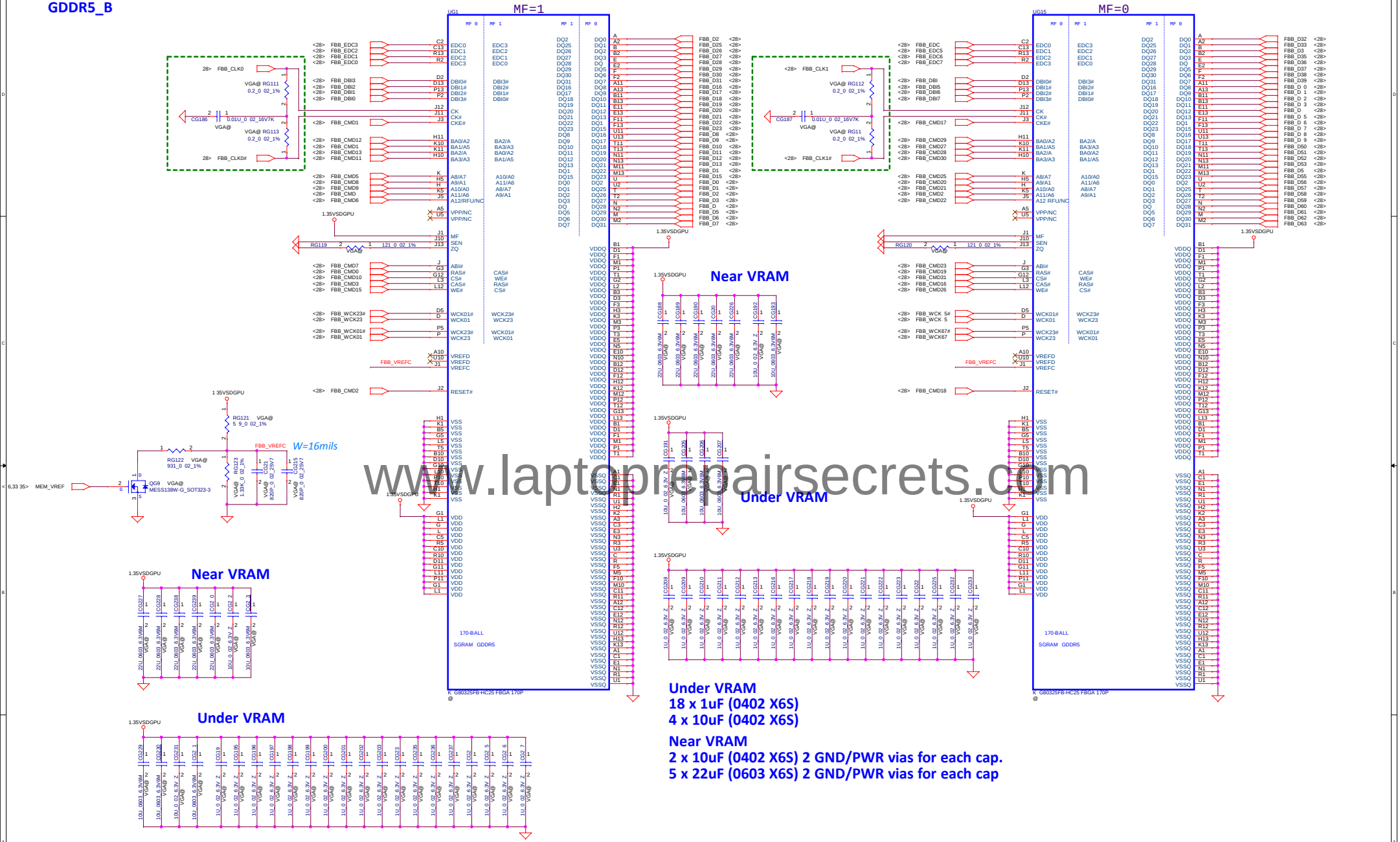
GDDR5_A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/15	Deciphered Date 2017/12/15	Title N17E-GDDR5_A
			Size Document Number DH53F M/B LA-F991P Rev 1A
			Date: Tuesday, Feb uary 13, 2018 Sheet 33 of 73

GDDR5_B



Under VRAM
18 x 1uF (0402 X6S)
4 x 10uF (0402 X6S)

Near VRAM
2 x 10uF (0402 X6S) 2 GND/PWR vias for each cap.
5 x 22uF (0603 X6S) 2 GND/PWR vias for each cap

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Issued Date	2016/12/15	Deciphered Date 2017/12/15	Title N17E-GDDR5 B
			Size Document Number DH53F M/B LA-F991P Rev 1A
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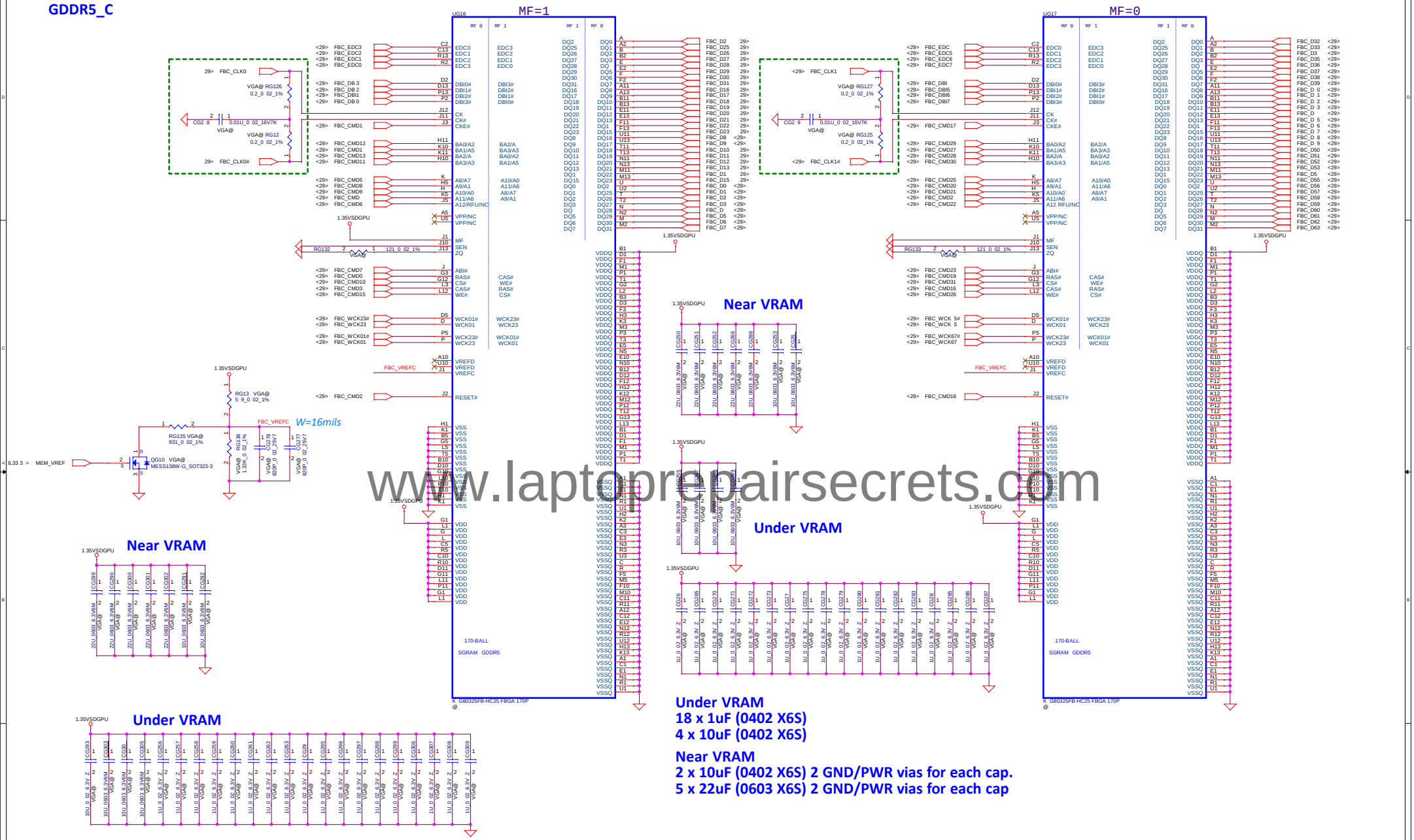
GDDR5_C



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.	
Title	N17E-GDDR5_C
Size	Document Number: DH53F M/B LA-F991P
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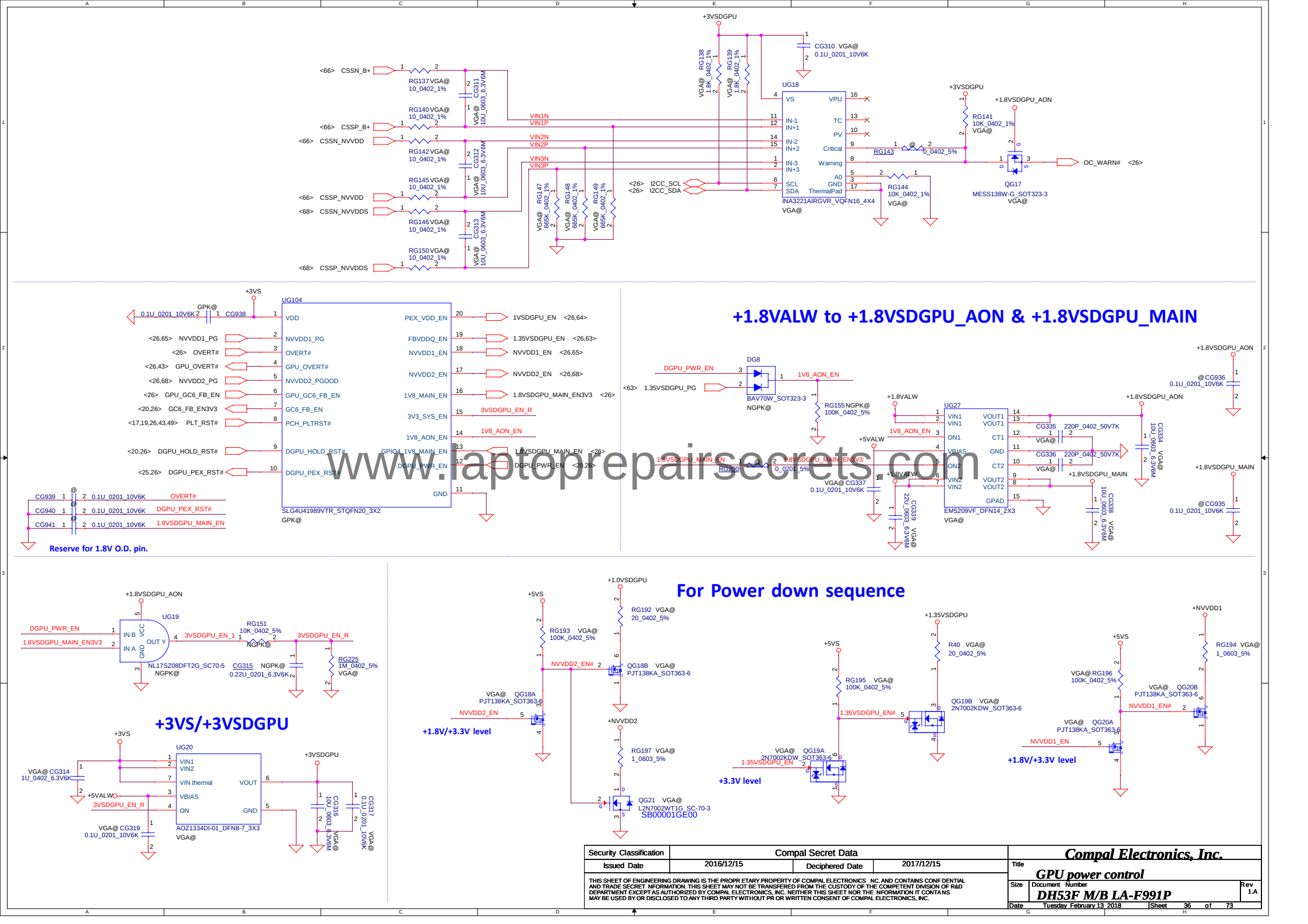

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **GPU power control**

Size: | Document Number: **DH53F M/B LA-F991P** | Rev: 1.A

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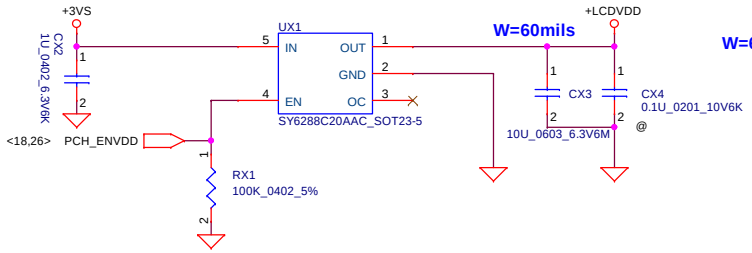
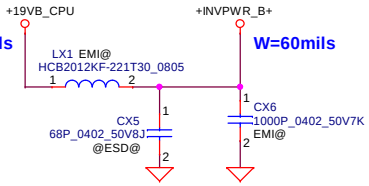
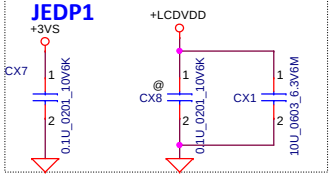
LCD POWER CIRCUIT

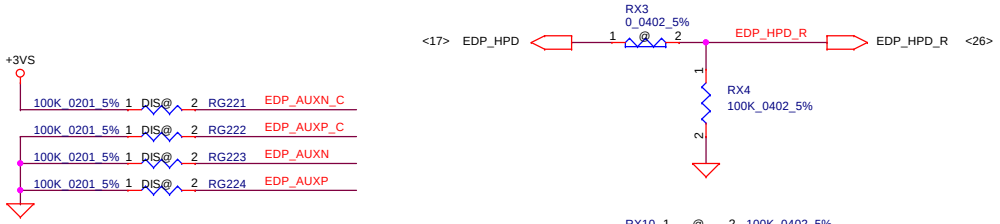


SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

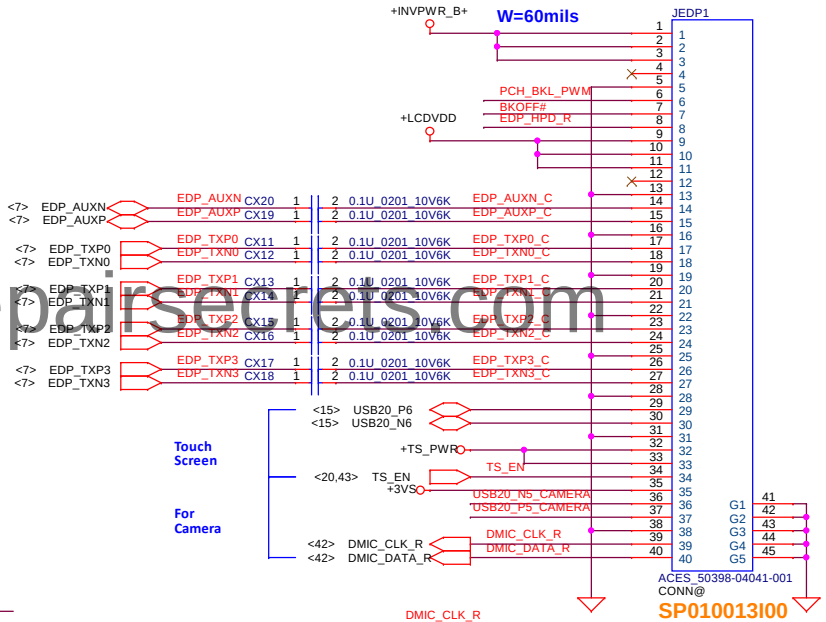


Place closed to JEDP1

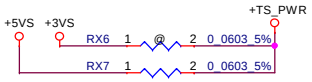




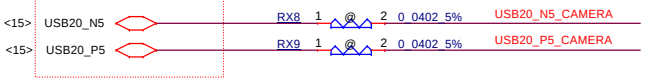
LED PANEL Conn.

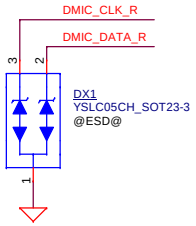


USB Touch Screen



Camera





Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title: eDP CONN.			
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
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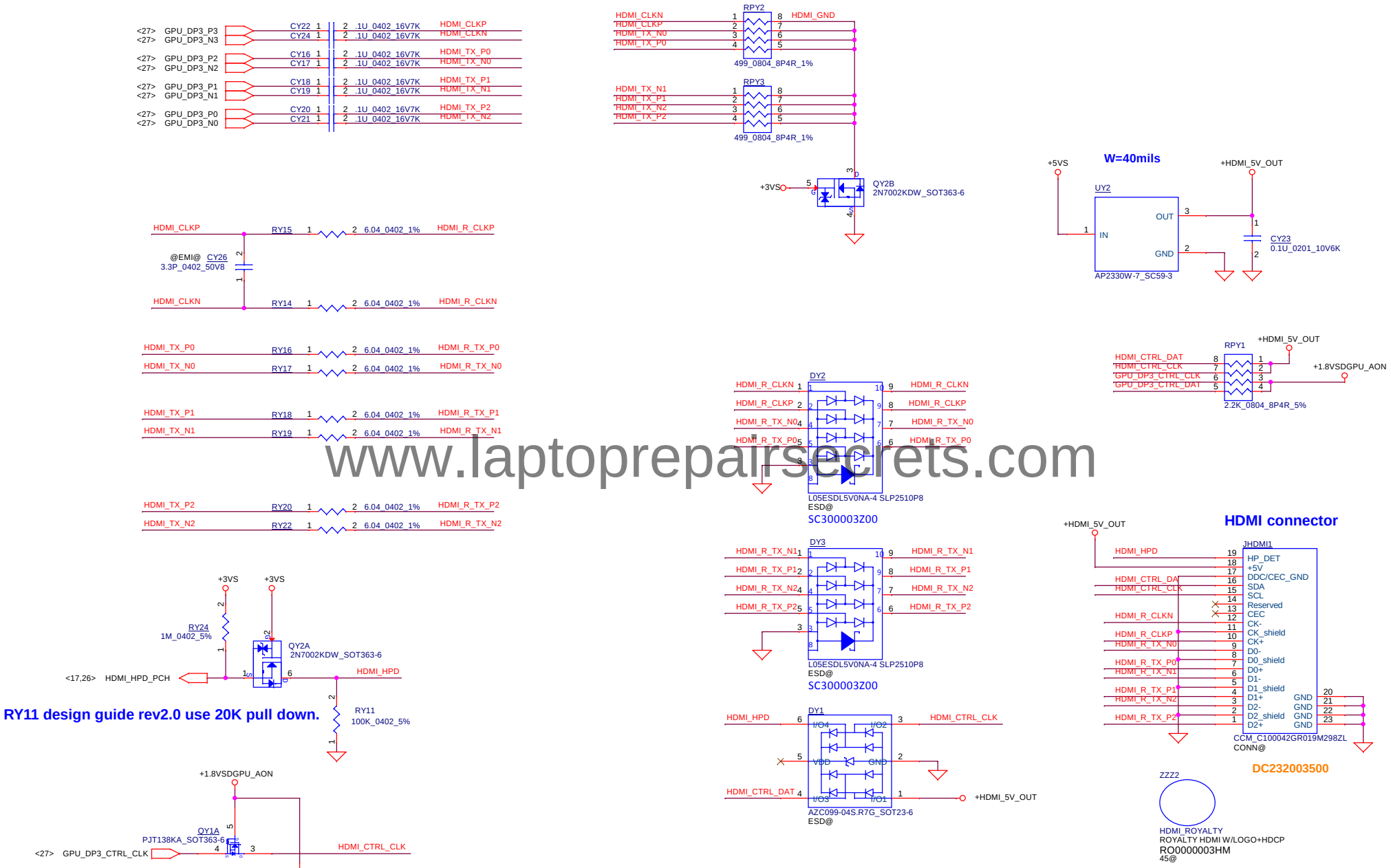

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	HDMI CONN.		
Size	Document Number		Rev
Custom	DH53F M/B LA-F991P		1.A
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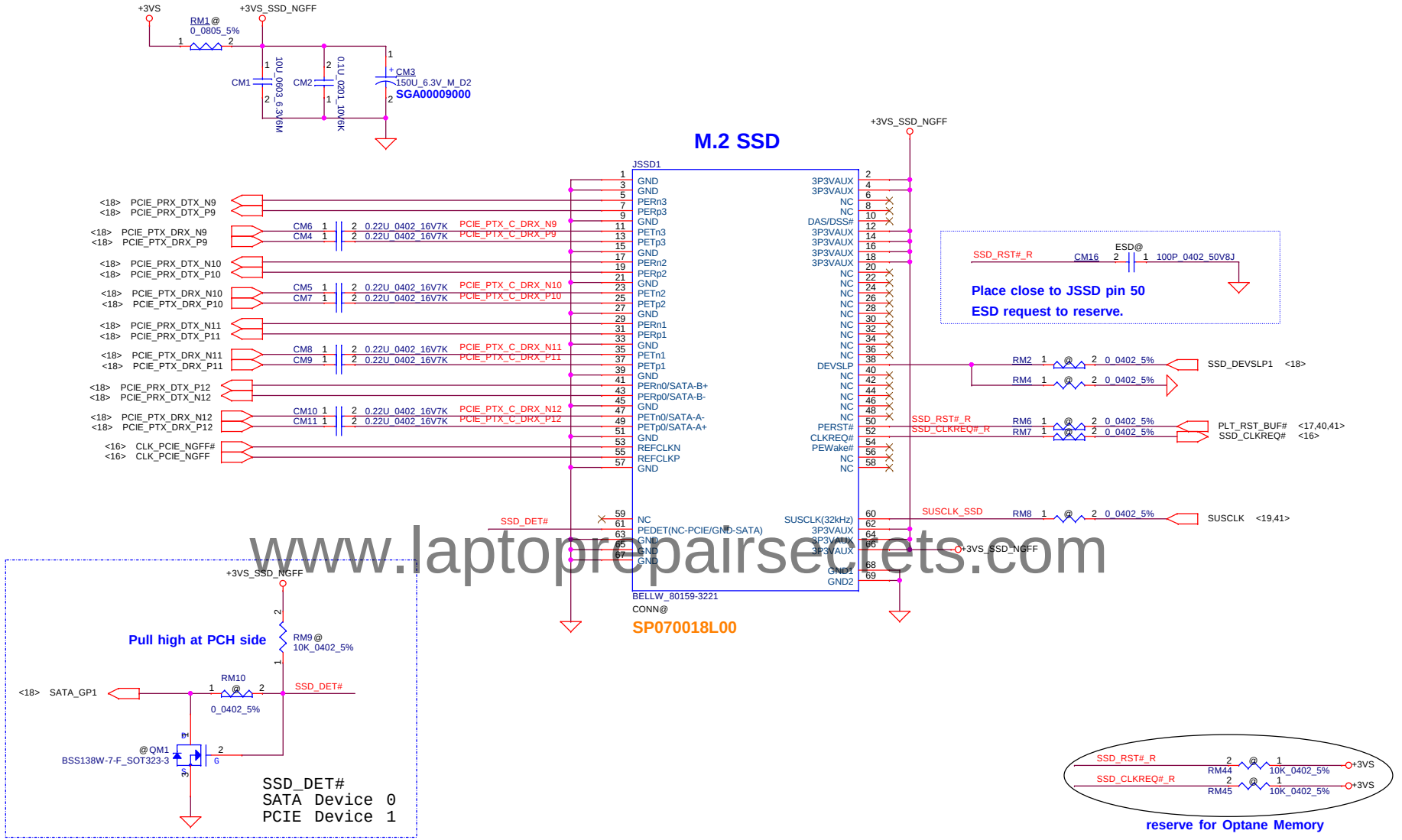

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title: mSATA-SSD			
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
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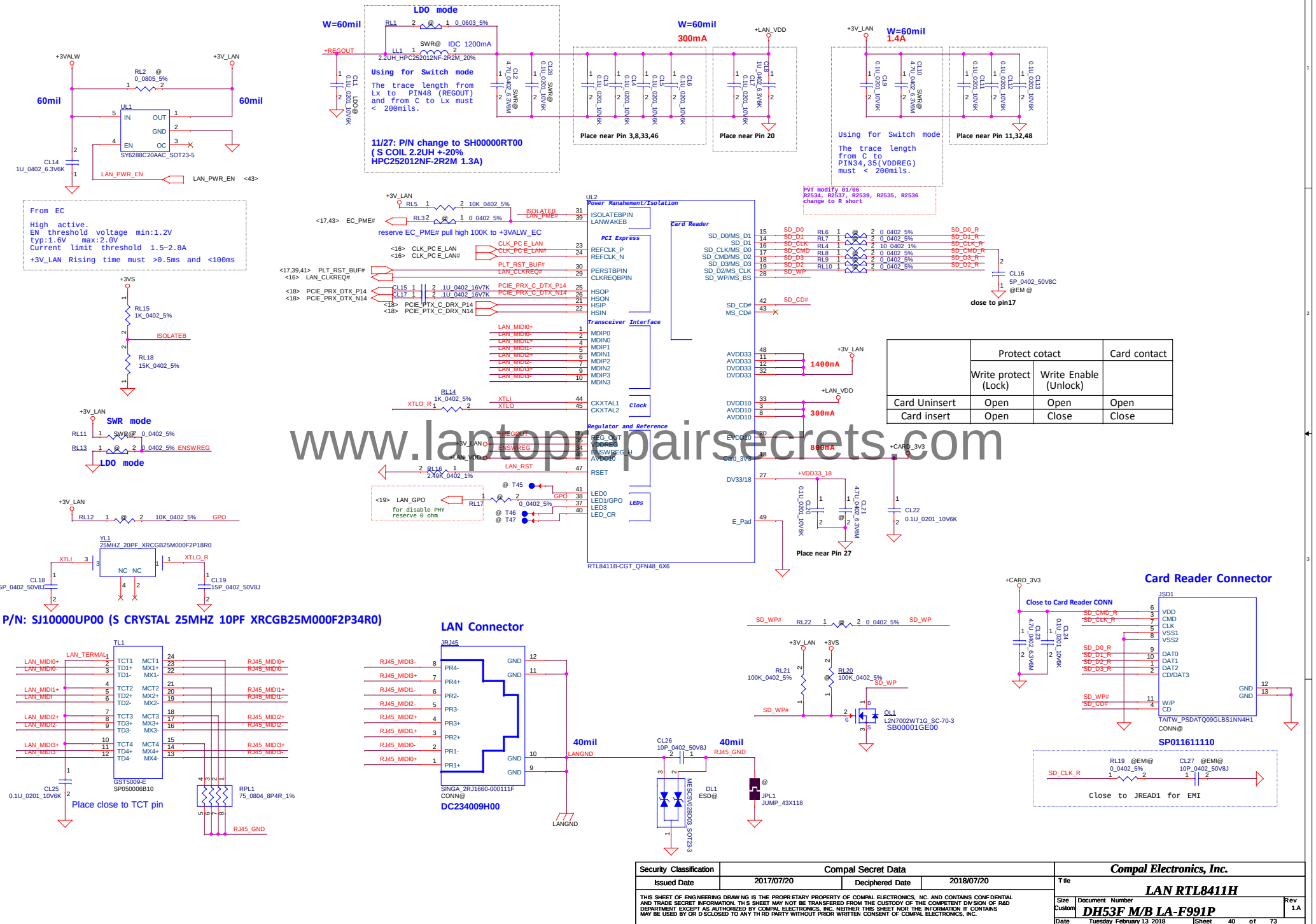
LAN-RTL8411B



	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	LAN RTL8411H		
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
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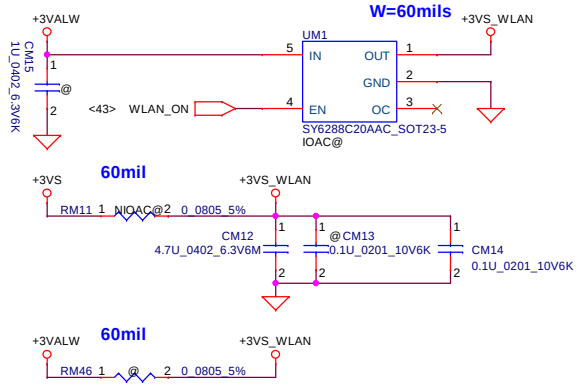
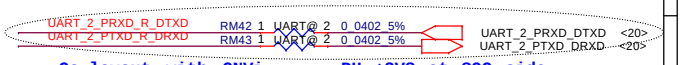
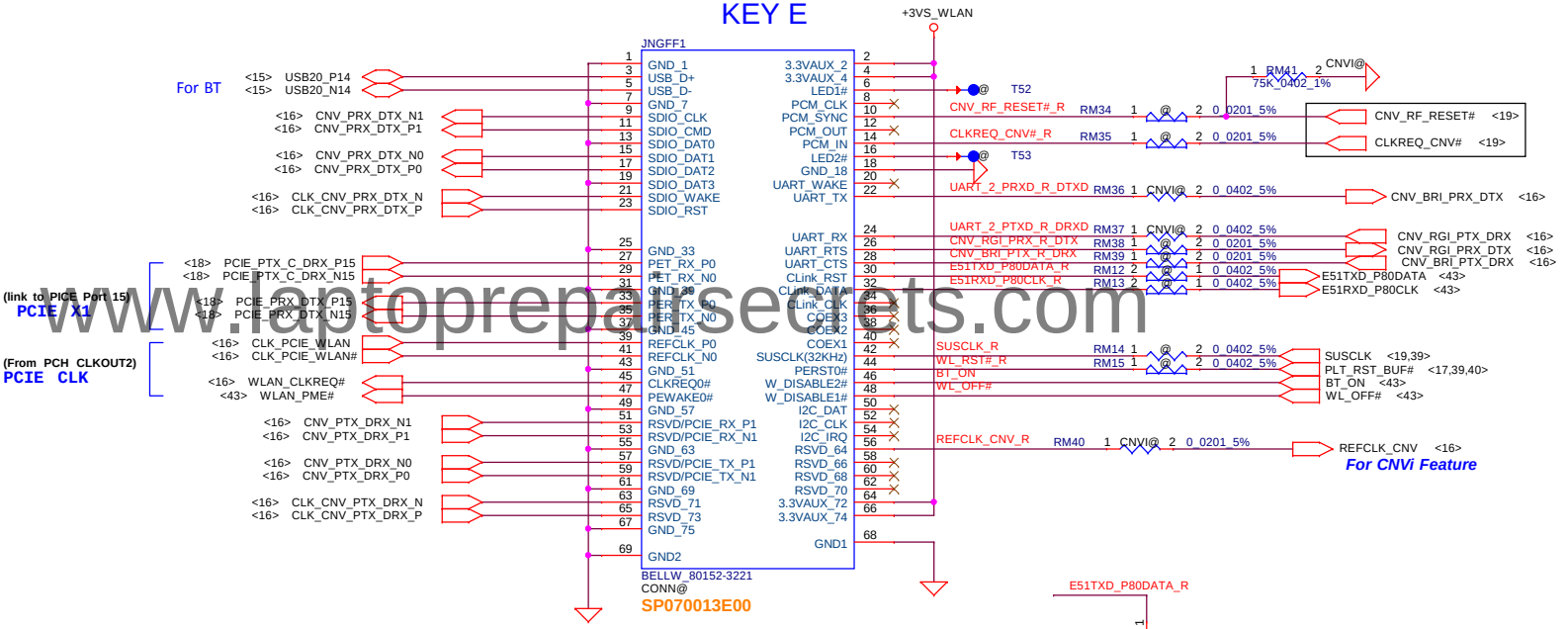
Wireless LAN

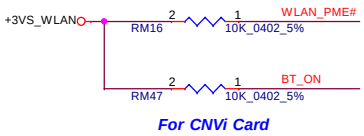


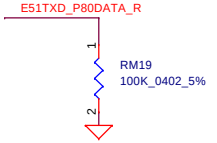


NGFF WL+BT (KEY E)

KEY E







Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: **M.2 Key E (WLAN)**

Size: Custom | Document Number: **DH53F M/B LA-F991P** | Rev: 1.A

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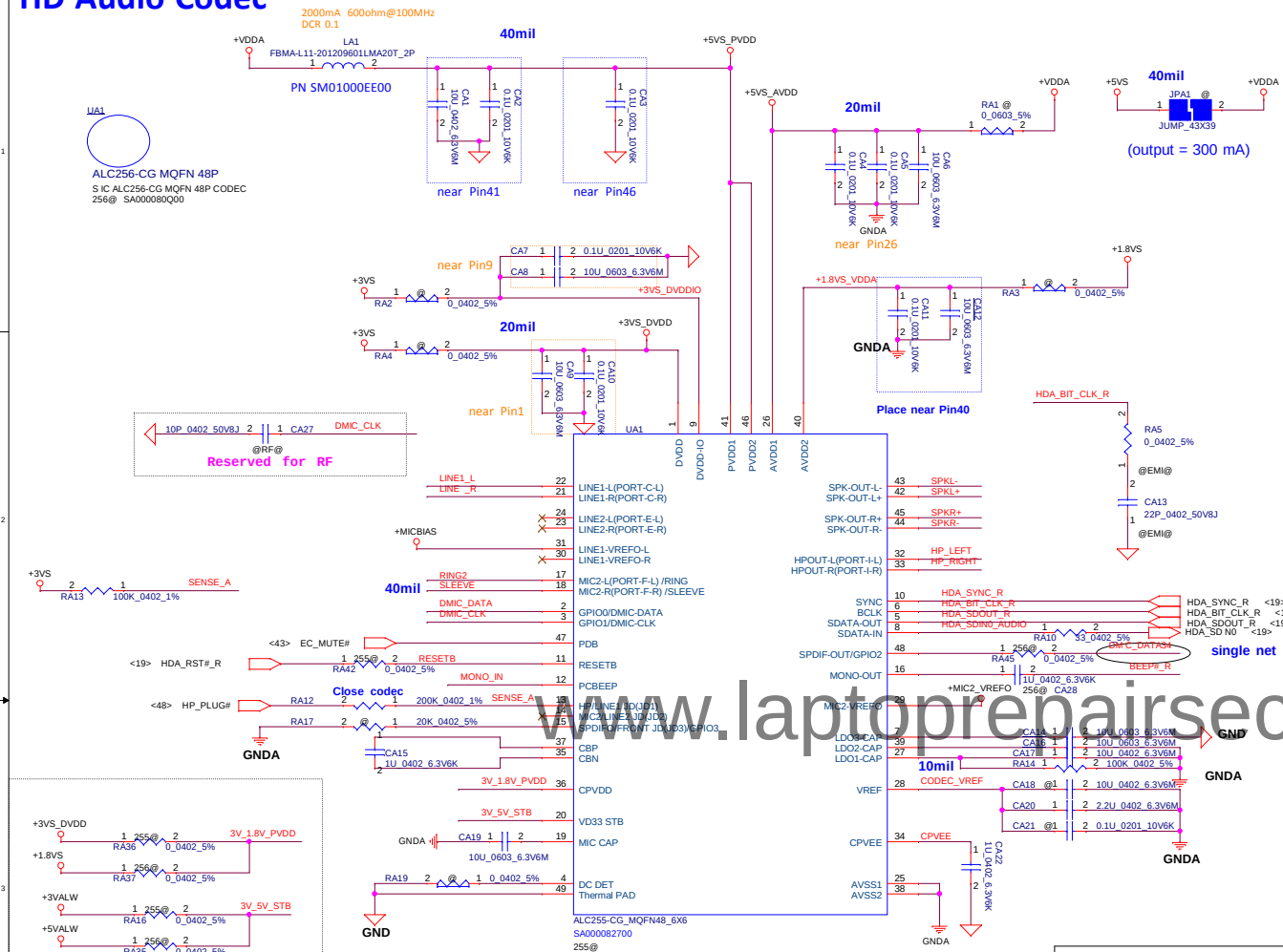
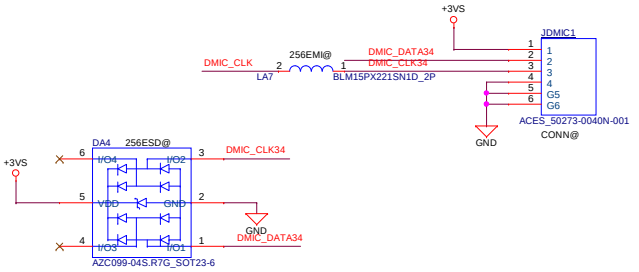
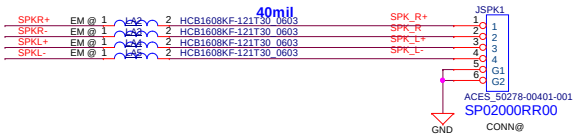
HD Audio Codec



DMIC3/4 Conn. (support on 256)

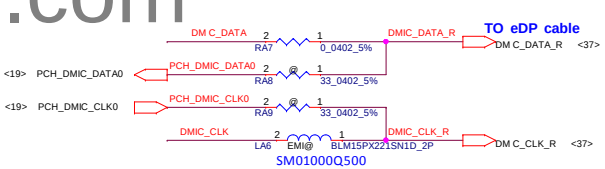


Int. Speaker Conn.

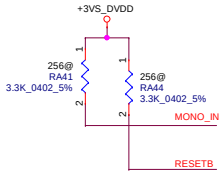


Digital MIC

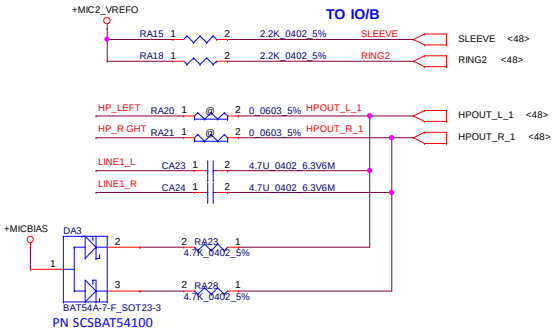
MIC BOM upload by Audio Team

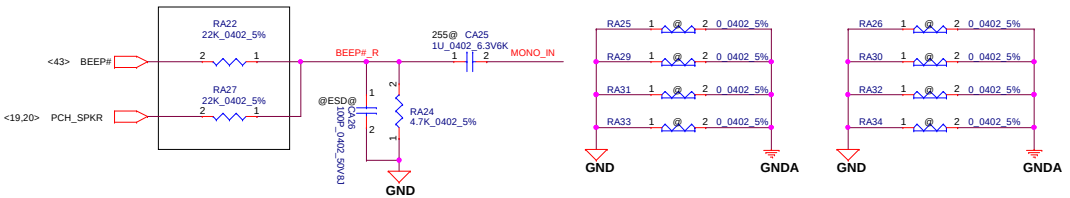


I2C for Co-lay ALC256



Headphone Out





Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	HD Audio Codec ALC255		
Size	Document Number		Rev
Custom	DH53F M/B LA-F991P		1.A
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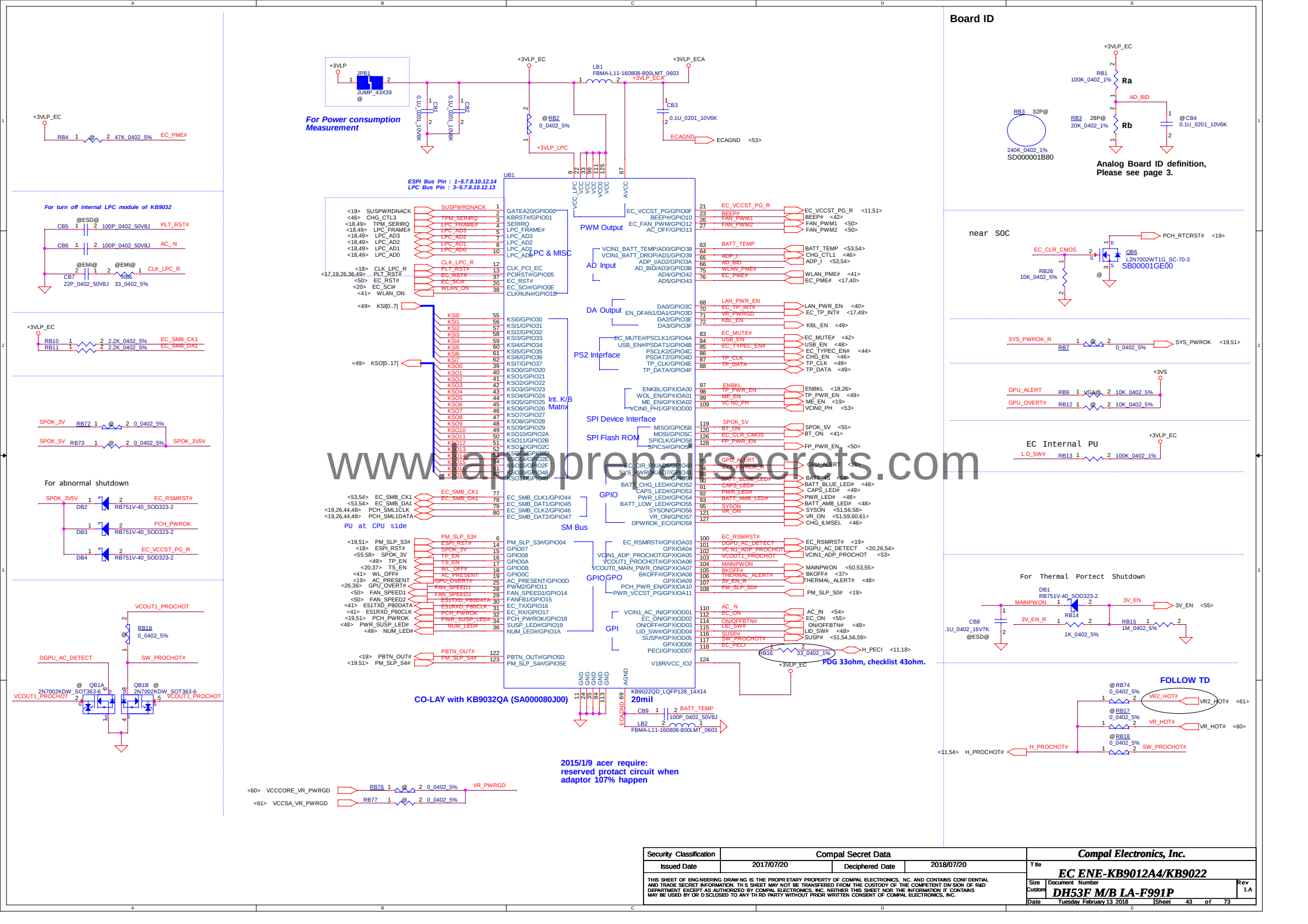

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title	EC ENE-KB9012A4/KB9022		
Size	Document Number		Rev
Custom	DH53F M/B LA-F991P		1.A
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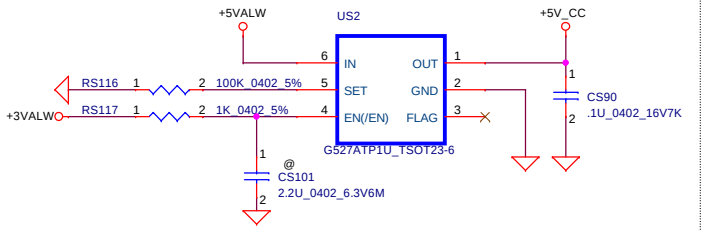
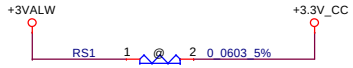
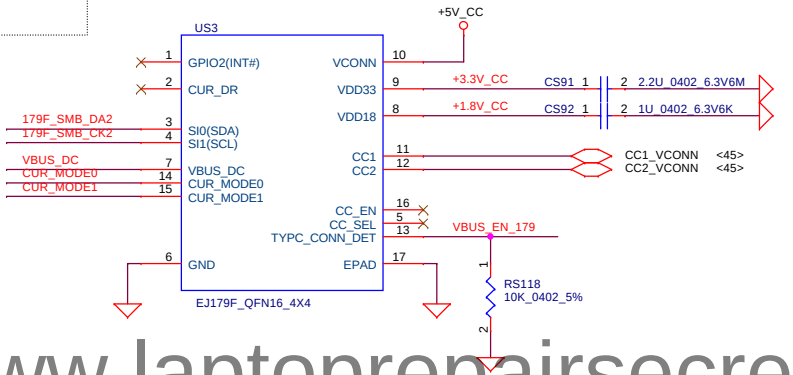
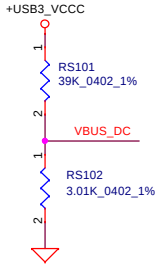






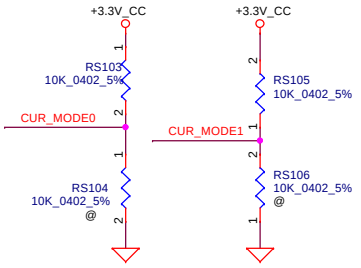


Scaled input
for detection of VBUS DC levels

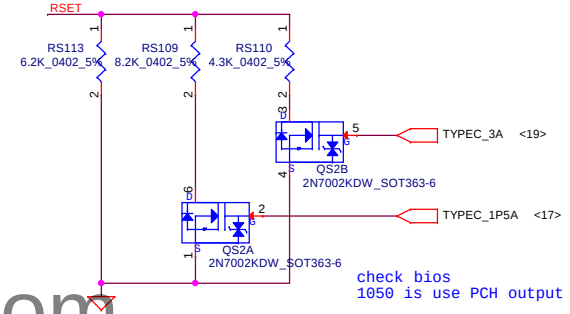
Remove INT#,
platform doesn't monitor it

CC_SEL
report CC1 or CC2 is connection

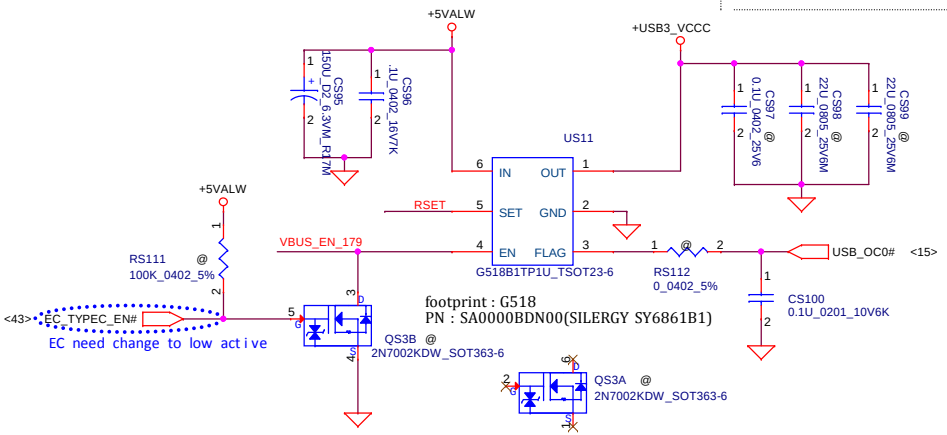
CC_EN
power path control "low active"



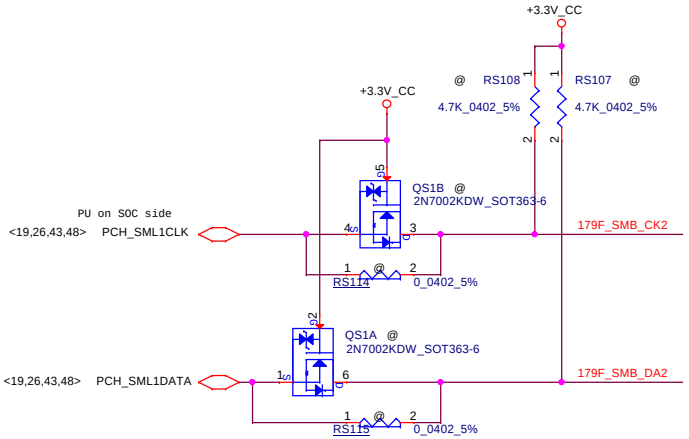
Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

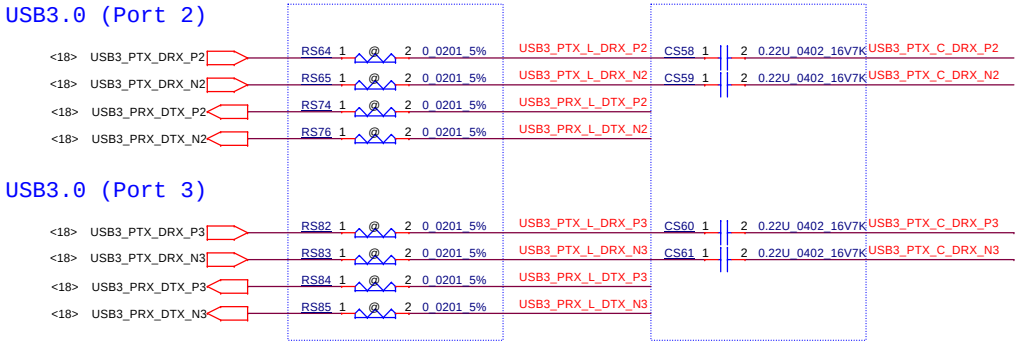


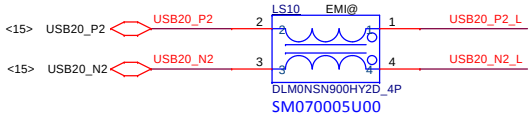
Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

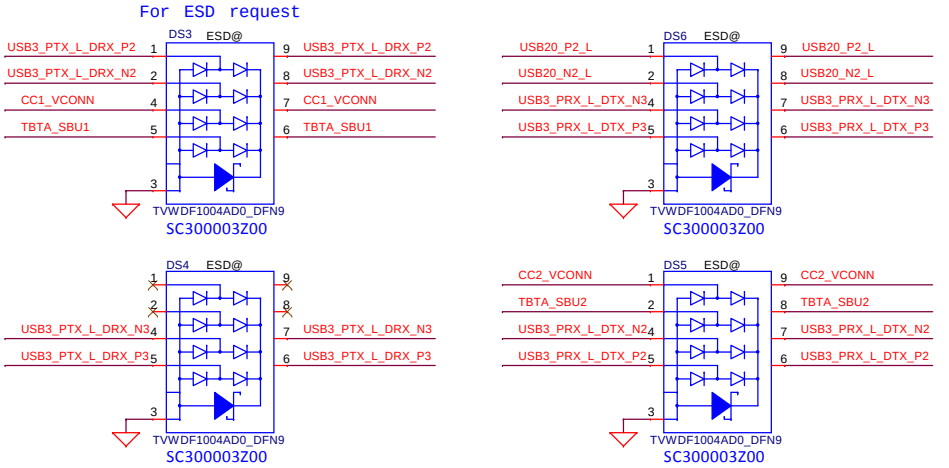


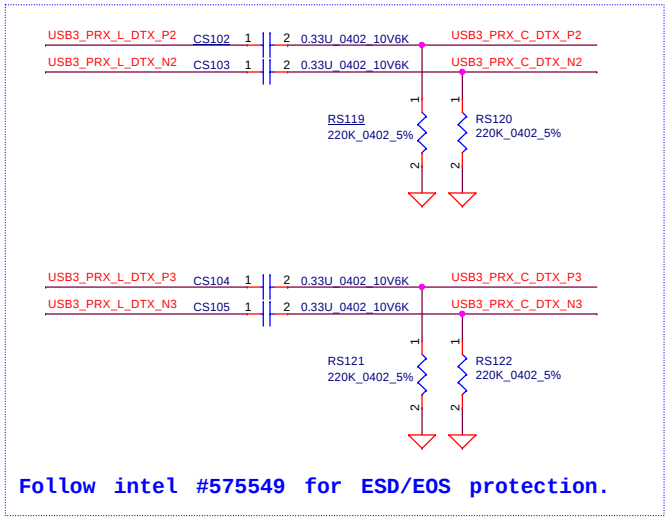
Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

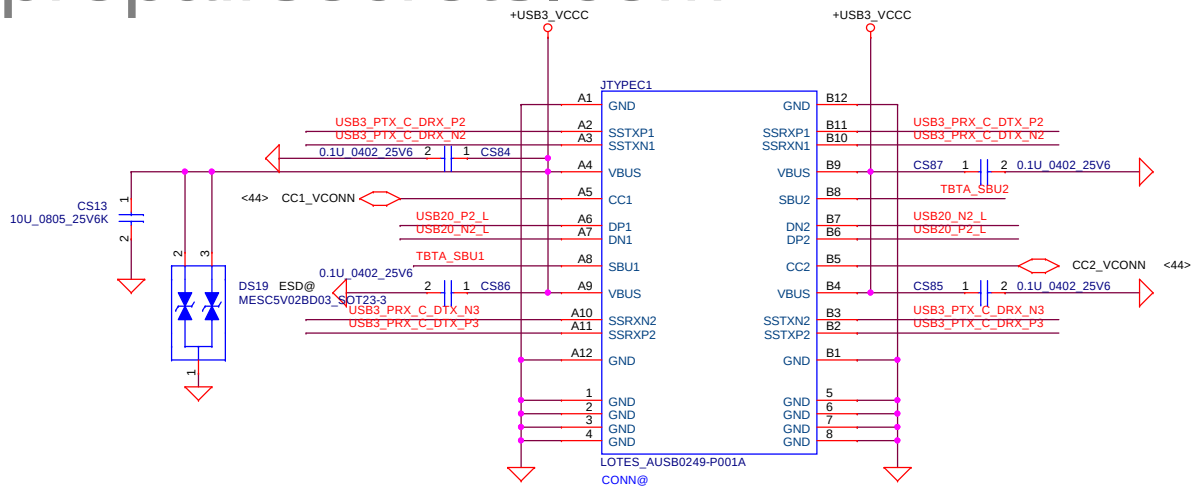
Compal Electronics, Inc.			
Title	CC+USB TYPE C		
Size Custom	Document Number DH53F M/B LA-F991P		Rev 1.A
Date Tuesday, February 13, 2018	Sheet 44 of 73		











CC1_VCONN & CC2_VCONN need 20mil trace width.

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: CC+USB TYPE C

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

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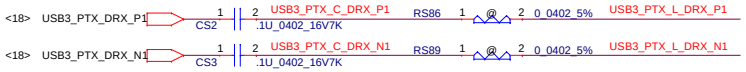
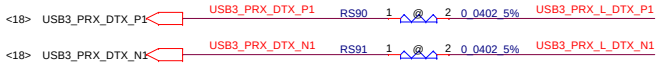
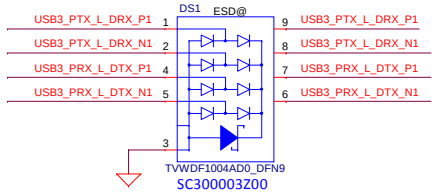
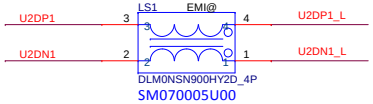
USB3.0

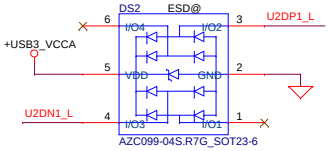




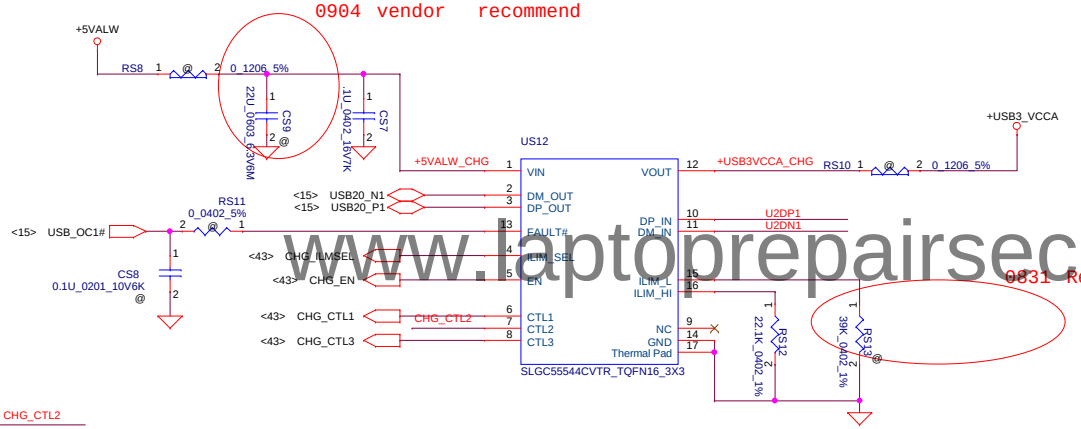
For ESD request



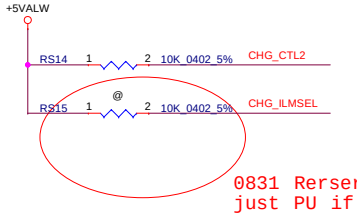




0904 vendor recommend

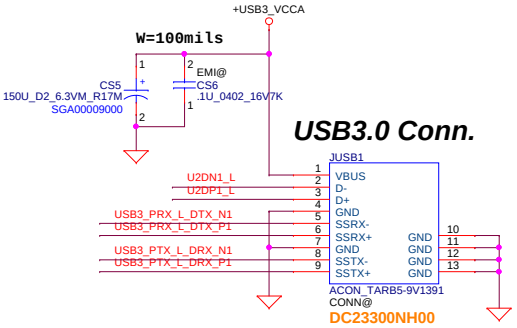


0831 Reserve ILIM_L R as vendor recommend



0831 Rerserve PU, check if SDP1 mode is need, just PU if no need

ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA(reserve)



USB Host Charger

CTL1	CTL2	CTL3	ILIM SEL	MODE	Current Limit Setting	Note
1	1	0	1	SDP1	ILIM H	Data Lines Connected
1	1	1	0	SDP2	ILIM L	Data Lines Connected
1	1	1	1	CDP	ILIM H	Data Lines Connected
0	1	1	1	DCP Auto	ILIM H	Data Lines Disconnected

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.

Title: USB3.0 Conn/USB Charger

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

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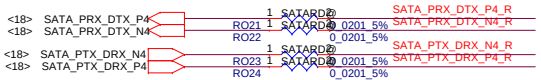
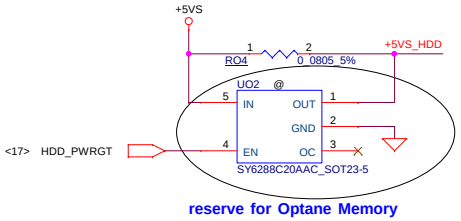
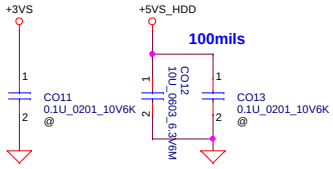
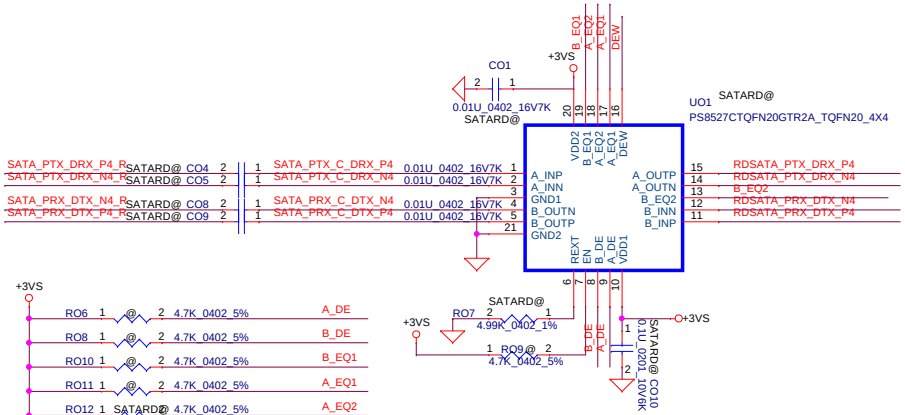
SATA Re-Driver and cable HDD Conn.



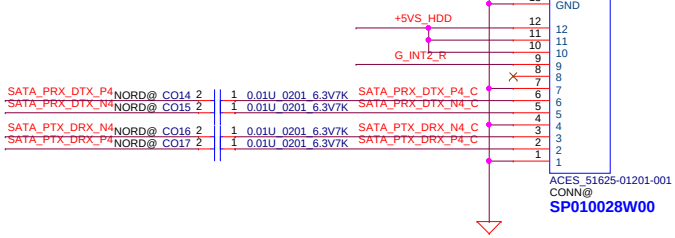


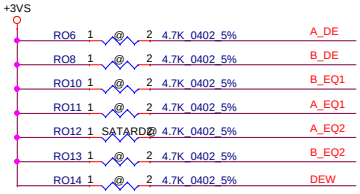
reserve for Optane Memory

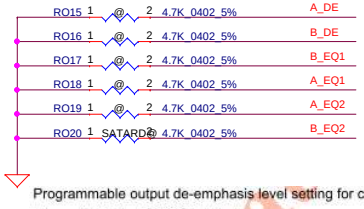




USE 8527 re-driver
SA00007JU10







Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

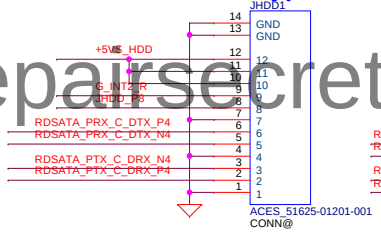
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

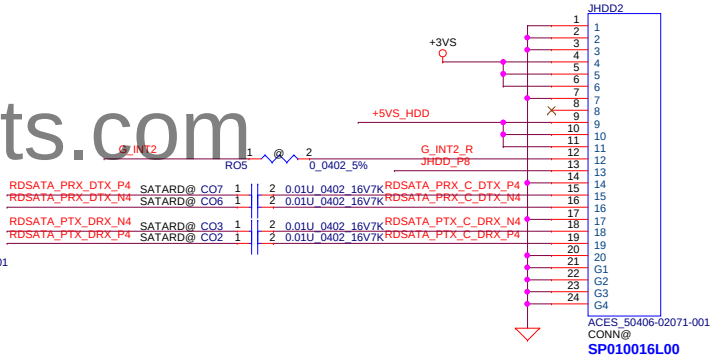
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

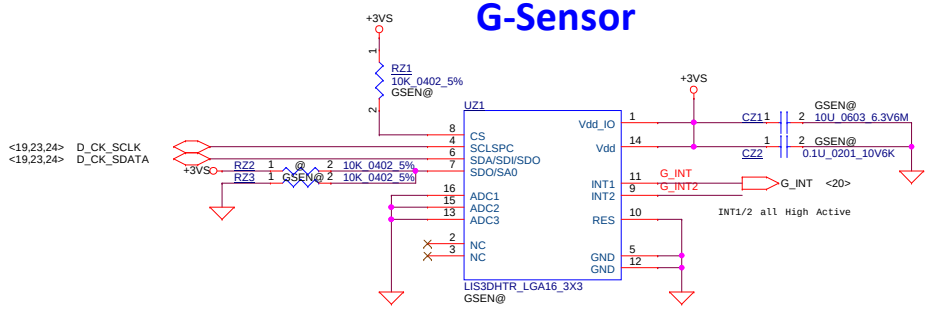
FFC Type



Cable Type



G-Sensor



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

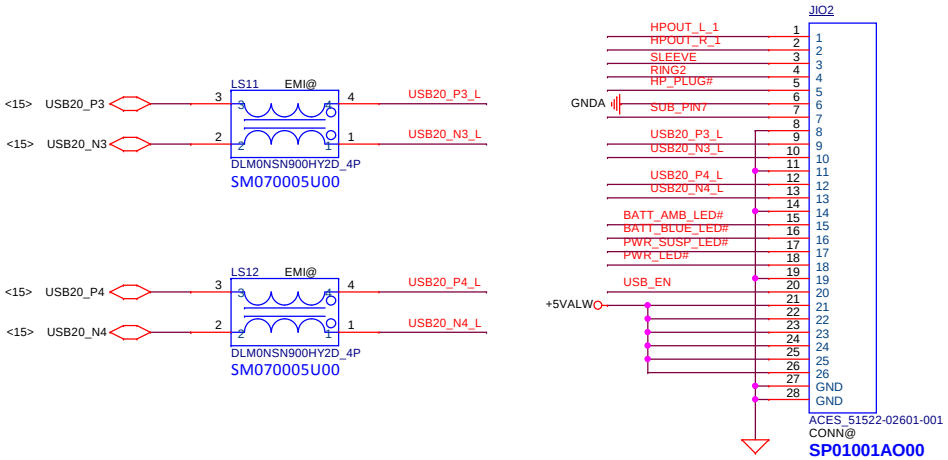
Compal Electronics, Inc.

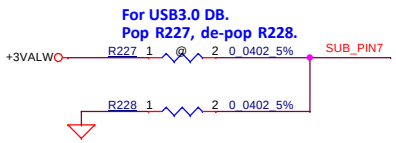
Title: HDD/ Re-Driver/ G-sensor

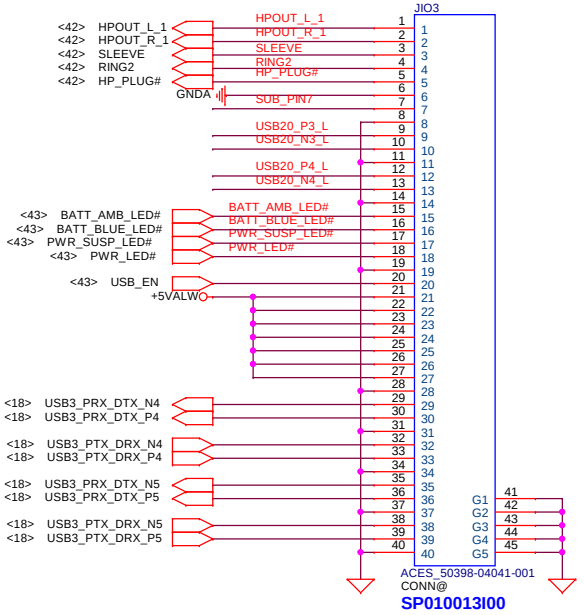
Size	Document Number	Rev
Custom	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 47 of 73

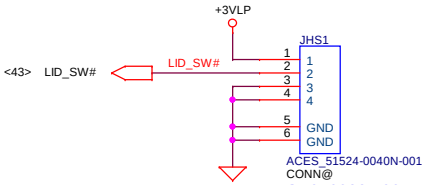
To USB/B FPC BTB CONN

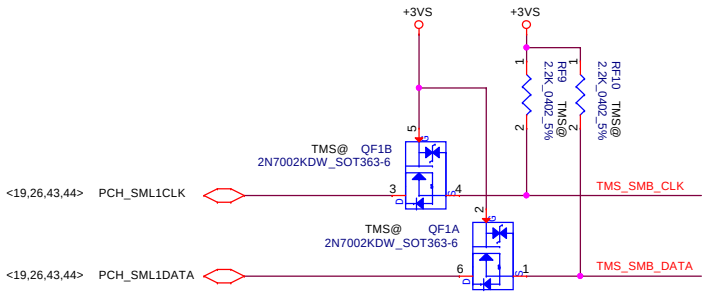




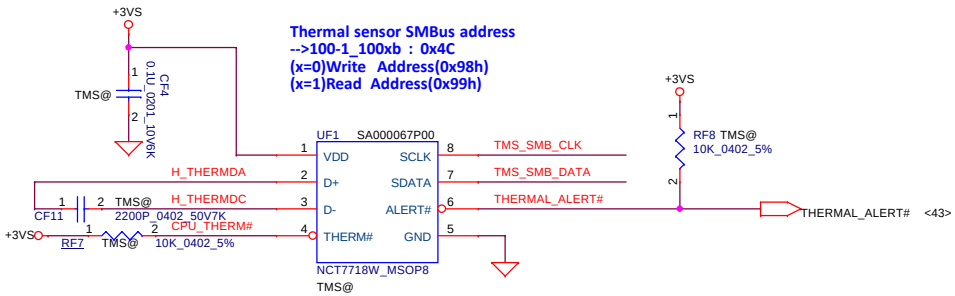


To Hall sensor/B





THERMAL SENSOR



Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title: FUN/B & LED/B			
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
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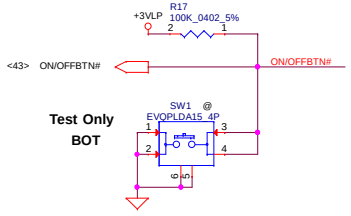
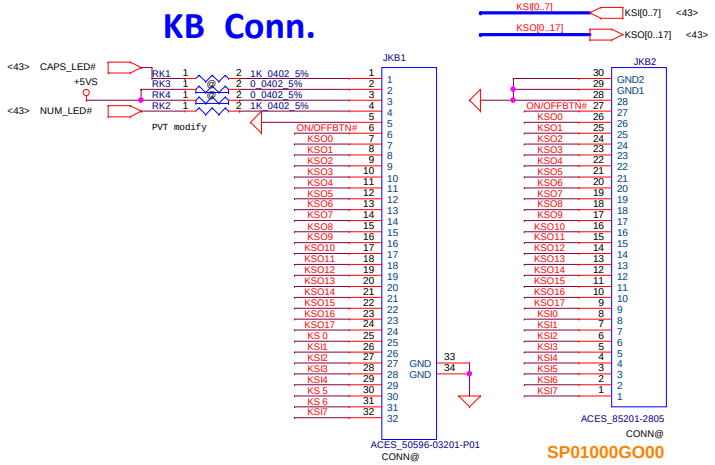
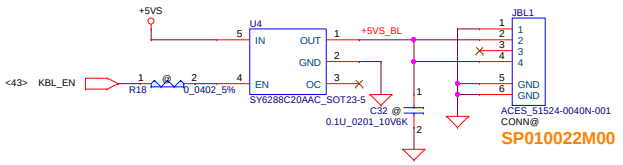
ON/OFF BTN



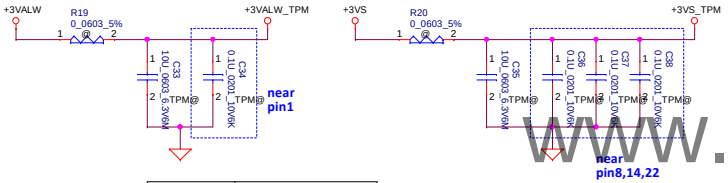
KB Conn.



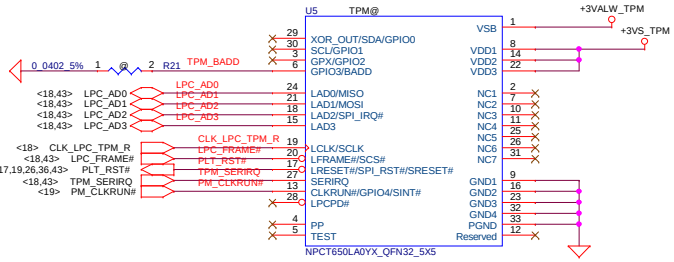
KB BackLight



TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)



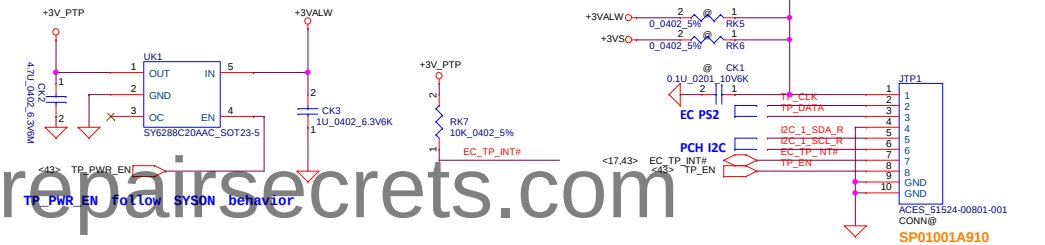
SERIRQ PH 10K to +3VS at PCH side

CLKRUN# PH 10K to +3VS at PCH side

LPCPD# had internal PH

P/N:SA00008ELC0 (S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0)

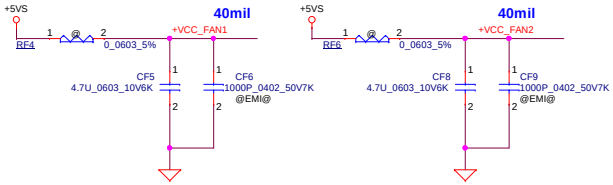
Touch Pad



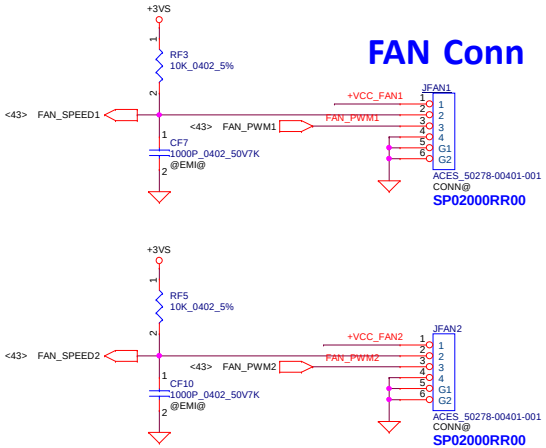
TP_PWR_EN Follow SYSON behavior

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

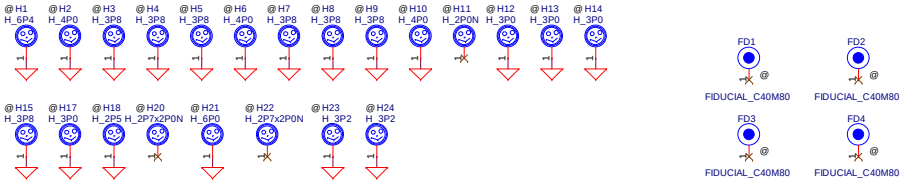
Compal Electronics, Inc.	
Title	KB & TP & TPM Connector
Size / Custom	Document Number: DH53F M/B LA-F991P
Rev	1.A
Date	Tuesday, February 13, 2018
Sheet	49 of 73



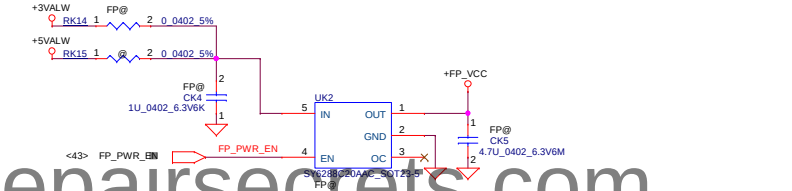
FAN Conn

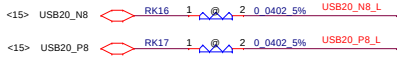


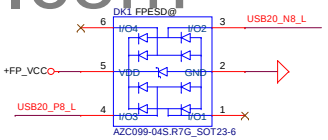
Screw Hole

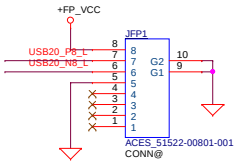


Finger Print







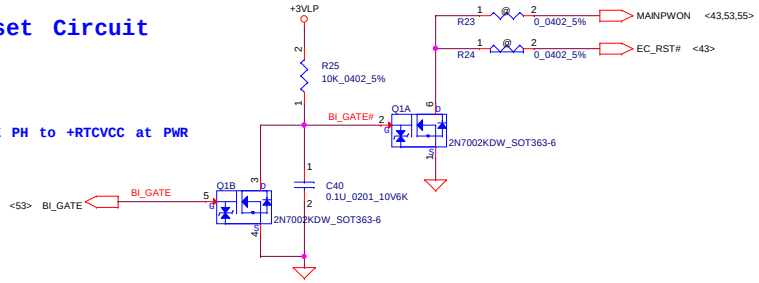


SP01001AE00

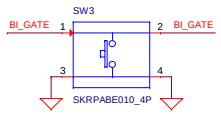
PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Reset Circuit

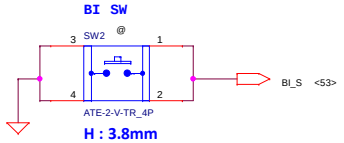
BI_GATE PH to +RTCVCC at PWR side



Reset Button



BI SW



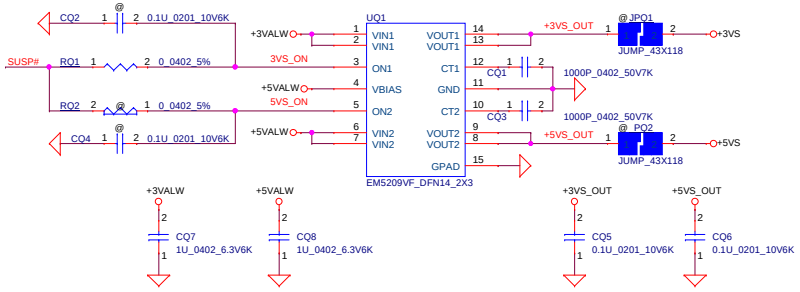
H : 3.8mm
Release : Battery Off
Push : Battery ON

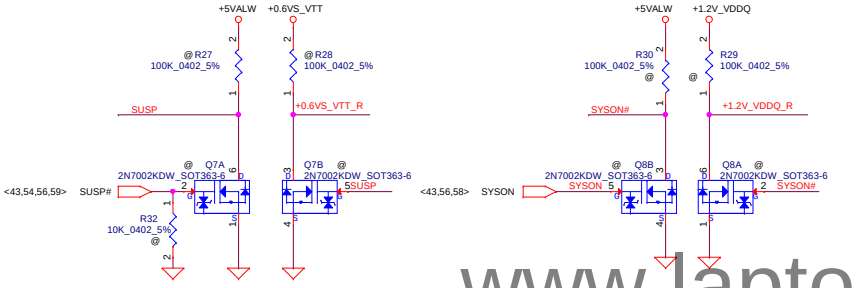
SN10000CV00

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

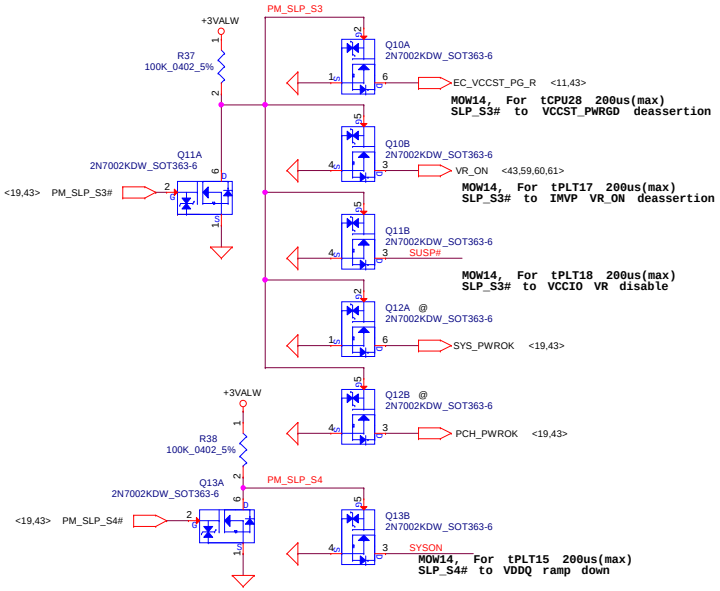
Compal Electronics, Inc.	
Title	FAN & FP & Screw Hole
Size: Custom	Document Number: DH53F M/B LA-F991P
Rev	1.A
Date: Tuesday, February 13, 2018	Sheet 50 of 73

System DC inferface

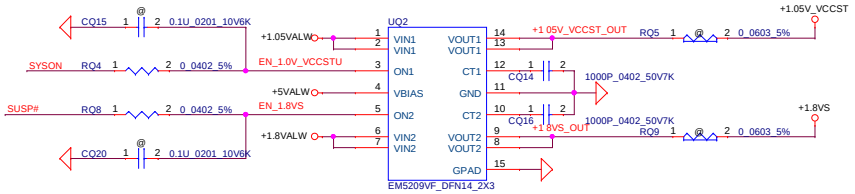




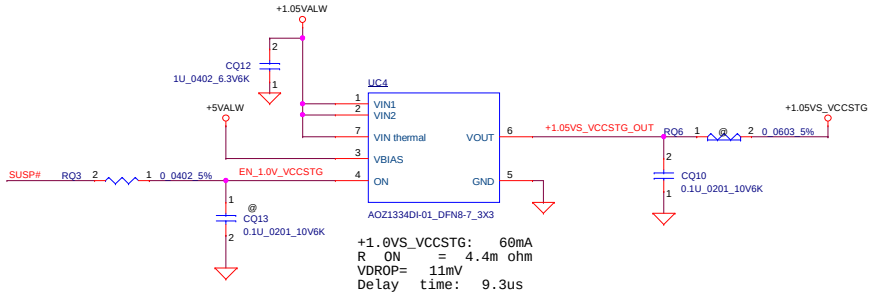
For Power ON/Off Sequence



+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



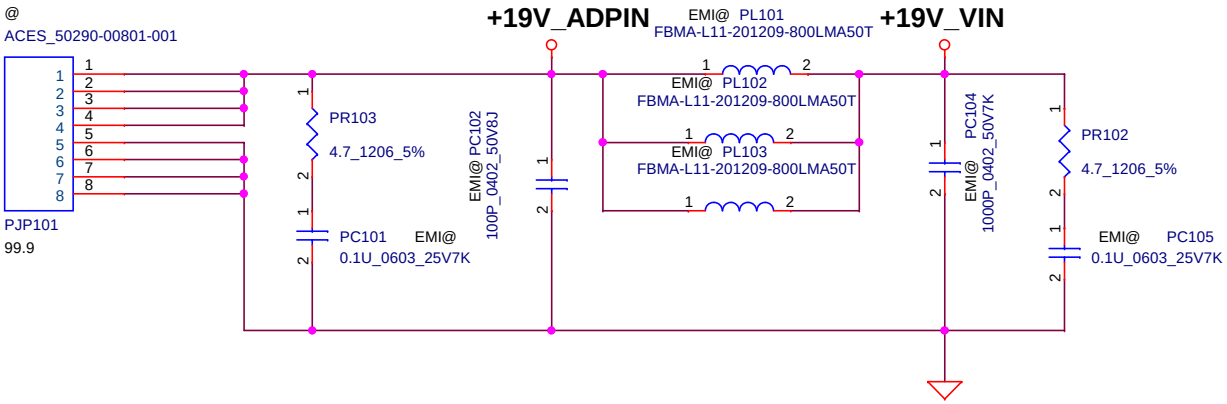
+1.05VALW TO +1.05VS_VCCSTG

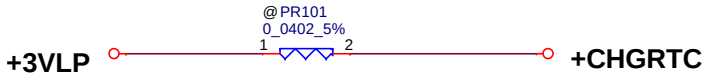


Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
Date: Tuesday, February 13, 2018	Sheet: 51 of 73		

change PL101 PL102 PL103 from M01000P200 to SM01000U600





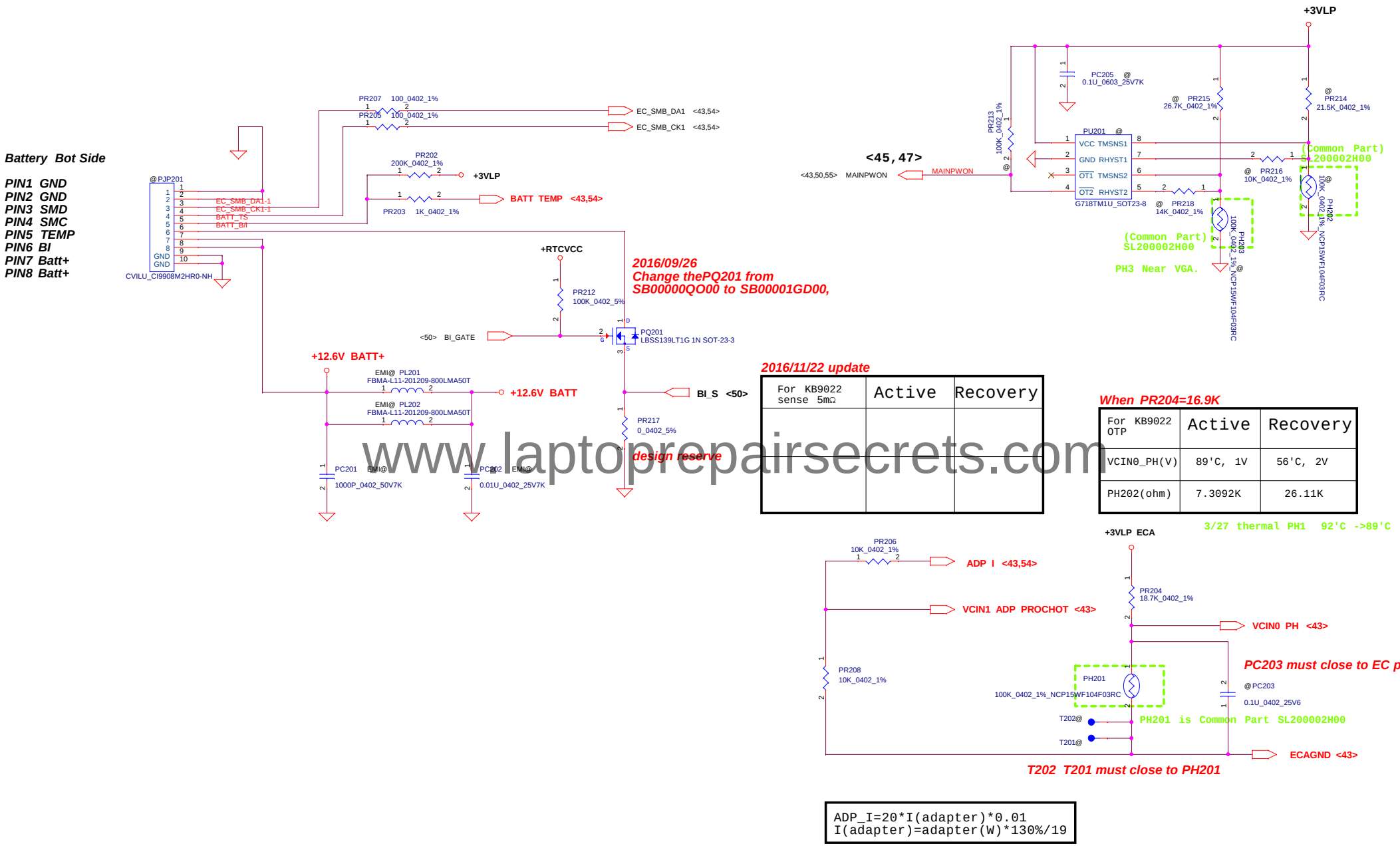
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DCIN

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 52 of 73



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

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Module model information

ISL95520_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 L2N7002WT1G_SC70-3

PR301 1M_0_02_1%

PR302 3M_0_02_5%

Need check the SOA for inrush

+19V_VIN

PQ310 TPCA8057-1N_DFN5X6-8

+19V_P1

PQ311 AON7380_DFN3X3-8-5

+19V_P2

PR339 @ 0.01_1206_1%

PR303 0.005_1206_1%

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

+19VB

EMI@ PL70 FBMA-L11-201209-800LMA50T

Isat: 10A
DCR: 14mohm

@PJP1 JUMP_3X118

Co-lay jump and ISN choke.

+19VB_CHG

PC302 10U_0805_25V6K

PC303 10U_0805_25V6K

PC305 0.1U_0_02_25V6

PC308 220P_0_02_25V7K

PC321 0.1U_0_02_25V6

@PC322 1000P_0_02_25V

PR306 99K_0_02_1%

PR307 .02K_0_02_1%

PR308 .02K_0_02_1%

PR310 66.5K_0_02_1%

PC301 220P_0_02_50V7K

L >H
2.04 vin min w/o 2M =17.41

H >L
2.02 vin min w 2M =17.77

PR30 0_0_02_5%

PR305 2_0_02_5%

PC306 0.1U_0_02_25V6

PR309 100_0_02_1%

+12.6V_BATT

PQ312 AON7380_DFN3X3-8-5

@PC308 0.1U_0_02_25V7K

CMSRC_CHG

ASGATE_CHG

support Turbo boost 2200P
no support Turbo boost 0.1u

PC307 0.22U_0603_25V7K

CSIP_CHG
CSIN_CHG
OPCN_CHG
OPCP_CHG
VBAT_CHG
BGATE_CHG

PU301 ISL88739AHRZ-T_QFN32_X

ACIN
ACOK
SDA
SCL
PROCHOT#
AMON
BMON
NC
AGND
PROG
COMP
CCLIM
FSET
BATGONE
CSON
CSOP
ACLIM
BOOT
UGATE
PHASE
LGATE
VDDP
VDD
DCIN
NTC

PR312 0_0603_5%

BST_CHG
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG

PQ305 AON7506_DFN33-8-5

PQ306 AON7506_DFN33-8-5

PC309 0.1U_0_02_16V_Z

PR319 7_0_02_5%

PC313 1U_0201_6.3V6K

PC31 1U_0201_6.3V6K

PR320 7_1206_5%

EMI@ PC315 680P_0_02_50V7K

PR323 100K_0_02_1%

PC318 1U_0603_25V6

PR32 10_1206_5%

VF = 0.38V

PD1 S SCH DIO BAS 0CW SOT-323

+19V_VIN

PR326 @ 0_0603_5%

+12.6V_BATT

PR315 0.01_1206_1%

PL301 1UH_PCMB063T-R7MS_8A_20%

17: V_BATT_CHG

+12.6V_BATT

PC310 10U_0805_25V6K

PC311 10U_0805_25V6K

PC312 10U_0805_25V6K

Support max charge 3.5A
Power loss: 0.245W
VCSPP-VCSON spec < 81mV

Choke 4.7uH SH00800YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)

For 4S per cell 4.35V battery

AC N_CHG

S_BATT@ PR3 2 2M_0_02_1%

S_BATT@ PQ308 LTC015EUBFS8TL_UMT3F

S_BATT@ PR3 3 100K_0_02_1%

< 3> BATT_ S

S_BATT@ PQ315 2N7002KW_SOT323-3

< 3,51,56,59> SUSP#

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 1mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VAD P x IAD P + VBA T x IBA T)
R Psys = 1 2V / Ipsys
KPSYS = 1 14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1 14 x (45+40) = 96 9uA
R Psys = 1 2V / 96 9uA = 12 3K ohm
==========
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1 14 x (65+40) = 119 7uA
R Psys = 1 2V / 96 9uA = 10K ohm

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

<43> AC_IN
<43,53> EC_SMB_DA1
<43,53> EC_SMB_CK1
<11, 3> H_PROCHOT#
<43,53> ADP_I

EC_SMB_DA1_R
EC_SMB_CK1_R
AMON_ISL95520
BMON_ISL95520

Close to EC.

Follow adapter and battery wattage in Vsys current source.
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

Close to EC

PR316 0.1U_0_02_25V6
PR317 0.1U_0_02_25V6
PR322 0_0_02_5%
PR325 10K_0_02_1%

VDD=5V

VDD_CHG
ACLIM_CHG
CCLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG

PR328 200K_0_02_1%
PR329 200K_0_02_1%
PR331 76.8K_0_02_1%
PR337 75K_0_02_1%
PR335 150K_0_02_1%
PC320 560P_0_02_50V7K
PR332 100_0_02_1%
PC321 0.015U_0_02_25V7K

OCCP setting

Hybrid boost power mode
Cell = 4s

Pull high on HW side

+3VS

@VGA@ PR3 0 10K_0_02_1%
@VGA@ PR3 1 10K_0_02_1%

<20 26, 3> DGPU_AC_DETECT

@VGA@ PQ31 RUM001L02_VMT3
@VGA@ PQ313B 2N7002KDW_SOT363-6
@VGA@ PQ313A 2N7002KDW_SOT363-6

H_PROCHOT#
AC_IN

@ PR309

PR336 180W@

L2N7002WT1G_SC70-3

CSOP_CHG
CSOP_CHG_R
CSON_CHG
CSON_CHG_R

PR330 2_0_02_5%
PC319 0.1U_0_02_25V6
@ PR33 0_0_02_5%

PR333=0 ohm, Fs=500KHZ ~ +/ 15%

BATT_TEMP < 3,53>

BATGONE(BATT TEMP)
logic high: above 2.4V
logic low: under 0.8V

ICClimit 7.73A
Delta I 1.44A
1C charge current 6.48A

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC LIM = VccLIM / 32 x Rs2
==========
AC LIM = Vac LIM / 32 x Rs1

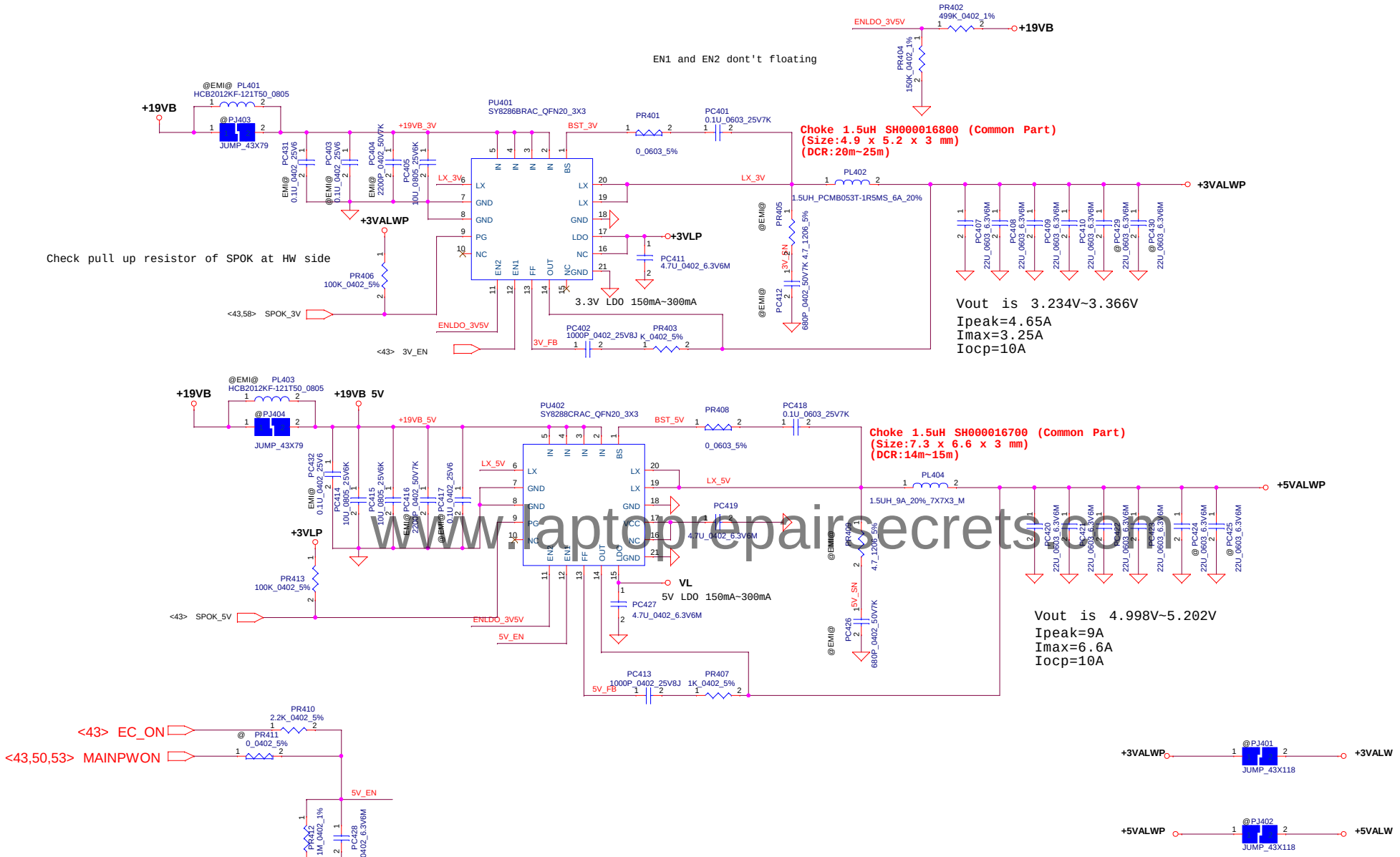
Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_CHARGER

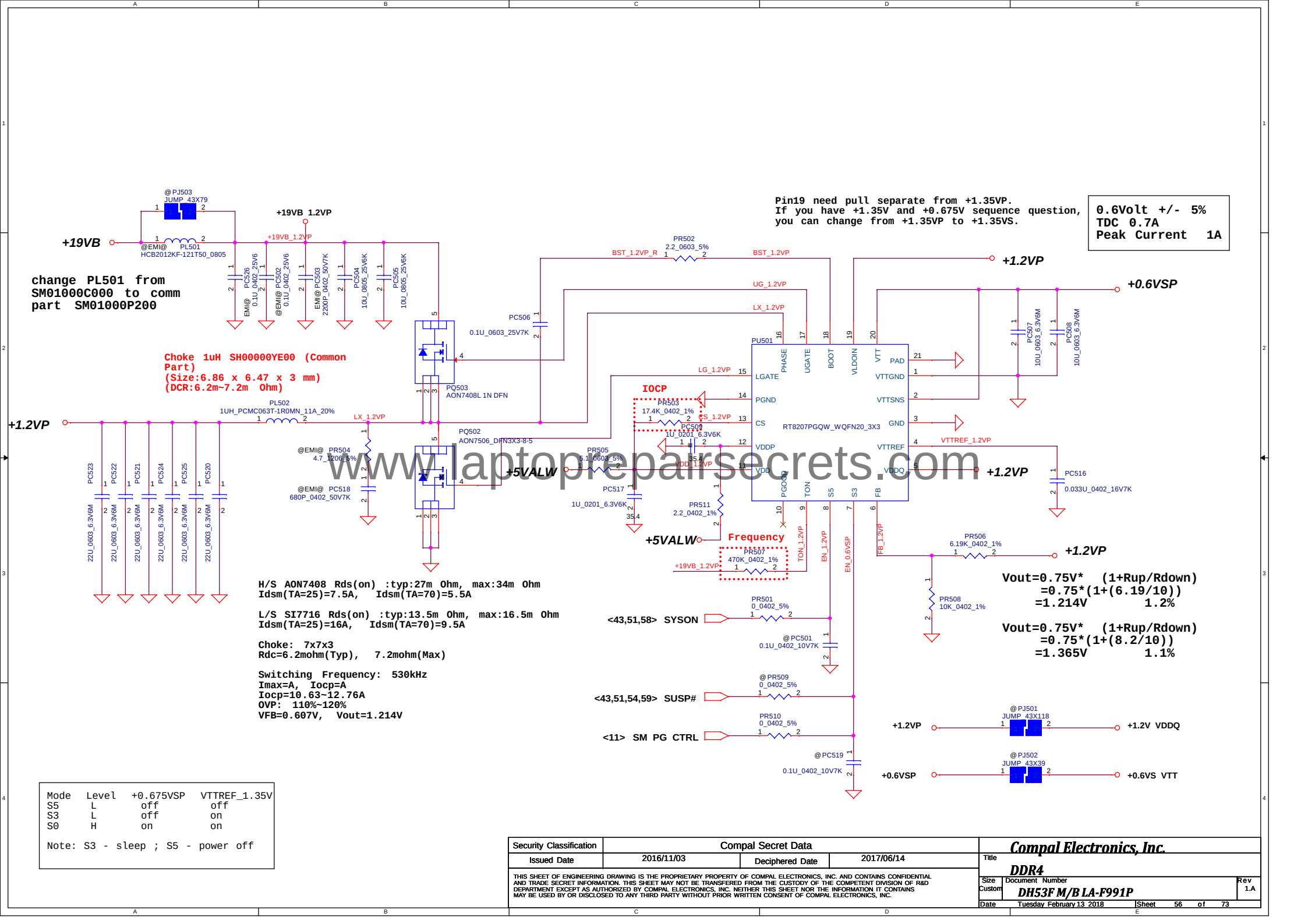
Size: | Document Number: | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 5 of 73



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: DH53F M/B LA-F991P		Rev: 1.A
Date: Tuesday, February 13, 2018	Sheet 55 of 73		



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

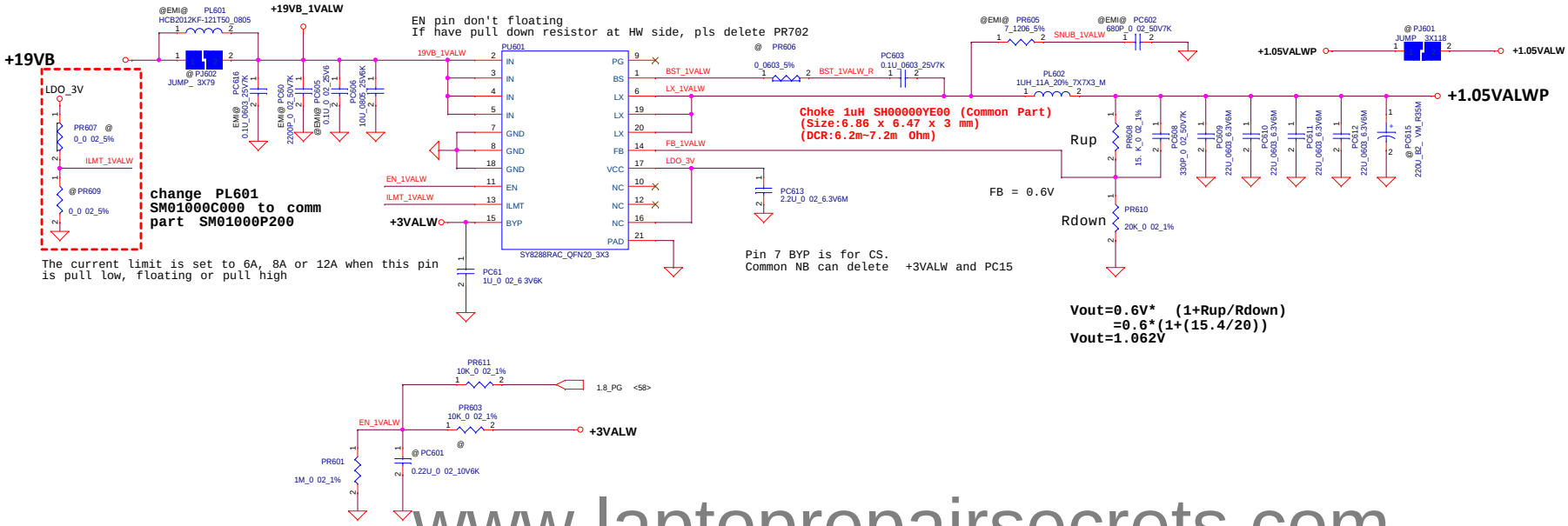
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 56 of 73



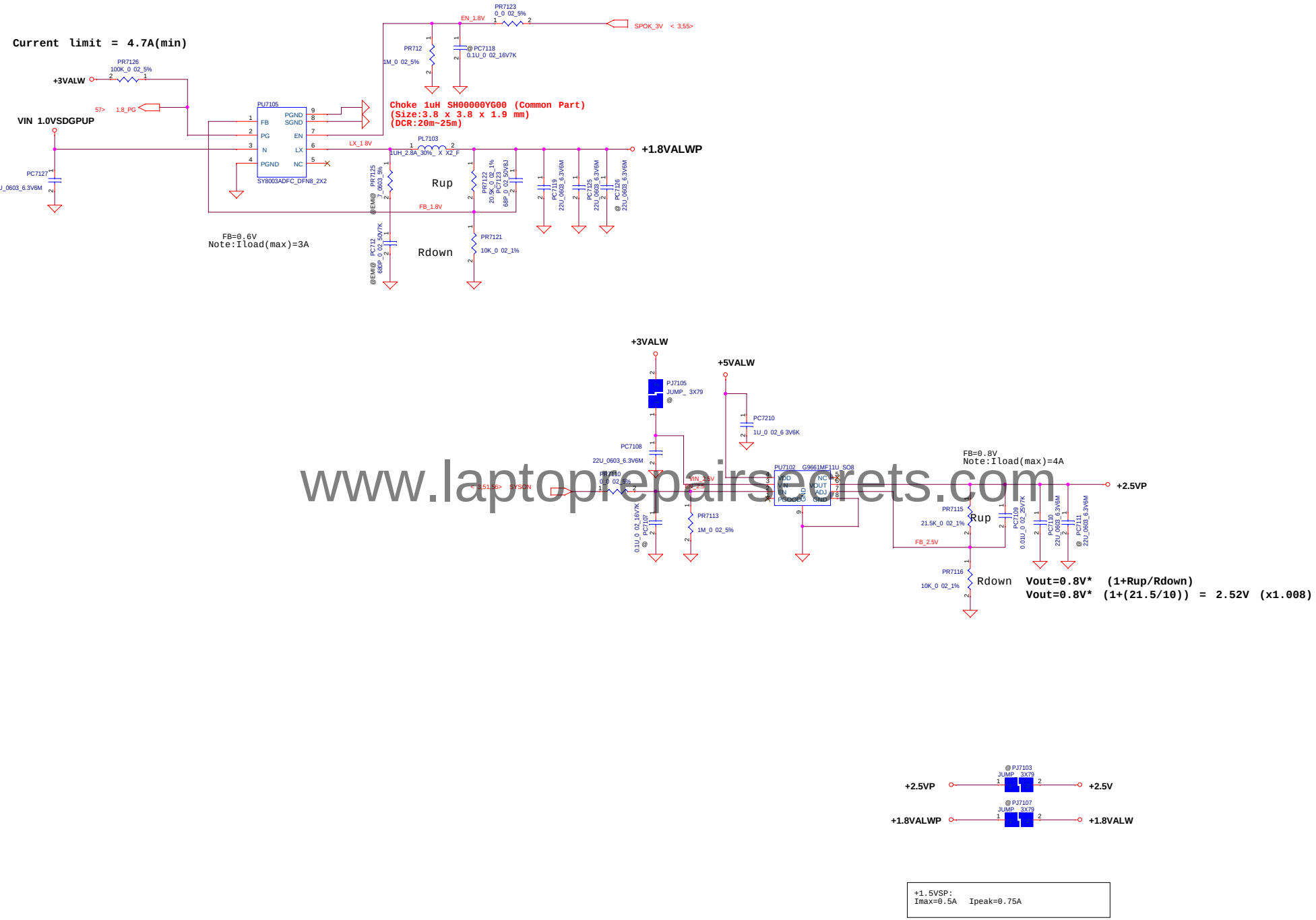
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc

Title: 1V

Size	Document Number	Rev
C	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 57 of 73



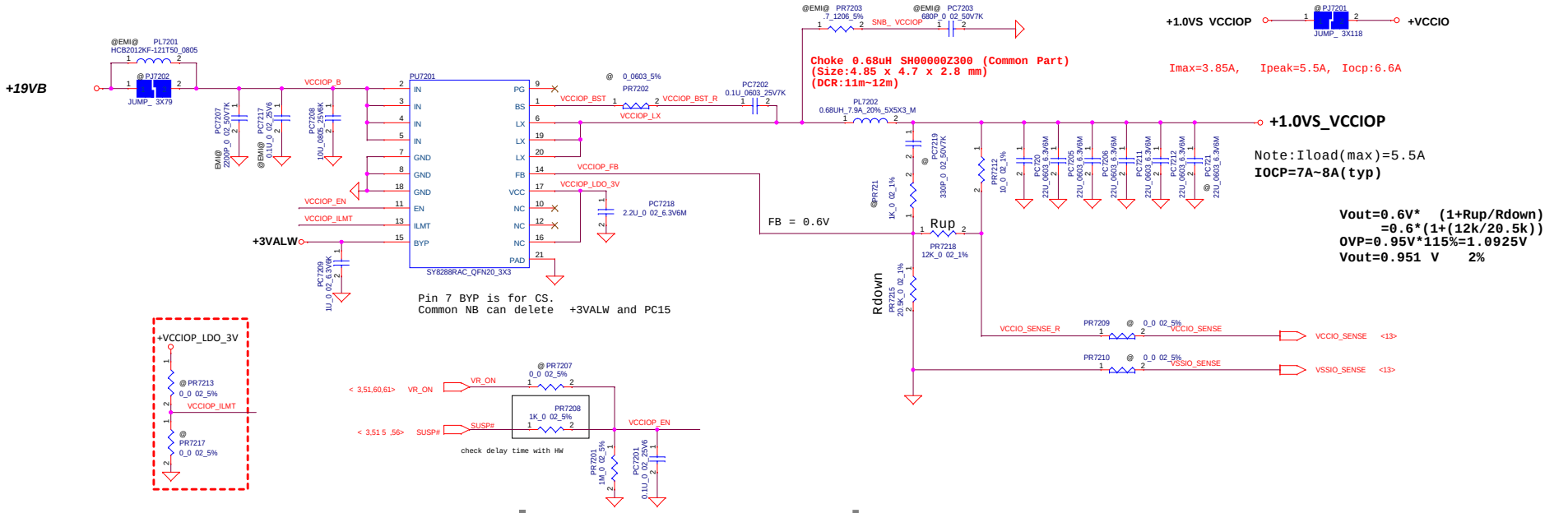
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc

Title: 1.5VS/2.5V

Size	Document Number	Rev
C	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 58 of 73



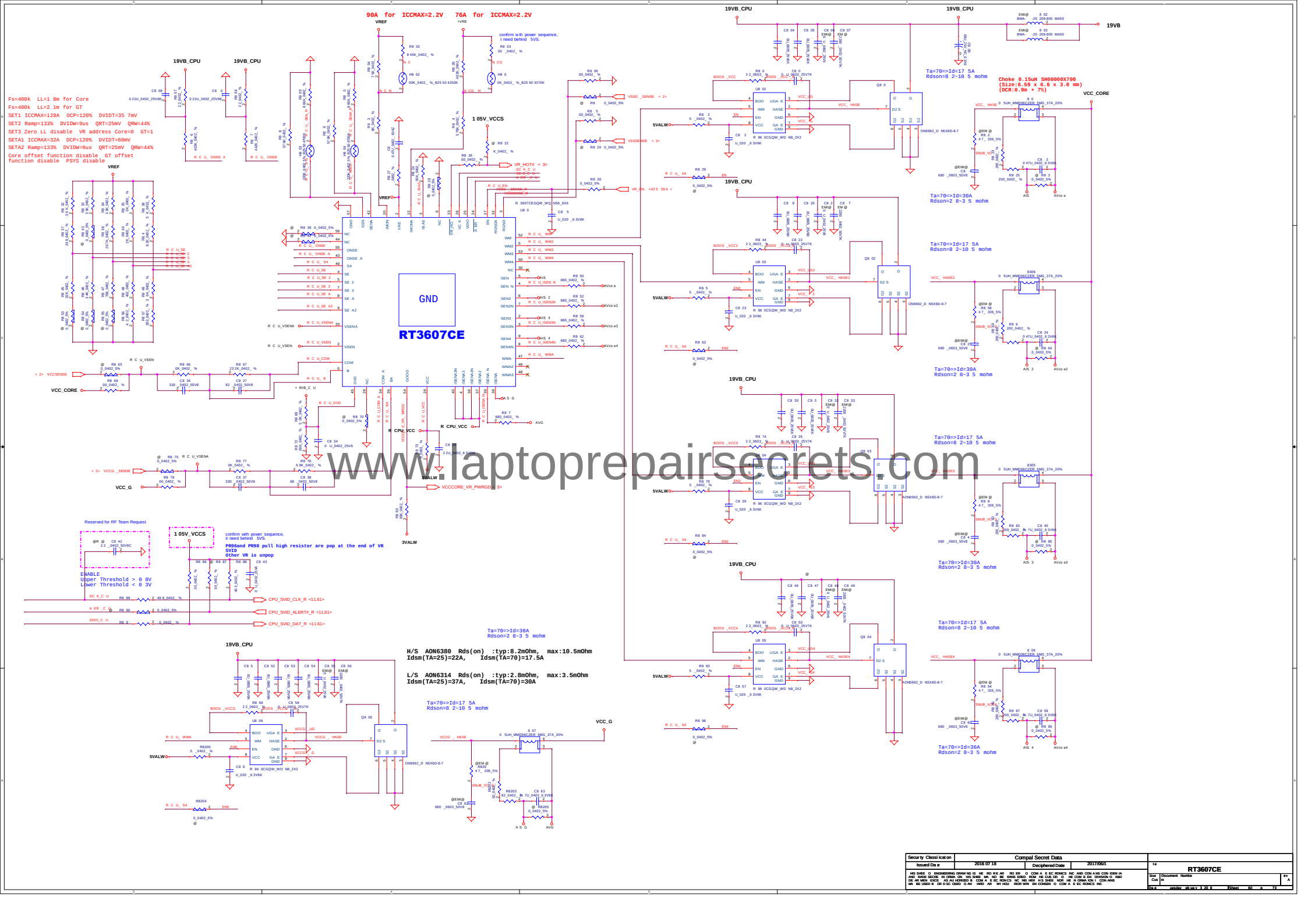
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

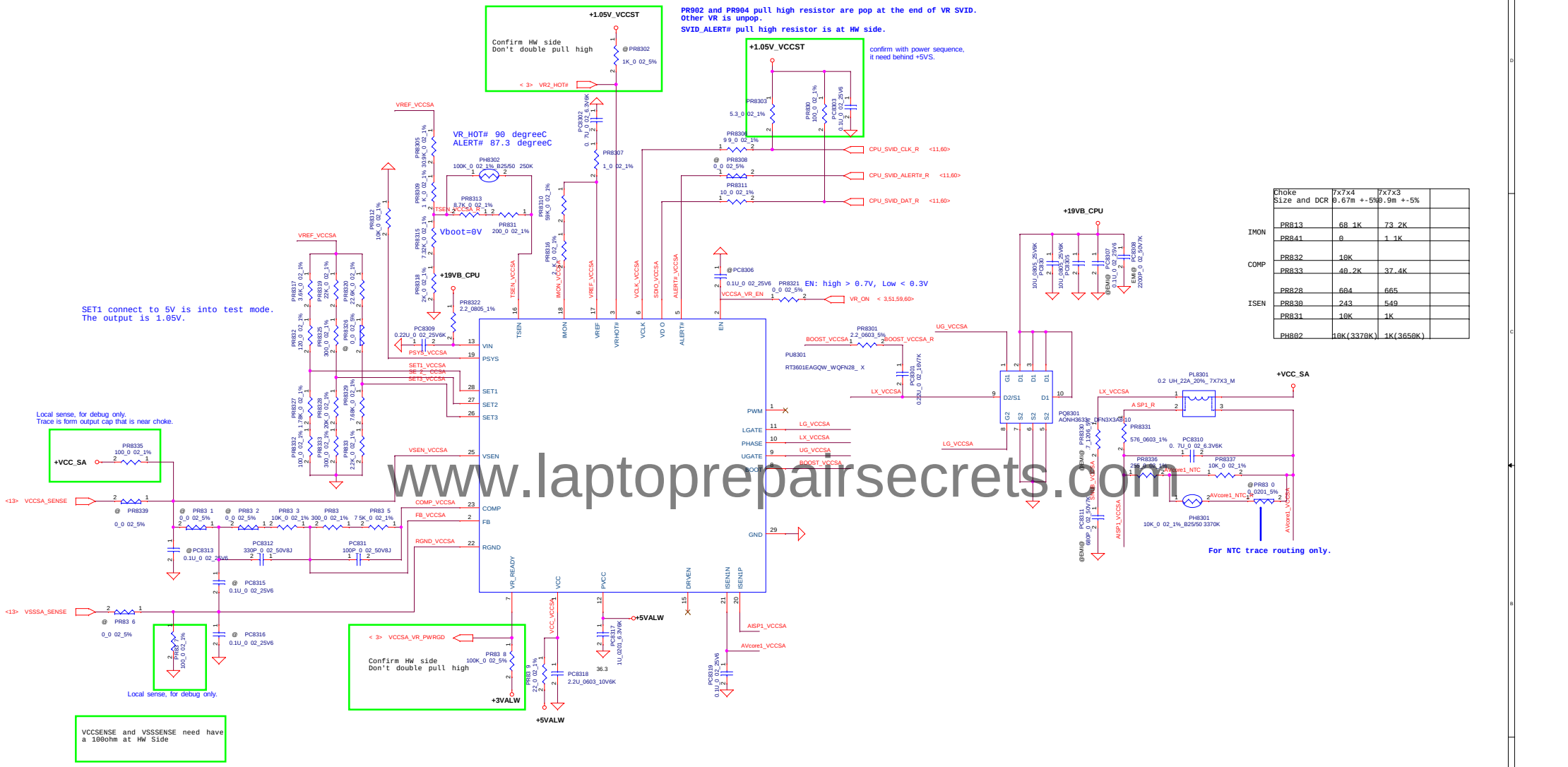
Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size	Document Number	Rev
C	1.0VS VCCIO	1.A

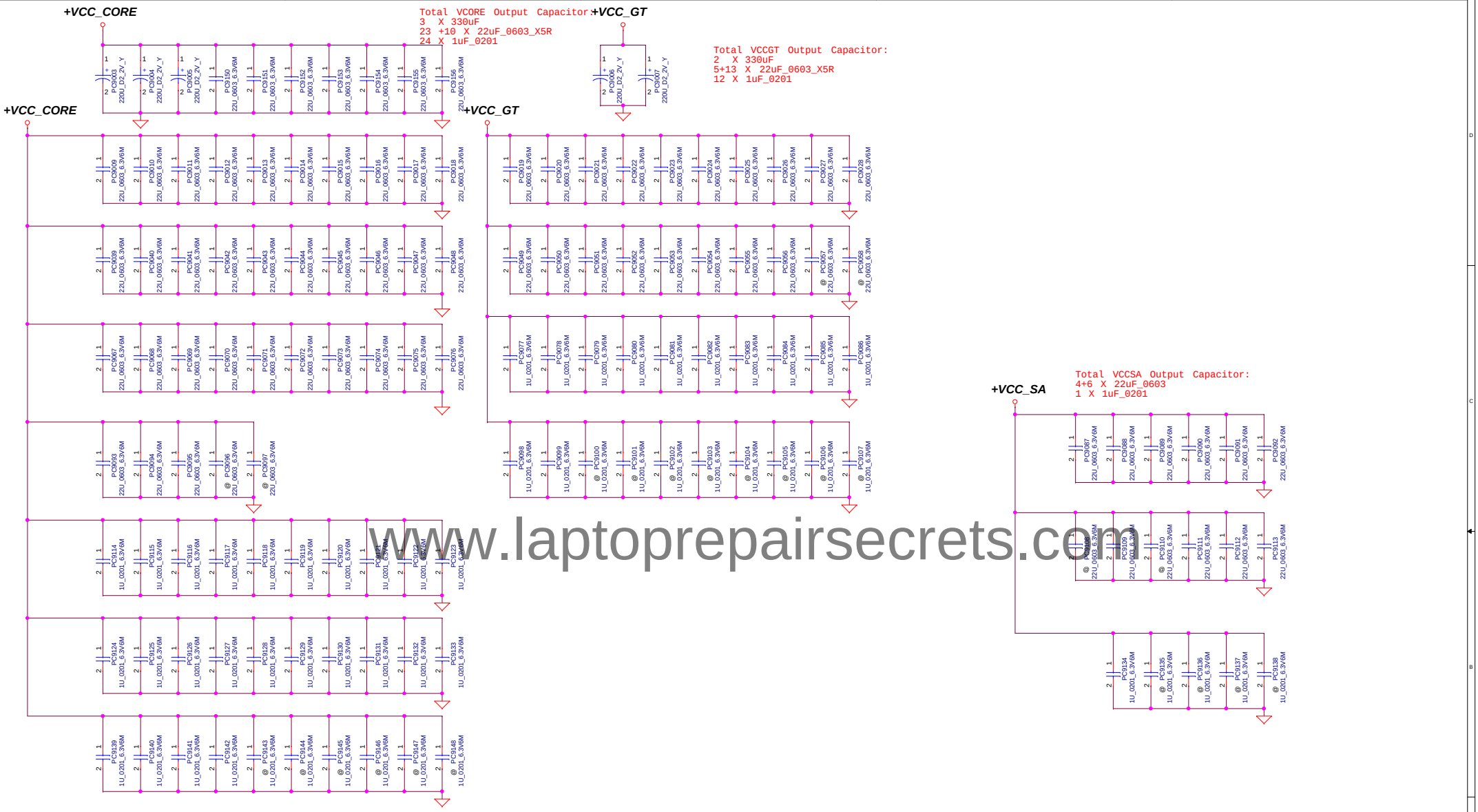
Date: Tuesday, February 13, 2018 Sheet 59 of 73





Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Title	RT3601EA VCC SA		
Size	Document Number		Rev 1A
Cust m			
Date:	Tuesday, Feb uary 13, 2018	Sheet 61 of 73	



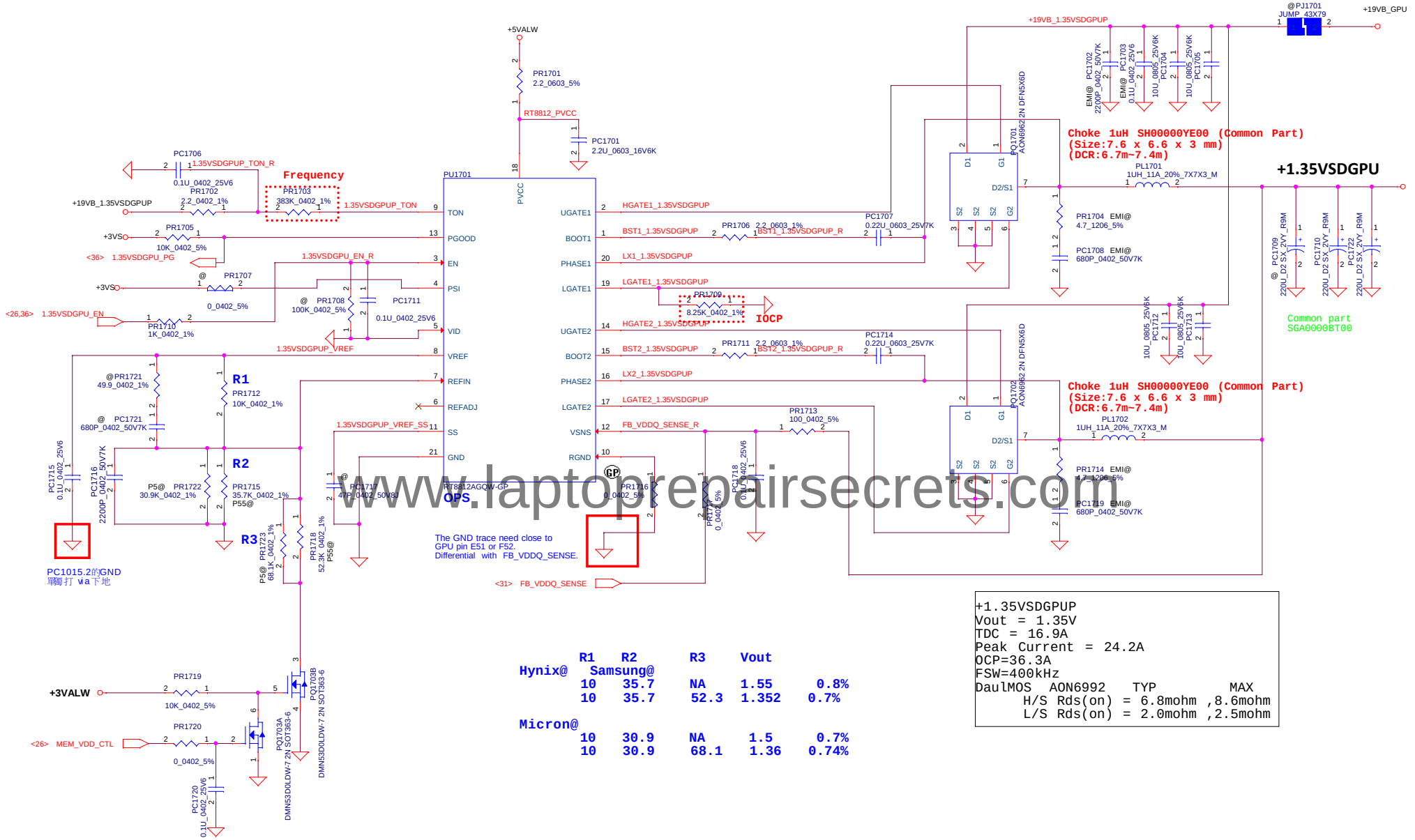
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size	Document Number	Rev
Custom		1.A

Date: Tuesday, February 13, 2018 Sheet 62 of 73



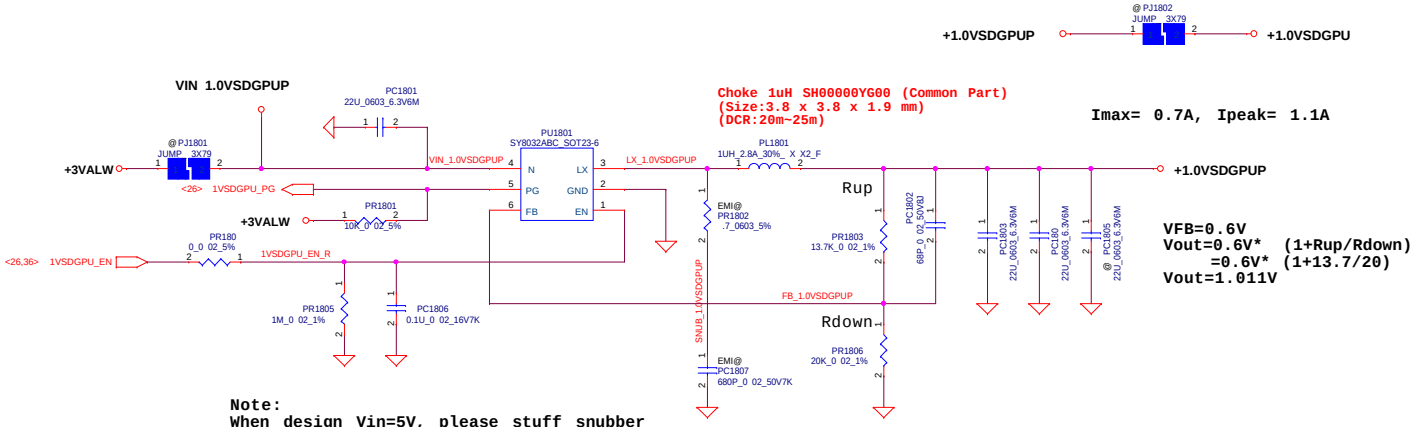
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VRAM

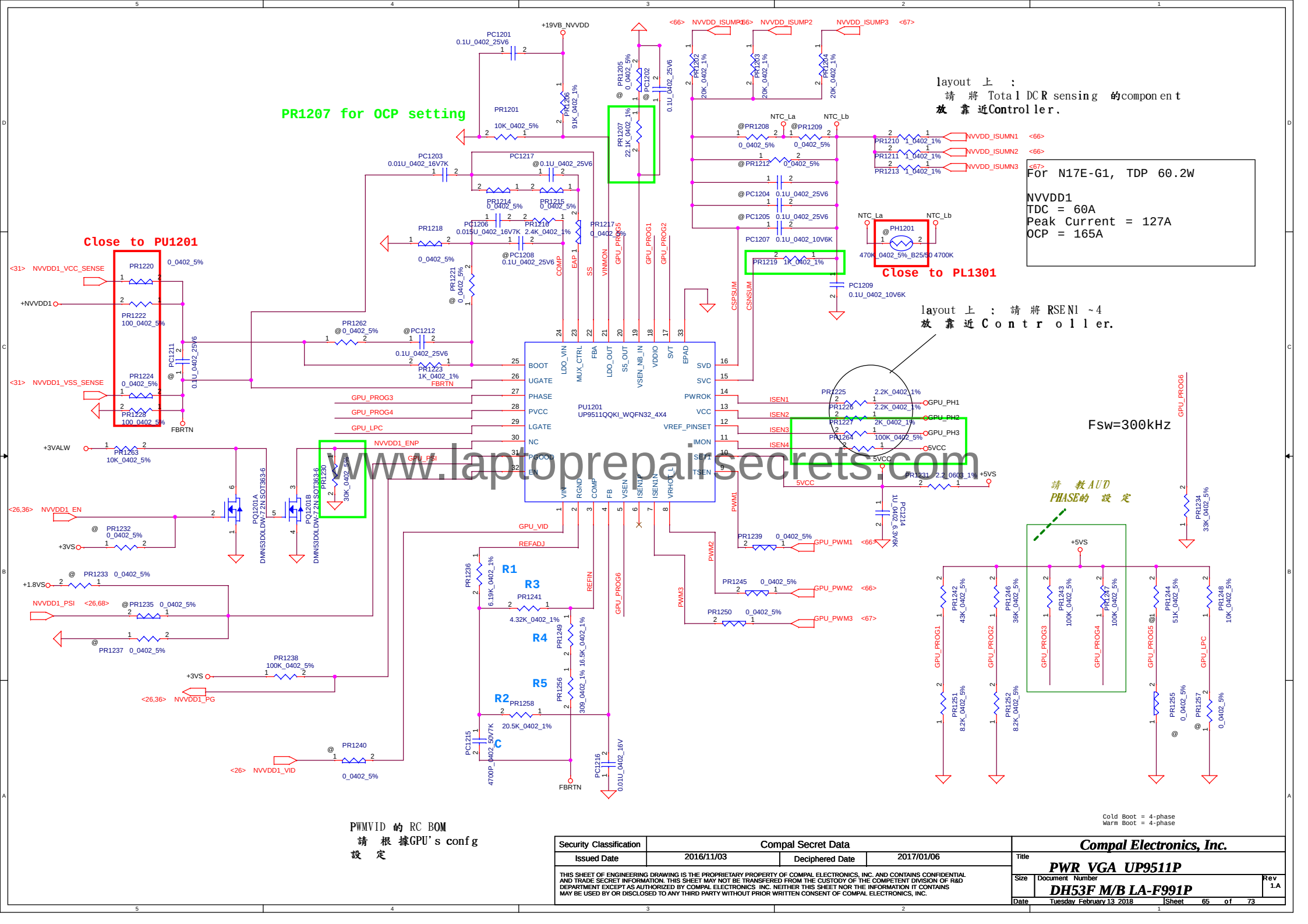
Size	Document Number	Rev
Custom	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 63 of 73



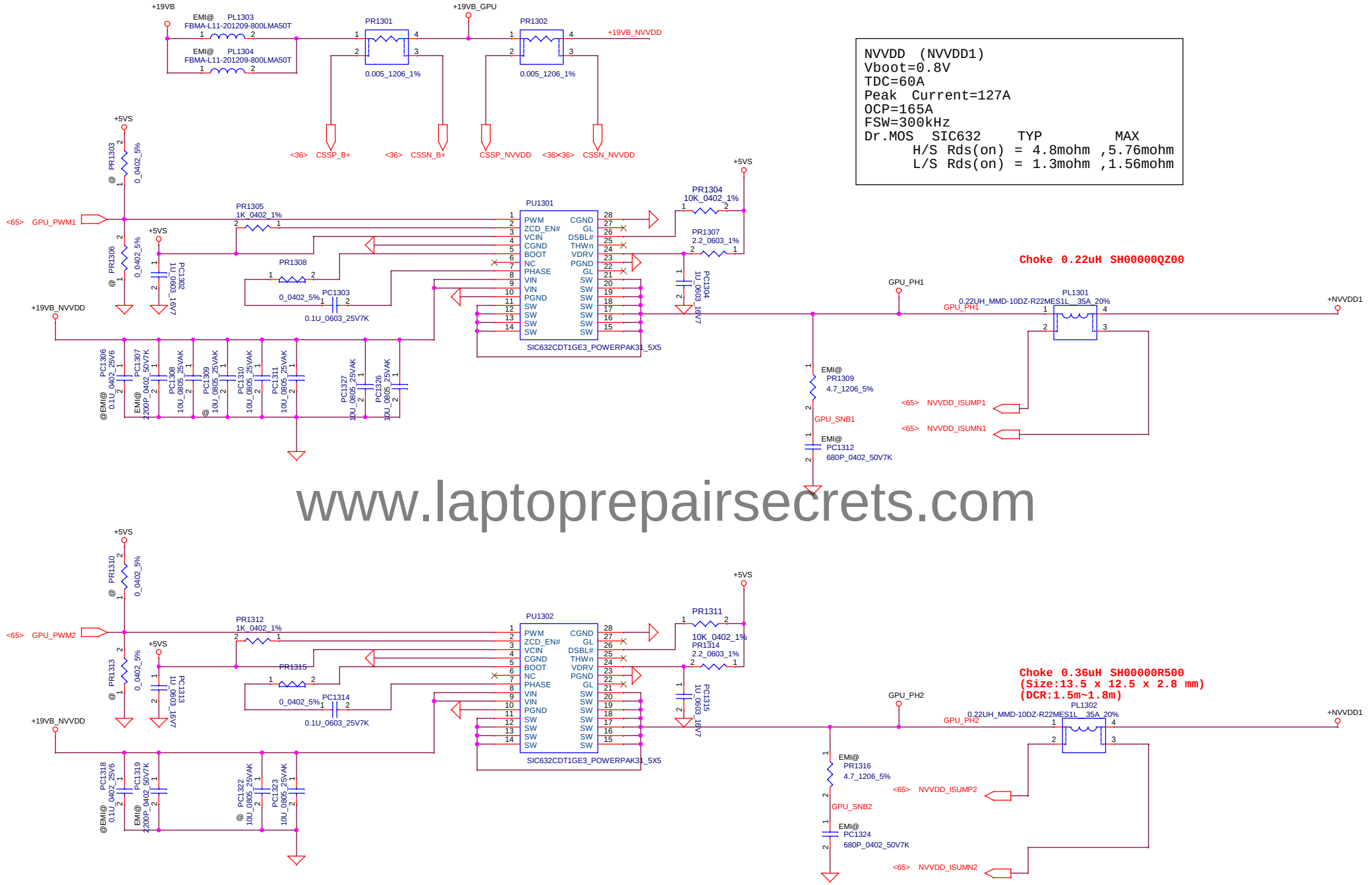
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc			
Title	1.05VSDGPU		
Size C	Document Number DH53F M/B LA-F991P		Rev 1.A
Date: Tuesday, February 13, 2018	Sheet 6 of 73		



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR_VGA_UP9511P		
Size	Document Number: DH53F M/B LA-F991P		Rev: 1.A
Date: Tuesday, February 13, 2018		Sheet 65 of 73	



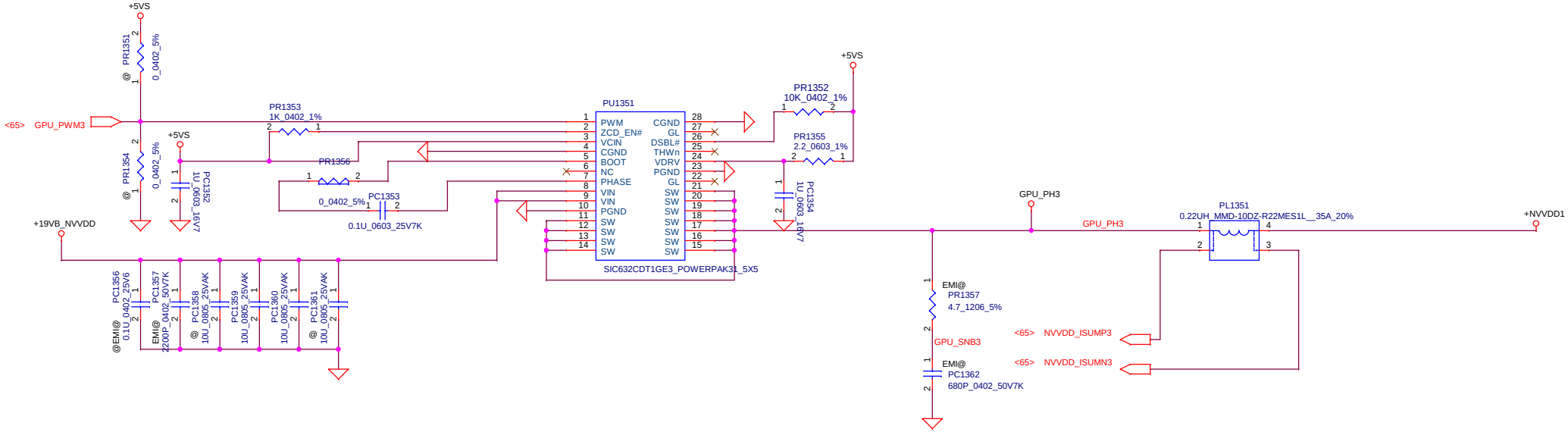
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR +NVVDD1**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 66 of 73



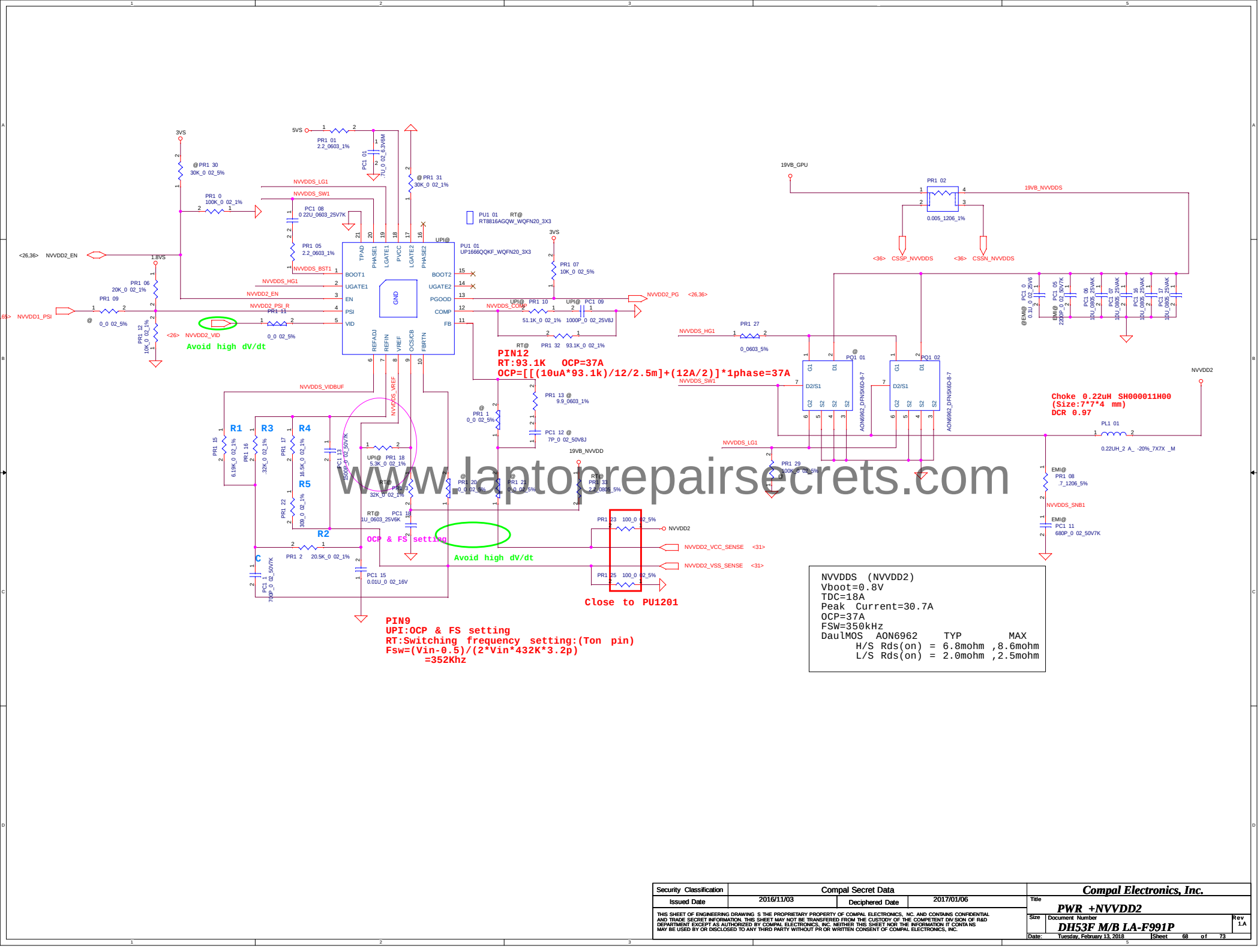
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR +NVVDD1**

Size | Document Number: **DH53F M/B LA-F991P** | Rev: 1.A

Date: Tuesday, February 13, 2018 | Sheet 67 of 73



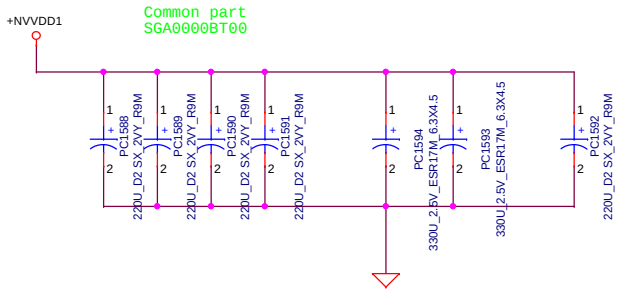
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

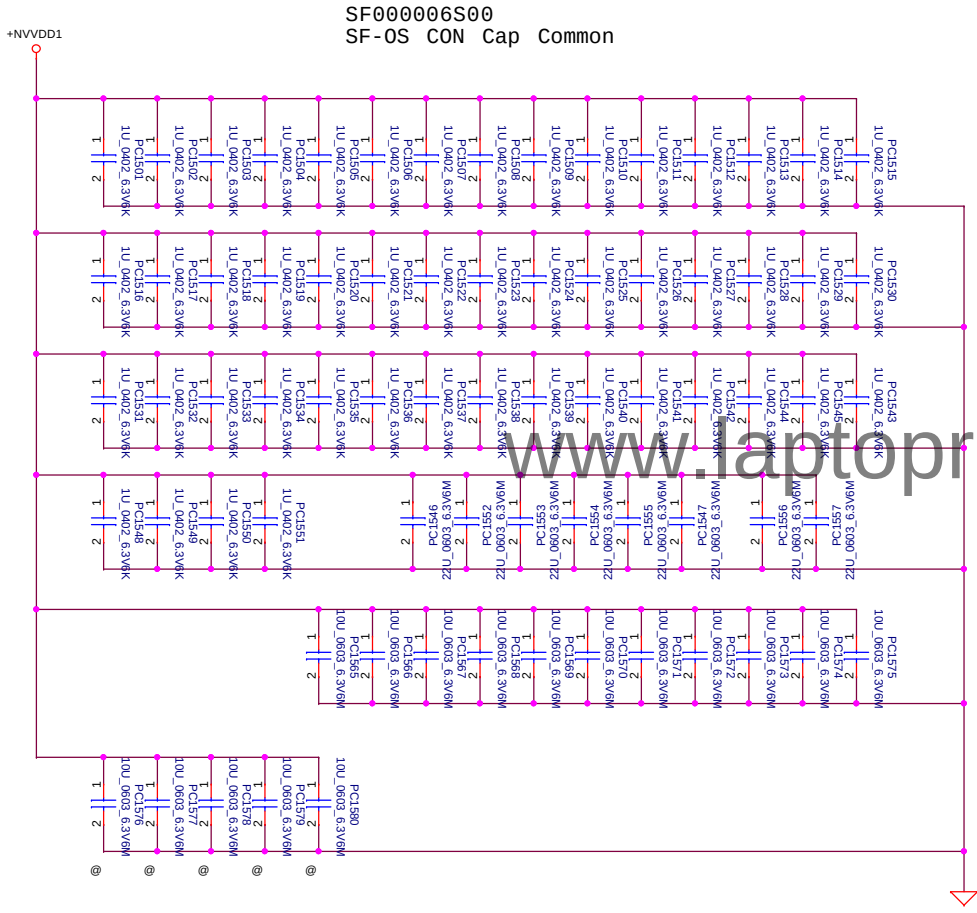
Compal Electronics, Inc.

Title: **PWR +NVVDD2**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A

Date: Tuesday, February 13, 2018 Sheet 68 of 73

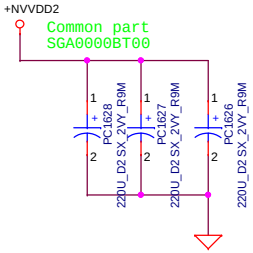


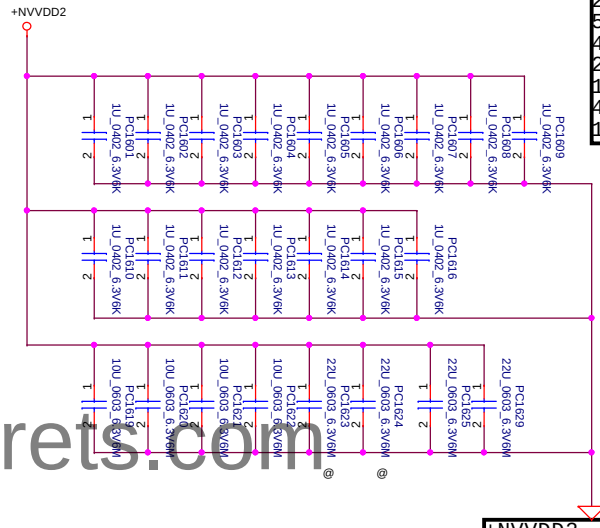



```
+NVVDD1
220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 23
4.7uF_0603 X 9
1uF_0402 X 49
```

```
+NVVDD1
220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 11(unpop 5)
1uF_0402 X 49
```

```
+NVVDD1
220uF X 4
330uF X 2
560uF X 1
22uF_0603 X 8
10uF_0603X 11(unpop 5)
1uF_0402 X 49
```






```
+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2
10uF_0603 X 4
4.7uF_0603 X 2
1uF_0402 X 16
```

```
+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16
```

```
+NVVDD2
220uF X 2
560uF X 1
22uF_0603 X 4 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16
```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Compal Electronics, Inc.

Title: **PWR_VGA DECOUPLING**

Size	Document Number	Rev
	DH53F M/B LA-F991P	1.A
Date: Tuesday, February 13, 2018	Sheet 69 of 73	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		Down Size	0.1		PQ311,PQ312: AON6366E 1N DFN5X6-8SB00001D800->AON7380_DFN3X3-8-5SB00001GM00 PC302,PC303,PC310,PC311,PC312: 10U_0603_25V6MSE00000X200->10U_0805_25V6KSE00000QK00 PC323: 10U_0603_25V6MSE00000X200->Del PC315,PC1312,PC1324,PC1362,PC1411: 680P_0603_50V7KSE025681K80->680P_0402_50V7KSE074681K80 PC412,PC426,PC602,PC7203,PC8311: 680P_0603_50V7KSE025681K80->680P_0402_50V7KSE074681K80Unpop PC102: 100P 50V J NPO 0603SE024101J80->100P 50V J NPO 0402SE071101J80 PC104: 1000P 50V K X7R 0603SE025102K80->1000P 50V K X7R 0402SE074102K80 PQ1401: AON6962_DFN5X6D-8-7SB00001ID00->Unpop	10/26	A
02		Down Size & NVVDDS IC COLAY	0.1		PR1301,PR1302,PR1402: 0.005_2512_1%SD000016U00->0.005_1206_1%SD000017R00 PC1410: 0.1U_0603_16VSE026104K80->Del PR1432: Add->93.1K_0402_1%SD034931280 PR1410: 51.1K_0402_1%SD034511280->un pop PC1409: 1000P_0402_25V8JSE068102J80->un pop PU1401: UP1666QQKF_WQFN20_3X3SA00009SX00->RT8816AGQW_WQFN20_3X3SA00009WE00 PR1414: 10K_0402_5%SD028100280->0_0402_5%SD028000080 PR1418: 45.3K_0402_1%SD034453280->un pop PR1419: 84.5K_0402_1%SD034845280->Del PR1433: Add->2.2_0805_5%SD002220B80 PC1418: Add->1U_0603_25V6KSE000006900 PR1434: Add->432K_0402_1%SD034432380 PC8134: 0.1U_0402_50V7KSE074104K80->0.1U_0402_25V6SE00000G880	10/26	A
03		CPU TEST	0.1		PU501_RT8207PGQW_WQFN20_3X3_->_RT8207PGQW_WQFN20_3X3-S PH8103,PH8104_150K_0402_5%_B25/50 4500K_SL200002K00_->_S THERM_ 220K +-5% 0402 B25/50 4700K_SL200002I00 PR8110, PR8109_8.87K_0402_1%_SD034887180_->_8.66K_0402_1%_SD034866180 PR8118, PR8119_93.1K_0402_1%_SD034931280_->_57.6K_0402_1%_SD034576280 PC8113,PC8124,PC8140,PC8159,PC8163_0.47U_0402_16V4Z_SE000002F80_->_0.47U_0402_6.3V6K_SE124474K80 PC8310_0.47U_0402_25V6K_SE00000WA00_->_0.47U_0402_6.3V6K_SE124474K80 PR8114_6.81K_0402_1%_SD034681180_->_5.76K_0402_1%_SD034576180 PR8113_2.49K_0402_1%_SD034249180_->_1.8K_0402_1%_SD00000R580 PR8117_560K_0402_1%_SD034560380_->_442K_0402_1%_SD034442300 PR8116_510K_0402_1%_SD00000RK80_->_402K_0402_1%_SD034402380 PR8141_100_0402_1%_SD034100080_->_8.2K_0402_1%_SD000004100 PR8149_1.05K_0402_1%_SD00000J480_->_3.16K_0402_1%_SD000006580 PR8176_20K_0402_1%_SD034200280_->_16.9K_0402_1%_SD034169280 PR8310_63.4K_0402_1%_SD03463K280_->_59K_0402_1%_SD034590280 PR8319_24.9K_0402_1%_SD034249280_->_22K_0402_1%_SD034220280 PR8325_0_0402_5%_SD028000080_->_300_0402_1%_SD034300080 PR8328_22K_0402_1%_SD034220280_->_20K_0402_1%_SD034200280 PR8333_680_0402_1%_SD034680080_->_300_0402_1%_SD034300080 PC8312_270P_0402_50V7K_SE074271K80_->_330P_0402_50V8J_SE000006I80 PR8331_470_0603_1%_SD014470080_->_576_0603_1%_SD014576080 PR8336_42.2_0402_1%_SD00000ZN00_->_255_0402_1%_SD034255080 PC9110 PC9108_22U_0603_6.3V6M_SE00000M000_->_unpop PC9112 PC9113_unpop_->_22U_0603_6.3V6M_SE00000M000 PC8126,PC8137_330P_0402_25V8J_SE00000FD80_->_330P_0402_50V8J_SE000006I80 PR8134_121K_0402_1%_SD034121380_->_13.3K_0402_1%_SD034133280 PR8138_49.9K_0402_1%_SD034499280_->_26.7K_0402_1%_SD034267280 PR8147_3.32K_0402_1%_SD034332180_->_768_0402_1%_SD00000TT80 PR8173_0_0603_5%_SD013000080_->_10_0603_1%_SD014100A80	10/26	A
04		down size &CHANGE VGA IC	0.2		PU1201_UP9511PQGJ_VQFN40_5X5_SA00009SW00_->_UPI9511QQKI WQFN 32P_SA0000BK300 PC8317,PC509,PC517_1U_0402_10V6K_SE00000QL10_->_1U 6.3V K X5R 0201_SE00000YB00 PC8112,PC8115,PC8123,PC8139,PC8157,PC8161_1U_0402_25V6K_SE000010V00_->_1U 6.3V K X5R 0201_SE00000YB00	11/08	A
05		Unpop reduce charger IC loss extra circuit. Unpop GPIO12& PROCHOT synchronous circuit.	0.2		PQ307_ LMUN5113T1G PNP SOT323-3_SB000013X00_->_Unpop PQ308_ LMUN5236T1G NPN SOT323-3_SB000011K00_->_Unpop PQ313_2N7002KDW 2N SOT-363-6_SB00000EO00_->_Unpop PQ314_RUM001L02 1N VMT3_SB000012900_->_Unpop PR340_10K_0402_1%_SD034100280_->_Unpop PR327_0_0603_5%_SD013000080_->_Unpop PR326_0_0603_5%_SD013000080_->_SMT PR310_51.1K_0402_1%_SD034511280_->_52.3K_0402_1%_SD034523280 PC1709_220U_D2_SX_2VY_R9M_SGA0000BT00_->_Unpop PC8147_10U_0805_25V6K_SE00000QK00_->_Unpop	11/15	A

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Compal Electronics, Inc.			
Title	PIR		
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Item	Fixed Issue		Rev.	PG#	Modify List	Date	Phase
01		0ohm ->R-Short	1.0		PR326,PR304,PR314,PR316,PR317,PR322,PR333,PR334,PR8111,PR8120,PR8128,PR8129,PR8139,PR8142, PR8143,PR8153,PR8154,PR8155,PR8163,PR8165,PR8170,PR8175,PR8184,PR8190,PR8198,PR8204,PR8308, PR8339,PR8341,PR8342,PR8346,PR8326,PR1414_SD028000080 chage to _R-Short 0402 PR326 0_0603_5%_SD013000080 ->R-Short 0603_SD013000080	12/17	A.2
02		material shortage	1.0		PC313,PC314_1U_0402_16V6K_SE00000OU00_->_1U 6.3V K X5R 0201_SE00000YB00 PC1303,PC1314,PC1353,PC8101,PC8122,PC8135,PC8150,PC8158 _0.1U_0603_50V7K_SE025104K80_->_0.1U 25V K X7R 0603_SE042104K80 PC305,PC324_0.1U_0402_25V7K_SE00000W210_->_0.1U_0402_25V6_SE00000G880	12/17	A.2
		Acer SW2 design reserve	1.0		PR217 0_0402_5%_SD028000080(unpop) -> SMT 0402_SD028000080	12/17	A.2
03		For 4S per cell 4.35V battery	1.0		PQ307_LMUN5113T1G_SOT323-3_SB000013X00_->del PR327unpop_0_0603_5%_SD013000080_->del PR342Add_->_2M_0402_1%_SD034200480 PR343Add_100K_0402_1%_SD034100380 PQ315Add_2N7002KW_SOT323-3_SB00000ST00	12/20	A.2
04		charger boost cap to 0.47uF but material shortage so down size.	1.0		PC309_0.22U_0603_25V7K_SE000005Z80_->_0.47U_0402_16V4Z_SE000002F80	12/21	A.2
05		ACDET change	1.0		PR306_392K_0402_1%_SD034392380_->_499K_0402_1%_SD034499380 PR310_52.3K_0402_1%_SD034523280_->_66.5K_0402_1%_SD034665280	12/28	A.2

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	46	USB	10/18	Correct USB charger connection.	1.Change RS15 connection to CHG_ILMSEL.	DVT	0.2
2	19,36	Placement	10/18	Placement	1.Remove RPH10, add RH197,RH198. 2.UG27 source change to +1.8VALW for +1.8VSDGPU_AON/+1.8VSDGPU_MAIN.	DVT	0.2
3	41	CNVI	10/18	For CNVI power rail.	1.Co-lay RM46 for CNVI +3VALW power rail.	DVT	0.2
4	42	Material	10/18	X1 code issue.	1.LA1 change to SM01000NS00.	DVT	0.2
5	48	USB	10/18	redriver verify.	1.Add one USB3.0 port to JIO3.	DVT	0.2
6		Placement	10/21	Placement	1. Change RM36,RM37,RM42,RM43 to 0402 size. 2. Change RH186,RH47,RH98~RH100,RH103,RH105,RD2,RD3,RD6,RD13,RD15,RD17,RM34,RM35 ,RM38,RM39,RS1,R19,R20,RQ5,RQ6,RQ9 to R-short. 3. Change RS8,RS10 to 1206 R-short. 4. Change RH97 to 0805 R-short.	DVT	0.2
7	11	ESD cap.	10/21	Sourcer request.	1.Change CC66,CC68 to SE074102K80.	DVT	0.2
8	43	EC	10/21	EC board ID.	1.Change RB3 to 12kohm/28P@ and 160kohm/32P@	DVT	0.2
9		Cap.	10/24	Sourcer request.	1. Change CA6,CA8,CA9,CA12,CA14,CA16,CA19,CC71~CC81,CC88~CC90,CG130,CG131 ,CG143~CG145,CG168,CG169,CG178~CG181,CG193,CG205~CG207,CG229,CG230,CG241,CG243 ,CG253~CG255,CG267~CG269,CG291,CG292,CG303~CG305,CX1,CX3 from 0402 to 0603 size.	DVT	0.2
10	50	Screw hole	10/25	Screw hole	1.Change H21 footprint to H_6P0.	DVT	0.2
11	48	USB EMI	10/25	EMI issue.	1.Add LS11,LS12.	DVT	0.2
12	41,43	CNVI	10/26	For CNVI power rail detect.	1.Add net CNVI_DET#,RB78,RB79.	DVT	0.2
13	46	USB	10/26	Correct USB charger connection.	1.Correct USB2.0 connection for US12.	DVT	0.2
14	42	DMIC	10/26	Acer request.	1.Change JDMIC1 from 8pin to 4pin.	DVT	0.2
15	47	SATA	11/03	Co-layout.	1.Co-lay JHDD3,CO14~CO17,RO21~EO24.	DVT	0.2
16	44	SMBus	11/08	Co-layout.	1.Co-lay RS114,RS115.	DVT	0.2
17	49	SW	11/14	Remove debug SW.	1.De-pop SW1.	DVT	0.2
18	44	Type-C	11/14	CC logic control by EC SMBus.	1.De-pop QS1,QS3,RS107,RS108,RS111. Pop RS114,RS115.	DVT	0.2
19	16	Cap.	11/14	by crystal vendor test result.	1.Change CH7,CH8 to 10pF.	DVT	0.2
20	45	Cap.	11/16	For shortage.	1.Change CS84~CS87 to SE00000G880.	DVT	0.2
21	43	CNVI	11/16	CNVI detect by SW.	1.De-pop RB78. Pop RB79.	DVT	0.2
22	43	CNVI	12/15	Remove CNVI detect.	1.Remove RB78, RB79 and netname CNVI_DET#.	PVT	1.0
23	18	PECI	12/15	For PECI issue.	1.De-pop RH41.	PVT	1.0
24	50	BI SW	12/15	By customer request.	1.De-pop SW2.	PVT	1.0
25	43	EC	12/15	Update EC board ID.	1.Change RB3 to 15kohm/28P@ and 200kohm/32P@	PVT	1.0
26	42	Inductor	12/15	Change source.	1.Change LA1 to SM01000EE00.	PVT	1.0
27		NPI	12/15	For NPI test.	1.Change RB19,RC17,RG143,RG200,RG202,RH101,RH102,RH5,RH6,RH92,RH93,RH94,RH96 ,RM2,RS114,RS115,RB72,RB76,RL1,RL13,RQ2 to R-short.	PVT	1.0

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
28	44	Type-C	12/18	Change current limit solution	1.Change US2 to SA00006Y700. 2.Add RS116,RS117,RS118. Reserve CS101.	PVT	1.0
29	43	EC	12/20	For PWR BATT_4S	1.Add net BATT_4S to EC pin89.	PVT	1.0
30	41	WLAN	12/20	For CNVi BT_ON	1.Add RM47.	PVT	1.0
31	21	PCH	12/20	For intel sensitive net	1.Pop CH29,CH34,CS100.	PVT	1.0
32	45	Type-C	12/21	For intel new topology	1.Change RS64,RS65,RS74,RS76,RS82~RS85 to 0201 size. 2.Add CS102~CS105,RS119~RS122.	PVT	1.0
33	36	GPU	12/21	Fine tune GPU sequence	1.Change CG315 to 0.22uF, RG190 to 16.9k ohm, add RG225.	PVT	1.0
34	20		12/28	For MB ID	1.De-pop RH86. Pop RH85,RH87.	PVT	1.0
35	7,15	CPU,PCH	12/28	Update intel chip to QS PN	1.SA0000BPJ10 for i5@, SA0000BPI10 for i7@, SA0000BPF10 for PCH@.	PVT	1.0
36	7	DAZ	12/28	Update MB DAZ PN.	1.DAZ29000100 for PCB@.	PVT	1.0
37	37	eDP	12/28	For eDP sequence	1.Pop RX1.	PVT	1.0
38	18,39	PCIE	01/11	For IRST support issue.	1.Change PCIE port17~20 to port 9~12 for PCIE SSD. 2.Change SATA port0A to port4 for SATA HDD. 3.Change SSD_DEVSLP4 to SSD_DEVSLP1. 4.Change SATA_GP4 to SATA_GP1.	PVT	1.C
39	45	Type-C	01/11	For intel new topology	1.Place CS58~CS61 close to connector and change net name.	PVT	1.C
40	43	EC	01/11	Update EC board ID.	1.Change RB3 to 20kohm/28P@ and 240kohm/32P@.	PVT	1.C
41	21	PCH	01/12	For layout routing.	1.Change RH93 to 0ohm footprint.	PVT	1.C
42	45	Type-C	01/16	For intel new topology	1.Change CS58~CS61 to 0.22uF.	PVT	1.C
43	7	CPU,DAZ	01/27	Update CPU,DAZ PN	1.SA0000BPZ10 for i7@, DAZ29000103 for PCB@.	PVT	1.C
44	7,15	CPU,PCH	02/13	Update CPU,PCH PN to MP PN.	1.SA0000BPJ40 for i5@,SA0000BPZ40 for i7@,SA0000BVP10 for PCH@.	Pre-MP	1.C

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Title: PIR-HW2

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