Compal Confidential

EH50F/EH51F
EH5VF/EH70F

MB Schematic Document

LA-H501P

Rev:1A

2019.02.22

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Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: EH5VF M/B LA-H501P	Rev: 1A
Date: Friday, February 22, 2019	Sheet 1 of 101	

HDMI Conn.

page 40

eDP

page 38

eDP

CoffeeLake H Processor
BGA1440
(42X28) (CFL-H_6+2)

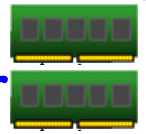
Processor page 06~13

Fan Control*2
page 77

Memory BUS
Dual Channel

1.2V DDR4 2400/2666

Interleaved Memory



260 pin DDR4-SO-DIMM X1
BANK 0, 1, 2, 3 page 23

260pin DDR4-SO-DIMM X1
BANK 4, 5, 6, 7 page 24

HDMI x 4 lanes

N18P-G0 with gDDR5 x4
or
N17P-G0-K1 with gDDR5 x3
page 25~36

PEG x16
8GT/s

NGFF
WLAN
USB port 7

page 52

PCIE 1.0
2.5GT/s
port 15

page 68

PCIE 3.0 x4
8GT/s
Port 9-12

page 68

PCIE 3.0 x4
8GT/s
Port 21-24

X4 DMI

Flexible IO

Cannonlake PCH - H
FCBGA(25X24)

874pin FCBGA

page 14~21

page 51

PCIE 2.0
5GT/s
port 14

page 67

SATA3.0
6.0 Gb/s
port 4

LAN(GbE)
Realtek 8118ASA

SATA Re-Driver
PARADE PS8527

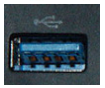
RJ45 conn.

page 32.

SATA HDD Conn.

page 47

USB 3.0
conn x1
USB (port 3)



USB 3.0
Type-C
USB (port 2)

CMOS
Camera
USB (port 5)

USB 3.0
conn x1
USB (port 1)

USBx8

48MHz page 72

page 42, 43

page 38

Finger_Print
USB (port 8)
page 66

USB charger
SLGC55544

page 71

HD Audio 3.3V 24MHz

HDA Codec
ALC255
page 42

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022
page 58

TPM
page 66

SPI

SPI ROM x1
page 16

Int. Speaker
page 42

Int. DMIC
on Camera/B
page 48

UAJ
on Sub/B
page 48

Touch Pad
PS2 / I2C

page 63

Int.KBD

page 63

RTC CKT.
page 20

Power On/Off CKT.
page 63

DC/DC Interface CKT.
page 78

Power Circuit DC/DC
page 81~97

Sub Board

HS/B page 66

IO/B page 73

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

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Title	Block Diagrams
Size: Custom	Document Number: EH5VF M/B LA-H501P
Rev	1A
Date: Friday, February 22, 2019	Sheet 2 of 101

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (W83L771)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
N18P GPU	N18P@
N17P GPU	N17P@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
KB backlight	KBLED@
KB LED driver	LED14P@
OVRM-ON	ON_X76@
OVRM-uPI	uPI_X76@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi	CNVI@
Finger Print	FP@
FinerPrint(with PBA)	PBA@
EMI requirement	EMI@
EMI require reserve	XEMI@
ESD requirement	ESD@
ESD require reserve	XESD@
FP ESD requirement	FPESD@
Pidgey ESD requirement	PGESD@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
i5 CPU	i5@
i7 CPU	i7@
H62 CPU	H62@
H82 CPU	H82@
LAN LDO mode	LDO@
LAN Switch mode	SWR@

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

43 Level	Description	BOM Structure
431AC5BOL01	SMT MB AF952 DH53F I5PG1 4G 28P 8L HDMI	255@/CHG@/CMC@/CNVI@/FP@/G0@/I5@/IOAC@/LDO@/SATARD@/TYPEC@/V15@/VGA@/X76@

BOARD ID Table

Board ID	PCB Revision	Board ID	PCB Revision
0	2050 Rev0.1	10	
1	2050 Rev0.2	11	
2	2050 Rev0.3	12	
3	2050 Rev1.0/1A	13	
4	2060 Rev0.1	14	
5	2060 Rev0.2	15	
6	2060 Rev0.3	16	
7	2060 Rev1.0	17	
8		18	
9		19	

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Title: Notes List

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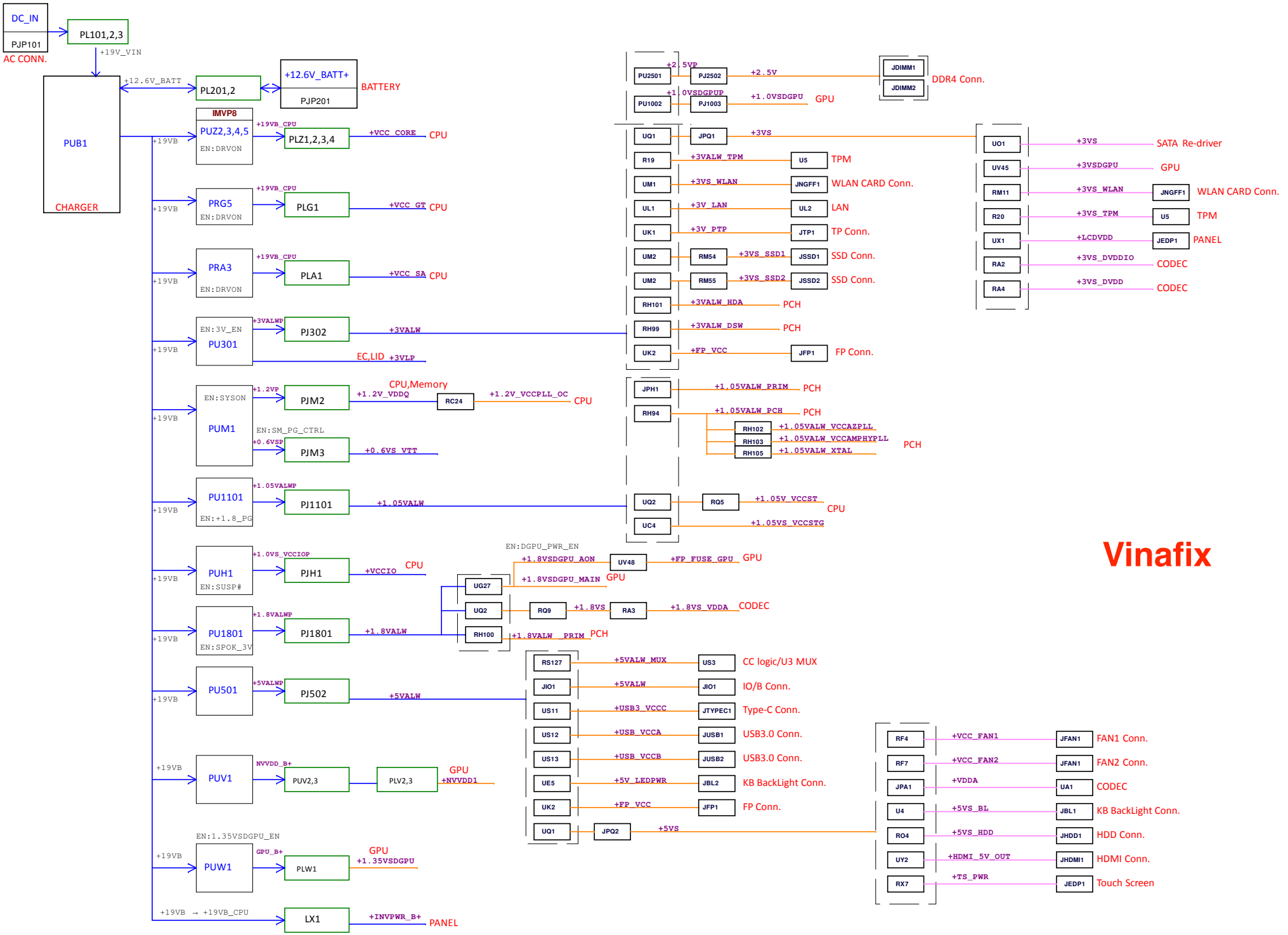
Date: Friday, February 22, 2019 | Sheet 3 of 101



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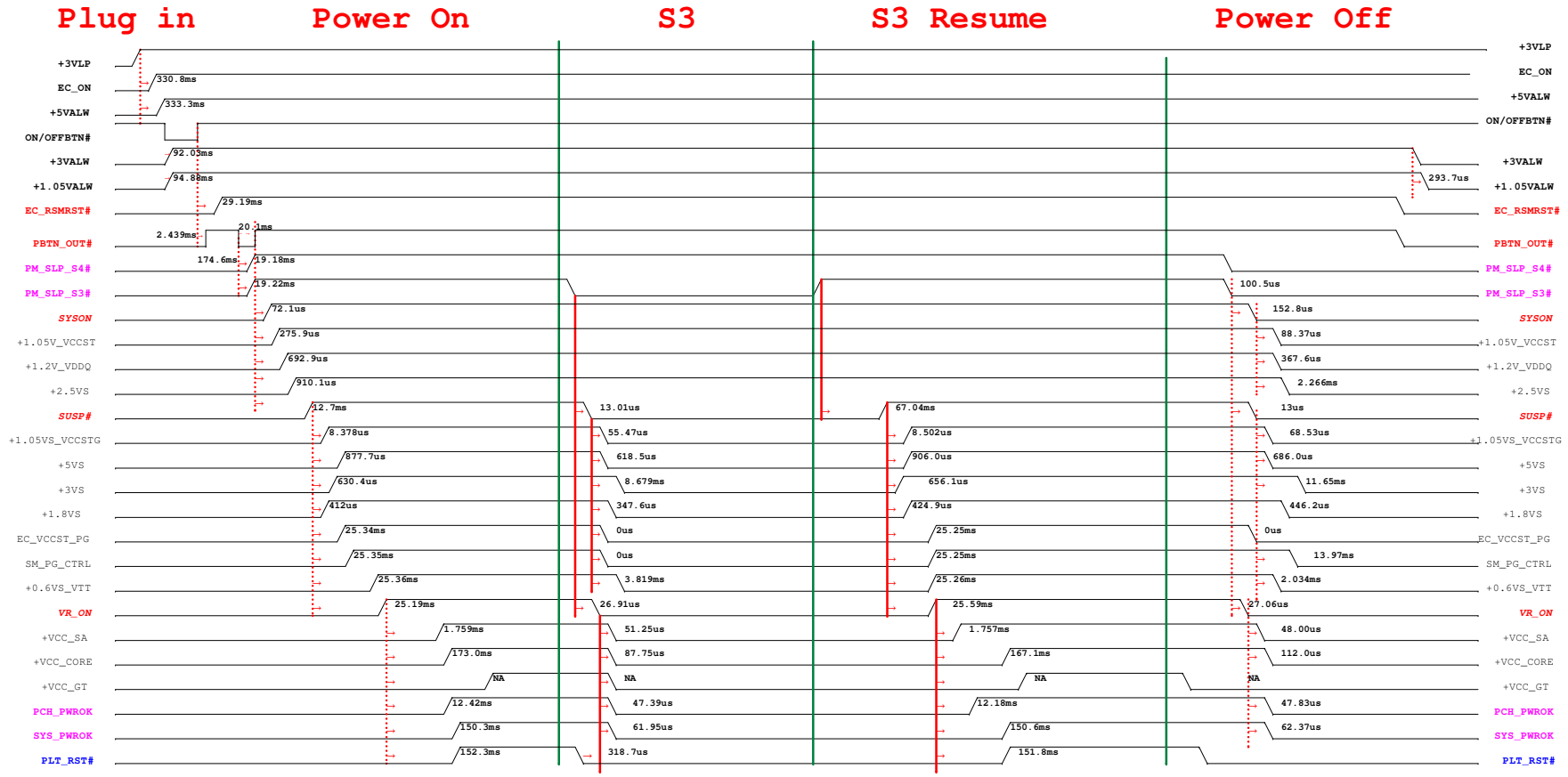
			Date: Friday, February 23, 2018 Sheet 4 of 50

DH5VF_EVT Power Sequence AC mode

BIOS ver: V0.02W1
EC: ver: V002AT04



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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 5 of 101

ZZZ
PCB10@

PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700100

ZZZ1
PCB1A@

PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700101

Coffee Lake-H CPU SKU

UC1
I5@

S IC CL8068403373522 SR3Z0 U0 2.3G ABO!
SA0000BPJ40

UC1
I5RQS@

S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00

UC1
I7@

S IC CL8068403359524 SR3YY U0 2.2G ABO!
SA0000BPZ40

UC1
I7RQS@

S IC CL8068404121817 QRR2 U0 2.6G FCBGA 1440
SA0000COF10

UC1
I5QS@

S IC CL8068403373522 QP89 U0 2.3G BGA
SA0000BPJ10

Cannon Lake PCH SKU

UH1
PCH@

S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!
SA0000BVP10

UH1
PCHQS@

S IC FHHM370 QNYF B0 BGA 874P PCH-H
SA0000BPF10

NV GPU SKU

UV1
N17P@

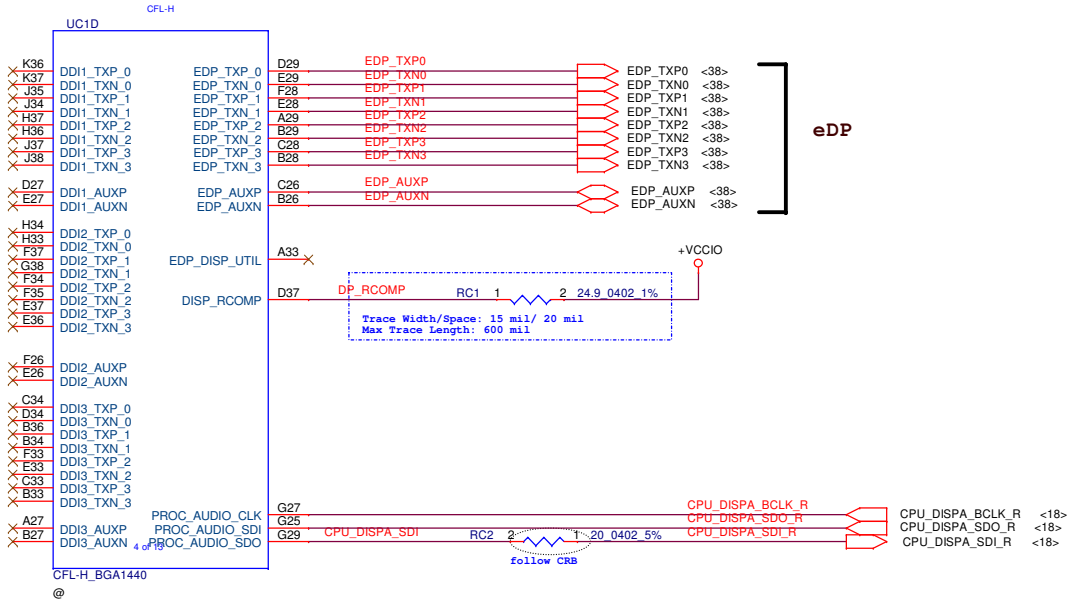
S IC N17P-G0-K1-A1 FCBGA 908P GPU ABO !
SA0000CFM20

UV1
N18PQS@

S IC N18P-G0-A1 QS FCBGA 960P GPU ABO !
SA0000CK210

UV1
N18PMP@

S IC N18P-G0-MP-A1 FCBGA 960P GPU ABO !
SA0000CK230



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Title: CFL-H(1/8)DDI/eDP

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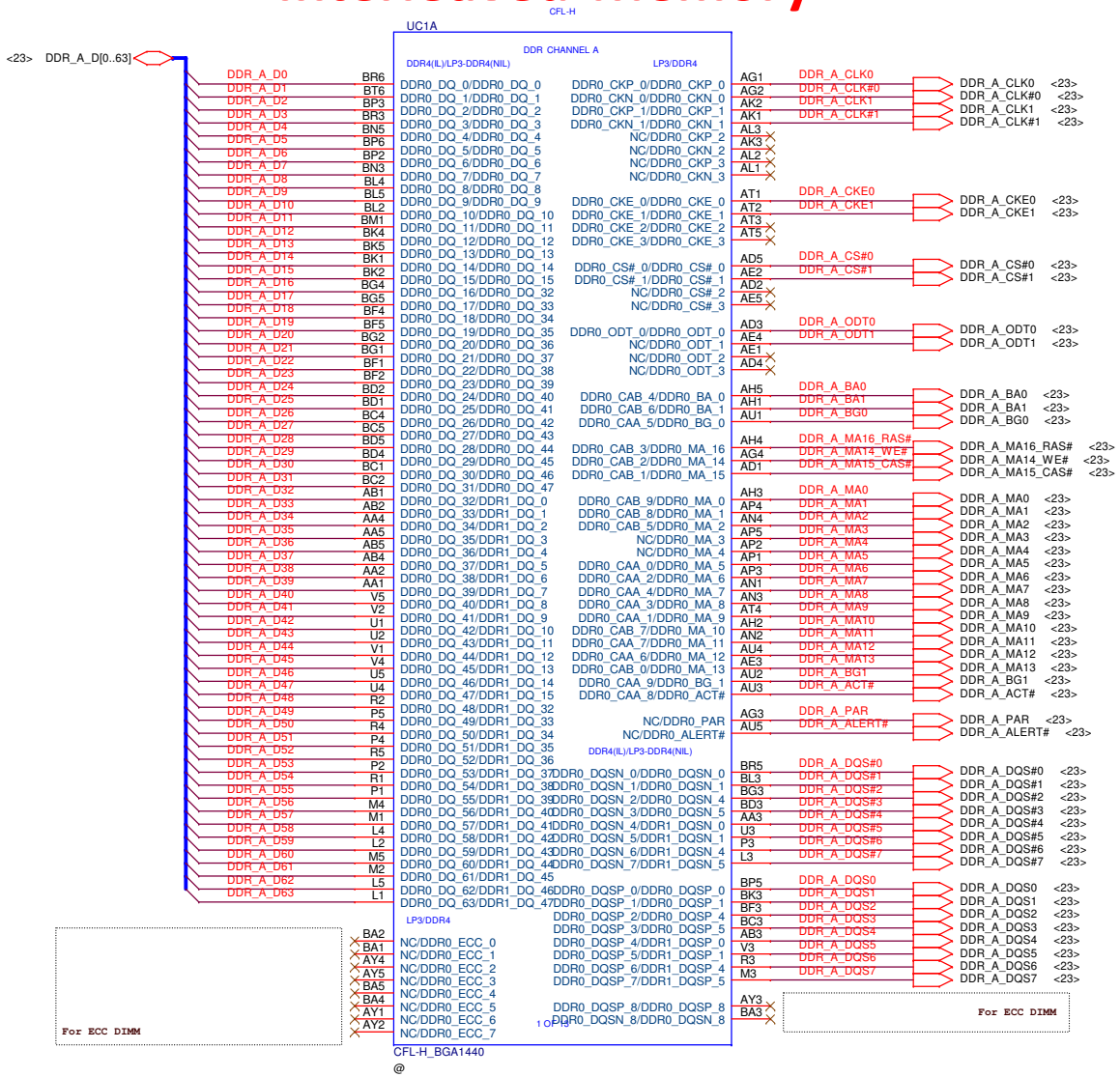
Date: Friday, February 22, 2019 | Sheet 6 of 101

CHANNEL-A

Interleaved Memory



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Compal Electronics, Inc.

Title: CFL-H(2/8)DIMMA

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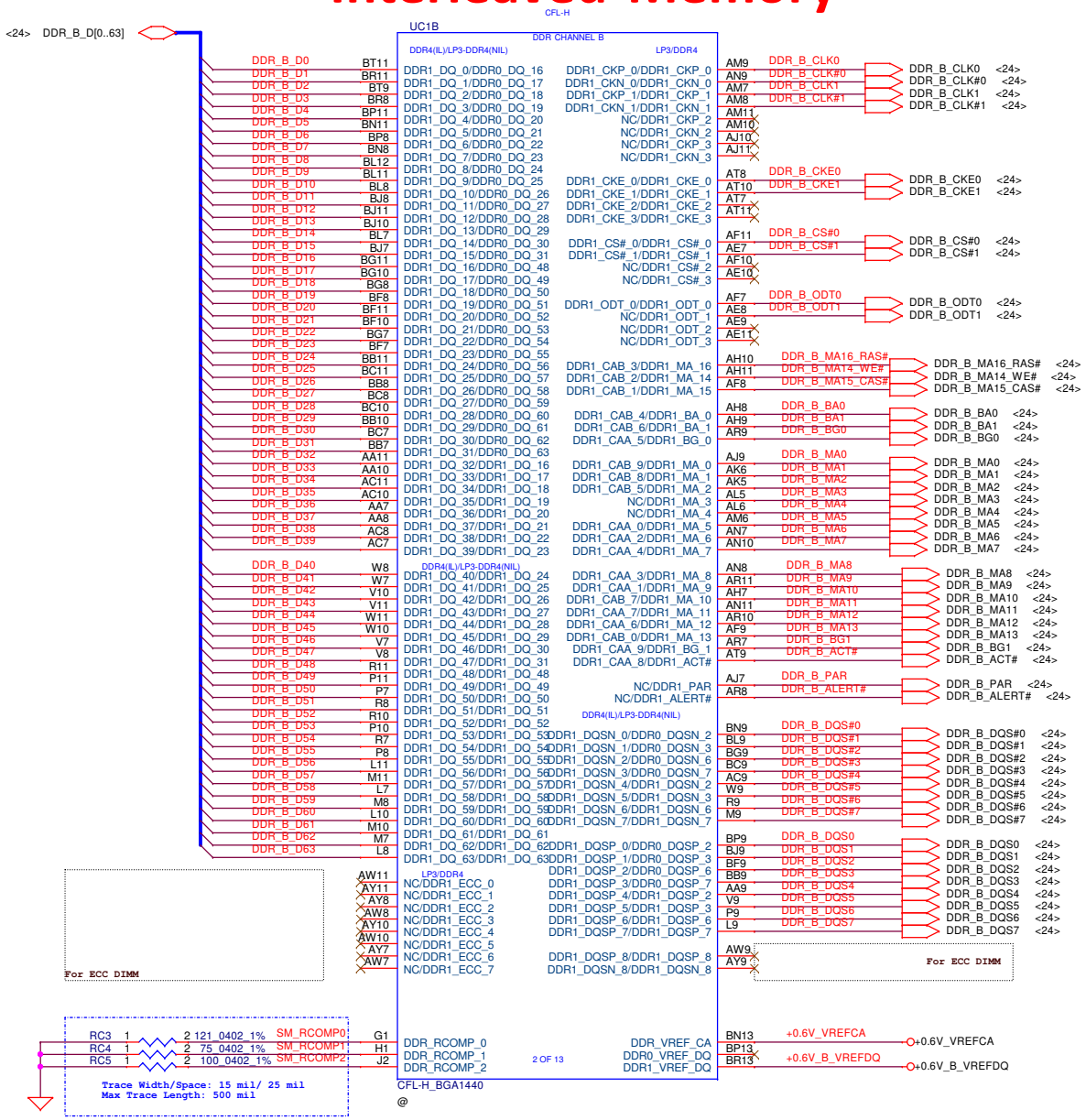
Date: Friday, February 22, 2019 | Sheet 7 of 101

CHANNEL-B

Interleaved Memory



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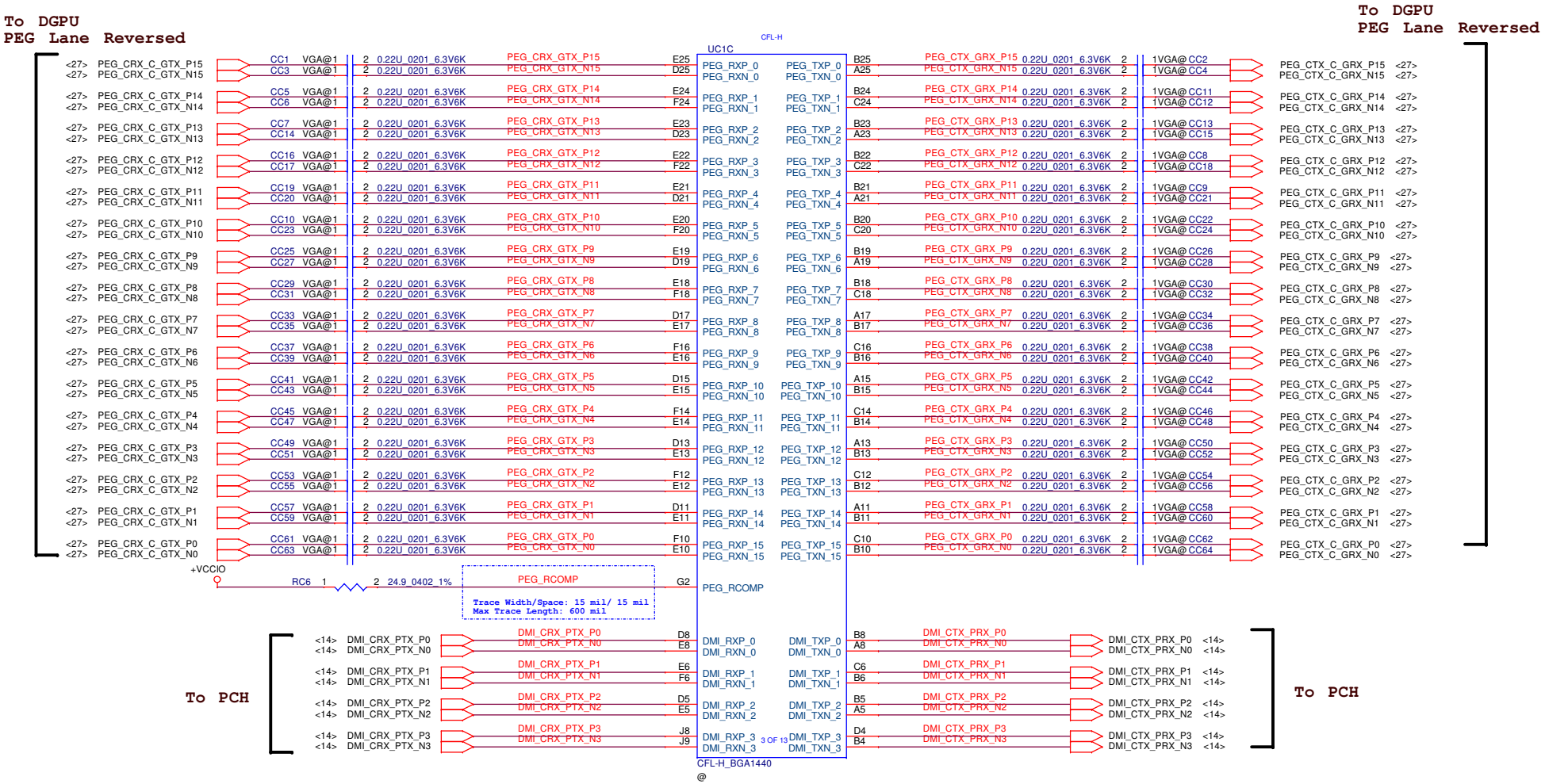
Title	CFL-H(3/8)DIMMB		
Size	Document Number		Rev
Custom	EH5VF M/B LA-H501P		1A
Date:	Friday, February 22, 2019	Sheet 8 of 101	

PEG&DMI



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Title: PEG/DMI			
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 9 of 101		

571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

CFL-H
UC1E
5 OF 13
CFL-H_BGA1440

PCH_CPU_BCLK_P / PCH_CPU_BCLK_N → BCLKP (B31) / BCLKN (A32)
PCH_CPU_PCIBCLK_P / PCH_CPU_PCIBCLK_N → PCI_BCLKP (D35) / PCI_BCLKN (C36)
PCH_CPU_24M_CLK_P / PCH_CPU_24M_CLK_N → CLK24P (E31) / CLK24N (D31)
CPU_SVID_ALERT# → VIDALERT# (BH31)
CPU_SVID_CLK → VIDSCK (BH32)
CPU_SVID_DAT → VIDSOUT (BH29)
H_PROCHOT#_R → PROCHOT# (BR30)
DDR_PG_CTRL → DDR_VTT_CNTL (BT13)
EC_VCCST_PG → VCCST_PWRGD (H13)
H_CPUPWRGD → PROCPWRGD (BT31)
H_PLTRST_CPU# → RESET# (BP35)
H_PM_SYNC_R → PM_SYNC (BM34)
H_PM_DOWN → PM_DOWN (BP31)
H_PECI → PECI (BT34)
H_THERMTRIP# → THERMTRIP# (J31)
SKTOCC# → SKTOCC# (BR33)
CATERR# → CATERR# (BM30)
PROC_SELECT# (BN1)
ZVM# (AT13, AW13)
MSM# (AU13, AY13)
RSVD1, RSVD2

CFG_0 (BN25) … CFG_19 (BN22) → CFG0 … CFG7
BPM#_0 (BR27) … BPM#_3 (BT30) → XDP_BPM#0 … XDP_BPM#3 → TC1 … TC4
PROC_TDO (BT28), PROC_TDI (BL32), PROC_TMS (BP28), PROC_TCK (BR28) → CPU_XDP_TDO, CPU_XDP_TDI, CPU_XDP_TMS, CPU_XDP_TCK0
PROC_TRST# (BP30), PROC_PREQ# (BL30), PROC_PRDY# (BP27) → CPU_XDP_TRST#, XDP_PREQ#, XDP_PRDY# → TC19, TC20
CFG_RCOMP (BT25) → CFG_RCOMP, RC18 49.9_0402_1%

CFG0 RC7 … CFG7 RC12 1K_0402_5%

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
* 0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

To be confirm

Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

Sensitive
Sensitive

1000P_0402_50V7K PGESD@ CC95 … CC103
XESD@ CC99
0.1U_0201_10V6K XESD@ CC65 H_CPUPWRGD
1000P_0402_50V7K ESD@ CC66 H_PROCHOT#_R
0.1U_0201_10V6K XESD@ CC67 H_THERMTRIP#
1000P_0402_50V7K ESD@ CC68 EC_VCCST_PG

Near CPU side
follow 1050 Request
8/21

+1.05V_VCCST
RH1 1K_0402_5% H_THERMTRIP#

PROC_SELECT# should be unconnected on CFL processor
EDS1.2 8/21

+1.2V_VDDQ
CC69 0.1U_0201_10V6K
UC3 74AUP1G07SE-7_SOT353-5
DDR_PG_CTRL → SM_PG_CTRL <85>
+3VS
RC23 330K_0402_5%

PU 330K follow CRB
8/21

+1.05VS_VCCSTG
Place to CPU side
RC76 CMC@ 51_0402_5% CPU_XDP_TMS
RC77 CMC@ 51_0402_5% CPU_XDP_TDI
RC78 CMC@ 51_0402_5% CPU_XDP_TDO
Place to CPU side
RC79 CMC@ 51_0402_5% CPU_XDP_TCK0
RC80 51_0402_5% PCH_JTAG_TCK1 → PCH_JTAG_TCK1 <18>
RC81 51_0402_5% CPU_XDP_TRST#

+1.05VS_VCCSTG
RC21 1K_0402_5%
<58,83> H_PROCHOT# → RC14 499_0402_1% H_PROCHOT#_R

+1.05V_VCCST
RC22 1K_0402_5%
<58,78> EC_VCCST_PG_R → RC151 60.4_0402_1% EC_VCCST_PG
<17> H_PM_DOWN_R → RC16 20_0402_5% H_PM_DOWN
RH2 13_0402_5%

SVID

+1.05V_VCCST
RC19 56_0402_1%
RC20 100_0402_1%
<89> CPU_SVID_ALERT#_R → RC13 220_0402_5% CPU_SVID_ALERT#
<89> CPU_SVID_DAT → CPU_SVID_DAT

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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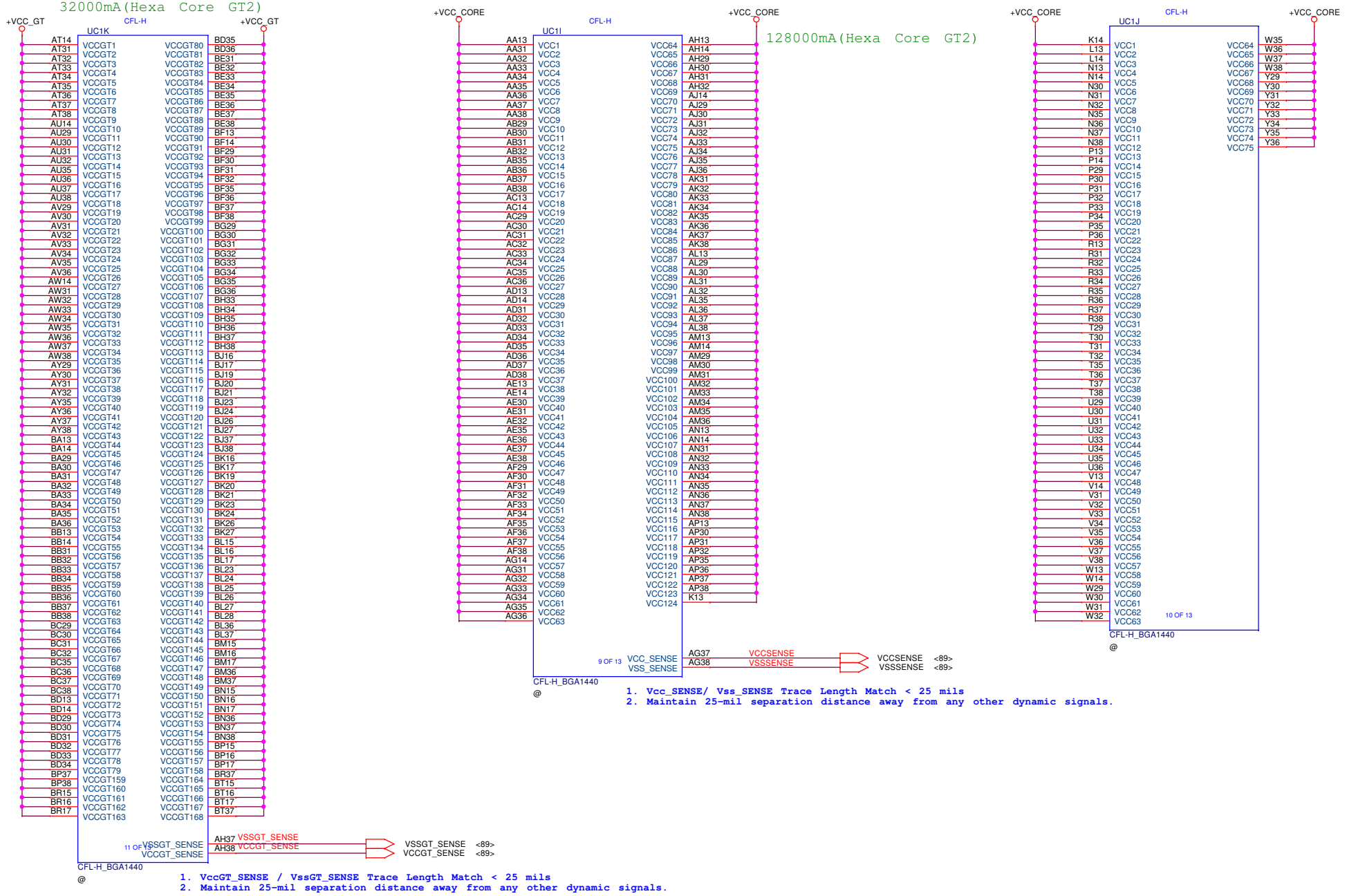
Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A
Date: Friday, February 22, 2019 | Sheet 10 of 101



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Issued Date	2017/10/30	Deciphered Date	2018/10/30

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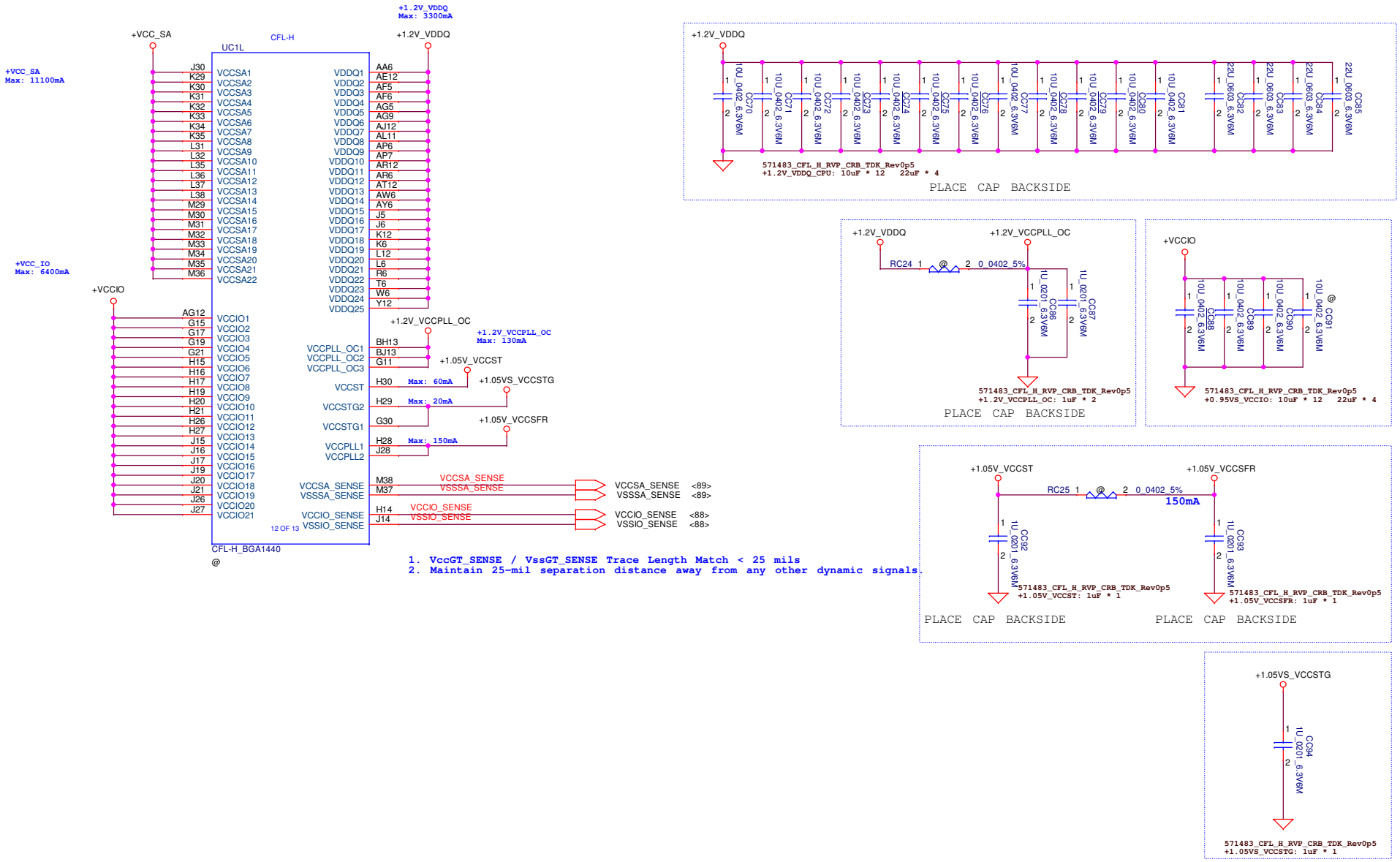
Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 11 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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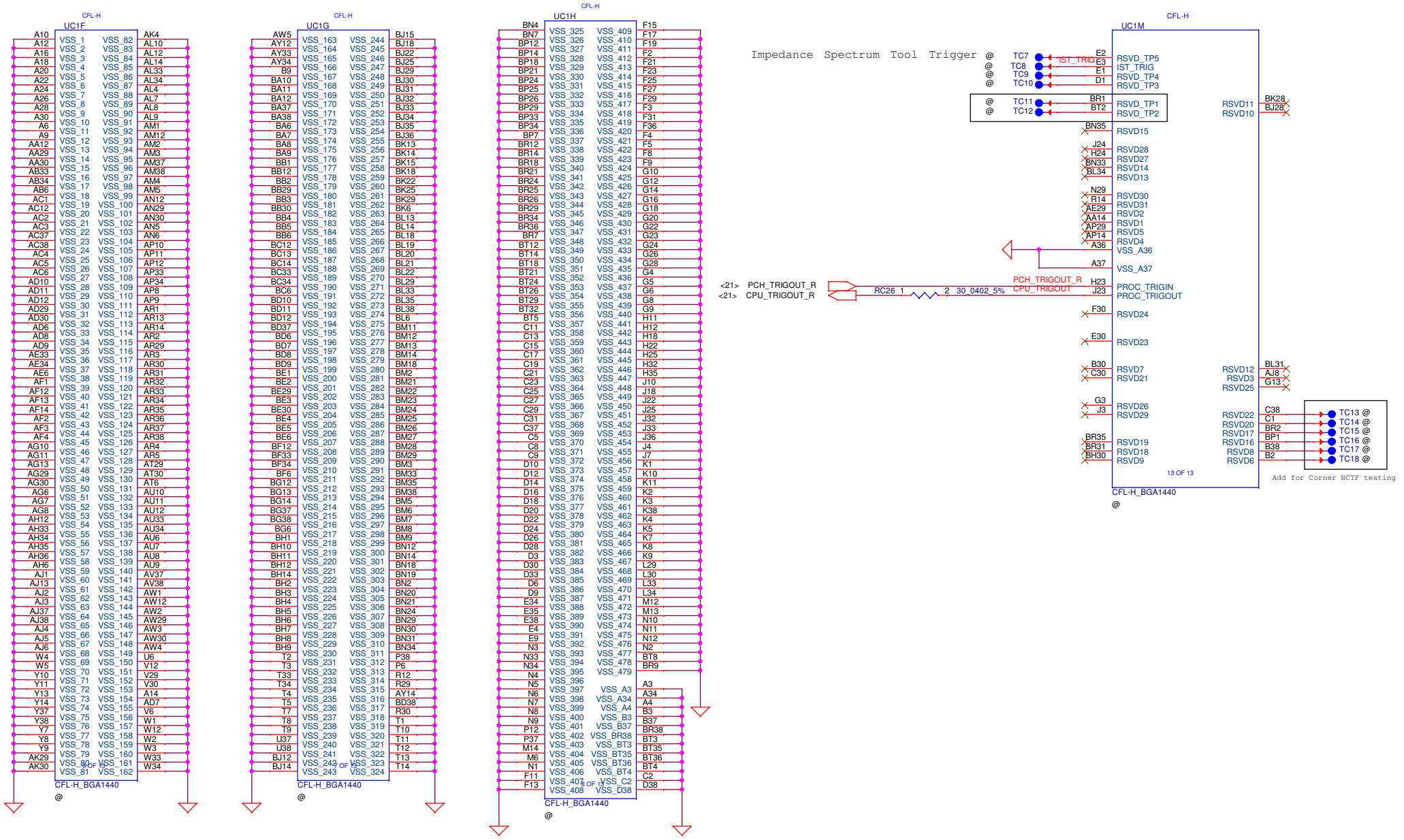
Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 12 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

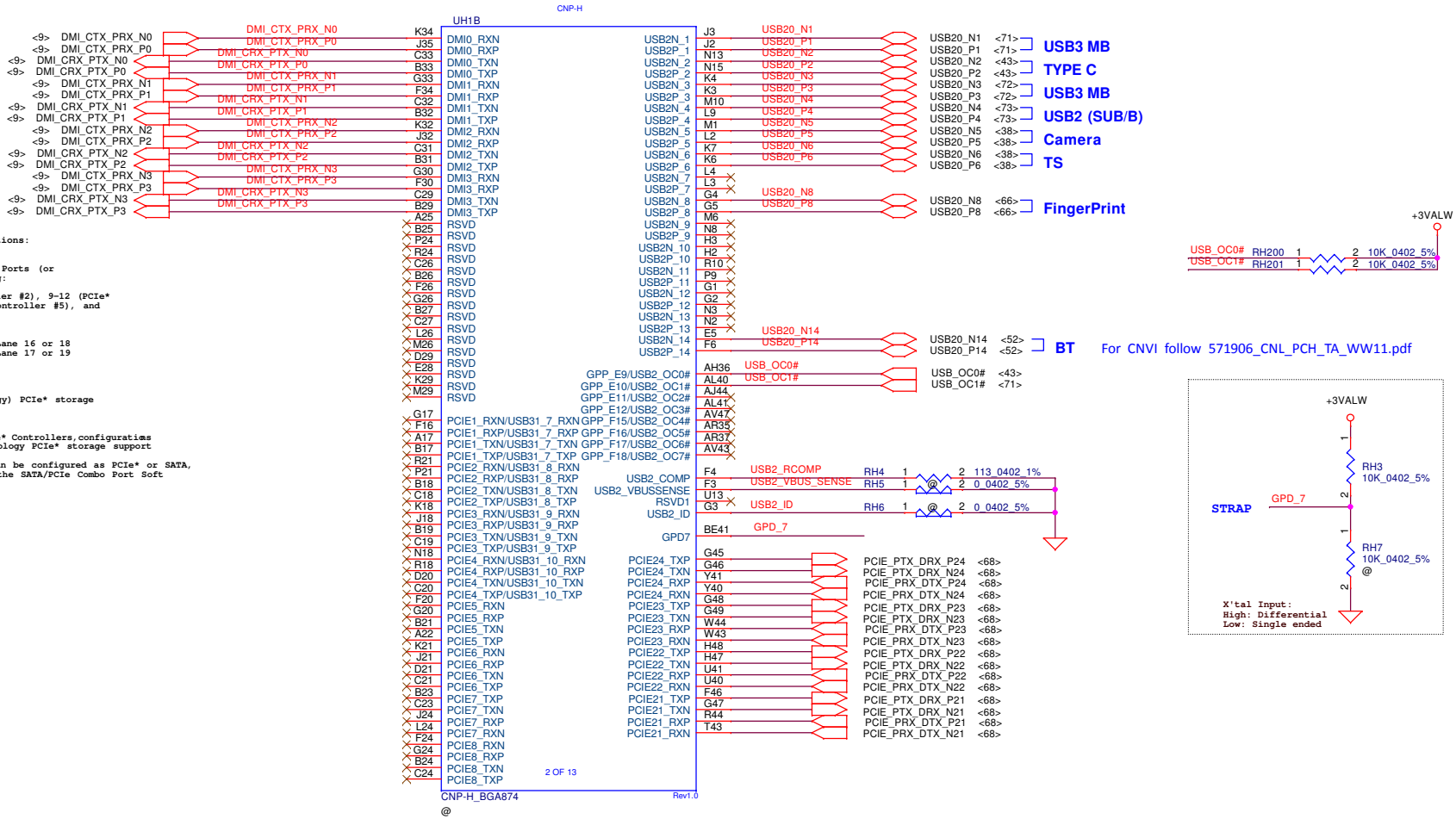
Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
Custom	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 13 of 101

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
  • When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5), and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*) " chapter for the PCH PCIe* Controllers,configuratims , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5 / GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 / GbE	PCIe* #10	PCIe* #11 / SATA 0a	PCIe* #12 / SATA 1a / GbE	PCIe* #13 / SATA 0b / GbE	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

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Issued Date	2017/10/30	Deciphered Date	2018/10/30

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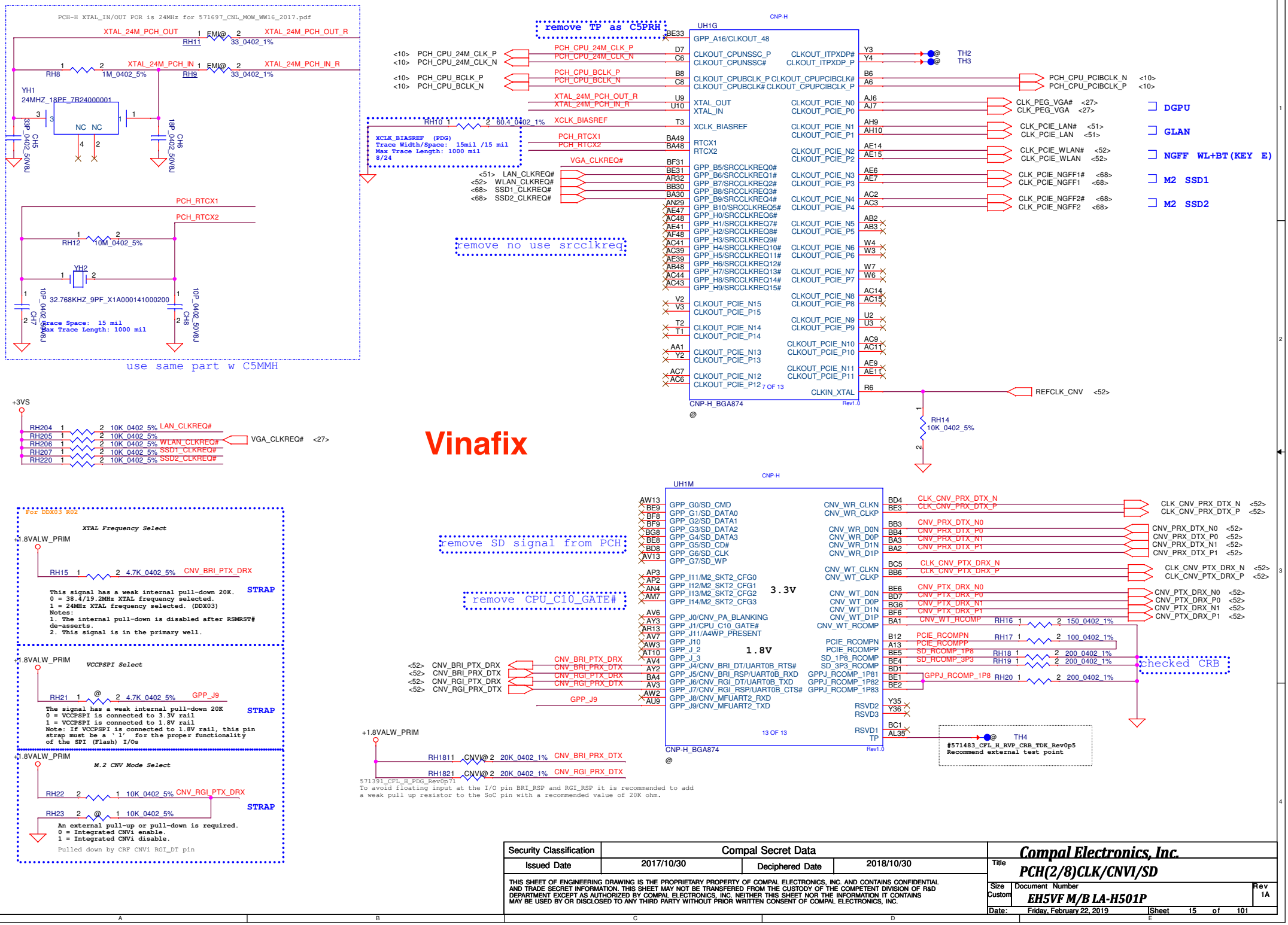
Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 14 of 101



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Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size	Document Number	Rev
Custom	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 15 of 101

no follow naming

can remove if no use DP
08/18

remove PCH DP SCLK/SDATA

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

<27,40> HDMI_HPD_PCH
<38> EDP_HPD

UH1E
CNP-H
CNP-H_BGA874
Rev1.0
5 OF 13

AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DDPD_HPD2/DISP_MISC2
AL15 GPP_I3/DDPF_HPD3/DISP_MISC3
AN6 GPP_I4/EDP_HPD/DISP_MISC4

AL13 GPP_I5/DDPB_CTRLCLK
AR8 GPP_I6/DDPB_CTRLDATA
AN13 GPP_I7/DDPC_CTRLCLK
AL10 GPP_I8/DDPC_CTRLDATA
AL9 GPP_I9/DDPD_CTRLCLK
AR3 GPP_I10/DDPD_CTRLDATA
AN40 GPP_F23/DDPF_CTRLDATA
AT49 GPP_F22/DDPF_CTRLCLK
AP41 GPP_F14/PS_ON#
M45 GPP_K23/IMGCLKOUT1
L48 GPP_K22/IMGCLKOUT0
T45 GPP_K21
T46 GPP_K20
AJ47 GPP_H23/TIME_SYNC0

remove CIO_PLUG_EVENT#

intel critical net recommend
RH1981 2 100K_0201_5%
PLT_RST# CH9 1 2 100P_0402_50V8J XESD@

<51,58> EC_PME# RH24 1 @ 2 0_0402_5% EC_PME#_R

UH1A
CNP-H
CNP-H_BGA874
Rev1.0
1 OF 13

BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
AV29 GPP_B13/PLTRST# PLT_RST# PLT_RST# <27,58,66>

R15 RSVD2
R13 RSVD1
Y47 GPP_K16/GSXCLK
Y46 GPP_K12/GSXDOUT
Y48 GPP_K13/GSXSLOAD
W46 GPP_K14/GSXDIN
AA45 GPP_K15/GSXSRESET#

GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH.

CRB connect GND
RH1861 @ 2 0_0402_5%
TH6 @

AL37 VSS
AN35 TP

<66> PCH_SPI_SI_R RH258 1 NTPM@ 2 0_0402_5% PCH_SPI_SI
<66> PCH_SPI_SO_R RH259 1 NTPM@ 2 0_0402_5% PCH_SPI_SO
PCH_SPI_CS#0
<66> PCH_SPI_CLK_R RH260 1 NTPM@ 2 0_0402_5% PCH_SPI_CLK

AU41 SPI0_MOSI
BA45 SPI0_MISO
AY47 SPI0_CS0#
AW47 SPI0_CLK
AW48 SPI0_CS1#

AL47 GPP_E3/CPU_GP0
AM45 GPP_E7/CPU_GP1
BF32 GPP_B3/CPU_GP2
BC33 GPP_B4/CPU_GP3
TP_INT# 2 1 DH1 RB751V-40_SOD323-2 EC_TP_INT# <58,63>
+3VS
TP_INT# RH28 2 1 100K_0402_5%

PCH_SPI_IO2
PCH_SPI_IO3
AY48 SPI0_IO2
BA46 SPI0_IO3
<66> PCH_SPI_CS#2 AT40 SPI0_CS2#

AE44 GPP_H18/SML4ALERT#
AJ46 GPP_H17/SML4DATA
AE43 GPP_H16/SML4CLK
AC47 GPP_H15/SML3ALERT# GPP_H15
AD48 GPP_H14/SML3DATA
AF47 GPP_H13/SML3CLK
AB47 GPP_H12/SML2ALERT# GPP_H12
AD47 GPP_H11/SML2DATA GPP_H12 <19>
AE48 GPP_H10/SML2CLK

BE19 GPP_D1/SPI1_CLK/SBK1_BK1
BF19 GPP_D0/SPI1_CS#/SBK0_BK0
BF18 GPP_D3/SPI1_MOSI/SBK3_BK3
BE18 GPP_D2/SPI1_MISO/SBK2_BK2
BC17 GPP_D22/SPI1_IO3
BD17 GPP_D21/SPI1_IO2

BB44 INTRUDER# SM_INTRUDER# 1M_0402_5% 2 1 RH30 +RTCVCC

RVP: 330K
A 1 M pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from Coin Cell Battery in G3 state.

* wait confirm CG7
PDG P348 quad mode support PH1K
CRB PU 20k
#571182_CFL_PCH_EDS_Rev1.0 recommend 100k
#571391_CFL_H_PDG_Rev0p71

+3VALW
RH25 2 1 1K_0402_5% PCH_SPI_IO2
RH26 2 1 1K_0402_5% PCH_SPI_IO3
RH27 2 1 1K_0402_5% PCH_SPI_SI_R
+3VALW
RH29 2 1 100K_0402_5% GPP_H15 STRAP

#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
571007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

PCH_SPI_CLK_R RH1951 @ 2 100K_0201_5%

intel critical net recommend

RH258 TPM@ 4.99_0402_1% SD034499B80
RH259 TPM@ 4.99_0402_1% SD034499B80
RH260 TPM@ 4.99_0402_1% SD034499B80

SPI ROM (16MByte)

+3VALW
UH2
PCH_SPI_CS#0 1
PCH_SPI_SO_0_R 2
PCH_SPI_IO2_0_R 3
4
/CS VCC 8
DO(IO1) /HOLD(IO3) 7
/WP(IO2) CLK 6
GND DI(IO0) 5
PCH_SPI_IO3_0_R
PCH_SPI_CLK_0_R
PCH_SPI_SI_0_R
CH10 0.1U_0201_10V6K
W25Q128FVSIQ_SO8
XMC P/N: SA0000B8400

+3VALW
PCH_SPI_CS#0 1 RH31 @ 2 4.7K_0402_5%

PCH_SPI_CLK_0_R 1 XEMI@ RH33 0_0402_5% 2
XEMI@ 1 CH12 68P_0402_50V8J 2

PCH_SPI_SI_0_R RH107 1 2 33_0402_1% PCH_SPI_SI_R
PCH_SPI_SO_0_R RH108 1 2 33_0402_1% PCH_SPI_SO_R
PCH_SPI_IO3_0_R RH109 1 2 33_0402_1% PCH_SPI_IO3
PCH_SPI_CLK_0_R RH110 1 2 33_0402_1% PCH_SPI_CLK_R
PCH_SPI_IO2_0_R RH111 1 2 33_0402_1% PCH_SPI_IO2

PCH PLTRST Buffer
RH32 1 @ 2 0_0402_5%
+3VS
CH11 0.1U_0201_10V6K
UH3
PLT_RST#
1 IN1 VCC 5
2 IN2 GND 3
OUT 4
MC74VHC1G08DFT2G_SC70-5
PLT_RST_BUF# <51,52,68>
RH199 100K_0201_5% @

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Compal Electronics, Inc.
Title: PCH(3/8)DDC/SPI
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A
Date: Friday, February 22, 2019 | Sheet 16 of 101

#571391_CFL_H_PDG_Rev0p5
- eSPI clock and eSPI data mismatched: <500 mils.
- eSPI clock and eSPI chip select mismatched: <500 mils.
- eSPI signal maximum 9 Vias
* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

USB3 MB / USB3 Type C

CNP-H UH1F

<71> USB3_PTX_DRX_N1	F9	USB31_1_TXN	1.8V (eSPI)	GPP_A1/LAD0/ESPI_IO0	BB39	LPC_AD0
<71> USB3_PTX_DRX_P1	F7	USB31_1_TXP		GPP_A2/LAD1/ESPI_IO1	AW37	LPC_AD1
<71> USB3_PRX_DTX_N1	D11	USB31_1_RXN		GPP_A3/LAD2/ESPI_IO2	AV37	LPC_AD2
<71> USB3_PRX_DTX_P1	C11	USB31_1_RXP		GPP_A4/LAD3/ESPI_IO3	BA38	LPC_AD3
<42> USB3_PTX_DRX_N2	C3	USB31_2_TXN				
<42> USB3_PTX_DRX_P2	D4	USB31_2_TXP		GPP_A5/LFRAME#/ESPI_CS0#	BE38	LPC_FRAME#
<42> USB3_PRX_DTX_N2	B9	USB31_2_RXN		GPP_A6/SERIRQ/ESPI_CS1#	AW35	TPM_SERIRQ
<42> USB3_PRX_DTX_P2	C9	USB31_2_RXP		GPP_A7/PIRQA#/ESPI_ALERT0#	BA36	LPC_PIRQA#
	C17	USB31_6_TXN		GPP_A0/RCIN#/ESPI_ALERT1#	BE39	RCIN#
	C16	USB31_6_TXP		GPP_A14/SUS_STAT#/ESPI_RESET#	BF38	ESPI_RST#
	G14	USB31_6_RXN				
	F14	USB31_6_RXP		GPP_A9/CLKOUT_LPC0/ESPI_CLK	BB36	CLK_LPC
	C15	USB31_5_TXN		GPP_A10/CLKOUT_LPC1	BB34	
	B15	USB31_5_TXP				
	J13	USB31_5_RXN		GPP_K19/SMI#	T48	
	K13	USB31_5_RXP		GPP_K18/NMI#	T47	
<72> USB3_PTX_DRX_P3	G12	USB31_3_TXP		GPP_E6/SATA_DEVSLP2	AH40	
<72> USB3_PTX_DRX_N3	F11	USB31_3_TXN		GPP_E5/SATA_DEVSLP1	AH35	SSD_DEVSLP1
<72> USB3_PRX_DTX_P3	C10	USB31_3_RXP		GPP_E4/SATA_DEVSLP0	AL48	
<72> USB3_PRX_DTX_N3	B10	USB31_3_RXN		GPP_F9/SATA_DEVSLP7	AP47	
				GPP_F8/SATA_DEVSLP6	AN37	
	C14	USB31_4_TXP		GPP_F7/SATA_DEVSLP5	AN46	
	B14	USB31_4_TXN		GPP_F6/SATA_DEVSLP4	AR47	
	J15	USB31_4_RXP		GPP_F5/SATA_DEVSLP3	AP48	
	K16	USB31_4_RXN	6 OF 13			

CNP-H_BGA874 Rev1.0 @

BB39 LPC_AD0 → LPC_AD0 <58>
AW37 LPC_AD1 → LPC_AD1 <58>
AV37 LPC_AD2 → LPC_AD2 <58>
BA38 LPC_AD3 → LPC_AD3 <58>

LPC Bus check straps
LPC : +3.3V

BE38 LPC_FRAME# → LPC_FRAME# <58>
AW35 TPM_SERIRQ → TPM_SERIRQ <58,66>
BA36 LPC_PIRQA#

BE39 RCIN#
BF38 ESPI_RST# — RH261 1 @ 2 0_0402_5% → OVRM_EN <36,58>

BB36 CLK_LPC — RH35 2 1 22_0402_5% → CLK_LPC_R <58>

+3VS
RCIN# 2 1 RH219 10K_0402_5%

AH40
AH35 SSD_DEVSLP1 → SSD_DEVSLP1 <68>
CONFIRM WITH SW

+3VS
TPM_SERIRQ 2 1 RH37 10K_0402_5%
LPC_PIRQA# 1 2 RH38 10K_0402_5%

For Intel CLINK

TH10 @ CL_CLK
TH11 @ CL_DATA
TH12 @ CL_RST#

CNP-H UH1C

	AR2	CL_CLK		PCIE9_RXN	G36	PCIE_PRX_DTX_N9
	AT5	CL_DATA		PCIE9_RXP	F36	PCIE_PRX_DTX_P9
	AU4	CL_RST#		PCIE9_TXN	C34	PCIE_PTX_DRX_N9
	P48	GPP_K8		PCIE9_TXP	D34	PCIE_PTX_DRX_P9
	V47	GPP_K9				
	V48	GPP_K10		PCIE10_RXN	K37	PCIE_PRX_DTX_N10
	W47	GPP_K11		PCIE10_RXP	J37	PCIE_PRX_DTX_P10
	L47	GPP_K0		PCIE10_TXN	C35	PCIE_PTX_DRX_N10
	L46	GPP_K1		PCIE10_TXP	B35	PCIE_PTX_DRX_P10
	U48	GPP_K2		PCIE15_RXN/SATA2_RXN	F44	PCIE_PRX_DTX_N15
	U47	GPP_K3		PCIE15_RXP/SATA2_RXP	E45	PCIE_PRX_DTX_P15
	N48	GPP_K4		PCIE_15_SATA_2_TXN	B40	PCIE_PTX_DRX_N15
	N47	GPP_K5		PCIE15_TXP/SATA2_TXP	C40	PCIE_PTX_DRX_P15
	P47	GPP_K6				
	R46	GPP_K7		PCIE16_RXN/SATA3_RXN	L41	
				PCIE16_RXP/SATA3_RXP	M40	
<68> PCIE_PTX_DRX_P11	C36	PCIE11_TXP/SATA0A_TXP		PCIE16_TXN/SATA3_TXN	B41	
<68> PCIE_PTX_DRX_N11	B36	PCIE11_TXN/SATA0A_TXN		PCIE16_TXP/SATA3_TXP	C41	
<68> PCIE_PRX_DTX_P11	F39	PCIE11_RXP/SATA0A_RXP				
<68> PCIE_PRX_DTX_N11	G38	PCIE11_RXN/SATA0A_RXN		PCIE17_RXN/SATA4_RXN	K43	SATA_PRX_DTX_N4
	AR42	GPP_F10/SATA_SCLOCK		PCIE17_RXP/SATA4_RXP	K44	SATA_PRX_DTX_P4
DGPU_PRSNT#	AR48	GPP_F11/SATA_SLOAD		PCIE17_TXN/SATA4_TXN	A42	SATA_PTX_DRX_N4
	AU47	GPP_F13/SATA_SDATAOUT0		PCIE17_TXP/SATA4_TXP	B42	SATA_PTX_DRX_P4
	AU46	GPP_F12/SATA_SDATAOUT1				
	C39	PCIE14_TXN/SATA1B_TXN		PCIE18_RXN/SATA5_RXN	P41	
	D39	PCIE14_TXP/SATA1B_TXP		PCIE18_RXP/SATA5_RXP	R40	
	D46	PCIE14_RXN/SATA1B_RXN		PCIE18_TXN/SATA5_TXN	C42	
	C47	PCIE14_RXP/SATA1B_RXP		PCIE18_TXP/SATA5_TXP	D42	
				GPP_E8/SATA_LED#	AK48	
	B38	PCIE13_TXN/SATA0B_TXN		GPP_E0/SATAXPCIE0/SATAGP0	AH41	
	C38	PCIE13_TXP/SATA0B_TXP		GPP_E1/SATAXPCIE1/SATAGP1	AJ43	SATA_GP1
	C45	PCIE13_RXN/SATA0B_RXN		GPP_E2/SATAXPCIE2/SATAGP2	AK47	
	C46	PCIE13_RXP/SATA0B_RXP		GPP_F0/SATAXPCIE3/SATAGP_3	AN47	
				GPP_F1/SATAXPCIE4/SATAGP4	AM46	
<68> PCIE_PTX_DRX_P12	E37	PCIE12_TXP/SATA1A_TXP		GPP_F2/SATAXPCIE5/SATAGP5	AM43	SATA_GP5
<68> PCIE_PTX_DRX_N12	D38	PCIE12_TXN/SATA1A_TXN		GPP_F3/SATAXPCIE6/SATAGP6	AM47	
<68> PCIE_PRX_DTX_P12	J41	PCIE12_RXP/SATA_1A_RXP		GPP_F4/SATAXPCIE7/SATAGP7	AM48	
<68> PCIE_PRX_DTX_N12	H42	PCIE12_RXN/SATA1A_RXN				
				GPP_F21/EDP_BKLTCTL	AU48	PCH_BKL_PWM
	B44	PCIE20_TXP/SATA7_TXP		GPP_F20/EDP_BKLTEN	AV46	ENBKL
	A44	PCIE20_TXN/SATA7_TXN		GPP_F19/EDP_VDDEN	AV44	PCH_ENVDD
	R37	PCIE20_RXP/SATA7_RXP				
	R35	PCIE20_RXN/SATA7_RXN		THRMTRIP#	AD3	PCH_THERMTRIP#
	D43	PCIE19_TXP/SATA6_TXP		PECI	AF2	PCH_PECI
	C44	PCIE19_TXN/SATA6_TXN		PM_SYNC	AF3	H_PM_SYNC
	N42	PCIE19_RXP/SATA6_RXP		PLTRST_CPU#	AG5	H_PLTRST_CPU#
	M44	PCIE19_RXN/SATA6_RXN	3 OF 13	PM_DOWN	AE2	H_PM_DOWN_R

CNP-H_BGA874 Rev1.0 @

M.2 SSD PCIE L3

PCIE_PRX_DTX_N9 → PCIE_PRX_DTX_N9 <68>
PCIE_PRX_DTX_P9 → PCIE_PRX_DTX_P9 <68>
PCIE_PTX_DRX_N9 → PCIE_PTX_DRX_N9 <68>
PCIE_PTX_DRX_P9 → PCIE_PTX_DRX_P9 <68>

M.2 SSD PCIE L2

PCIE_PRX_DTX_N10 → PCIE_PRX_DTX_N10 <68>
PCIE_PRX_DTX_P10 → PCIE_PRX_DTX_P10 <68>
PCIE_PTX_DRX_N10 → PCIE_PTX_DRX_N10 <68>
PCIE_PTX_DRX_P10 → PCIE_PTX_DRX_P10 <68>

NGFF WL+BT(KEY E)

PCIE_PRX_DTX_N15 → PCIE_PRX_DTX_N15 <52>
PCIE_PRX_DTX_P15 → PCIE_PRX_DTX_P15 <52>
PCIE_PTX_DRX_N15 — .1U_0402_16V7K 1 2 CH1 → PCIE_PTX_C_DRX_N15 <52>
PCIE_PTX_DRX_P15 — .1U_0402_16V7K 1 2 CH2 → PCIE_PTX_C_DRX_P15 <52>

M.2 SSD PCIE L1

<68> PCIE_PTX_DRX_P11
<68> PCIE_PTX_DRX_N11
<68> PCIE_PRX_DTX_P11
<68> PCIE_PRX_DTX_N11

HDD

SATA_PRX_DTX_N4 → SATA_PRX_DTX_N4 <67>
SATA_PRX_DTX_P4 → SATA_PRX_DTX_P4 <67>
SATA_PTX_DRX_N4 → SATA_PTX_DRX_N4 <67>
SATA_PTX_DRX_P4 → SATA_PTX_DRX_P4 <67>

GLAN

<51> PCIE_PTX_C_DRX_N14 — CH3 2 1 .1U_0402_16V7K → PCIE_PTX_DRX_N14
<51> PCIE_PTX_C_DRX_P14 — CH4 2 1 .1U_0402_16V7K → PCIE_PTX_DRX_P14
<51> PCIE_PRX_DTX_N14 → PCIE_PRX_DTX_N14
<51> PCIE_PRX_DTX_P14 → PCIE_PRX_DTX_P14

+3VS
SATA_GP1 RH39 2 1 10K_0402_5%

M.2 SSD PCIE/SATA select pin

SATA_GP1 <68>
RH187 1 PRA@ 2 10K_0402_5%
SATA_GP5 — @ TH13
CONFIRM WITH SW

M.2 SSD PCIE L0

<68> PCIE_PTX_DRX_P12
<68> PCIE_PTX_DRX_N12
<68> PCIE_PRX_DTX_P12
<68> PCIE_PRX_DTX_N12

PCH_BKL_PWM → PCH_BKL_PWM <38>
ENBKL <58>
PCH_ENVDD <38>

PCH_THERMTRIP# — RH40 1 2 620_0402_5% → PCH_THERMTRIP#_R <10>
PCH_PECI — RH41 1 @ 2 13_0402_5% → H_PECI <10,58>
H_PM_SYNC — RH42 1 2 30_0402_5% → H_PM_SYNC_R → H_PM_SYNC_R <10>
H_PLTRST_CPU# → H_PLTRST_CPU# <10>
H_PM_DOWN_R → H_PM_DOWN_R <10>

#571391_CFL_H_PDG_Rev0p5.pdf

H_PECI 0.1U_0201_10V6K 1 2 CH50 XESD@

+3VALW
RH43 10K_0402_5% UMA@
DGPU_PRSNT#
RH44 10K_0402_5% VGA@

	GPP_F13 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

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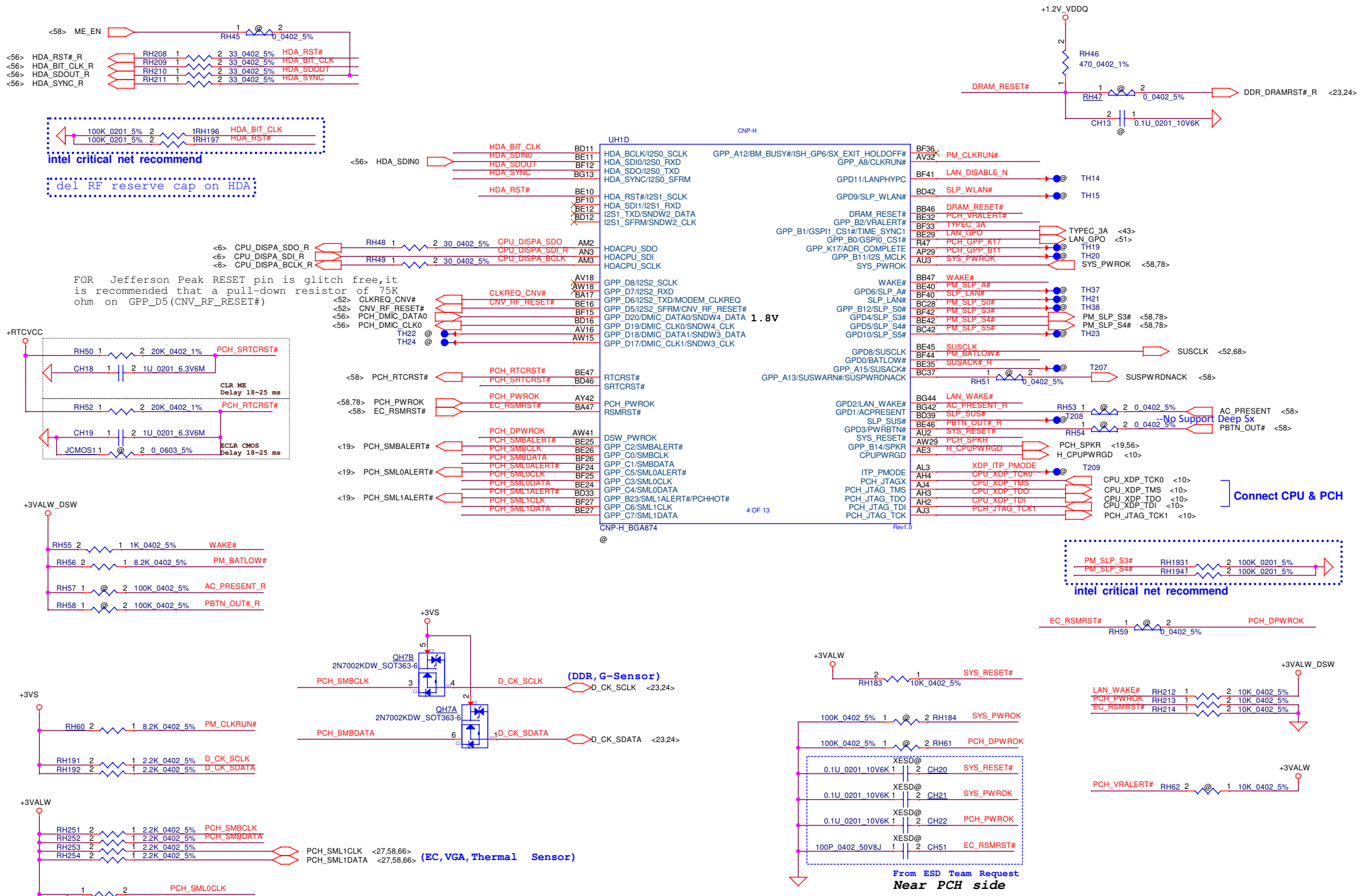
Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 17 of 101



Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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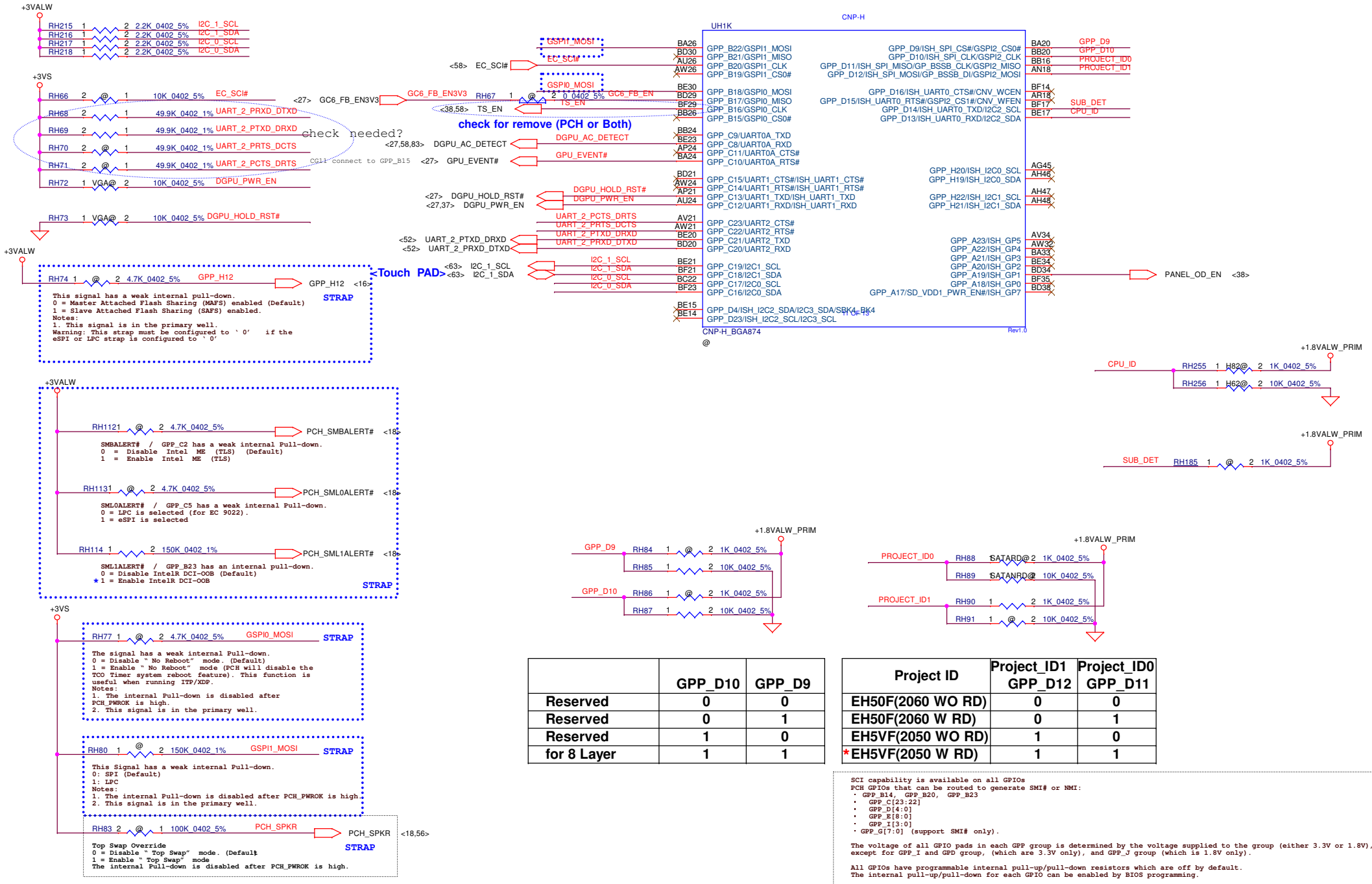
Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS/DMIC		
Size	Document Number		Rev
Custom	EH5VF M/B LA-H501P		1A
Date:	Friday, February 22, 2019	Sheet	18 of 101



	GPP_D10	GPP_D9
Reserved	0	0
Reserved	0	1
Reserved	1	0
for 8 Layer	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
EH50F(2060 WO RD)	0	0
EH50F(2060 W RD)	0	1
EH5VF(2050 WO RD)	1	0
*EH5VF(2050 W RD)	1	1

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14, GPP_B20, GPP_B23
- GPP_C[23:22]
- GPP_D[4:0]
- GPP_E[8:0]
- GPP_I[3:0]
- GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPD group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

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Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 19 of 101

GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

Place Near UH1 VCCPRIM_1_0523~29 3-5MM FROM PACKAGE EDGE

place near VCCDUSB FOR W22/W23

1-3MM FROM PACKAGE VCCPRIM_MPHY W31

1-3MM FROM PACKAGE EDGE

1-5MM FROM PACKAGE EDGE FOR VCCAPLL C1/C2

1-3MM FROM PACKAGE EDGE FOR VCCA_BCLK V19

1-5MM FROM PACKAGE EDGE FOR VCCAPLL B1/B2/B3

1-3MM FROM PACKAGE EDGE

LC filter close to pin

1uF 1-3MM FROM PACKAGE EDGE

reserve filter follow CRB 8/21

1-3MM FROM PACKAGE FOR PGPPEF AE35/AE37

1-3MM FROM PACKAGE FOR PGPPHK AC35/AC36

1-3MM FROM PACKAGE FOR VCCPRIM AY8/BB7

reserved for cnvi

near AG19/AG20

change to 10k

SP02000RO00

Vinafix

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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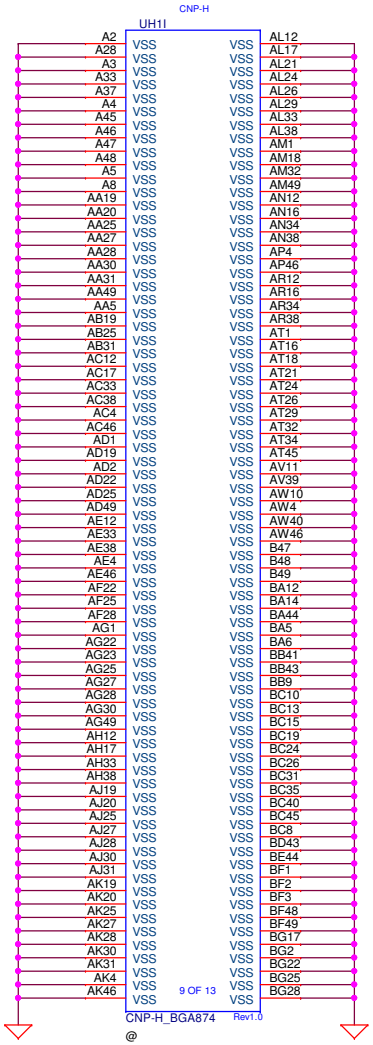
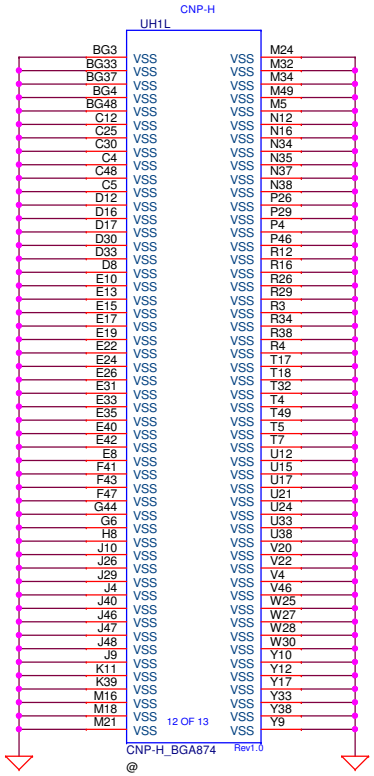
Compal Electronics, Inc.

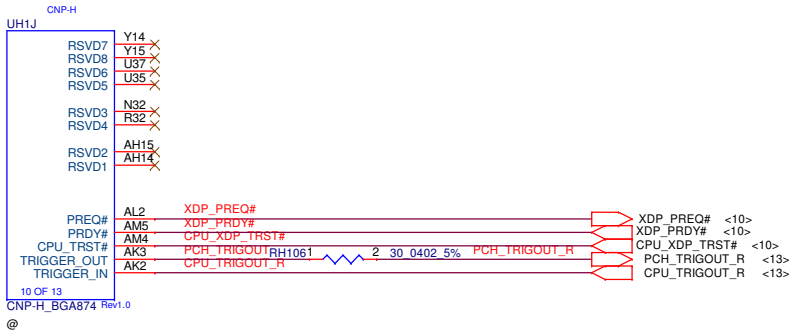
Title: PCH(7/8)Power

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 20 of 101







Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 21 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 22 of 101

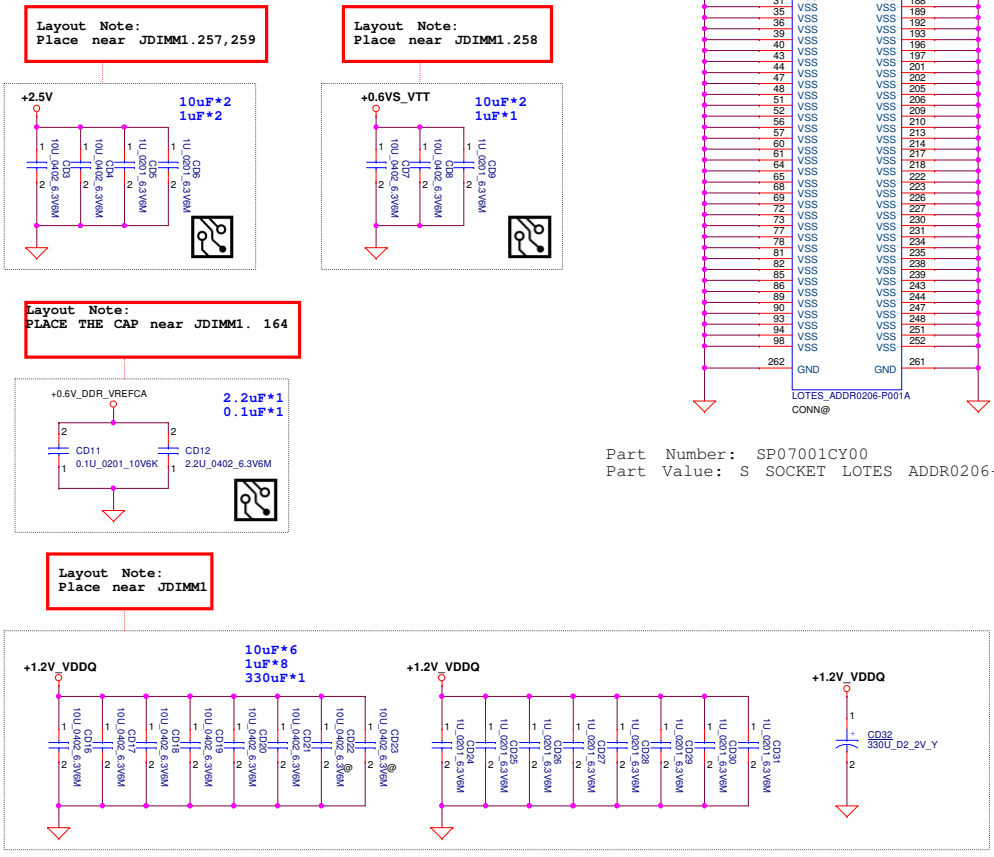
CHANNEL-A

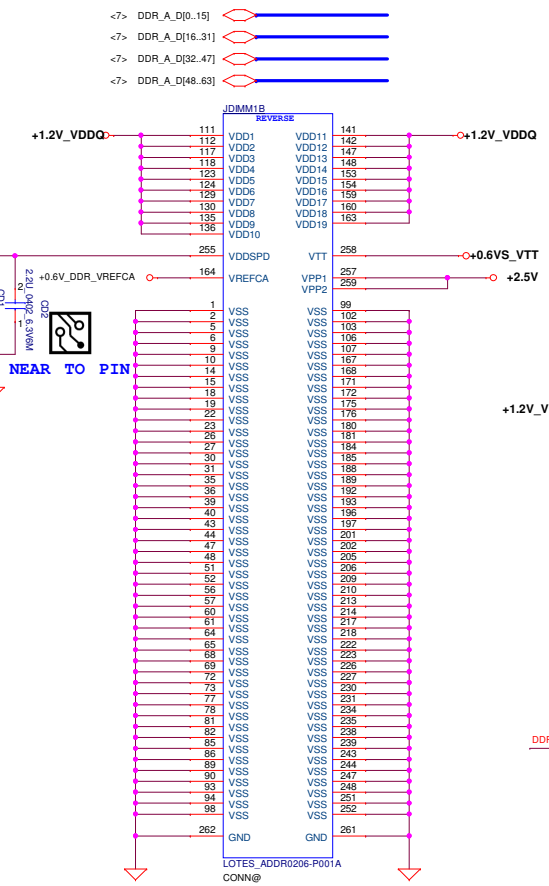
BOT REVERSE TYPE (4 mm)

Interleaved Memory

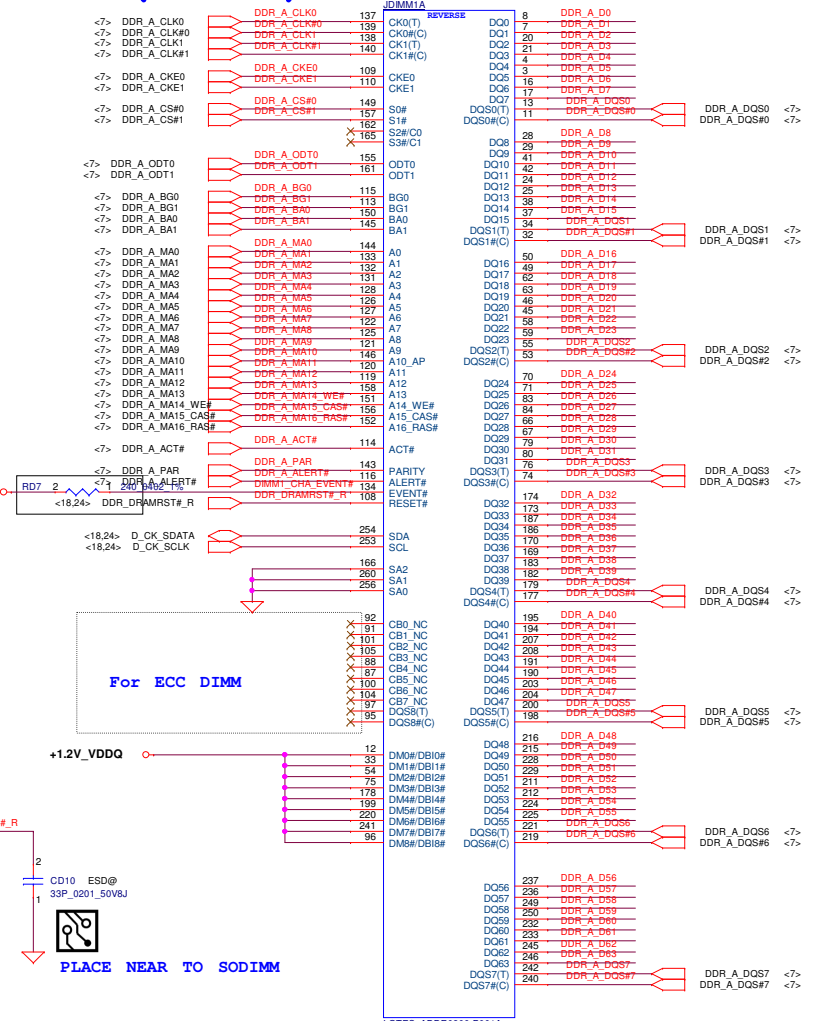
TOP: JDIMM1 CONN Non-ECC DIMM

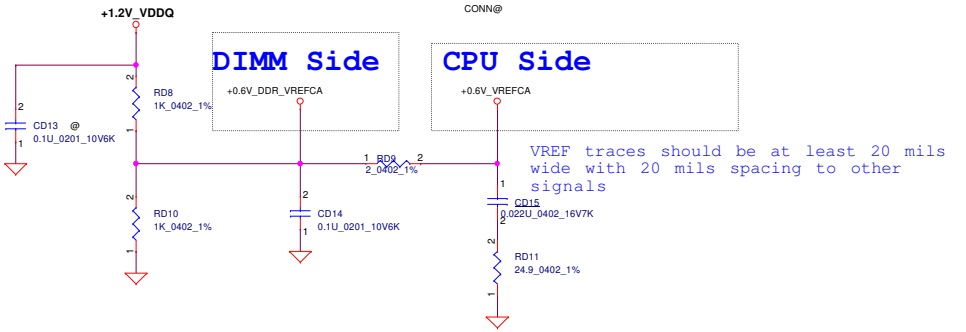
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S





Part Number: SP07001CY00
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4





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Issued Date	2017/10/30	Deciphered Date 2018/10/30

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Compal Electronics, Inc.

Title: DDRIV_CHA: DIMM0

Size | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 23 of 101

CHANNEL-B

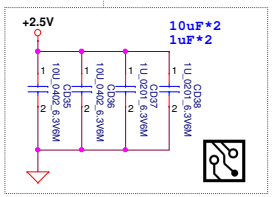
TOP: JDIMM2 CONN Non-ECC DIMM

Interleaved Memory

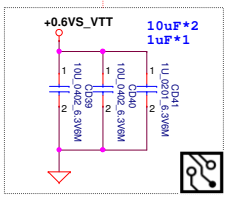
BOT STD (4 mm)

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

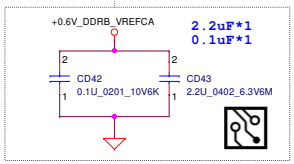
Layout Note:
Place near JDIMM3.257,259



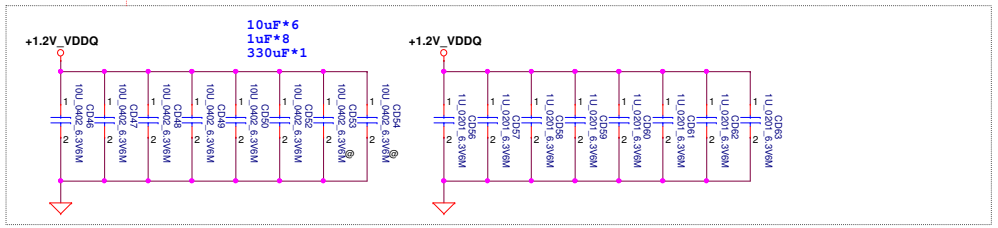
Layout Note:
Place near JDIMM3.258

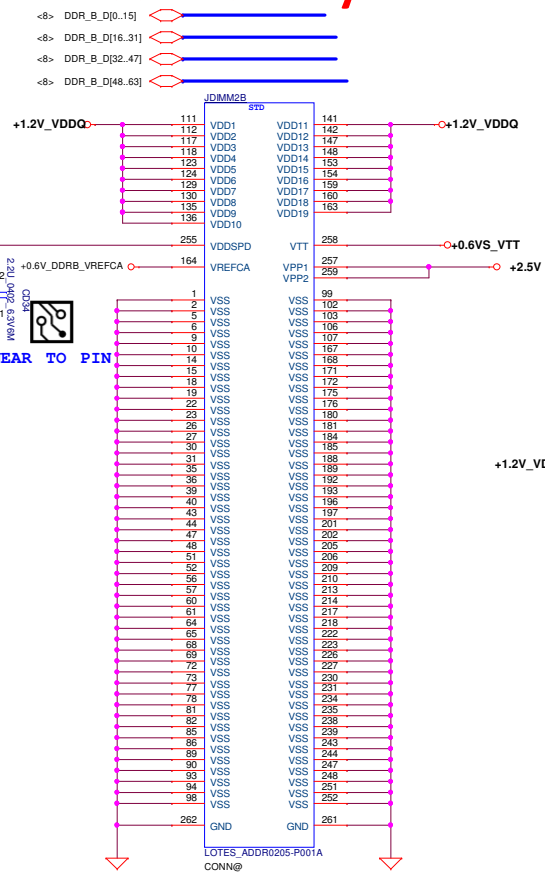


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3

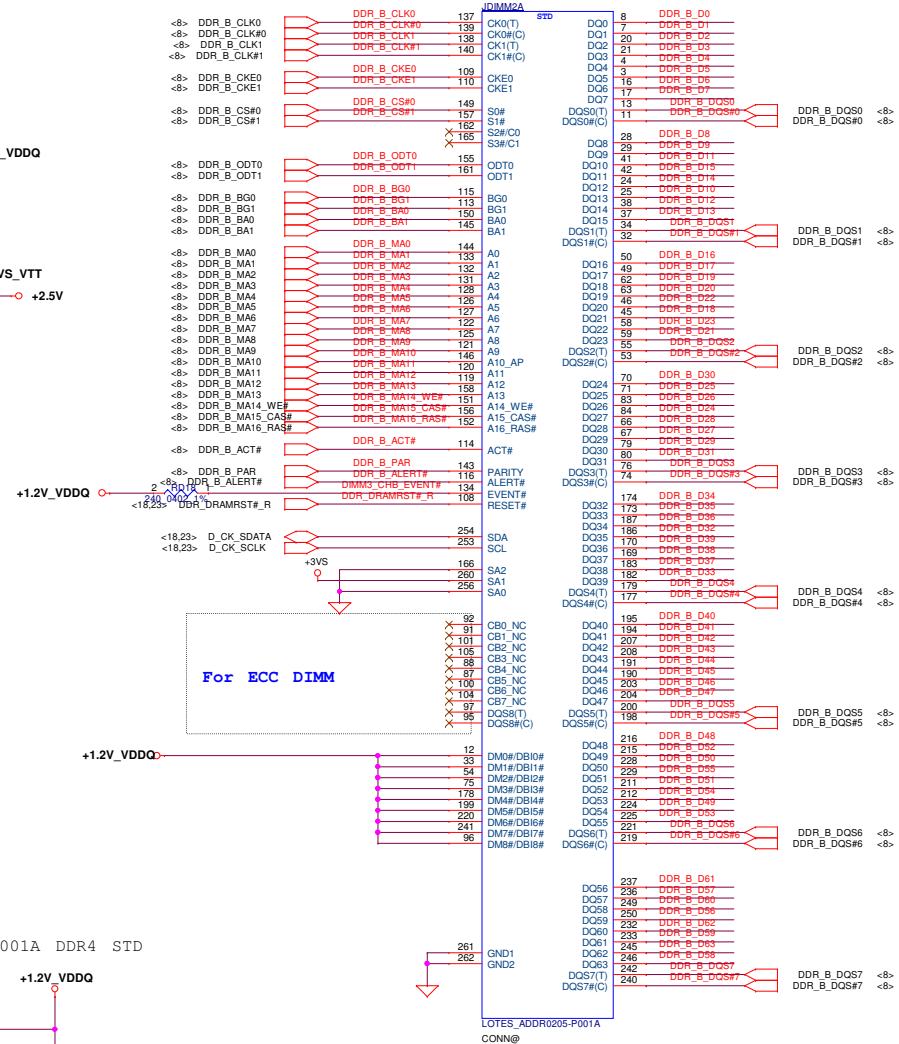


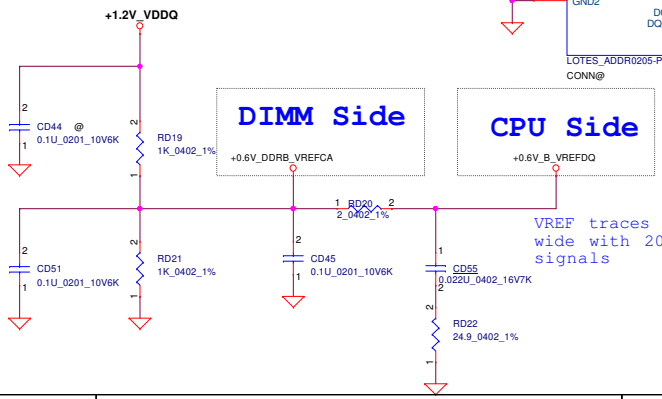
Layout Note:
Place near JDIMM3





Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD





Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size	Document Number	Rev
	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 | Sheet 24 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 25 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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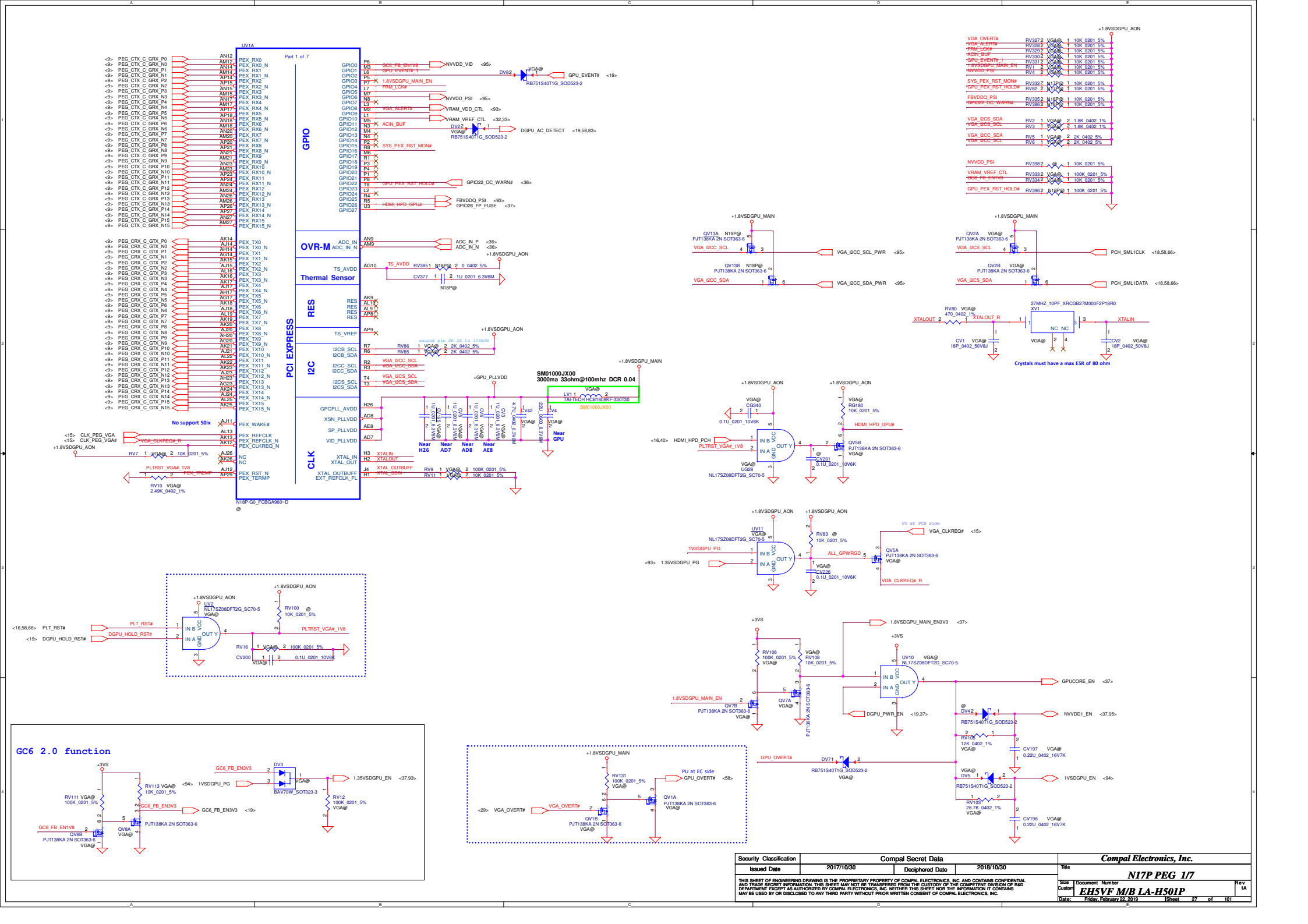
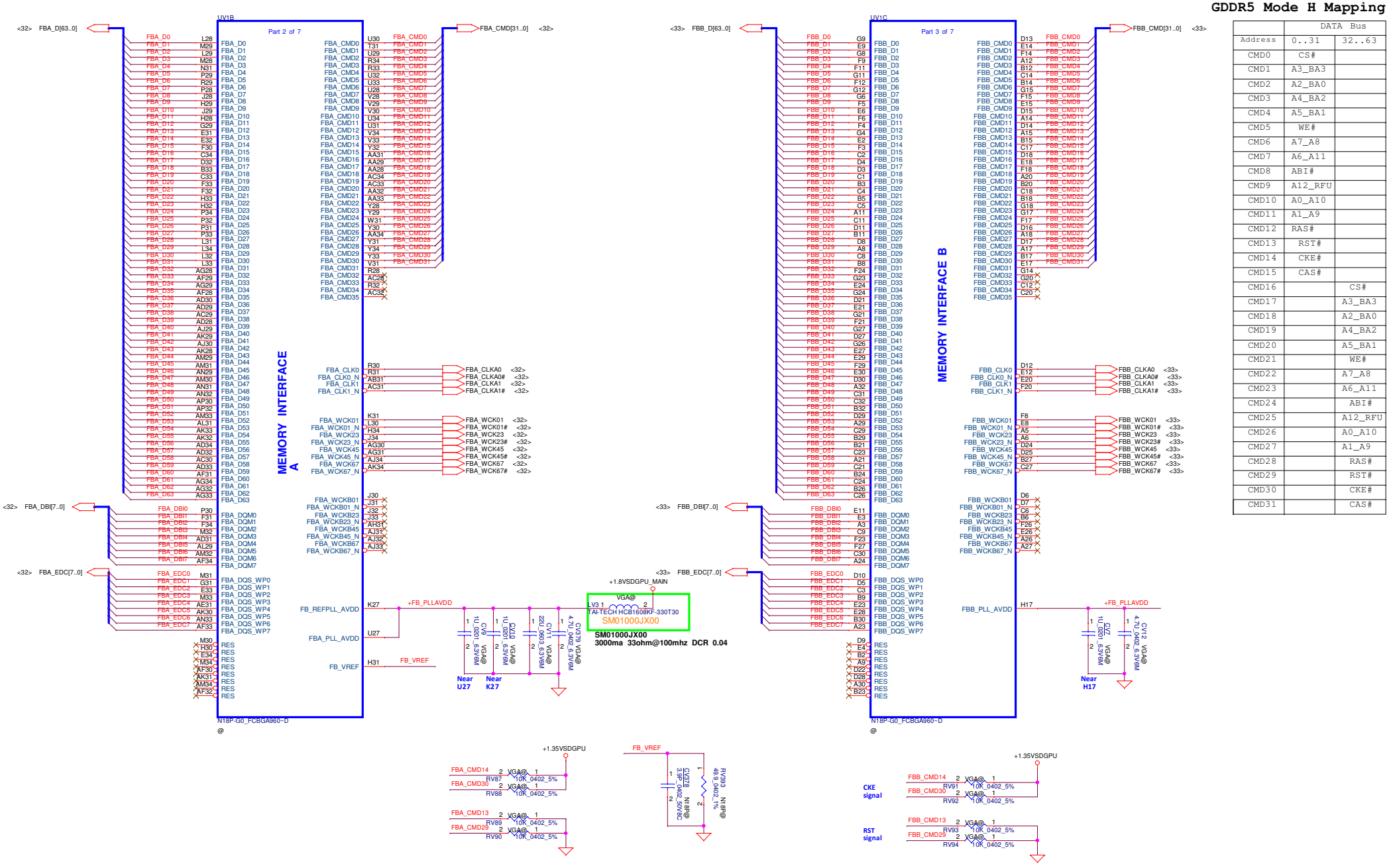
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 26 of 101


UV1A
Part 1 of 7
PCI EXPRESS
GPIO
OVR-M
Thermal Sensor
RES
I2C
CLK
N18P-G0_FCBGA960-D
SM01000JX00
3000ma 33ohm@100mhz DCR 0.04
GC6 2.0 function
Crystals must have a max ESR of 80 ohm
Compal Electronics, Inc.
N17P PEG 1/7
EH5VF M/B LA-H501P
Security Classification
Compal Secret Data
Issued Date
2017/10/30
Deciphered Date
2018/10/30
Rev 1A
Date: Friday, February 22, 2019
Sheet 27 of 101



GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Vinafix

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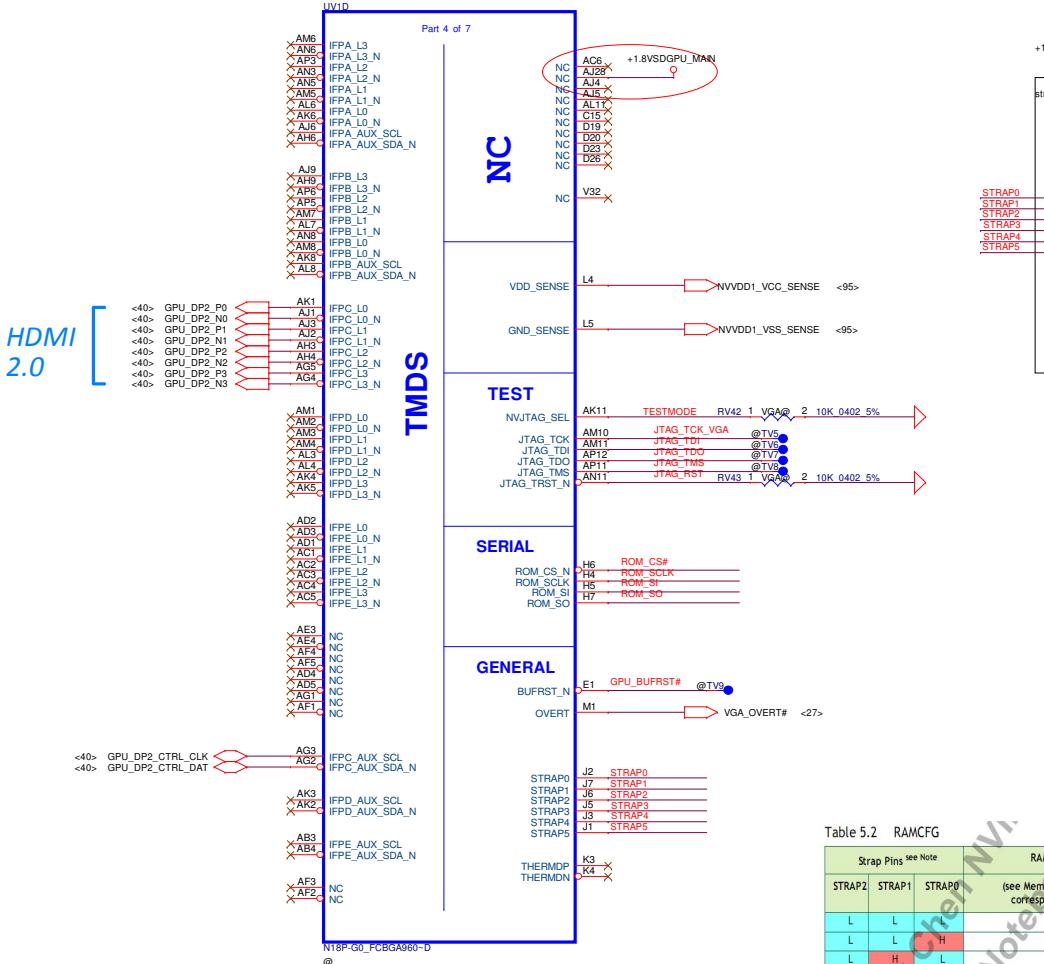
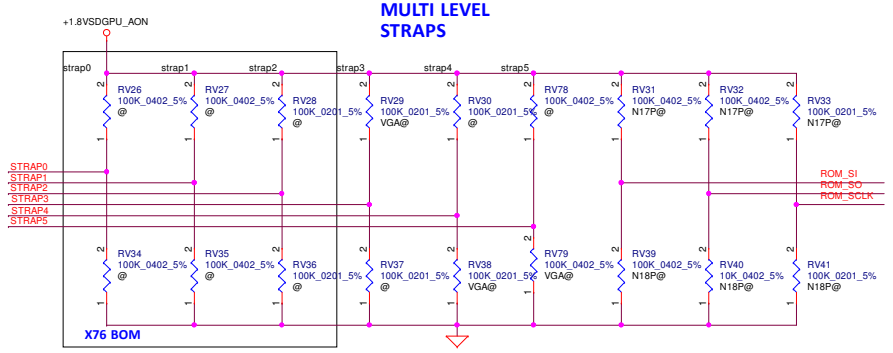
Size	Document Number		Rev
Custom	EH5VF M/B LA-H501P		1A
Date:	Friday, February 22, 2019	Sheet	28 of 101





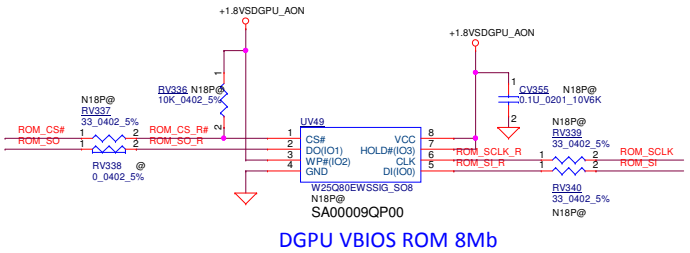


Table 3. N17P-G1/G0/G0-K1[4] GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[3]

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[2]	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

Notes:
1. For N18P-G0, the maximum allowable memory case temperature is 85 °C.
2. DVS may be required to run WCLK > 3500 MHz. TBD.

Sonny Chen NVIDIA Confidential Notebook 2016-05-03 16:2
Jeff Tu NVIDIA Confidential ACER Notebook 2018-10-24 20:4
NVIDIA Confidential Notebook 2018-09-02 10:34:

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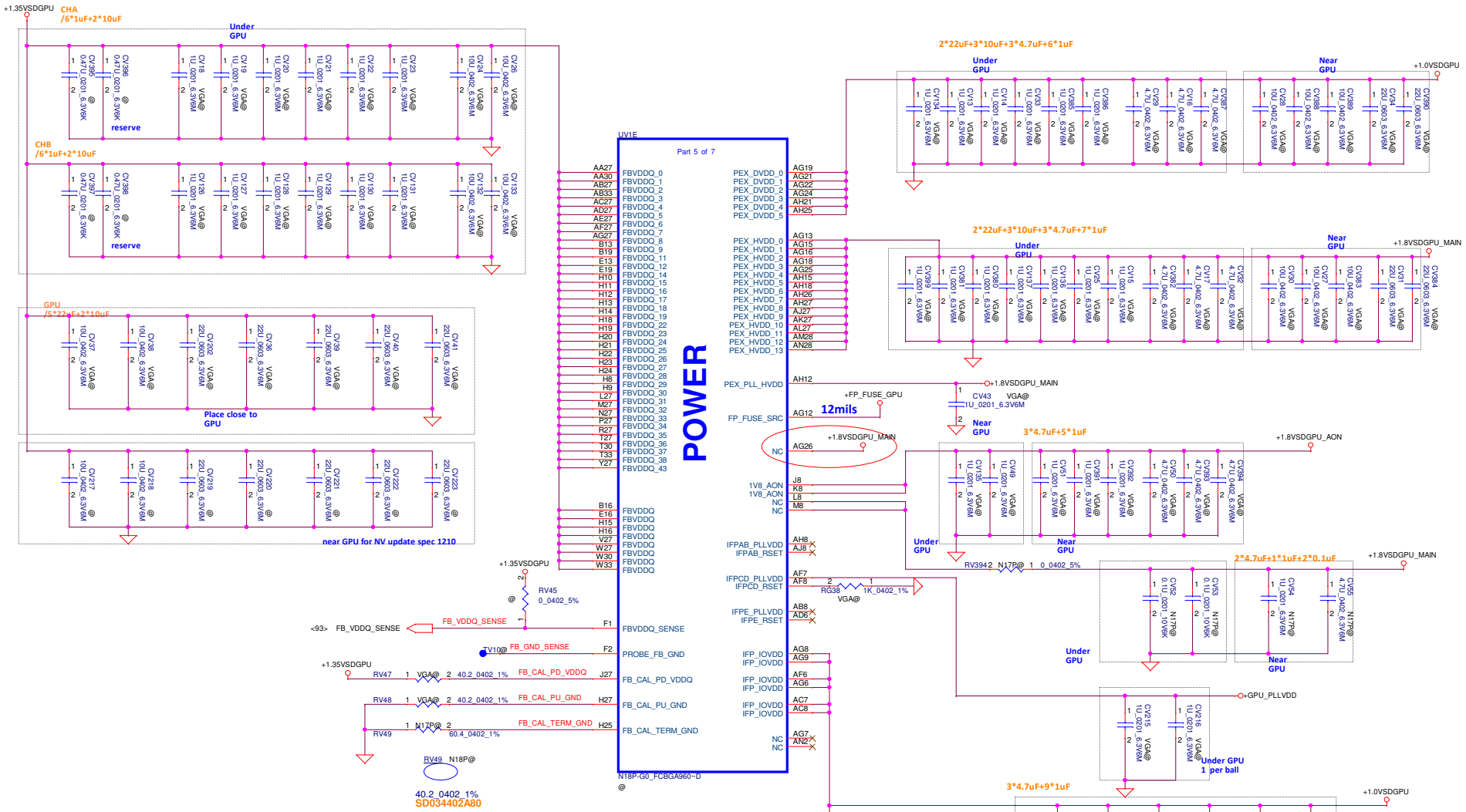
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 29 of 101



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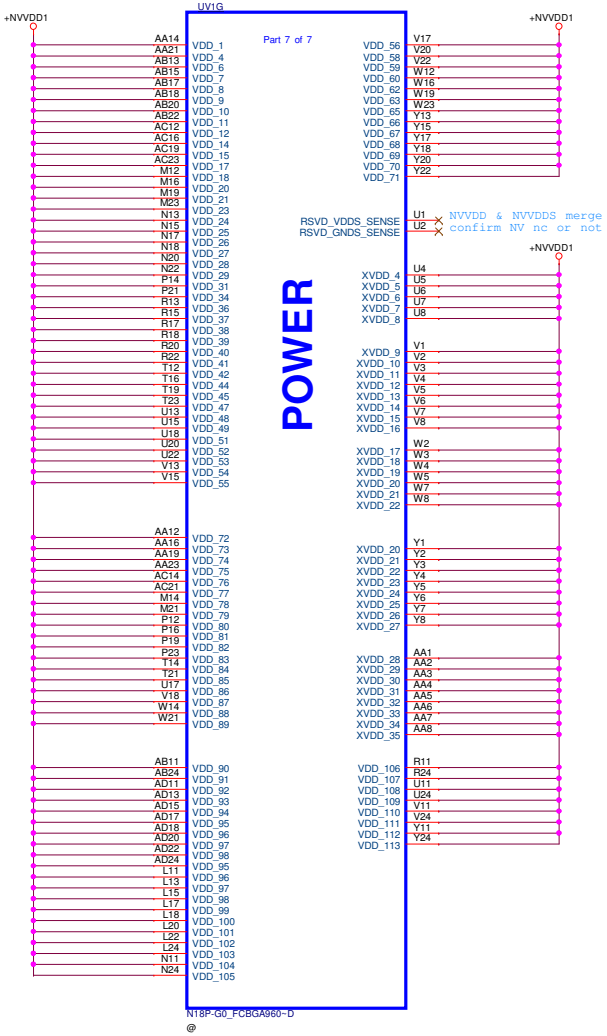
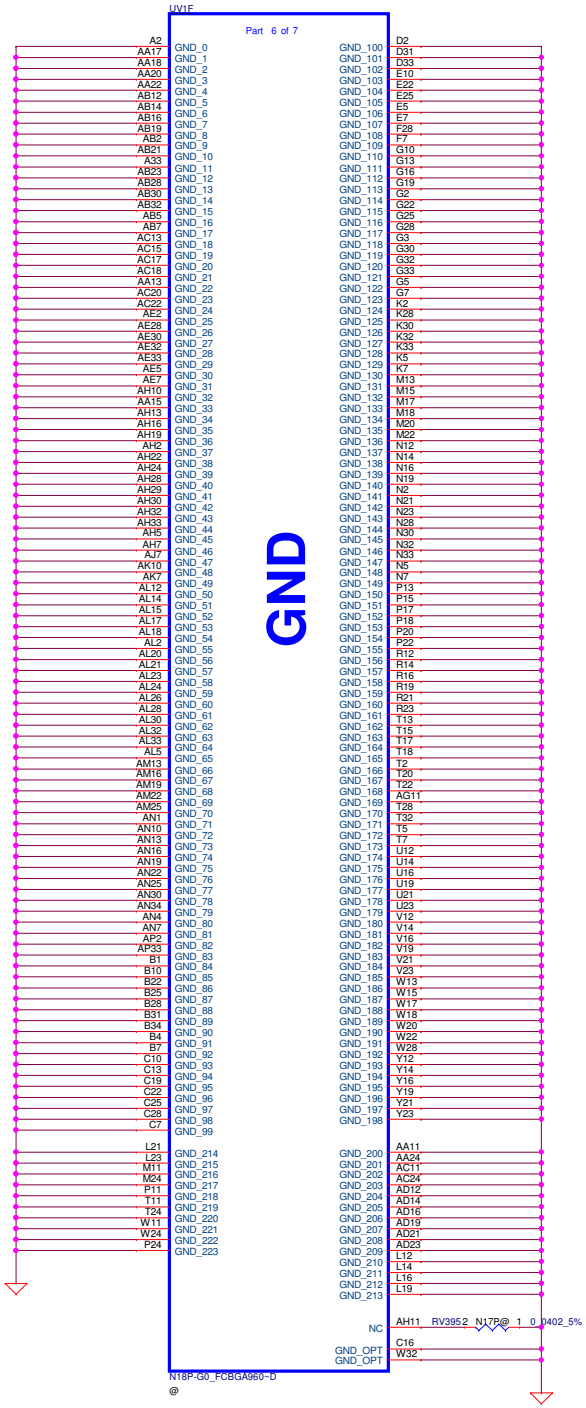
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 30 of 101		

N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2





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Title: N17P POWER & GND 5/7

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 31 of 101

Security Classification	Compal Secret Data		
Issued Date	2017/10/30	Deciphered Date	2018/10/30

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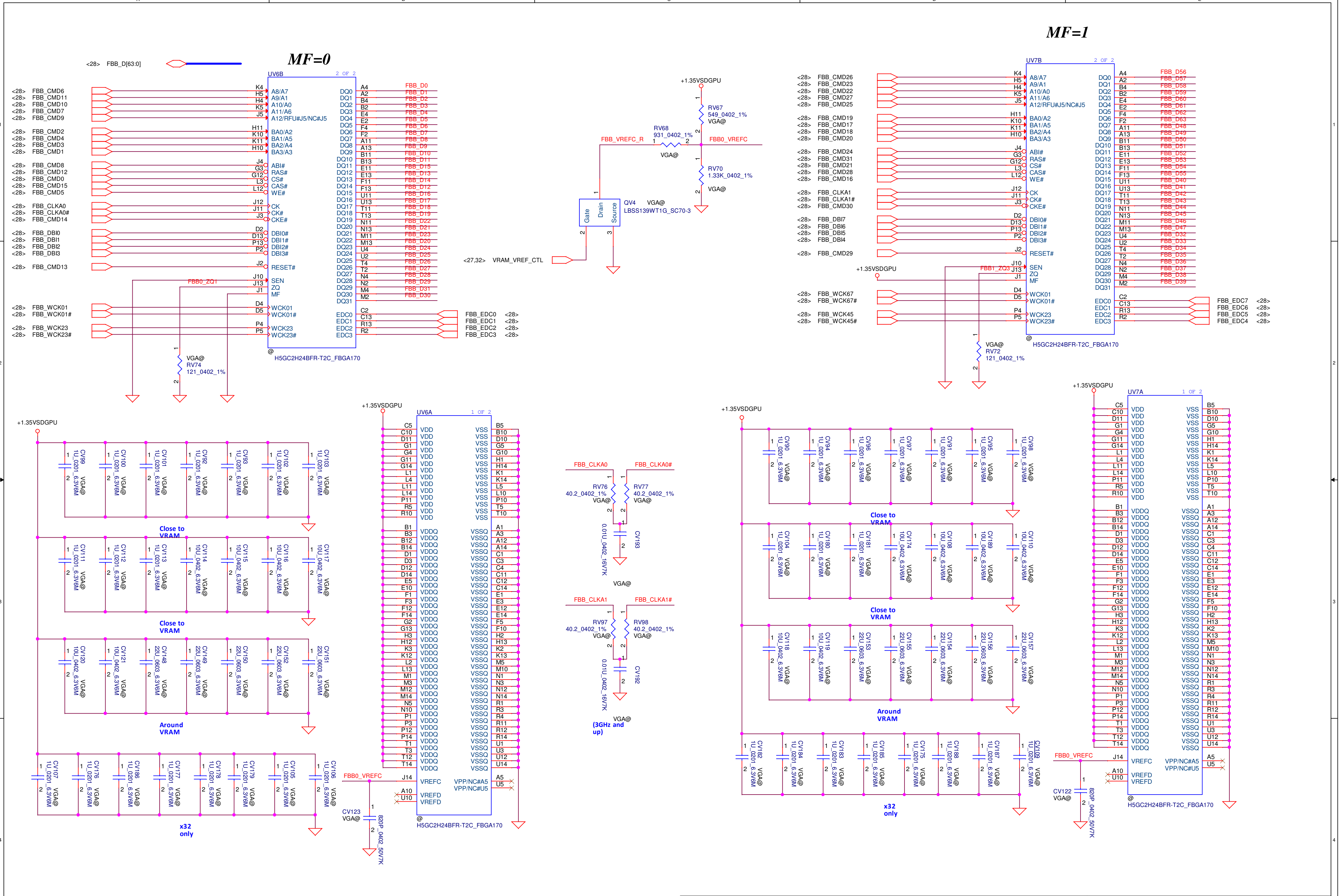
Title	N17P GDDR5 CHA 6/7		
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 32 of 101		



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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 34 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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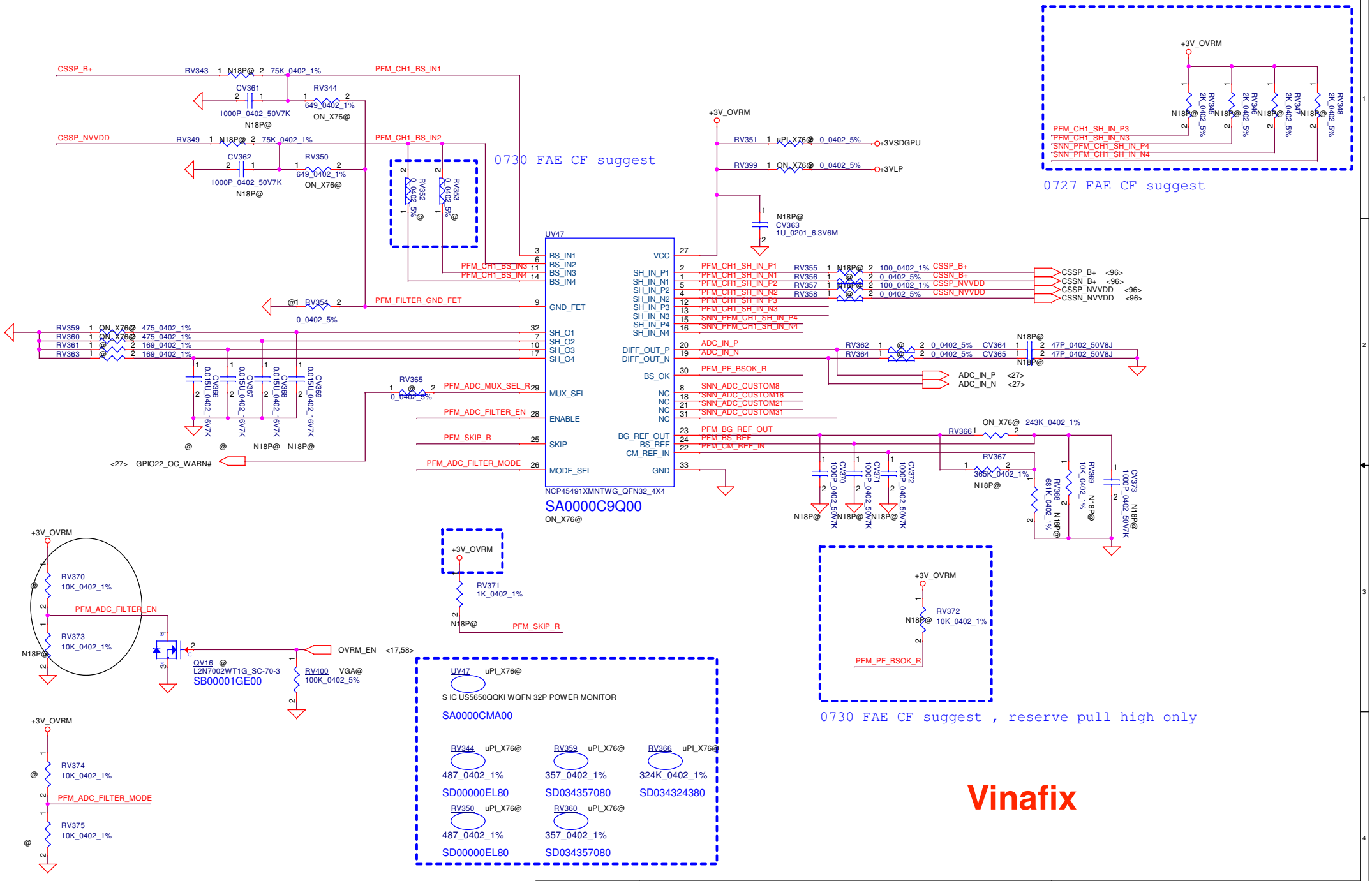
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 35 of 101



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Title: OVR-M			
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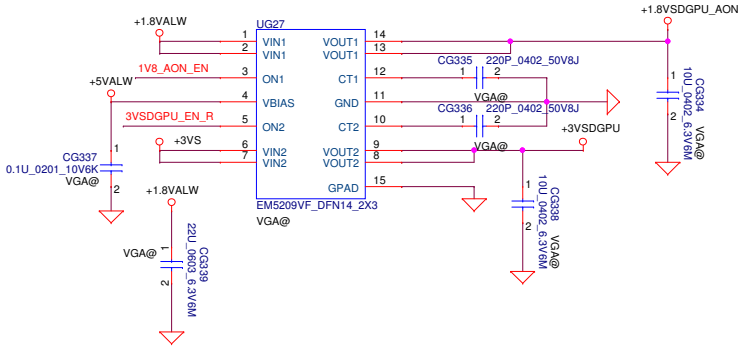
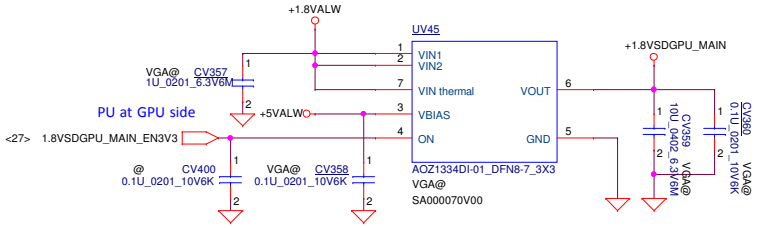
Date: Friday, February 22, 2019	Sheet 36 of 101		

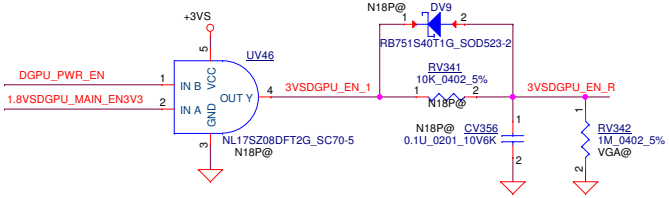
+1.8V_AON/+3VSDGPU



+1.8V_MAIN



For Power down sequence



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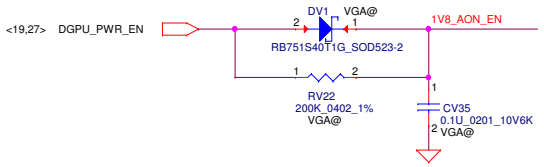

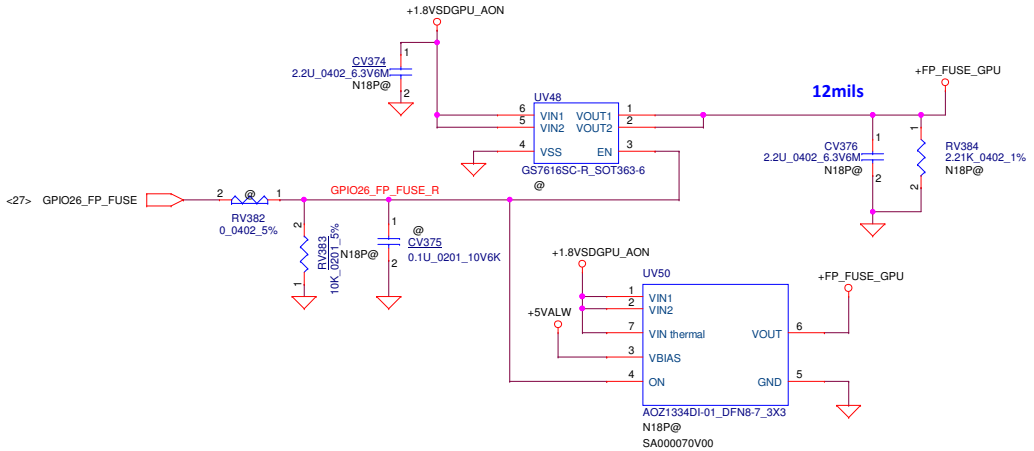

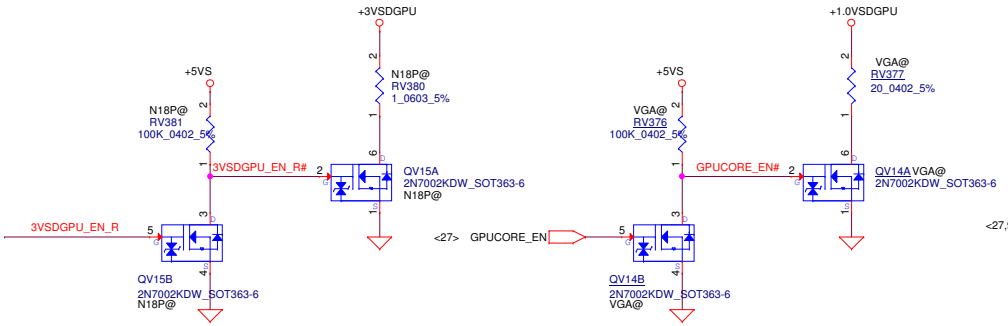

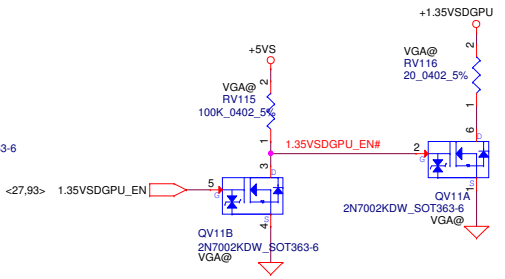

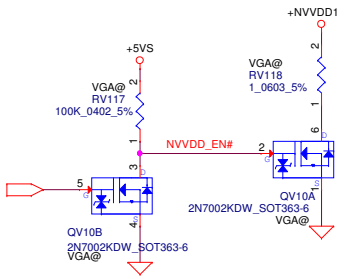

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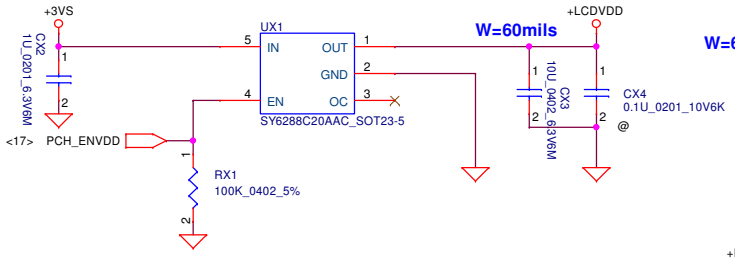
Size	Document Number: EH5VF M/B LA-H501P
Rev	1A
Date: Friday, February 22, 2019	Sheet 37 of 101

LCD POWER CIRCUIT



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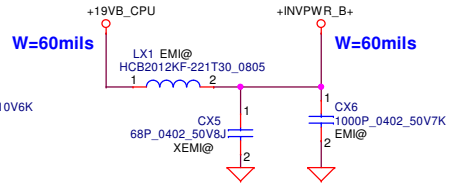
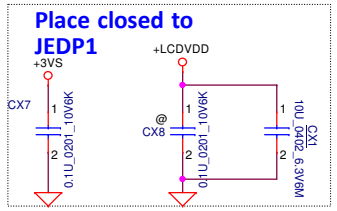
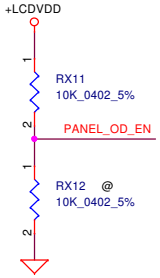
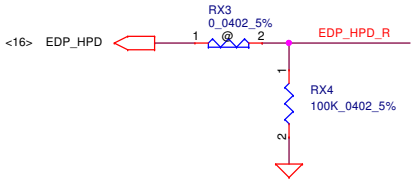
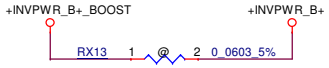
220ohm@100mhz
DCR 0.04

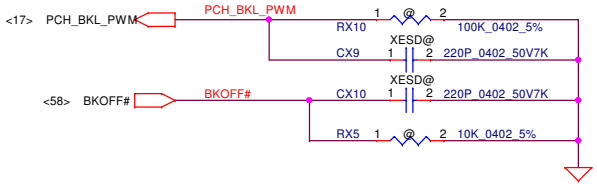




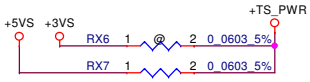




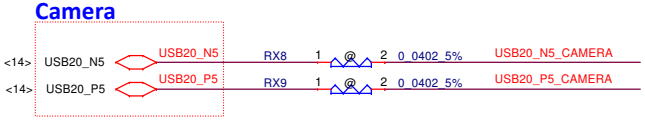




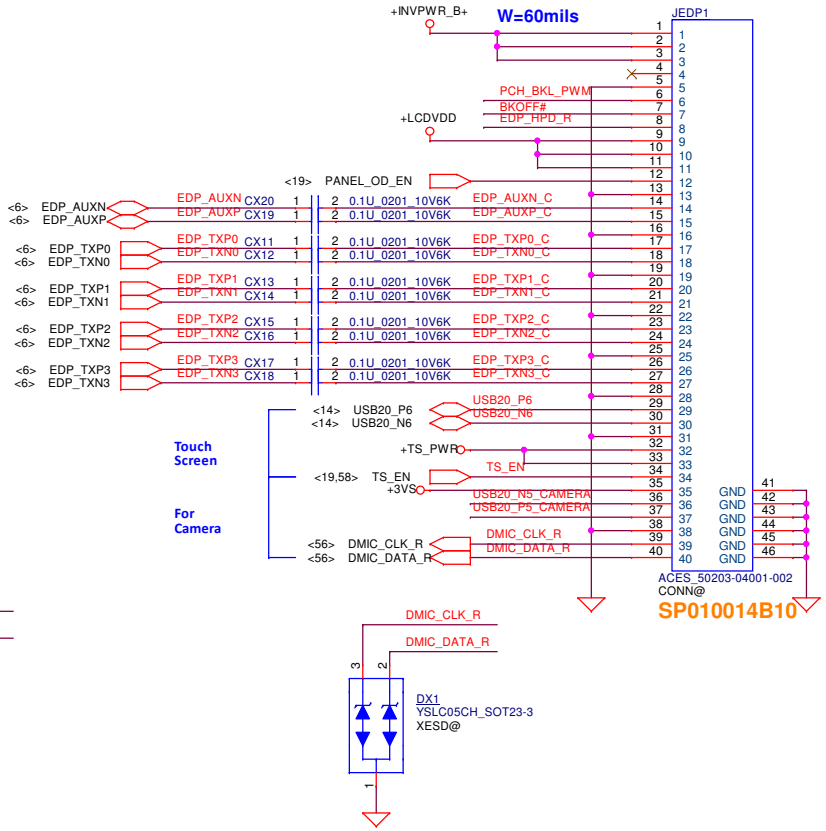
USB Touch Screen



Camera



LED PANEL Conn.



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Compal Electronics, Inc.

Title: eDP CONN.

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Date: Friday, February 22, 2019 | Sheet 38 of 101

Reserve Page

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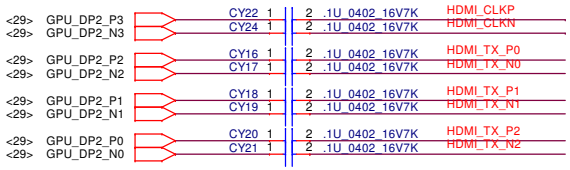
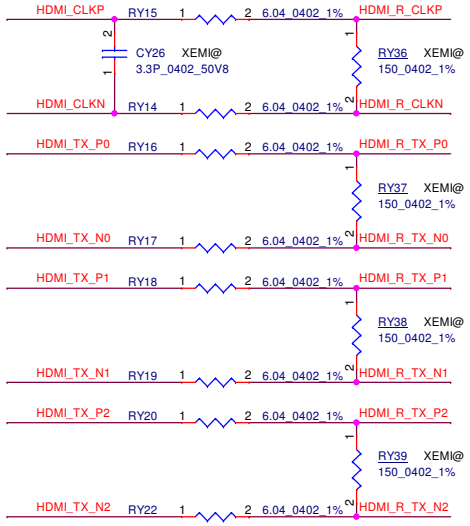
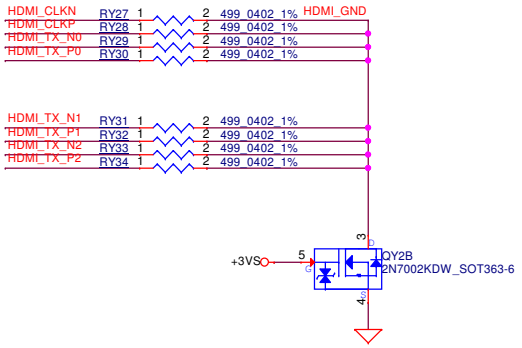
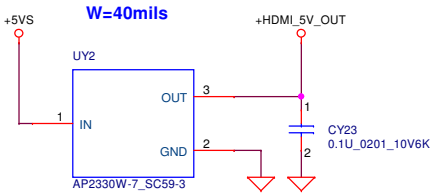
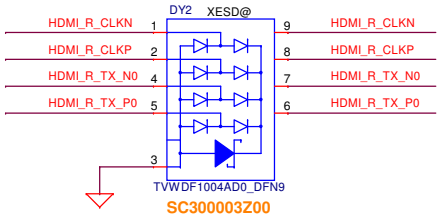
Compal Electronics, Inc.		
Title	*DP CONN*	
Size: Custom	Document Number: *EH5VF M/B LA-H501P*	Rev: 1A
Date: Friday, February 22, 2019	Sheet 39 of 101	

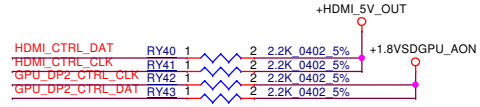


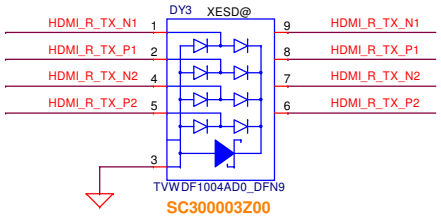


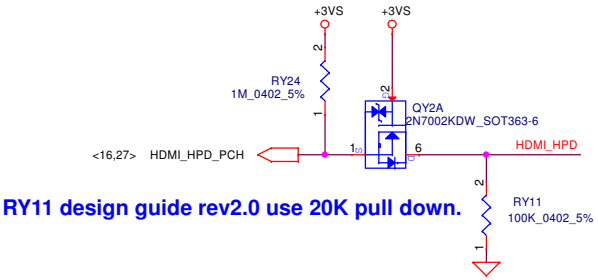


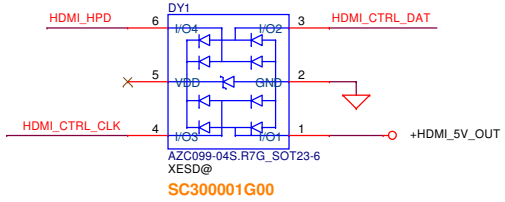


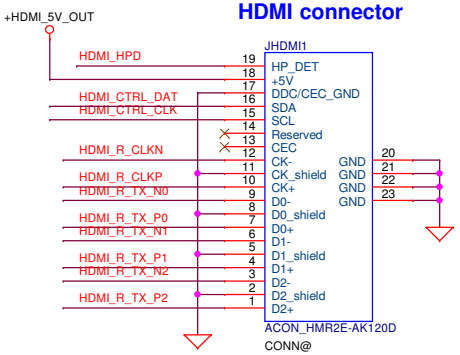


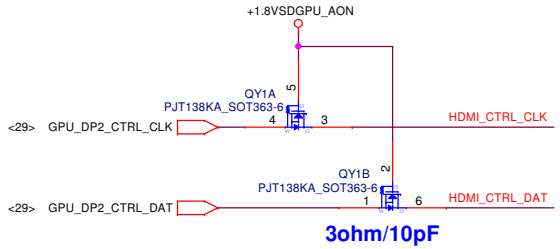












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Compal Electronics, Inc.

Title: HDMI CONN.

Size	Document Number	Rev
Custom	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 40 of 101

Reserve Page

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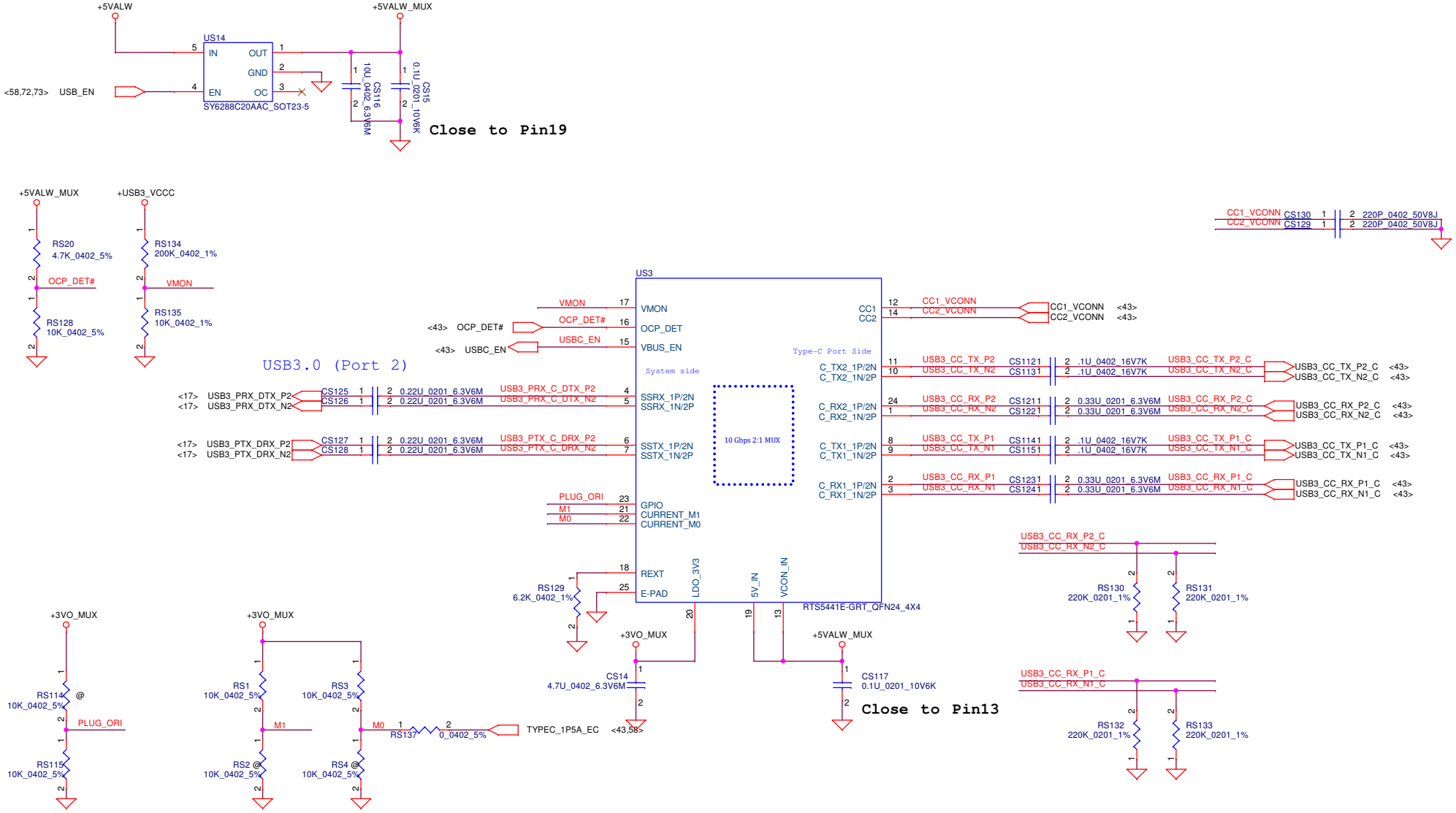
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 41 of 101



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

confirm realtek hand-shake

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Issued Date	2017/07/20	Deciphered Date	2018/07/20

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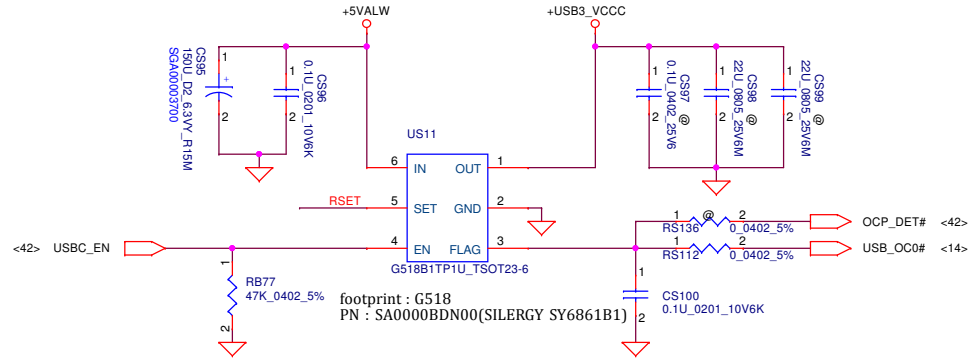
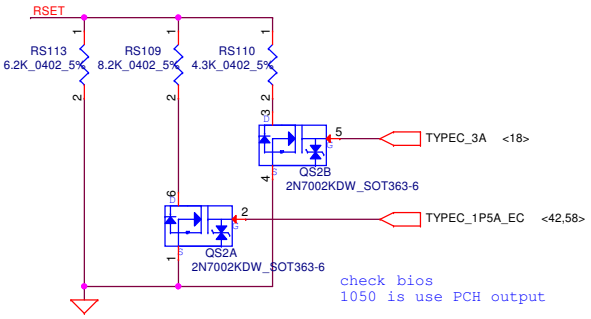
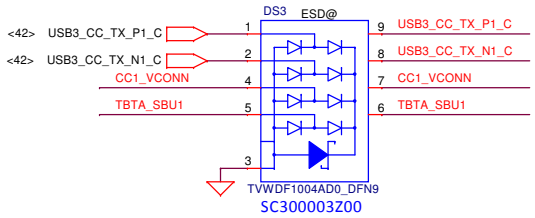
Compal Electronics, Inc.			
Title	CC+USB TYPE C		
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 42 of 101		

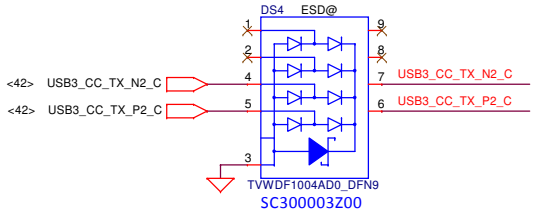


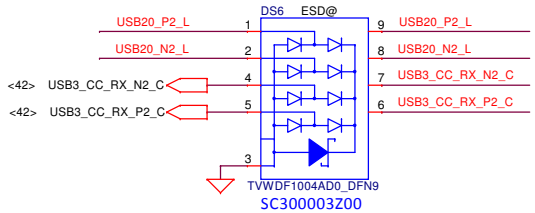


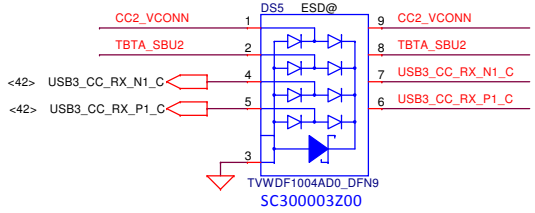
G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

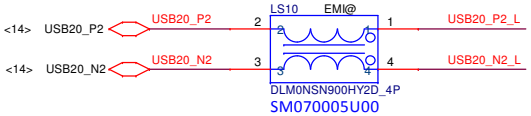
For ESD request

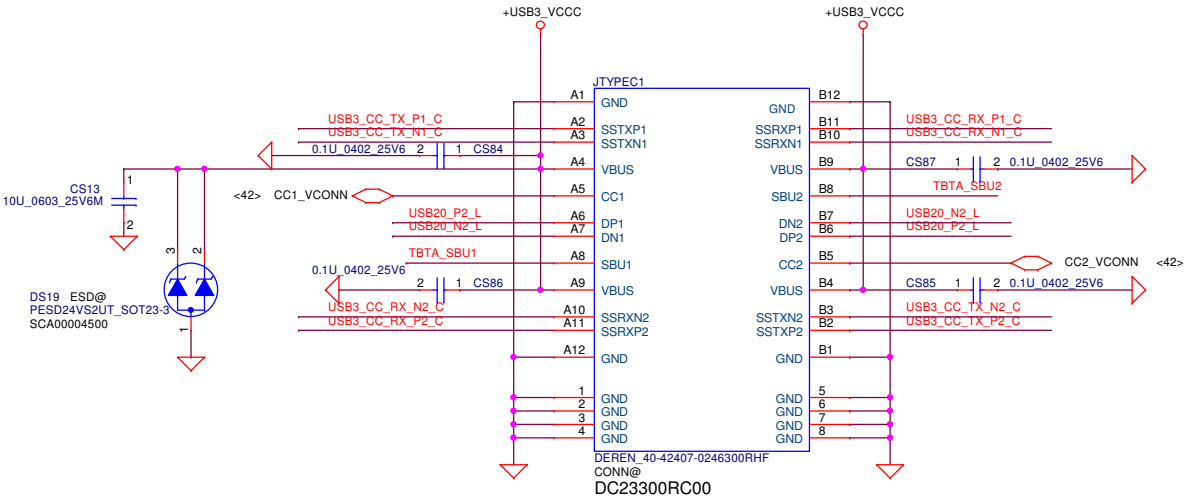












CC1_VCONN & CC2_VCONN need 20miil trace width.

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Compal Electronics, Inc.

Title: CC+USB TYPE C

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Date: Friday, February 22, 2019 | Sheet 43 of 101

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 44 of 101

Reserve Page

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Title: *N18E-GDDR6_D*

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Date: Friday, February 22, 2019 | Sheet 45 of 101

Reserve Page

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Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 46 of 101

Reserve Page

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Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 47 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Size	Document Number: EH5VF M/B LA-H501P	Rev: 1A
Date: Friday, February 22, 2019	Sheet 48 of 101	

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 49 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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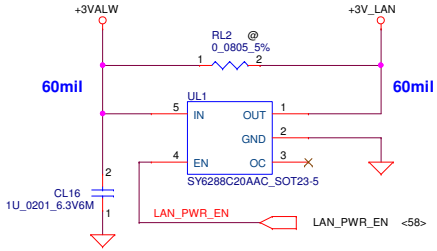
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 50 of 101

+3V_LAN Rising time (10%~90%) must >0.5mS and <100mS



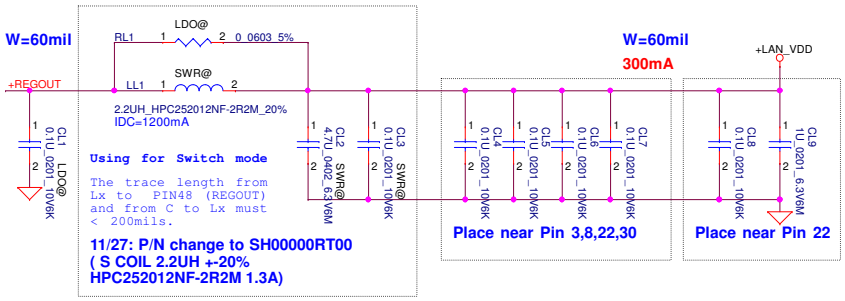
From EC

High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms

RTL8111H LDO mode

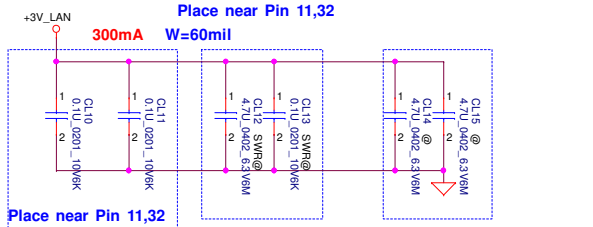
RTL8118ASA SWR mode



Using for Switch mode

The trace length from C to Lx must < 200mils.

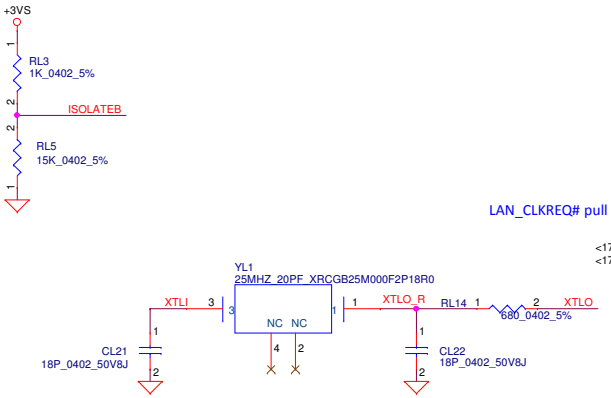
11/27: P/N change to SH00000RT00
(S COIL 2.2UH +-20%
HPC252012NF-2R2M 1.3A)



Using for Switch mode

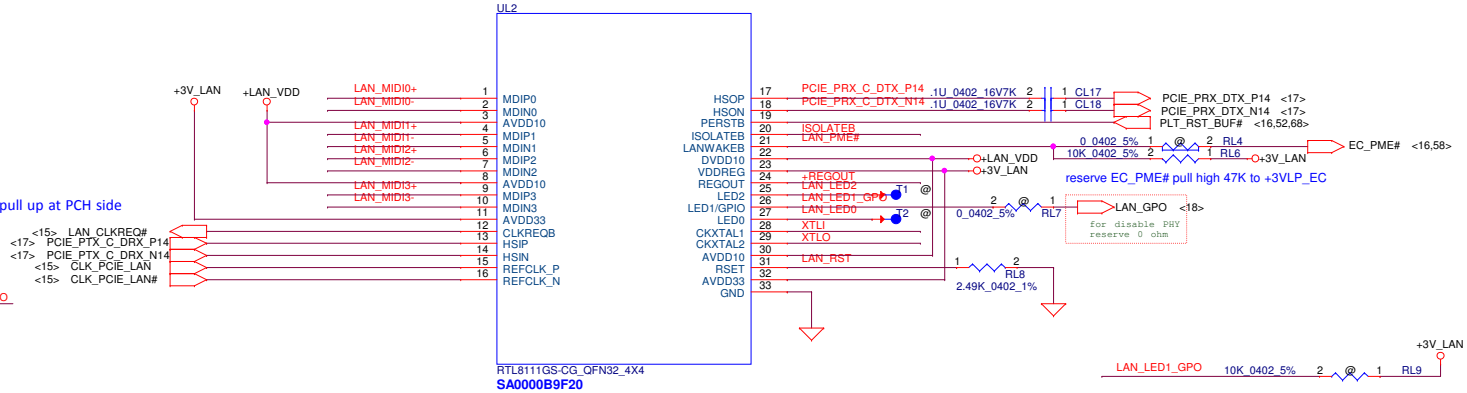
The trace length from C to PIN46,47(VDDREG) must < 200mils.

Reserve for surge improvement
Place near Pin 11,32



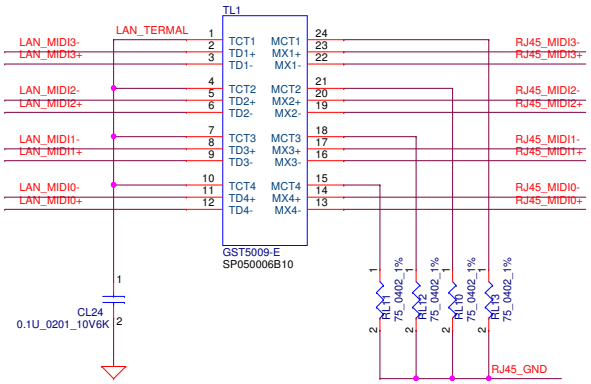
P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

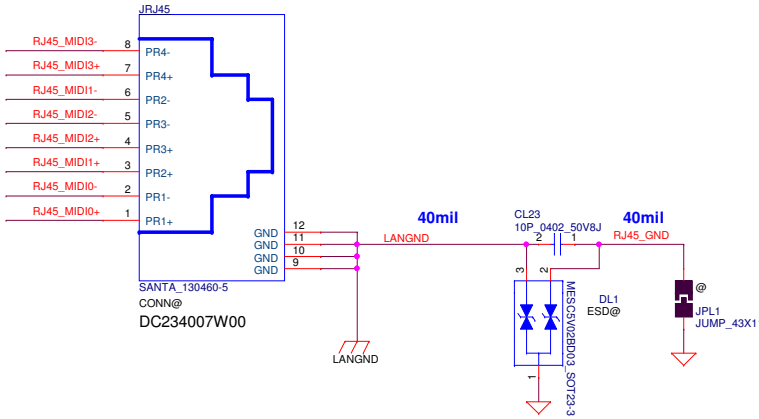
LAN_CLKREQ# pull up at PCH side



SA0000B9F20, S IC RTL8118ASA-CG QFN 32P E-LAN CTRL

LAN Connector





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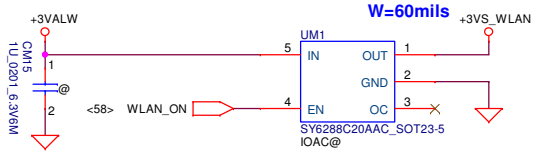
Compal Electronics, Inc.

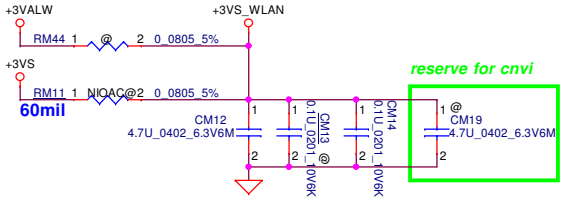
Title: LAN RTL8118ASA

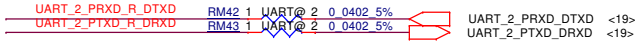
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 51 of 101

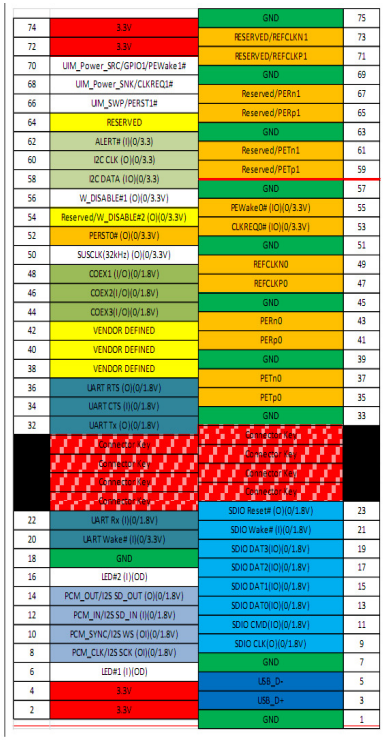
Wireless LAN



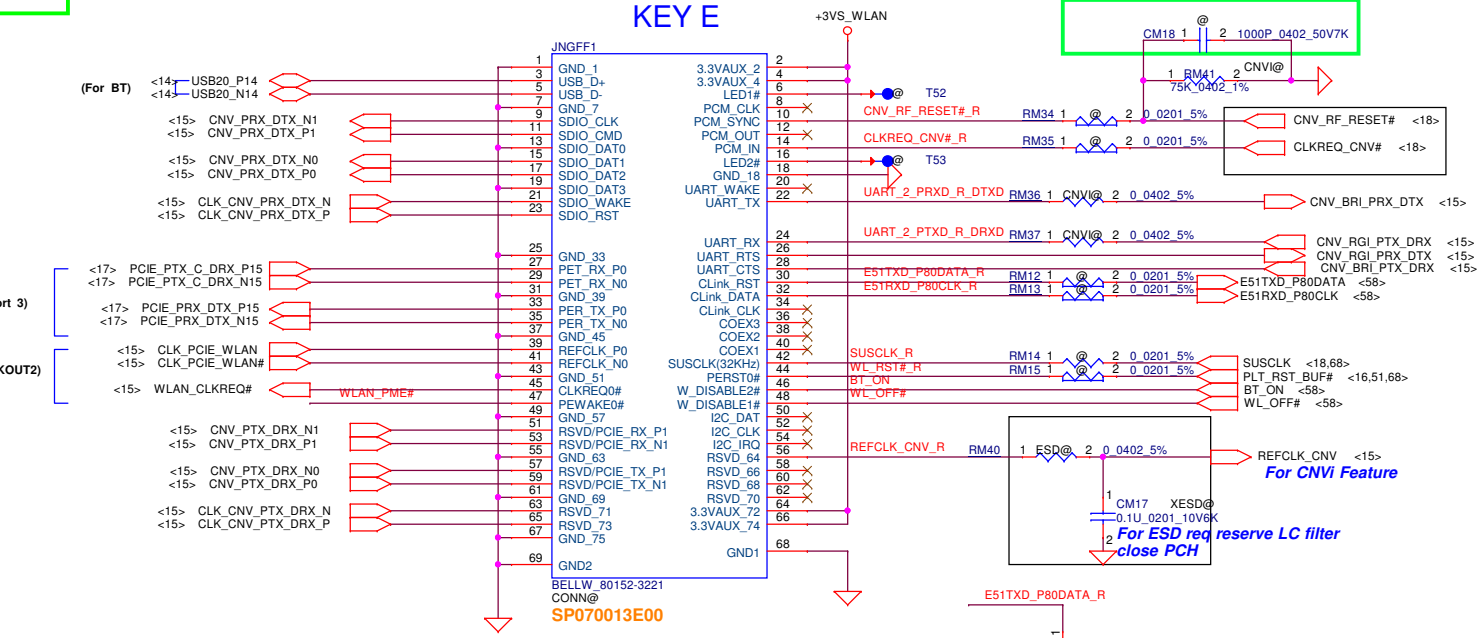




NGFF WL+BT (KEY E)



KEY E



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Title: M.2 Key E (WLAN)			
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 52 of 101		

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Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 53 of 101

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Date: Friday, February 22, 2019 | Sheet 54 of 101

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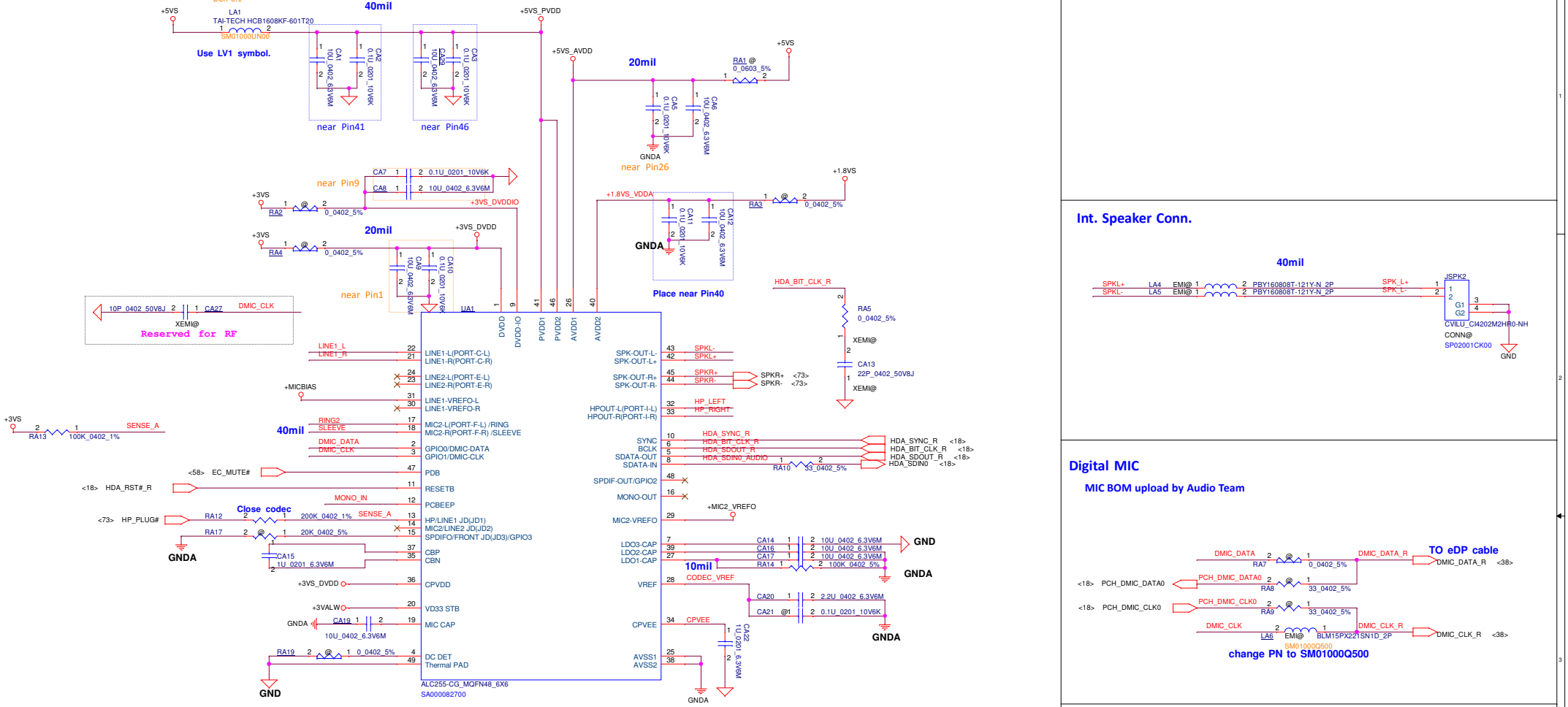
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 55 of 101

HD Audio Codec

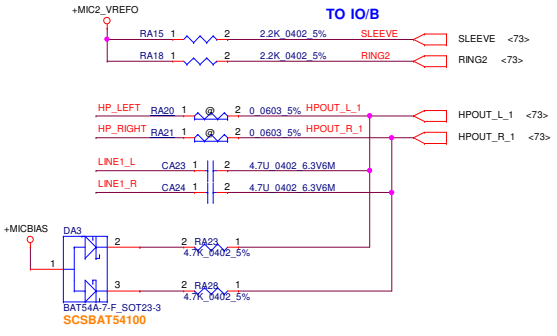


Int. Speaker Conn.

Digital MIC

MIC BOM upload by Audio Team

Headphone Out



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Compal Electronics, Inc.			
Title	HD Audio Codec ALC255		
Size	Document Number		Rev
Custom	EH5VF M/B LA-H501P		1A
Date:	Friday, February 22, 2019	Sheet	56 of 101

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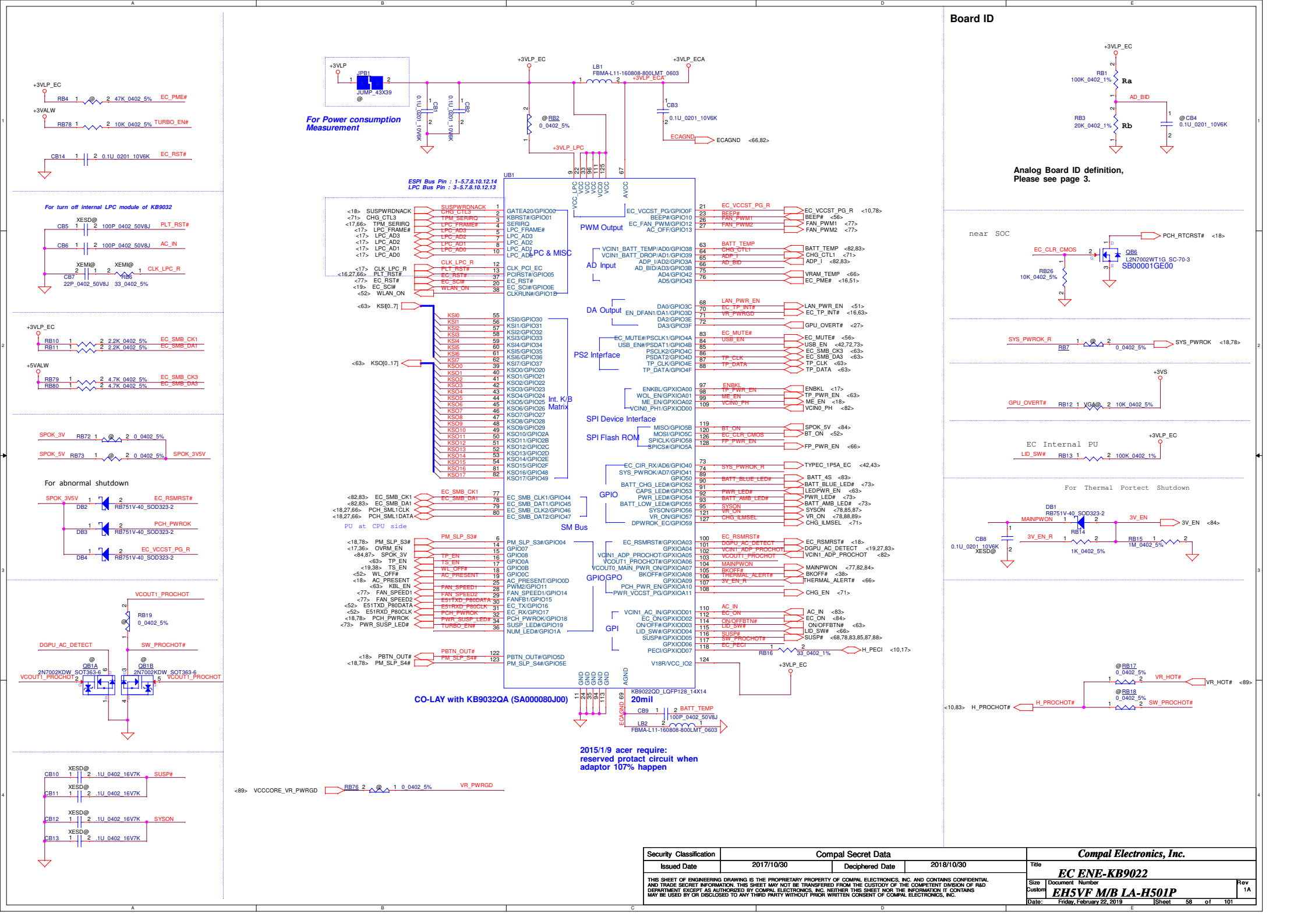
Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 57 of 101


Board ID
Analog Board ID definition,
Please see page 3.
near SOC
EC Internal PU
For Thermal Portect Shutdown
For abnormal shutdown
For turn off internal LPC module of KB9032
For Power consumption Measurement
ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
CO-LAY with KB9032QA (SA000080J00)
20mil
2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen
PU at CPU side
Security Classification
Compal Secret Data
Issued Date
2017/10/30
Deciphered Date
2018/10/30
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Compal Electronics, Inc.
Title
EC ENE-KB9022
Size
Custom
Document Number
EH5VF M/B LA-H501P
Rev
1A
Date: Friday, February 22, 2019
Sheet 58 of 101

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Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

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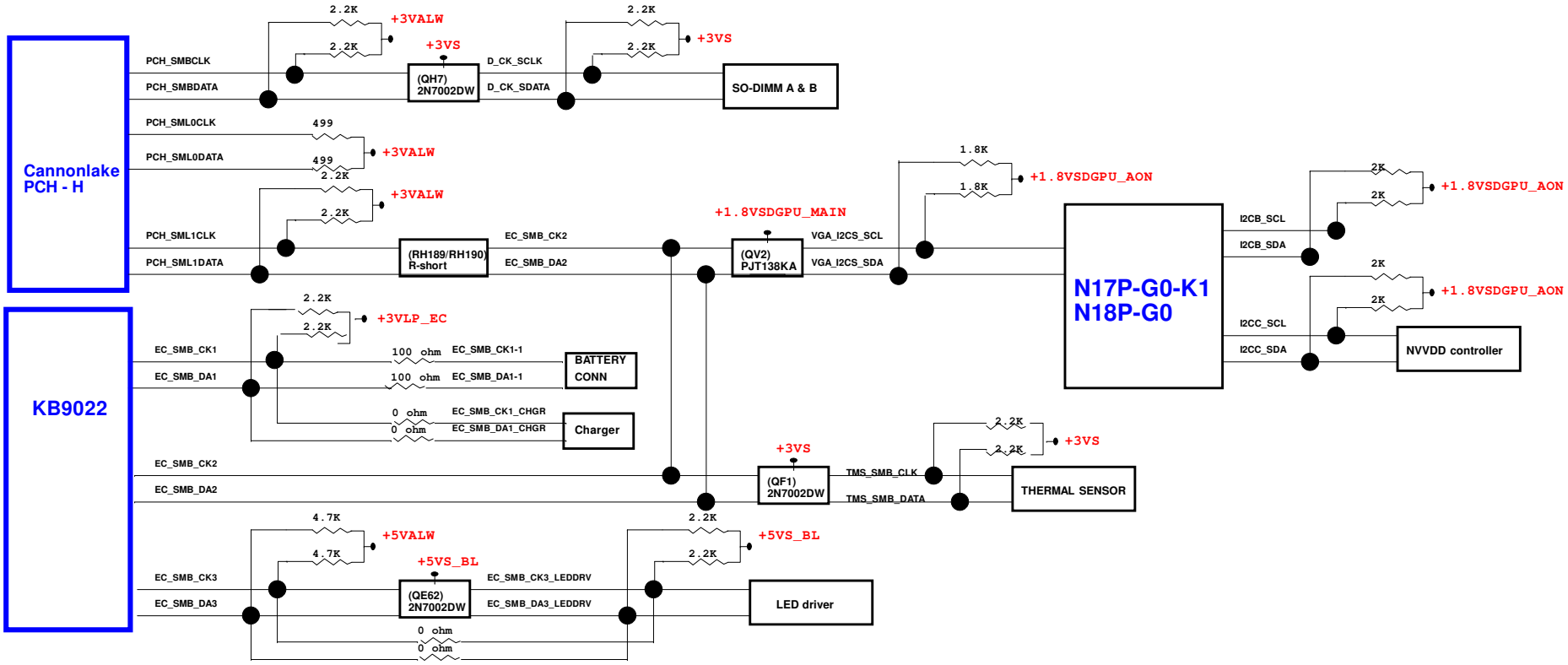
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 60 of 101



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Title: N17E-GDDR5_D

Size	Document Number	Rev
	EH5VF M/B LA-H501P	1A

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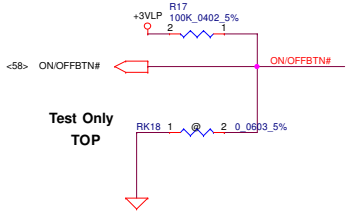
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

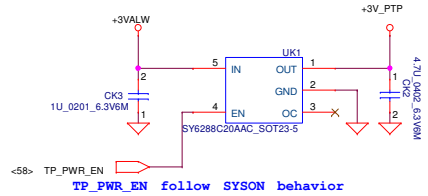
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 62 of 101

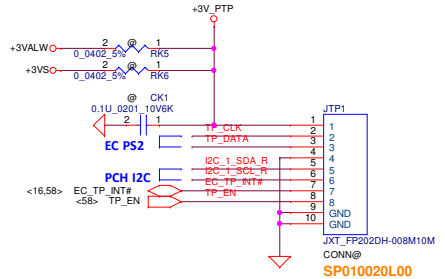
ON/OFF BTN

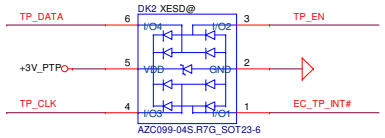


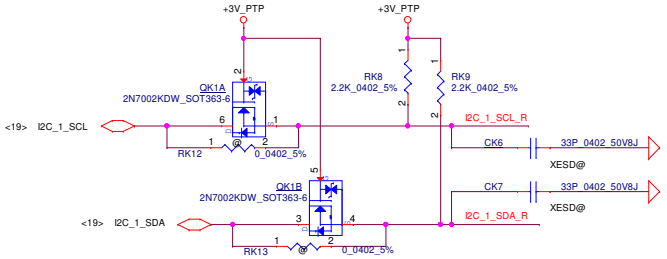
Touch Pad

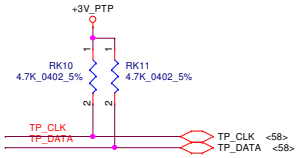


TP_PWR_EN follow SYSON behavior

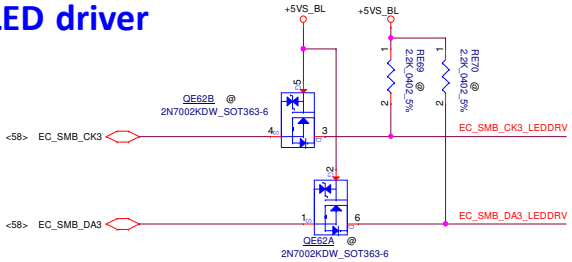


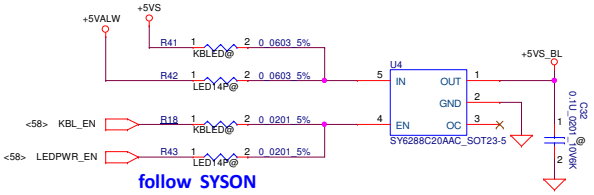






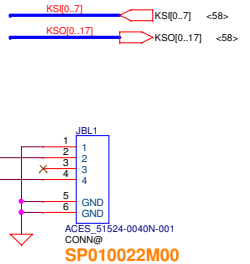
LED driver

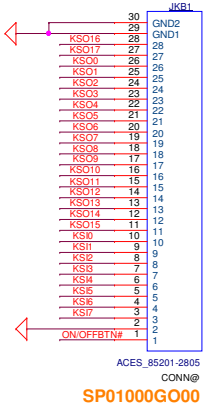


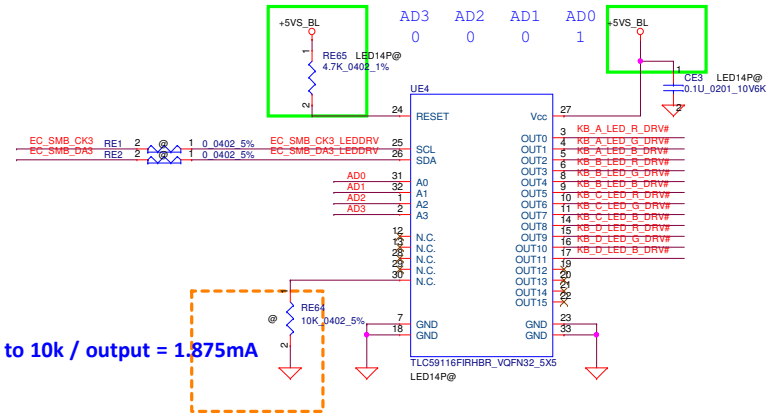


follow SYSON

KB Conn. / Backlight

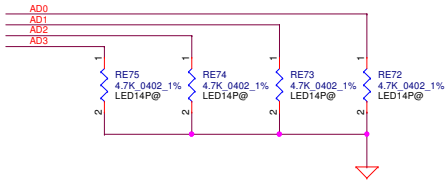


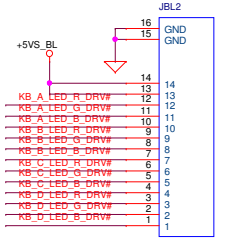




set RE7 to 10k / output = 1.875mA

Raptor: NC for 59116F





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Compal Electronics, Inc.

Title: KB & TP & TPM Connector

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Title: *N18E-GDDR6_D*

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Date: Friday, February 22, 2019 | Sheet 64 of 101

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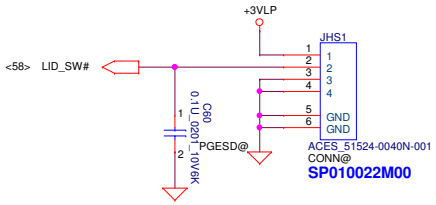
Title: *N18E-GDDR6_D*

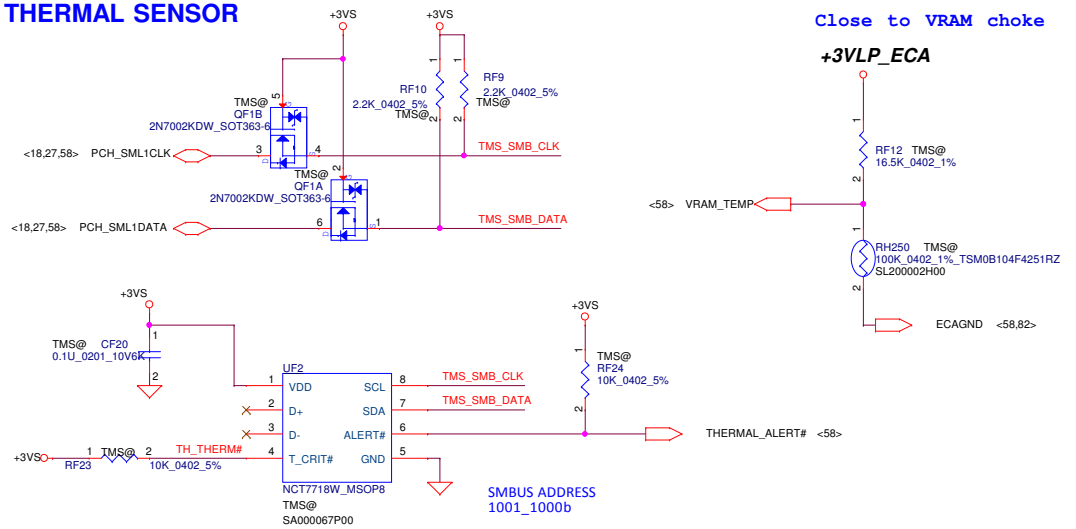
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 65 of 101

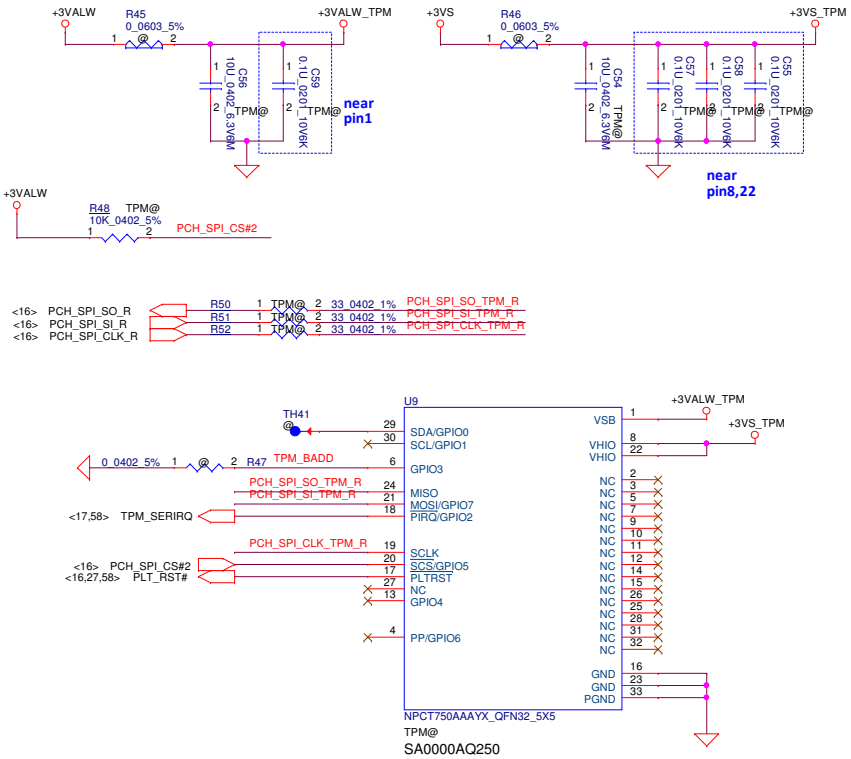
To Hall sensor/B



THERMAL SENSOR

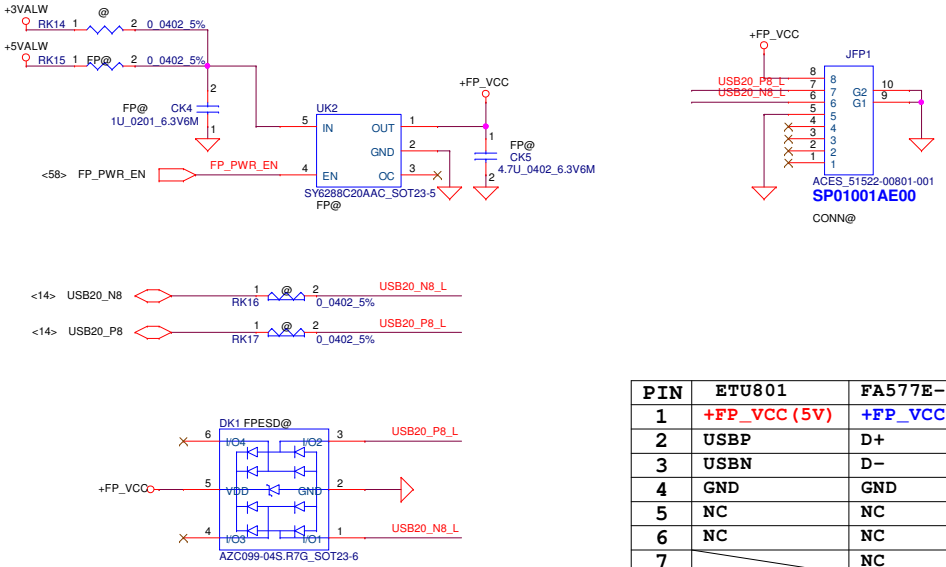


TPM



SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

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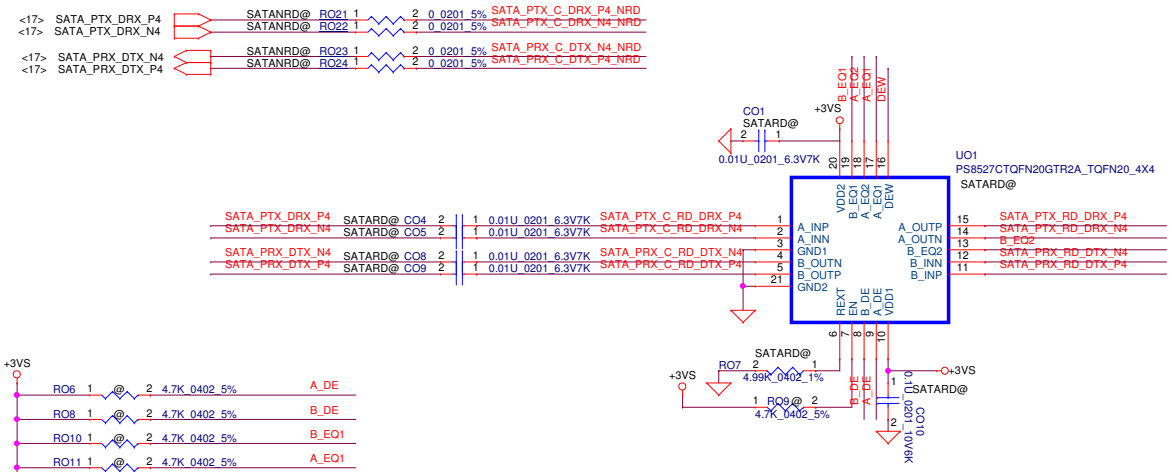
Compal Electronics, Inc.

Title: Sensors/FP/TPM

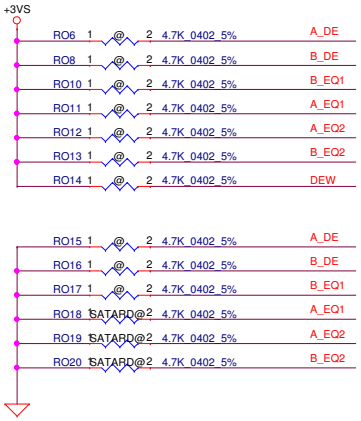
Size | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 66 of 101

SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10



Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

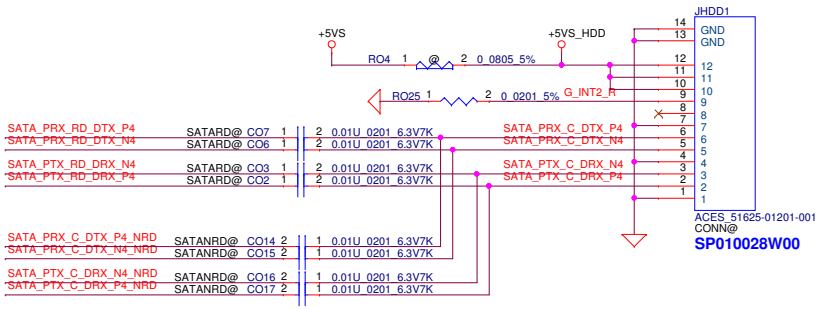
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

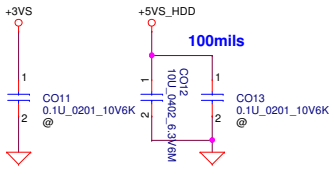
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

FFC Type





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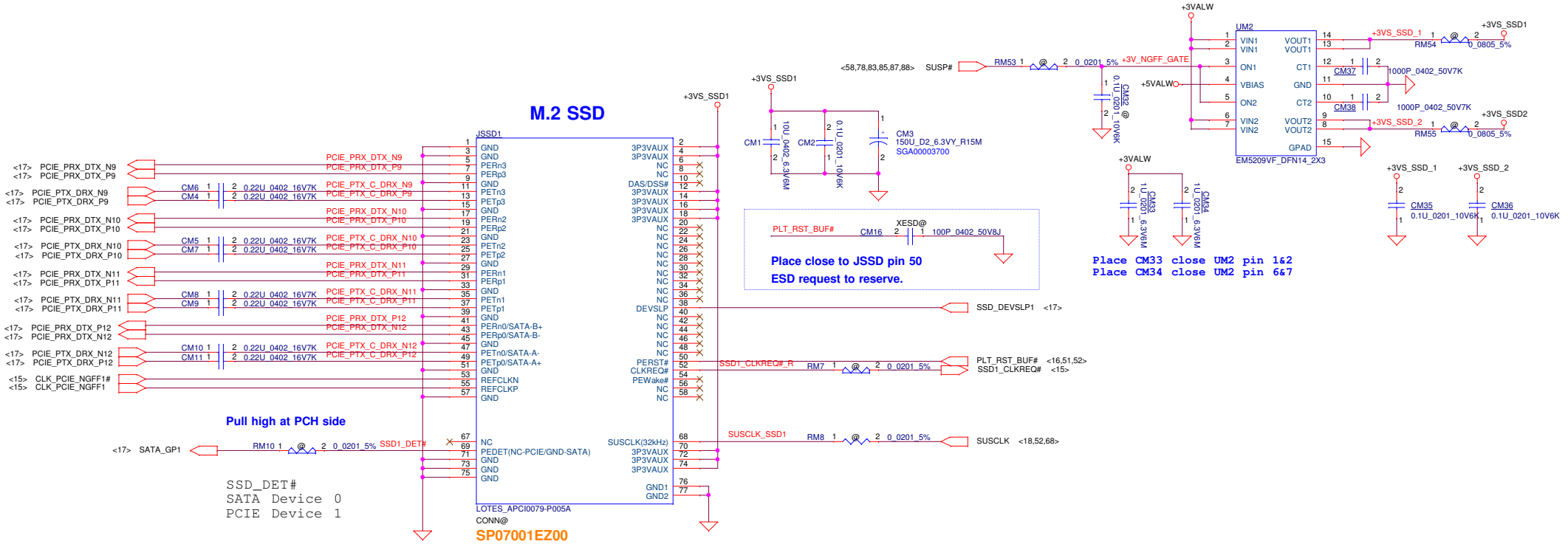
Compal Electronics, Inc.			
Title: HDD/ Re-Driver/ G-sensor			
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 67 of 101		



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Issued Date	2017/10/30	Deciphered Date	2018/10/30

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Compal Electronics, Inc.			
Title: SATA/PCIE-SSD			
Size: Custom	Document Number: EH5VF M/B LA-H501P		Rev: 1A
Date: Friday, February 22, 2019	Sheet 68 of 101		

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Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 69 of 101

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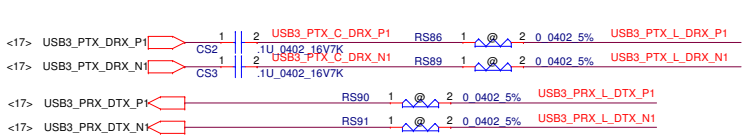
Compal Electronics, Inc.

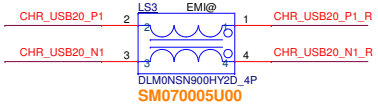
Title: *N18E-GDDR6_D*

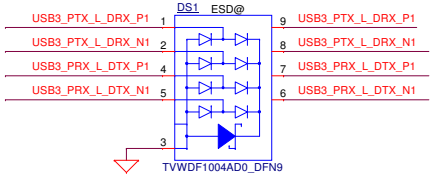
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

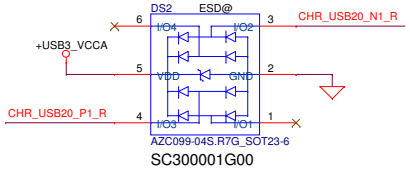
Date: Friday, February 22, 2019 | Sheet 70 of 101

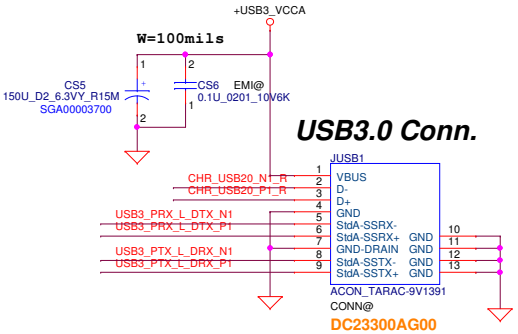
USB3.0



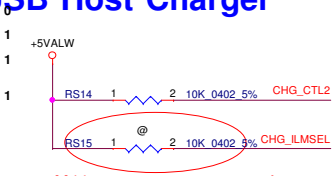




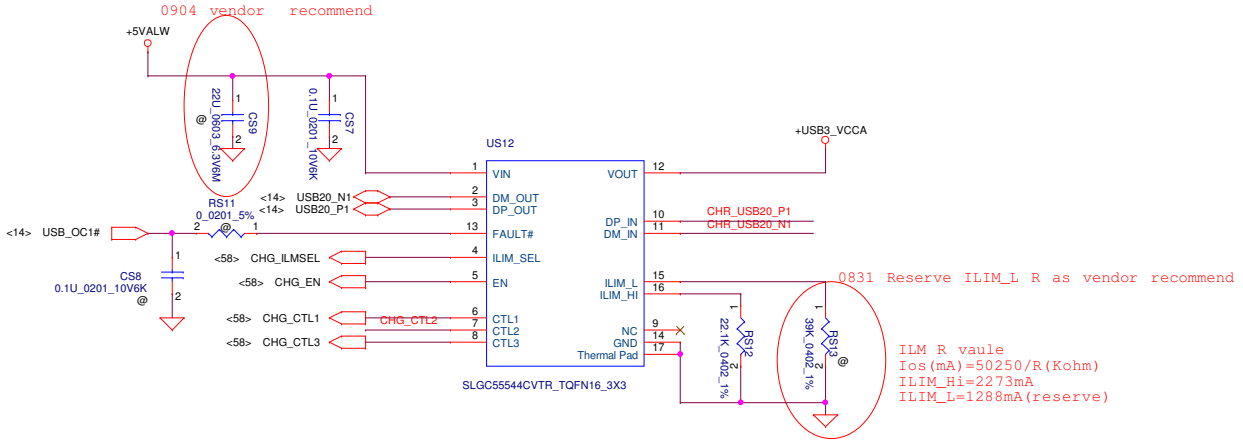




USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
	1	1	1	1	CDP	ILIM_H	Data Lines Connected

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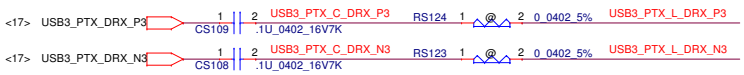
Compal Electronics, Inc.

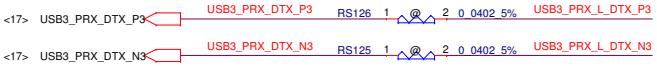
Title: USB3.0 Conn/USB Charger

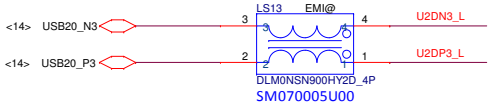
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

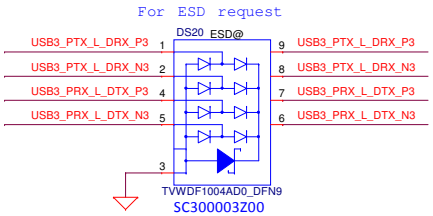
Date: Friday, February 22, 2019 | Sheet 71 of 101

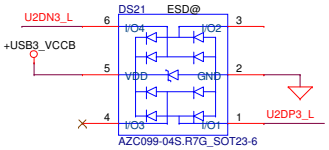
USB3.0

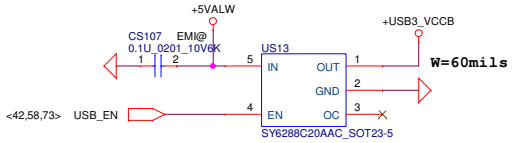


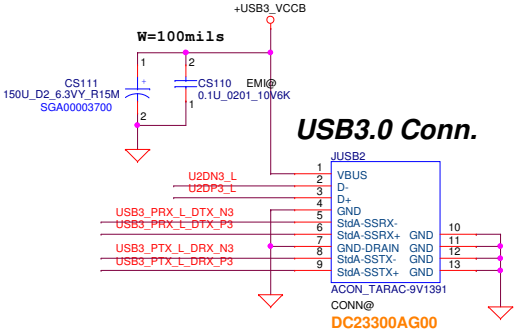












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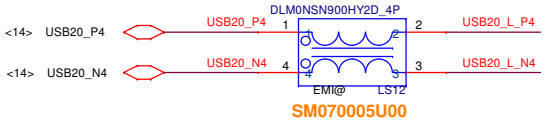
Compal Electronics, Inc.

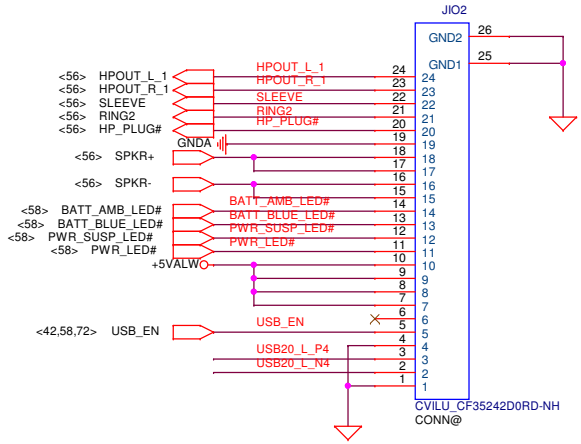
Title: N18E-GDDR6_D

Size | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 72 of 101

IO/B CONN





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Compal Electronics, Inc.

Title: IO/B

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Date: Friday, February 22, 2019 | Sheet 73 of 101

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

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Date: Friday, February 22, 2019 | Sheet 74 of 101

Reserve Page

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 75 of 101

Reserve Page

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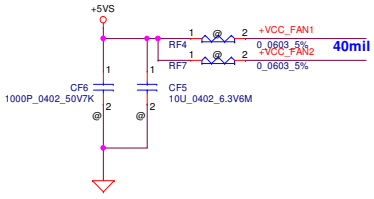
Compal Electronics, Inc.

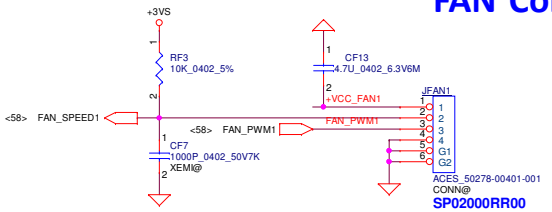
Title: *N18E-GDDR6_D*

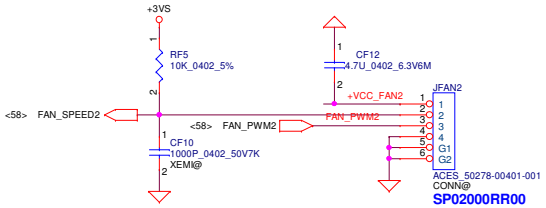
Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 76 of 101

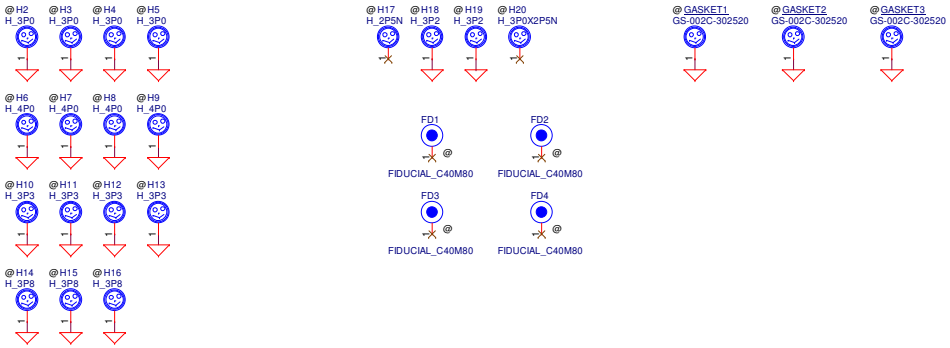


FAN Conn

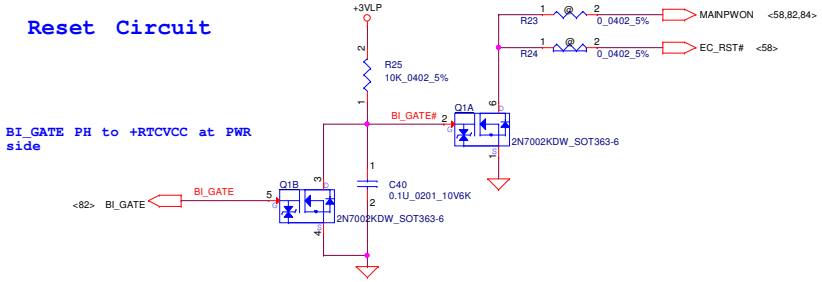




Screw Hole

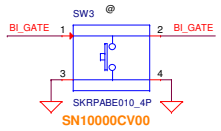


Reset Circuit



BI_GATE PH to +RTCVCC at PWR side

Reset Button



SN10000CV00

change PN to SN10000CV00

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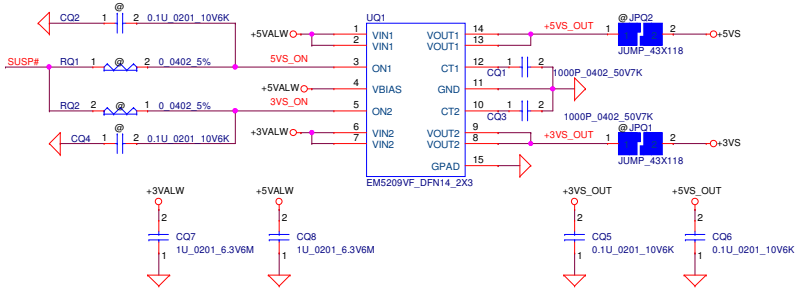
Compal Electronics, Inc.

Title: FAN & Screw Hole

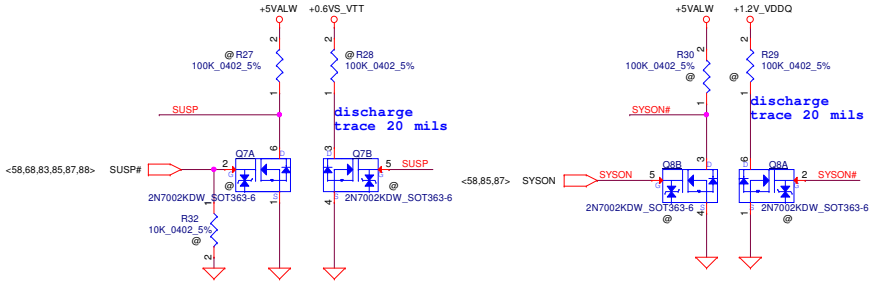
Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 77 of 101

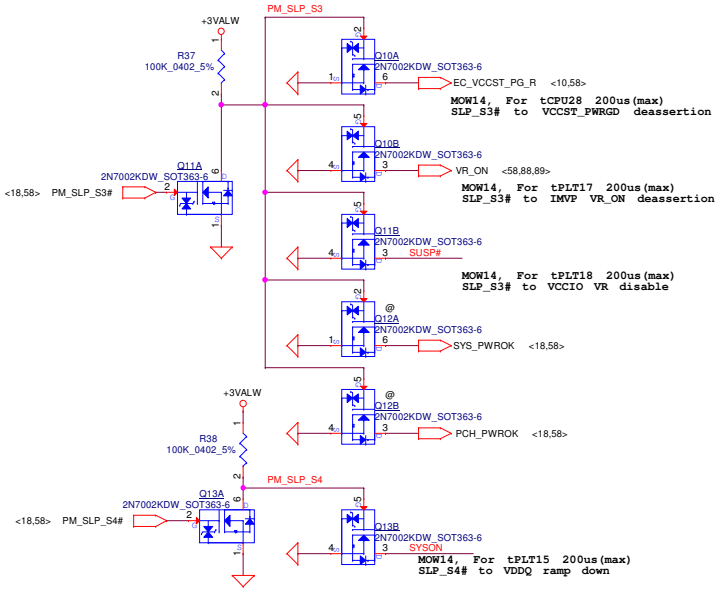
System DC inferface



Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7



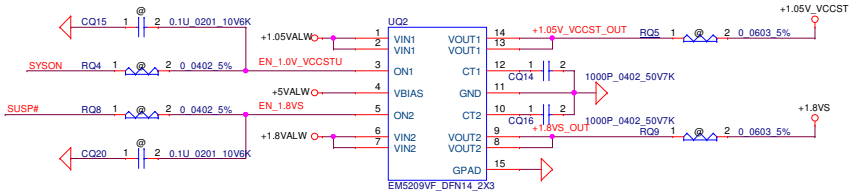
For Power ON/Off Sequence



P/N: SB00000EO00 footprint use SB00000ZU00

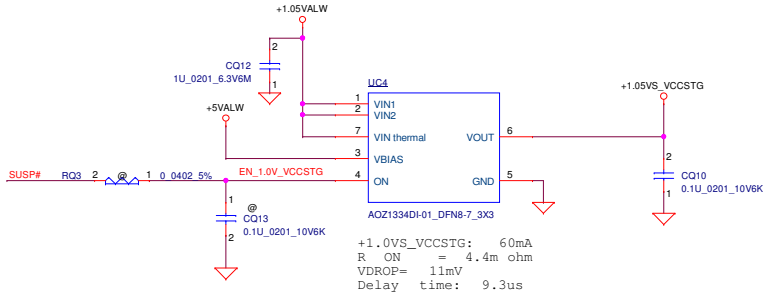
Vinafix

+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



Place CQ11 close UQ2 pin 1&2
Place CQ24 close UQ2 pin 6&7

+1.05VALW TO +1.05VS_VCCSTG



+1.0VS_VCCSTG: 60mA
R ON = 4.4m ohm
VDROP= 11mV
Delay time: 9.3us

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 78 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 79 of 101

Reserve Page

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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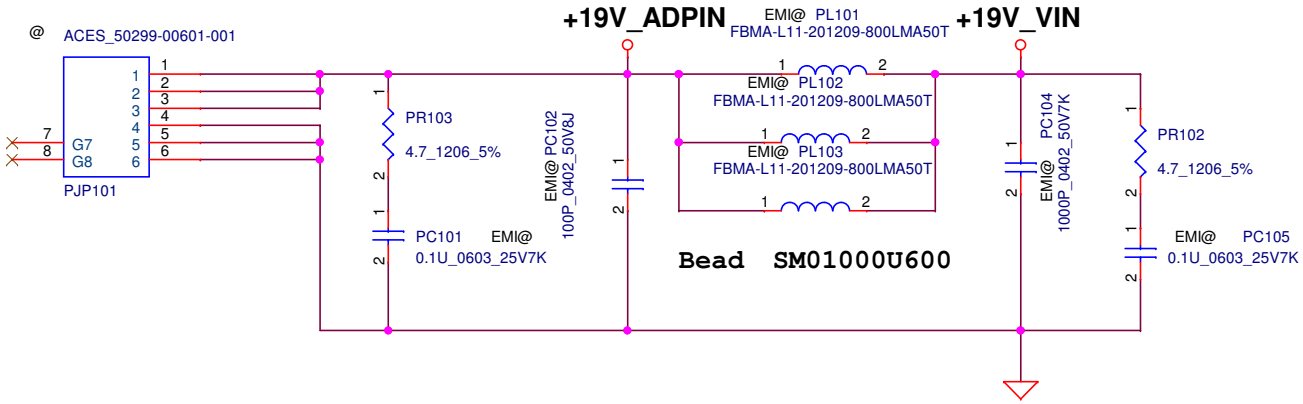
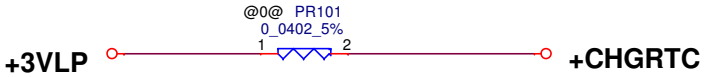
Compal Electronics, Inc.

Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 80 of 101





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Issued Date	2016/11/03	Deciphered Date	2017/06/14

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Compal Electronics, Inc.

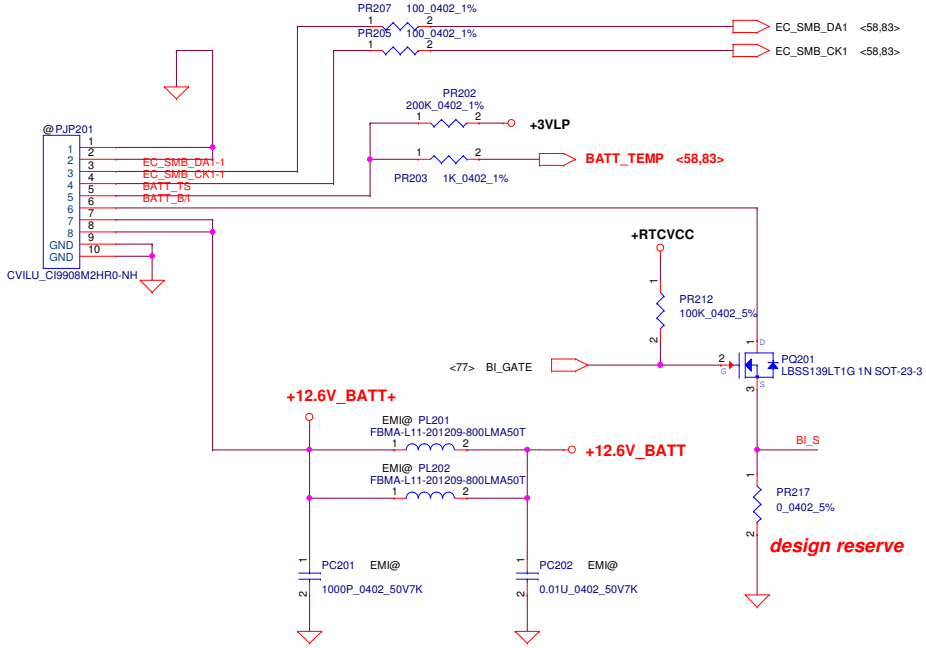
Title: DCIN

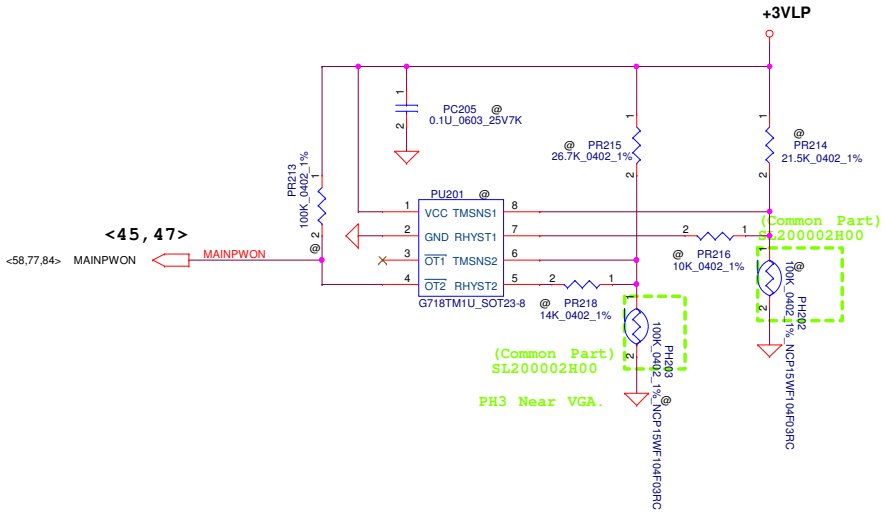
Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 81 of 100

Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

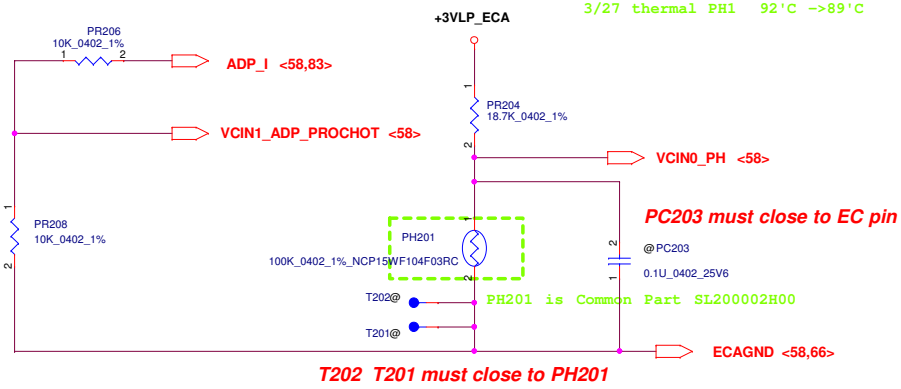




When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	89'C, 1V	56'C, 2V
PH202(ohm)	8.0524K	26.11K

3/27 thermal PH1 92'C ->89'C




```
ADP_I=20*I(adapter)*0.01
I(adapter)=adapter(W)*130%/19
```

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

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Compal Electronics, Inc.

Title: **BATTERY CONN/OTP**

Size: Custom | Document Number: **DH53F M/B LA-F991P** | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 82 of 100

Module model information

ISL95520_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

Isat: 10A
DCR: 14mohm

L->H
2.04 vin min w/o 2M =17.41

H->L
2.02 vin min w 2M =17.77

support Turbo boost : 2200P
no support Turbo boost : 0.1u

Choke 4.7uH SH00000YC00 (Common Part)
(Size:6.6 x 7.3 x 3 mm)
(DCR:28m~33m)

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W

Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VAD P + IAD P + VBA T x IBIA)
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.

adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

Follow adapter and battery wattage in Vsys current source base on CPU Core VR design. The resistor is pop on CPU VR schematic.

Pull high on HW side

PR333=0 ohm, Fs=500KHZ ~ +/- 15%

Hybrid boost power mode
Cell = 4s

BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2

(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ).
CC_LIM = VccLIM / 32 x Rs2

AC_LIM = Vac_LIM / 32 x Rs1

For 4S per cell 4.35V battery

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Issued Date	2014/11/05	Deciphered Date	2014/12/15

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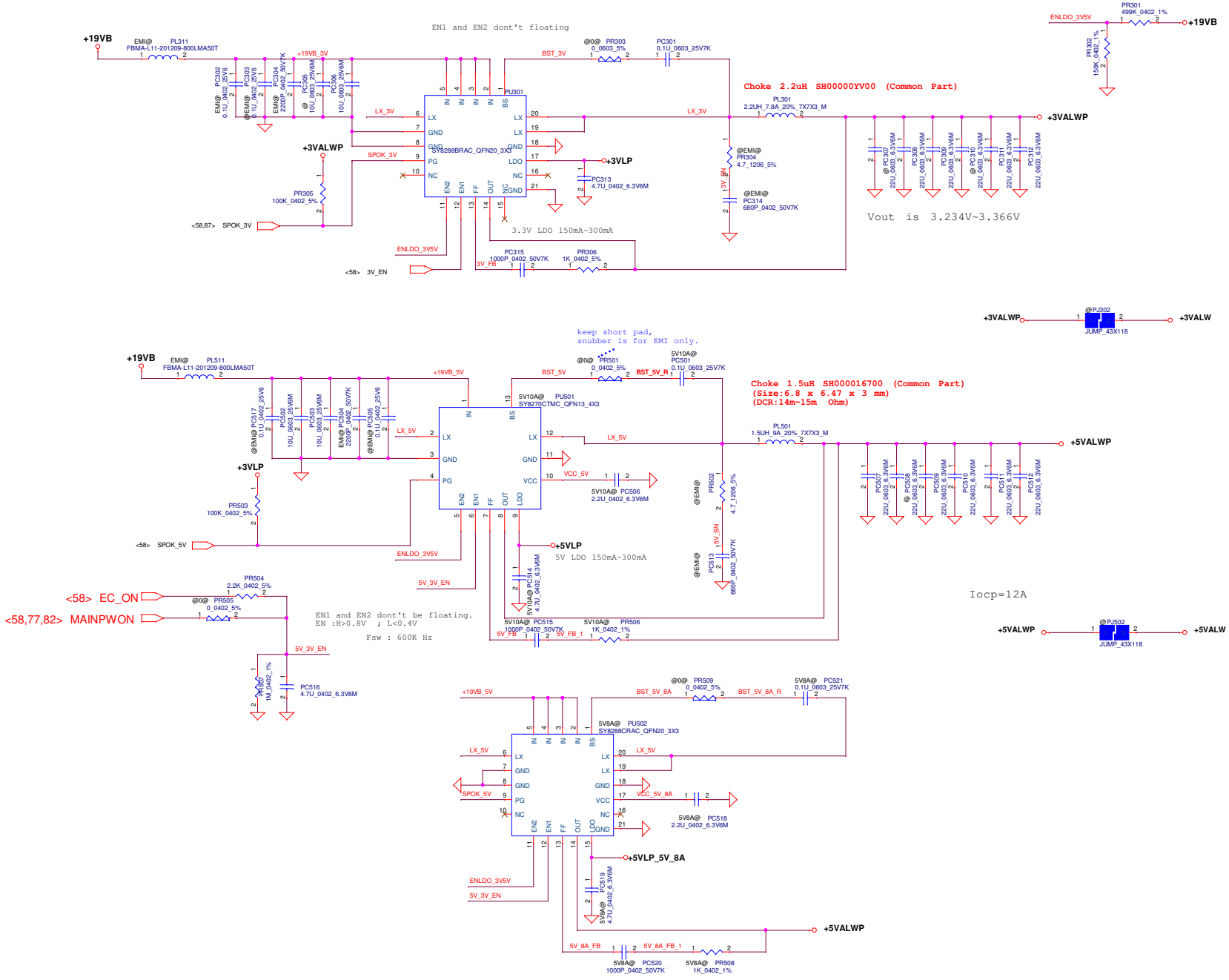
Compal Electronics, Inc.

Title: PWR_CHARGER

Size: | Document Number: | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 83 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2019/11/15

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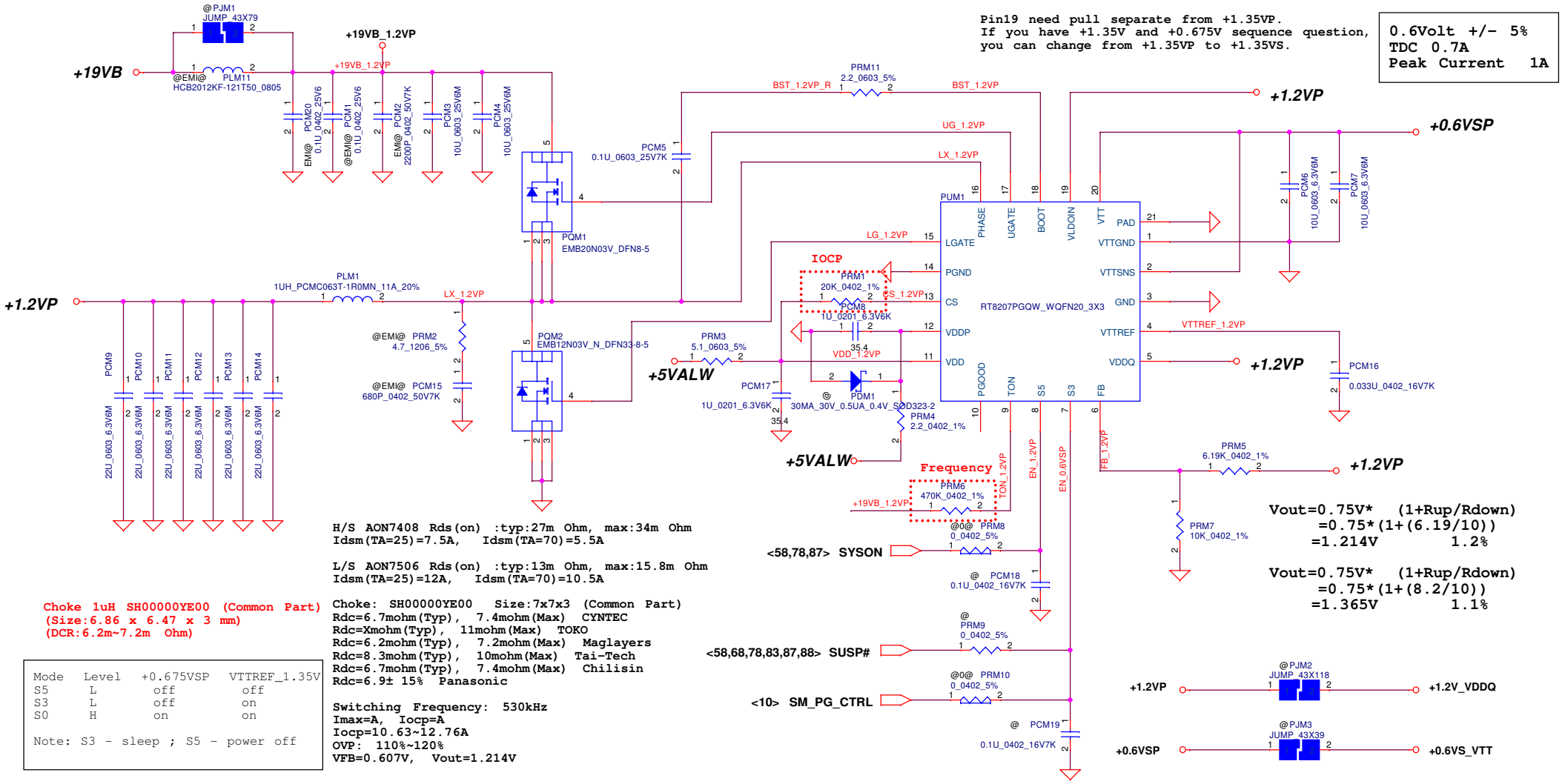
Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1A

Date: Friday, February 22, 2019 Sheet 84 of 100



Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13m Ohm, max:15.8m Ohm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic

Switching Frequency: 530kHz
Imax=A, Iocp=A
Iocp=10.63~12.76A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

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Compal Electronics, Inc.

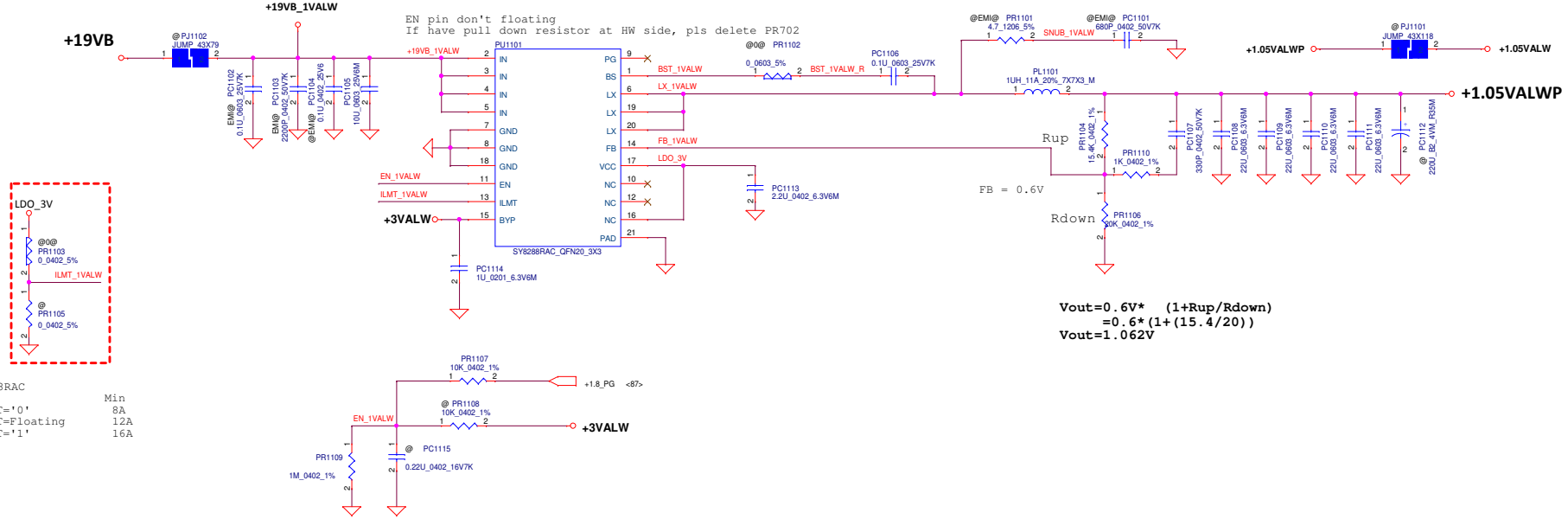
Title: DDR4

Size: Custom | Document Number: DH53F M/B LA-F991P | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 85 of 100

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m~7.2m Ohm)

Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic



8288RAC

	Min
ILMT='0'	8A
ILMT=Floating	12A
ILMT='1'	16A

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

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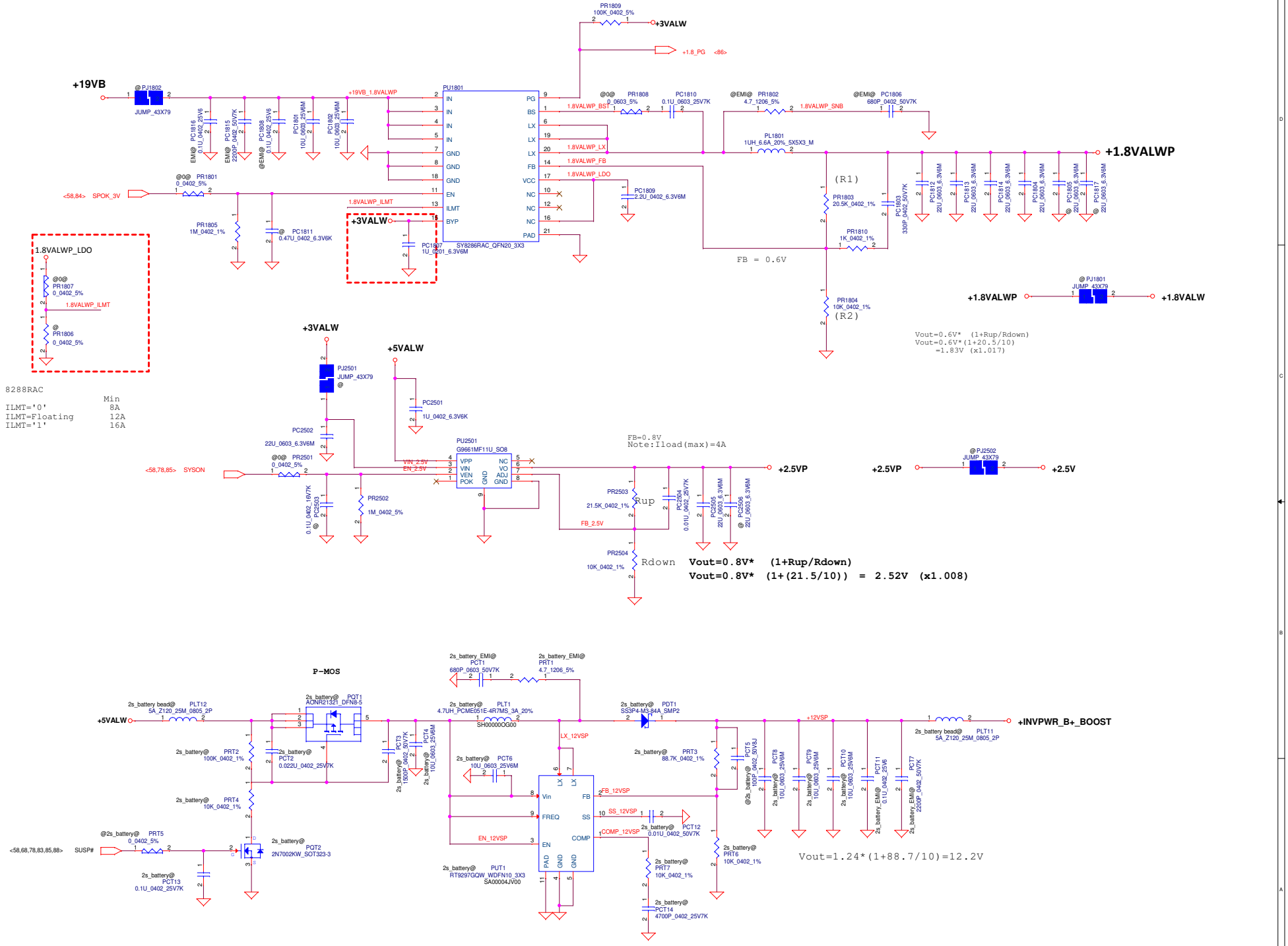
Compal Electronics, Inc.

Title: 1V

Size	Document Number	Rev
C	DH53F M/B LA-F991P	1A

Date: Friday, February 22, 2019 Sheet 86 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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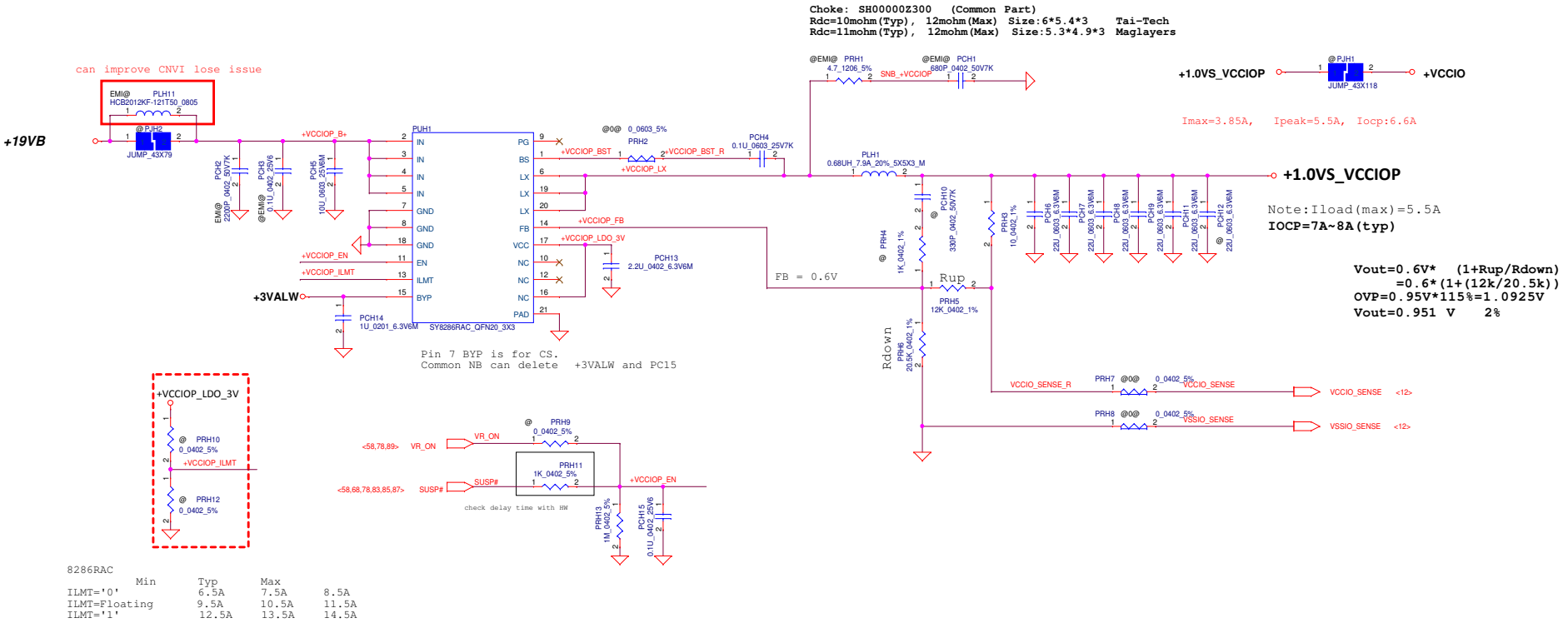
Compal Electronics, Inc.

Title: 1.5VS/2.5V

Size	Document Number	Rev
	EH5VF M/B LA-H501P	1A

Date: Friday, February 22, 2019 Sheet 87 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

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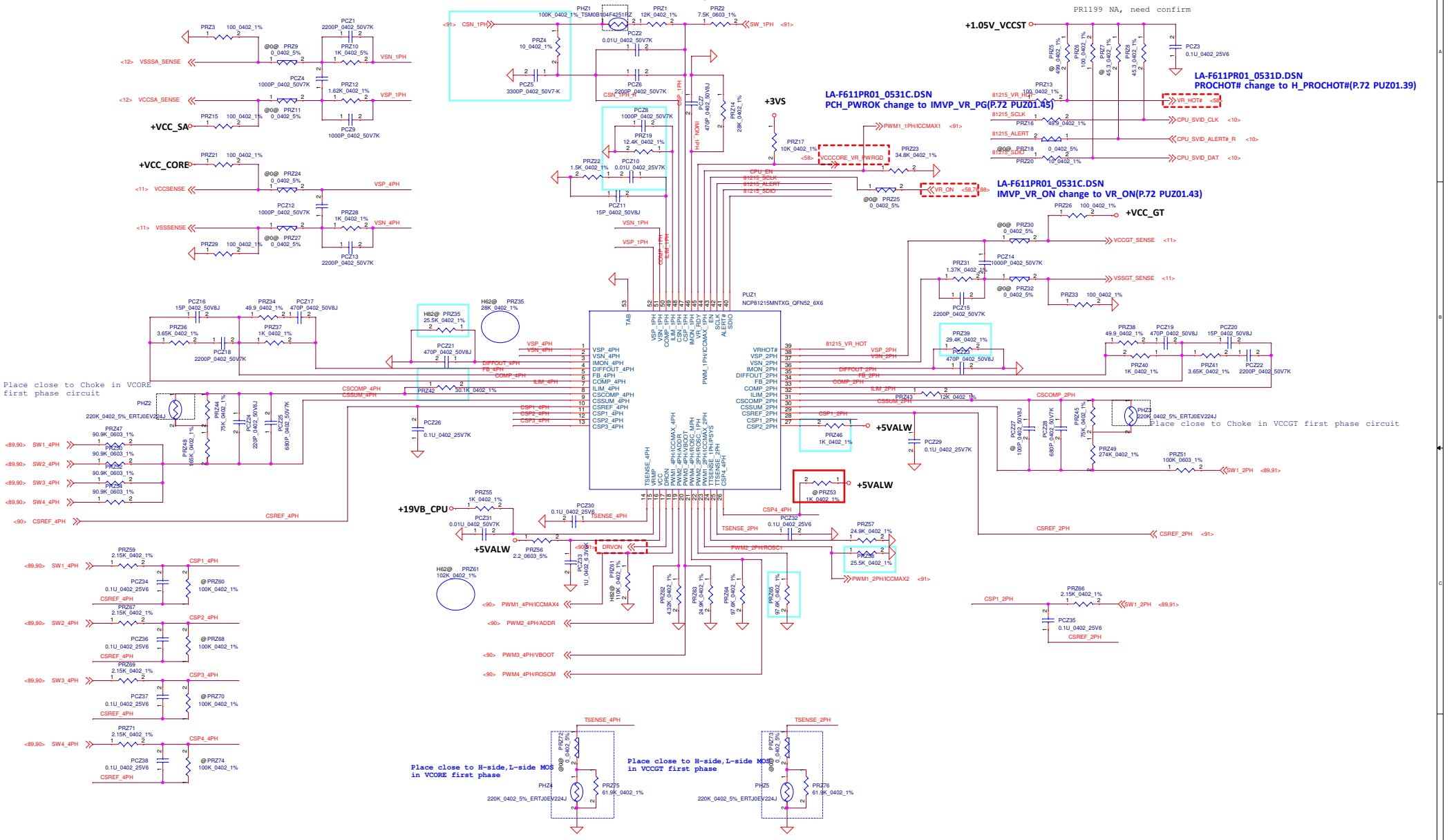
Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size: C | Document Number: 1.0VS_VCCIO | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 88 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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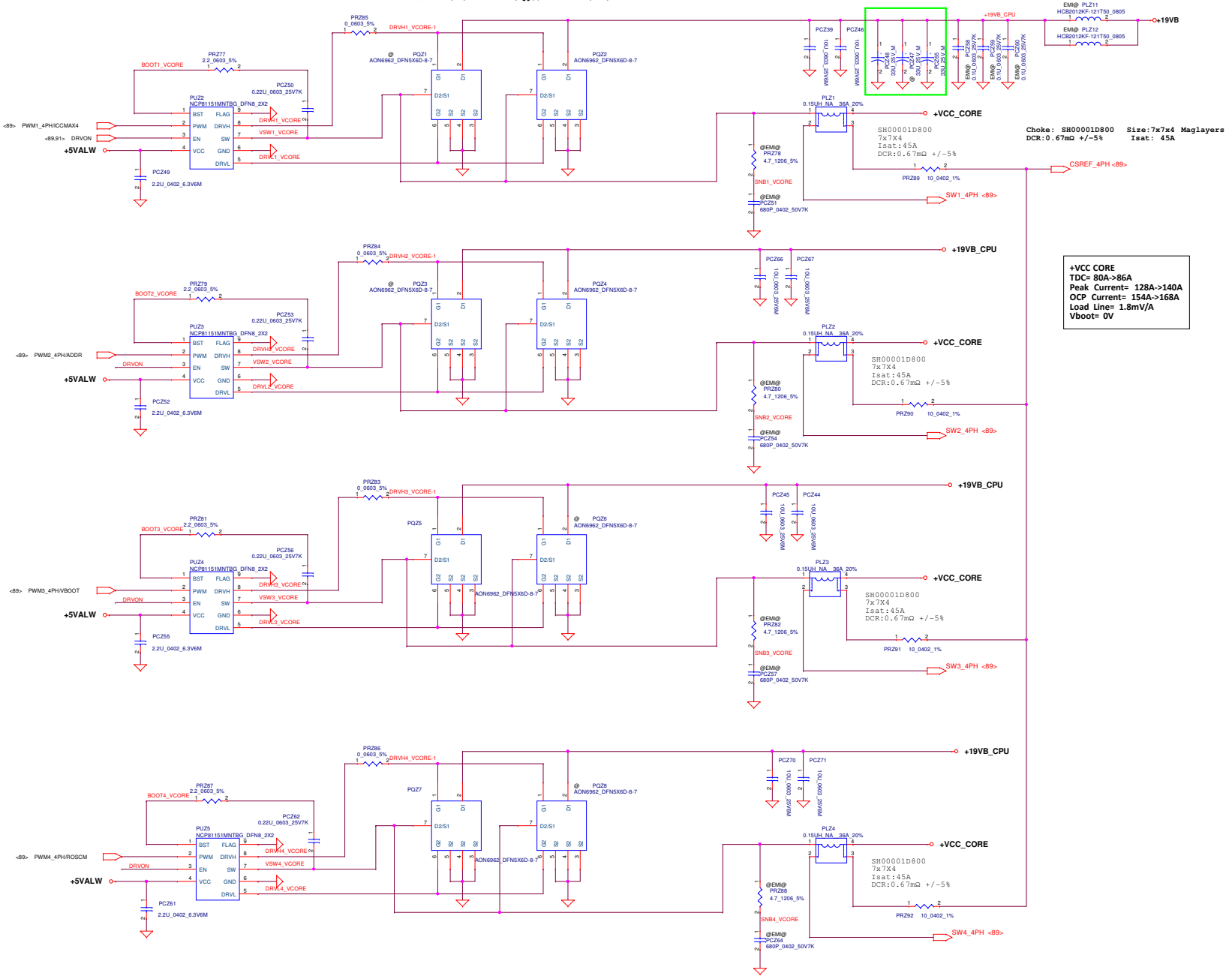
Size	Document Number	Rev
Custom	CPU IC SKL_H 42	1A
Date: Friday, February 22, 2019	Sheet 89 of 100	

Main Func = CORE

MOSFET: DFN 5X6E
H/S Rds(on): 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on): 0.8mohm(Typ), 1.05mohm(Max)



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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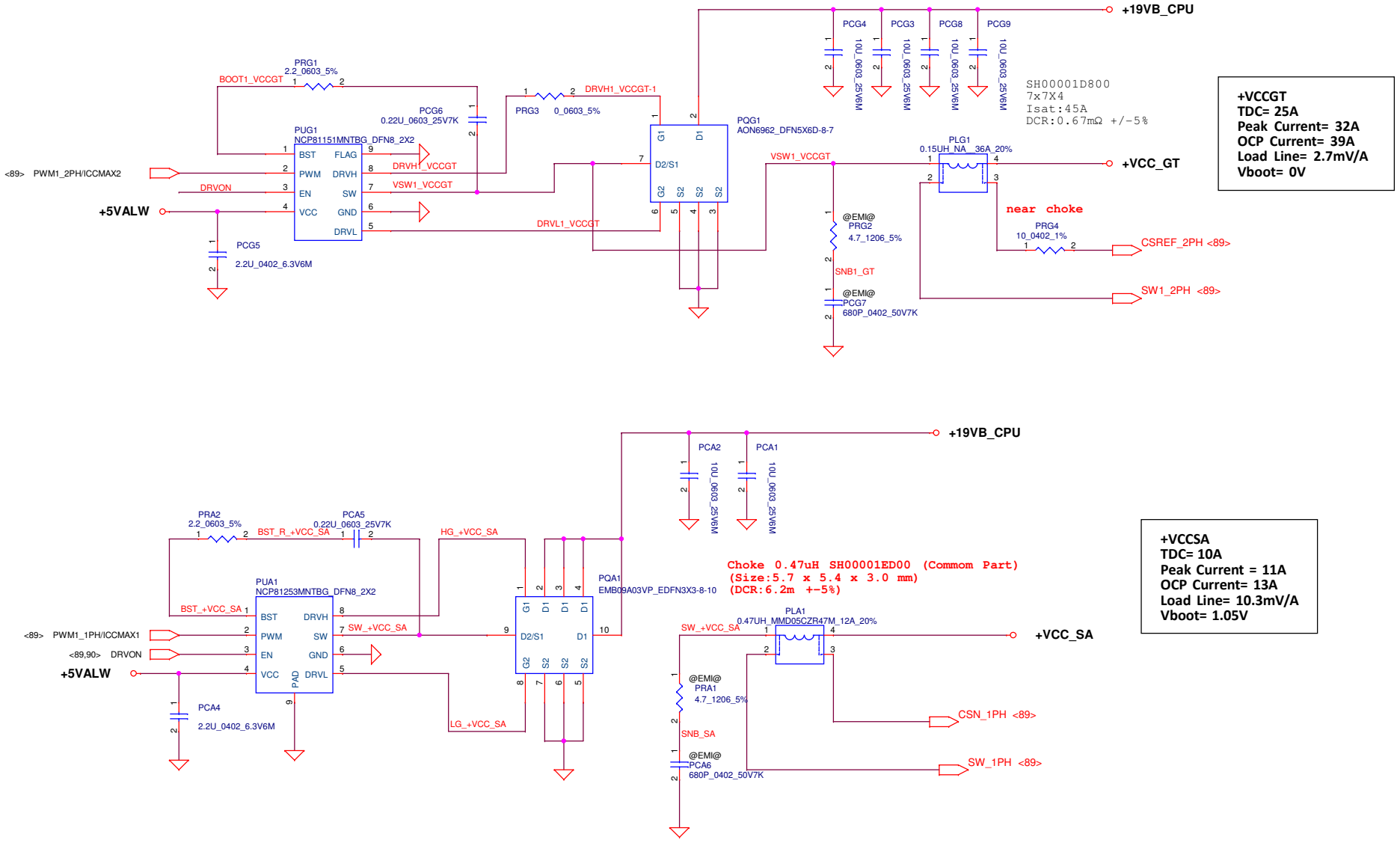
Title	CPU_CORE		
Size	Document Number		Rev
Custom			1A
Date:	Friday, February 22, 2019	Sheet	90 of 100

Main Func = VCCGT/+VCCSA



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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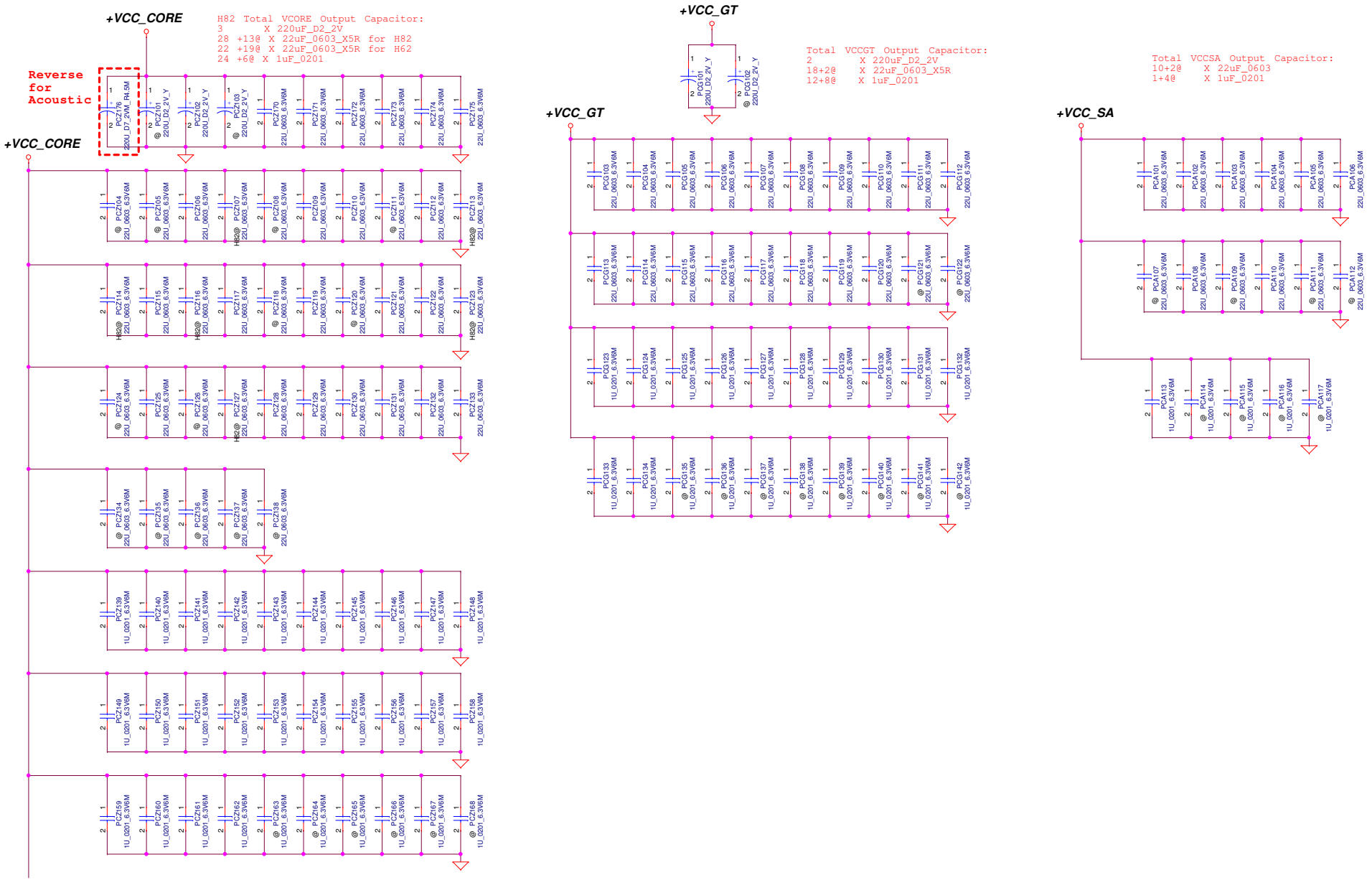
Compal Electronics, Inc.		
Title	+VCC_GT/+VCC_SA	
Size	Document Number	Rev
	C1PRG_LA-E051P	1A
Date: Friday, February 22, 2019	Sheet 91 of 100	



Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

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Compal Electronics, Inc.

Title: DH53F M/B LA-F991P

Size	Document Number	Rev
Custom		1A

Date: Friday, February 22, 2019 Sheet 92 of 100

Samesung VRAM
When,VRAM_VDD_CTL=High
Vboot=Vref*R2/(R1+R2+80)
=2*35.7K/(10K+35.7K+80)
=1.56V
When,VRAM_VDD_CTL=Low
Vboot=Vref*R2/(R1+R2+80)
=2*(35.7K//52.3K)/(10K+(35.7K//52.3K)+80)
=1.356V

Micron & Hynix VRAM
When,VRAM_VDD_CTL=High
Vboot=2*30.9K/(10K+30.9K+80)
=1.51V
When,VRAM_VDD_CTL=Low
Vboot=2*(30.9K//68.1K)/(10K+(30.9K//68.1K)+80)
=1.36V

MOSFET: DFN 5X6E
H/S Rds(on): 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on): 0.8mohm(Typ), 1.05mohm(Max)

+1.35VSDGPU
TDC 14A
Peak Current 20A
OCP current 30A
fsw=400kHz

13X8X4
Isat:55A
DCR:1.3mΩ (+/-5%)

+1.35VSDGPU

Rref1
Rref2
REFADJ
REF1
RBOOT
REF2

PUW1 RT8816BGQW_WQFN20_3X3
POW1 AOE6930_DFN5X6E8-10
PLW1 0.47UH_MHT-MHDZIR47MEM1-RT_30A_20%
PLW11 FBMA-L11-201209-800LMA50T

Rocset for 75.6A

for cost 權後換30U 改 回 20

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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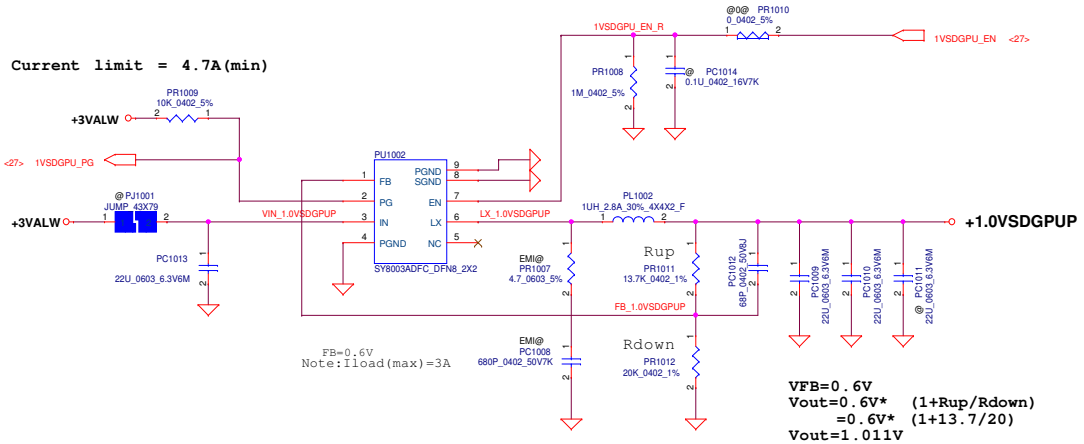
Compal Electronics, Inc.

Title: **PWR_+1.5VRAM**

Size | Document Number | Rev 1A

Date: Friday, February 22, 2019 | Sheet 93 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

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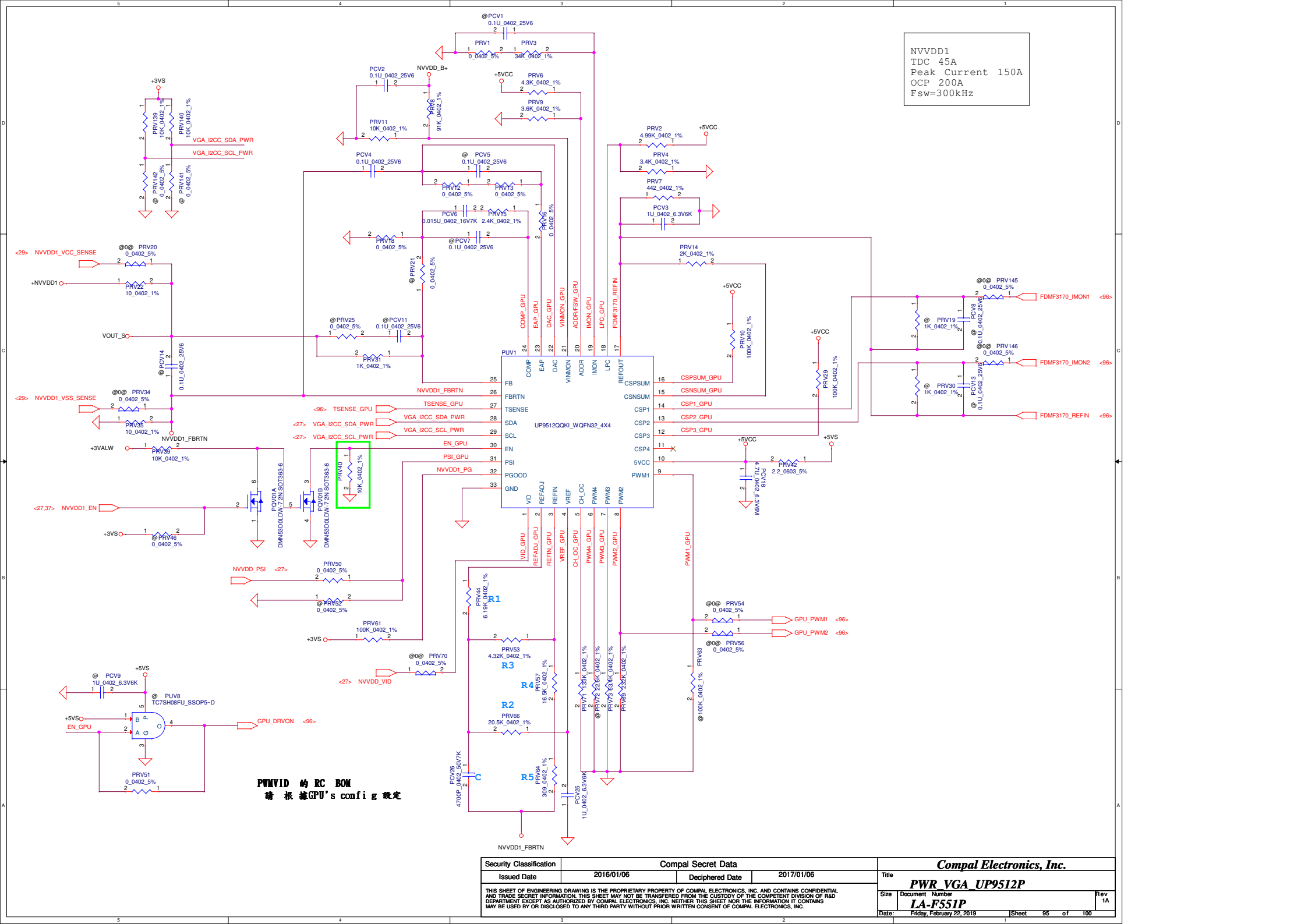
Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
C	DH53F M/B LA-F991P	1A

Date: Friday, February 22, 2019 Sheet 94 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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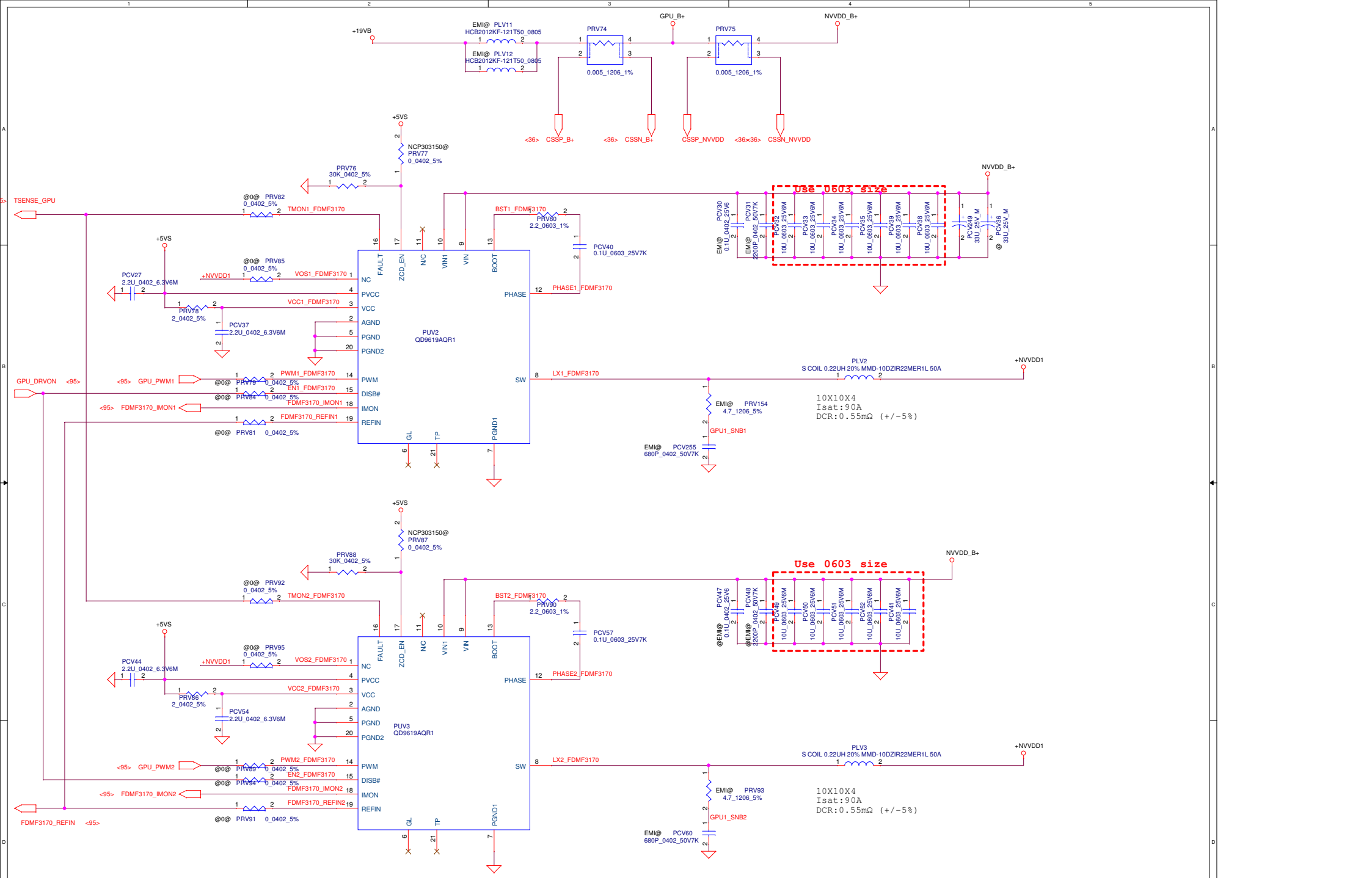
Compal Electronics, Inc.	
Title	PWR_VGA_UP9512P
Size	Document Number: LA-F551P
Rev	1A
Date:	Friday, February 22, 2019
Sheet	95 of 100



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

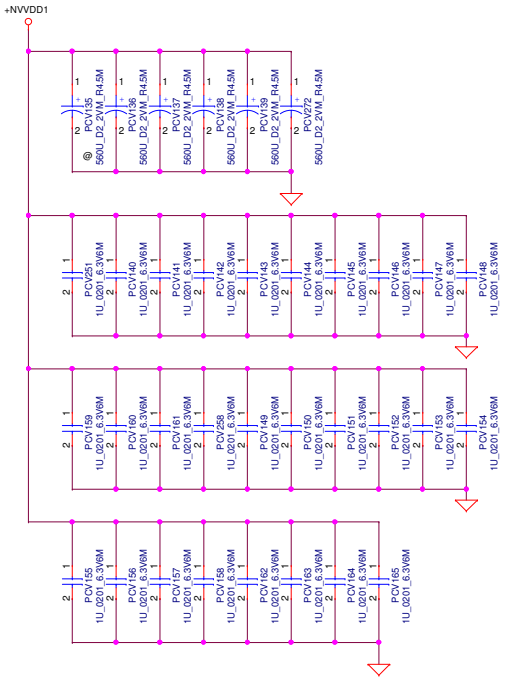
Title: **PWR_+NVVDD1**

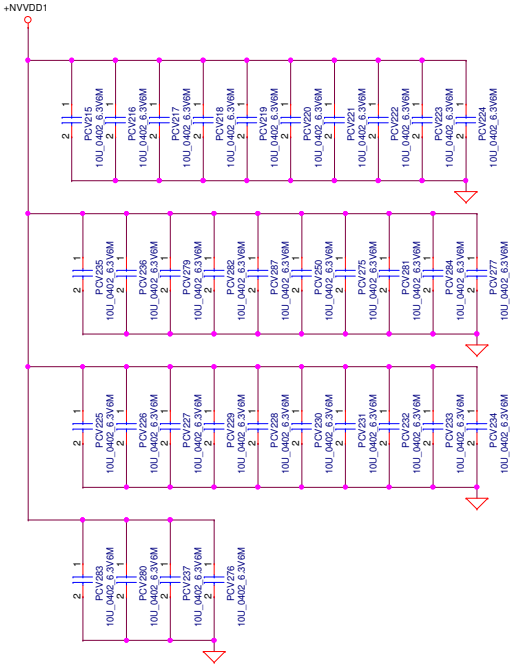
Size	Document Number	Rev
	LA-F551P	1A

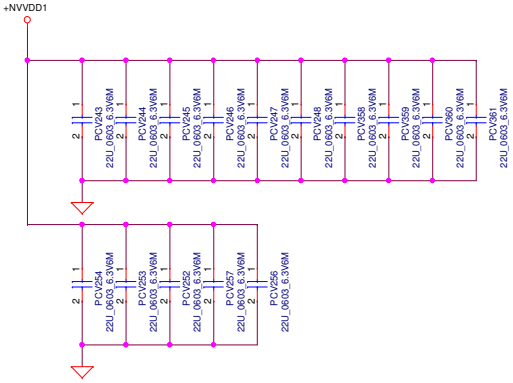
Date: Friday, February 22, 2019 | Sheet 96 of 100

N18P-G0
+NVVDD
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)







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Title: **PWR_VGA DECOUPLING**

Size	Document Number	Rev
	LA-F551P	1A

Date: Friday, February 22, 2019 | Sheet 97 of 100

Reserve Page

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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Title: *N18E-GDDR6_D*

Size | Document Number: *EH5VF M/B LA-H501P* | Rev: 1A

Date: Friday, February 22, 2019 | Sheet 98 of 100

Reserve Page

Security Classification	Compal Secret Data		
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Title	*N18E-GDDR6_D*	
Size	Document Number *EH5VF M/B LA-H501P*	Rev 1A
Date: Friday, February 22, 2019	Sheet 99 of 100	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PRG5 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Chnage the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B

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Size: Custom | Document Number: EH5VF M/B LA-H501P | Rev: 1A
Date: Friday, February 22, 2019 | Sheet 100 of 100

Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	6	Chipset	11/14	Update CPU,PCH,GPU PN.		DVT	0.2
2	43,68, 71,72	Source	11/14	Change material source.	1.Change CS95,CM3,CM20,CS5,CS111 to SGA00003700.	DVT	0.2
3	58	EC	11/14	Design change.	1.Add CB14 on EC_RST#.	DVT	0.2
4	27,37	GPU	11/14	Design change and fine tune sequence.	1.Remove RV397, pop RV335. 2.Reserve CV400, change RV106 to 100kohm. 3.Change RV105 to 10kohm, CV197 to 0.22uF, depop DV4. 4.Change RV22 to 200kohm. 5.Change UV45,UV48 to SA000070V00.	DVT	0.2
5	66	Sensor	11/15	Design change.	1.Remove R39,R40,C41,U6.	DVT	0.2
6	58	EC	11/16	Board ID.	1.Change RB3 to 12kohm.	DVT	0.2
7	43,56	Source	11/16	Change material source.	1.Change CS13 to SE00000X200,0603 size. 2.Change DS19 to SCA00004500. 3.Change LA4,LA5 to SM01000BW00. 4.Change UF2 to SA000067P00. 5.Change QV3,QV4 to SB00001GC00. 6.Change UH3 to SA00000OH00. 7.Change UC3 to SA00007WE00.	DVT	0.2
8	32	VRAM	11/19	For N17P-G0-K1 SKU.	1.Change UV4 related component BOM structure to VRAM4G@.	DVT	0.2
9			11/20	Design change.	1.Change RV338,RH94,RH96,RH99,RH101,RH102,RH103,RH105,RX8,RX9 to R-short.	DVT	0.2
10	67	HDD	11/20	Follow DVR1012,HDD CONN P11 pull-down.	1.Add RO25, remove T211.	DVT	0.2
11	10	ESD	11/21	For ESD request.	1.Add CC101,CC102,CC103, change CD10 to 33pF and pop.	DVT	0.2
12	27,51	Crystal	11/21	By Crystal EA result.	1.Add RL14, change CL21,CL22 to 18pF. 2.Change RV80 to 470ohm, CV1,CV2 to 18pF.	DVT	0.2
13	43	TYPEC	11/23	Update CONN symbol.	1.Change JTYPEC1 to DC23300RC00.	DVT	0.2
14	42,43 ,58	TYPEC	12/18	Follow 2018 Type-C spec.	1.Remove RS127, add US14. 2.Remove TYPEC_1P5A net from PCH. 3.Add TYPEC_1P5A_EC net from EC. 4.Add RS137.	DVT	0.3
15	36	GPU	12/18	OVRM issue.	1.Change RV399 power source to +3VLP. 2.Change RV345~RV348,RV370,RV371,RV372,RV374 power rail to +3V_OVRM. 3.Add QV16,RV400,OVRM_EN net to EC/PCH, reserve RH261.	DVT	0.3
16	58	EC	12/18	Update board ID.	1.Change RB3 to 15k.	DVT	0.3
17			12/27	Design change.	1.Change RA7,RQ1,RQ2,RQ3,RQ4,RQ8,RV352,RV353,RV356,RV358,RV362,RV364,RV365 ,RV382,RM53 to R-short.	PVT	1.0
18	63,77	ESD/EMI	01/03	For ESD/EMI request.	1.Reserve DK2,CK6,CK7 for ESD. 2.Add SPRING1~3 for EMI.	PVT	1.0
19	58	EC	01/03	Update board ID.	1.Change RB3 to 20k.	PVT	1.0
20	66	ESD	01/31	For ESD request.	1.Add C60.	PVT	1A

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Date: Friday, February 22, 2019 | Sheet 101 of 101