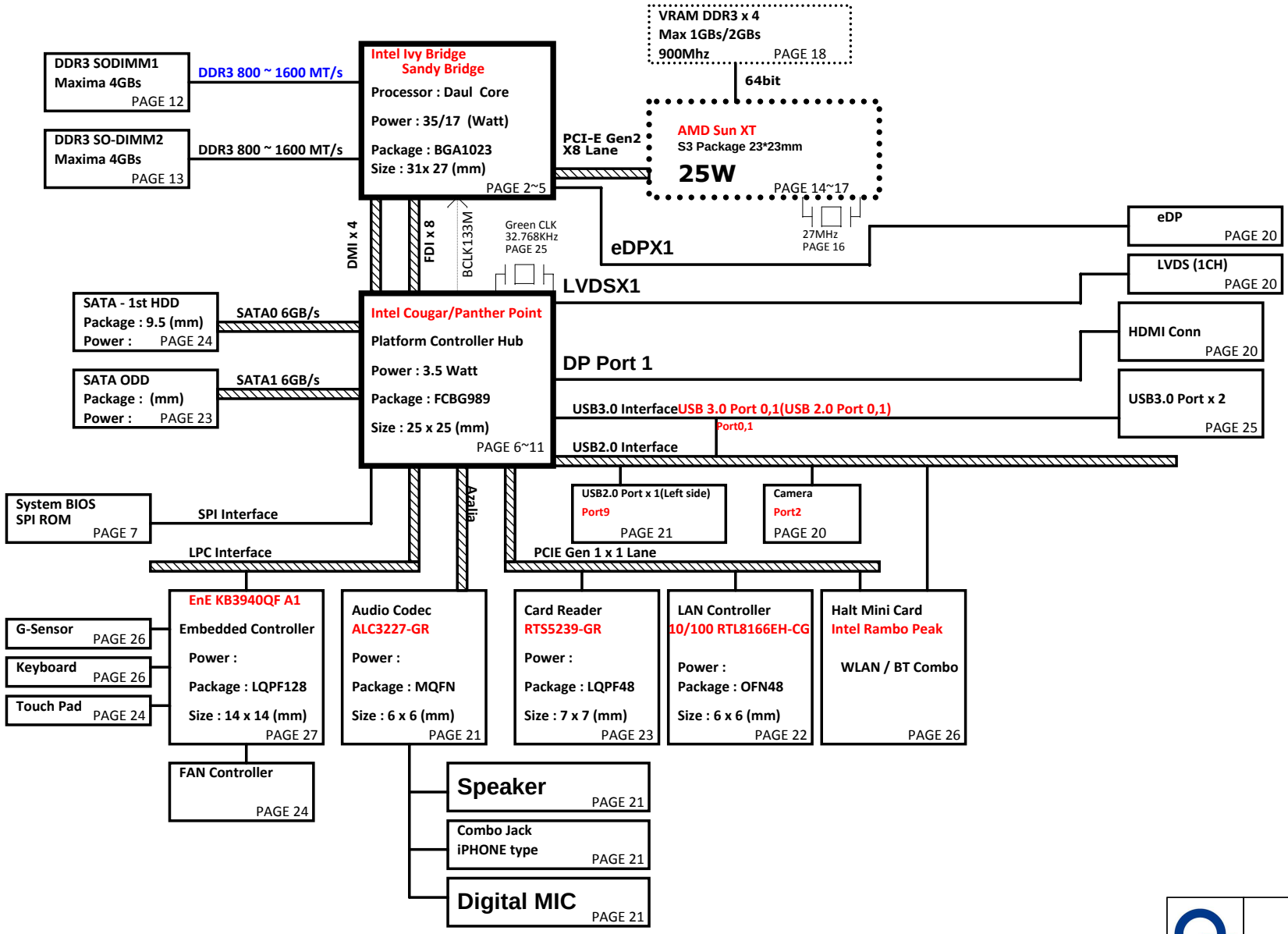
U81 DIS/UMA (14"/15.6") Ultra/Slim
Intel Chief River Platform Block Diagram

01

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT :U81
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Size	Document Number	Rev
Custom	Block Diagram	1A

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Ivy Bridge Processor (DMI,PEG,FDI)

02

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

+1.5V_CPU (4,10,21,26)
+1.5VSUS (4,12,13,31,37)
+1.05V (4,6,7,8,10,26,27,30,33)
+3V_DEEP_SUS (6,7,8,9,10,35)
+3V (6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36)

10/30:reserved for eDP

10/30:modify for eDP

10/9: for reserve

Placement close to EC.

PEG x8

CPU RESET#

Intel DG request

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

DDR3 DRAM RESET

for DS3

PV shortpad

SM_DRAMPWROK
Processor Input.

Processor pull-up (CPU)

eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms

Local Thermal Sensor

PV change to Q29.1 for correct function

G781-1P8(9Ah)

Place under CPU heat pipe

For iFDIM
Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

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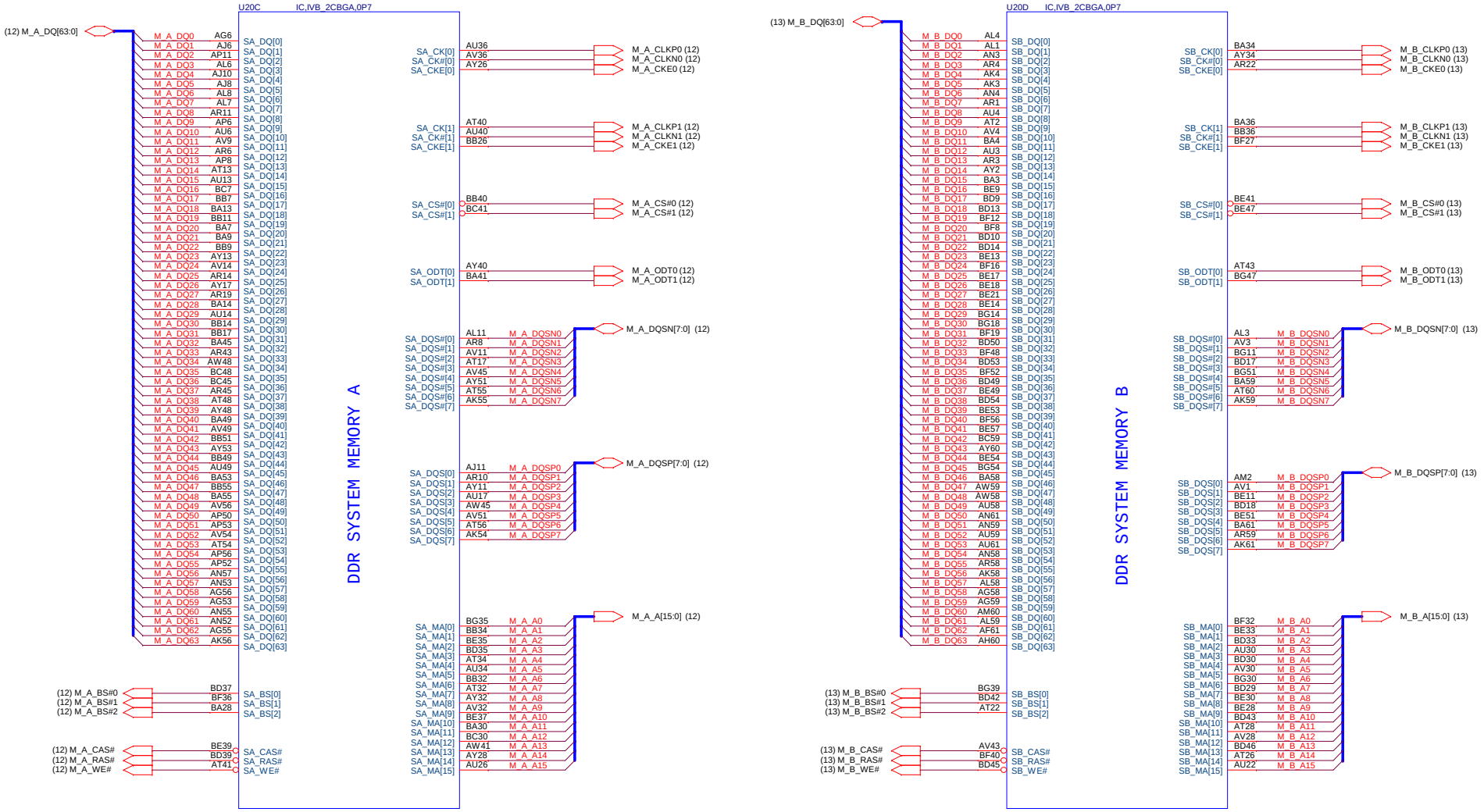
Custom	IVB 1/4 (DMI/PEG/FDI)	1A

Date: Friday, May 24, 2013 | Sheet 2 of 37

Ivy Bridge Processor (DDR3)



PROJECT :U81
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Size	Document Number	Rev
Custom	IVB 2/4 (DDR3 I/F)	1A

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POWER

POWER

04

U20F

U20G

IC,IVB_2CBGA,0P7

IC,IVB_2CBGA,0P7

CORE SUPPLY

PEG IO AND DDR IO

GRAPHICS

DDR3 - 1.5V RAILS

VREF

QUIET RAILS

1.8V RAIL

SA RAIL

SENSE LINES

SVID

VCCSA VID Lines

IVB:8.5A

330uFx2pcs bulk BOT
22uFx12pcs cavity_BOT
1uFx12pcs BGA TOP

330uFx2pcs bulk BOT
22uFx10pcs cavity_BOT
2.2uFx13pcs BGA TOP

330uFx3pcs bulk BOT
22uFx14pcs cavity_BOT
2.2uFx16pcs BGA TOP

Zo impedance: 27.4ohm

IVB: 1.5A

330uF x1, 10uF_8 x1, 1uF_4 x2

IVB: 6A

330uFx1, 10uFx4

100- ±1% pull-up to VCC near processor.

Zo impedance: 27.4ohm

Zo impedance: 55 ohm

R close to CPU

IVB: 5A

CPU center

CRB: 1uf*1

Zo:55 ohm

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

20mils width

+VDDR_REF_CPU and DDR_VTTREF must use 10mils width

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

CPU VDDQ

+VCC_CORE

+VCC_GFX

+1.05V

+1.8V

+1.5V_CPU

+1.5VSUS

+3VPCU

+VCCSA

PROJECT :U81
Quanta Computer Inc.

Size: Custom | Document Number: IVB 3/4 (POWER) | Rev: 1A

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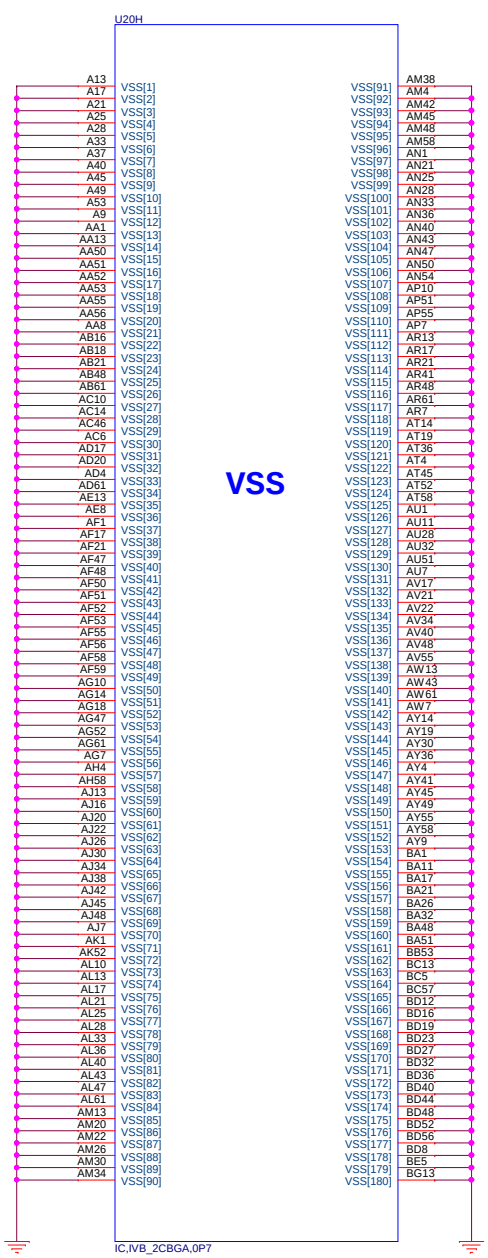
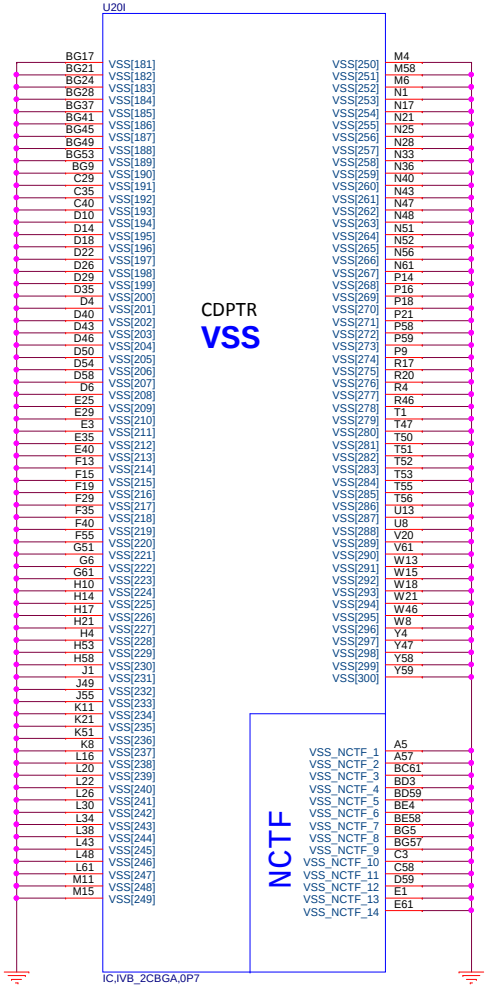
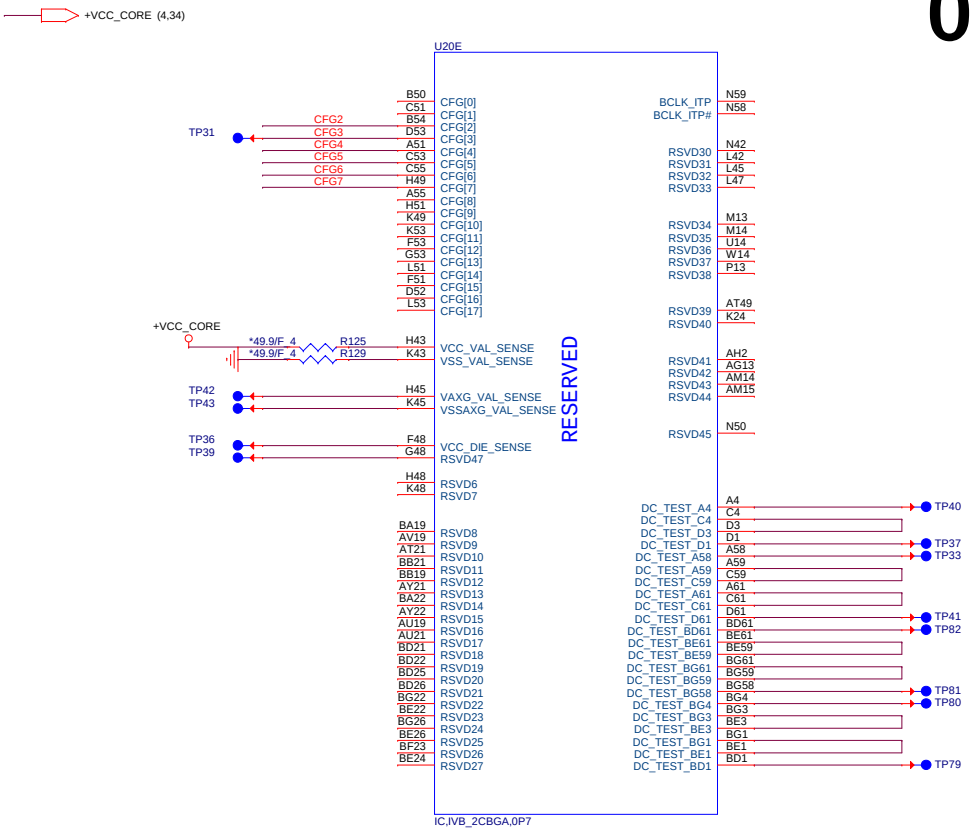
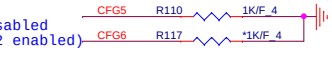






CFG[6:5] (PCIE Port Bifurcation Straps)

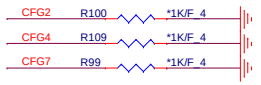
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



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Size	Document Number	Rev
Custom	IVB 4/4 (RSV,GND)	1A

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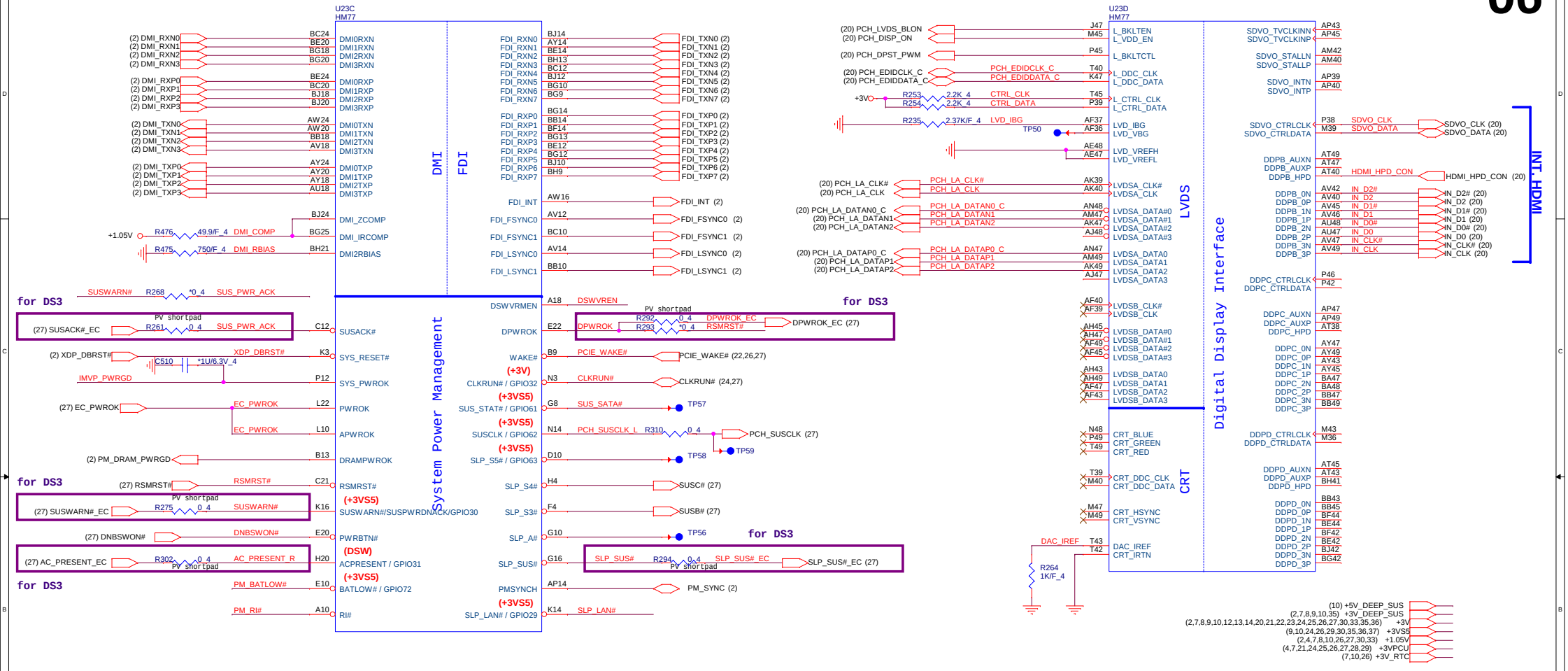
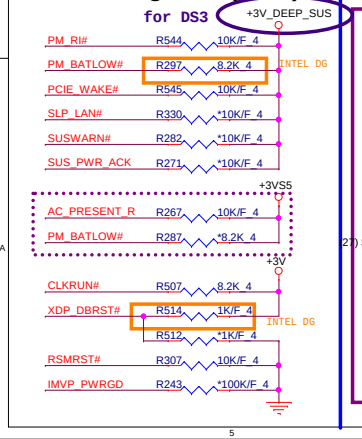
Cougar Point/Panther Point (DMI,FDI,PM)

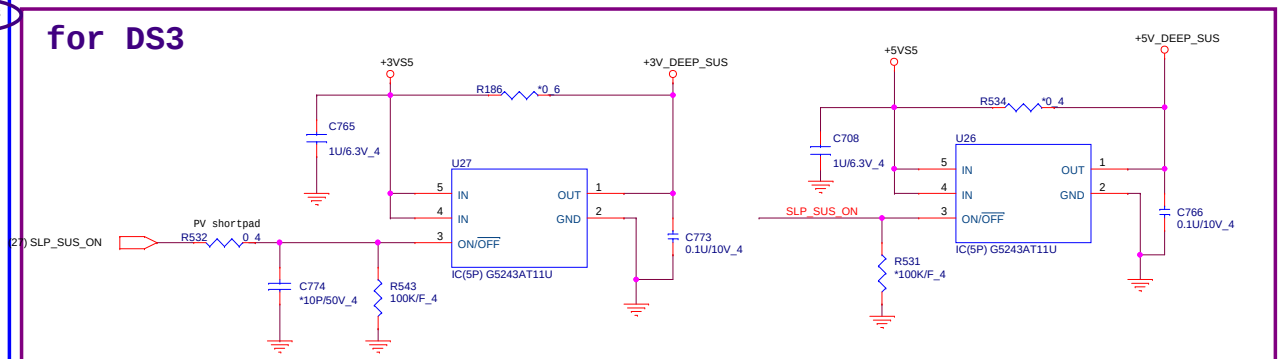
Cougar Point/Panther Point (LVDS,DDI)

06

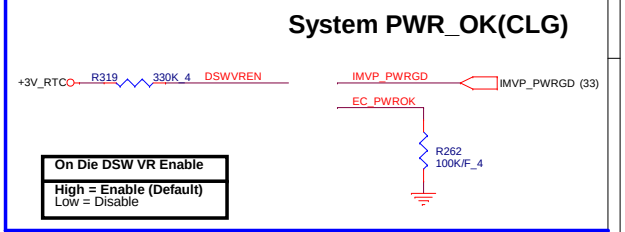


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



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Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
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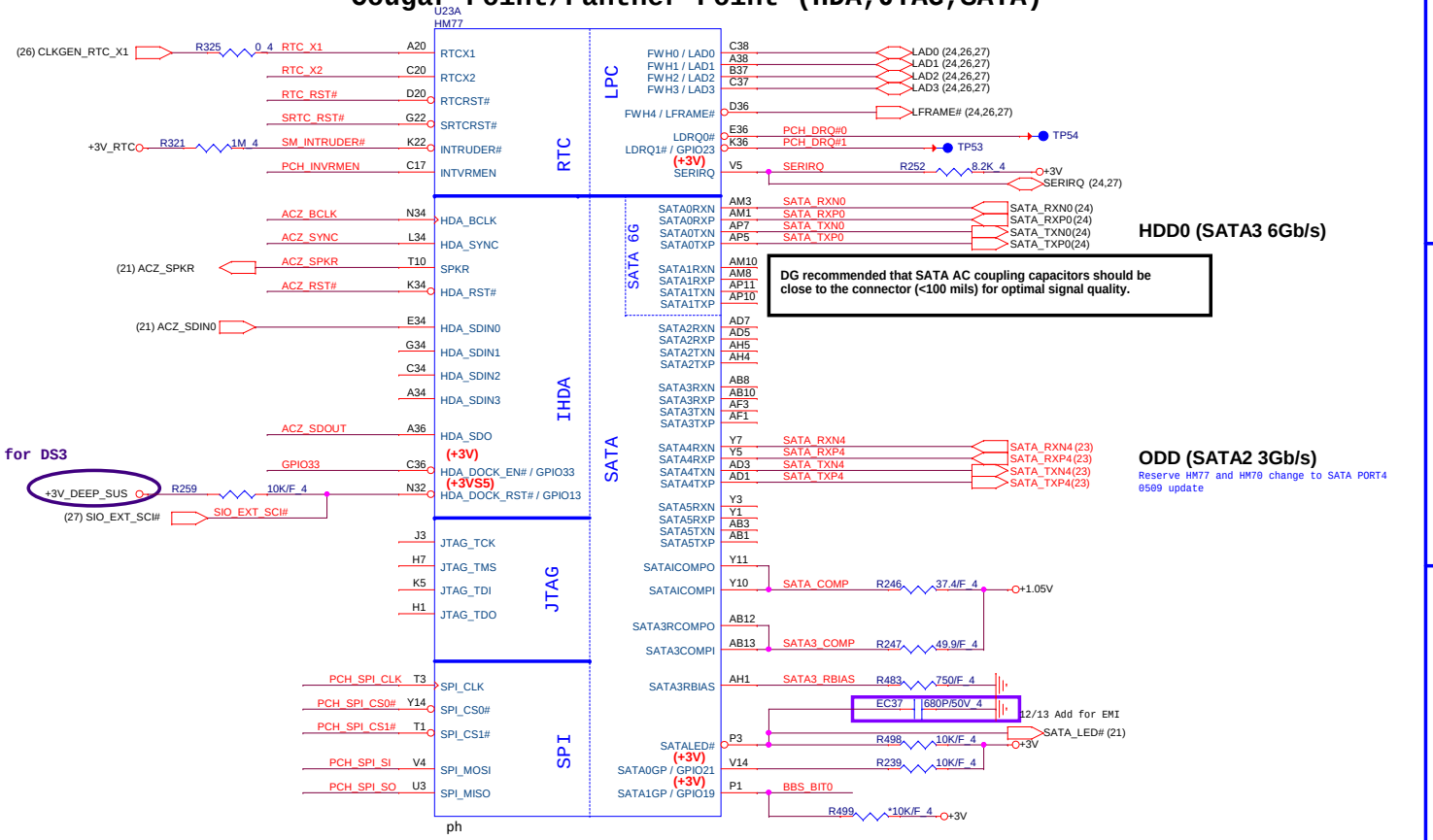
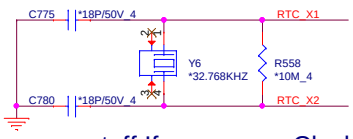
Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH Strap Table

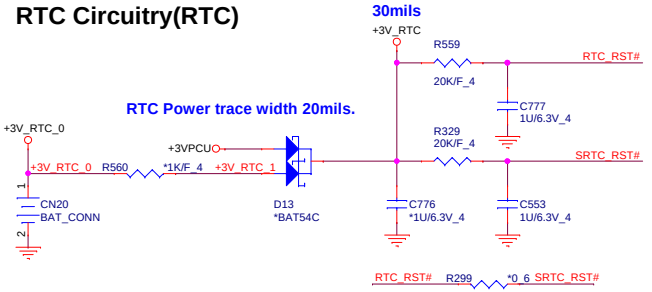
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

RTC Clock 32.768KHz

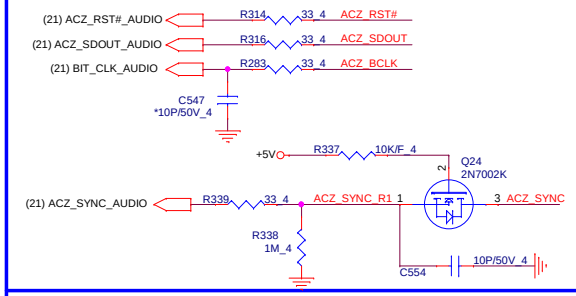


no stuff If use green Clock

RTC Circuitry(RTC)

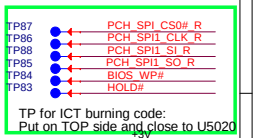


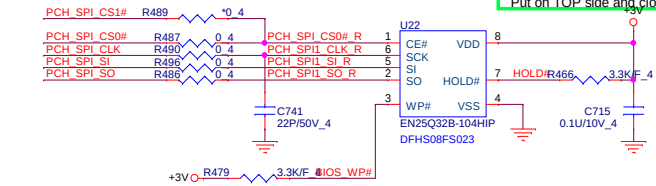
HDA Bus(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023(91960-0084L-8P-SOCKET)

PCH SPI ROM(CLG)





+3V (2,6,8,9,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36)
+5V (10,20,21,23,24,25,26,35)
+1.8V (4,10,31,37)
+1.05V (2,4,6,8,10,26,27,30,33)
+3VS5 (6,9,10,24,26,29,30,35,36,37)
+3VPCU (4,21,24,25,26,27,28,29)
+3V_RTC (6,10,26)

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Quanta Computer Inc.

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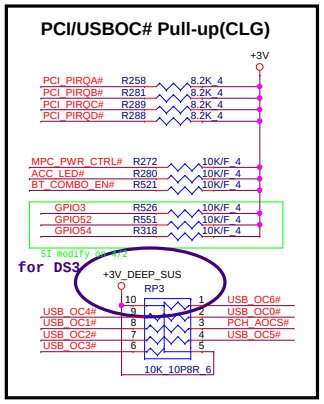
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

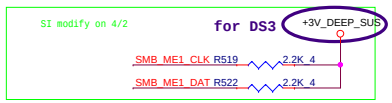
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

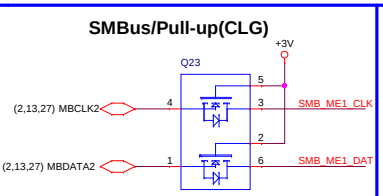
PCI/USBOC# Pull-up(CLG)



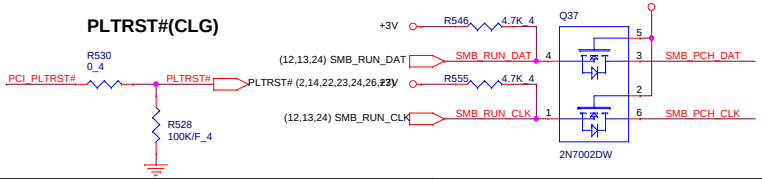
SMBus/Pull-up(CLG)



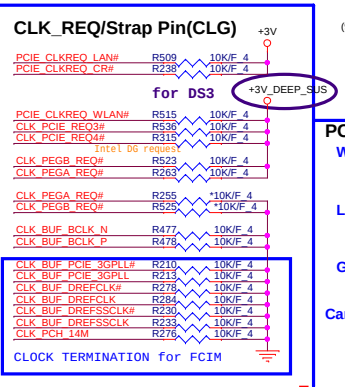
SMBus/Pull-up(CLG)



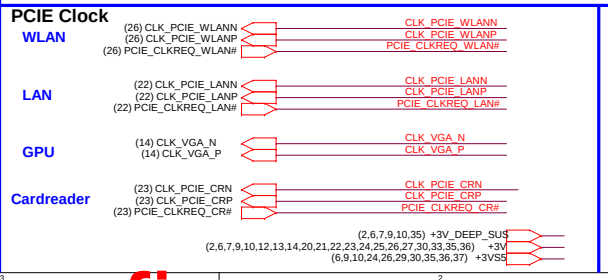
PLTRST#(CLG)



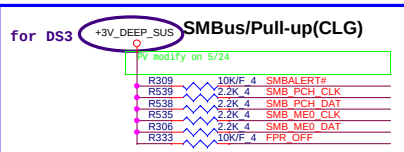
CLK_REQ/Strap Pin(CLG)



PCIE Clock



SMBus/Pull-up(CLG)



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Quanta Computer Inc.

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Custom	PCH 3/6 (PCIE/USB/CLK)	1A
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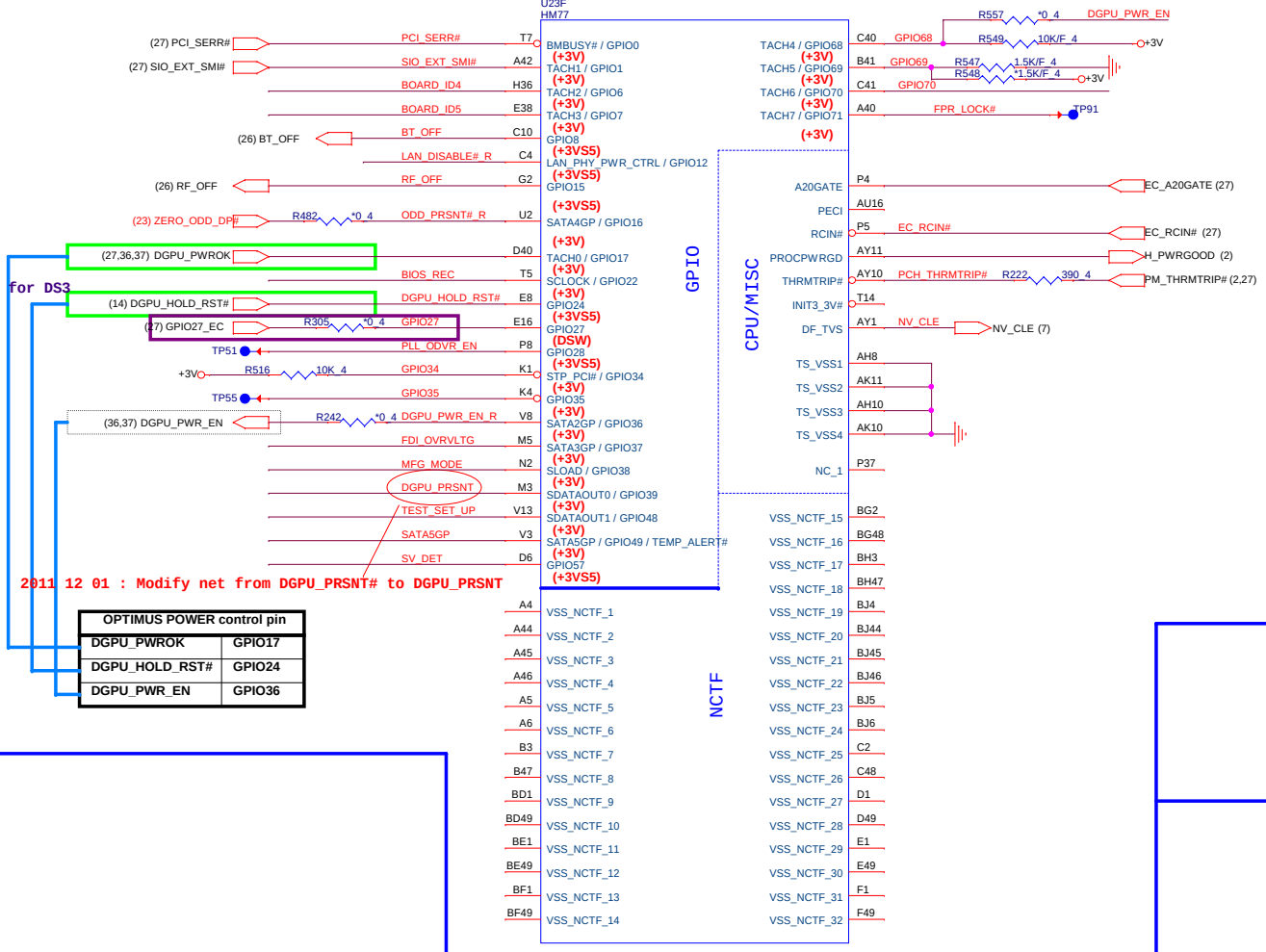
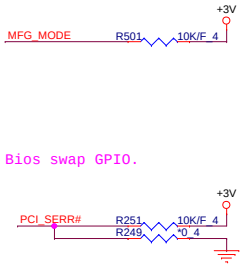
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09

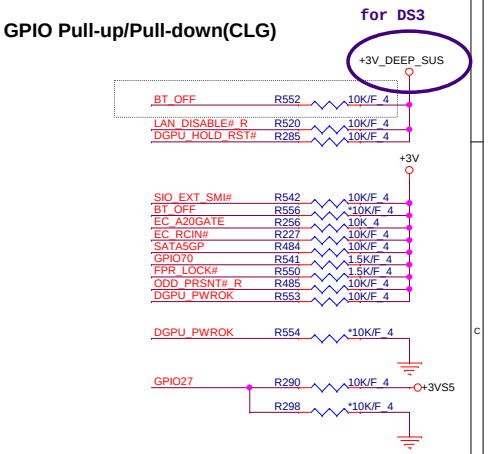


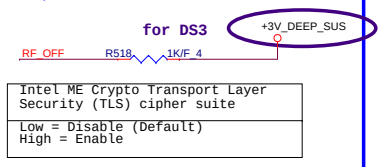
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

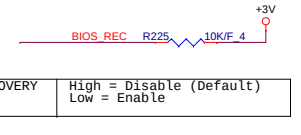
MFG-TEST

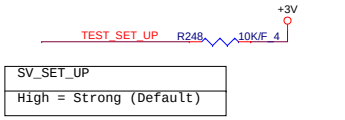


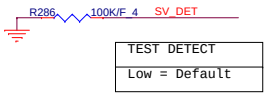
GPIO Pull-up/Pull-down(CLG)

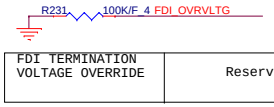






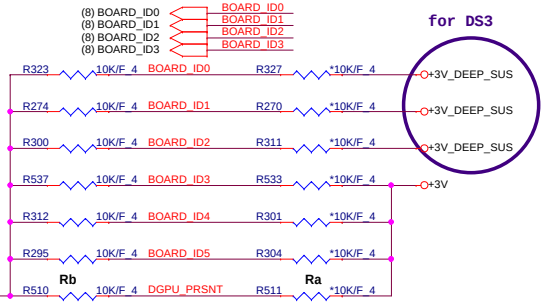






Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA: 0 DIS: 1
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

(2,6,7,8,10,35) +3V_DEEP_SUS
(2,6,7,8,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36) +3V
(6,10,24,26,29,30,35,36,37) +3VS5

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Custom	PCH 4/6 (GPIO/MISC)	1A

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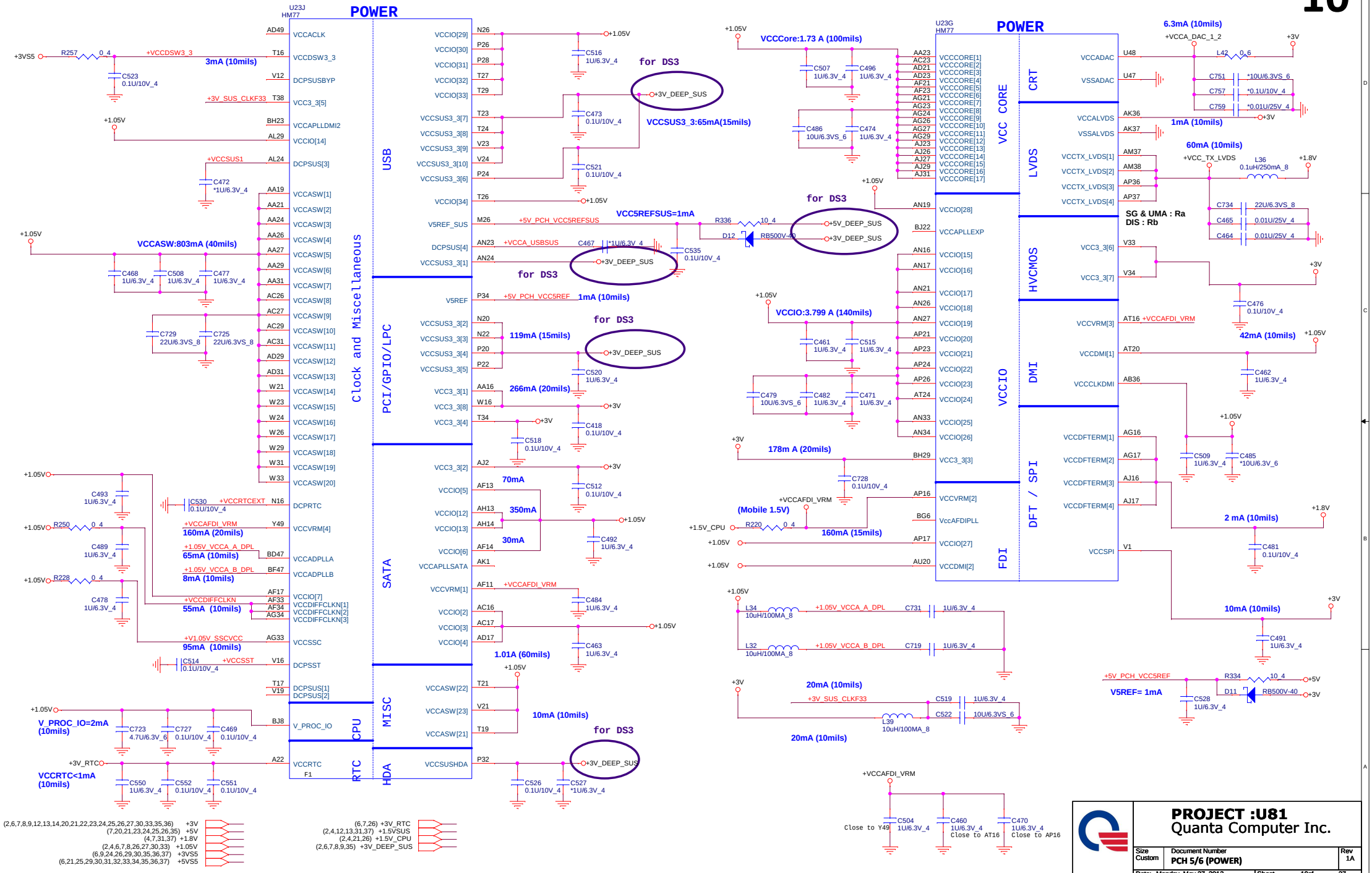
Cougar Point/Panther Point (POWER)



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Quanta Computer Inc.

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Custom	PCH 5/6 (POWER)	1A

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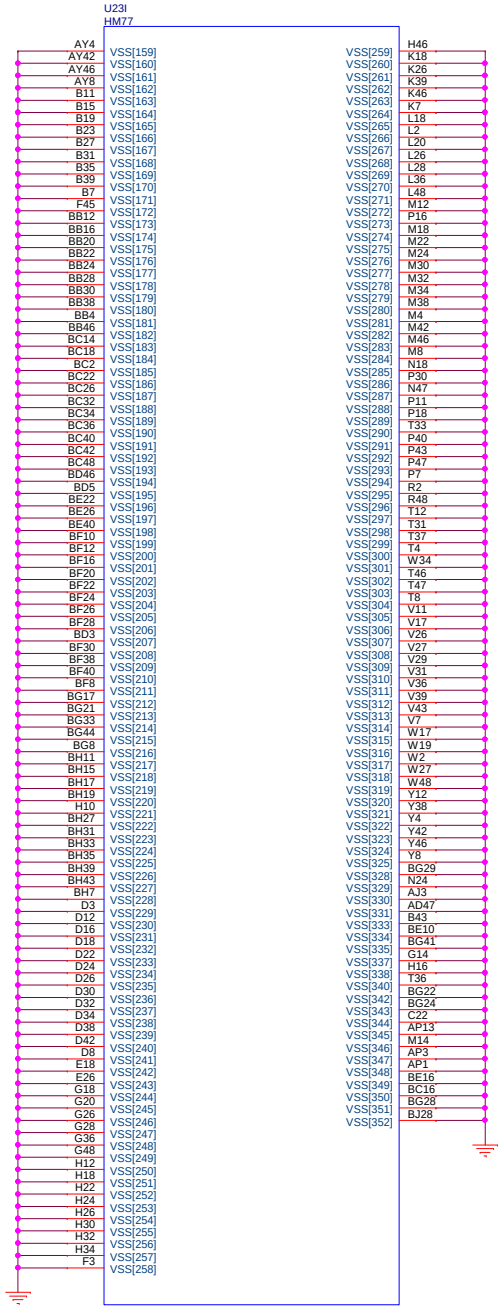
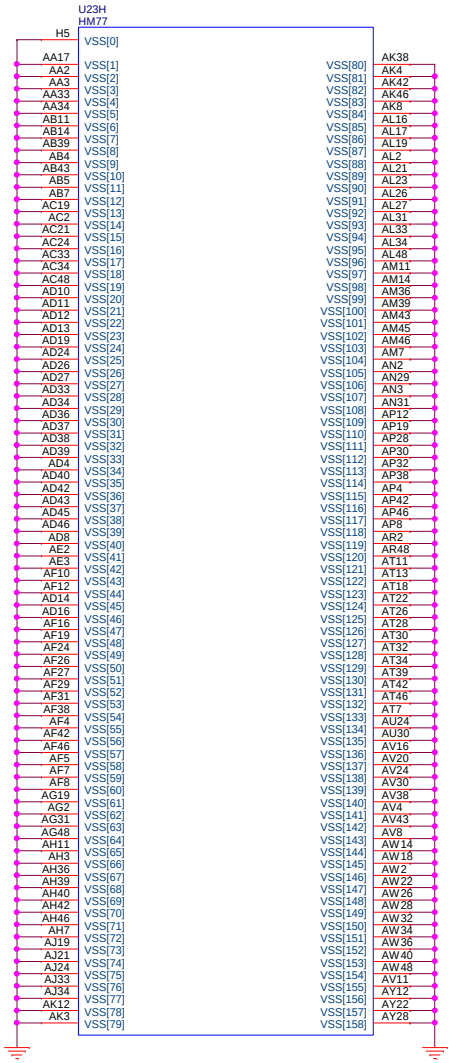
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



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Quanta Computer Inc.

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Custom	PCH 6/6 (GND)	1A

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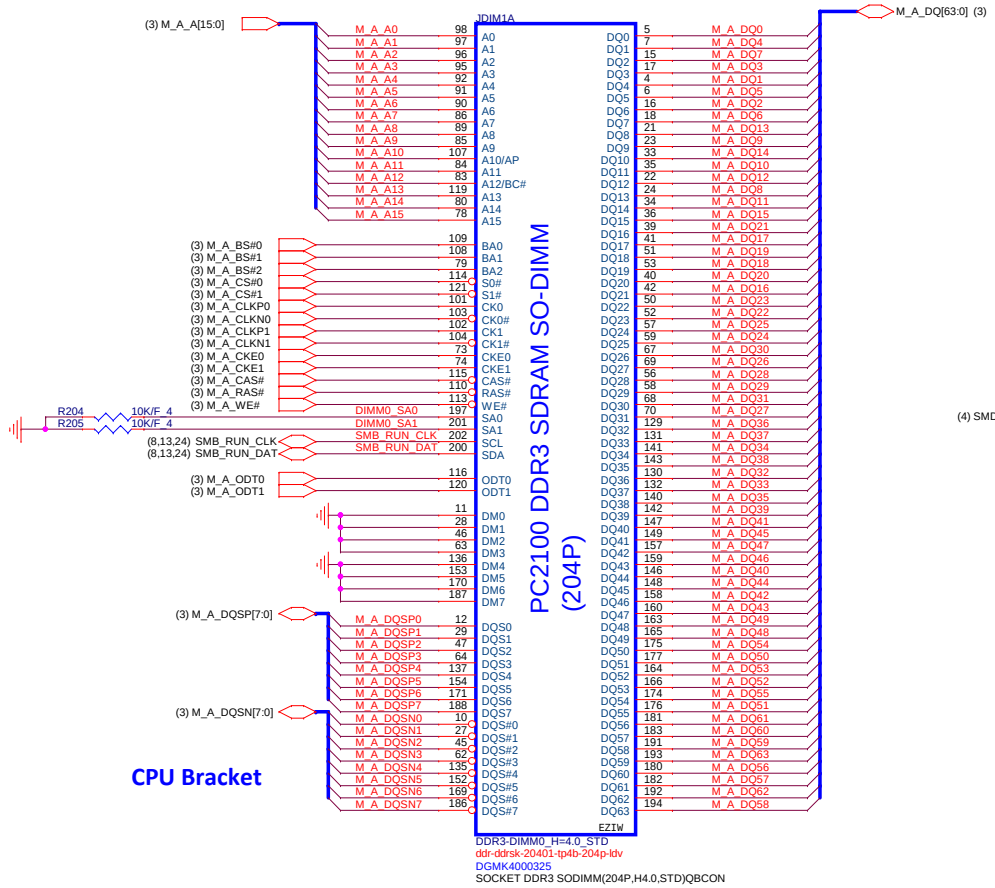

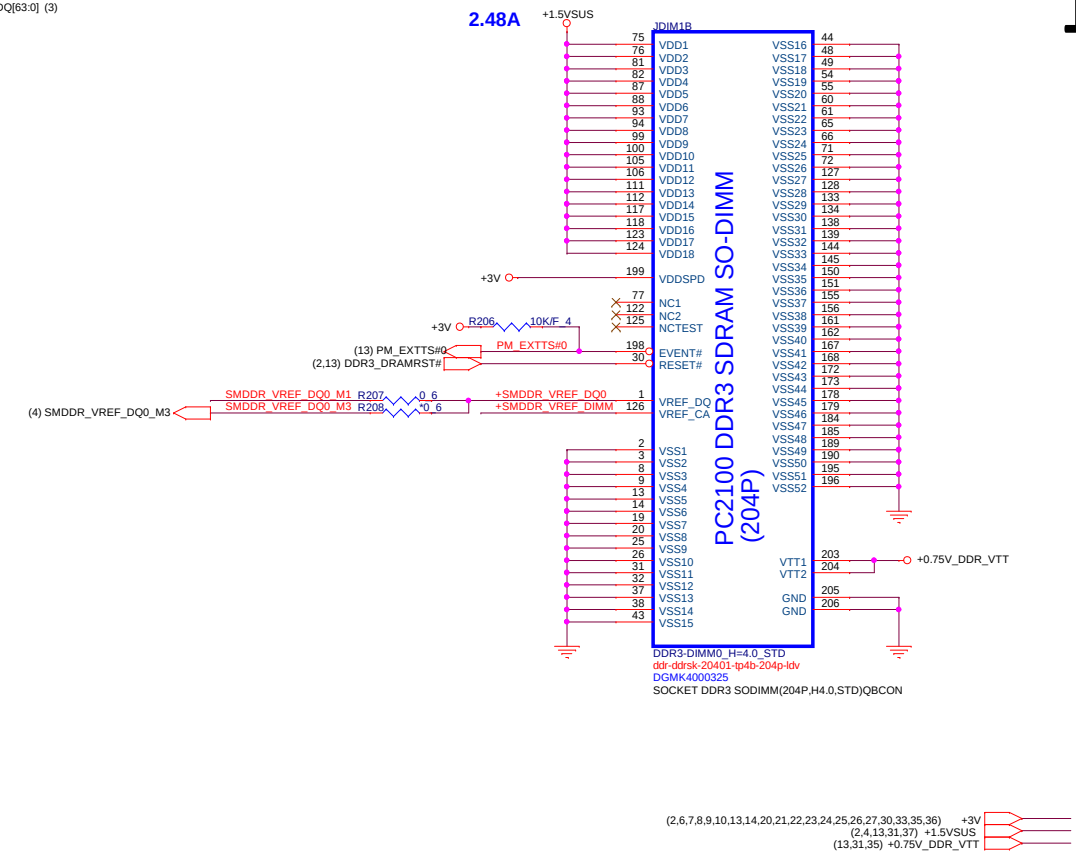

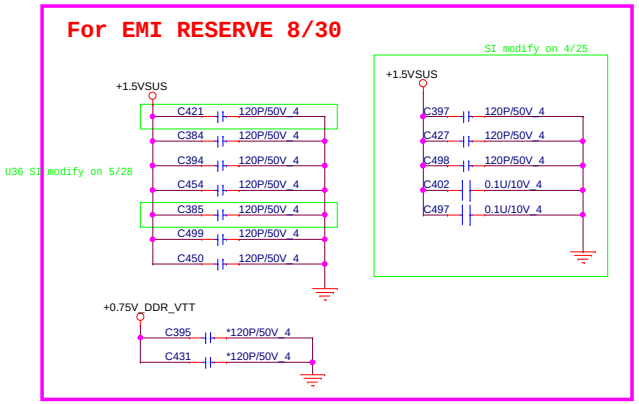

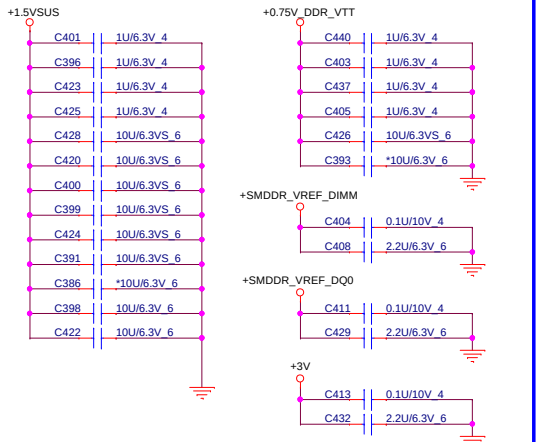

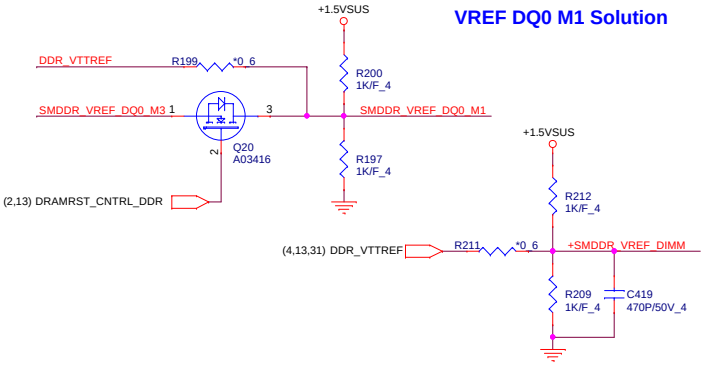

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
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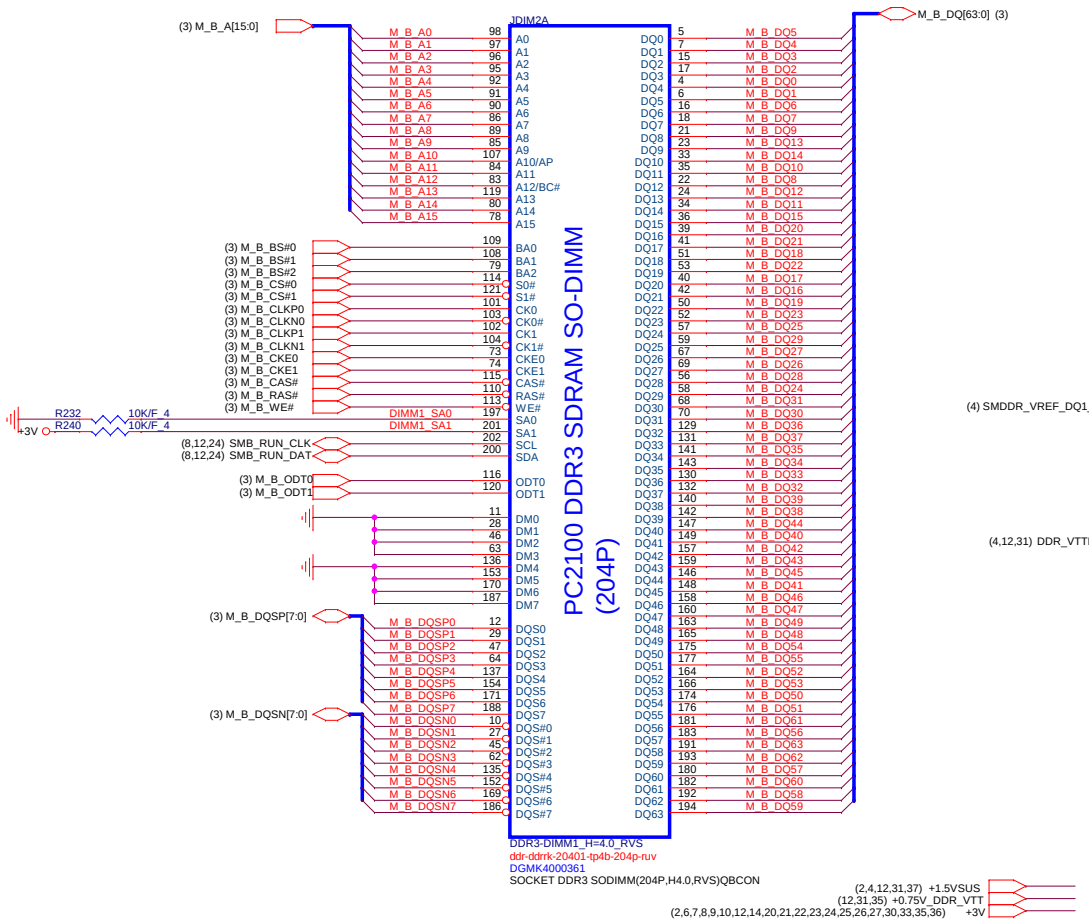
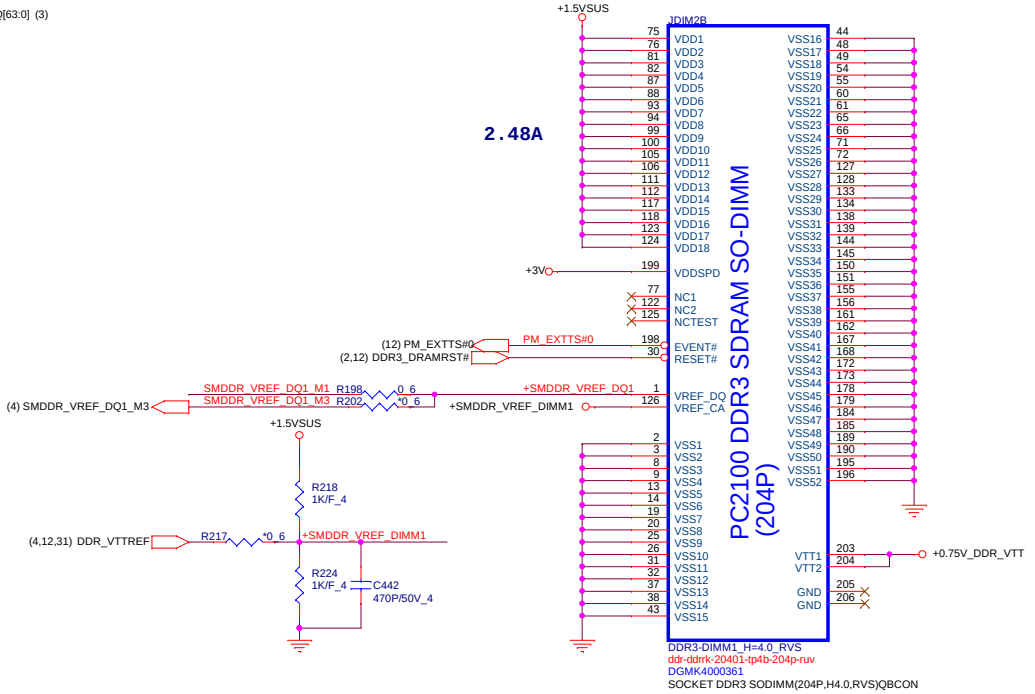
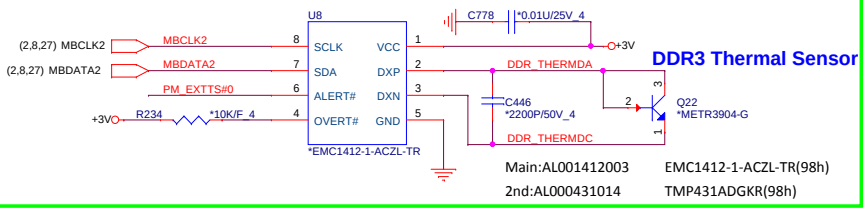


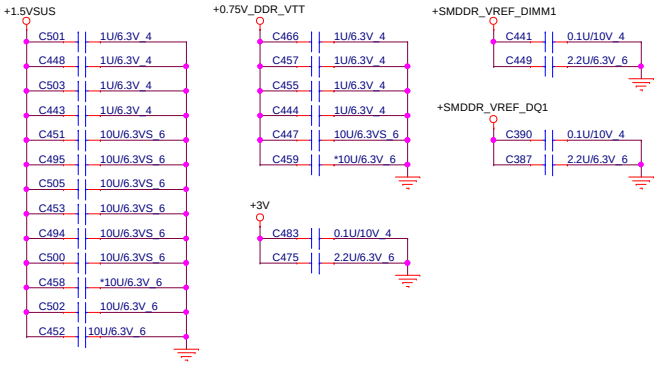


10/23:add for DDR Thermal Sensor

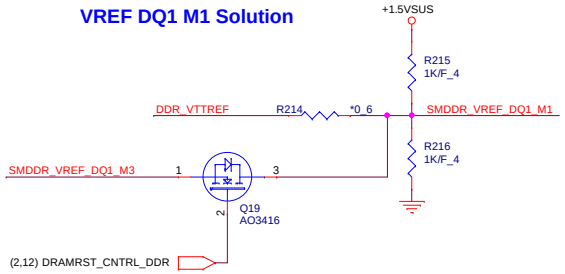
Local Thermal Sensor



Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A
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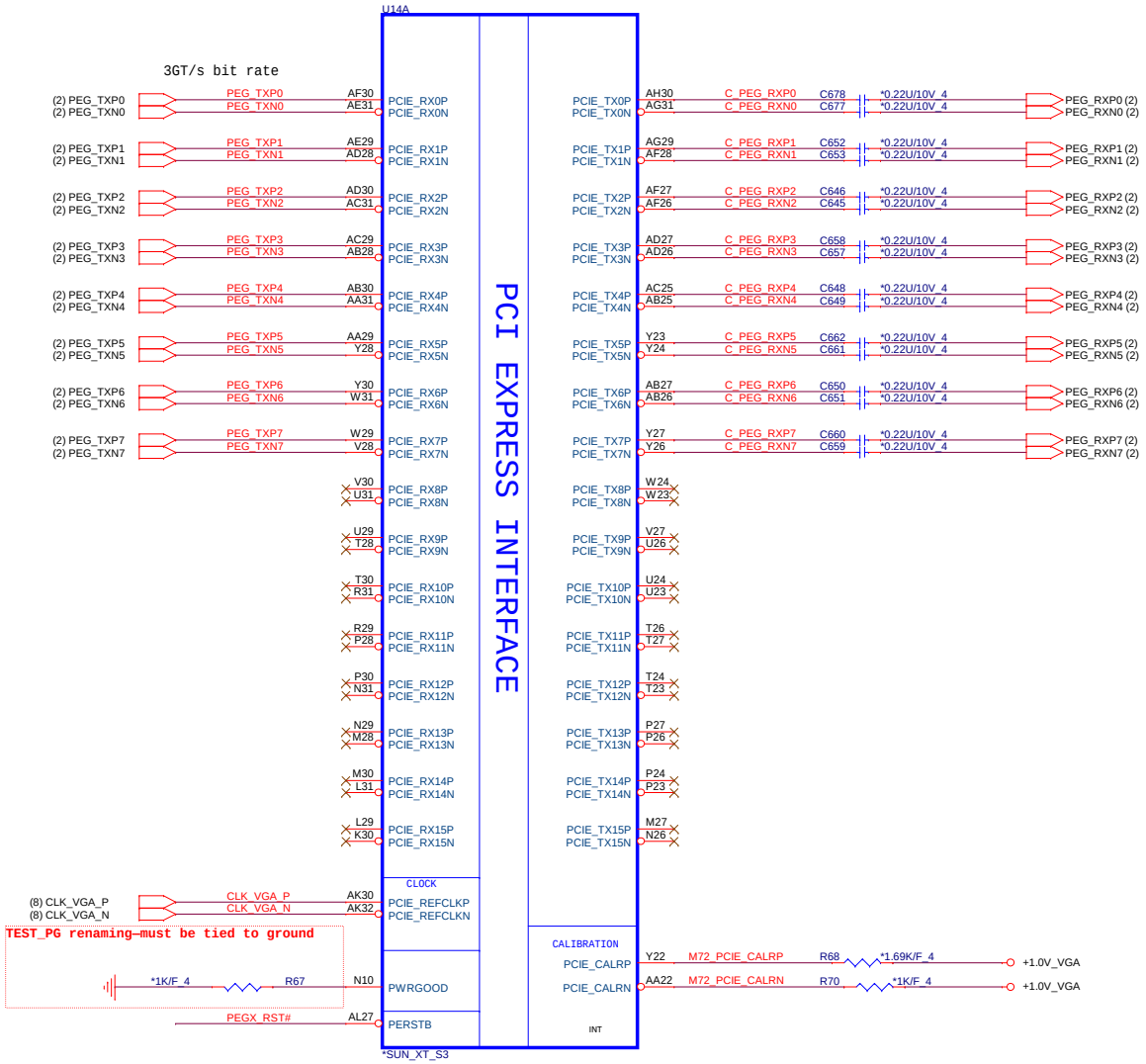

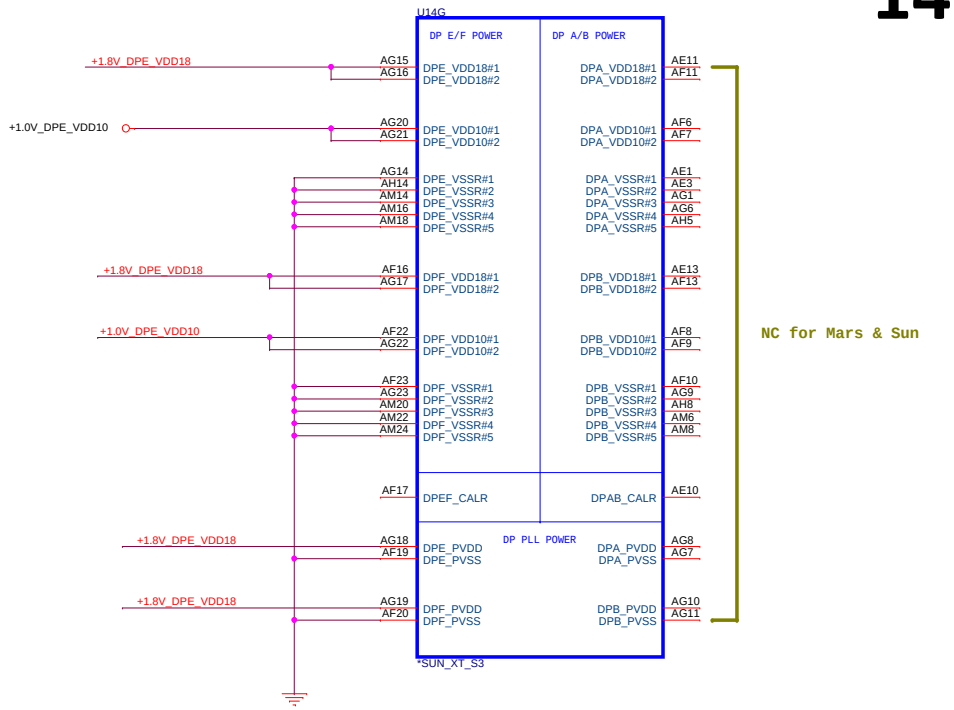

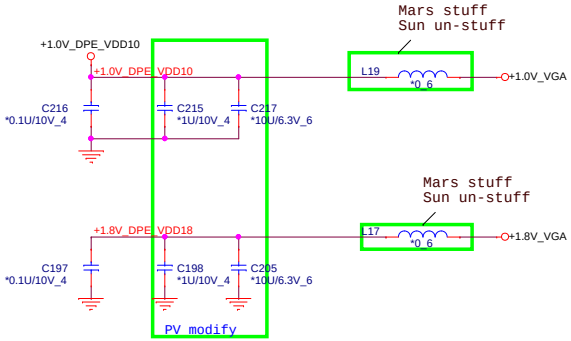

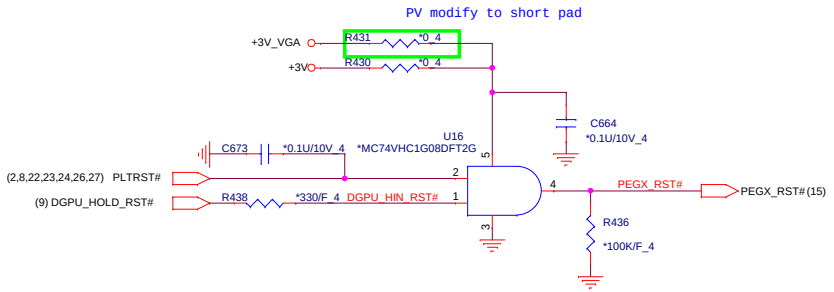

+1.0V_VGA (15,17,24,37)
+1.8V_VGA (15,17,37)

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 PCIE_Interface	1A
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GPIO10 GPIO30 GPIO16 GPIO20 GPIO15 Sun XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

PV modify

MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix- F(Huma)	128Mx16 *4, 900Mhz	H5TC2G63FFR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128M16JT-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC4G63FAFR-11C	6.98K	4.99K
100	Samsung- B die	256Mx16 *4, 900Mhz	K4W4G1646B-HC1A	4.53K	4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K

BIT5 => BIT0

PS0 => 11001
PS1 => 01000
PS2 => 00000
PS3 => 11000

Default

NC for Sun

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

Memory ID

Mars stuff Sun un-stuff

Mars stuff Ra Sun stuff Rb

Mars stuff Rc, Rd, Ca Sun un-stuff Rc, Rd, Ca

Fo Mars/ Chelsea
Change La, Lb
Bead to 0 ohm

For Thems: La,Lb:
CX8PG471000/BLM18PG471SN1D/1A_6

1.8V(75mA DPLL_PVDD)

1.0V(125mA DPLL_VDDC)

1.8V(5mA TSVDD)

Reserved. Do not connect on the PCB.

For AMD tuning timing purpose

SI Modify

For Mars: Stuff Ra only=> VDDC 1.1V
For Thems: Stuff Ra, Rb=> VDDC 1.0V

For Int Clk 27Mhz

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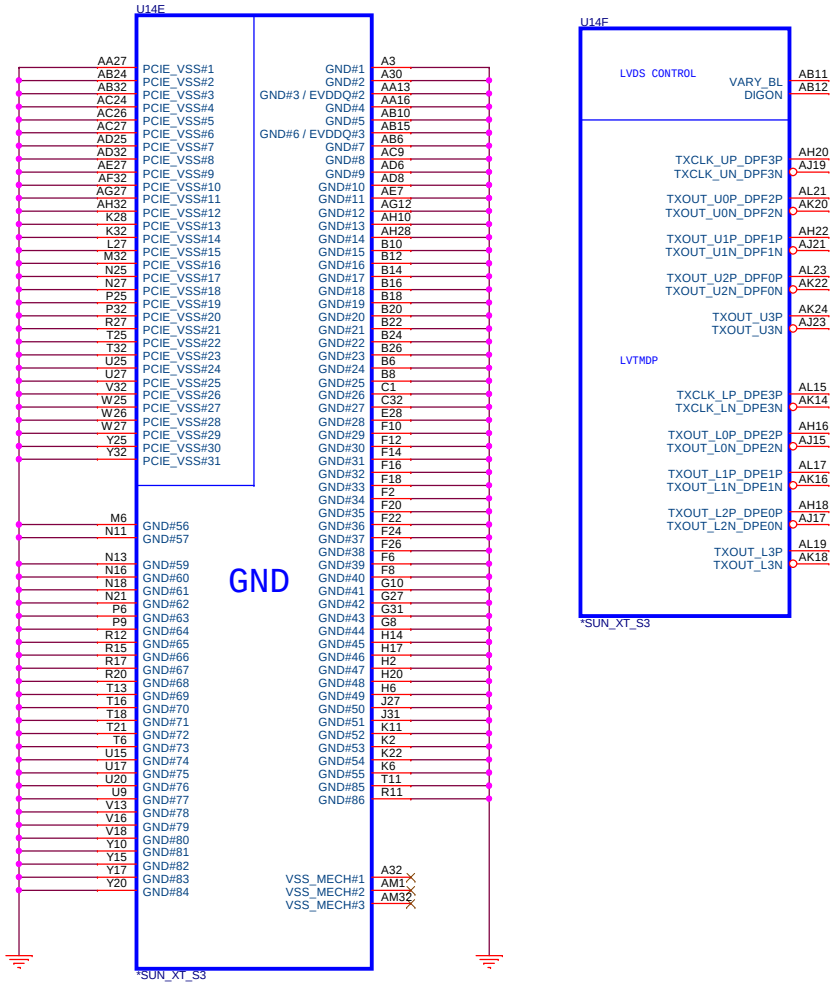


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

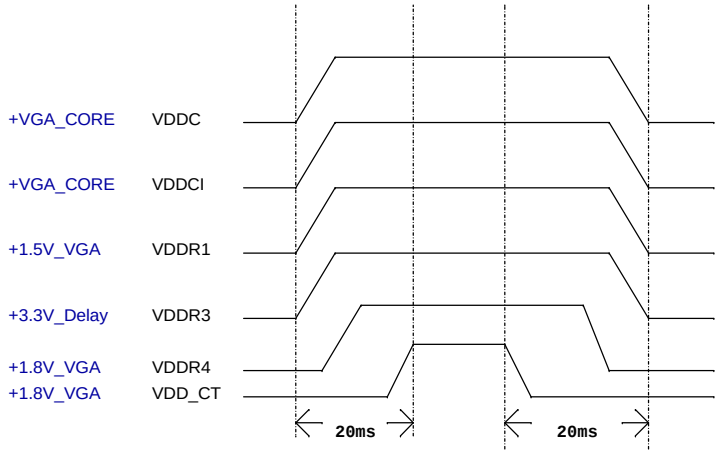
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

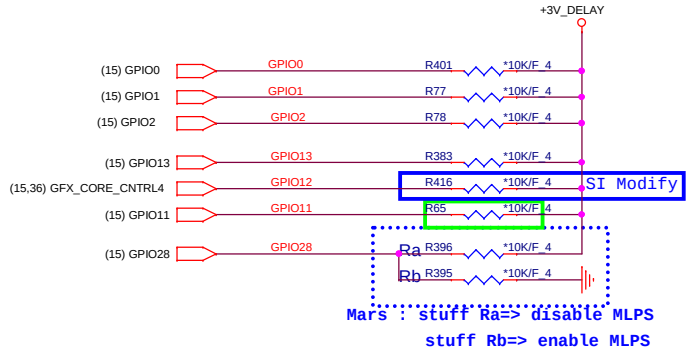
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



+3V_DELAY (15,17)

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 GND / LVDS/ Straps	1A
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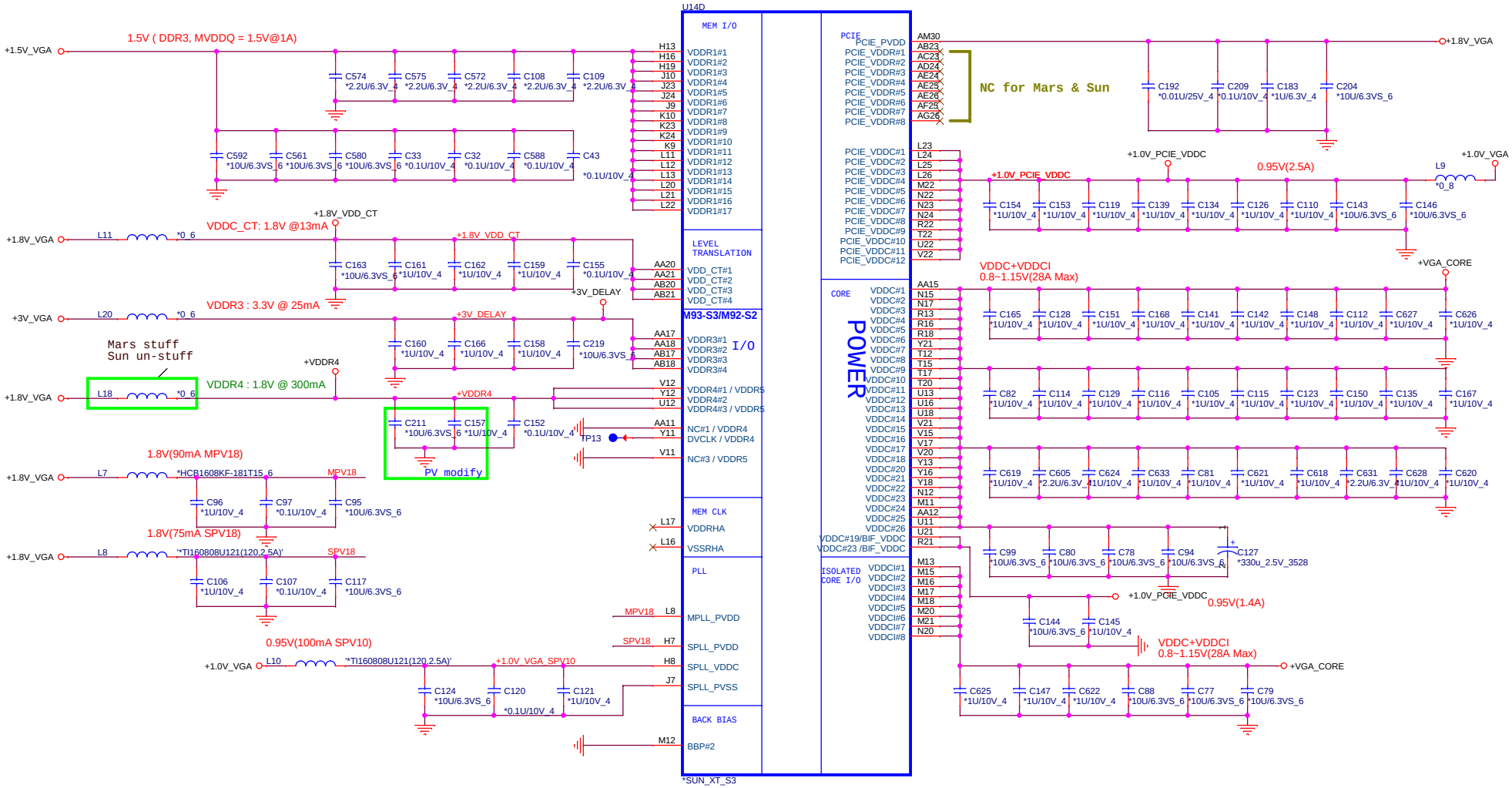

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 Power_and_NC	1A

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(19) VMA_ODT0 — VMA_ODT0
(19) VMA_ODT1 — VMA_ODT1
(19) VMA_RAS0# — VMA_RAS0#
(19) VMA_RAS1# — VMA_RAS1#
(19) VMA_CAS0# — VMA_CAS0#
(19) VMA_CAS1# — VMA_CAS1#
(19) VMA_WE0# — VMA_WE0#
(19) VMA_WE1# — VMA_WE1#
(19) VMA_CS0# — VMA_CS0#
(19) VMA_CS1# — VMA_CS1#
(19) VMA_CKE0 — VMA_CKE0
(19) VMA_CKE1 — VMA_CKE1
(19) VMA_CLK0 — VMA_CLK0
(19) VMA_CLK0# — VMA_CLK0#
(19) VMA_CLK1 — VMA_CLK1
(19) VMA_CLK1# — VMA_CLK1#
(19) VMA_WDQS[7..0] — VMA_WDQS[7..0]
(19) VMA_RDQS[7..0] — VMA_RDQS[7..0]
(19) VMA_DM[7..0] — VMA_DM[7..0]
(19) VMA_DQ[63..0] — VMA_DQ[63..0]
(19) VMA_MA[14..0] — VMA_MA[14..0]
(19) VMA_BA0 — VMA_BA0
(19) VMA_BA1 — VMA_BA1
(19) VMA_BA2 — VMA_BA2

support 1Gbit VRAM (64M X 16)

U14C

MEMORY INTERFACE

VMA_DQ0	K27	DQA_0	MAA_0	K17	VMA_MA0
VMA_DQ1	J29	DQA_1	MAA_1	J20	VMA_MA1
VMA_DQ2	H30	DQA_2	MAA_2	H23	VMA_MA2
VMA_DQ3	H32	DQA_3	MAA_3	G23	VMA_MA3
VMA_DQ4	G29	DQA_4	MAA_4	G24	VMA_MA4
VMA_DQ5	F28	DQA_5	MAA_5	H24	VMA_MA5
VMA_DQ6	F32	DQA_6	MAA_6	J19	VMA_MA6
VMA_DQ7	F30	DQA_7	MAA_7	K19	VMA_MA7
VMA_DQ8	C30	DQA_8	MAA_8	J14	VMA_MA8
VMA_DQ9	F27	DQA_9	MAA_9	K14	VMA_MA9
VMA_DQ10	A28	DQA_10	MAA_10	J11	VMA_MA10
VMA_DQ11	C28	DQA_11	MAA_11	J13	VMA_MA11
VMA_DQ12	E27	DQA_12	MAA_12	H11	VMA_MA12
VMA_DQ13	G26	DQA_13	MAA_13/BA2	G11	VMA_BA2
VMA_DQ14	D26	DQA_14	MAA_14/BA0	J16	VMA_BA0
VMA_DQ15	F25	DQA_15	MAA_15/BA1	L15	VMA_BA1
VMA_DQ16	A25	DQA_16			
VMA_DQ17	C25	DQA_17	DQMA_0	E32	VMA_DM0
VMA_DQ18	E25	DQA_18	DQMA_1	E30	VMA_DM1
VMA_DQ19	D24	DQA_19	DQMA_2	A21	VMA_DM2
VMA_DQ20	E23	DQA_20	DQMA_3	C21	VMA_DM3
VMA_DQ21	F23	DQA_21	DQMA_4	E13	VMA_DM4
VMA_DQ22	D22	DQA_22	DQMA_5	D12	VMA_DM5
VMA_DQ23	F21	DQA_23	DQMA_6	E3	VMA_DM6
VMA_DQ24	E21	DQA_24	DQMA_7	F4	VMA_DM7
VMA_DQ25	D20	DQA_25			
VMA_DQ26	F19	DQA_26	RDQSA_0	H28	VMA_RDQS0
VMA_DQ27	A19	DQA_27	RDQSA_1	C27	VMA_RDQS1
VMA_DQ28	D18	DQA_28	RDQSA_2	A23	VMA_RDQS2
VMA_DQ29	F17	DQA_29	RDQSA_3	E19	VMA_RDQS3
VMA_DQ30	A17	DQA_30	RDQSA_4	E15	VMA_RDQS4
VMA_DQ31	C17	DQA_31	RDQSA_5	D10	VMA_RDQS5
VMA_DQ32	E17	DQA_32	RDQSA_6	D6	VMA_RDQS6
VMA_DQ33	D16	DQA_33	RDQSA_7	G5	VMA_RDQS7
VMA_DQ34	F15	DQA_34			
VMA_DQ35	A15	DQA_35	WDQSA_0	H27	VMA_WDQS0
VMA_DQ36	D14	DQA_36	WDQSA_1	A27	VMA_WDQS1
VMA_DQ37	F13	DQA_37	WDQSA_2	C23	VMA_WDQS2
VMA_DQ38	A13	DQA_38	WDQSA_3	C19	VMA_WDQS3
VMA_DQ39	C13	DQA_39	WDQSA_4	C15	VMA_WDQS4
VMA_DQ40	E11	DQA_40	WDQSA_5	E9	VMA_WDQS5
VMA_DQ41	A11	DQA_41	WDQSA_6	C5	VMA_WDQS6
VMA_DQ42	C11	DQA_42	WDQSA_7	H4	VMA_WDQS7
VMA_DQ43	F11	DQA_43			
VMA_DQ44	A9	DQA_44	ODTA0	L18	VMA_ODT0
VMA_DQ45	C9	DQA_45	ODTA1	K16	VMA_ODT1
VMA_DQ46	F9	DQA_46			
VMA_DQ47	D8	DQA_47	CLKA0	H26	VMA_CLK0
VMA_DQ48	E7	DQA_48	CLKA0B	H25	VMA_CLK0#
VMA_DQ49	A7	DQA_49			
VMA_DQ50	C7	DQA_50	CLKA1	G9	VMA_CLK1
VMA_DQ51	F7	DQA_51	CLKA1B	H9	VMA_CLK1#
VMA_DQ52	A5	DQA_52			
VMA_DQ53	E5	DQA_53	RASA0B	G22	VMA_RAS0#
VMA_DQ54	C3	DQA_54	RASA1B	G17	VMA_RAS1#
VMA_DQ55	E1	DQA_55			
VMA_DQ56	G7	DQA_56	CASA0B	G19	VMA_CAS0#
VMA_DQ57	G6	DQA_57	CASA1B	G16	VMA_CAS1#
VMA_DQ58	G1	DQA_58			
VMA_DQ59	G3	DQA_59	CSA0B_0	H22	VMA_CS0#
VMA_DQ60	J6	DQA_60	CSA0B_1	J22	
VMA_DQ61	J1	DQA_61			
VMA_DQ62	J3	DQA_62	CSA1B_0	G13	VMA_CS1#
VMA_DQ63	J5	DQA_63	CSA1B_1	K13	
	K26	MVREFDA	CKEA0	K20	VMA_CKE0
	J26	MVREFSA	CKEA1	J17	VMA_CKE1
	J25	MEM_CALRN0	WEA0B	G25	VMA_WE0#
	K7	NC/TESTEN#2	WEA1B	H10	VMA_WE1#
	J8	MEM_CALRP1/DPC_CALR	PX_EN	AB16	PX_EN
	K25	MEM_CALRP0	RSVD#2	G14	VMA_MA14
			RSVD#3	G20	VMA_MA13
DRAM_RST	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA			
CLKTESTB	L7	CLKTESTB			

*SUN_XT_S3

PX_EN — TP74

+1.5V_VGA
R380 40.2/F_4
MVREFD
C607 *1U/10V_4
R381 100/F_4
+1.5V_VGA
R57 40.2/F_4
MVREFS
C125 *1U/10V_4
R61 100/F_4

R363 *1K/F_4
R369 *120/F_4

C133 *0.1U/10V_4
C602 *0.1U/10V_4
R62 *51.1/F_4
R368 *51.1/F_4

route 50ohms single-ended/100ohms diff and keep short

From GPU
25mm (max) — 5mm (max) — 25mm (max)
DRAM_RST — R48 *10/F_4 — R4 *51.1/F_4 — DRAM_RST_M — DRAM_RST_M (19)
R49 *4.99K/F_4
C21 *120P/50V_4

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

+1.5V_VGA (17,19,24,37)

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 MEM_Interface	1A

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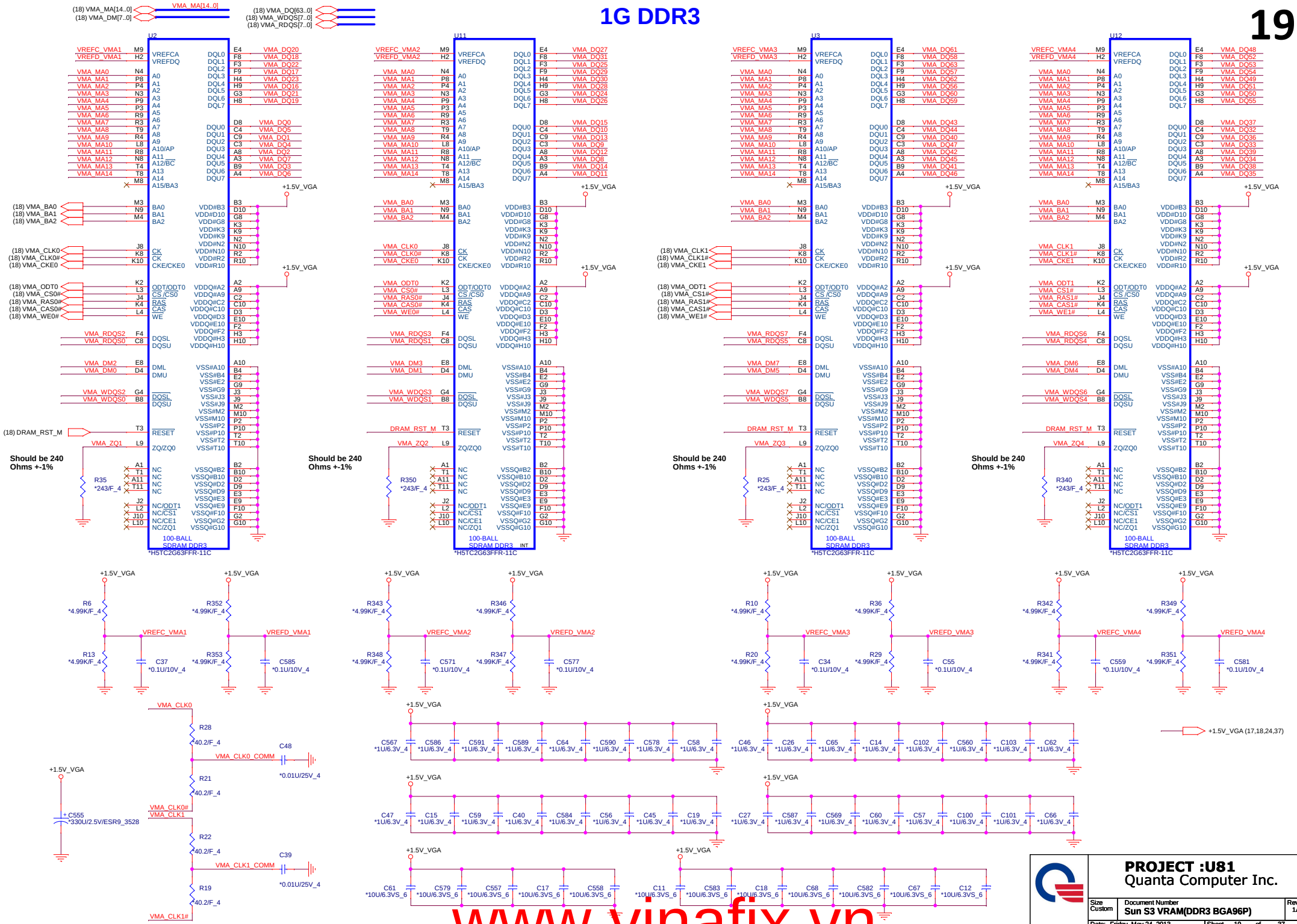
1G DDR3



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Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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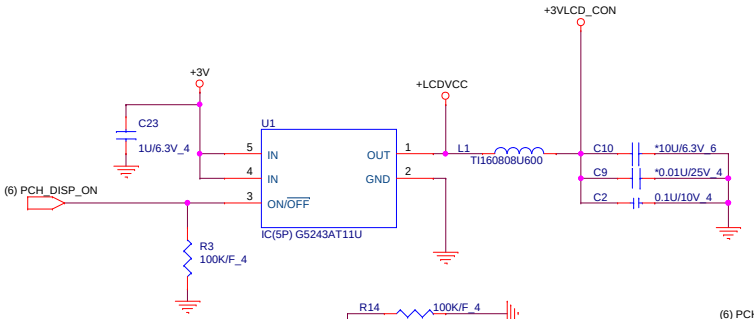
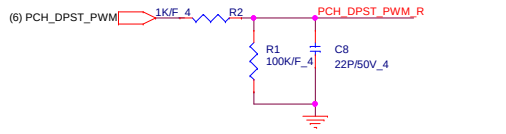
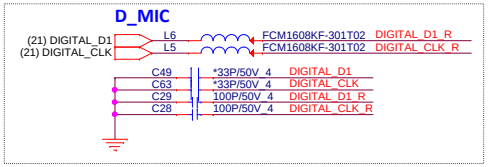
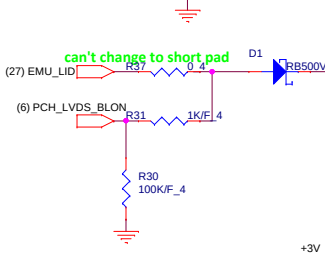
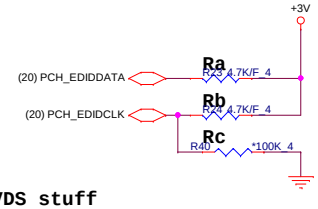
LVDS Conn.

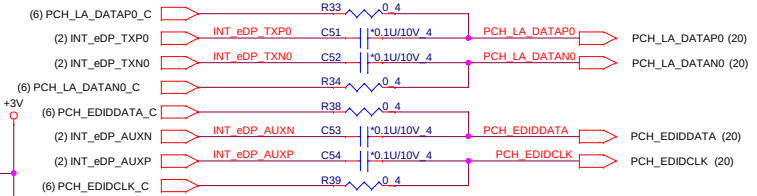


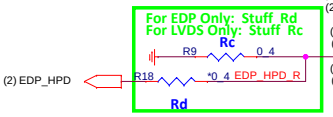


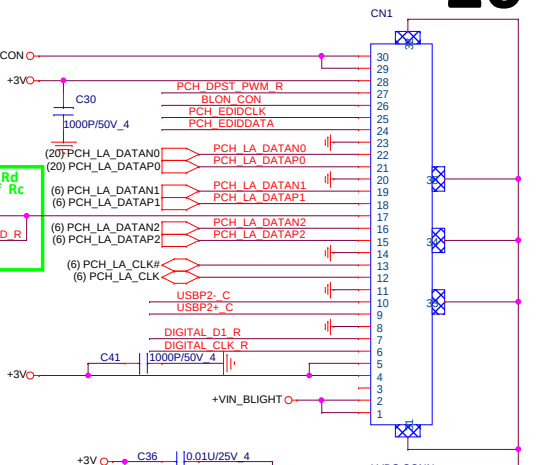










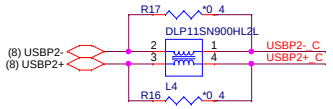


Only for eDP reserve

For LVDS stuff
Ra=4.7k,Rb=4.7k,Rc un-stuff
For eDP reserve
Ra=100k,Rc=100k,Rb un-stuff

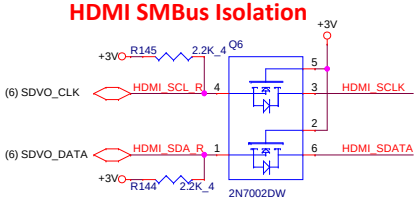
For EDP Only: stuff Cap
For LVDS only stuff Resister

USB CAMERA



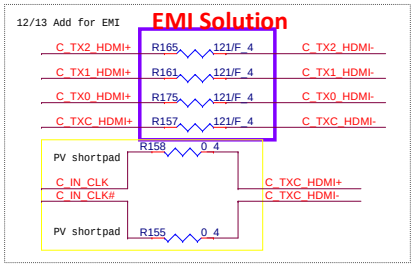
HDMI Conn.

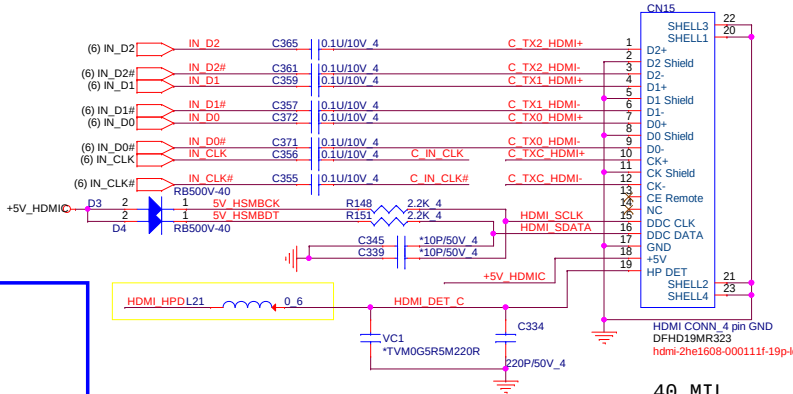
HDMI SMBus Isolation

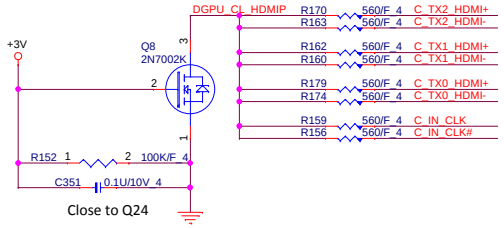


Close to HDMI connector

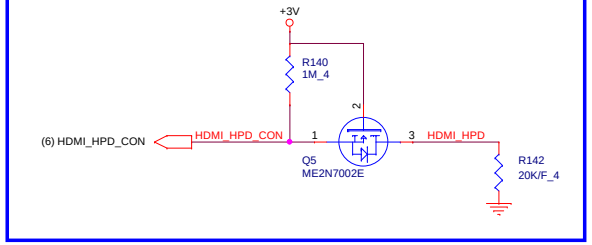
EMI Solution

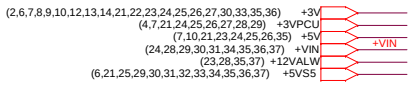


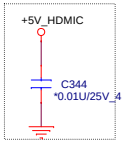




Close to Q24

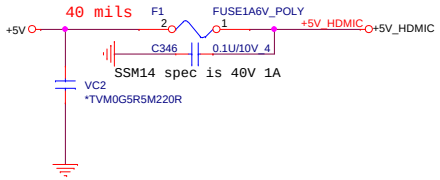






for EMI request

40 MIL



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Custom	LCD/HDMI/Camera	1A
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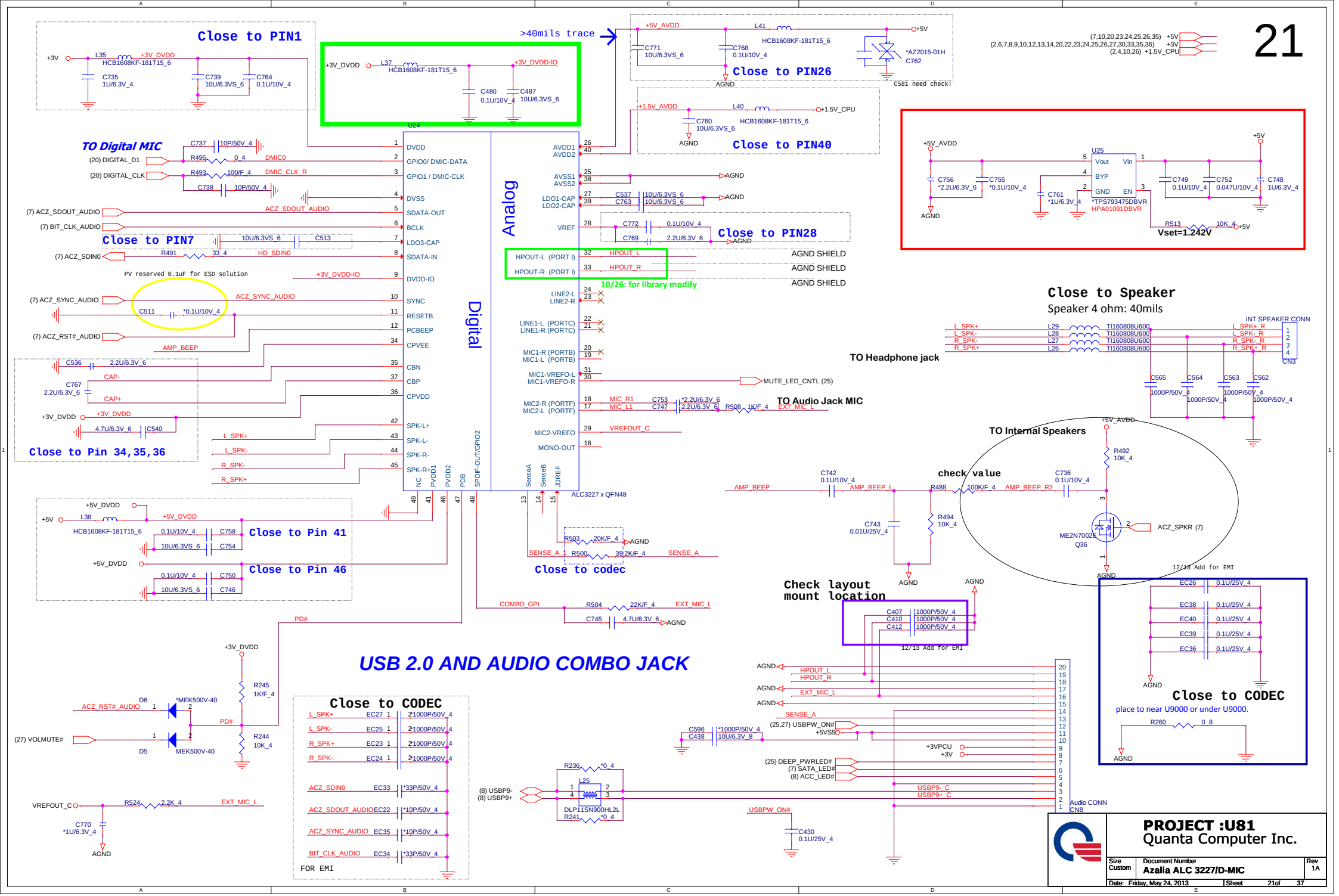
21
Close to PIN1
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN28
Close to PIN7
Close to Pin 34,35,36
Close to Pin 41
Close to Pin 46
Close to codec
TO Digital MIC
Analog
Digital
U24
ALC3227 x QFN48
10/26: for library modify
AGND SHIELD
Vset=1.242V
Close to Speaker
Speaker 4 ohm: 40mils
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
check value
Check layout mount location
12/13 Add for EMI
USB 2.0 AND AUDIO COMBO JACK
Close to CODEC
FOR EMI
place to near U9000 or under U9000.
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Quanta Computer Inc.
Azalia ALC 3227/D-MIC
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www.vinafix.vn

For EMI 0 ~ 22 ohm

R58 10/F_4

LAN_XTAL1 — XTAL1

XTAL2 — R55 0_4 — PV shortpad — LAN_XTAL25_IN (26)

Y1 *25MHZ +-10PPM

C118 *33P/50V_4

C104 *33P/50V_4

Power trace Layout 寬度> 60mil

>60mil

>60mil

+1.05V_LAN_REGOUT

Trace<30 mil
Width > 60 mil

Cz

C132 0.1U/10V_4

For 10/100
NA: Ca Cb
Stuff La(0ohm),Cz

For 10/100
Place Cc,Cd
close to each VDD10 pin-- 8, 30

+1.05V_LAN

Cc C86 0.1U/10V_4

Cd C87 0.1U/10V_4

Cg C98 1U/6.3V_4

Ch C93 0.1U/10V_4

10/24: add for FAE review

For 10/100
Place Cg Ch close to each VDD10 pin-- 30 (reserve)

+1.05V_LAN

R50 2.49K/F_4 LANRSET

+3V_LAN

TP5 LAN_ALED#

TP4

TP6 LAN_WLED#

FOR 8166: Stuff R40, NA R41

PV EMI suggestion

EC16 470P/50V_4

EC4 470P/50V_4

+3V

R64 1K_4

ISOLATEB

R63 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U5

RTL 8166EH

Please add 9 GND VIAs connection with thermal PAD

GND

AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2(LED1)

MDI0+ MDI0- VDD10 MDI1+ MDI1- VDD10

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# ISOLATEB PLTRST#

PCIE_RXN2_LAN_L C138 0.1U/10V_4 PCIE_RXP2_LAN_L C137 0.1U/10V_4

PLTRST# (2,8,14,23,24,26,27)
PCIE_RXN2_LAN (8)
PCIE_RXP2_LAN (8)

MDP3(NC) MDN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N

RTL8166EH

FOR 10/100 : RTL8166EH

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN2_LAN PCIE_TXP2_LAN

CLK_PCIE_LANN (8)
CLK_PCIE_LANP (8)
PCIE_TXN2_LAN (8)
PCIE_TXP2_LAN (8)

+3V_LAN

LAN_CLKRQ

(8) PCIE_CLKREQ_LAN# — PCIE_CLKREQ_LAN# R53 0_4 — PV shortpad

U4

10/24: swap 0 & 1 for Layout routing

MDI1+_1 MDI1-_1 MDI0+_1 MDI0-_1

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI1+ TRA_V_DAC MDI1- MDI0- TRA_V_DAC MDI0+

R354 75/F_4 LAN_MCTG1

R41 75/F_4 LAN_MCTG0

C576 10P/3KV_1808

NS681684

C70 0.01U/25V_4

For 10/100
Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32

+3V_LAN

+3VLANVCC

C131 0.1U/10V_4 Ca

C83 0.1U/10V_4 Cb

C84 *4.7U/6.3V_6

C85 *4.7U/6.3V_6

(2,6,7,8,9,10,12,13,14,20,21,23,24,25,26,27,30,33,35,36) +3V
(26,35) +3VLANVCC

LAN conn

RJ45

10/26: swap led
+/- & RJ45 Library

(White) LAN_WLED LAN_WLED#

(Amber) LAN_ALED LAN_ALED#

CN13

LED_AMB_P A1 LED_AMB_N A2

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

MDI1- MDI1+ MDI0- MDI0+

GND1 GND

LED_GRE_P B1 LED_GRE_N B2

RJ45_CONN

R5 0_6

R44 0_6

C72 10P/50V_4

12/13 Add for EMI

SI Change correct PN(for Slim-G)

+3VLANVCC — R345 360_4 — C570 1000P/50V_4 — LAN_ALED

朝前

+3VLANVCC — R355 360_4 — LAN_WLED — C593 1000P/50V_4

朝前

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Custom	LAN RTL8166EH /RJ45 conn	1A

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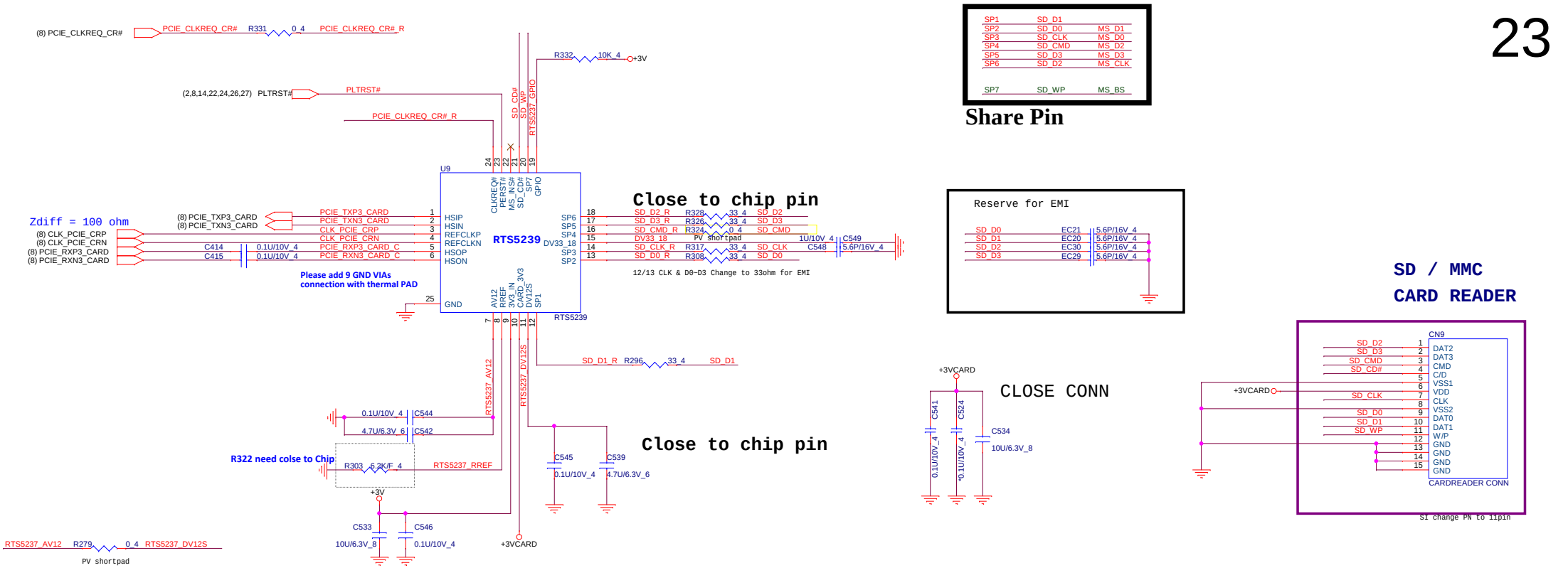
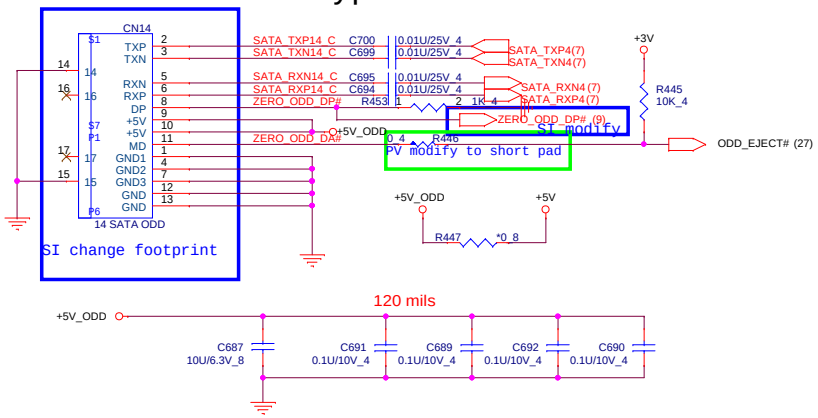


SATA ODD CONNECTOR

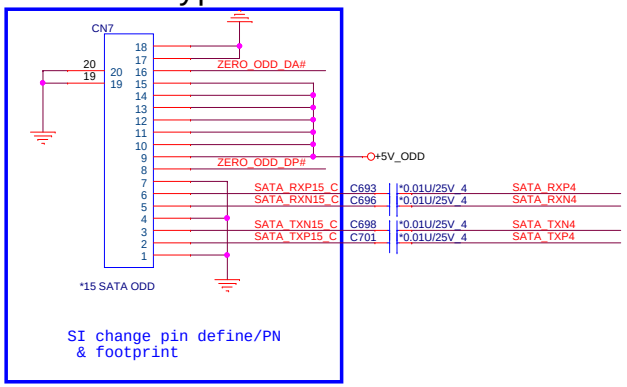
14" SATA ODD

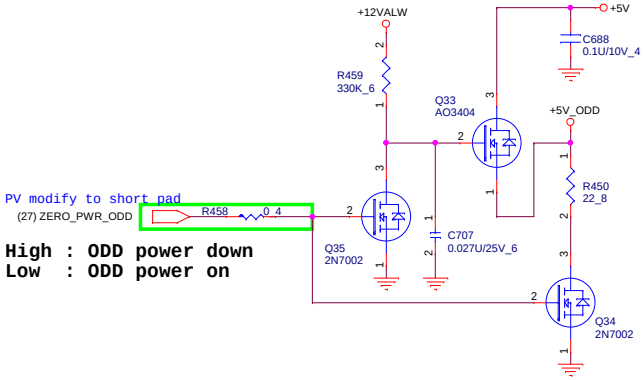
Bypass CAP close conn



15" SATA ODD

New Type





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Custom	CR RTS5239 & CR SOCKET	1A
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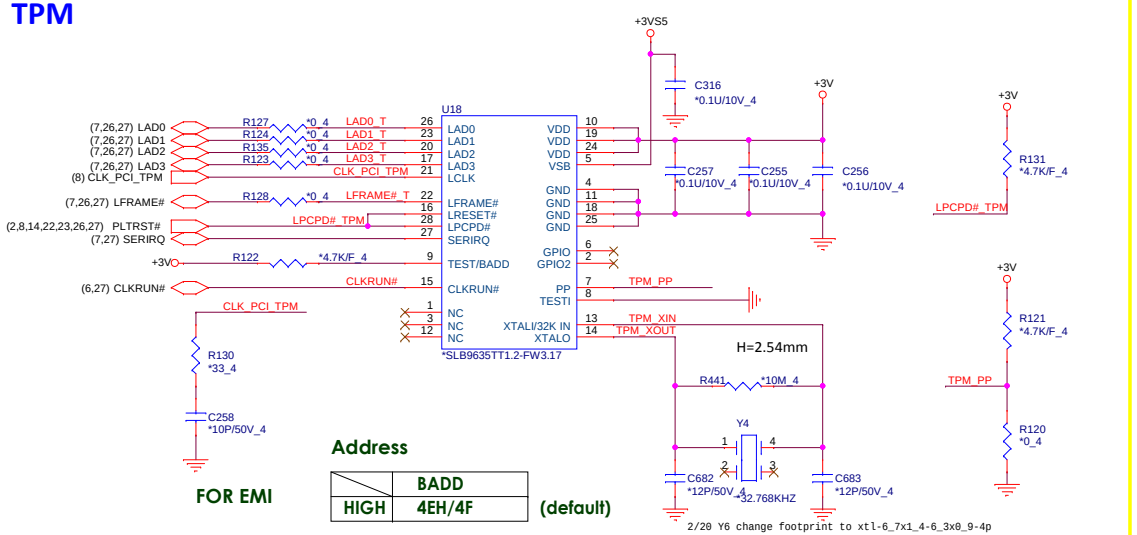
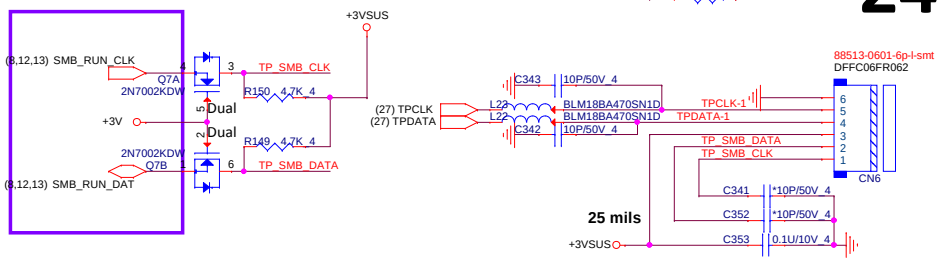
TPM

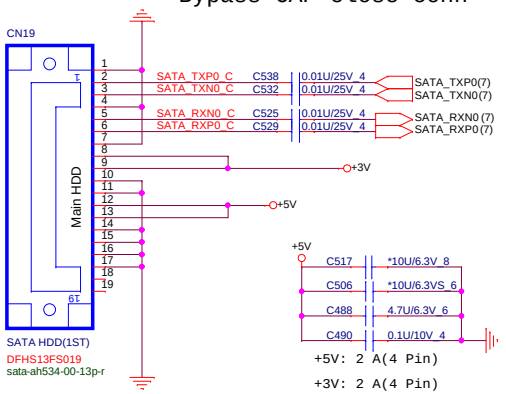


Touch Pad Connector

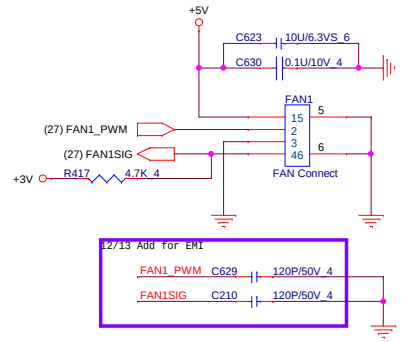


SATA HDD Connector(Cable type)

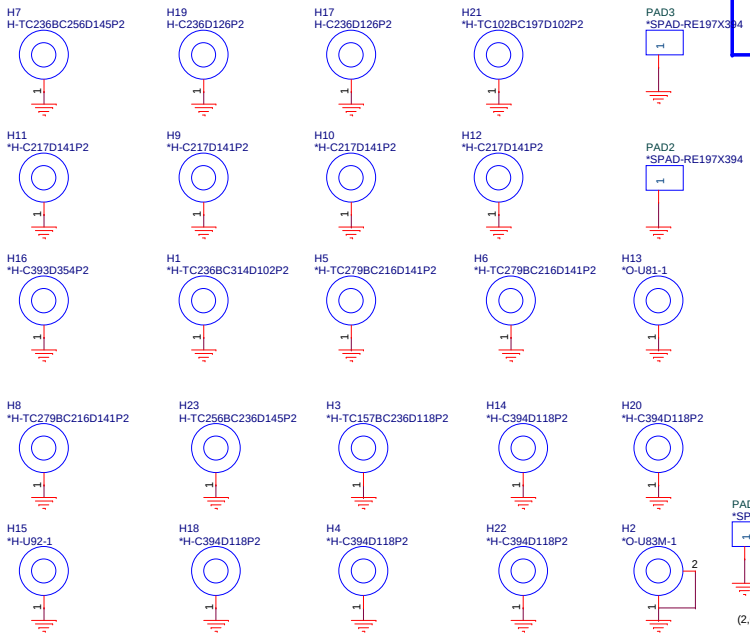
Bypass CAP close conn

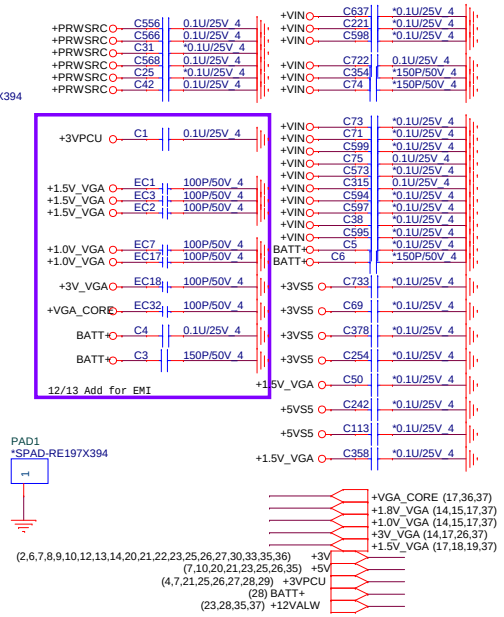


FAN

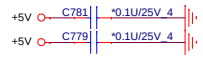


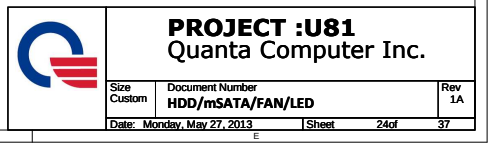
Hole



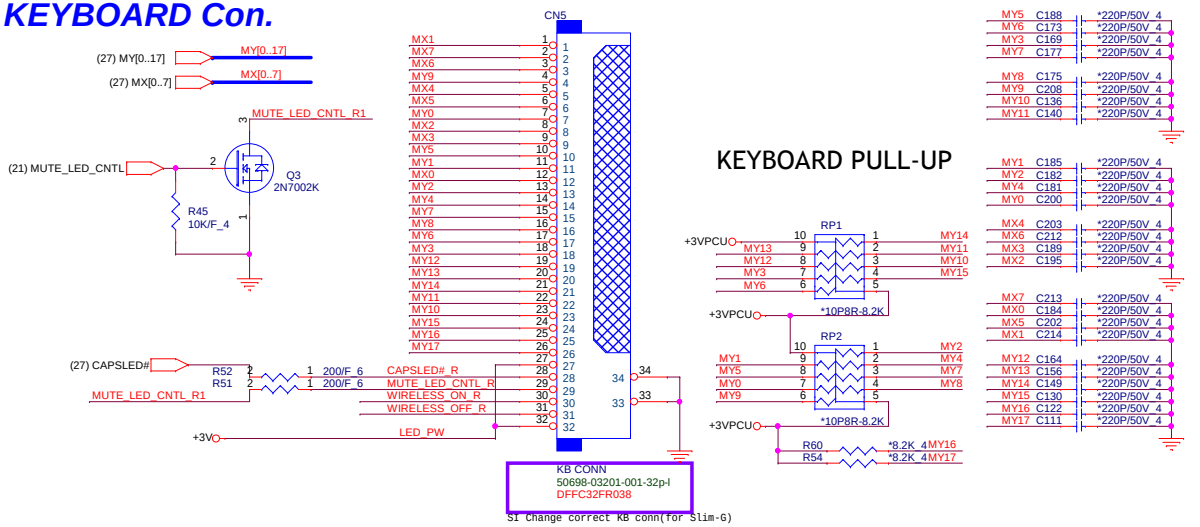


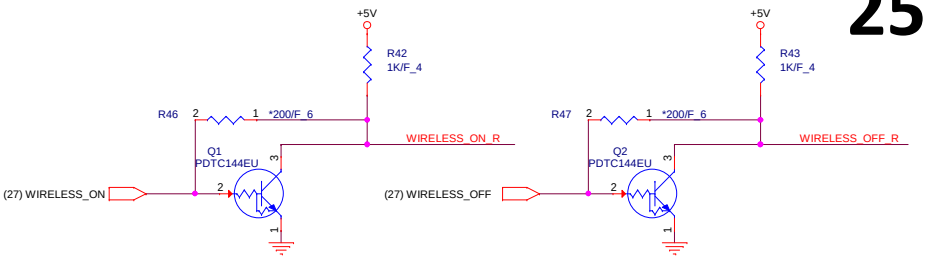
Mini PCI-E Card 2- Full size mSATA



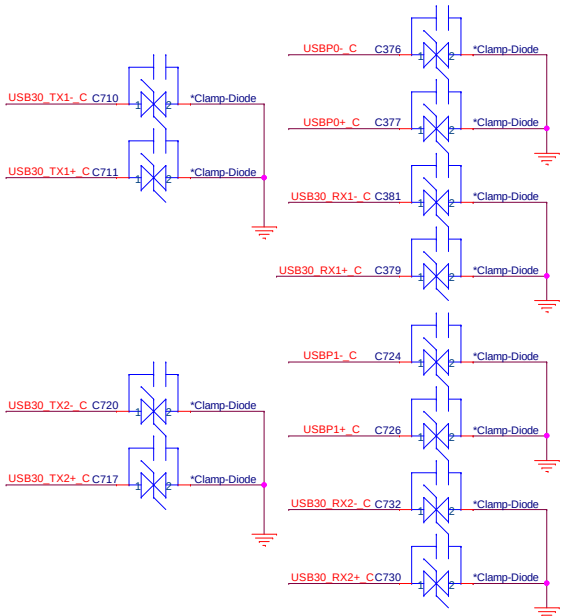


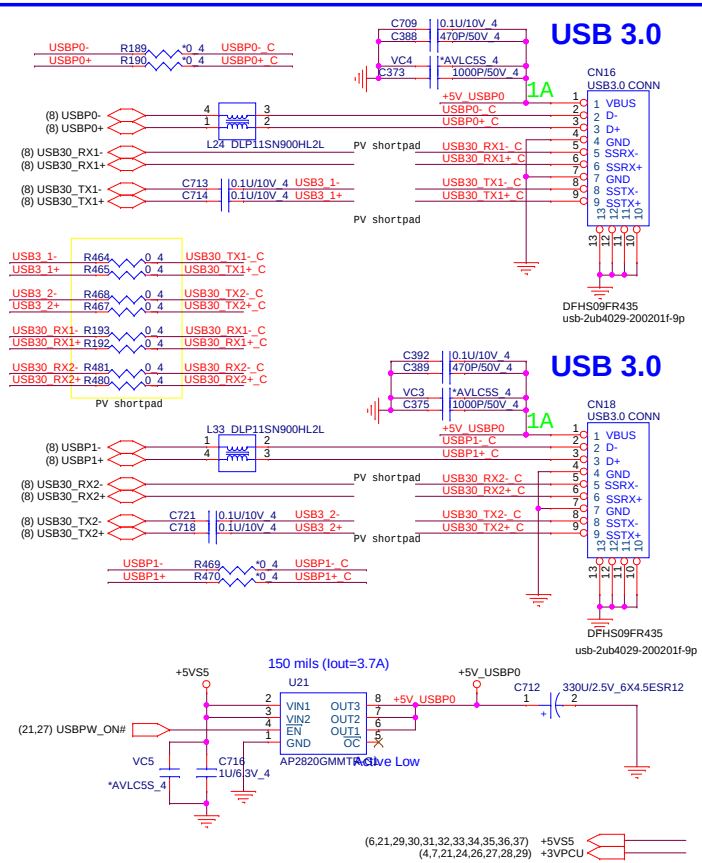
KEYBOARD Con.



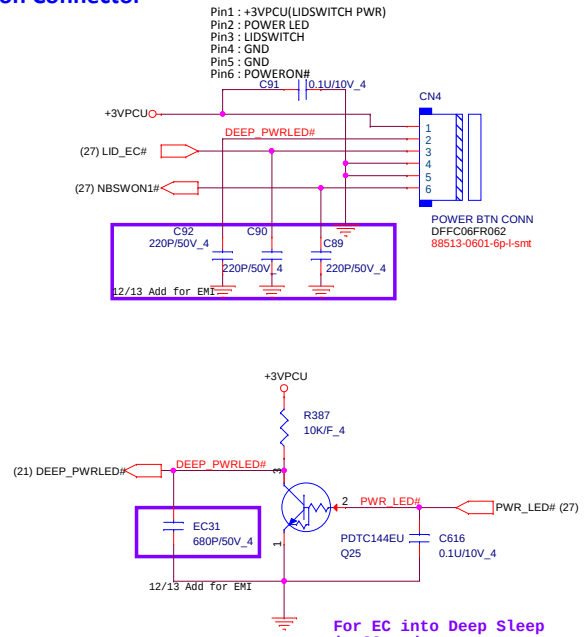


USB 2.0/3.0 Combo





Power Botton Connector



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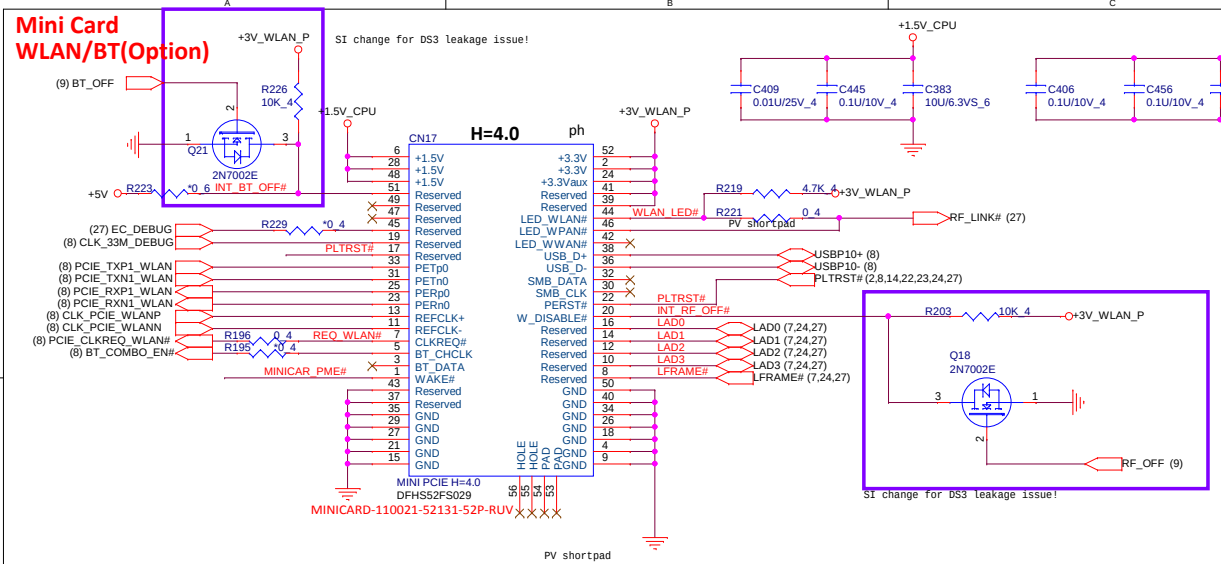
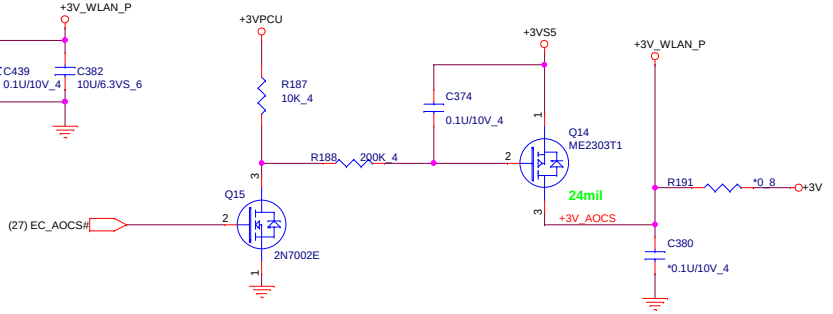
Mini Card WLAN/BT(Option)

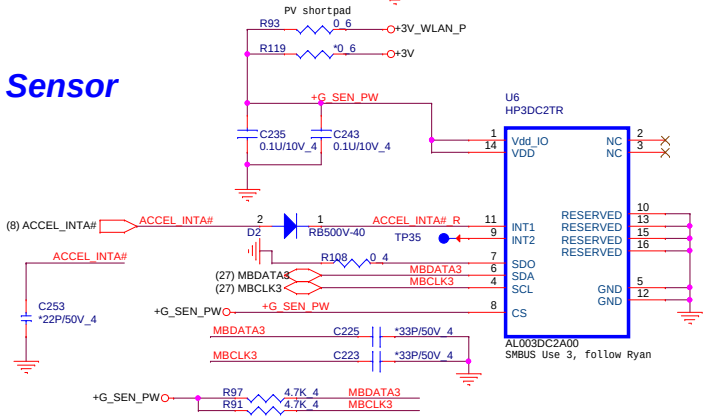




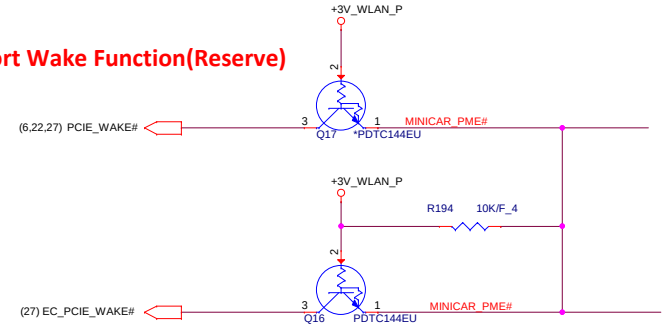
For EMI Suggestion

CLK_33M_DEBUG R201 *0_4 EC19 *33P/50V_4

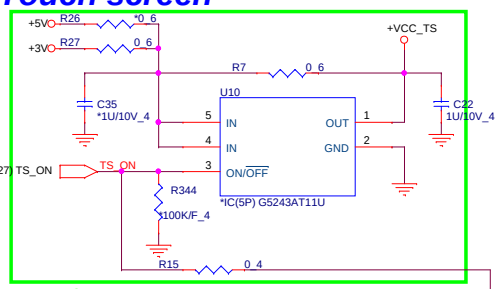
Accelerometer Sensor



Support Wake Function(Reserve)

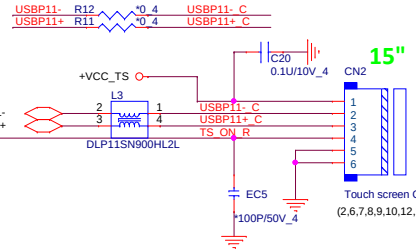


Touch screen



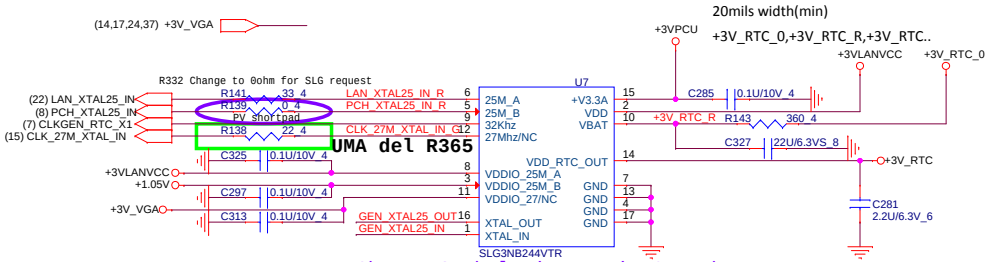
Close to CN3

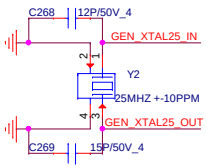
DEL TS 14" connector Circuit & Reserve +3V TS Power for AUO TS

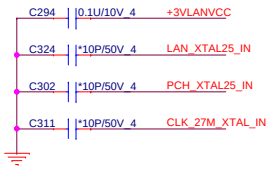


10/25:modify for 14/15 co-lay

Green CLK Circuitry







	U21 P/N
DIS	AL000314000
UMA	AL3NB244000

(2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,27,30,33,35,36) +3V
(7,10,20,21,23,24,25,35) +5V
(4,7,21,24,25,27,28,29) +3VPCU

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Size	Document Number	Rev
Custom	WLAN/G-Sensor/G-CLK/TS	1A

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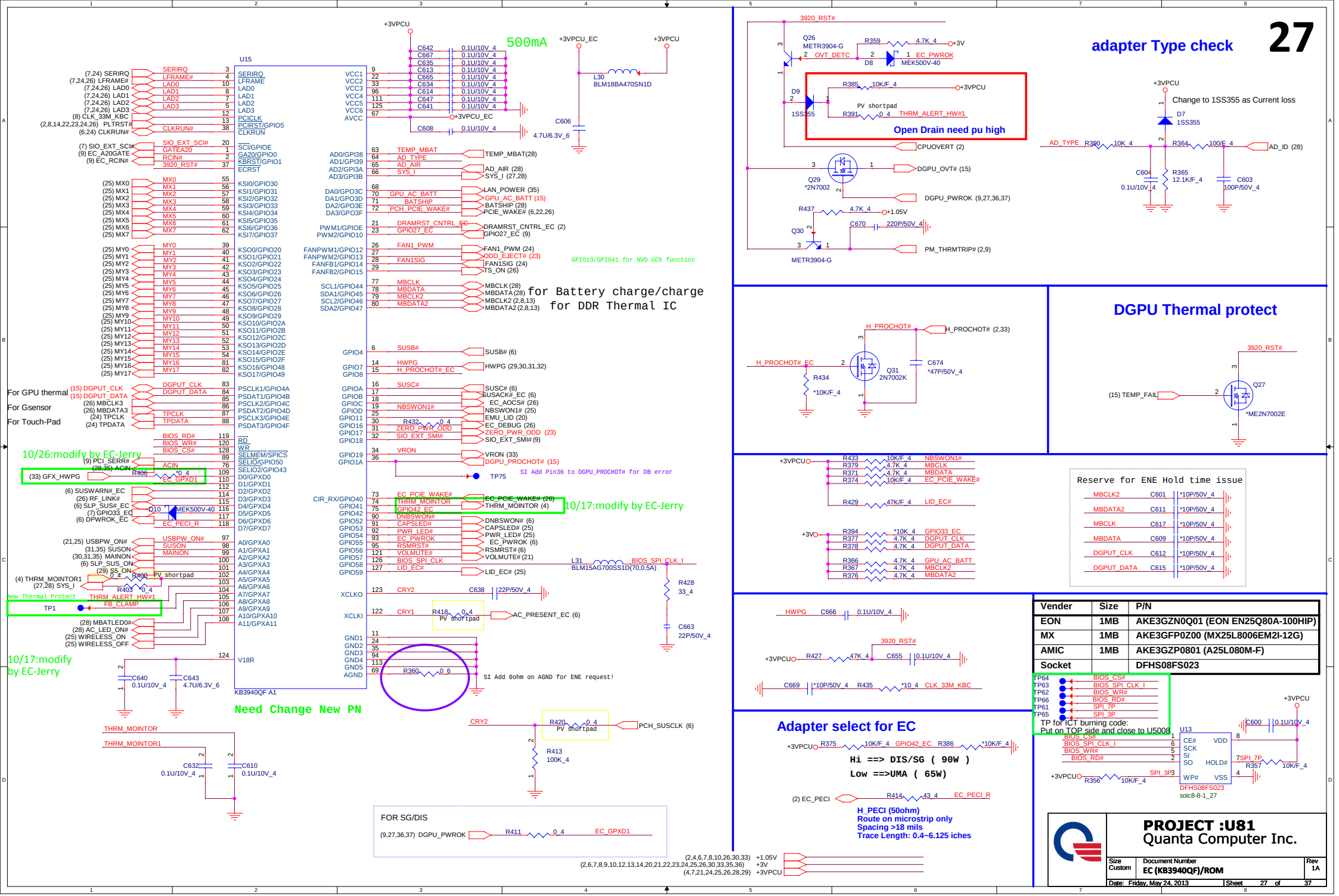

Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

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Size	Document Number	Rev
Custom	EC (KB3940QF)/ROM	1A
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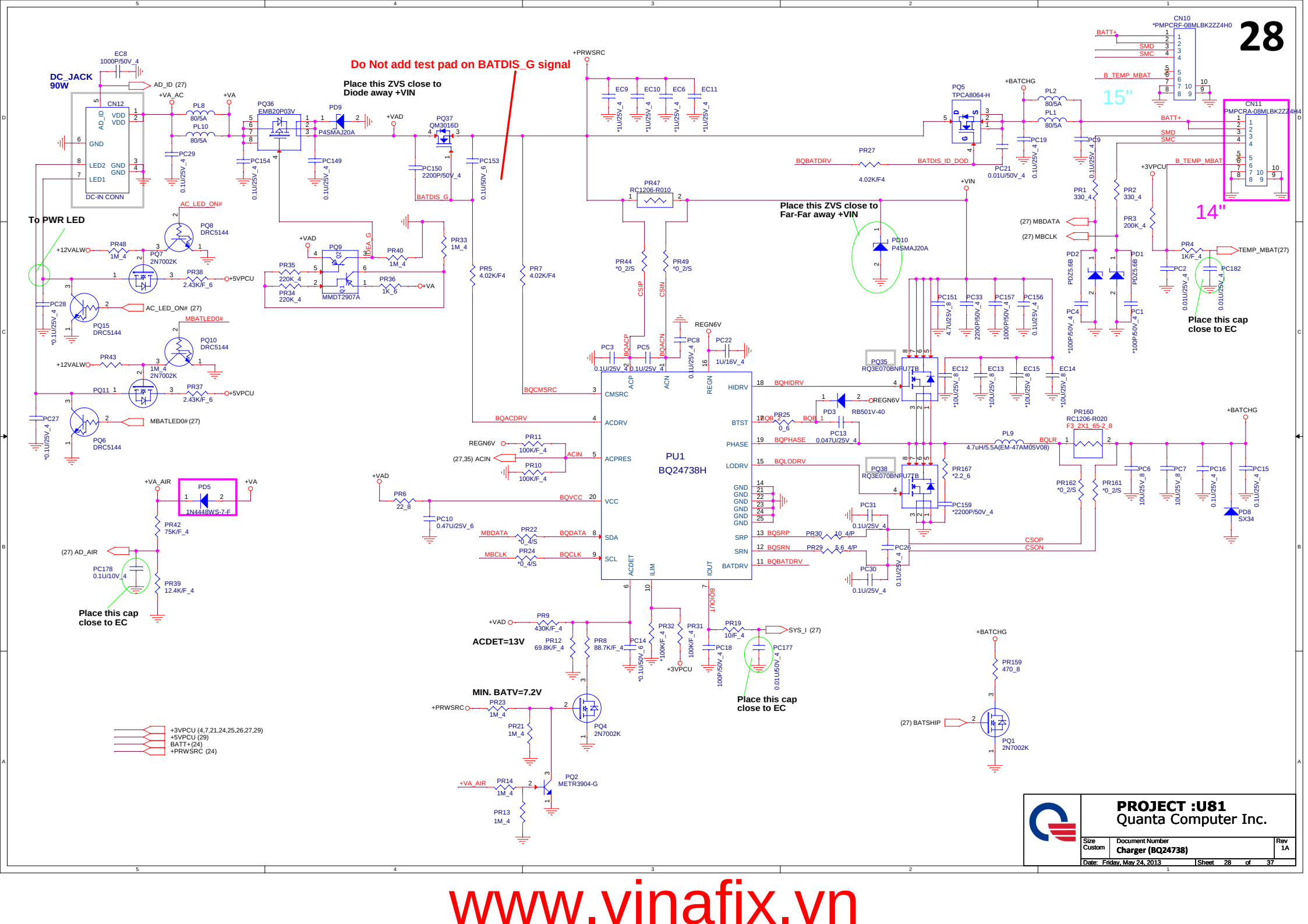
28
DC_JACK
90W
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
PU1
BQ24738H
ACDET=13V
MIN. BATV=7.2V
15"
14"
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Charger (BQ24738)
Size Custom
Rev 1A
Date: Friday, May 24, 2013
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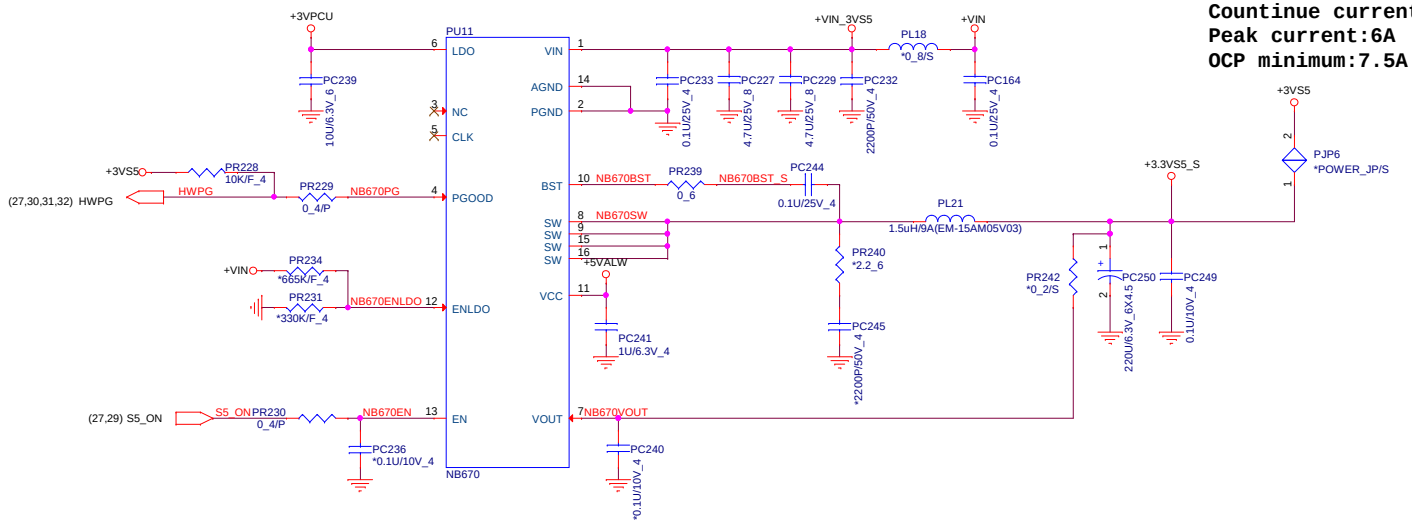
www.vinafix.vn

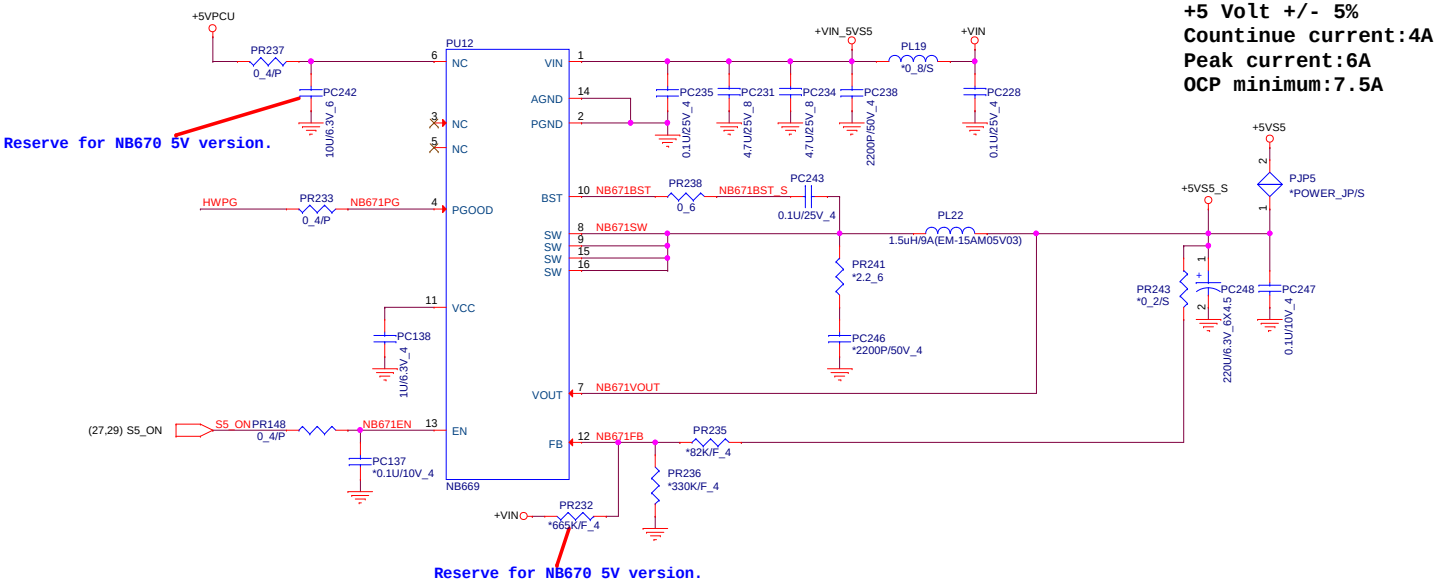
DC/DC +3VS5/+5VS5

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



+3VS5 (6,9,10,24,26,30,35,36,37)
+5VS5 (6,21,25,30,31,32,33,34,35,36,37)

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(NB669/NB670)	1A

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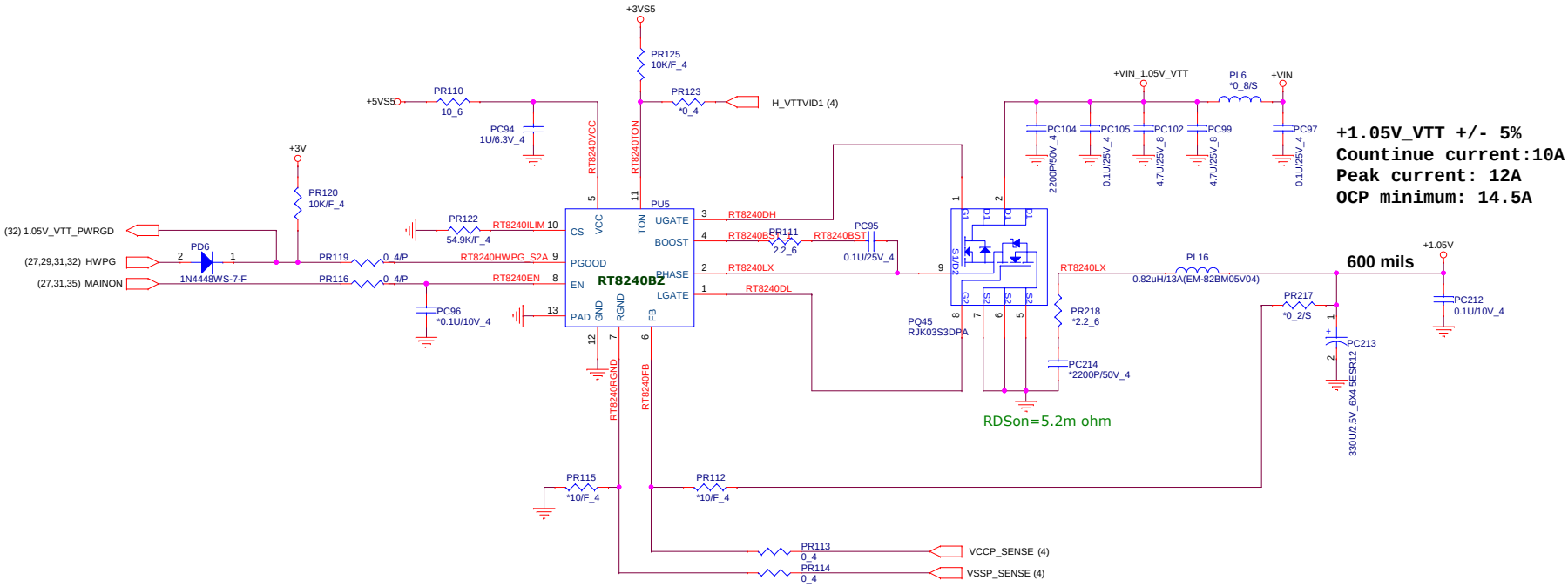

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Size	Document Number	Rev
Custom	1.05V(RT8240BZ)	1A

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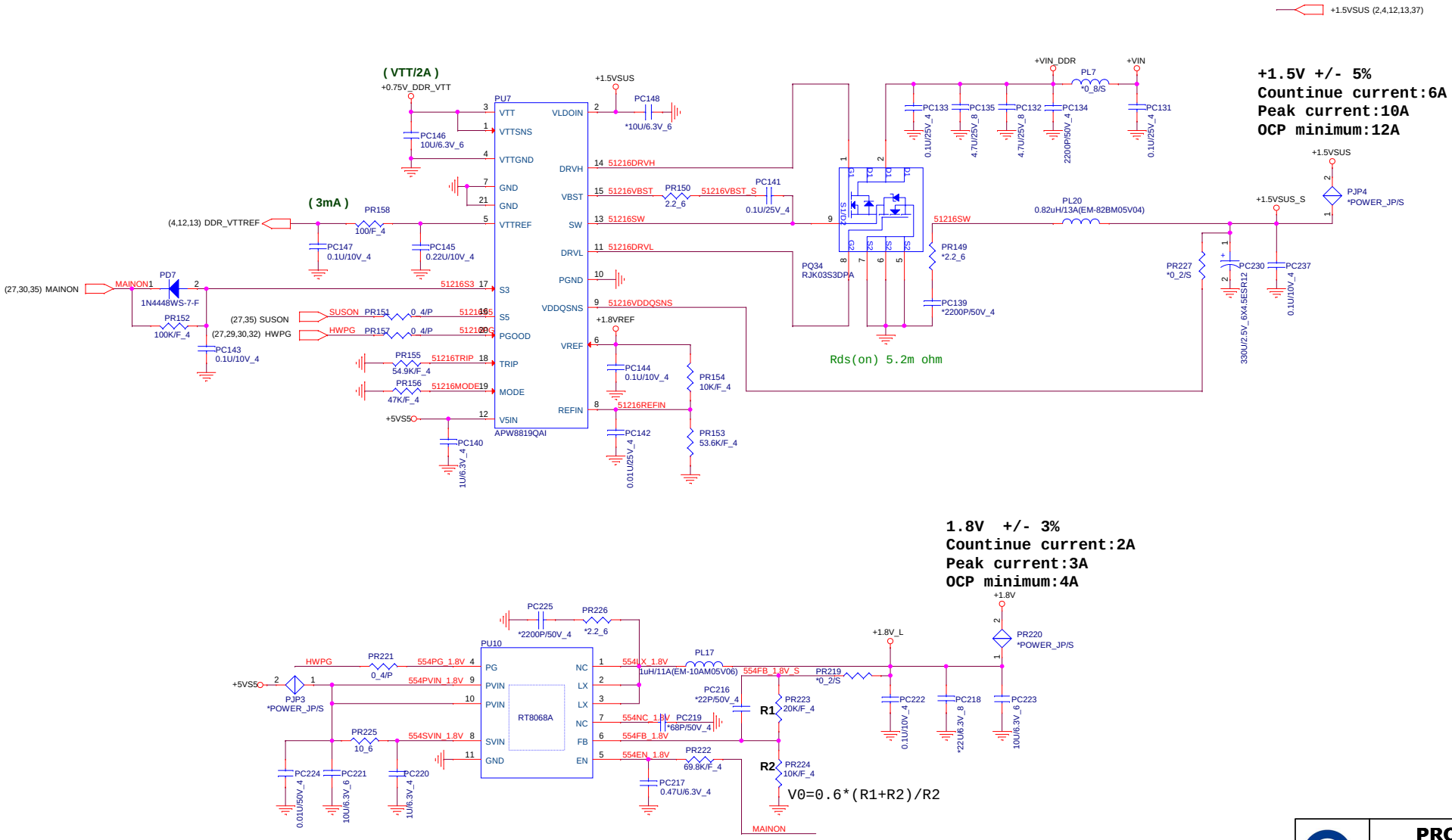

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Size	Document Number	Rev
Custom	DDR3 (APW8819)	1A

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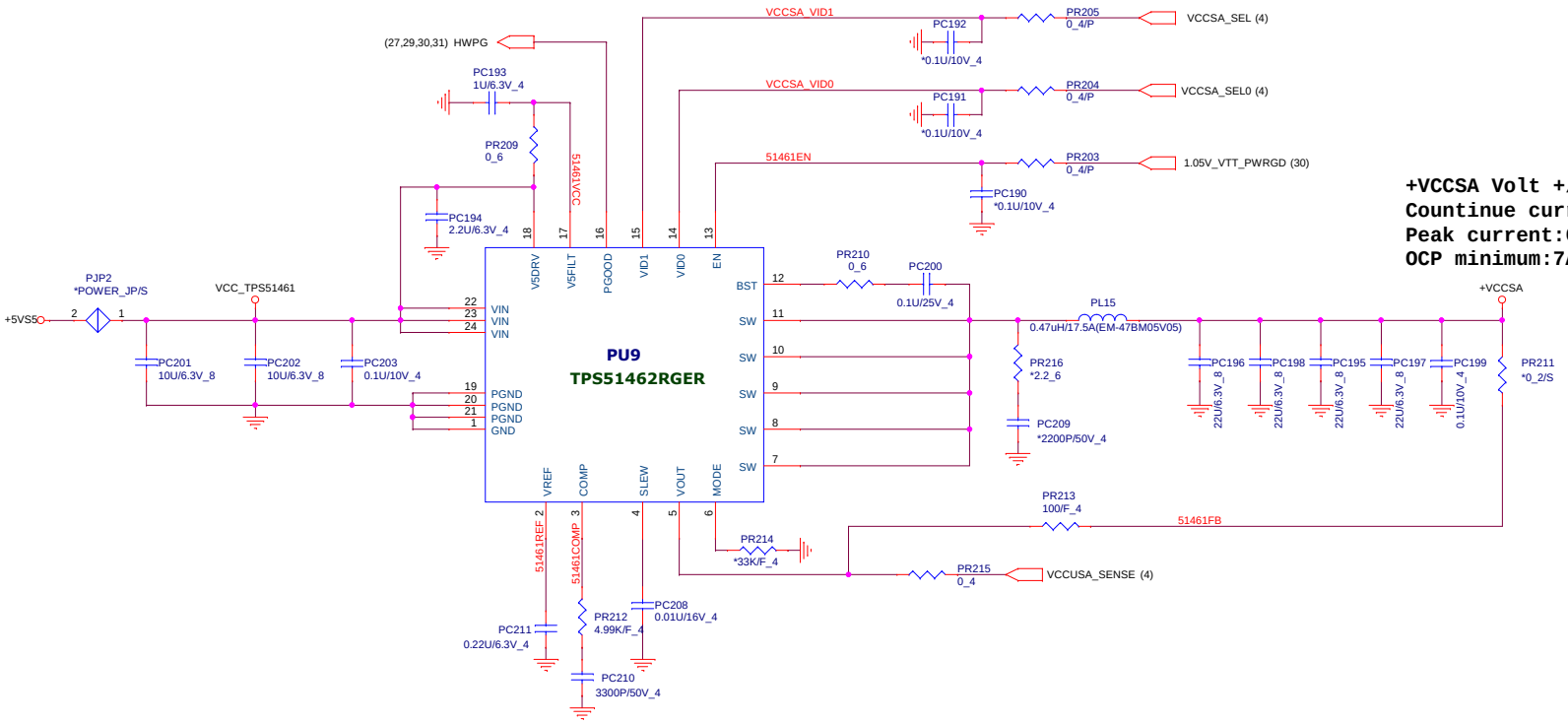
TPS51462RGER/AL051462000

For CPU SV system agent
voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

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Size	Document Number	Rev
Custom	VCCSA(TPS51462RGER)	1A

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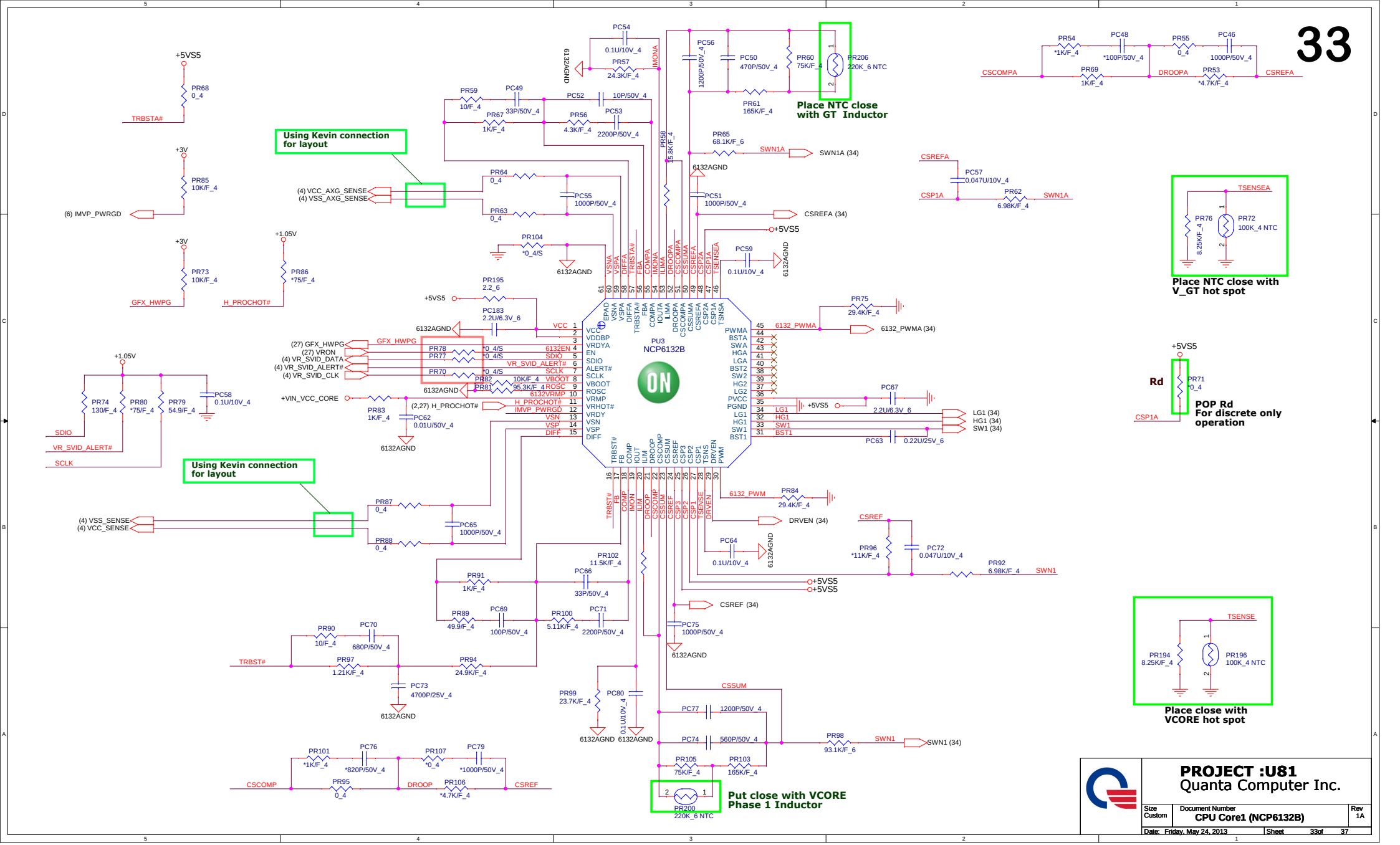
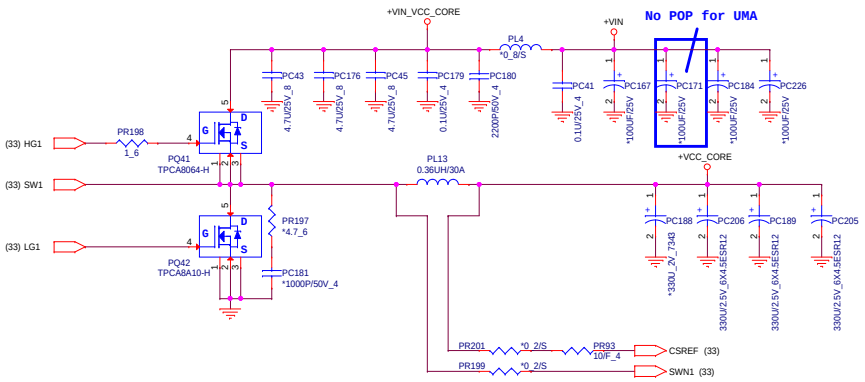
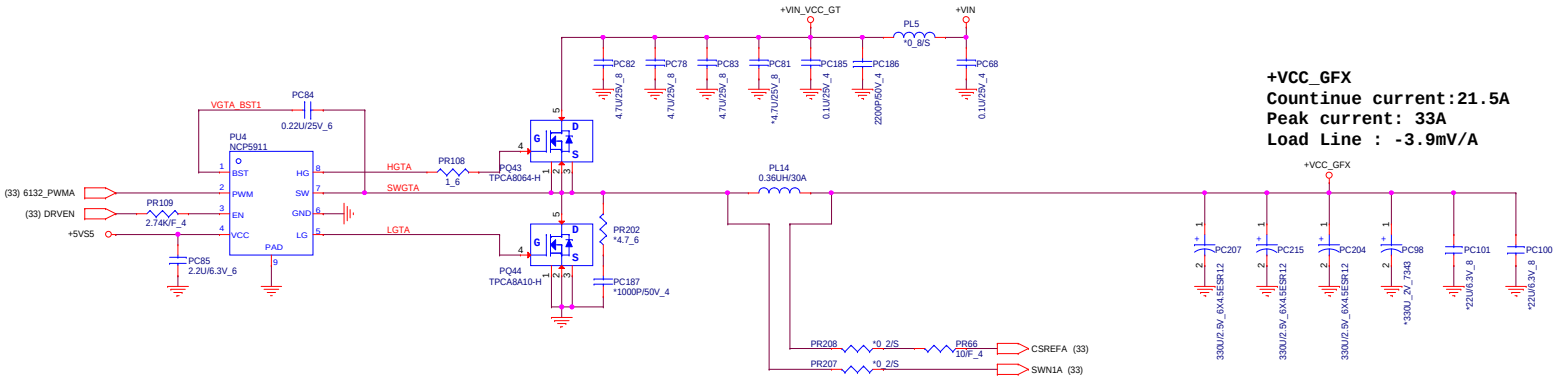




+VCC_CORE (ULV 17W)

Countinue current:16A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A

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Size	Document Number	Rev
C	CPU Core2 (NCP5911)	1A
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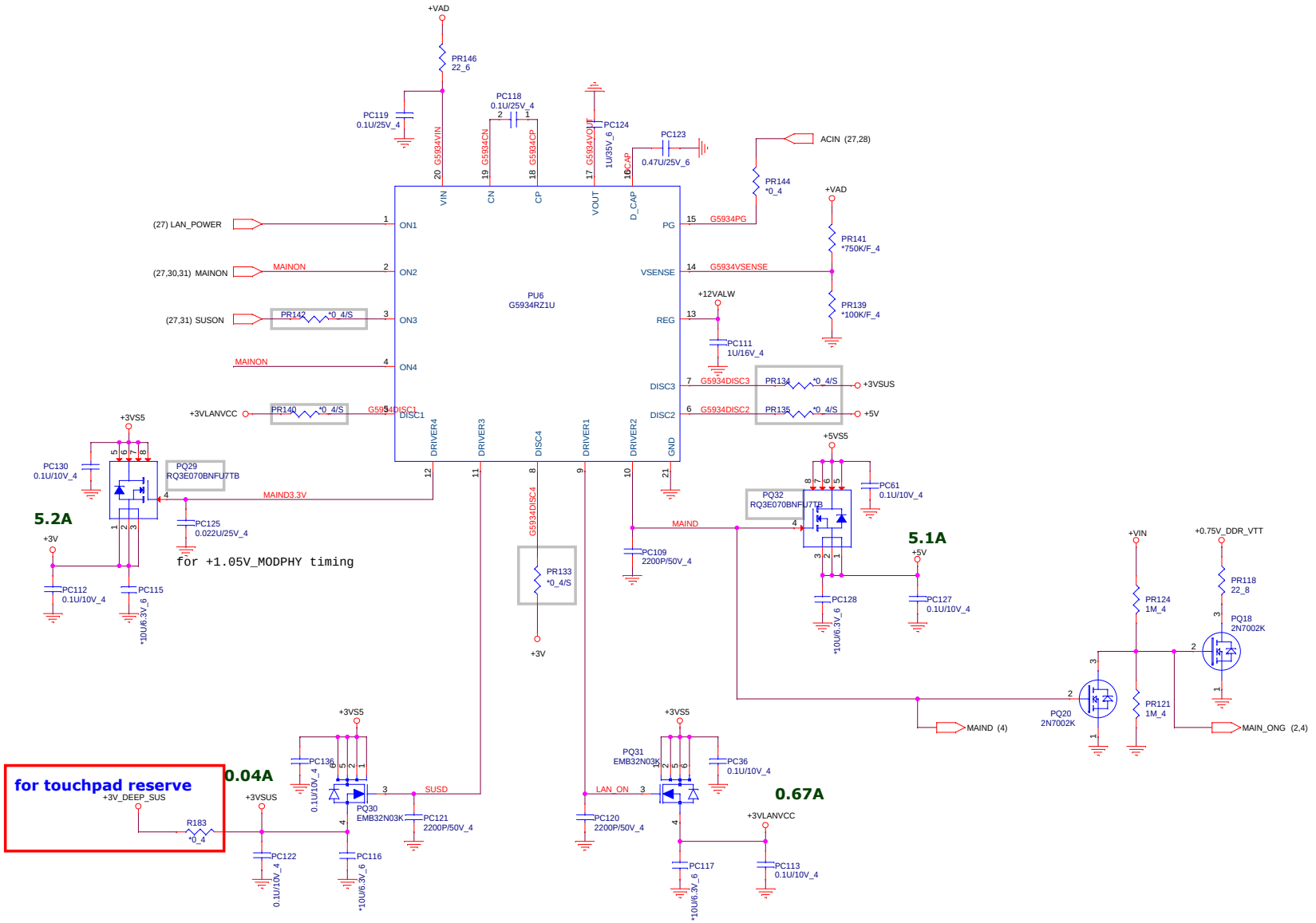

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Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
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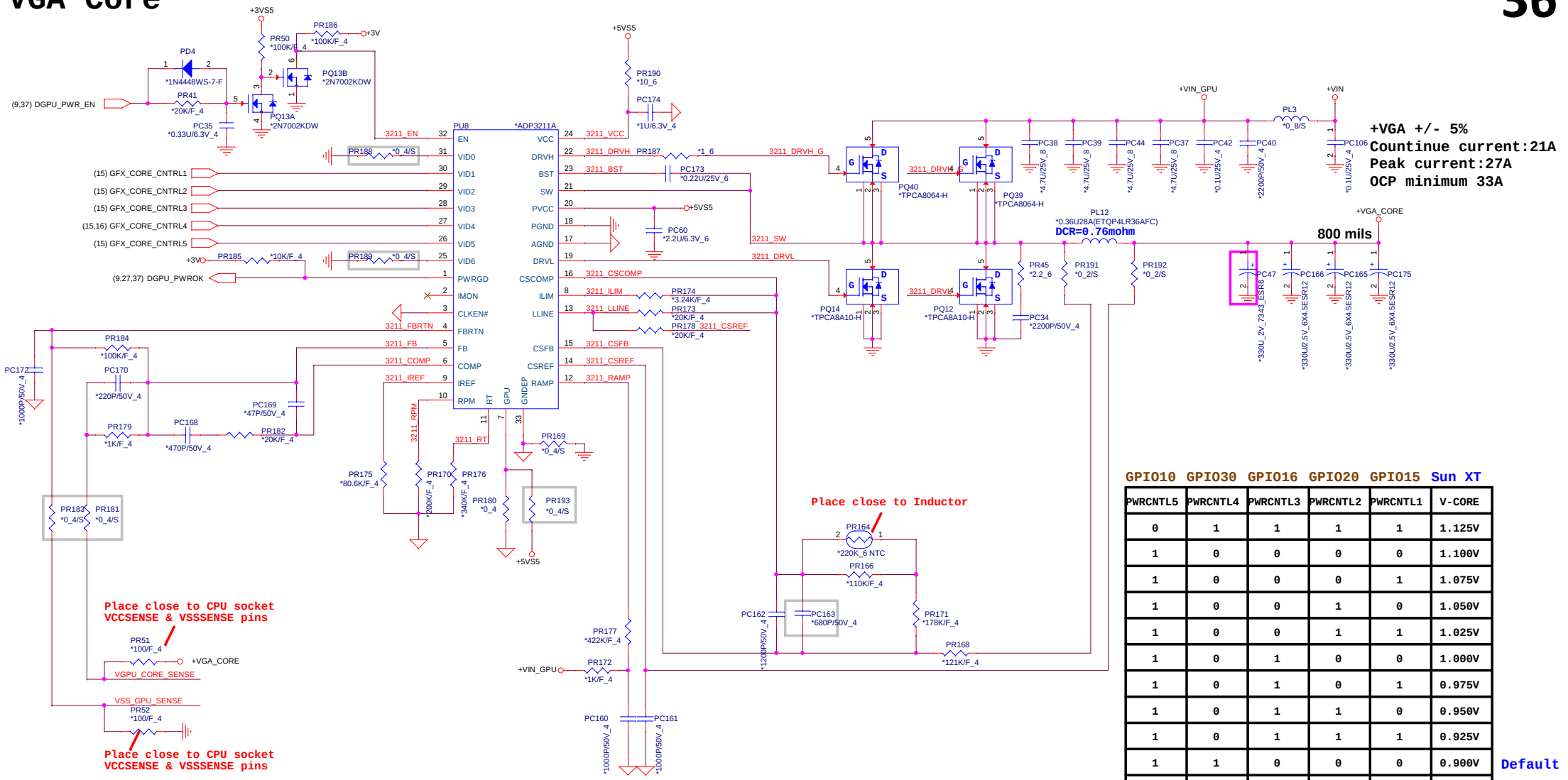
VGA Core



GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT	
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	Default
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

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Size	Document Number	Rev
Custom	+VGACORE (ADP3211)	1A
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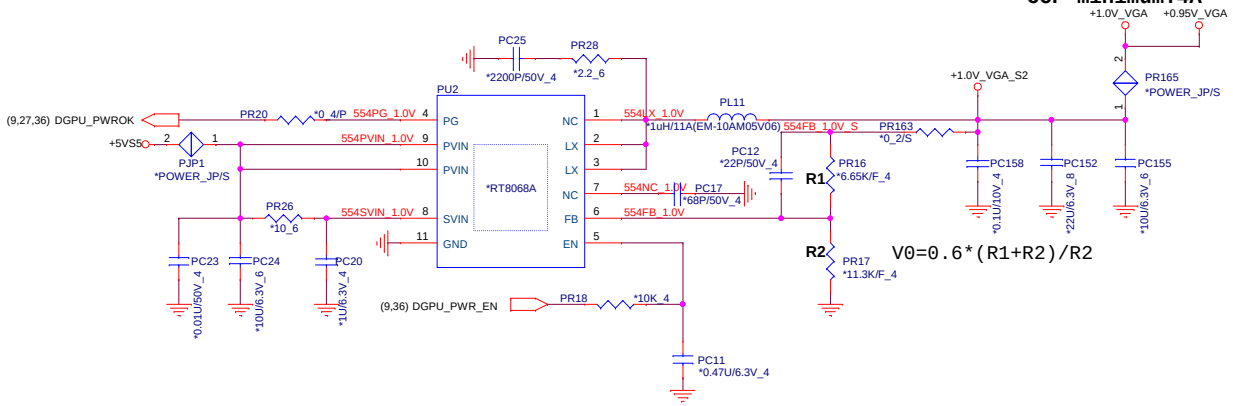
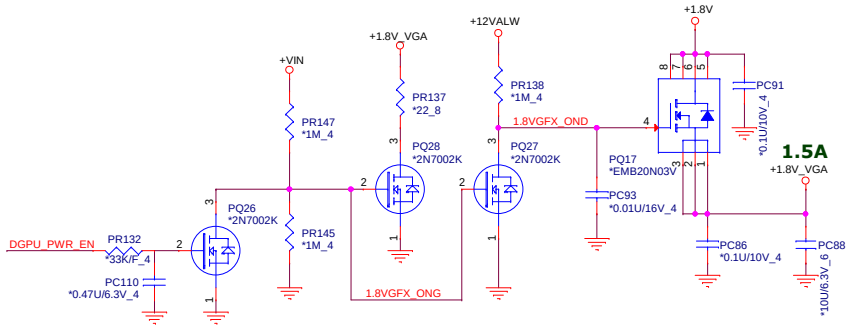
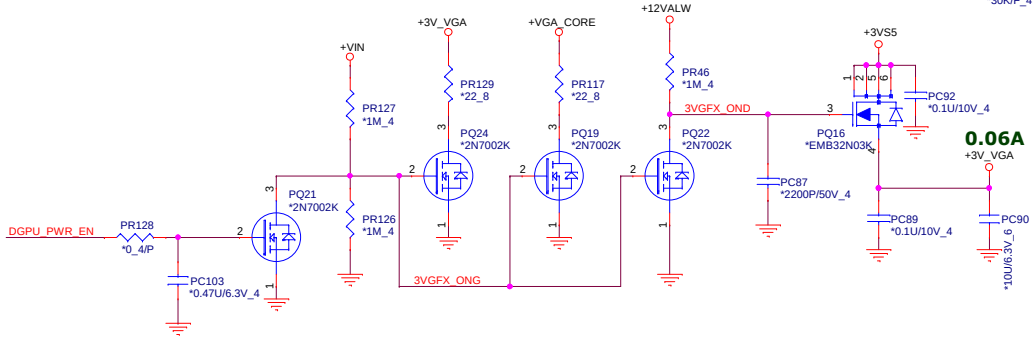
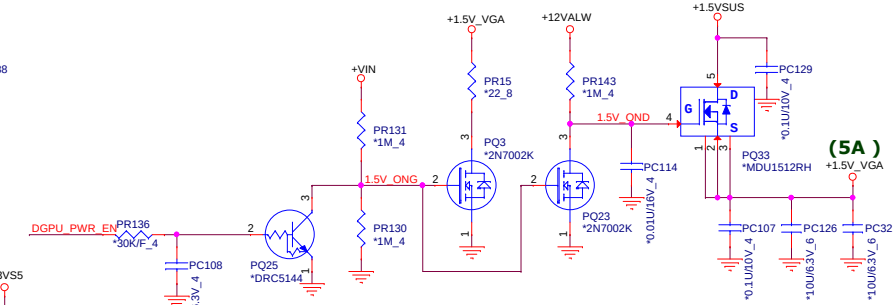
VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A









+1.5V_VGA (17,18,19,24)
+1.8V_VGA (14,15,17)
+1.0V_VGA (14,15,17,24)
+3V_VGA (14,17,24,26)

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Size	Document Number	Rev
Custom	+1.0V_VGA/1.8V_VGA/3V_VGA	1A
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