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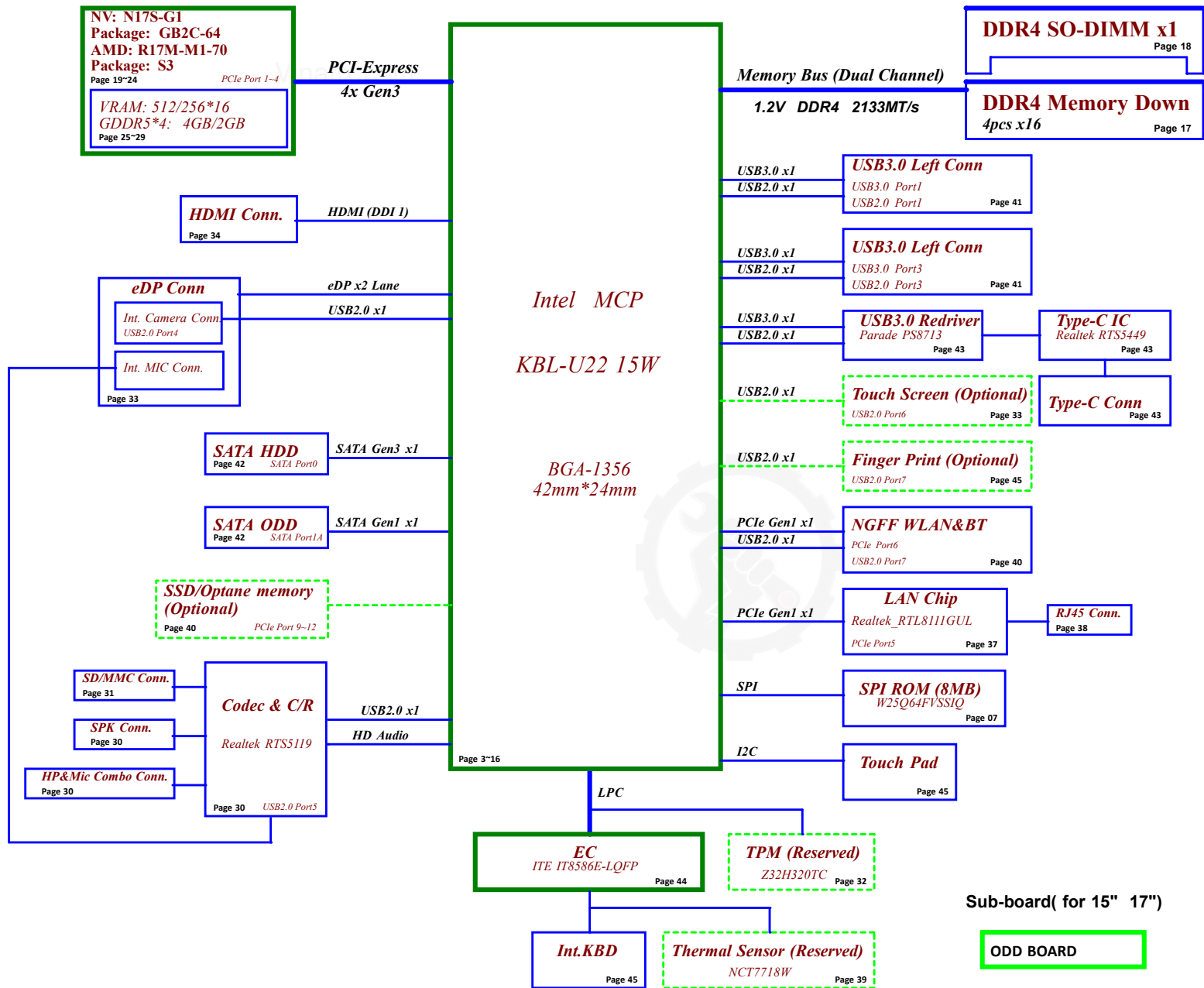
EG523 MB Schematics Document

KabyLake-U42 with DDR4 + AMD R17M-M1-70 GPU with GDDR5

2017-03-15

REV: 0.1

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Cover Page			
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				Custom	EG523	0.1	
Date:				Thursday, May 04, 2017 Sheet 1 of 60			



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane				
State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

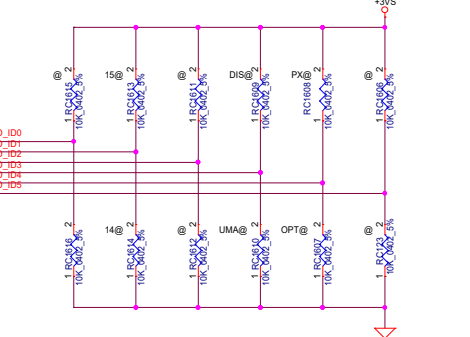
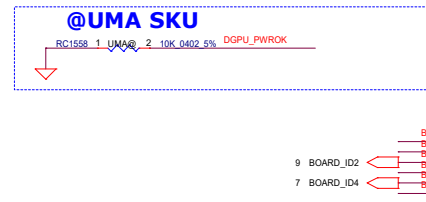
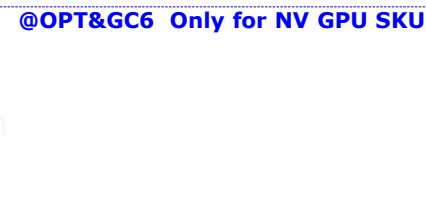
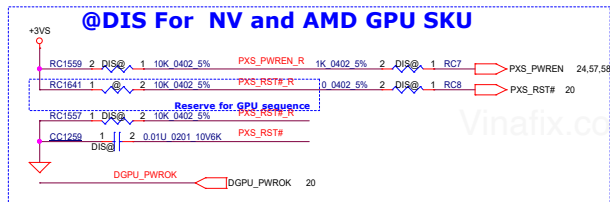
EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	DDR4 SODIMM	need to update	Wlan	need to update
Charger	0001 0010 b	PCH	need to update				
		DGPU	need to update				

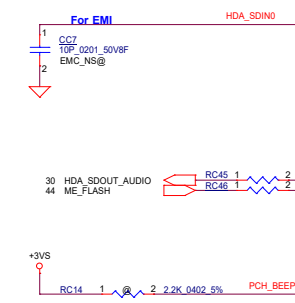
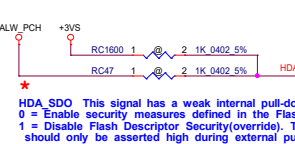
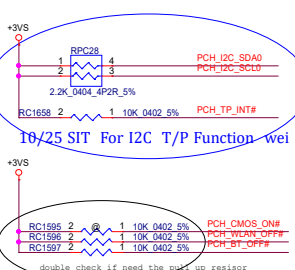
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1~4 X4 PCIE
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9~12 X4 PCIE
	Optane Memory
SATA	0 HDD
	1A ODD
	1B used as PCIE
	2 used as PCIE

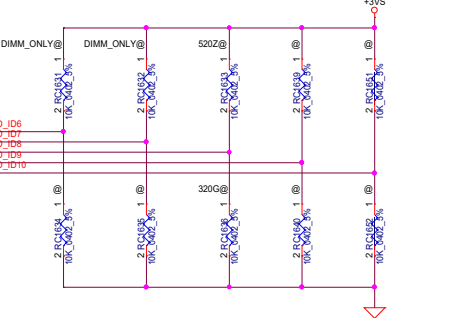
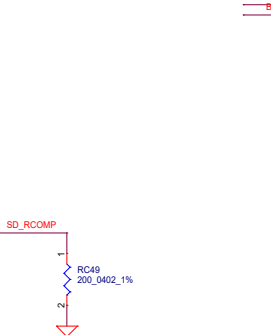
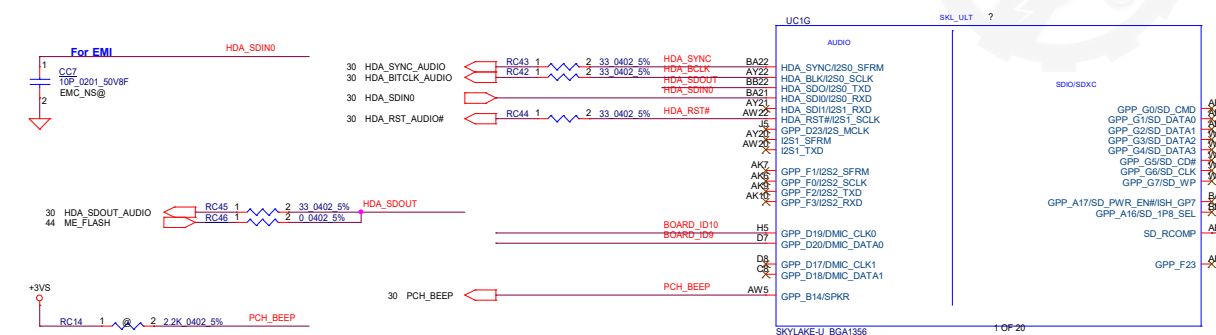
BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part



Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	RC1615 RC1613
Board_ID2	0 Reserved	RC1612
	1 Reserved	RC1611
Board_ID3	0 UMA	RC1610
	1 DIS	RC1609
Board_ID4	0 NV GPU	RC1607
	1 AMD GPU	RC1608
Board_ID5	0 Reserved	RC1623
	1 Reserved	RC1606

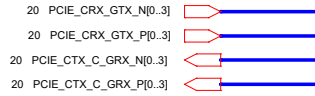


Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0 MOSI /GPP_B18	No Reboot	0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode.	0	Rising edge of PCH_PWROK
GSPI1 MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) 1 = LPC	0	Rising edge of PCH_PWROK



Board ID	Description	Stuff R
Board_ID [6,7]	00 Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01 Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10 Micron 8Gb 2400 MT/s	RC1631 RC1635
	11 SO-DIMM Only	RC1631 RC1632
Board_ID8	0 320G	RC1636
	1 520Z	RC1633
Board_ID9	0 Reserved	RC1640
	1 Reserved	RC1639
Board_ID10	0 Reserved	RC1652
	1 Reserved	RC1651

@DIS For NV and AMD GPU SKU



DGPU

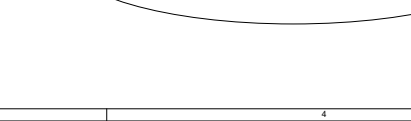
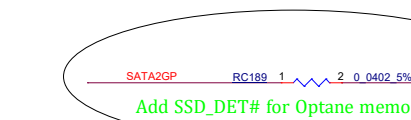
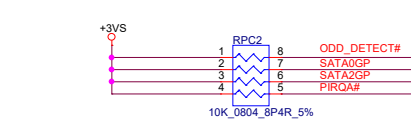
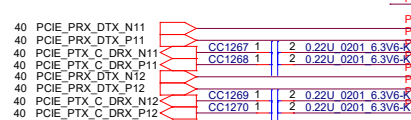
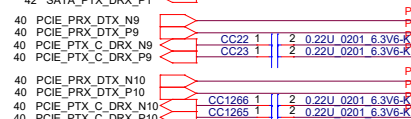
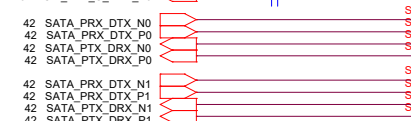
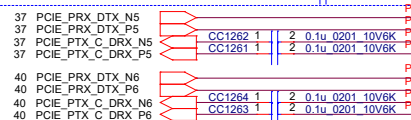
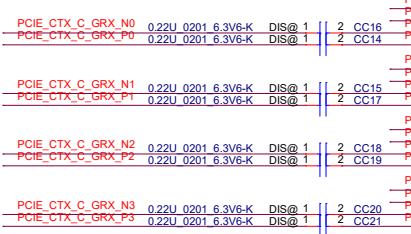
LAN

WLAN

SATA HDD

SATA ODD

Optane Memory



UC1H

SKL_UL1 ?

PCIe/USB3/SATA

SSIC / USB3

PCIe1_RXN/USB3_5_RXN

USB3_1_RXN

PCIe1_RXP/USB3_5_RXP

USB3_1_RXP

PCIe1_TXN/USB3_5_TXN

USB3_1_TXN

PCIe1_TXP/USB3_5_TXP

USB3_1_TXP

PCIe2_RXN/USB3_6_RXN

USB3_2_RXN/SSIC_1_RXN

PCIe2_RXP/USB3_6_RXP

USB3_2_RXP/SSIC_1_RXP

PCIe2_TXN/USB3_6_TXN

USB3_2_TXN/SSIC_1_TXN

PCIe2_TXP/USB3_6_TXP

USB3_2_TXP/SSIC_1_TXP

PCIe3_RXN

USB3_3_RXN/SSIC_2_RXN

PCIe3_RXP

USB3_3_RXP/SSIC_2_RXP

PCIe3_TXN

USB3_3_TXN/SSIC_2_TXN

PCIe3_TXP

USB3_3_TXP/SSIC_2_TXP

PCIe4_RXN

USB3_4_RXN

PCIe4_RXP

USB3_4_RXP

PCIe4_TXN

USB3_4_TXN

PCIe4_TXP

USB3_4_TXP

PCIe5_RXN

USB2N_1

PCIe5_RXP

USB2P_1

PCIe5_TXN

USB2N_2

PCIe5_TXP

USB2P_2

PCIe6_RXN

USB2N_3

PCIe6_RXP

USB2P_3

PCIe6_TXN

USB2N_4

PCIe6_TXP

USB2P_4

PCIe7_RXN/SATA0_RXN

USB2N_5

PCIe7_RXP/SATA0_RXP

USB2P_5

PCIe7_TXN/SATA0_TXN

USB2N_6

PCIe7_TXP/SATA0_TXP

USB2P_6

PCIe8_RXN/SATA1A_RXN

USB2N_7

PCIe8_RXP/SATA1A_RXP

USB2P_7

PCIe8_TXN/SATA1A_TXN

USB2N_8

PCIe8_TXP/SATA1A_TXP

USB2P_8

PCIe9_RXN

USB2N_9

PCIe9_RXP

USB2P_9

PCIe9_TXN

USB2N_10

PCIe9_TXP

USB2P_10

PCIe10_RXN

USB2N_11

PCIe10_RXP

USB2P_11

PCIe10_TXN

USB2N_12

PCIe10_TXP

USB2P_12

PCIe11_RXN/SATA1B_RXN

USB2N_13

PCIe11_RXP/SATA1B_RXP

USB2P_13

PCIe11_TXN/SATA1B_TXN

USB2N_14

PCIe11_TXP/SATA1B_TXP

USB2P_14

PCIe12_RXN/SATA2_RXN

USB2N_15

PCIe12_RXP/SATA2_RXP

USB2P_15

PCIe12_TXN/SATA2_TXN

USB2N_16

PCIe12_TXP/SATA2_TXP

USB2P_16

PCIe13_RXN/SATA3_RXN

USB2N_17

PCIe13_RXP/SATA3_RXP

USB2P_17

PCIe13_TXN/SATA3_TXN

USB2N_18

PCIe13_TXP/SATA3_TXP

USB2P_18

PCIe14_RXN/SATA4_RXN

USB2N_19

PCIe14_RXP/SATA4_RXP

USB2P_19

PCIe14_TXN/SATA4_TXN

USB2N_20

PCIe14_TXP/SATA4_TXP

USB2P_20

PCIe15_RXN/SATA5_RXN

USB2N_21

PCIe15_RXP/SATA5_RXP

USB2P_21

PCIe15_TXN/SATA5_TXN

USB2N_22

PCIe15_TXP/SATA5_TXP

USB2P_22

USB3_1_RXN

USB3_1_RXP

USB3_1_TXN

USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN

USB3_2_RXP/SSIC_1_RXP

USB3_2_TXN/SSIC_1_TXN

USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN

USB3_3_RXP/SSIC_2_RXP

USB3_3_TXN/SSIC_2_TXN

USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN

USB3_4_RXP

USB3_4_TXN

USB3_4_TXP

USB2N_1

USB2P_1

USB2N_2

USB2P_2

USB2N_3

USB2P_3

USB2N_4

USB2P_4

USB2N_5

USB2P_5

USB2N_6

USB2P_6

USB2N_7

USB2P_7

USB2N_8

USB2P_8

USB2N_9

USB2P_9

USB2N_10

USB2P_10

USB2N_11

USB2P_11

USB2N_12

USB2P_12

USB2N_13

USB2P_13

USB2N_14

USB2P_14

USB2N_15

USB2P_15

USB2N_16

USB2P_16

USB2N_17

USB2P_17

USB2N_18

USB2P_18

USB2N_19

USB2P_19

USB2N_20

USB2P_20

USB2N_21

USB2P_21

USB2N_22

USB2P_22

USB3_1_RXN

USB3_1_RXP

USB3_1_TXN

USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN

USB3_2_RXP/SSIC_1_RXP

USB3_2_TXN/SSIC_1_TXN

USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN

USB3_3_RXP/SSIC_2_RXP

USB3_3_TXN/SSIC_2_TXN

USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN

USB3_4_RXP

USB3_4_TXN

USB3_4_TXP

USB2N_1

USB2P_1

USB2N_2

USB2P_2

USB2N_3

USB2P_3

USB2N_4

USB2P_4

USB2N_5

USB2P_5

USB2N_6

USB2P_6

USB2N_7

USB2P_7

USB2N_8

USB2P_8

USB2N_9

USB2P_9

USB2N_10

USB2P_10

USB2N_11

USB2P_11

USB2N_12

USB2P_12

USB2N_13

USB2P_13

USB2N_14

USB2P_14

USB2N_15

USB2P_15

USB2N_16

USB2P_16

USB2N_17

USB2P_17

USB2N_18

USB2P_18

USB2N_19

USB2P_19

USB2N_20

USB2P_20

USB2N_21

USB2P_21

USB2N_22

USB2P_22

USB3_1_RXN

USB3_1_RXP

USB3_1_TXN

USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN

USB3_2_RXP/SSIC_1_RXP

USB3_2_TXN/SSIC_1_TXN

USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN

USB3_3_RXP/SSIC_2_RXP

USB3_3_TXN/SSIC_2_TXN

USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN

USB3_4_RXP

USB3_4_TXN

USB3_4_TXP

USB2N_1

USB2P_1

USB2N_2

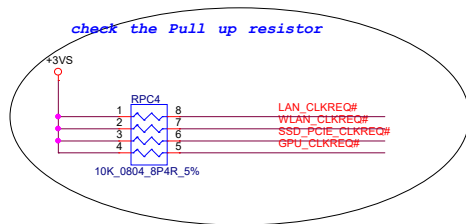
USB2P_2

USB2N_3

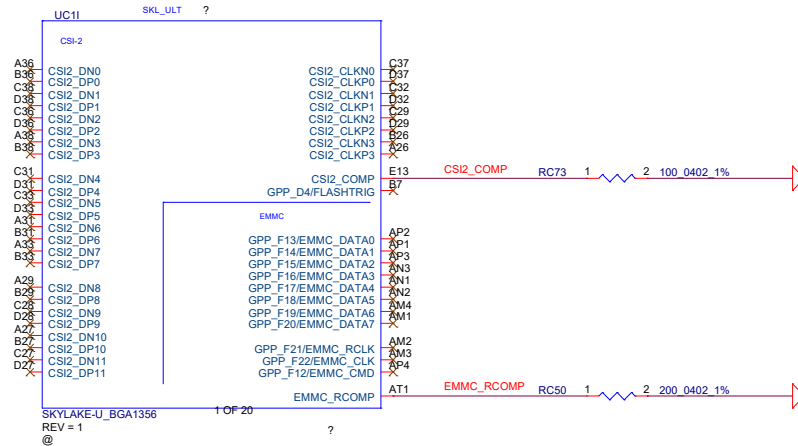
USB2P_3

USB2N_4

USB2P_4

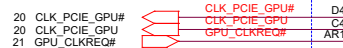


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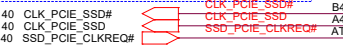


@DIS For NV and AMD GPU SKU

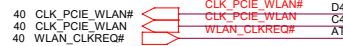
PCIE CLK0 DGPU



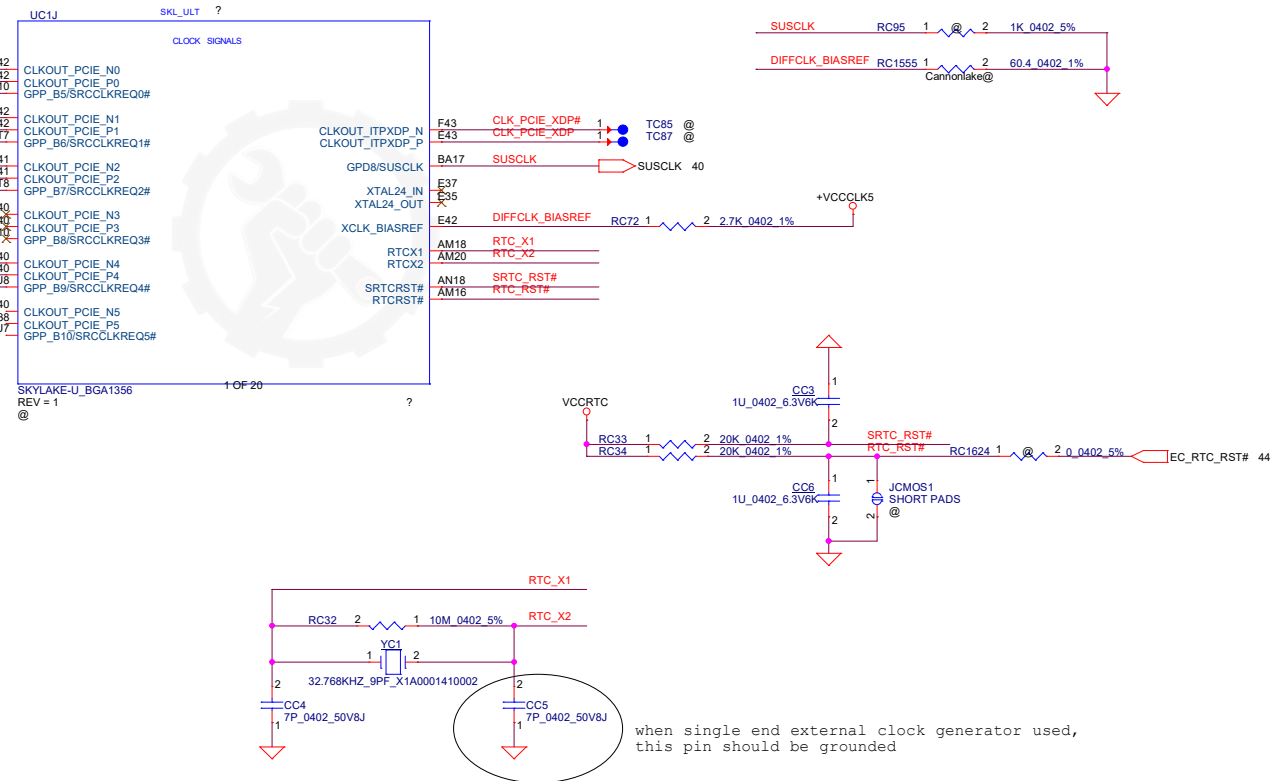
Optane memory




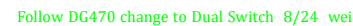
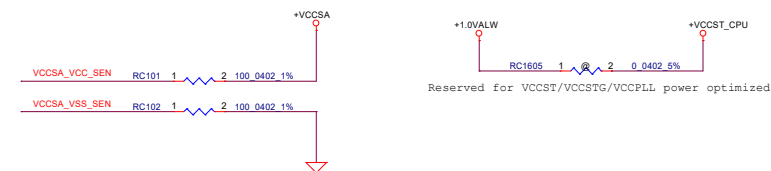
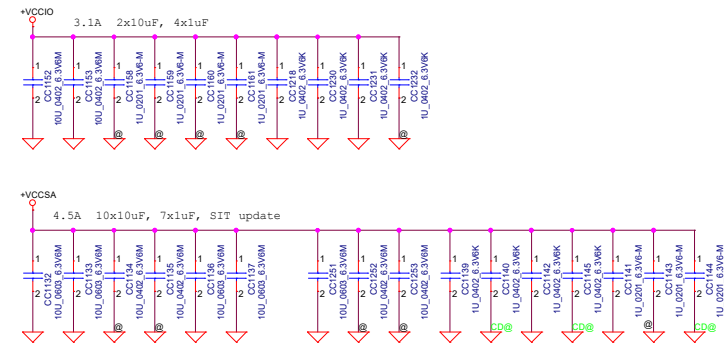
PCIE CLK5 WLAN




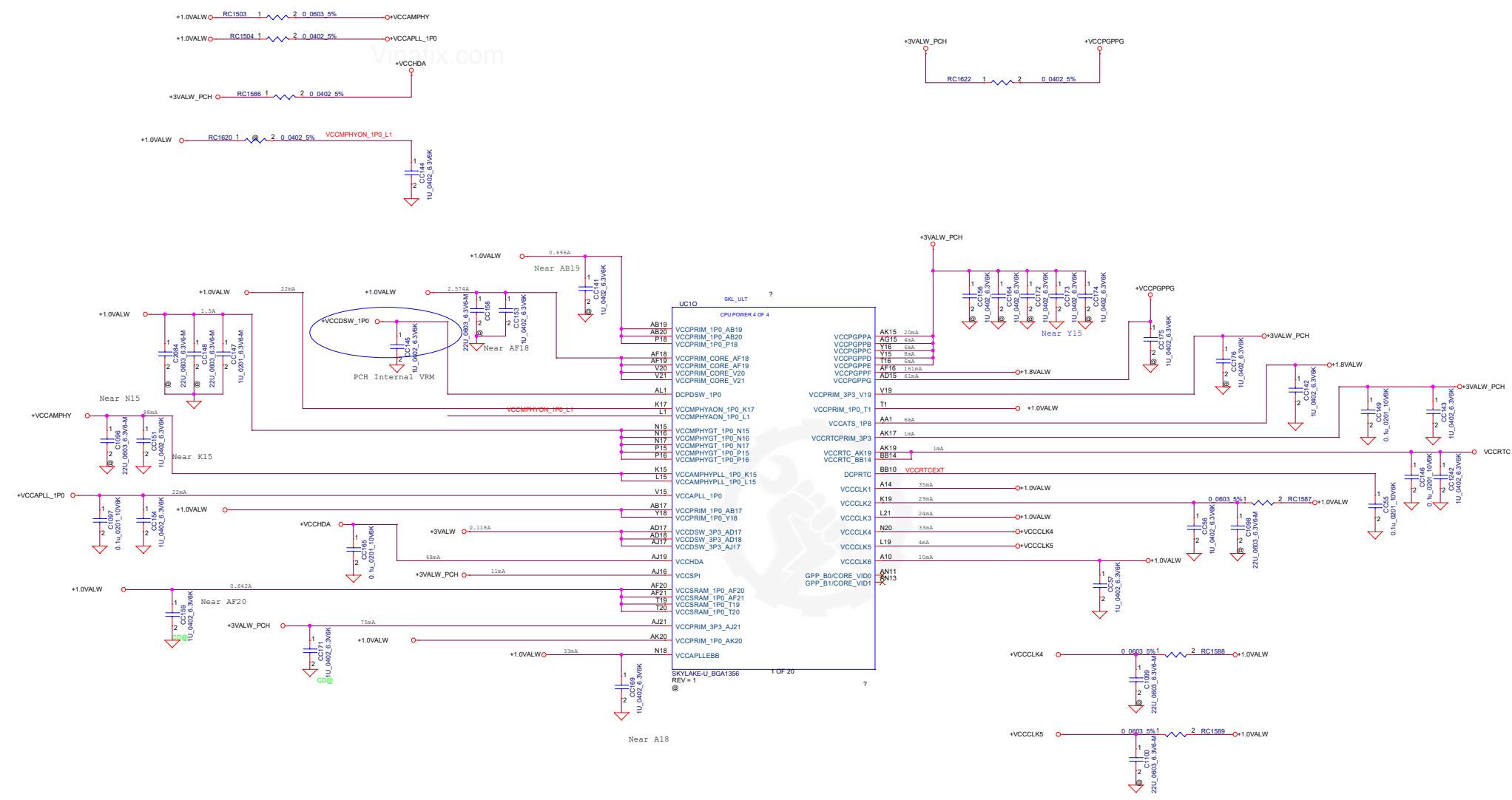
PCIE CLK4 LAN

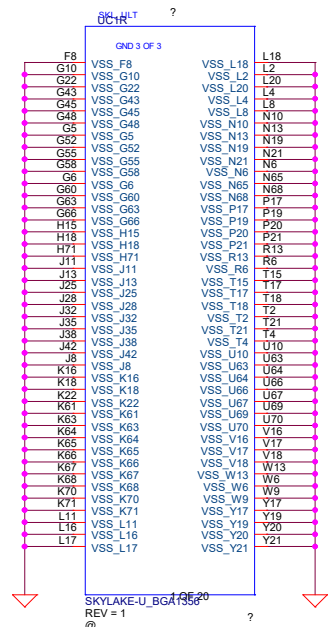
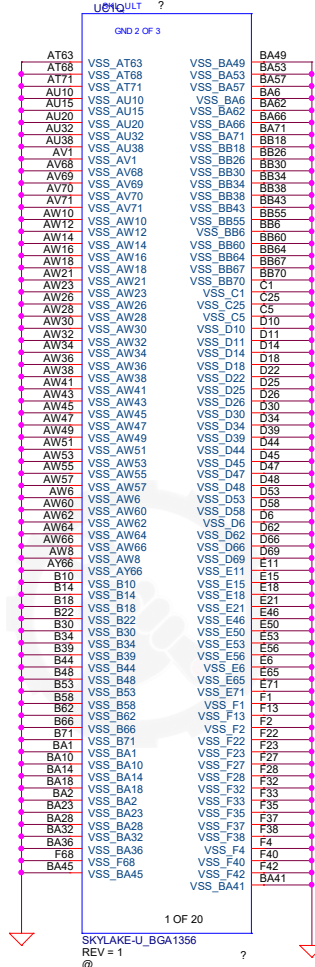



Security Classification		LC Future Center Secret Data		Title				
Issued Date	2016/12/14	Deciphered Date	2017/12/13	MCP (CSI2,EMMC,CLOCK)				
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				Custom	EG523	0.1		
				Date:	Thursday, May 04, 2017	Sheet	10 of 60	

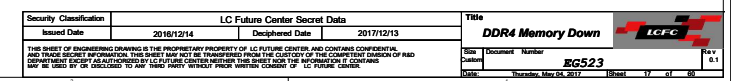


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Size		Document Number		EG521		Rev
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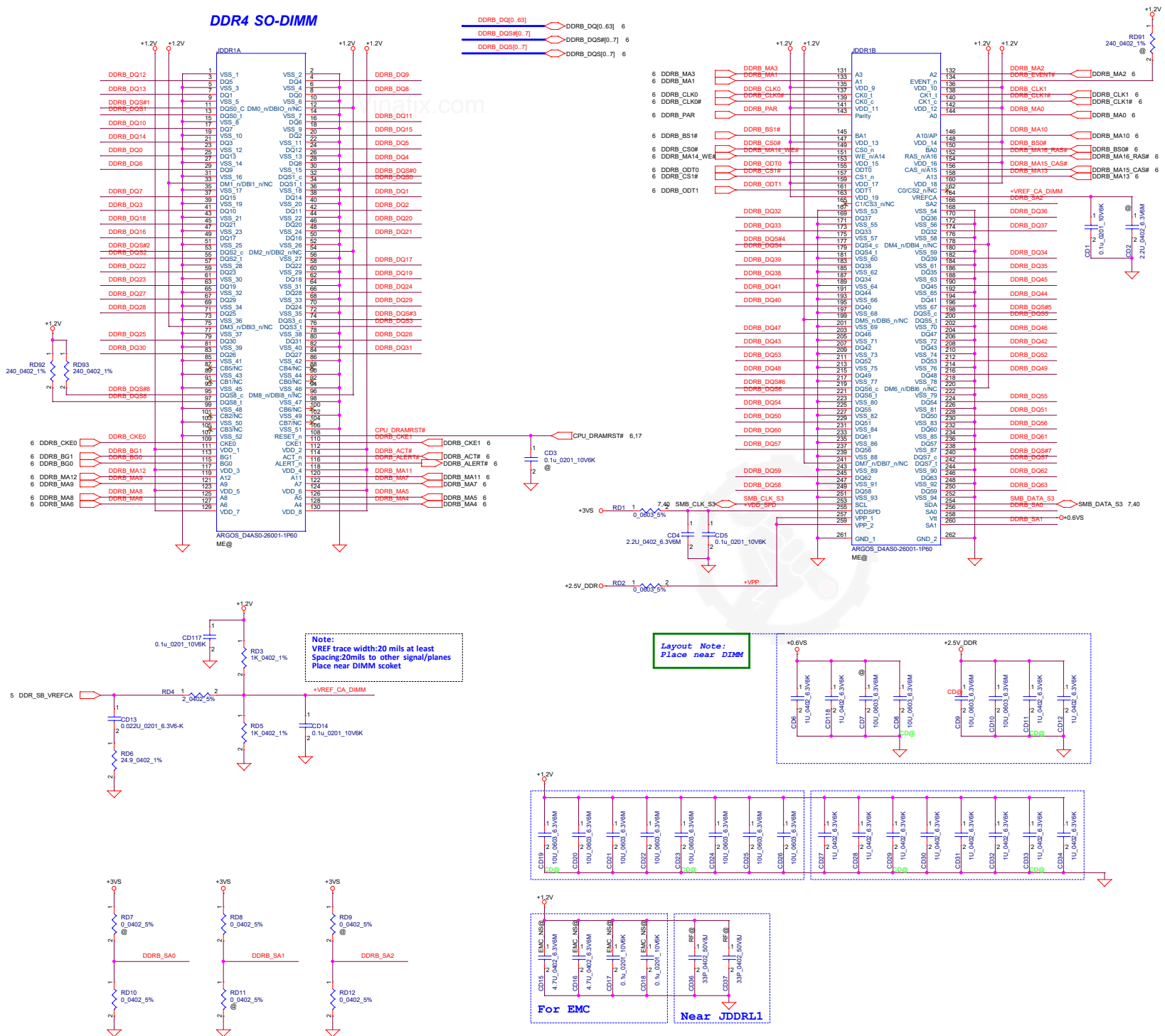





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				Date:	Thursday, May 04, 2017	Sheet 15 of 60



DDR4 SO-DIMM



SPD Address = 2H

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Custom	EG523				1 of 50
				Sheet	16 of 50

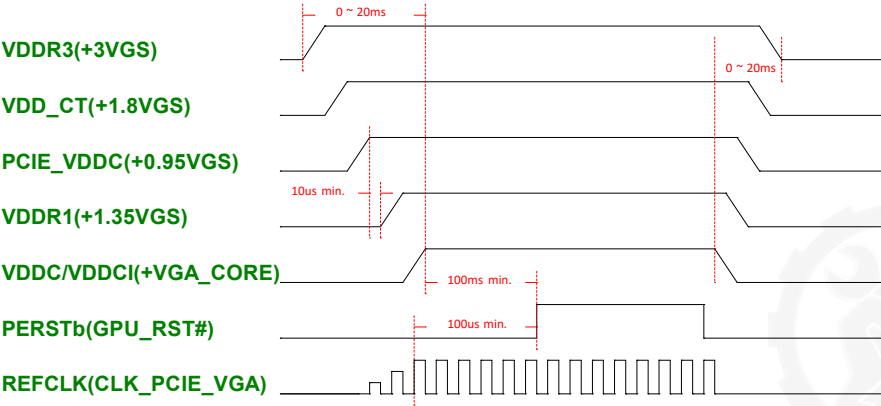
Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s) For power down, reversing the ramp-up sequence is recommended.

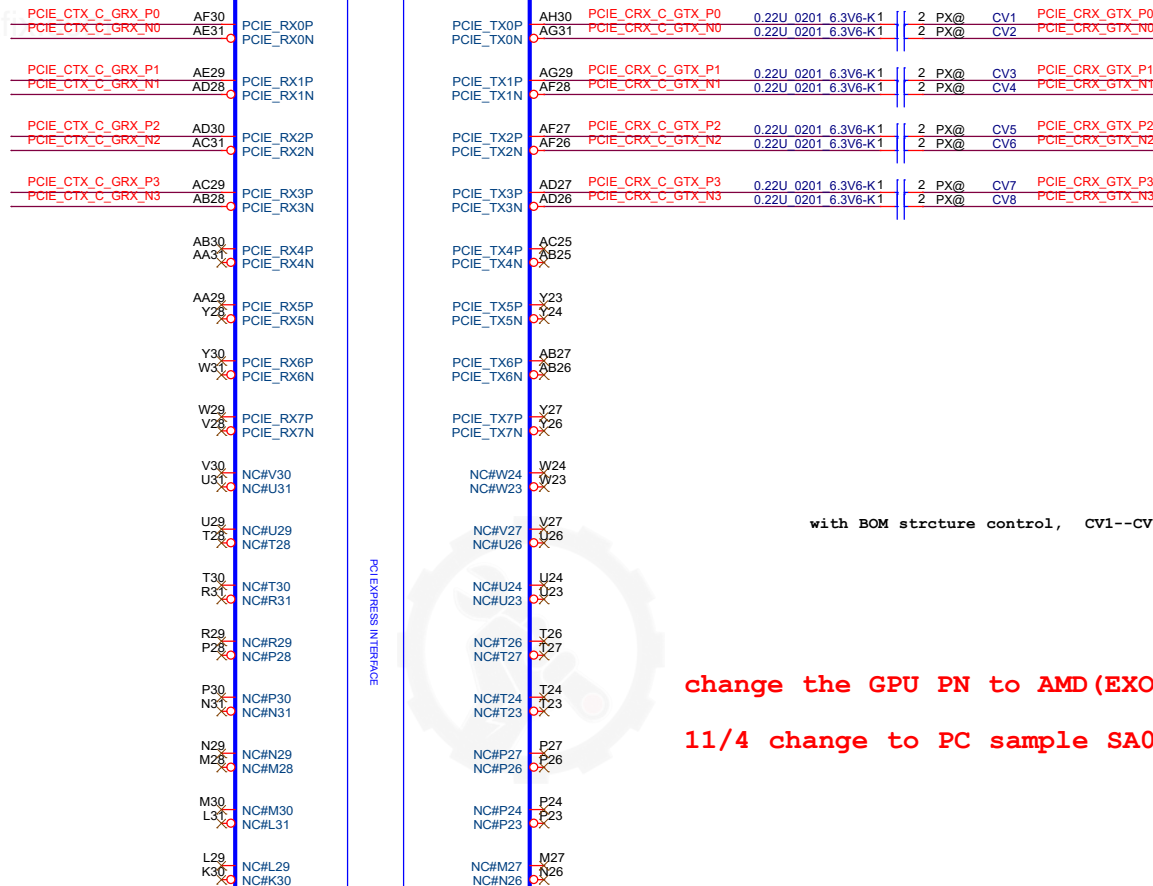


VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70-A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

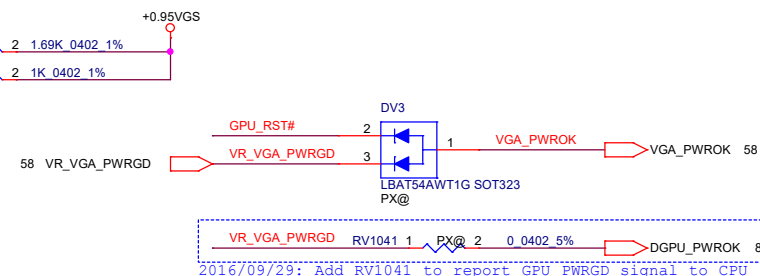
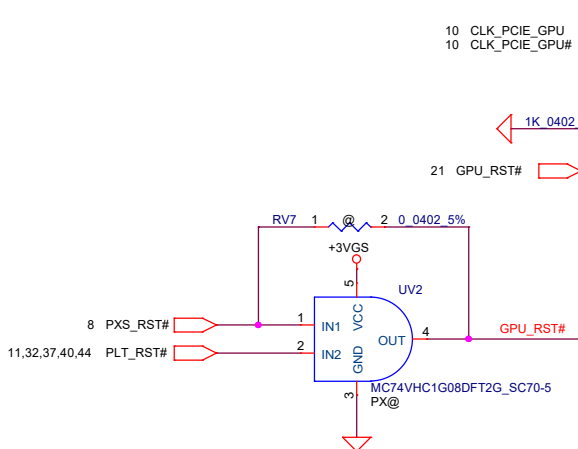
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9 PCIE_CTX_C_GRX_N[0..3] PCIE_CTX_C_GRX_N[0..3]

PCIE_CRX_GTX_P[0..3] PCIE_CRX_GTX_P[0..3] 9
PCIE_CRX_GTX_N[0..3] PCIE_CRX_GTX_N[0..3] 9



with BOM struture control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD (EXO-S3 PRO), symbol check ok
11/4 change to PC sample SA000074V10

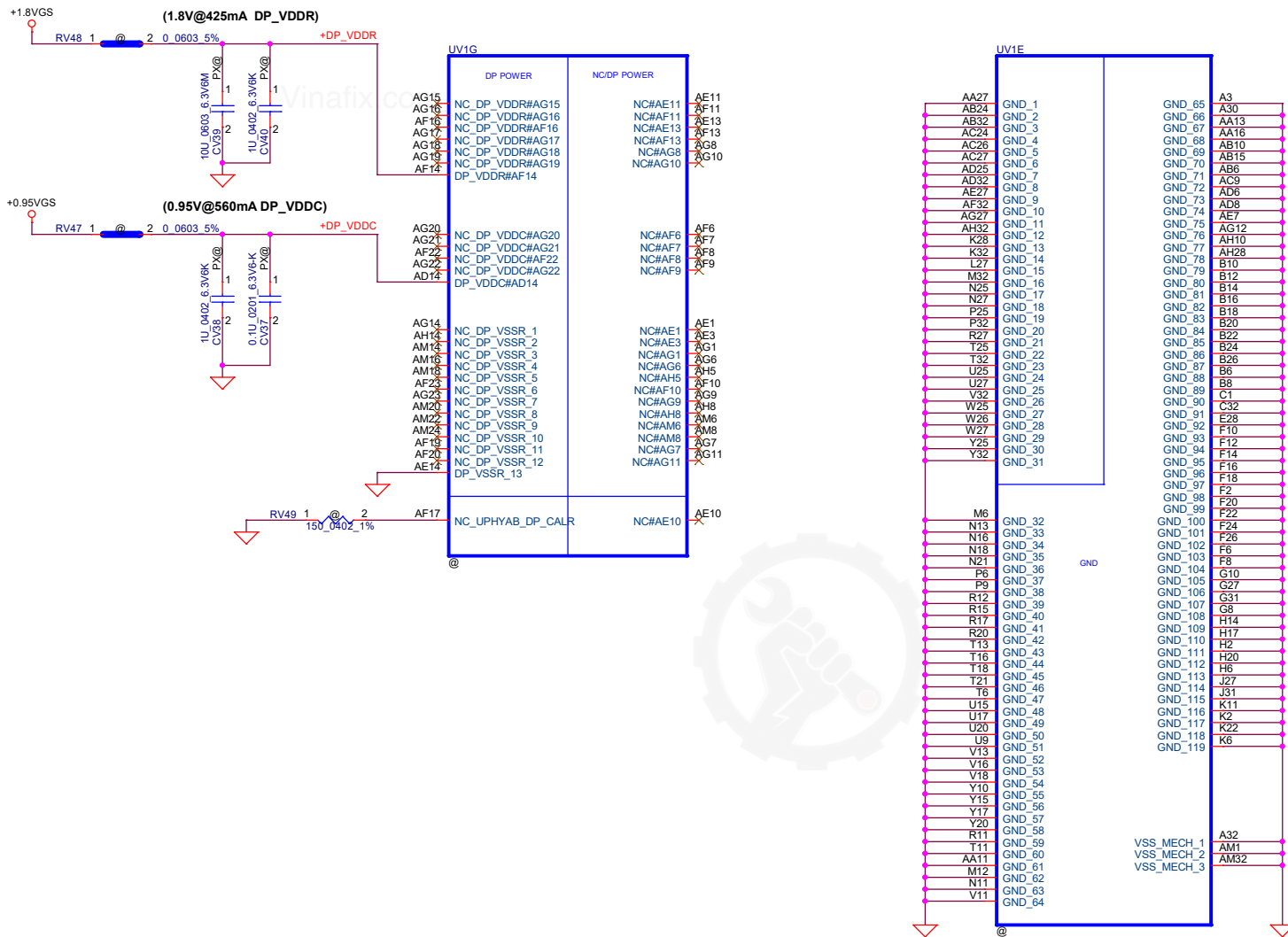


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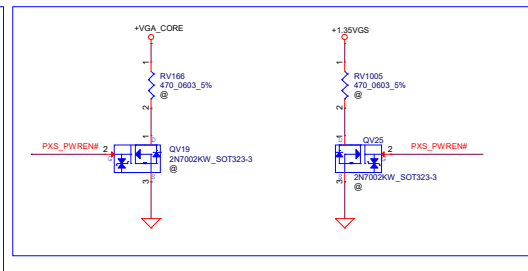
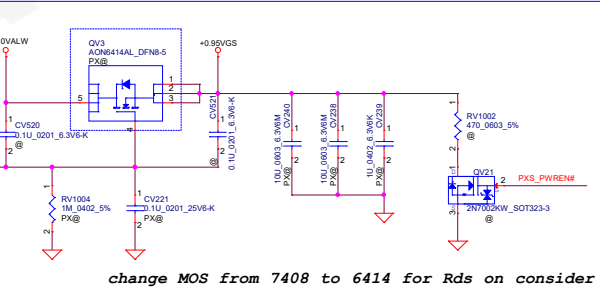
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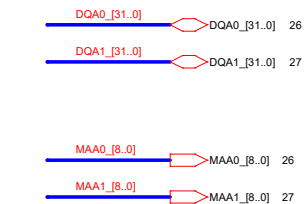
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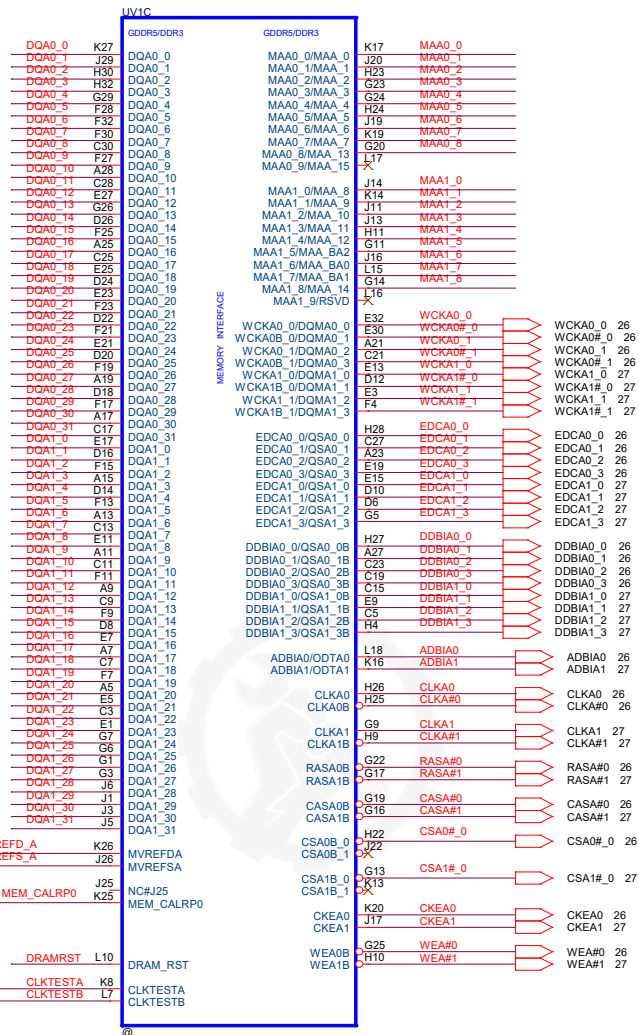
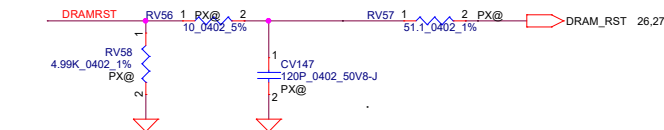
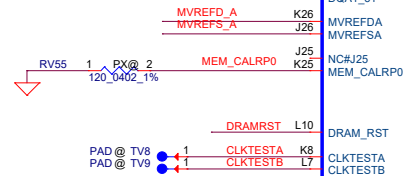
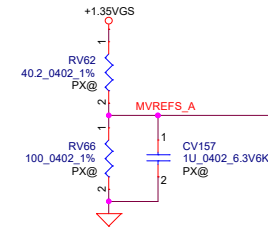
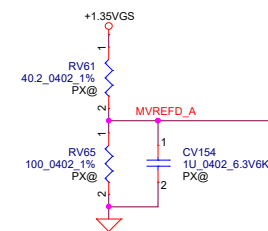
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Issued Date	2016/12/14	Deciphered Date	2017/12/13	ATI_R17M-M1-70_DP Power	
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				Date: Thursday, May 04, 2017	Sheet 23 of 60
				Rev 0.1	



Title			
ATI_R17M-M1-70_Power			
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				Date: Thursday, May 04, 2017	Rev 0.1
				Sheet 25	of 60

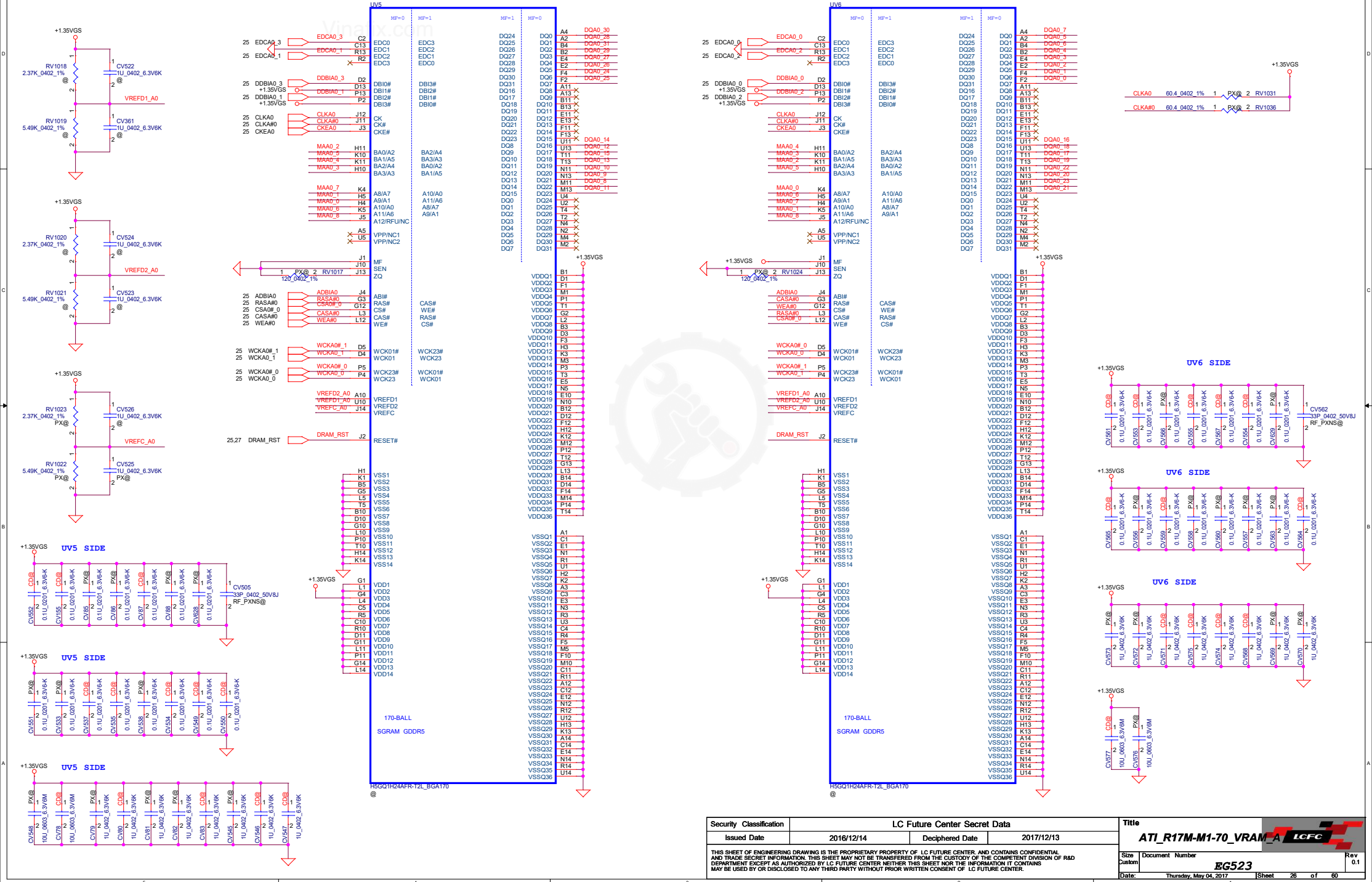
Lower 32 bits

DQAO[31..0] 25

 MAAO[8..0] 25

MF=0 No Mirror

MF=1 Mirror



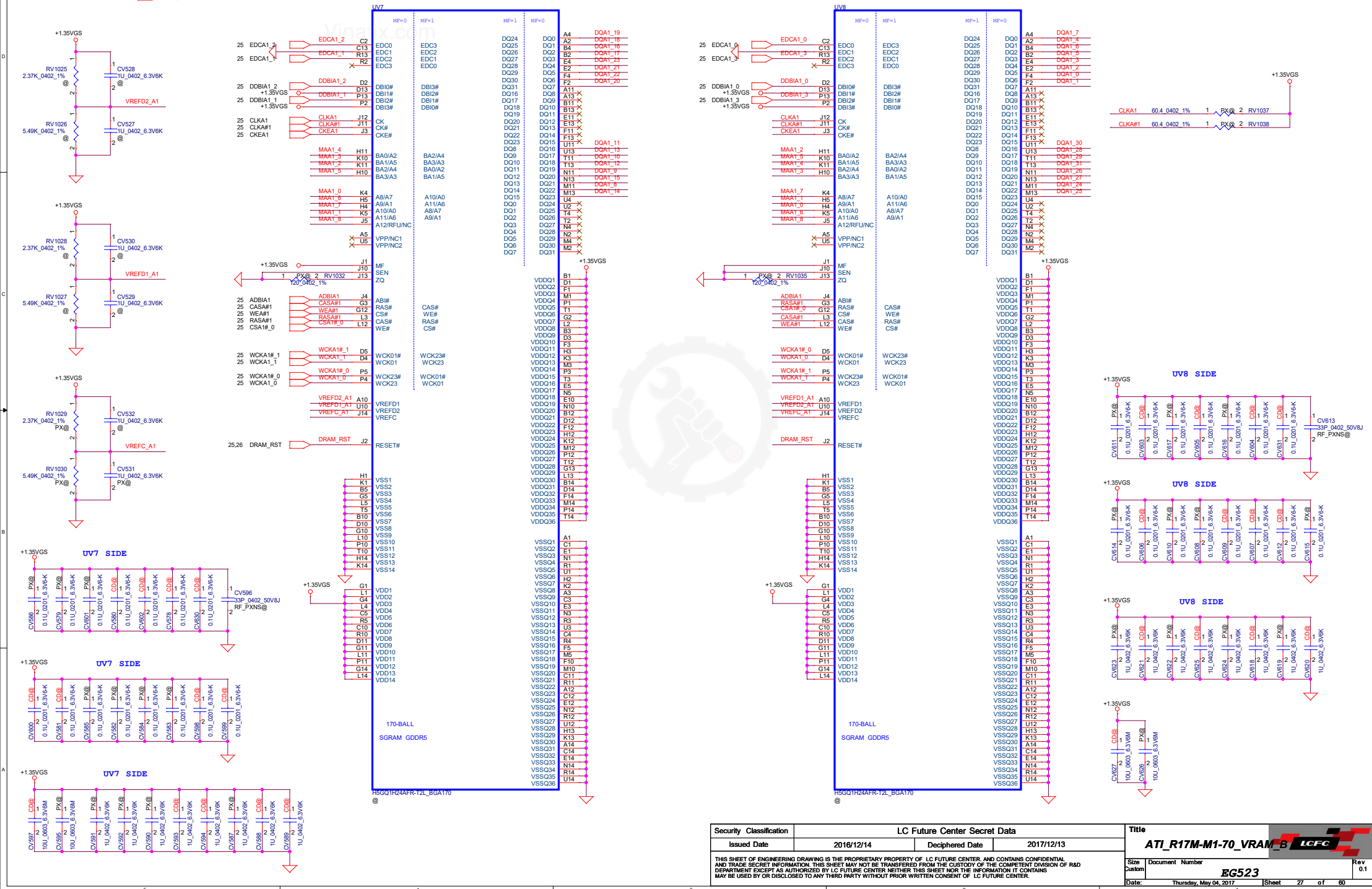
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				Sheet	26 of 60

Upper 32 bits

DQA1_[31..0] 25
MAA1_[8..0] 25

MF=1 Mirror

MF=0 No Mirror



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				Sheet 28 of 60	

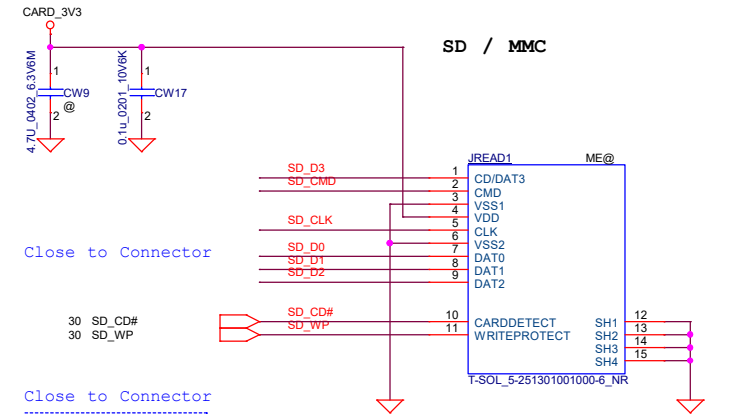
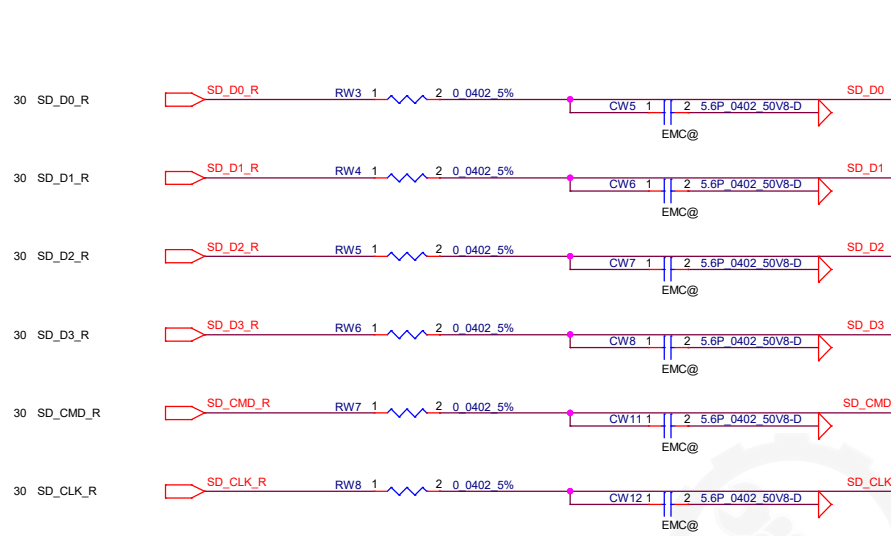
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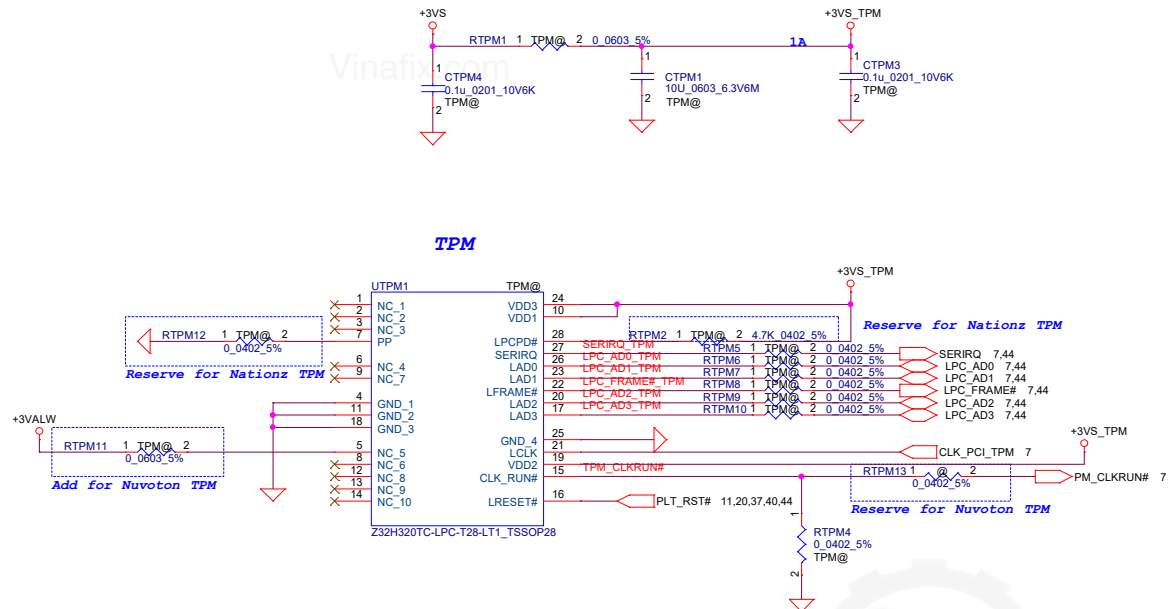
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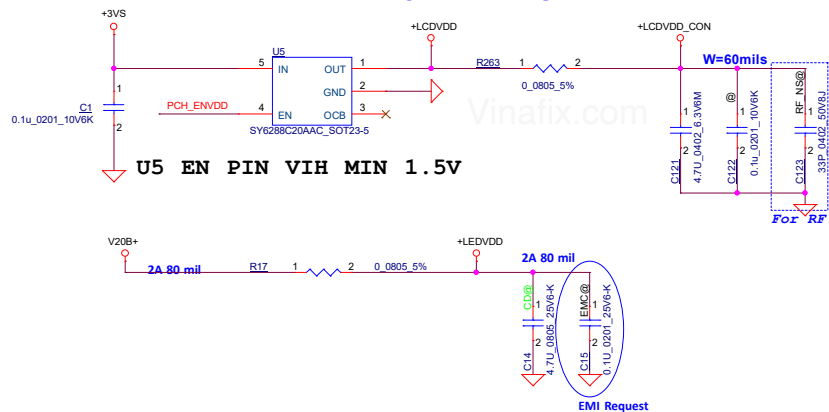
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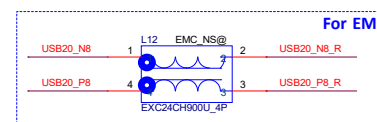
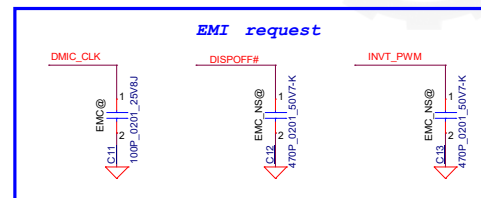
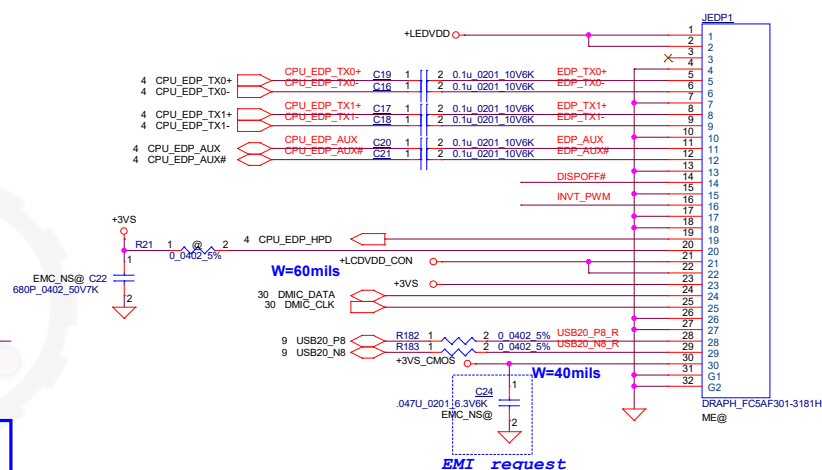
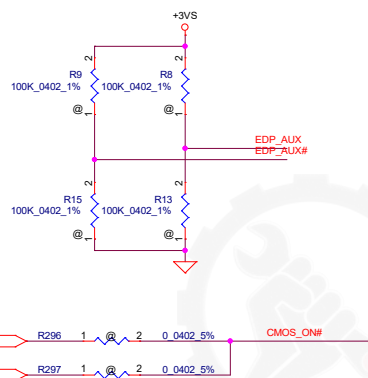
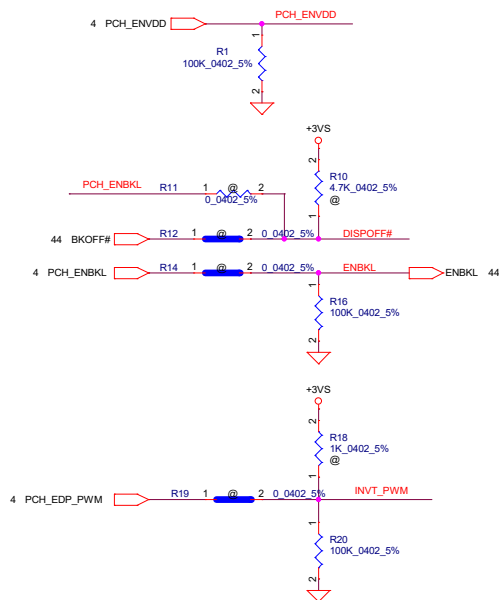
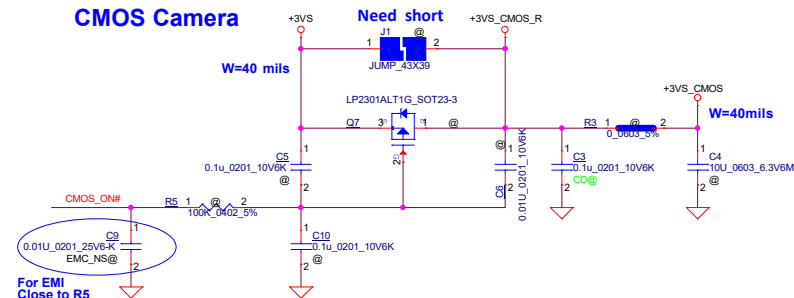
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RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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Date:		Thursday, May 04, 2017				Sheet		32 of 60	

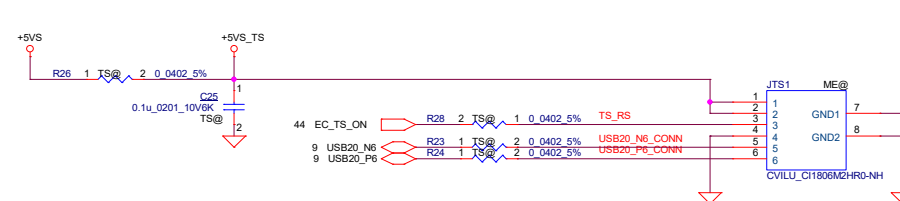
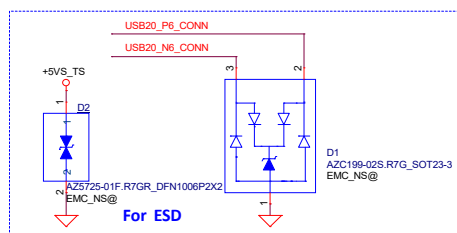
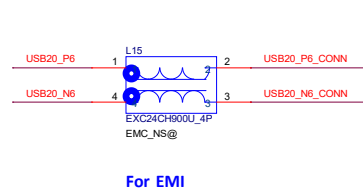
LCD POWER CIRCUIT



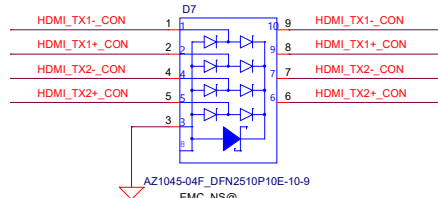
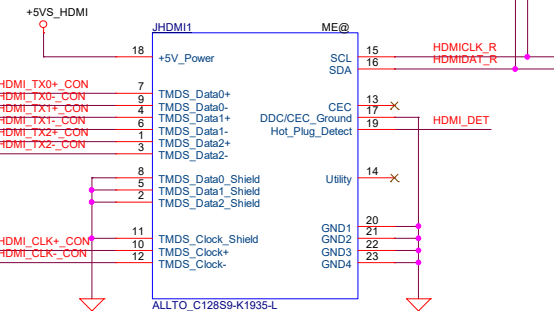
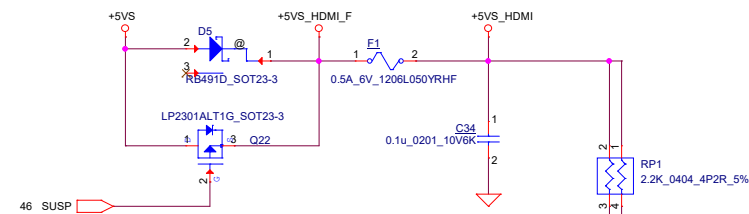
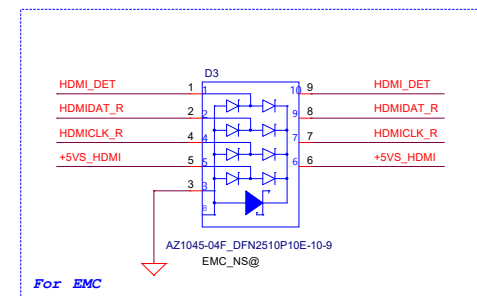
CMOS Camera



Touch Screen




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Size	Document Number	Rev
Custom	EG523	0.
Date:	Thursday, May 04, 2017	Sheet 34 of 60


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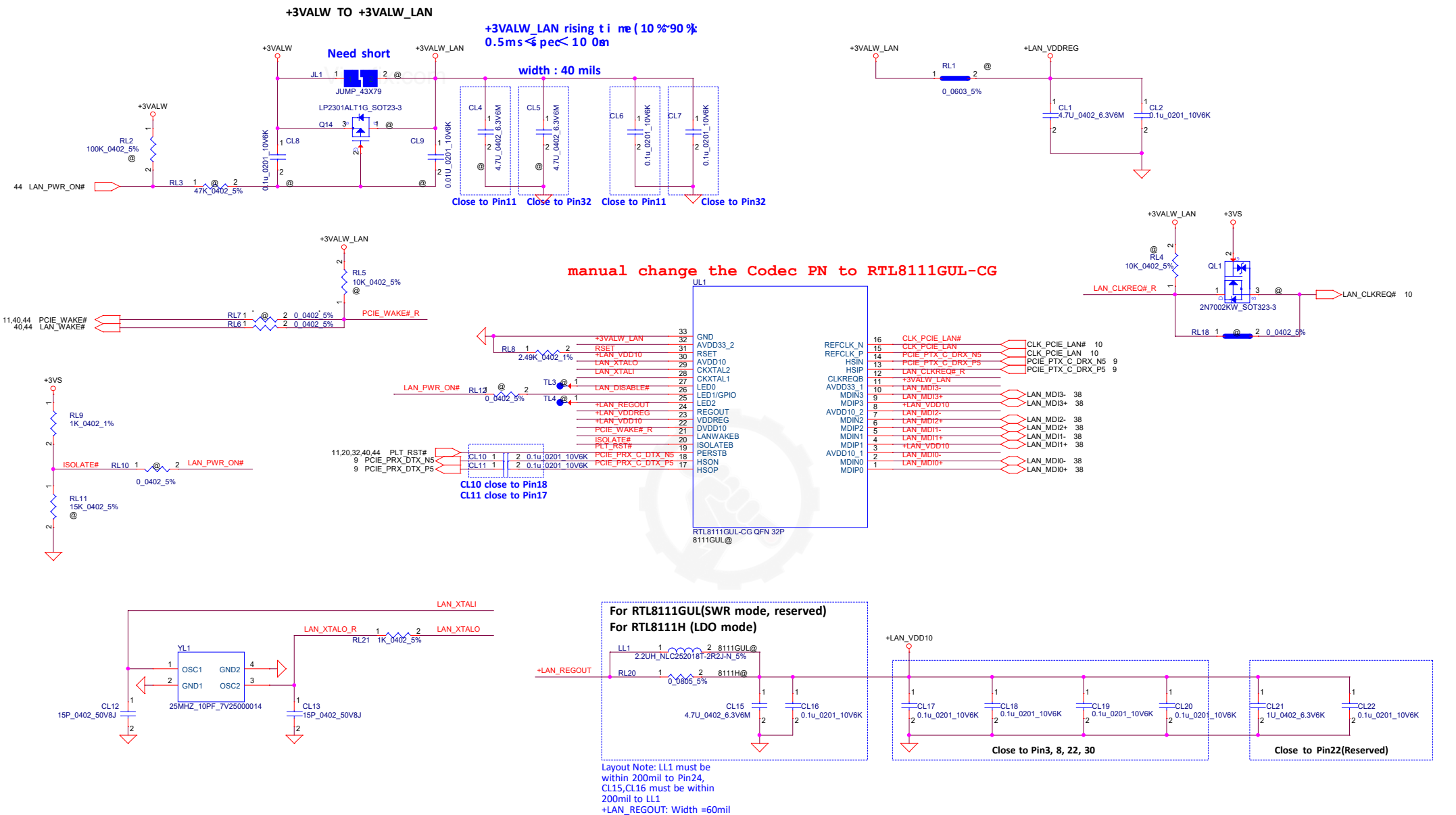


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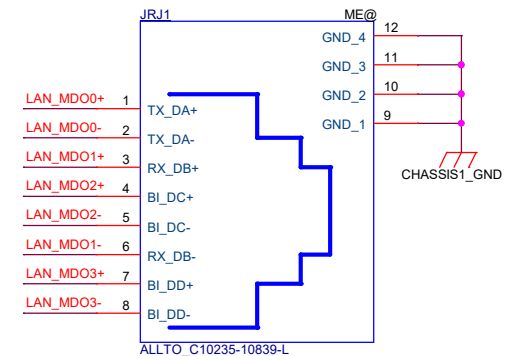
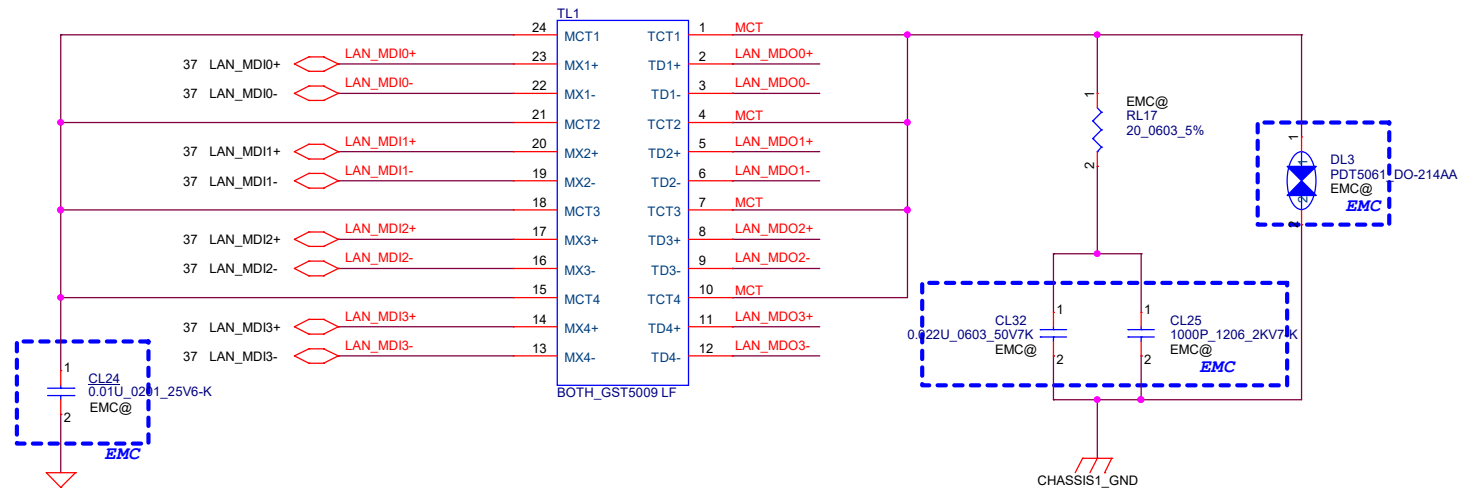
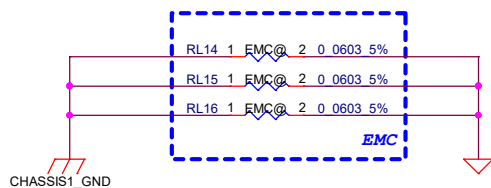
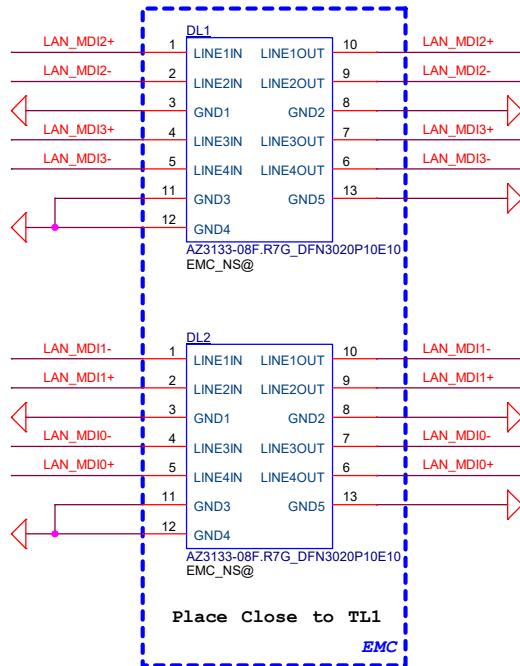
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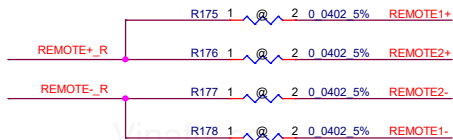
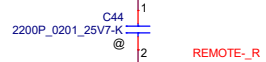
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8/16 Update RJ45 P/N DC021608091 wei

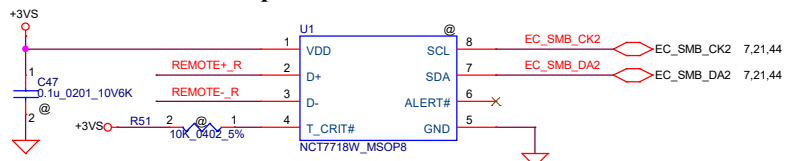
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				Date: Thursday, May 04, 2017	Sheet 38 of 60
				Rev 0.1	

Close to U1

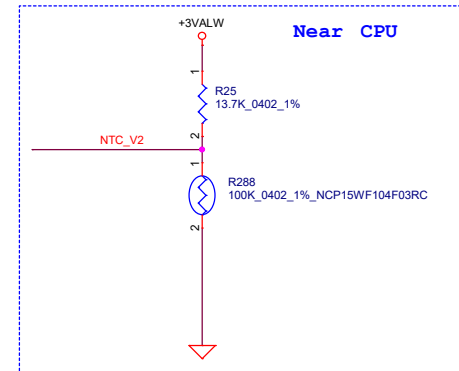
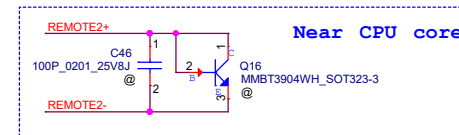
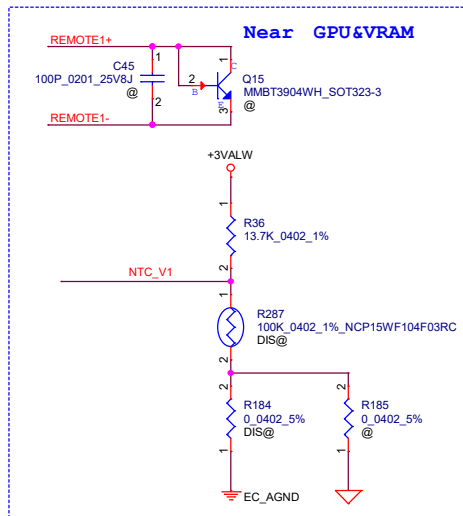


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Trace length:<8"

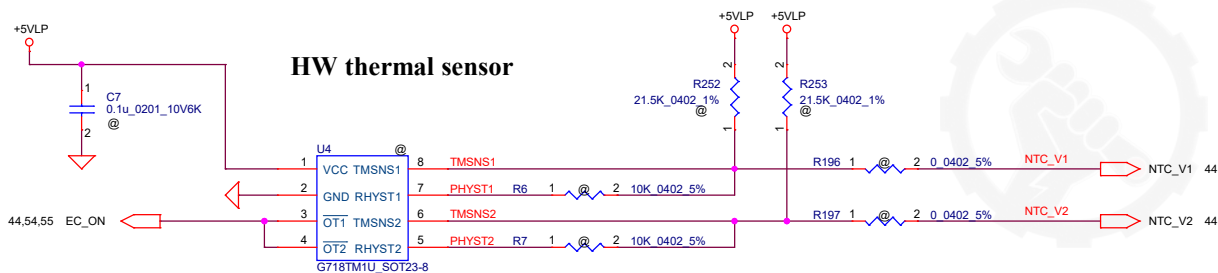
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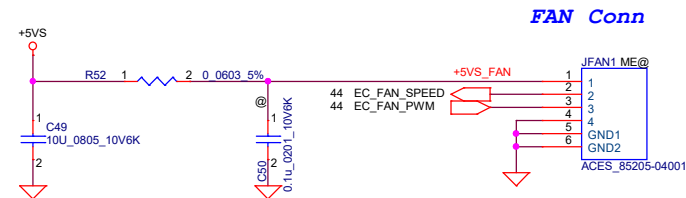
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HW thermal sensor

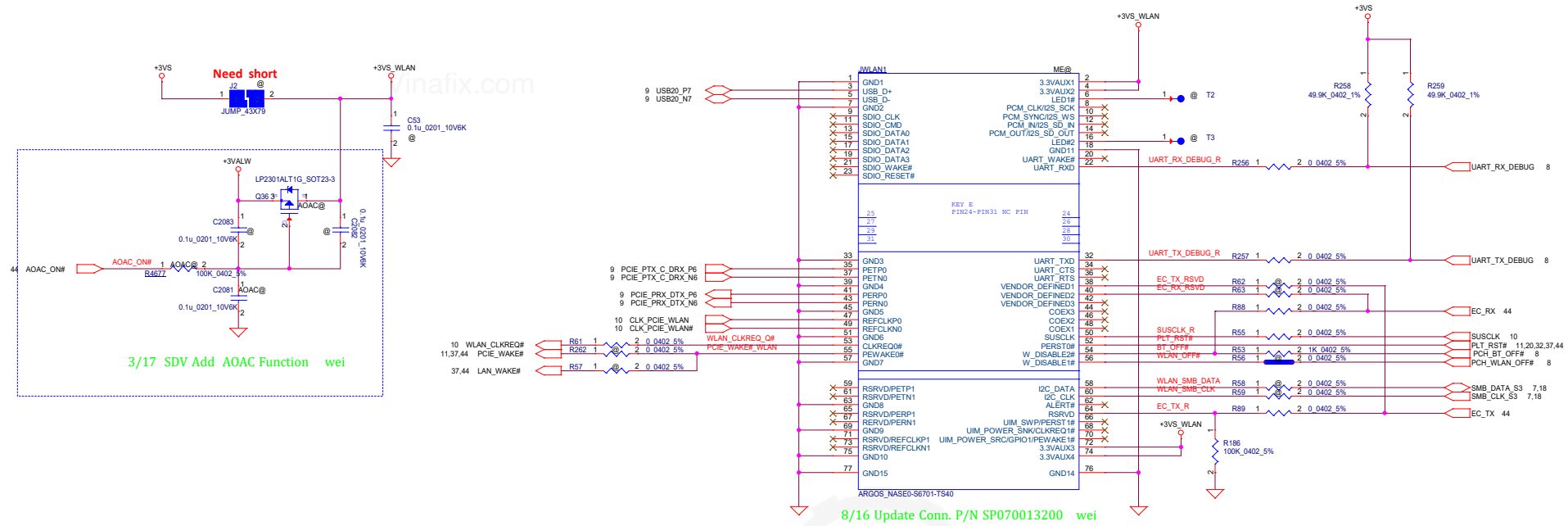


over temperature threshold:
 $RSET = 3 * RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
56+/-30C

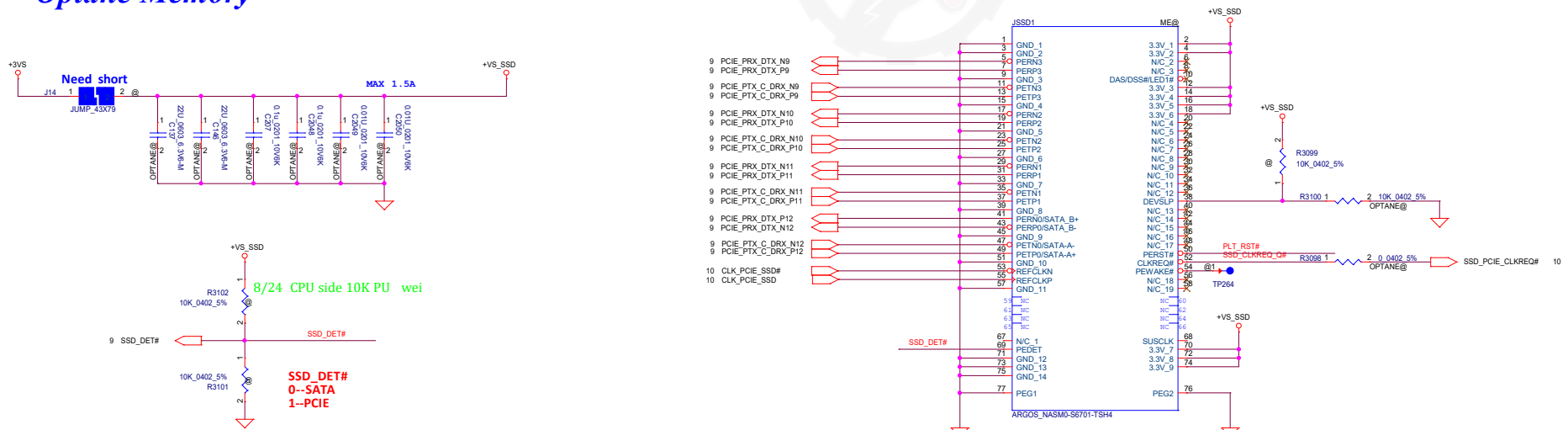



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				Date:	Thursday, May 04, 2017	Sheet 39 of 60

Mini-Express Card(WLAN/WiMAX)

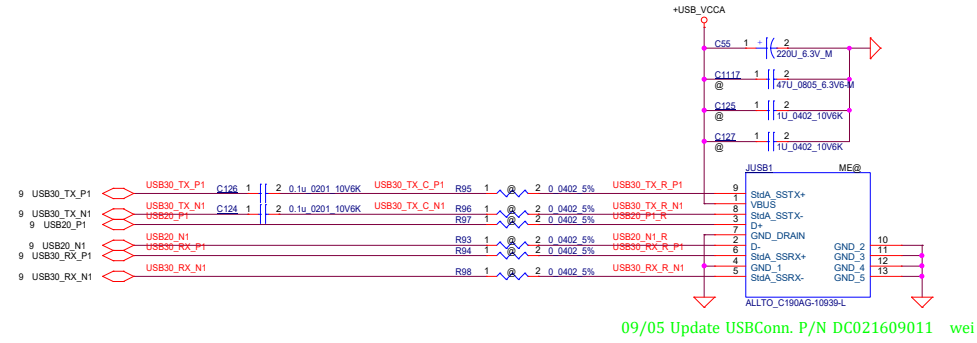
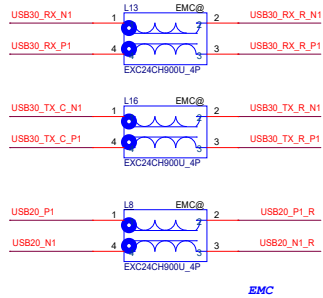
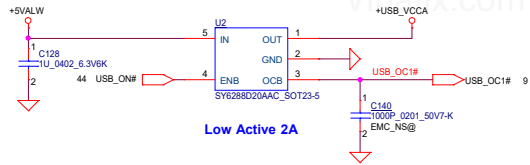


Optane Memory

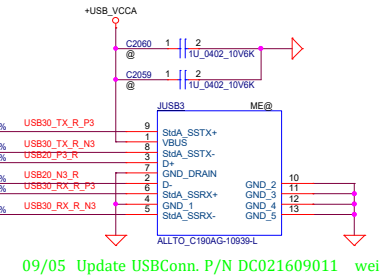
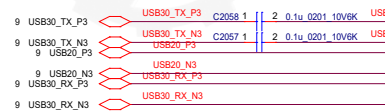
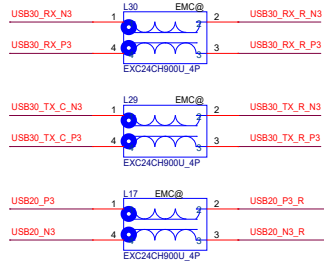
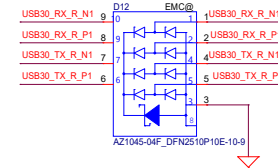
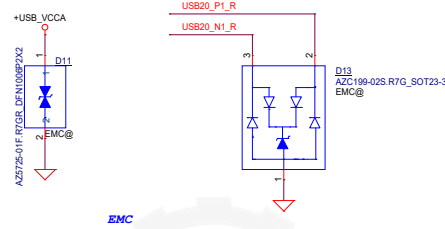


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Issued Date		2016/12/14		Deciphered Date		2017/12/13				NGFF WLAN&SSD	
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		EG523									
Date:		Thursday, May 04, 2017				Sheet		40 of 60			

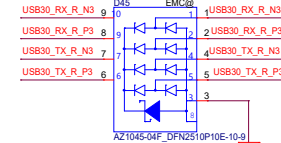
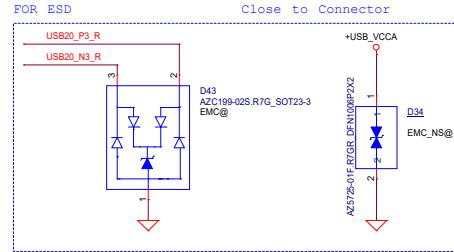
LEFT SIDE USB3.0 PORT x2



09/05 Update USBConn. P/N DC021609011 wei



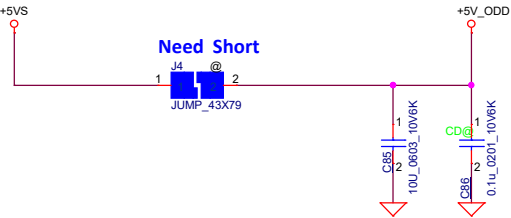
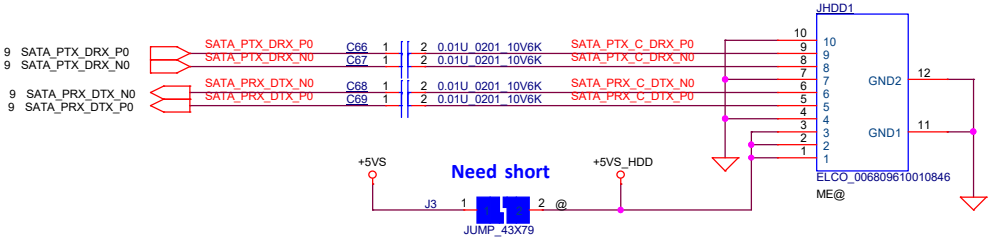
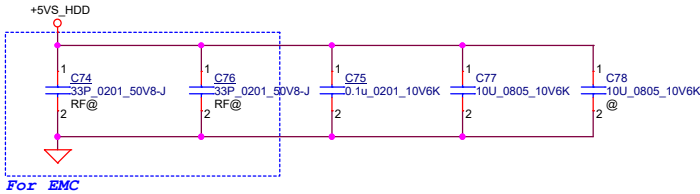
09/05 Update USBConn. P/N DC021609011 wei



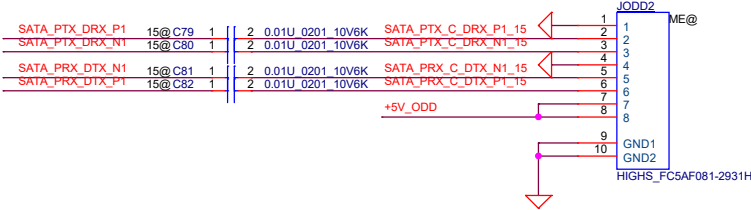
Security Classification	LC Future Center Secret Data		Title	USB3.0 PORT (LEFT)	
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Size	Document Number
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			Date:	Thursday, May 04, 2017	Sheet 41 of 80

SATA HDD Conn.


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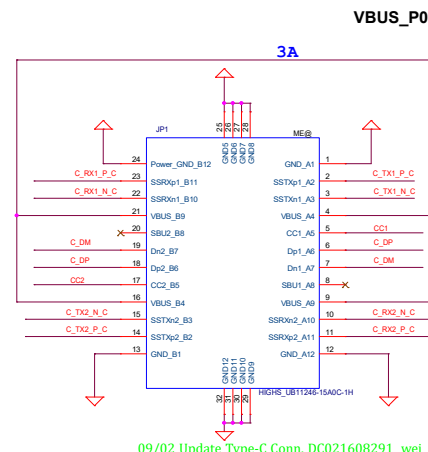
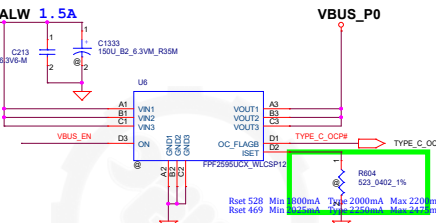
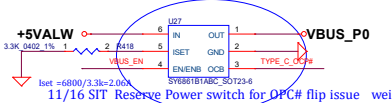
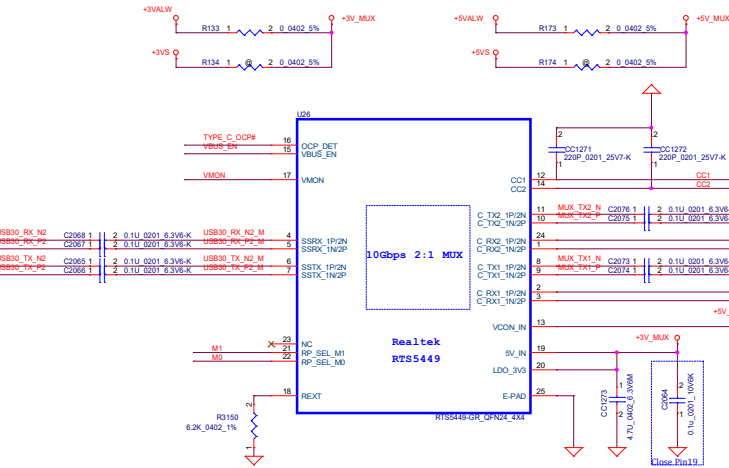
FOR 14" SATA ODD Conn.



8/16 Update Conn. P/N SP01001YV00 wei

Security Classification		LC Future Center Secret Data				Title									
Issued Date		2016/12/14		Deciphered Date		2017/12/13				HDD/ODD CONN					
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Date:		Thursday, May 04, 2017		Sheet 42		of 60									

9 USB30_TX_N2
9 USB30_TX_P2
9 USB30_RX_N2
9 USB30_RX_P2



Rp configuration

Rp:1.5A (now)

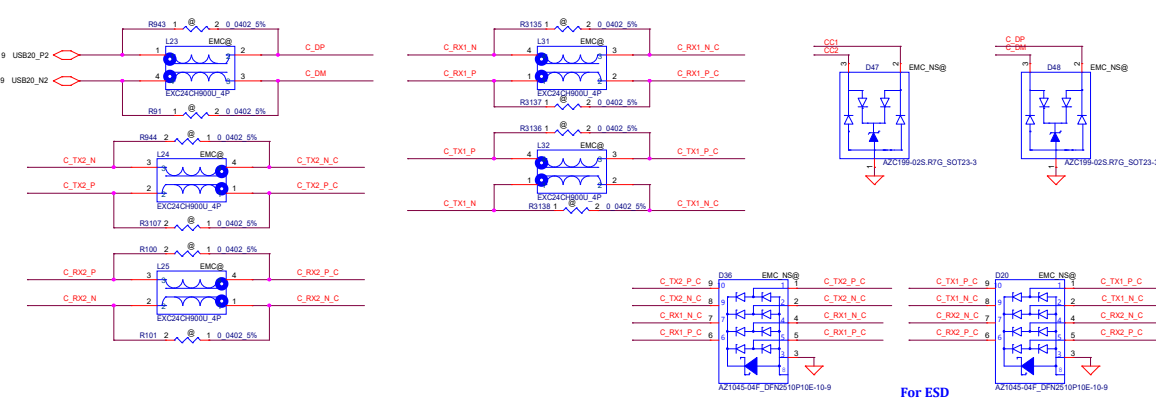
Rp	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

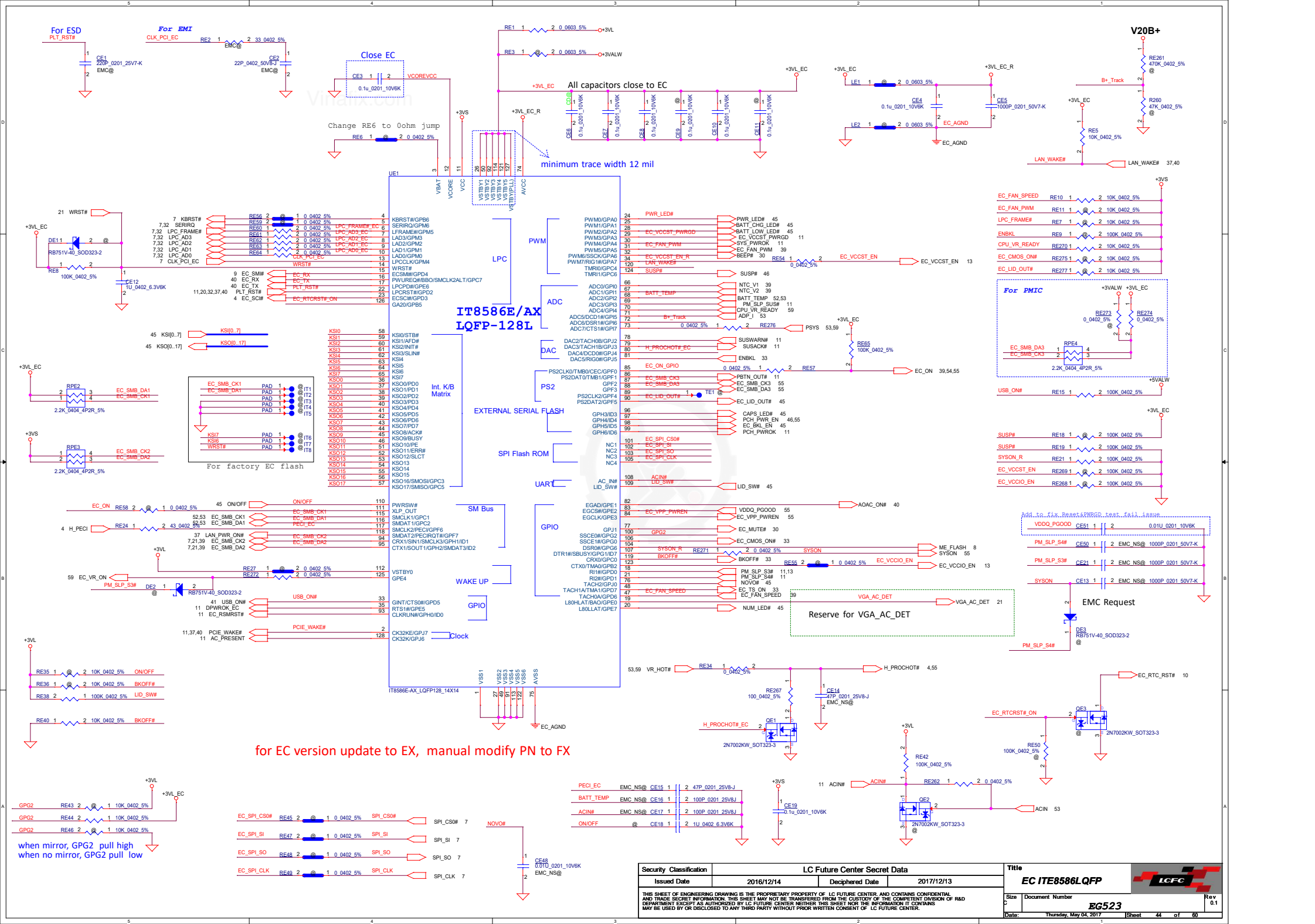
For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

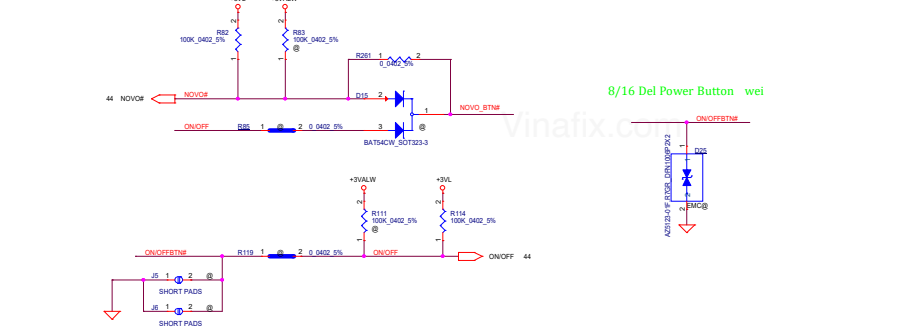
For C_VBUS power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

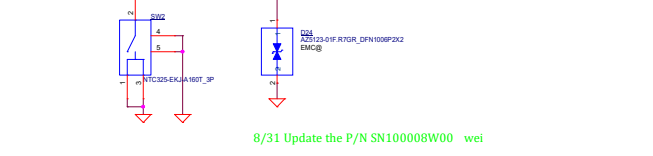




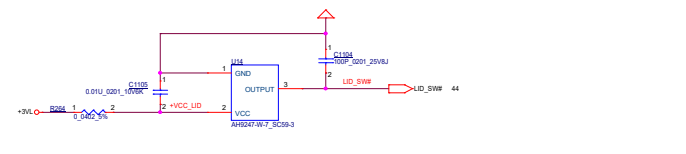
ON/OFF switch



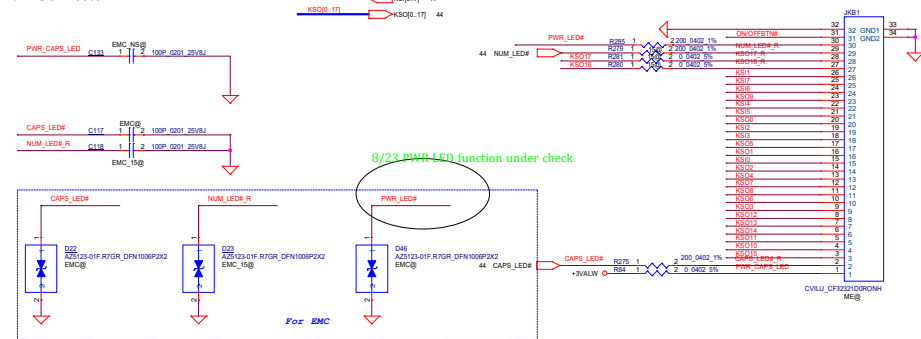
Novo button



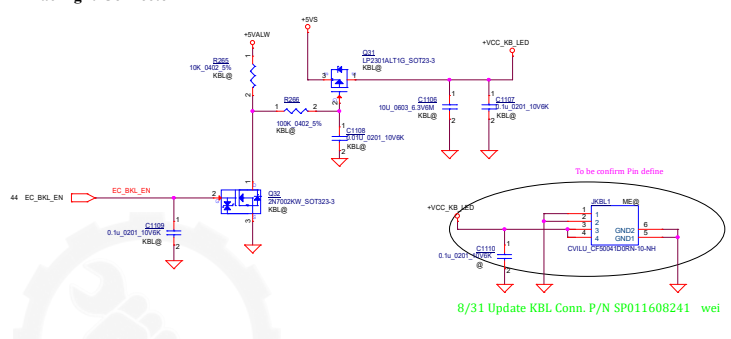
LID switch



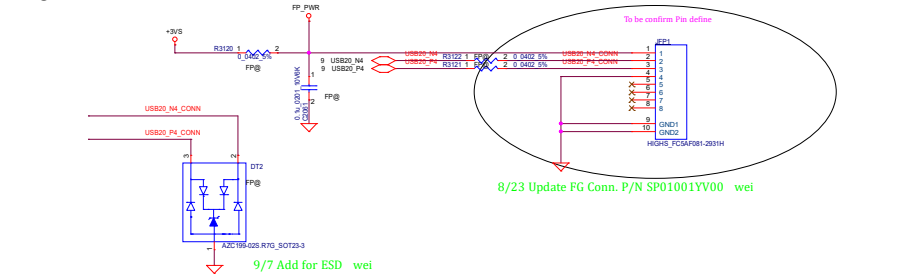
K/B Connector



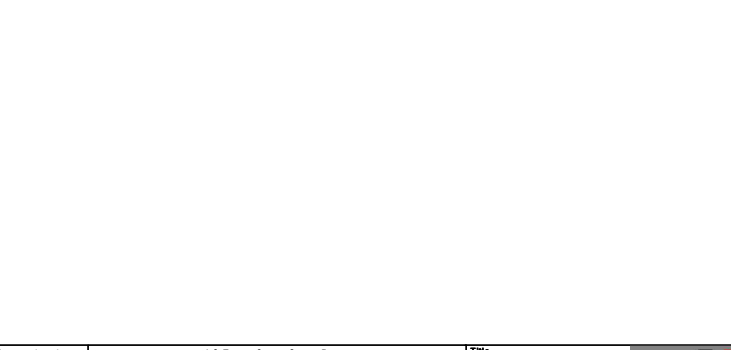
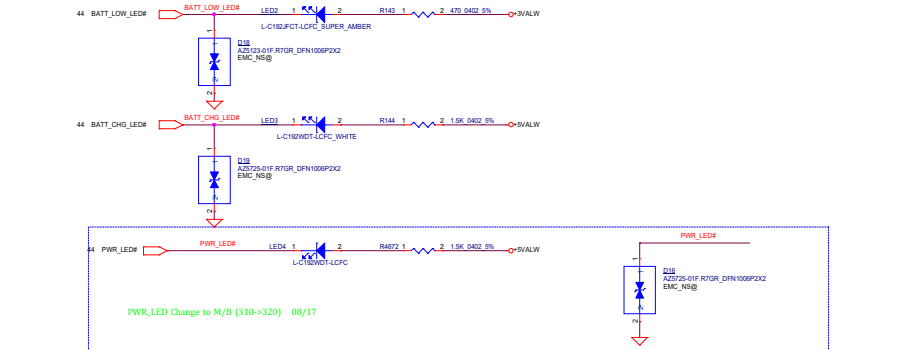
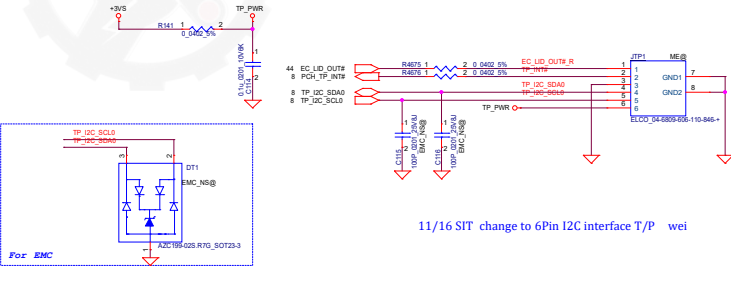
KB Backlight Connector



Finger Print Connector



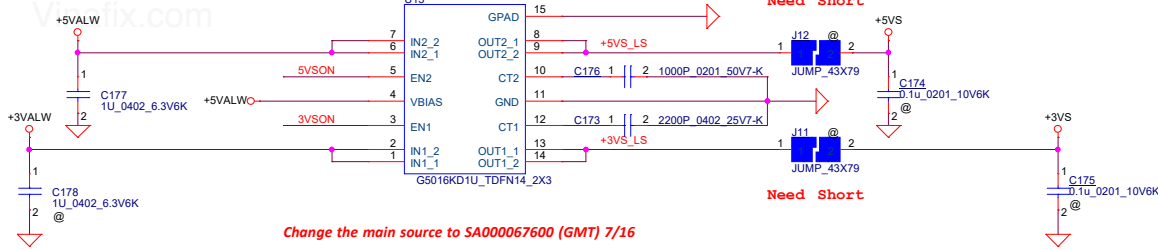
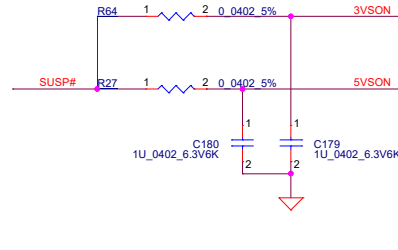
TP/B Connector



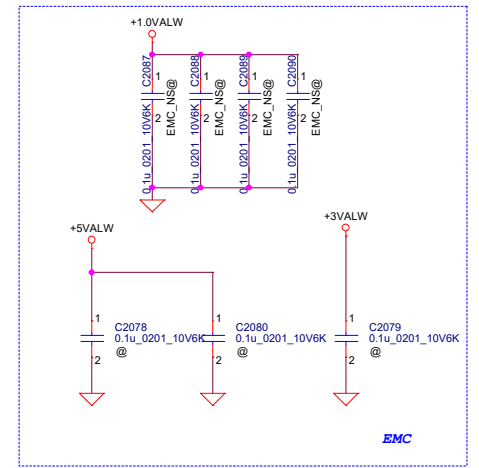
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

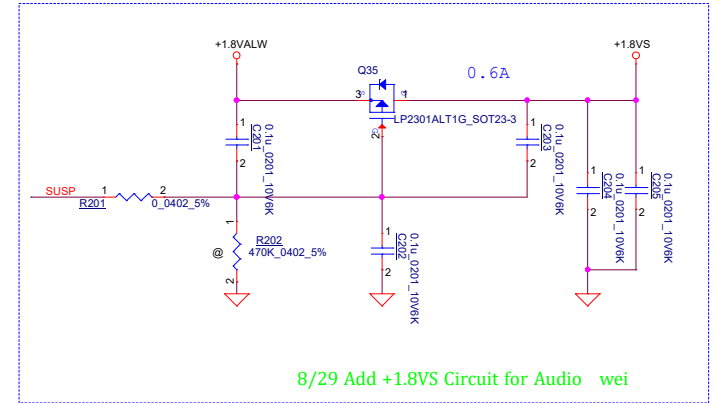
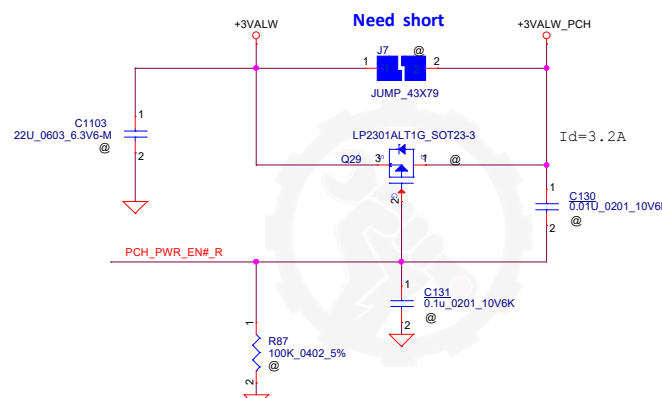
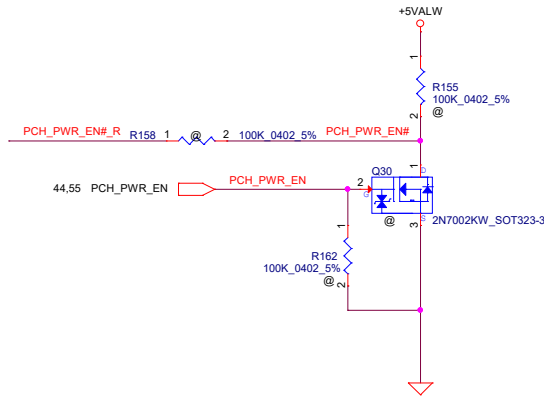
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



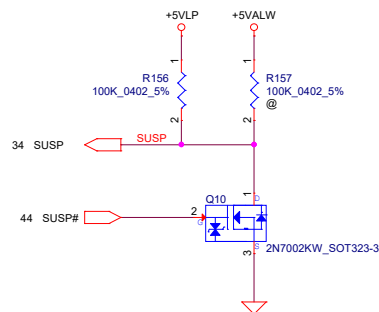
Change the main source to SA000067600 (GMT) 7/16



EMC



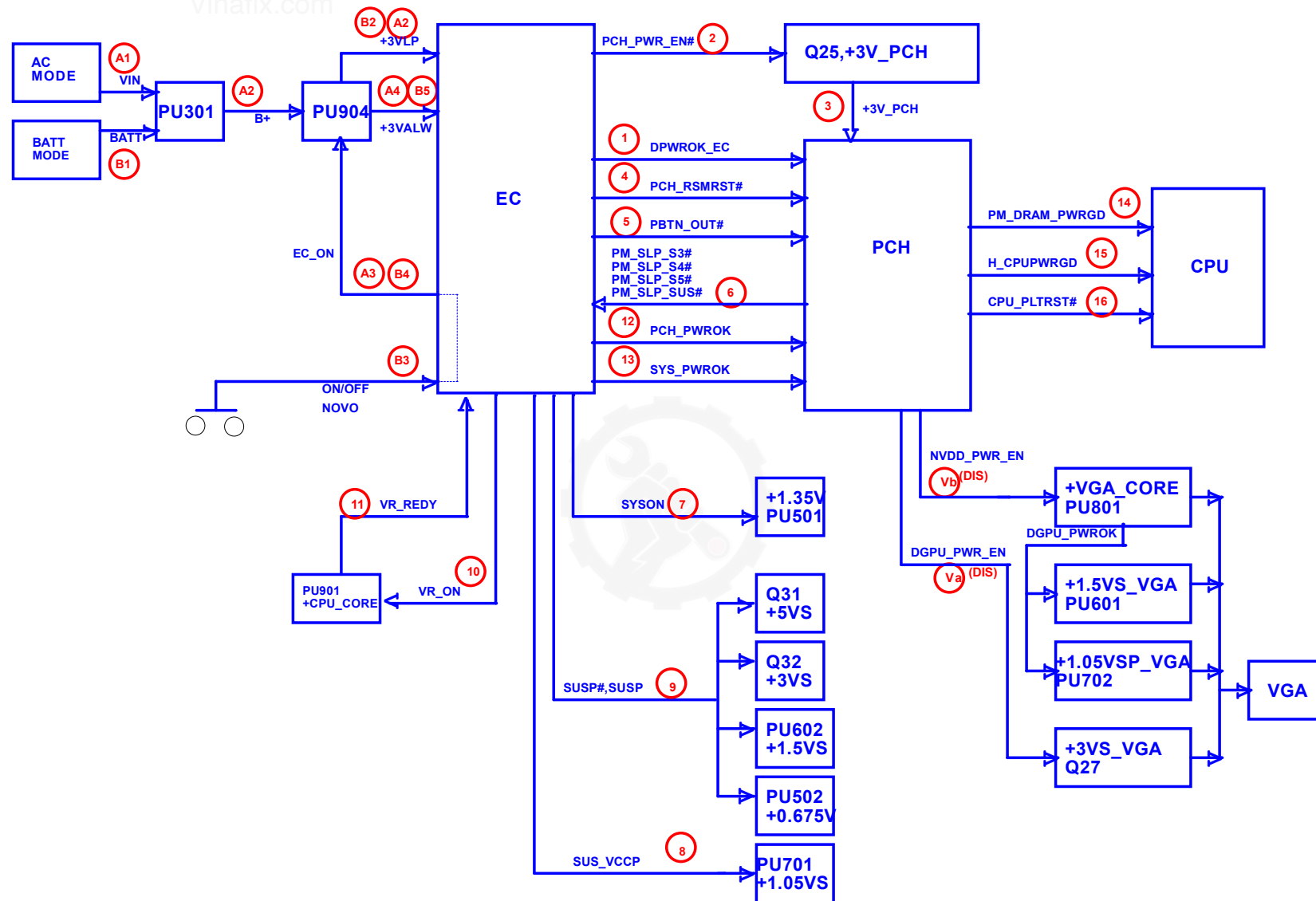
8/29 Add +1.8VS Circuit for Audio wei



For DisCharge



08/29: Need double check enable signal and the resistance



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Title		Rev	
Power sequence block		0.1	
Size	Document Number	BG523	
Custom			
Date	Thursday, May 04, 2017	Sheet	47 of 60

ZZZ1

NMB453@

NM-B453

DA60013Q00

HA

PCB_MB

UC1

I7@

KBL-R CPU

SA00008J600

UC1

I5@

KBL-R CPU

SA00008J500

CPU
CPU

UL1

8111H@

RTL8111H-CG

SA000074W00

LAN Chip

UL1

PX@

R17M-M1-70 GPU

SA000086K00

GPU

ZZZ2

DRAM_S4G@

Samsung

X7643712009

ZZZ2

DRAM_M4G@

Micron

X7643712008

ZZZ2

DRAM_H4G@

Hynix

X7643712007

2400MT/s DRAM X76 BOM

ZZZ4

S4GX4@

Samsung

X7643912002

ZZZ4

H4GX4@

Hynix

X7643912001

ZZZ4

M4GX4@

Micron

X7643912003

ZZZ4

S8GX4@

Samsung

X7643A12002

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ZZZ4

M8GX4@

Micron

X7643A12003

VRAM X76 BOM

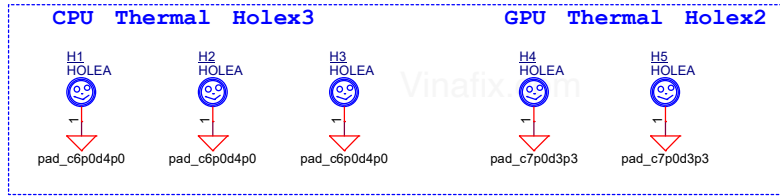
ZZZ3

HDMI@

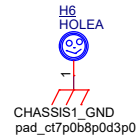
HDMI PN

RO00000040J

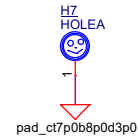
HDMI Royalty



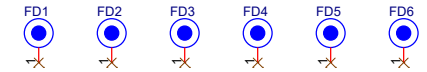
Close to RJ45



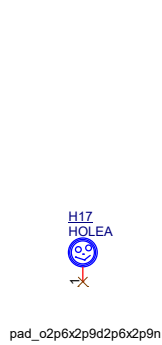
Close to Audio jack



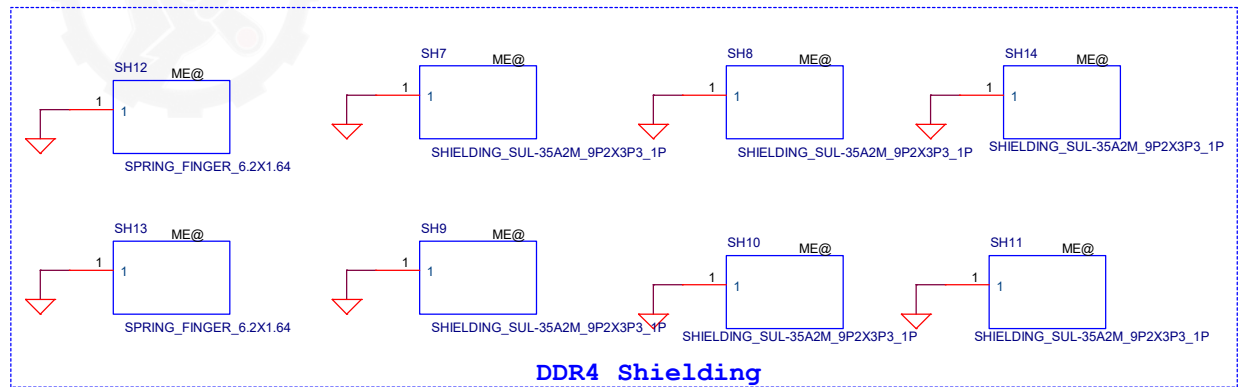
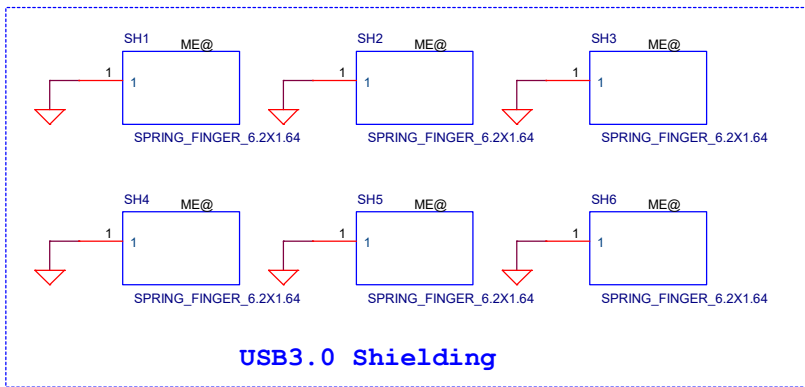
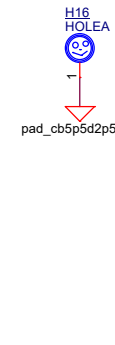
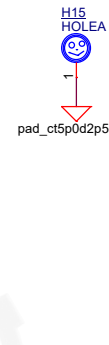
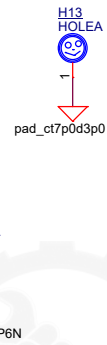
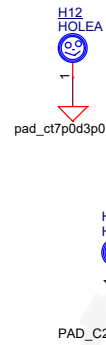
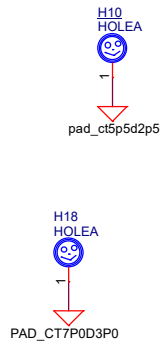
PCB Federal Mark PAD




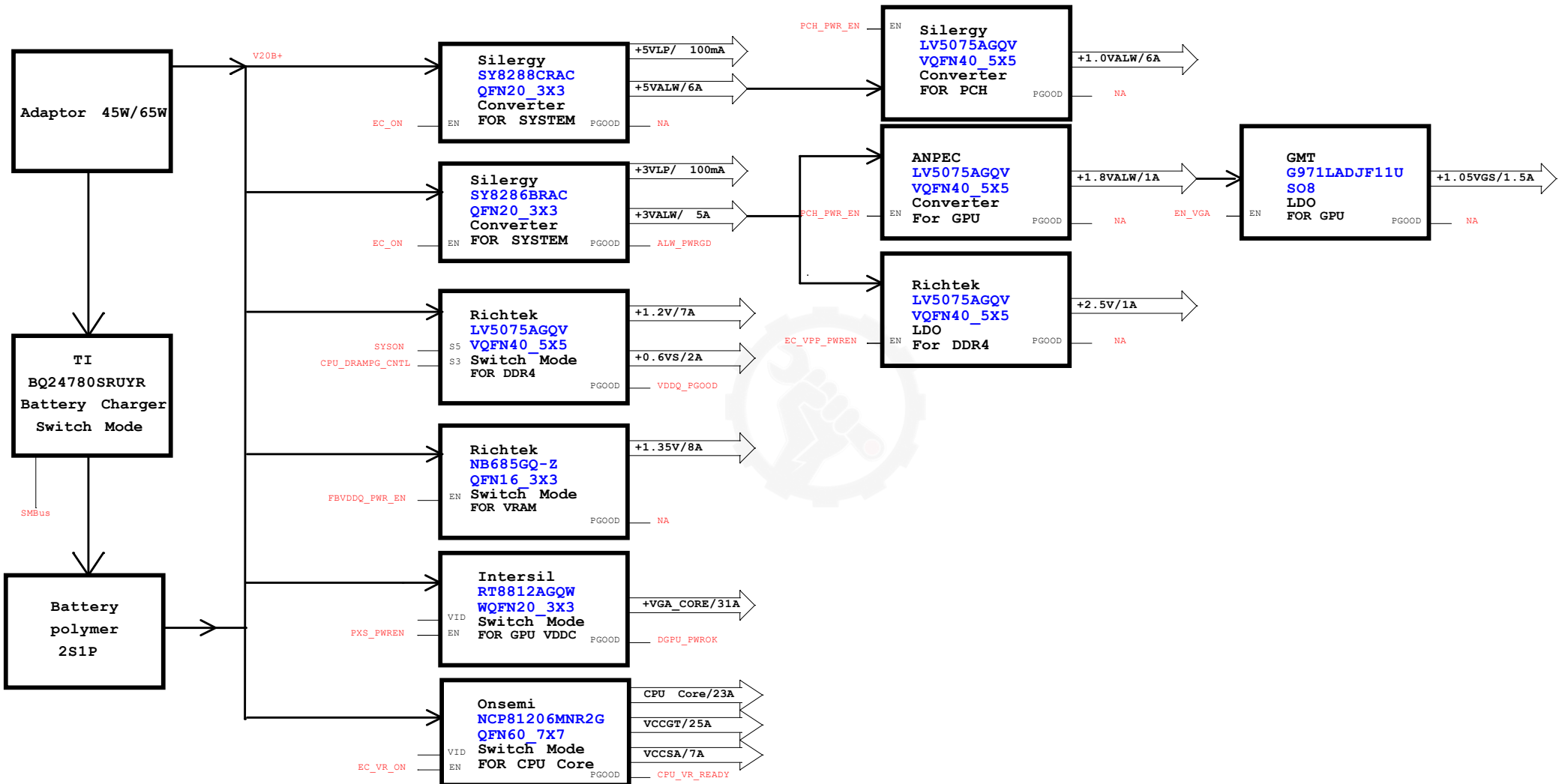
DC-IN x2

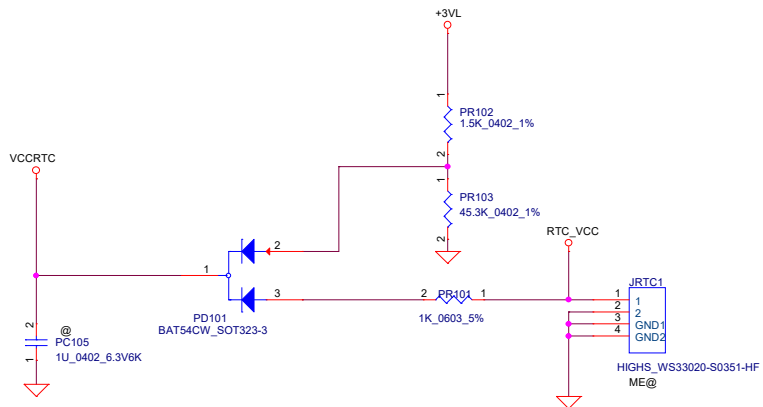
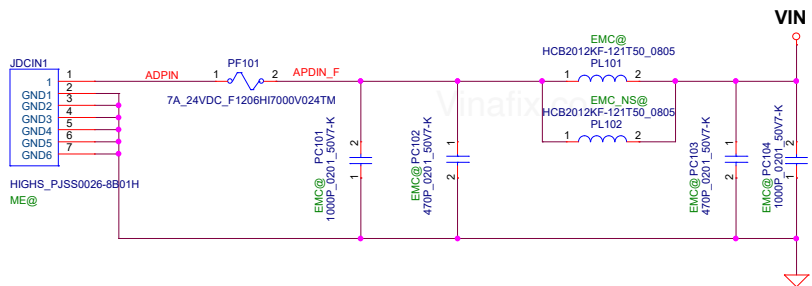


WLAN Standoff



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				B	EG523	0.1
				Date:	Thursday, May 04, 2017	Sheet 49 of 60





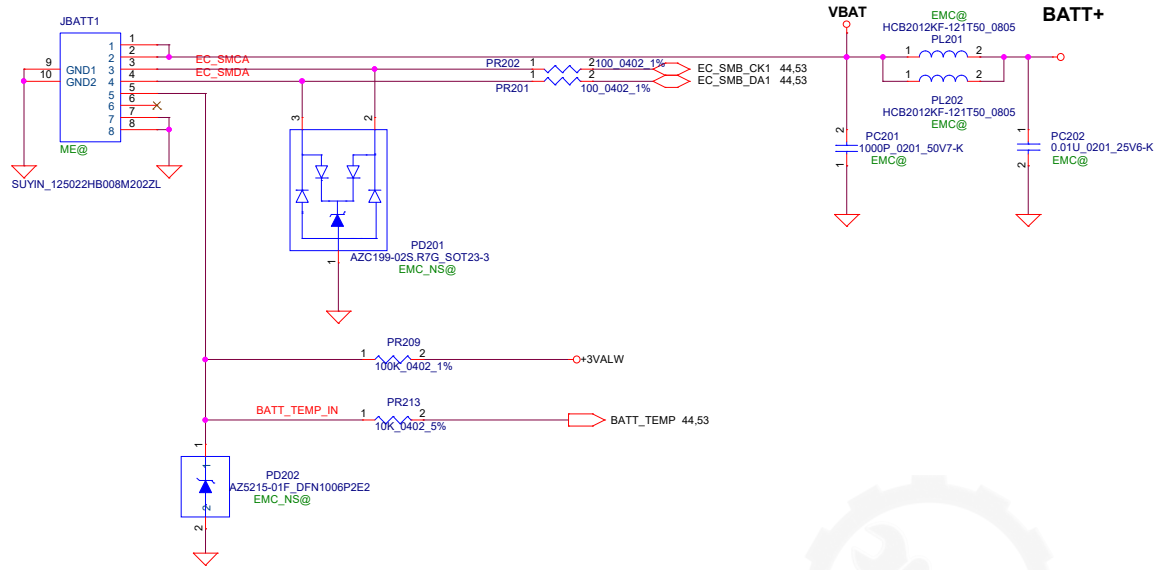
RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR-DCIN / RTC charger	
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				Date:	Thursday, May 04, 2017
				Sheet	51 of 60
				Rev	0.1

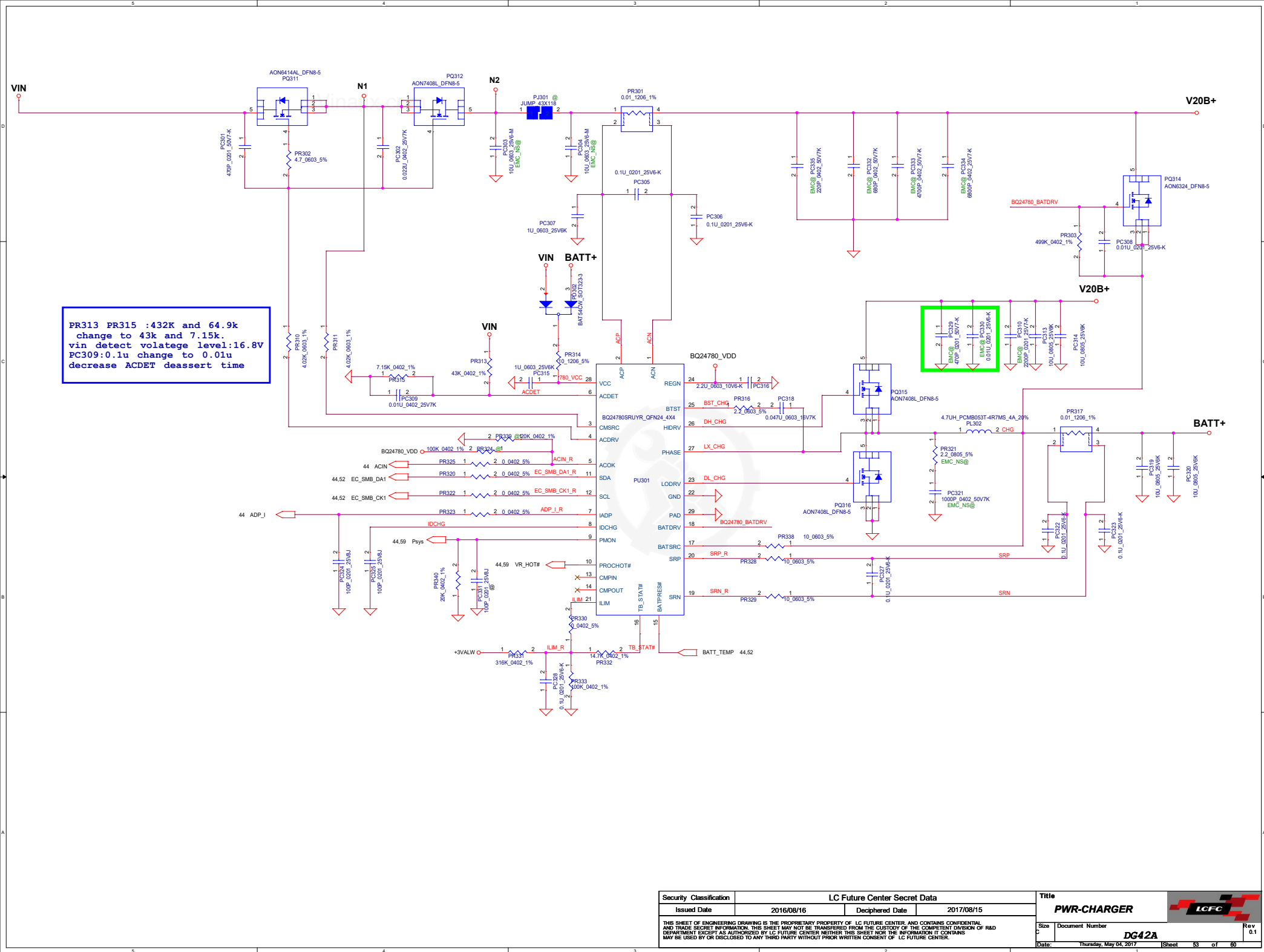
Vinafix.com

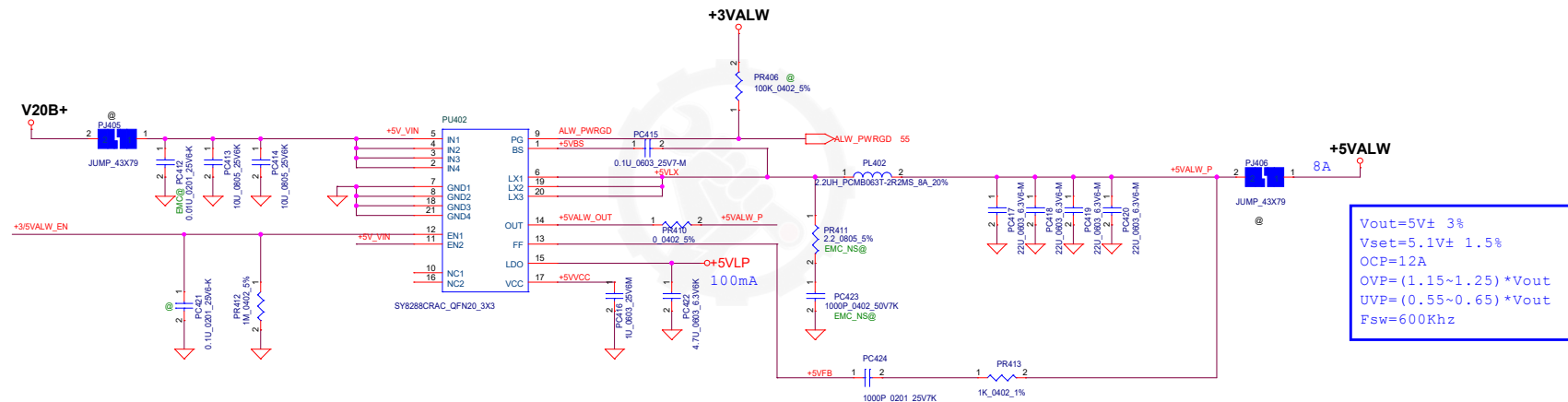
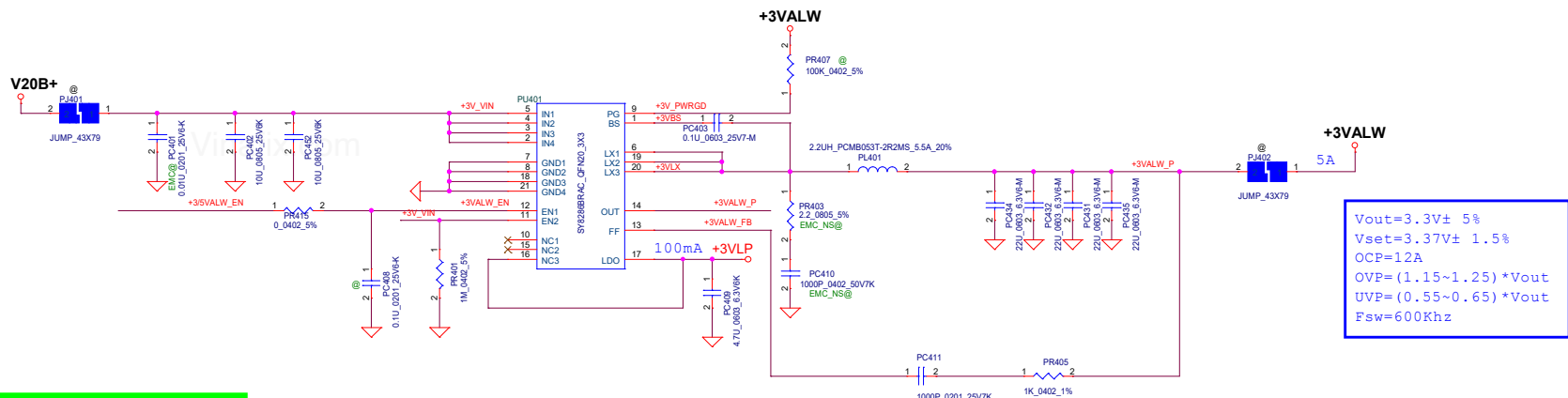
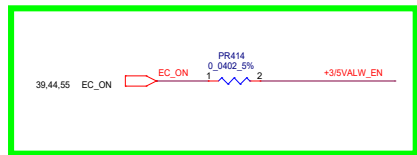


2S1P polymer battery
voltage level: +6V ~
8.4 V




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR-BATTERY CONN/OTF ICFC	
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				Date: Thursday, May 04, 2017	Rev 0.1
				Sheet 52 of 60	



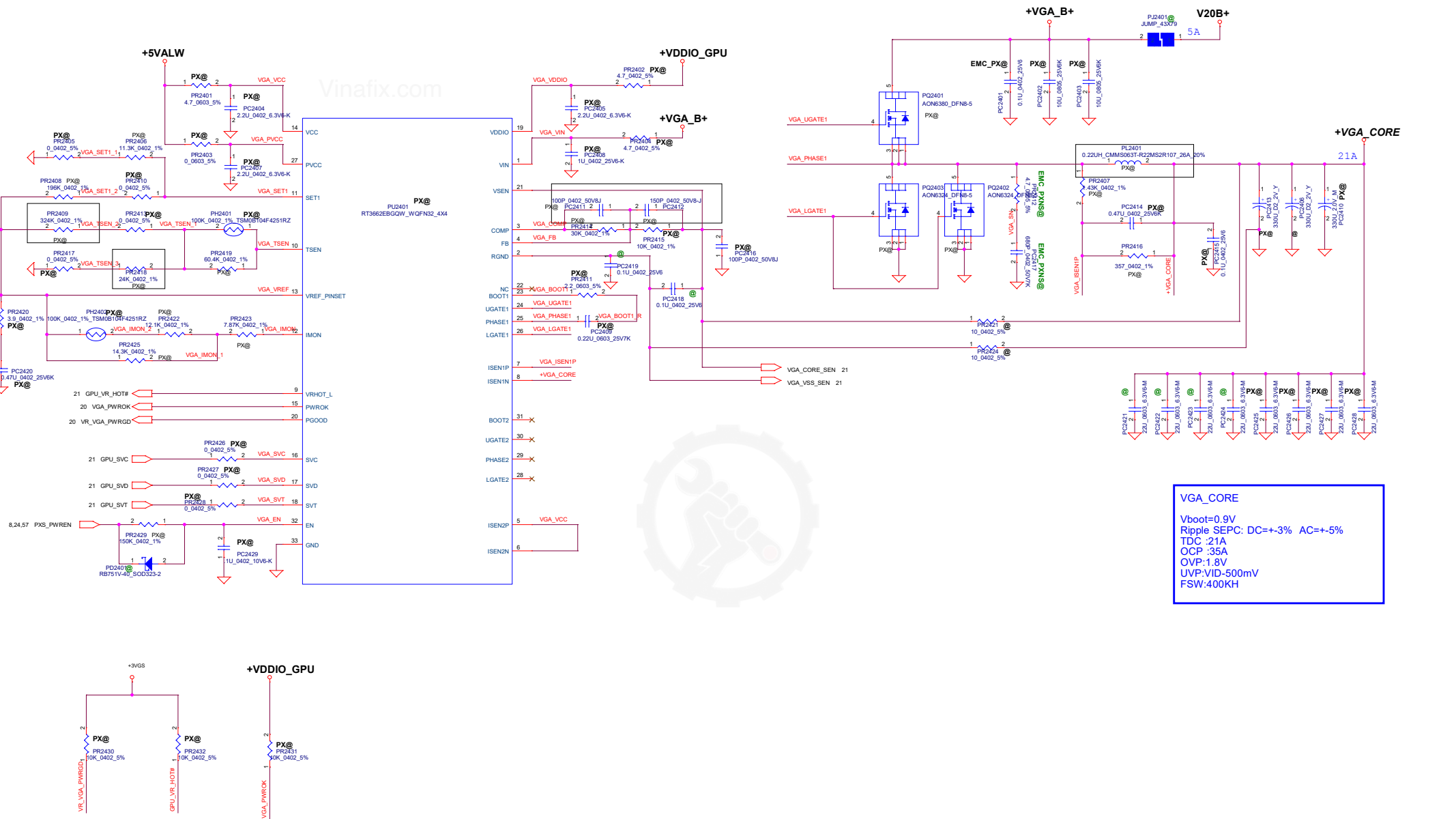


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Issued Date		2016/08/16		Deciphered Date			2017/08/15		PWR				
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						DG42A							
3						2						1	
						Date: Thursday, May 04, 2017						Sheet 56 of 60	

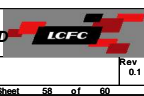
Vinafix.com



VGA_CORE

Vboot=0.9V
 Ripple SEPC: DC=+3% AC=+5%
 TDC :21A
 OCP :35A
 OVP:1.8V
 UVP:VID-500mV
 FSW:400KH

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR-VGA_CORE_AMD	
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				Sheet	58 of 60
				Date	Thursday, May 04, 2017



Rev 0.1

SVID Specification	
Config	
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
28.7K	550K	550K

RVboot	Core	GT	SA
35.7K	0V	0V	1.05V

