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CML-H MB Schematic Document

LA-J561P

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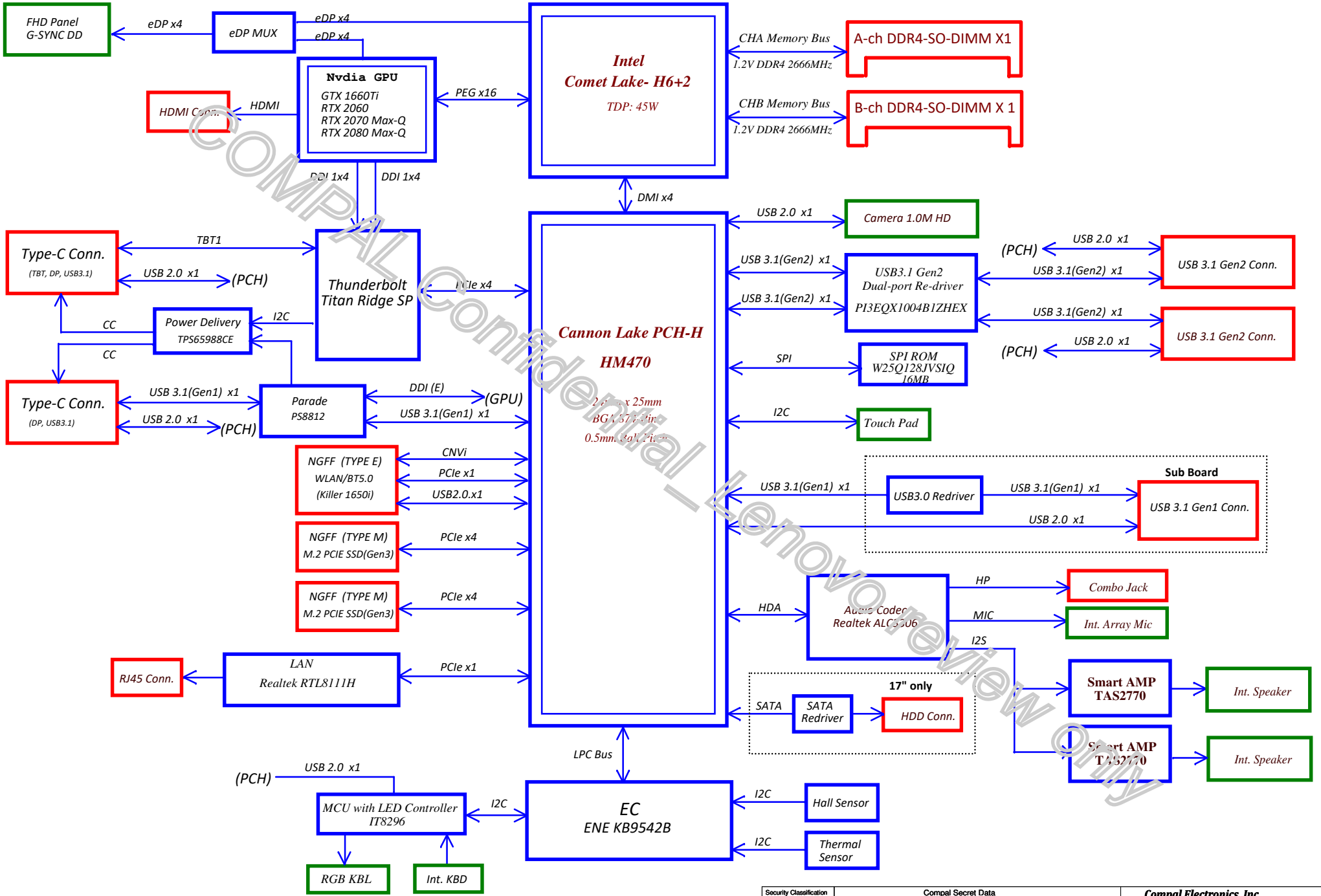
Comet Lake H Block Diagram



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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.84[illegible] V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.0[illegible] V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.2[illegible] V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.3[illegible]	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.40[illegible]	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.53[illegible]	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	NA		NA
DDI2	NA		NA
DDI3	NA		NA
eDP	Embedded Display		EDP_HPD

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA3
PCH_SML0CLK PCH_SML0DATA	+3VS	NA			
PCH_SML1CLK PCH_SML1DATA	+3VS	EC	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1 EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		TBT	Reserved	TBC	TBC
SMBUS Port2 EC_SMB_CK2 EC_SMB_DA2	+3VS				
		PCH	TBC		
		GPU	0x9E/0x9F	TBC	TBC
		Type-C PS8812			
		THERMAL	0x4D	0x9A	0x9B
		USB3.1 re-driver	0x29	0x52	0x53
SMBUS Port4 EC_SMB_CK4 EC_SMB_DA4	+3VS	KB/LED Controller	0x1F	0x3E	0X3F
			TBC		

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS	EC KB9542	TBC	TBC	TBC
I2C_1_SCL I2C_1_SDA	+3VS	Touch Pad	0x15	TBC	TBC

BOM Structure Table (1/2)

Function	Stuff	Note
Unit SKU	UMA@	
	DIS@	
Project SKU	15@	
	17@	
CFL-H SKU	CPU1@	i5-9400H-R1
	CPU2@	i9-9880H-R1
	CPU3@	i9-9980HK-R1
DGPU SKU	N18G0@	
	N18G1@	
	N18G2@	
	N18G3@	
PCH SKU HM370	PCH1@	HM370 QNYF
N18 x SKU	GPU1@	1660Ti-G0-R1
	GPU2@	2060-G1-R1
	GPU3@	2070-G2-R1
	GPU4@	2080-G3-R1
VRAM 6G	M6G@	X7685138L01
	S6G@	X7685138L02
VRAM 8G	M8G@	X7685138L03
	S8G@	X7685138L04
Intel RTD3	RTD3@	
	NORTD3@	
eSPI I/F	ESPI@	
	LPC@	
Debug	CMC@	
Panel SKU	GSYNC@	
	NOGSYNC@	
Intel TBT TR	TBT@	
Intel CNVi	CNVI@	
LAN Mode	8111H_SW@	
	8111H_LDO@	
FIN FPC	FIN1@	IT8296 Control
	FIN2@	
OVRM	ON@	NCP45491
	UPI@	US5650PQKI
ME Connector	ME@	
EMI Components	EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@

HSIO Port Table(PCH) HM470

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 1		Left Back
1	USB3.1_2	2			USB3.1 PORT 2		Right Back
2	USB3.1_3	3			USB3.1 PORT 3		Right Fornt
3	USB3.1_4	4			USB3.1 PORT 4		Left Fornt
4	USB3.0_5	5					
5	USB3.0_6	6					
6	USB3.0_7	7					
7	USB3.0_8	8					
8							
9							
10							
11							
12							
13							
14	PCIE_9 / GbE		9				
15	PCIE_10		10		NGFF SSD2	CLK5 & & CLKREQ#5	
16	PCIE_11 / SATA_0A		11	0			
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	LAN	CLK2 & & CLKREQ#2	
20	PCIE_15		15	2	WLAN+BT NGFF	CLK3 & & CLKREQ#3	
21	PCIE_16		16	3			
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	Thunderbolt Intel Titan Ridge SP	CLK0 & & CLKREQ#0	
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21				
27	PCIE_22		22		NGFF SSD1	CLK1 & & CLKREQ#1	
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 PORT 2
2	USB3.1 PORT 1
3	USB3.1 PORT 3
4	LED Controller IT8296
5	TBT TYPE-C
6	Camera
7	DP TYPE-C
8	
9	
10	
11	
12	
13	
14	W[illegible] NGFF

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.0VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	[illegible] +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	[illegible]VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	[illegible] power rail	ON	ON	ON	ON*	OFF
+1.8VS	Syst[illegible].8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for deeper power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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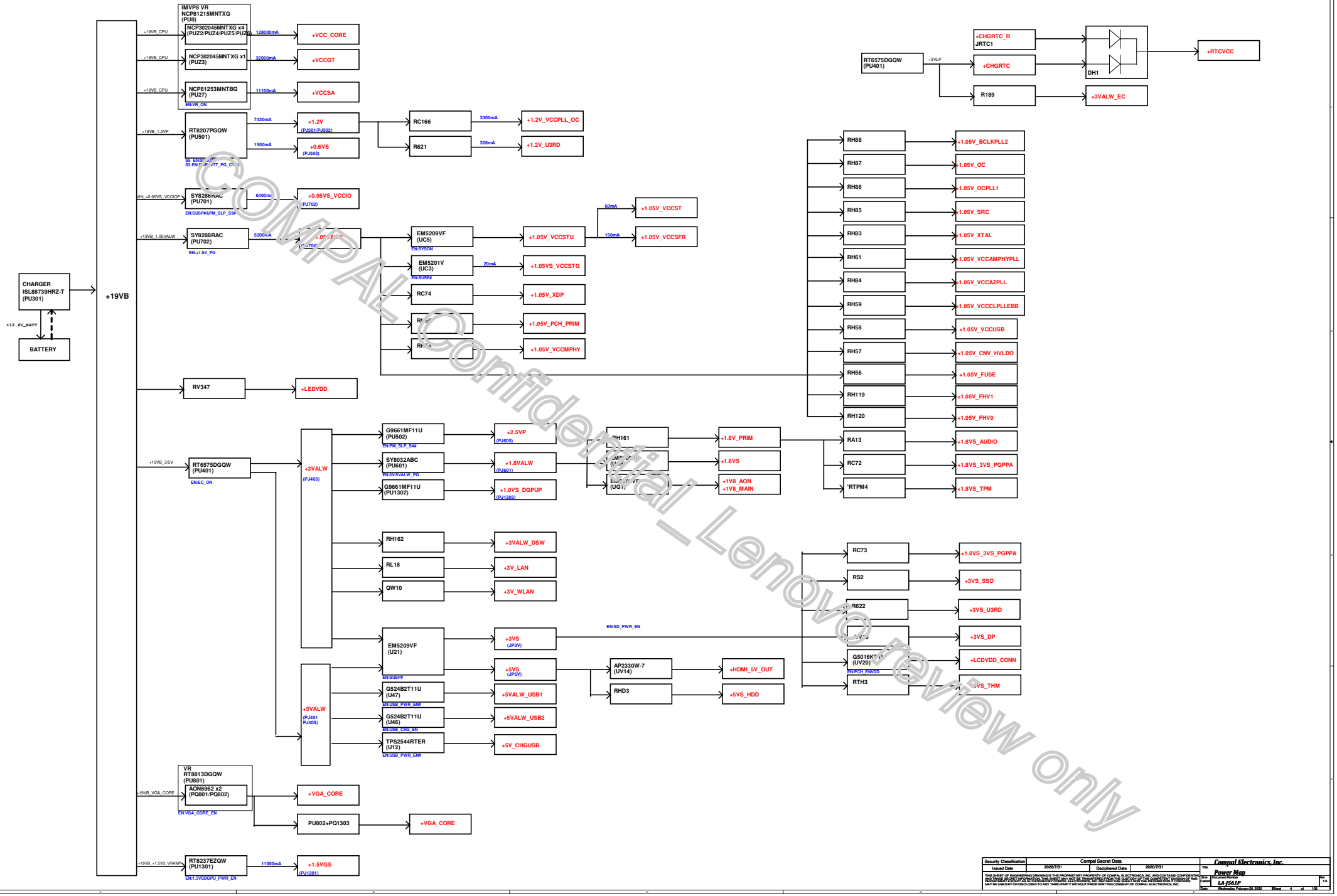

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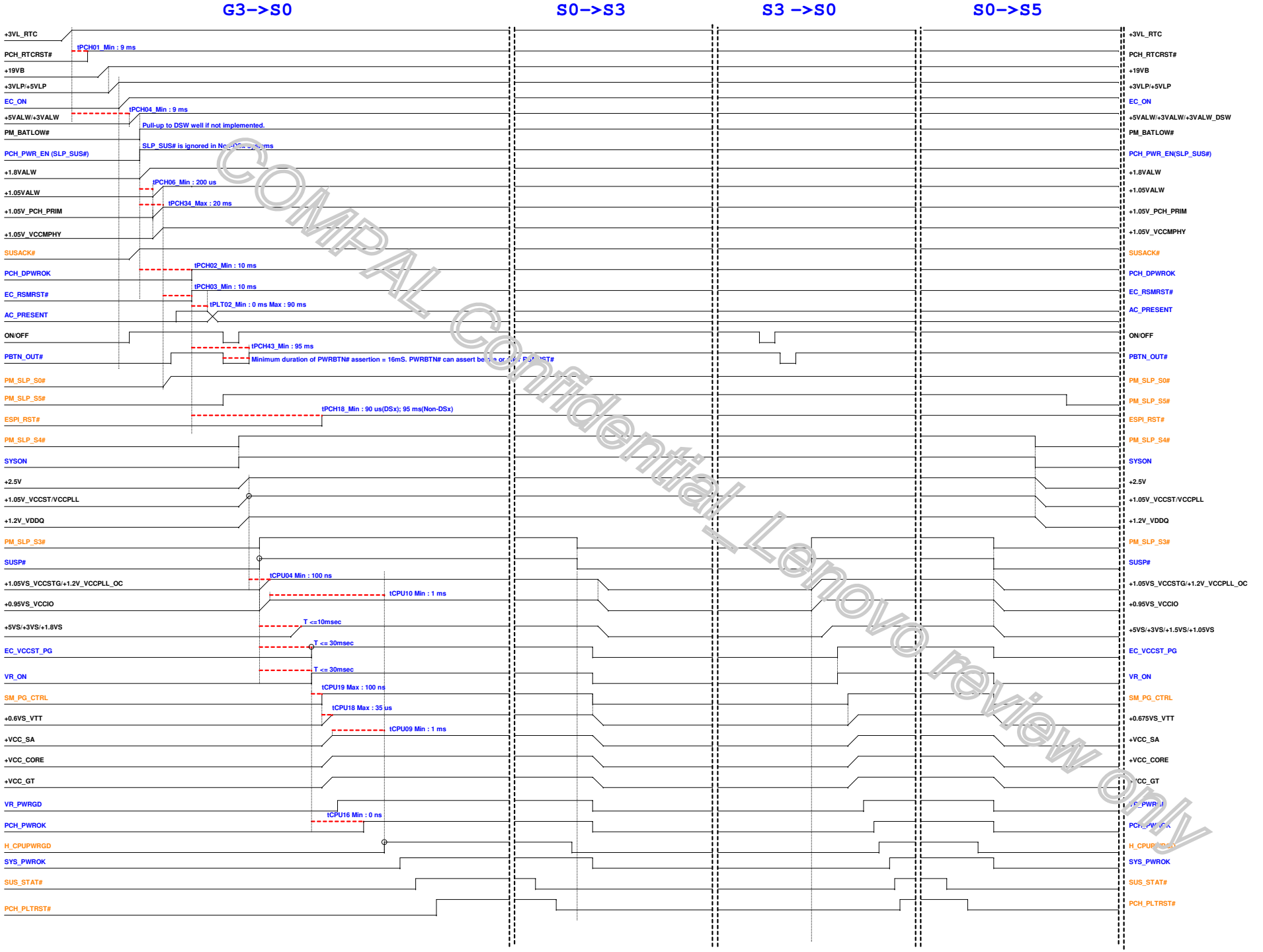
[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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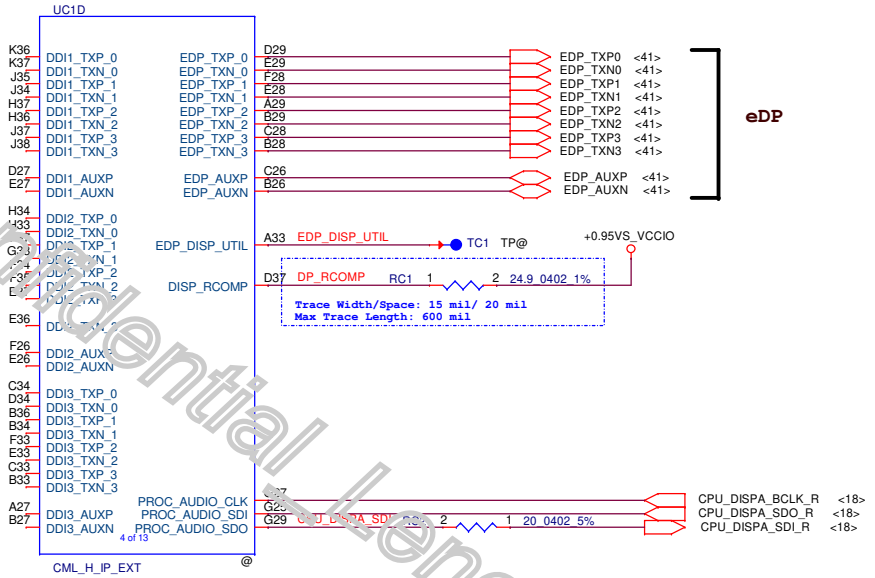

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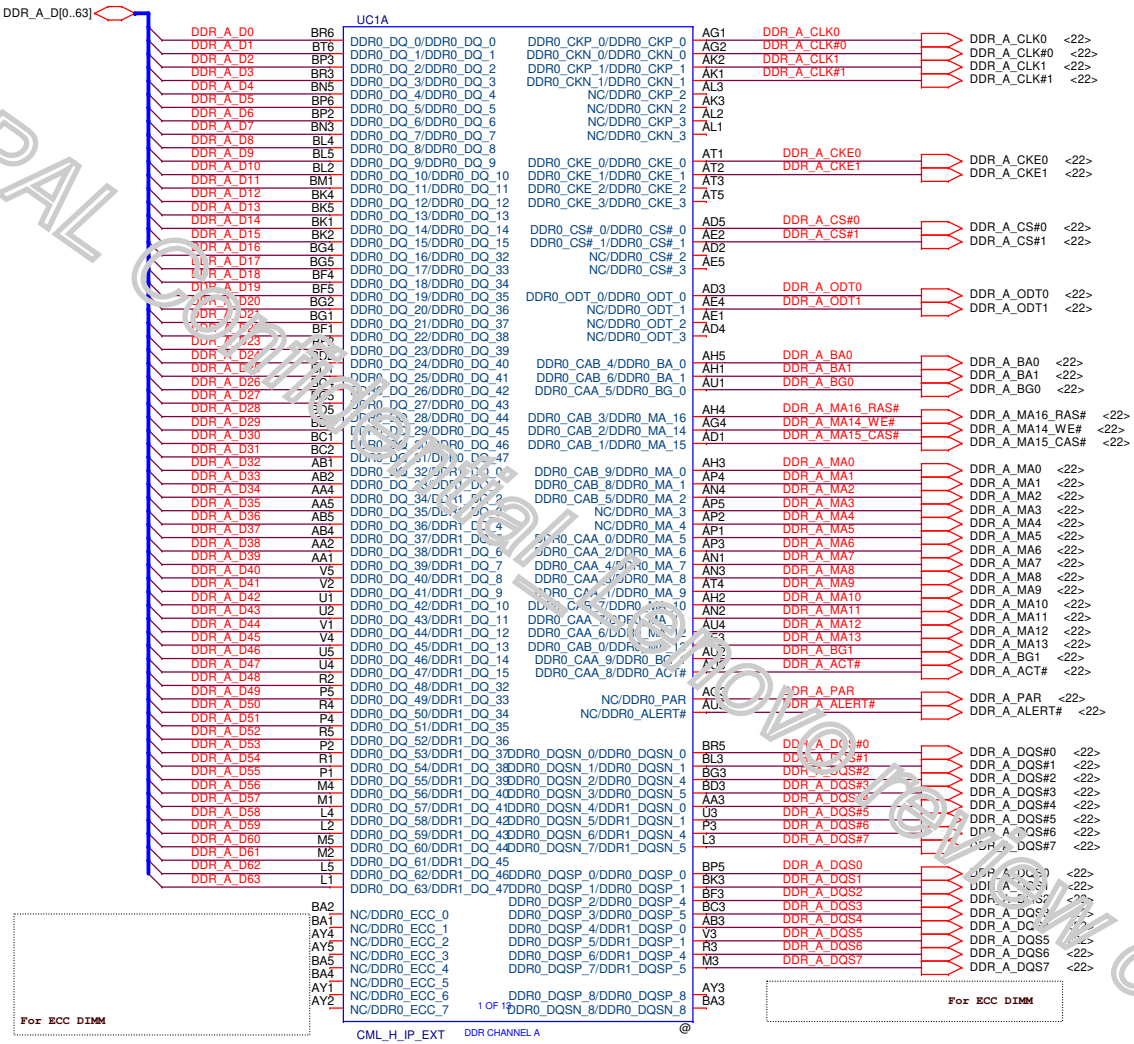
CHANNEL–A

Interleaved Memory



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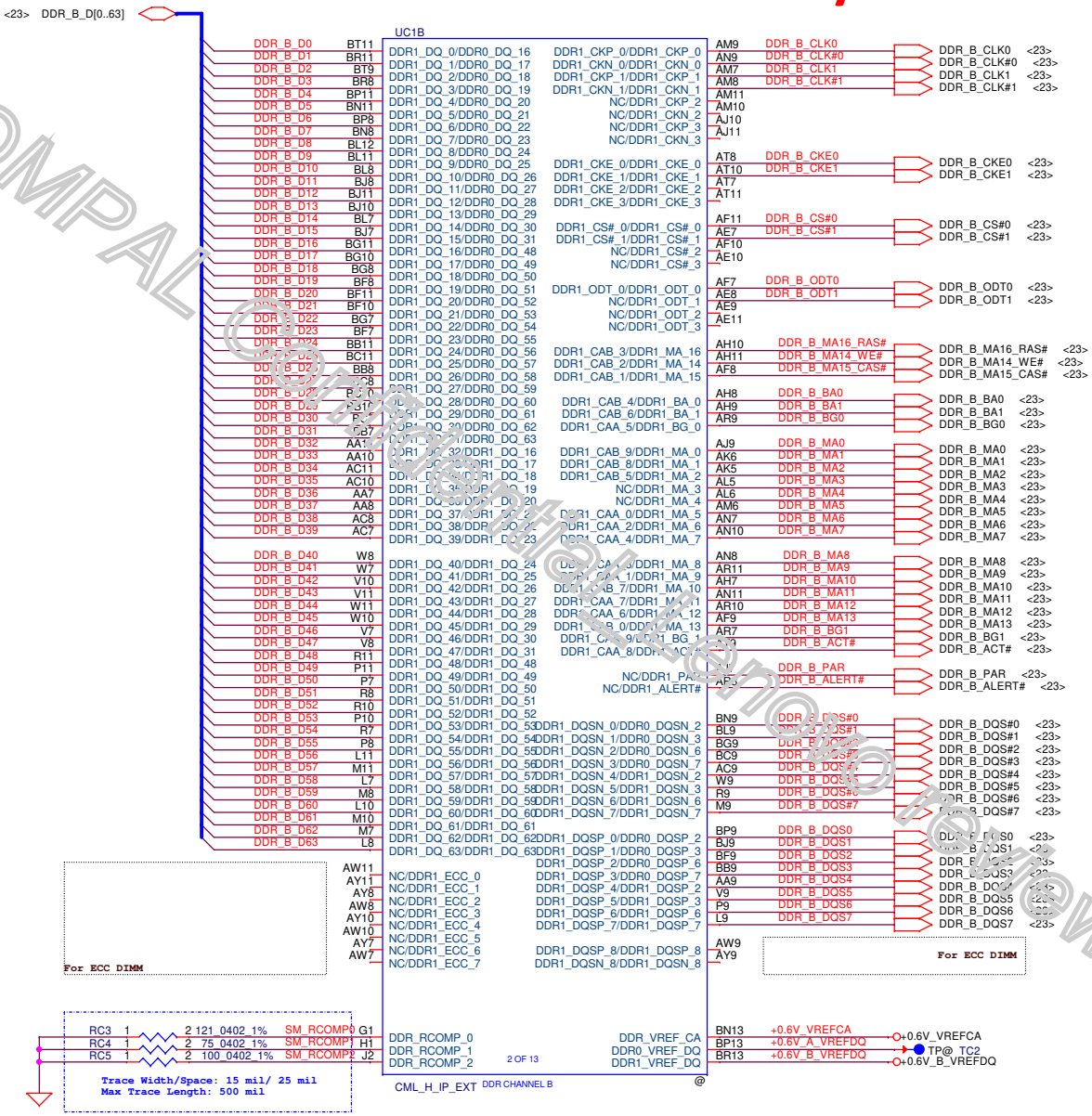
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 7 of 100		

CHANNEL-B

Interleaved Memory



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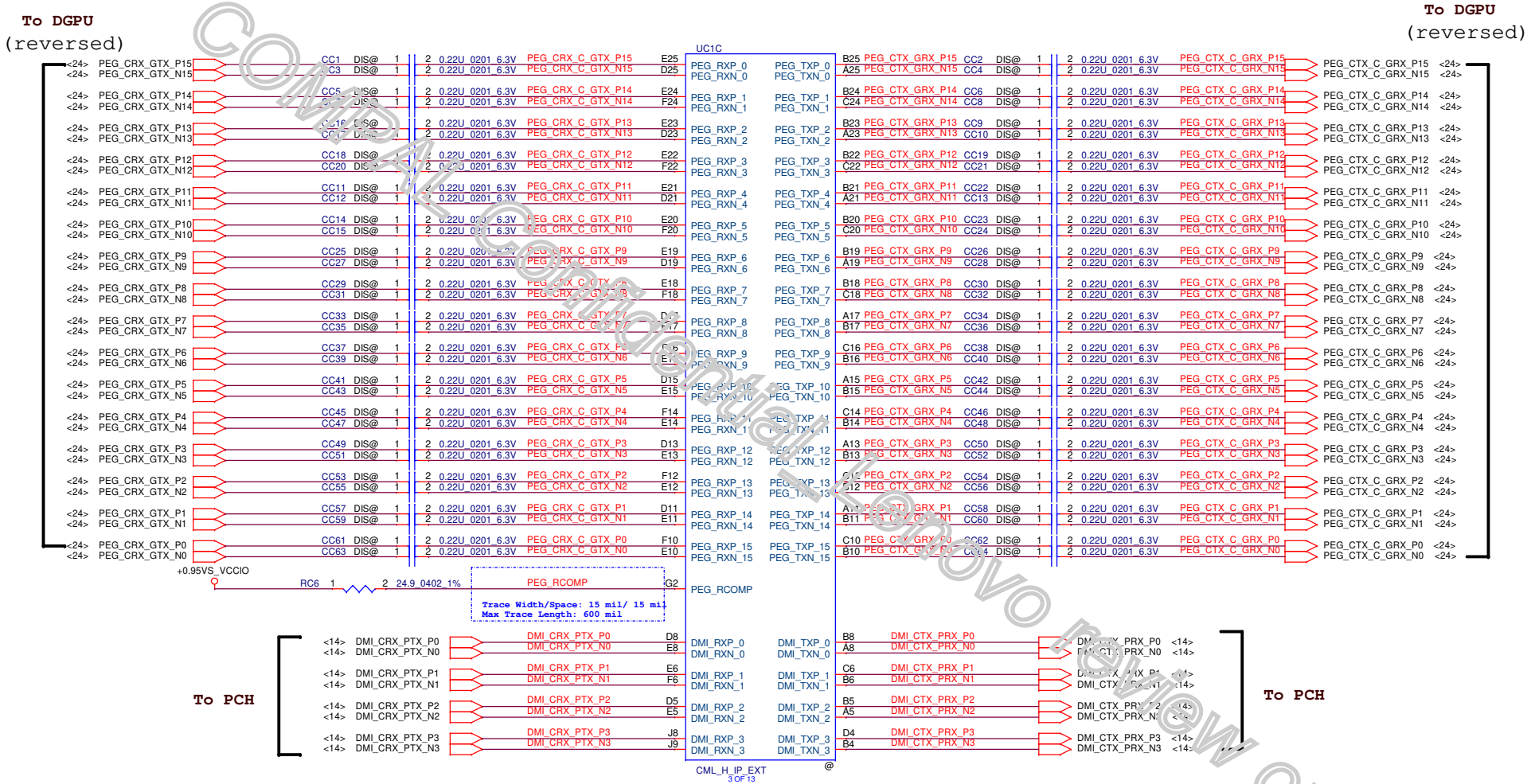
PEG&DMI



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Size: Custom	Document Number: LA-J561P		Rev: 1.0
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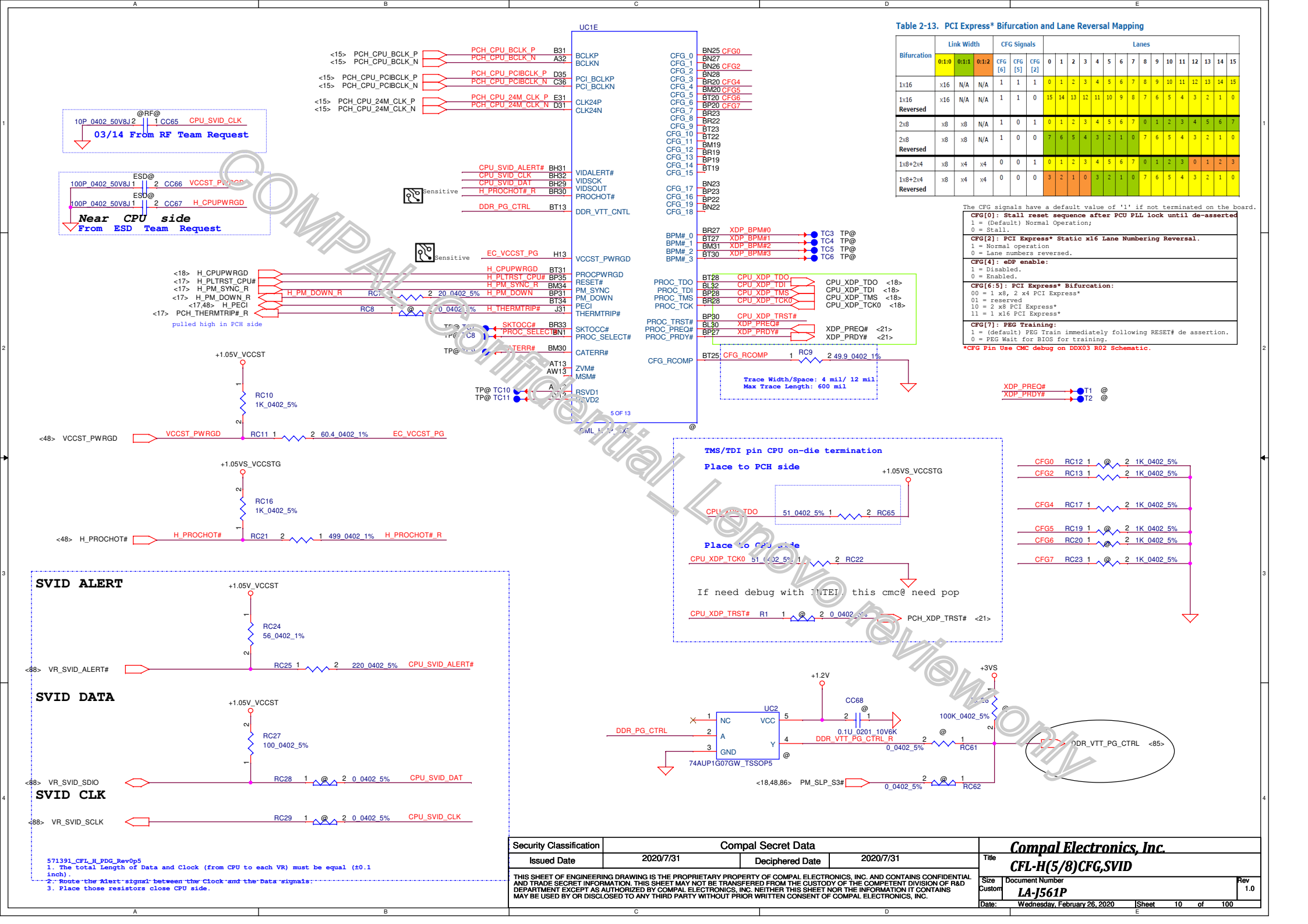

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

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Title	CFL-H(5/8)CFG,SVID		
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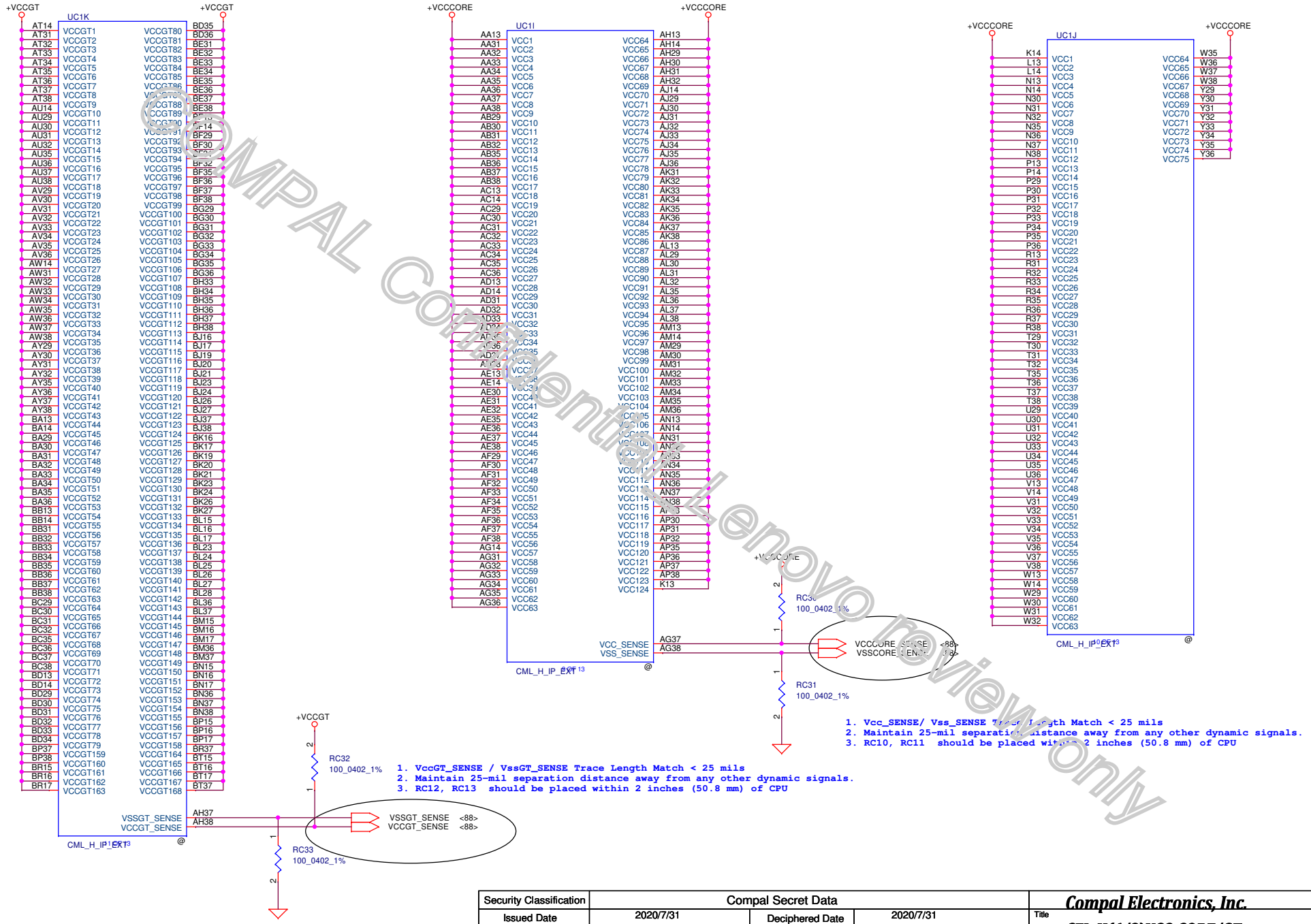
GT
32000mA(Hexa Core GT2)

128000mA(Hexa Core GT2)



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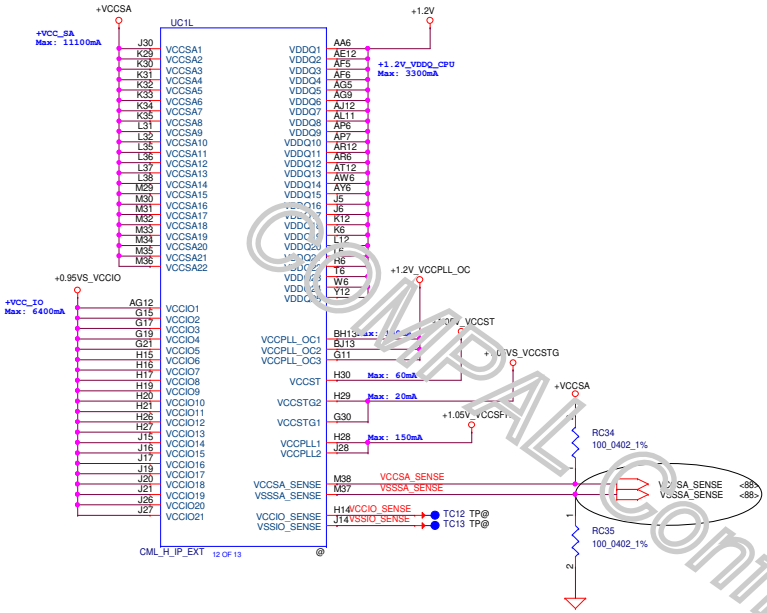
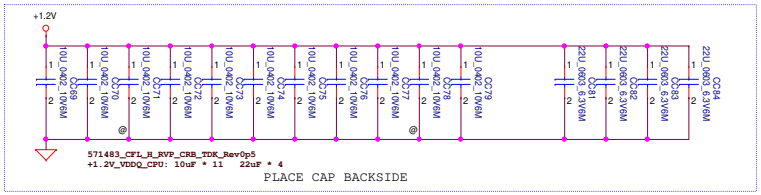
Compal Electronics, Inc.

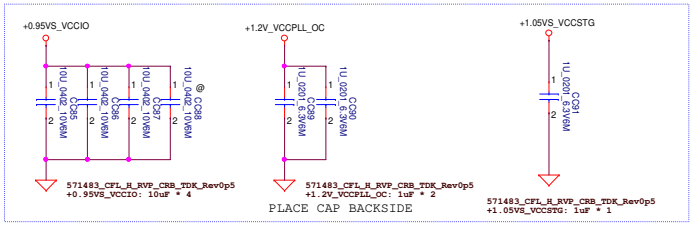
Title: CFL-H(6/8)VCC CORE/GT

Size: Custom | Document Number: LA-J561P | Rev: 1.0

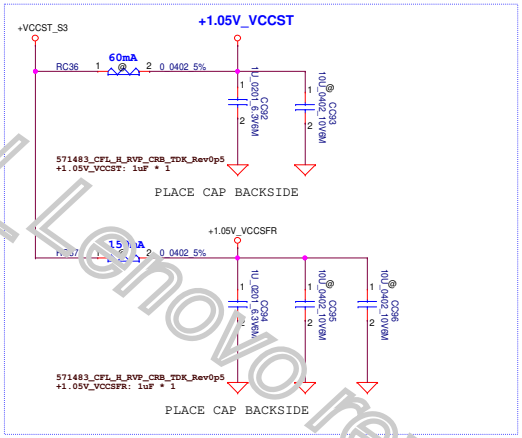
Date: Wednesday, February 26, 2020 | Sheet 11 of 100

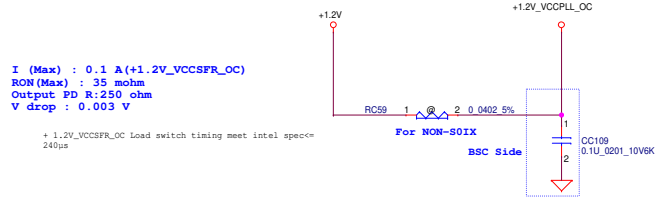




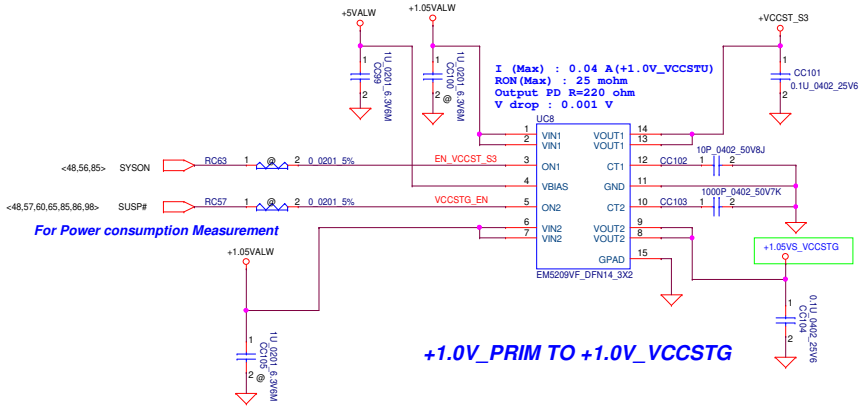


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC15, RC16 should be placed within 2 inches (50.8 mm) of CPU





+1.0V_PRIM to +VCCST_S3



+1.0V_PRIM TO +1.0V_VCCSTG

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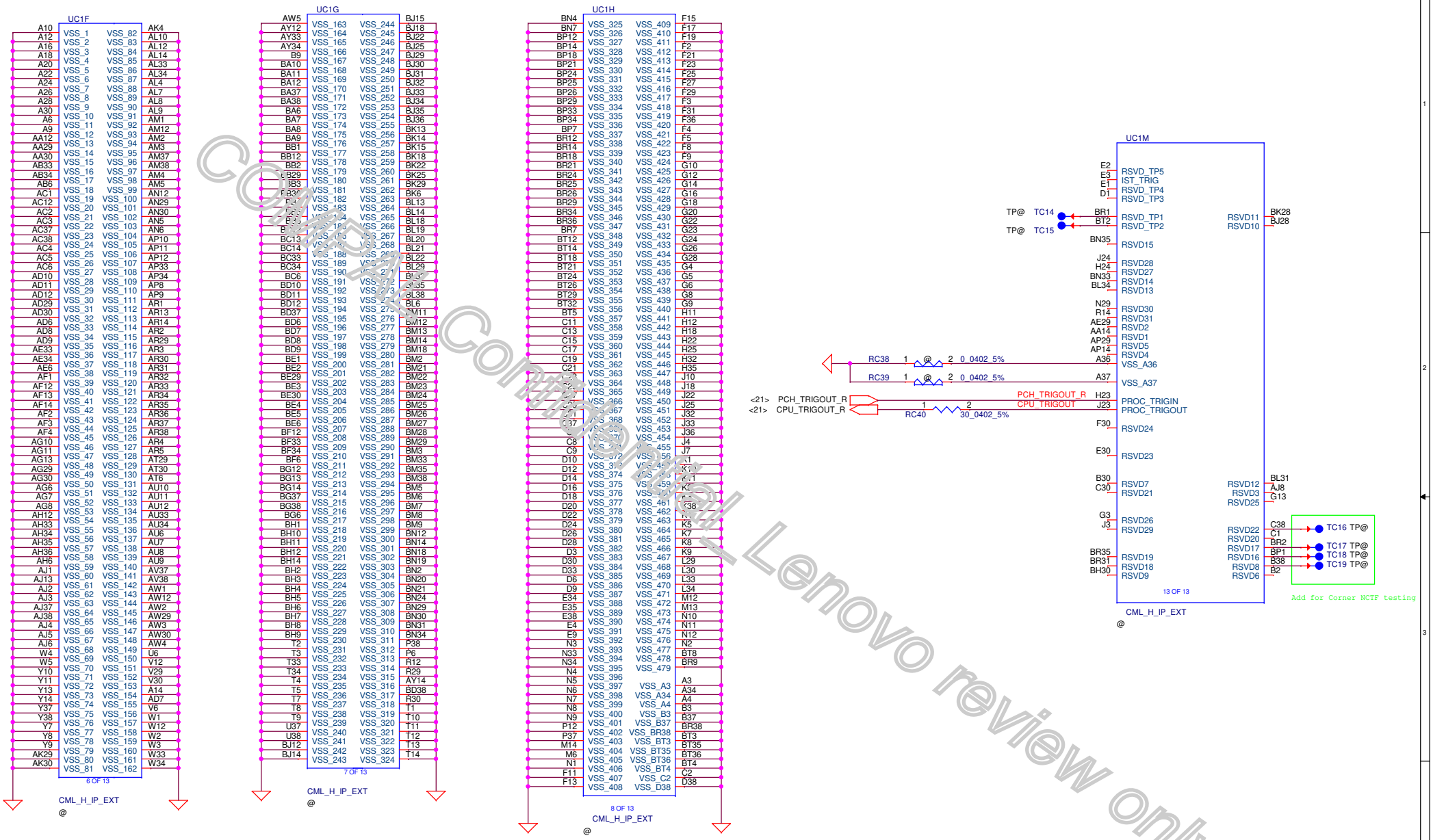
Compal Electronics, Inc.			
Title	CFL-H(7/8)VCCSA/VCCIO/VDDQ		
Size C	Document Number LA-J561P		Rev 1.0
Date: Wednesday, February 26, 2020	Sheet 12 of 100		



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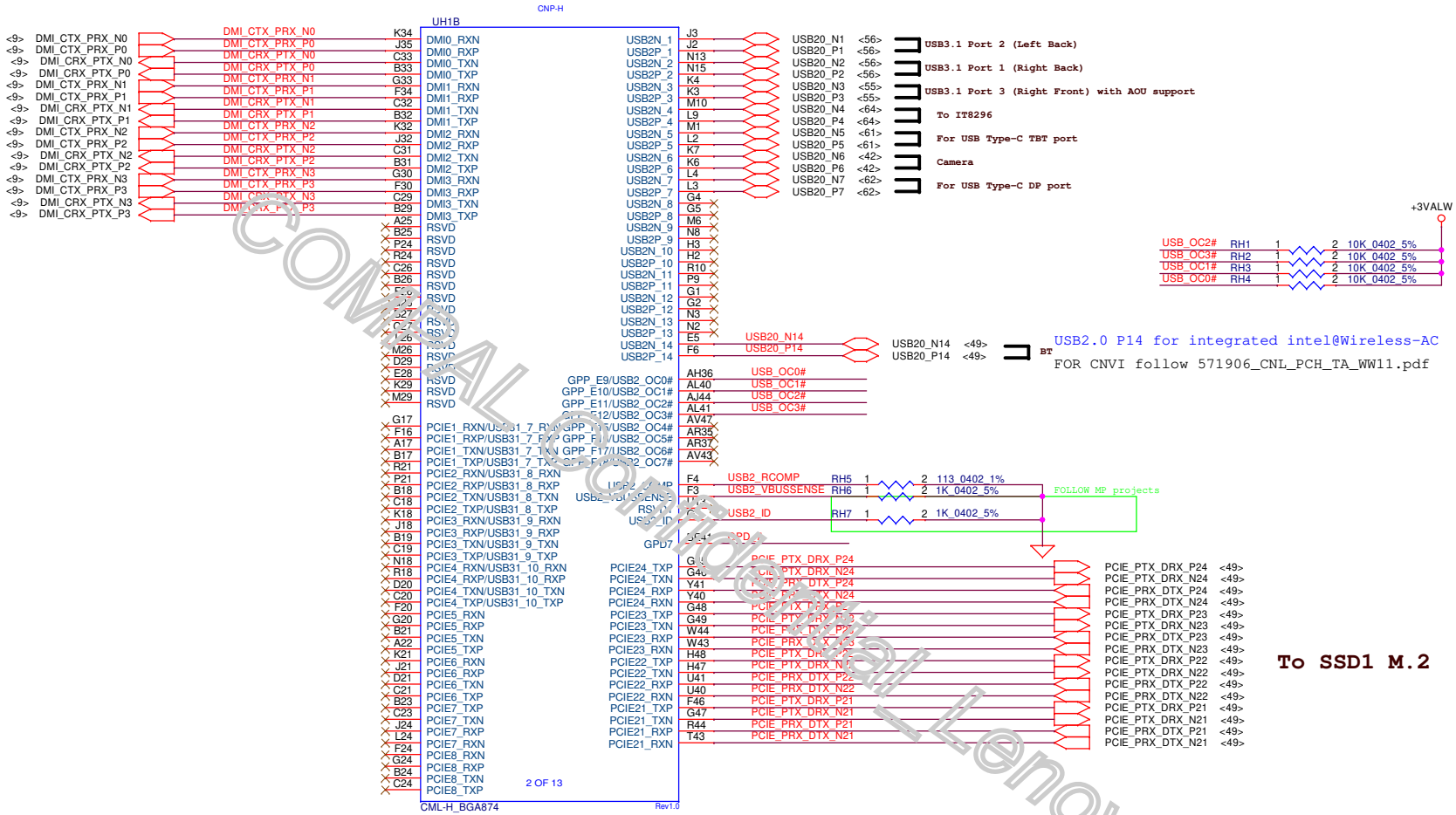
Compal Electronics, Inc.			
Title: CFL-H(8/8)GND/RSVD			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 13 of 100		



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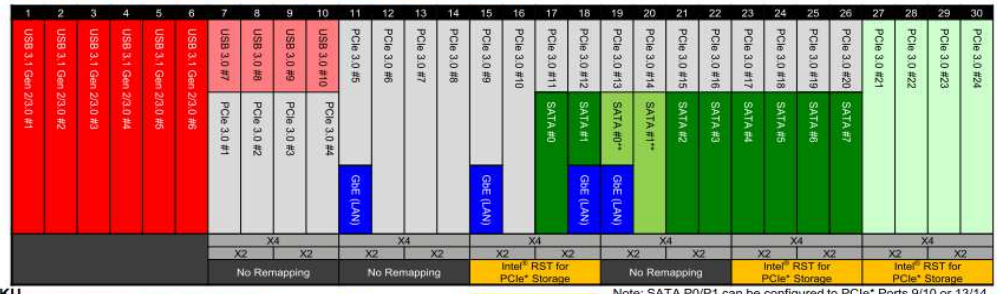
Comet Lake PCH-H HSIO Lane Assignments

- Up to 30 High-Speed I/O Lanes with Port Flexibility.

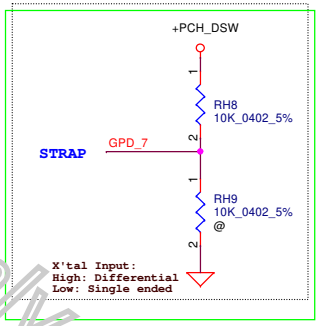


PCH SKU

Note: SATA P0/P1 can be configured to PCIe* Ports 9/10 or 13/14

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
–A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5) and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



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Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size	Document Number	Rev
Custom	LA-J561P	1.0

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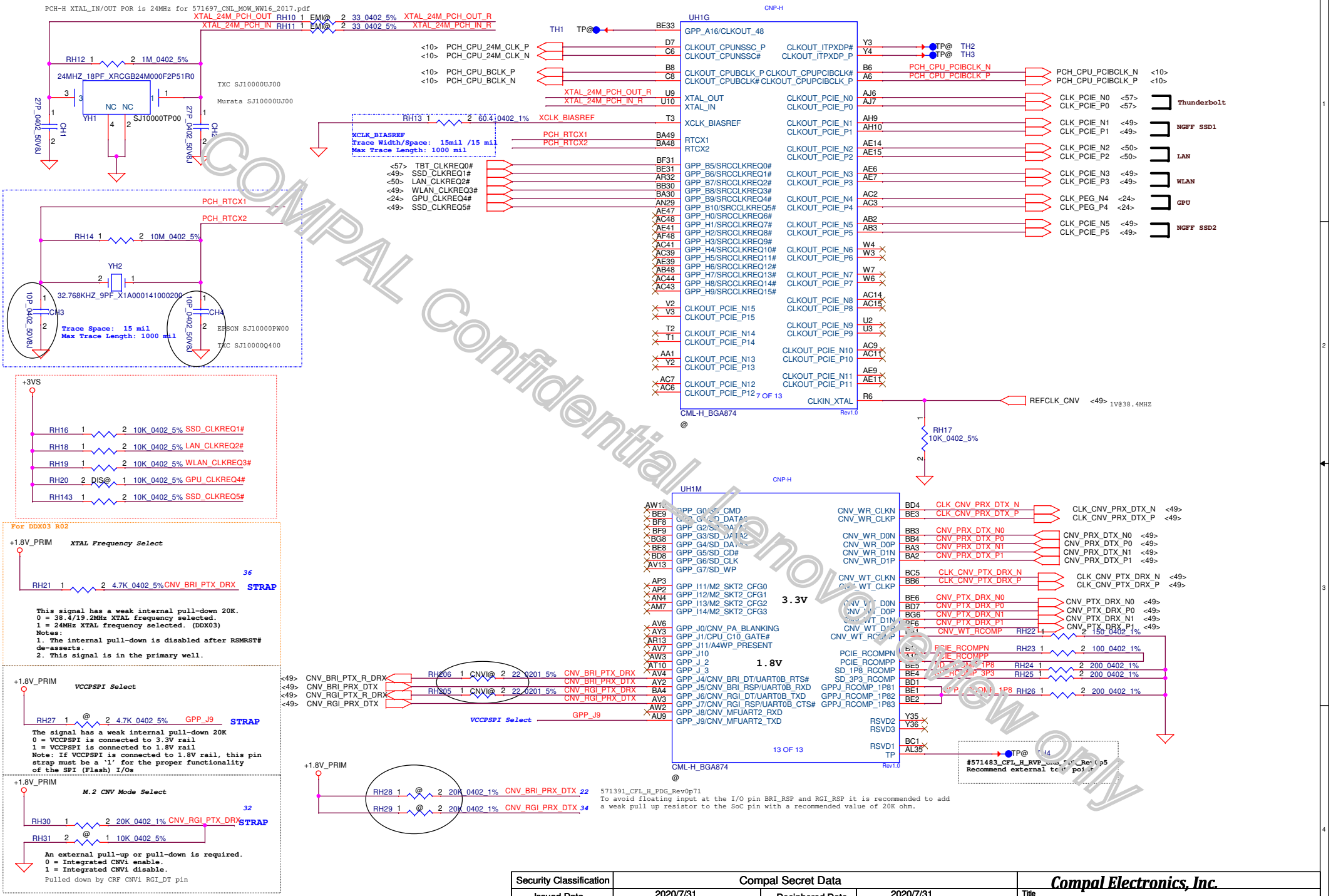

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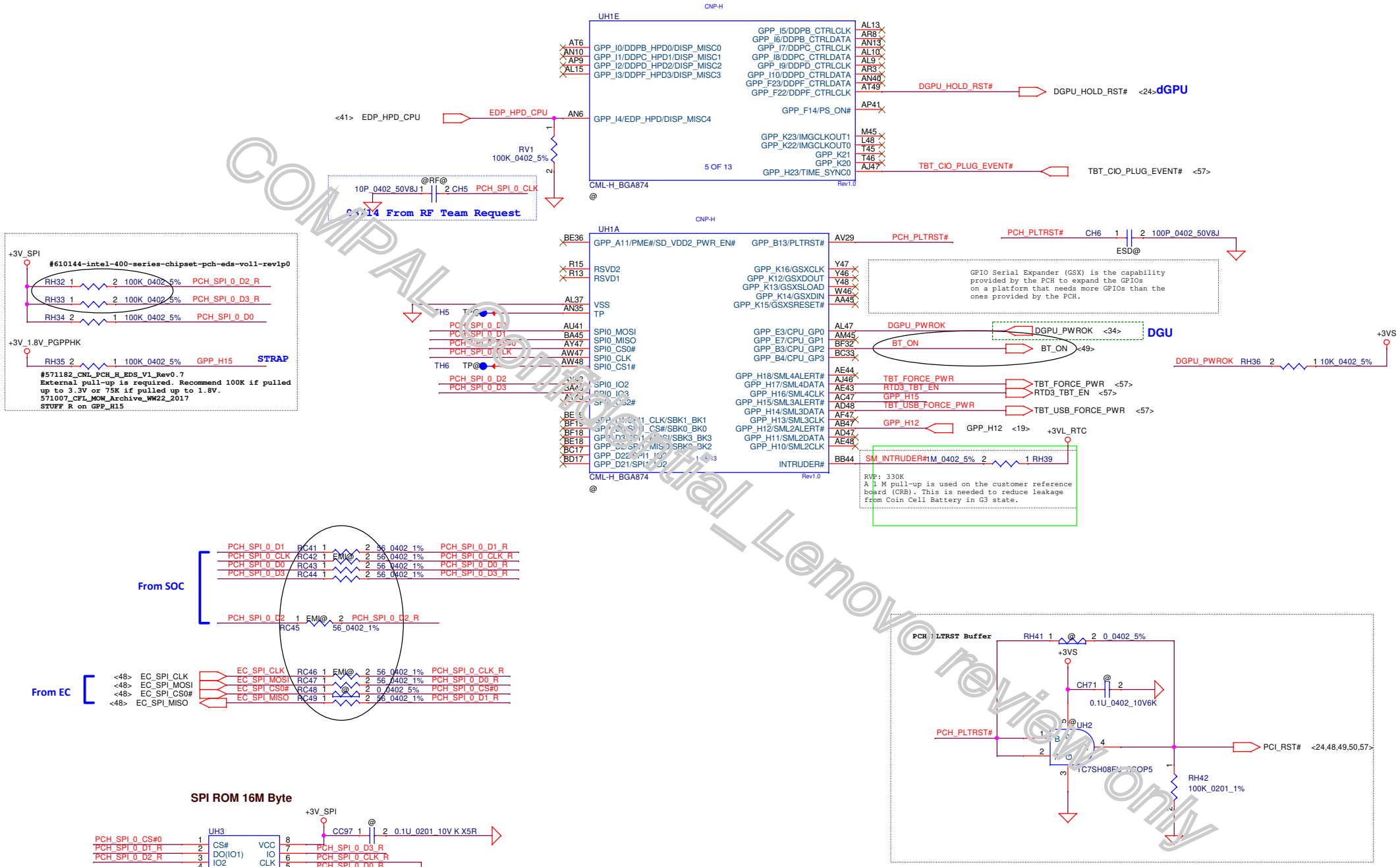
Compal Electronics, Inc.			
Title	PCH(2/8)CLK/CNVI/SD		
Size	Document Number		Rev
Custom	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	15 of 100



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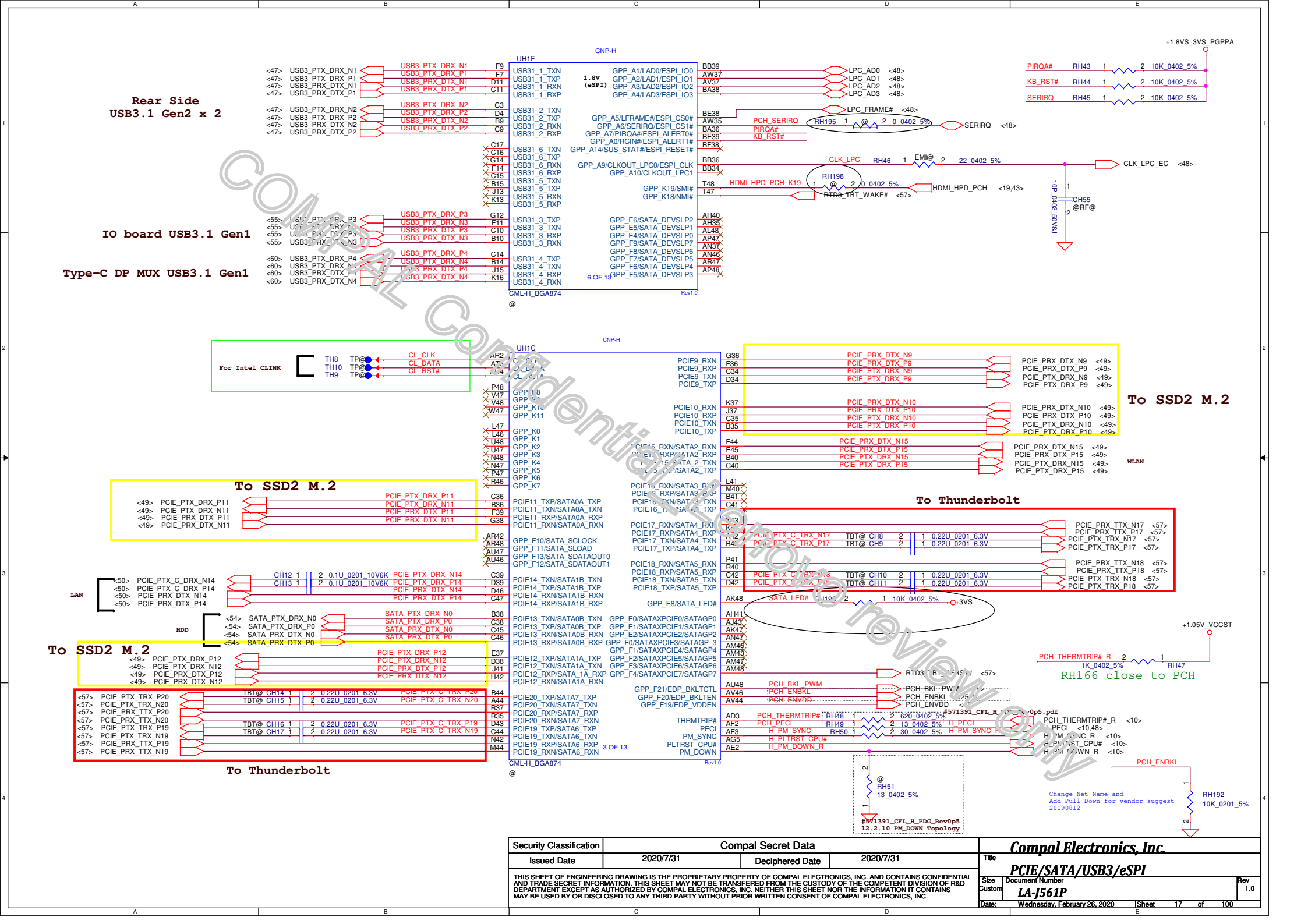
Compal Electronics, Inc.			
Title	PCH(3/8)DDC/SPI		
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 16 of 100		



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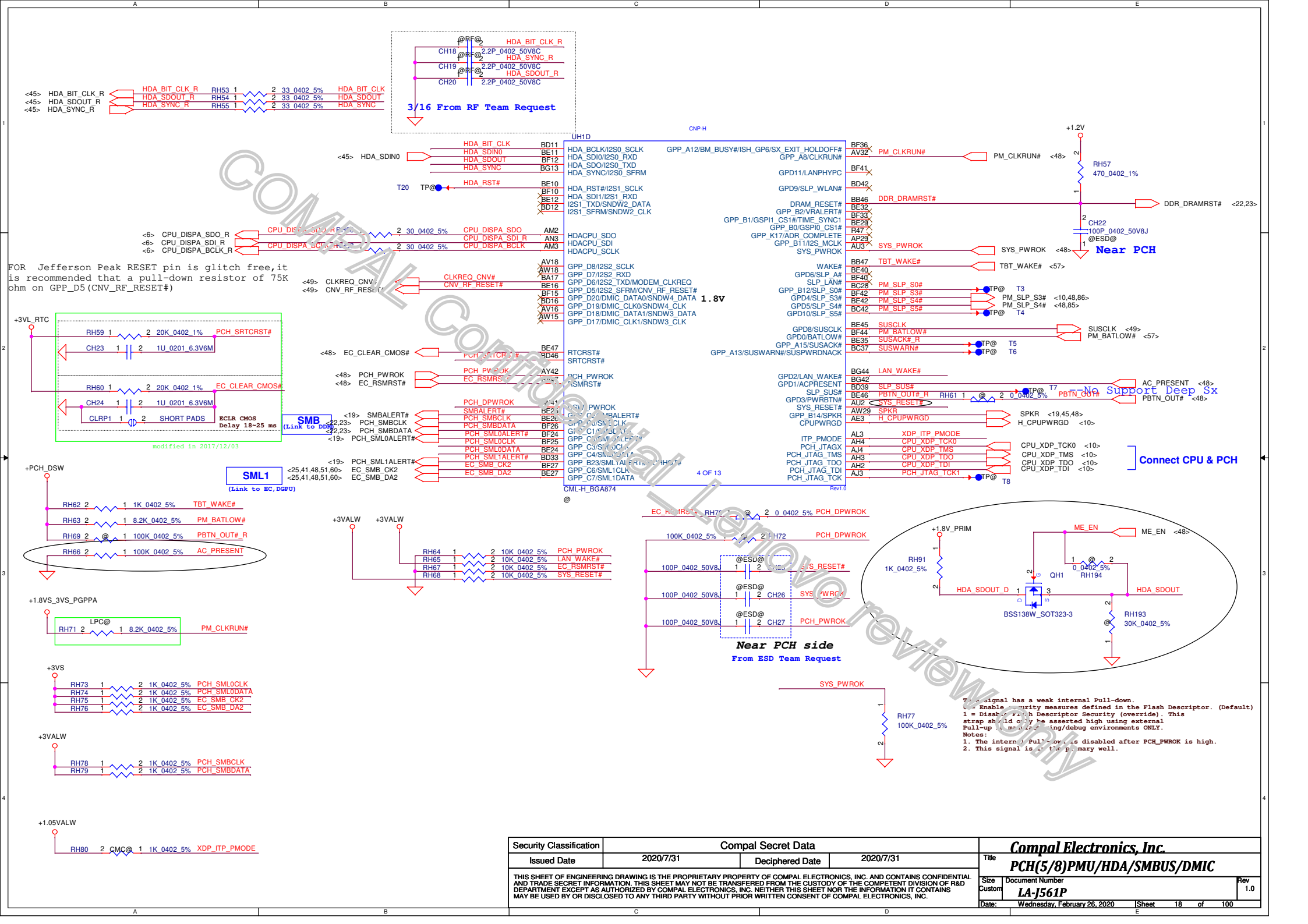
Compal Electronics, Inc.			
Title: PCIE/SATA/USB3/eSPI			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 17 of 100		



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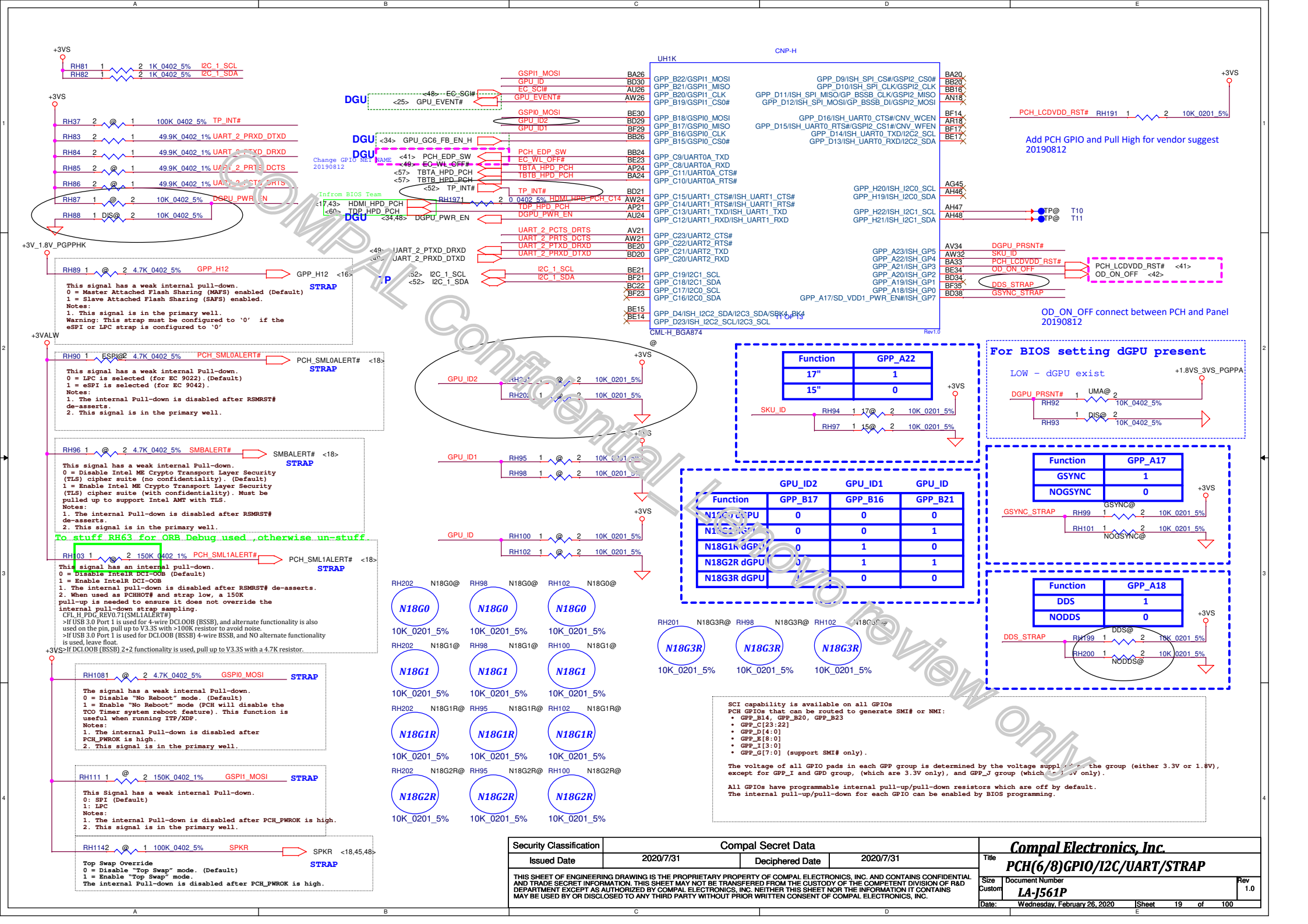
Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS/DMIC		
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 18 of 100		



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Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	LA-J561P	1.0

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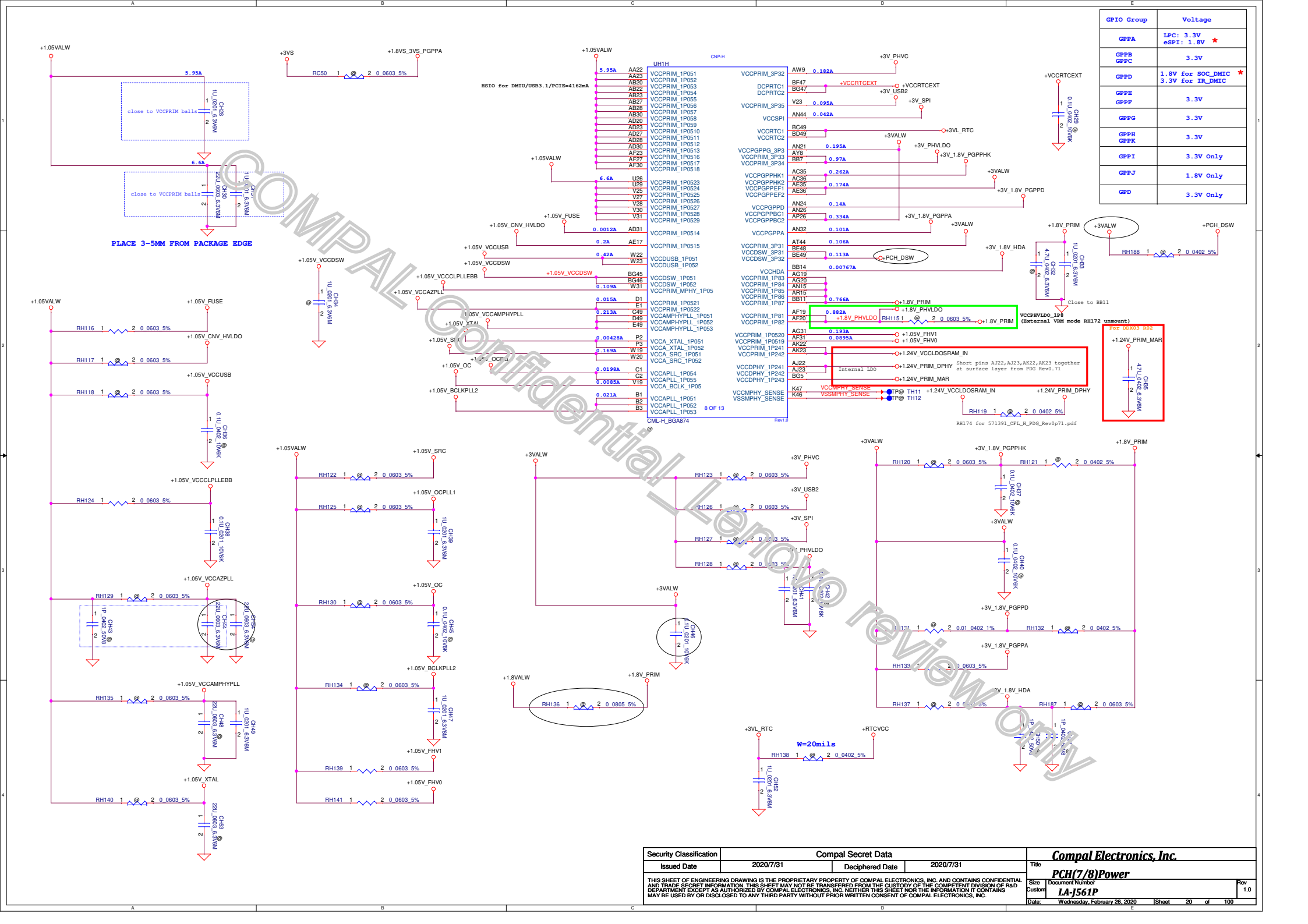

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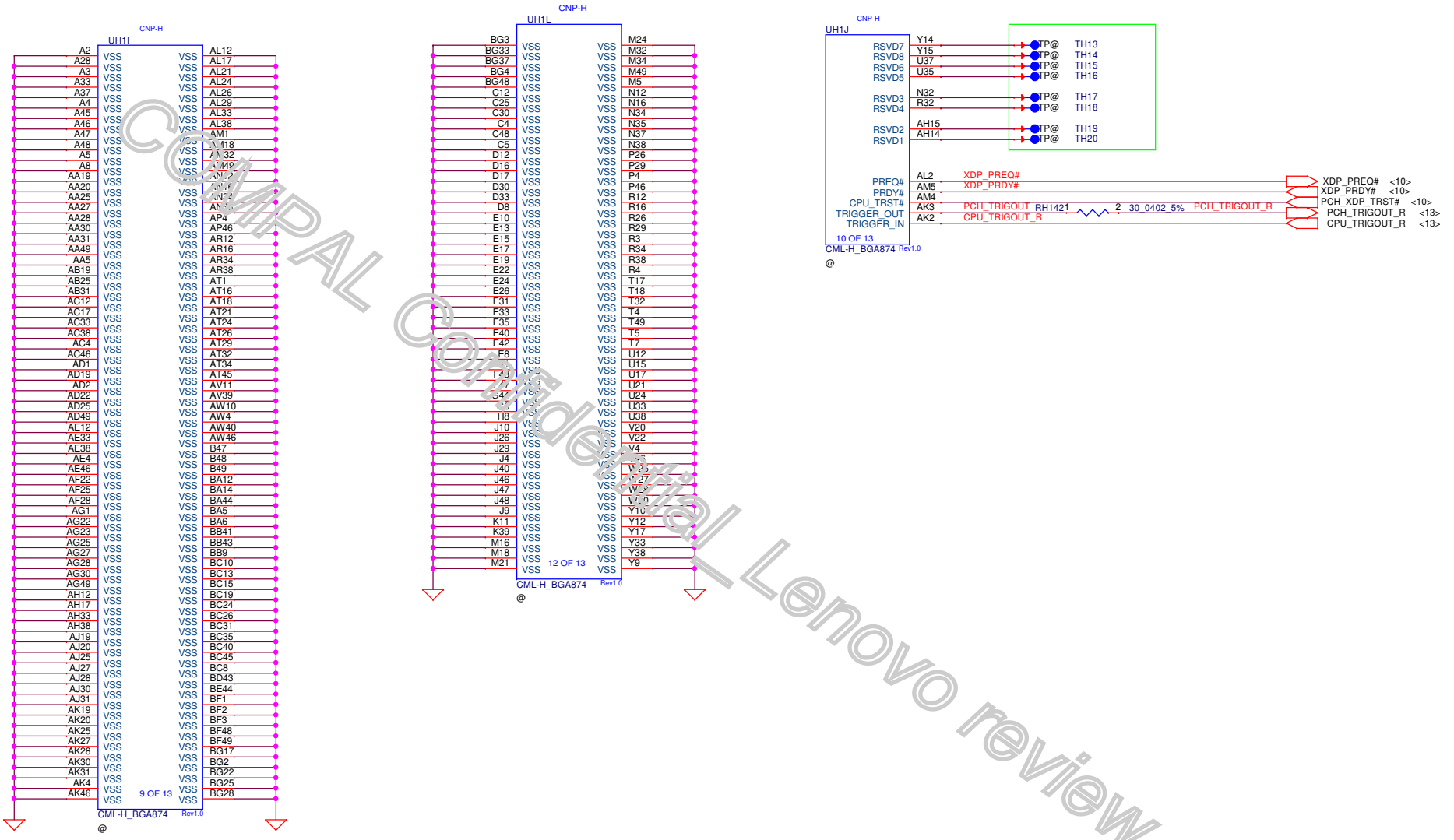
Compal Electronics, Inc.			
Title: PCH(7/8)Power			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet: 20	of: 100	



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Title: **PCH(8/8)GND/RSVD**

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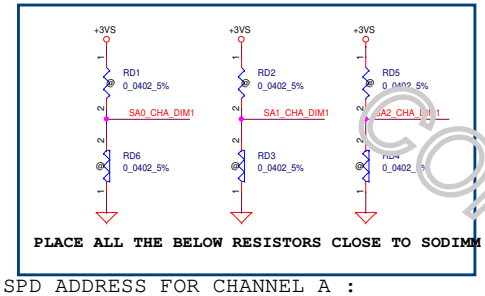
CHANNEL-A

BOT

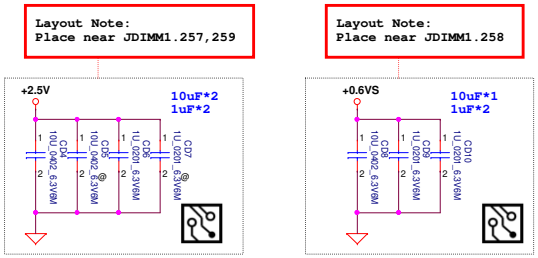
REVERSE TYPE (4 mm)

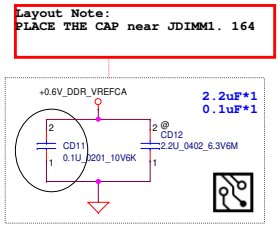
Interleaved Memory

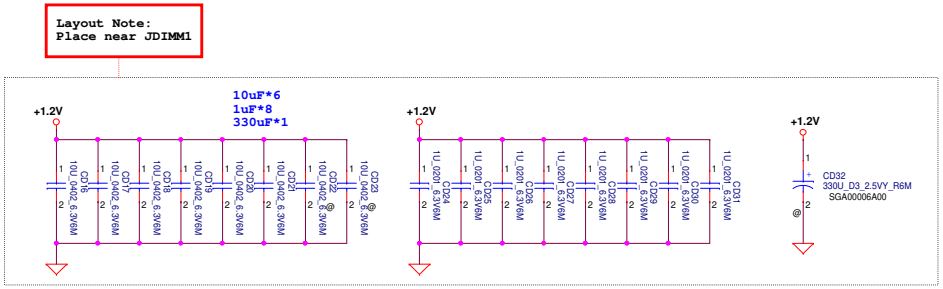
TOP: JDIMM1 CONN Non-ECC DIMM

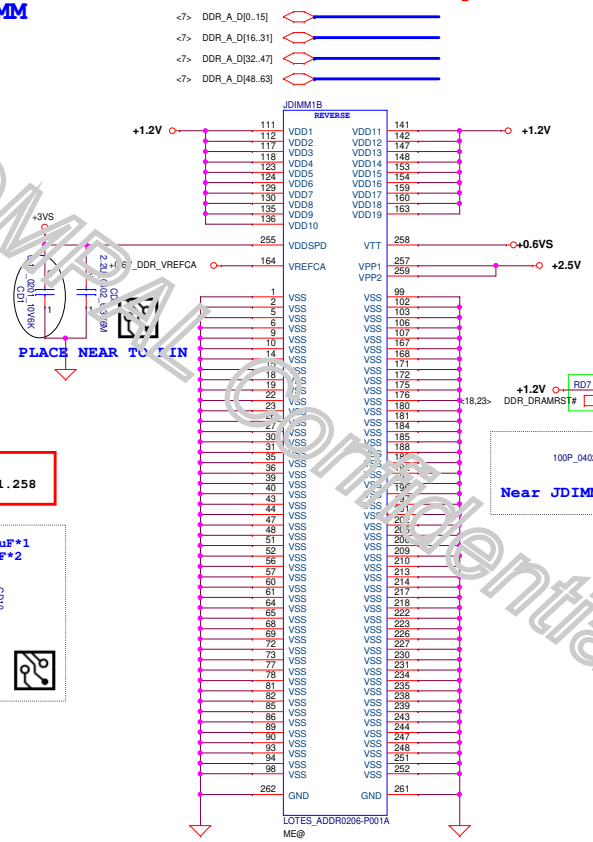


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

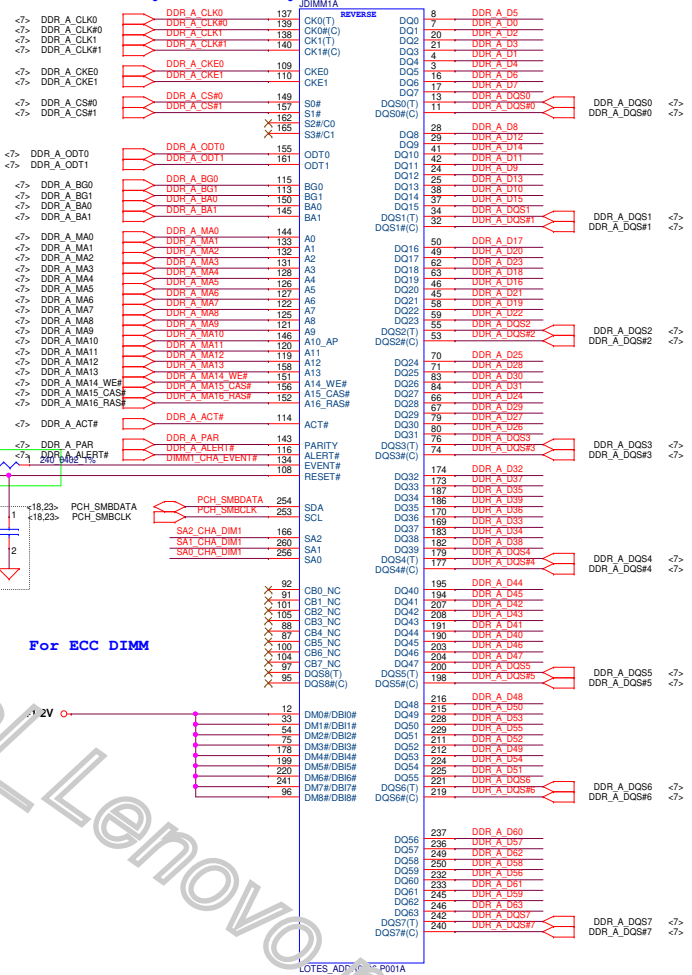


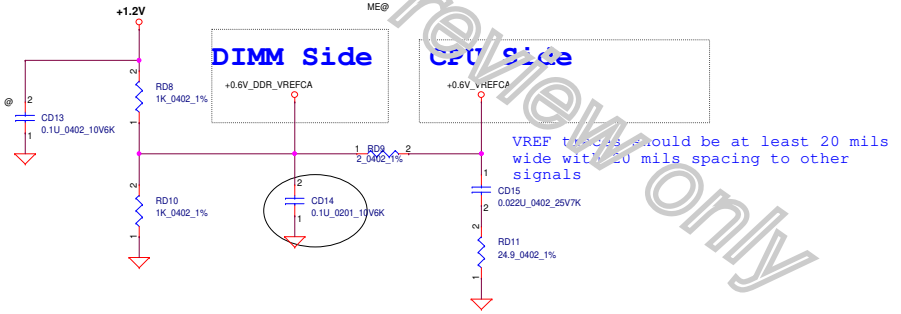






Part Number:SP07001FYH0
Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4





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Compal Electronics, Inc.			
Title	DDRIV_CHA: DIMM0		
Size	Document Number		Rev
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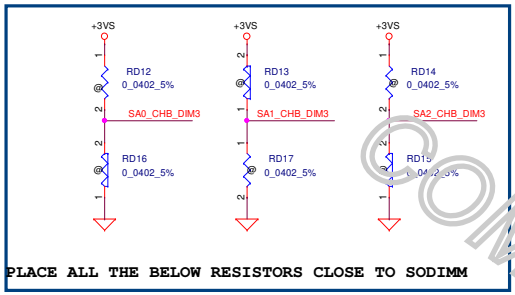
CHANNEL-B

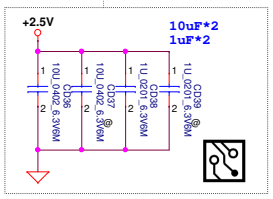
TOP: JDIMM3 CONN Non-ECC DIMM



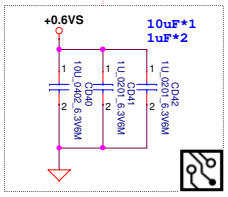
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

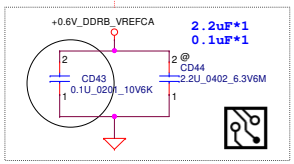
Layout Note:
Place near JDIMM3.257,259



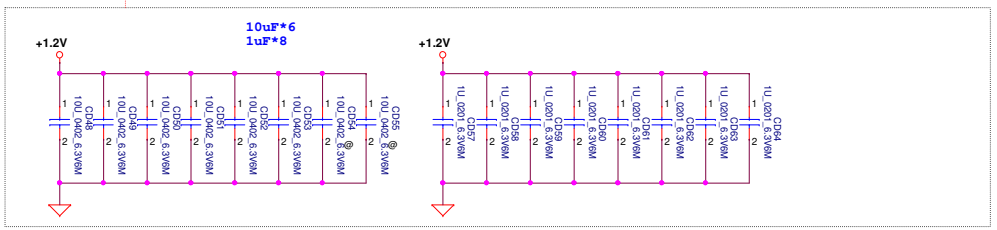
Layout Note:
Place near JDIMM3.258



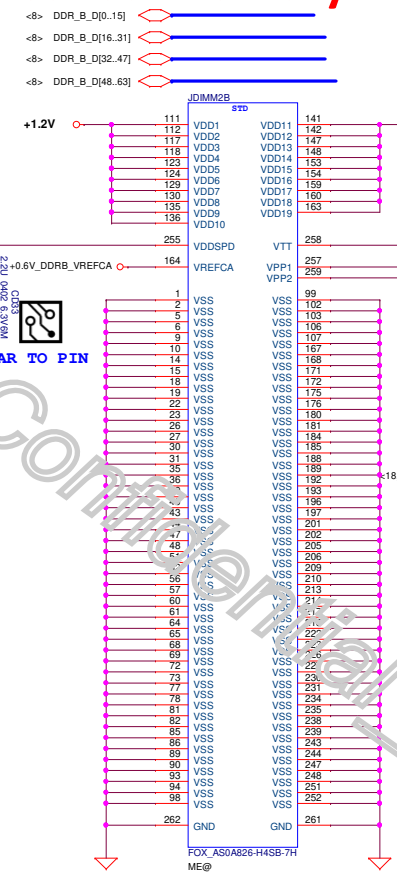
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



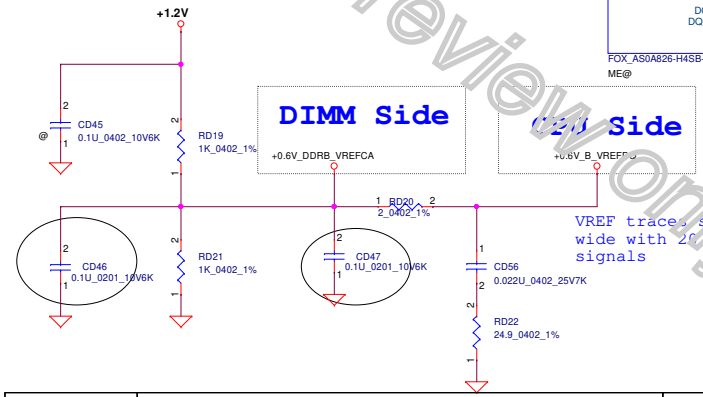
Layout Note:
Place near JDIMM3



Interleaved Memory



Part Number:SP07001CEA0
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4



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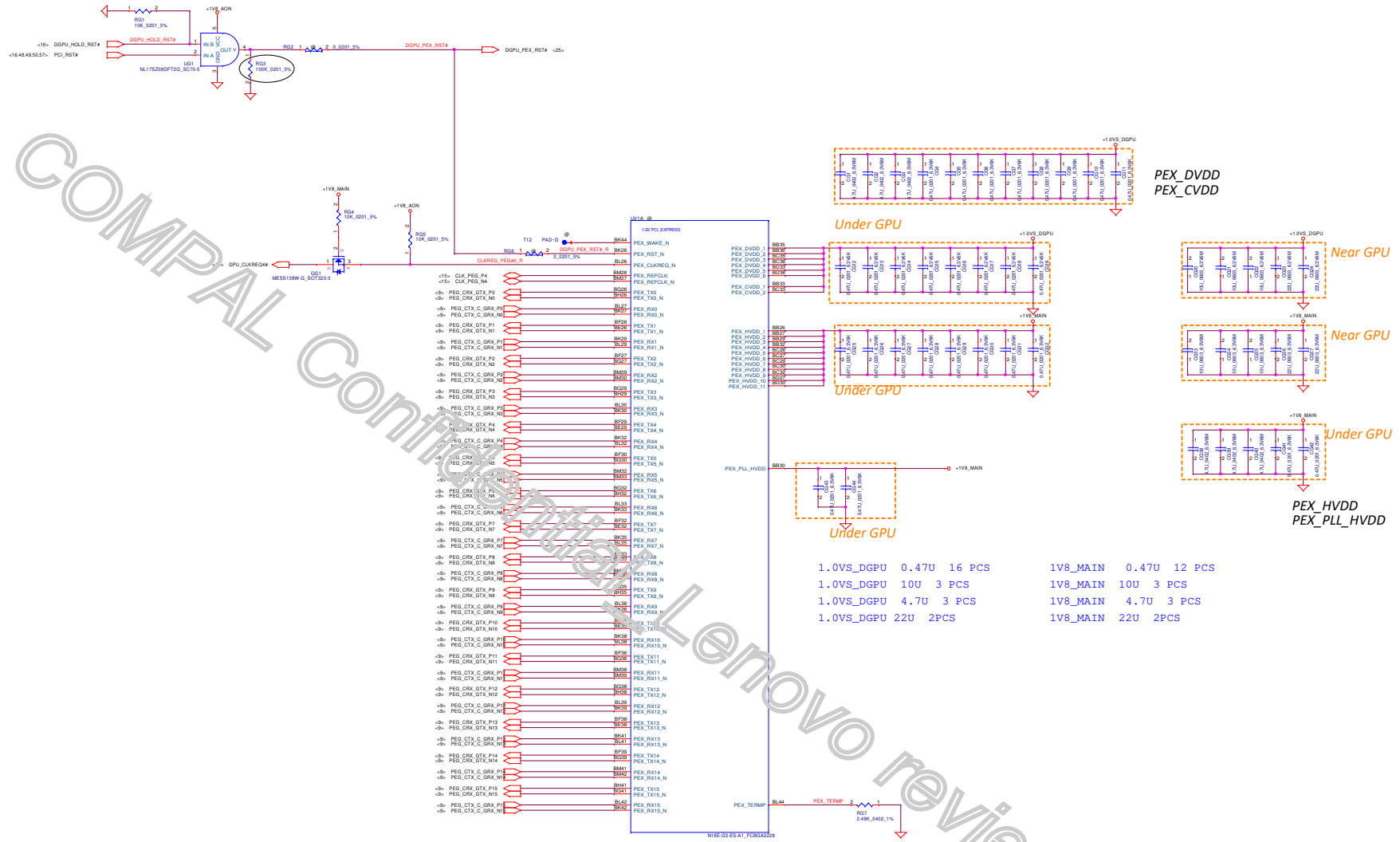
GC OFF 1.0 GPU Power ON/OFF



1.0VS_DGPU 0.47U 16 PCS
1.0VS_DGPU 10U 3 PCS
1.0VS_DGPU 4.7U 3 PCS
1.0VS_DGPU 22U 2PCS

1V8_MAIN 0.47U 12 PCS
1V8_MAIN 10U 3 PCS
1V8_MAIN 4.7U 3 PCS
1V8_MAIN 22U 2PCS

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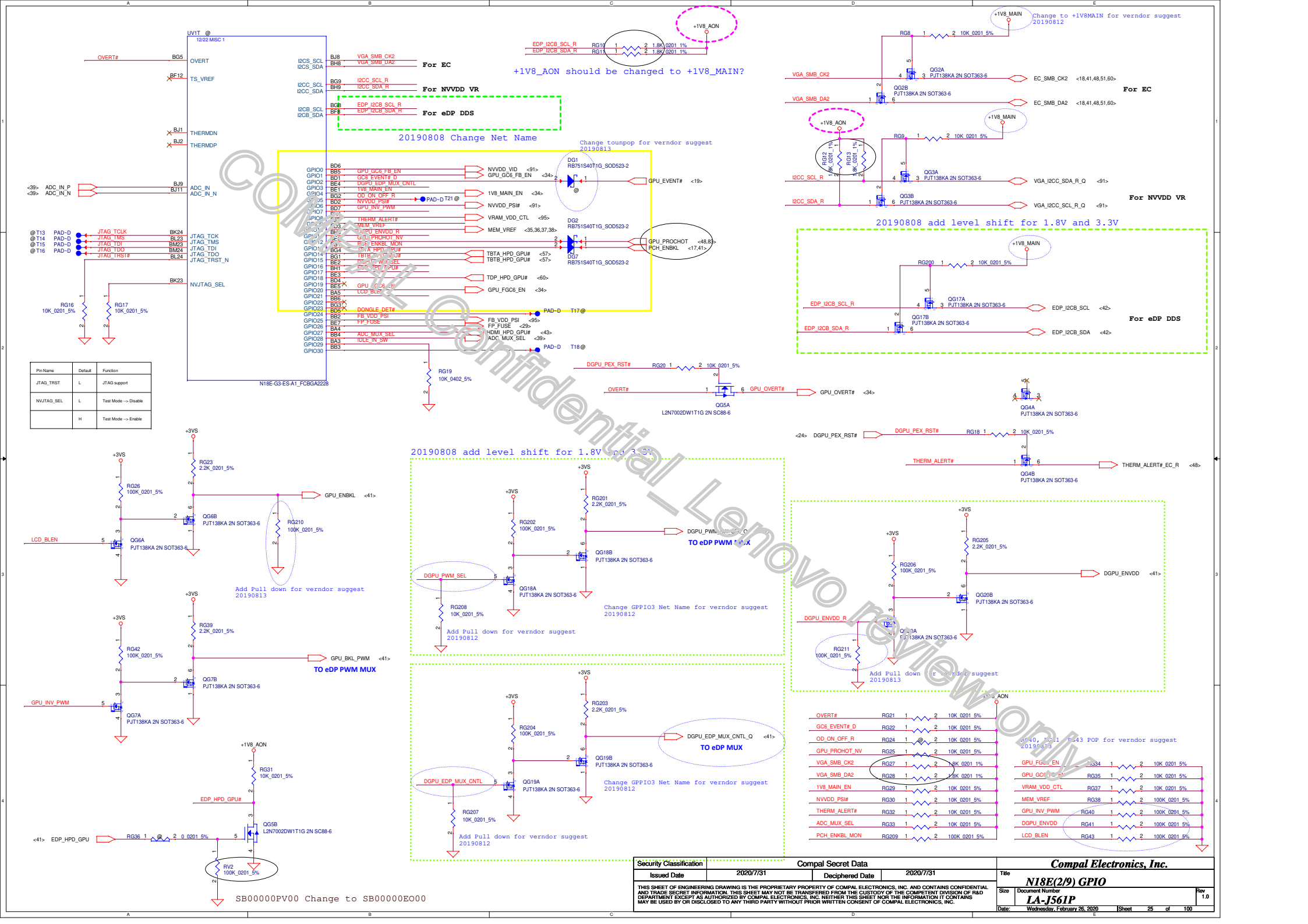

Pin Name	Default	Function
JTAG_TRST	L	JTAG support
NVJTAG_SEL	L	Test Mode --> Disable
	H	Test Mode --> Enable

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Title: **N18E(2/9) GPIO**

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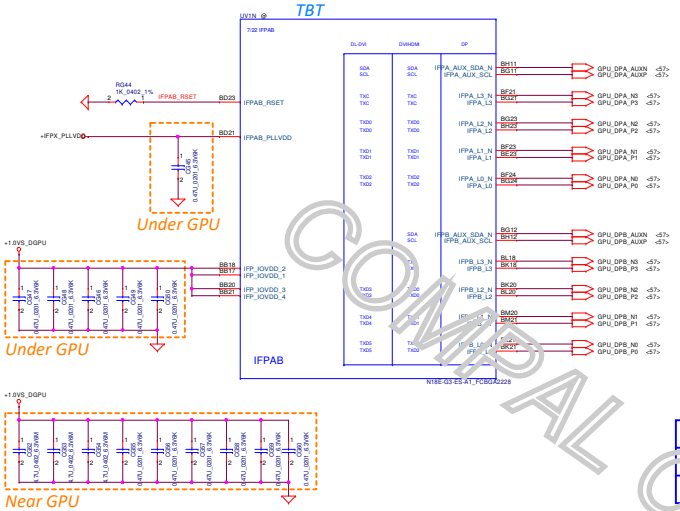


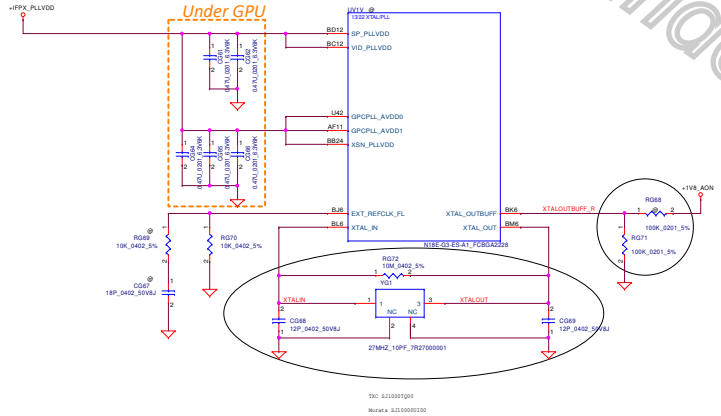


Table 11.3 RAMCFG

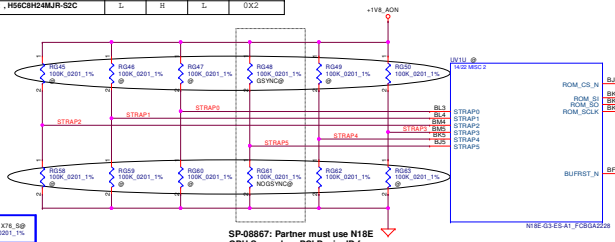
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)

GDDR6 VRAM	Strap2	Strap1	Strap0	RAMCFG
Samsung , K4Z80325BC-HC14	L	L	L	0X0
Micron , MT61K256M32JE-14:A	L	L	H	0X1
Hynix , H56C8H24MJR-S2C	L	H	L	0X2

Table 11.4 FS_OVERT* Strap Enablement

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.

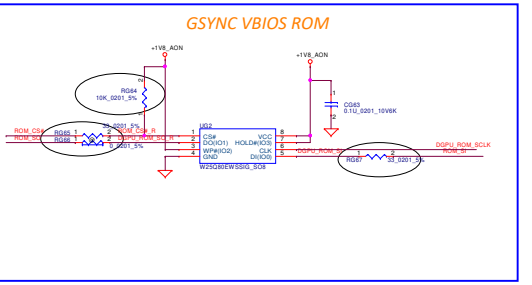


Samsung	RG58 X76_S@ 100K_0201_1%	RG59 X76_S@ 100K_0201_1%	RG60 X76_S@ 100K_0201_1%
Micron	RG58 X76_M@ 100K_0201_1%	RG59 X76_M@ 100K_0201_1%	RG47 X76_M@ 100K_0201_1%

Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be enabled, so that graphics circuits with multiple GPUs can have separate SMBus configurations for each GPU. In dual GPU configurations, use of the alternate address on one GPU (setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via function setting of '1').
- **PCIE_CFG**: This function selects characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '1' selects normal ("full") signal swing. N18x graphics circuits should strap for this setting. A setting of '0' designates reduced signal amplitude, available if special concerns require (consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to configure the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook applications. N18x graphics circuits (consult NVIDIA for details on proper bit setting for other applications).



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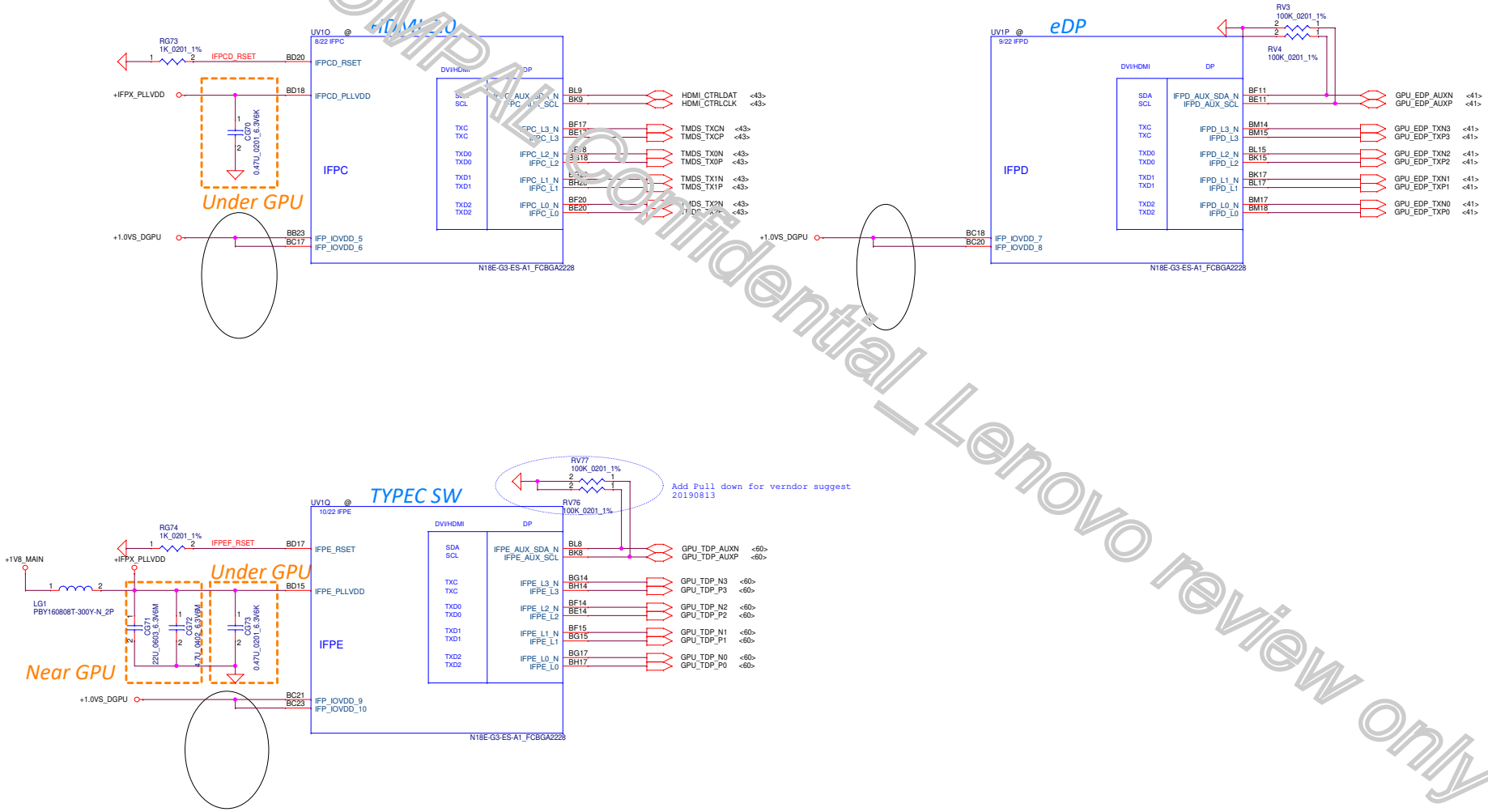

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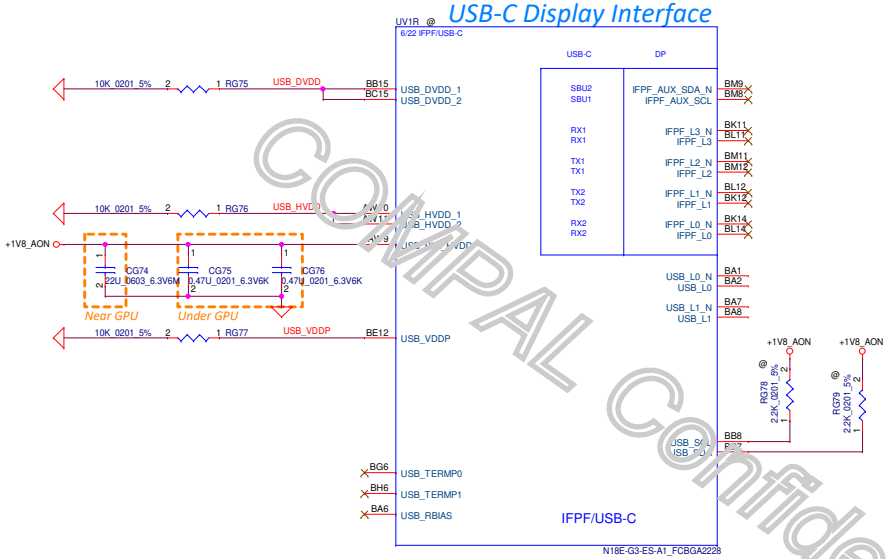

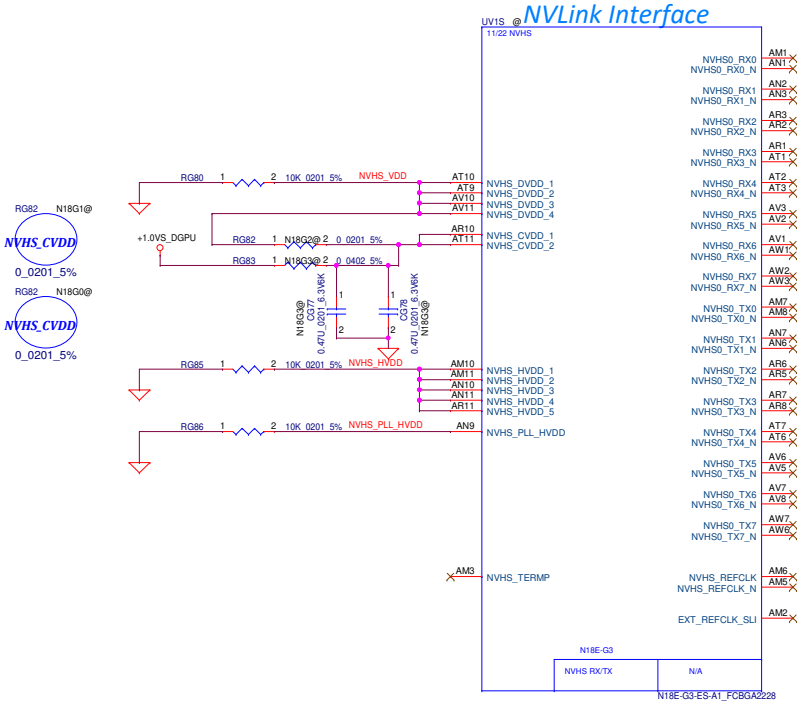

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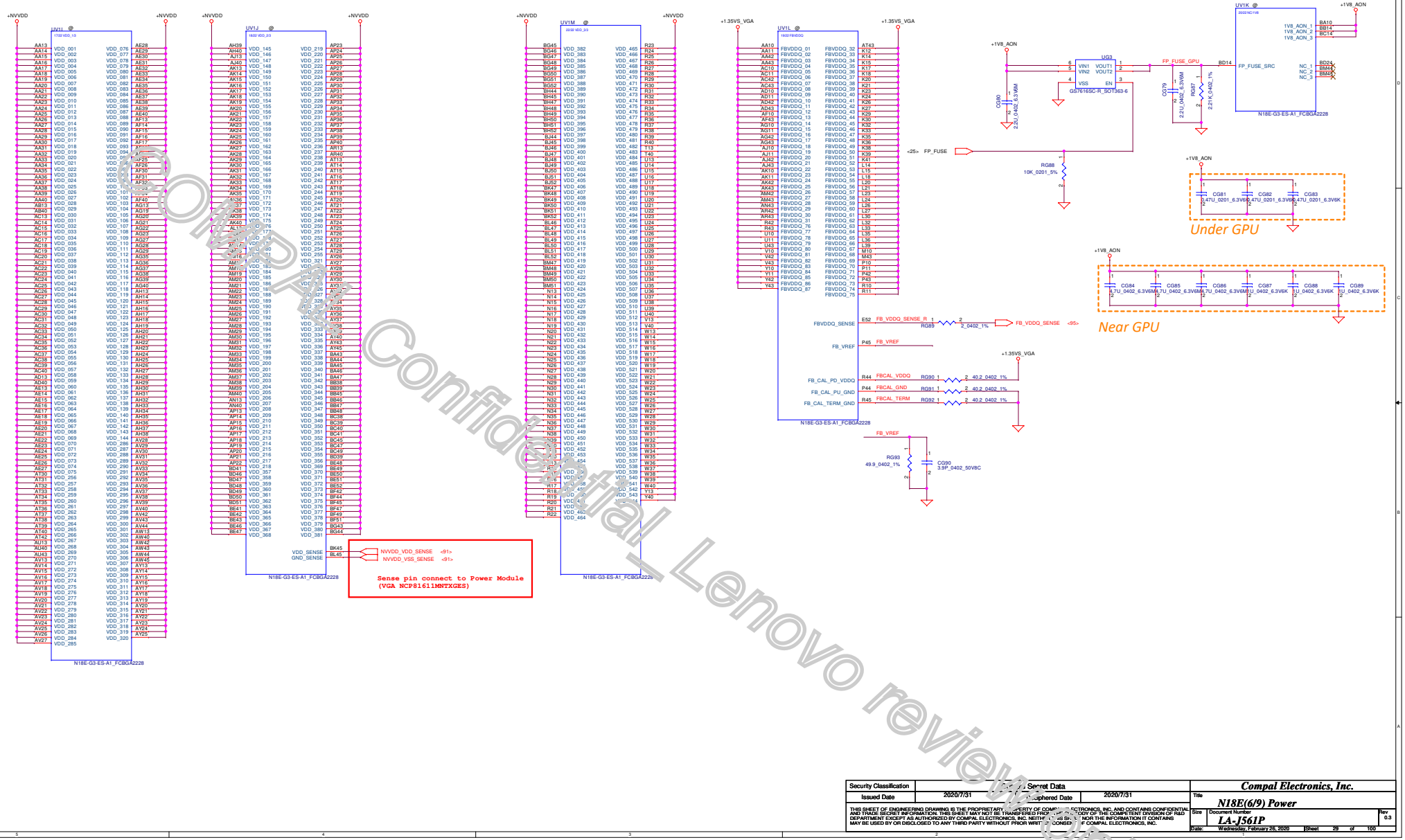

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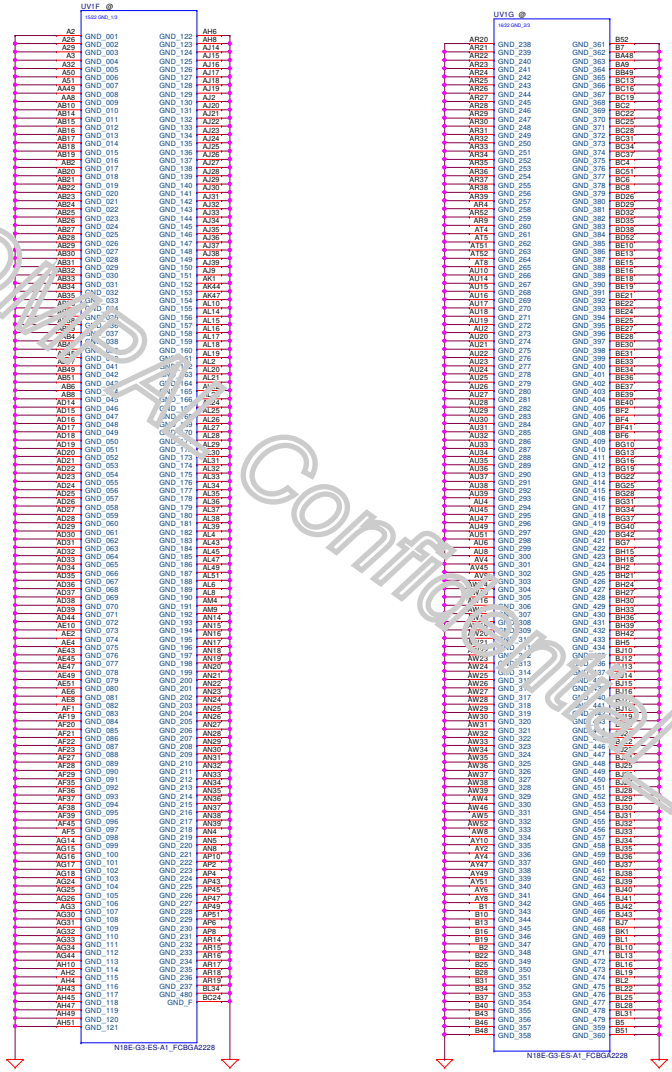

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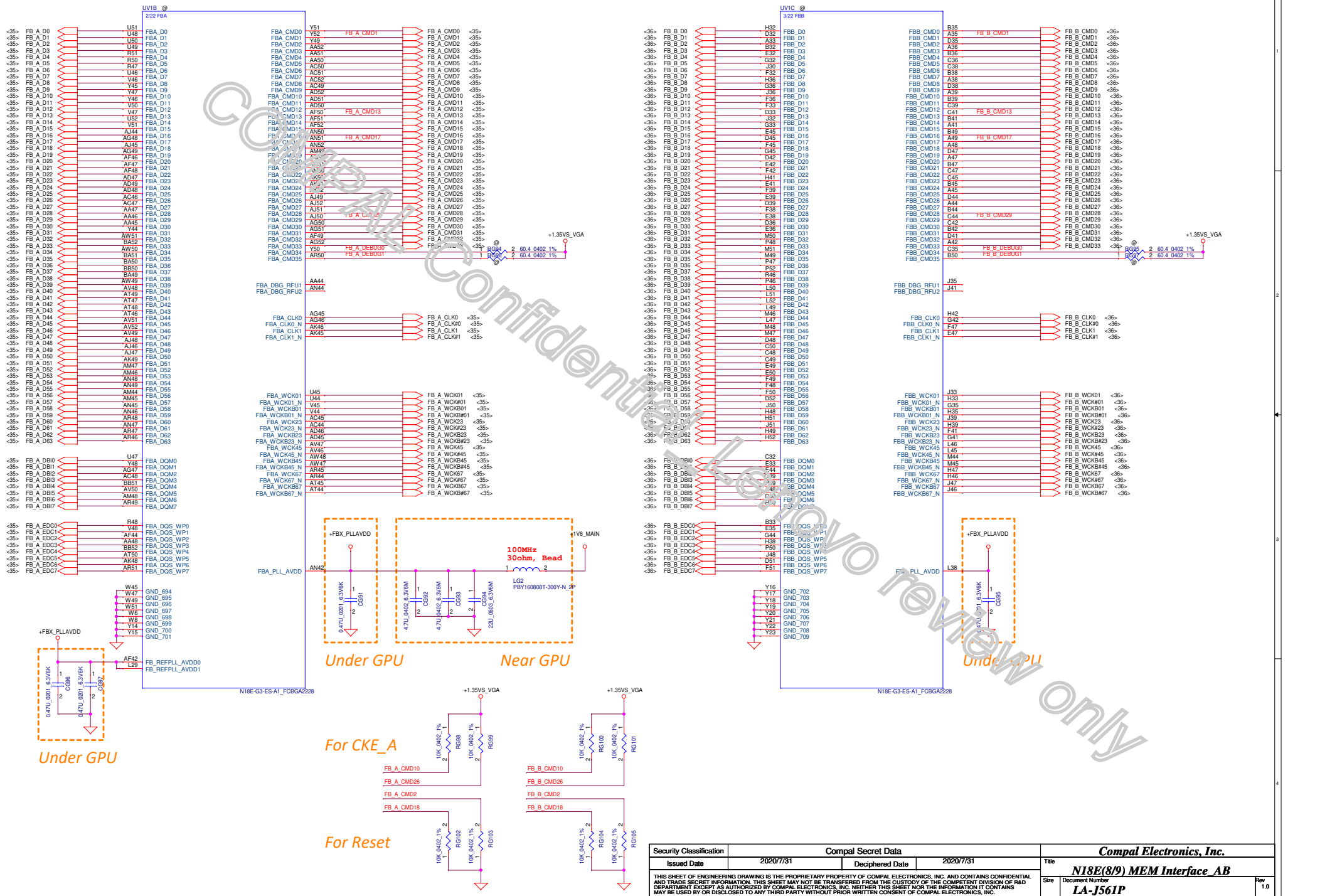

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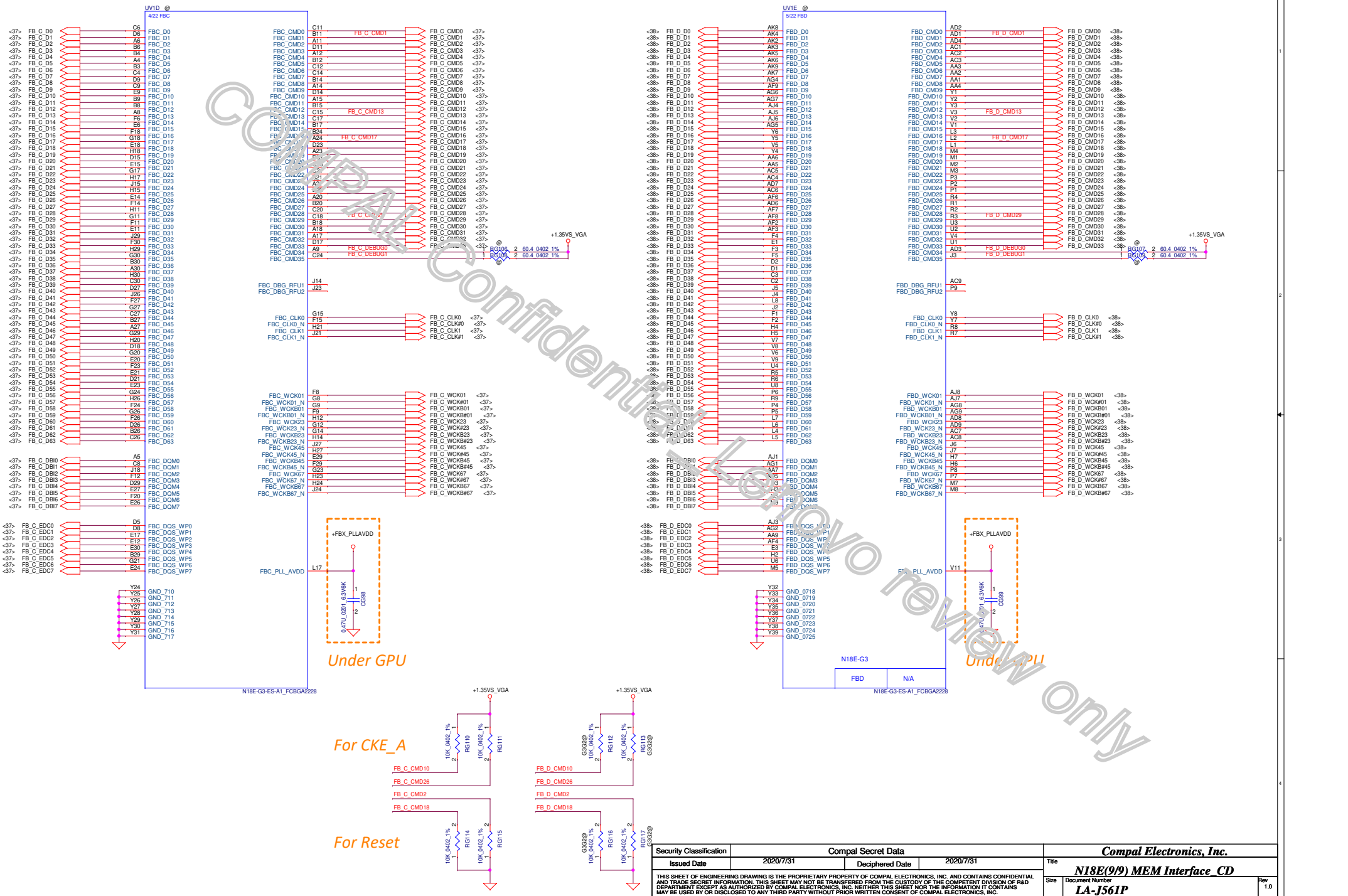

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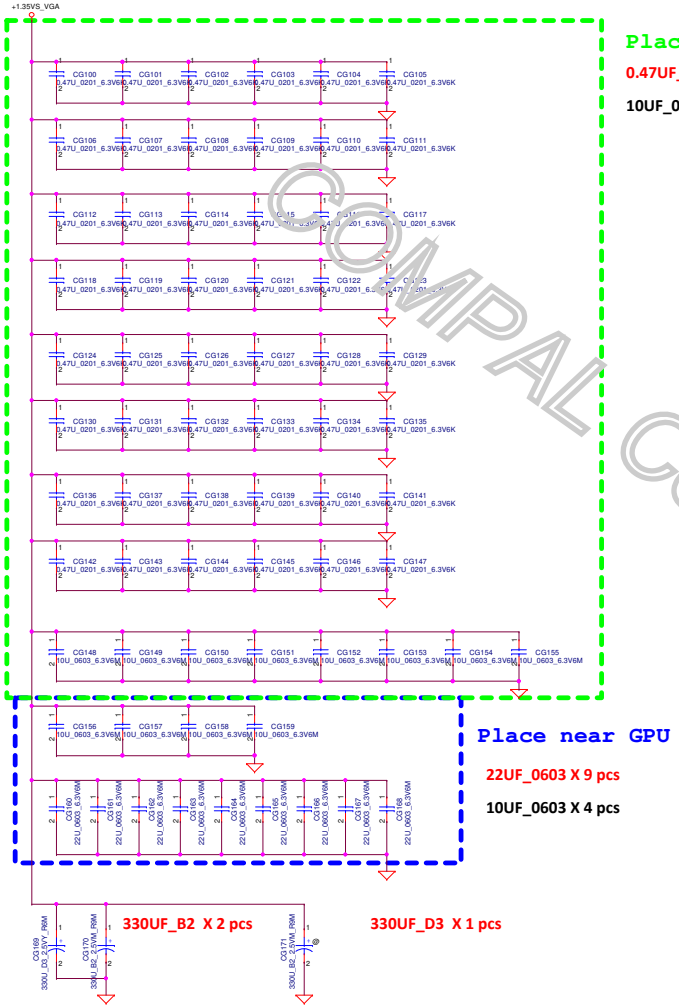
GPU Decoupling - NV Spec Recommendation

FBVDDQ_GPU



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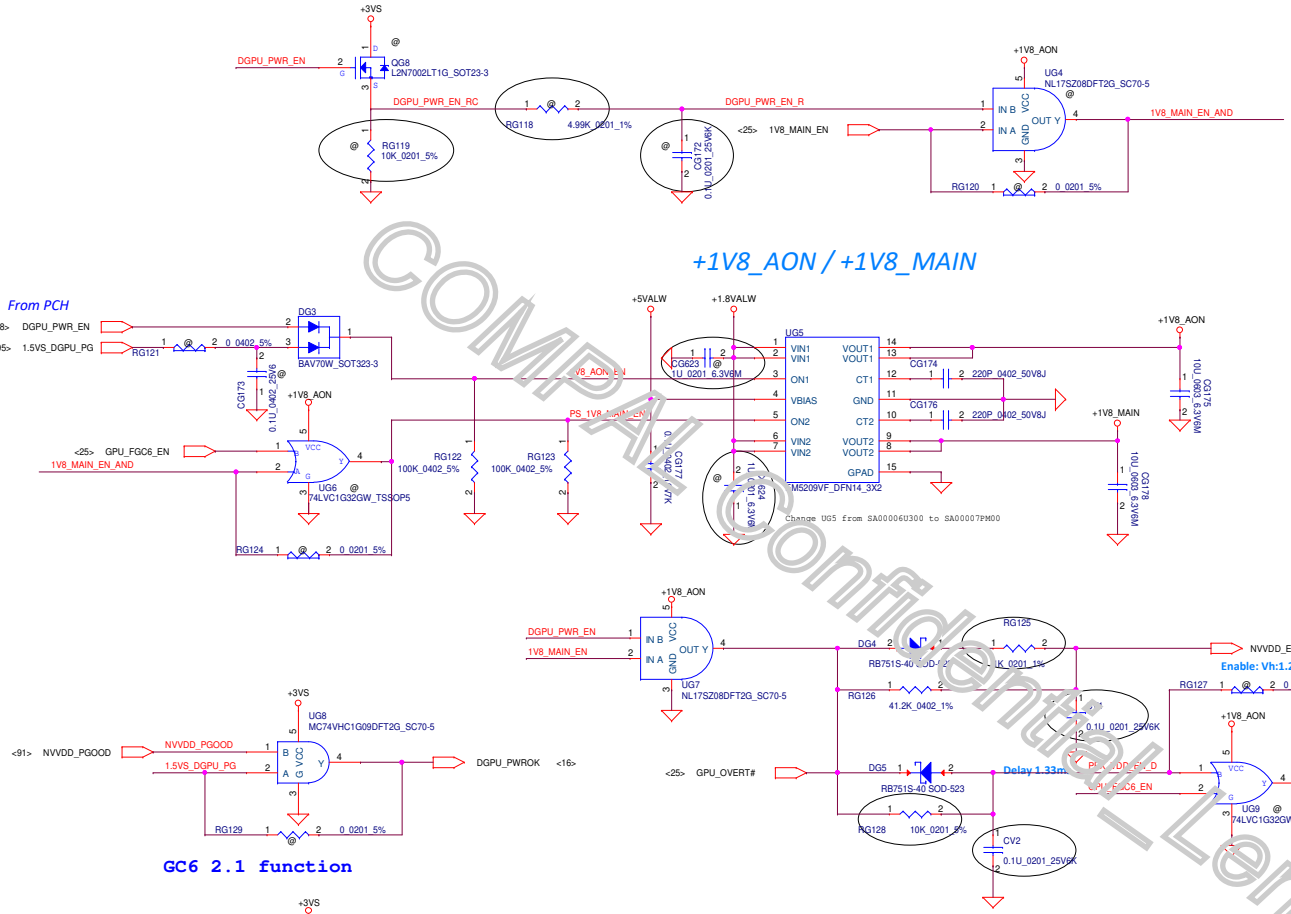

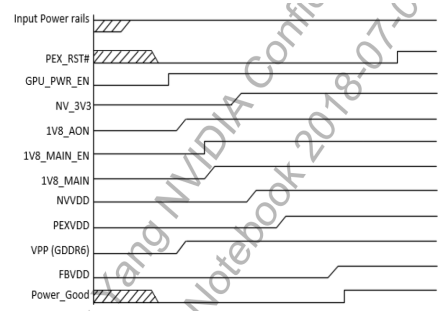

Figure 5.6 Power-Up Sequence

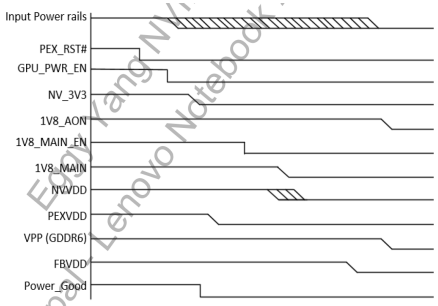

Figure 5.7 Power-Down Sequence

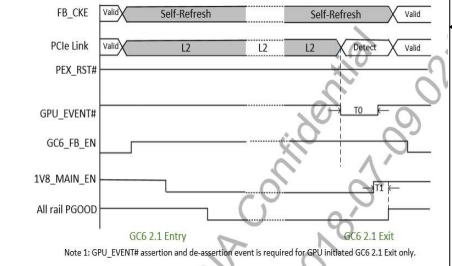

Figure 6.12 GC6 2.1 Entry/Exit Sequence Timing Diagram

	1V8_AON	1V8_MAIN	NVVDD	PEXVDD	FBVDD
GC6 2.1	ON	OFF	OFF	OFF	ON
FGC6	ON	ON	OFF	ON	ON

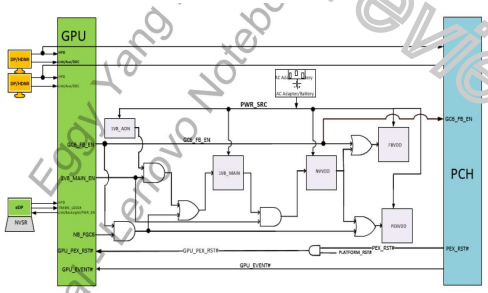

Figure 6.11 FGC6 Block Diagram

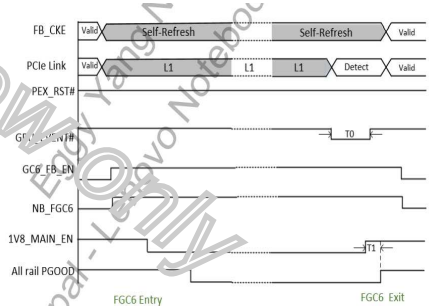

Figure 6.13 FGC6 Entry /Exit Timing Diagram

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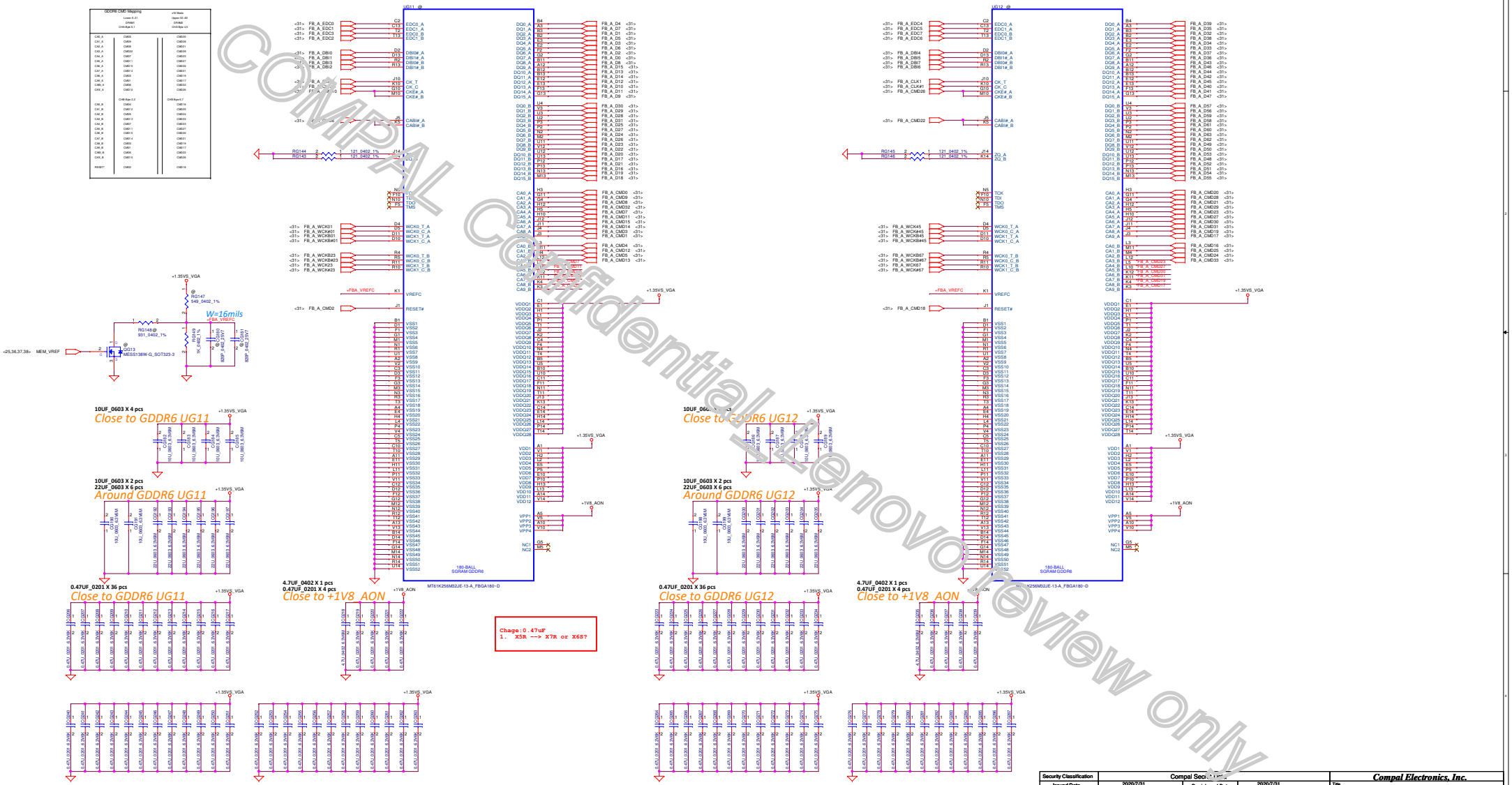
VRAM A



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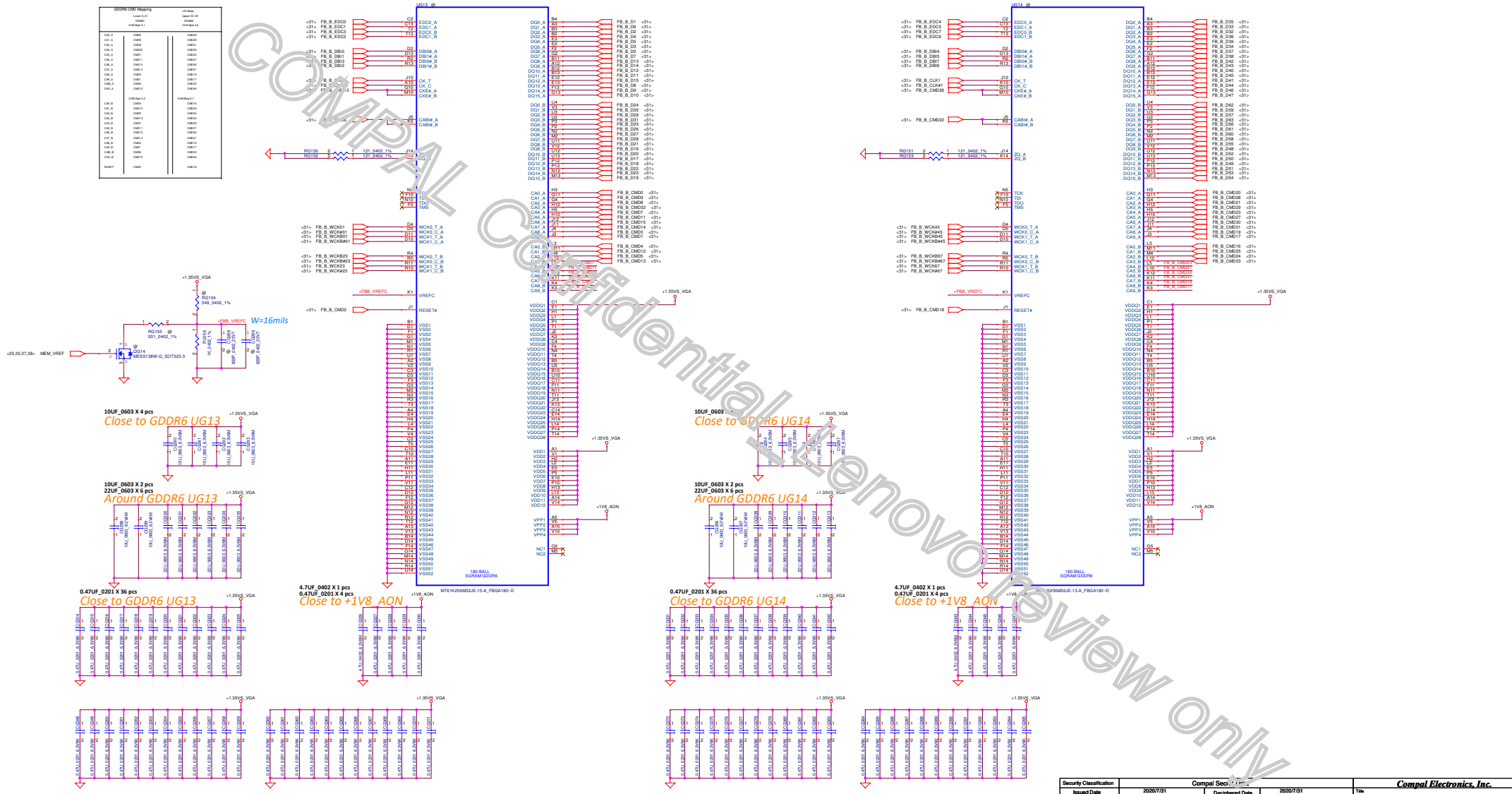
VRAM B



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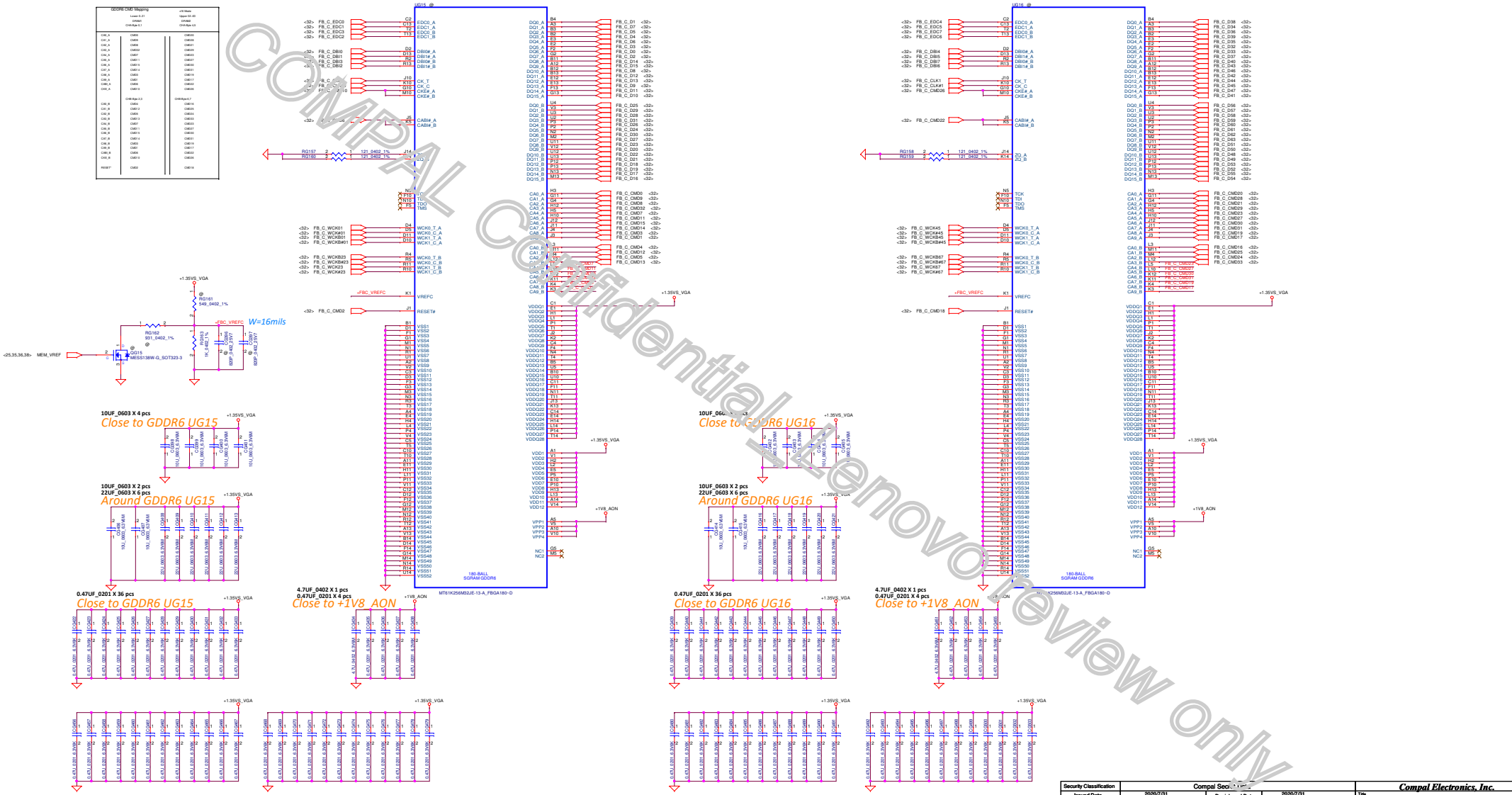
VRAM C



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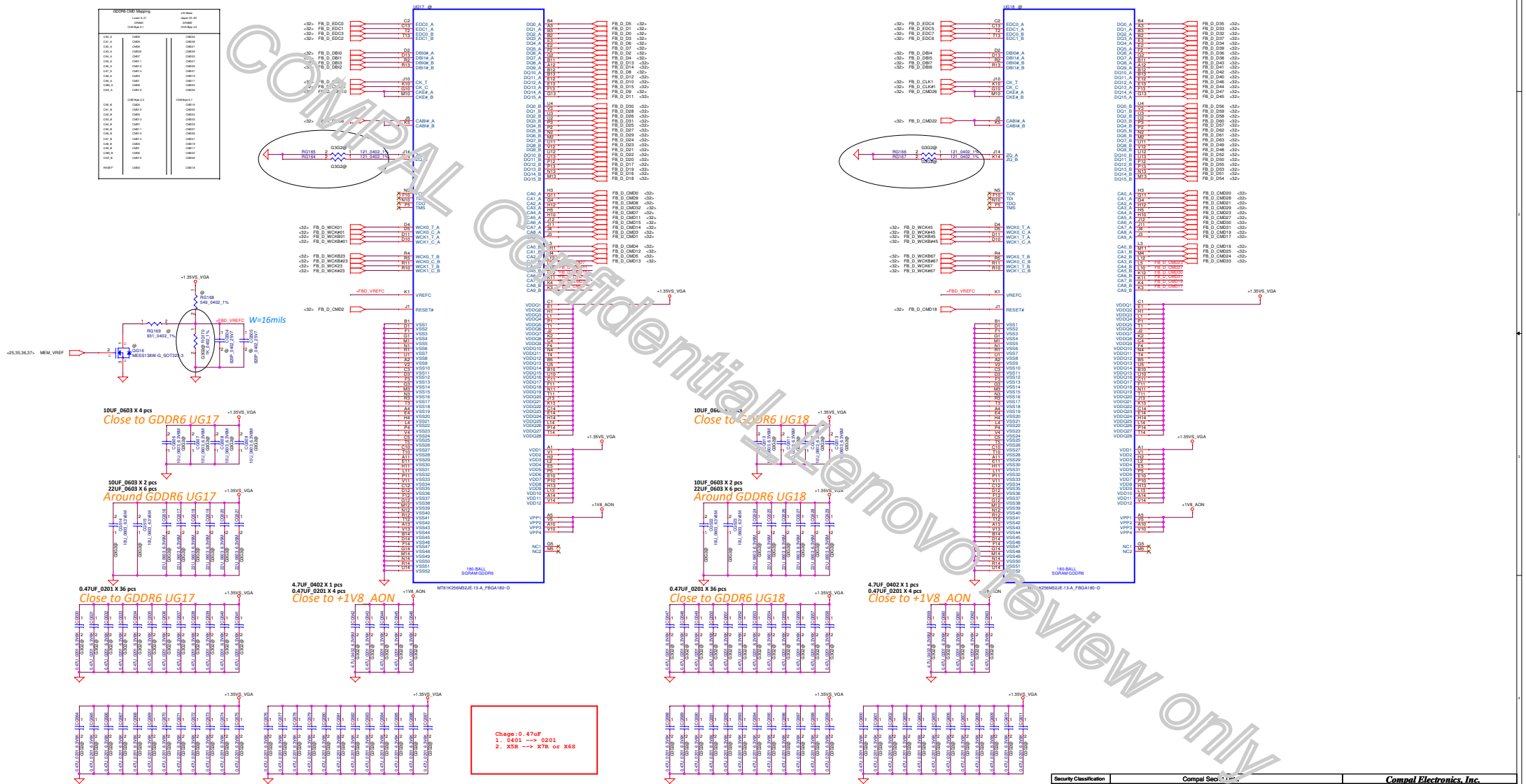

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			Title: GDDR6_D_CH2
			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 38 of 100

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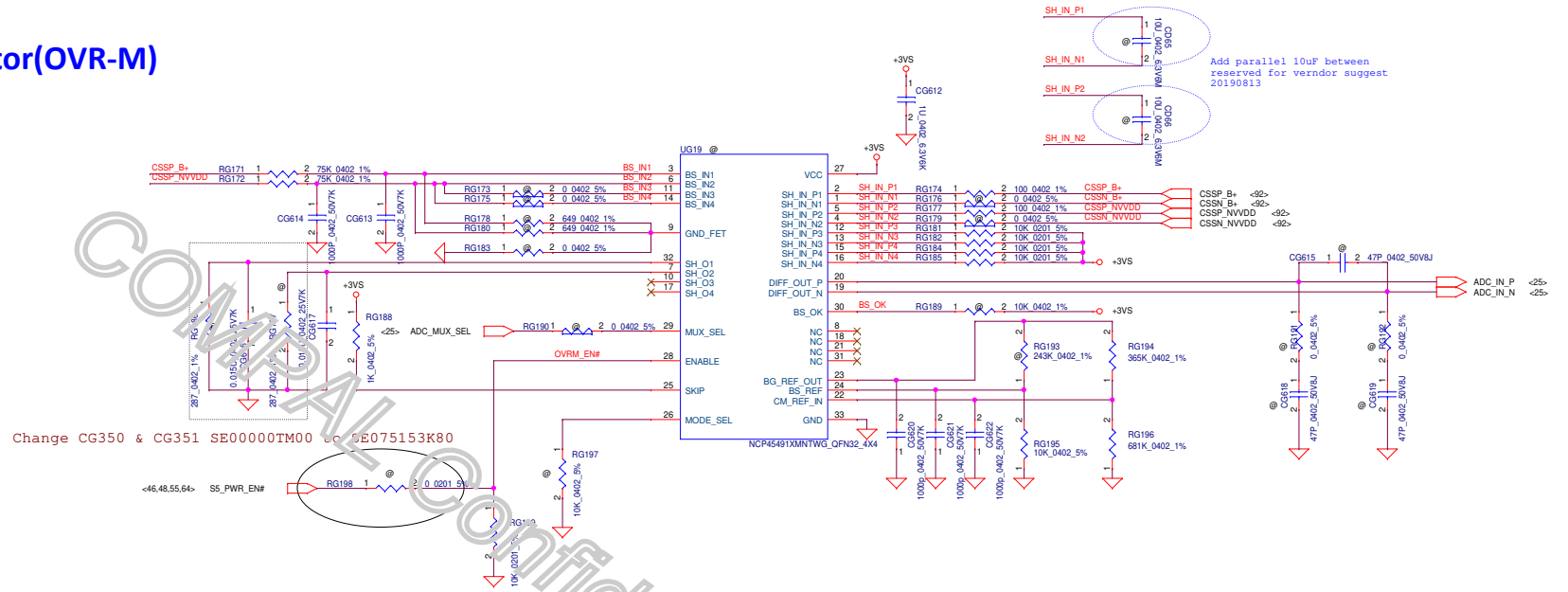
Power Monitor(OVR-M)



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OVR-M(OnSemi)

RG178 ON@ — ON — 649_0402_1%
RG180 ON@ — ON — 649_0402_1%
UG19 ON@ — ON — NCP45492 — SA0000CQX00
RG186 ON@ — ON — 287_0402_1%
RG187 ON@ — ON — 287_0402_1%
RG193 ON@ — ON — 243K_0402_1%

OVR-M(UPI)

RG178 UPI@ — UPI — 487_0402_1%
RG180 UPI@ — UPI — 487_0402_1%
UG19 UPI@ — UPI — US5650QQKI — SA0000CMA00
RG186 UPI@ — UPI — 215_0402_1%
RG187 UPI@ — UPI — 215_0402_1%
RG193 UPI@ — UPI — 324K_0402_1%

Table 13. Power Monitoring with OnSemi OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

ON (X7678038L59)		
UG19	SA0000C9Q00	S IC NCP45491XMNTWG QFN 32P MONITOR
RG225, RG226	SD000008O80	S RES 1/16W 649 +-1% 0402
RG222, RG228	SD034287080	S RES 1/16W 287 +-1% 0402
RG242	SD000004200	S RES 1/16W 243K +-1% 0402

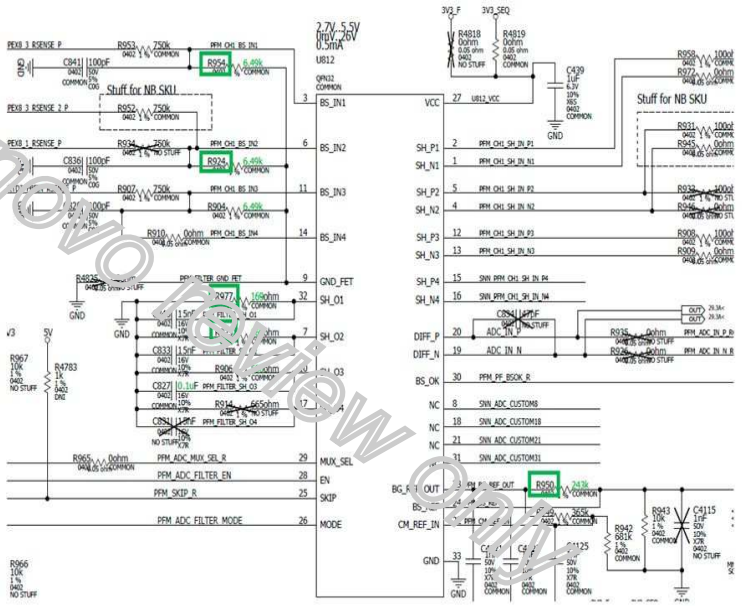
Table 14. Power Monitoring with uPI OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	487 Ω	127 Ω	324 kΩ	75 kΩ	1.0 nF
115W to130W	487 Ω	143 Ω	324 kΩ	75 kΩ	1.0 nF
100W to 110W	487 Ω	165 Ω	324 kΩ	75 kΩ	1.0 nF
75W to 90W	487 Ω	215 Ω	324 kΩ	75 kΩ	1.0 nF
70W or lower	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF

NV location	R954, R924	R977, R923	R950	R953, R952	C841, C836
Y740 location	RG225, RG226	RG222, RG228	RG242	RG259, RG227	CG341, CG342

uPI (X7678038L60)		
UG19	SA0000CEV00	S IC US5650PQKI WQFN 32P POWER MONITOR
RG225, RG226	SD00000EL80	S RES 1/16W 487 +-1% 0402
RG222, RG228	SD000000180	S RES 1/16W 215 +-1% 0402
RG242	SD034324380	S RES 1/16W 324K +-1% 0402

Reference ORB R997 ,R923



igure 1. Power Monitoring with OVR-M

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Title: OVR-M

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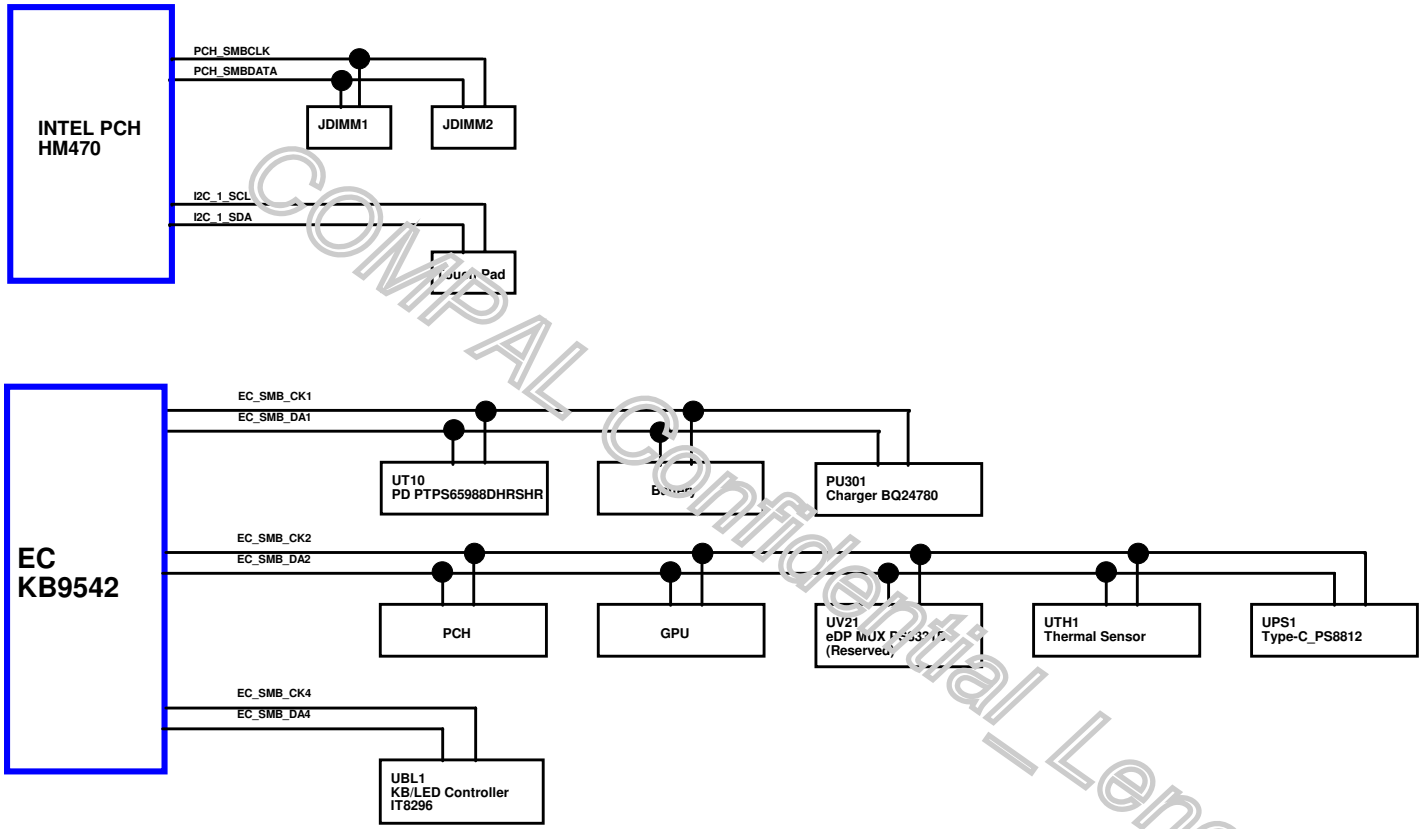
SMBus Block Diagram



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Compal Electronics, Inc.		
Title: TBD		
Size	Document Number: LA-J561P	Rev: 1.0
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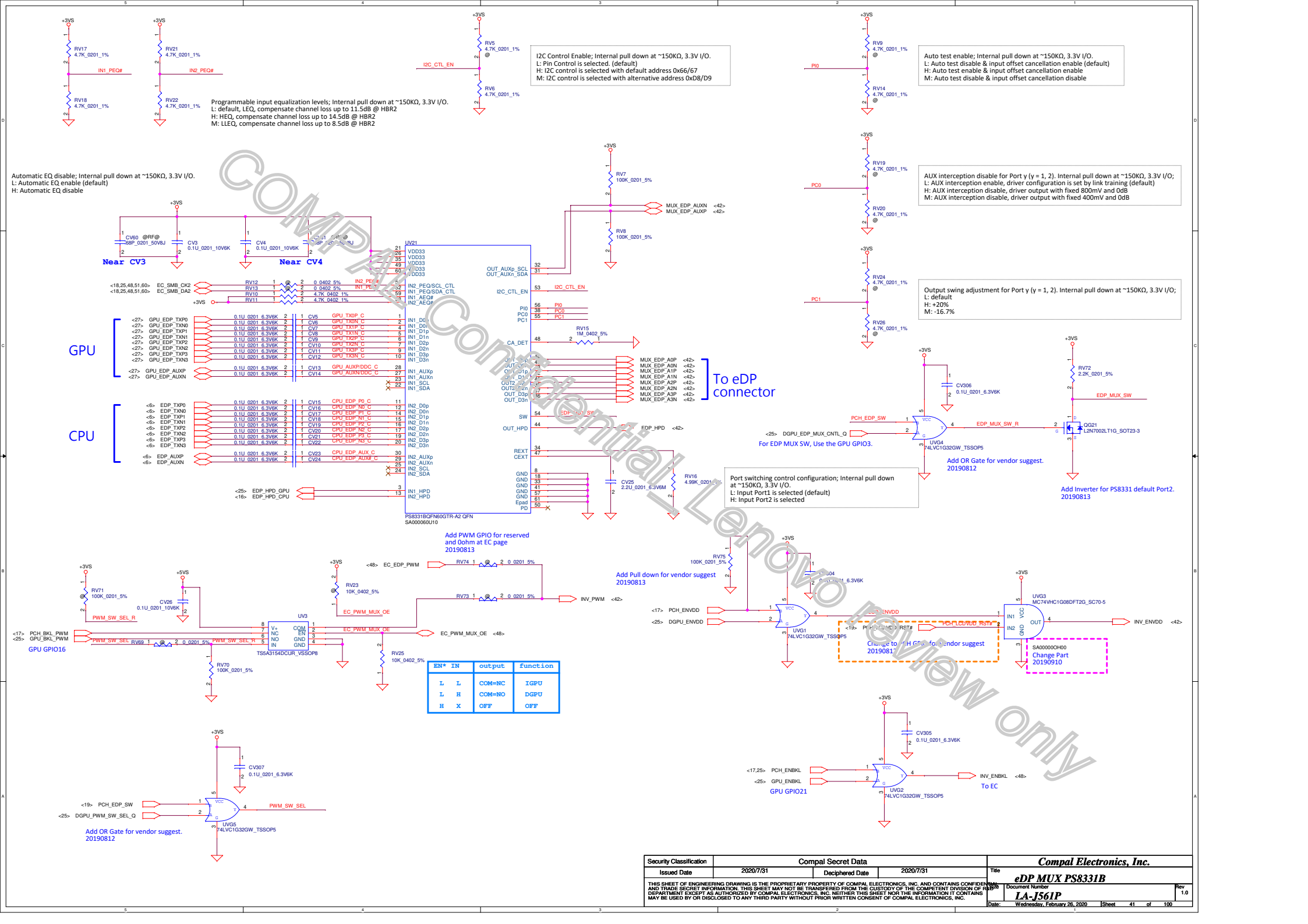
RV17 4.7K_0201_1%
IN1_PEQ#
RV18 4.7K_0201_1%
RV21 4.7K_0201_1%
IN2_PEQ#
RV22 4.7K_0201_1%
Programmable input equalization levels; Internal pull down at ~150KΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2
I2C_CTL_EN
RV5 4.7K_0201_1%
RV6 4.7K_0201_1%
I2C Control Enable; Internal pull down at ~150KΩ, 3.3V I/O.
L: Pin Control is selected. (default)
H: I2C control is selected with default address 0x66/67
M: I2C control is selected with alternative address 0xD8/D9
PI0
RV9 4.7K_0201_1%
RV14 4.7K_0201_1%
Auto test enable; Internal pull down at ~150KΩ, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable
PC0
RV19 4.7K_0201_1%
RV20 4.7K_0201_1%
AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O;
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB
PC1
RV24 4.7K_0201_1%
RV26 4.7K_0201_1%
Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O;
L: default
H: +20%
M: -16.7%
Automatic EQ disable; Internal pull down at ~150KΩ, 3.3V I/O.
L: Automatic EQ enable (default)
H: Automatic EQ disable
Near CV3
Near CV4
CV60 @RF@ 68P_0201_50V8J
CV3 0.1U_0201_10V6K
CV4 0.1U_0201_10V6K
CV61 @RF@ 68P_0201_50V8J
RV7 100K_0201_5%
RV8 100K_0201_5%
MUX_EDP_AUXN <42>
MUX_EDP_AUXP <42>
UV21
PS8331BQFN60GTR-A2 QFN
SA000060U10
VDD33
OUT_AUXp_SCL
OUT_AUXn_SDA
I2C_CTL_EN
PI0
PC0
PC1
CA_DET
RV15 1M_0402_5%
EC_SMB_CK2 <18,25,48,51,60>
EC_SMB_DA2 <18,25,48,51,60>
RV12 0_0402_5%
RV13 0_0402_5%
RV10 4.7K_0402_1%
RV11 4.7K_0402_1%
IN2_PEQ/SCL_CTL
IN1_PEQ/SDA_CTL
IN1_AEQ#
IN2_AEQ#
GPU
GPU_EDP_TXP0 <27>
GPU_EDP_TXN0 <27>
GPU_EDP_TXP1 <27>
GPU_EDP_TXN1 <27>
GPU_EDP_TXP2 <27>
GPU_EDP_TXN2 <27>
GPU_EDP_TXP3 <27>
GPU_EDP_TXN3 <27>
GPU_EDP_AUXP <27>
GPU_EDP_AUXN <27>
GPU_TX0P_C
GPU_TX0N_C
GPU_TX1P_C
GPU_TX1N_C
GPU_TX2P_C
GPU_TX2N_C
GPU_TX3P_C
GPU_TX3N_C
GPU_AUXP/DDC_C
GPU_AUXN/DDC_C
IN1_D0p
IN1_D0n
IN1_D1p
IN1_D1n
IN1_D2p
IN1_D2n
IN1_D3p
IN1_D3n
IN1_AUXp
IN1_AUXn
IN1_SCL
IN1_SDA
CPU
EDP_TXP0 <6>
EDP_TXN0 <6>
EDP_TXP1 <6>
EDP_TXN1 <6>
EDP_TXP2 <6>
EDP_TXN2 <6>
EDP_TXP3 <6>
EDP_TXN3 <6>
EDP_AUXP <6>
EDP_AUXN <6>
CPU_EDP_P0_C
CPU_EDP_N0_C
CPU_EDP_P1_C
CPU_EDP_N1_C
CPU_EDP_P2_C
CPU_EDP_N2_C
CPU_EDP_P3_C
CPU_EDP_N3_C
CPU_EDP_AUX_C
CPU_EDP_AUX#_C
IN2_D0p
IN2_D0n
IN2_D1p
IN2_D1n
IN2_D2p
IN2_D2n
IN2_D3p
IN2_D3n
IN2_AUXp
IN2_AUXn
IN2_SCL
IN2_SDA
EDP_HPD_GPU <25>
EDP_HPD_CPU <16>
IN1_HPD
IN2_HPD
SW
OUT_HPD
EDP_HPD <42>
REXT
CEXT
RV16 4.99K_0201_1%
CV25 2.2U_0201_6.3V6M
GND
Epad
PD
MUX_EDP_A0P <42>
MUX_EDP_A0N <42>
MUX_EDP_A1P <42>
MUX_EDP_A1N <42>
MUX_EDP_A2P <42>
MUX_EDP_A2N <42>
MUX_EDP_A3P <42>
MUX_EDP_A3N <42>
To eDP connector
Port switching control configuration; Internal pull down at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected
Add PWM GPIO for reserved and 0ohm at EC page
20190813
EC_EDP_PWM <48>
RV74 0_0201_5%
RV73 0_0201_5%
INV_PWM <42>
RV23 10K_0402_5%
EC_PWM_MUX_OE
EC_PWM_MUX_OE <48>
RV25 10K_0402_5%
RV71 100K_0201_5%
CV26 0.1U_0201_10V6K
PWM_SW_SEL_R
PCH_BKL_PWM <17>
GPU_BKL_PWM <25>
GPU GPIO16
PWM_SW_SEL RV69 0_0201_5%
PWM_SW_SEL_R
UV3
TS5A3154DCUR_VSSOP8
RV70 100K_0201_5%
EN* IN | output | function
L L | COM=NC | IGPU
L H | COM=NO | DGPU
H X | OFF | OFF
RV75 100K_0201_5%
CV304 0.1U_0201_6.3V6K
PCH_ENVDD <17>
DGPU_ENVDD <25>
UVG1 74LVC1G32GW_TSSOP5
Add Pull down for vendor suggest
20190813
Change to H GPIO for vendor suggest
20190817
UVG3 MC74VHC1G08DFT2G_SC70-5
INV_ENVDD <42>
SA00000OH00
Change Part
20190910
CV306 0.1U_0201_6.3V6K
PCH_EDP_SW
DGPU_EDP_MUX_CNTL_Q <25>
For EDP MUX SW, Use the GPU GPIO3.
UVG4 74LVC1G32GW_TSSOP5
EDP_MUX_SW_R
Add OR Gate for vendor suggest.
20190812
RV72 2.2K_0201_5%
EDP_MUX_SW
QG21 L2N7002LT1G_SOT23-3
Add Inverter for PS8331 default Port2.
20190813
CV307 0.1U_0201_6.3V6K
PCH_EDP_SW <19>
DGPU_PWM_SW_SEL_Q <25>
PWM_SW_SEL
UVG5 74LVC1G32GW_TSSOP5
Add OR Gate for vendor suggest.
20190812
CV305 0.1U_0201_6.3V6K
PCH_ENBKL <17,25>
GPU_ENBKL <25>
GPU GPIO21
INV_ENBKL <48>
To EC
UVG2 74LVC1G32GW_TSSOP5
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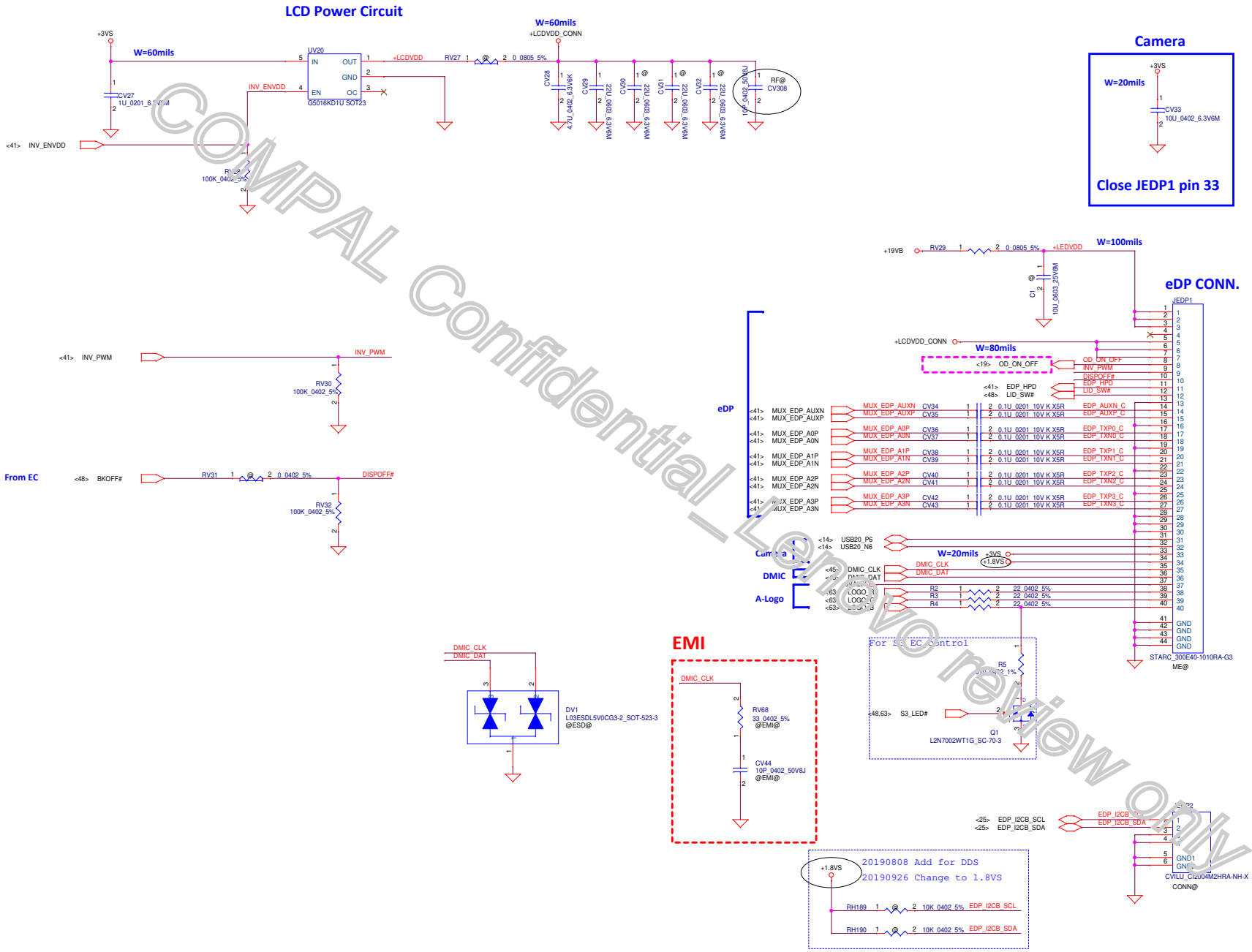
Compal Electronics, Inc.
Title: eDP MUX PS8331B
Size: B
Document Number: LA-J561P
Rev: 1.0
Date: Wednesday, February 26, 2020
Sheet 41 of 100



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Title	eDP / Camera		
Size C	Document Number LA-J561P		Rev 1.0
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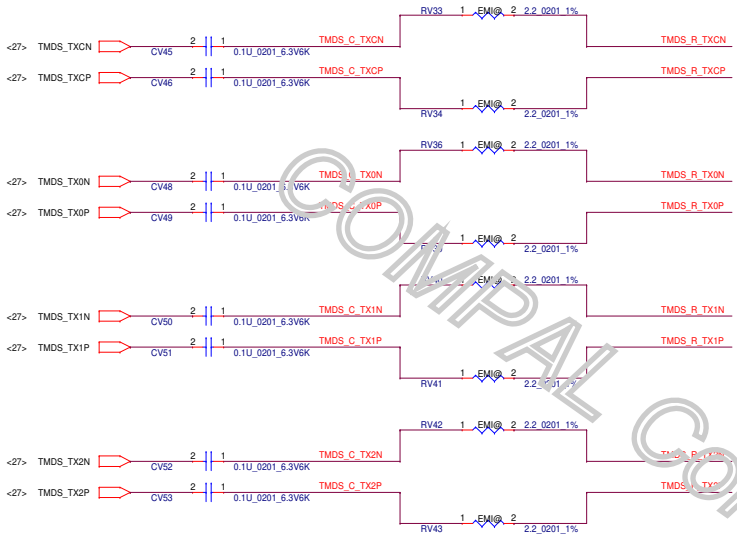
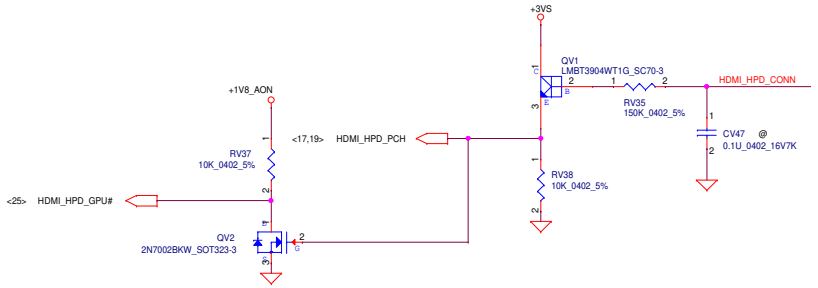
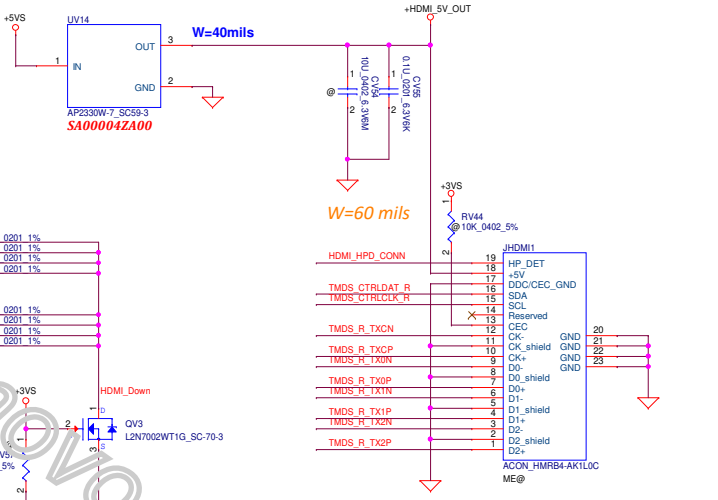
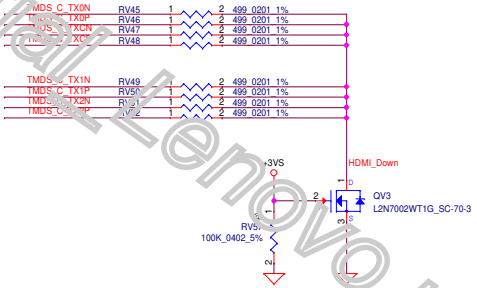
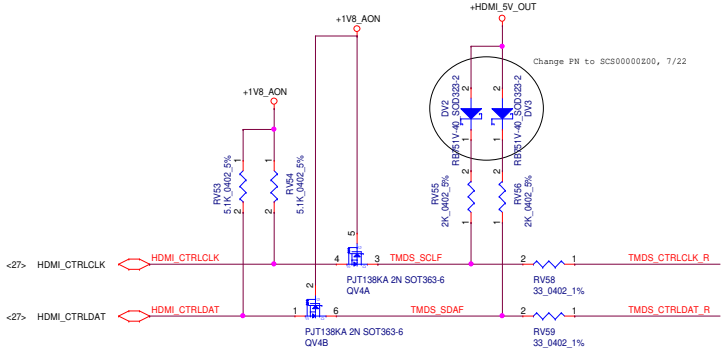


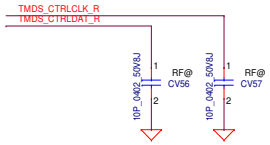








To GPU



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Title: HDMI			
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Title	***Reserved***	
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POWER

For vendor suggest,3.3V change to 1.8V

+5VS, +5VS_AVDD_CODEC, RA2 0_0402_5%, CA27 4.7U_0402_6.3V6K, CA1 0.1U_0201_6.3V6K, CA2 1U_0201_6.3V6M, AGND

CA1, CA27 close UA1 pin 41, 46

CA2 close UA1 pin 46

+1.8VS, +1.8VS_AVDD_CODEC, RA3 0_0402_5%, CA3 2.2U_0402_6.3V6M, AGND

CA3 close UA1 pin 20

+1.8VS, +1.8VS_DVDD_CODEC, RA4 0_0402_5%, CA4 1U_0201_6.3V6M, CA5 1U_0201_6.3V6M

CA4 close UA1 pin 3

CA5 close UA1 pin 18

ALC3306

The AMP is 1.8V, so the DVDD should be 1.8V.
DVDD >= DVDDIO

RA14 chamge to @, because pin2 is fo internal AMP control.

I2C DATA and CLK add 0 ohm for KB Light.

To eDP CONN

To PCH

UA1 ALC3306-CG

I2SEN/SPDIFOUT/GPIO2/DMICDATA34
PDB
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
I2C_DATA
I2C_CLK
I2S_IN
I2S_OUT
I2S_BCLK
I2S_MCLK/GPIO3
I2S_LRCK
DC_DET/EAPD
BCLK
SYNC
SDATA-IN
SDATA-OUT
LDO3-CAP
LDO2-CAP
CPVEE
CBN2
CBP2
Thermal PAD
CP1
CN1
CP2
CN2
HPOUT-R
HPOUT-L
MIC2-VREFO-L
MIC2-VREFO-R
MIC2-R/SLEEVE
MIC2-CAP
PCBEEP
VREF
LDO1-CAP
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R-
SPK-OUT-R+
JD1(HP JD)
GPIO4/JD2(I2S-IN/I2S-OUT JD)
AVSS2
AVSS1

ALC3306-CG_MQFN48P_6X6

For vendor suggest, RA21 change to @.

+1.8VS_DVDD_CODEC, RA25 2.2K_0402_5%, AUDIO_SMCLK0, RA26 2.2K_0402_5%, AUDIO_SMDAT0

+1.8VS, RA29 100K_0402_5%, SWF_SDZ_R, RA31 100K_0402_5%, SMA_IRQ#, RA33 200K_0402_1%

CA22 22P_0402_50V8J @EMI@ I2S_BCLK_SA
CA23 22P_0402_50V8J @EMI@ I2S_DOUT_SA
CA24 22P_0402_50V8J @EMI@ I2S_LRCK_SA

place close audio codec

Audio Jack (close Audio codec)

09/18 update to +1.8VS_DVDD_CODEC

place close audio codec

+1.8VS_DVDD_CODEC, RA1 100K_0402_1%, RA5 200K_0402_1%, PLUG_IN_R, PLUG_IN

Combo Jack (Normal Open)

+MIC2-VREFO_R, +MIC2-VREFO_L, RA6 2.2K_0402_5%, RA7 2.2K_0402_5%

W=40mils
W=40mils

MIC2_SLEEVE, MIC2_RING2, HP_OUTL, HP_OUTR

EMI

RA8, RA9, RA10, RA11 BLM15BD121SN1D_2P, 47_0402_5%

HGNDB, HGNDA, HPOUT_L, HPOUT_R

CA6 470P_0402_50V7K EMI@
CA7 470P_0402_50V7K EMI@
CA8 220P_0402_50V7K EMI@
CA9 220P_0402_50V7K EMI@

AGND

JHP1 SINGA_2SJ3095-215111F CONN@

#3 M/G
#1 L
#5
#6
#2 R
#4 G/M

HP-Out-Right
HP-Out-Left
Ring2
Sleeve

08/02 update

DA1 PESD5V0U2BT_SOT23-3 ESD@
DA2 S ZEN ROW L03ESDL5V6CC3-2 C/A SOT-23 ESD @ESD@

ESD for Audio

EC Beep

<48> BEEP#
<18,19,48> SPKR

RA22 47K_0402_5%
RA23 47K_0402_5%

place close audio codec

BEEP_IN, CA20 1U_0201_6.3V6M, PC_BEEP
CA21 100P_0402_50V8J @ESD@
RA24 27K_0402_5%
AGND

EMI

RA27, RA28, RA30, RA32 0_0402_5%

GND, AGND

CA25 EMI@ 0.1U_0201_10V6K
CA26 EMI@ 0.1U_0201_10V6K

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Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

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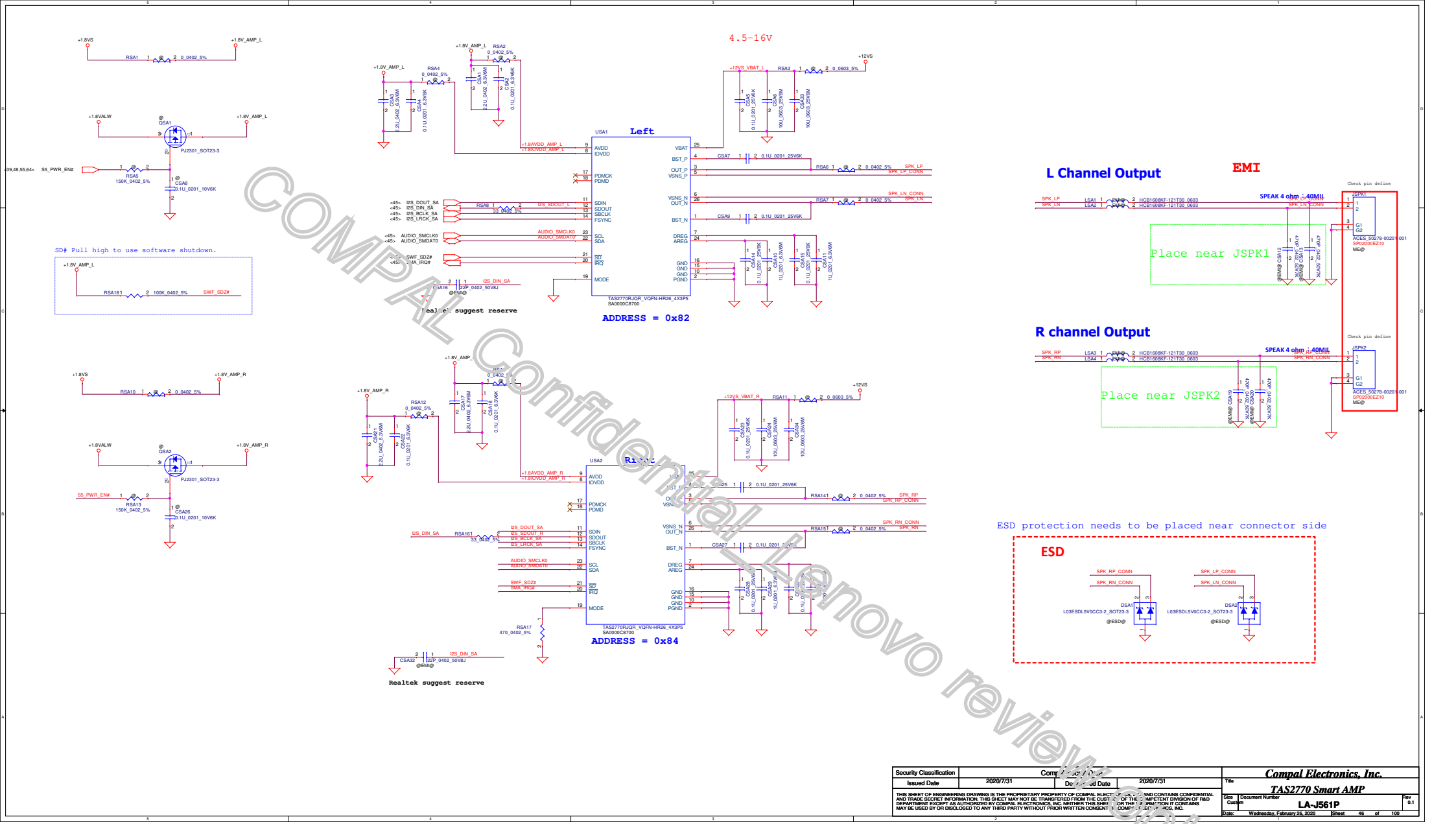
Compal Electronics, Inc.	
Title	HD Audio Codec_ALC3268
Size: Custom	Document Number: LA-J561P
Rev	0.1
Date: Wednesday, February 26, 2020	Sheet 45 of 100



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Security Classification	Compal Confidential	Compal Electronics, Inc.	
Issued Date	2020/7/31	Deciphered Date	2020/7/31
Title	TAS2770 Smart AMP		
Size	Document Number	Rev	
Custom	LA-J561P	0.1	
Date:	Wednesday, February 26, 2020	Sheet	46 of 100

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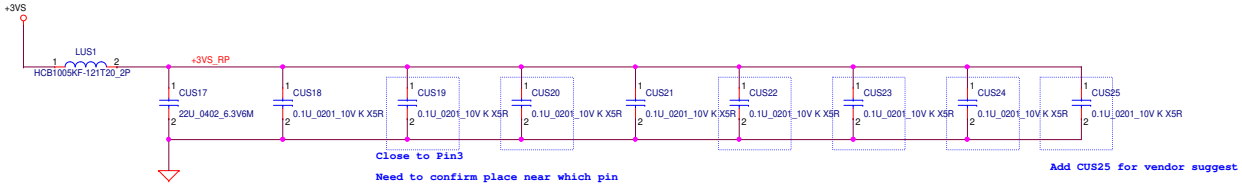
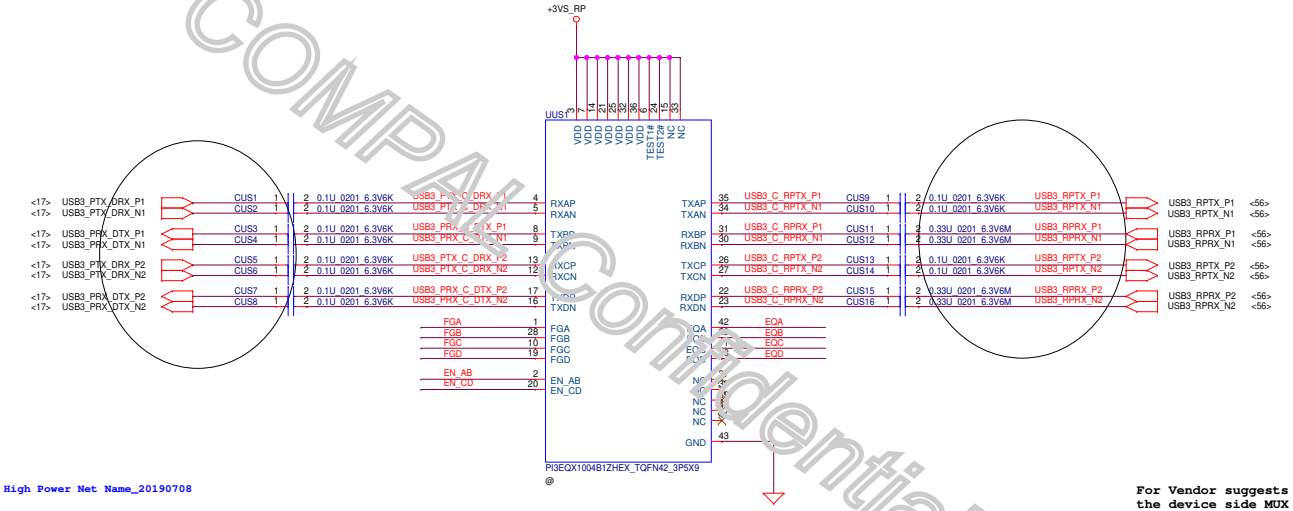
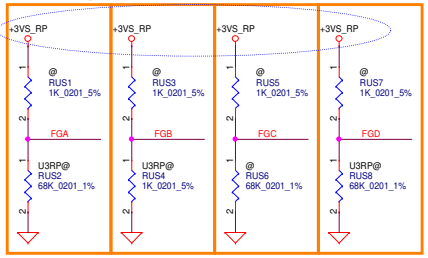




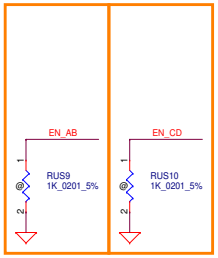
Update Pull High Power Net Name_20190708

For Vendor suggests the RC can provide
the device side MUX tolerance enough to 3.3V DC level or not.
RUS19, RUS20, RUS21 and RUS22 = 200kohm.
CUS11, CUS12, CUS15 and CUS16 = 0.33uF.

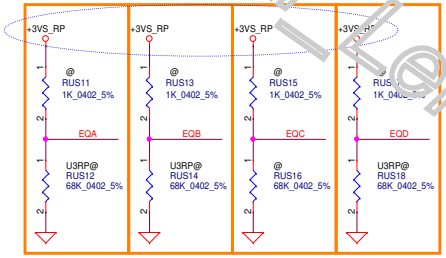
DC flat gain selection

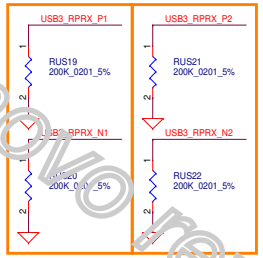


Channel Enable



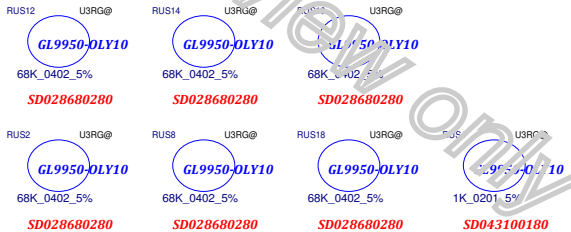
EQ selection





Waiting for Layout TLC to set up EQ anf Gain value.

Post-channel / Pre-channel	less than 2inch		2inch to 4inch		up to 4inch	
For PI3EQX1004/B1	TX	RX	TX	RX	TX	RX
under 7inch	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Pull low to GND	EQA=68kohm to GND FGA=Floating	EQB=Floating FGB=Pull low to GND
7inch to 9inch	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=Floating	EQA=Floating FGA=Floating	EQB=Floating FGB=Floating
up to 12inch	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Pull low to 68kohm	EQB=68kohm to GND FGB=1kohm to VDD	EQA=1kohm to VDD FGA=Floating	EQB=Floating FGB=1kohm to VDD



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: USB3.1 GEN2 Redriver
			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 47 of 100

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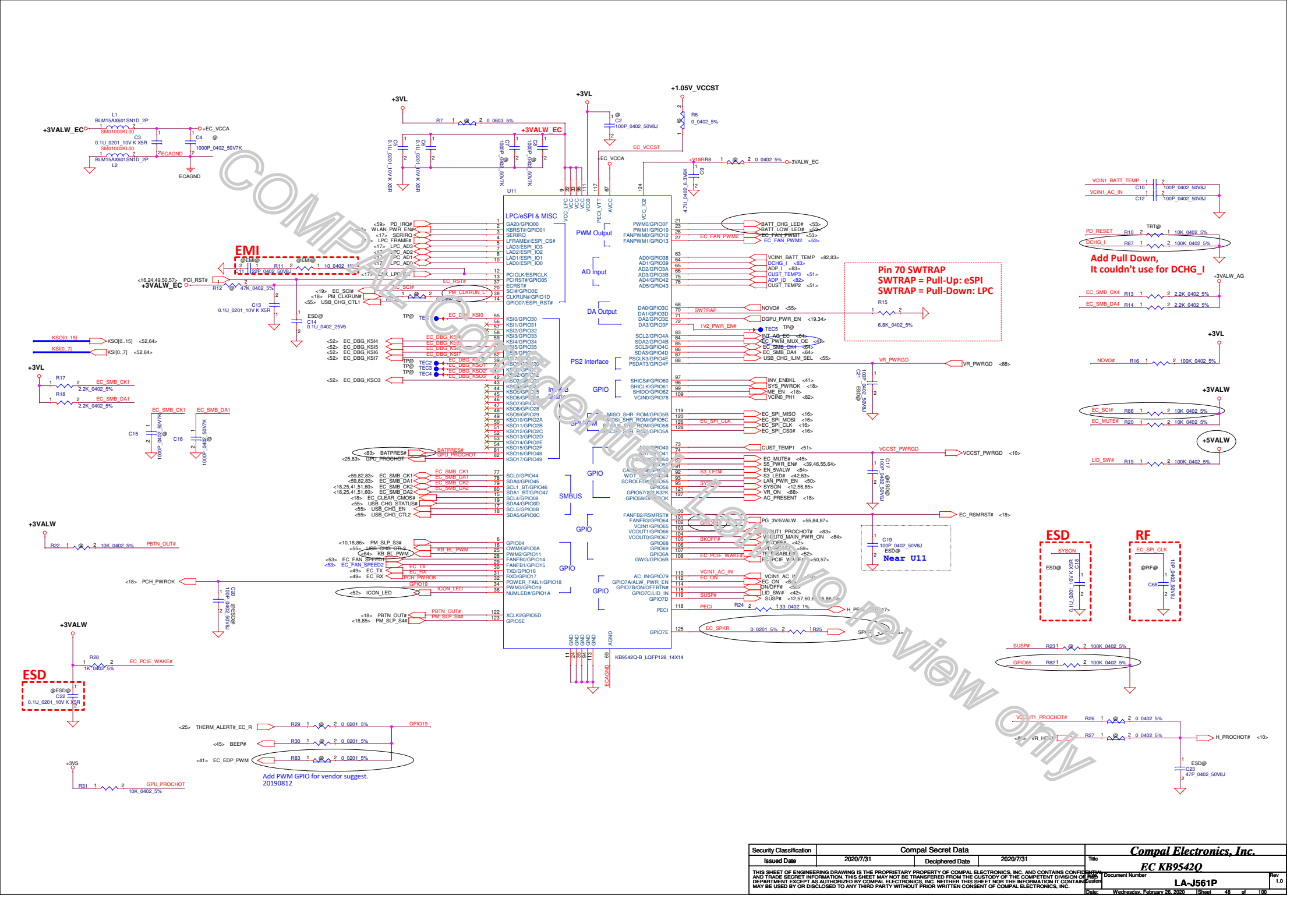

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Compal Electronics, Inc.			
Title: EC KB9542Q			
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 48 of 100		

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

For Power consumption Measurement

Harrison Peak:800mA@peak current

KEY E

422.18mA

USB2 P14 (For Bluetooth)

CNVi Rx

PCIe X1 (link to PICe Port 14)

PCIe CLK (From PCH CLKOUT3)

CNVi

For CNVi Feature

Close to KEY E pin2,4

Close to KEY E pin72,74

The connectivity module power supply pin shall be connected directly to thr rail DSW.
From
567240_Intel_Wireless_AC_9560_Jefferson_Peak_EPS_Rev1.1

Follow 566468_CNL_UY_PDG_Rev0p73.pdf

KEY M for 15" only SSD

NGFF SSD1 (KEY M)

PCIE X4 (link to PICE Port 21~24)

PCIE CLK (From PCH CLKOUT1)

For Power consumption Measurement

Close to JSSD1 KEY M pin2,4

1129 symbol changed

NGFF SSD2 (KEY M)

PCIE X4 (link to PICE Port 9~12)

PCIE CLK (From PCH CLKOUT5)

For Power consumption Measurement

Close to JSSD2 KEY M pin2,4

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: WLAN(KEY E)/SSD(KEY M)
			Size: Document Number: LA-J561P Rev: 1.0
			Date: Wednesday, February 26, 2020 Sheet 49 of 100

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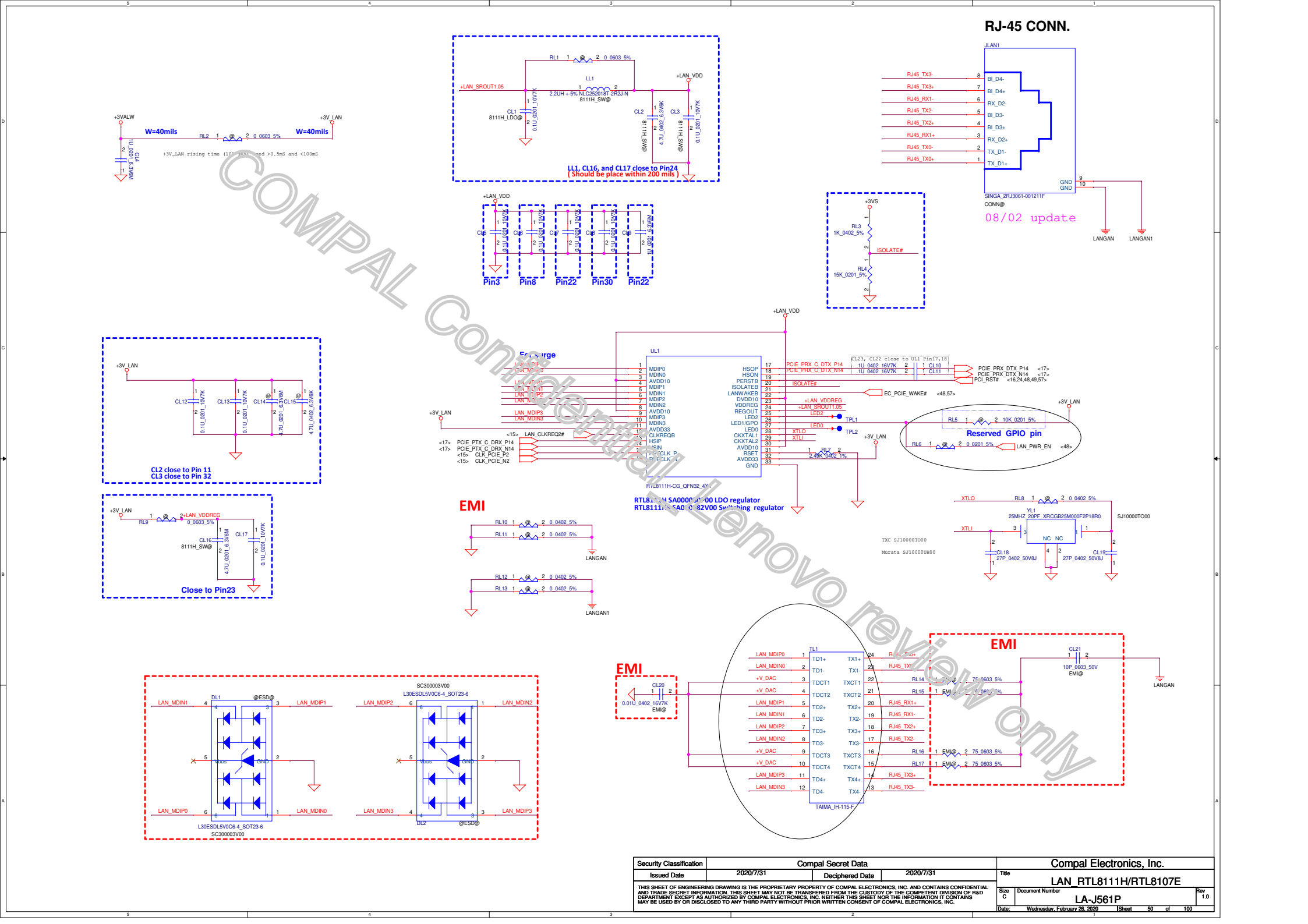

Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

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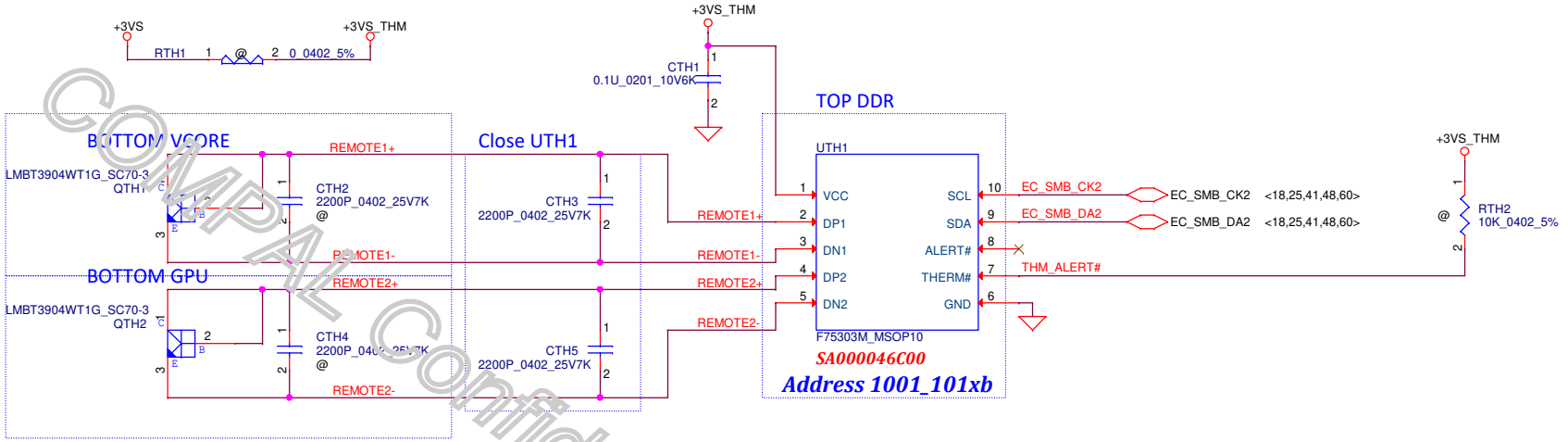
Compal Electronics, Inc.

Title: LAN_RTL8111H/RTL8107E

Size	Document Number	Rev
C	LA-J561P	1.0

Date: Wednesday, February 26, 2020 Sheet 50 of 100

THERMAL SENSOR For Smart Performance



REMOTE1,2 (+/-) :
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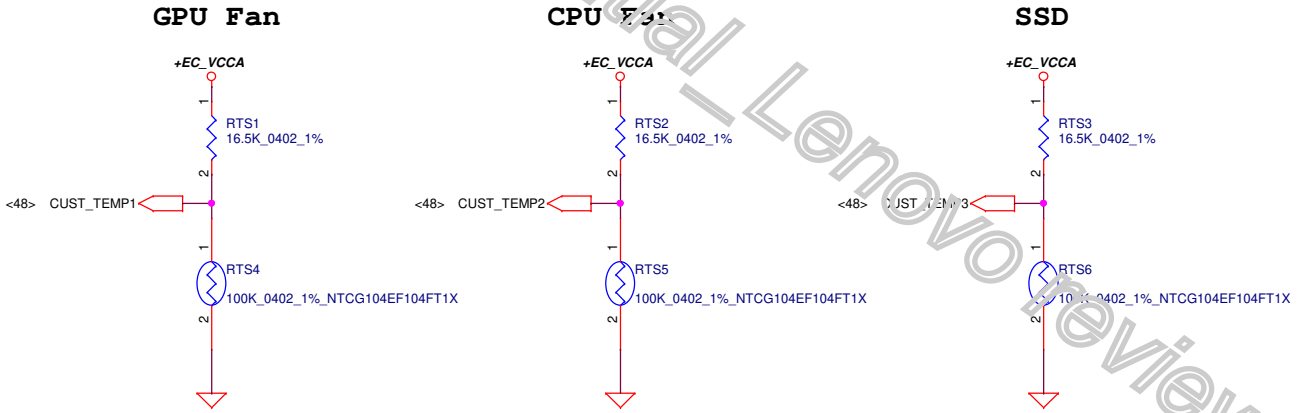
Trace length:<8"



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Compal Electronics, Inc.			
Title: Thermal Sensor			
Size: B	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 51 of 100		

Bom Structure

Coffee Lake-H CPU SKU

UC1 CPU1@ CML-H
CML-H ES 65W QTJ0
SA0000D3G10

UC1 CPU2@ CML-H
CML-H ES 45W QTJ1
SA0000D3I10

UC1 CPU3@ CML-H
CML-H ES 45W QTJ2
SA0000D3N10

Cannn Lake PCH HM370

UH1 PCH1@ Pre-QS
HM470 QUCJ
SA0000DDP20

PCB

ZZZ2 PCB@
PCB FLY00 LA-J561P LS-J561P
DAZ2VH00201

VRAM 6G

ZZZ M6G@
MT61K256M32JE-14:A
X7685138L01

ZZZ S6G@
K4Z80325BC-HC14
X7685138L02

ZZZ MICR_6@ VRAM
MT61K256M32JE-14:A
SA0000BND60

ZZZ SAM_6@ VRAM
K4Z80325BC-HC14
SA0000C6260

VRAM 8G

ZZZ M8G@
MT61K256M32JE-14:A
X7685138L03

ZZZ S8G@
K4Z80325BC-HC14
X7685138L04

ZZZ MICR_8@ VRAM
MT61K256M32JE-14:A
SA0000BND60

ZZZ SAM_8@ VRAM
K4Z80325BC-HC14
SA0000C6260

X4E_15

ZZZ X4E_15@
EMC EE AJ561 FLY00
X4EAKK38L01

U3 GEN2 re-driver

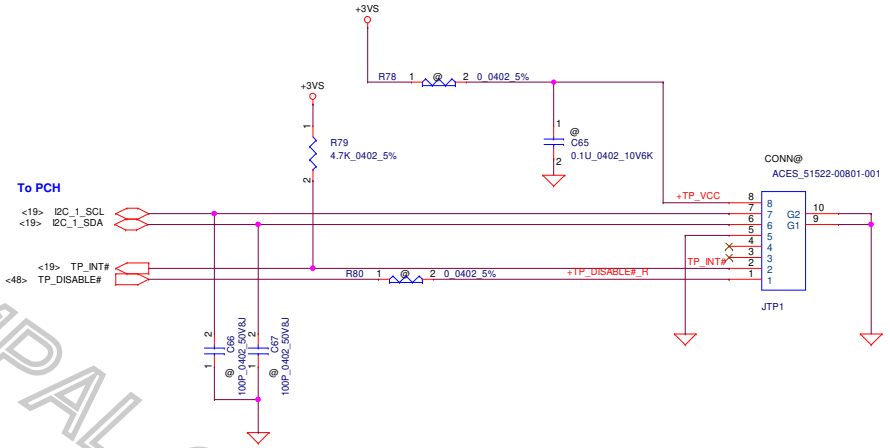
ZZZ PERICOM@
PI3EQX1004B1ZHEX
X7685138L07

ZZZ1 GENESYS@
GL9950-OLY10
X7685138L08

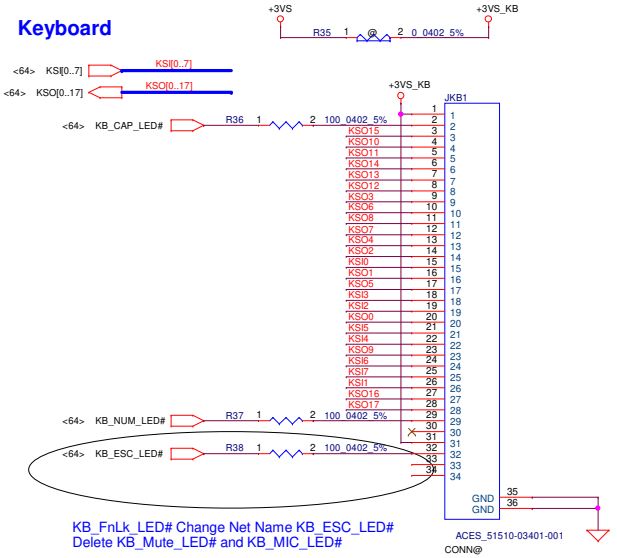
UUS1 U3RP@
PI3EQX1004B1ZHEX
SA0000CEM00

UUS1 U3RG@
GL9950-OLY10
SA0000D5Q00

Touch Pad

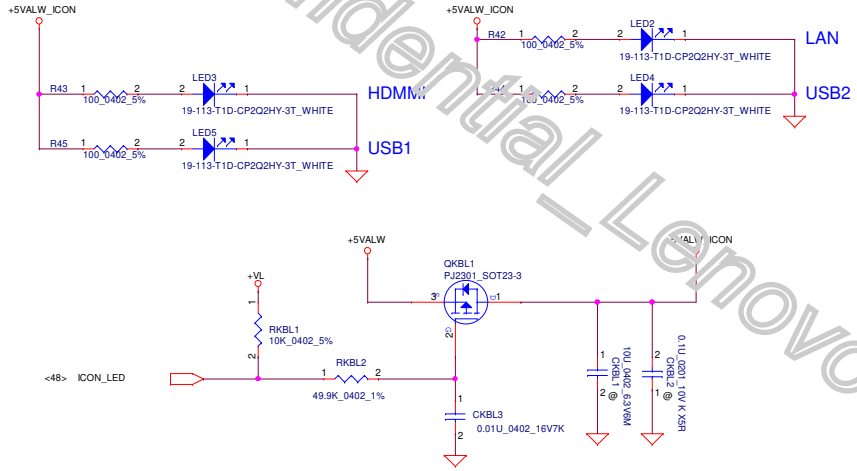


Keyboard

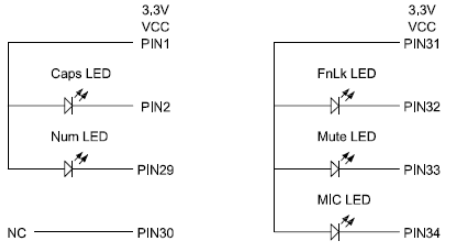


KB_FnLk_LED# Change Net Name KB_ESC_LED#
Delete KB_Mute_LED# and KB_MIC_LED#

Icon LED



KB LED



Nvidia GPU SKU

UV1 GPU1@ 1660Ti-G0-R1
N18E-G0-A1
SA0000CK420

UV1 GPU2@ 2060-G1-R1
N18E-G1-B-KD-A1
SA0000DDK10

UV1 GPU3@ 2070-G2-R1
N18E-G2-A1
SA0000CCX30

UV1 GPU4@ 2080-G3-R1
N18E-G3-A1
SA0000CD540

UV1 GPU5@ 2060-G1R-R1
N18E-G1R-MP-A1
SA0000D4N50

UV1 GPU6@ 2070-G2R-R1
N18E-G2R-A1
SA0000D4M30

UV1 GPU7@ 2080-G3R-R1
N18E-G3R-A1
SA0000D4L20

0911 update

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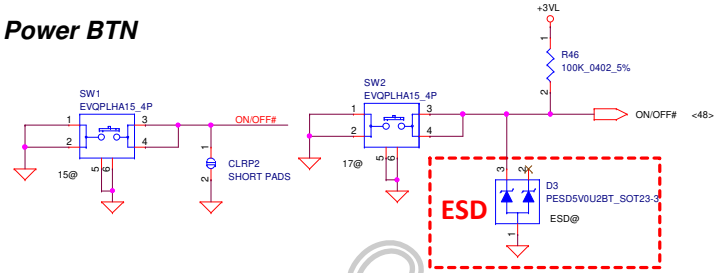
Compal Electronics, Inc.	
Title	KB/TP/LID/BOM S.
Size	Document Number: LA-J561P
Rev	1.0
Date: Thursday, February 27, 2020	Sheet 52 of 100

Power BTN

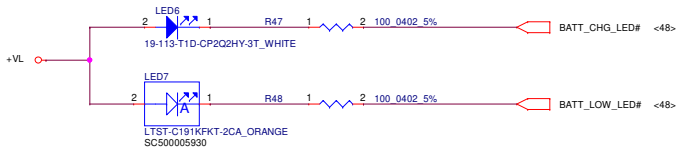


For 15"

For 17"

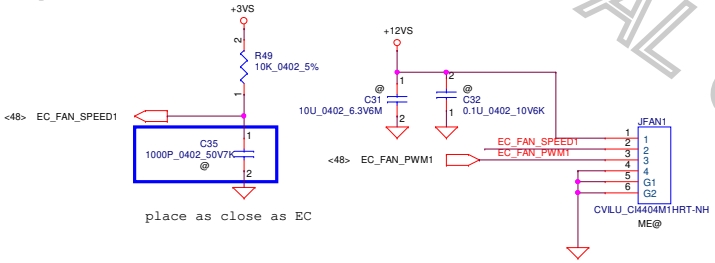
Change P/N SCA02900 to SCA00000T00

DCIN LED



CPU Fan Control Circuit

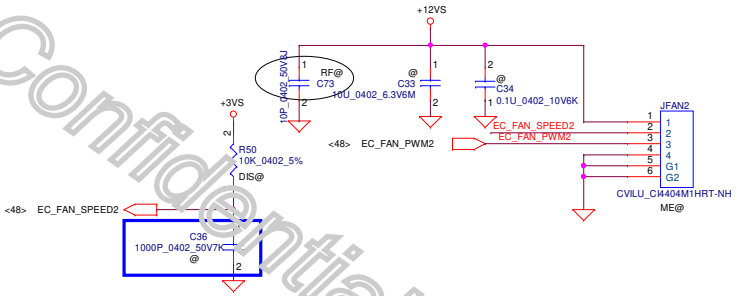
Right Side



place as close as EC

GPU Fan Control Circuit

Left Side



place as close as EC

PCB

ZZZ

LA-J561P

DAB0005X000

Screw Hole

H9 HOLEA H_3P3
H10 HOLEA H_2P5
H11 HOLEA H_2P5
H12 HOLEA H_2P5N
H14 HOLEA H_2P5N
H16 HOLEA H_2P5N
H19 HOLEA H_2P5
H20 HOLEA H_2P5

CPU/GPU Thermal Standoff

H7 HOLEA H_3P2 **WLAN**
H8 HOLEA H_3P2 **SSD**
H1 HOLEA H_3P3
H2 HOLEA H_3P3
H3 HOLEA H_3P3
H4 HOLEA H_3P3
H5 HOLEA H_3P3
H6 HOLEA H_3P3

Fiducial Mark

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

DDR Shielding Clip

Larger

CLIP1 @ HOLEA_35A2M
CLIP2 @ HOLEA_35A2M
CLIP3 @ HOLEA_35A2M

Smaller

CLIP6 @ HOLEA_12A2M
CLIP7 @ HOLEA_12A2M
CLIP8 @ HOLEA_12A2M
CLIP9 @ HOLEA_12A2M
CLIP10@ HOLEA_12A2M
CLIP15@ HOLEA_12A2M
CLIP11@ HOLEA_12A2M
CLIP4 @ HOLEA_12A2M
CLIP5 @ HOLEA_12A2M
CLIP12@ HOLEA_12A2M
CLIP13@ HOLEA_12A2M
CLIP14@ HOLEA_12A2M

Position Hole

H13 HOLEA H_2P9N
H15 HOLEA H_2P5N
H17 HOLEA H_2P3X2P8N
H18 HOLEA H_2P3X2P8N

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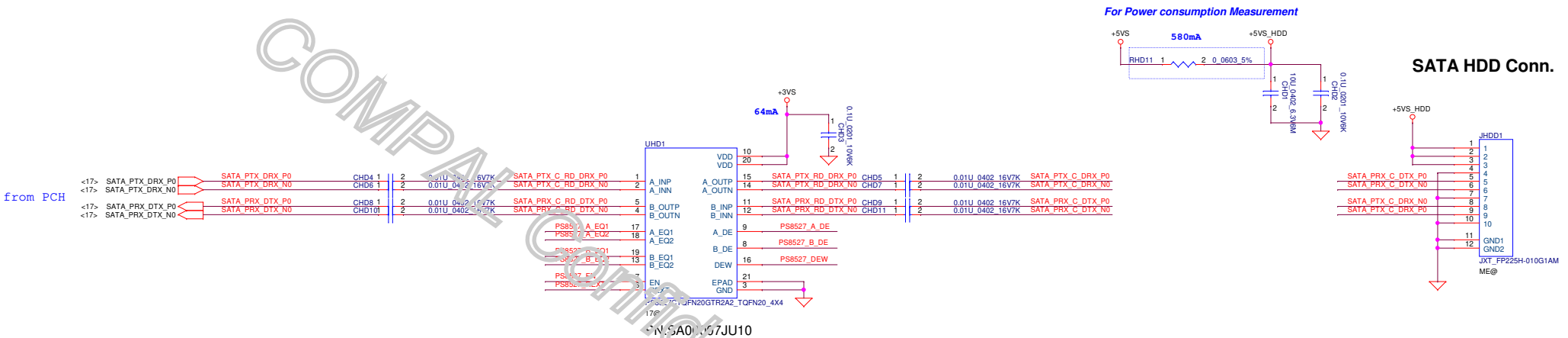
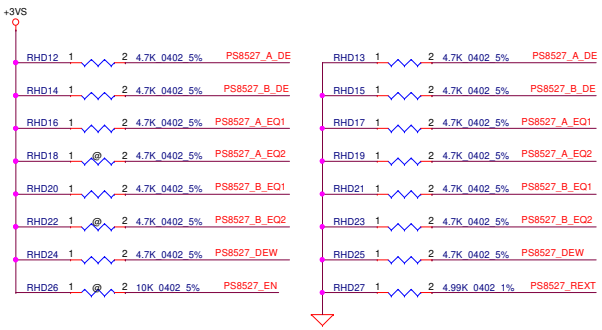
Title	FAN/LED/PBTN/PCB PN/SCREWS		
Size	Document Number		Rev
	LA-J561P		0.3
Date	Wednesday, February 26, 2020	Sheet	53 of 100

SATA HDD





Equalizer control and program for channel A.

Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

De-emphasis width setting for channel A& B .

Internally tied to VDD/2(M status).

DEW	DE pulse duration optimized for
M	SATA 6Gbp/s(default)
L	SATA 6Gbp/s
H	SATA 3Gbp/s

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Issued Date	2020/7/31	Deciphered Date	2020/7/31

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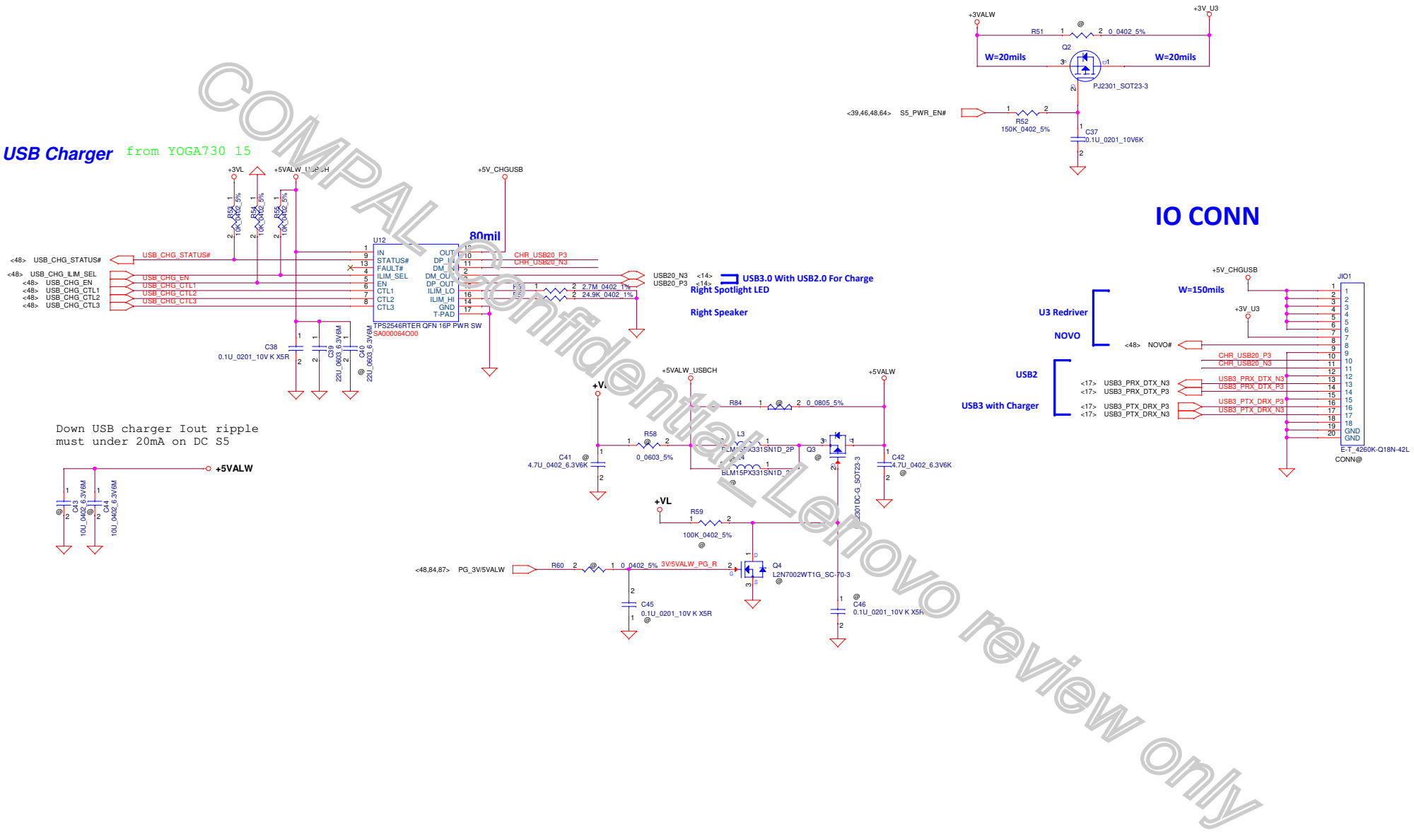
Compal Electronics, Inc.			
Title: HDD Connector			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 54 of 100		



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Issued Date	2020/7/31	Deciphered Date	2020/7/31

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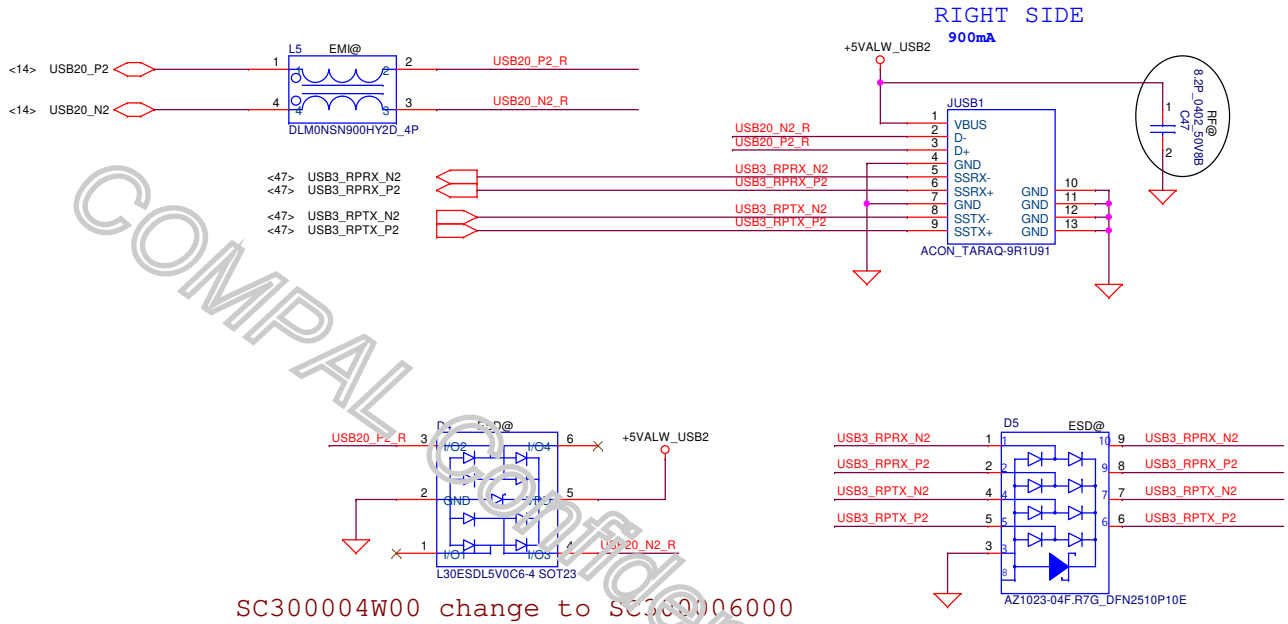
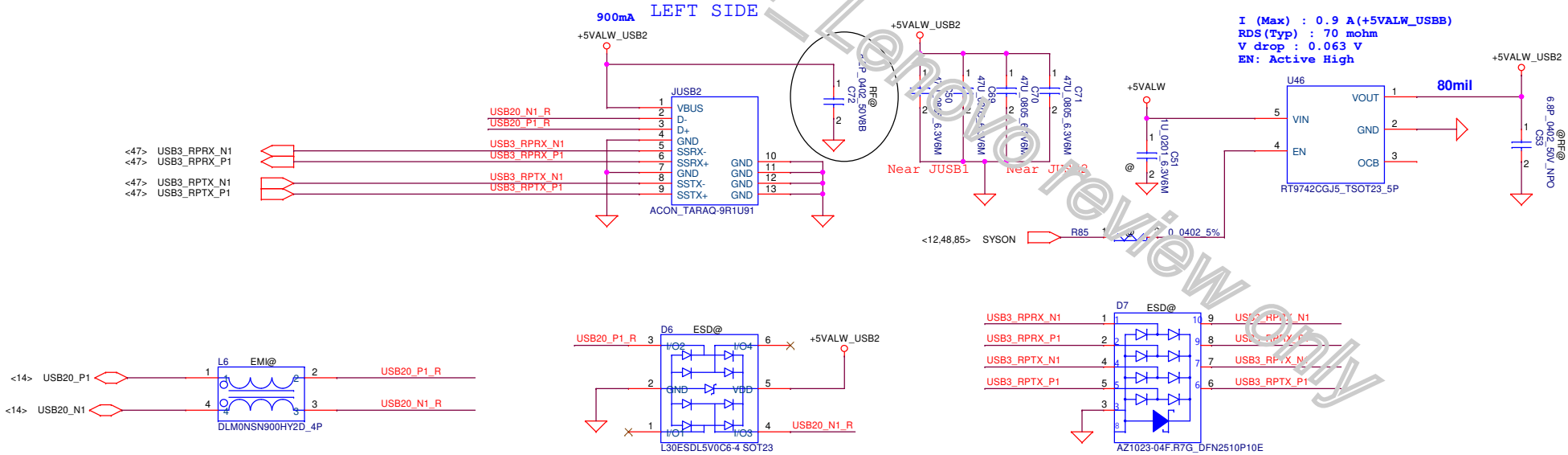
Compal Electronics, Inc.			
Title	USB3 Port 3 CONN.		
Size	Document Number		Rev
	LA-J561P		1.0
Date:	Wednesday, February 26, 2020	Sheet	55 of 100

MB_USB3.1 Conn. (Port 1)



SC300004W00 change to SC300006000

MB_USB3.1 Conn. (Port 2)



SC300004W00 change to SC300006000

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Compal Electronics, Inc.			
Title: USB3 Port1/2 Conn.			
Size	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 56 of 100		

Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From PCH PCIe TX

To SoC PCIe RX

From GPU DDI

Follow TR_DP_TI_PD_HOST_REF_DESIGN_ROV...
PE isn't POR -
Please don't use

Place as close as possible to pins

USB2 Rbias Place as close as possible to pins

PCIE RBIAS
Place as close as possible to pins

TBT Wake function select

TR NORTD3 Desidn	To PCH Wake pin
AR NORTD3 Design	To EC Wake pin
TR RTD3 Design	To PCH GPIO pin for INTEL SPEC

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled

DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

JTAG

SPI ROM

TBT RTD3

RTD3 Support:
In order to support RTD3, DG_PERST# and DG_PEWAKE# signals should reserve connections to dedicated PCH GPIOs per TBT Controllers.
In order to support RTD3, the following signals should be routed from TCH to TBT Controller:
DG_PERST#
DG_CLKREQ#
DG_PEWAKE#
DG_RTD3_PWR_EN

25M XTAL

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

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Issued Date	2020/7/31	Deciphered Date	2020/7/31

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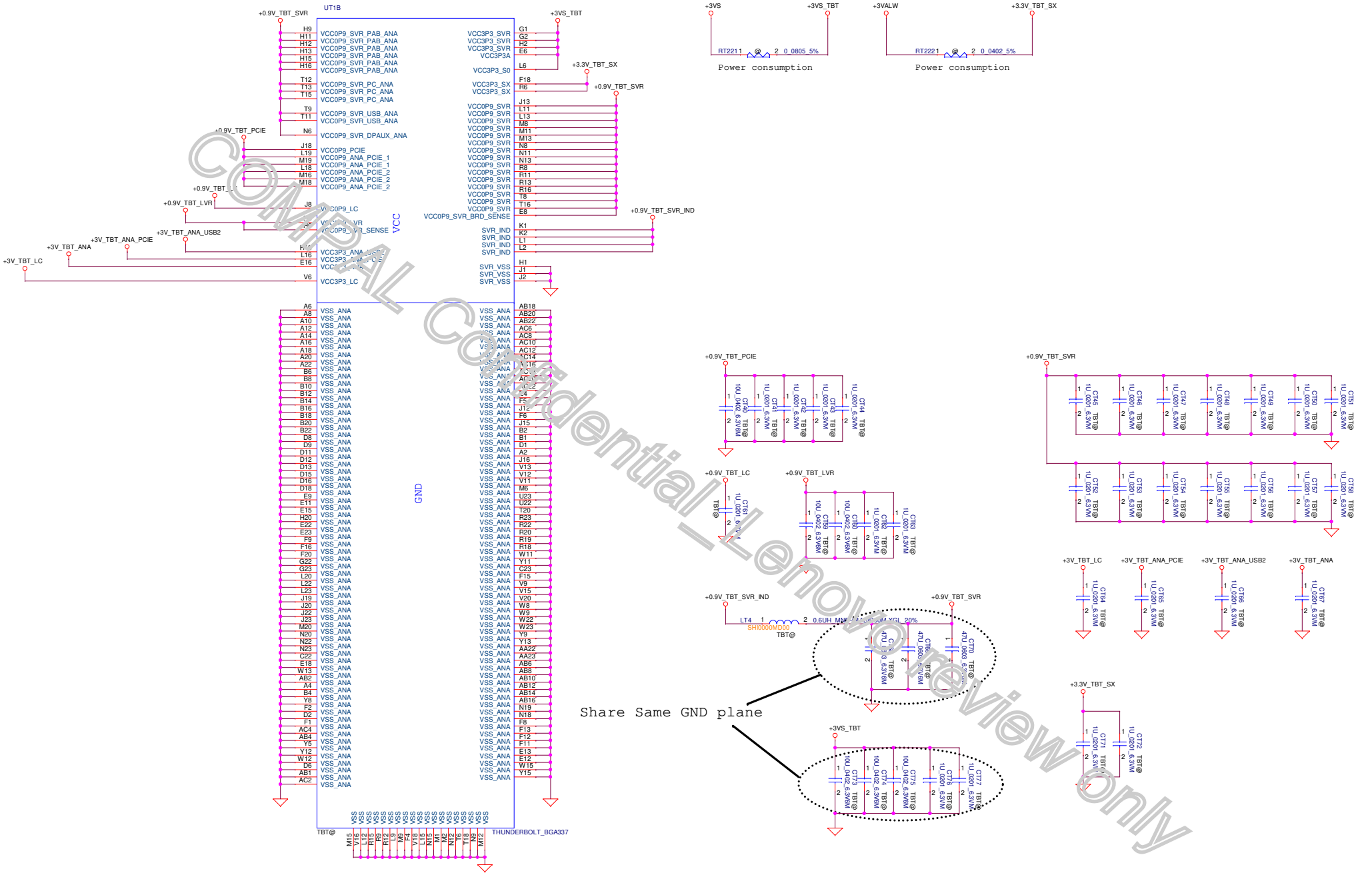
Compal Electronics, Inc.			
Title: Thunderbolt Titanrid (1/2)			
Size: Custom	Document Number: LA-I561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet: 57	of: 100	



Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

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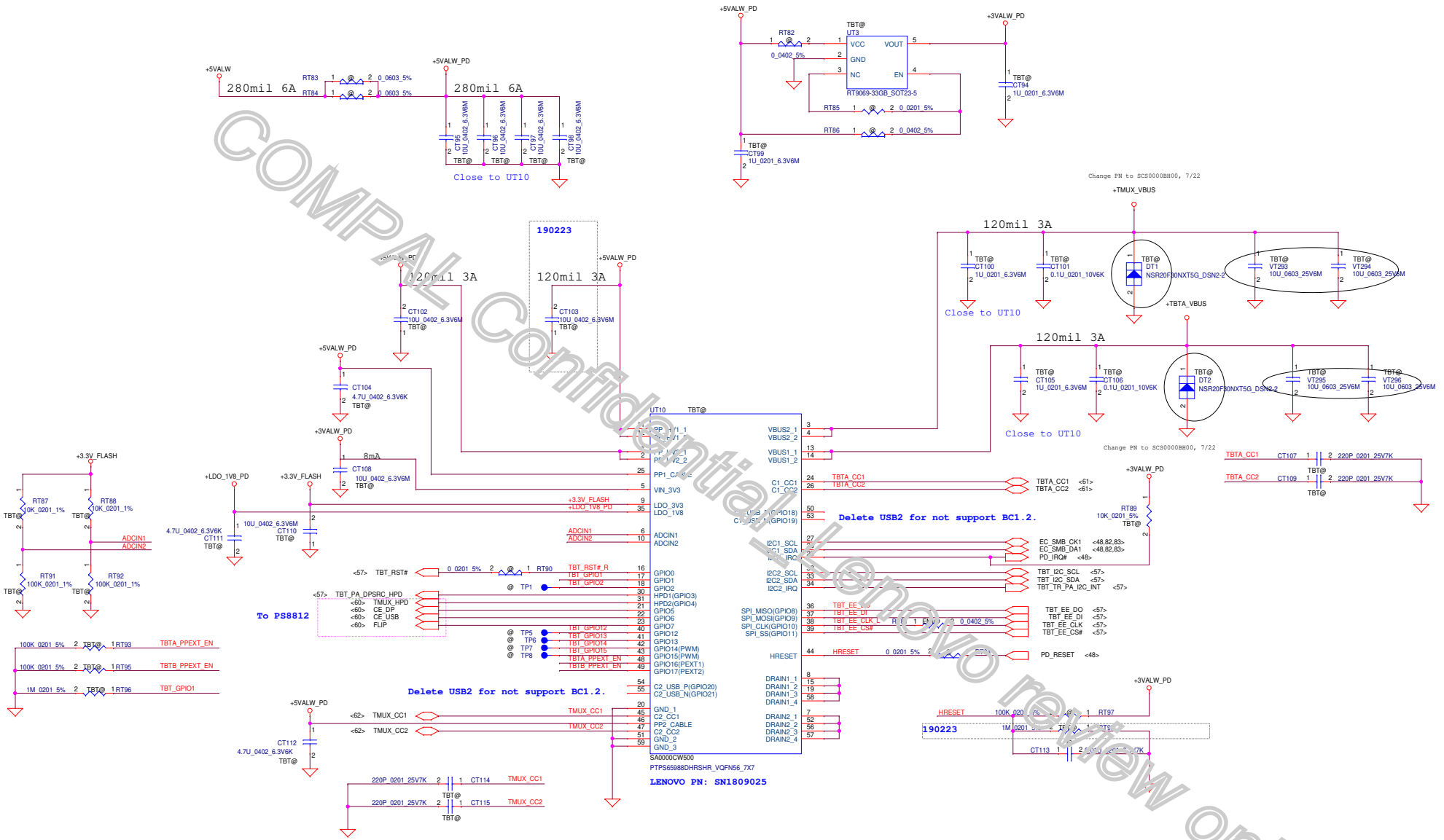
Compal Electronics, Inc.			
Title	Thunderbolt Titanrid (2/2)		
Size: Custom	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020	Sheet 58 of 100		



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Security Classification	Compal Secret Data		
Issued Date	2020/7/31	Deciphered Date	2020/7/31

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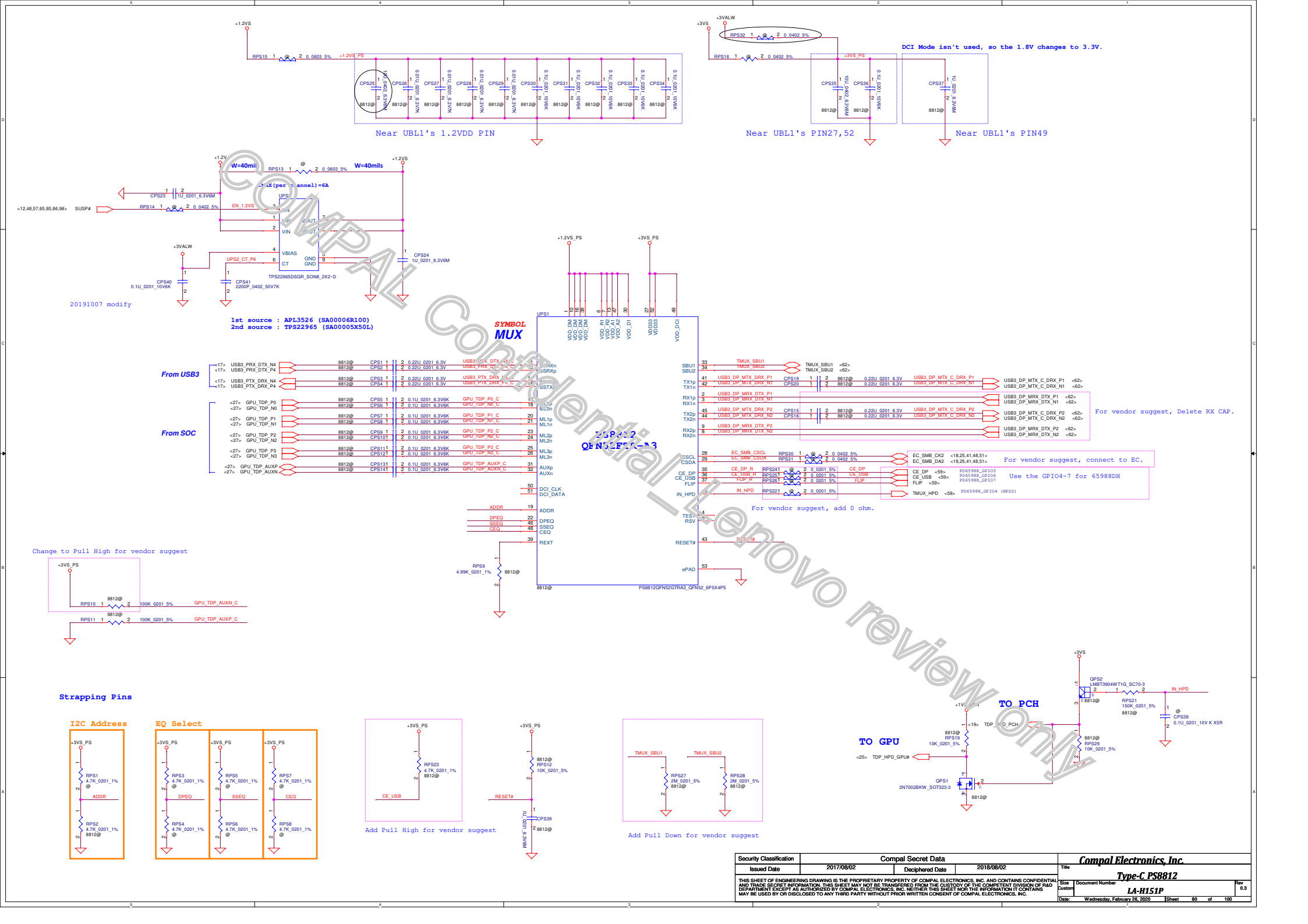
Compal Electronics, Inc.	
Title	CC_TPS65988
Size	Document Number: LA-J561P
Rev	0.1
Date:	Wednesday, February 26, 2020
Sheet	59 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/02	Deciphered Date 2018/08/02	Title: Type-C PS8812
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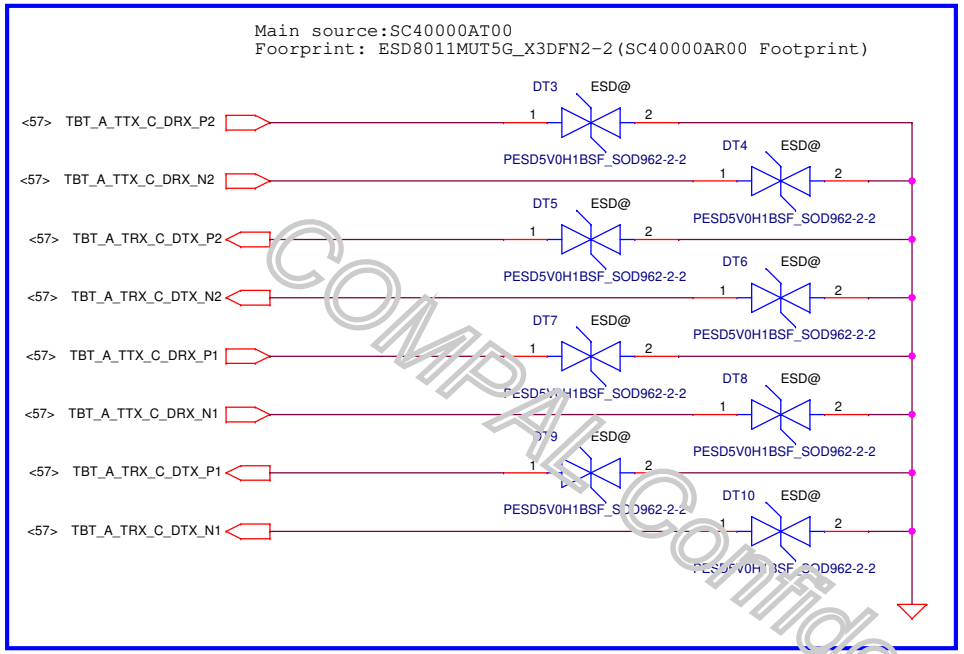
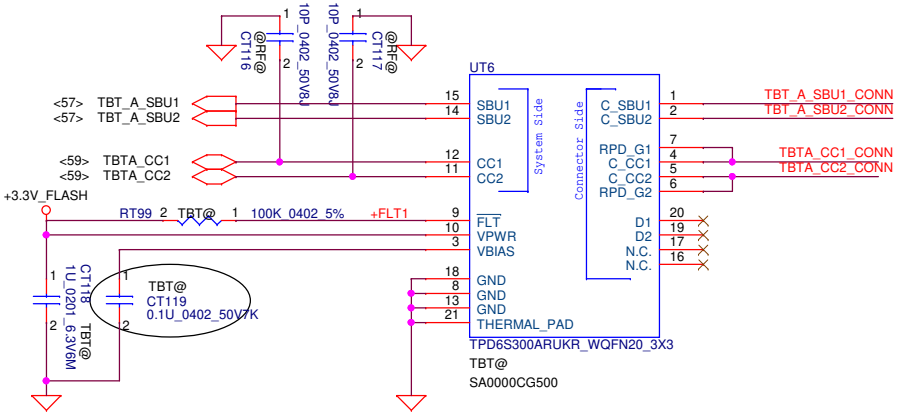
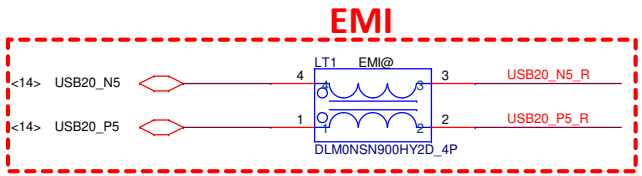
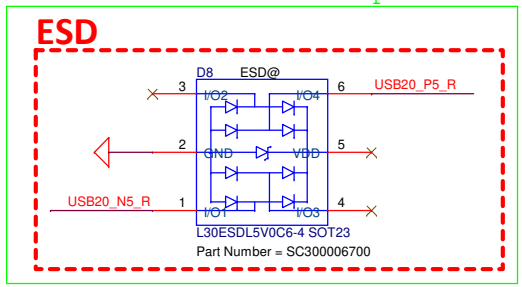
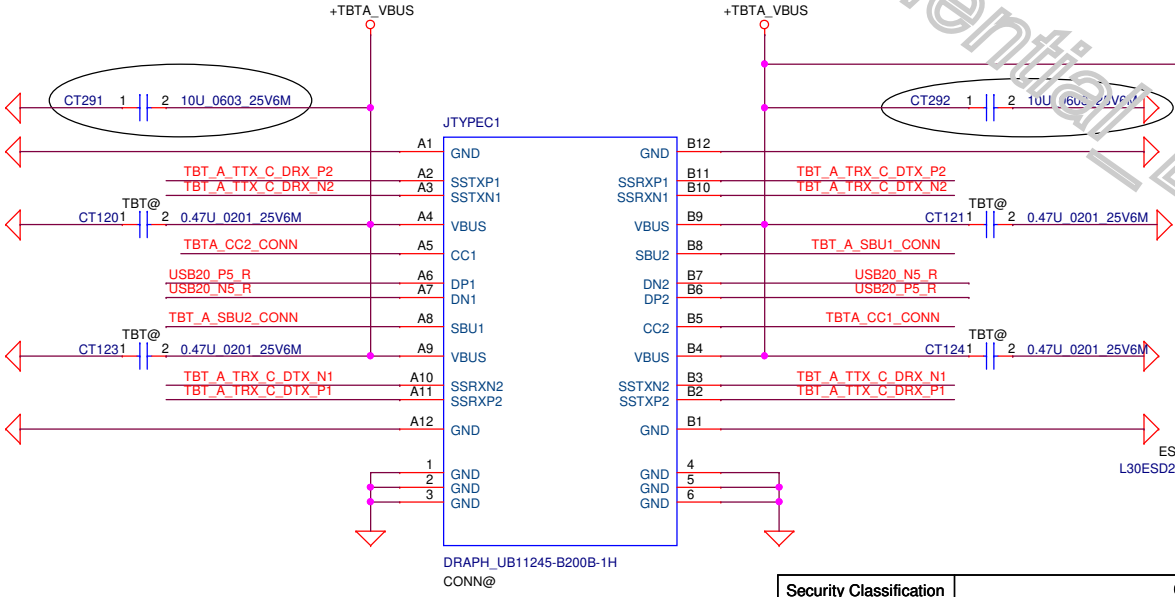


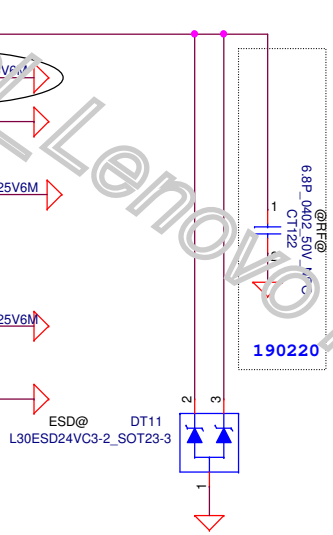


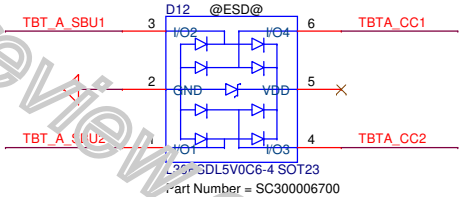


different from USB3.0 port's ESD









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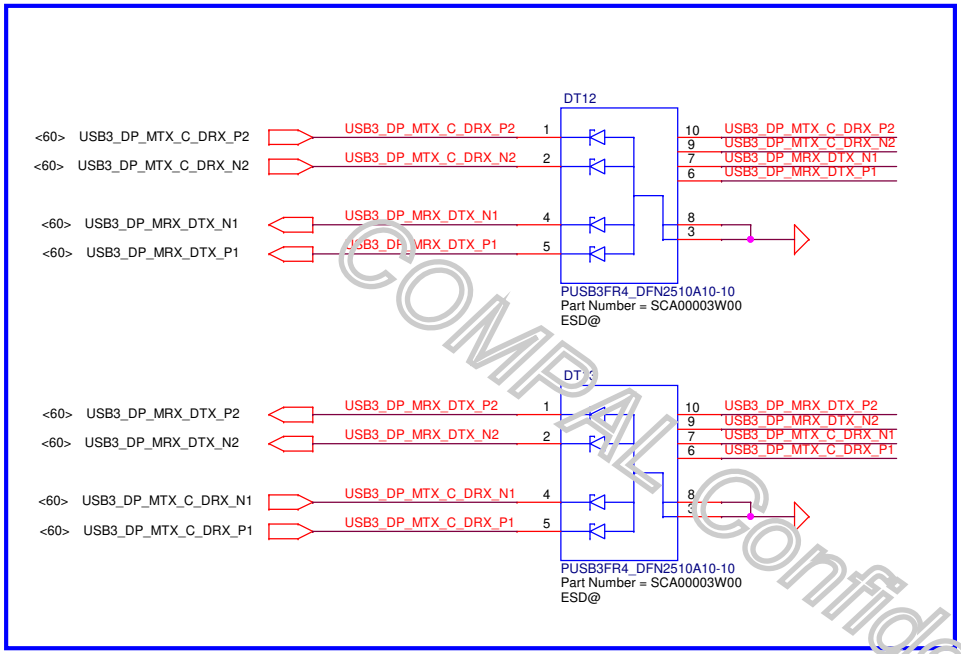
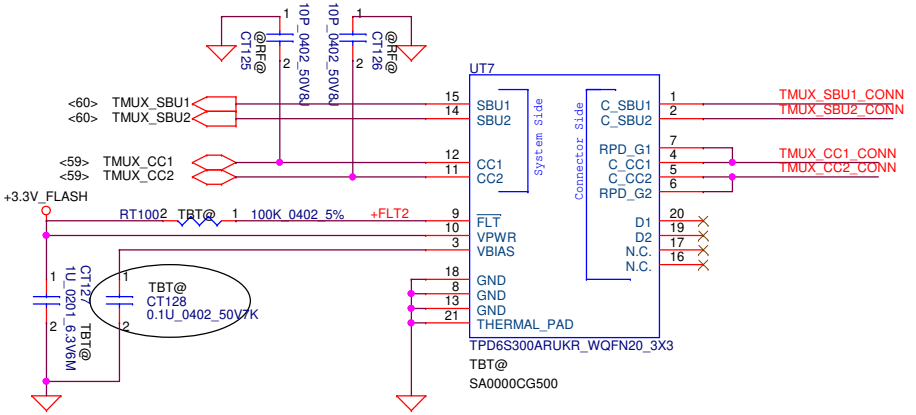
Compal Electronics, Inc.

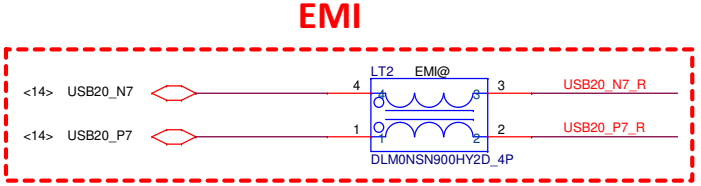
Title: USB3.1 TypeC Conn

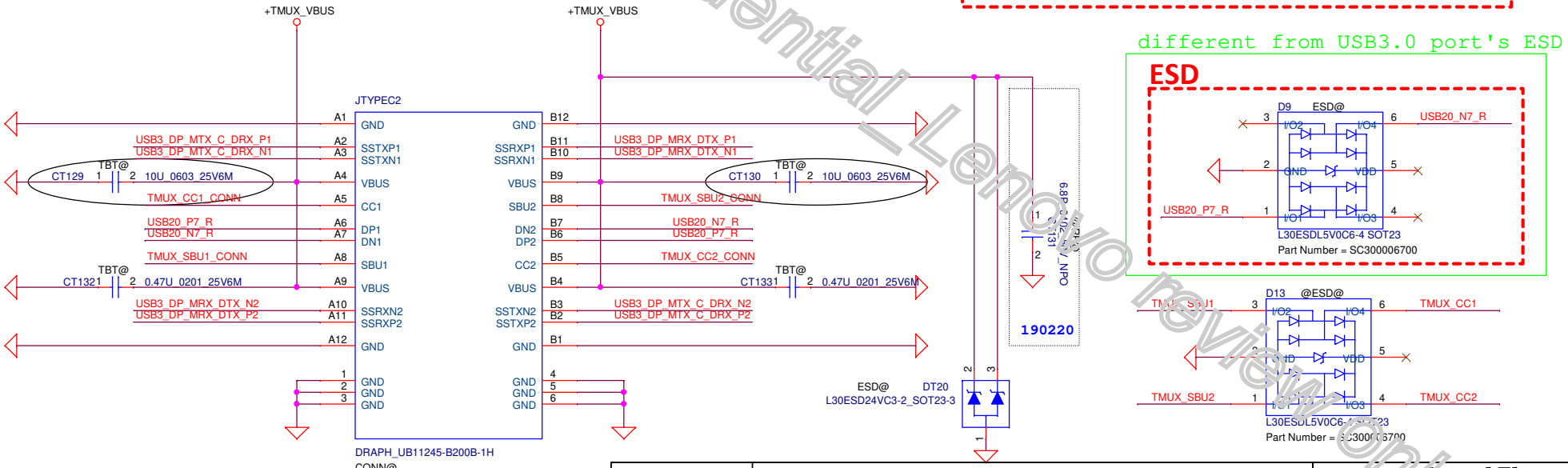
Size | Document Number: LA-J561P | Rev: 0.1

Date: Wednesday, February 26, 2020 | Sheet 61 of 100









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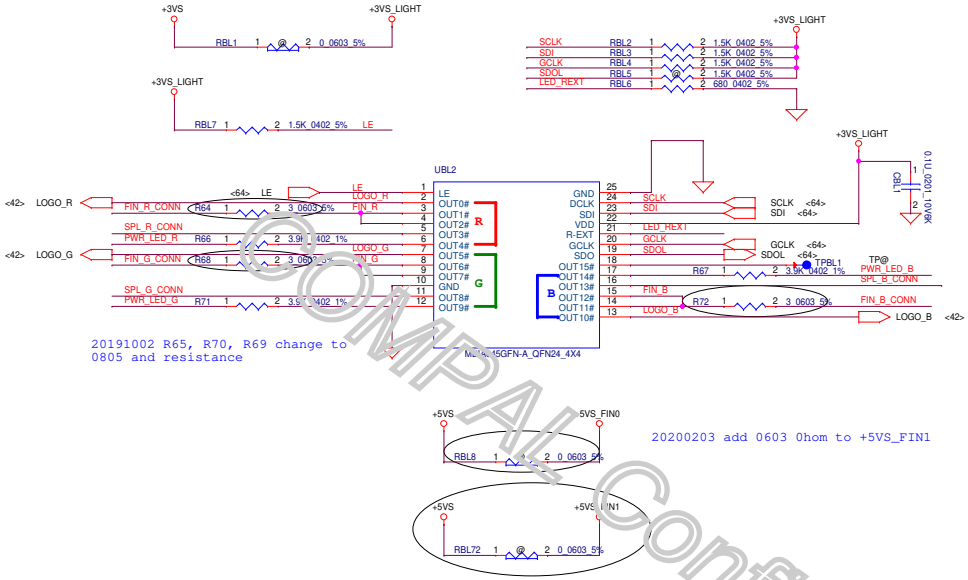
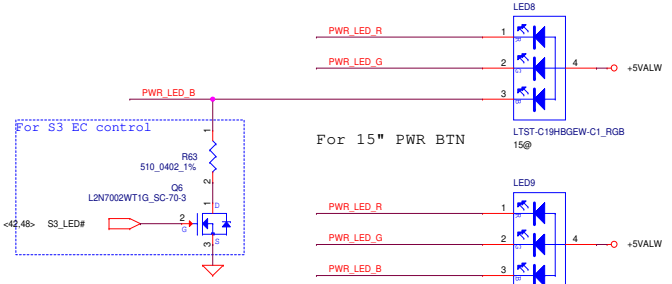
Compal Electronics, Inc.

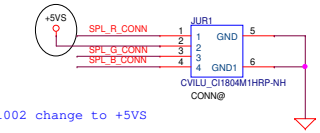
Title: USB3.1 TypeC Conn

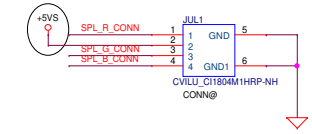
Size | Document Number: LA-J561P | Rev: 0.1

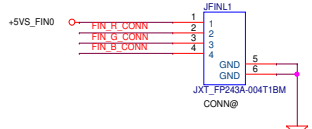
Date: Wednesday, February 26, 2020 | Sheet 62 of 100

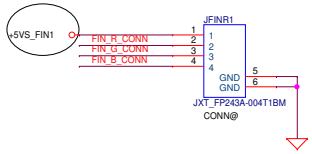












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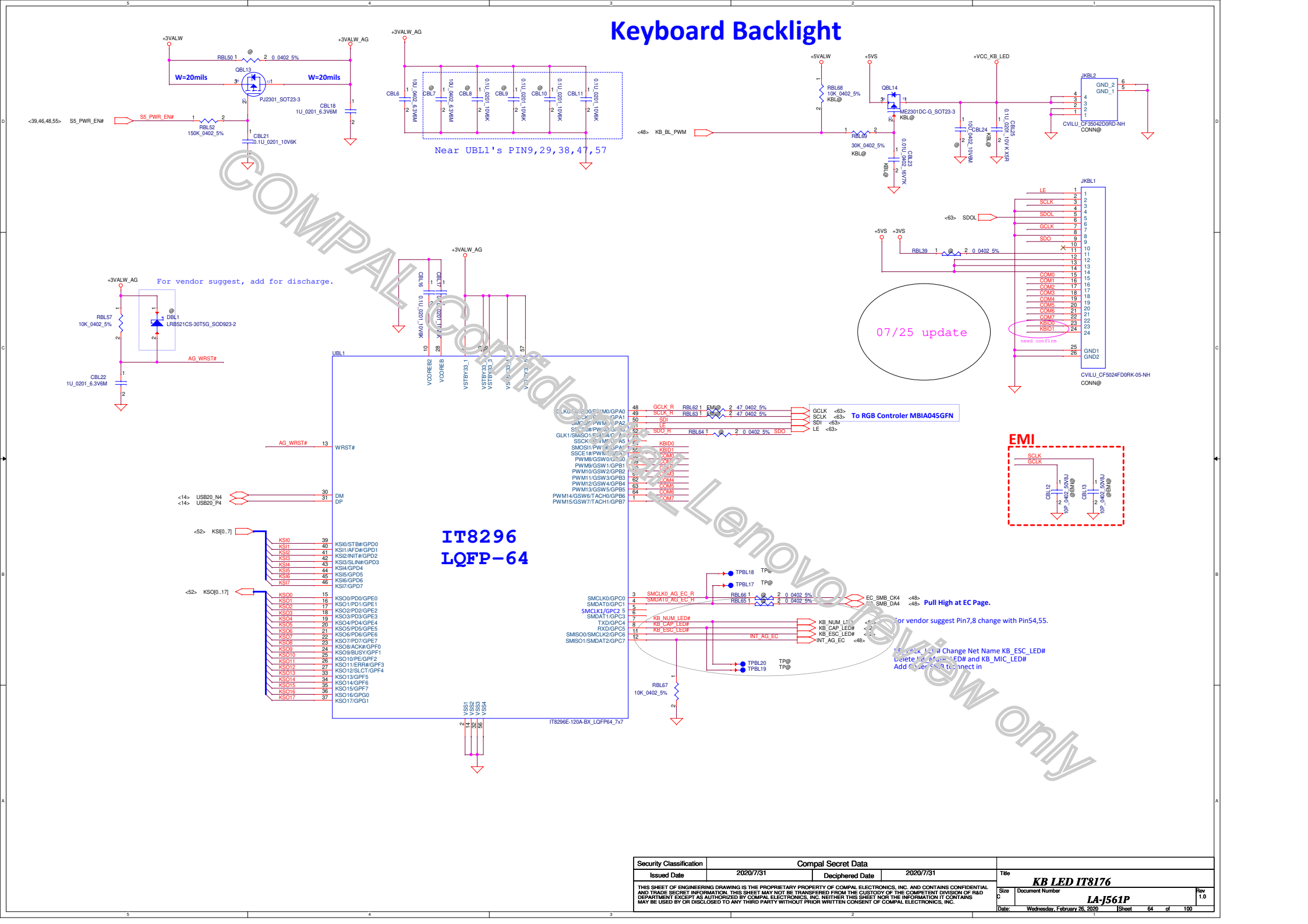
Compal Electronics, Inc.			
Title: FIN LED			
Size: C	Document Number: LA-J561P		Rev: 1.0
Date: Wednesday, February 26, 2020		Sheet: 63 of 100	

Keyboard Backlight



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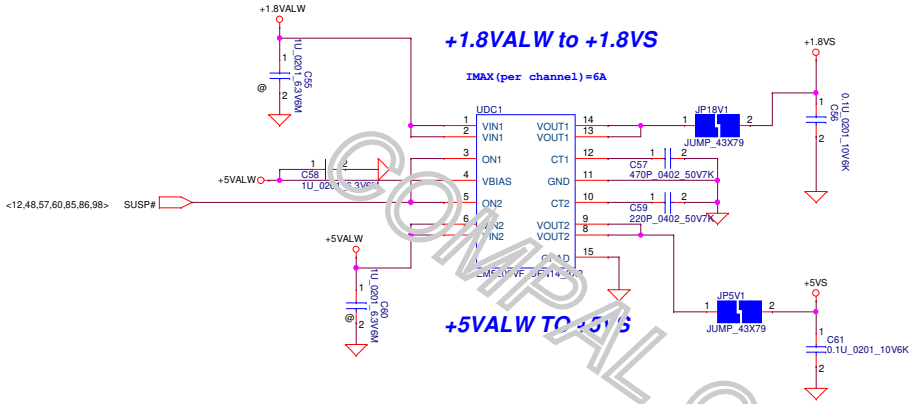
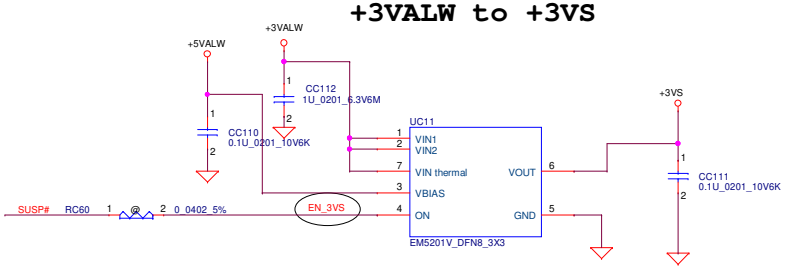
Title	KB LED IT8176		
Size C	Document Number LA-J561P		Rev 1.0
Date: Wednesday, February 26, 2020	Sheet 64 of 100		





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Compal Electronics, Inc.

Title: **DC INTERFACE**

Size	Document Number	Rev
	LA-J561P	1.0

Date: Wednesday, February 26, 2020 | Sheet 65 of 100

Note Color

Version change list (P.I.R. List)

FVT for HW

Item	Page	Modify List	Reason for change	Date
1	18	Add QH1 for ME_EN to HDA_SDOUT level shift	Add level shift for PCH and EC different power plan to solve audio device conldn't recognize	2019/09/06
2	57	Change RT15 and RT16 to 2.2K	Follow INTEL TBT SPEC	2019/09/06
3	41	UGV3 change part to SA00000OH00	Follow GPU DDS function design	2019/09/10
4	47	RUS2, RUS4, RUS6, RUS8, RUS12, RUS14, RUS16, RUS18 change to 68K ohm	Follow vendor recommend to modify DC flat gain and EQ	2019/09/11
5	52	Change JDBG1 CONN to TWVM_FPC0510-06RP-TAGHA	For NPI test only	2019/09/11
6	42	Change EDP_I2CB_SCL and EDP_I2CB_SDA pull-up power from +3VS to +1V8_MAIN for reserved	For DDS panel design update from GPU vendor	2019/09/12
7	58	LT4 (SHI0000MD00) change footprint to MAG_MND-04ABIR60M-XGL_2P	Follow DFB request for shift risk	2019/09/17
8	18	Add RH194 for reserved	For ME_EN reserved	2019/09/18
9	45	Change RA1.2 from +3VS to +1.8VS_DVDD_CODEC	Follow vendor recommend to change JHP1 PLUG_IN voltage divider +3VS to +1.8VS_DVDD_CODEC	2019/09/18
10	53	Add CLIP12, CLIP13, CLIP14	For ME and RF request	2019/09/19
11	55	Add R84	For side USB charger PWR reserved	2019/09/23
12	56	Add R85 and change U46 EN signals to SYSON	For upper USB port S3 resume	2019/09/23
13	60	UPS1 pin28 and pin29 swap	For PS8812 SMBUS signals modify	2019/09/23
14	47	Change RUS4 and RUS8 to 1K ohm	Follow vendor recommend to modify DC flat gain and EQ	2019/09/24
15	42	Change EDP_I2CB_SCL and EDP_I2CB_SDA to pull-up +1.8VS	Follow Nvidia vendor recommend to modify	2019/09/26
16	60	Change QPS1A to QPS2	Update location	2019/09/26
17	41,48	Change RV74 and R29 to pop	For DDS PWM function control from EC	2019/09/27
18	63	Add R86 and R87 to BOM control +3VS/+5VS	For Soucer ask to implement new UL module	2019/09/27
19	65	Change JUMP location name from JP3V1 to JP18V1	For naming update	2019/10/02
20	56	Add C72 0402 8.2P capacitor	For RF request	2019/10/02
21	63	Remove R86 and R87	For UL module use +5VS only	2019/10/02
22	63	RBL8 change 0402 to 0603 0 ohm	For LED power	2019/10/02
23	63	R65, R70, R69 change to 0805 and resistance update	For vendor recommend to change it	2019/10/02
24	17	Add RH195 0402 0 ohm	For debug reserved	2019/10/04
25	60	Remove QPL1 and change to UPS2 related circuit	For UPS1 1.2V power switch modify	2019/10/04

Note Color

Version change list (P.I.R. List)

SIT for HW

Item	Page	Modify List	Reason for change	Date
1	60	Add RPS32 and change CPS25 to 10uF	For PS8812 debug to modify and reserved	2019/10/21
2	57	Add RT230 pull up to +3.3V_TBT_SX, RT13 change to un-pop, RT15 change to un-pop and RT16 change to TBT@	For TBT RTD3 debug and updated	2019/10/24
3	34	Add CG623 and CG624 for reserved	For GPU 1.8V dual load switch reserved	2019/11/5
4	20	Change RH136 from 0603 to 0805	For PCH +1.8V_PRIM power	2019/11/6
5	18	Change RH66 to Pull down	Follow INTEL CML-H PCH-H design specificaion	2019/11/7
6	18	Change ME_EN related circuit	Follow previous project design	2019/11/7
7	17	Add RH196 PU to +3VS	Add SATA_LED net pull up circuit	2019/11/7
8	50	Change TL1 to SP050006P00	For thermal interference to change transformer type	2019/11/14
9	16,19,49,52	Change PCH GPP_B3 connect to BT_ON & TP_INT connect to GPP_C15	Follow INTEL instruction to modify for BT native error recovery method issue	2019/11/14
10	48	Modify LID_SW# pull up to +5VALW	For MR sensor vendor recommend	2019/11/21
11	16	Change RH32 and RH33 to 100K pull up	Follow INTEL CML-H ESD REV1P0 to modify	2019/11/21
12	17,19	Add RH197 and RH198 for HDMI_HPD_PCH	For BIOS request to reserved that connect to GPP_K19	2019/11/21
13	19	Add RH199 and RH200 for DDS strap	For BIOS request to add the DDS strap	2019/11/21
14	50	TL1 signals swap	For Layout Routing	2019/11/25
15	19	Add RH201 and RH202 for GPU_ID2 strap	For BIOS request to add the GPU_ID2	2019/11/25
16	49	RW23 change to PD	For CNVi check list modify	2019/11/25
17	18	Add QH5, RH203 and RH204 level shift circuit	For SMBUS level shift to separate +3VALW and +3VS	2019/11/26
18	49	RS2 and RS4 change to 0805	For SSD1 and SSD2 power source optimization	2019/11/26
19	20	RH115 change to 0603 reserved	For PCH internal 1.8V modify	2019/11/26
20	16	Change RC41~RC49 from 33 hom to 56 ohm	For INTEL Design Guide update	2019/11/26
21	14-21	Change UH1 footprint to CML-H_BGA_874P-T	Follow COMPAL ORB schematics	2019/11/26
22	15,49	Change RH205, RH206, RW5, RW10 to 22ohm and RH30 to 20Kohm	Follow CNVi check list to update	2019/11/27
23	18	Remove QH5, RH203 and RH204 level shift circuit	Follow COMPAL ORB	2019/11/27
24	18	Change RH71 to 8.2K	Follow INTEL documents	2019/11/28
25	48	Change R24 to 33ohm	Follow INTEL documents	2019/11/28
26	63	Change JFINL1 and JFINR1 CONN to SP01002X400	Follow ME request to modify	2019/11/28
27	42,53	Add C73 and CV308	Follow RF request to add capacitors	2019/11/28
28	42	JEDP1 pin34 modify to +1.8VS	For solve +1.8VALW OVP issue and change DMIC power source	2019/12/3
29	61,62	Add CT291-CT294	For solve TYPEC issue	2019/12/4
30	48	Add R87	For EC Prochot pin issue	2019/12/4
31	50	Change RL14-RL17 from 0402 to 0603	For EMI request	2019/12/5
32	55	Change R65, R69, R70 to 0 ohm	For U lighting design modify	2019/12/5
33	59,61,62	Add C293-C296 and modiy C291, C292, C129, C130 to 0603	For solve TYPEC issue	2019/12/5
34	63	Change RH66, RH67 and RH71 to 3.9K	For customer request	2019/12/20
35	42	Change RH189 and RH190 to un-pop	For NV vendor recommend	2019/12/20

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Note Color

Version change list (P.I.R. List)

MP for HW

Item	Page	Modify List	Reason for change	Date
1	63	Add RBL72 0603 0ohm	Add 0hom to improve FIN lighting issue	2020/02/03
2	63	Delete QBL1, QBL3, RBL10, RBL12 and RBL14	Remove components for FIN lighting PWR	2020/02/03
3	63	Change R64, R68, R72 from 22ohm to 3ohm 0603 resistors	Fine tune for FIN lighting	2020/02/04
4	63	Remove RBL5	Fine tune for FIN lighting	2020/02/05
5	63	Delete R65,R69 and R70 0ohm to short RGB signals directly	Fine tune for U lighting	2020/02/06
6	64	Change KBID0/KBID1 to UBL1 pin5.pin6	Not support Keyboard Audio Lighting Mode	2020/02/12
7	63,64	Add Q7,Q8,Q9 to control FIN Lighting directly from UBL1 pin53.pin54.pin55	Follow LD request to modify it	2020/02/12
8	63	UBL2 modify the SPL_R_CONN, SPL_G_CONN, SPL_B_CONN to UBL1 SPL_R, SPL_G, SPL_B controlled by 3 pins.	Increase U lighting signals strength	2020/02/12
9	63	Add R88,R89,R90 and net name SPL_R_CONN_R, SPL_G_CONN_R, SPL_B_CONN_R	Increase FIN lighting signals strength	2020/02/20
10	64	Delete RBL70,RBL71 and QBL2	Not support Keyboard Audio Lighting Mode	2020/02/25
11	64	Change KBID0/KBID1 to UBL1 pin54.pin55	For KB function change back	2020/02/25
12	63	Delete Q7,Q8,Q9,R88,R89,R90 and change R64, R68, R72 connect to UBL1	Fine tune for FIN lighting	2020/02/25

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Title: PIR-HW

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Title: **miniDP**

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Y/SO Power

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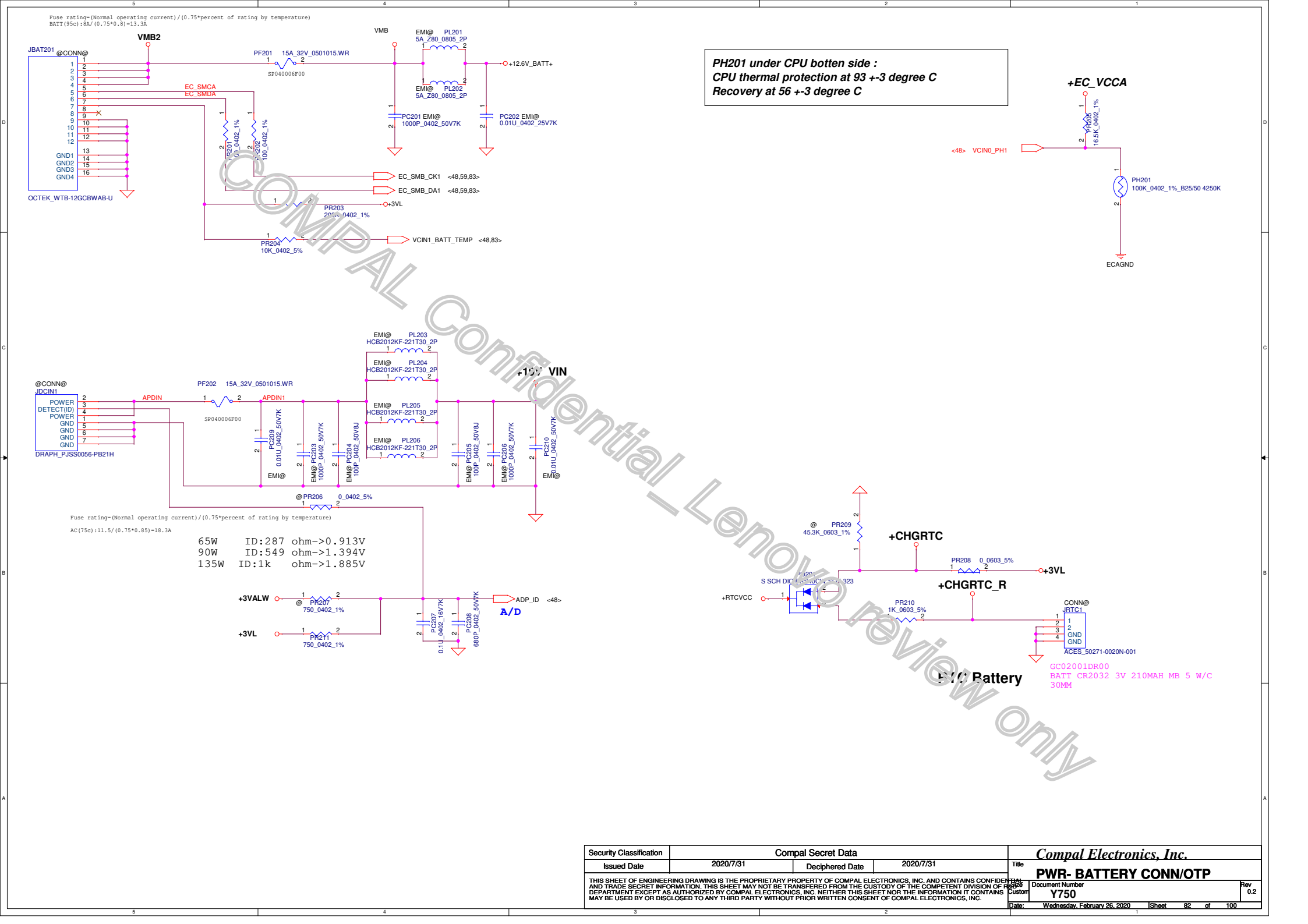

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Title	PWR- BATTERY CONN/OTP		
Size: Custom	Document Number: Y750		Rev: 0.2
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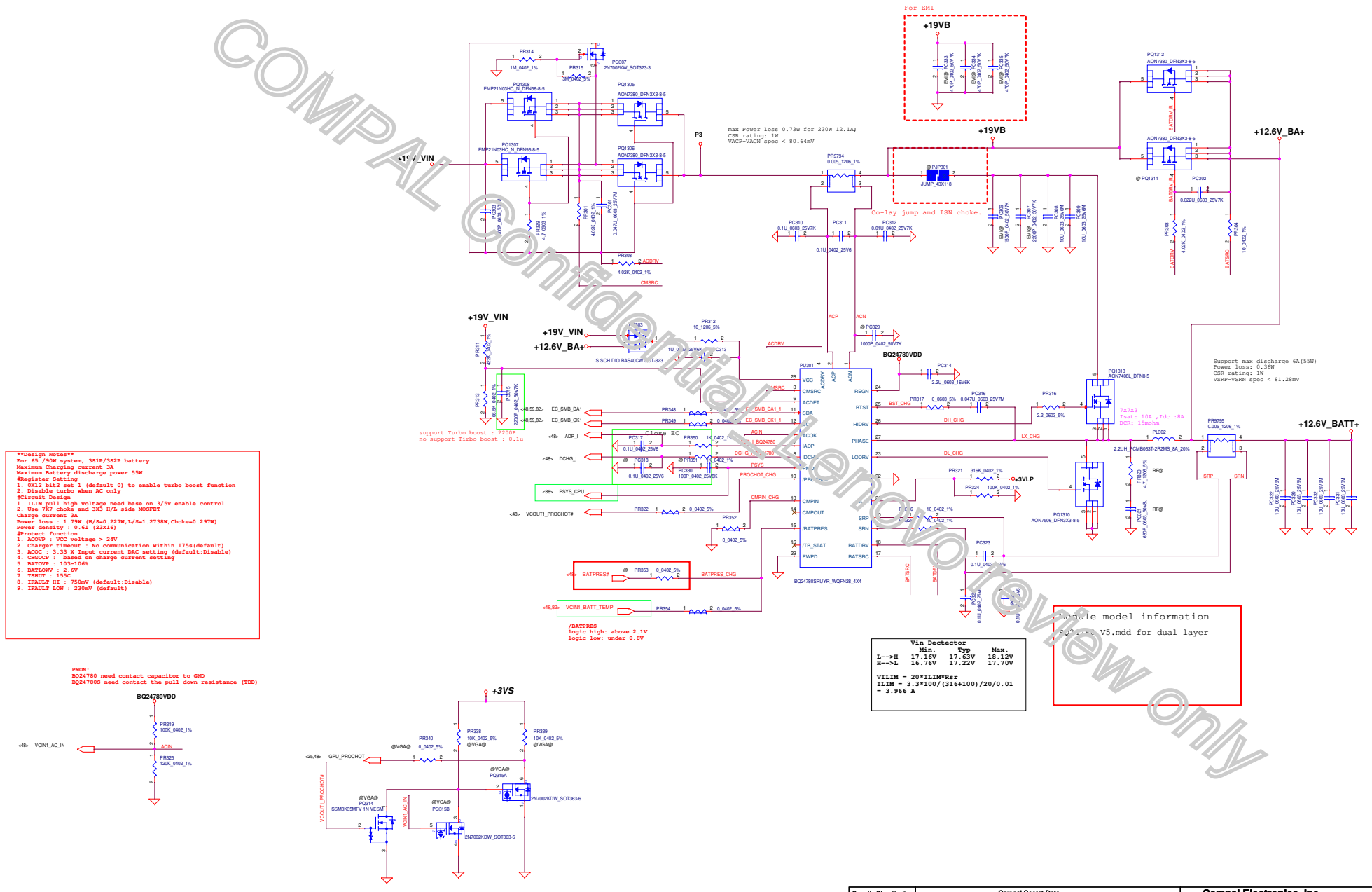

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Module model information

RT6575D_DMOS_single_V2.mdd
RT6575D_DMOS_dual_V2.mdd

(Common Part)
Choke 4.7uH SH00000YC00

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA

POK need p... high ... will pull hig... ... transfer circui...

+19VB
+12.6VB_3/5V
+3VALWP
+5VALWP
+3VLP
+5VLP
+3VL
+5VALW

PU401 RT6575DGQW(2)_WQFN20_3X3
PQ401 AONH36334_DFN3X3A8-10
PQ402 AONY36352_DFN5X6D-8-7
PL401 5A_Z80_0805_2P
PL411 5A_Z80_0805_2P
PL402 3.3UH_6.3A_20%_7X7X3_M
PL403 3.3UH_TMPA1004S-3R3MN-D__10A_20%

3.3V
FSW=355kHz
COP: 11.95A
Vout2=2V*(1+13.7k/20k)=3.37V

5.09V
FSW=300kHz
COP: 23.95A
Vout1=2V*(1+30.9k/20k)=5.09V

OVP=Vout*(11?.5%~117.5%)

OCP=Vtrip/Rd...*ripple/2
Vtrip=Ics(min)*...cs/3+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

Vos=√SQU(Vomax)+L*SQU(I)/C)

EN
Rising=1.6~0.3V
Need inform HW to change NET NAME

<48> VCOUT0_MAIN_PWR_ON
<48> EC_ON
EN_5V3V
EN_5VALW <48>

JUMP_43X118
JUMP_43X39

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Title	+3VALW/+5VALW		
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Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Vout=0.75V(1+6.04k/10k) =1.203V
OCP=12.8A

Vout=0.8V* (1+Rup/Rdown)

Down size

Down size

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Title: RT8207P

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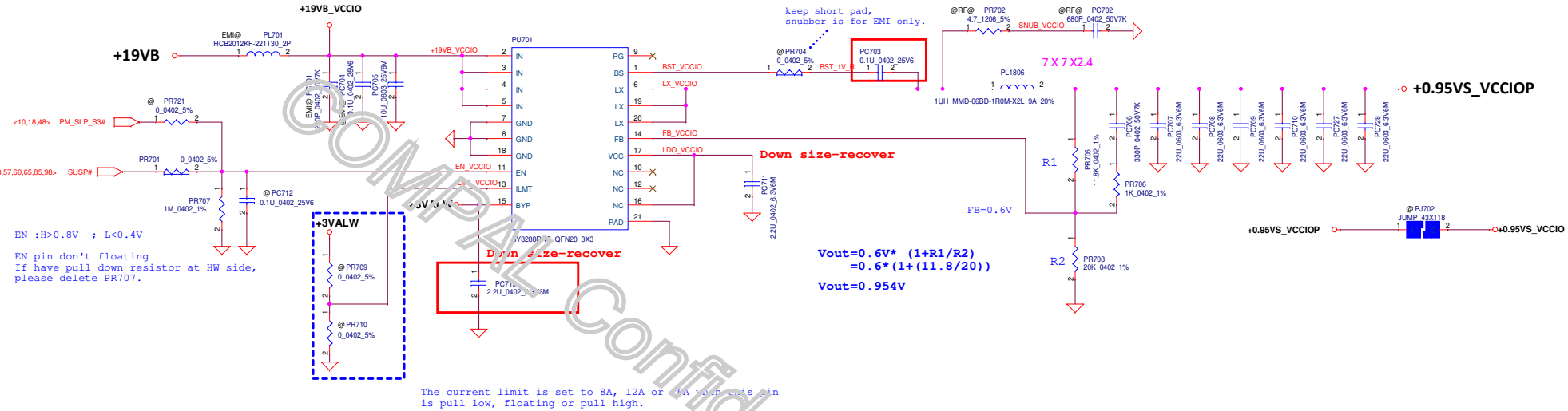
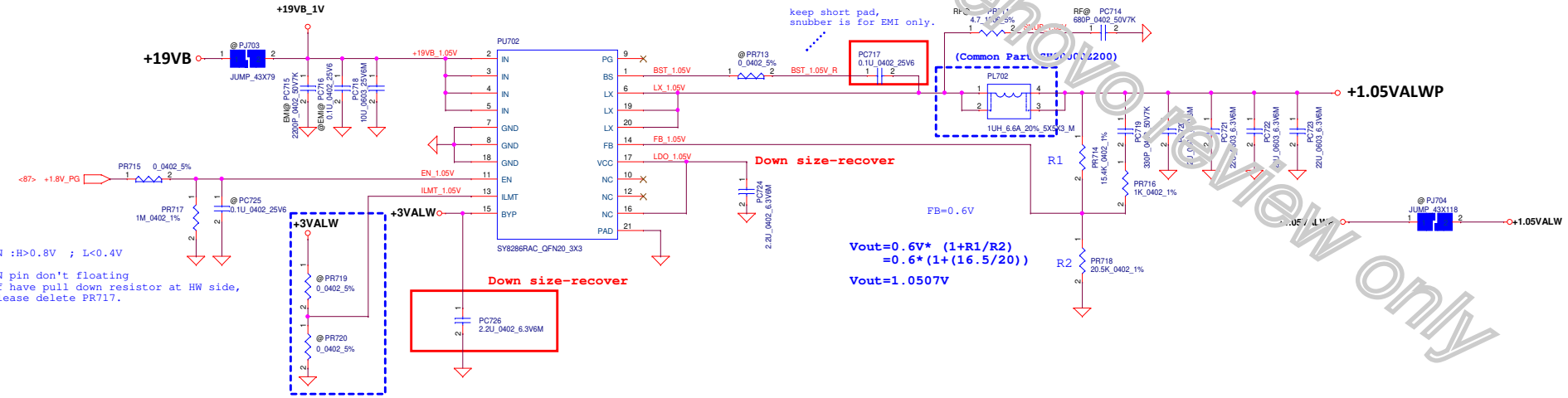
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



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Title: SY8286

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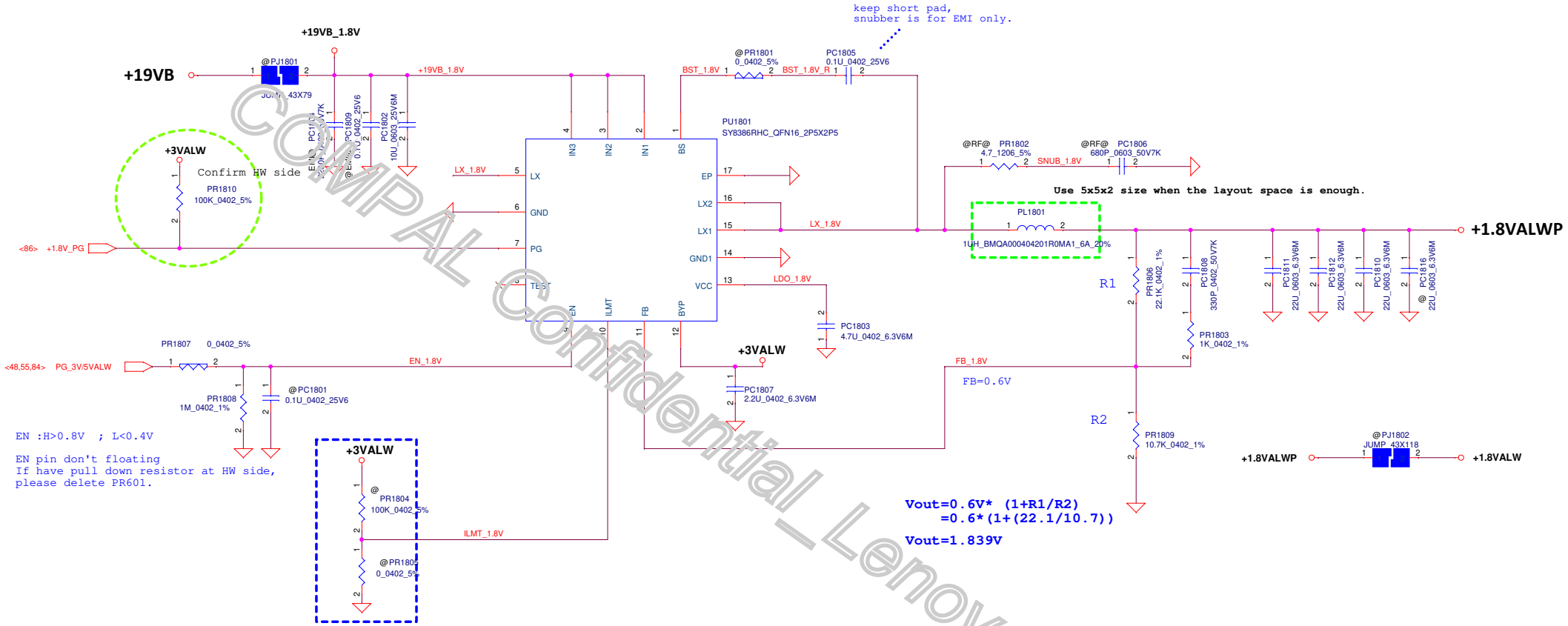

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Title: APL5930

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Module model information

NCP81205_H42_V6A.mdd for IC portion

NCP81205_H42_V6B.mdd for SW portion

SKL Refresh	H42(45W)	
TDC@VCORE	56A	
IccMax@VCORE	68A	
OCP@VCORE	75A	
TDC@VGT	39A	
IccMax@VGT	54A	
OCP@VGT	61A	
TDC@VCCSA	10A	
IccMax@VCCSA	11A	
OCP@VCCSA	16.5A	
Fsw	600KHz	
DCR	0.9mohm +/-7%	

VCCSA:

H42: IccMAX@SA= 11A RIccMAX@SA= 34.8K ---> PR109

RIccMAX@SA= IccMAX*2V/10uA/64A

H42: IOUTSP@SA= 11A RIOUTSP@SA=19.6K ---> PR102

RIOUTSP= 2V/(gm*(Rth+RCSSP)*IccMAX*DCR/(RPHSP+Rth+RCSSP))

H42: OCP@SA= 16.5A RLIMSP@SA=8.45K ---> PR101

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR/(RPHSP+Rth+RCSSP))

Load line@SA= 9.1m

RDRPSP@SA=1.4K ---> PR95

RDRPSP= Load line*(RPHSP+Rth+RCSSP)/(gm * DCR) /(Rth+RCSSP)

CML-H82 (45W) baseline

IA: Max current=140A, loadline=1.1mohm,

GT: 0~1.52V, Max current=32A, loadline=2.7mohm

SA: 0~1.52V, Max current=11A, loadline=10.3mohm

OCP

IA: 168A

GT: 40A

SA: 16.5A

OVP

DAC+370mV

VCCGT:

H42 OCP@GT= 61A RLIM@GT=16.2K ---> PR130

RLIM= 1.3*LIMIT * Load line/10

H42 IccMAX@GT= 54A RIccMAX2ph= 42.2K ---> PR150

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@GT= 54A RIOUT@GT=24.9K ---> PR126

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@GT= 2.65m RPH@GT=75K ---> PR139,PR141,PR144

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

VCCCORE:

H42 OCP@Vcore= 75A RLIM@VCORE=13.7K ---> PR129

RLIM= IoutLIMIT * Load line/10

H42 IccMAX@Vcore= 68A RIccMAX2ph= 52.3K ---> PR154

RIccMAX2ph= (IccMAX2Ph*2V)/ (10uA*256A)

H42 Iout@Vcore= 68A RIOUT@Vcore=22.6K ---> PR120

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

H42 Load line@VCORE= 1.8m RPH@Vcore=113K ---> PR135,PR137,PR140

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))*IOUTTOTAL * DCR/RPH

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Title: NCP81215 H62

Size: Document Number: Custom — Rev: 0.2

Date: Wednesday, February 26, 2020 — Sheet 88 of 100

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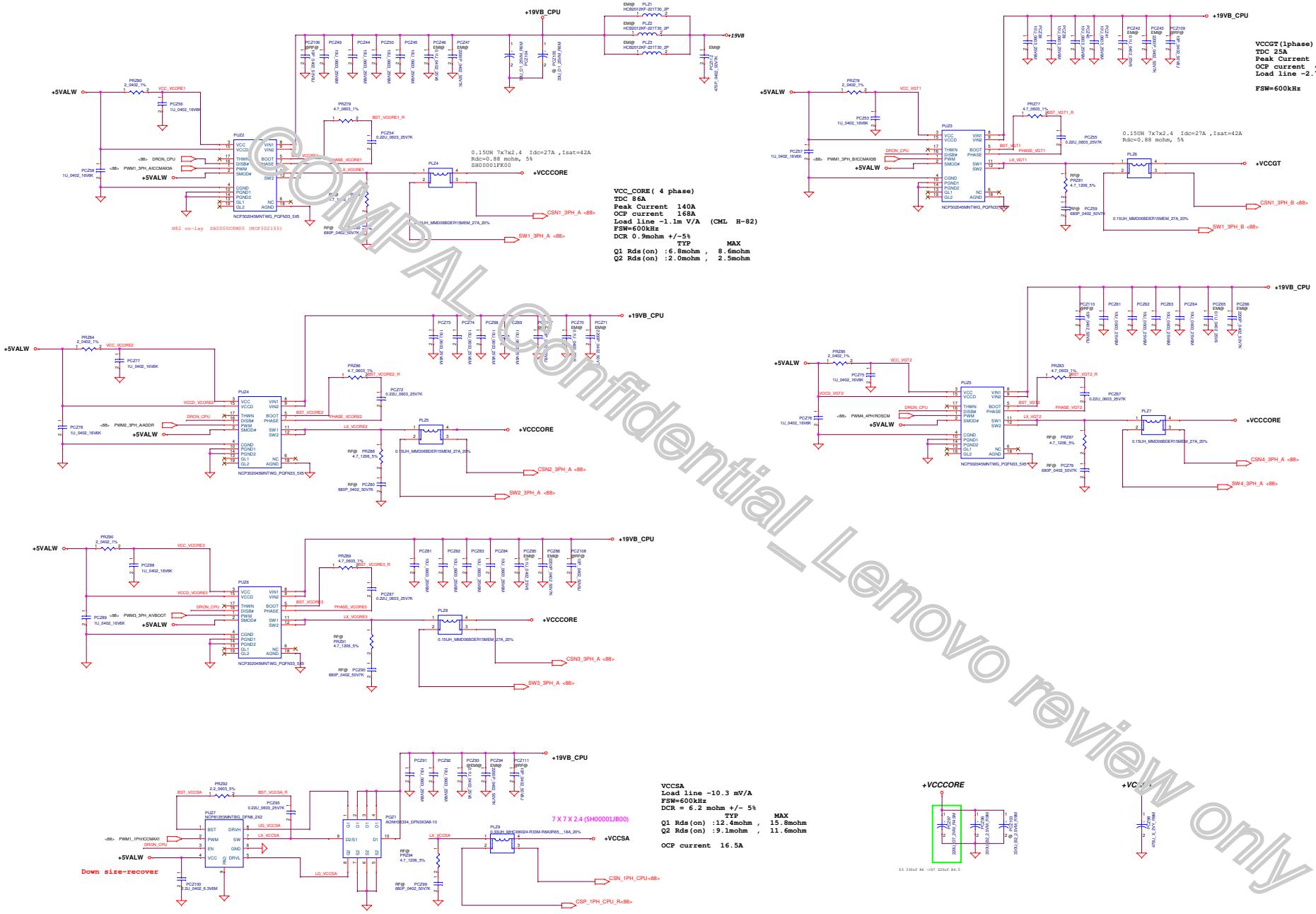

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Issued Date	2020/7/31	2020/7/31	Title: NCP81215_PowerStage
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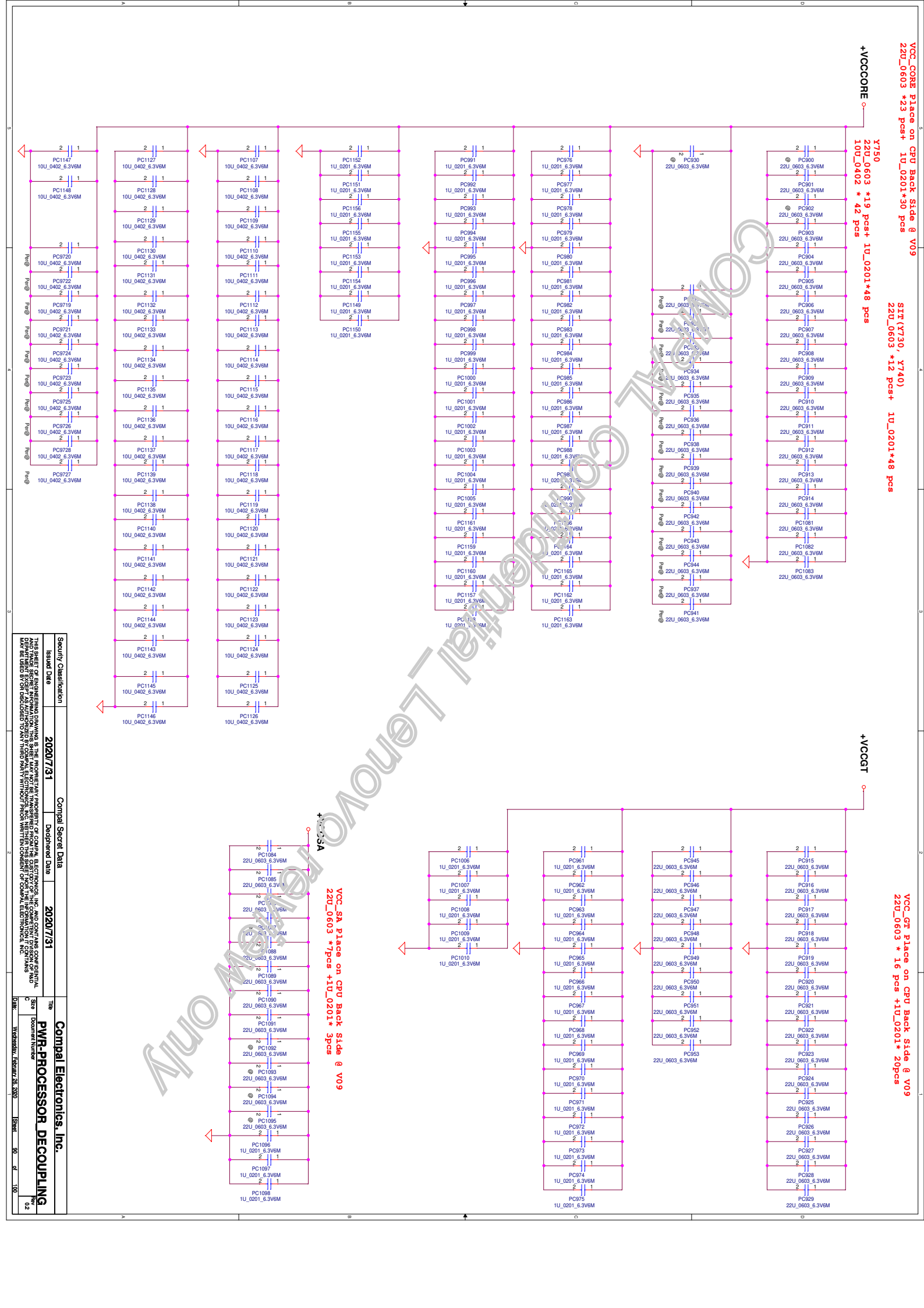
Size	Document Number		Rev
Custom			0.2
Date: Wednesday, February 26, 2020	Sheet 88 of 100		



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Issued Date	2020/7/31	Deciphered Date	2020/7/31

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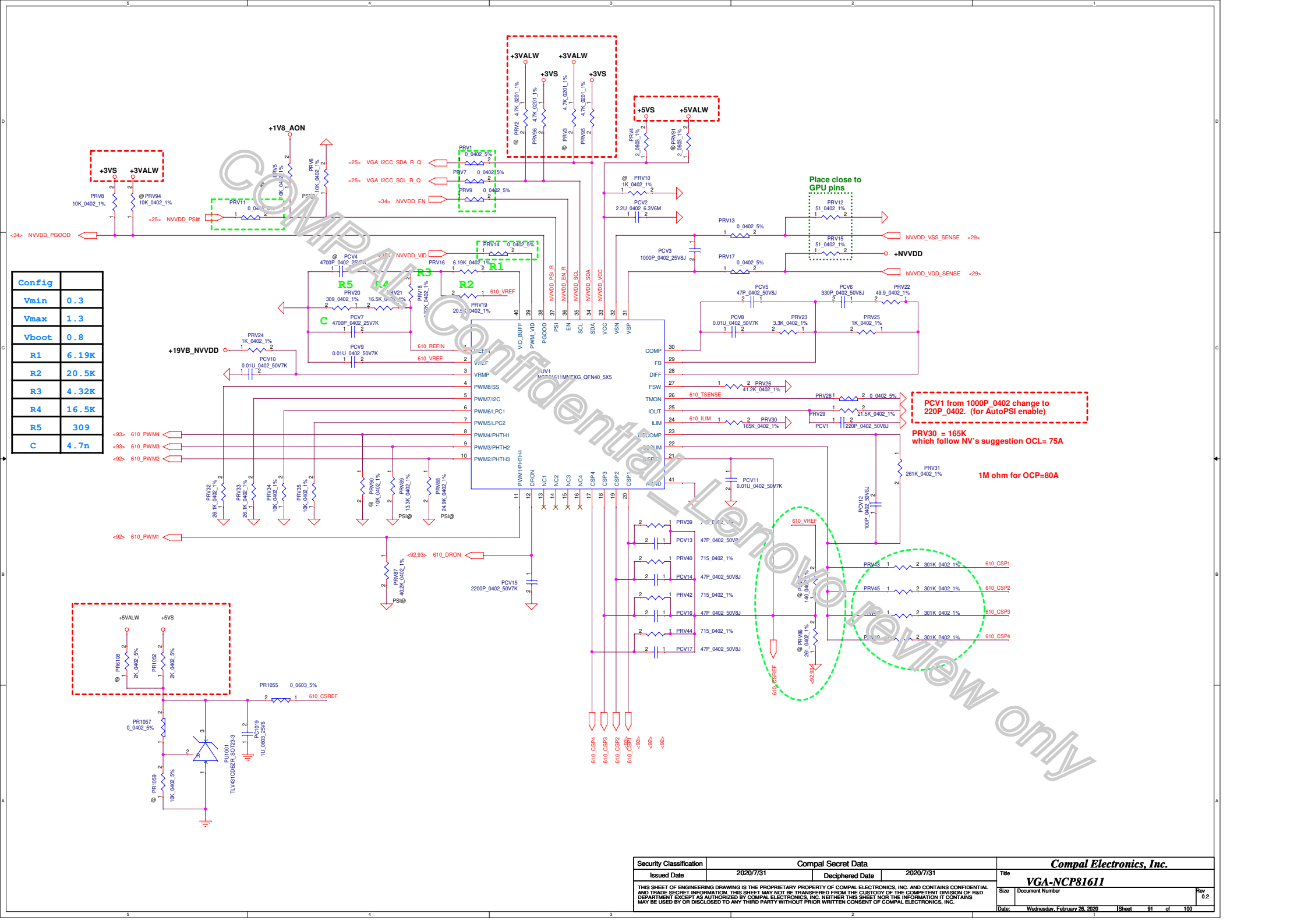
Title	Compal Electronics, Inc.		
Size	Document Number		Rev
C	PWR-PROCESSOR_DECOUPLING		0.2
Date: Wednesday, February 26, 2020	Sheet 90	of 100	



Config	
Vmin	0.3
Vmax	1.3
Vboot	0.8
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	309
C	4.7n

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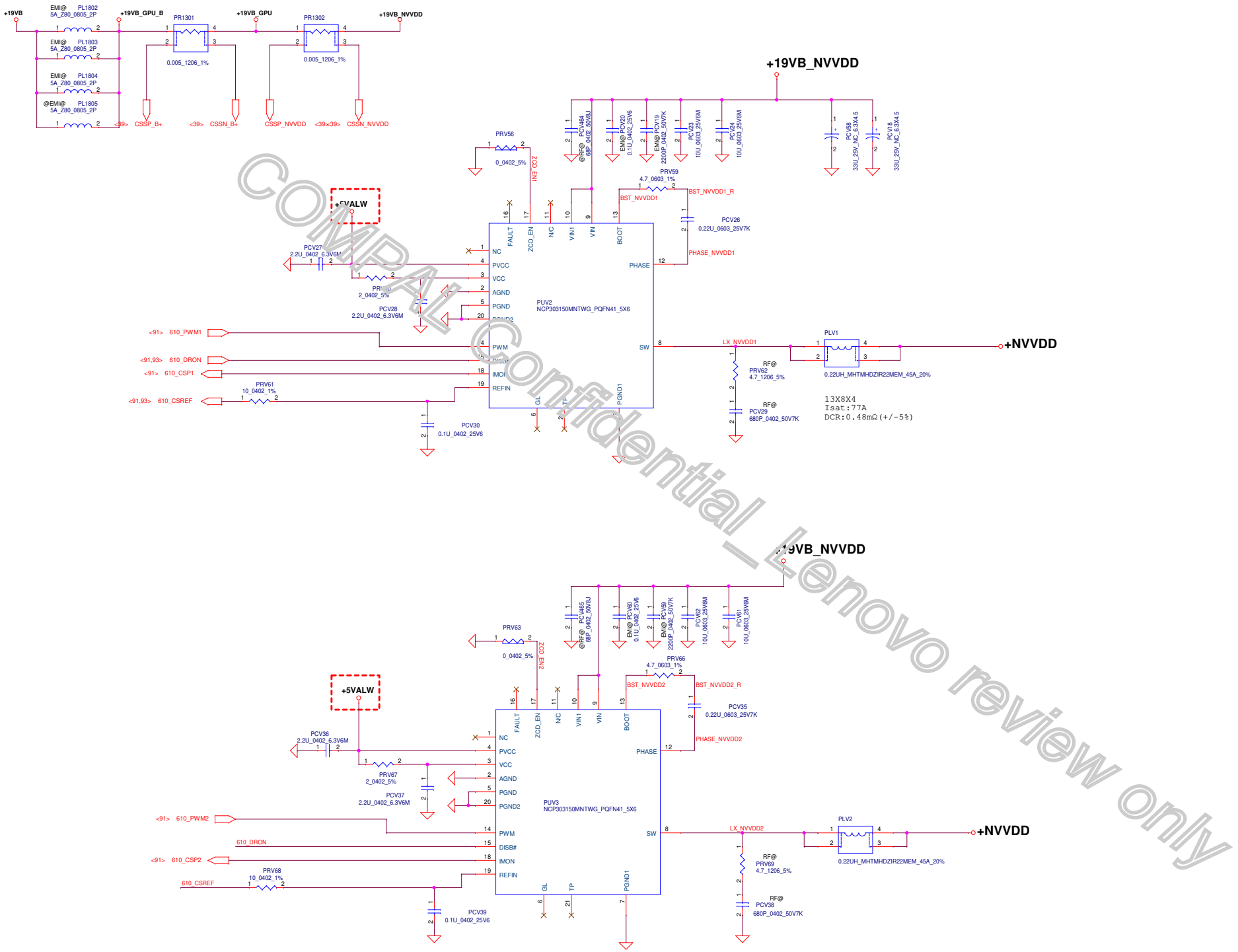
Compal Electronics, Inc.			
Title	VGA-NCP81611		
Size	Document Number		Rev 0.2
Date: Wednesday, February 26, 2020	Sheet 91 of 100		



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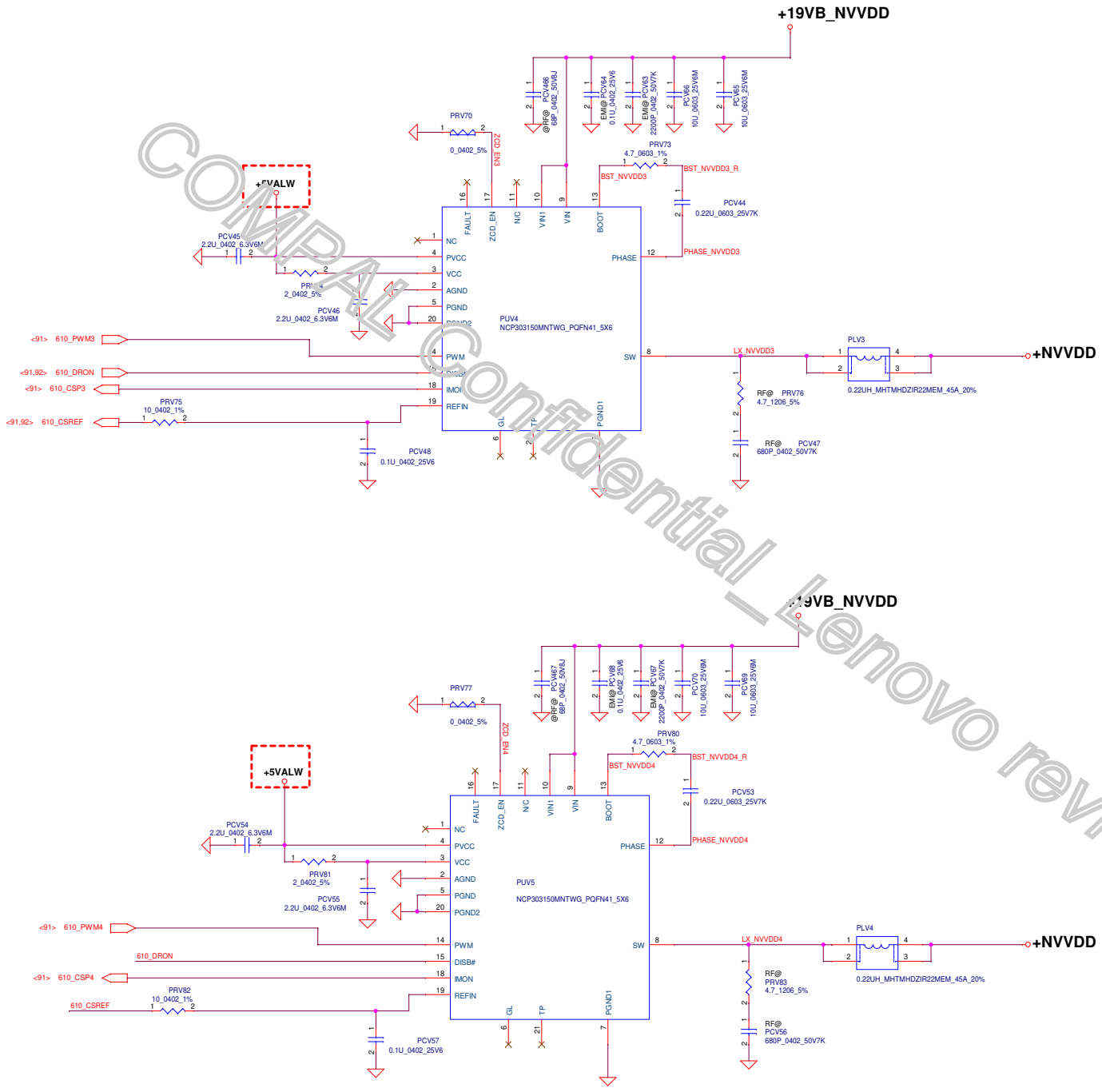
Compal Electronics, Inc.			
Title	PWR-NVVDD1		
Size	Document Number		Rev 0.2
Date: Wednesday, February 26, 2020	Sheet 92 of 100		



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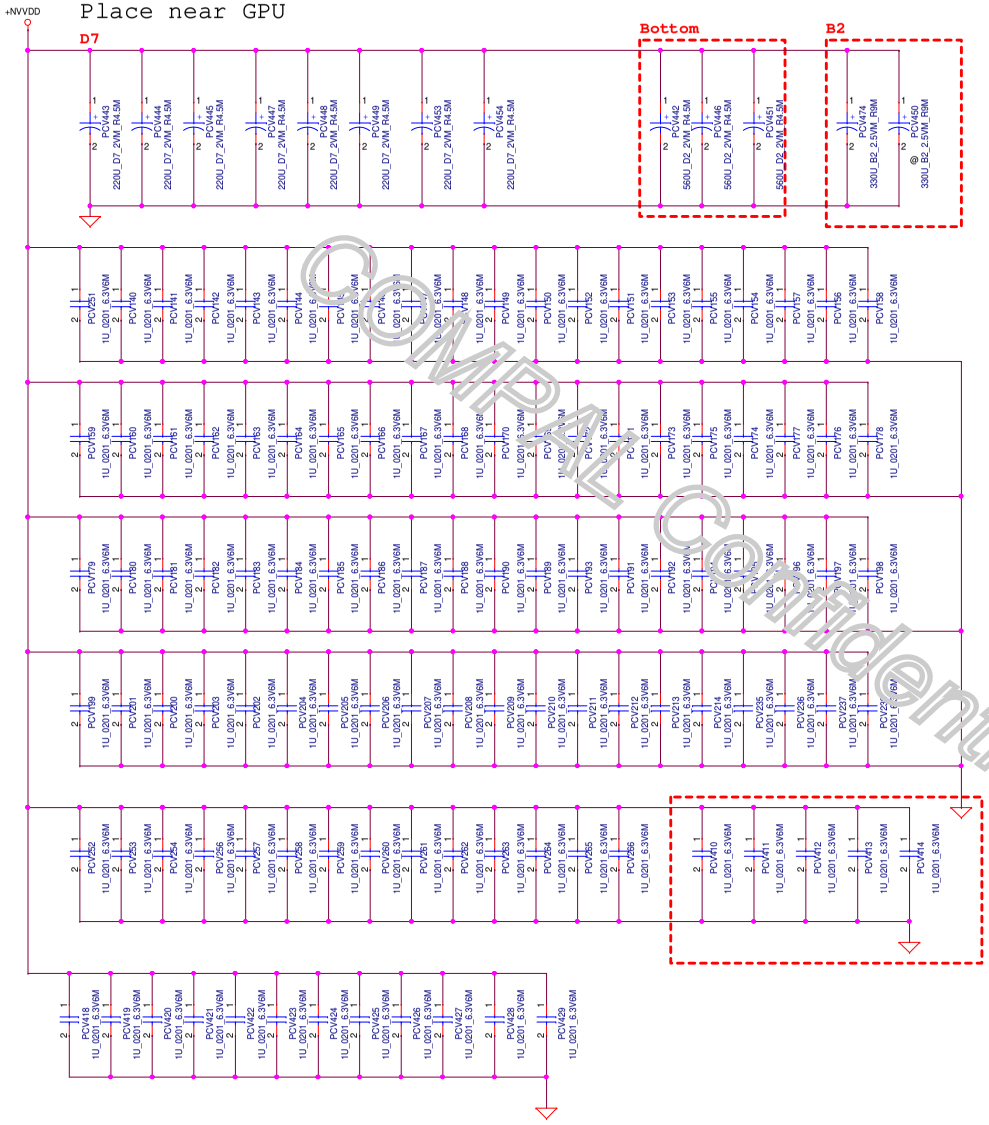
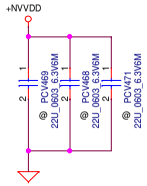
Compal Electronics, Inc.

Title: **PWR-NVVDD2**

Size	Document Number	Rev
		0.2

Date: Wednesday, February 26, 2020 | Sheet 93 of 100



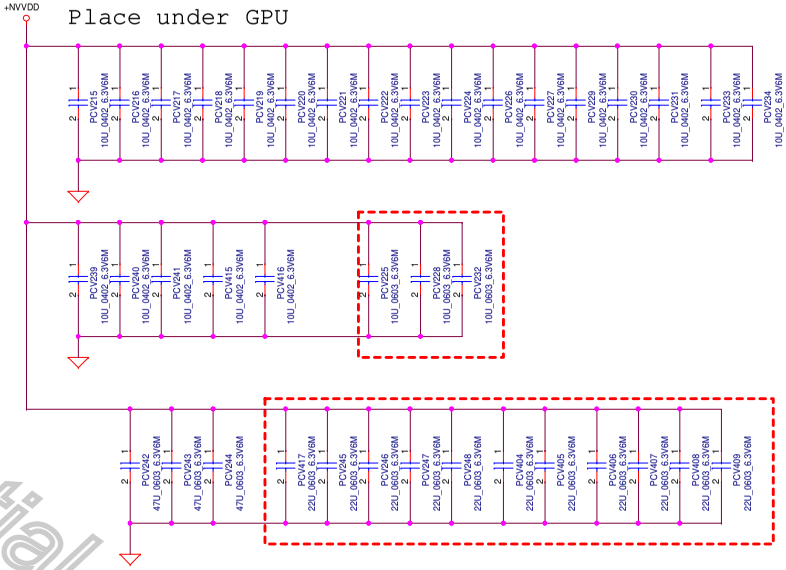


N18E-G3
+NVVDD
220uF X 8
560uF X 3
330uF X 1
47uF_0603 X 3
22uF_0603 X 11
10uF_0402X 22
1uF_0201 X 111
10uF_0603 X 3

N18E-G2
+NVVDD
470uF X 2
330uF X 6
47uF_0603 X 3
22uF_0603 X 4 +7
10uF_0402X 22
1uF_0201 X 94 +17
10uF_0603 X 3

Reserve

N17E-G3
+NVVDD
470uF X 11
47uF_0805 X 3
10uF_0603X 27
4.7uF_0603 X 11
1uF_0402 X 65



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

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NVIDIA Confi
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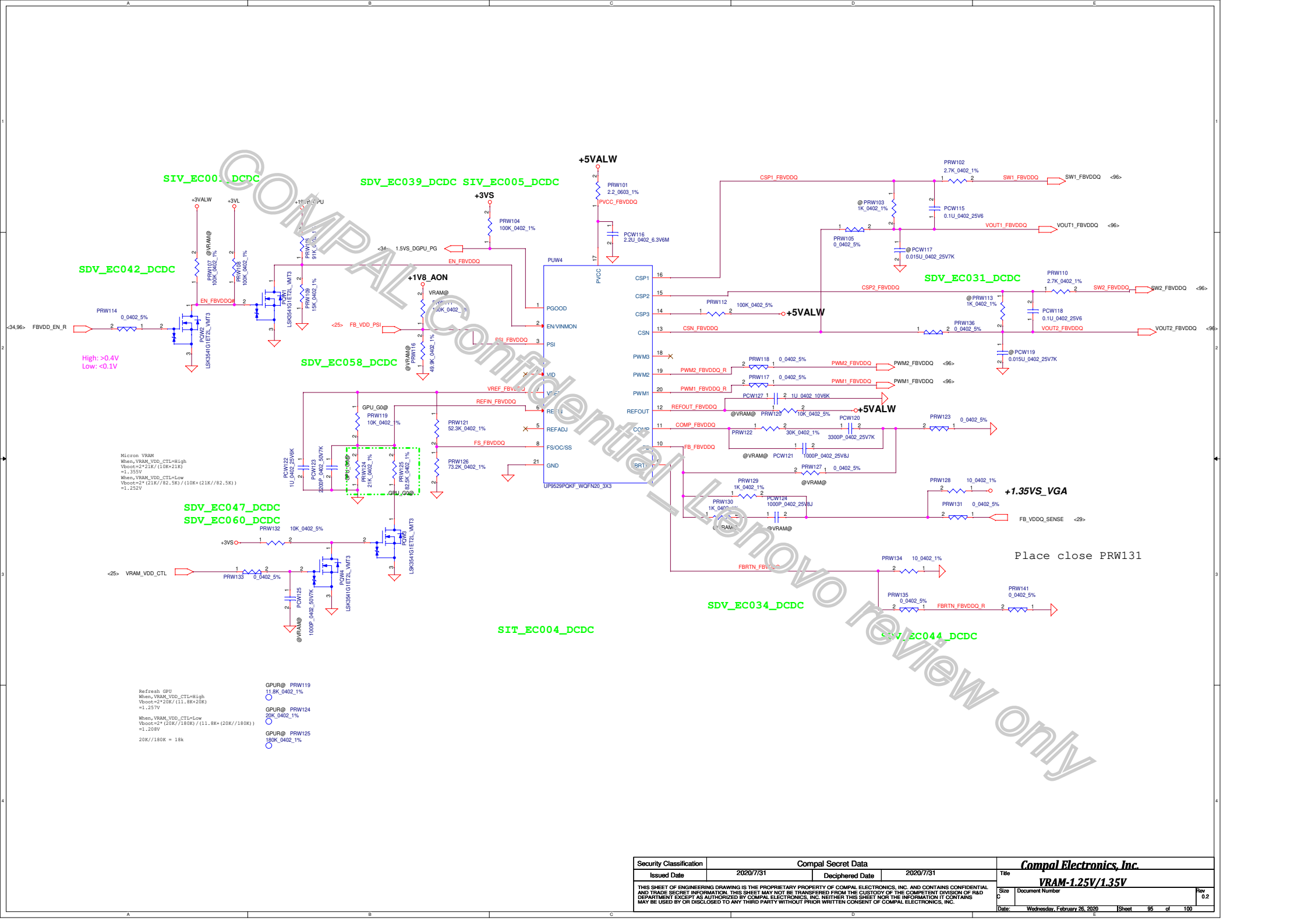
Title	PWR-VGA_DECOUPLING		
Size	Document Number		Rev
	LA-J561P		0.2
Date:	Wednesday, February 26, 2020	Sheet	94 of 100



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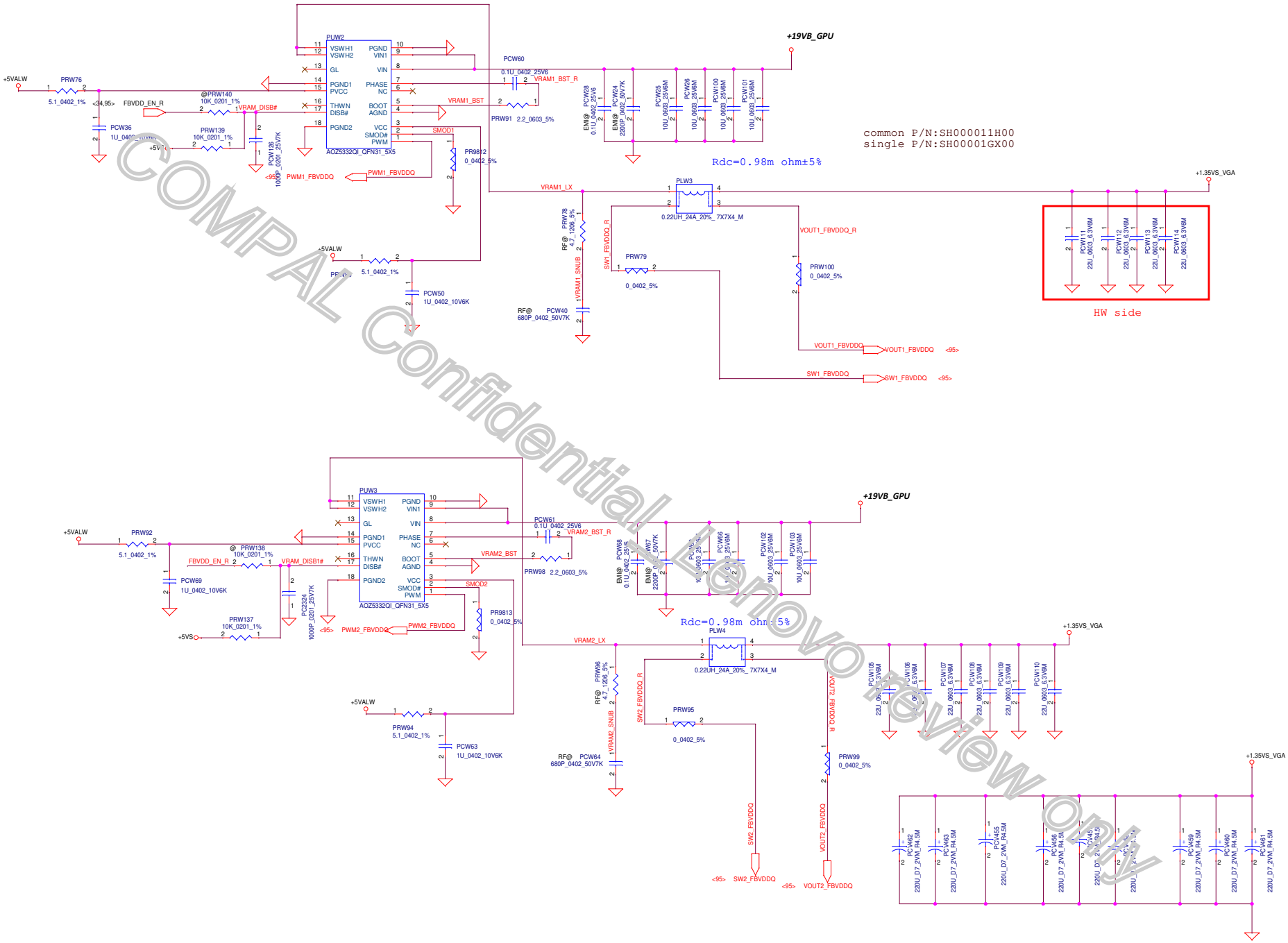
Compal Electronics, Inc.

Title: **VRAM-1.25V/1.35V**

Size	Document Number	Rev
C		0.2

Date: Wednesday, February 26, 2020 Sheet 95 of 100



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Compal Electronics, Inc.

Title: **VRAM_Power**

Size	Document Number	Rev
C		0.2

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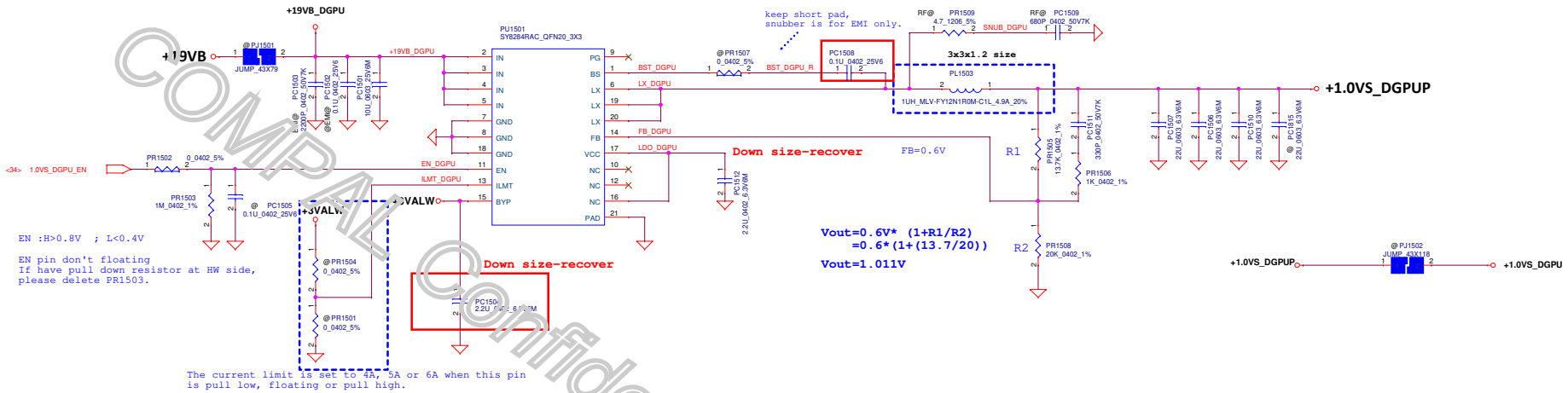
Module model information

SY8288_V2_single.mdd
SY8288_V2_dual.mdd



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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/7/31	Deciphered Date 2020/7/31	Title: PWR_1.0V_DGPU
			Size: Document Number: Rev: 0.2
			Date: Wednesday, February 26, 2020 Sheet 97 of 100

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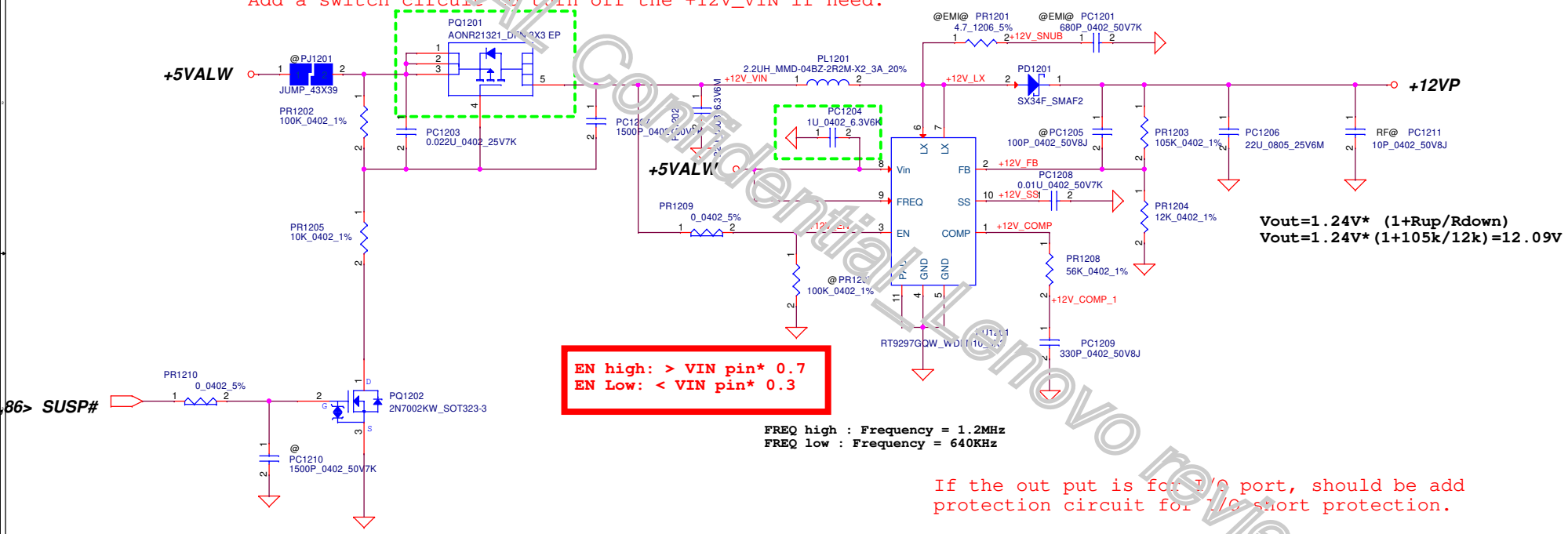
Module model information

RT9297_V1.mdd

Must check PL501 and PD501 rating
for your application.

Add a switch circuit to turn off the +12V_VIN if need.



Vout=1.24V* (1+Rup/Rdown)
Vout=1.24V*(1+105k/12k)=12.09V

EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add protection circuit for I/O short protection.

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Compal Electronics, Inc.

Title: **PWR- 12V**

Size: Custom | Document Number: **LA-J561P** | Rev: 0.2

Date: Wednesday, February 26, 2020 | Sheet 98 of 100

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	2512 size is X1 code	92	PR1301 & PR1302 From 0.005_2512_1% change to 0.005_1206_1%	9/25	SIV
2	Refresh GPU, VRAM Voltage change	95	Add BOM Structure GPUR@ (PRW119 = 11.8k , PRW124 = 20k , PRW125 = 180k)	9/25	SIV
3	Sourcer suggest	91	PCV1 From SE068221J80 (220P 25V J NPO 0402) change to SE082221J80 (220P 50V J NPO 0402) PC303 From SE025102J80 (1000P 50V J X7R 0603) change to SE025102K80 (1000P 50V K X7R 0603)	9/27	SIV
4	EMI suggest		PL501 , PLZ1 , PLZ2 , PL203 & PL204 From SM01000U600 (5A_Z80_0805_2P) change to SM01000EJ00 (HCB2012KF-221T30_2P) Add PLZ3 & PL206 (SM01000EJ00, HCB2012KF-221T30_2P) Add PCZ112 , PC333 , PC334 , PC335(SE074471K80 ,470P_0402_50V7K) Change PR316 from 0 ohm to 2.2_0603_5% Mount PC306,(SE074152K80 1500P_0402_50V7K) PJ701 change to PL701 (SM01000EJ00, HCB2012KF-221T30_2P) Add PC209 , PC210(0.01U_0402_50V7K)	9/27	SIV
5	RTCVTT change, For CML	82	PR208 change to 0_0603_5% , Unmount PR209	9/27	SIV
6	CPU Test result	88	Change PR136 from 165K_0402 to 143K_0402 , Change PR139 from 78.7K_0402 to 90.9K_0402	10/14	SIV
7	Auto PSI function	91	Change PRV88 from 20K_0402 to 24.9K_0402 , Change PRV89 from 10K_0402 to 13.3K_0402	10/14	SIV
8	DCR sense fine tuning	95	Change PRW102, PRW110 from 2.26K_0402 to 2.7K_0402	10/14	SIV
9	Uniform size	96	Change PR9812,PR9813 from 0_0201 to 0_0402_5%	11/29	SIT
10	RF suggest	84,85,98	Add PC1211 , PC421 & PC527 , (10P_0402_50V8J)	11/29	SIT
11	CPU Test result , Part count reduce	90	Unmount PC900,PC902,PC930	12/03	SIT
12	For CPU PRPCHOT issue	83	Unmount PR351, PC318	12/04	SIT
13	Part count reduce	83,88,90, 95,98	PR90 , PR94 , PR107 , PR111 , PR114 , PR117 , PRV5 , PRV7 , PRV9 , PRV11 , PRV13 , PRV17 PRW114 , PRW135 , PRW131 , PRW135 , PRW141 , PR1209 , PR1210 , PR348 , PR 349 From 0_0402_5% change to R-short.	2020/01/17	SVT
14	Part count reduce	95, 96	PR9812, PR9813, PRW79, PRW100, PRW95, PRW99, PRW117, PRW118, PRW123, PR208, PR412 ,PR413, PR701, PR715, PR1807, PR1502 From 0_0402_5% change to R-short.	2020/01/20	SVT
15	Part count reduce		PR103,PR322,PR352,PR354,PR414,PRV28,PRW105,PRW136,PRW141,PR1055,PR317 From 0_0402_5% change to R-short.	2020/02/25	SVT
16	Cost Down	83	Unmount PQ314 , PQ315 ,PR338	2020/02/25	SVT
16	For ACS5 ID pin issue	82	Unmount PR207 , Mount PR211	2020/02/26	SVT

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Title: **PWR-PIR**

Size	Document Number	Rev
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Title	PWR-Reserve		
Size A	Document Number LA-J561P		Rev 0.2
Date: Wednesday, February 26, 2020		Sheet 100 of 100	