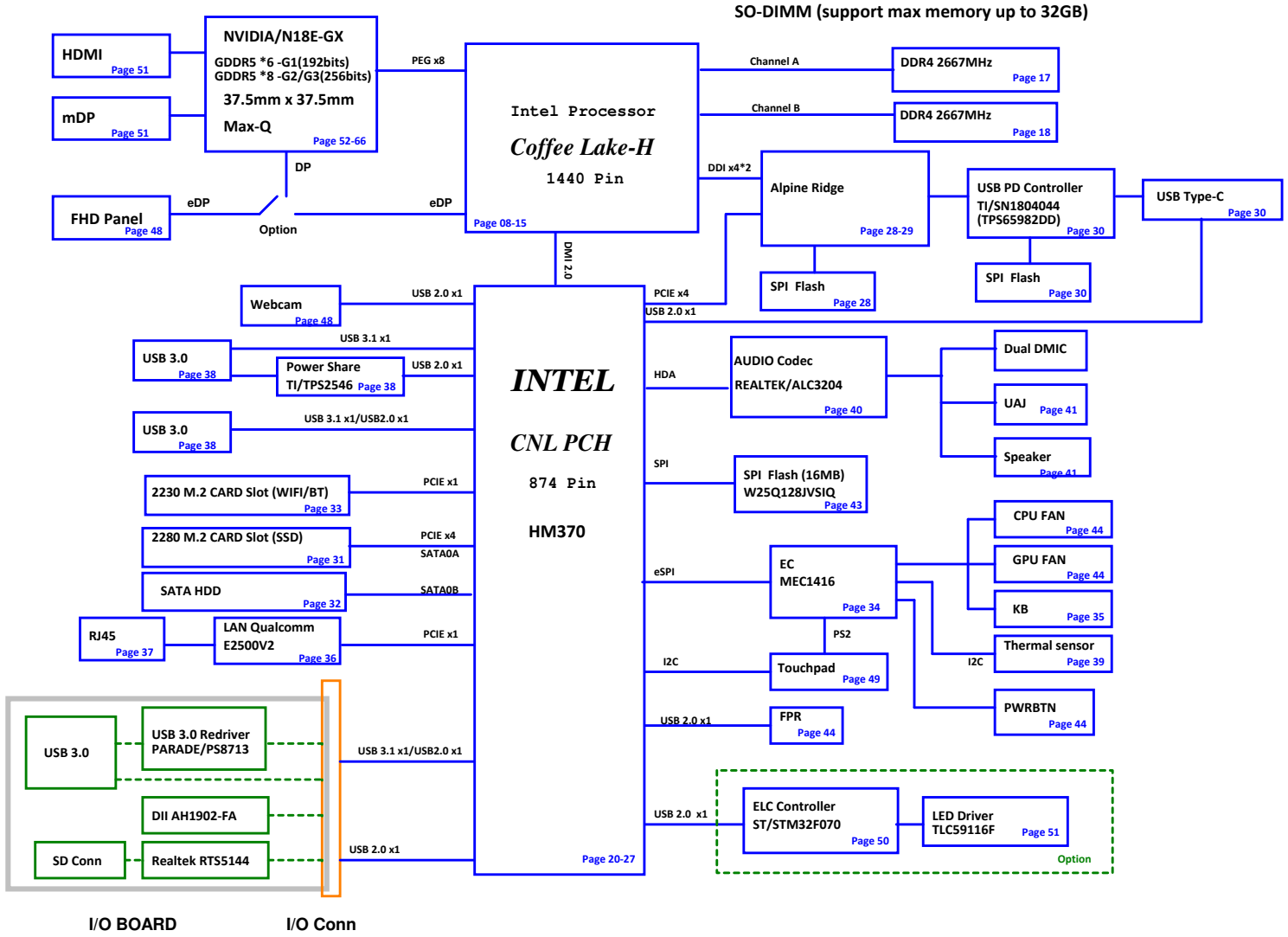
Vulcan (Coffee Lake-H)Revision_1.0

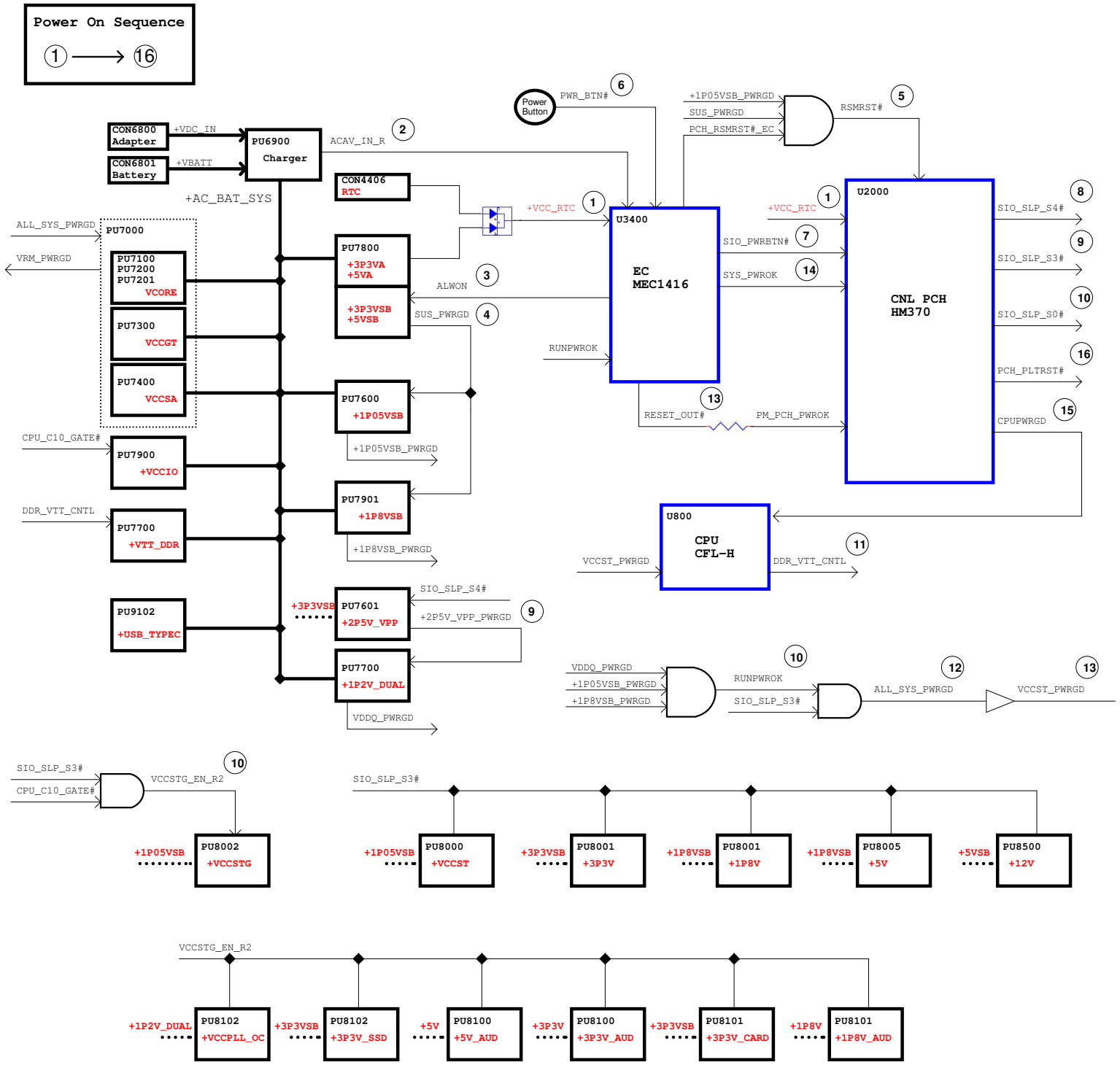


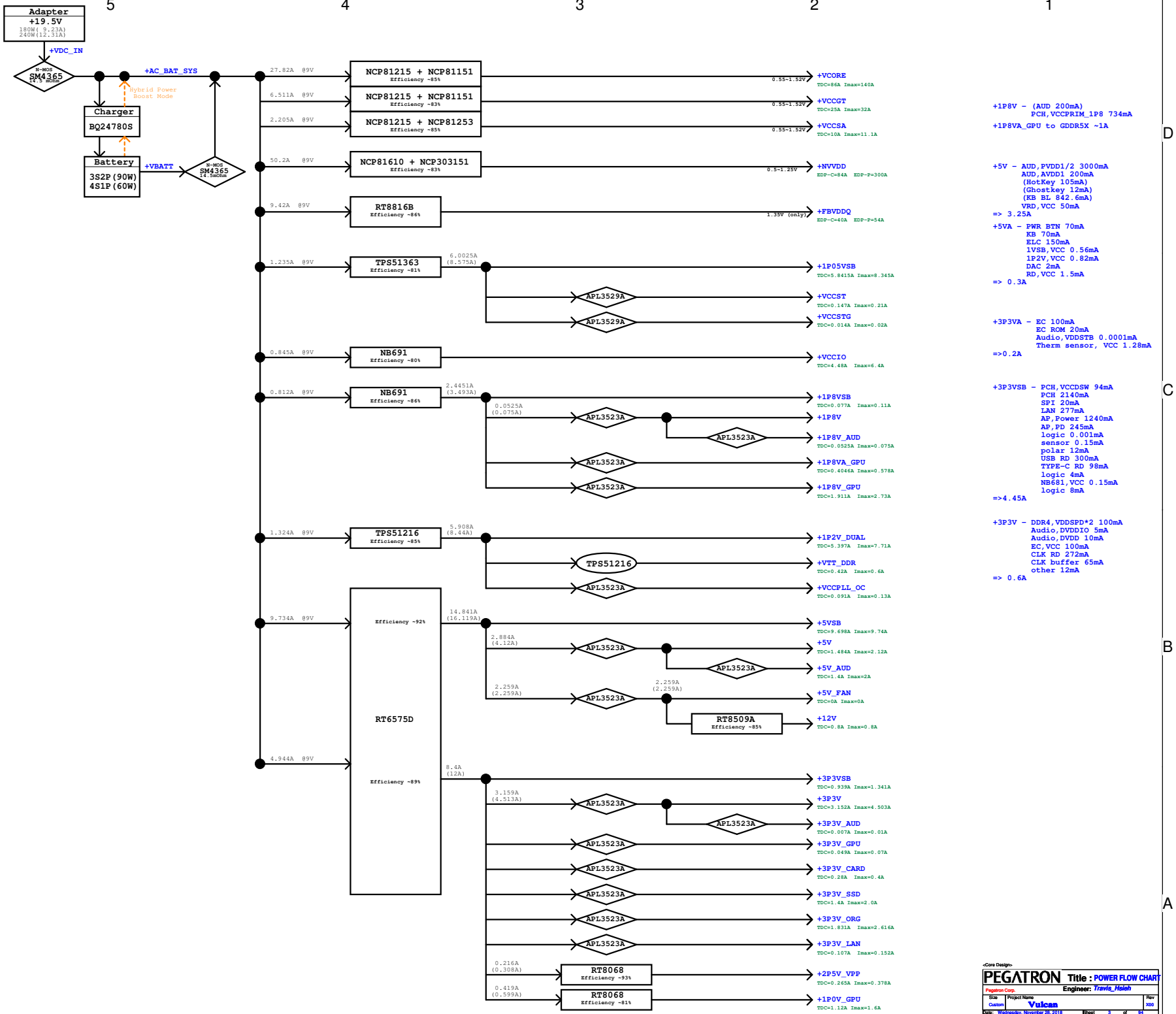
PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
C	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 1 of 94


Power On Sequence
1 → 16
Power Button
PWR_BTN#
6
+1P05VSB_PWRGD
SUS_PWRGD
PCH_RSMRST#_EC
RSMRST#
5
CON6800 Adapter
CON6801 Battery
+VDC_IN
+VBATT
PU6900 Charger
ACAV_IN_R
2
+AC_BAT_SYS
CON4406 RTC
+VCC_RTC
1
U3400
EC MEC1416
U2000
CNL PCH HM370
SIO_SLP_S4#
8
SIO_SLP_S3#
9
SIO_SLP_S0#
10
PCH_PLTRST#
16
CPUPWRGD
15
SIO_PWRBTN#
7
SYS_PWROK
14
ALL_SYS_PWRGD
VRM_PWRGD
PU7000
PU7100 PU7200 PU7201 VCORE
PU7300 VCCGT
PU7400 VCCSA
PU7800 +3P3VA +5VA
+3P3VSB +5VSB
ALWON
3
SUS_PWRGD
4
RUNPWROK
RESET_OUT#
13
PM_PCH_PWROK
PU7600 +1P05VSB
+1P05VSB_PWRGD
CPU_C10_GATE#
PU7900 +VCCIO
DDR_VTT_CNTL
PU7700 +VTT_DDR
PU7901 +1P8VSB
+1P8VSB_PWRGD
U800
CPU CFL-H
VCCST_PWRGD
DDR_VTT_CNTL
11
PU9102 +USB_TYPEC
+3P3VSB
PU7601 +2P5V_VPP
SIO_SLP_S4#
+2P5V_VPP_PWRGD
9
PU7700 +1P2V_DUAL
VDDQ_PWRGD
VDDQ_PWRGD
+1P05VSB_PWRGD
+1P8VSB_PWRGD
RUNPWROK
SIO_SLP_S3#
10
ALL_SYS_PWRGD
12
VCCST_PWRGD
13
SIO_SLP_S3#
CPU_C10_GATE#
10
VCCSTG_EN_R2
+1P05VSB
PU8002 +VCCSTG
SIO_SLP_S3#
+1P05VSB
PU8000 +VCCST
+3P3VSB
PU8001 +3P3V
+1P8VSB
PU8001 +1P8V
+1P8VSB
PU8005 +5V
+5VSB
PU8500 +12V
VCCSTG_EN_R2
+1P2V_DUAL
PU8102 +VCCPLL_OC
+3P3VSB
PU8102 +3P3V_SSD
+5V
PU8100 +5V_AUD
+3P3V
PU8100 +3P3V_AUD
+3P3VSB
PU8101 +3P3V_CARD
+1P8V
PU8101 +1P8V_AUD
PEGATRON
Title : SIGNAL&RESET MAP
Pegatron Corp.
Engineer: Travis_Haleh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 2 of 94


Adapter
+19.5V
180W(9.23A)
240W(12.31A)
+VDC_IN
N-MOS
SM4365
14.5 mOhm
+AC_BAT_SYS
Hybrid Power Boost Mode
Charger
BQ24780S
Battery
3S2P(90W)
4S1P(60W)
+VBATT
N-MOS
SM4365
14.5mOhm
27.82A @9V
NCP81215 + NCP81151
Efficiency ~85%
0.55~1.52V
+VCORE
TDC=86A Imax=140A
6.511A @9V
NCP81215 + NCP81151
Efficiency ~83%
0.55~1.52V
+VCCGT
TDC=25A Imax=32A
2.205A @9V
NCP81215 + NCP81253
Efficiency ~85%
0.55~1.52V
+VCCSA
TDC=10A Imax=11.1A
50.2A @9V
NCP81610 + NCP303151
Efficiency ~83%
0.5~1.25V
+NVVDD
EDP-C=84A EDP-P=300A
9.42A @9V
RT8816B
Efficiency ~86%
1.35V (only)
+FBVDDQ
EDP-C=40A EDP-P=54A
1.235A @9V
TPS51363
Efficiency ~81%
6.0025A
(8.575A)
+1P05VSB
TDC=5.8415A Imax=8.345A
APL3529A
+VCCST
TDC=0.147A Imax=0.21A
APL3529A
+VCCSTG
TDC=0.014A Imax=0.02A
0.845A @9V
NB691
Efficiency ~80%
+VCCIO
TDC=4.48A Imax=6.4A
0.812A @9V
NB691
Efficiency ~86%
2.4451A
(3.493A)
+1P8VSB
TDC=0.077A Imax=0.11A
0.0525A
(0.075A)
APL3523A
+1P8V
APL3523A
+1P8V_AUD
TDC=0.0525A Imax=0.075A
APL3523A
+1P8VA_GPU
TDC=0.4046A Imax=0.578A
APL3523A
+1P8V_GPU
TDC=1.911A Imax=2.73A
1.324A @9V
TPS51216
Efficiency ~85%
5.908A
(8.44A)
+1P2V_DUAL
TDC=5.397A Imax=7.71A
TPS51216
+VTT_DDR
TDC=0.42A Imax=0.6A
APL3523A
+VCCPLL_OC
TDC=0.091A Imax=0.13A
9.734A @9V
Efficiency ~92%
14.841A
(16.119A)
+5VSB
TDC=9.698A Imax=9.74A
2.884A
(4.12A)
APL3523A
+5V
TDC=1.484A Imax=2.12A
APL3523A
+5V_AUD
TDC=1.4A Imax=2A
2.259A
(2.259A)
APL3523A
2.259A
(2.259A)
+5V_FAN
TDC=0A Imax=0A
RT8509A
Efficiency ~85%
+12V
TDC=0.8A Imax=0.8A
RT6575D
4.944A @9V
Efficiency ~89%
8.4A
(12A)
+3P3VSB
TDC=0.939A Imax=1.341A
3.159A
(4.513A)
APL3523A
+3P3V
TDC=3.152A Imax=4.503A
APL3523A
+3P3V_AUD
TDC=0.007A Imax=0.01A
APL3523A
+3P3V_GPU
TDC=0.049A Imax=0.07A
APL3523A
+3P3V_CARD
TDC=0.28A Imax=0.4A
APL3523A
+3P3V_SSD
TDC=1.4A Imax=2.0A
APL3523A
+3P3V_ORG
TDC=1.831A Imax=2.616A
APL3523A
+3P3V_LAN
TDC=0.107A Imax=0.152A
0.216A
(0.308A)
RT8068
Efficiency ~93%
+2P5V_VPP
TDC=0.265A Imax=0.378A
0.419A
(0.599A)
RT8068
Efficiency ~81%
+1P0V_GPU
TDC=1.12A Imax=1.6A
+1P8V - (AUD 200mA)
PCH,VCCPRIM_1P8 734mA
+1P8VA_GPU to GDDR5X ~1A
+5V - AUD,PVDD1/2 3000mA
AUD,AVDD1 200mA
(HotKey 105mA)
(Ghostkey 12mA)
(KB BL 842.6mA)
VRD,VCC 50mA
=> 3.25A
+5VA - PWR BTN 70mA
KB 70mA
ELC 150mA
1VSB,VCC 0.56mA
1P2V,VCC 0.82mA
DAC 2mA
RD,VCC 1.5mA
=> 0.3A
+3P3VA - EC 100mA
EC ROM 20mA
Audio,VDDSTB 0.0001mA
Therm sensor, VCC 1.28mA
=>0.2A
+3P3VSB - PCH,VCCDSW 94mA
PCH 2140mA
SPI 20mA
LAN 277mA
AP,Power 1240mA
AP,PD 245mA
logic 0.001mA
sensor 0.15mA
polar 12mA
USB RD 300mA
TYPE-C RD 98mA
logic 4mA
NB681,VCC 0.15mA
logic 8mA
=>4.45A
+3P3V - DDR4,VDDSPD*2 100mA
Audio,DVDDIO 5mA
Audio,DVDD 10mA
EC,VCC 100mA
CLK RD 272mA
CLK buffer 65mA
other 12mA
=> 0.6A
<Core Design>
PEGATRON
Title : POWER FLOW CHART
Pegatron Corp.
Engineer: Travis_Hsieh
Size
Custom
Project Name
Vulcan
Rev
X00
Date: Wednesday, November 28, 2018
Sheet 3 of 54

Schematics Change History

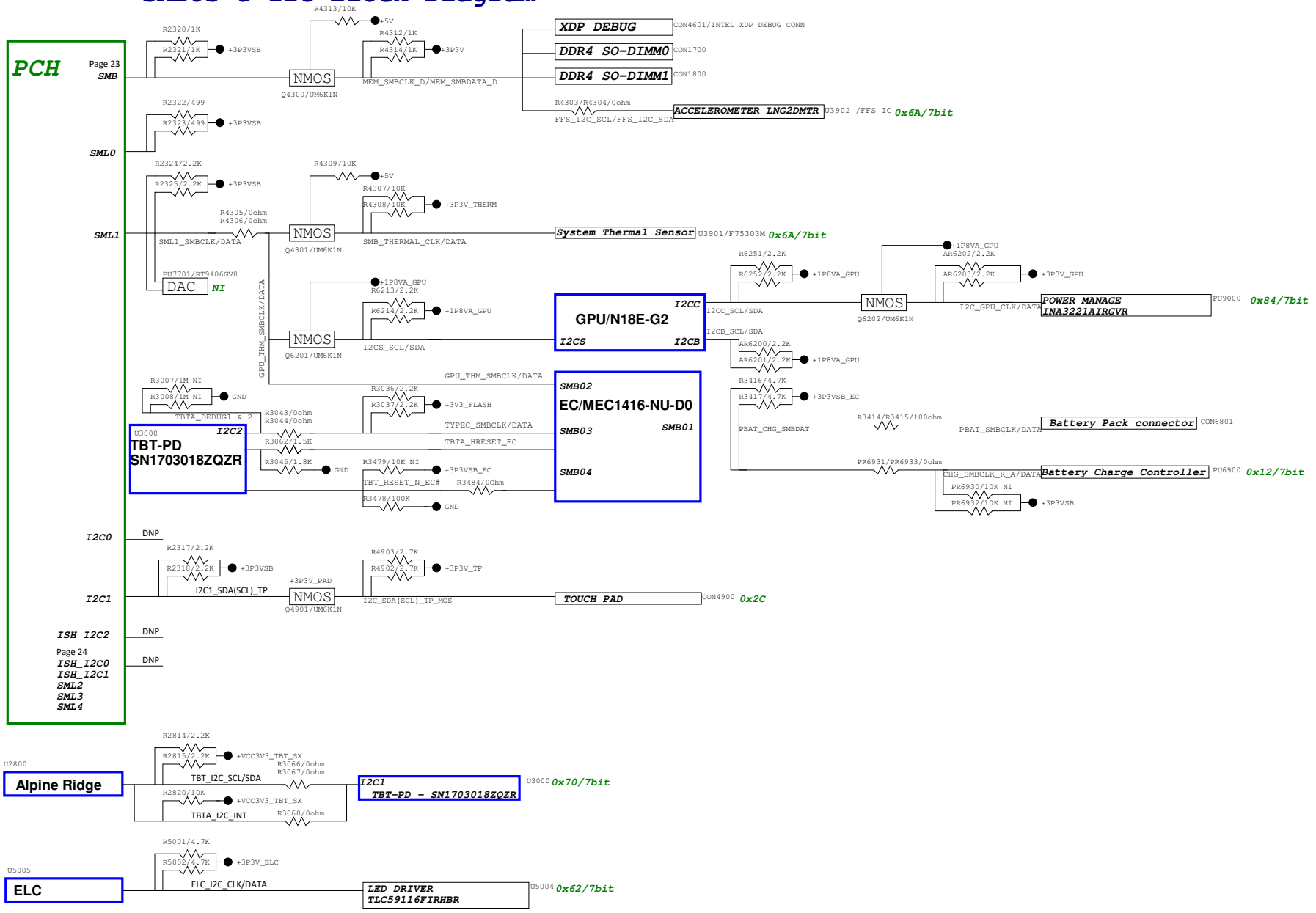
Version	Date	Description	Comments
1.00			

<Core Design>

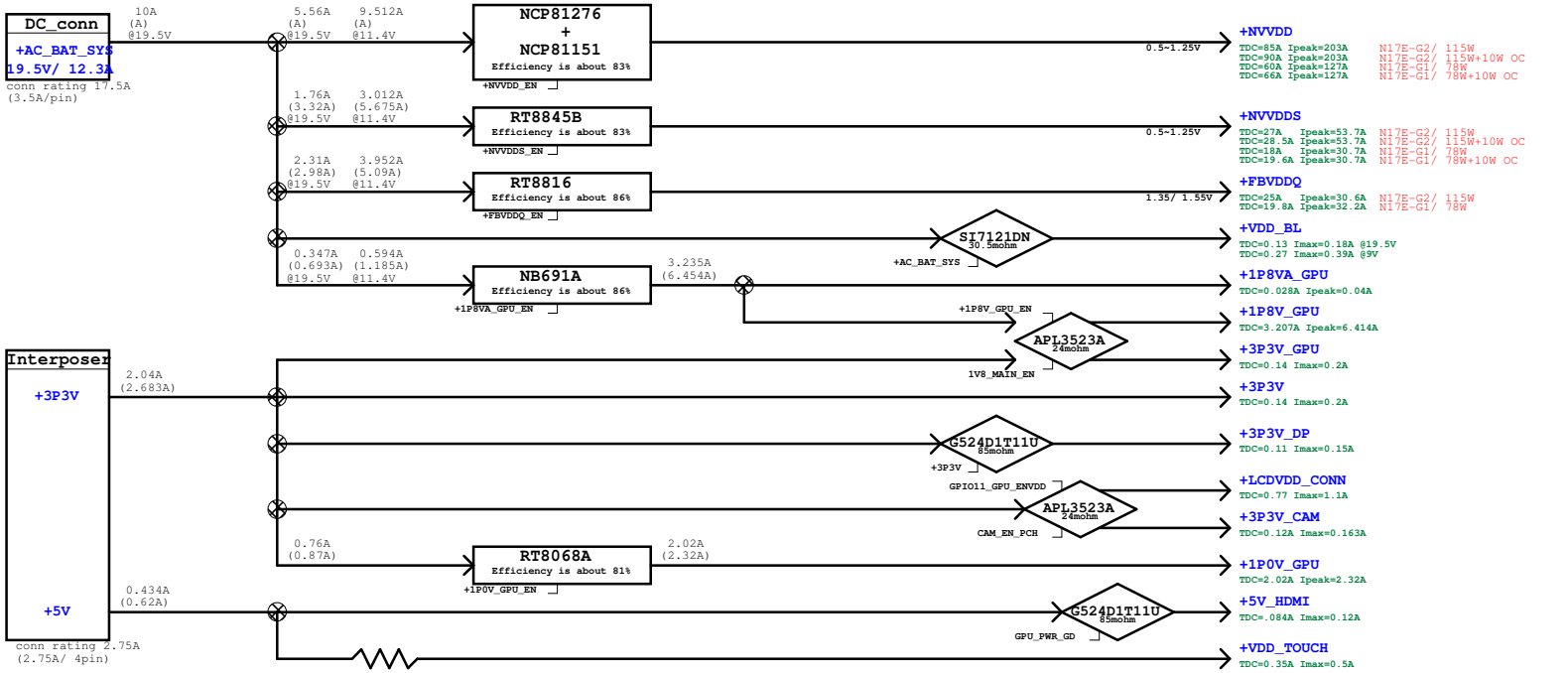
PEGATRON DT-MB RESTRICTED SECRET

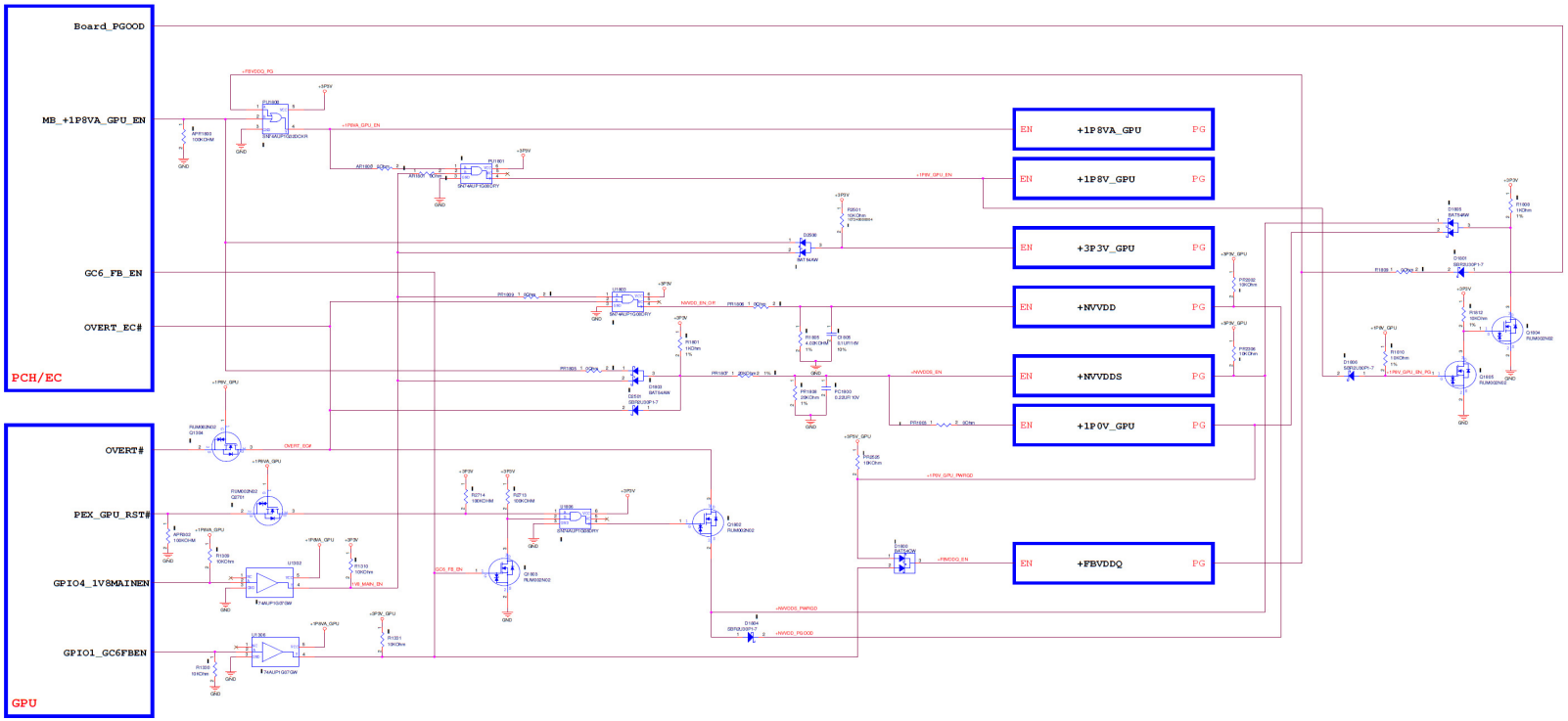
PEGATRON	Title : CHANGE HISTORY		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A3	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018		Sheet 4 of 94	

SMBUS & I2C Block Diagram



PEGATRON Title : SMBus & I2C Flow
Engineer: Travis_Hsieh





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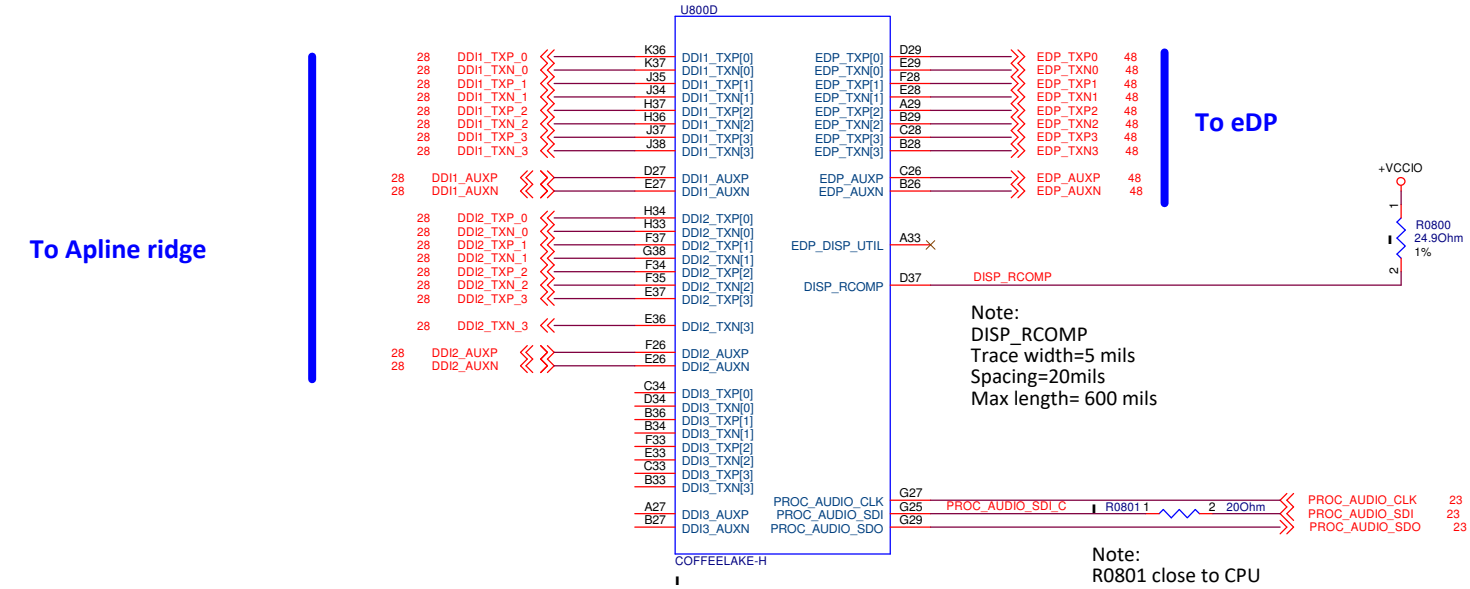
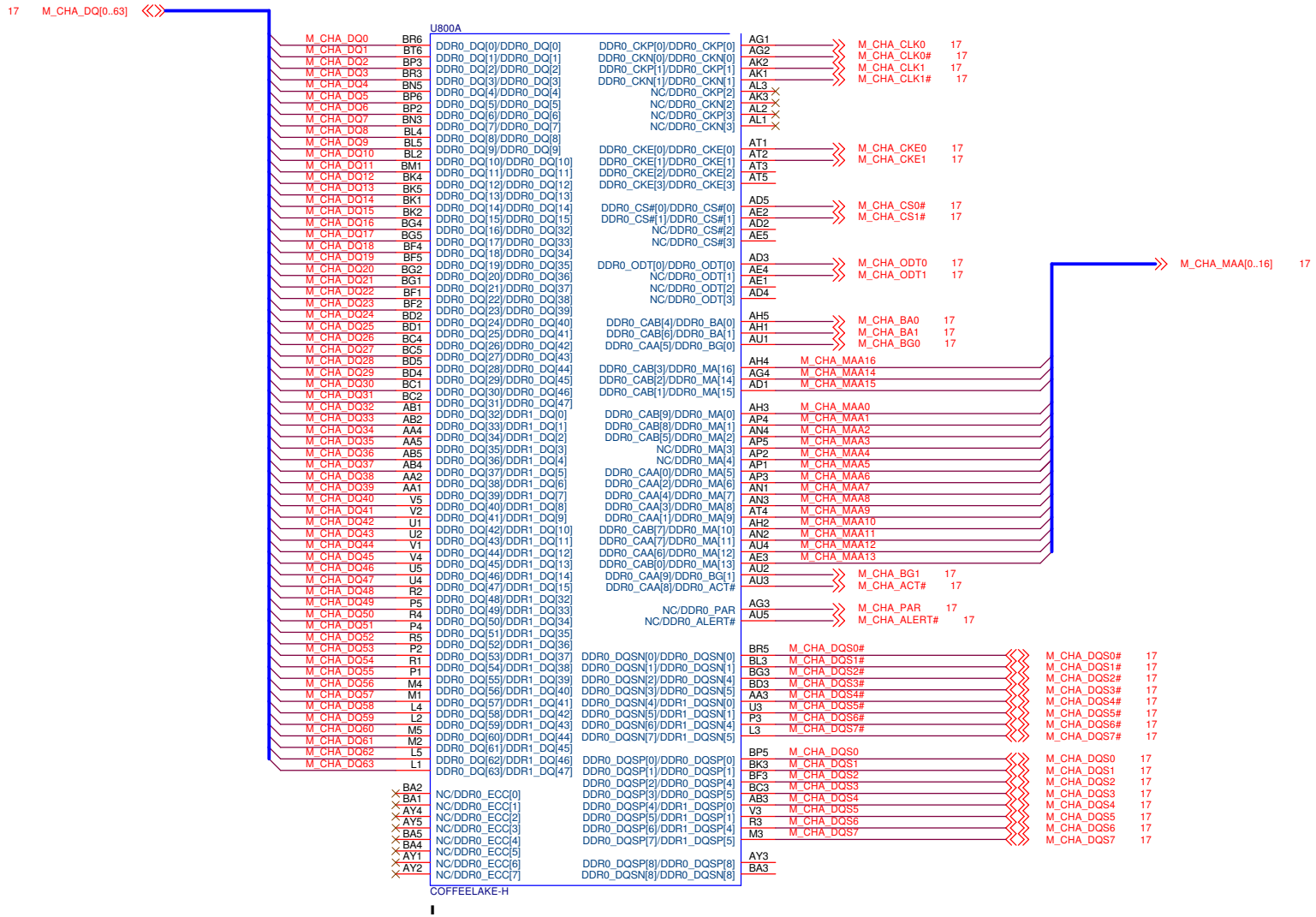
PEGATRON Title : GPU Power flow & sequence
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 6 of 94

Reserved Page



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU DDI/EDP	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 8 of 94	



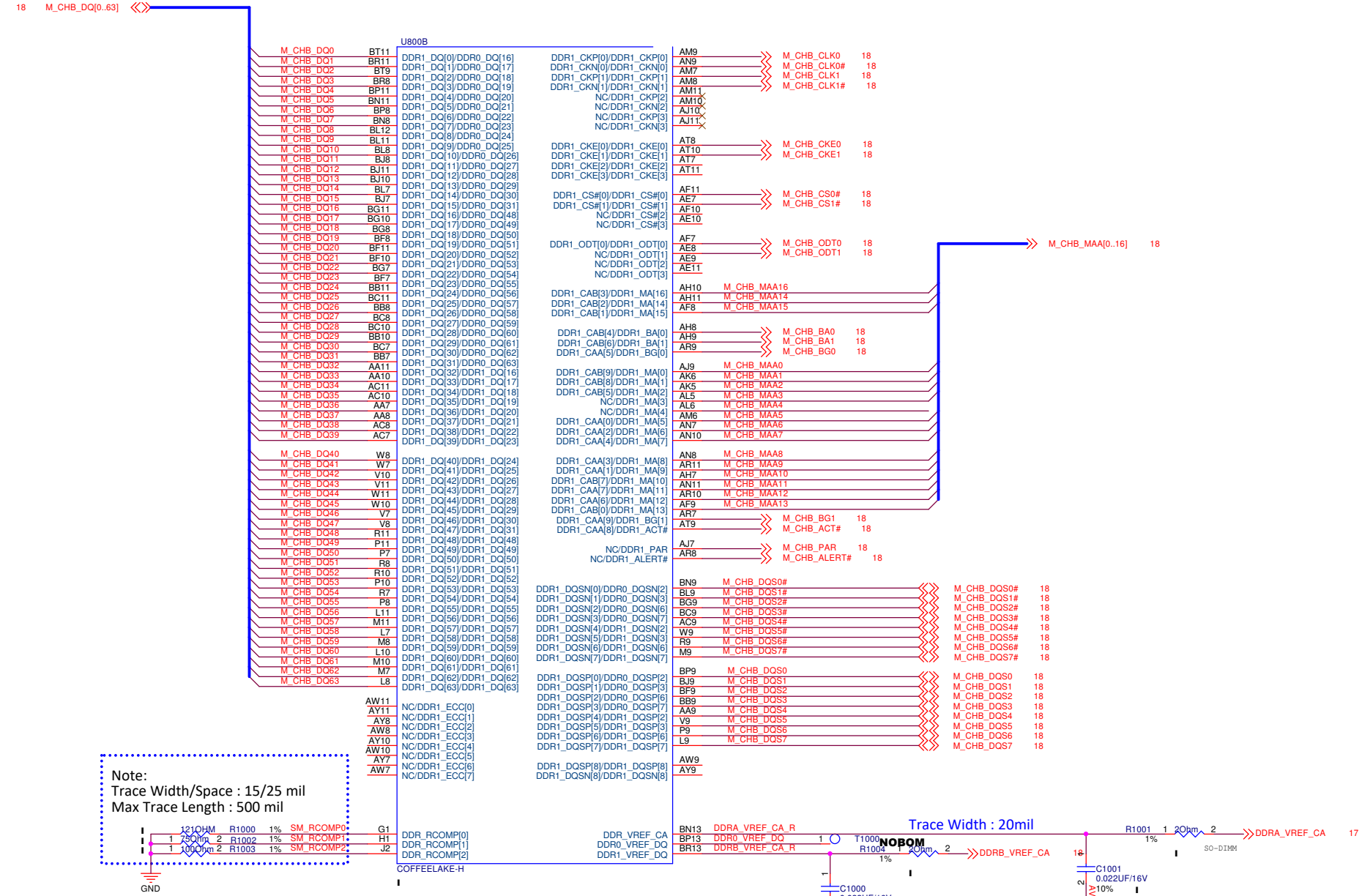
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHA

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 9 of 94



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max Length (mils)			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1]/[2]	Byte [1]/[2]	Region	Breakout [1,2]	Total		
RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121	
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75	
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

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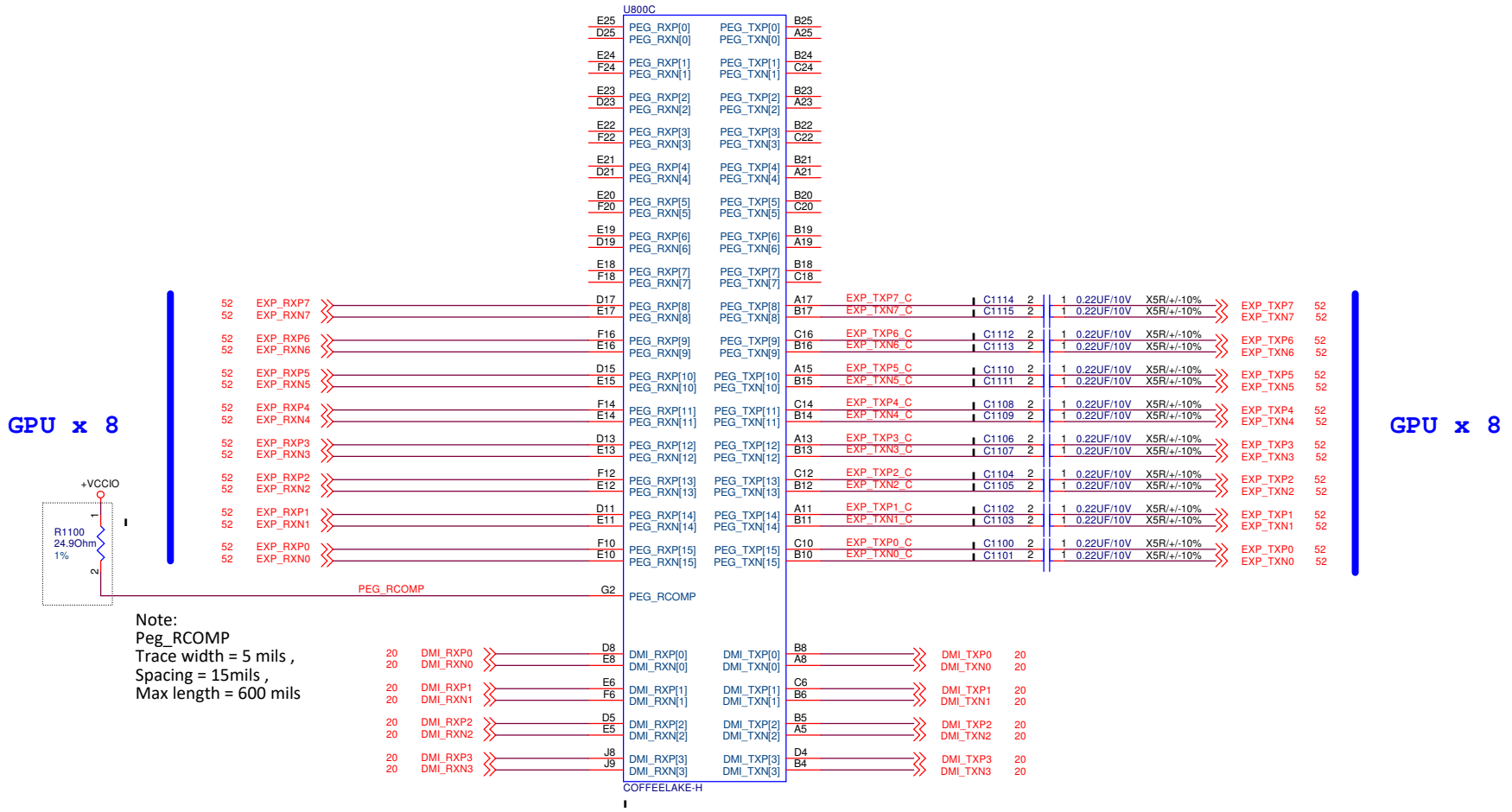


Note:
Peg_RCOMP
Trace width = 5 mils ,
Spacing = 15mils ,
Max length = 600 mils

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU PEG/DMI

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 11 of 94

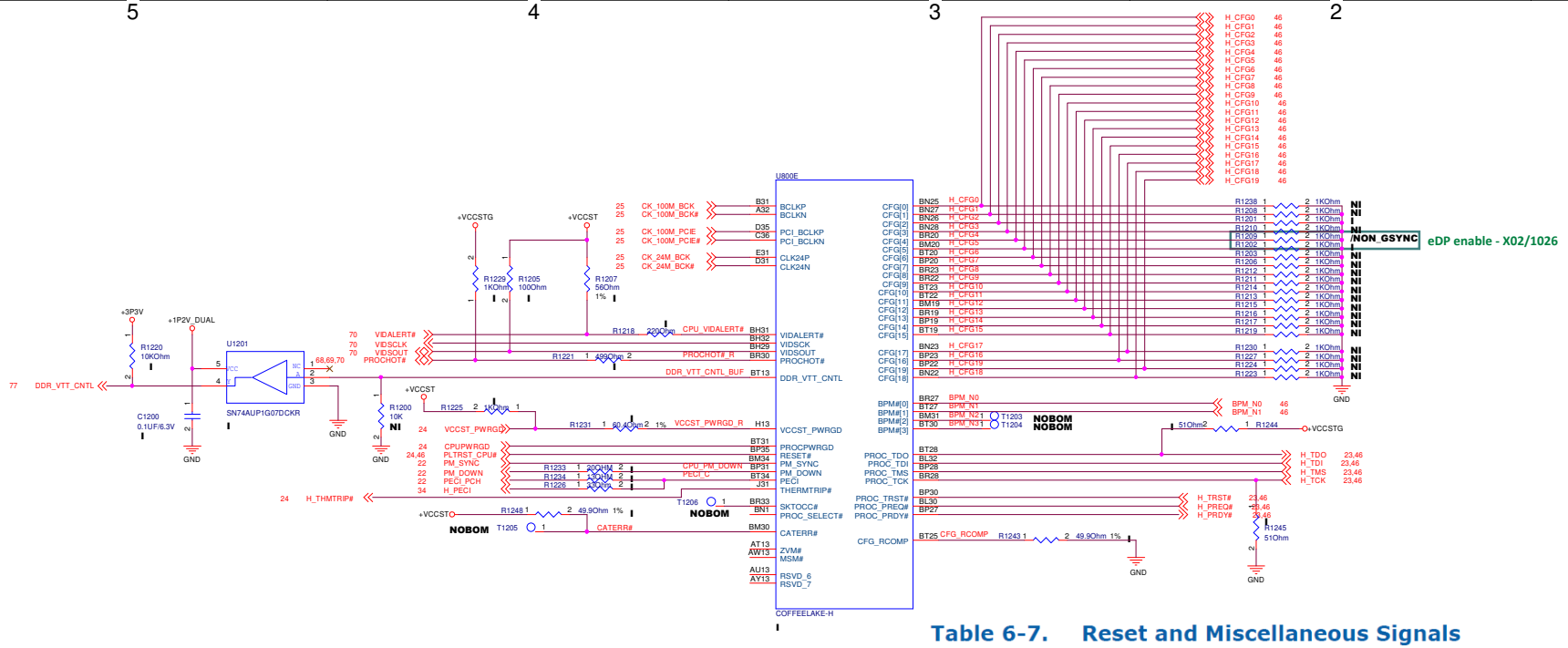


Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.

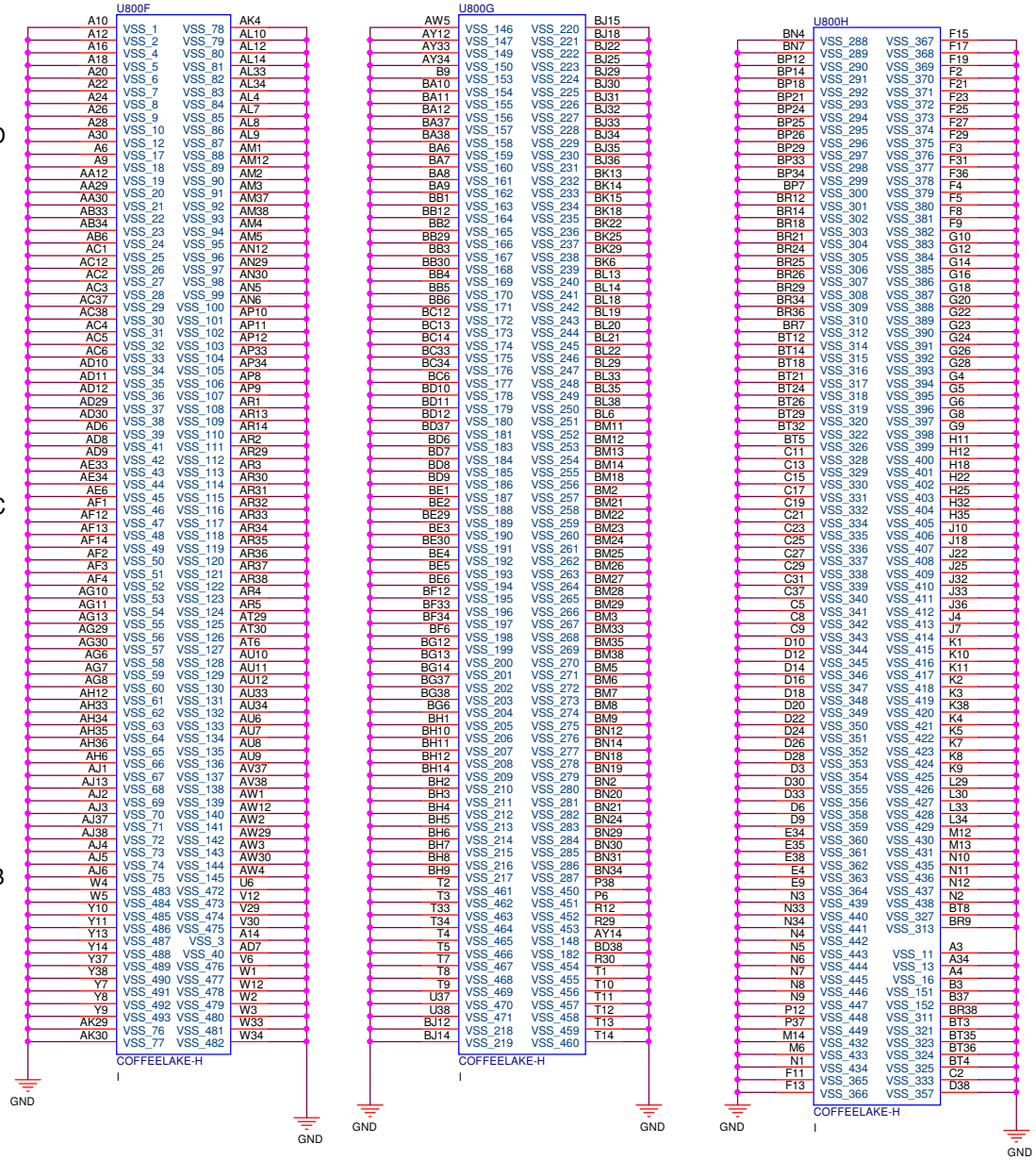
Table 6-10. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

Table 51-39. Processor/PCH Strapping Checklist (Sheet 2 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			

PEGATRON	Title : CPU other		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 12 of 94		



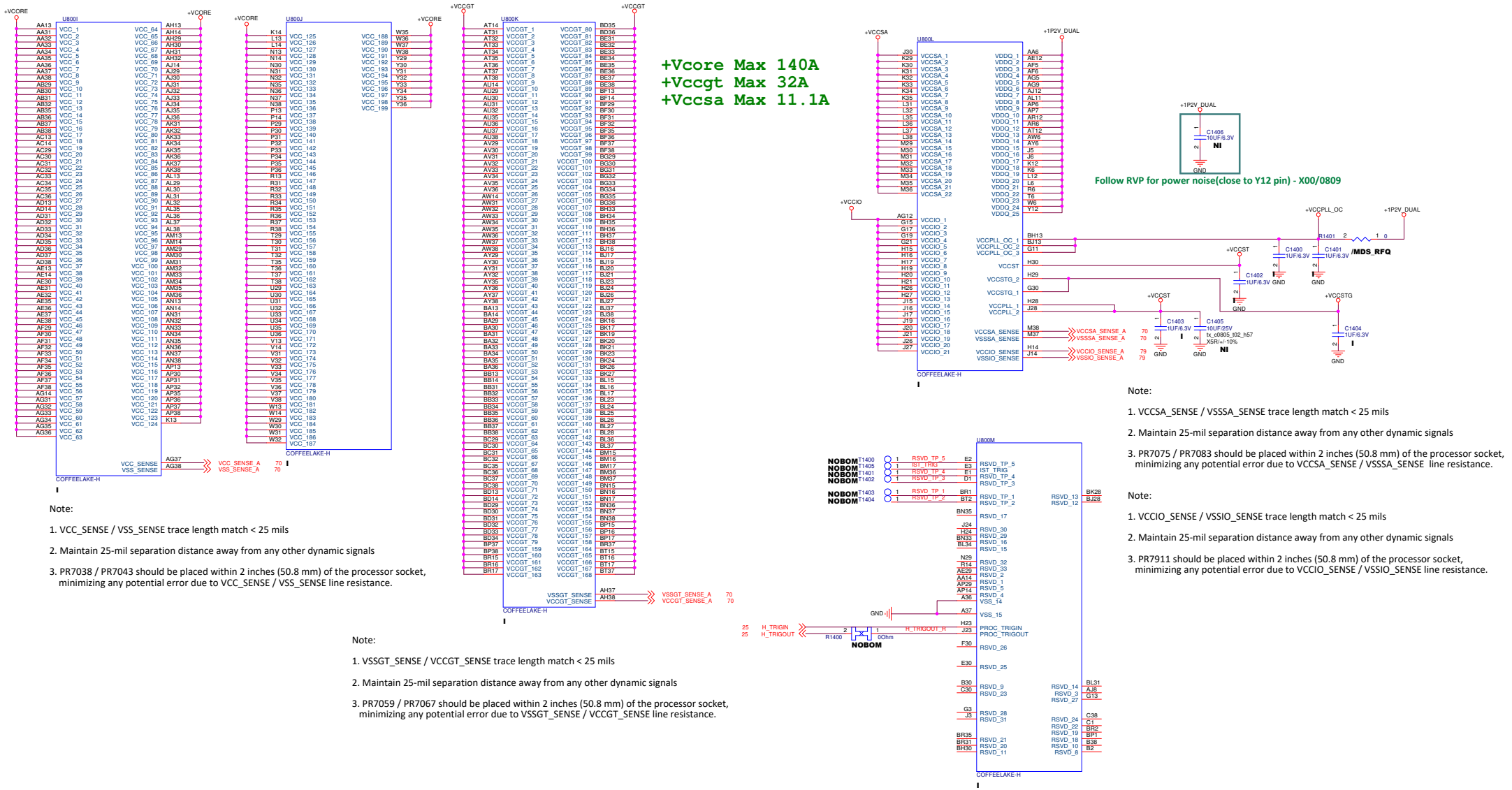
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 13 of 94



Note:

1. VCC_SENSE / VSS_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7038 / PR7043 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCC_SENSE / VSS_SENSE line resistance.

Note:

1. VSSGT_SENSE / VCCGT_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7059 / PR7067 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VSSGT_SENSE / VCCGT_SENSE line resistance.

Note:

1. VCCSA_SENSE / VSSSA_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7075 / PR7083 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCSA_SENSE / VSSSA_SENSE line resistance.

Note:

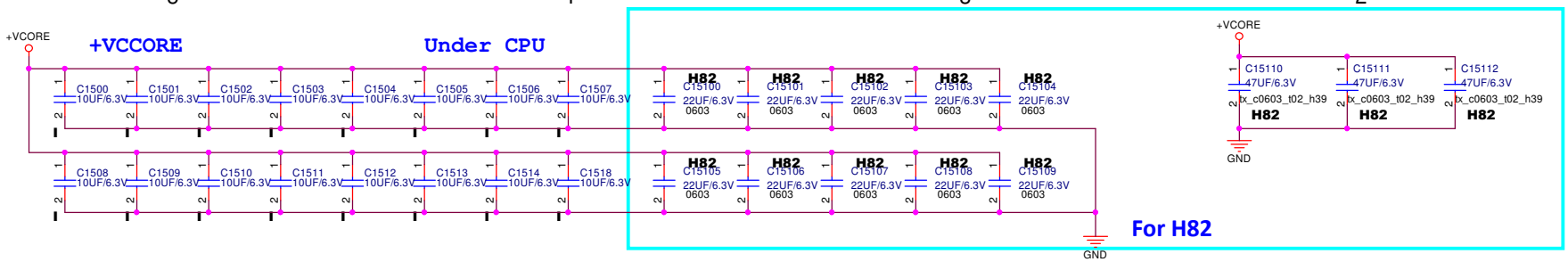
1. VCCIO_SENSE / VSSIO_SENSE trace length match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals
3. PR7911 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCIO_SENSE / VSSIO_SENSE line resistance.

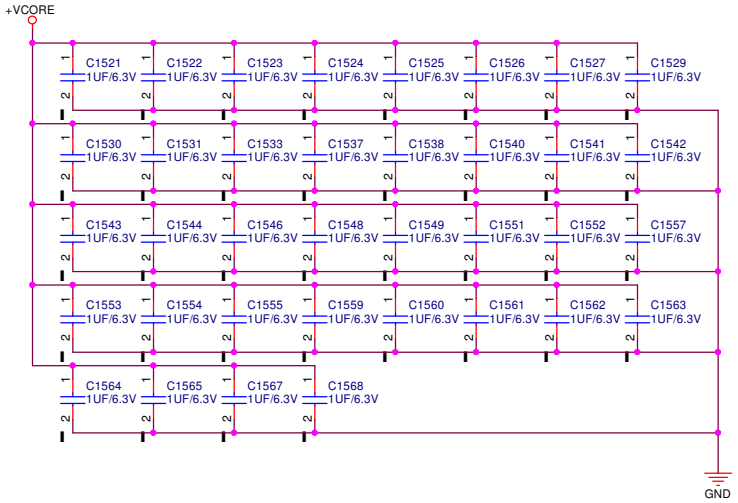
PEGATRON Title : CPU POWER

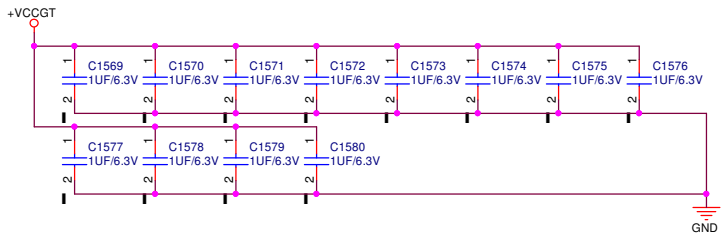
Pegatron Corp. Engineer: Travis_Hsieh

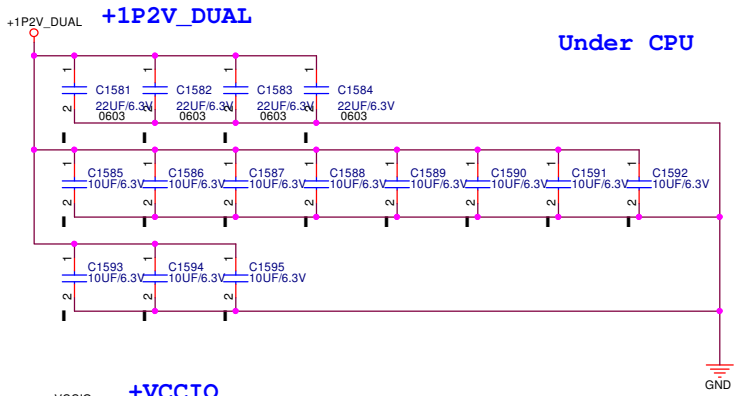
Size	Project Name	Rev
A2	Vulcan	X00

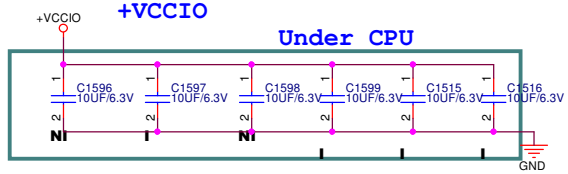
Date: Wednesday, November 28, 2018 Sheet 14 of 94











Change for power noise fail - X00/0717

Table 50-3. Decoupling Requirements for CFL H Processor

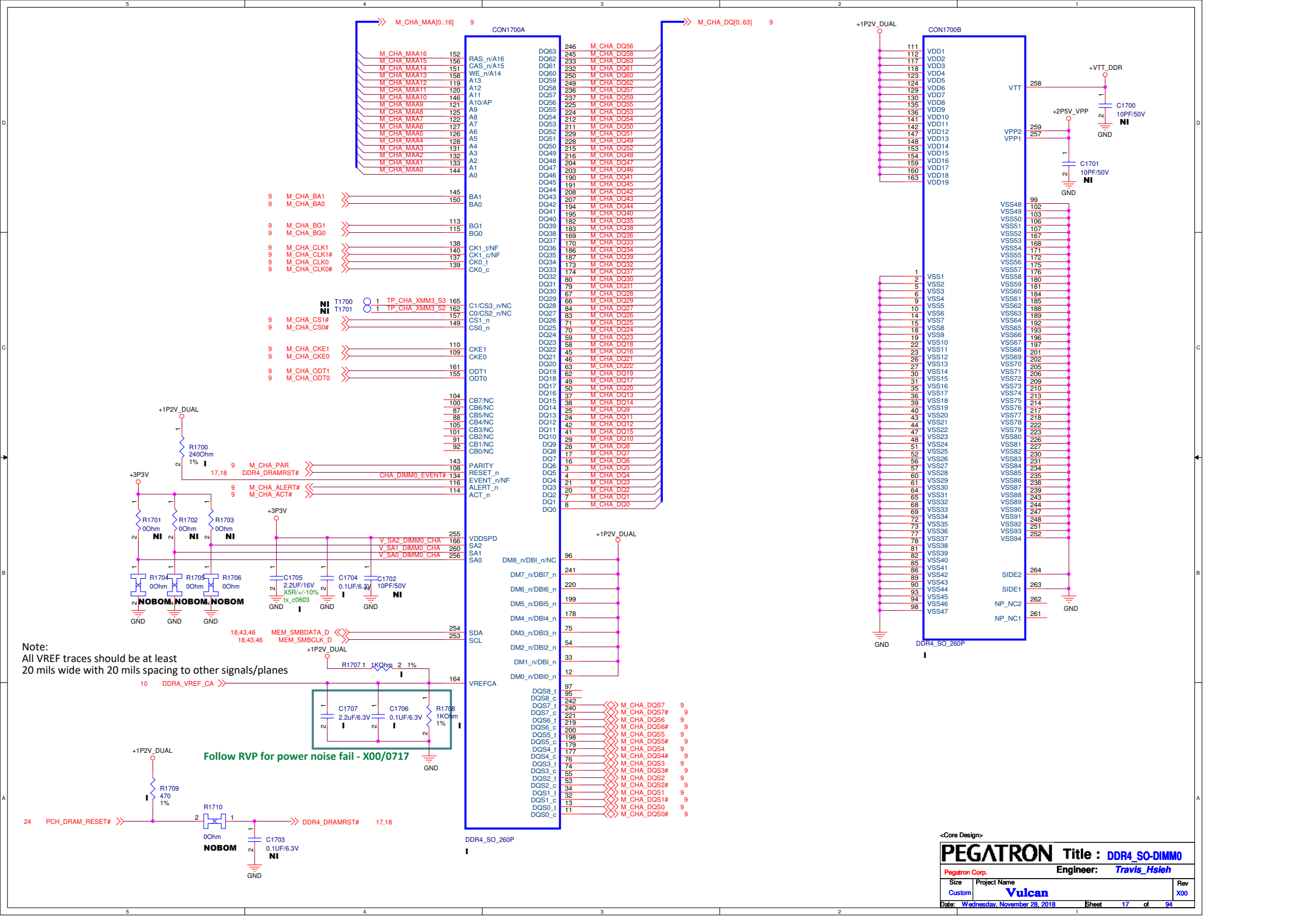
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

PEGATRON	Title : CPU DECOUPLING		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size A3	Project Name Vulcan		Rev X00
Date: Wednesday, November 28, 2018	Sheet 15 of 94		

Reserved Page

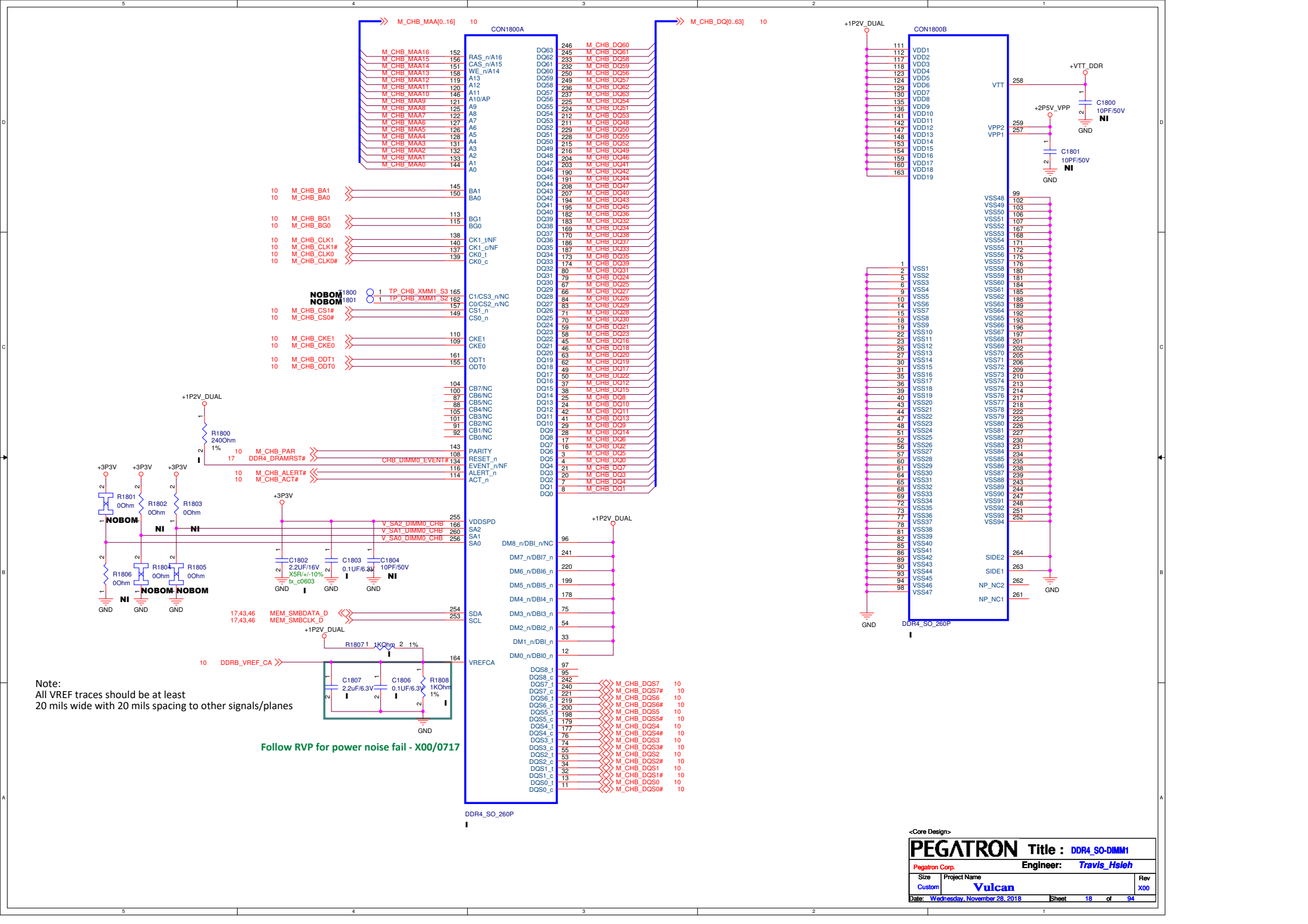
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Reserved	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 16 of 94	



<Core Design>

PEGATRON	Title : DDR4_SO-DIMM0	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 17 of 94	


M_CHB_MAA[0..16] 10
M_CHB_DQ[0..63] 10
CON1800A
CON1800B
DDR4_SO_260P
+1P2V_DUAL
+3P3V
+VTT_DDR
+2P5V_VPP
GND
NOBOM
NI
Note:
All VREF traces should be at least
20 mils wide with 20 mils spacing to other signals/planes
Follow RVP for power noise fail - X00/0717
<Core Design>
PEGATRON
Title : DDR4_SO-DIMM1
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
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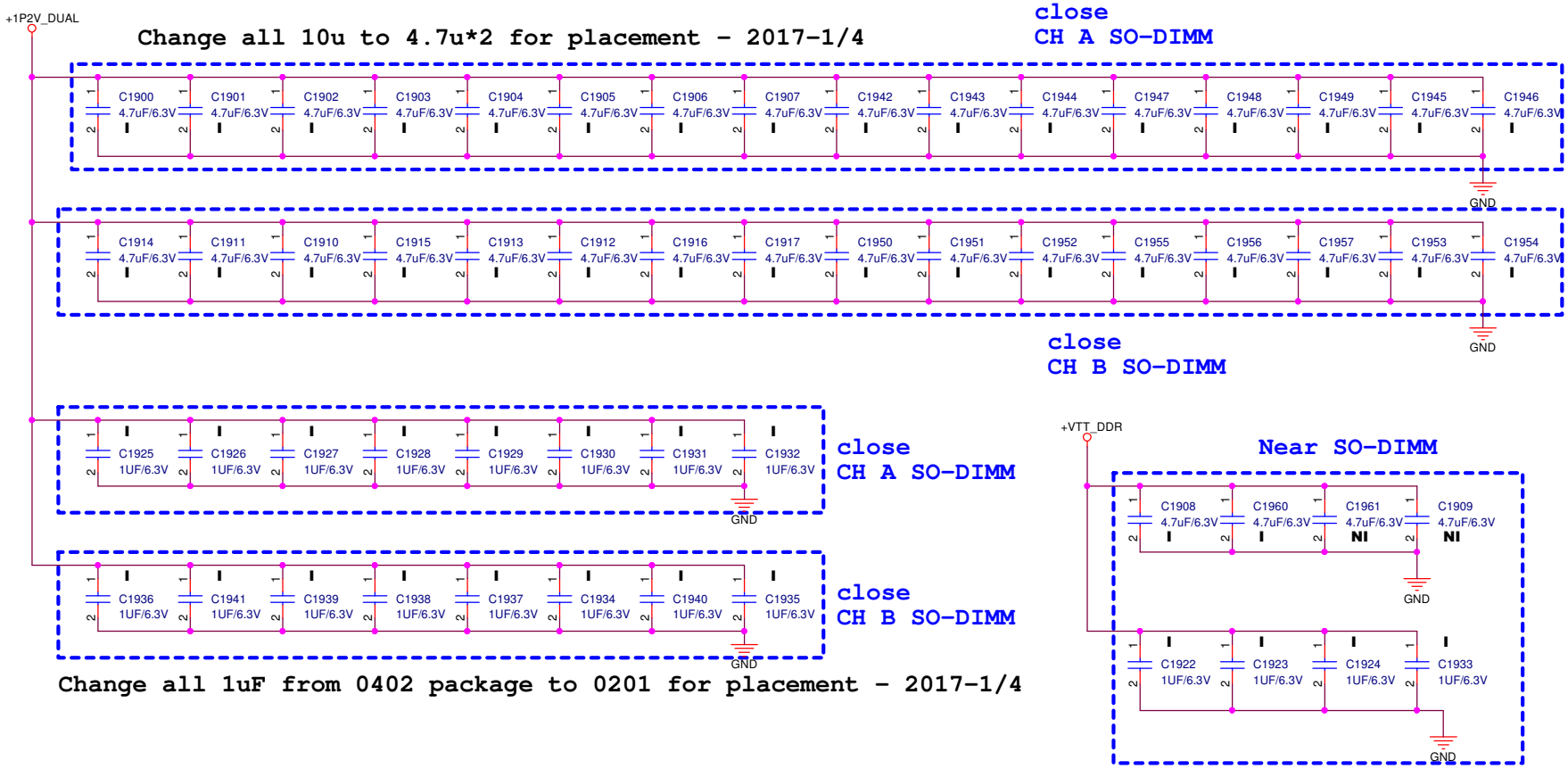
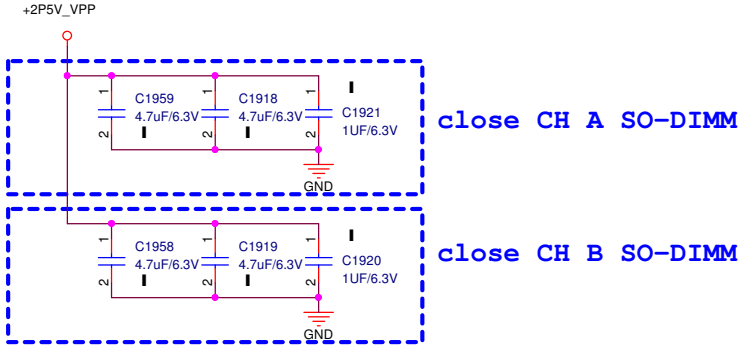


DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR DECOUPLING	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 19 of 94	

U2000A

DMI

USB2.0

PCIE/USB/SATA

USB3.1

PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE	SATA 0a		SATA 1a	SATA 0b	GbE	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7			
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

PCH-H Details	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4				PCIe* Controller #5				PCIe* Controller #6			
									Cycle Router #1								Cycle Router #3				Cycle Router #2			
Flex I/O Lane #	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HM370 1x4									RP 9				RP 13				RP 17				RP 21			
HM370 1x4 LR									RP 9				RP 13				RP 17				RP 21			
HM370 2x2									RP 9	RP 11			RP 13	RP 15			RP 17	RP 19			RP 21	RP 23		
HM370 1x2+2x1									RP 9	RP 11	RP 12		RP 13	RP 15	RP 16		RP 17	RP 19	RP 20		RP 21	RP 23	RP 24	
HM370 2x1+1x2									RP 12	RP 11	RP 9		RP 15	RP 15	RP 13		RP 20	RP 18	RP 17		RP 24	RP 23	RP 21	
HM370 4x1									RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 16	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

M.2 PCIE X4 #1

IO USB3.1(Type-A_1)

RIGHT USB3.1(Type-A) -Power share

USB3.1(Type-A Rear)

TBT USB3.1(Type-C)

WEBCAM

Card Reader

Finger Print Reader

ELC

M.2 2230 WLAN KEY-E

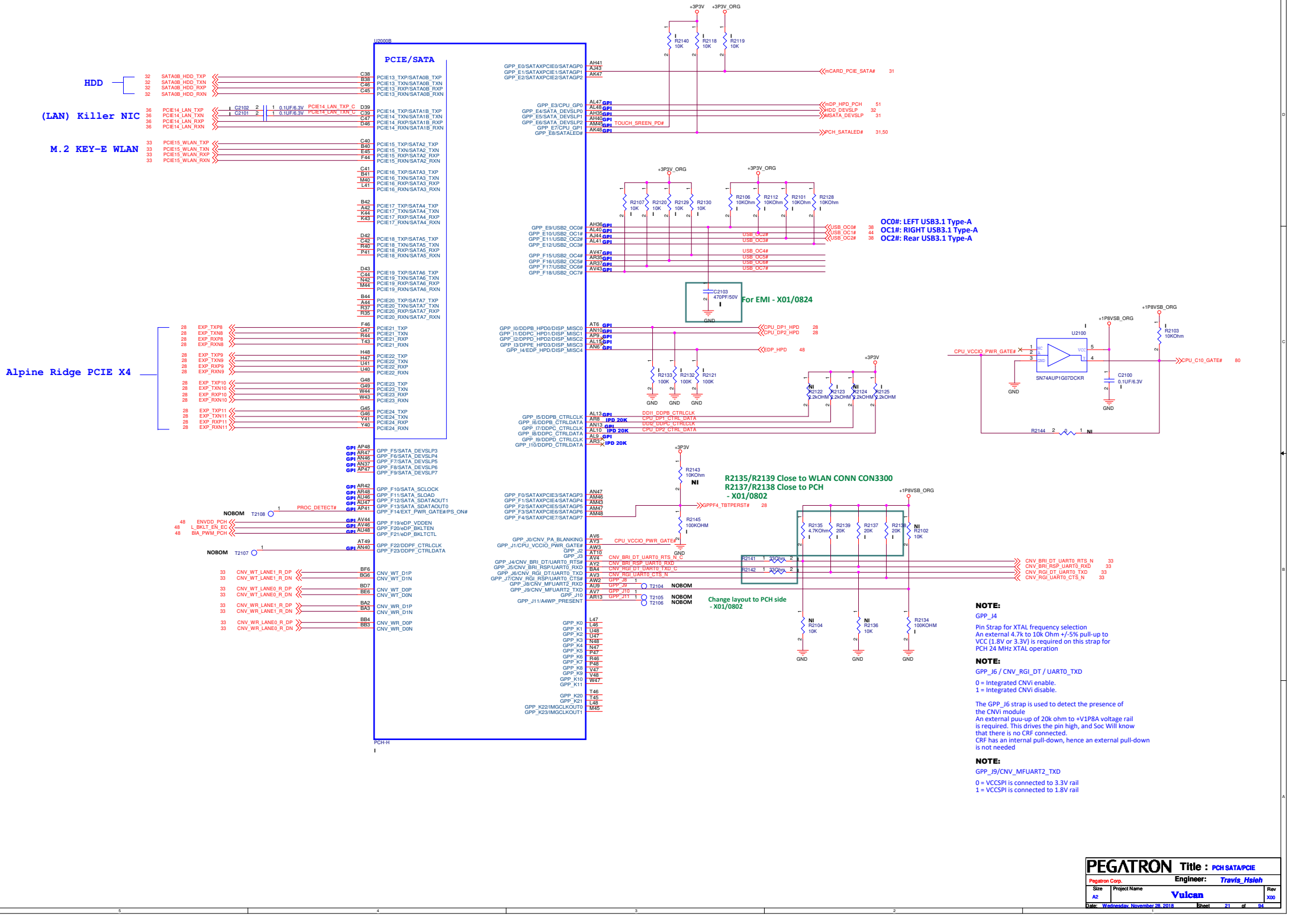
Change from port7 due to INTEL CNVi uggest - X01/0801

IO USB3.1(Type-A_1)

RIGHT USB3.1(Type-A) -Power share

USB3.1(Type-A Rear)

Title :	PCH DMI_PCIE_USB_SATA
Pegatron Corp.	Engineer: Travis_Hsieh
Size: A3	Project Name: Vulcan
Rev: X00	
Date: Wednesday, November 28, 2018	Sheet 20 of 94


HDD
(LAN) Killer NIC
M.2 KEY-E WLAN
Alpine Ridge PCIE X4
U2000B
PCIE/SATA
PCH-H
+3P3V
+3P3V_ORG
+1P8VSB_ORG
R2140 10K
R2118 10K
R2119 10K
mCARD_PCIE_SATA#
mDP_HPD_PCH
HDD_DEVSLP
mSATA_DEVSLP
TOUCH_SREEN_PD#
PCH_SATALED#
R2107 10K
R2120 10K
R2129 10K
R2130 10K
R2106 10KOhm
R2112 10KOhm
R2101 10KOhm
R2128 10KOhm
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4#
USB_OC5#
USB_OC6#
USB_OC7#
OC0#: LEFT USB3.1 Type-A
OC1#: RIGHT USB3.1 Type-A
OC2#: Rear USB3.1 Type-A
C2103 470PF/50V
For EMI - X01/0824
GND
CPU_DP1_HPD
CPU_DP2_HPD
EDP_HPD
R2133 100K
R2132 100K
R2121 100K
R2122 2.2KOHM
R2123 2.2KOHM
R2124 2.2KOHM
R2125 2.2KOHM
DDI1_DDPB_CTRLCLK
CPU_DP1_CTRL_DATA
DDI2_DDPC_CTRLCLK
CPU_DP2_CTRL_DATA
U2100
SN74AUP1G07DCKR
CPU_VCCIO_PWR_GATE#
CPU_C10_GATE#
C2100 0.1UF/6.3V
R2103 10KOhm
R2144
R2143 10KOhm
R2145 100KOHM
GPPF4_TBTPERST#
R2135/R2139 Close to WLAN CONN CON3300
R2137/R2138 Close to PCH
- X01/0802
R2135 4.7KOhm
R2139 20K
R2137 20K
R2138 20K
R2102 10K
R2141 330Ohm
R2142 330Ohm
CNV_BRI_DT_UART0_RTS_N
CNV_BRI_RSP_UART0_RXD
CNV_RGI_DT_UART0_TXD
CNV_RGI_UART0_CTS_N
Change layout to PCH side
- X01/0802
R2104 10K
R2136 10K
R2134 100KOHM
NOBOM
T2104
T2105
T2106
T2107
T2108
PROC_DETECT#
ENVDD_PCH
L_BKLT_EN_EC
BIA_PWM_PCH
SATA0B_HDD_TXP
SATA0B_HDD_TXN
SATA0B_HDD_RXP
SATA0B_HDD_RXN
PCIE14_LAN_TXP
PCIE14_LAN_TXN
PCIE14_LAN_RXP
PCIE14_LAN_RXN
C2102 0.1UF/6.3V
C2101 0.1UF/6.3V
PCIE15_WLAN_TXP
PCIE15_WLAN_TXN
PCIE15_WLAN_RXP
PCIE15_WLAN_RXN
EXP_TXP8
EXP_TXN8
EXP_RXP8
EXP_RXN8
EXP_TXP9
EXP_TXN9
EXP_RXP9
EXP_RXN9
EXP_TXP10
EXP_TXN10
EXP_RXP10
EXP_RXN10
EXP_TXP11
EXP_TXN11
EXP_RXP11
EXP_RXN11
CNV_WT_LANE1_R_DP
CNV_WT_LANE1_R_DN
CNV_WT_LANE0_R_DP
CNV_WT_LANE0_R_DN
CNV_WR_LANE1_R_DP
CNV_WR_LANE1_R_DN
CNV_WR_LANE0_R_DP
CNV_WR_LANE0_R_DN
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_D0P
CNV_WT_D0N
CNV_WR_D1P
CNV_WR_D1N
CNV_WR_D0P
CNV_WR_D0N
NOTE:
GPP_J4
Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation
NOTE:
GPP_J6 / CNV_RGI_DT / UART0_TXD
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
The GPP_J6 strap is used to detect the presence of the CNVi module
An external puu-up of 20k ohm to +V1P8A voltage rail is required. This drives the pin high, and Soc Will know that there is no CRF connected.
CRF has an internal pull-down, hence an external pull-down is not needed
NOTE:
GPP_J9/CNV_MFUART2_TXD
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
PEGATRON
Title : PCH SATA/PCIE
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 21 of 94

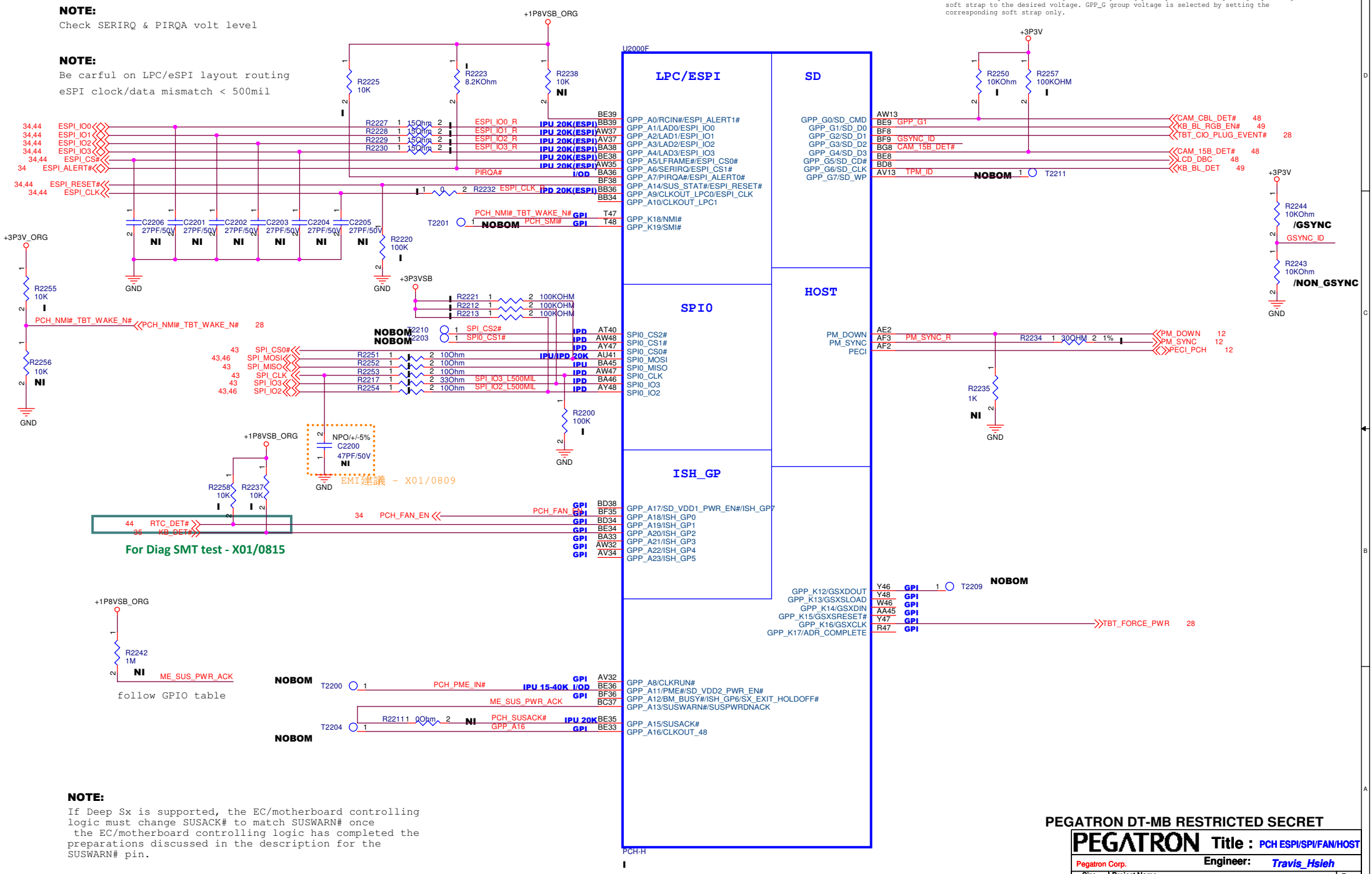
NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

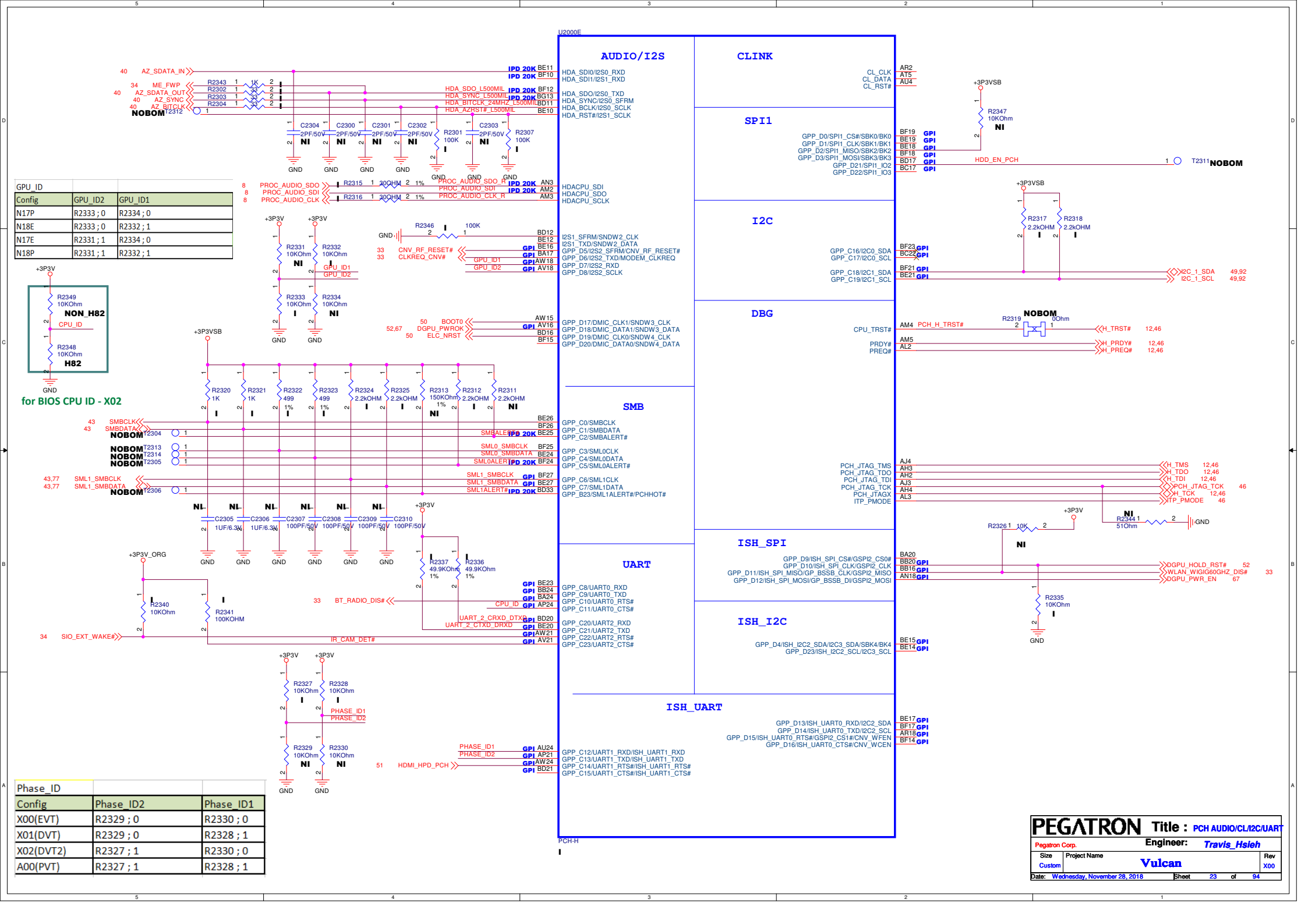
NOTE:
Check GPP_A0 power well

NOTE: GPP_G 1.8V for GPU
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



NOTE:
If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

PEGATRON Title : PCH ESPI/SPI/FAN/HOST
Pegatron Corp. Engineer: Travis_Hsieh
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 22 of 94



GPU_ID		
Config	GPU_ID2	GPU_ID1
N17P	R2333 ; 0	R2334 ; 0
N18E	R2333 ; 0	R2332 ; 1
N17E	R2331 ; 1	R2334 ; 0
N18P	R2331 ; 1	R2332 ; 1

Phase_ID		
Config	Phase_ID2	Phase_ID1
X00(EVT)	R2329 ; 0	R2330 ; 0
X01(DVT)	R2329 ; 0	R2328 ; 1
X02(DVT2)	R2327 ; 1	R2330 ; 0
A00(PVT)	R2327 ; 1	R2328 ; 1

PEGATRON Title : PCH AUDIO/CL/I2C/UART

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 23 of 94

NOTE:
GPP_B22/GSPI1_MOSI

This Signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI0_MOSI/GPP_B18

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

for EA - X01/0830

for EA - X01/0830

for EA - X02/1121

for EA - X01/0830

for sequence - X01/0830

NOTE:
GPP_B14 / SPKR

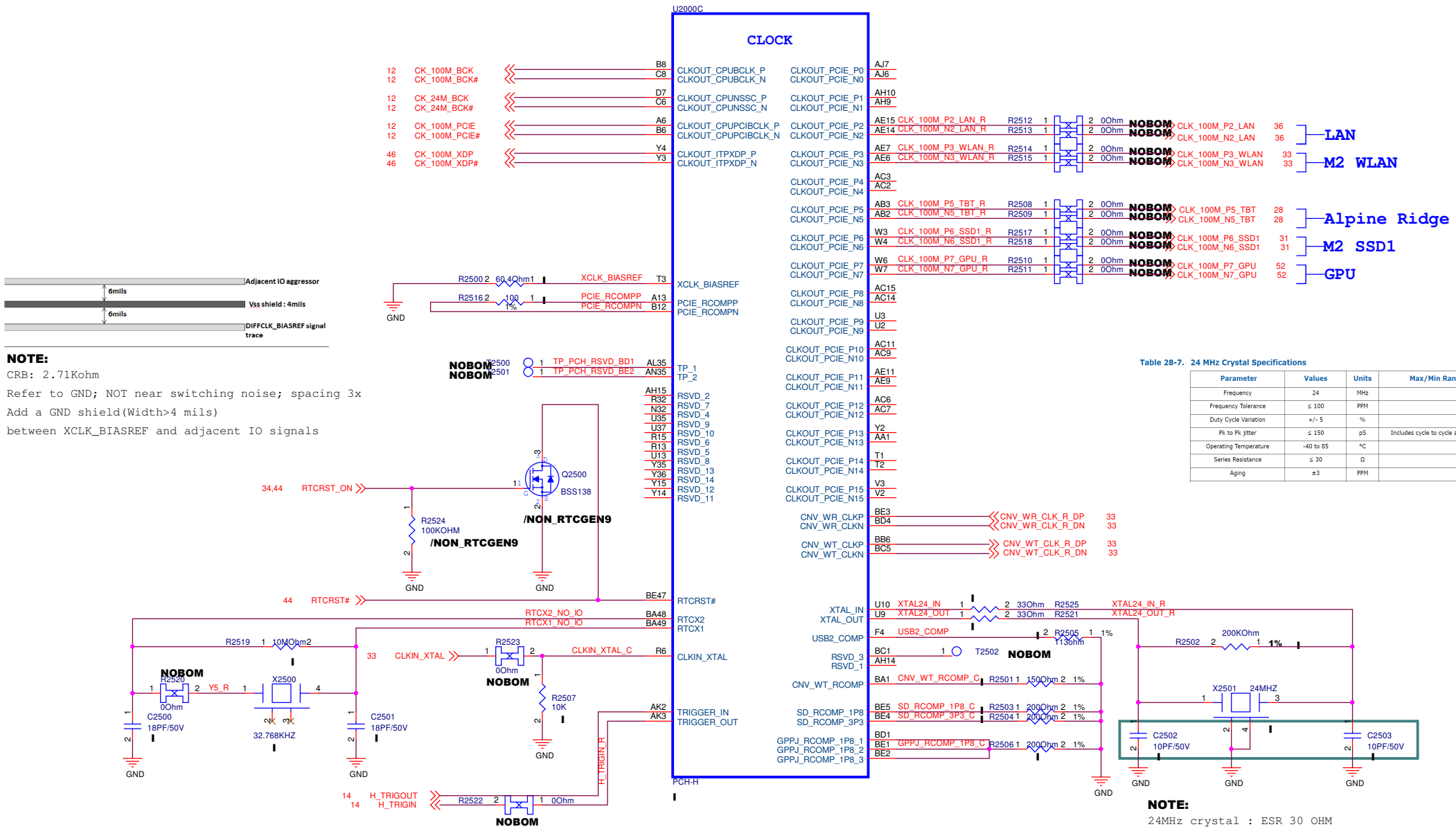
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

NOTE:
GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

PEGATRON	Title : PCH SML/I2C/MISC		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 24 of 94		



NOTE:

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

between XCLK_BIASREF and adjacent IO signals

Table 28-7. 24 MHz Crystal Specifications

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

NOTE:

24MHz crystal : ESR 30 OHM

follow vendor test report - X01/0829

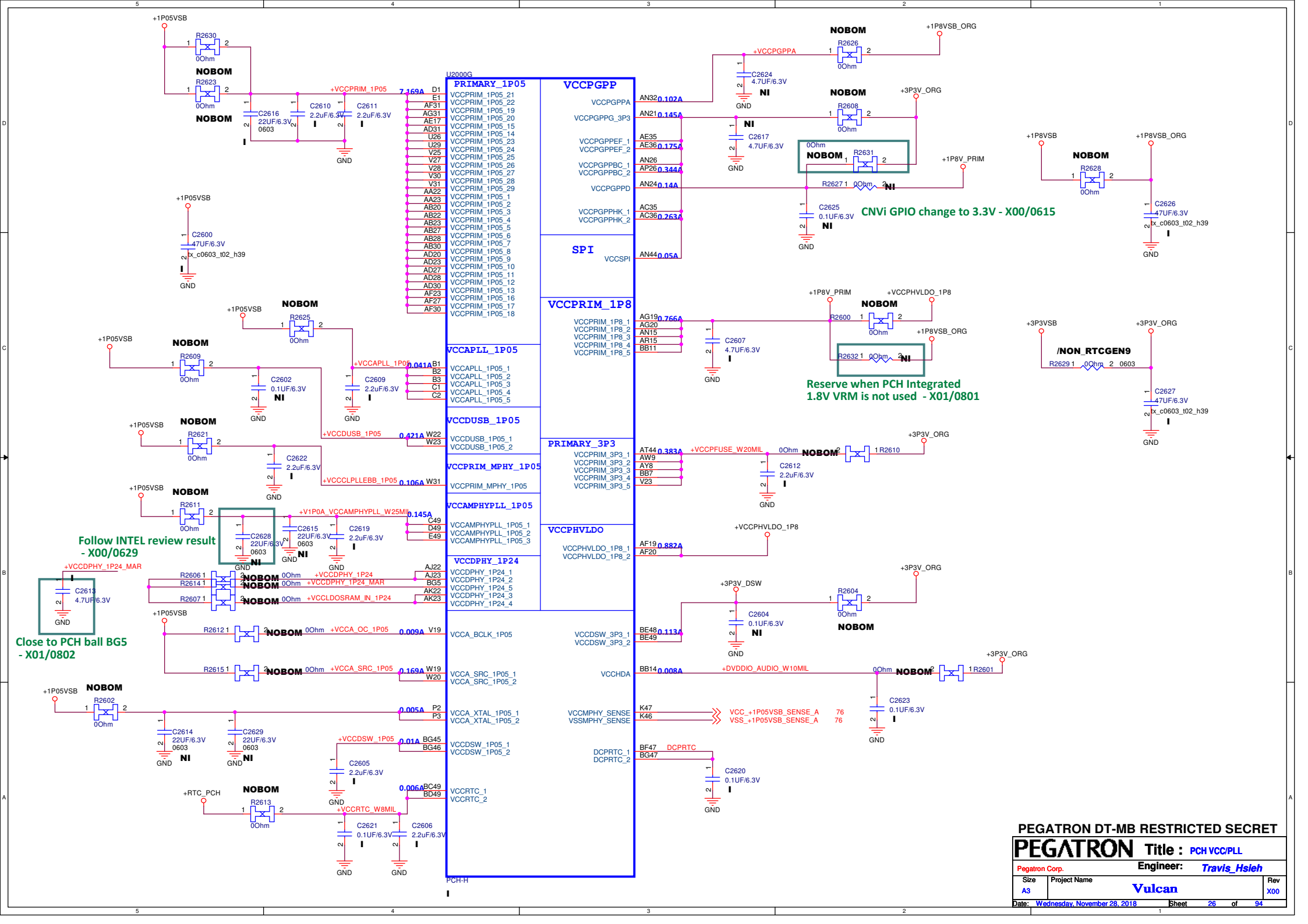
PEGATRON DT-MB RESTRICTED SECRET

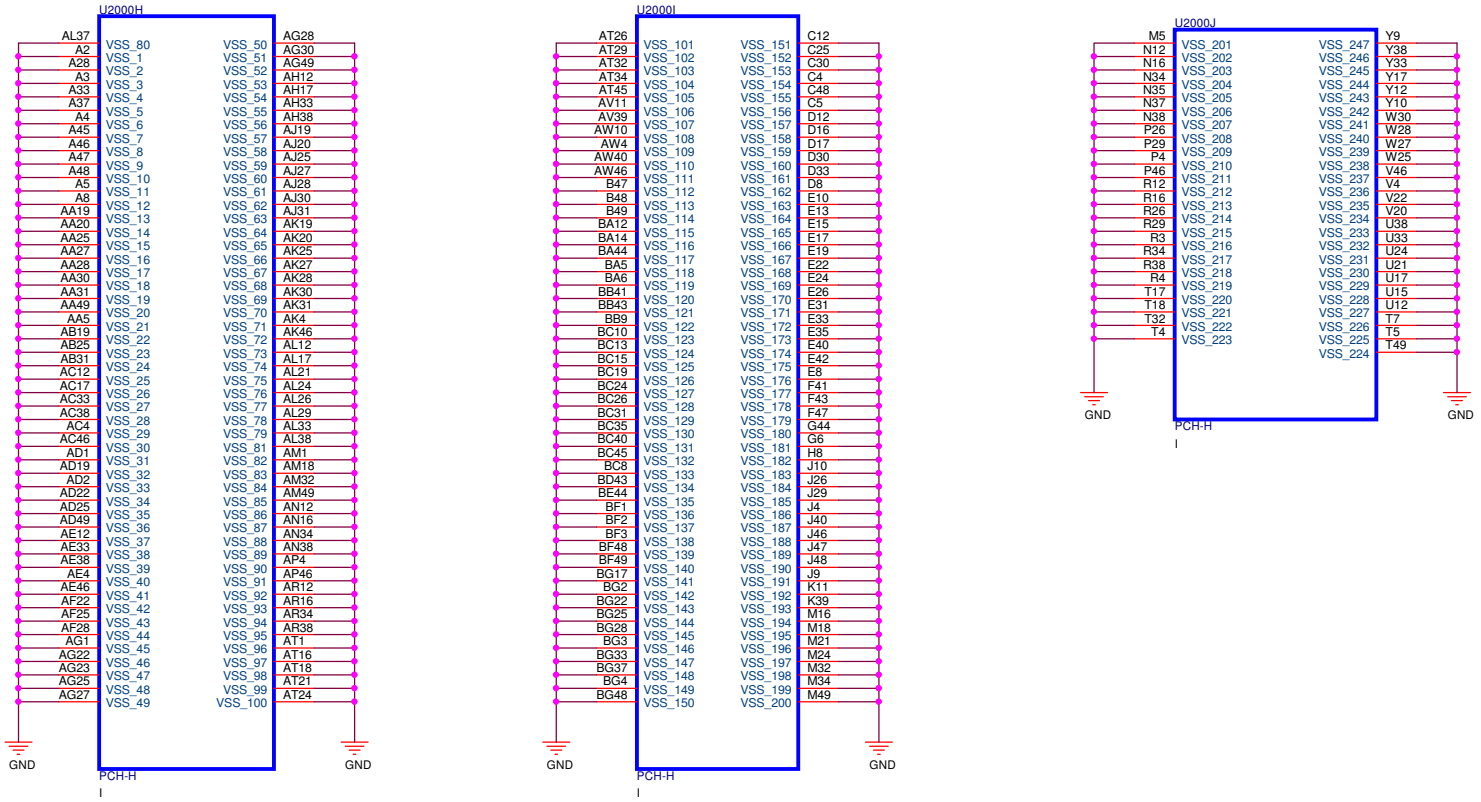
PEGATRON Title : PCH CLOCK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 25 of 94


U2000G
PRIMARY_1P05
VCCPRIM_1P05_21
VCCPRIM_1P05_22
VCCPRIM_1P05_19
VCCPRIM_1P05_20
VCCPRIM_1P05_15
VCCPRIM_1P05_14
VCCPRIM_1P05_23
VCCPRIM_1P05_24
VCCPRIM_1P05_25
VCCPRIM_1P05_26
VCCPRIM_1P05_27
VCCPRIM_1P05_28
VCCPRIM_1P05_29
VCCPRIM_1P05_1
VCCPRIM_1P05_2
VCCPRIM_1P05_3
VCCPRIM_1P05_4
VCCPRIM_1P05_5
VCCPRIM_1P05_6
VCCPRIM_1P05_7
VCCPRIM_1P05_8
VCCPRIM_1P05_9
VCCPRIM_1P05_10
VCCPRIM_1P05_11
VCCPRIM_1P05_12
VCCPRIM_1P05_13
VCCPRIM_1P05_16
VCCPRIM_1P05_17
VCCPRIM_1P05_18
VCCAPLL_1P05
VCCAPLL_1P05_1
VCCAPLL_1P05_2
VCCAPLL_1P05_3
VCCAPLL_1P05_4
VCCAPLL_1P05_5
VCCDUSB_1P05
VCCDUSB_1P05_1
VCCDUSB_1P05_2
VCCPRIM_MPHY_1P05
VCCPRIM_MPHY_1P05
VCCAMPHYPLL_1P05
VCCAMPHYPLL_1P05_1
VCCAMPHYPLL_1P05_2
VCCAMPHYPLL_1P05_3
VCCDPHY_1P24
VCCDPHY_1P24_1
VCCDPHY_1P24_2
VCCDPHY_1P24_5
VCCDPHY_1P24_3
VCCDPHY_1P24_4
VCCA_BCLK_1P05
VCCA_SRC_1P05_1
VCCA_SRC_1P05_2
VCCA_XTAL_1P05_1
VCCA_XTAL_1P05_2
VCCDSW_1P05_1
VCCDSW_1P05_2
VCCRTC_1
VCCRTC_2
PCH-H
VCCPGPP
VCCPGPPA
VCCPGPPG_3P3
VCCPGPPEF_1
VCCPGPPEF_2
VCCPGPPBC_1
VCCPGPPBC_2
VCCPGPPD
VCCPGPPHK_1
VCCPGPPHK_2
SPI
VCCSPI
VCCPRIM_1P8
VCCPRIM_1P8_1
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
PRIMARY_3P3
VCCPRIM_3P3_1
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
VCCPRIM_3P3_5
VCCPHVLDO
VCCPHVLDO_1P8_1
VCCPHVLDO_1P8_2
VCCDSW_3P3_1
VCCDSW_3P3_2
VCCHDA
VCCMPHY_SENSE
VSSMPHY_SENSE
DCPRTC_1
DCPRTC_2
+1P05VSB
+VCCPRIM_1P05
+VCCAPLL_1P05
+VCCDUSB_1P05
+VCCCLPLLEBB_1P05
+V1P0A_VCCAMPHYPLL_W25MIL
+VCCDPHY_1P24
+VCCDPHY_1P24_MAR
+VCCLDOSRAM_IN_1P24
+VCCA_OC_1P05
+VCCA_SRC_1P05
+VCCDSW_1P05
+RTC_PCH
+VCCRTC_W8MIL
+VCCPGPPA
+3P3V_ORG
+1P8VSB_ORG
+1P8V_PRIM
+VCCPHVLDO_1P8
+3P3V_DSW
+3P3VSB
+VCCPFUSE_W20MIL
+DVDDIO_AUDIO_W10MIL
VCC_+1P05VSB_SENSE_A
VSS_+1P05VSB_SENSE_A
DCPRTC
NOBOM
NI
GND
CNVi GPIO change to 3.3V - X00/0615
Reserve when PCH Integrated
1.8V VRM is not used - X01/0801
Follow INTEL review result
- X00/0629
Close to PCH ball BG5
- X01/0802
/NON_RTCGEN9
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCH VCC/PLL
Pegatron Corp.
Engineer: Travis_Hsieh
Size A3
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 26 of 94



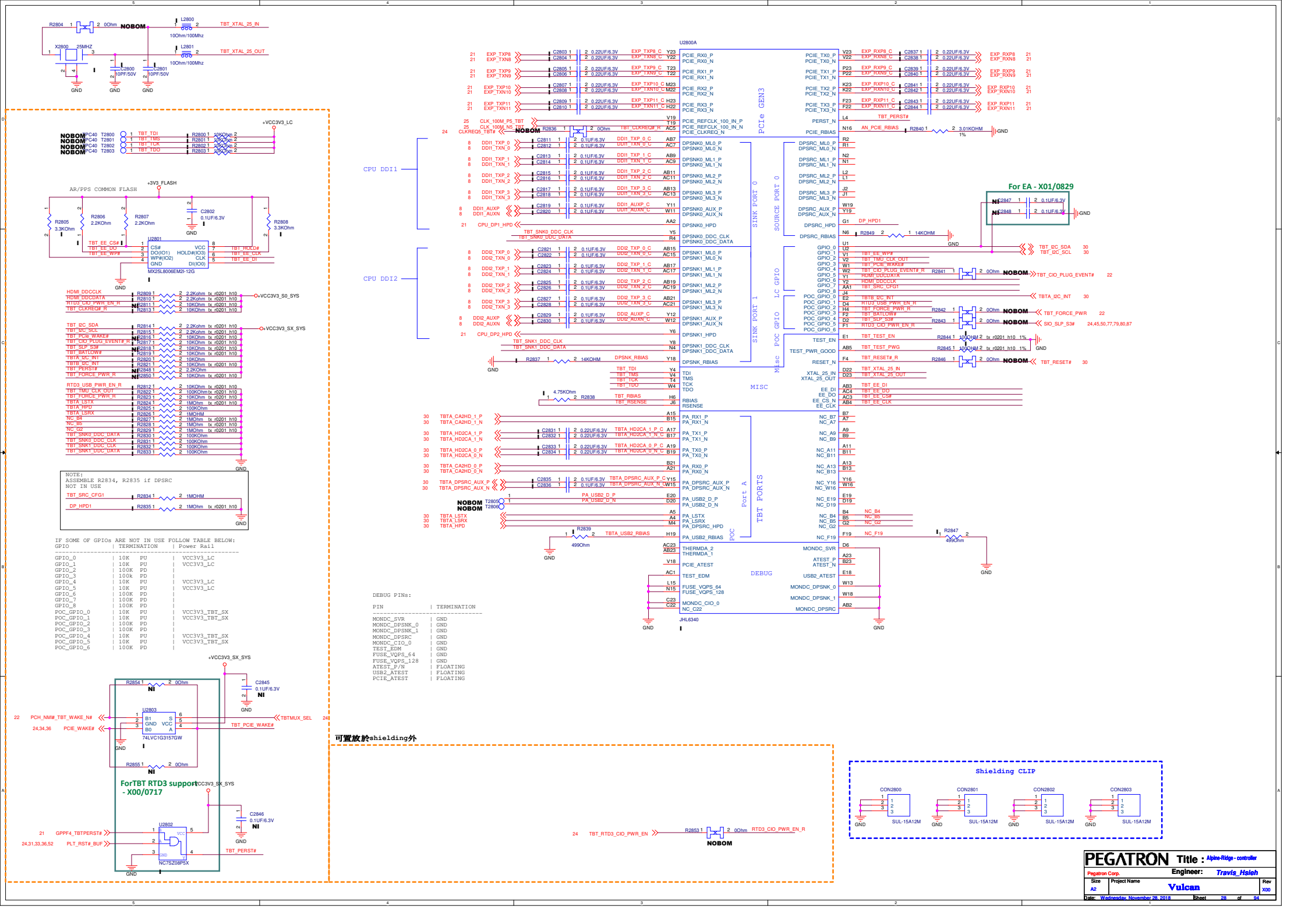
PEGATRON DT-MB RESTRICTED SECRET

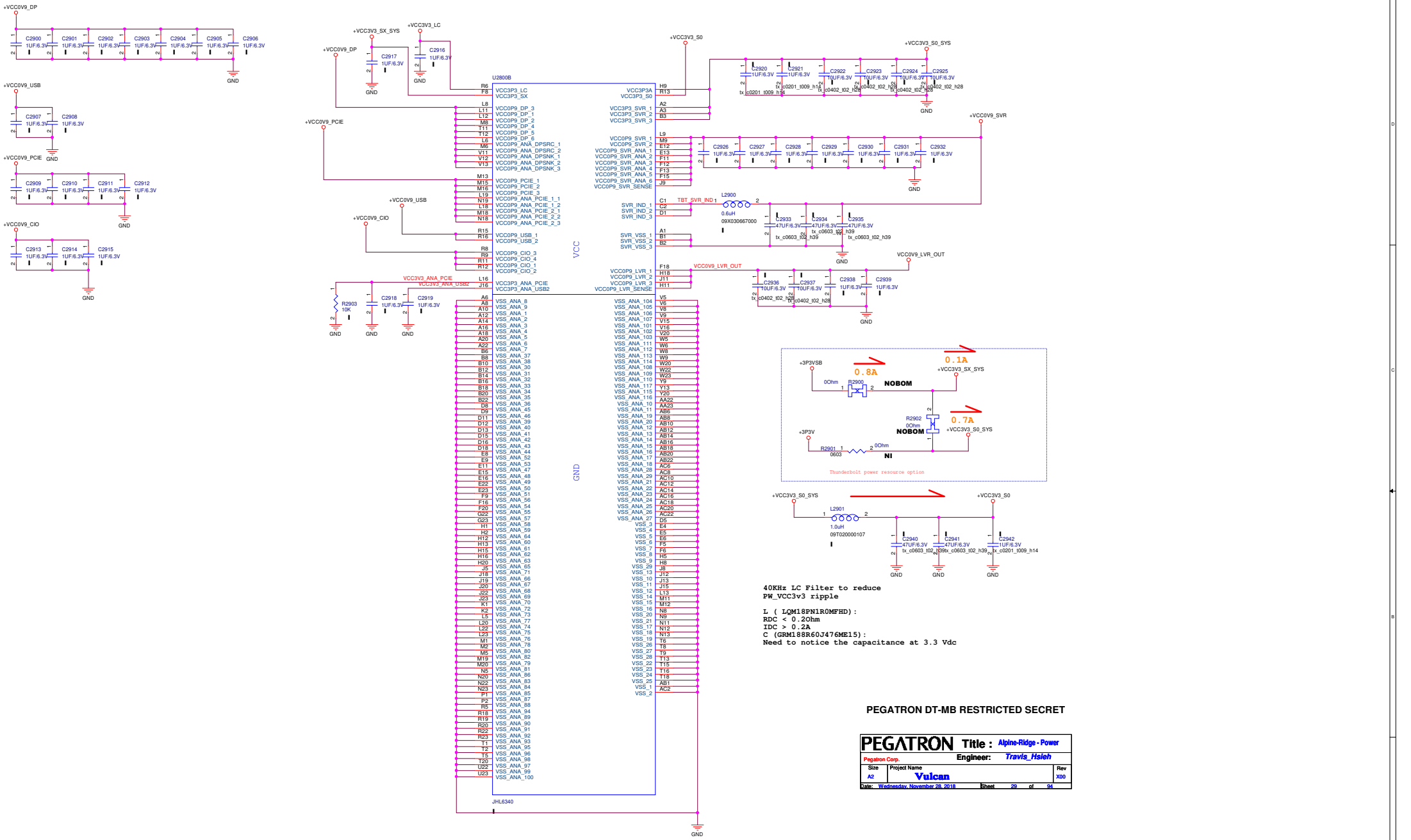
PEGATRON Title : PCH VSS

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

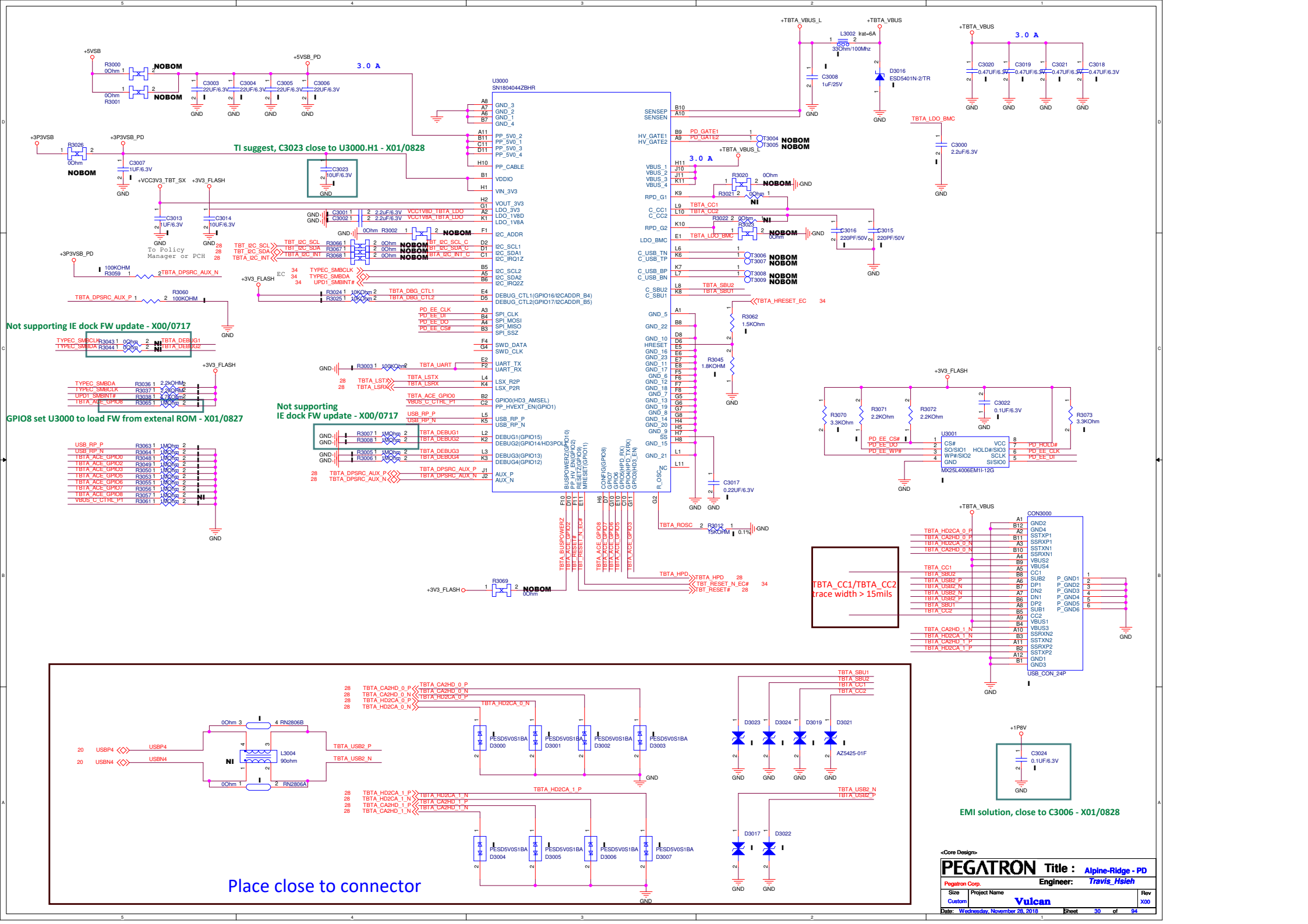
Date: Wednesday, November 28, 2018 Sheet 27 of 94


U2800A
CPU DDI1
CPU DDI2
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
LC GPIO
POC GPIO
SINK PORT 1
Misc
MISC
TBT PORTS
Port A
POC
DEBUG
JHL6340
For EA - X01/0829
Shielding CLIP
ForTBT RTD3 support - X00/0717
可置放於shielding外
NOTE:
ASSEMBLE R2834, R2835 if DPSRC
NOT IN USE
IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:
GPIO | TERMINATION | Power Rail
GPIO_0 | 10K PU | VCC3V3_LC
GPIO_1 | 10K PU | VCC3V3_LC
GPIO_2 | 100K PD |
GPIO_3 | 100k PD |
GPIO_4 | 10K PU | VCC3V3_LC
GPIO_5 | 10K PU | VCC3V3_LC
GPIO_6 | 100K PD |
GPIO_7 | 100K PD |
GPIO_8 | 100K PD |
POC_GPIO_0 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_1 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_2 | 100K PD |
POC_GPIO_3 | 100K PD |
POC_GPIO_4 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_5 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_6 | 100K PD |
DEBUG PINs:
PIN | TERMINATION
MONDC_SVR | GND
MONDC_DPSNK_0 | GND
MONDC_DPSNK_1 | GND
MONDC_DPSRC | GND
MONDC_CIO_0 | GND
TEST_EDM | GND
FUSE_VQPS_64 | GND
FUSE_VQPS_128 | GND
ATEST_P/N | FLOATING
USB2_ATEST | FLOATING
PCIE_ATEST | FLOATING
AR/PPS COMMON FLASH
MX25L8006EM2I-12G
PEGATRON
Title : Alpine-Ridge - controller
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 28 of 94

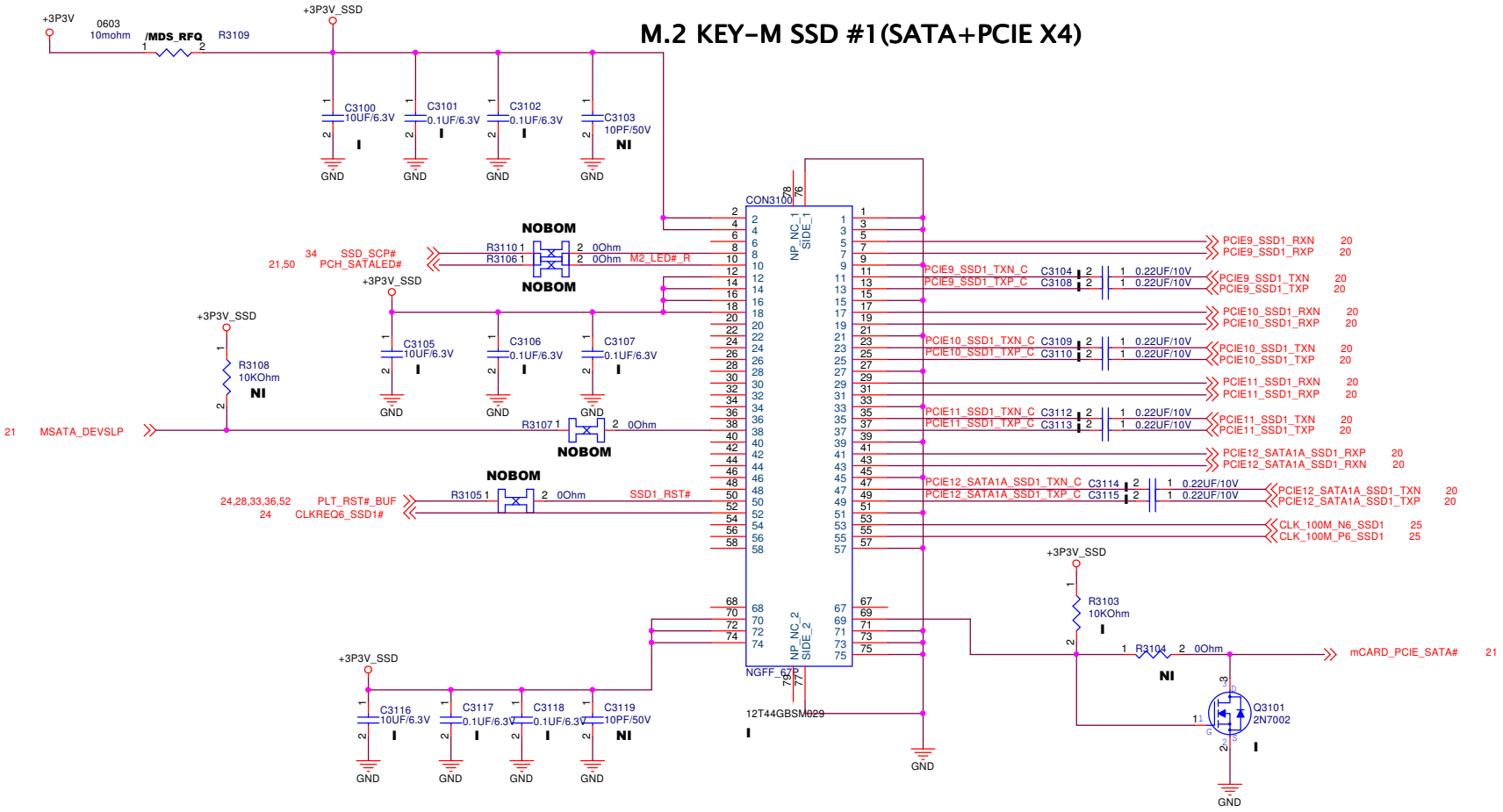


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Alpine-Ridge - Power		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 29 of 94		

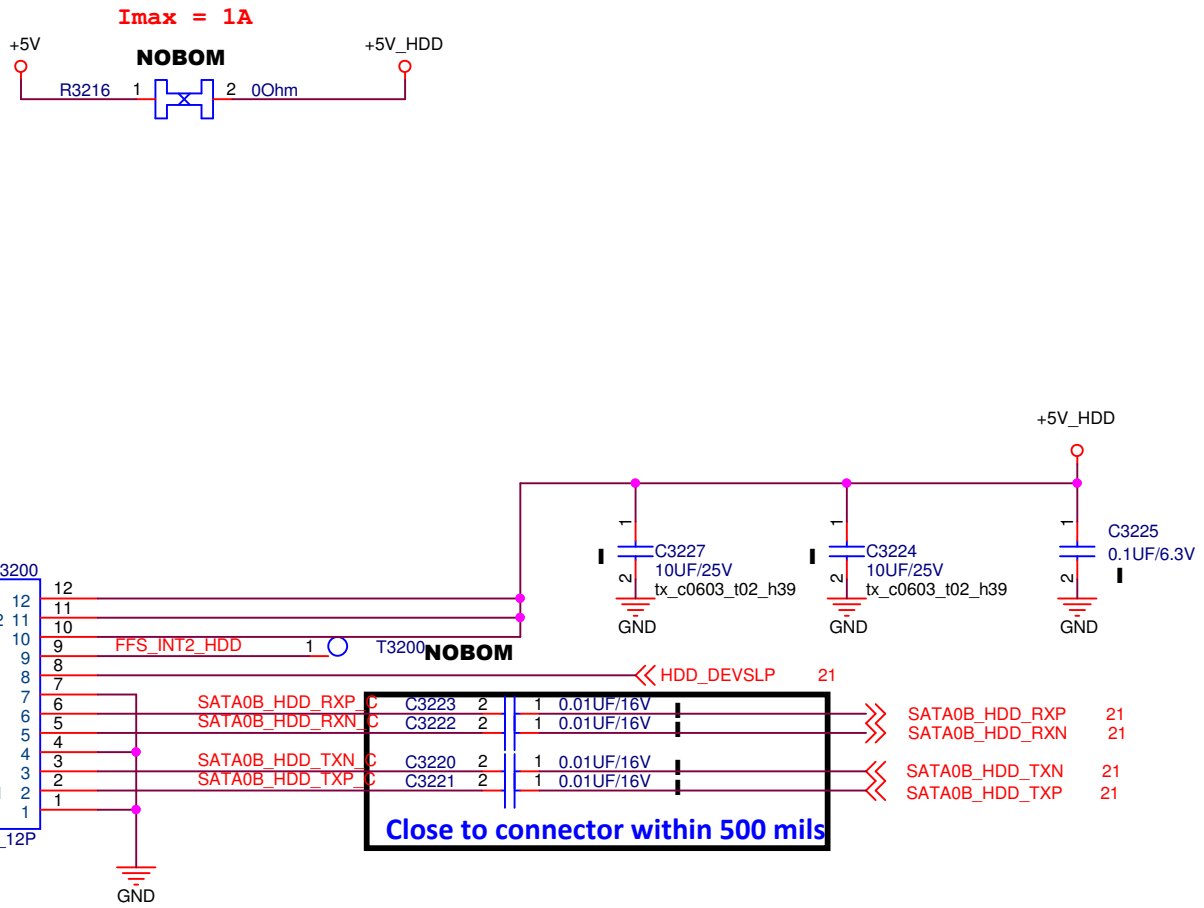

TI suggest, C3023 close to U3000.H1 - X01/0828
Not supporting IE dock FW update - X00/0717
GPIO8 set U3000 to load FW from extenal ROM - X01/0827
Not supporting IE dock FW update - X00/0717
TBTA_CC1/TBTA_CC2 trace width > 15mils
EMI solution, close to C3006 - X01/0828
Place close to connector
U3000
SN1804044ZBHR
CON3000
USB_CON_24P
U3001
MX25L4006EM1I-12G
Title : Alpine-Ridge - PD
Engineer: Travis_Hsieh
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 30 of 94

M.2 KEY-M SSD #1(SATA+PCIE X4)



PEGATRON	Title : M.2 2280 SSD #1	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 31 of 94	

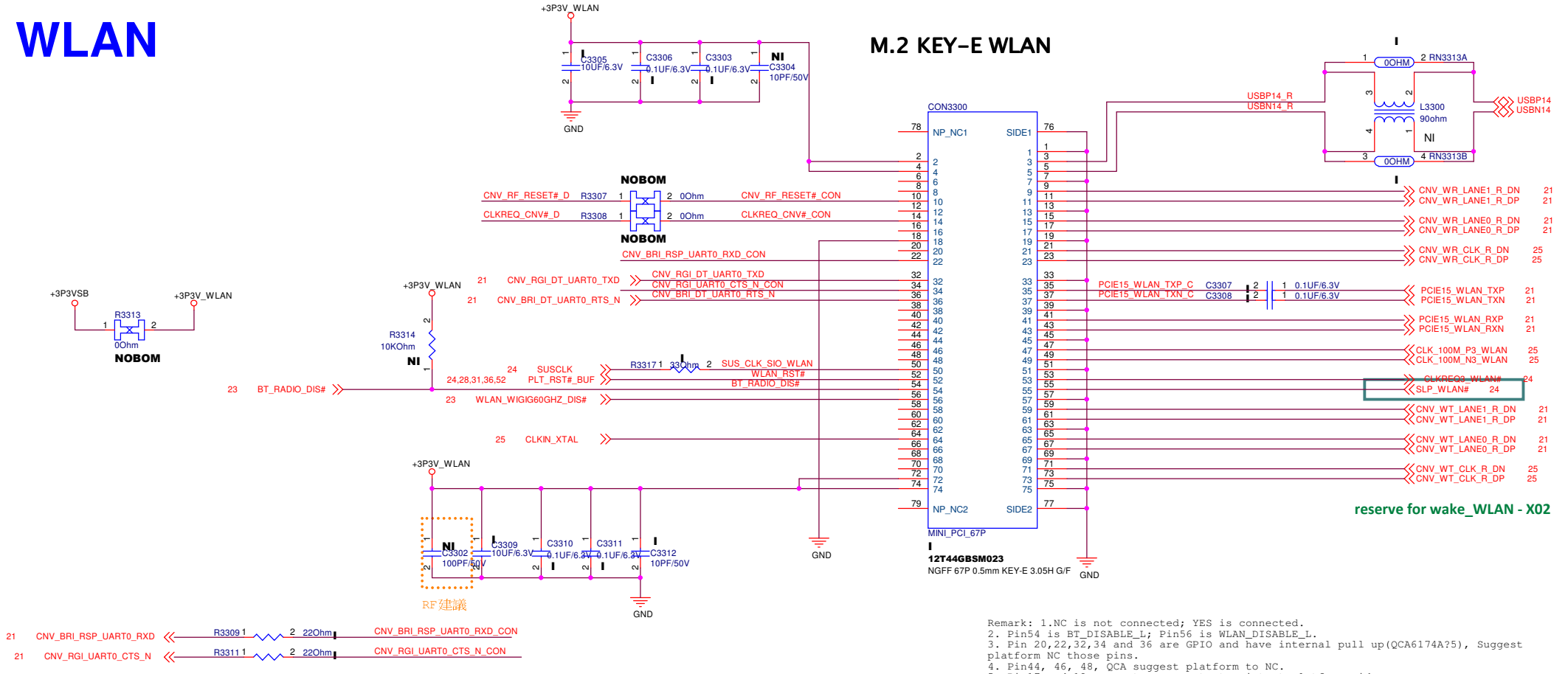
HDD



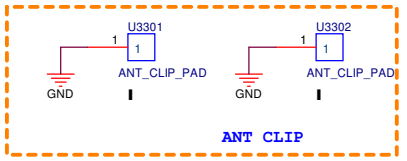
PEGATRON	Title : SATA HDD	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 32 of 94	

WLAN

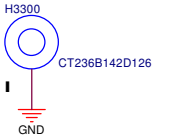
M.2 KEY-E WLAN

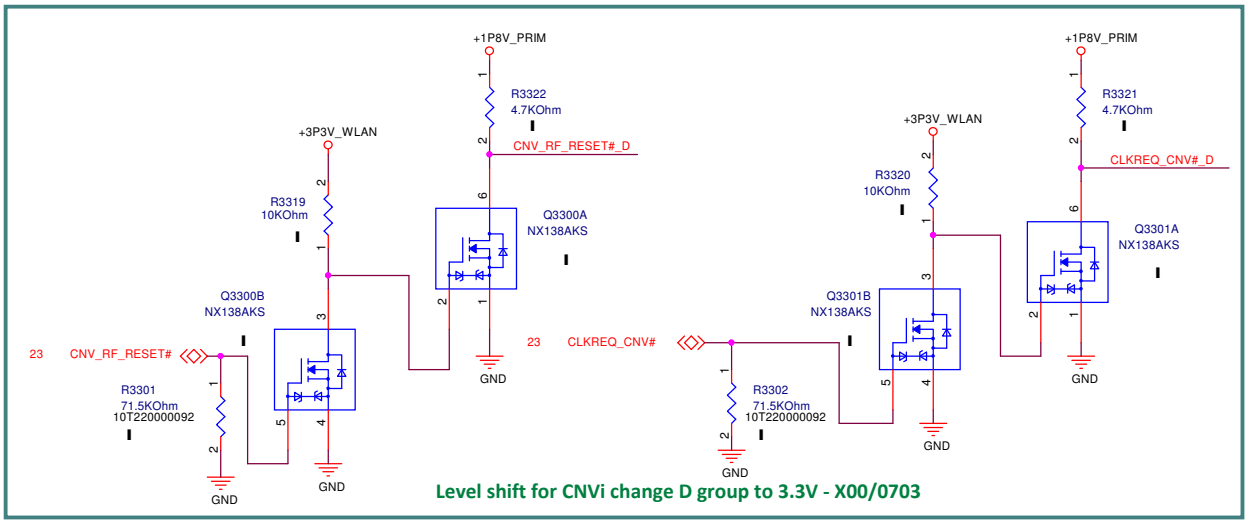


Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.



RTC CLIP
13X020219000
U3303





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : M.2 KEY-A 2230 WLAN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 33 of 94

Pull Up

EC Power

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note:
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel.
If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Imax:12.5mA

PD reset follow reference design - X00

R3493 for EMC - X01/0730

Battery power monitor to EC ADC pin

Adapter power monitor to EC ADC pin

debug test point placement together bottom side

Turn off ELC in MDS - X02 10/24

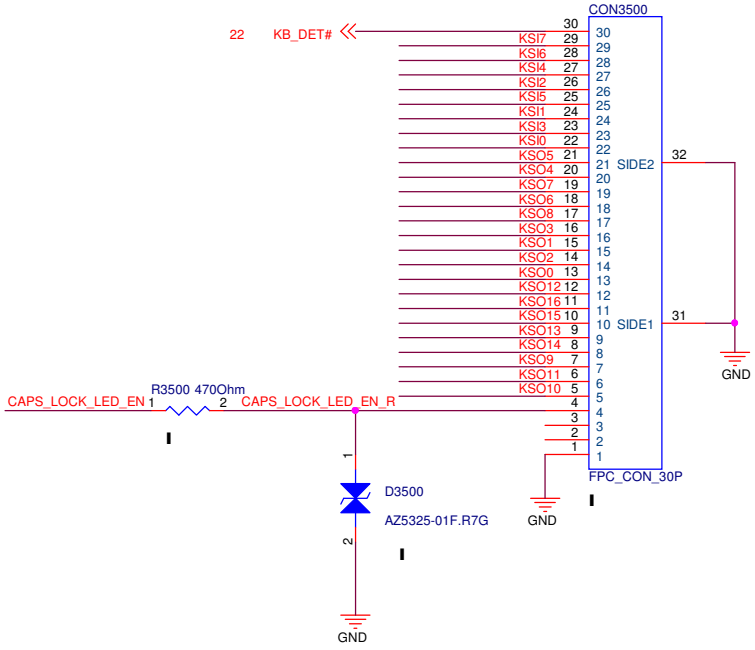
4 Resistor colay (R3497,R3410,R3498,R3499)

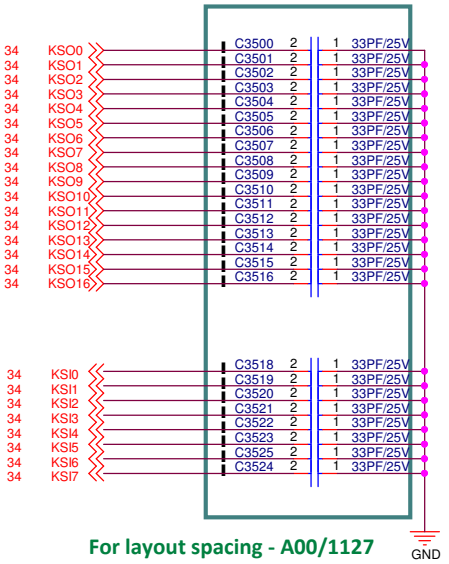
Board_ID		
config	Pull-High res ; R3412	Voltage
X00(EVT)	10K	3
X01(DVT)	17.8K	2.801
X02(DVT2)	27K	2.598
X03(reserve1)	37.4K	2.402
A00(PVT)	49.9K	2.201
A01	64.9K	2.001
A02	82.5K	1.808
A03	107K	1.594
Reserve2	154K	1.299
Reserve3	200K	1.1

MODEL_ID					
config	CPU	GPU	Pull-High res ; R3410	Voltage	
0	H62	N17P_G1/N18P_G0	10K	3	P-50W
1	H82	N17P_G1/N18P_G0	17.8K	2.801	
2	H62	N18P_G1	27K	2.598	P-60W
3	H82	N18P_G1	37.4K	2.402	
4	Reserve		49.9K	2.201	
5	Reserve		64.9K	2.001	
6	H62	N17E_G1/N18E_G1/N18E_G0	82.5K	1.808	E-60W/65W
7	H82	N17E_G1/N18E_G1/N18E_G0	107K	1.594	
8	H62	N18E_G2_G3	154K	1.299	E-80W
9	H82	N18E_G2_G3	200K	1.1	

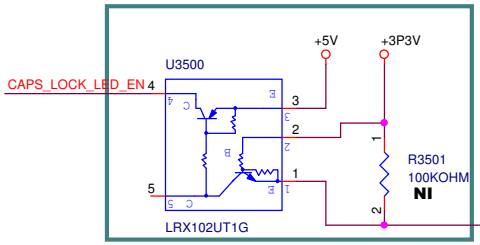
PEGATRON Title : EC
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 34 of 94

KeyBoard connector





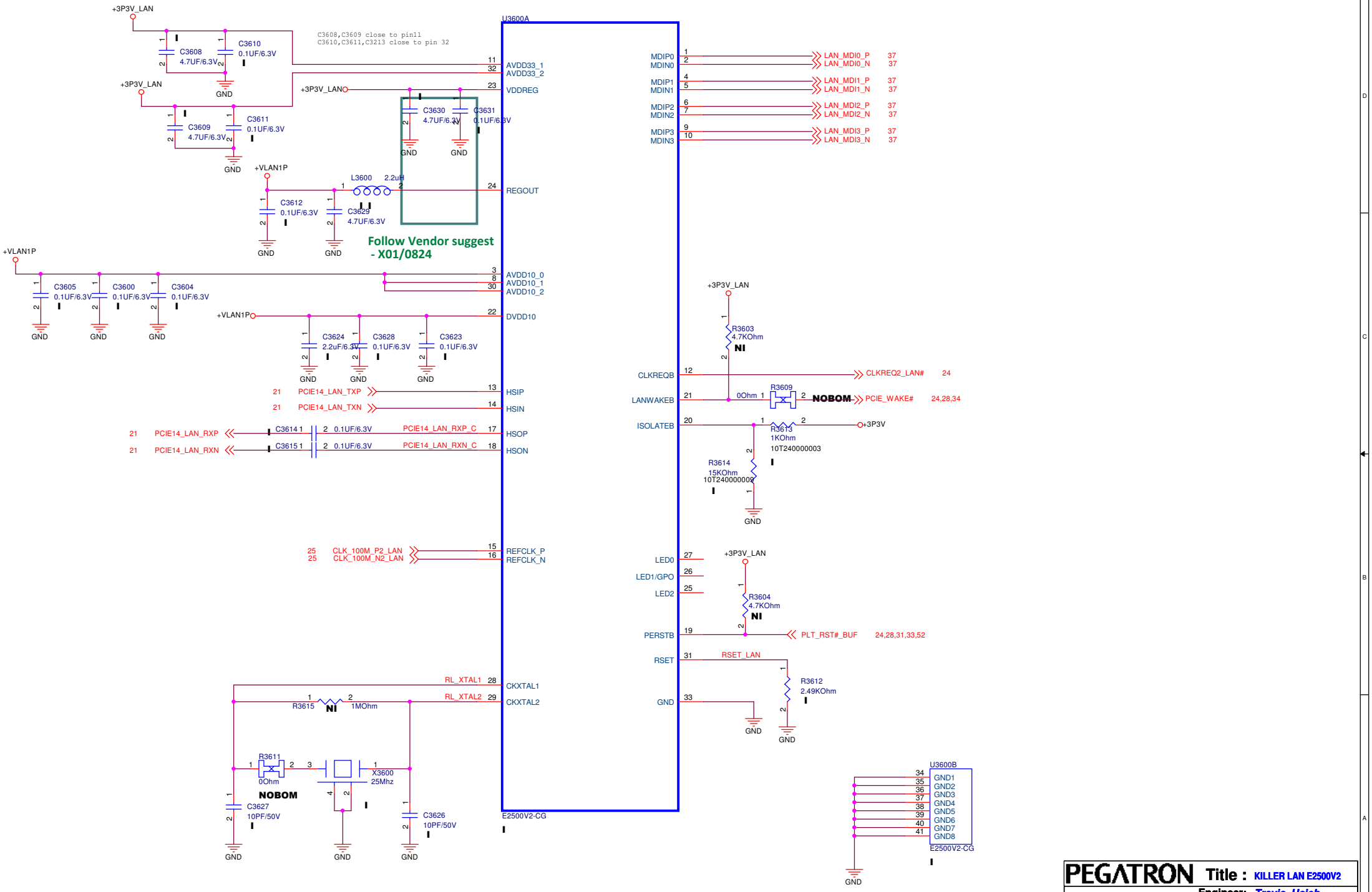
For layout spacing - A00/1127



TX pool change to MX per CE request - X01/0801

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : KB & NKRO	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: B	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 35 of 94	

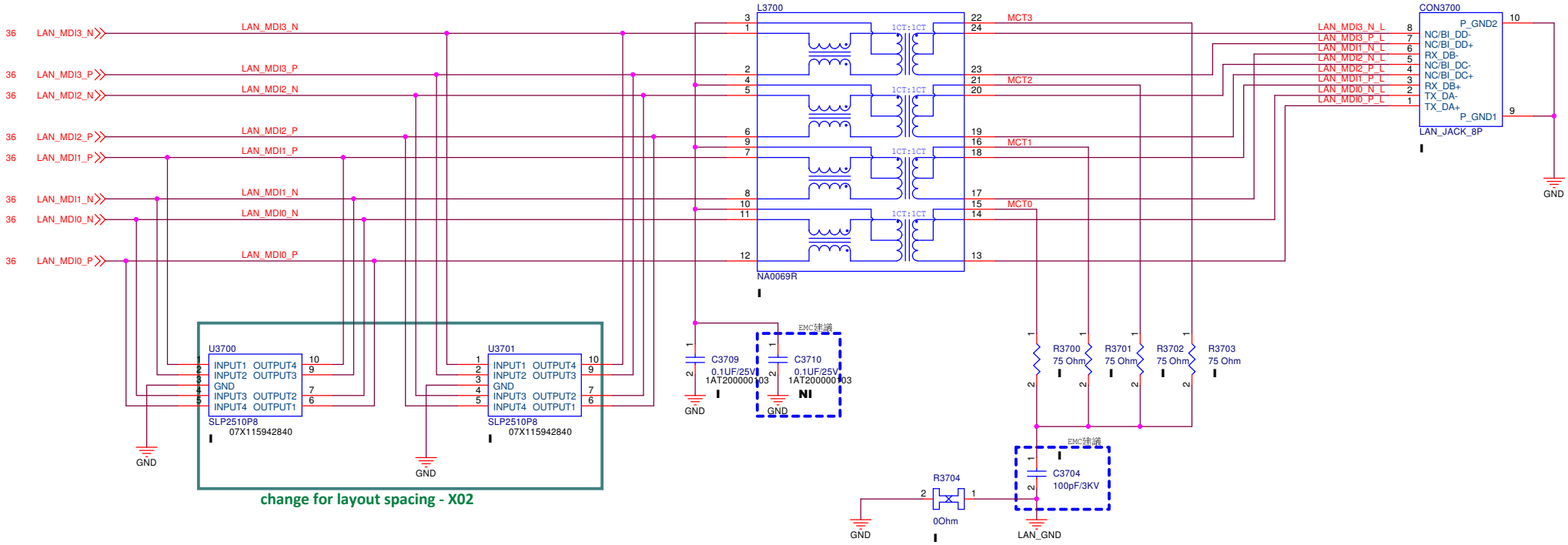


PEGATRON Title : KILLER LAN E2500V2

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 36 of 95



change for layout spacing - X02

<Core Design>

PEGATRON	Title : LAN JACK	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 37 of 94	

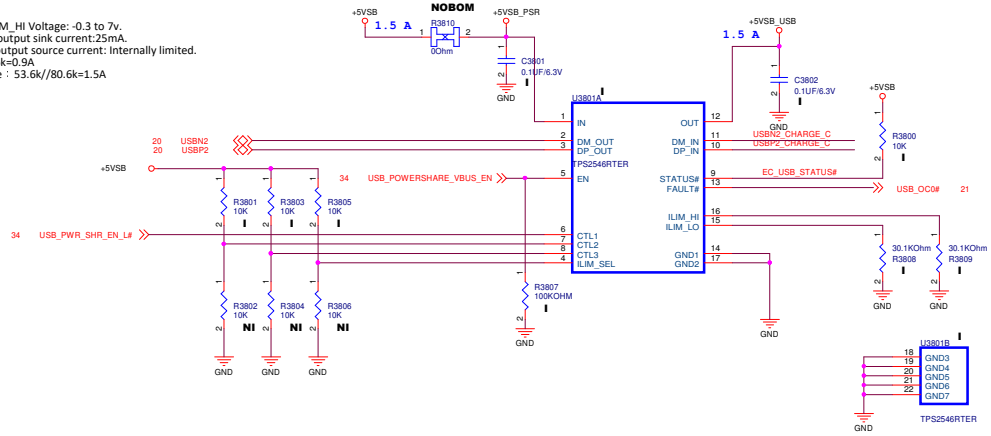
Power Share

Table 2. Truth Table

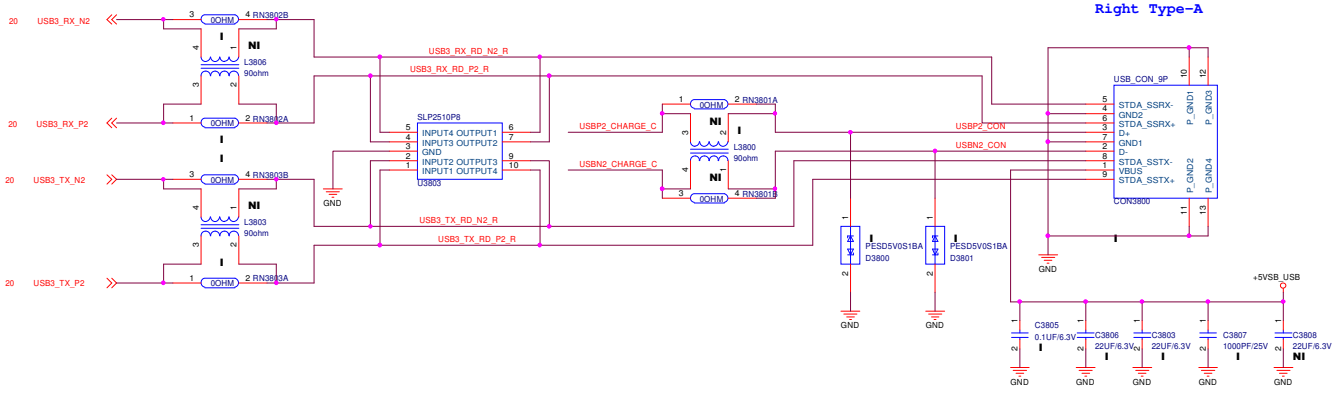
CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP _Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data Lines Connected and Load Detect Active

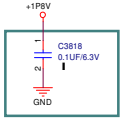
(1) TPS2546 : Current limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the "Load Detection – Power Wake" limits.
(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.

STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.
SDP Mode(S0/S3/S4/S5) : 53.6k=0.9A
CDP(S0)& DCP(S3/S4/S5) Mode : 53.6k//80.6k=1.5A



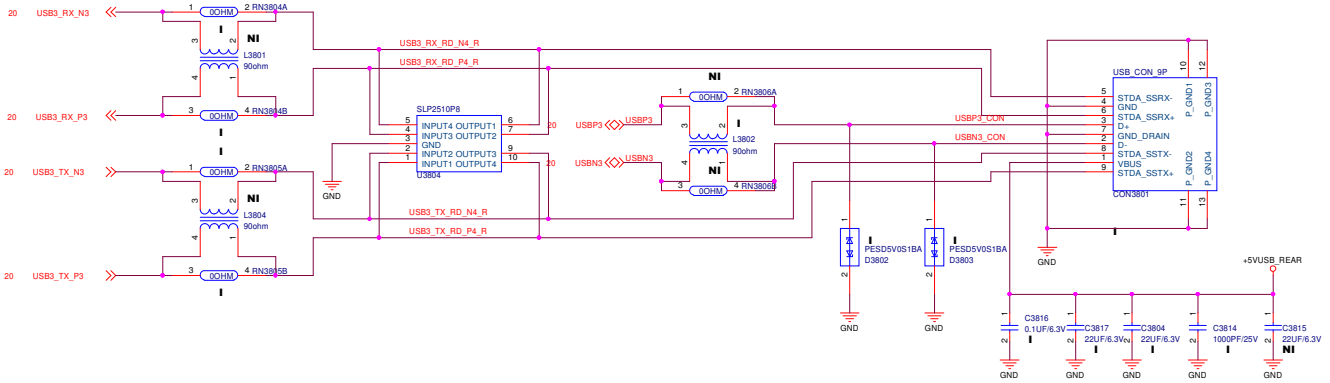
Right Type-A

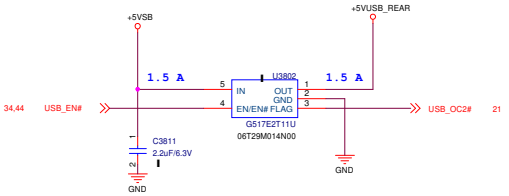




EMI solution, close to CON3800 - X01/0828

Rear Type-A





<Core Design>

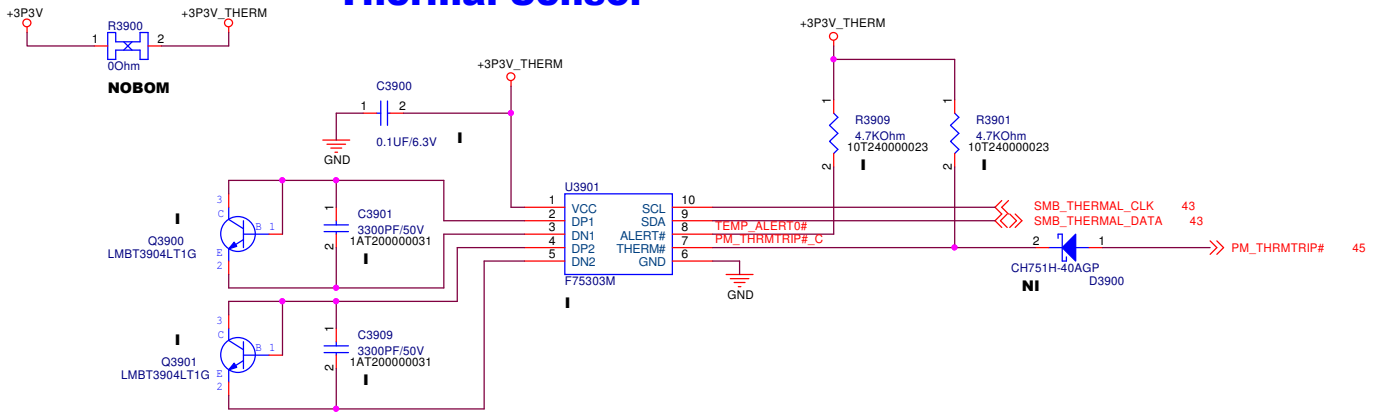
PEGATRON Title : USB CONN & POWER

Pegatron Corp. Engineer: Travis_Hsieh

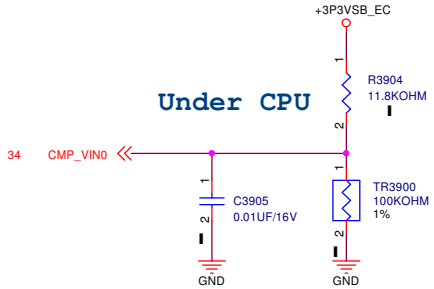
Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 38 of 94

Thermal Sensor



U3901: Under GPU thermal pipe
Q3900: Under CPU thermal pipe
Q3901: Close to SSD connector



<Core Design>

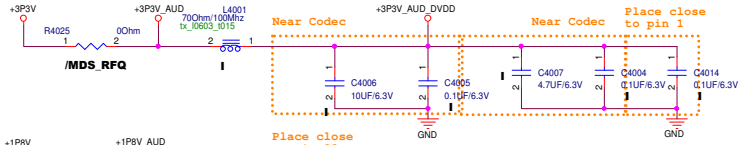
PEGATRON Title : SENSOR

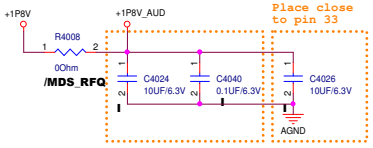
Pegatron Corp. Engineer: Travis_Hsieh

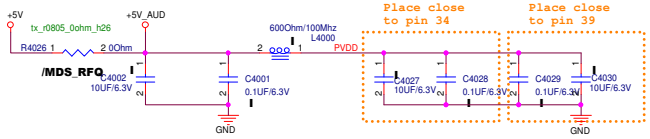
Size	Project Name	Rev
A3	Vulcan	X00

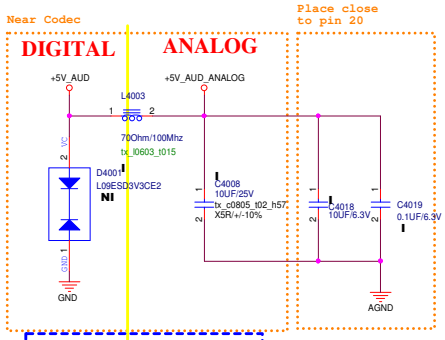
Date: Wednesday, November 28, 2018 Sheet 39 of 94

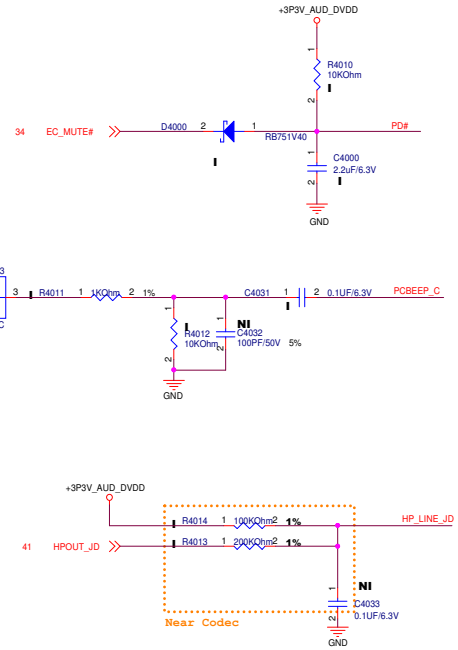
AUDIO CODEC- ALC3204



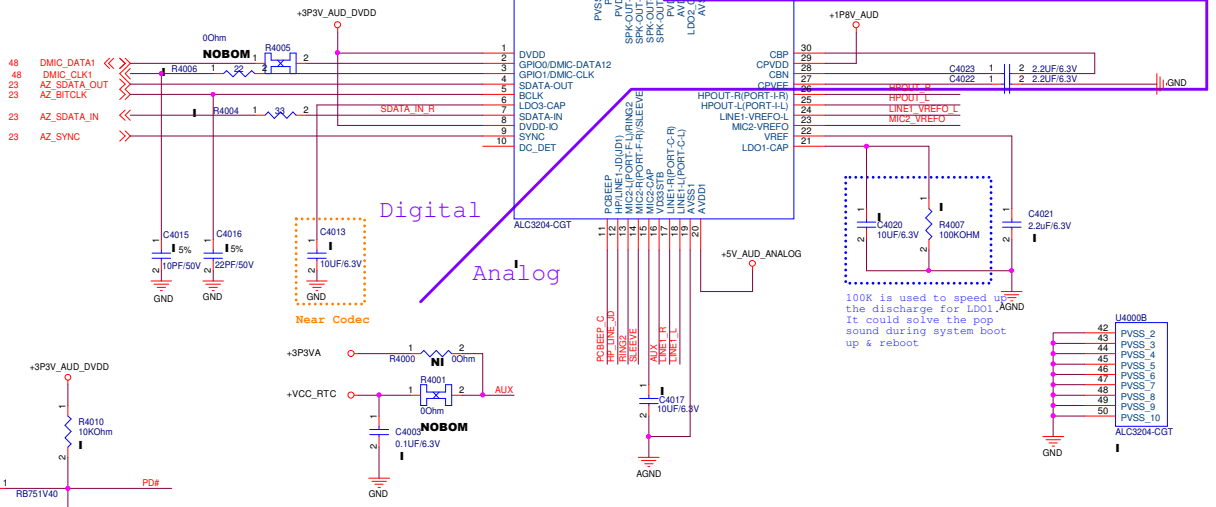


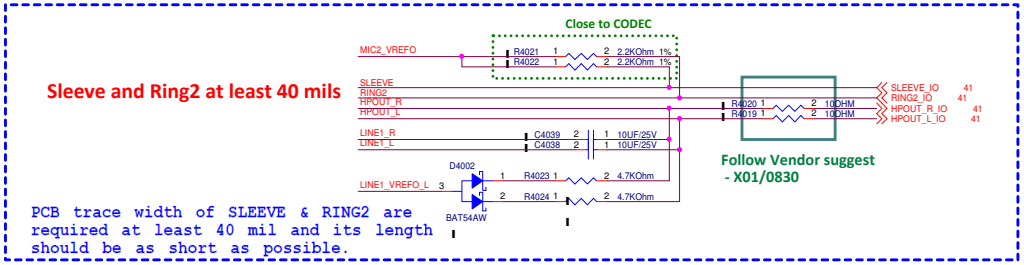


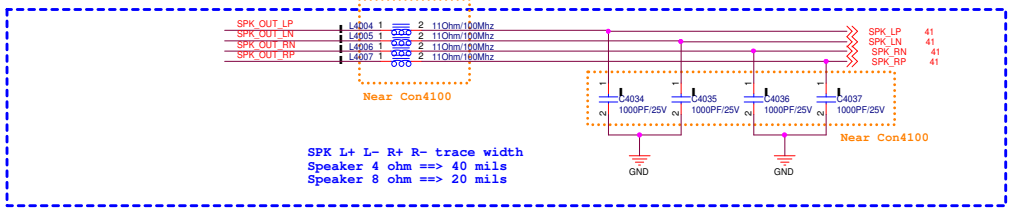




Digital Analog







R4003 Place at Codec bottom side.
R4002 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

<Core Design>

PEGATRON Title : AUDIO ALC3204

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 40 of 94

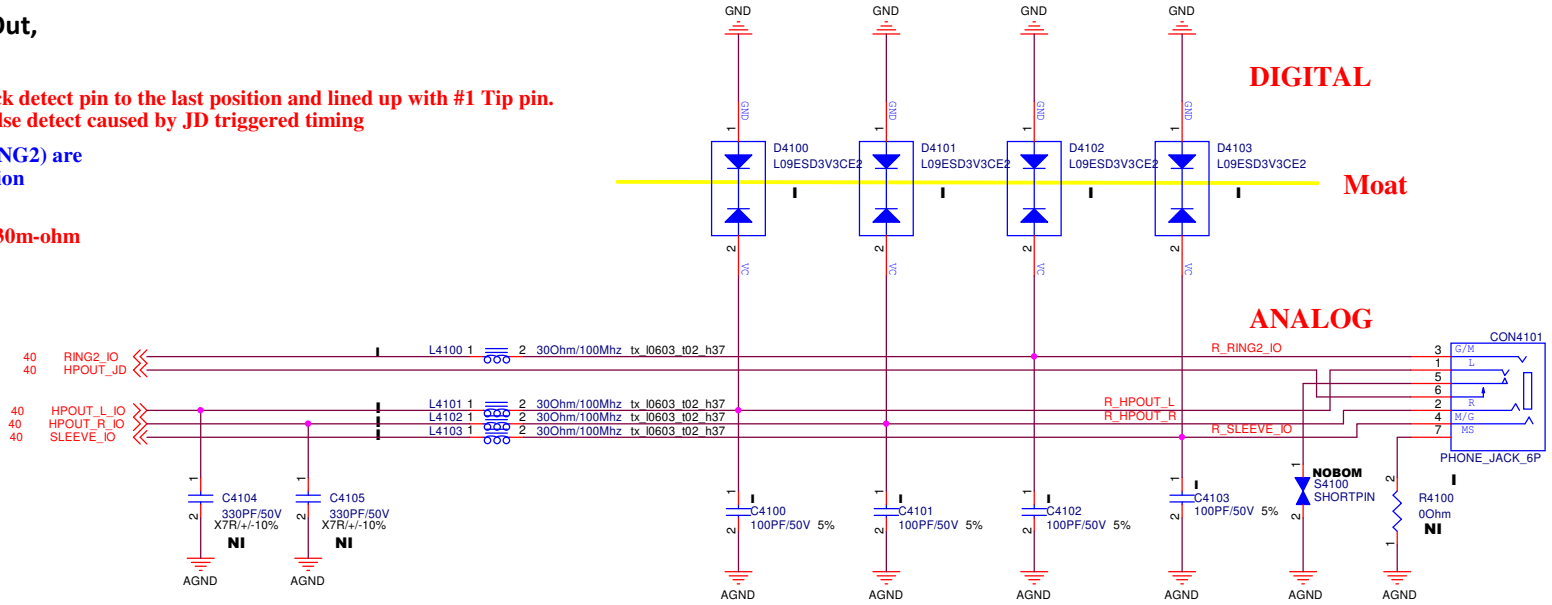
GLOBAL HEADSET CONNECTOR

**OMTP/CTIA headset, Headphone, Line-Out,
Microphone input, Line input.**

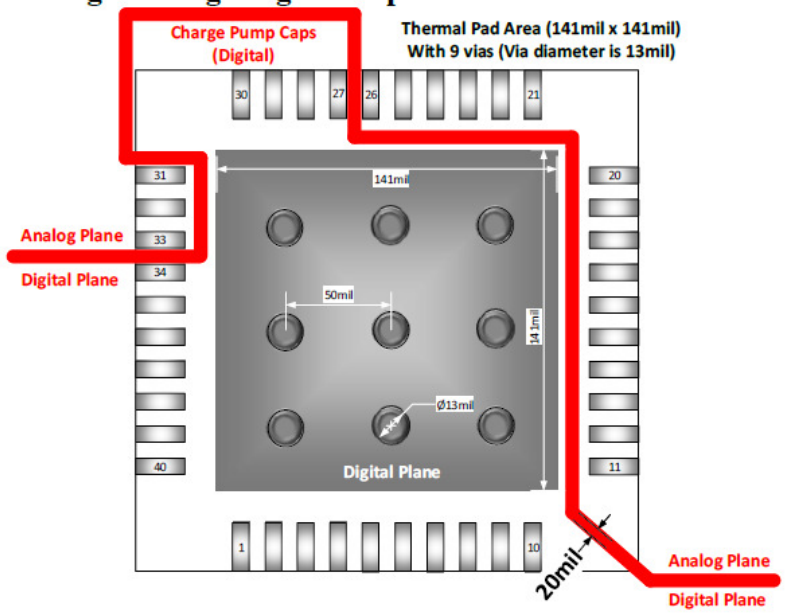
**This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin.
This kind of design will significantly improve the false detect caused by JD triggered timing**

**PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are
required at least 40 mil for HP crosstalk consideration
and, its length should be as short as possible.**

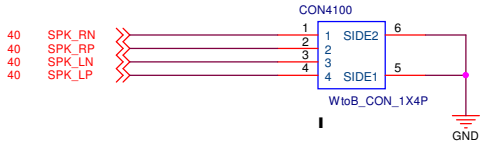
**L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm
to get the best audio performance for HP crosstalk.**



Separate Analog and Digital ground plane



SPEAKER CONN



<Core Design>

PEGATRON Title : AUDIO JACK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

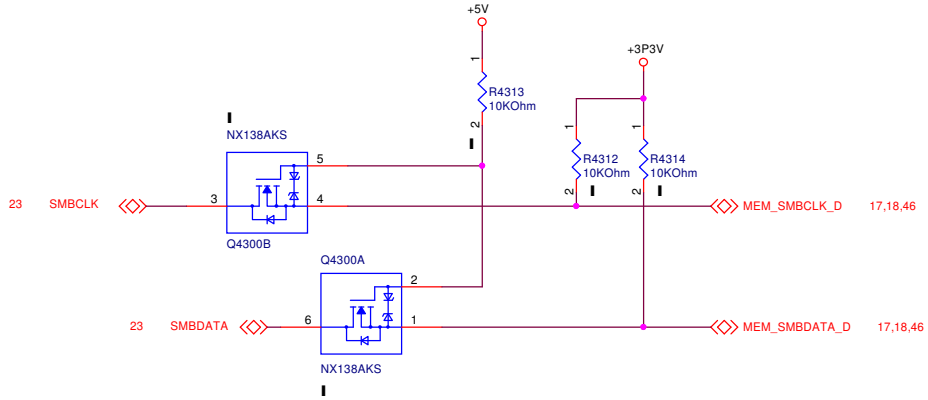
Date: Wednesday, November 28, 2018 Sheet 41 of 94

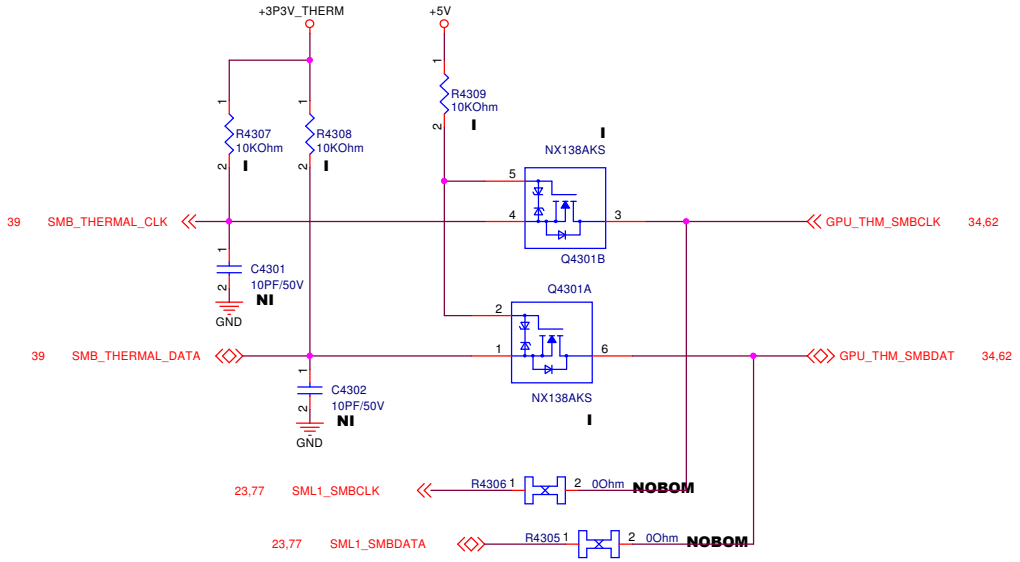
Reserved Page

<Core Design>

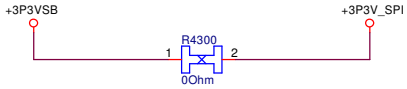
PEGATRON	Title : Reserved	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 42 of 94	

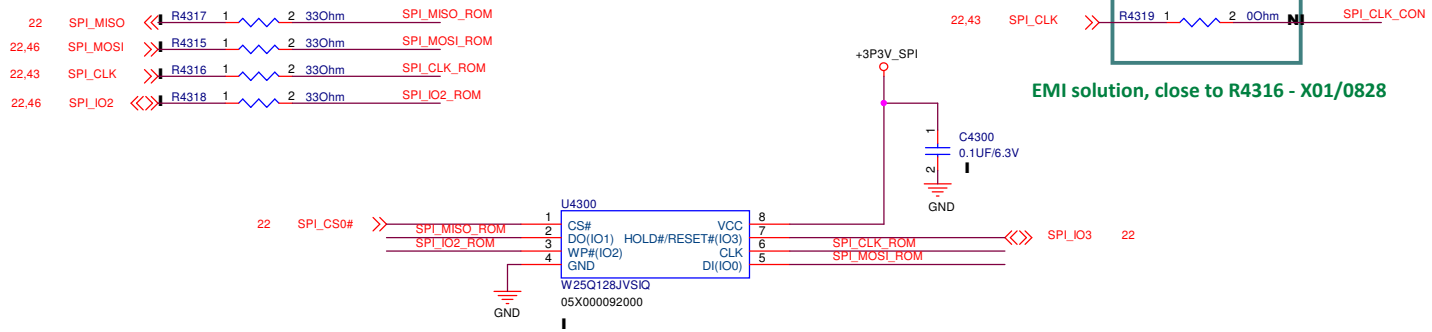
SMBUS



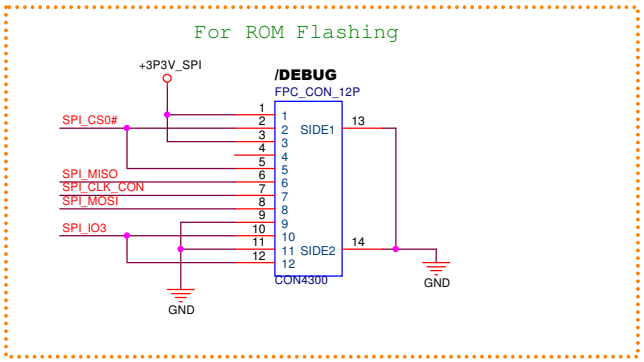


SPI ROM (Quad I/O Supported)



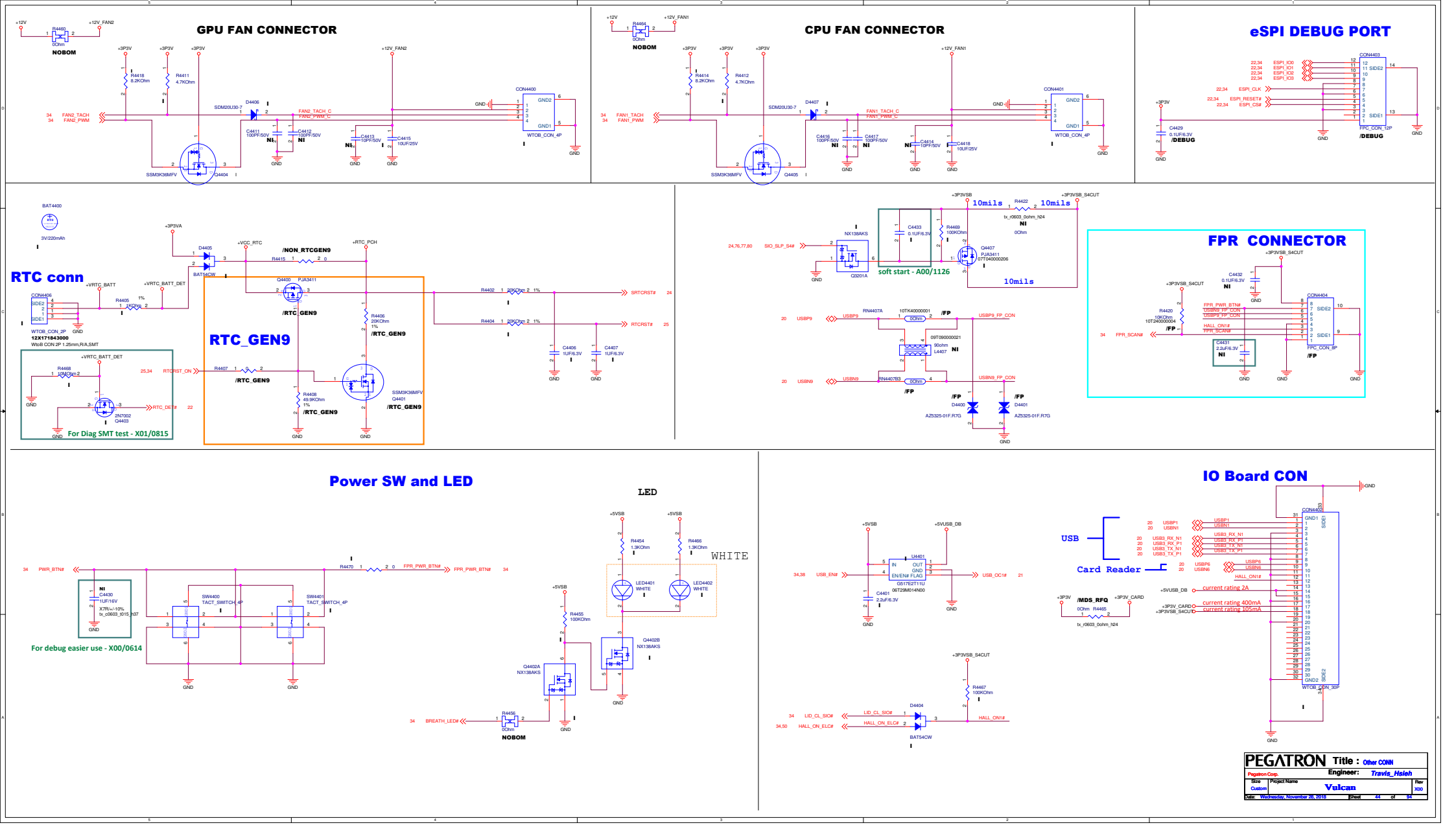


EMI solution, close to R4316 - X01/0828



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SM BUS & SPI ROM		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size A3	Project Name Vulcan		Rev X00
Date: Wednesday, November 28, 2018	Sheet 43 of 94		


GPU FAN CONNECTOR
CPU FAN CONNECTOR
eSPI DEBUG PORT
RTC conn
RTC_GEN9
FPR CONNECTOR
soft start - A00/1126
Power SW and LED
LED
IO Board CON
USB
Card Reader
For Diag SMT test - X01/0815
For debug easier use - X00/0614
NOBOM
/DEBUG
/FP
/RTC_GEN9
WHITE
current rating 2A
current rating 400mA
current rating 105mA
PEGATRON
Title : Other CONN
Engineer: Travis_Hsieh
Pegatron Corp.
Vulcan
Wednesday, November 28, 2018
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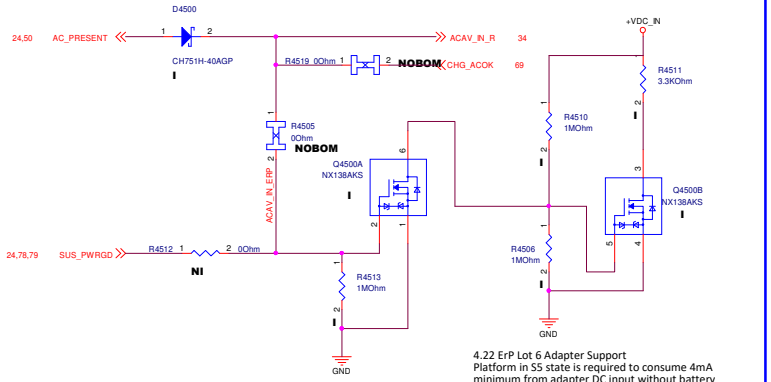
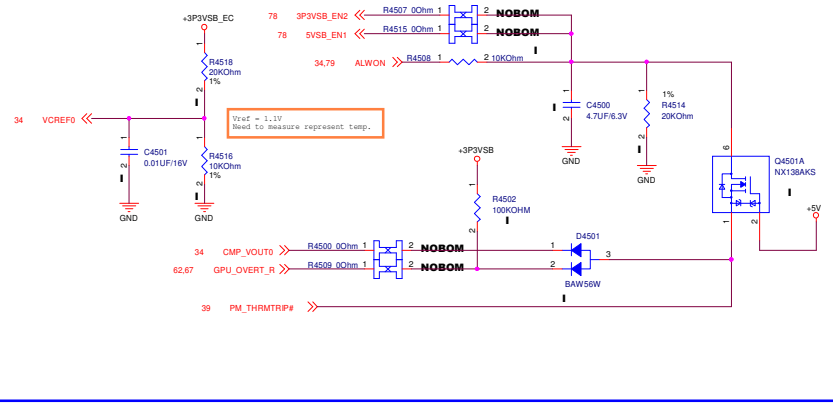
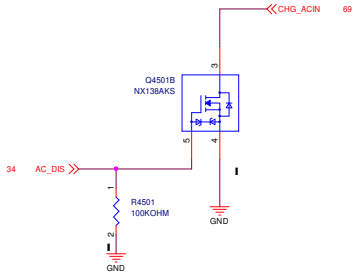
ACAV_IN Circuit



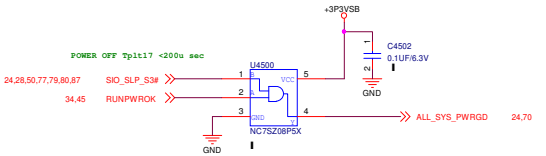
4.22 ErP Lot 6 Adapter Support
Platform in S5 state is required to consume 4mA minimum from adapter DC input without battery attached at the moment of plugging in system.

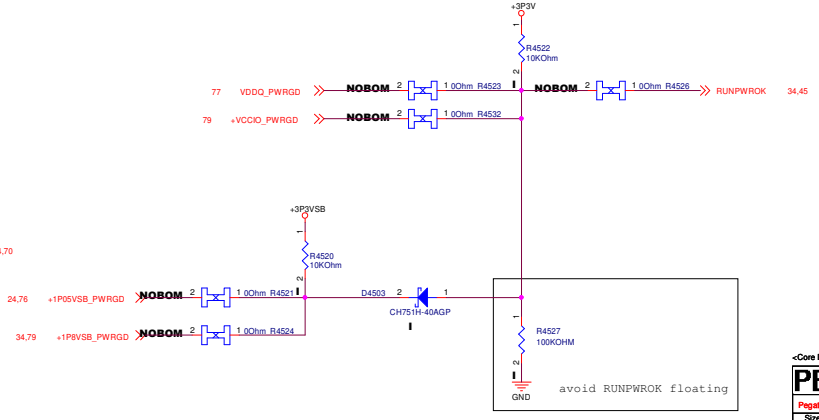
Thermal CMP Circuit





POWER GOOD DETECTER





<Core Design>

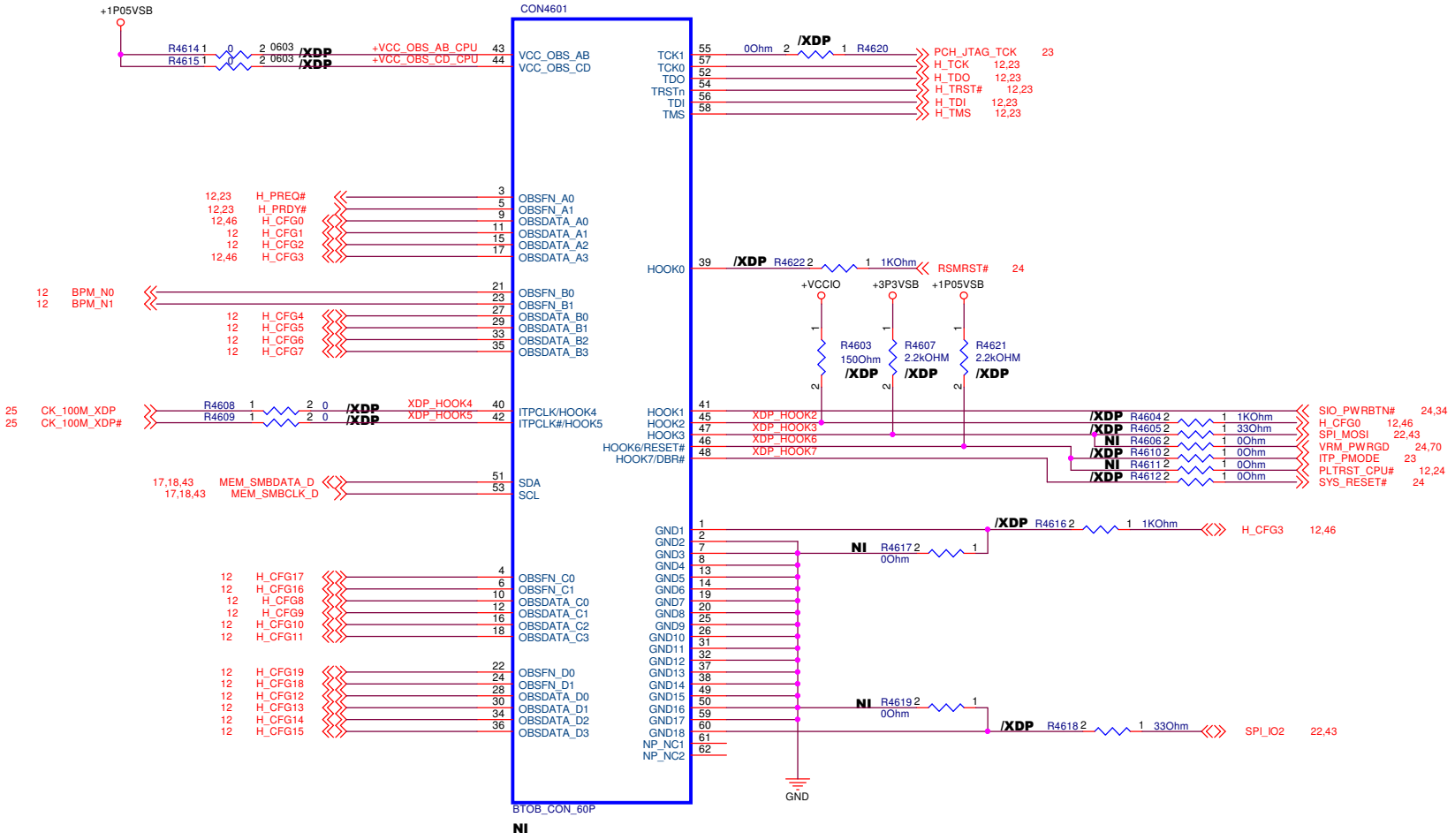
PEGATRON Title : ACAV_IN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 45 of 94

INTEL XDP DEBUG CONN



PEGATRON Title : XDP

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 46 of 94

NOBOM

PCB4700

PCB

PCB_BOARD

CCL = Y

H4730 CT217B142D126 GND

H4729 CT217B142D126 GND

I

Fan Nut

For CPU

H4708 C276D157 **NOBOM**

H4710 C276D157 **NOBOM**

H4712 C276D157 **NOBOM**

H4719 C276D157 **NOBOM**

For GPU

H4723 C236D157 **NOBOM**

H4716 C236D157 **NOBOM**

H4700 C236D157 **NOBOM**

GND

H4748 C315D157 **NOBOM**

H4747 C315D157 **NOBOM** **B**

H4746 C315D157 **NOBOM**

H4745 C315D157 **NOBOM**

H4744 C315D236 **NOBOM** **N**

H4743 C315D217 **NOBOM** **G**

H4742 RT374X276B276D157 **NOBOM** **E**

H4750 O122x83DO122x83N **NOBOM** **J**

H4751 C118D118N **NOBOM** **K**

H4753 C315D157 **NOBOM**

H4754 C315D157 **NOBOM** **M**

H4755 CT315BR315X311D91 **NOBOM** **O**

H4756 RT339X394RB528D91 **NOBOM** **P**

H4757 O39x197DO39x197N **NOBOM** **Q**

GND

<Doc Number>

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCB & Label & Screw

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 47 of 94

Supply max 2.5A

Panel power

+3P3VSB — W=100mils — NOBOM — R4852 0Ohm — +3P3VSB_PANEL_IN

change for power drop test - X01/0828

C4834 2.2uF/6.3V — GND

U4800 G5250A1T12U: IN, OUT, GND, DSG, EN

R4859 33Ohm — +3P3V_PANEL_O

+3P3V_PANEL_O — R4835 0Ohm NOBOM — W=100mils — +3P3V_PANEL

C4833 4.7UF/6.3V — GND

+AC_BAT_SYS — W=60mils — L4801 120Ohm/100Mhz — C4808 0.1UF/25V — GND

NOBOM — R4857 0Ohm — F4800 4A/32V

EMC預留 - X02 10/24

+VDD_BL_CONN — C4806 2.2UF/25V X5R/+/-10% — C4807 0.1UF/25V — C4809 68PF/50V — C4810 2200PF/50V — GND

34 LCD_VCC_TEST_EN — D4801 BAT54C — R4836 100KOHM — GND

21 ENVDD_PCH — R4853 0Ohm — /NON_GSYNC

62 LCD_VCC_EN_GPU — D4807 SDM20U30-7 — /GSYNC

NON G-SYNC ; CPU

8	EDP_TXN0	R4800 0Ohm	/NON_GSYNC
8	EDP_TXP0	R4801 0Ohm	/NON_GSYNC
8	EDP_TXN1	R4802 0Ohm	/NON_GSYNC
8	EDP_TXP1	R4803 0Ohm	/NON_GSYNC
8	EDP_TXN2	R4804 0Ohm	/NON_GSYNC
8	EDP_TXP2	R4805 0Ohm	/NON_GSYNC
8	EDP_TXN3	R4806 0Ohm	/NON_GSYNC
8	EDP_TXP3	R4807 0Ohm	/NON_GSYNC
8	EDP_AUXN	R4808 0Ohm	/NON_GSYNC
8	EDP_AUXP	R4809 0Ohm	/NON_GSYNC
21	EDP_HPD	R4810 0Ohm	/NON_GSYNC

EDP_MUX_AUXN — EDP_MUX_AUXP — EDP_MUX_HPD_CON

61	IFPD_EDP_AUXN	R4811 0Ohm	/GSYNC
61	IFPD_EDP_AUXP	R4812 0Ohm	/GSYNC
62	IFPD_HPD	R4813 0Ohm	/GSYNC
61	IFPD_EDP_TXN0	R4814 0Ohm	/GSYNC
61	IFPD_EDP_TXP0	R4815 0Ohm	/GSYNC
61	IFPD_EDP_TXN1	R4816 0Ohm	/GSYNC
61	IFPD_EDP_TXP1	R4817 0Ohm	/GSYNC
61	IFPD_EDP_TXN2	R4818 0Ohm	/GSYNC
61	IFPD_EDP_TXP2	R4819 0Ohm	/GSYNC
61	IFPD_EDP_TXN3	R4820 0Ohm	/GSYNC
61	IFPD_EDP_TXP3	R4821 0Ohm	/GSYNC

EDP_MUX_TXN0 — EDP_MUX_TXP0 — EDP_MUX_TXN1 — EDP_MUX_TXP1 — EDP_MUX_TXN2 — EDP_MUX_TXP2 — EDP_MUX_TXN3 — EDP_MUX_TXP3

G-SYNC ; GPU

21 L_BKLT_EN_EC — R4854 0Ohm — /NON_GSYNC

62 LCD_BLEN_GPU — D4808 BAT54C — R4847 100KOHM — GND

BKLT_IN_EC_D 34

+3P3V — F4801 0.5A/32V — +3P3V_MIC — C4837 0.1UF/6.3V — GND

Follow Vendor comment - X00/0516

+3P3V_CAM — C4805 0.1UF/6.3V — GND

R4851 0Ohm NOBOM

eDP CONNECTOR

FPC_CON_40P

22 LCD_DBC

40 DMIC_CLK1 — DMIC_CLK1

40 DMIC_DATA1 — DMIC_DATA1

EDP_MUX_TXP0	C4813	0.1UF/6.3V	EDP_TXP0_C
EDP_MUX_TXN0	C4815	0.1UF/6.3V	EDP_TXN0_C
EDP_MUX_TXP1	C4817	0.1UF/6.3V	EDP_TXP1_C
EDP_MUX_TXN1	C4819	0.1UF/6.3V	EDP_TXN1_C
EDP_MUX_TXP2	C4821	0.1UF/6.3V	EDP_TXP2_C
EDP_MUX_TXN2	C4823	0.1UF/6.3V	EDP_TXN2_C
EDP_MUX_TXP3	C4824	0.1UF/6.3V	EDP_TXP3_C
EDP_MUX_TXN3	C4826	0.1UF/6.3V	EDP_TXN3_C
EDP_MUX_AUXP	C4832	0.1UF/6.3V	EDP_AUXP_C
EDP_MUX_AUXN	C4830	0.1UF/6.3V	EDP_AUXN_C

EDP_HPD_CON — R4840 NOBOM 0Ohm

22 CAM_CBL_DET# — +3P3V_MIC

SIDE1 41 — SIDE2 42 — CON4800 — GND

20 USBP5 — 0OHM RN4800B — USBP5_RD_R

NI L4800 90ohm 09T090002I00

20 USBN5 — 0OHM RN4800A — USBN5_RD_R

DMIC_CLK1 — DMIC_DATA1

C4835 12PF/50V NI — C4836 12PF/50V NI — D4804 AZ5125-01J — D4805 AZ5125-01J — GND

+3P3V_PANEL — W=60mils — C4803 0.1UF/6.3V — NI C4839 10PF/50V — GND

Reserve for Panel Overdrive - X00/0717

34 PANEL_BKEN_EC — R4858 0Ohm — D4809 SDM20U30-7

RF預留 - X02 10/24

34 PANEL_OVERDRI — R4856 0Ohm NI

22 CAM_1SB_DET# — CAM_1SB_DET#

34 LCD_TST — R4828 NOBOM 0Ohm — BIA_PWM_PCH_R

21 BIA_PWM_PCH — D4802 SDM20U30-7 — /NON_GSYNC

LCD_VCC_TEST_EN — D4803 SDM20U30-7

62 BL_PWM_GPU — D4806 SDM20U30-7 — /GSYNC

+VDD_BL_CONN — R4834 100KOHM — R4839 100KOHM — NI C4838 10PF/50V — GND

RF預留 - X02 10/24

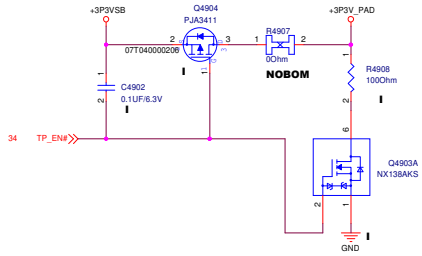
<Core Design>

PEGATRON Title : eDP CON.

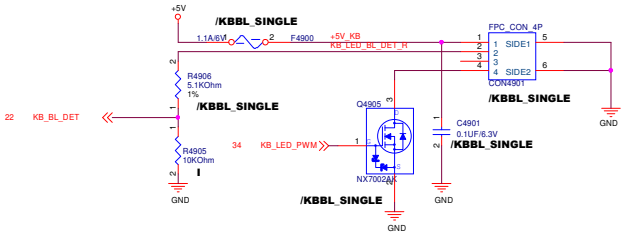
Pegatron Corp. Engineer: Travis_Hsieh

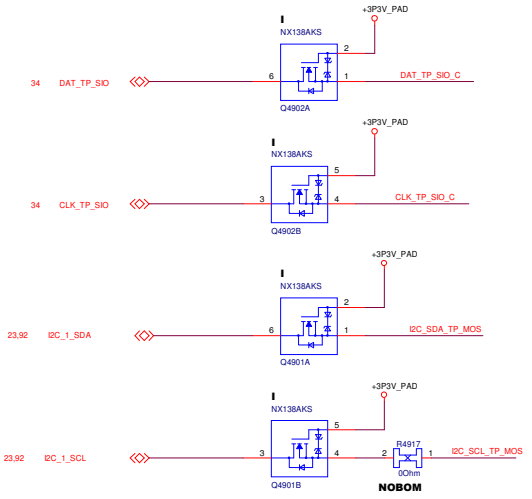
Size	Project Name	Rev
A2	Vulcan	X00

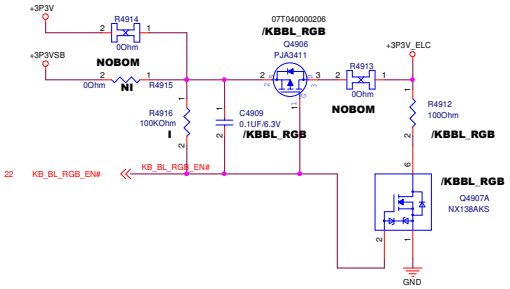
Date: Wednesday, November 28, 2018 Sheet 48 of 94



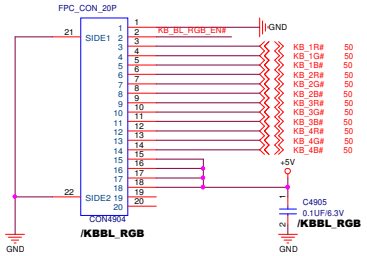
KB BL Conn



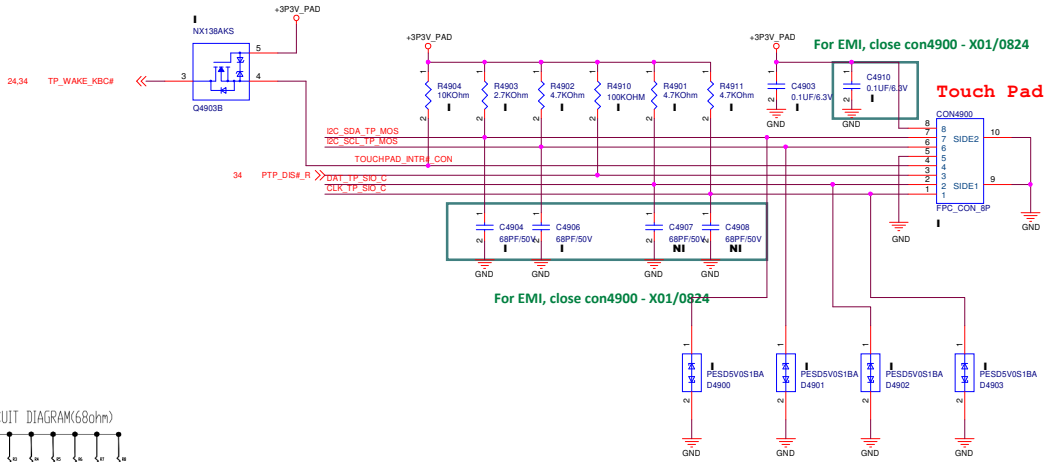


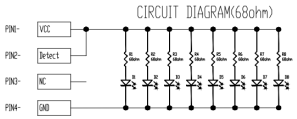


KB_BL_ID		
Config	KB_BL_RGB_EN#	KB_BL_DET
KB_BL_RGB	0	0
KB_BL_SINGLE	1	1
KB_NON_BL	1	0
N/A	1	1



Keyboard backlight





VCC : +5V
LED Vf : 2.8 ~ 3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.8V)
Power consumption	158.82 mA	284.71 mA

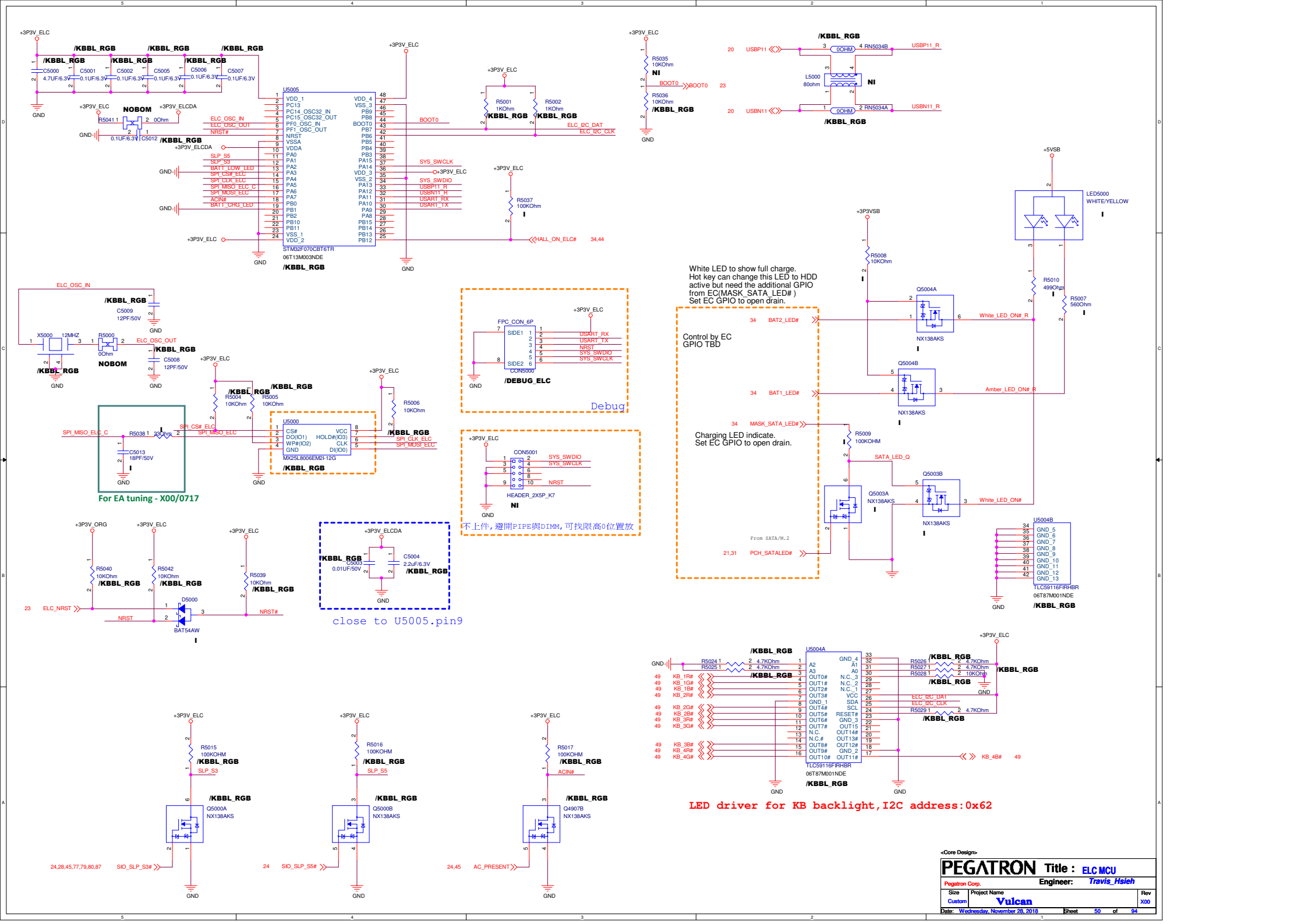
<Core Design>

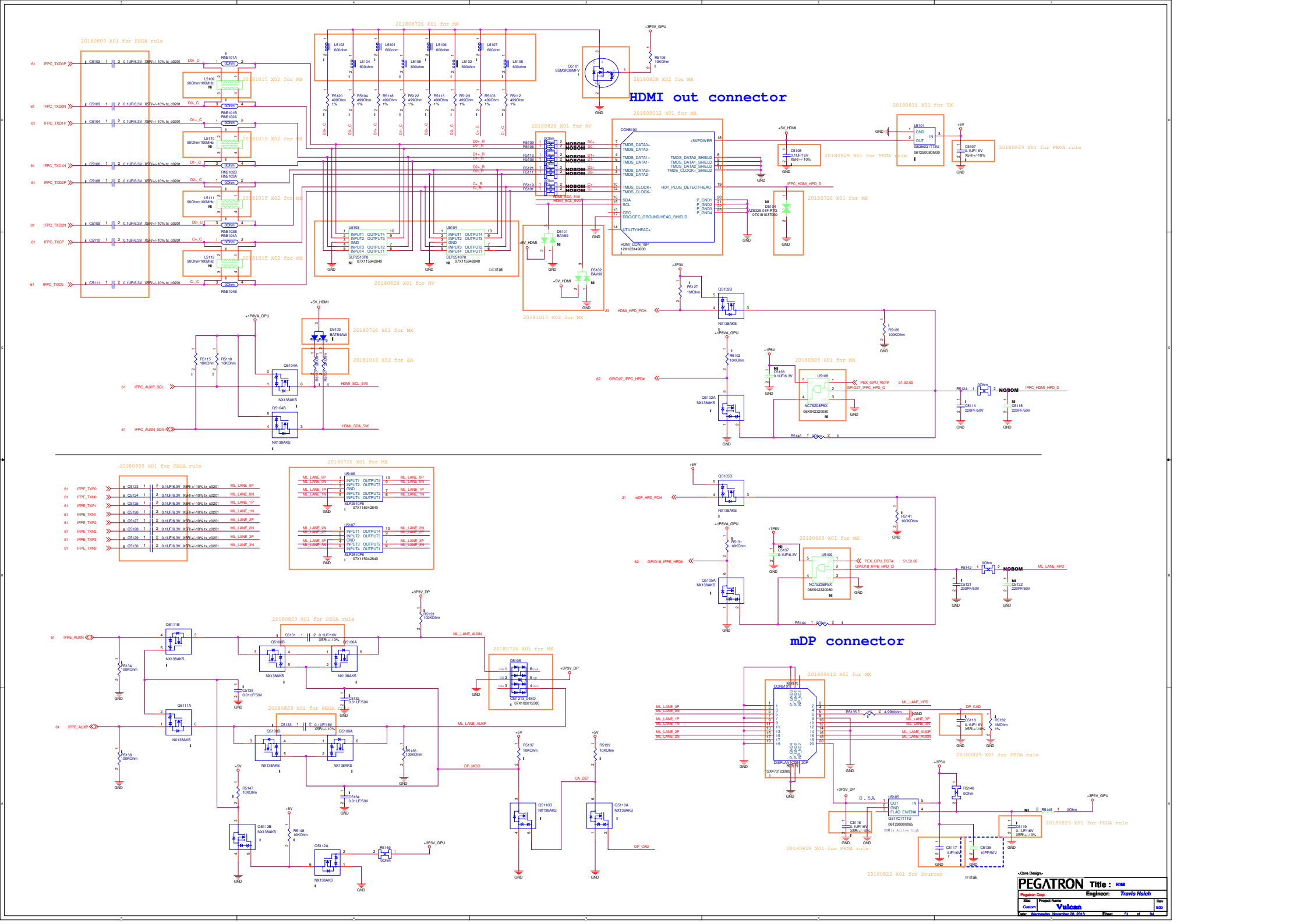
PEGATRON Title : Touch & Keyboard BL

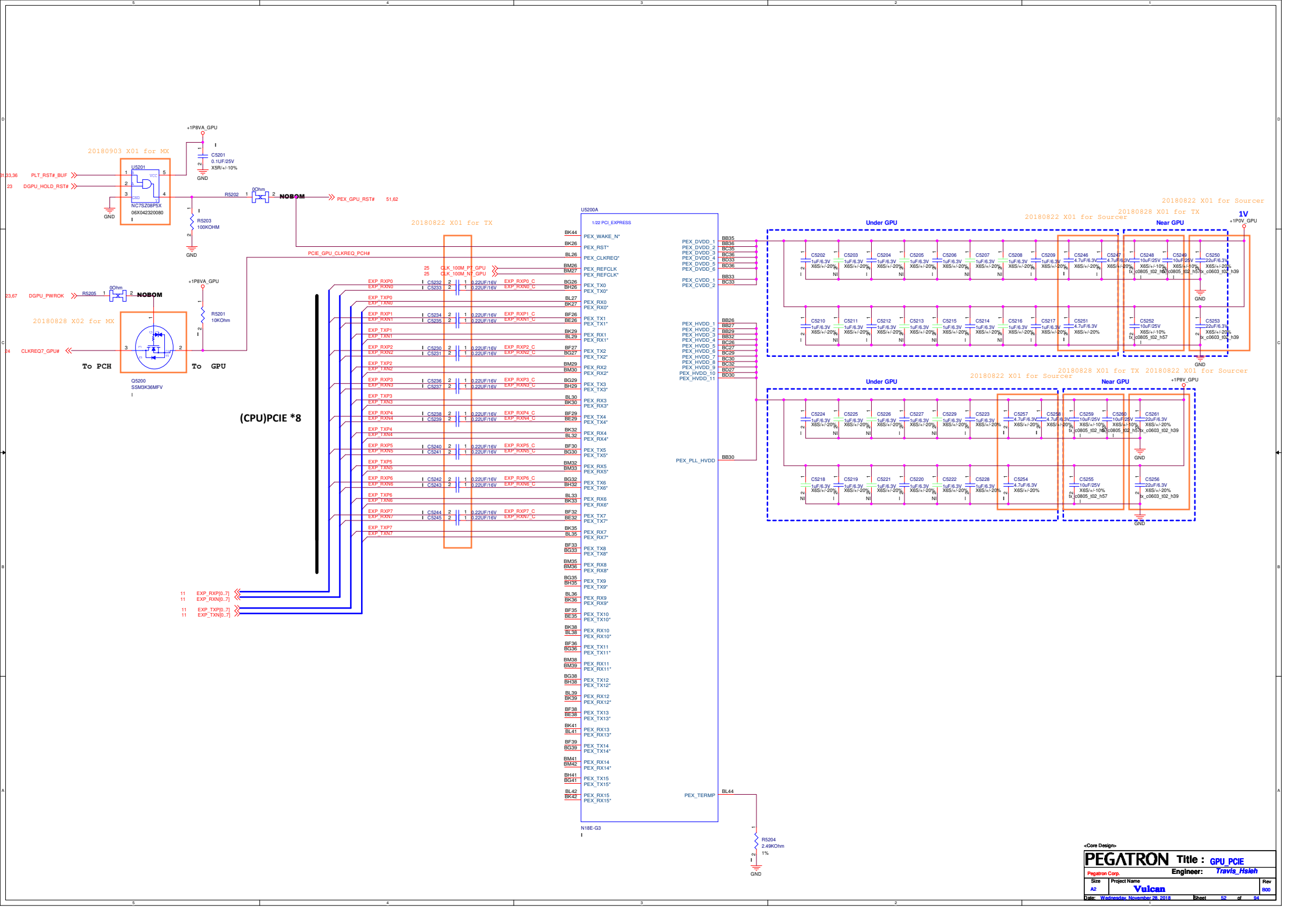
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 49 of 94


+3P3V_ELC
/KBBL_RGB
C5000 4.7UF/6.3V
C5001 0.1UF/6.3V
C5002 0.1UF/6.3V
C5005 0.1UF/6.3V
C5006 0.1UF/6.3V
C5007 0.1UF/6.3V
GND
NOBOM
+3P3V_ELCDA
R5041 0Ohm
C5012 0.1UF/6.3V
U5005
STM32F070CBT6TR
06T13M003NDE
ELC_OSC_IN
ELC_OSC_OUT
NRST#
SLP_S5
SLP_S3
BAT1_LOW_LED
SPI_CS#_ELC
SPI_CLK_ELC
SPI_MISO_ELC_C
SPI_MOSI_ELC
ACIN#
BAT1_CHG_LED
BOOT0
SYS_SWCLK
SYS_SWDIO
USBPT1_R
USBN11_R
USART_RX
USART_TX
ELC_I2C_DAT
ELC_I2C_CLK
R5001 1KOhm
R5002 1KOhm
R5037 100KOhm
HALL_ON_ELC#
R5035 10KOhm NI
R5036 10KOhm
R5034B 0OHM
R5034A 0OHM
L5000 80ohm NI
USBP11_R
USBN11_R
LED5000 WHITE/YELLOW
+3P3VSB
+5VSB
R5008 10KOhm
R5010 499Ohm
R5007 560Ohm
Q5004A NX138AKS
Q5004B NX138AKS
White_LED_ON#_R
Amber_LED_ON#_R
White_LED_ON#
BAT2_LED#
BAT1_LED#
MASK_SATA_LED#
SATA_LED_Q
R5009 100KOHM
Q5003A NX138AKS
Q5003B NX138AKS
PCH_SATALED#
From SATA/M.2
White LED to show full charge.
Hot key can change this LED to HDD active but need the additional GPIO from EC(MASK_SATA_LED#)
Set EC GPIO to open drain.
Control by EC GPIO TBD
Charging LED indicate.
Set EC GPIO to open drain.
U5004B TLC59116FIRHBR 06T87M001NDE
GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13
X5000 12MHZ
C5009 12PF/50V
C5008 12PF/50V
R5000 0Ohm
ELC_OSC_IN
ELC_OSC_OUT
FPC_CON_6P
CON5000
/DEBUG_ELC
Debug
R5004 10KOhm
R5005 10KOhm
R5006 10KOhm
U5000
MX25L8006EM2I-12G
SPI_MISO_ELC_C
R5038 33Ohm
C5013 18PF/50V
SPI_CS#_ELC
SPI_MISO_ELC
SPI_CLK_ELC
SPI_MOSI_ELC
For EA tuning - X00/0717
CON5001
HEADER_2X5P_K7
NI
SYS_SWDIO
SYS_SWCLK
NRST
不上件，避開PIPE與DIMM，可找限高0位置放
+3P3V_ORG
R5040 10KOhm
R5042 10KOhm
R5039 10KOhm
ELC_NRST
NRST
NRST#
D5000
BAT54AW
+3P3V_ELCDA
C5003 0.01UF/50V
C5004 2.2uF/6.3V
close to U5005.pin9
U5004A TLC59116FIRHBR 06T87M001NDE
R5024 4.7KOhm
R5025 4.7KOhm
R5026 4.7KOhm
R5027 4.7KOhm
R5028 10KOhm
R5029 4.7KOhm
KB_1R# KB_1G# KB_1B# KB_2R#
KB_2G# KB_2B# KB_3R# KB_3G#
KB_3B# KB_4R# KB_4G#
KB_4B#
LED driver for KB backlight,I2C address:0x62
R5015 100KOHM
R5016 100KOHM
R5017 100KOHM
SLP_S3
SLP_S5
ACIN#
Q5000A NX138AKS
Q5000B NX138AKS
Q4907B NX138AKS
24,28,45,77,79,80,87
SIO_SLP_S3#
24
SIO_SLP_S5#
24,45
AC_PRESENT
<Core Design>
PEGATRON
Title : ELC MCU
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 50 of 94


HDMI out connector
mDP connector
20180809 X01 for PEGA rule
20180726 X01 for MX
20180828 X02 for MX
20180828 X01 for NV
20181015 X02 for MX
20180831 X01 for TX
20180829 X01 for PEGA rule
20180903 X01 for MX
20181018 X02 for EA
20180822 X01 for Sourcer
IFPC_TXD0P
IFPC_TXD0N
IFPC_TXD1P
IFPC_TXD1N
IFPC_TXD2P
IFPC_TXD2N
IFPC_TXCP
IFPC_TXCN
IFPC_AUXP_SCL
IFPC_AUXN_SDA
HDMI_SCL_5V0
HDMI_SDA_5V0
HDMI_HPD_PCH
IFPC_HDMI_HPD_D
PEX_GPU_RST#
GPIO27_IFPC_HPD_O
IFPE_TXP0
IFPE_TXN0
IFPE_TXP1
IFPE_TXN1
IFPE_TXP2
IFPE_TXN2
IFPE_TXP3
IFPE_TXN3
IFPE_AUXN
IFPE_AUXP
nDP_HPD_PCH
GPIO18_IFPE_HPD#
ML_LANE_AUXN
ML_LANE_AUXP
DP_MOD
CA_DET
DP_CAD
ML_LANE_HPD
GPIO18_IFPE_HPD_O
+5V_HDMI
+3P3V_GPU
+3P3V_DP
+1P8VA_GPU
+1P8V
+3P3V
+5V
GND
PEGATRON
Title : HDMI
Engineer: Travis Hsieh
Project Name: Vulcan
Rev: B00
Date: Wednesday, November 28, 2018
Sheet 51 of 94


20180903 X01 for MX
+1P8VA_GPU
C5201
0.1UF/25V
X5R/+/-10%
GND
U5201
NC7SZ08P5X
06X042320080
PLT_RST#_BUF
DGPU_HOLD_RST#
R5202
0Ohm
NOBOM
PEX_GPU_RST#
R5203
100KOHM
20180822 X01 for TX
PCIE_GPU_CLKREQ_PCH#
20180828 X02 for MX
DGPU_PWROK
R5205
R5201
10KOhm
CLKREQ7_GPU#
To PCH
To GPU
Q5200
SSM3K36MFV
(CPU)PCIE *8
EXP_RXP[0..7]
EXP_RXN[0..7]
EXP_TXP[0..7]
EXP_TXN[0..7]
U5200A
1/22 PCI_EXPRESS
N18E-G3
PEX_TERMP
R5204
2.49KOhm
1%
20180822 X01 for Sourcer
20180828 X01 for TX
Under GPU
Near GPU
1V
+1P0V_GPU
+1P8V_GPU
<Core Design>
PEGATRON
Title : GPU_PCIE
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev B00
Date: Wednesday, November 28, 2018
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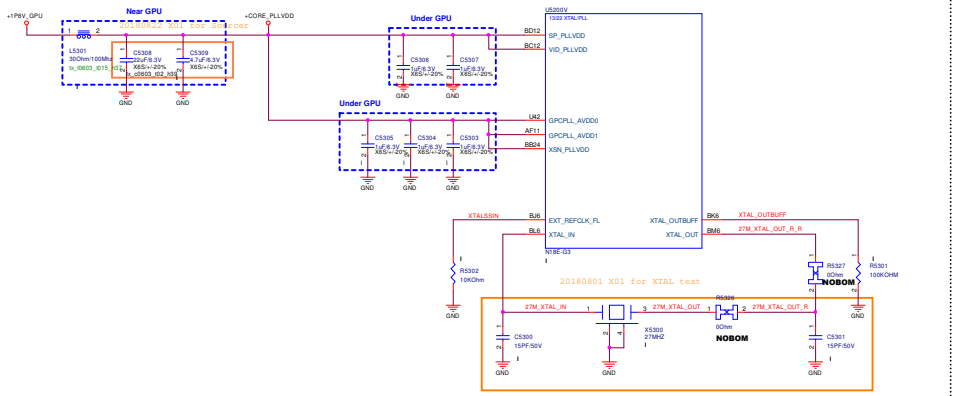


Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

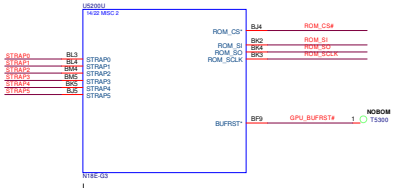
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

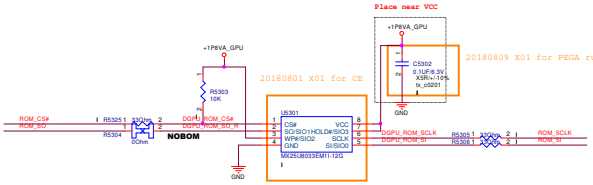
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Straps 需確認strap及ROM(Memory 選未確定)



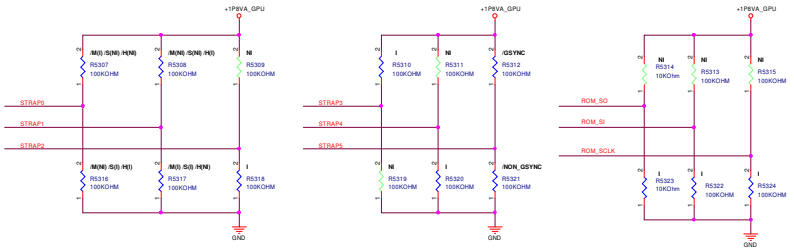


Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx2Chx16	1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:

1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.

Need NV check

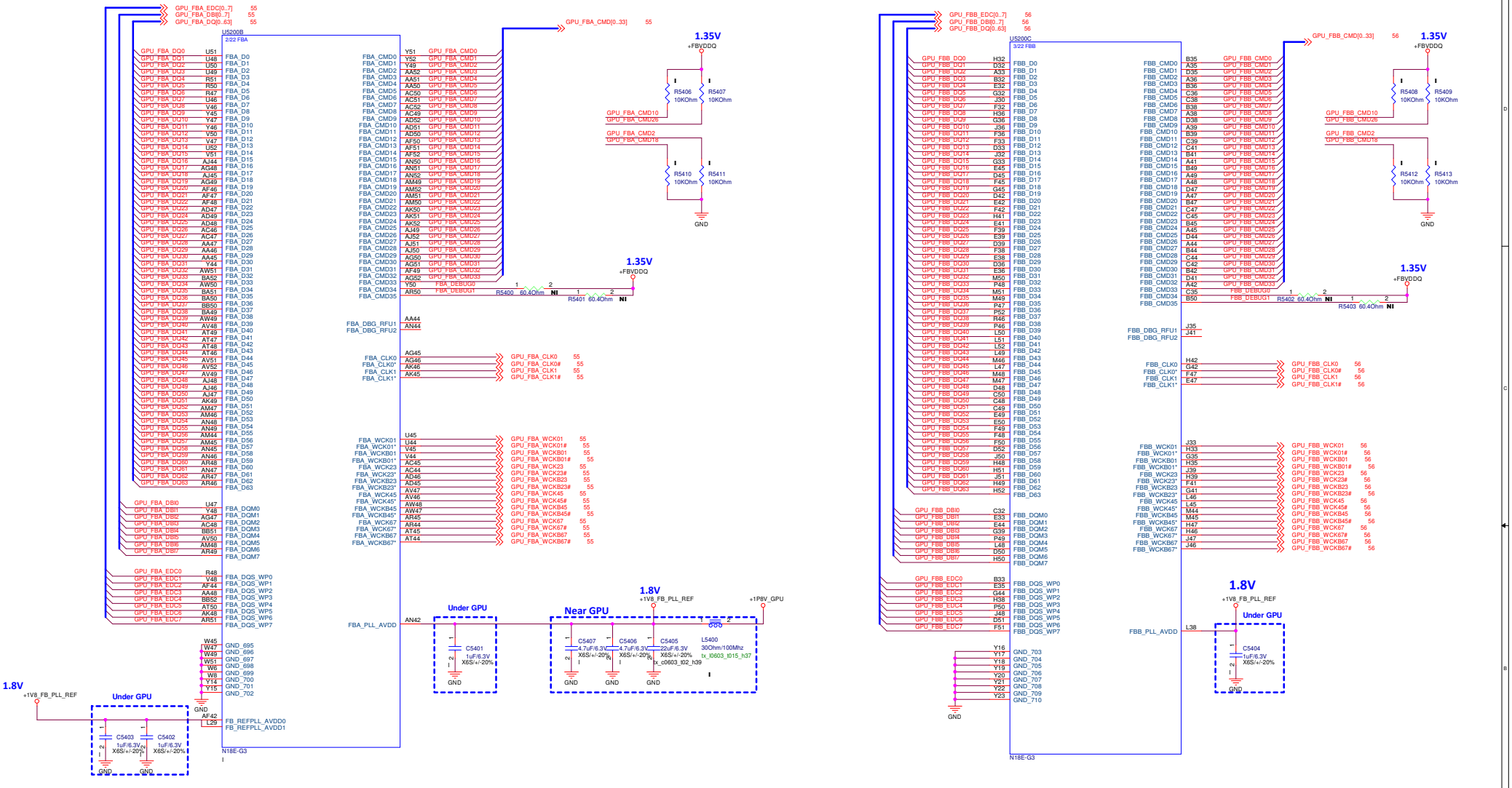


Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate
			Hynix	H56C8H24MJR-S2C	M-die	0x2	14 Gbps	N/A	Full	Production candidate

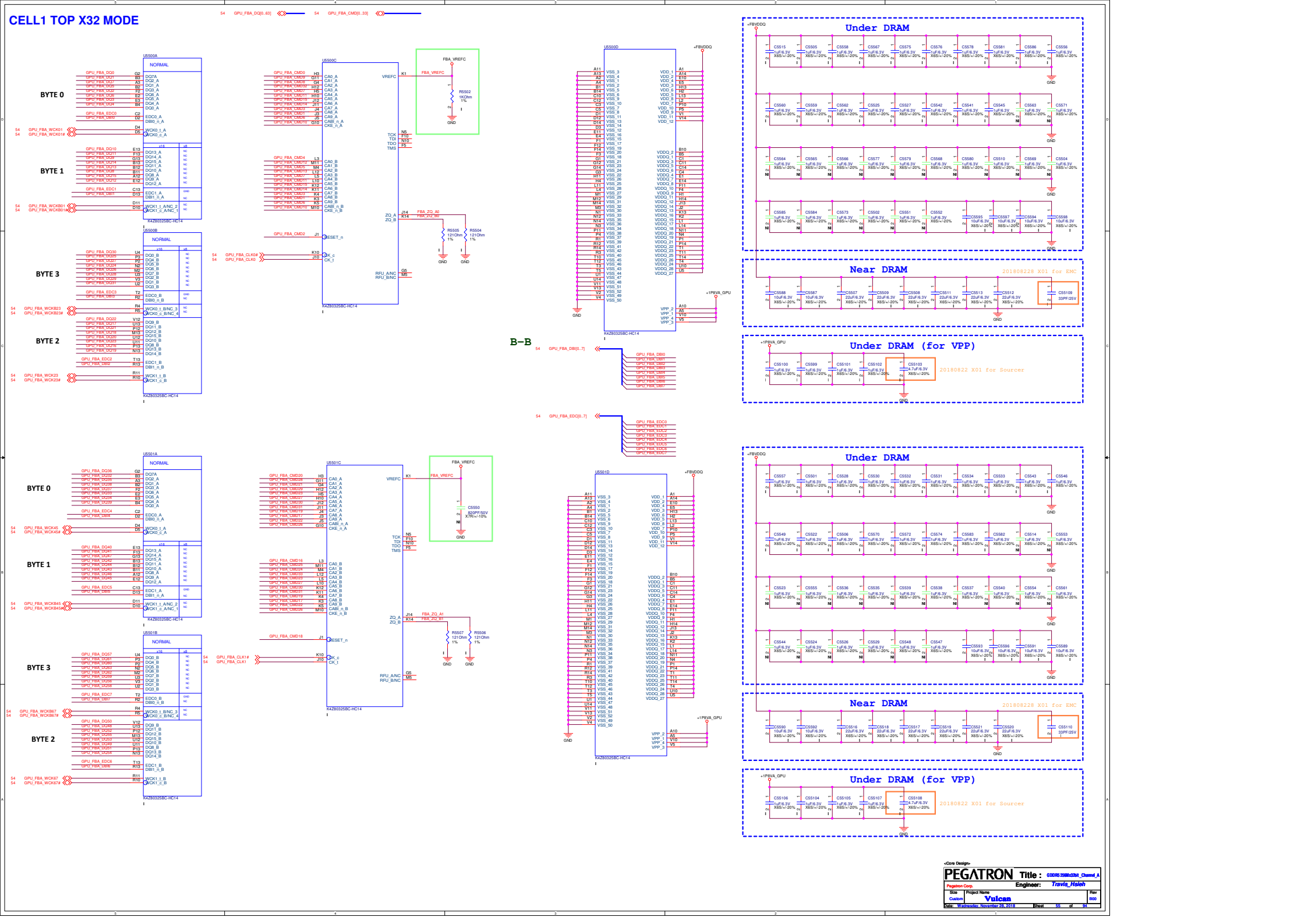
Notes:

1. For N18E-G2, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

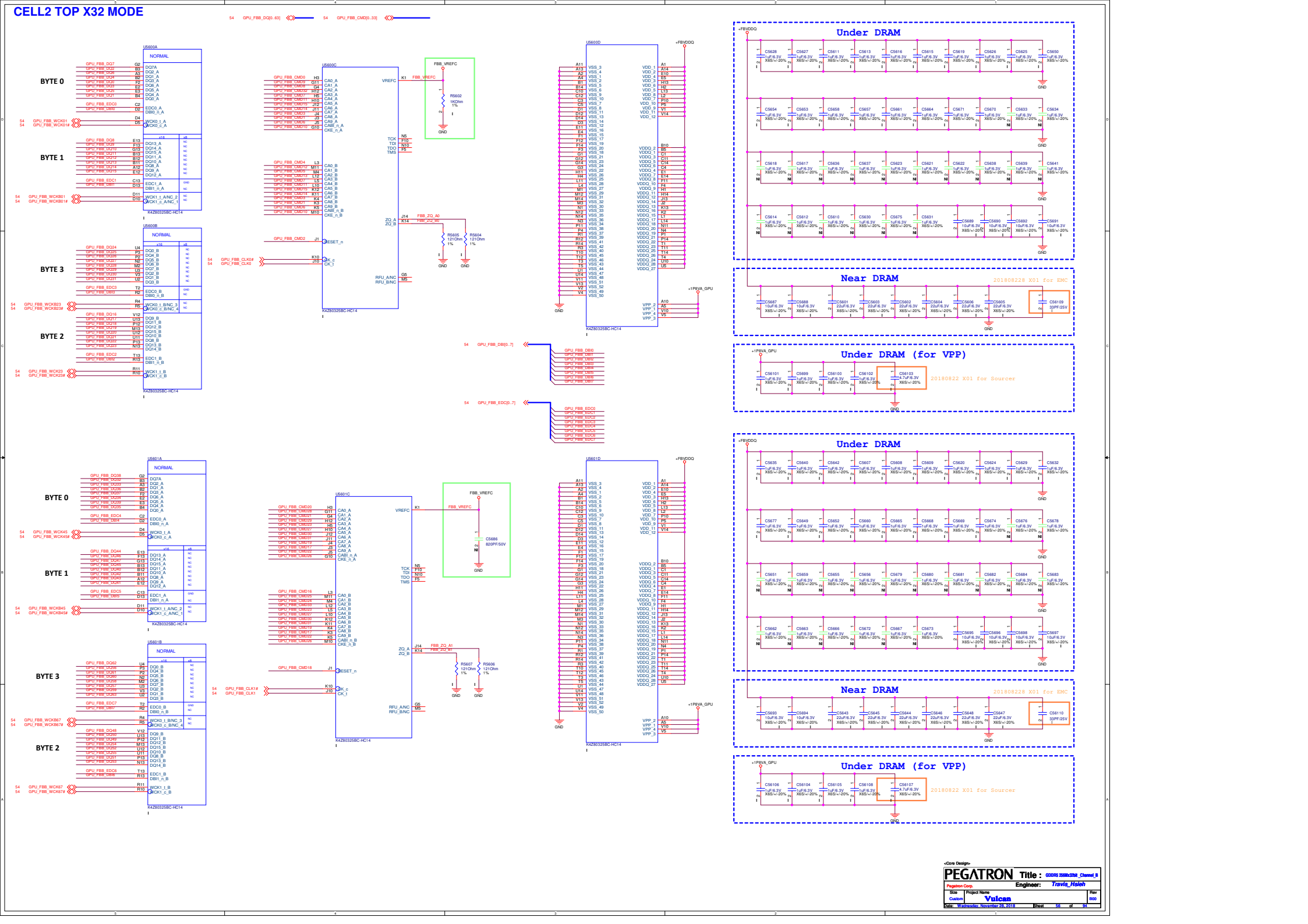
PEGATRON Title : GPU-Xtal & Straps
Pegatron Corp. Engineer: Travis_Haleh
Size: Custom | Project Name: Vulcan | Rev: B00
Date: Wednesday, November 28, 2018 Sheet 53 of 94


U5200B
2/22 FBA
N18E-G3
U5200C
3/22 FBB
N18E-G3
1.35V
+FBVDDQ
1.8V
+1V8_FB_PLL_REF
+1P8V_GPU
Under GPU
Near GPU
GND
R5406 10KOhm
R5407 10KOhm
R5410 10KOhm
R5411 10KOhm
R5408 10KOhm
R5409 10KOhm
R5412 10KOhm
R5413 10KOhm
R5400 60.4Ohm NI
R5401 60.4Ohm NI
R5402 60.4Ohm NI
R5403 60.4Ohm NI
C5401 1uF/6.3V X6S/+/-20%
C5403 1uF/6.3V X6S/+/-20%
C5402 1uF/6.3V X6S/+/-20%
C5404 1uF/6.3V X6S/+/-20%
C5407 4.7uF/6.3V X6S/+/-20%
C5406 4.7uF/6.3V X6S/+/-20%
C5405 22uF/6.3V X6S/+/-20%
L5400 30Ohm/100Mhz
tx_l0603_l02_h39
tx_l0603_l015_h37
GPU_FBA_EDC[0..7] 55
GPU_FBA_DBI[0..7] 55
GPU_FBA_DQ[0..63] 55
GPU_FBA_CMD[0..33] 55
GPU_FBB_EDC[0..7] 56
GPU_FBB_DBI[0..7] 56
GPU_FBB_DQ[0..63] 56
GPU_FBB_CMD[0..33] 56

CELL1 TOP X32 MODE



CELL2 TOP X32 MODE



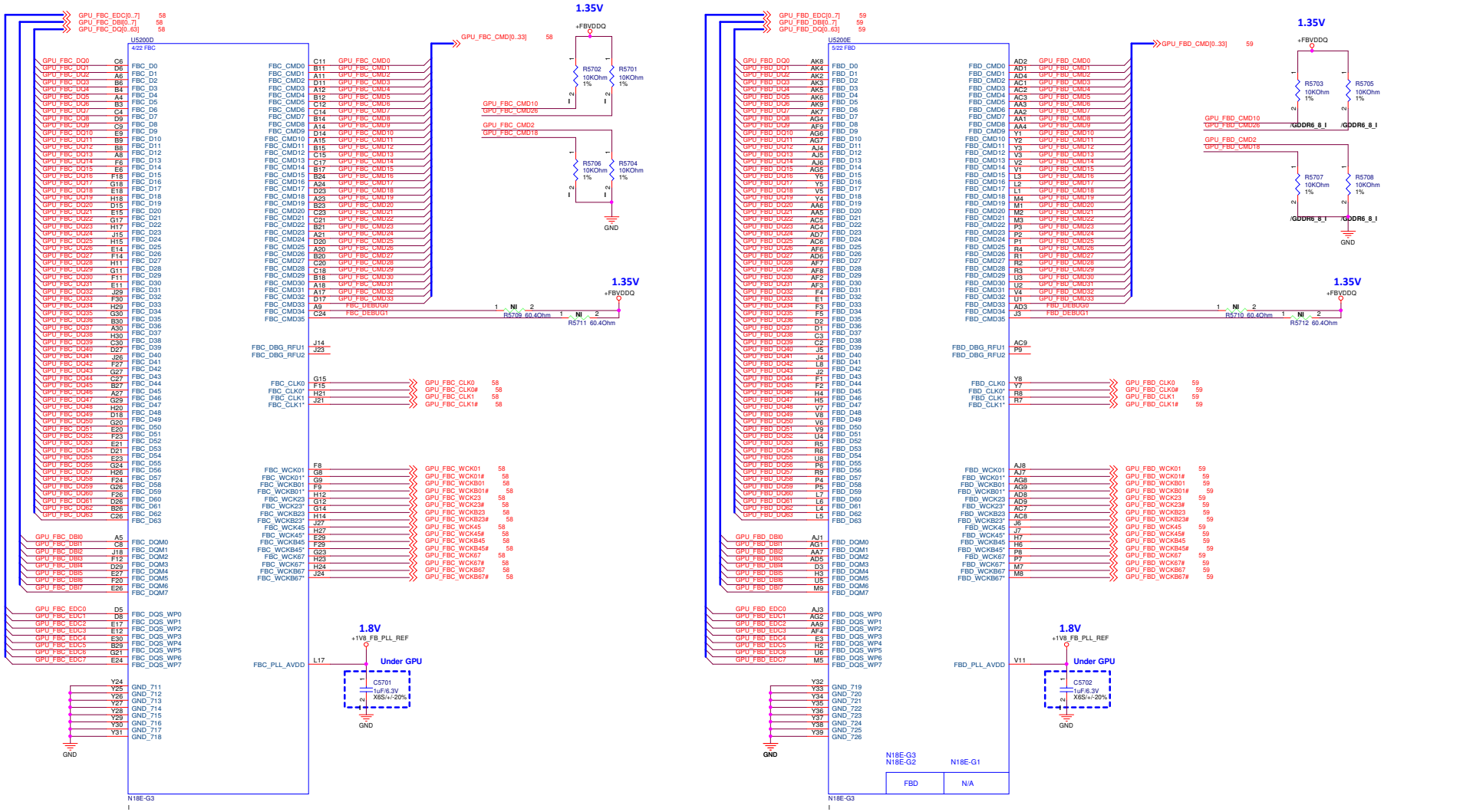
<Core Design>

PEGATRON Title : GDDR5 256Mx32bit_Channel_B

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	900

Date: Wednesday, November 28, 2018 Sheet 58 of 94



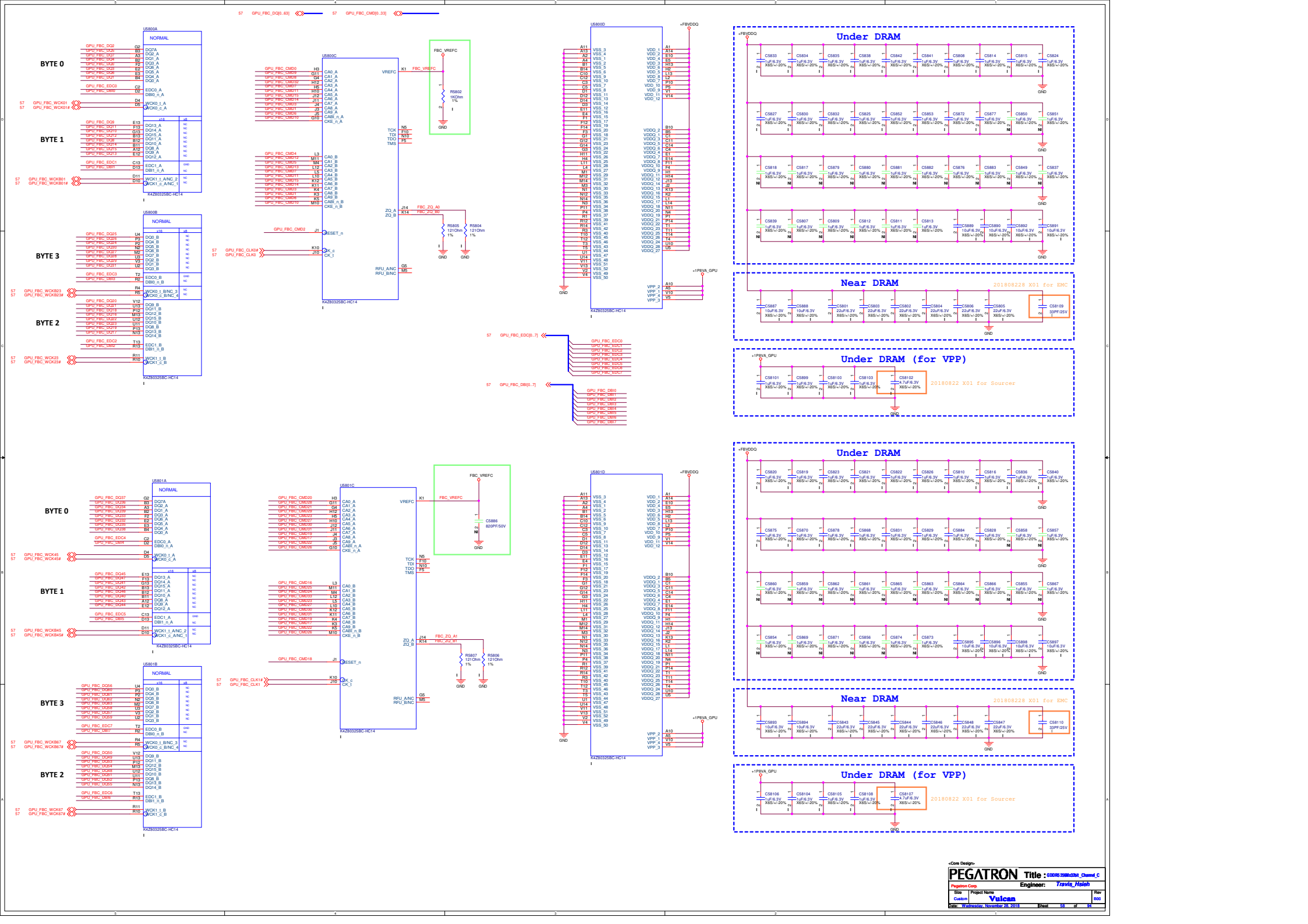
<Core Design>

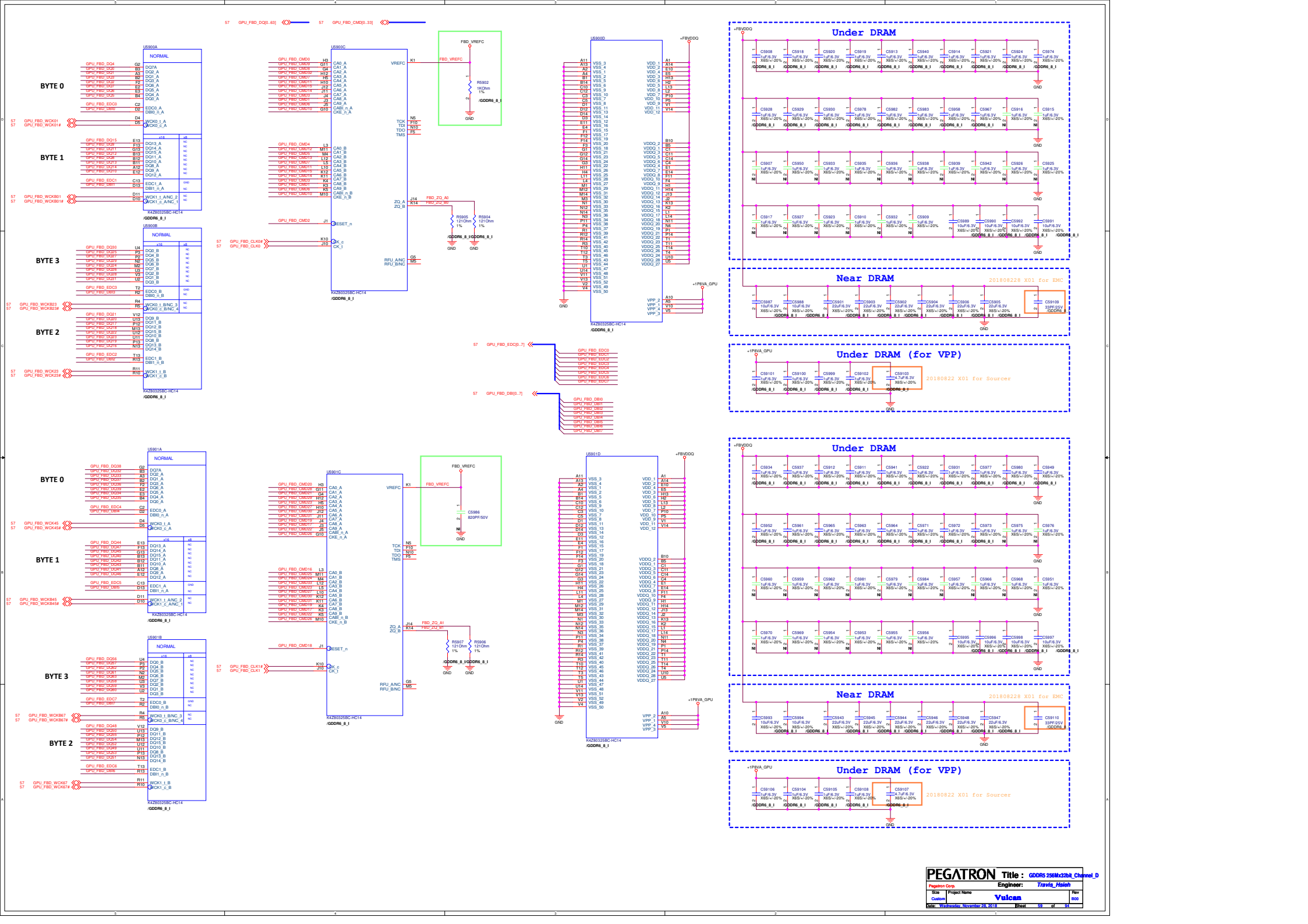
PEGATRON Title : GPU-BUFFER PARTITION C/D

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 57 of 94


BYTE 0
BYTE 1
BYTE 3
BYTE 2
U5800A
U5800B
U5800C
U5800D
U5801A
U5801B
U5801C
U5801D
NORMAL
K4Z80325BC-HC14
FBC_VREFC
R5802 1KOhm 1%
R5805 121Ohm 1%
R5804 121Ohm 1%
C5886 820PF/50V
R5807 121Ohm 1%
R5806 121Ohm 1%
+FBVDDQ
+1P8VA_GPU
GND
Under DRAM
Near DRAM
Under DRAM (for VPP)
201808228 X01 for EMC
20180822 X01 for Sourcer
<Core Design>
PEGATRON
Title : DDDR5 256Mx32bit_Channel_C
Pegatron Corp.
Engineer: Travis_Hsieh
Size: Custom
Project Name: Vulcan
Rev: B00
Date: Wednesday, November 28, 2018
Sheet 58 of 94


BYTE 0
BYTE 1
BYTE 3
BYTE 2
U5900A
U5900B
U5900C
U5900D
U5901A
U5901B
U5901C
U5901D
NORMAL
K4Z80325BC-HC14
/GDDR6_8_I
FBD_VREFC
R5902 1KOhm 1%
R5905 121Ohm 1%
R5904 121Ohm 1%
R5907 121Ohm 1%
R5906 121Ohm 1%
C5986 820PF/50V
+FBVDDQ
+1P8VA_GPU
Under DRAM
Near DRAM
Under DRAM (for VPP)
201808228 X01 for EMC
20180822 X01 for Sourcer
PEGATRON
Title : GDDR5 256Mx32bit_Channel_D
Pegatron Corp.
Engineer: Travis_Hsieh
Size: Custom
Project Name: Vulcan
Rev: B00
Date: Wednesday, November 28, 2018
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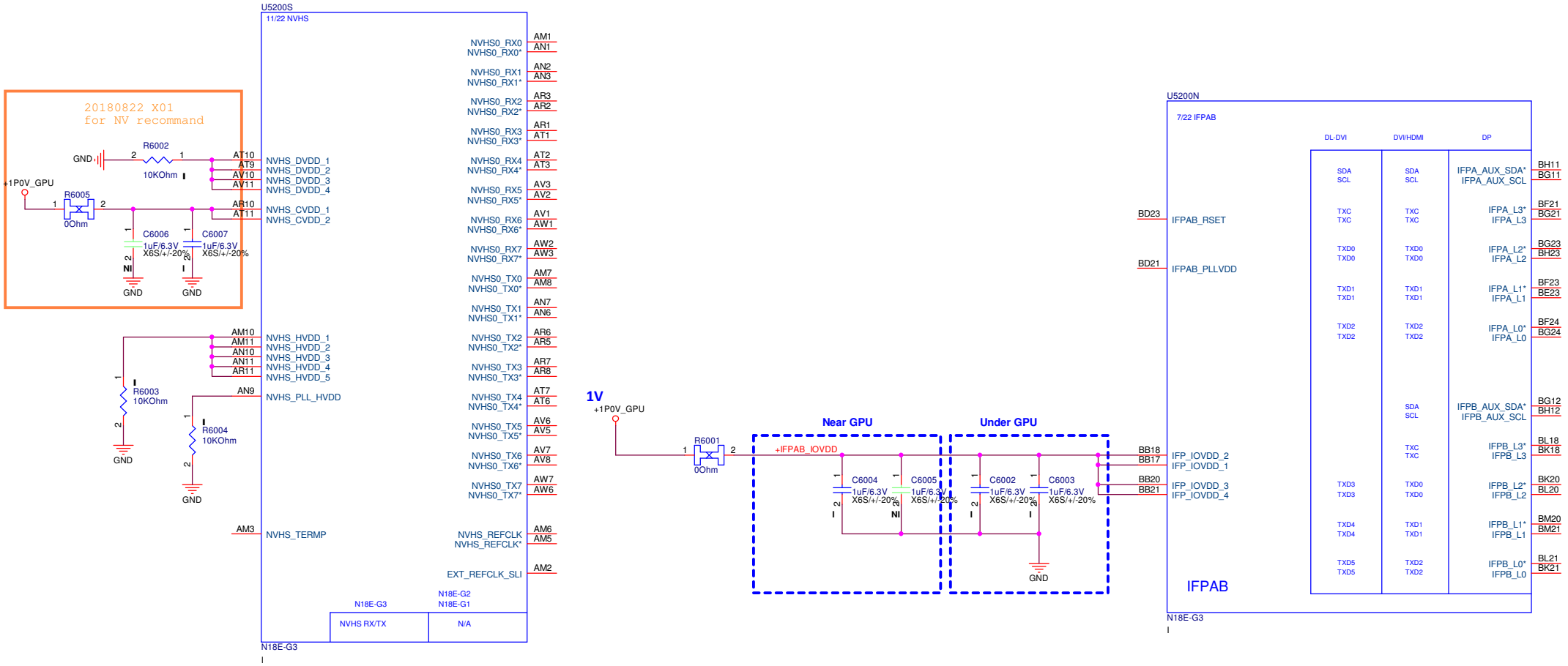


PEGATRON Title : GPU_MIO

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 60 of 94

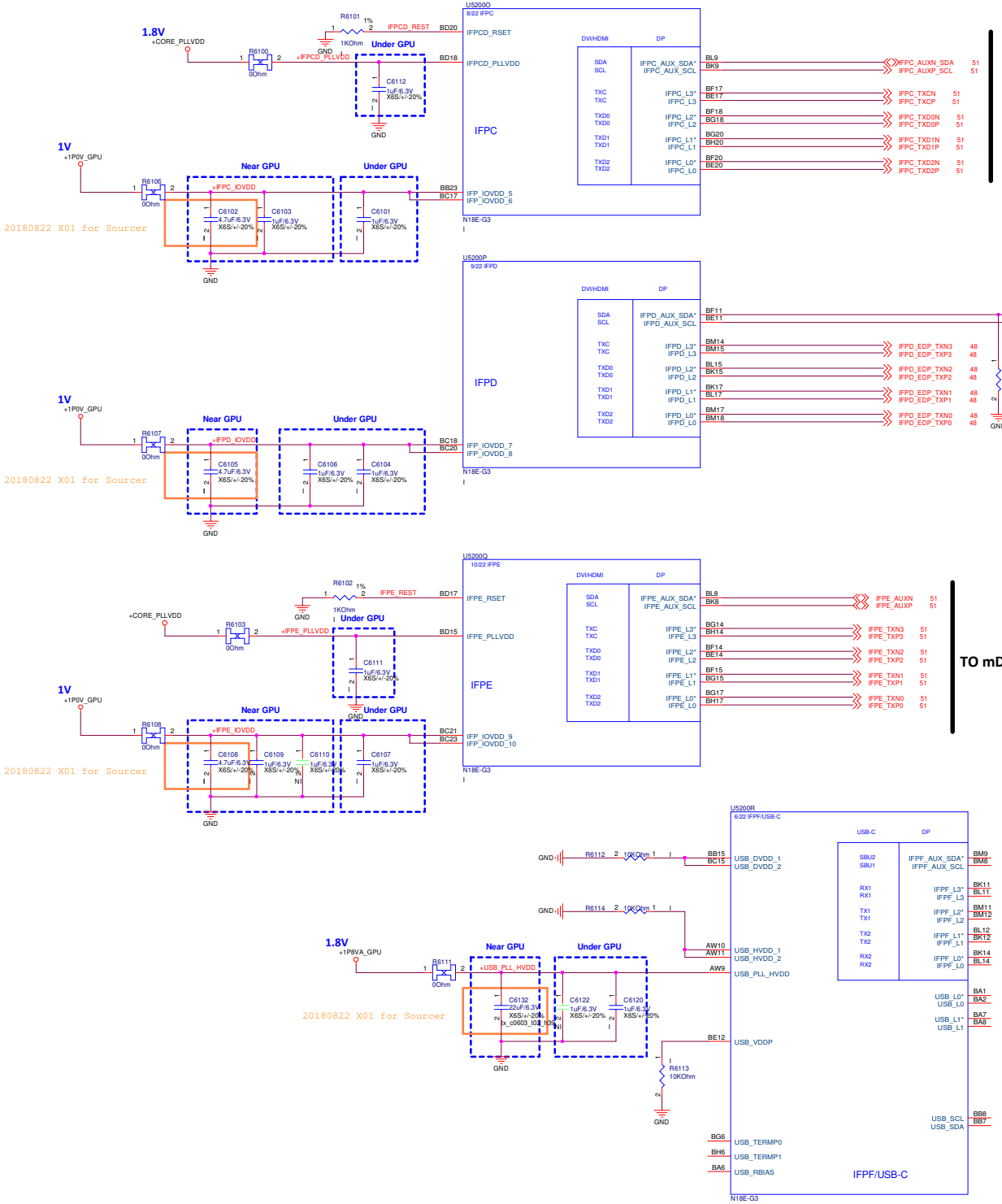


Table 9.6 HDMI Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA

Table 9.11 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

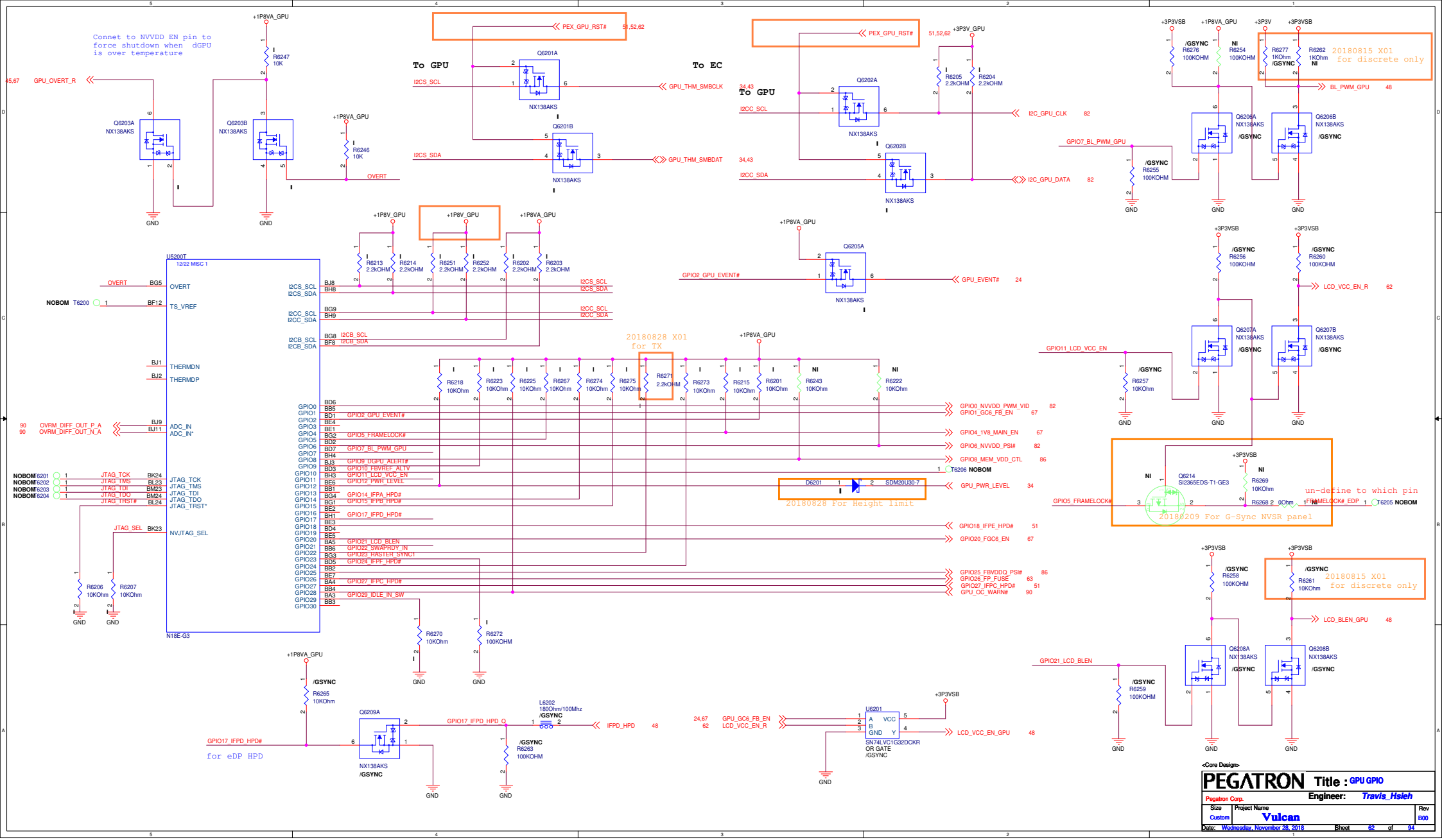
<Core Design>

PEGATRON Title : GPU mini DP/HDMI/MUX

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 61 of 94


Connet to NVVDD EN pin to force shutdown when dGPU is over temperature
To GPU
To EC
To GPU
20180828 X01 for TX
20180828 For Height limit
20180815 X01 for discrete only
20180209 For G-Sync NVSR panel
un-define to which pin
for eDP HPD
U5200T
12/22 MISC 1
N18E-G3
PEGATRON
Title : GPU GPIO
Engineer: Travis_Hsieh
Pegatron Corp.
Size: Custom
Project Name: Vulcan
Rev: B00
Date: Wednesday, November 28, 2018
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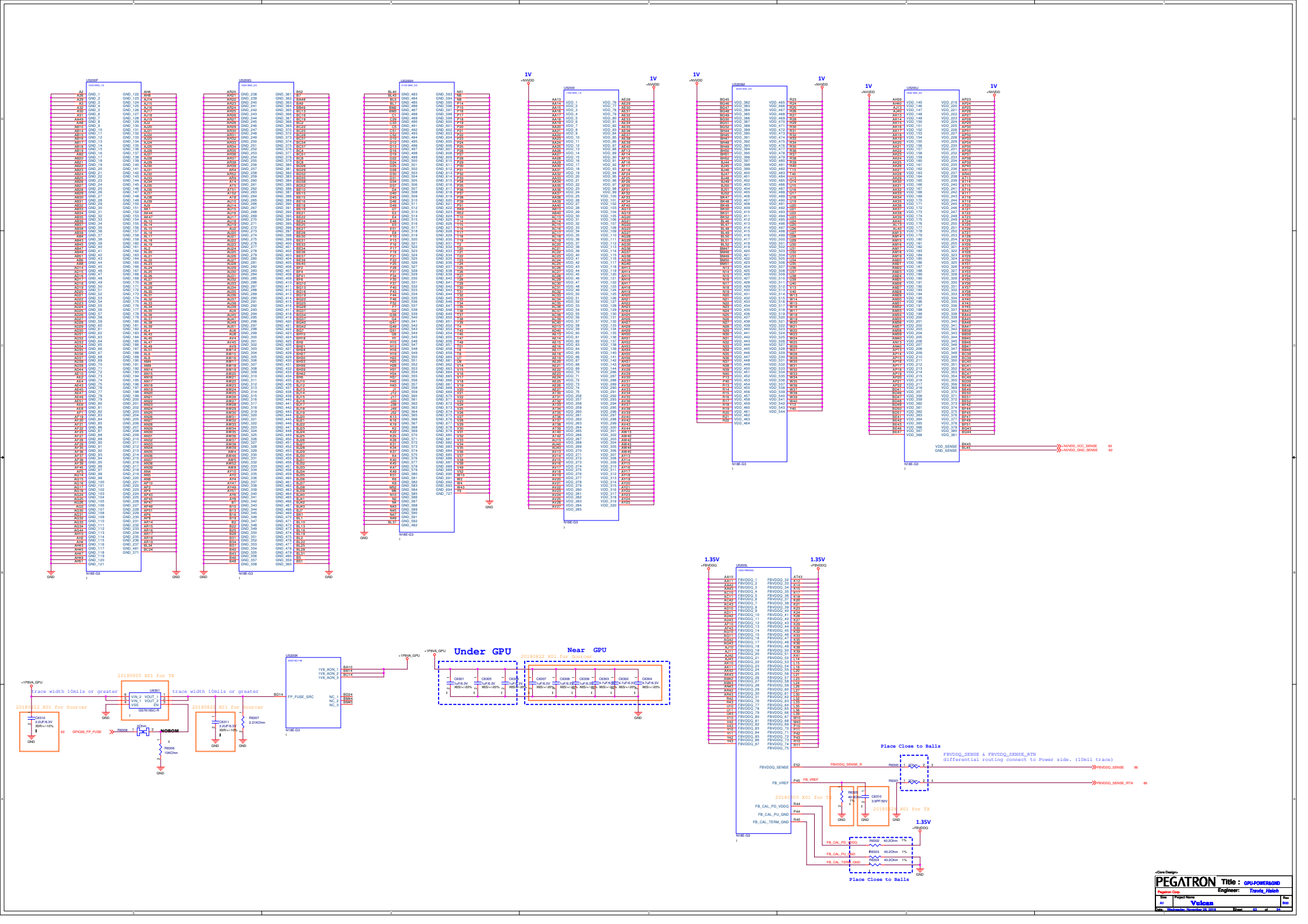

Under GPU
Near GPU
20180822 X01 for Sourcer
20180905 X01 for TX
trace width 10mils or greater
NOBOM
Place Close to Balls
FBVDDQ_SENSE & FBVDDQ_SENSE_RTN
differential routing connect to Power side. (10mil trace)
PEGATRON
Title : GPU-POWER&GND
Engineer: Travis_Haleh
Project Name: Vulcan
Rev: 0X6
Date: Wednesday, November 28, 2018
Sheet 83 of 94

+FBVDDQ

Under GPU

Partition A

C6413 1uF/6.3V X6S/+/-20%
C6414 1uF/6.3V X6S/+/-20%
C6415 1uF/6.3V X6S/+/-20%
C6416 1uF/6.3V X6S/+/-20%
C6417 1uF/6.3V X6S/+/-20%
C6418 1uF/6.3V X6S/+/-20%
C64237 10uF/6.3V X6S/+/-20%
C64238 10uF/6.3V X6S/+/-20%
GND

C6421 1uF/6.3V X6S/+/-20%
C6422 1uF/6.3V X6S/+/-20%
C6423 1uF/6.3V X6S/+/-20%
C6424 1uF/6.3V X6S/+/-20%
C6419 1uF/6.3V X6S/+/-20%
C6420 1uF/6.3V X6S/+/-20%
GND

Partition B

C6433 1uF/6.3V X6S/+/-20%
C6434 1uF/6.3V X6S/+/-20%
C6435 1uF/6.3V X6S/+/-20%
C6436 1uF/6.3V X6S/+/-20%
C6425 1uF/6.3V X6S/+/-20%
C6426 1uF/6.3V X6S/+/-20%
C64267 10uF/6.3V X6S/+/-20%
C64268 10uF/6.3V X6S/+/-20%
GND

C6429 1uF/6.3V X6S/+/-20%
C6430 1uF/6.3V X6S/+/-20%
C6432 1uF/6.3V X6S/+/-20%
C6431 1uF/6.3V X6S/+/-20%
C6427 1uF/6.3V X6S/+/-20%
C6428 1uF/6.3V X6S/+/-20%
GND

Partition C

C6445 1uF/6.3V X6S/+/-20%
C6446 1uF/6.3V X6S/+/-20%
C6447 1uF/6.3V X6S/+/-20%
C6448 1uF/6.3V X6S/+/-20%
C6437 1uF/6.3V X6S/+/-20%
C6438 1uF/6.3V X6S/+/-20%
C64269 10uF/6.3V X6S/+/-20%
C64270 10uF/6.3V X6S/+/-20%
GND

C6441 1uF/6.3V X6S/+/-20%
C6442 1uF/6.3V X6S/+/-20%
C6444 1uF/6.3V X6S/+/-20%
C6443 1uF/6.3V X6S/+/-20%
C6439 1uF/6.3V X6S/+/-20%
C6440 1uF/6.3V X6S/+/-20%
GND

Partition D

C6458 1uF/6.3V X6S/+/-20%
C6457 1uF/6.3V X6S/+/-20%
C6459 1uF/6.3V X6S/+/-20%
C6460 1uF/6.3V X6S/+/-20%
C6449 1uF/6.3V X6S/+/-20%
C6451 1uF/6.3V X6S/+/-20%
C64271 10uF/6.3V X6S/+/-20%
C64272 10uF/6.3V X6S/+/-20%
GND

C6453 1uF/6.3V X6S/+/-20%
C6455 1uF/6.3V X6S/+/-20%
C6456 1uF/6.3V X6S/+/-20%
C6454 1uF/6.3V X6S/+/-20%
C6450 1uF/6.3V X6S/+/-20%
C6452 1uF/6.3V X6S/+/-20%
GND

Near GPU

C64243 10uF/6.3V X6S/+/-20%
C64244 10uF/6.3V X6S/+/-20%
C64245 10uF/6.3V X6S/+/-20%
C64246 10uF/6.3V X6S/+/-20%
GND

C64247 22uF/6.3V X6S/+/-20%
C64248 22uF/6.3V X6S/+/-20%
C64249 22uF/6.3V X6S/+/-20%
C64250 22uF/6.3V X6S/+/-20%
C64251 22uF/6.3V X6S/+/-20%
C64252 22uF/6.3V X6S/+/-20%
C64253 22uF/6.3V X6S/+/-20%
C64254 22uF/6.3V X6S/+/-20%
C64255 22uF/6.3V X6S/+/-20%
GND

Close to GDDR

+FBVDDQ
ESR=6mOhm/Irms=3.5A
NI CE6400 330UF/2V
H2
ESR=6mOhm/Irms=3.5A
NI CE6401 330UF/2V
GND

+NVVDD

Near GPU

+NVVDD
ELU_T=1000hrs_105c/+/-20%
CE6403 470UF/2V
ELU_T=1000hrs_105c/+/-20%
CE6404 470UF/2V
ELU_T=1000hrs_105c/+/-20%
CE6405 470UF/2V
GND

Under GPU

C6401 47UF/4V X6S/+/-20%
C6402 47UF/4V X6S/+/-20%
C6461 47UF/4V X6S/+/-20%
tx_c0805_t02_h57x
GND

C64239 22UF/4V X6S/+/-20%
C64240 22UF/4V X6S/+/-20%
C64241 22UF/4V X6S/+/-20%
C64242 22UF/4V X6S/+/-20%
tx_c0805_t02_h55x
GND

Under GPU

C64256 10uF/6.3V X6S/+/-20%
C64257 10uF/6.3V X6S/+/-20%
C64258 10uF/6.3V X6S/+/-20%
C64259 10uF/6.3V X6S/+/-20%
C64260 10uF/6.3V X6S/+/-20%
C64261 10uF/6.3V X6S/+/-20%
C64262 10uF/6.3V X6S/+/-20%
C64263 10uF/6.3V X6S/+/-20%
C64264 10uF/6.3V X6S/+/-20%
C64265 10uF/6.3V X6S/+/-20%
C64266 10uF/6.3V X6S/+/-20%
C64280 10uF/6.3V X6S/+/-20%
C64281 10uF/6.3V X6S/+/-20%
C64282 10uF/6.3V X6S/+/-20%
C64283 10uF/6.3V X6S/+/-20%
C64273 10uF/6.3V X6S/+/-20%
C64274 10uF/6.3V X6S/+/-20%
C64275 10uF/6.3V X6S/+/-20%
C64276 10uF/6.3V X6S/+/-20%
C64277 10uF/6.3V X6S/+/-20%
C64278 10uF/6.3V X6S/+/-20%
C64279 10uF/6.3V X6S/+/-20%
C64284 10uF/6.3V X6S/+/-20%
GND

C6475 1uF/6.3V X6S/+/-20%
C6474 1uF/6.3V X6S/+/-20%
C6491 1uF/6.3V X6S/+/-20%
C6488 1uF/6.3V X6S/+/-20%
C6494 1uF/6.3V X6S/+/-20%
C6493 1uF/6.3V X6S/+/-20%
C6465 1uF/6.3V X6S/+/-20%
C64101 1uF/6.3V X6S/+/-20%
C64102 1uF/6.3V X6S/+/-20%
C6497 1uF/6.3V X6S/+/-20%
C64205 1uF/6.3V X6S/+/-20%
C64206 1uF/6.3V X6S/+/-20%
C64197 1uF/6.3V X6S/+/-20%
C64179 1uF/6.3V X6S/+/-20%
C64219 1uF/6.3V X6S/+/-20%
C64216 1uF/6.3V X6S/+/-20%
C64221 1uF/6.3V X6S/+/-20%
C64155 1uF/6.3V X6S/+/-20%
C64220 1uF/6.3V X6S/+/-20%
C64228 1uF/6.3V X6S/+/-20%
GND

C64131 1uF/6.3V X6S/+/-20%
C64128 1uF/6.3V X6S/+/-20%
C64113 1uF/6.3V X6S/+/-20%
C6476 1uF/6.3V X6S/+/-20%
C6485 1uF/6.3V X6S/+/-20%
C6498 1uF/6.3V X6S/+/-20%
C6482 1uF/6.3V X6S/+/-20%
C6477 1uF/6.3V X6S/+/-20%
C64193 1uF/6.3V X6S/+/-20%
C64207 1uF/6.3V X6S/+/-20%
C64195 1uF/6.3V X6S/+/-20%
C64194 1uF/6.3V X6S/+/-20%
C64227 1uF/6.3V X6S/+/-20%
C6495 1uF/6.3V X6S/+/-20%
C64236 1uF/6.3V X6S/+/-20%
C64202 1uF/6.3V X6S/+/-20%
C64217 1uF/6.3V X6S/+/-20%
C64203 1uF/6.3V X6S/+/-20%
C64204 1uF/6.3V X6S/+/-20%
C64192 1uF/6.3V X6S/+/-20%
GND

C6489 1uF/6.3V X6S/+/-20%
C6467 1uF/6.3V X6S/+/-20%
C64211 1uF/6.3V X6S/+/-20%
C64198 1uF/6.3V X6S/+/-20%
C64156 1uF/6.3V X6S/+/-20%
C64225 1uF/6.3V X6S/+/-20%
C64212 1uF/6.3V X6S/+/-20%
C64232 1uF/6.3V X6S/+/-20%
C64229 1uF/6.3V X6S/+/-20%
C6405 1uF/6.3V X6S/+/-20%
C6406 1uF/6.3V X6S/+/-20%
C6407 1uF/6.3V X6S/+/-20%
C6472 1uF/6.3V X6S/+/-20%
C6480 1uF/6.3V X6S/+/-20%
C6473 1uF/6.3V X6S/+/-20%
C6464 1uF/6.3V X6S/+/-20%
C6478 1uF/6.3V X6S/+/-20%
C64107 1uF/6.3V X6S/+/-20%
C64109 1uF/6.3V X6S/+/-20%
C64117 1uF/6.3V X6S/+/-20%
GND

C6470 1uF/6.3V X6S/+/-20%
C6463 1uF/6.3V X6S/+/-20%
C6481 1uF/6.3V X6S/+/-20%
C64124 1uF/6.3V X6S/+/-20%
C64123 1uF/6.3V X6S/+/-20%
C64119 1uF/6.3V X6S/+/-20%
C64118 1uF/6.3V X6S/+/-20%
C64116 1uF/6.3V X6S/+/-20%
C64121 1uF/6.3V X6S/+/-20%
C64147 1uF/6.3V X6S/+/-20%
C64135 1uF/6.3V X6S/+/-20%
C64134 1uF/6.3V X6S/+/-20%
C64151 1uF/6.3V X6S/+/-20%
C64150 1uF/6.3V X6S/+/-20%
C64148 1uF/6.3V X6S/+/-20%
C64169 1uF/6.3V X6S/+/-20%
C64170 1uF/6.3V X6S/+/-20%
C64167 1uF/6.3V X6S/+/-20%
C64143 1uF/6.3V X6S/+/-20%
C64165 1uF/6.3V X6S/+/-20%
GND

C64158 1uF/6.3V X6S/+/-20%
C64141 1uF/6.3V X6S/+/-20%
C64161 1uF/6.3V X6S/+/-20%
C64182 1uF/6.3V X6S/+/-20%
C64183 1uF/6.3V X6S/+/-20%
C64185 1uF/6.3V X6S/+/-20%
C64172 1uF/6.3V X6S/+/-20%
C64174 1uF/6.3V X6S/+/-20%
C64175 1uF/6.3V X6S/+/-20%
C64214 1uF/6.3V X6S/+/-20%
C64230 1uF/6.3V X6S/+/-20%
C64188 1uF/6.3V X6S/+/-20%
C64137 1uF/6.3V X6S/+/-20%
C64209 1uF/6.3V X6S/+/-20%
C64122 1uF/6.3V X6S/+/-20%
C6499 1uF/6.3V X6S/+/-20%
C64108 1uF/6.3V X6S/+/-20%
C6490 1uF/6.3V X6S/+/-20%
C6469 1uF/6.3V X6S/+/-20%
C6403 1uF/6.3V X6S/+/-20%
GND

C64149 1uF/6.3V X6S/+/-20%
C64210 1uF/6.3V X6S/+/-20%
C64200 1uF/6.3V X6S/+/-20%
C64208 1uF/6.3V X6S/+/-20%
C64132 1uF/6.3V X6S/+/-20%
C64130 1uF/6.3V X6S/+/-20%
C64120 1uF/6.3V X6S/+/-20%
C64140 1uF/6.3V X6S/+/-20%
C6409 1uF/6.3V X6S/+/-20%
C64133 1uF/6.3V X6S/+/-20%
C64145 1uF/6.3V X6S/+/-20%
C6404 1uF/6.3V X6S/+/-20%
C64139 1uF/6.3V X6S/+/-20%
C64138 1uF/6.3V X6S/+/-20%
C64136 1uF/6.3V X6S/+/-20%
C64144 1uF/6.3V X6S/+/-20%
C64146 1uF/6.3V X6S/+/-20%
C64201 1uF/6.3V X6S/+/-20%
C64142 1uF/6.3V X6S/+/-20%
C6487 1uF/6.3V X6S/+/-20%
GND

C6412 1uF/6.3V X6S/+/-20%
C64168 1uF/6.3V X6S/+/-20%
C6479 1uF/6.3V X6S/+/-20%
C64154 1uF/6.3V X6S/+/-20%
C64152 1uF/6.3V X6S/+/-20%
C64171 1uF/6.3V X6S/+/-20%
C6408 1uF/6.3V X6S/+/-20%
C64160 1uF/6.3V X6S/+/-20%
C64114 1uF/6.3V X6S/+/-20%
C64153 1uF/6.3V X6S/+/-20%
C64112 1uF/6.3V X6S/+/-20%
C64163 1uF/6.3V X6S/+/-20%
C64159 1uF/6.3V X6S/+/-20%
C64196 1uF/6.3V X6S/+/-20%
C6462 1uF/6.3V X6S/+/-20%
C64164 1uF/6.3V X6S/+/-20%
C64166 1uF/6.3V X6S/+/-20%
C6486 1uF/6.3V X6S/+/-20%
C64162 1uF/6.3V X6S/+/-20%
C64157 1uF/6.3V X6S/+/-20%
GND

C64100 1uF/6.3V X6S/+/-20%
C64186 1uF/6.3V X6S/+/-20%
C6484 1uF/6.3V X6S/+/-20%
C6483 1uF/6.3V X6S/+/-20%
C64173 1uF/6.3V X6S/+/-20%
C64191 1uF/6.3V X6S/+/-20%
C64190 1uF/6.3V X6S/+/-20%
C64180 1uF/6.3V X6S/+/-20%
C64189 1uF/6.3V X6S/+/-20%
C64129 1uF/6.3V X6S/+/-20%
C64127 1uF/6.3V X6S/+/-20%
C64115 1uF/6.3V X6S/+/-20%
C64199 1uF/6.3V X6S/+/-20%
C64178 1uF/6.3V X6S/+/-20%
C64176 1uF/6.3V X6S/+/-20%
C64184 1uF/6.3V X6S/+/-20%
C64187 1uF/6.3V X6S/+/-20%
C6466 1uF/6.3V X6S/+/-20%
C64181 1uF/6.3V X6S/+/-20%
C6468 1uF/6.3V X6S/+/-20%
GND

C64104 1uF/6.3V X6S/+/-20%
C64103 1uF/6.3V X6S/+/-20%
C64215 1uF/6.3V X6S/+/-20%
C6492 1uF/6.3V X6S/+/-20%
C64111 1uF/6.3V X6S/+/-20%
C64231 1uF/6.3V X6S/+/-20%
C64125 1uF/6.3V X6S/+/-20%
C64126 1uF/6.3V X6S/+/-20%
C64110 1uF/6.3V X6S/+/-20%
C64213 1uF/6.3V X6S/+/-20%
C64177 1uF/6.3V X6S/+/-20%
C64224 1uF/6.3V X6S/+/-20%
C6496 1uF/6.3V X6S/+/-20%
C64218 1uF/6.3V X6S/+/-20%
C64105 1uF/6.3V X6S/+/-20%
C64223 1uF/6.3V X6S/+/-20%
C64226 1uF/6.3V X6S/+/-20%
C64106 1uF/6.3V X6S/+/-20%
C64222 1uF/6.3V X6S/+/-20%
C6471 1uF/6.3V X6S/+/-20%
GND

Under GPU

C64235 1uF/6.3V X6S/+/-20%
C6410 1uF/6.3V X6S/+/-20%
C64234 1uF/6.3V X6S/+/-20%
C64233 1uF/6.3V X6S/+/-20%
C6411 1uF/6.3V X6S/+/-20%
GND

20180831 X01 for EMC

+FBVDDQ
C64285 1 2 0.1UF/25V X5R/+/-10%
+NVVDD
C64286 1 2 0.1UF/25V X5R/+/-10%

20180830 X01 for EMC close to H4745

+FBVDDQ_VIN
C64287 0.1UF/25V X5R/+/-10%
GND

<Core Design>

PEGATRON Title : GPU-Decoupling
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 64 of 94

PEGATRON Title : TYPE-C_PD

Pegatron Corp. Engineer: Travis_Hsieh

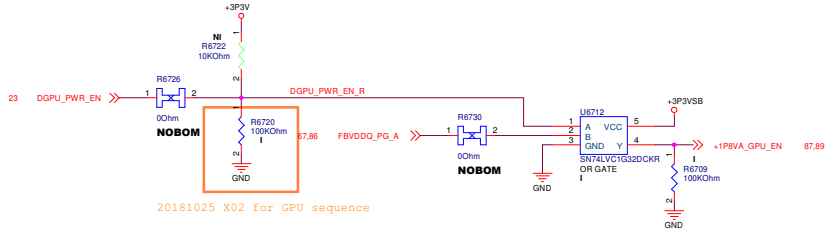
Size	Project Name	Rev
C	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 65 of 94

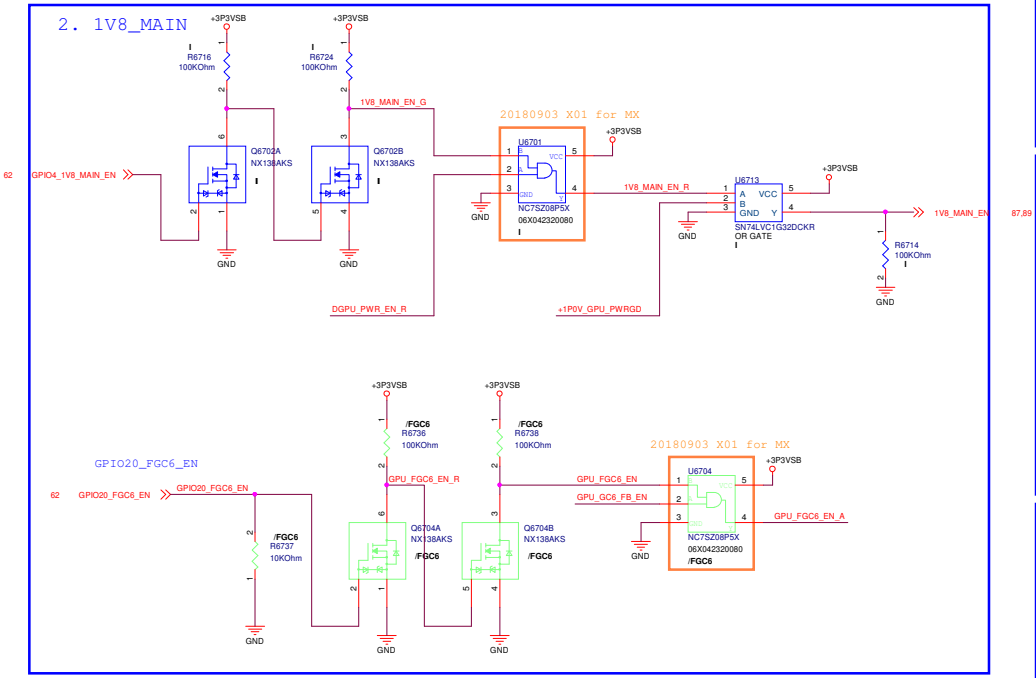
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Type-C MUX	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: 800
Date: Wednesday, November 28, 2018	Sheet 68 of 94	

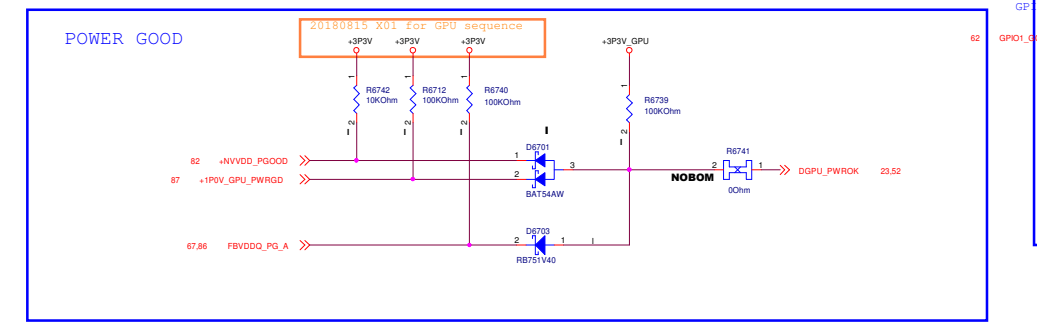
1.1V8_AON



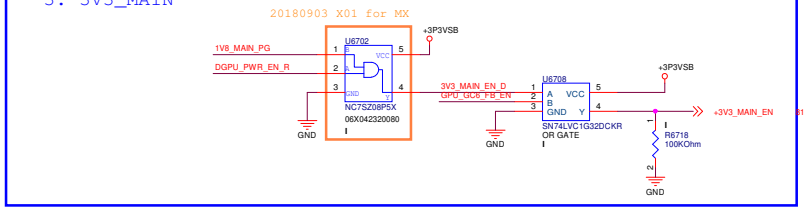
2. 1V8_MAIN



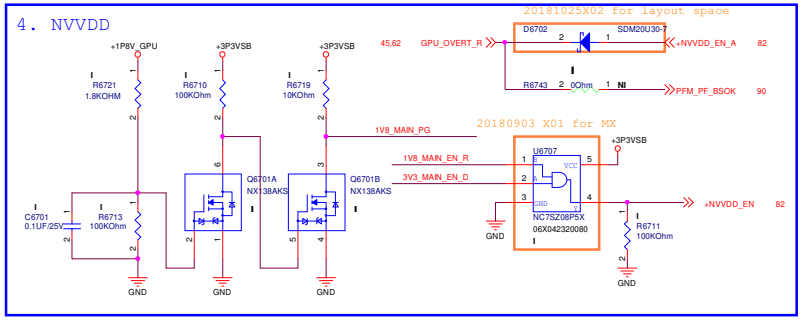
POWER GOOD



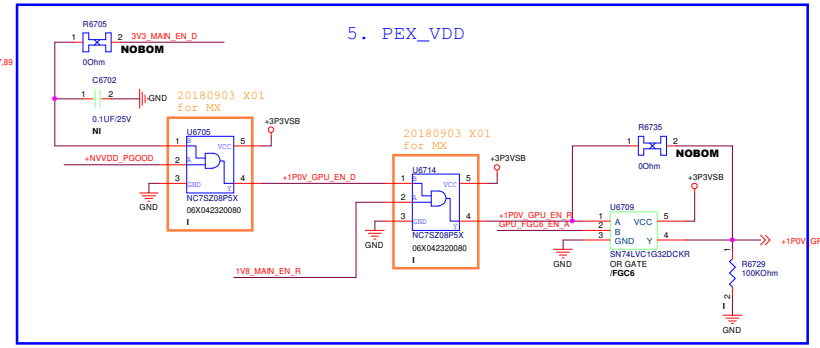
3. 3V3_MAIN



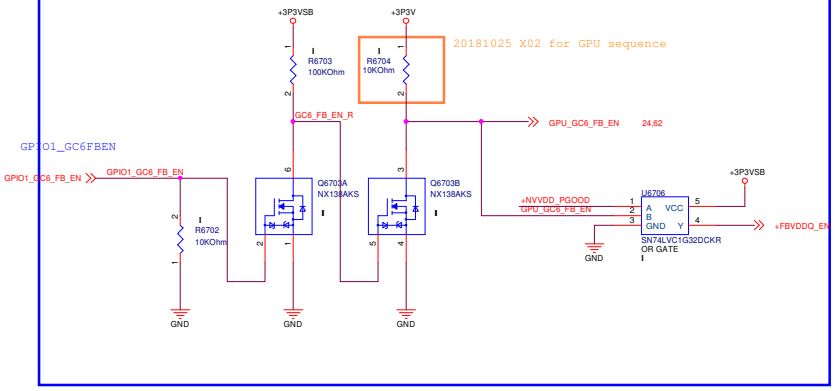
4. NVVDD



5. PEX_VDD



6. FBVDDQ



<Core Design>

PEGATRON Title : GPU_POWER Sequence

Pegatron Corp. Engineer: Travis_Hsieh

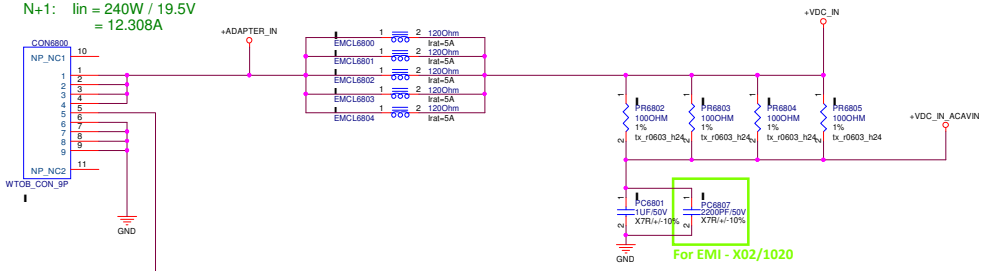
Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 67 of 94

DC-IN connector

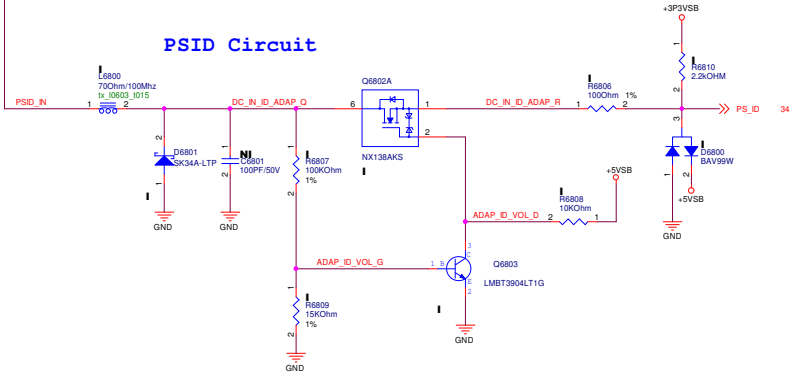
N : Iin = 180W / 19.5V
= 9.231A

N+1: Iin = 240W / 19.5V
= 12.308A



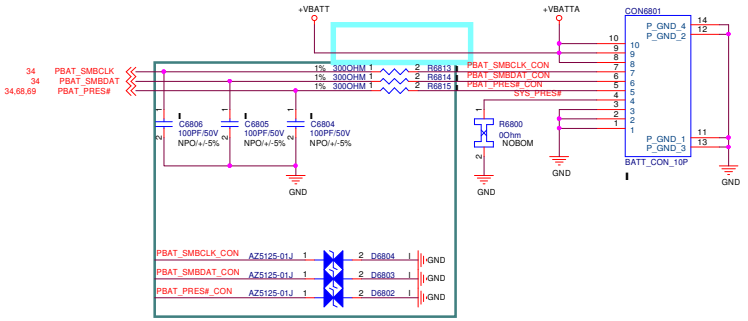
For EMI - X02/1020

PSID Circuit



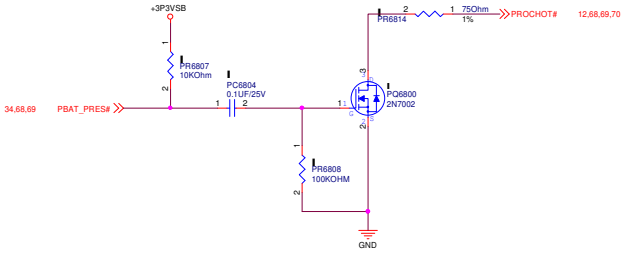
Remove JP6800 and JP6801

Battery Pack connector

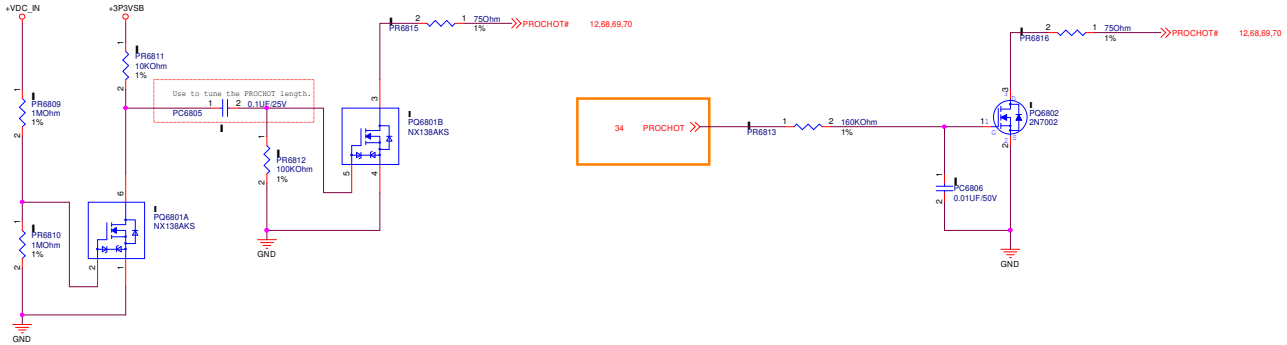


For Battery damage EC issue - X01/0824

Adapter Protection Circuit



Battery Protection Circuit



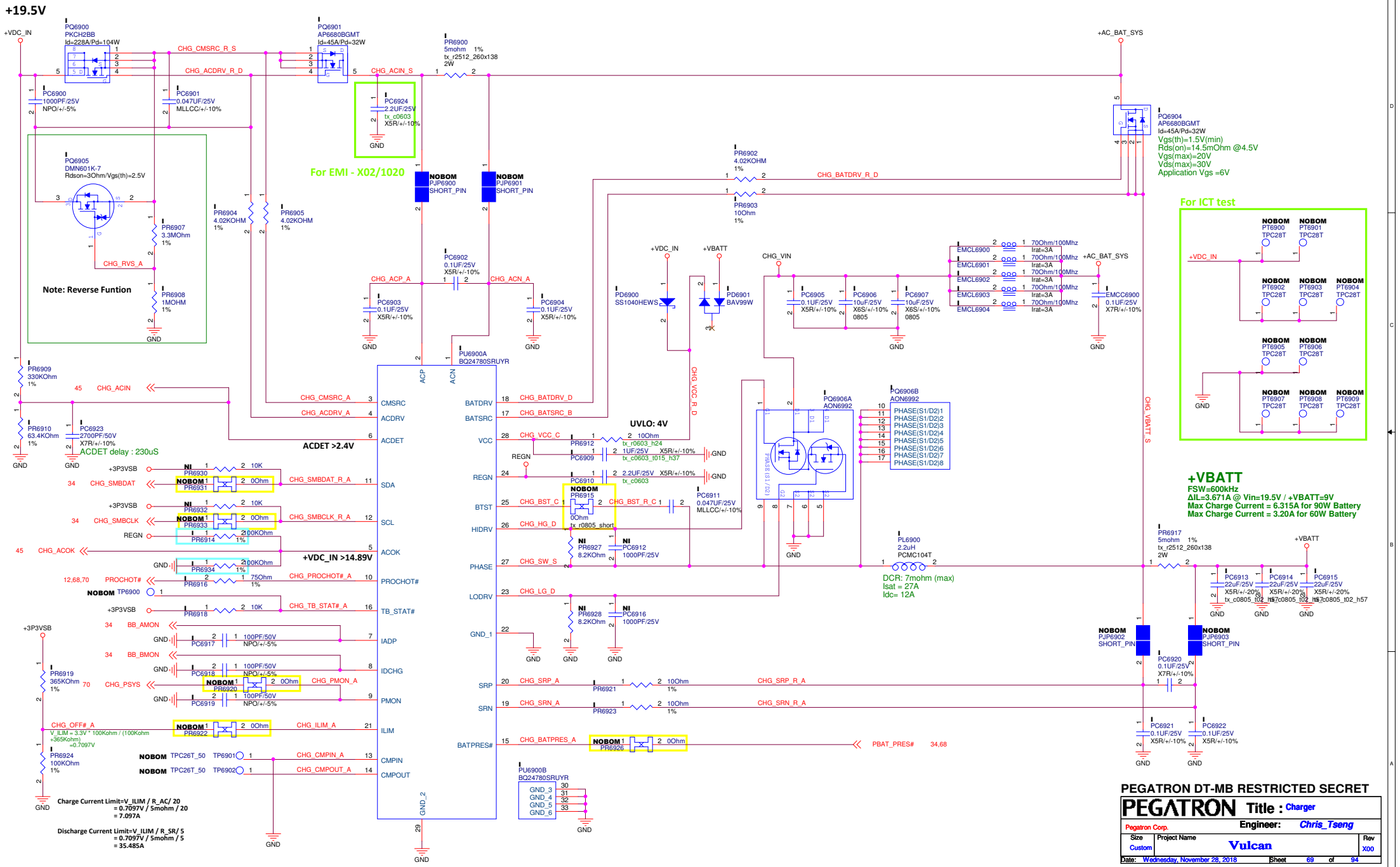
<Core Design>

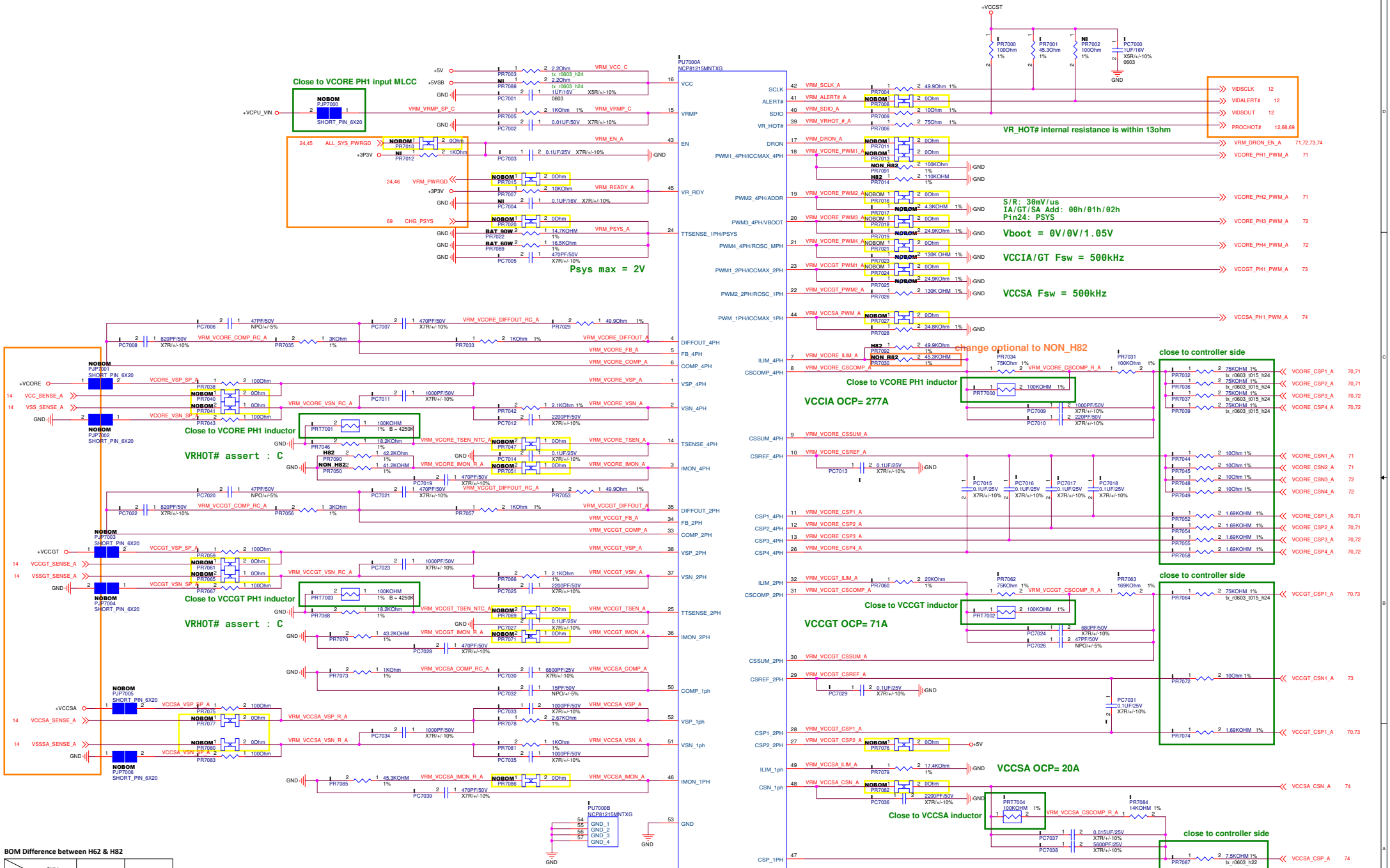
PEGATRON Title : DC_IN

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 68 of 94


+19.5V
+VDC_IN
+AC_BAT_SYS
PQ6900 PKCH2BB Id=228A/Pd=104W
PQ6901 AP6680BGMT Id=45A/Pd=32W
PR6900 5mohm 1% tx_r2512_260x138 2W
CHG_CMSRC_R_S
CHG_ACDRV_R_D
CHG_ACIN_S
PC6900 1000PF/25V NPO/+/-5%
PC6901 0.047UF/25V MLLCC/+/-10%
PC6924 2.2UF/25V tx_c0603 X5R/+/-10%
For EMI - X02/1020
NOBOM PJP6900 SHORT_PIN
NOBOM PJP6901 SHORT_PIN
PQ6904 AP6680BGMT Id=45A/Pd=32W
Vgs(th)=1.5V(min)
Rds(on)=14.5mOhm @4.5V
Vgs(max)=20V
Vds(max)=30V
Application Vgs =6V
PR6902 4.02KOHM 1%
PR6903 10Ohm 1%
CHG_BATDRV_R_D
For ICT test
PQ6905 DMN601K-7 Rdson=3Ohm/Vgs(th)=2.5V
Note: Reverse Funtion
PR6907 3.3MOhm 1%
PR6908 1MOHM 1%
CHG_RVS_A
PR6904 4.02KOHM 1%
PR6905 4.02KOHM 1%
PC6902 0.1UF/25V X5R/+/-10%
CHG_ACP_A
CHG_ACN_A
PC6903 0.1UF/25V X5R/+/-10%
PC6904 0.1UF/25V X5R/+/-10%
PU6900A BQ24780SRUYR
ACP
ACN
PD6900 SS1040HEWS
PD6901 BAV99W
+VBATT
CHG_VIN
PC6905 0.1UF/25V X5R/+/-10%
PC6906 10uF/25V X6S/+/-10% 0805
PC6907 10uF/25V X6S/+/-10% 0805
EMCL6900 EMCL6901 EMCL6902 EMCL6903 EMCL6904
70Ohm/100Mhz Irat=3A
EMCC6900 0.1UF/25V X7R/+/-10%
CHG_VCC_R_D
CHG_VBATT_S
PR6909 330KOhm 1%
PR6910 63.4KOhm 1%
PC6923 2700PF/50V X7R/+/-10%
CHG_ACIN
ACDET delay : 230uS
ACDET >2.4V
UVLO: 4V
+VDC_IN >14.89V
CHG_CMSRC_A
CHG_ACDRV_A
CHG_SMBDAT
CHG_SMBCLK
CHG_ACOK
CHG_PROCHOT#_A
CHG_TB_STAT#_A
BB_AMON
BB_BMON
CHG_PSYS
CHG_PMON_A
CHG_OFF#_A
CHG_ILIM_A
CHG_CMPIN_A
CHG_CMPOUT_A
PROCHOT#
TB_STAT#
PBAT_PRES#
CMSRC
ACDRV
ACDET
SDA
SCL
ACOK
PROCHOT#
TB_STAT#
IADP
IDCHG
PMON
ILIM
CMPIN
CMPOUT
BATDRV
BATSRC
VCC
REGN
BTST
HIDRV
PHASE
LODRV
GND_1
SRP
SRN
BATPRES#
GND_2
CHG_BATDRV_D
CHG_BATSRC_B
CHG_VCC_C
CHG_BST_C
CHG_HG_D
CHG_SW_S
CHG_LG_D
CHG_SRP_A
CHG_SRN_A
CHG_BATPRES_A
PQ6906A AON6992
PQ6906B AON6992
PHASE(S1/D2)1
PHASE(S1/D2)2
PHASE(S1/D2)3
PHASE(S1/D2)4
PHASE(S1/D2)5
PHASE(S1/D2)6
PHASE(S1/D2)7
PHASE(S1/D2)8
PL6900 2.2uH PCMC104T
DCR: 7mohm (max)
Isat = 27A
Idc= 12A
+VBATT
FSW=600kHz
ΔIL=3.671A @ Vin=19.5V / +VBATT=9V
Max Charge Current = 6.315A for 90W Battery
Max Charge Current = 3.20A for 60W Battery
PR6917 5mohm 1% tx_r2512_260x138 2W
PC6913 22uF/25V X5R/+/-20% tx_c0805_t02_h57
PC6914 22uF/25V X5R/+/-20% tx_c0805_t02_h57
PC6915 22uF/25V X5R/+/-20% tx_c0805_t02_h57
NOBOM PJP6902 SHORT_PIN
NOBOM PJP6903 SHORT_PIN
PC6920 0.1UF/25V X7R/+/-10%
PC6921 0.1UF/25V X5R/+/-10%
PC6922 0.1UF/25V X5R/+/-10%
PR6919 365KOhm 1%
PR6924 100KOhm 1%
Charge Current Limit=V_ILIM / R_AC/ 20
= 0.7097V / 5mohm / 20
= 7.097A
Discharge Current Limit=V_ILIM / R_SR/ 5
= 0.7097V / 5mohm / 5
= 35.485A
PU6900B BQ24780SRUYR
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : Charger
Pegatron Corp.
Engineer: Chris_Tseng
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 69 of 94



BOM Difference between H62 & H82

SKU / Part Reference	H62	H82
PR7050 / PR7090	41.2KΩ	42.2KΩ
PR7014 / PR7091	110KΩ	100KΩ
PR7030 / PR7092	45.3KΩ (OCP = 252A)	49.9KΩ (OCP = 277A)

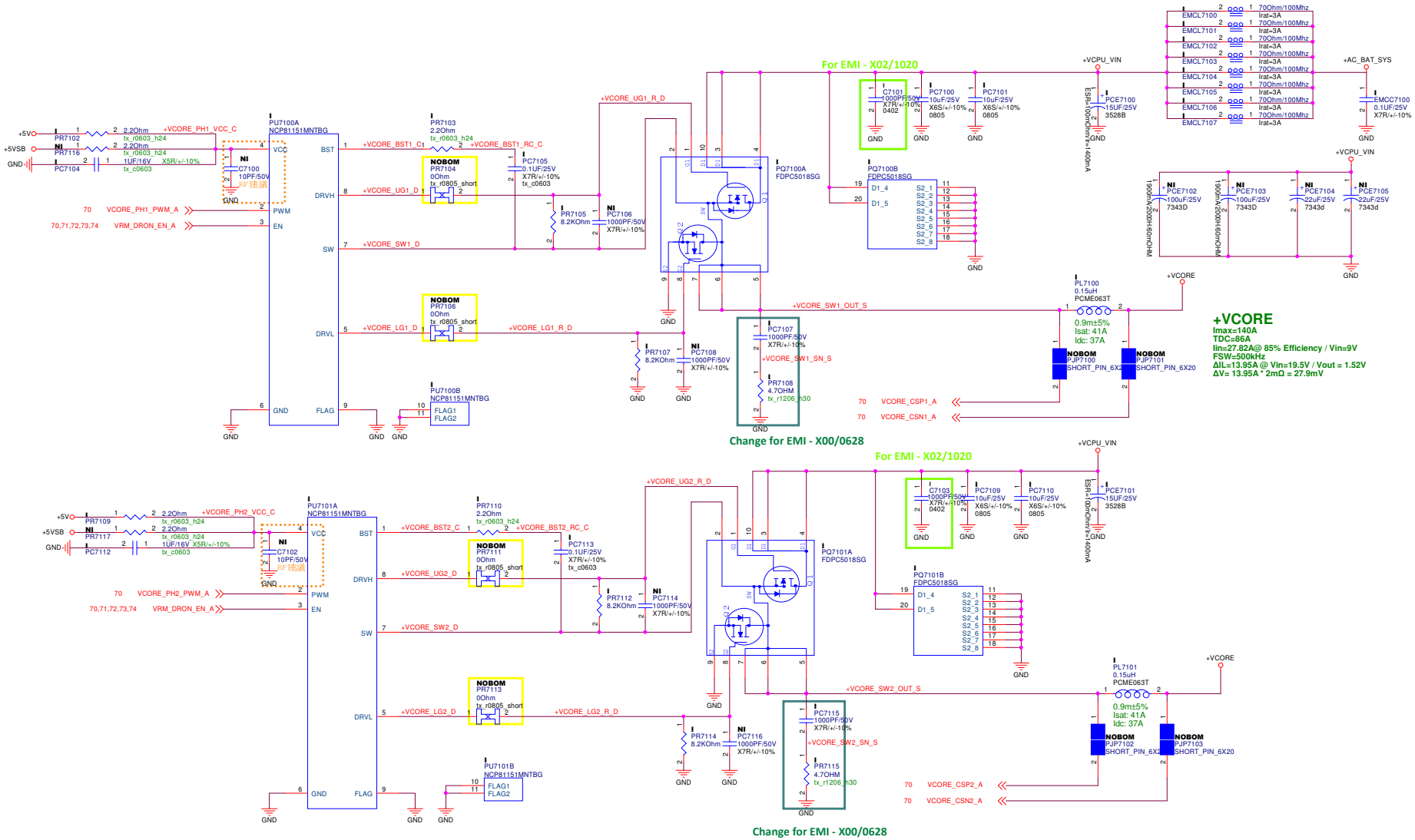
<Core Design>

PEGATRON Title : VR CONTROLLER

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 70 of 94



OWNER	+VCORE OC Point	Low Limit	High Limit
Atticus	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)
Terry	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)

I_Low Limit = I_DVID + Io_Cout
= 26A + (30mV/uS) * 1748uF
= 78.44A

※ Controller will shut down after 50uS when 184.99A ≤ Iout < 277.49A
Controller will shut down immediately when Iout trigger 277.49A

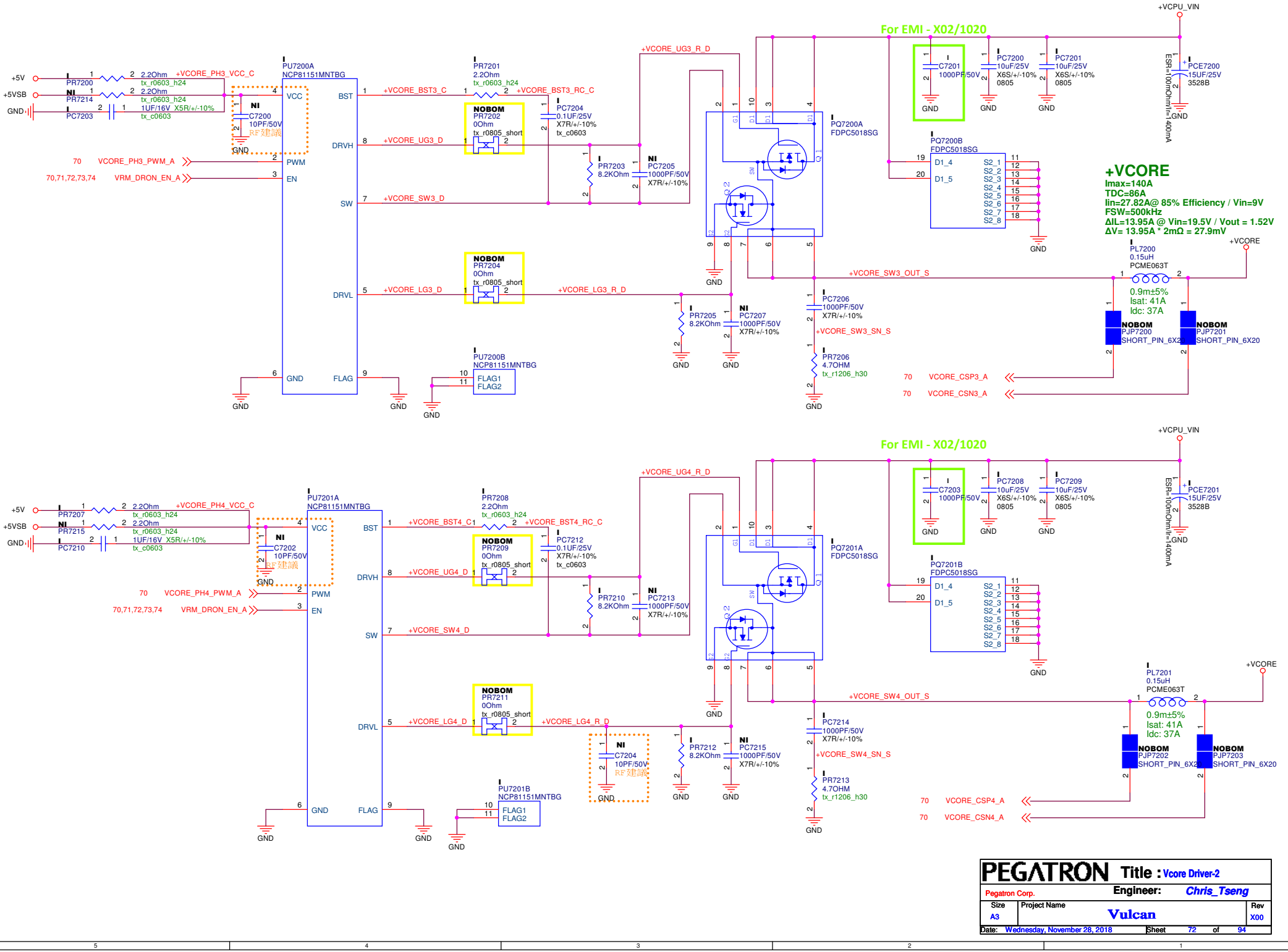
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Vcore Driver-1

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 71 of 94


For EMI - X02/1020
+VCPU_VIN
+VCORE
Imax=140A
TDC=86A
Iin=27.82A@ 85% Efficiency / Vin=9V
FSW=500kHz
ΔIL=13.95A @ Vin=19.5V / Vout = 1.52V
ΔV= 13.95A * 2mΩ = 27.9mV
PU7200A NCP81151MNTBG
PU7200B NCP81151MNTBG
PU7201A NCP81151MNTBG
PU7201B NCP81151MNTBG
PQ7200A FDPC5018SG
PQ7200B FDPC5018SG
PQ7201A FDPC5018SG
PQ7201B FDPC5018SG
PL7200 0.15uH PCME063T
PL7201 0.15uH PCME063T
0.9m±5%
Isat: 41A
Idc: 37A
+VCORE_PH3_VCC_C
+VCORE_BST3_C
+VCORE_BST3_RC_C
+VCORE_UG3_R_D
+VCORE_UG3_D
+VCORE_SW3_D
+VCORE_LG3_D
+VCORE_LG3_R_D
+VCORE_SW3_OUT_S
+VCORE_SW3_SN_S
VCORE_PH3_PWM_A
VRM_DRON_EN_A
VCORE_CSP3_A
VCORE_CSN3_A
+VCORE_PH4_VCC_C
+VCORE_BST4_C
+VCORE_BST4_RC_C
+VCORE_UG4_R_D
+VCORE_UG4_D
+VCORE_SW4_D
+VCORE_LG4_D
+VCORE_LG4_R_D
+VCORE_SW4_OUT_S
+VCORE_SW4_SN_S
VCORE_PH4_PWM_A
VRM_DRON_EN_A
VCORE_CSP4_A
VCORE_CSN4_A
NOBOM PJP7200 SHORT_PIN_6X20
NOBOM PJP7201 SHORT_PIN_6X20
NOBOM PJP7202 SHORT_PIN_6X20
NOBOM PJP7203 SHORT_PIN_6X20
RF建議
PEGATRON
Title : Vcore Driver-2
Pegatron Corp.
Engineer: Chris_Tseng
Size A3
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
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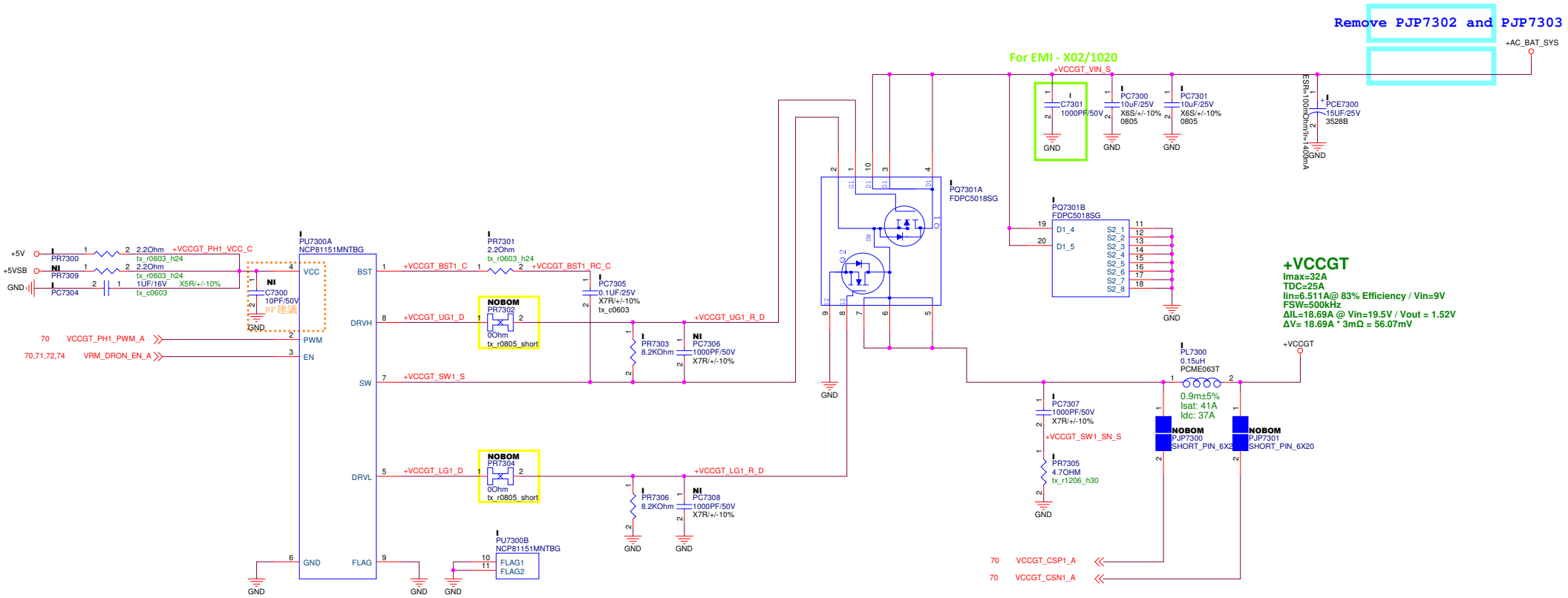


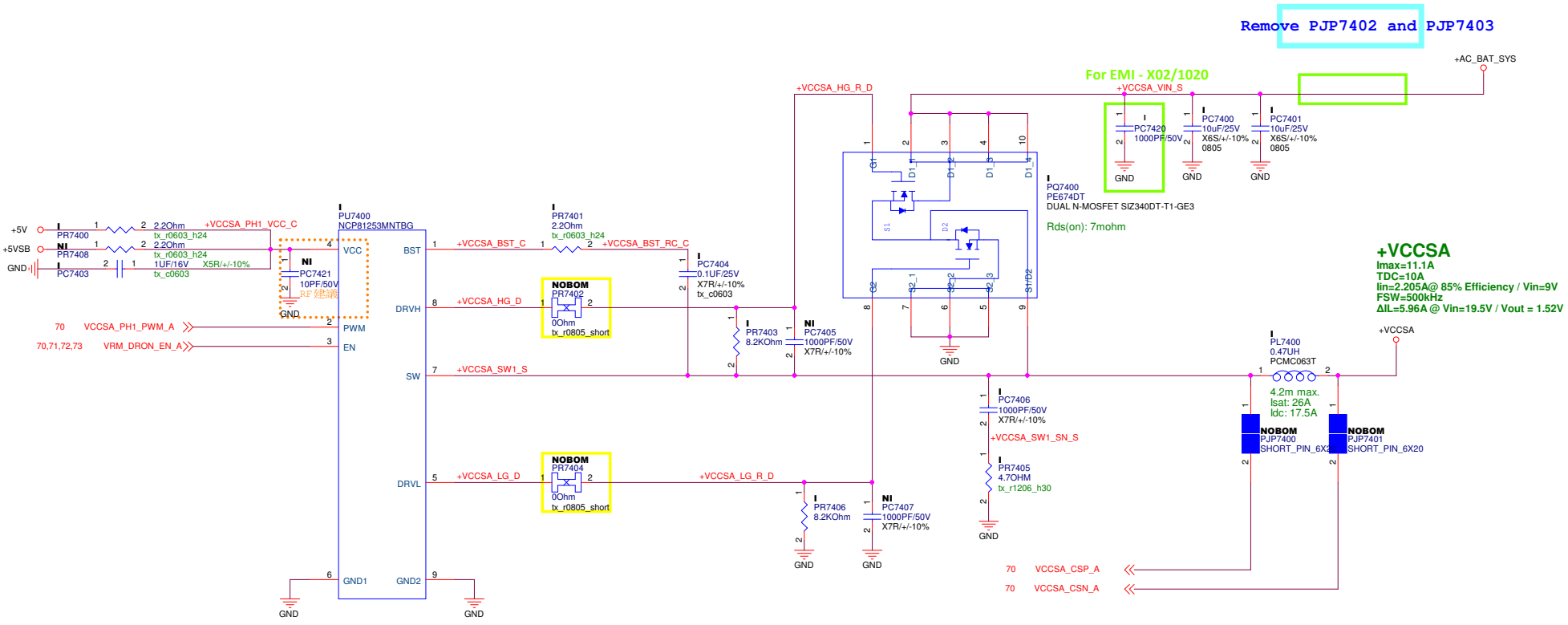
OWNER	+VCCGT OC Point	Low Limit	High Limit
Atticus	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A
Terry	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A

I_Low Limit = I_DVID + Io_Cout
= 8A + (30mV/uS) * 1156uF
= 42.68A

※ Controller will shut down after 50uS when 47.51A ≤ Iout < 71.27A
Controller will shut down immediately when Iout trigger 71.27A

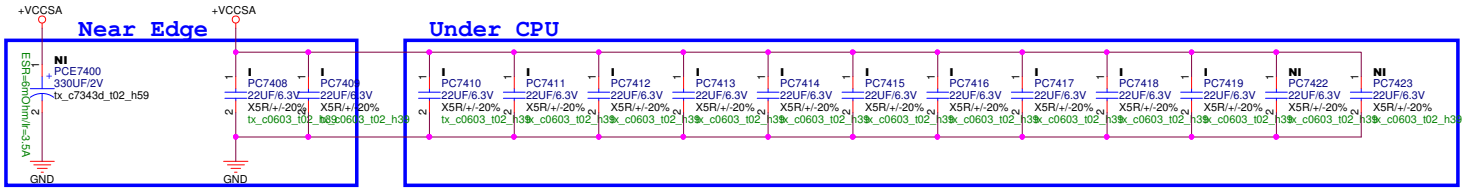
PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON Title : VccGT Driver
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 73 of 94



OWNER	+VCCSA OC Point	Low Limit	High Limit
Atticus	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A
Terry	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A

```
I_Low Limit = I_DVID + Io_Cout
            = 5A + (30mV/uS) * 265uF
            = 12.95A
```

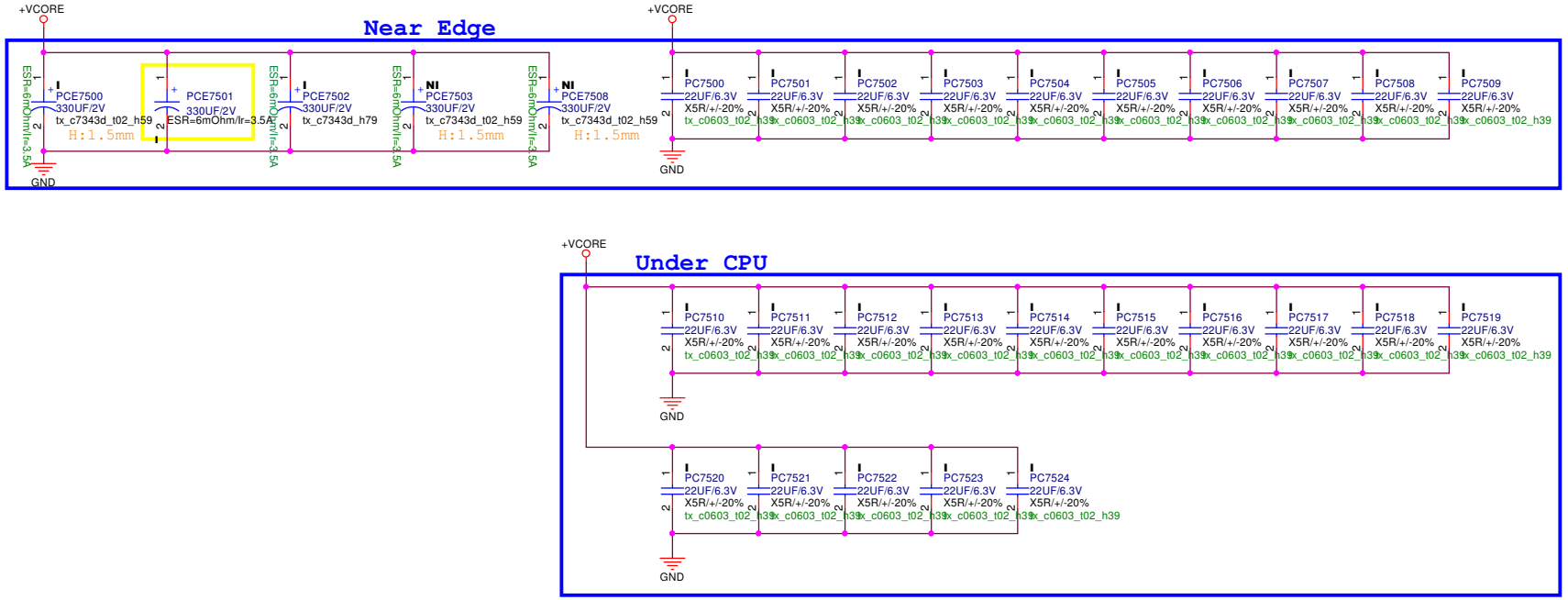


VCCSA Output CAP

330uF/2V/H=2mm * 1(NI)
22uF/6.3V * 12 (I)
22uF/6.3V * 2 (NI)

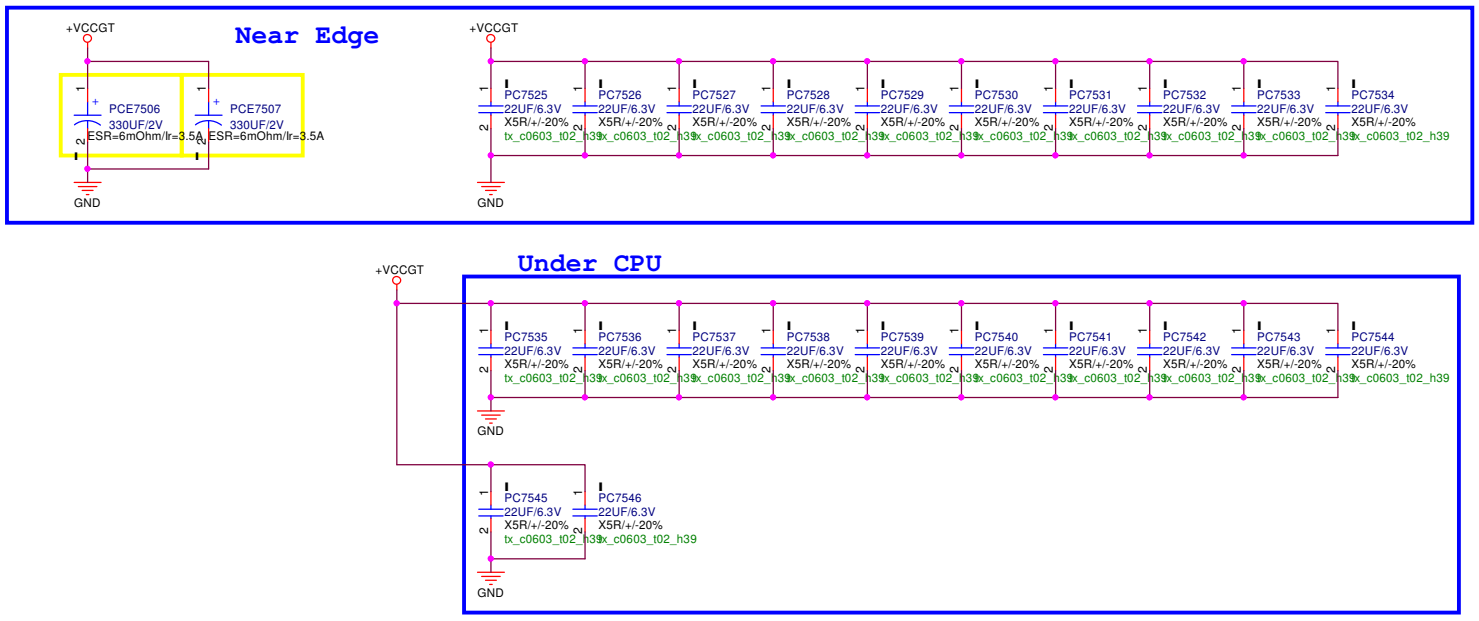
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VccSA Driver	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 74 of 94	



Vcore Output CAP

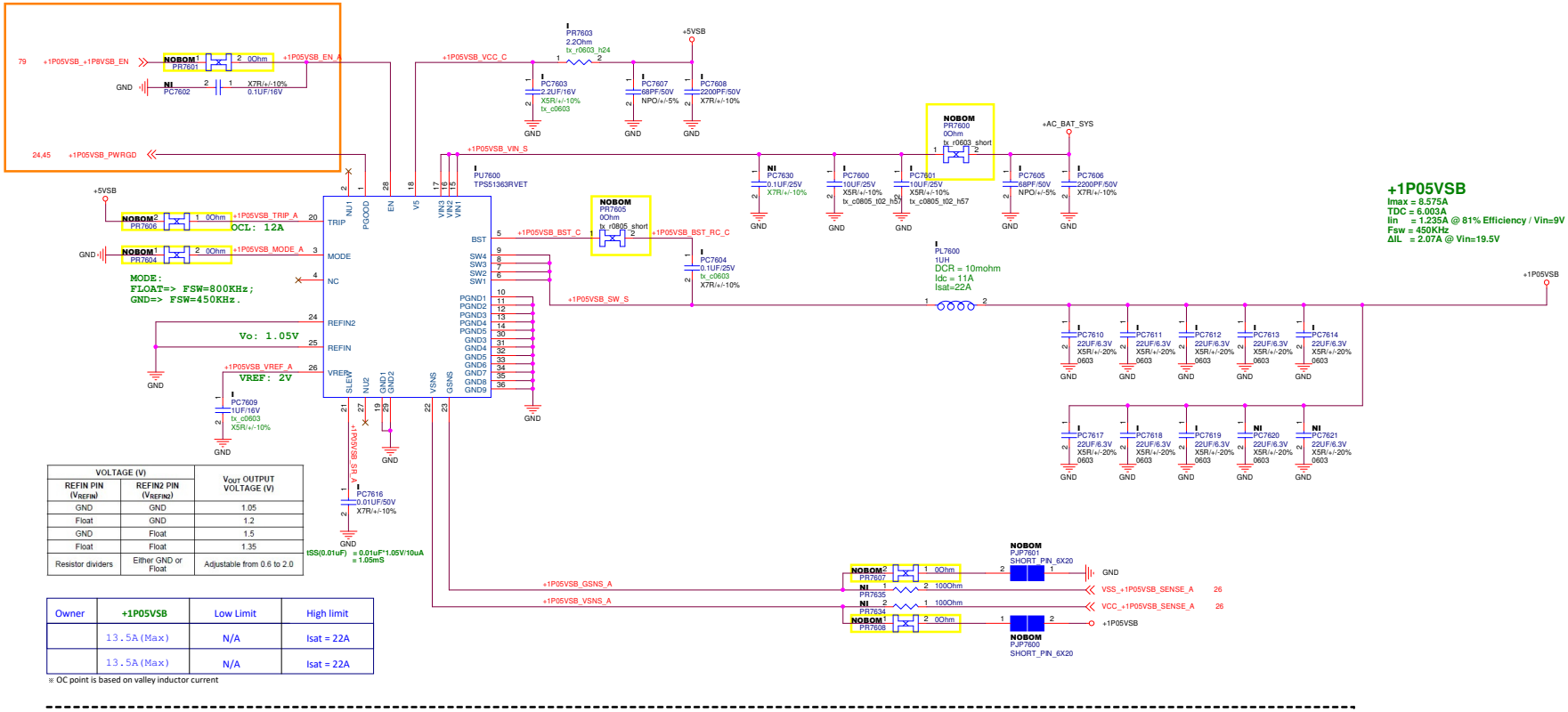
330uF/2V/H=2mm * 2 (I)
330uF/2V/H=1.5mm * 1(I)
330uF/2V/H=1.5mm * 2(NI)
22uF * 25



VCCGT Output CAP

330uF/2V/H=2mm * 2 (I)
22uF * 22

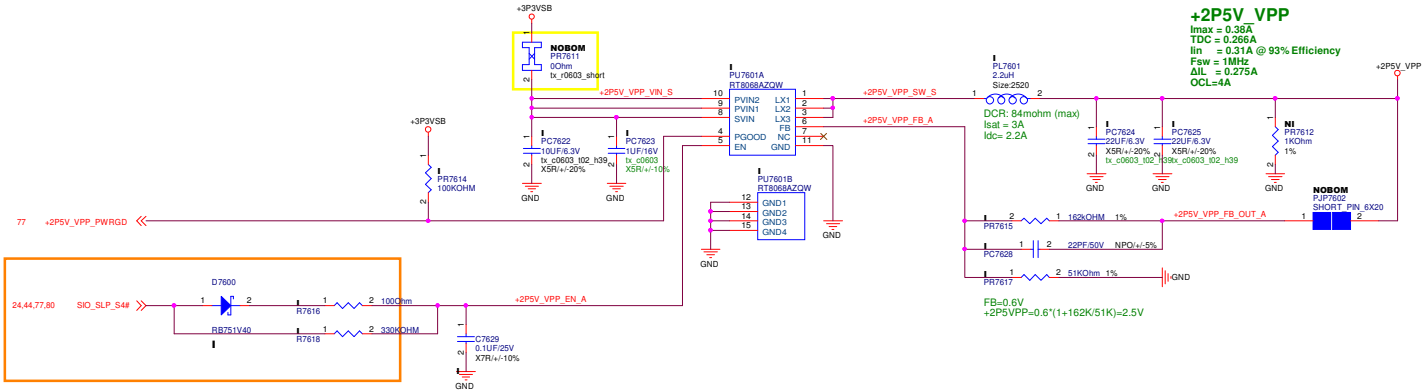
PEGATRON	Title :	Vcore & VccGT CAP
Pegatron Corp.	Engineer:	Chris_Tseng
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 75 of 94	



VOLTAGE (V)		V_{OUT} OUTPUT VOLTAGE (V)
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

Owner	+1P05VSB	Low Limit	High limit
	13.5A(Max)	N/A	Isat = 22A
	13.5A(Max)	N/A	Isat = 22A

※ OC point is based on valley inductor current



Owner	+2P5V_VPP	Low Limit	High limit
	4.0A	N/A	0.66uH @ 6A
	4.0A	N/A	0.66uH @ 6A

※ OC point is based on peak inductor current

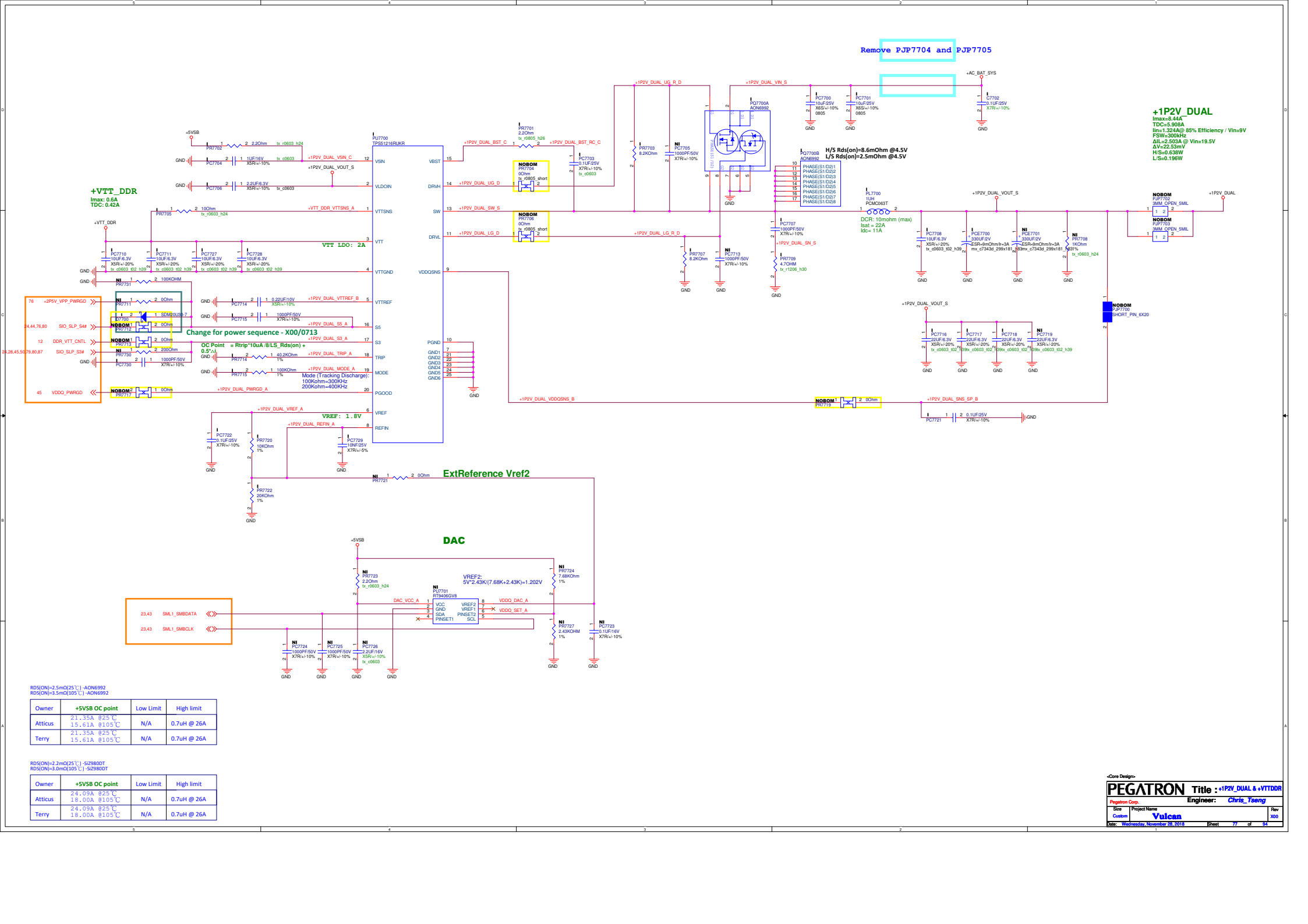
PEGATRON DT-MB RESTRICTED SECRET

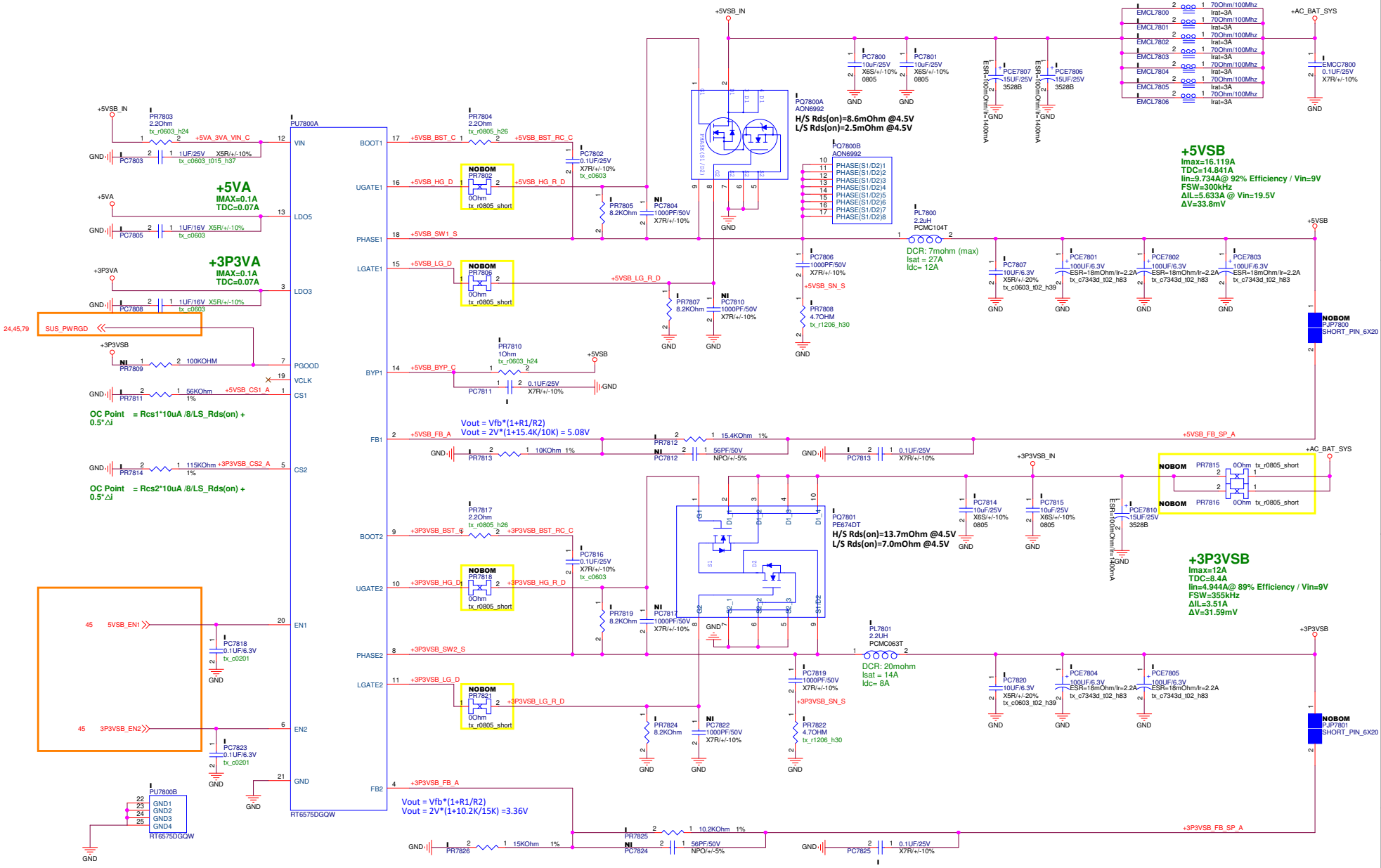
PEGATRON Title : +1P05VSB/+2P5VPP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 76 of 94


Remove PJP7704 and PJP7705
+1P2V_DUAL
Imax=8.44A
TDC=5.908A
Iin=1.324A@ 85% Efficiency / Vin=9V
FSW=300kHz
ΔIL=2.503A @ Vin=19.5V
ΔV=22.53mV
H/S=0.638W
L/S=0.196W
+VTT_DDR
Imax: 0.6A
TDC: 0.42A
VTT LDO: 2A
H/S Rds(on)=8.6mOhm @4.5V
L/S Rds(on)=2.5mOhm @4.5V
DCR: 10mohm (max)
Isat = 22A
Idc= 11A
Change for power sequence - X00/0713
OC Point = Rtrip*10uA /8/LS_Rds(on) + 0.5*ΔI
Mode (Tracking Discharge):
100Kohm=300KHz
200Kohm=400KHz
VREF: 1.8V
ExtReference Vref2
DAC
VREF2: 5V*2.43K/(7.68K+2.43K)=1.202V
TPS51216RUKR
RT9406GV8
AON6992
PCMCI063T
RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992
Owner | +5VSB OC point | Low Limit | High limit
Atticus | 21.35A @25℃ 15.61A @105℃ | N/A | 0.7uH @ 26A
Terry | 21.35A @25℃ 15.61A @105℃ | N/A | 0.7uH @ 26A
RDS(ON)=2.2mΩ(25℃) -SiZ980DT
RDS(ON)=3.0mΩ(105℃) -SiZ980DT
Owner | +5VSB OC point | Low Limit | High limit
Atticus | 24.09A @25℃ 18.00A @105℃ | N/A | 0.7uH @ 26A
Terry | 24.09A @25℃ 18.00A @105℃ | N/A | 0.7uH @ 26A
<Core Design>
PEGATRON
Title : +1P2V_DUAL & +VTTDDR
Pegatron Corp.
Engineer: Chris_Tseng
Size: Custom
Project Name: Vulcan
Rev: X00
Date: Wednesday, November 28, 2018
Sheet 77 of 94



RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992

Owner	+5VSB OC point	Low Limit	High limit
	30.82A @25℃ 22.82A @105℃	N/A	1.6uH @ 36A
	32.3165A @25℃ 23.89A @105℃	N/A	1.6uH @ 36A

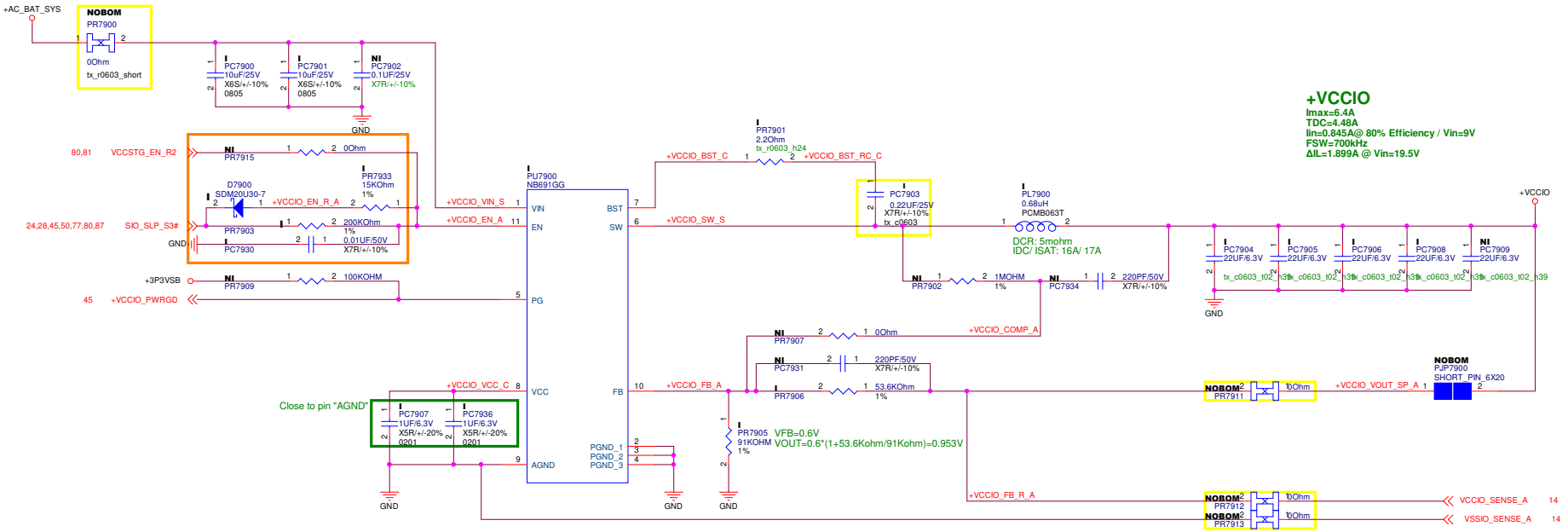
RDS(ON)=7.0mΩ(25℃) -SIZ340DT-T1-GE3
RDS(ON)=9.8mΩ(105℃) -SIZ340DT-T1-GE3

Owner	+3P3VSB OC point	Low Limit	High limit
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A

RDS(ON)=2.2mΩ(25℃) -SIZ980DT
RDS(ON)=3.08mΩ(105℃) -SIZ980DT

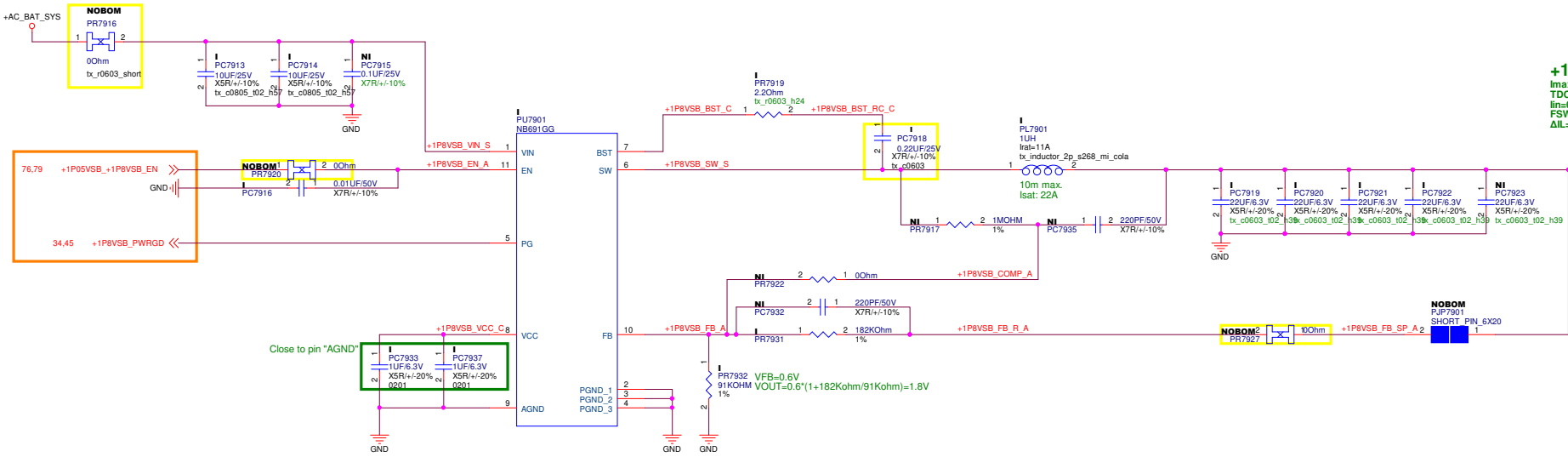
Owner	+5VSB OC point	Low Limit	High limit
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A

PEGATRON Title : +3P3VSB / +5VSB
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 78 of 94



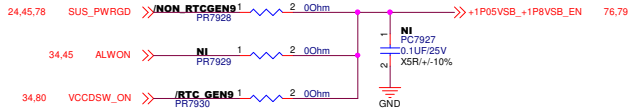
+VCCIO
Imax=6.4A
TDC=4.48A
Iin=0.845A@ 80% Efficiency / Vin=9V
FSW=700kHz
ΔIL=1.899A @ Vin=19.5V

Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 17A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 17A



+1P8VSB
Imax=3.493A
TDC=2.4451A
Iin=0.812A@ 86% Efficiency / Vin=9V
FSW=700kHz
ΔIL=2.334A @ Vin=19.5V

Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 22A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 22A



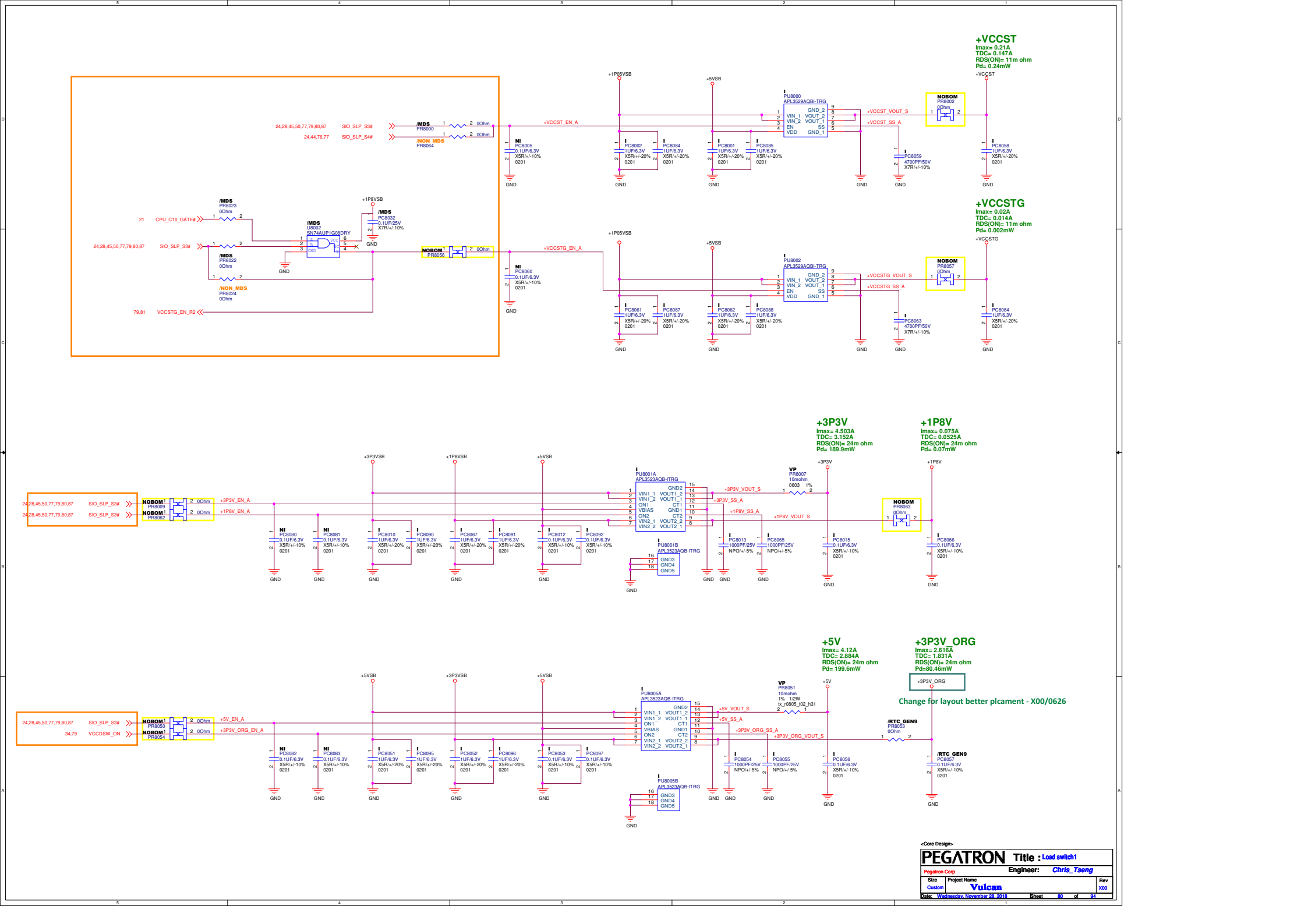
<Core Design>

PEGATRON Title : 79.+VCCIO/ +1P8V

Pegatron Corp. Engineer: Chris_Tseng

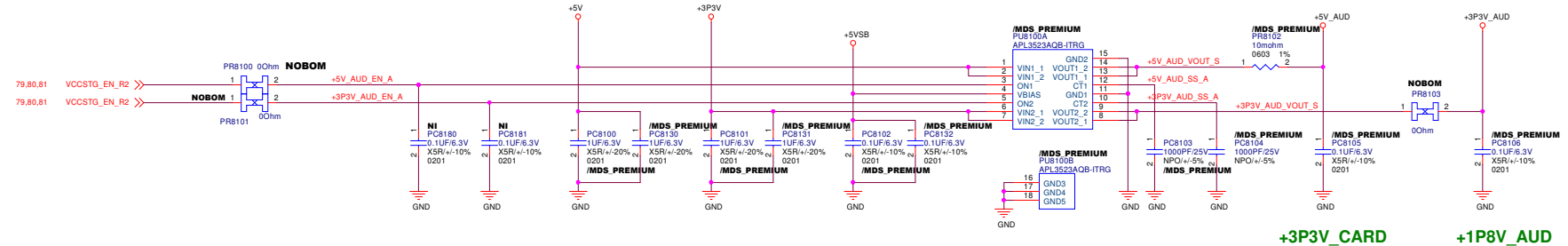
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 79 of 94


+VCCST
Imax= 0.21A
TDC= 0.147A
RDS(ON)= 11m ohm
Pd= 0.24mW
+VCCSTG
Imax= 0.02A
TDC= 0.014A
RDS(ON)= 11m ohm
Pd= 0.002mW
+3P3V
Imax= 4.503A
TDC= 3.152A
RDS(ON)= 24m ohm
Pd= 189.9mW
+1P8V
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24m ohm
Pd= 0.07mW
+5V
Imax= 4.12A
TDC= 2.884A
RDS(ON)= 24m ohm
Pd= 199.6mW
+3P3V_ORG
Imax= 2.616A
TDC= 1.831A
RDS(ON)= 24m ohm
Pd=80.46mW
Change for layout better plcament - X00/0626
PEGATRON
Title : Load switch1
Pegatron Corp.
Engineer: Chris_Tseng
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 80 of 94

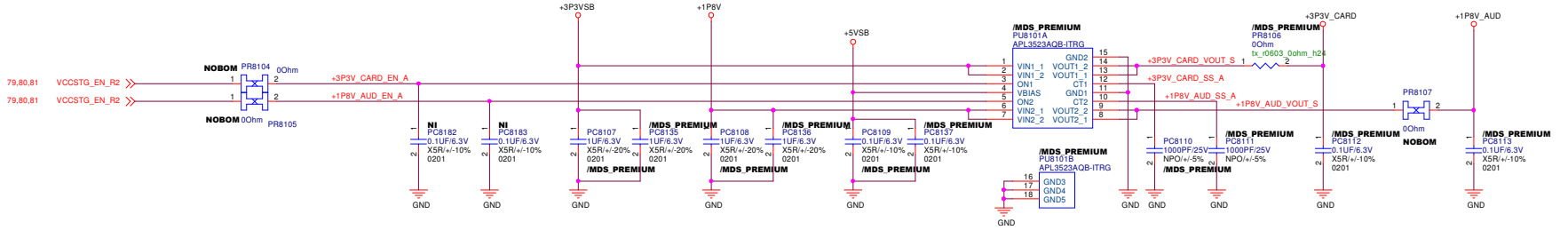
+5V_AUD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW

+3P3V_AUD
Imax= 0.01A
TDC= 0.007A
RDS(ON)= 24mohm
Pd=0.001mW



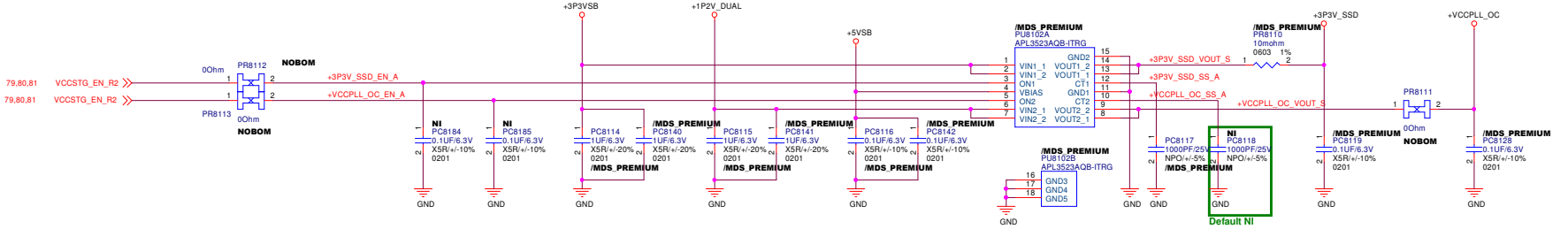
+3P3V_CARD
Imax= 0.4A
TDC= 0.28A
RDS(ON)= 24m ohm
Pd= 1.9mW

+1P8V_AUD
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24mohm
Pd=0.07mW



+3P3V_SSD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW

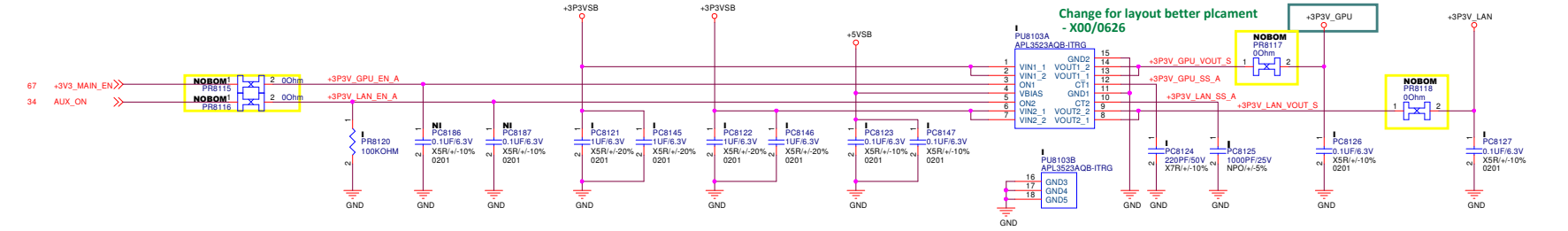
+VCCPLL_OC
Imax= 0.13A
TDC= 0.091A
RDS(ON)= 24mohm
Pd=0.2mW



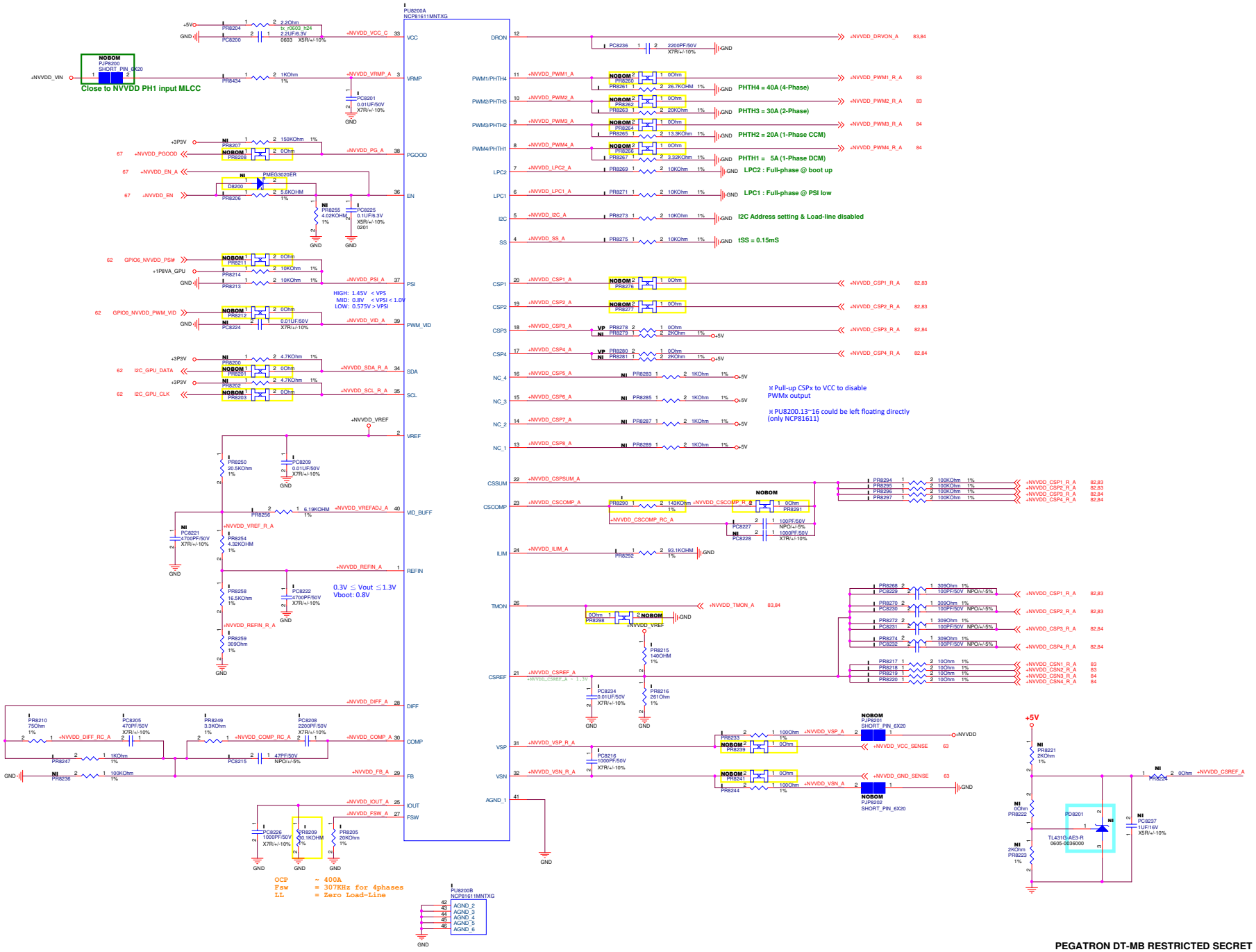
+3P3V_GPU
Imax= 0.07A
TDC= 0.049A
RDS(ON)= 24mohm
Pd=0.06mW

+3P3V_LAN
Imax= 0.152A
TDC= 0.107A
RDS(ON)= 24mohm
Pd=0.27mW

Change for layout better plcament
- X00/0626



PEGATRON	Title :	Load switch2	
Pegatron Corp.	Engineer:	Chris_Tseng	
Size: Custom	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 81 of 94		



PEGATRON DT-MB RESTRICTED SECRET

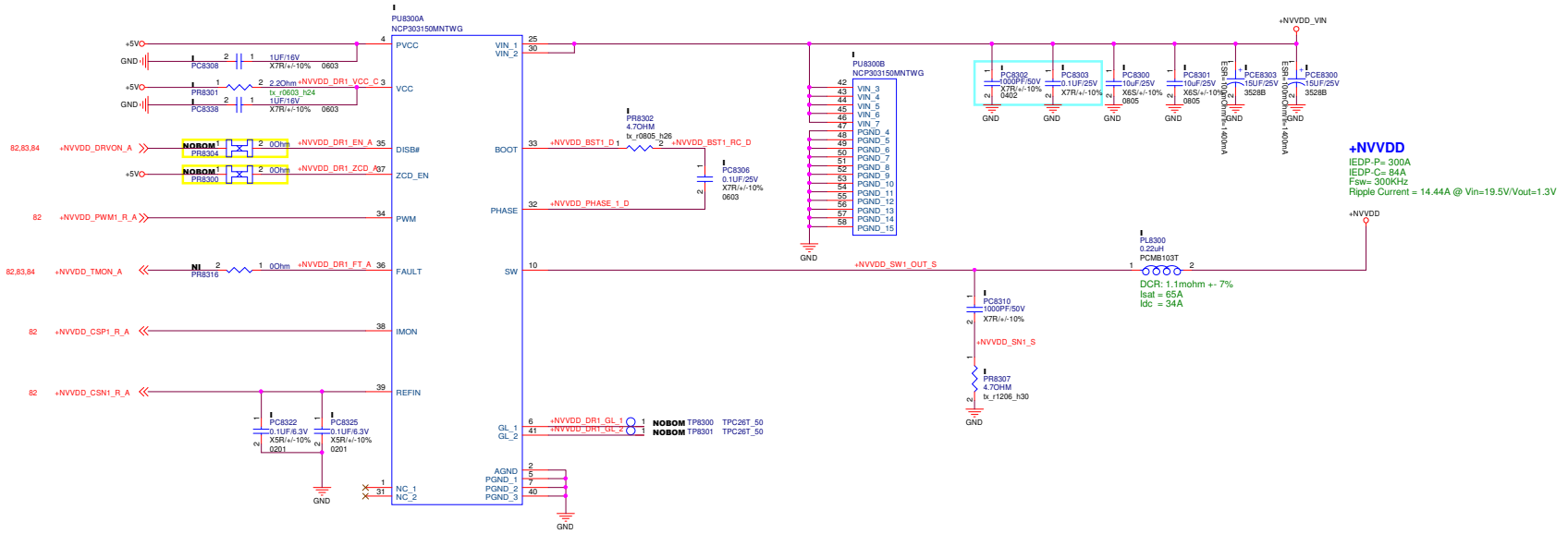
<Core Design>

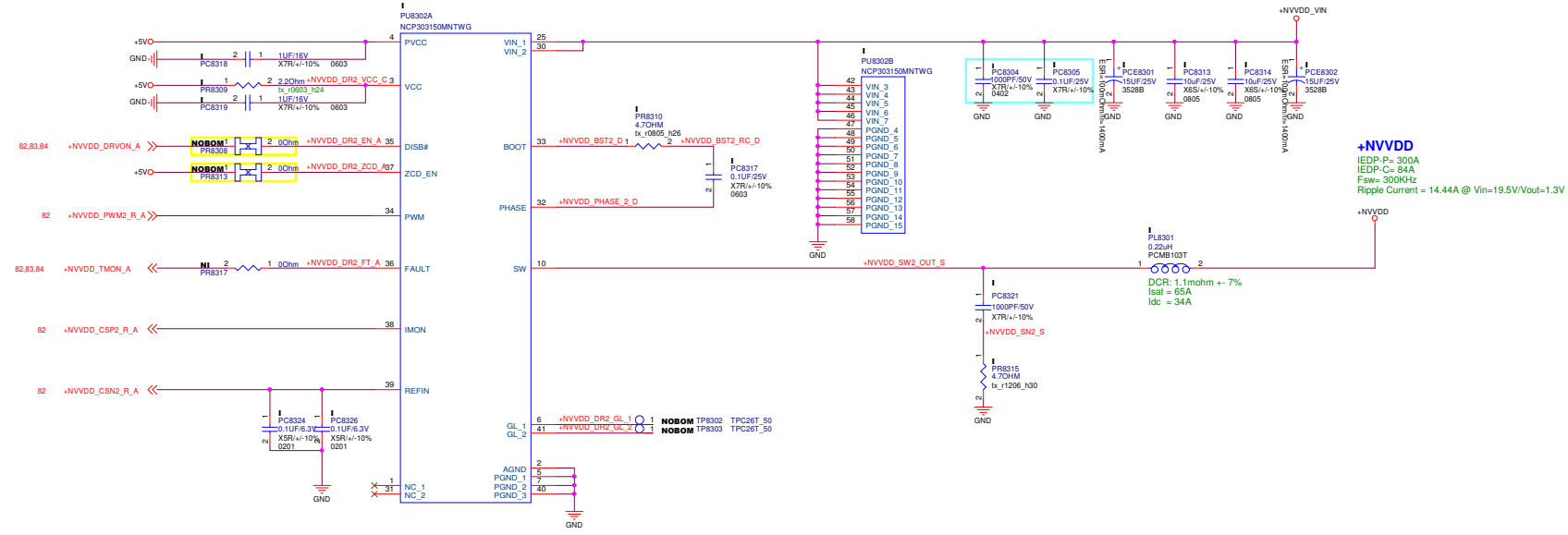
PEGATRON Title : +NVVDD Controller

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 82 of 94





PEGATRON DT-MB RESTRICTED SECRET

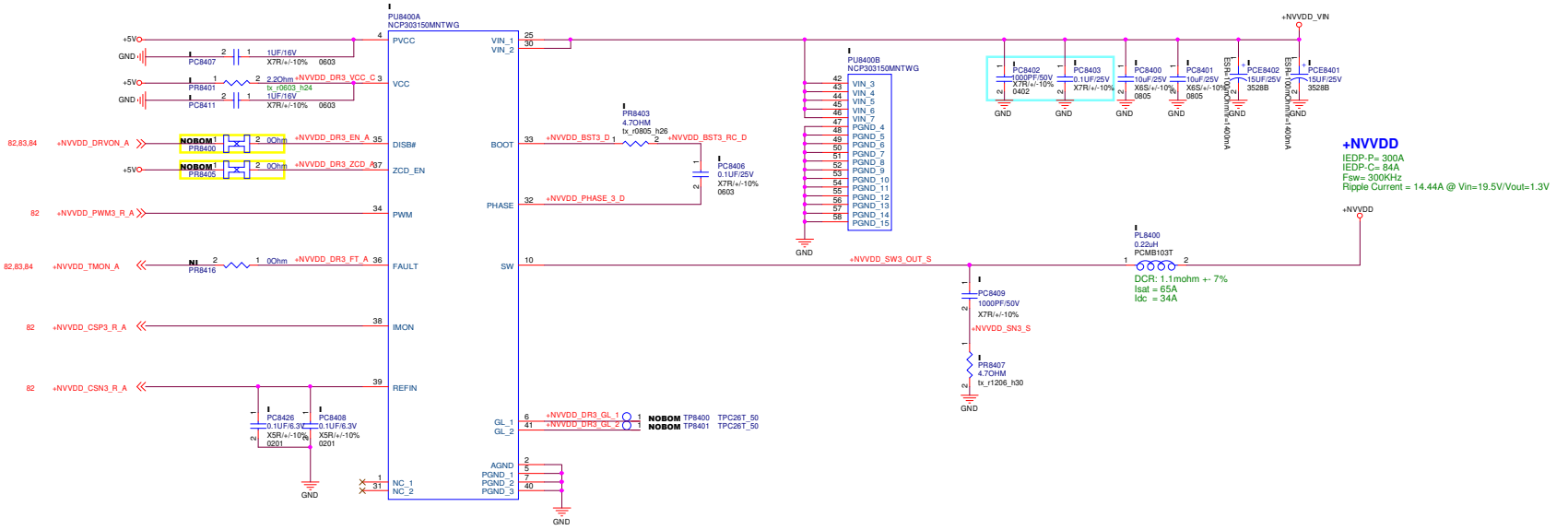
<Core Design>

PEGATRON Title : +NVDD Driver /Cap

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 83 of 94



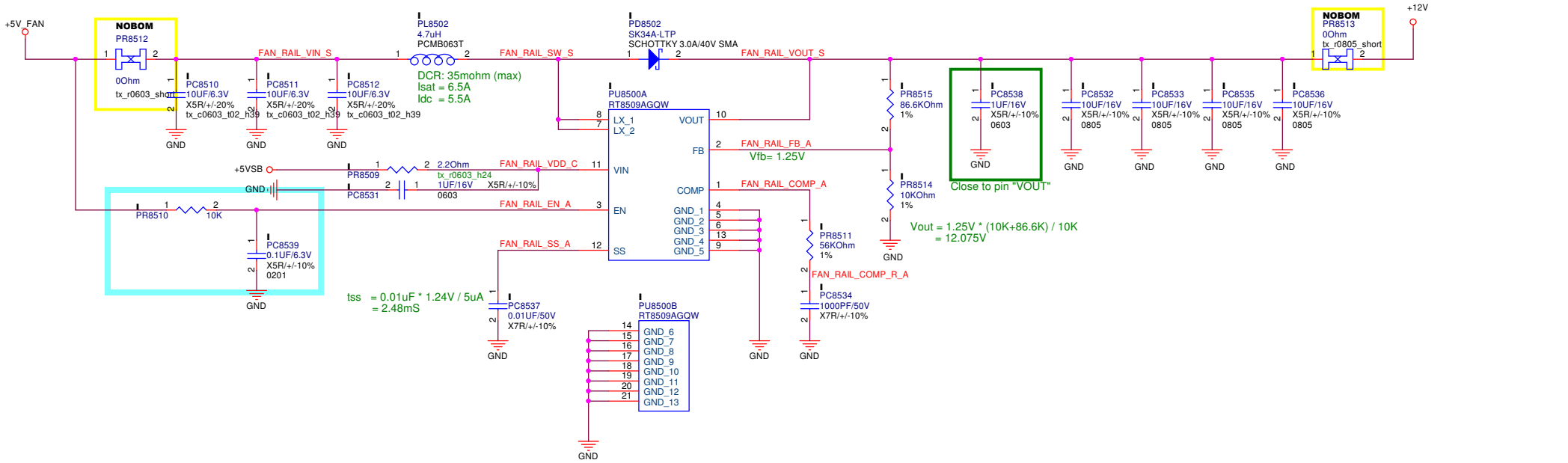
<Core Design>

PEGATRON Title : +NVVDD Driver-2

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 84 of 94



Owner	+12V OC point	Low Limit	High limit
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A

※ OC point is based on peak inductor current

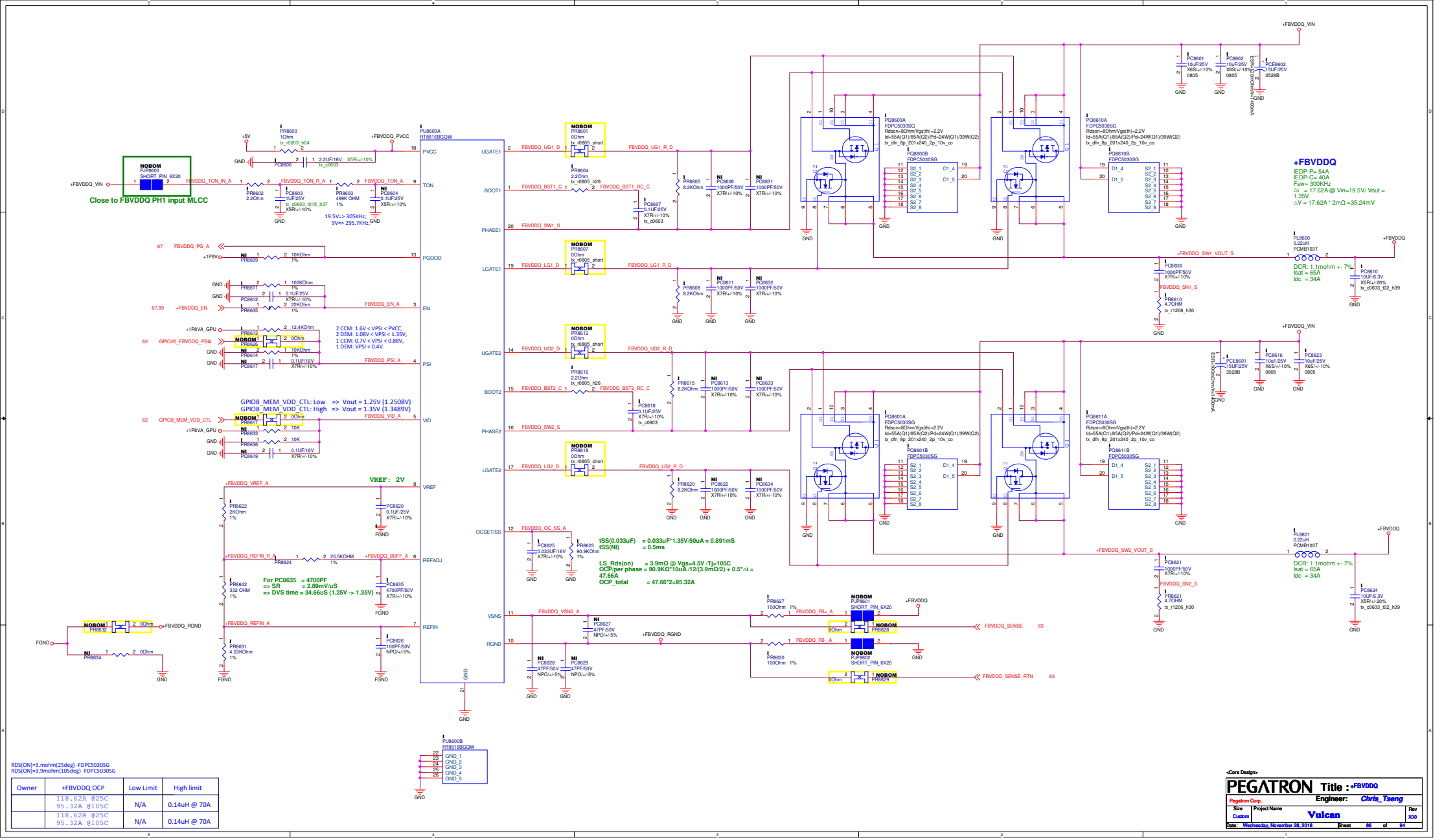
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +12V

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 85 of 94



RDS(ON)=3.mohm(25deg) -FDPC5030SG
RDS(ON)=3.9mohm(105deg) -FDPC5030SG

Owner	+FBVDDQ OCP	Low Limit	High limit
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A

<Core Design>

PEGATRON Title : +FBVDDQ

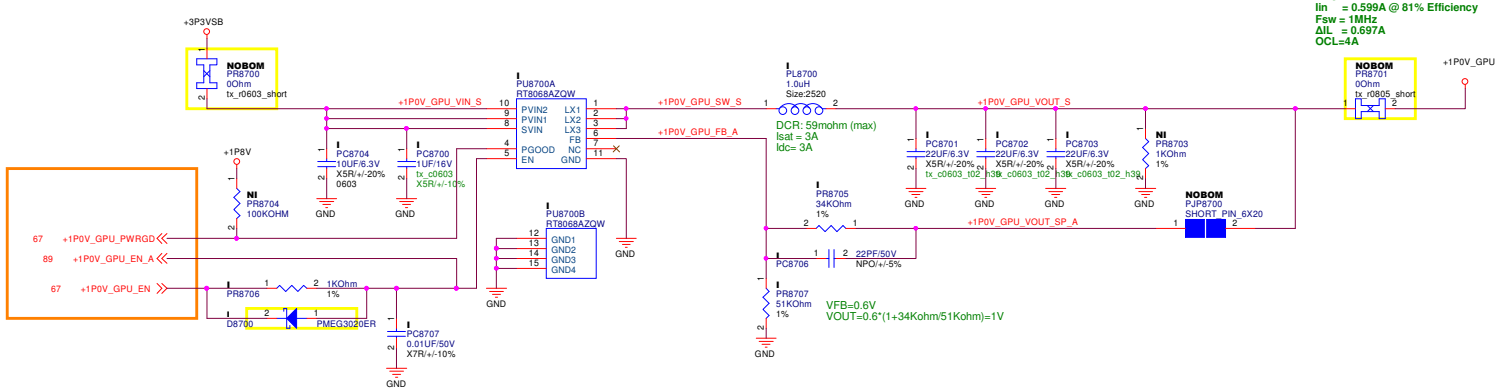
Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 86 of 94

+1P0V_GPU

Imax = 1.6A
TDC =1.12A
Iin = 0.599A @ 81% Efficiency
Fsw = 1MHz
ΔIL = 0.697A
OCL=4A



Owner	+1P0V_GPU	Low Limit	High limit
Atticus	4.0A	N/A	0.44uH @ 6A
Terry	4.0A	N/A	0.44uH @ 6A

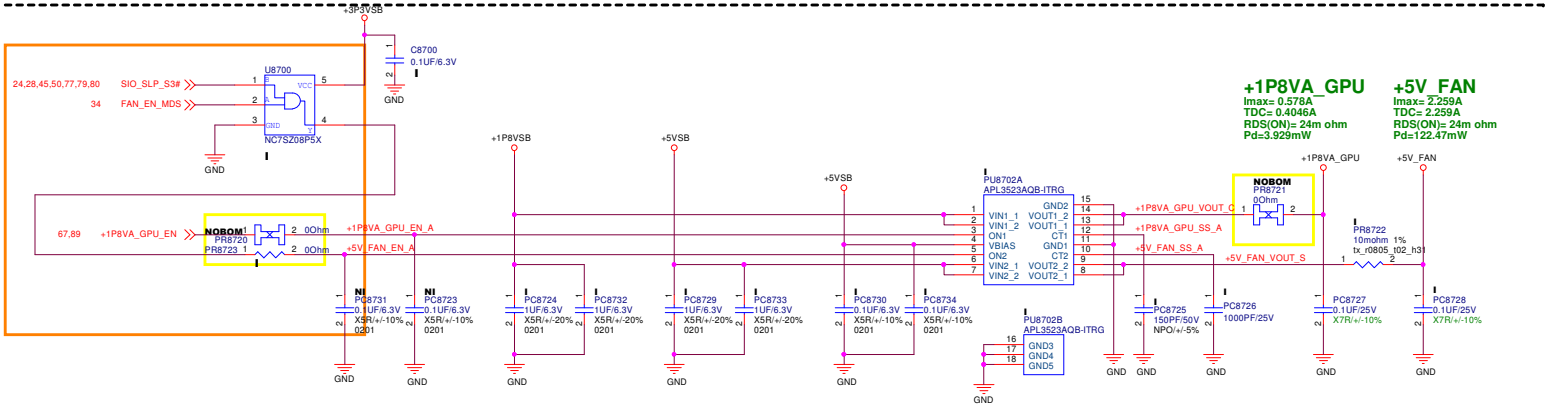
※ OC point is based on peak inductor current

+1P8VA_GPU

Imax= 0.578A
TDC= 0.4046A
RDS(ON)= 24m ohm
Pd=3.929mW

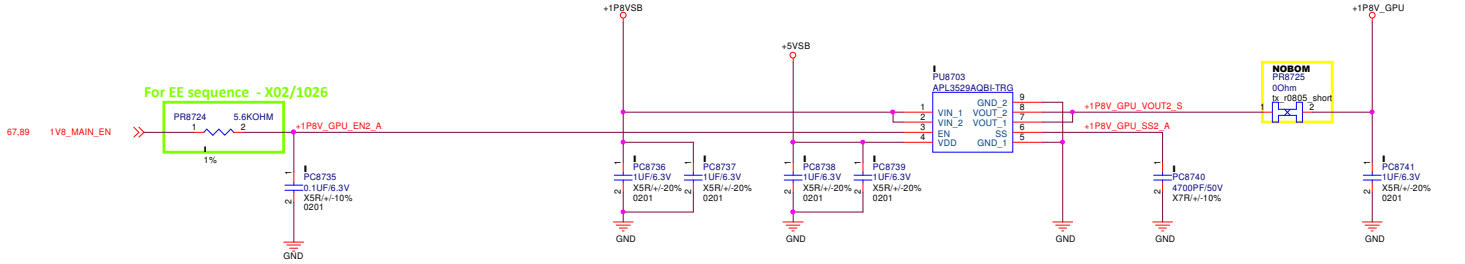
+5V_FAN

Imax= 2.259A
TDC= 2.259A
RDS(ON)= 24m ohm
Pd=122.47mW



+1P8V_GPU

Imax= 2.73A
TDC= 1.911A
RDS(ON)= 11m ohm
Pd=40.17mW



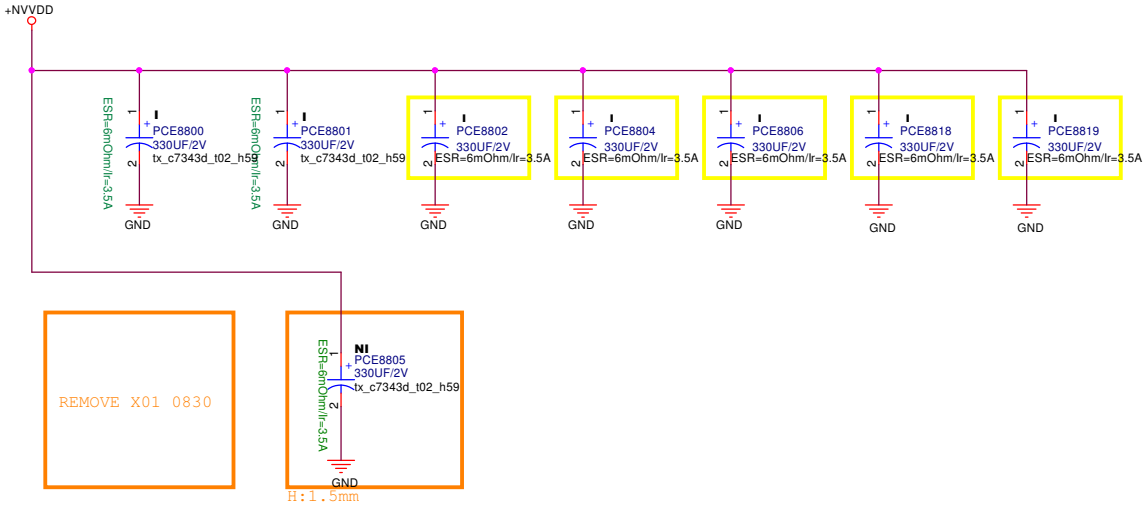
<Core Design>

PEGATRON Title : +1P0V_GPU/+1P8V_GPU & LDO

Pegatron Corp. Engineer: Chris_Tseng

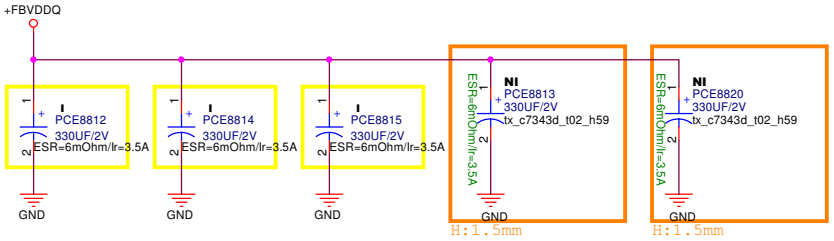
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 87 of 94



+NVVDD Output CAP(w/ +NVVDDS)

330uF/2V/H=2mm * 7 (I)
330uF/2V/H=1.5mm * 2(NI)



+FBVDDQ Output CAP

330uF/2V/H=2mm * 3 (I)
330uF/2V/H=1.5mm * 2(NI)

<Core Design>

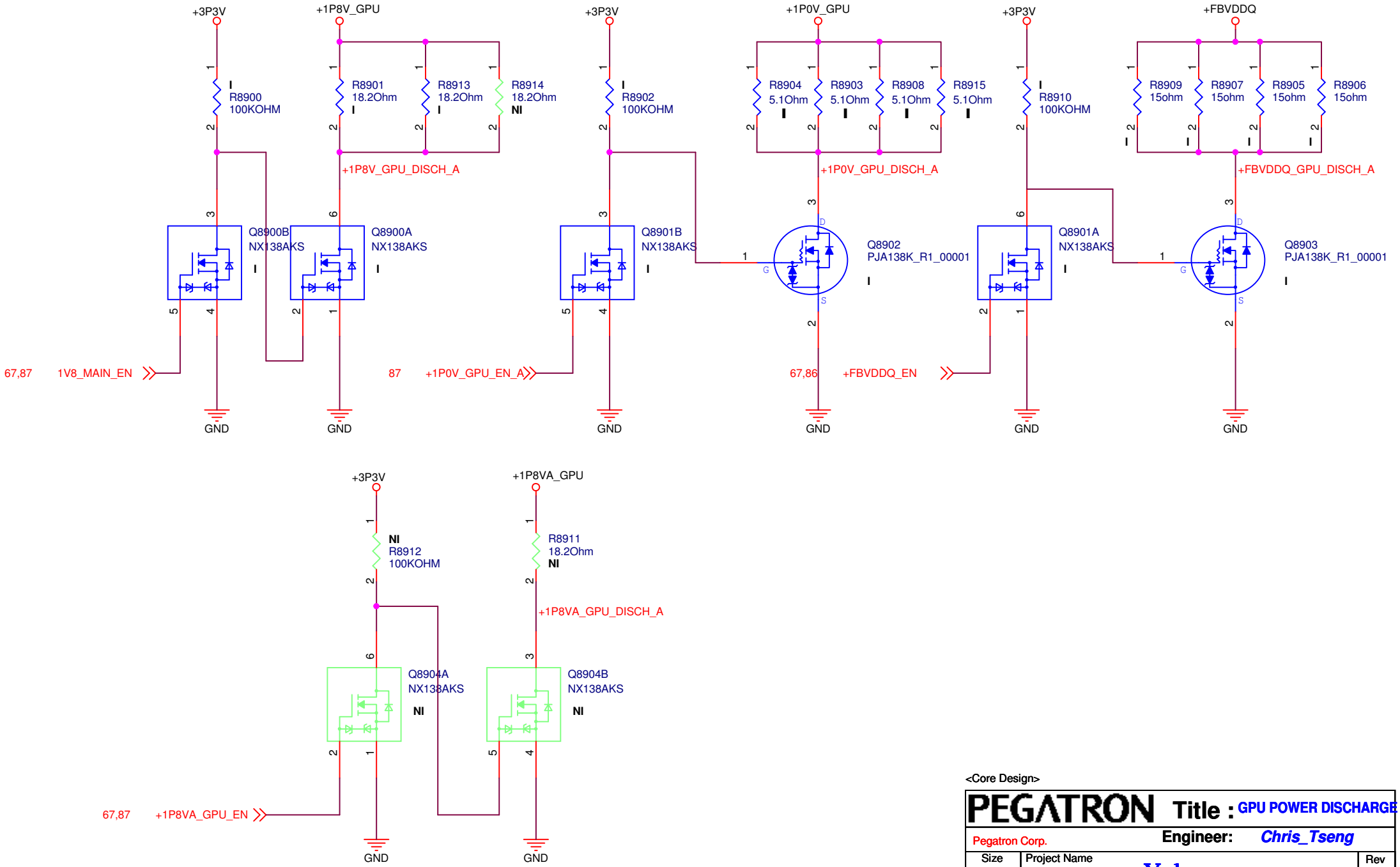
PEGATRON Title : GPU_POWER_CAP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

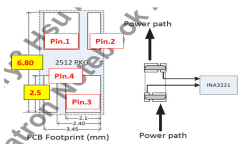
Date: Wednesday, November 28, 2018 Sheet 88 of 94

GPU POWER DISCHARGE



<Core Design>

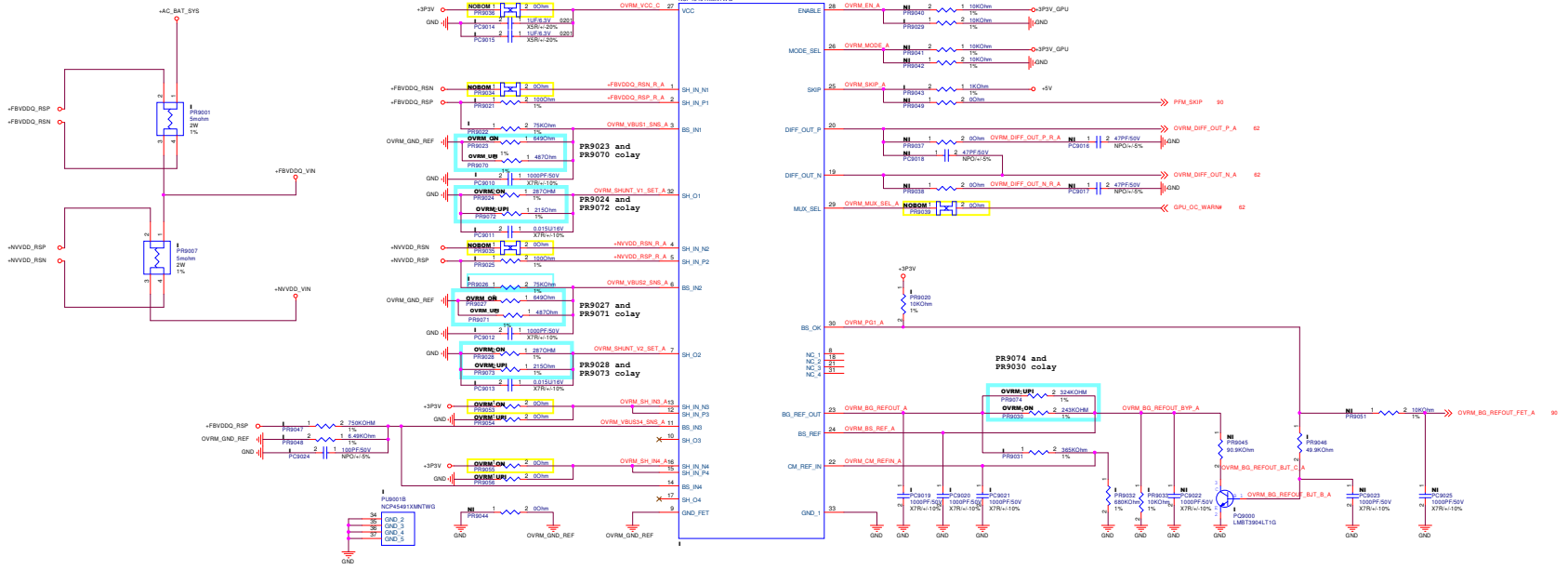
PEGATRON	Title : GPU POWER DISCHARGE	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: A4	Project Name: Vulcan	Rev: B00
Date: Wednesday, November 28, 2018	Sheet 89 of 94	



+AC_BAT_SYS (GPU power only)

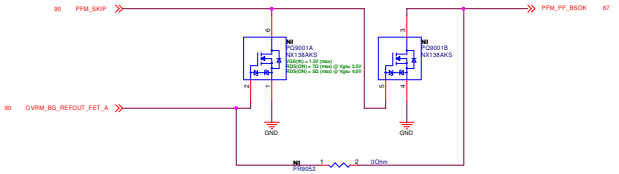
Input Current: 12A @19V (1ms moving average)
Input Current: 10A @19V (5ms moving average)
Input Current : 4.21A @19V (1s movingi average)

Input Current: 25.33A @9V (1ms moving average)
Input Current: 21.11A @9V (5ms moving average)
Input Current : 8.89A @9V (1s movingi average)



OnSemi		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9023	PR9027	PR9024	PR9028	PR9030	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF

uPI		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9070	PR9071	PR9072	PR9073	PR9074	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF

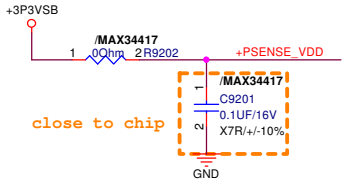


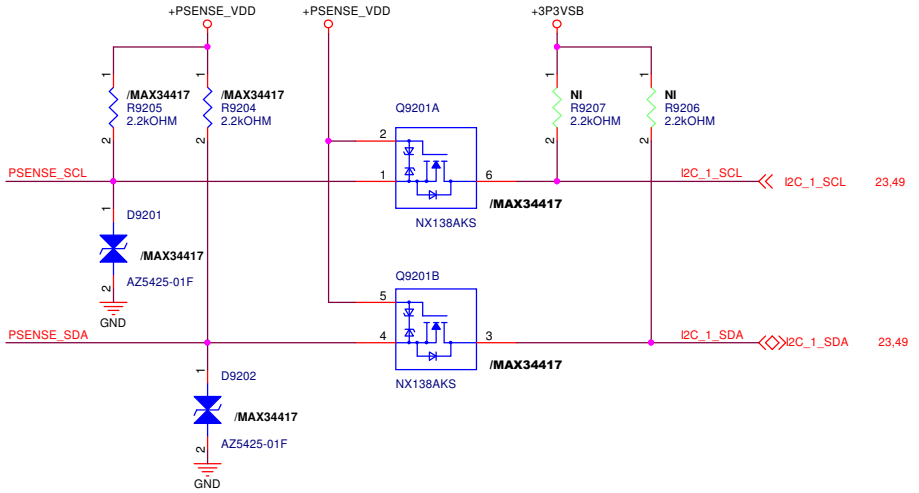
<Core Design>
PEGATRON Title : Power sense
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 90 of 98

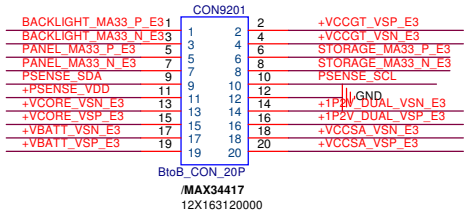
<Core Design>

PEGATRON	Title : RESERVE	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: A2	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 91 of 94	

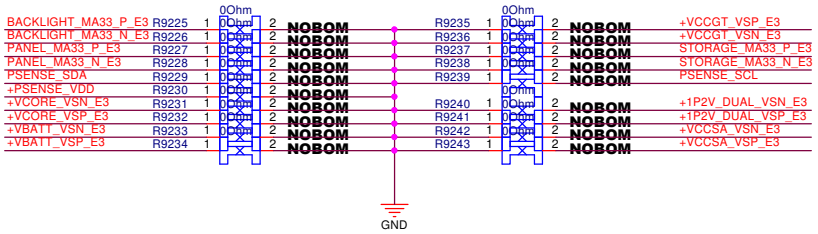
POWER SENSE







VCCGT		SSD/HDD				VDDQ		VCCSA	
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19
PANEL Backlight		PANEL Logic				VCORE		Battery	



	Chip Channel	Connector pin	Item	Location	Sense Resistor	Note
Sensor 1 [10h]	1	P1+/-	CPU_VCCGT	PR7307 (10m ohm) PR7308 (10m ohm)	5m ohm (0x05)	VCCGT
	2	P2+/-	STORAGE	R3109 (10m ohm)	10m ohm (0x0A)	SSD
				R3216 (10m ohm)		HDD(SATA)
	3	P3+/-	DISPLAY_CTLR	R4852 (10m ohm)	10m ohm (0x0A)	Panel Logic
	4	P4+/-	DISPLAY_BACKLIGHT	R4800 (10m ohm)	10m ohm (0x0A)	Panel Backlight
Sensor 2 [1Eh]	1	P5+/-	STYSTEM	R6811 (5m ohm)	5m ohm (0x05)	Battery
	2	P6+/-	CPU_VCORE	PR7100 (10m ohm) PR7101 (10m ohm)	5m ohm (0x05)	VCORE
	3	P7+/-	CPU_VDDQ	PR7700 (10m ohm)	10m ohm (0x0A)	VDDQ
	4	P8+/-	CPU_VCCSA	PR7407 (10m ohm)	10m ohm (0x0A)	VCCSA

<Core Design>

PEGATRON Title : POWER SENSE MAX34417

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 92 of 94

<Core Design>

PEGATRON Title : RESERVE

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

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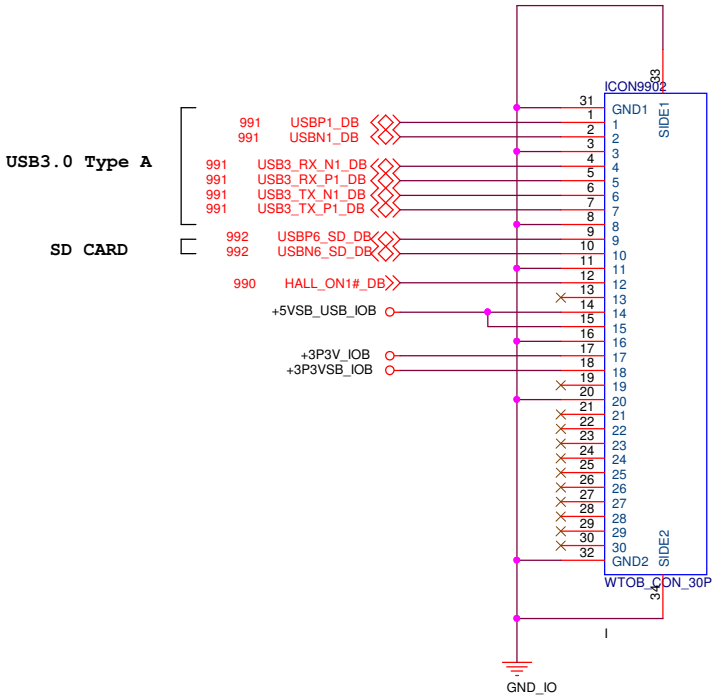
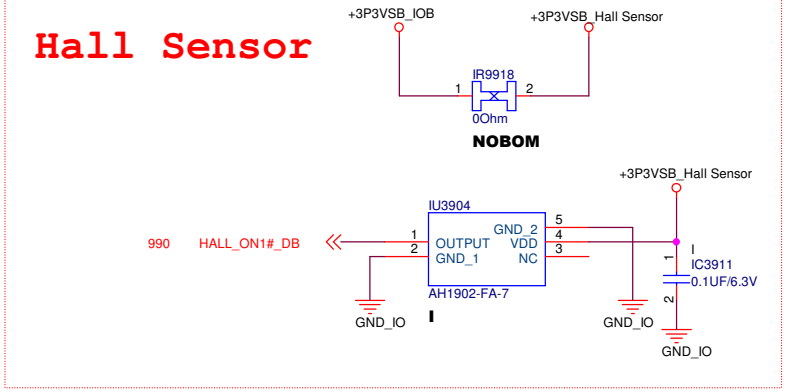
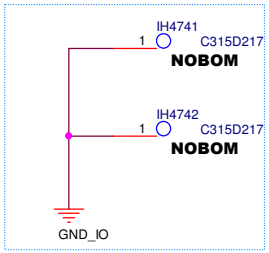
990.IO port/Hall sensor



Hall Sensor



Screw Hole



<Core Design>

PEGATRON Title : IO port/Hall sensor

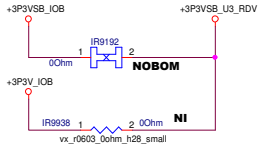
Pegatron Corp. Engineer: Alex_Tsai

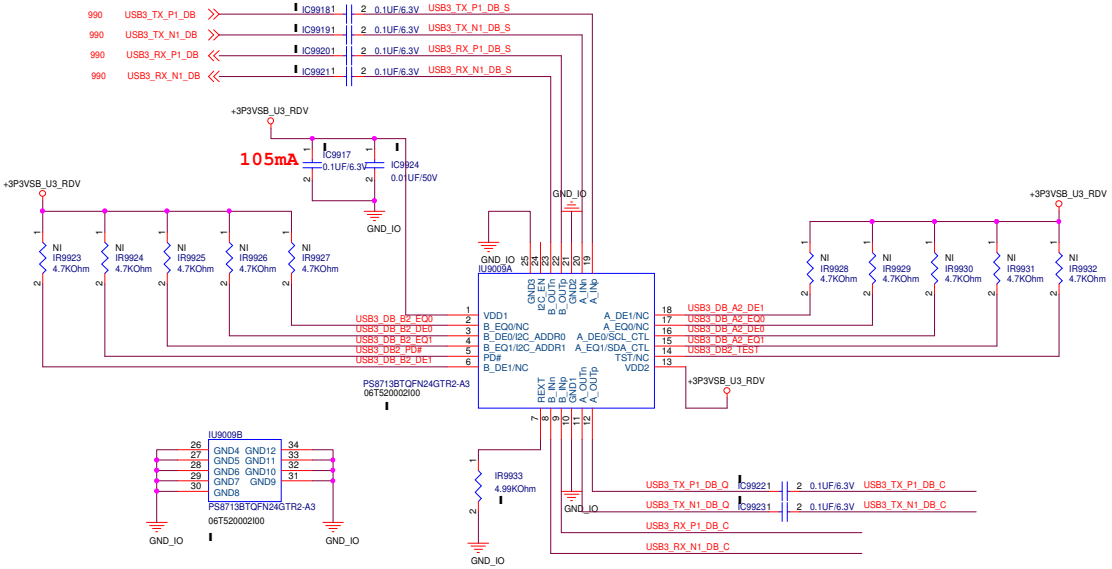
Size	Project Name	Rev
B	Vulcan	X00

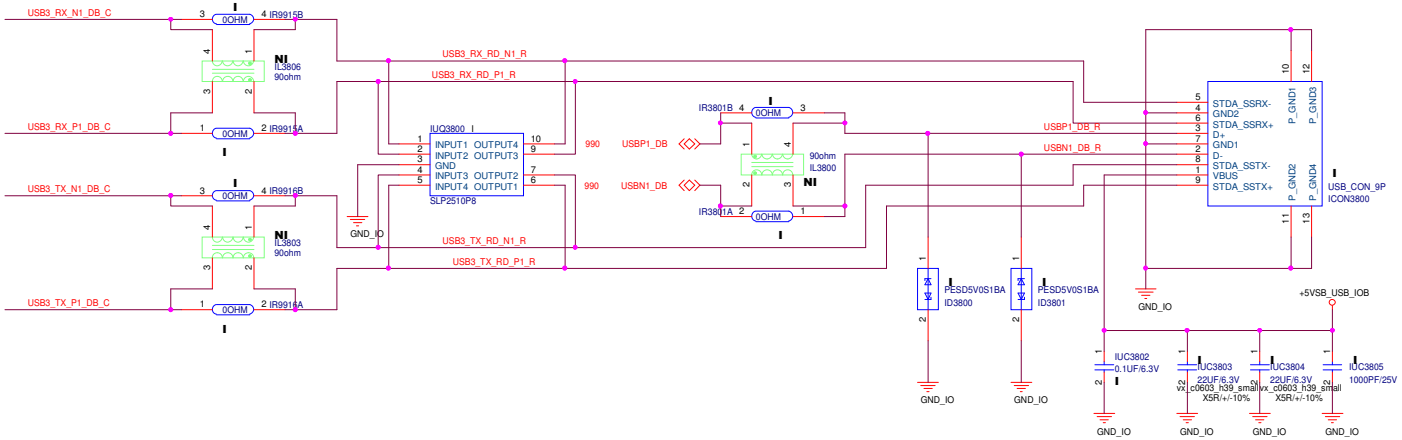
Date: Wednesday, November 28, 2018 Sheet 990 of 94

991.USB PORT

Imax: 105mA





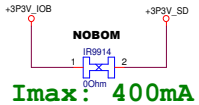


<Core Design>

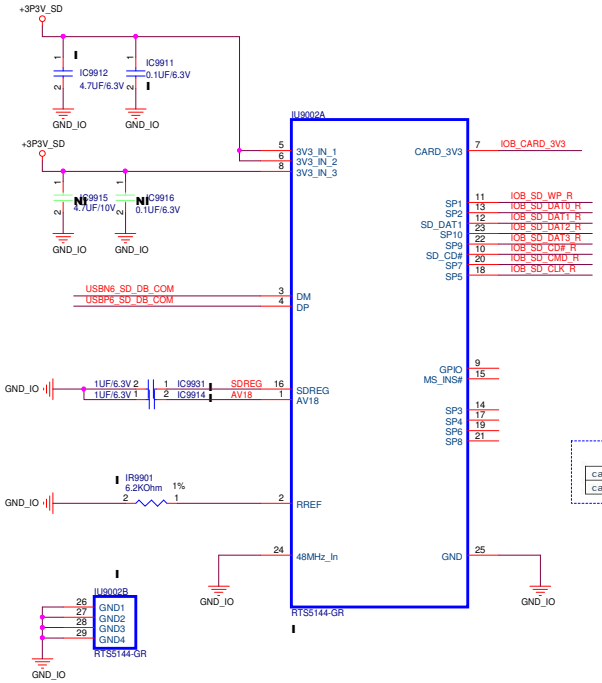
PEGATRON	Title : USB DB PORT	
Pegatron Corp.	Engineer: Alex_Tsai	
Size: C	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 991 of 94	

992.Card_reader_RTS5144-GR

POWER

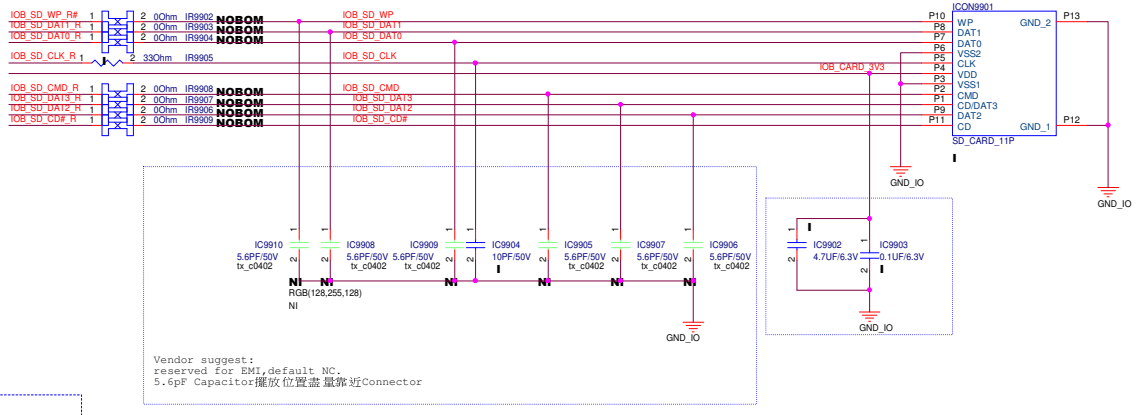


Imax: 400mA

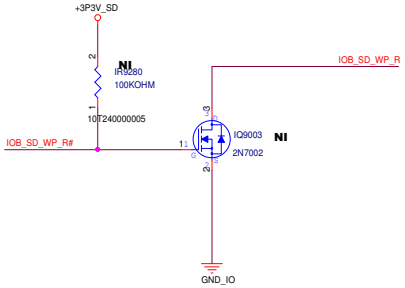


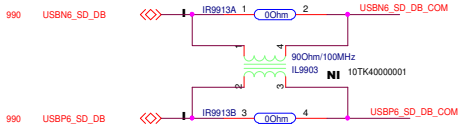
card lock	SD_WP pin high
card unlock	SD_WP pin low

WITHOUT CARD	CARD INSERTED:LOCK	CARD INSERTED:UNLOCK
W/P GND C/D VSS1 P3	W/P GND C/D VSS1 P3	W/P GND C/D VSS1 P3



Vendor suggest:
reserved for EMI,default NC.
5.6pF Capacitor擺放位置盡量靠近Connector





<Core Design>

PEGATRON Title : Card_reader_RTS5144GR

Pegatron Corp. Engineer: Alex_Tsai

Size	Project Name	Rev
C	Vulcan	X00

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