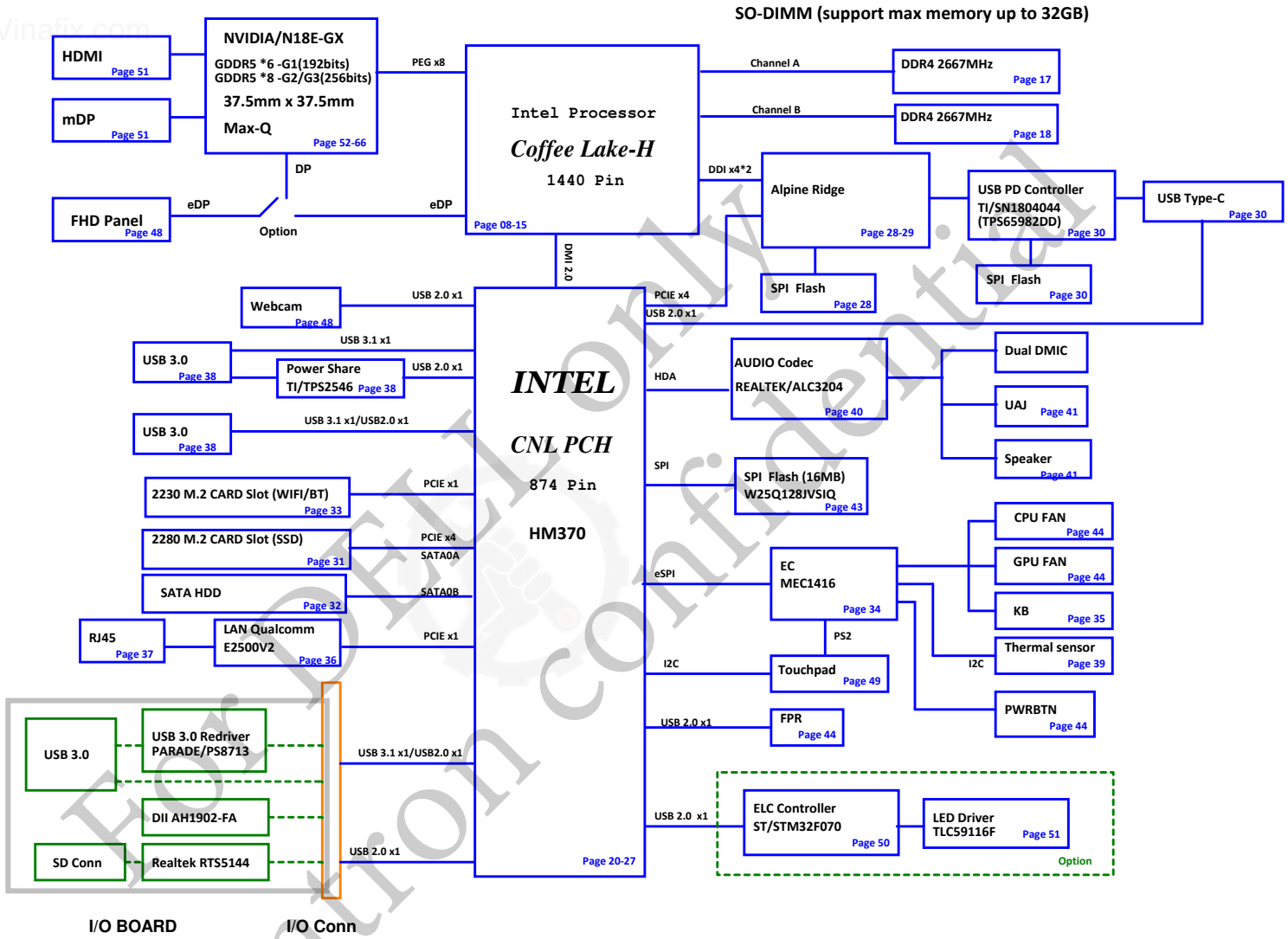
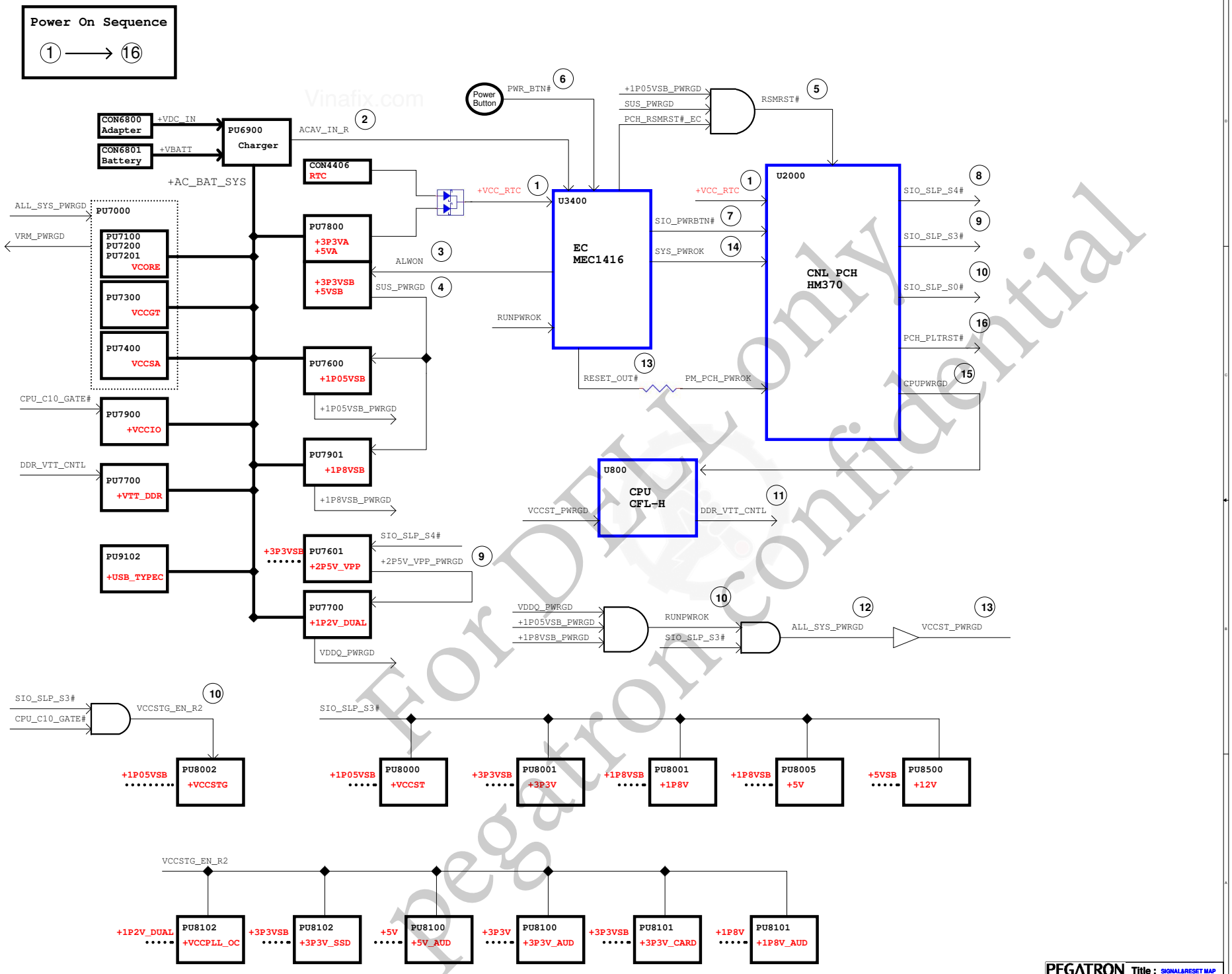
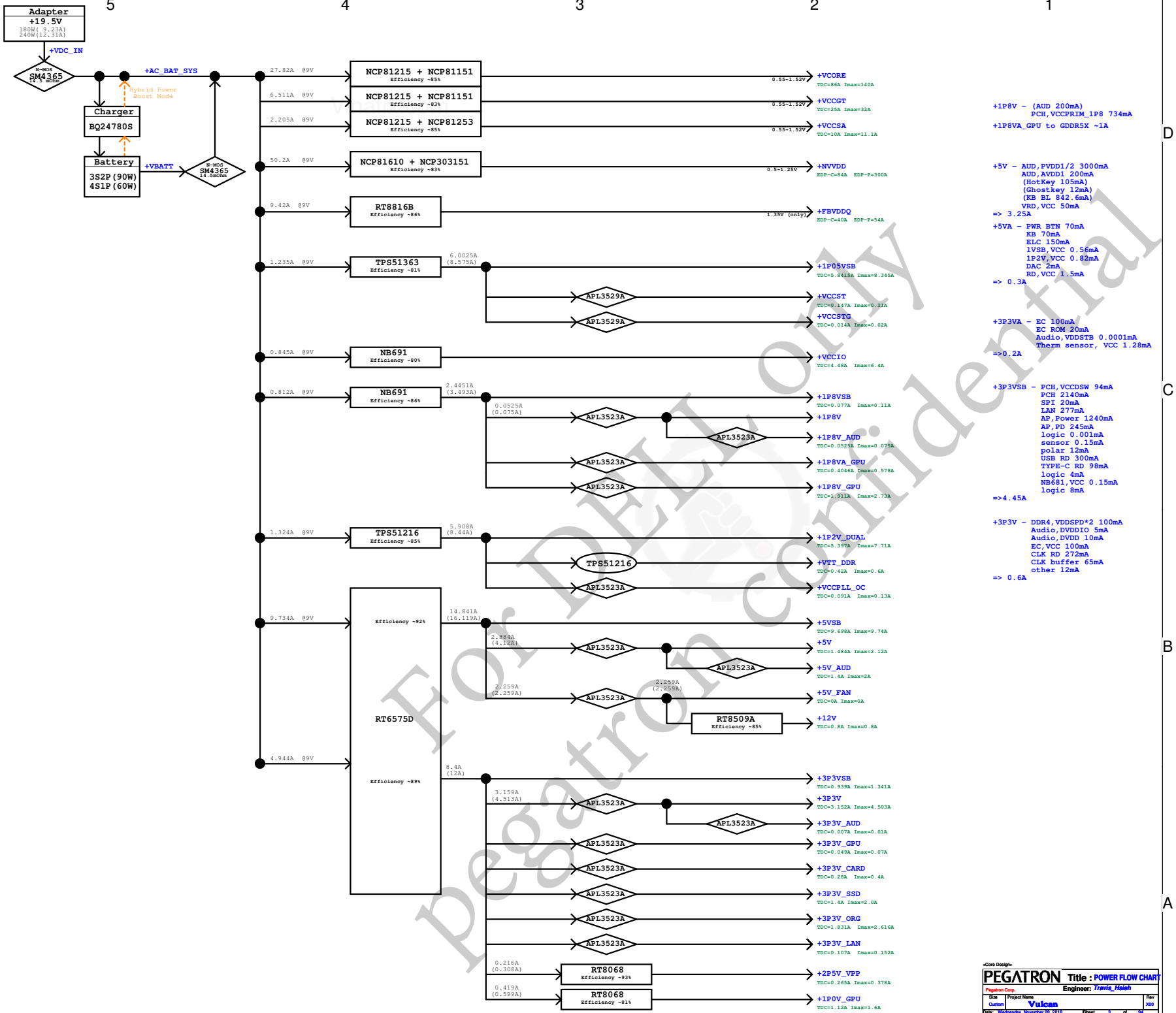
Vulcan (Coffee Lake-H)Revision_1.0

PAGE	TITLE
01	BLOCK DIAGRAM
02	SIGNAL & RESET MAP
03	POWER FLOW CHART
04	CHANGE HISTORY
05	SMBus & I2C Flow
06	Power flow & sequence
07	POWER SEQUENCE
08	CPU DDI/EDP
09	CPU DDR4 CHA
10	CPU DDR4 CHB
11	CPU DMI/PEG
12	CPU MISC
13	CPU VSS
14	CPU POWER
15	CPU DECOUPLING
16	ME DISABLE
17	DDR4_SO-DIMM0
18	DDR4_SO-DIMM1
19	DDR4 DECOUPLING
20	PCH DMI/PCIE/USB/SATA
21	PCH SATA/PCIE
22	PCH ESPI/SPI/FAN/HOST 3-8
23	PCH AUDIO/CL/I2C/UART 4-8
24	PCH SML/I2C/MISC
25	PCH CLOCK
26	PCH VCC
27	PCH VSS
28	Alpine-Ridge - Controller
29	Alpine-Ridge - Power
30	Type-C_PD
31	M.2 PCIE X4 SSD
32	SATA_HDD
33	M.2 WLAN KEY-E
34-35	EC_MEC1416/KEYBOARD
36-37	LAN NIC KILLER & LAN JACK
38	USB CONN and power
39	SENSOR
40	AUDIO CODEC ALC3204
41	AUDIO JACK
42	TPM
43	SM BUS & SPI ROM
44	Other Conn
45-46	ACAV_IN & XDP CONN
47	PCB & Label & Screw
48	eDP Conn
49	Touch & Keyboard BL
50	ELC MCU
51	HDMI
52	GPU_PCIE
53	GPU-Xtal & Straps
54	GPU-BUFFER PARTITION A/B
55	GDDR5X 256Mx32bit _Channel_A
56	GDDR5X 256Mx32bit _Channel_B
57	GPU-BUFFER PARTITION C/D
58	GDDR5X 256Mx32bit _Channel_C
59	GDDR5X 256Mx32bit _Channel_D
60	GPU-MIO&IFPAB_DDI
61	GPU HDMI/TYPC-C
62	GPU-GPIO
63	GPU-POWER&GND
64	GPU-Decoupling
65	GPU-MIO
66	GPU-IFPAB_DDI
67	GPU-POWER Sequence
68	DC_IN
69	Charger
70	VR CONTROLLER
71-72	Vcore Driver
73	Vccgt Driver
74	Vccsa Driver
75	Vcore & VccGT CAP
76	+1P05VSB/+2P5VPP
77	+1P2V_DUAL & +VTTDDR
78	+3VA / +5VA
79	+VCCIO / +1P8V
80-81	Load switch
82	NVVDD CONTROLLER
83-84	NVVDD Driver
85	+12V_FAN
86	+FBVDDQ
87	+1P0V_GPU/+1P8V_GPU & LDO
88	GPU_POWER_CAP
89	GPU POWER DISCHARGE
90	Power Sense
91	



PEGATRON Title : BLOCK DIAGRAM
Pegatron Corp. Engineer: Travis_Hsieh
Size C | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 | Sheet 1 of 94

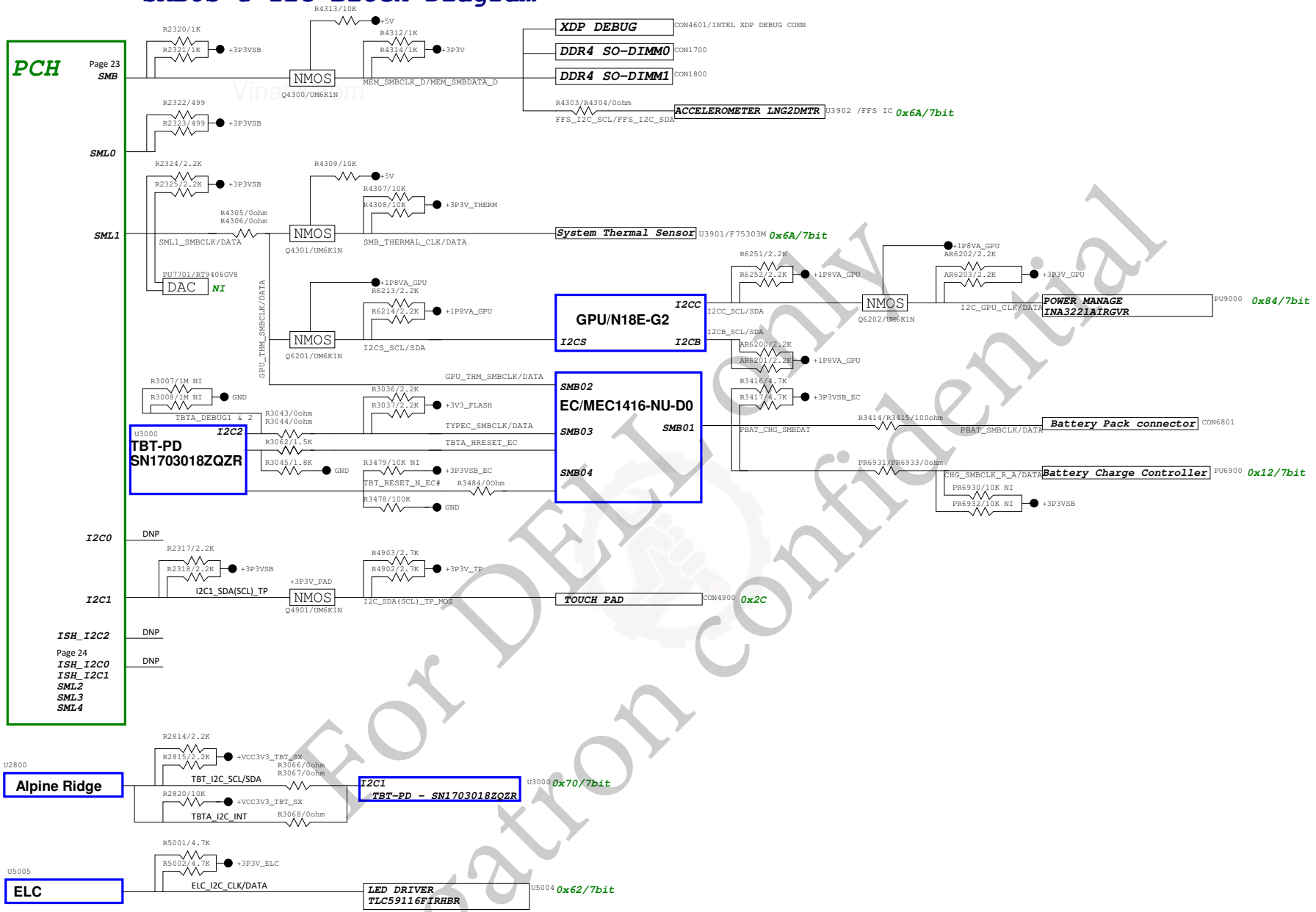


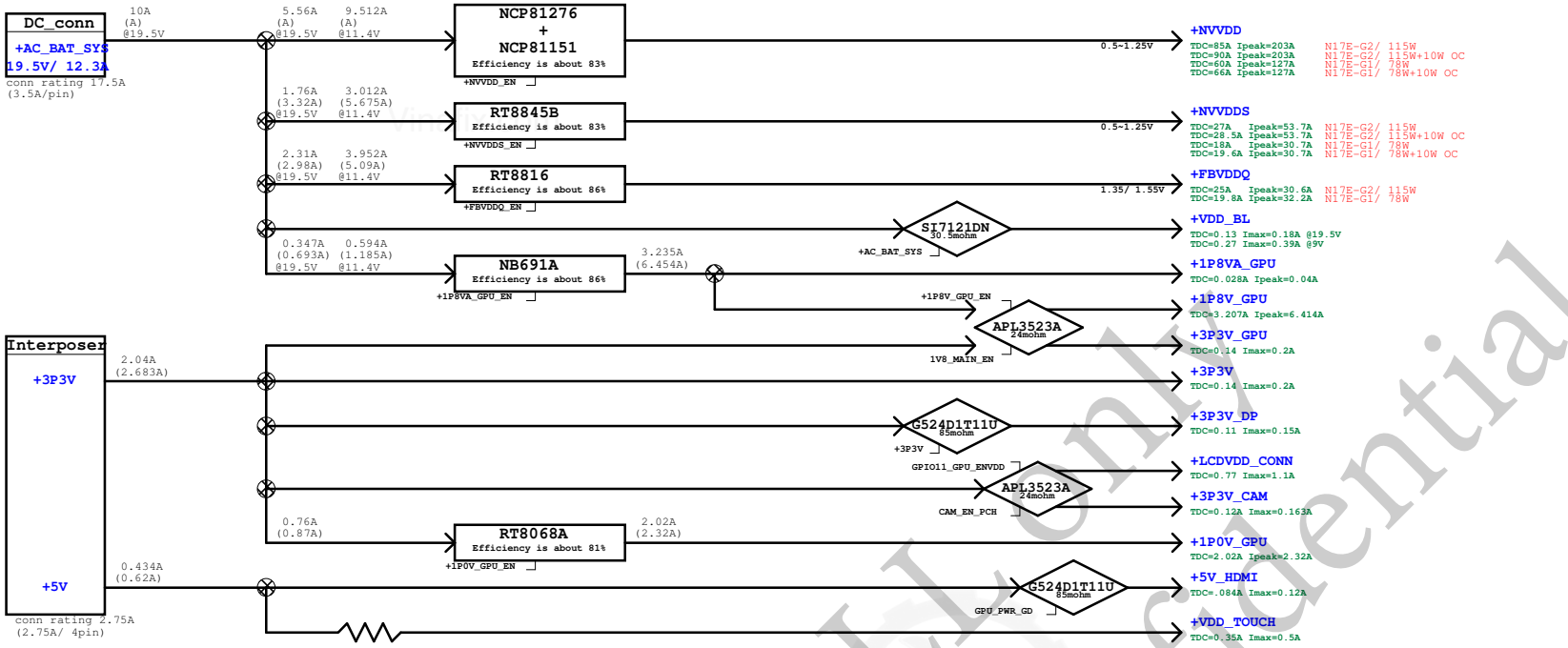


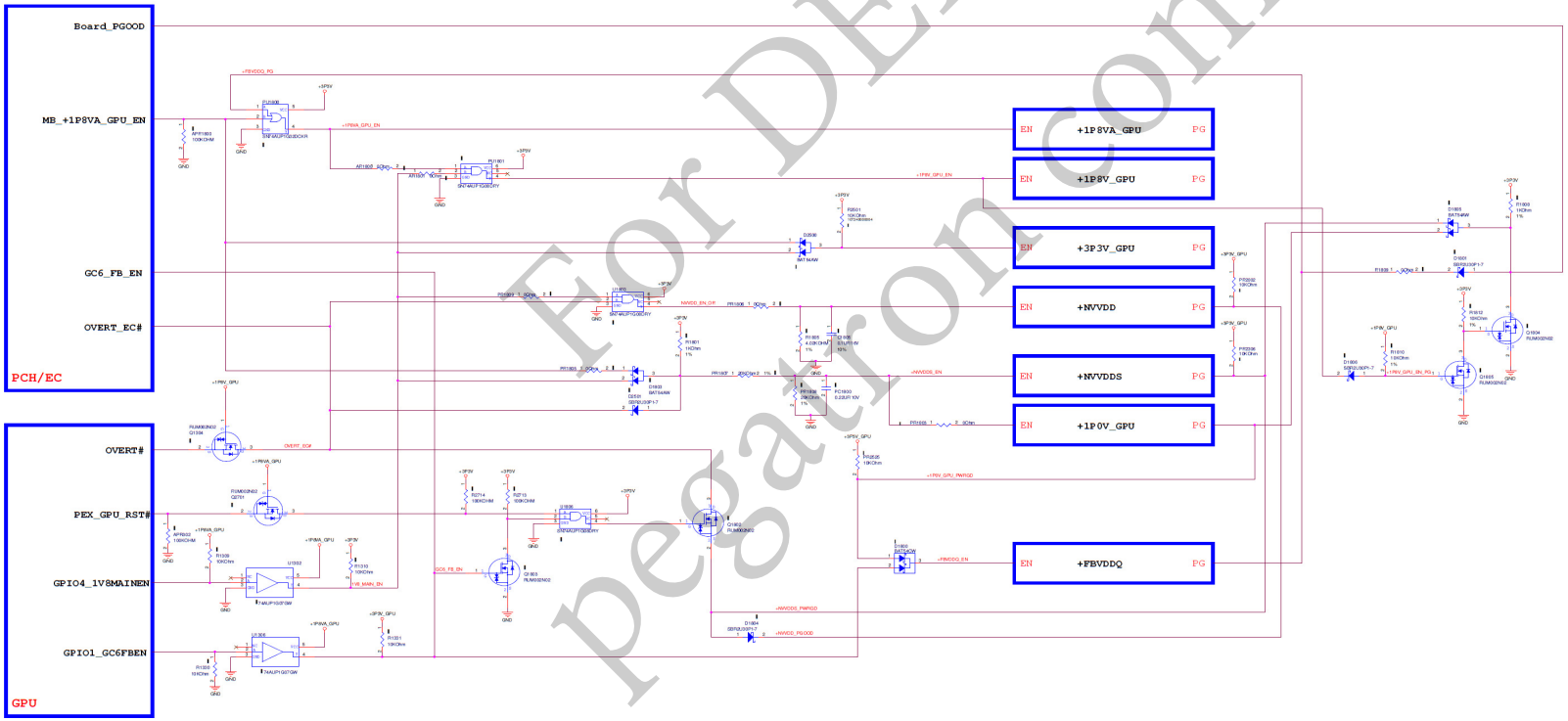
Schematics Change History

Version	Date	Description	Comments
1.00			

SMBUS & I2C Block Diagram







<Core Design>

PEGATRON Title : GPU Power flow & sequence

Pegatron Corp. Engineer: Travis_Hsieh

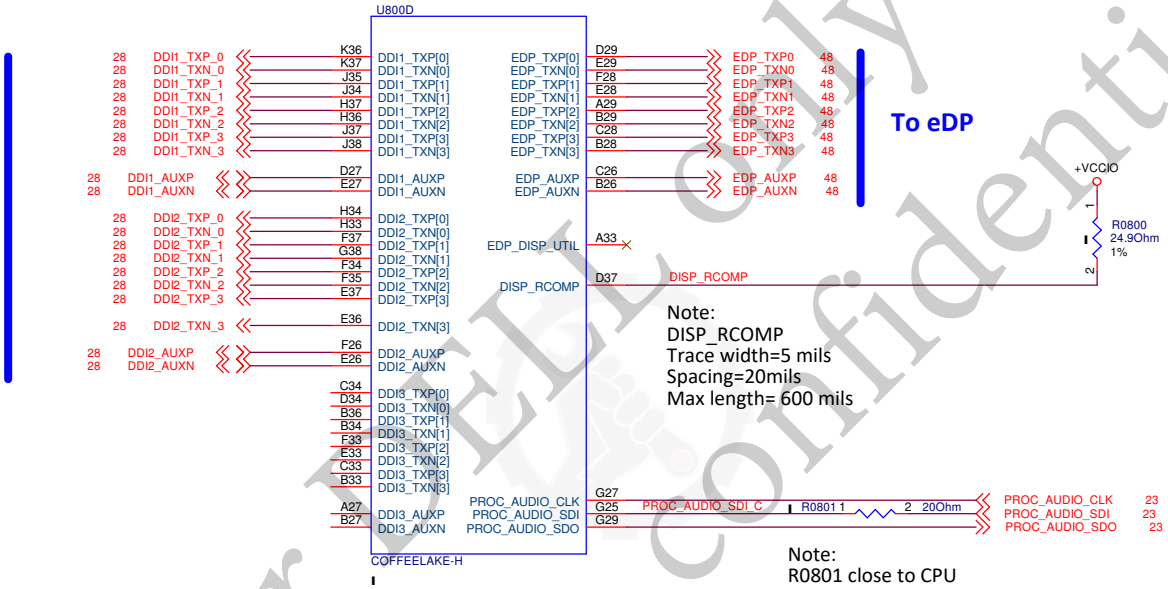
Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 6 of 94

Reserved Page

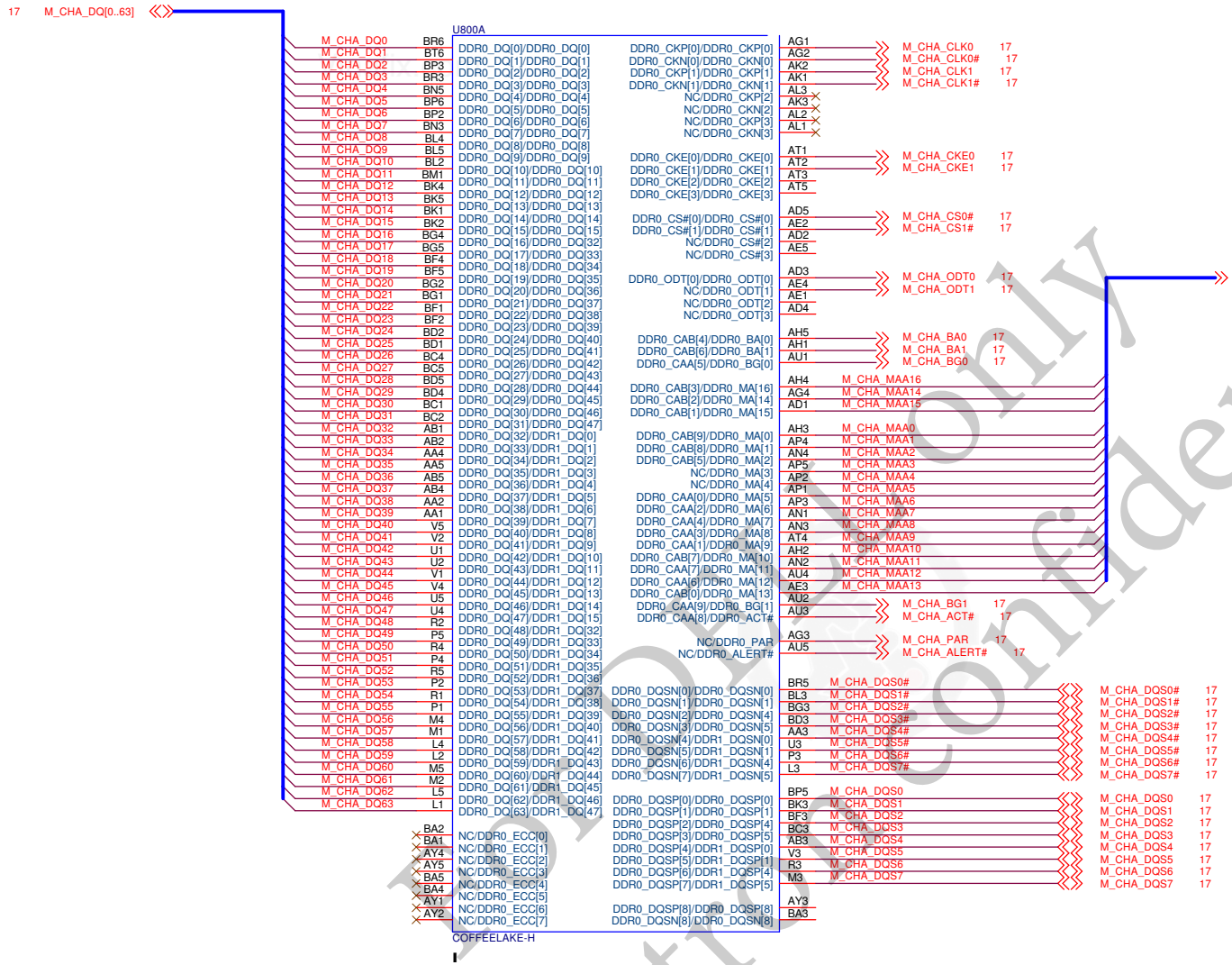
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : POWER SEQUENCE	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 7 of 94	



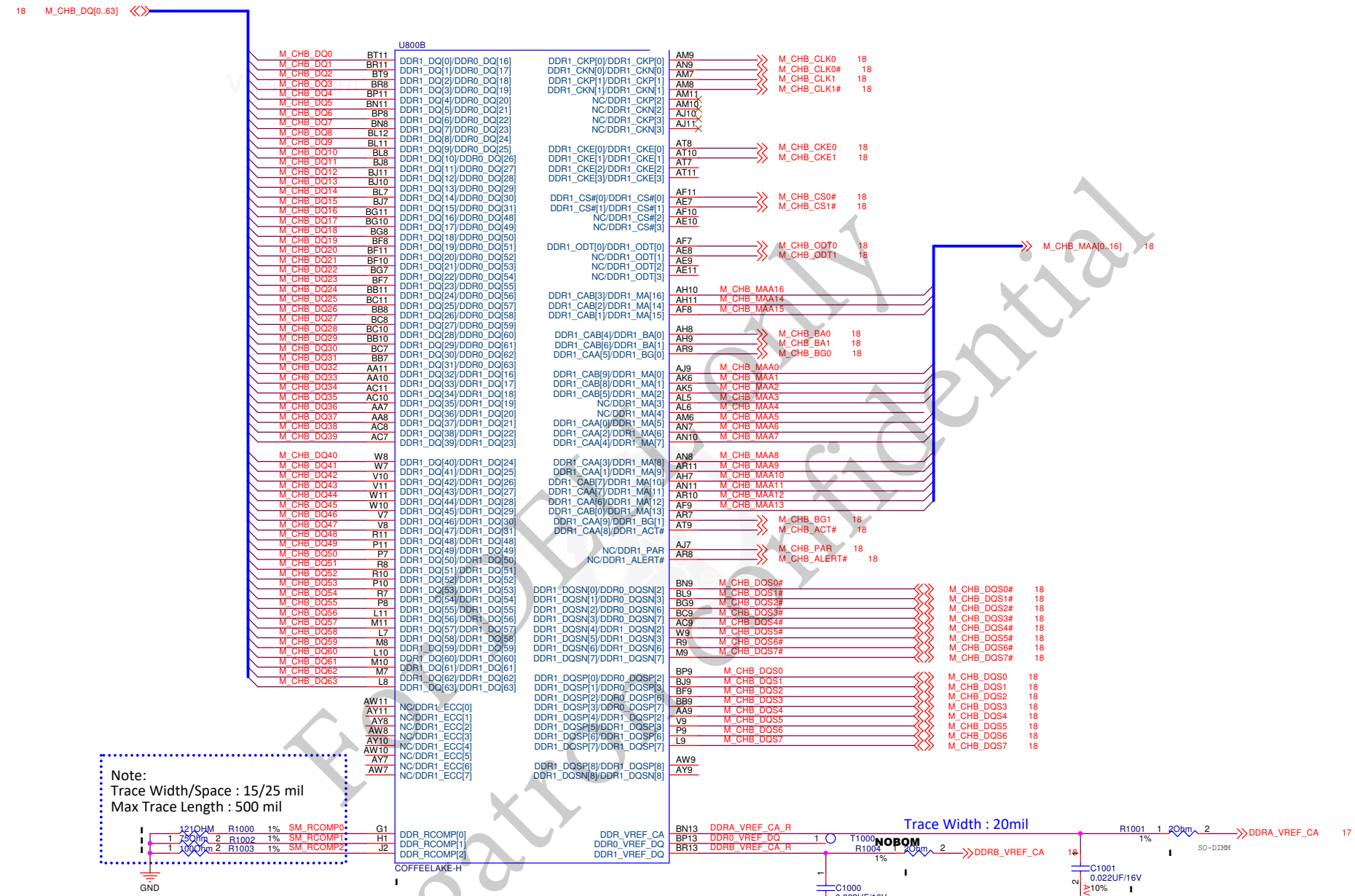
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU DDI/EDP	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 8 of 94	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU DDR4 CHA	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 9 of 94	



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)			Max Length (mils)			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1]/[2]	Byte [1]/[2]	Region	Breakout [1,2]	Total	
RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121	
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75	
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100	

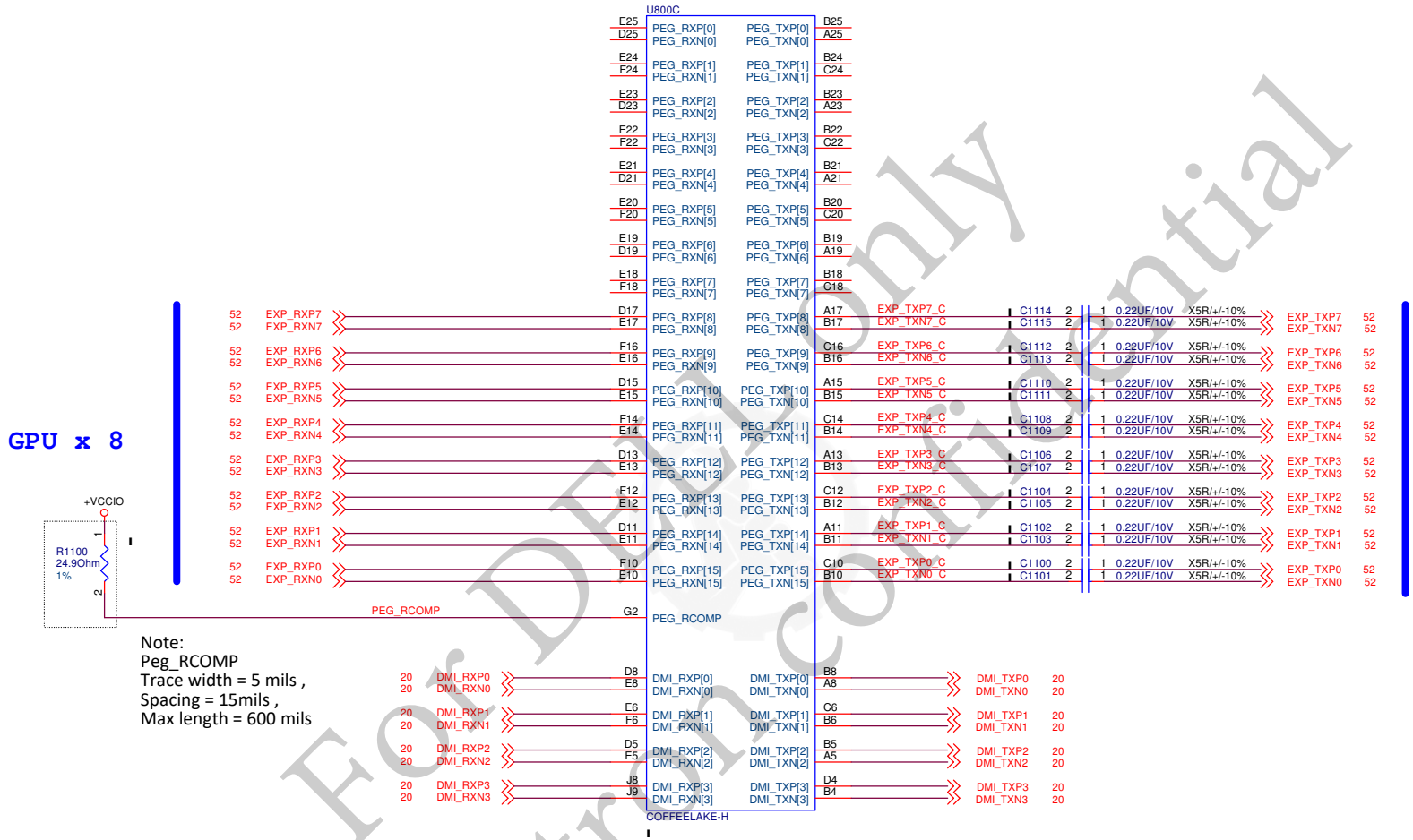
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 10 of 94



Note:
Peg_RCOMP
Trace width = 5 mils ,
Spacing = 15mils ,
Max length = 600 mils

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU PEG/DMI	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 11 of 94	

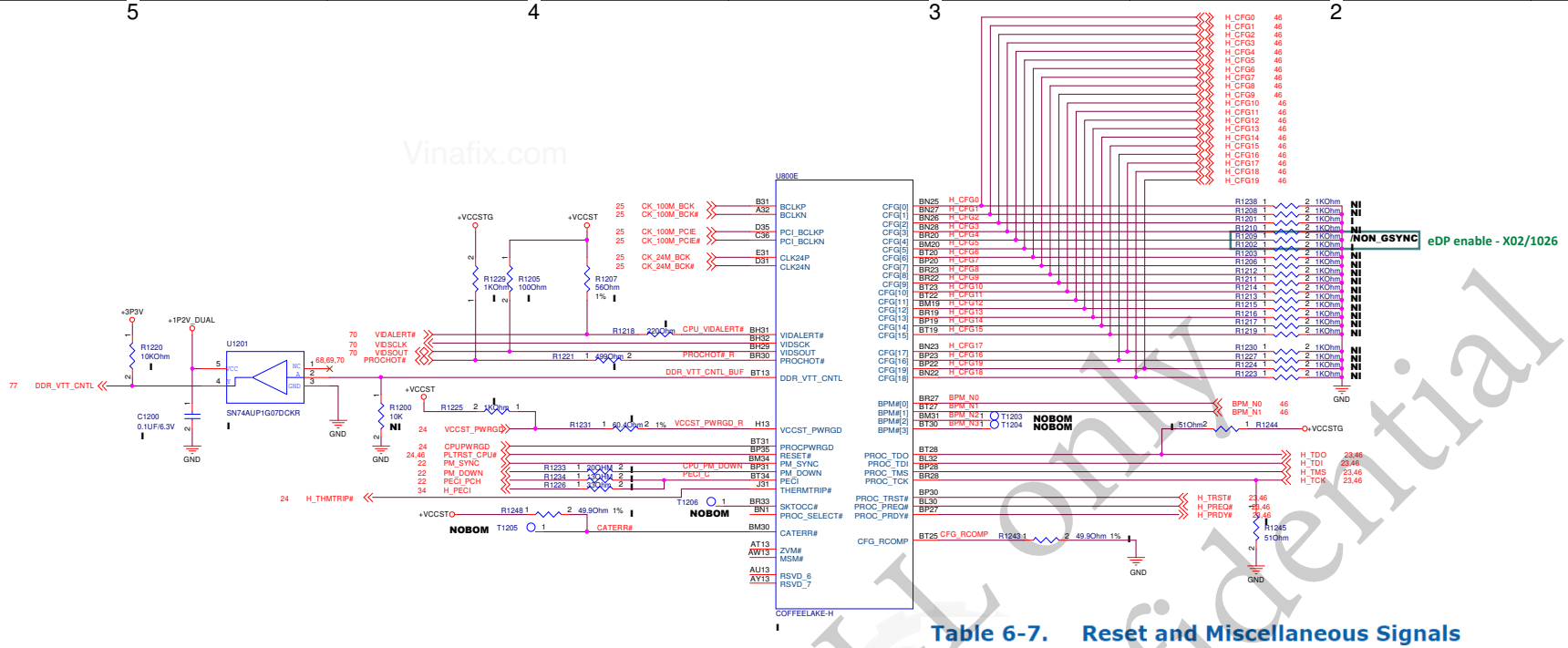


Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.

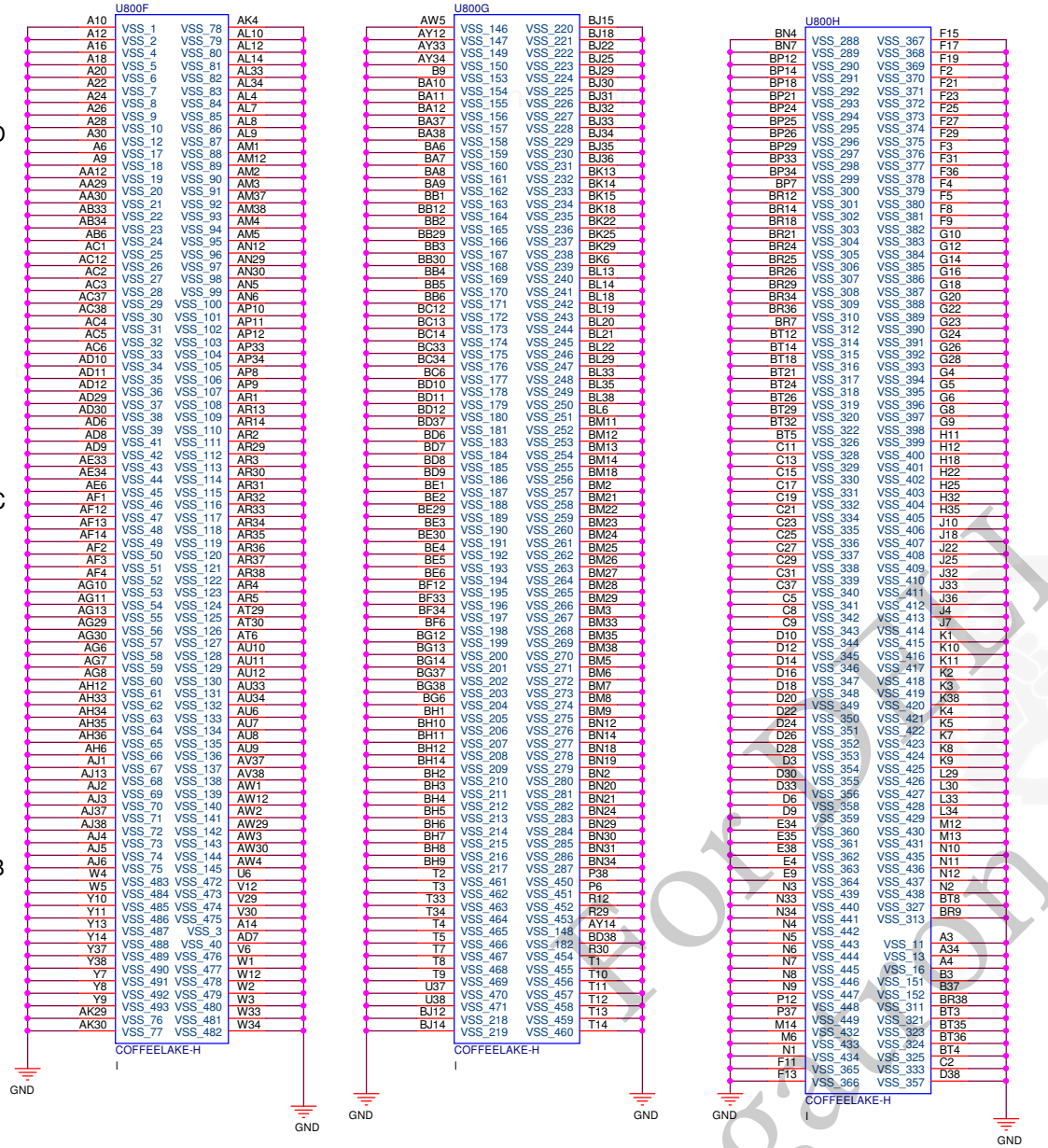
Table 6-10. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

Table 51-39. Processor/PCH Strapping Checklist (Sheet 2 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			

PEGATRON Title : CPU other
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 12 of 94



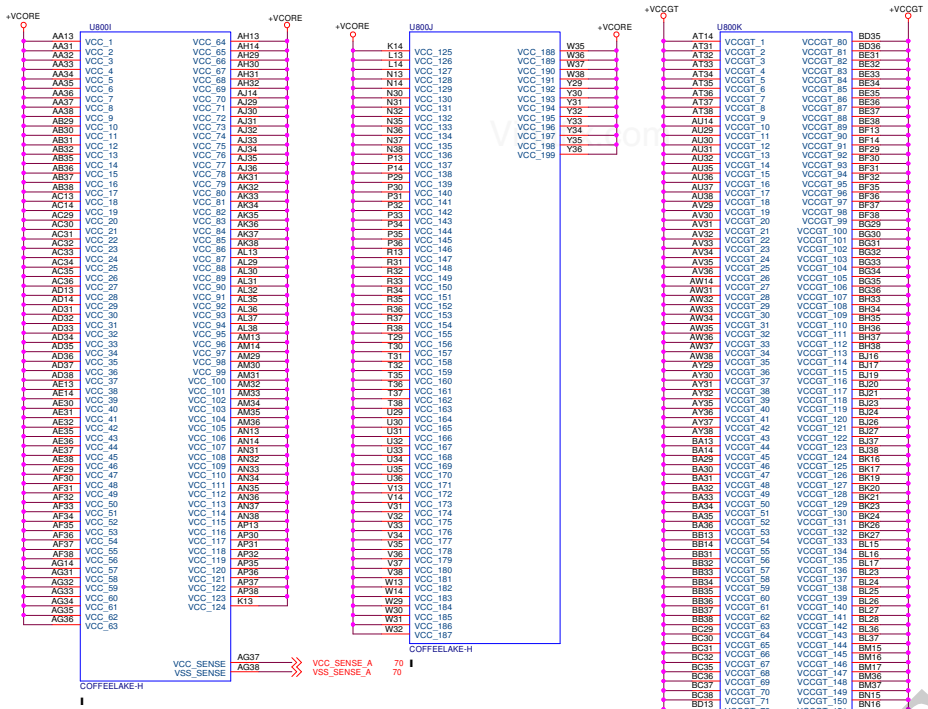
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 13 of 94



Note:

1. VCC_SENSE / VSS_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7038 / PR7043 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCC_SENSE / VSS_SENSE line resistance.

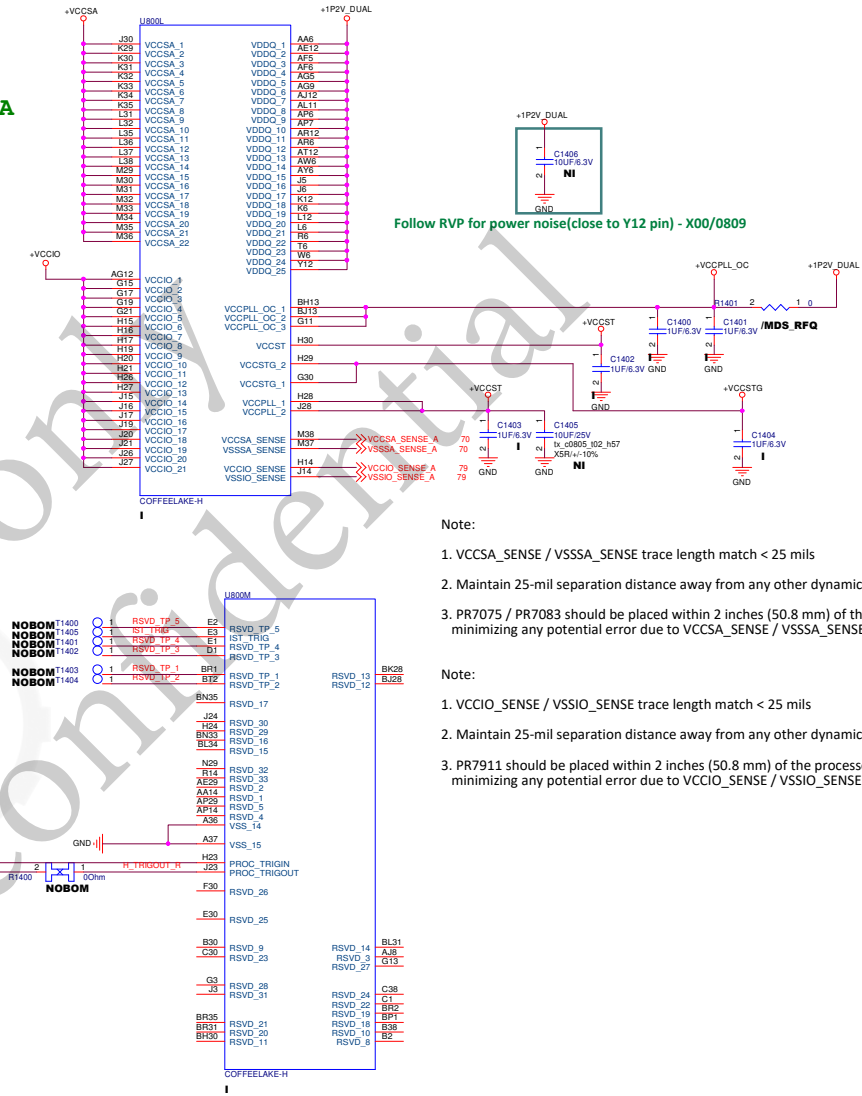
Note:

1. VSSGT_SENSE / VCCGT_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7059 / PR7067 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VSSGT_SENSE / VCCGT_SENSE line resistance.

+Vcore Max 140A
+Vccgt Max 32A
+Vccsa Max 11.1A



Note:

1. VCCSA_SENSE / VSSSA_SENSE trace length match < 25 mils

2. Maintain 25-mil separation distance away from any other dynamic signals

3. PR7075 / PR7083 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCSA_SENSE / VSSSA_SENSE line resistance.

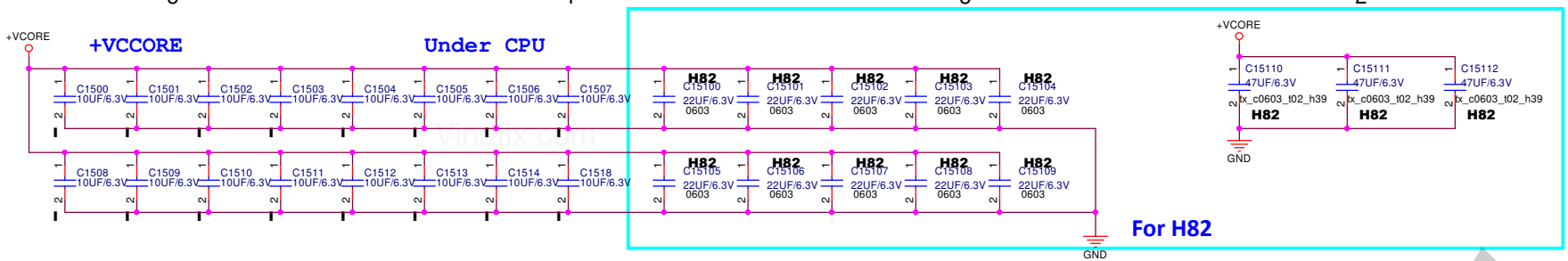
Note:

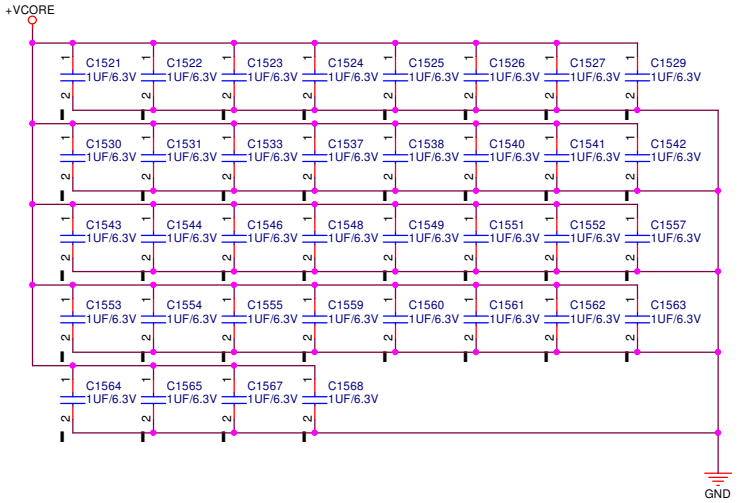
1. VCCIO_SENSE / VSSIO_SENSE trace length match < 25 mils

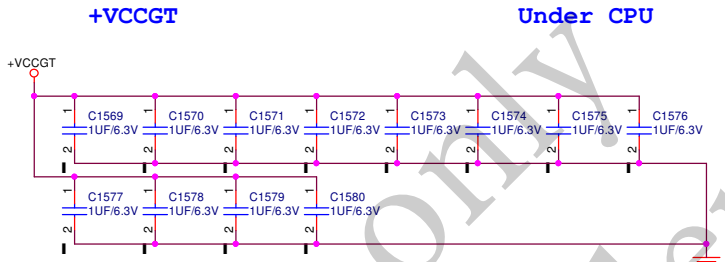
2. Maintain 25-mil separation distance away from any other dynamic signals

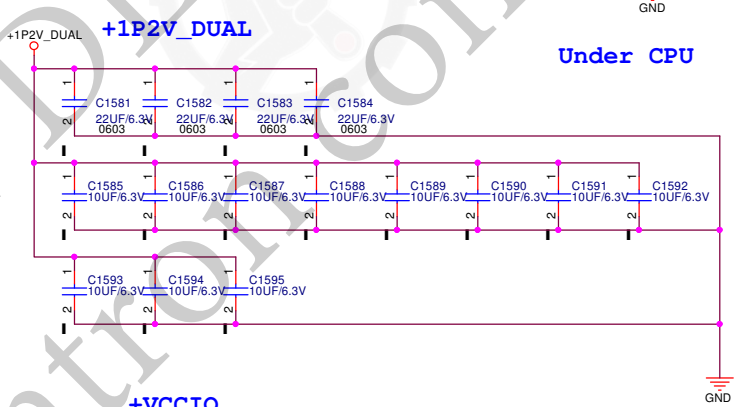
3. PR7911 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to VCCIO_SENSE / VSSIO_SENSE line resistance.

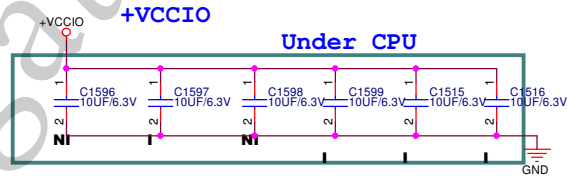
PEGATRON	Title : CPU POWER	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A2	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 14 of 94	











Change for power noise fail - X00/0717

Table 50-3. Decoupling Requirements for CFL H Processor

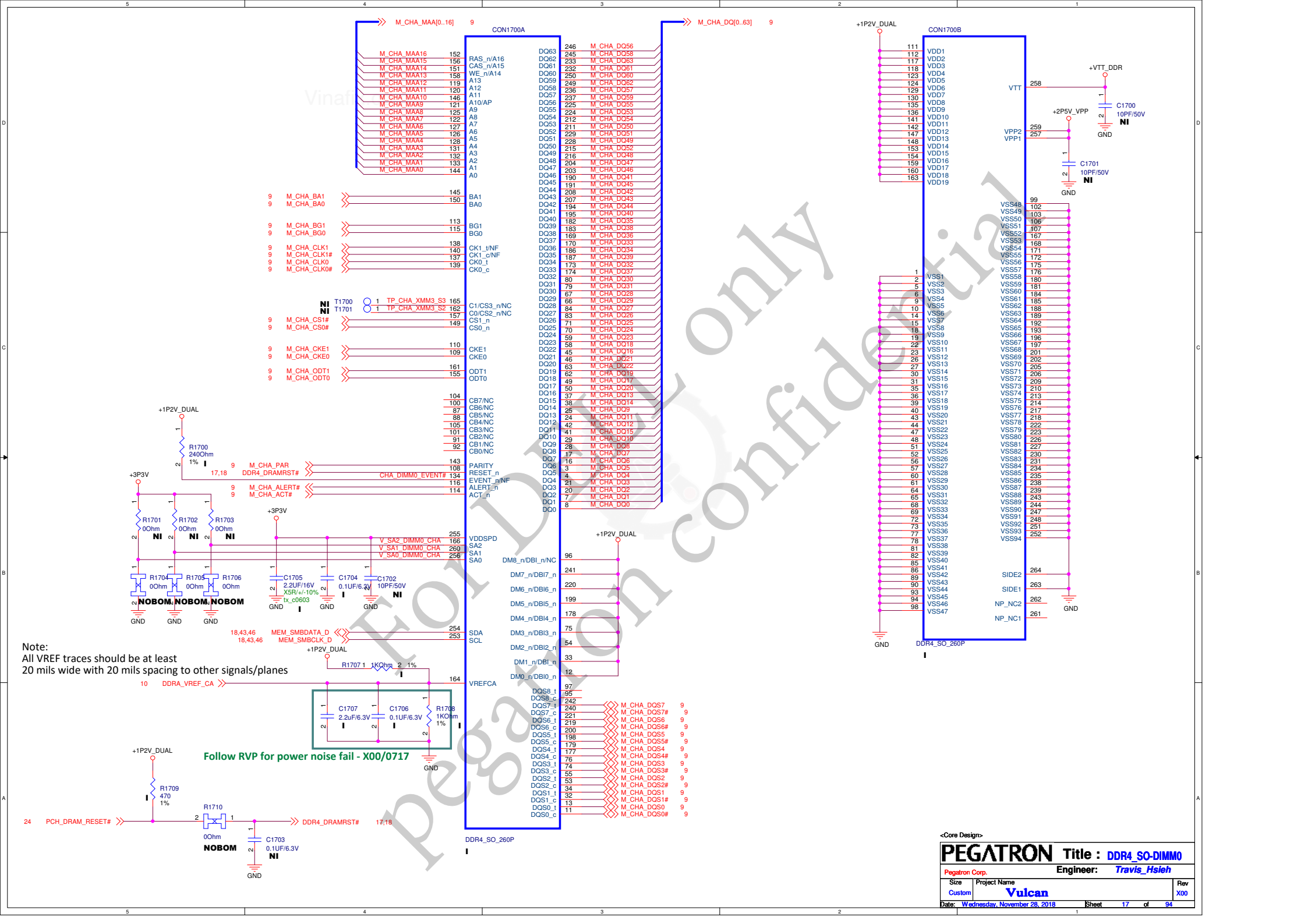
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

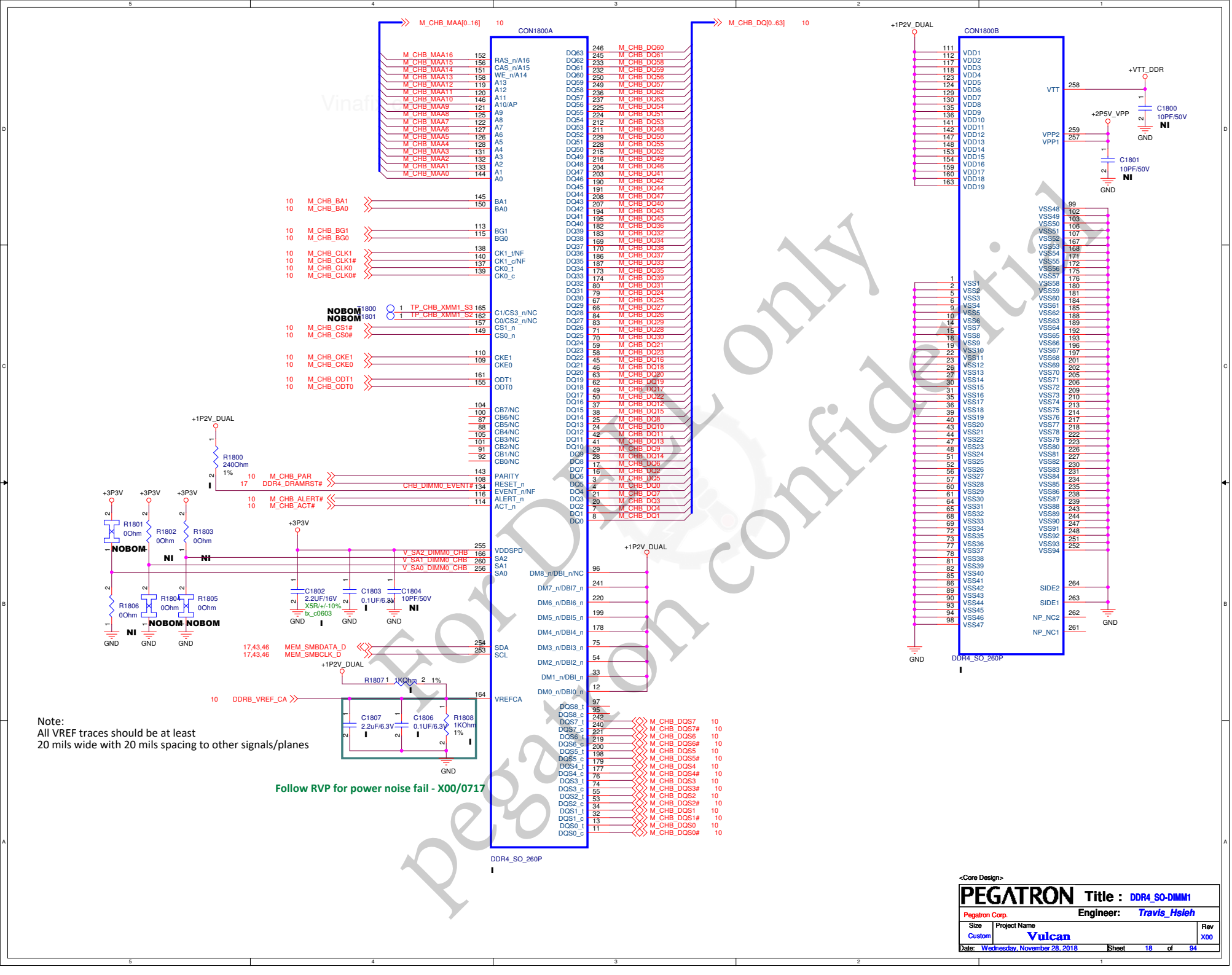
PEGATRON Title : CPU DECOUPLING
Pegatron Corp. Engineer: Travis_Hsieh
Size A3 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 | Sheet 15 of 94

Reserved Page

PEGATRON DT-MB RESTRICTED SECRET

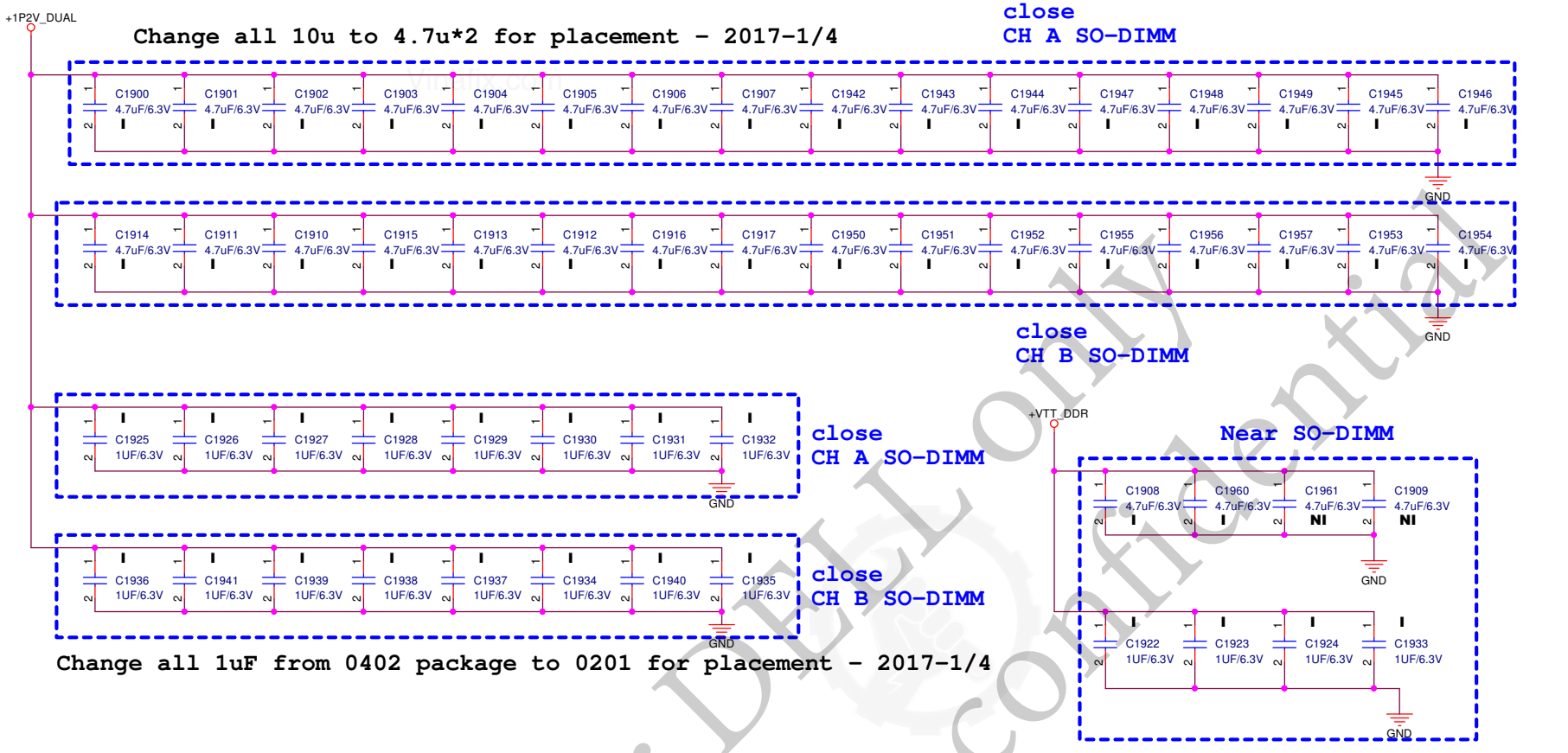
PEGATRON	Title : Reserved	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 16 of 94	


M_CHA_MAA[0..16] 9
M_CHA_DQ[0..63] 9
CON1700A
CON1700B
+1P2V_DUAL
+3P3V
+VTT_DDR
+2P5V_VPP
DDR4_SO_260P
R1700 240Ohm 1%
R1701 0Ohm NI
R1702 0Ohm NI
R1703 0Ohm NI
R1704 0Ohm NOBOM
R1705 0Ohm NOBOM
R1706 0Ohm NOBOM
R1707 1KOhm 1%
R1708 1KOhm 1%
R1709 470 1%
R1710 0Ohm NOBOM
C1700 10PF/50V NI
C1701 10PF/50V NI
C1702 10PF/50V NI
C1703 0.1UF/6.3V NI
C1704 0.1UF/6.3V
C1705 2.2UF/16V X5R/+/-10% tx_c0603
C1706 0.1UF/6.3V
C1707 2.2uF/6.3V
M_CHA_PAR
M_CHA_ALERT#
M_CHA_ACT#
CHA_DIMM0_EVENT#
DDR4_DRAMRST#
V_SA2_DIMM0_CHA
V_SA1_DIMM0_CHA
V_SA0_DIMM0_CHA
MEM_SMBDATA_D
MEM_SMBCLK_D
DDRA_VREF_CA
PCH_DRAM_RESET#
Follow RVP for power noise fail - X00/0717
Note:
All VREF traces should be at least
20 mils wide with 20 mils spacing to other signals/planes
For DELL only
pegatron confidential
<Core Design>
PEGATRON
Title : DDR4_SO-DIMM0
Pegatron Corp.
Engineer: Travis_Hsieh
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 17 of 94



Note:
All VREF traces should be at least
20 mils wide with 20 mils spacing to other signals/planes

Follow RVP for power noise fail - X00/0717

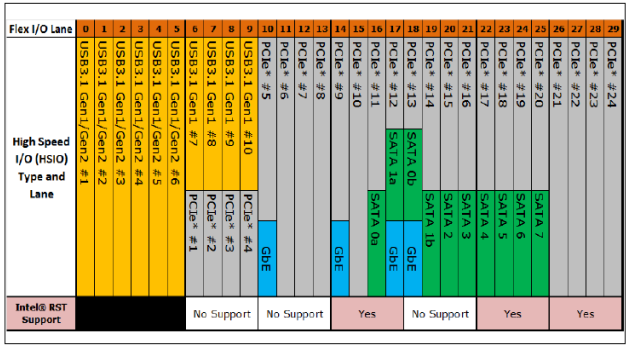


DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR DECOUPLING		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: Custom	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 19 of 94		



PCH-H Details	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3	PCIe* Controller #4	PCIe* Controller #5	PCIe* Controller #6
			Cycle Router #1		Cycle Router #3	Cycle Router #2
Flex I/O Lane #	6 7 8 9	10 11 12 13	14 15 16 17	18 15 20 21	22 23 24 25	26 27 28 29
PCIe* Lane #	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
HM370 1x4			RP 9	RP 13	RP 17	RP 21
HM370 1x4 LR			RP 9	RP 13	RP 17	RP 21
HM370 2x2			RP 9 RP 11	RP 13 RP 15	RP 17 RP 19	RP 21 RP 23
HM370 1x2+2x1			RP 9 RP 11 RP 12	RP 13 RP 15 RP 16	RP 17 RP 19 RP 20	RP 21 RP 23 RP 24
HM370 2x1+1x2			RP 12 RP 11 RP 9	RP 16 RP 15 RP 13	RP 20 RP 19 RP 17	RP 24 RP 23 RP 21
HM370 4x1			RP 9 RP 10 RP 11 RP 12	RP 13 RP 14 RP 15 RP 16	RP 17 RP 18 RP 19 RP 20	RP 21 RP 22 RP 23 RP 24

U2000A

DMI

11 DMI_TXN0 — K34 DMI0_RXN
11 DMI_TXP0 — J35 DMI0_RXP
11 DMI_RXN0 — C33 DMI0_TXN
11 DMI_RXP0 — B33 DMI0_TXP

11 DMI_TXN1 — G33 DMI1_RXN
11 DMI_TXP1 — F34 DMI1_RXP
11 DMI_RXN1 — C32 DMI1_TXN
11 DMI_RXP1 — B32 DMI1_TXP

11 DMI_TXN2 — K32 DMI2_RXN
11 DMI_TXP2 — J32 DMI2_RXP
11 DMI_RXN2 — C31 DMI2_TXN
11 DMI_RXP2 — B31 DMI2_TXP

11 DMI_TXN3 — G30 DMI3_RXN
11 DMI_TXP3 — F30 DMI3_RXP
11 DMI_RXN3 — C29 DMI3_TXN
11 DMI_RXP3 — B29 DMI3_TXP

M29 DMI4_RXN
K29 DMI4_RXP
E28 DMI4_TXN
D29 DMI4_TXP

M26 DMI5_RXN
L26 DMI5_RXP
C27 DMI5_TXN
B27 DMI5_TXP

G26 DMI6_RXN
F26 DMI6_RXP
B26 DMI6_TXN
C26 DMI6_TXP

R24 DMI7_RXN
P24 DMI7_RXP
B25 DMI7_TXN
A25 DMI7_TXP

PCIE/USB/SATA

B17 PCIE1_TXP/USB31_7_TXP
A17 PCIE1_TXN/USB31_7_TXN
F16 PCIE1_RXP/USB31_7_RXP
G17 PCIE1_RXN/USB31_7_RXN

C18 PCIE2_TXP/USB31_8_TXP
B18 PCIE2_TXN/USB31_8_TXN
P21 PCIE2_RXP/USB31_8_RXP
R21 PCIE2_RXN/USB31_8_RXN

C19 PCIE3_TXP/USB31_9_TXP
B19 PCIE3_TXN/USB31_9_TXN
J18 PCIE3_RXP/USB31_9_RXP
K18 PCIE3_RXN/USB31_9_RXN

C20 PCIE4_TXP/USB31_10_TXP
D20 PCIE4_TXN/USB31_10_TXN
R18 PCIE4_RXP/USB31_10_RXP
N18 PCIE4_RXN/USB31_10_RXN

A22 PCIE5_TXP
B21 PCIE5_TXN
G20 PCIE5_RXP
F20 PCIE5_RXN

C21 PCIE6_TXP
D21 PCIE6_TXN
J21 PCIE6_RXP
K21 PCIE6_RXN

B23 PCIE7_TXP
C23 PCIE7_TXN
J24 PCIE7_RXP
L24 PCIE7_RXN

C24 PCIE8_TXP
B24 PCIE8_TXN
G24 PCIE8_RXP
F24 PCIE8_RXN

D34 PCIE9_TXP
C34 PCIE9_TXN
F36 PCIE9_RXP
G36 PCIE9_RXN

B35 PCIE10_TXP
C35 PCIE10_TXN
J37 PCIE10_RXP
K37 PCIE10_RXN

C36 PCIE11_TXP/SATA0A_TXP
B36 PCIE11_TXN/SATA0A_TXN
F39 PCIE11_RXP/SATA0A_RXP
G38 PCIE11_RXN/SATA0A_RXN

E37 PCIE12_TXP/SATA1A_TXP
D38 PCIE12_TXN/SATA1A_TXN
J41 PCIE12_RXP/SATA_1A_RXP
H42 PCIE12_RXN/SATA1A_RXN

PCH-H

M.2 PCIE X4 #1

31 PCIE9_SSD1_TXP
31 PCIE9_SSD1_TXN
31 PCIE9_SSD1_RXP
31 PCIE9_SSD1_RXN

31 PCIE10_SSD1_TXP
31 PCIE10_SSD1_TXN
31 PCIE10_SSD1_RXP
31 PCIE10_SSD1_RXN

31 PCIE11_SSD1_TXP
31 PCIE11_SSD1_TXN
31 PCIE11_SSD1_RXP
31 PCIE11_SSD1_RXN

31 PCIE12_SATA1A_SSD1_TXP
31 PCIE12_SATA1A_SSD1_TXN
31 PCIE12_SATA1A_SSD1_RXP
31 PCIE12_SATA1A_SSD1_RXN

USB2.0

J2 USB2P_1 — IPD 14~24KOHM — USBP1 44 — IO USB3.1(Type-A_1)
J3 USB2N_1 — IPD 14~24KOHM — USBN1 44

N15 USB2P_2 — IPD 14~24KOHM — USBP2 38 — RIGHT USB3.1(Type-A) -Power share
N13 USB2N_2 — IPD 14~24KOHM — USBN2 38

K3 USB2P_3 — IPD 14~24KOHM — USBP3 38 — USB3.1(Type-A Rear)
K4 USB2N_3 — IPD 14~24KOHM — USBN3 38

L9 USB2P_4 — IPD 14~24KOHM — USBP4 30 — TBT USB3.1(Type-C)
M10 USB2N_4 — IPD 14~24KOHM — USBN4 30

L2 USB2P_5 — IPD 14~24KOHM — USBP5 48 — WEBCAM
M1 USB2N_5 — IPD 14~24KOHM — USBN5 48

K6 USB2P_6 — IPD 14~24KOHM — USBP6 44 — Card Reader
K7 USB2N_6 — IPD 14~24KOHM — USBN6 44

L3 USB2P_7 — IPD 14~24KOHM — 1 — T2000 NOBOM
L4 USB2N_7 — IPD 14~24KOHM — 1 — T2001 NOBOM

G5 USB2P_8 — IPD 14~24KOHM
G4 USB2N_8 — IPD 14~24KOHM

N8 USB2P_9 — IPD 14~24KOHM — USBP9 44 — Finger Print Reader
M6 USB2N_9 — IPD 14~24KOHM — USBN9 44

H2 USB2P_10 — IPD 14~24KOHM
H3 USB2N_10 — IPD 14~24KOHM

P9 USB2P_11 — IPD 14~24KOHM — USBP11 50 — ELC
R10 USB2N_11 — IPD 14~24KOHM — USBN11 50

G2 USB2P_12 — IPD 14~24KOHM
G1 USB2N_12 — IPD 14~24KOHM

N2 USB2P_13 — IPD 14~24KOHM
N3 USB2N_13 — IPD 14~24KOHM

F6 USB2P_14 — IPD 14~24KOHM — USBP14 33 — M.2 2230 WLAN KEY-E
E5 USB2N_14 — IPD 14~24KOHM — USBN14 33

Change from port7 due to INTEL CNVi uggest - X01/0801

USB3.1

F7 USB31_1_TXP — USB3_TX_P1
F9 USB31_1_TXN — USB3_TX_N1
C11 USB31_1_RXP
D11 USB31_1_RXN

USB3_TX_P1 44 — IO USB3.1(Type-A_1)
USB3_TX_N1 44
USB3_RX_P1 44
USB3_RX_N1 44

D4 USB31_2_TXP — USB3_TX_P2_C — C2002 1 — 2 0.1UF/6.3V
C3 USB31_2_TXN — USB3_TX_N2_C — C2003 1 — 2 0.1UF/6.3V
C9 USB31_2_RXP
B9 USB31_2_RXN

USB3_TX_P2 38
USB3_TX_N2 38 — RIGHT USB3.1(Type-A) -Power share
USB3_RX_P2 38
USB3_RX_N2 38

G12 USB31_3_TXP — USB3_TX_P3_C — C2004 1 — 2 0.1UF/6.3V
F11 USB31_3_TXN — USB3_TX_N3_C — C2005 1 — 2 0.1UF/6.3V
C10 USB31_3_RXP
B10 USB31_3_RXN

USB3_TX_P3 38 — USB3.1(Type-A Rear)
USB3_TX_N3 38
USB3_RX_P3 38
USB3_RX_N3 38

C14 USB31_4_TXP
B14 USB31_4_TXN
J15 USB31_4_RXP
K16 USB31_4_RXN

B15 USB31_5_TXP
C15 USB31_5_TXN
K13 USB31_5_RXP
J13 USB31_5_RXN

C16 USB31_6_TXP
C17 USB31_6_TXN
F14 USB31_6_RXP
G14 USB31_6_RXN

G3 USB2_ID
F3 USB2_VBUSSENSE — USB2_VBUSSENSE

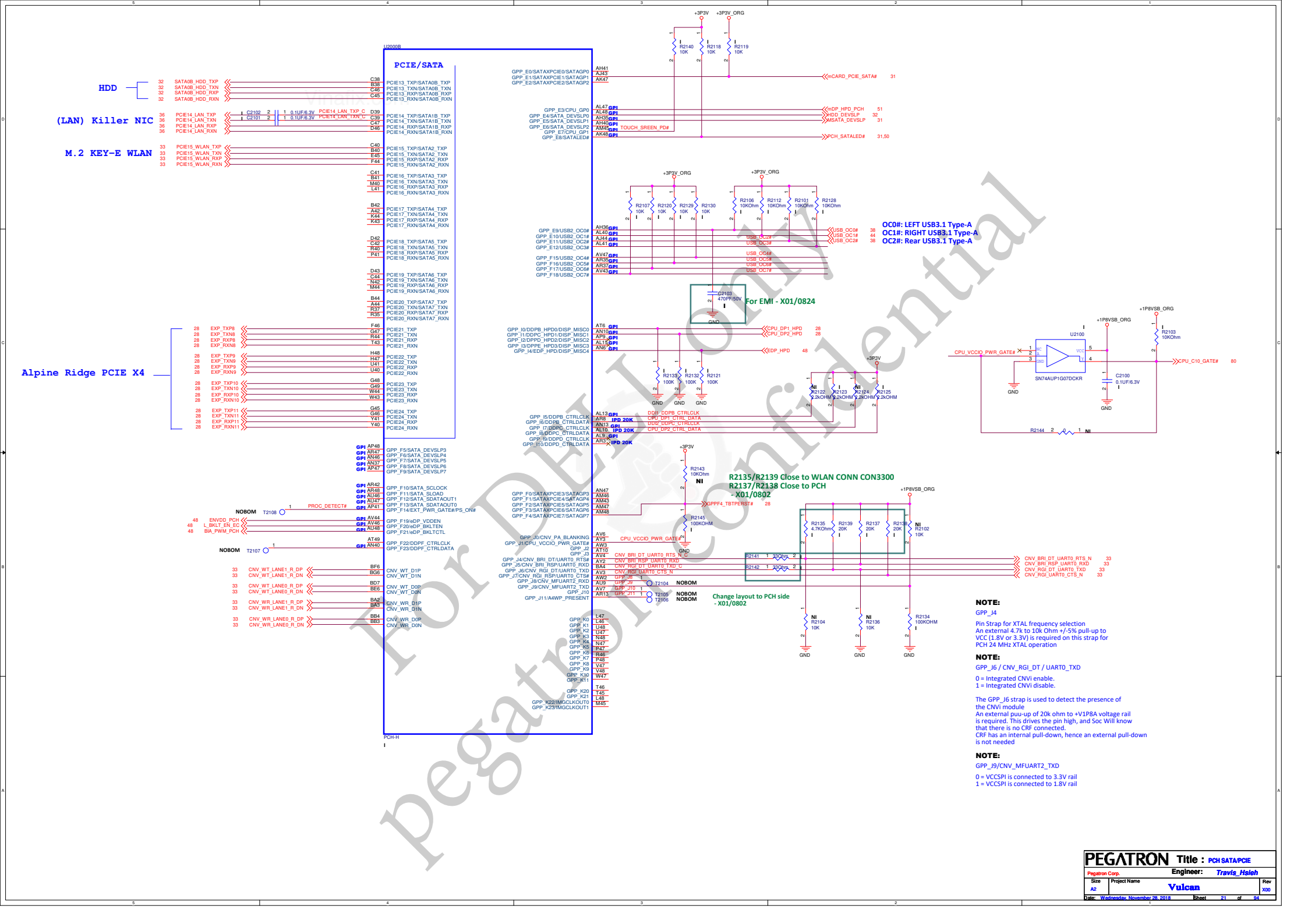
R2000 1K NI — GND
R2001 0Ohm NOBOM — GND

PEGATRON Title : PCH DMI_PCIE_USB_SATA

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 20 of 94


HDD
(LAN) Killer NIC
M.2 KEY-E WLAN
Alpine Ridge PCIE X4
U2000B
PCIE/SATA
PCH-H
SATA0B_HDD_TXP
SATA0B_HDD_TXN
SATA0B_HDD_RXP
SATA0B_HDD_RXN
PCIE14_LAN_TXP
PCIE14_LAN_TXN
PCIE14_LAN_RXP
PCIE14_LAN_RXN
PCIE14_LAN_TXP_C
PCIE14_LAN_TXN_C
0.1UF/6.3V
PCIE15_WLAN_TXP
PCIE15_WLAN_TXN
PCIE15_WLAN_RXP
PCIE15_WLAN_RXN
EXP_TXP8
EXP_TXN8
EXP_RXP8
EXP_RXN8
EXP_TXP9
EXP_TXN9
EXP_RXP9
EXP_RXN9
EXP_TXP10
EXP_TXN10
EXP_RXP10
EXP_RXN10
EXP_TXP11
EXP_TXN11
EXP_RXP11
EXP_RXN11
PROC_DETECT#
ENVDD_PCH
L_BKLT_EN_EC
BIA_PWM_PCH
CNV_WT_LANE1_R_DP
CNV_WT_LANE1_R_DN
CNV_WT_LANE0_R_DP
CNV_WT_LANE0_R_DN
CNV_WR_LANE1_R_DP
CNV_WR_LANE1_R_DN
CNV_WR_LANE0_R_DP
CNV_WR_LANE0_R_DN
mCARD_PCIE_SATA#
mDP_HPD_PCH
HDD_DEVSLP
mSATA_DEVSLP
TOUCH_SREEN_PD#
PCH_SATALED#
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4#
USB_OC5#
USB_OC6#
USB_OC7#
OC0#: LEFT USB3.1 Type-A
OC1#: RIGHT USB3.1 Type-A
OC2#: Rear USB3.1 Type-A
For EMI - X01/0824
CPU_DP1_HPD
CPU_DP2_HPD
EDP_HPD
DDI_DDPB_CTRLCLK
CPU_DP1_CTRL_DATA
DDPC_DDPC_CTRLCLK
CPU_DP2_CTRL_DATA
GPPF4_TBTPERST#
R2135/R2139 Close to WLAN CONN CON3300
R2137/R2138 Close to PCH
- X01/0802
CPU_VCCIO_PWR_GATE#
CNV_BRI_DT_UART0_RTS_N
CNV_BRI_RSP_UART0_RXD
CNV_BRI_DT_UART0_TXD_C
CNV_RGI_UART0_CTS_N
Change layout to PCH side
- X01/0802
CPU_C10_GATE#
SN74AUP1G07DCKR
NOTE:
GPP_J4
Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation
NOTE:
GPP_J6 / CNV_RGI_DT / UART0_TXD
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
The GPP_J6 strap is used to detect the presence of the CNVi module
An external puu-up of 20k ohm to +V1P8A voltage rail is required. This drives the pin high, and Soc Will know that there is no CRF connected.
CRF has an internal pull-down, hence an external pull-down is not needed
NOTE:
GPP_J9/CNV_MFUART2_TXD
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
PEGATRON
Title : PCH SATA/PCIE
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 21 of 94
For DEL only
pegatron confidential

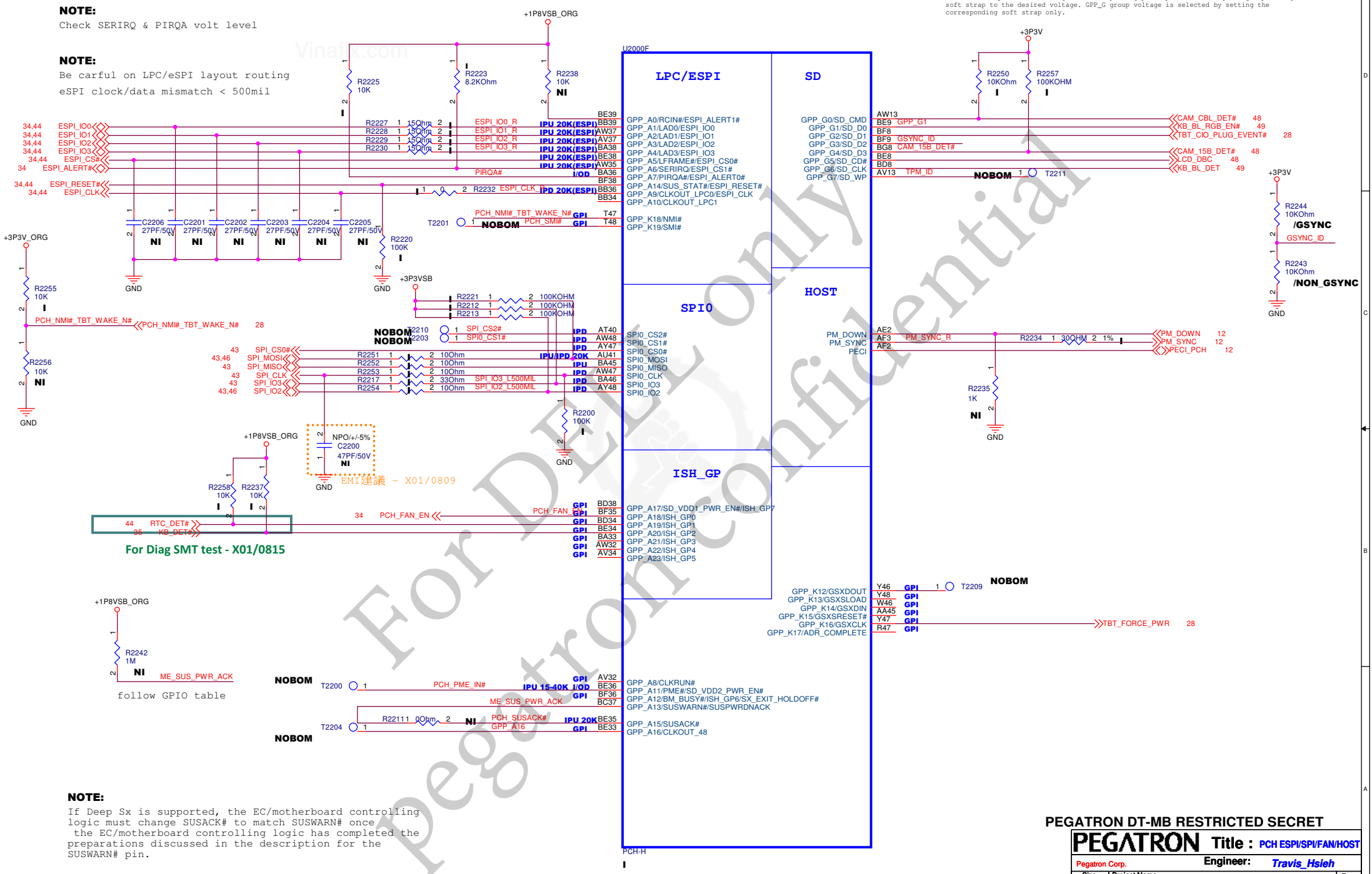
NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:
Check GPP_A0 power well

NOTE: GPP_G 1.8V for GPU
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

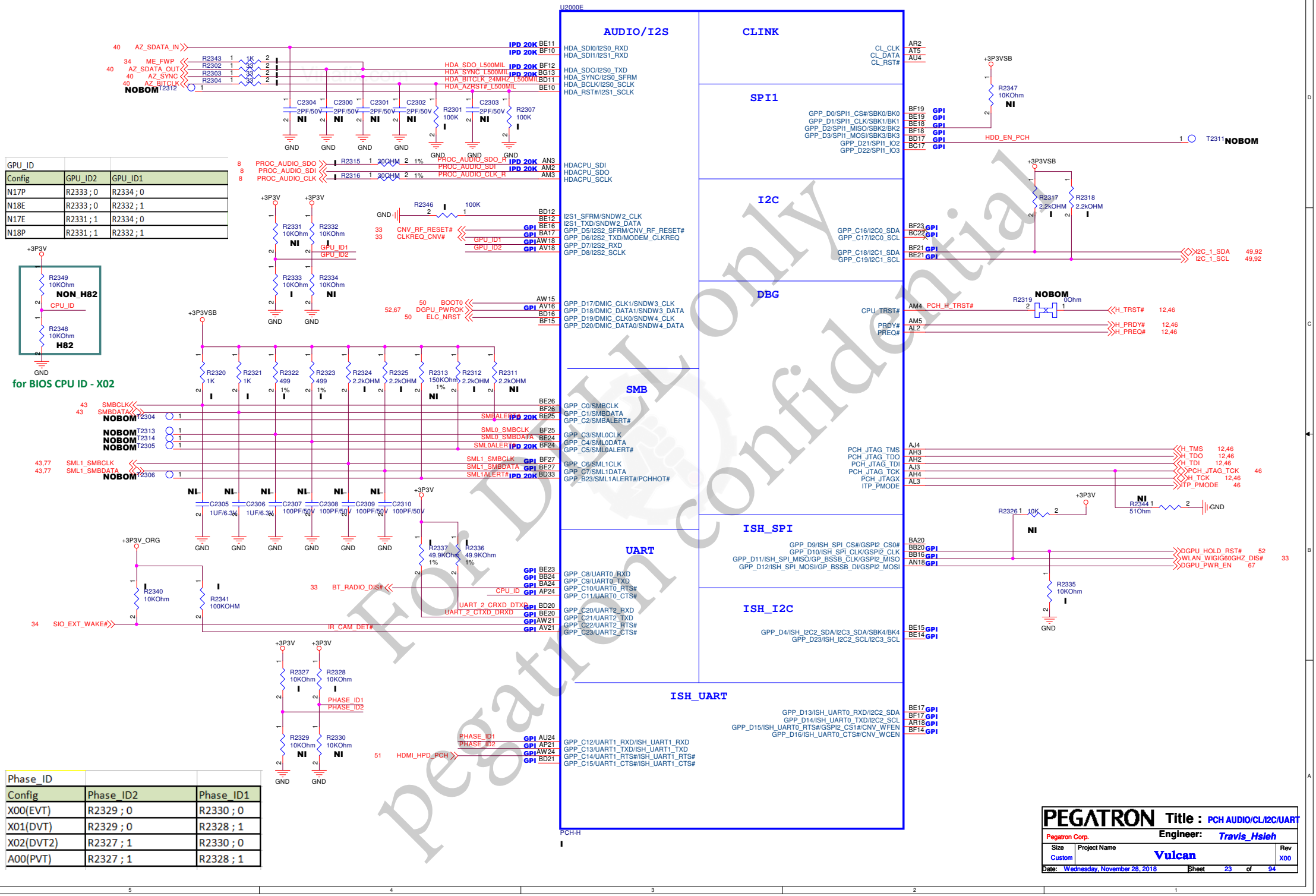


For Diag SMT test - X01/0815

NOTE:
If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH ESPI/SPI/FAN/HOST	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 22 of 94	



GPU_ID		
Config	GPU_ID2	GPU_ID1
N17P	R2333 ; 0	R2334 ; 0
N18E	R2333 ; 0	R2332 ; 1
N17E	R2331 ; 1	R2334 ; 0
N18P	R2331 ; 1	R2332 ; 1

Phase_ID		
Config	Phase_ID2	Phase_ID1
X00(EVT)	R2329 ; 0	R2330 ; 0
X01(DVT)	R2329 ; 0	R2328 ; 1
X02(DVT2)	R2327 ; 1	R2330 ; 0
A00(PVT)	R2327 ; 1	R2328 ; 1

PEGATRON Title : PCH AUDIO/CL/I2C/UART

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 23 of 94

NOTE:
GPP_B22/GSPI1_MOSI

This Signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI0_MOSI/GPP_B18

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:
GPP_B14 / SPKR

0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

NOTE:
GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

for EA - X01/0830

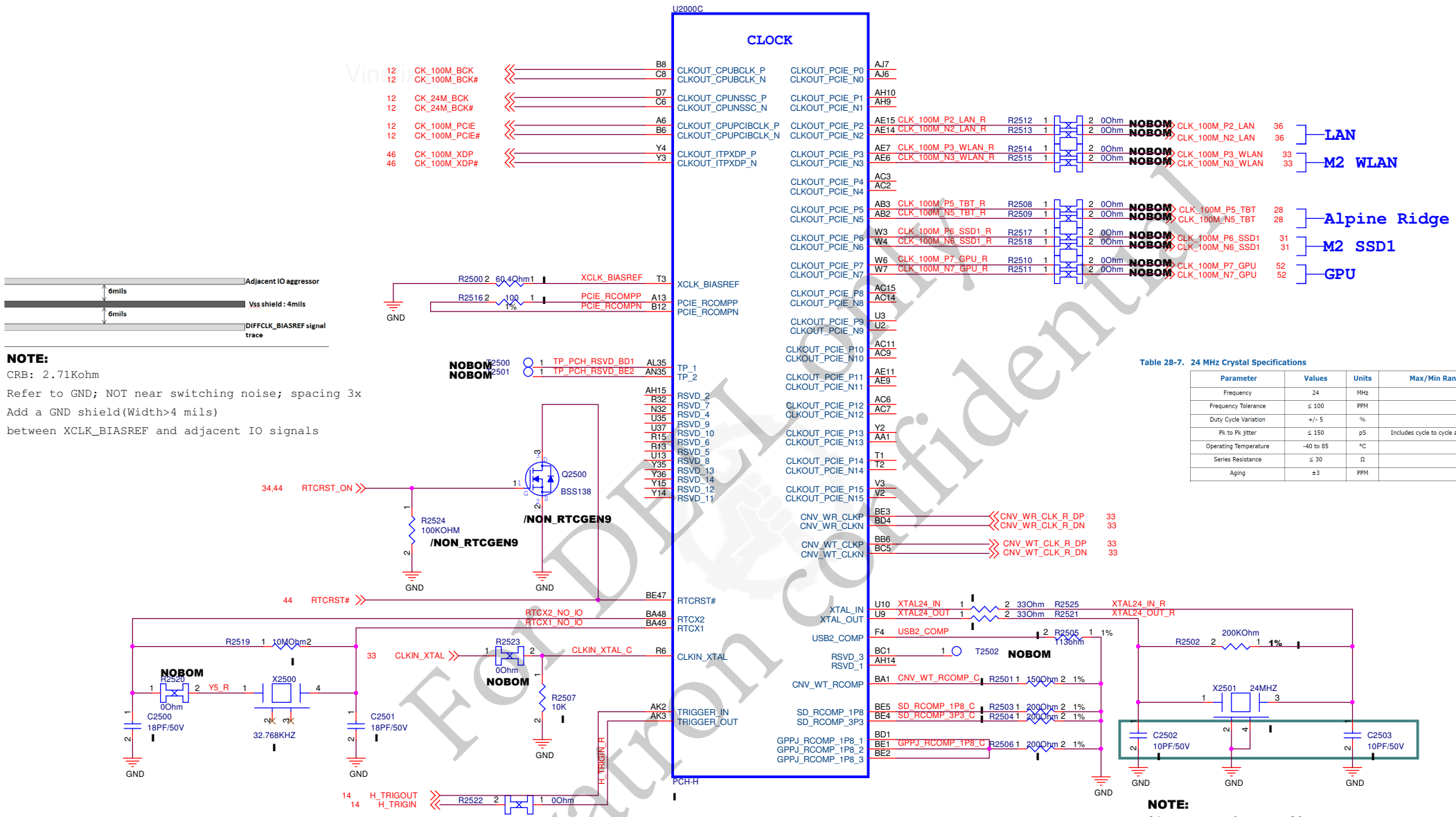
for EA - X01/0830

for EA - X02/1121

for EA - X01/0830

for sequence - X01/0830

PEGATRON	Title : PCH SML/I2C/MISC		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 24 of 94		



NOTE:

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

between XCLK_BIASREF and adjacent IO signals

Table 28-7. 24 MHz Crystal Specifications

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

NOTE:

24MHz crystal : ESR 30 OHM

follow vendor test report - X01/0829

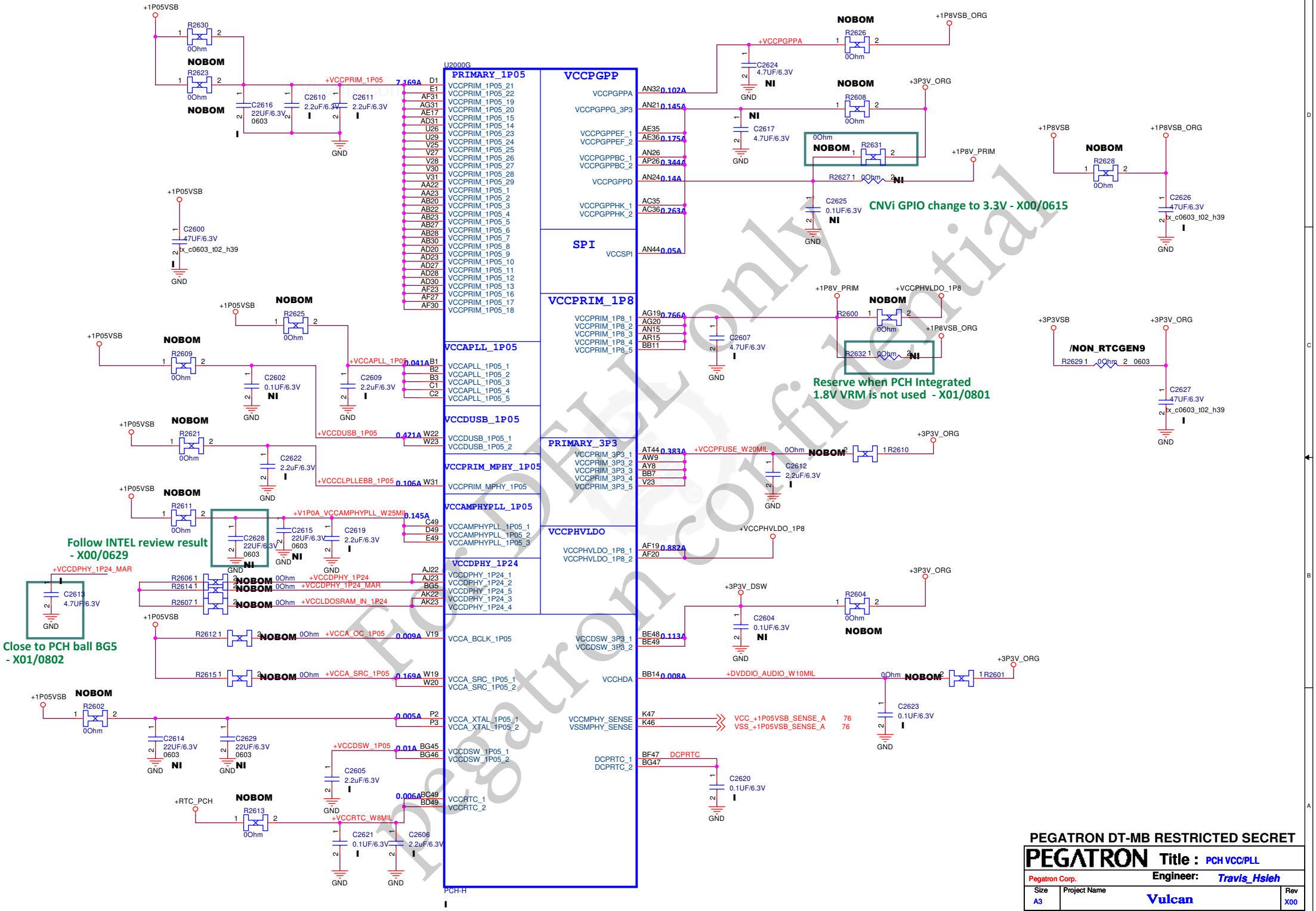
PEGATRON DT-MB RESTRICTED SECRET

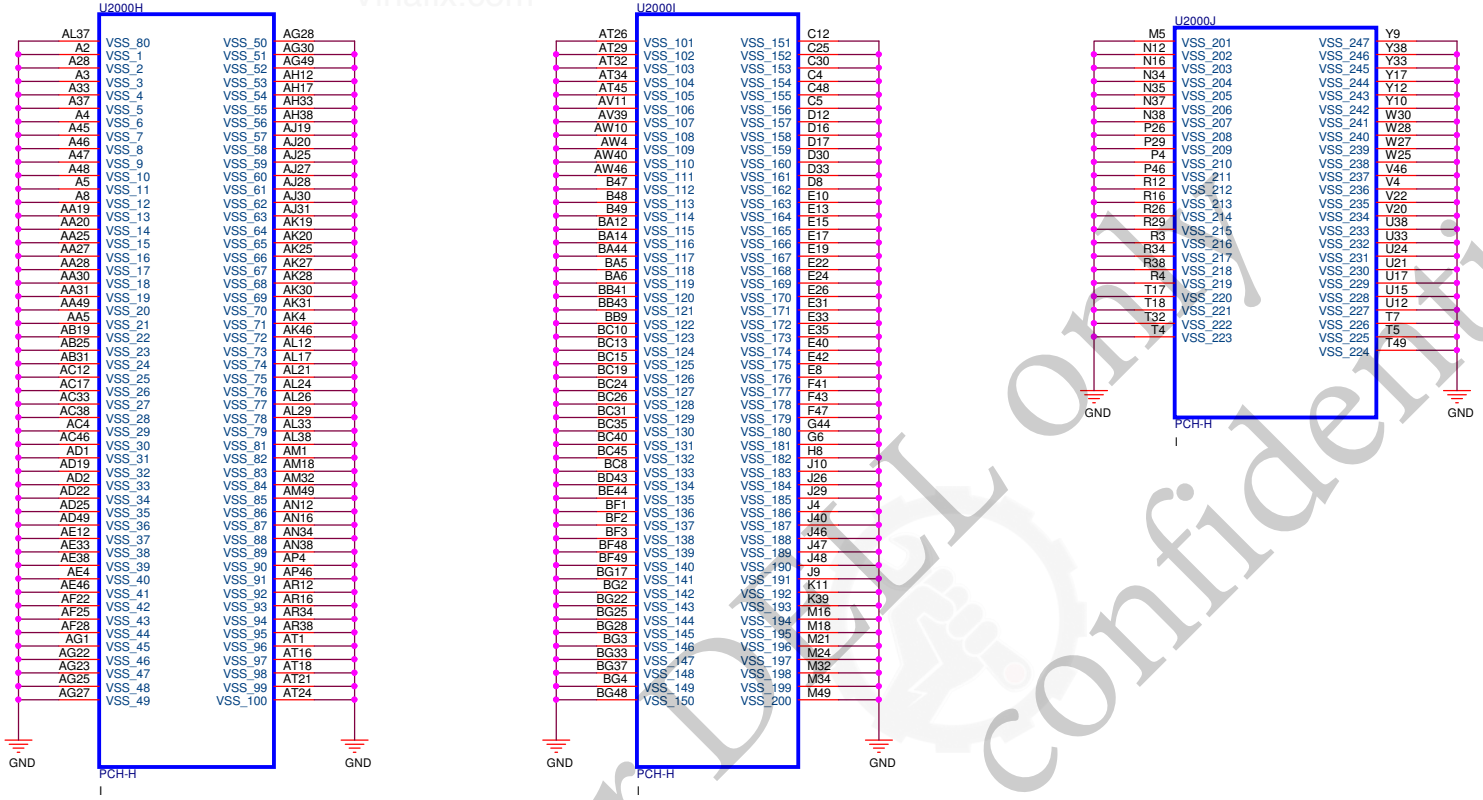
PEGATRON Title : PCH CLOCK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

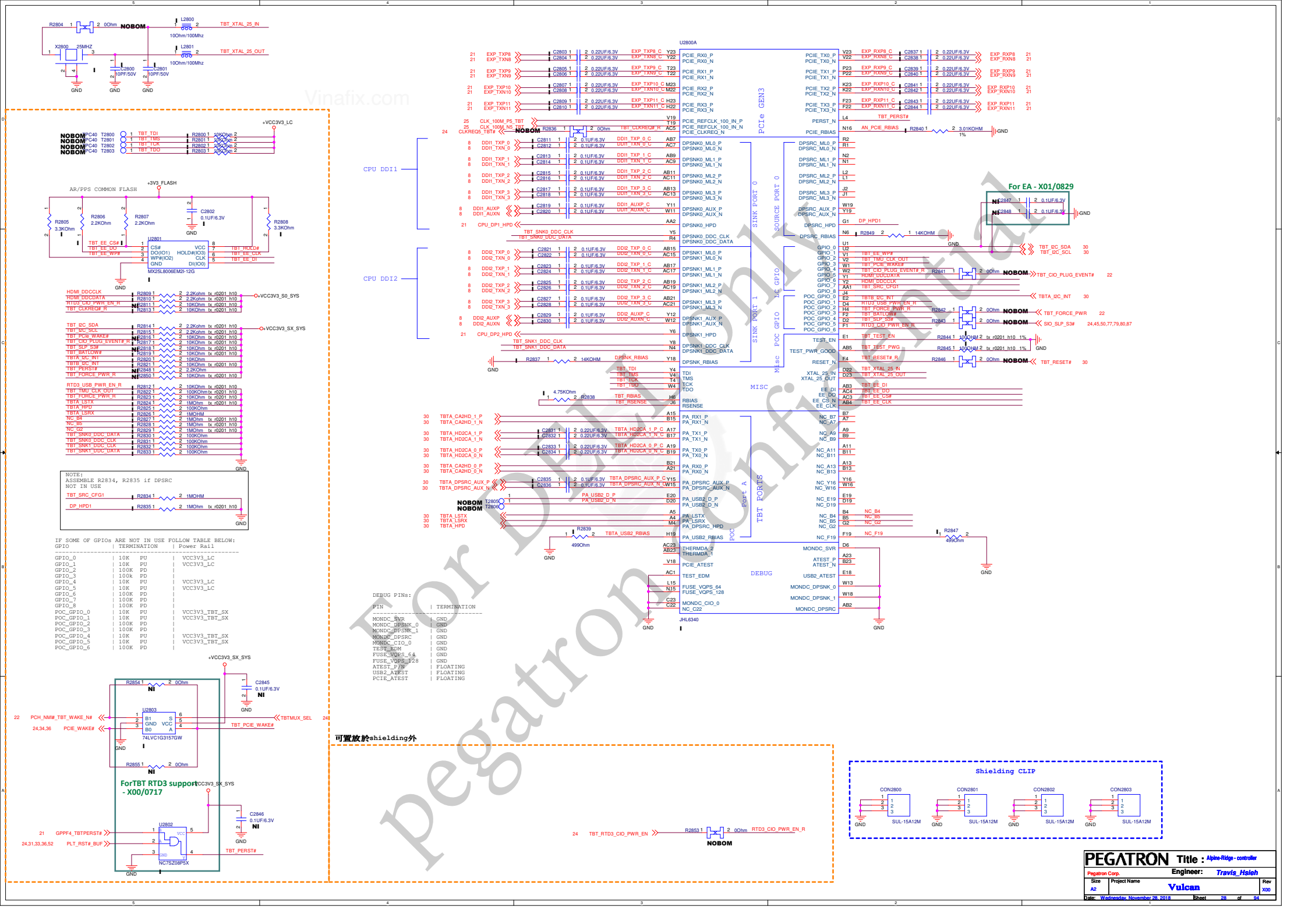
Date: Wednesday, November 28, 2018 Sheet 25 of 94

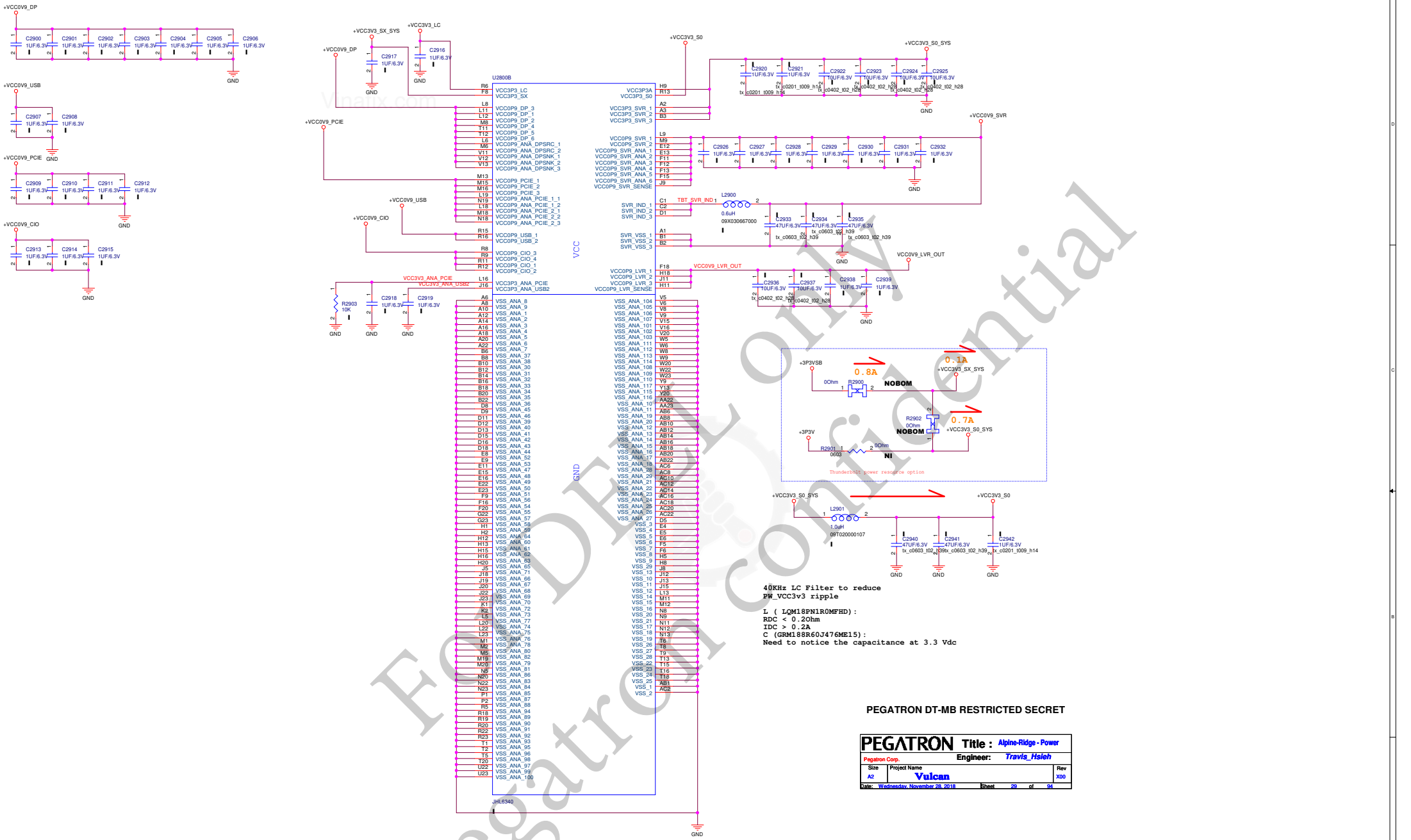

U2000G
PRIMARY_1P05
VCCPRIM_1P05_21
VCCPRIM_1P05_22
VCCPRIM_1P05_19
VCCPRIM_1P05_20
VCCPRIM_1P05_15
VCCPRIM_1P05_14
VCCPRIM_1P05_23
VCCPRIM_1P05_24
VCCPRIM_1P05_25
VCCPRIM_1P05_26
VCCPRIM_1P05_27
VCCPRIM_1P05_28
VCCPRIM_1P05_29
VCCPRIM_1P05_1
VCCPRIM_1P05_2
VCCPRIM_1P05_3
VCCPRIM_1P05_4
VCCPRIM_1P05_5
VCCPRIM_1P05_6
VCCPRIM_1P05_7
VCCPRIM_1P05_8
VCCPRIM_1P05_9
VCCPRIM_1P05_10
VCCPRIM_1P05_11
VCCPRIM_1P05_12
VCCPRIM_1P05_13
VCCPRIM_1P05_16
VCCPRIM_1P05_17
VCCPRIM_1P05_18
VCCAPLL_1P05
VCCAPLL_1P05_1
VCCAPLL_1P05_2
VCCAPLL_1P05_3
VCCAPLL_1P05_4
VCCAPLL_1P05_5
VCCDUSB_1P05
VCCDUSB_1P05_1
VCCDUSB_1P05_2
VCCPRIM_MPHY_1P05
VCCPRIM_MPHY_1P05
VCCAMPHYPLL_1P05
VCCAMPHYPLL_1P05_1
VCCAMPHYPLL_1P05_2
VCCAMPHYPLL_1P05_3
VCCDPHY_1P24
VCCDPHY_1P24_1
VCCDPHY_1P24_2
VCCDPHY_1P24_5
VCCDPHY_1P24_3
VCCDPHY_1P24_4
VCCA_BCLK_1P05
VCCA_SRC_1P05_1
VCCA_SRC_1P05_2
VCCA_XTAL_1P05_1
VCCA_XTAL_1P05_2
VCCDSW_1P05_1
VCCDSW_1P05_2
VCCRTC_1
VCCRTC_2
PCH-H
VCCPGPP
VCCPGPPA
VCCPGPPG_3P3
VCCPGPPEF_1
VCCPGPPEF_2
VCCPGPPBC_1
VCCPGPPBC_2
VCCPGPPD
VCCPGPPHK_1
VCCPGPPHK_2
SPI
VCCSPI
VCCPRIM_1P8
VCCPRIM_1P8_1
VCCPRIM_1P8_2
VCCPRIM_1P8_3
VCCPRIM_1P8_4
VCCPRIM_1P8_5
PRIMARY_3P3
VCCPRIM_3P3_1
VCCPRIM_3P3_2
VCCPRIM_3P3_3
VCCPRIM_3P3_4
VCCPRIM_3P3_5
VCCPHVLDO
VCCPHVLDO_1P8_1
VCCPHVLDO_1P8_2
VCCDSW_3P3_1
VCCDSW_3P3_2
VCCHDA
VCCMPHY_SENSE
VSSMPHY_SENSE
DCPRTC_1
DCPRTC_2
+1P05VSB
+1P8VSB_ORG
+1P8V_PRIM
+3P3V_ORG
+3P3V_DSW
+VCCPRIM_1P05
+VCCAPLL_1P05
+VCCDUSB_1P05
+VCCCLPLLEBB_1P05
+V1P0A_VCCAMPHYPLL_W25MIL
+VCCDPHY_1P24_MAR
+VCCDPHY_1P24
+VCCLDOSRAM_IN_1P24
+VCCA_OC_1P05
+VCCA_SRC_1P05
+VCCDSW_1P05
+VCCRTC_W8MIL
+RTC_PCH
+VCCPGPPA
+VCCPHVLDO_1P8
+VCCPFUSE_W20MIL
+DVDDIO_AUDIO_W10MIL
/NON_RTCGEN9
DCPRTC
NOBOM
NI
GND
Follow INTEL review result - X00/0629
Close to PCH ball BG5 - X01/0802
CNVi GPIO change to 3.3V - X00/0615
Reserve when PCH Integrated 1.8V VRM is not used - X01/0801
For DELL only
pegatron confidential
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : PCH VCC/PLL
Pegatron Corp. Engineer: Travis_Hsieh
Size A3 Project Name Vulcan Rev X00
Date: Wednesday, November 28, 2018 Sheet 26 of 94



PEGATRON DT-MB RESTRICTED SECRET

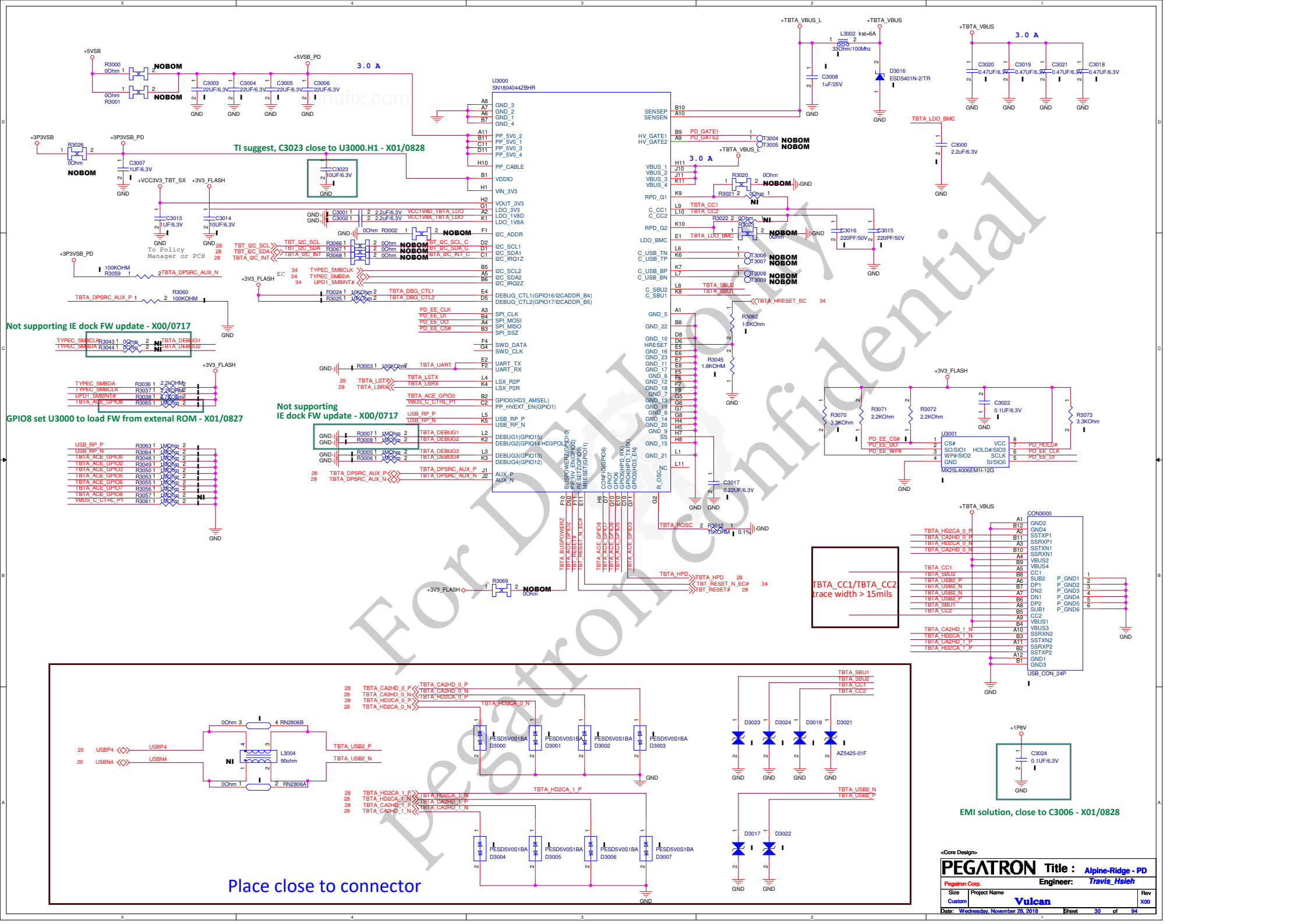
PEGATRON	Title : PCH VSS	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 27 of 94	


U2800A
CPU DDI1
CPU DDI2
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
SINK PORT 1
I2C GPIO
POC GPIO
Misc
MISC
TBT PORTS
Port A
POC
DEBUG
JHL6340
For EA - X01/0829
U2801
MX25L8006EM2I-12G
U2803
74LVC1G3157GW
U2802
NC7SZ08P5X
ForTBT RTD3 support
- X00/0717
可置放於shielding外
Shielding CLIP
CON2800
CON2801
CON2802
CON2803
SUL-15A12M
DEBUG PINs:
PIN | TERMINATION
MONDC_SVR | GND
MONDC_DPSNK_0 | GND
MONDC_DPSNK_1 | GND
MONDC_DPSRC | GND
MONDC_CIO_0 | GND
TEST_EDM | GND
FUSE_VQPS_64 | GND
FUSE_VQPS_128 | GND
ATEST_P/N | FLOATING
USB2_ATEST | FLOATING
PCIE_ATEST | FLOATING
IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:
GPIO | TERMINATION | Power Rail
GPIO_0 | 10K PU | VCC3V3_LC
GPIO_1 | 10K PU | VCC3V3_LC
GPIO_2 | 100K PD
GPIO_3 | 100k PD
GPIO_4 | 10K PU | VCC3V3_LC
GPIO_5 | 10K PU | VCC3V3_LC
GPIO_6 | 100K PD
GPIO_7 | 100K PD
GPIO_8 | 100K PD
POC_GPIO_0 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_1 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_2 | 100K PD
POC_GPIO_3 | 100K PD
POC_GPIO_4 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_5 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_6 | 100K PD
NOTE:
ASSEMBLE R2834, R2835 if DPSRC
NOT IN USE
AR/PPS COMMON FLASH
Shielding CLIP
PEGATRON
Title : Alpine-Ridge - controller
Pegatron Corp.
Engineer: Travis_Hsieh
Size A2
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 28 of 94
For DFT only
pegatron confidential

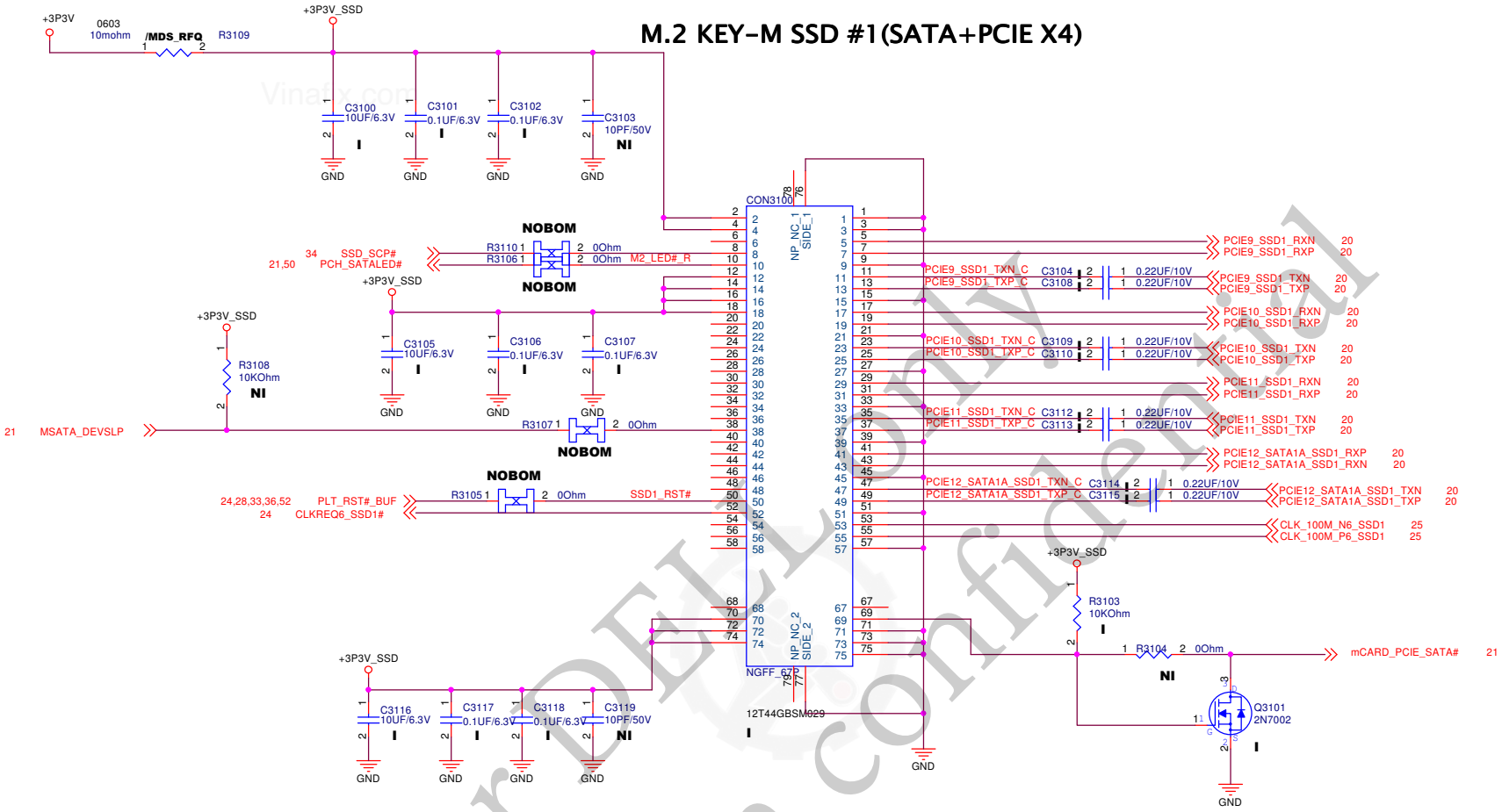


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Alpine-Ridge - Power		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: A2	Project Name: Vulcan		Rev: X00
Date: Wednesday, November 28, 2018	Sheet 29 of 94		

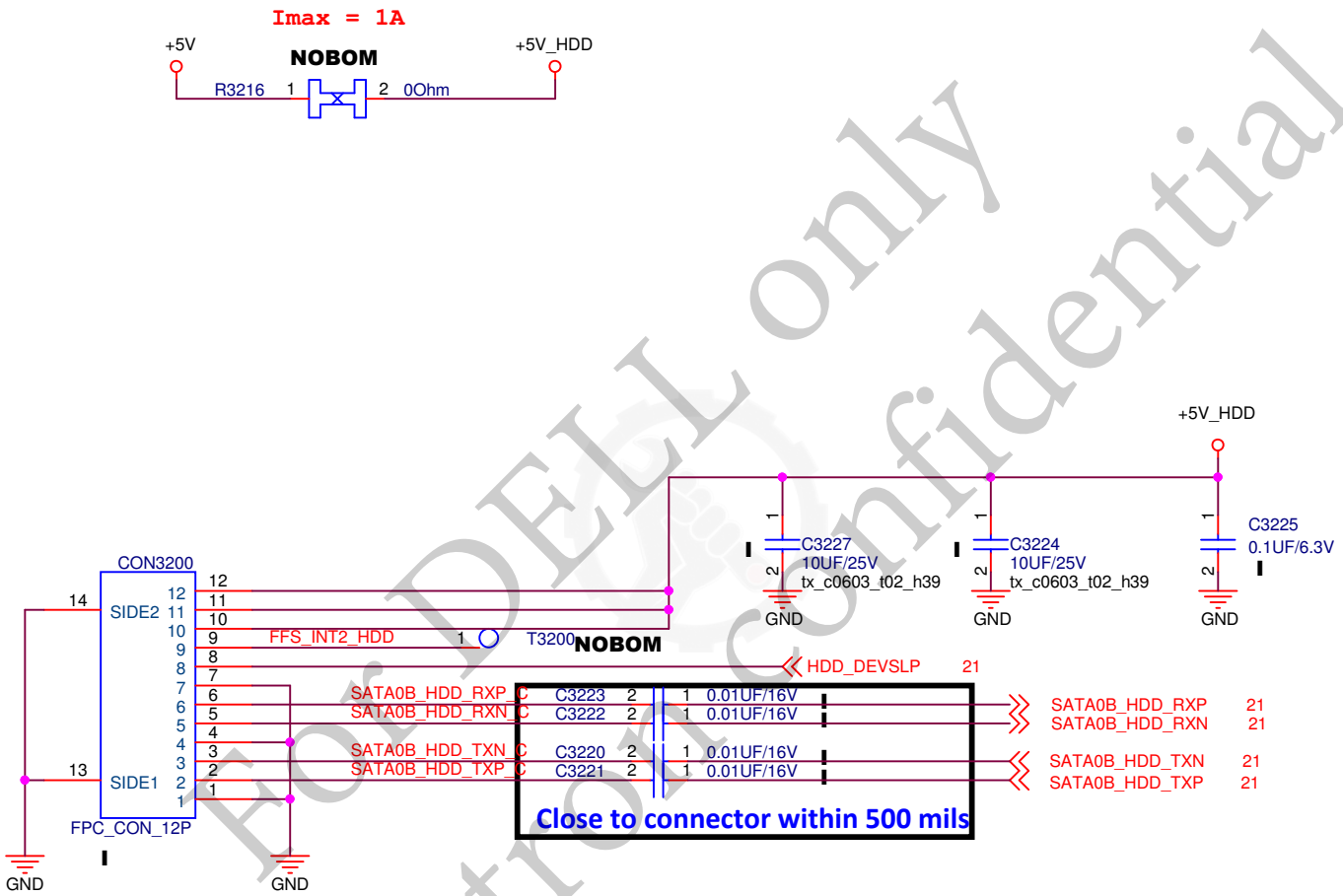

U3000
SN1804044ZBHR
3.0 A
TI suggest, C3023 close to U3000.H1 - X01/0828
Not supporting IE dock FW update - X00/0717
GPIO8 set U3000 to load FW from extenal ROM - X01/0827
Not supporting
IE dock FW update - X00/0717
TBTA_CC1/TBTA_CC2
trace width > 15mils
EMI solution, close to C3006 - X01/0828
Place close to connector
For DFI only
pegatron confidential
PEGATRON
Title : Alpine-Ridge - PD
Engineer: Travis_Hsieh
Pegatron Corp.
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 30 of 94

M.2 KEY-M SSD #1(SATA+PCIE X4)



PEGATRON	Title : M.2 2280 SSD #1	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 31 of 94	

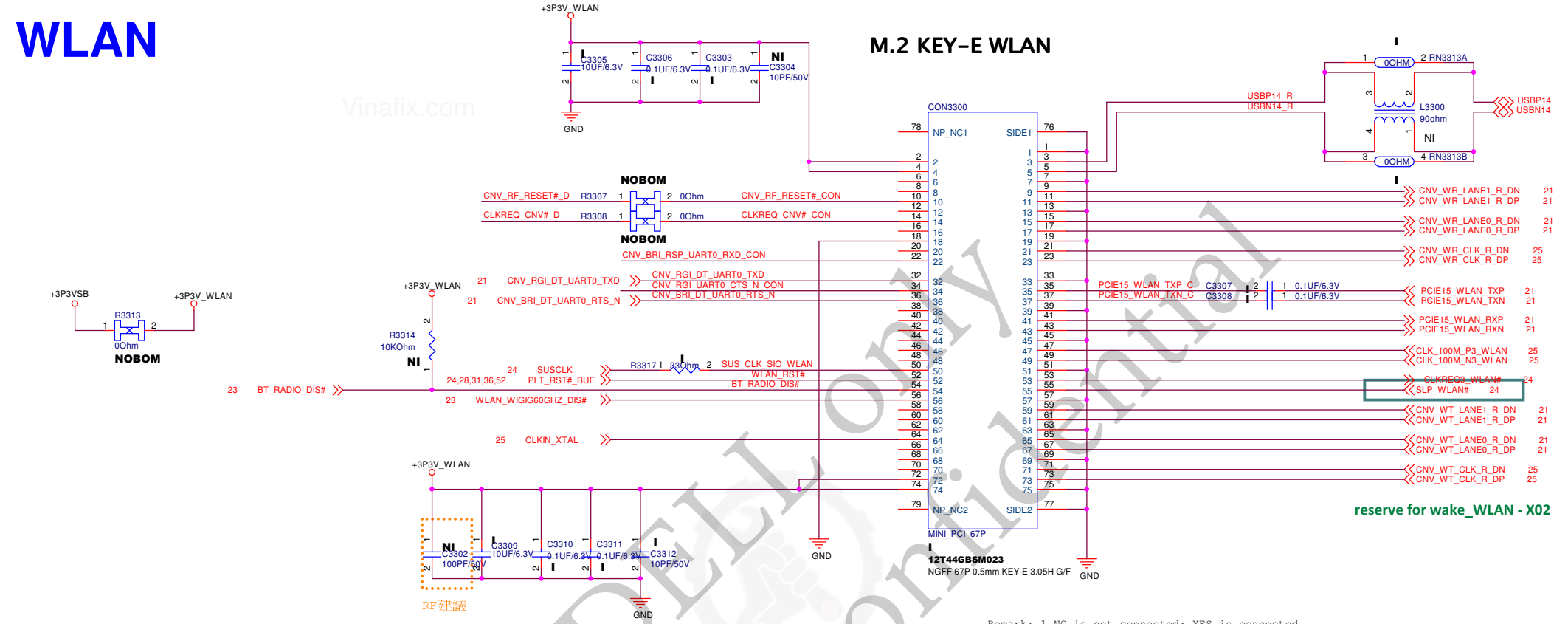
HDD



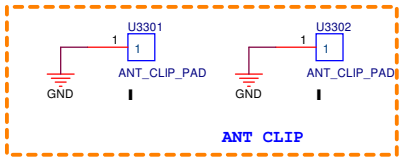
PEGATRON	Title : SATA HDD	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 32 of 94	

WLAN

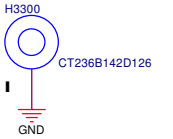
M.2 KEY-E WLAN

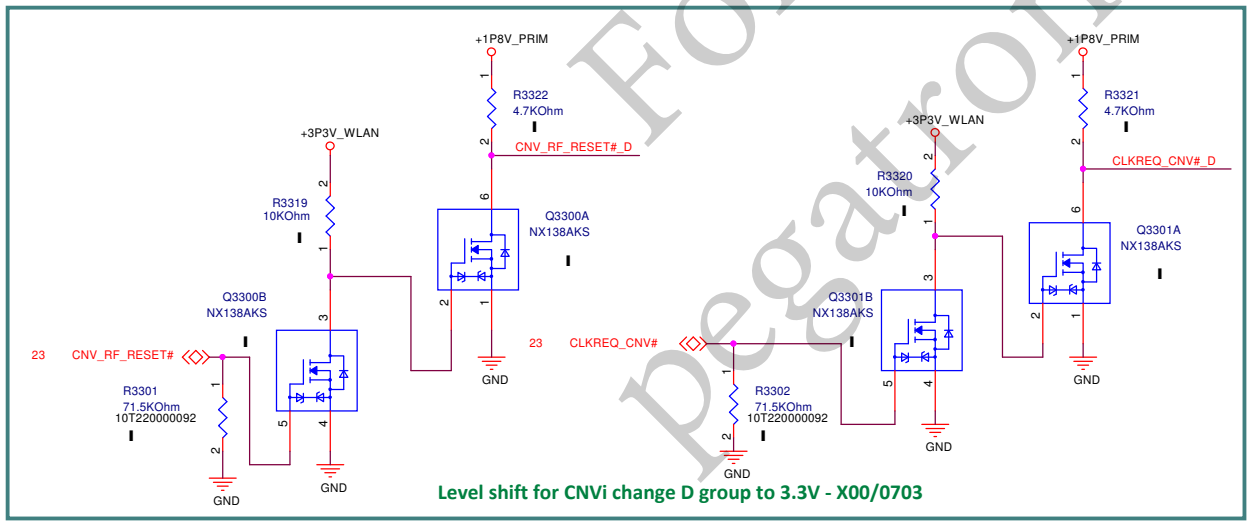


Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.



RTC CLIP
13X020219000
U3303





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : M.2 KEY-A 2230 WLAN	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 33 of 94	

Pull Up

EC Power

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note:
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel.
If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Imax:12.5mA

PD reset follow reference design - X00

/RTC_GEN3

R3493 for EMC - X01/0730

debug test point placement together bottom side

Adapter power monitor to EC ADC pin

Battery power monitor to EC ADC pin

Turn off ELC in MDS - X02 10/24

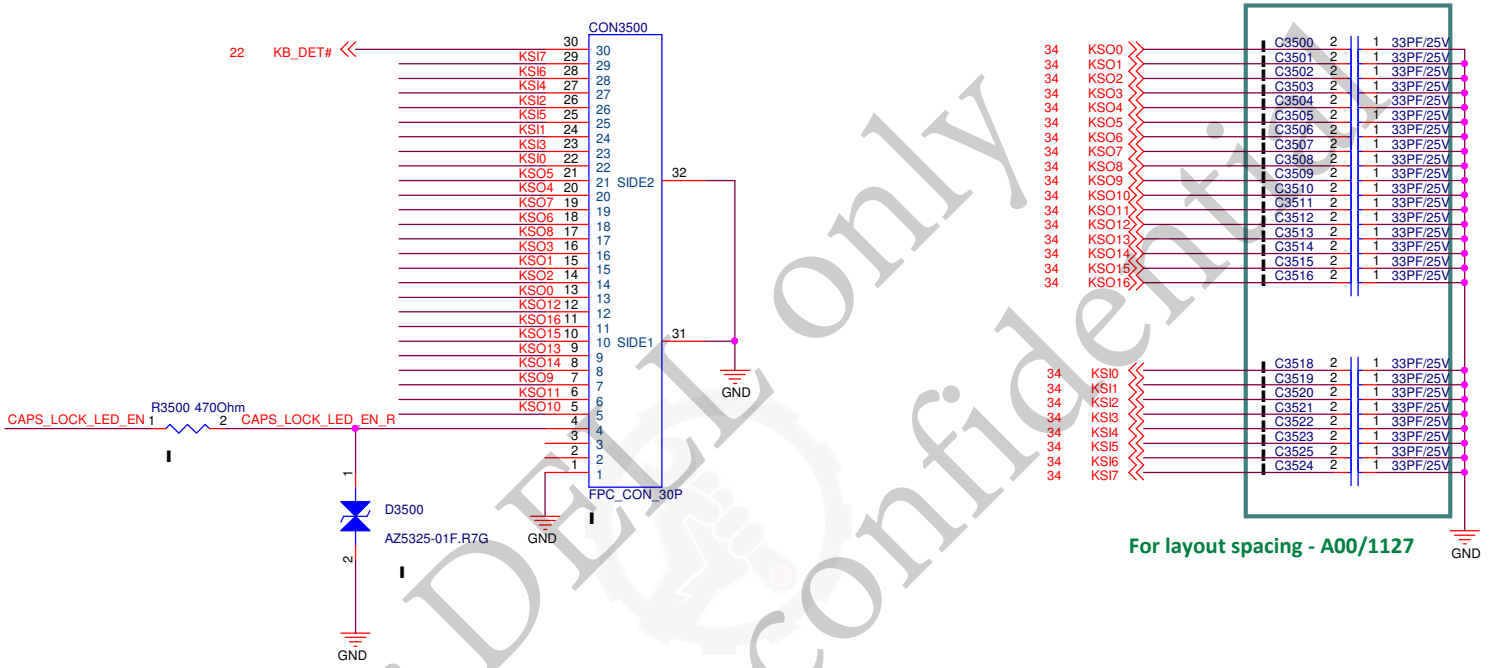
4 Resistor colay (R3497,R3410,R3498,R3499)

Board_ID		
config	Pull-High res ; R3412	Voltage
X00(EVT)	10K	3
X01(DVT)	17.8K	2.801
X02(DVT2)	27K	2.598
X03(reserve1)	37.4K	2.402
A00(PVT)	49.9K	2.201
A01	64.9K	2.001
A02	82.5K	1.808
A03	107K	1.594
Reserve2	154K	1.299
Reserve3	200K	1.1

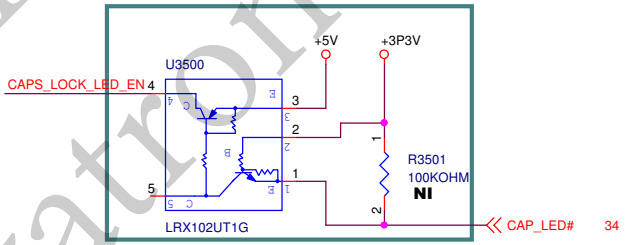
MODEL_ID					
config	CPU	GPU	Pull-High res ; R3410	Voltage	
0	H62	N17P_G1/N18P_G0	10K	3	P-50W
1	H82	N17P_G1/N18P_G0	17.8K	2.801	
2	H62	N18P_G1	27K	2.598	P-60W
3	H82	N18P_G1	37.4K	2.402	
4	Reserve		49.9K	2.201	
5	Reserve		64.9K	2.001	
6	H62	N17E_G1/N18E_G1/N18E_G0	82.5K	1.808	E-60W/65W
7	H82	N17E_G1/N18E_G1/N18E_G0	107K	1.594	
8	H62	N18E_G2_G3	154K	1.299	E-80W
9	H82	N18E_G2_G3	200K	1.1	

PEGATRON Title : EC
Pegatron Corp. Engineer: Travis_Hsieh
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 34 of 94

KeyBoard connector



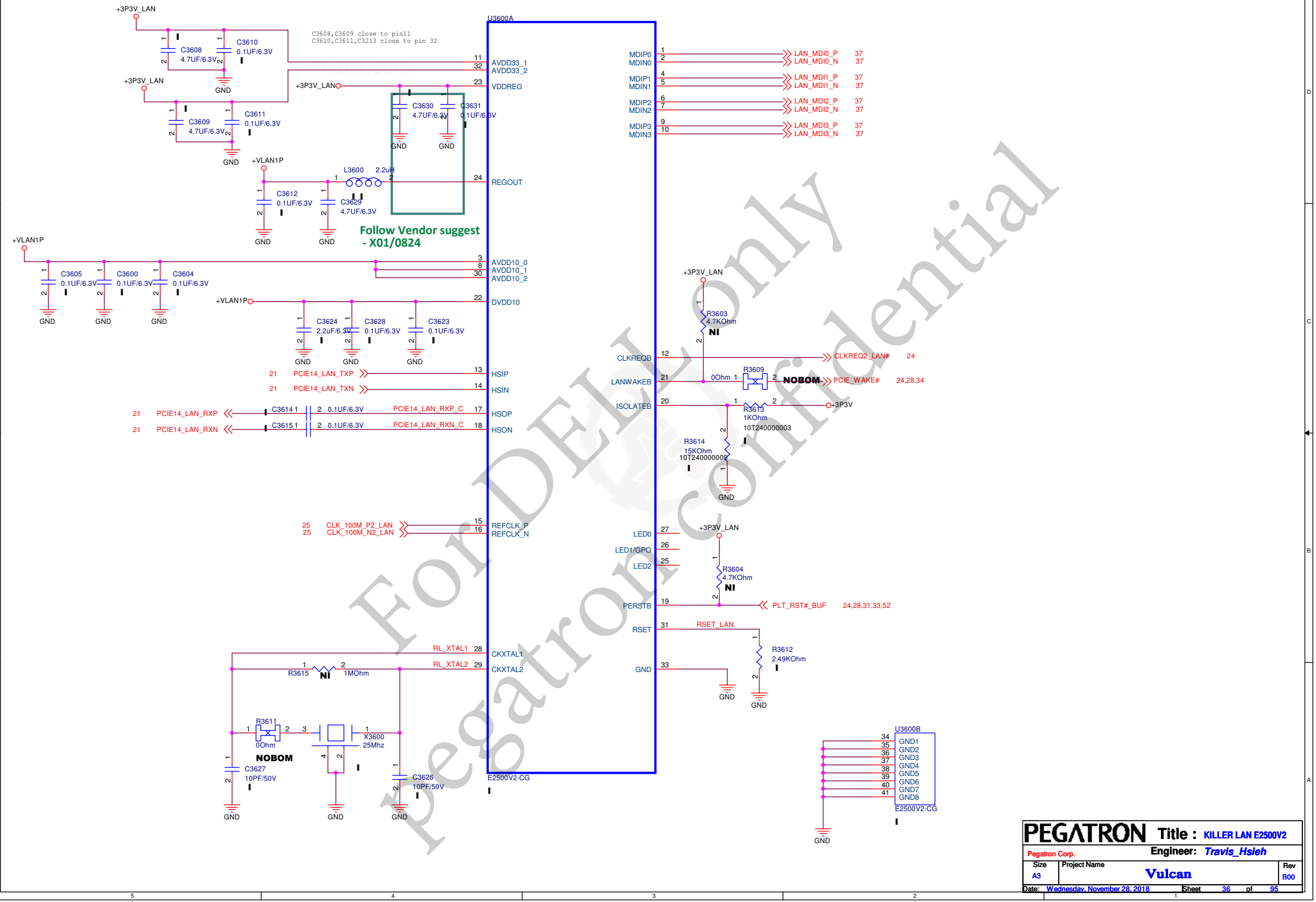
For layout spacing - A00/1127



TX pool change to MX per CE request - X01/0801

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : KB & NKRO	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: B	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 35 of 94	

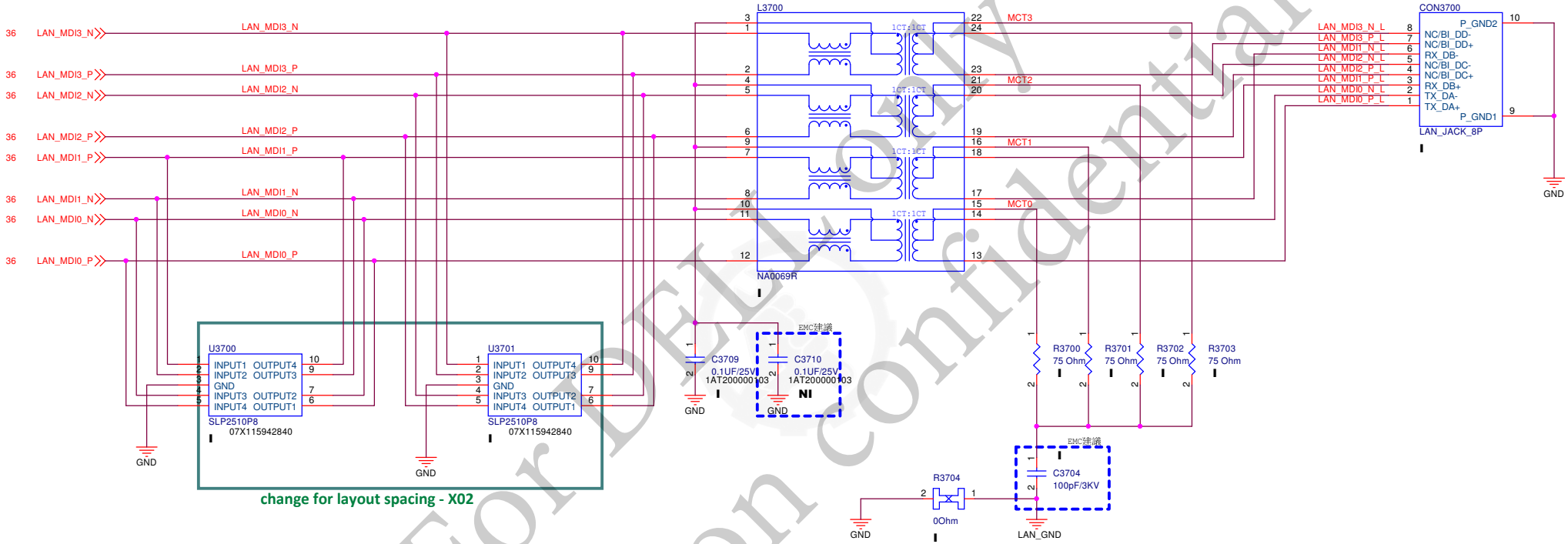


PEGATRON Title : KILLER LAN E2500V2

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 36 of 95



<Core Design>

PEGATRON Title : LAN JACK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 37 of 94

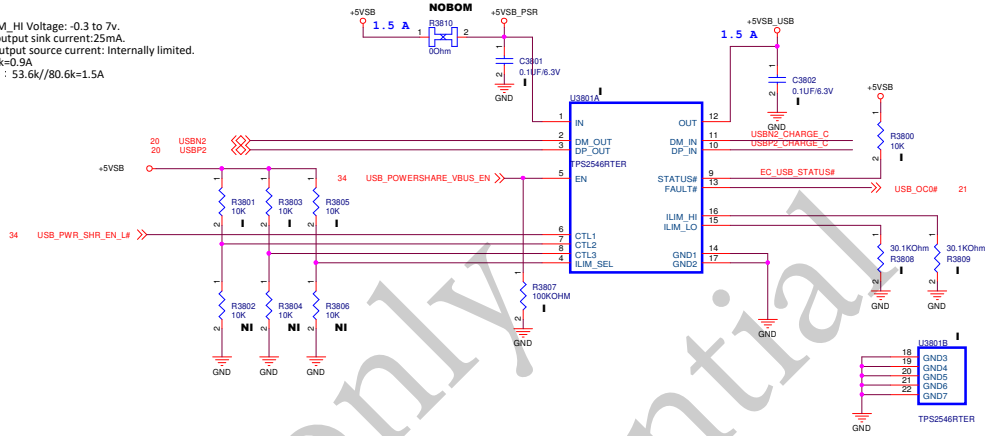
Power Share

Table 2. Truth Table

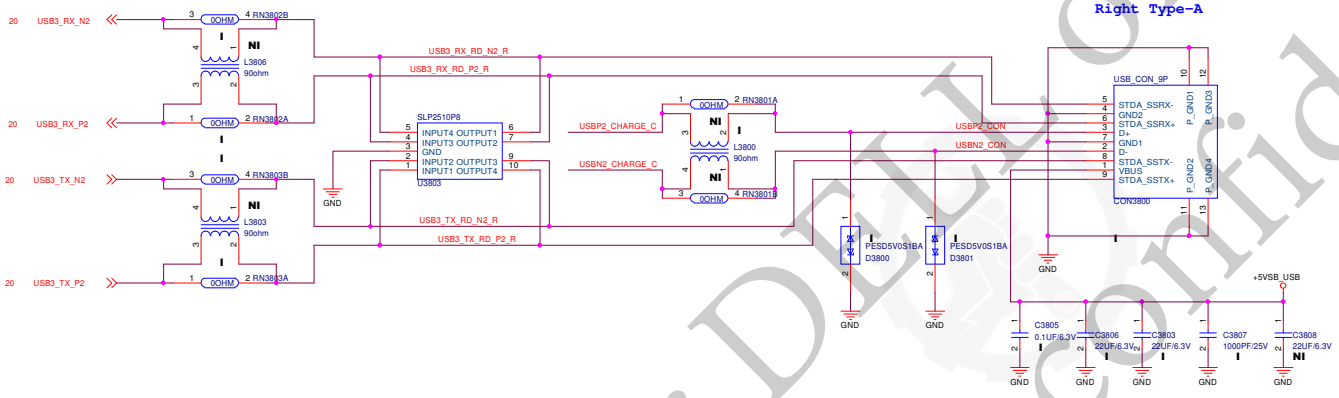
CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP _Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	DCP load present(5)	Data Lines Connected and Load Detect Active

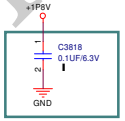
(1) TPS2546 : Current limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the "Load Detection – Power Wake" limits.
(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.

STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.
SDP Mode(S0/S3/S4/S5) : 53.6k=0.9A
CDP(S0)& DCP(S3/S4/S5) Mode : 53.6k//80.6k=1.5A



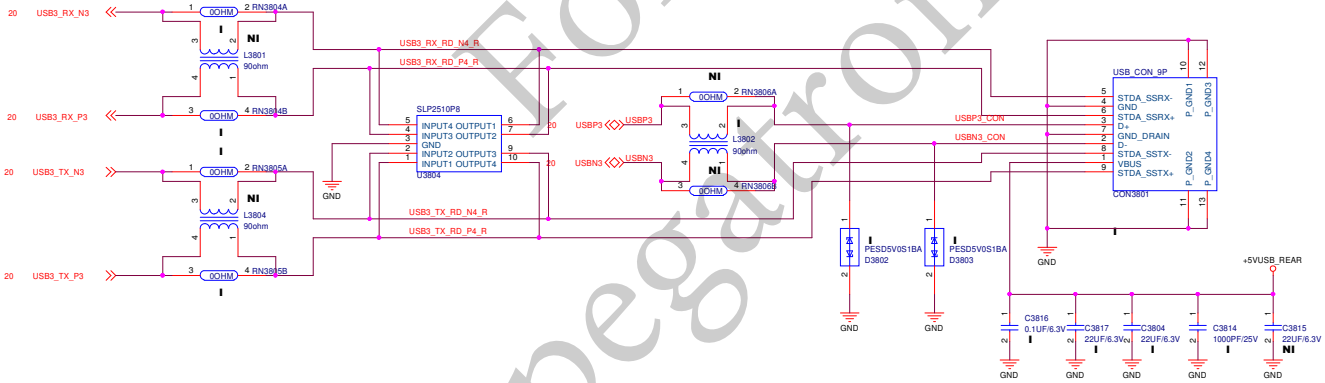
Right Type-A

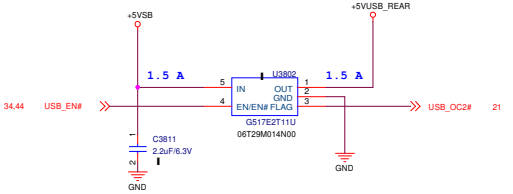




EMI solution, close to CON3800 - X01/0828

Rear Type-A

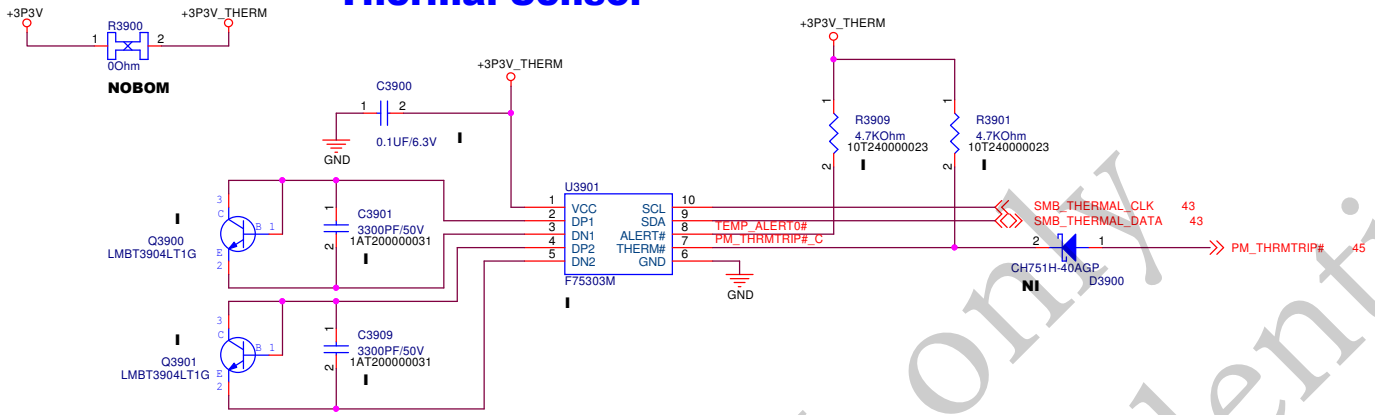




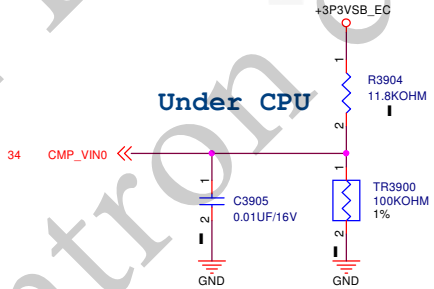
<Core Design>

PEGATRON Title : USB CONN & POWER
Pegatron Corp. Engineer: Travis_Hsieh
Size: A2 | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 38 of 94

Thermal Sensor



U3901: Under GPU thermal pipe
Q3900: Under CPU thermal pipe
Q3901: Close to SSD connector



<Core Design>

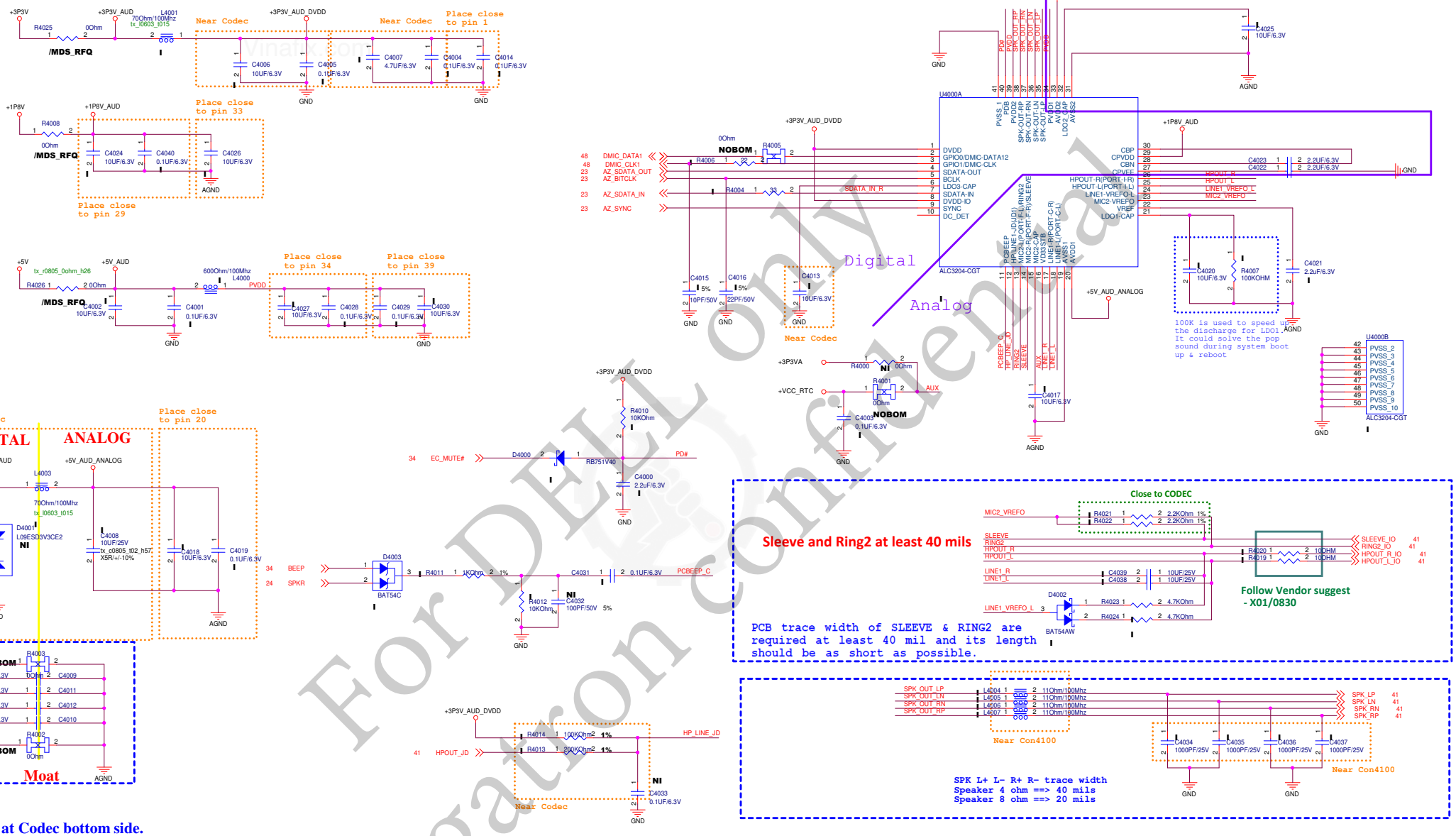
PEGATRON Title : SENSOR

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 39 of 94

AUDIO CODEC- ALC3204



R4003 Place at Codec bottom side.
R4002 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

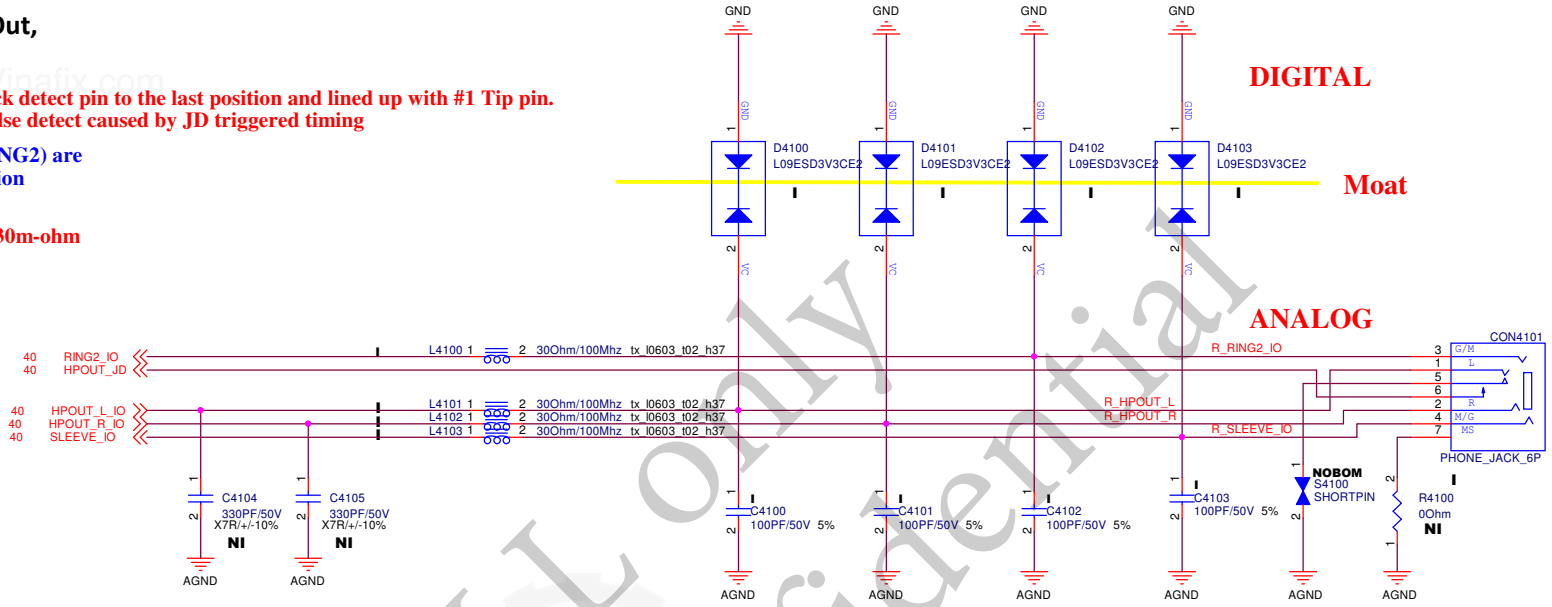
GLOBAL HEADSET CONNECTOR

OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

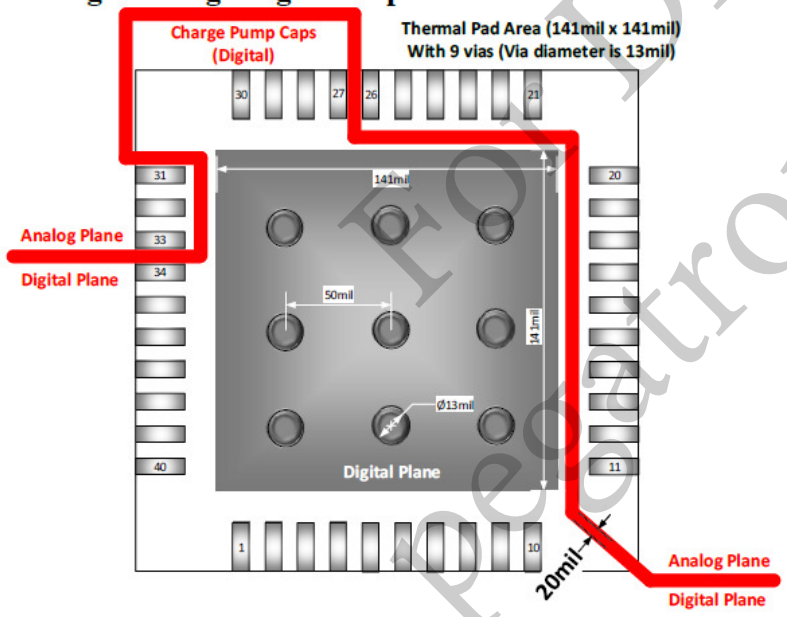
This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin.
This kind of design will significantly improve the false detect caused by JD triggered timing

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.

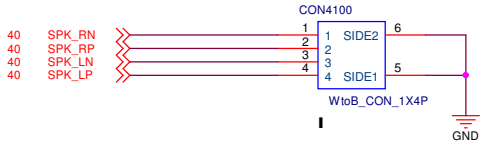
L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.



Separate Analog and Digital ground plane



SPEAKER CONN



<Core Design>

PEGATRON Title : AUDIO JACK

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	X00

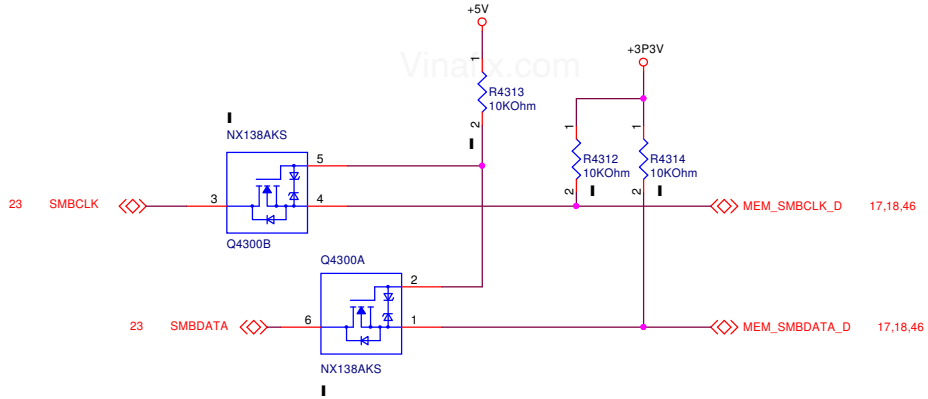
Date: Wednesday, November 28, 2018 Sheet 41 of 94

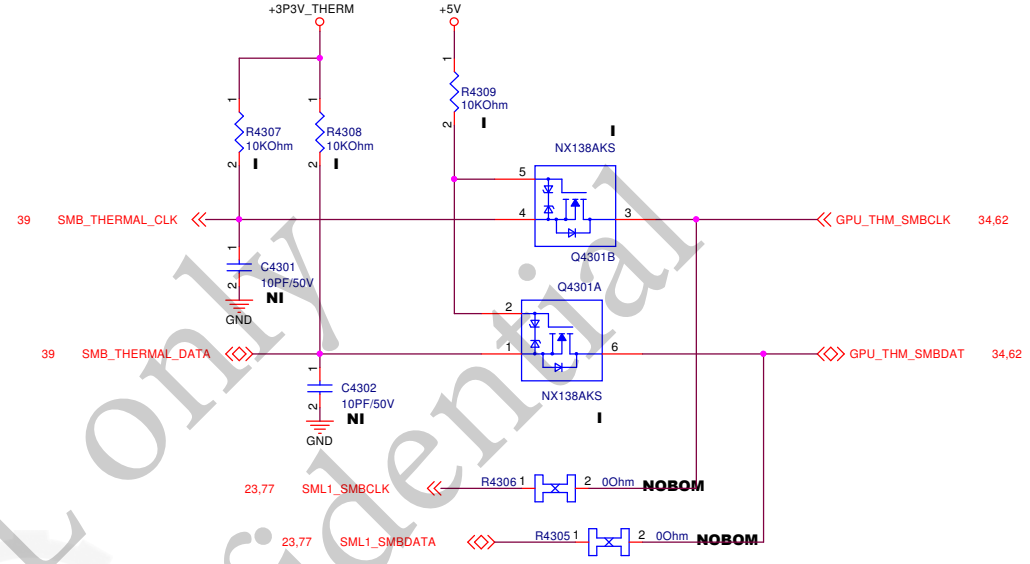
Reserved Page

<Core Design>

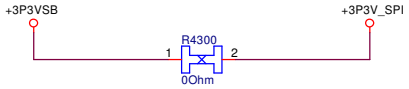
PEGATRON	Title : Reserved	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A4	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 42 of 94	

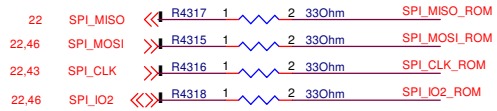
SMBUS

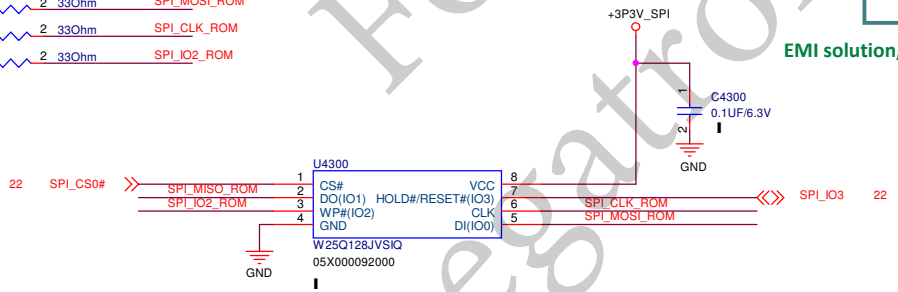


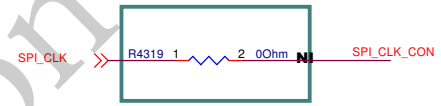


SPI ROM (Quad I/O Supported)

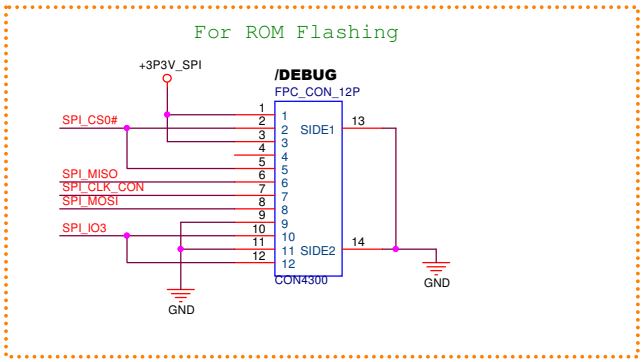






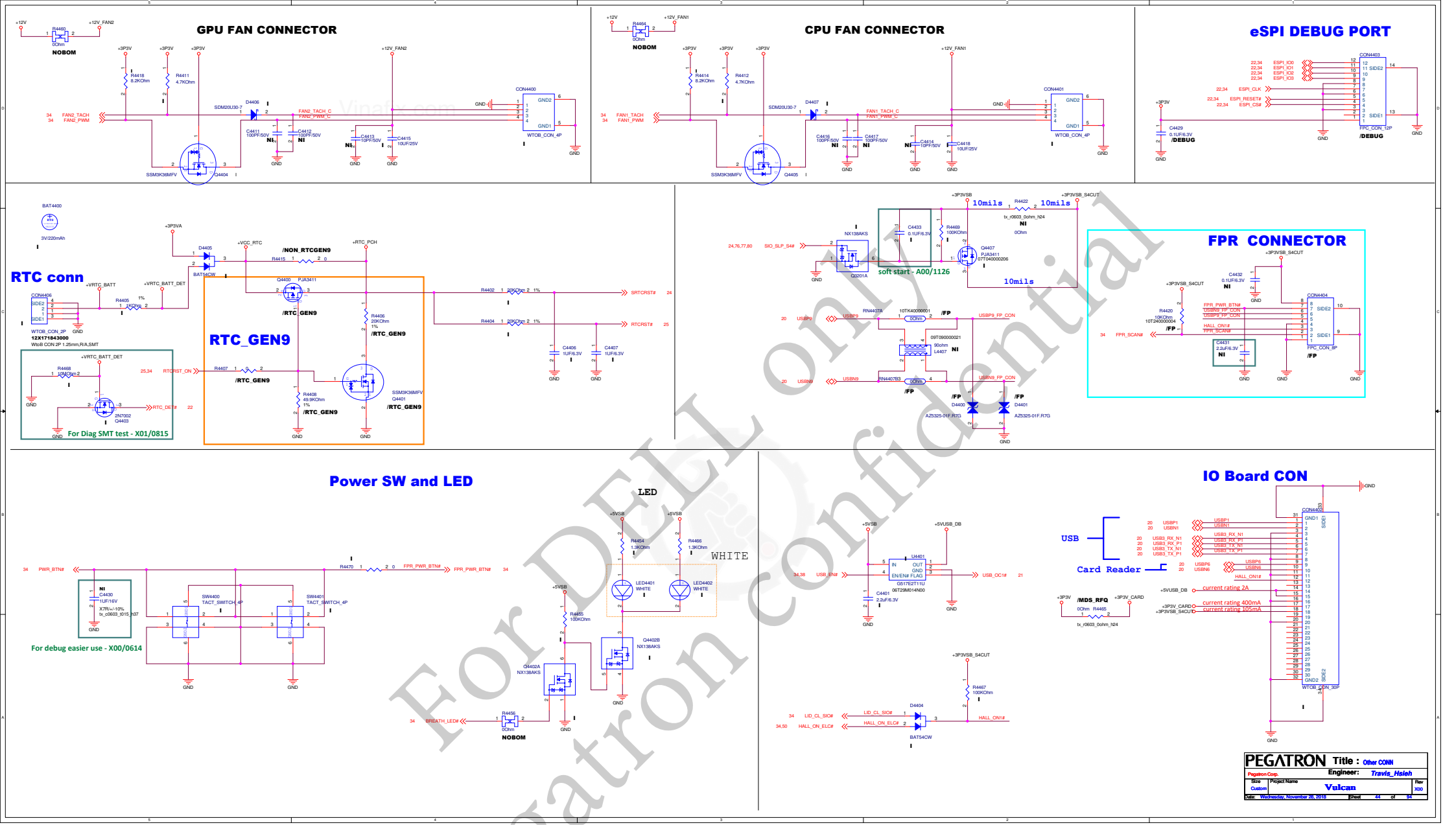


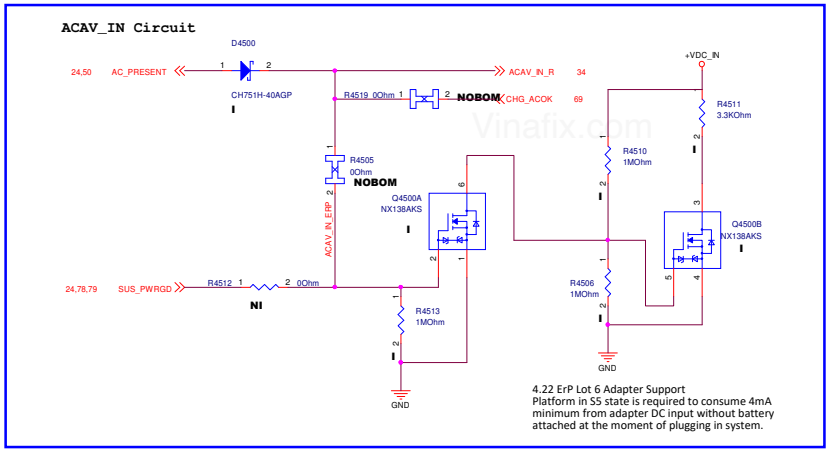
EMI solution, close to R4316 - X01/0828

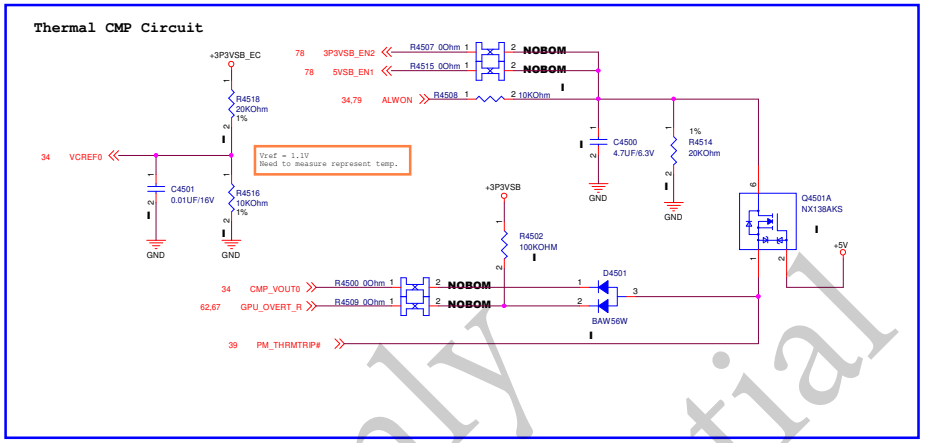


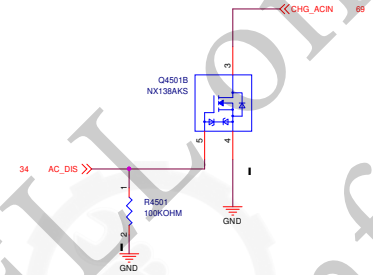
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SM BUS & SPI ROM		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size A3	Project Name Vulcan		Rev X00
Date: Wednesday, November 28, 2018	Sheet 43 of 94		

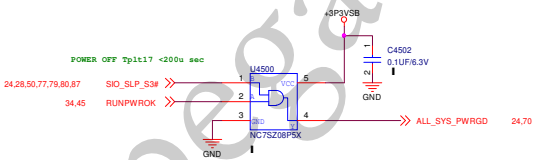


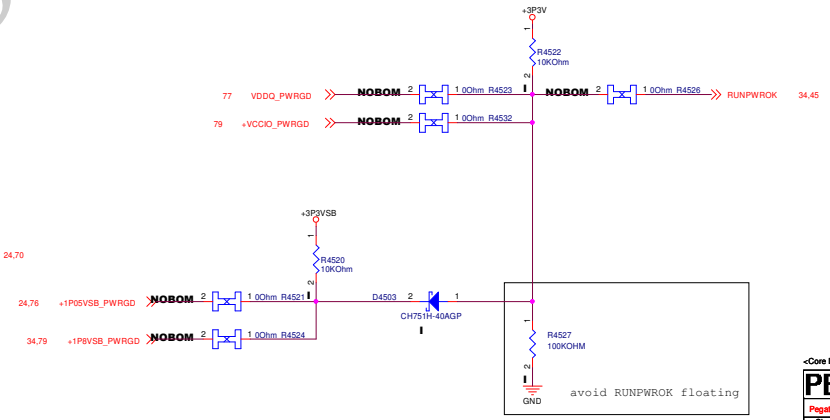






POWER GOOD DETECTER





<Core Design>

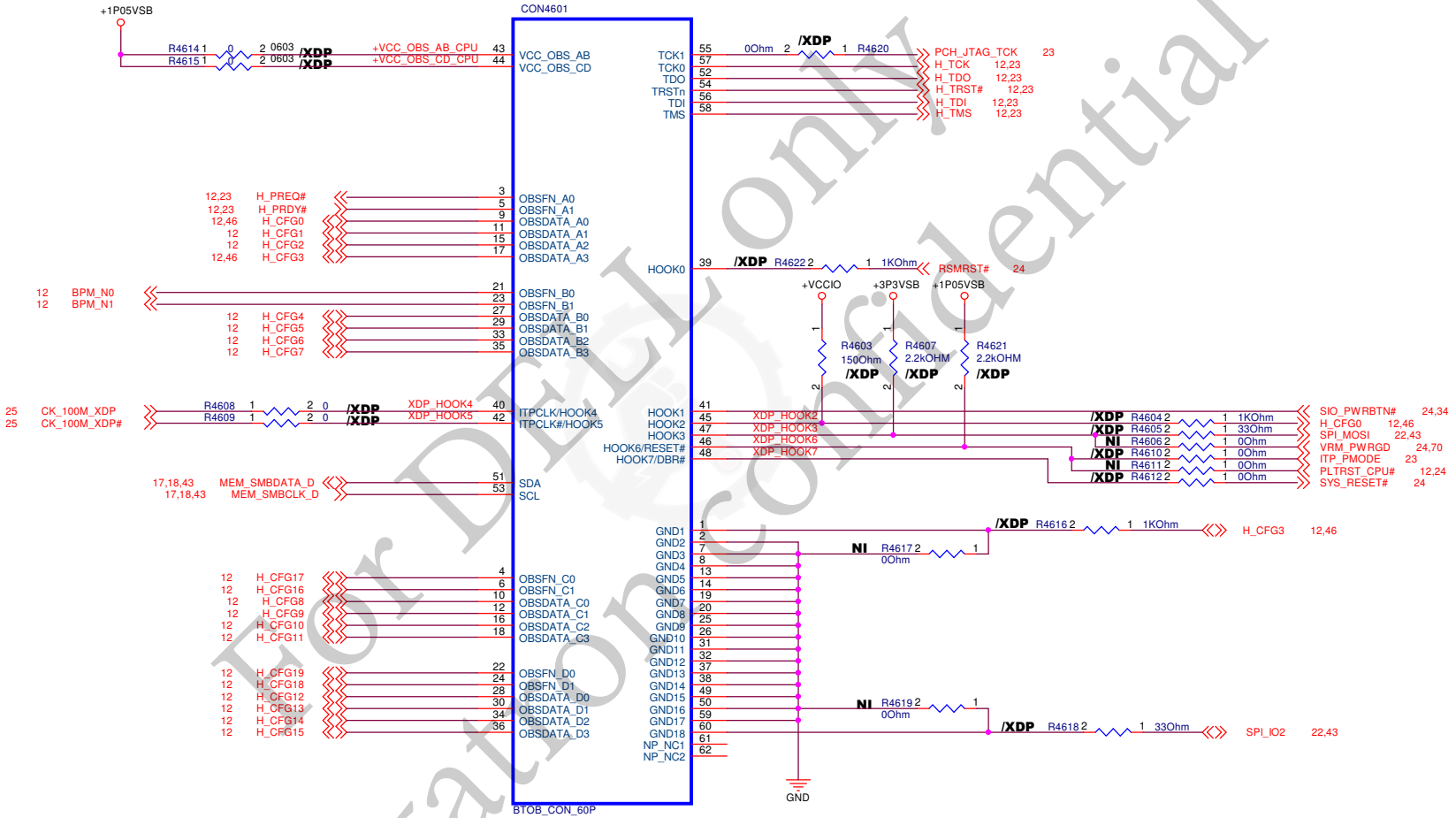
PEGATRON Title : ACAV_IN

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 45 of 94

INTEL XDP DEBUG CONN



PEGATRON	Title : XDP	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 46 of 94	

NOBOM
PCB4700
PCB
PCB_BOARD
CCL = Y

H4730 CT217B142D126 GND
H4729 CT217B142D126 GND
I

Fan Nut

H4708 C276D157 NOBOM
H4710 C276D157 NOBOM
H4712 C276D157 NOBOM
H4719 C276D157 NOBOM
NOBOM
For CPU

H4723 C236D157 NOBOM
H4716 C236D157 NOBOM
H4700 C236D157 NOBOM
For GPU

GND

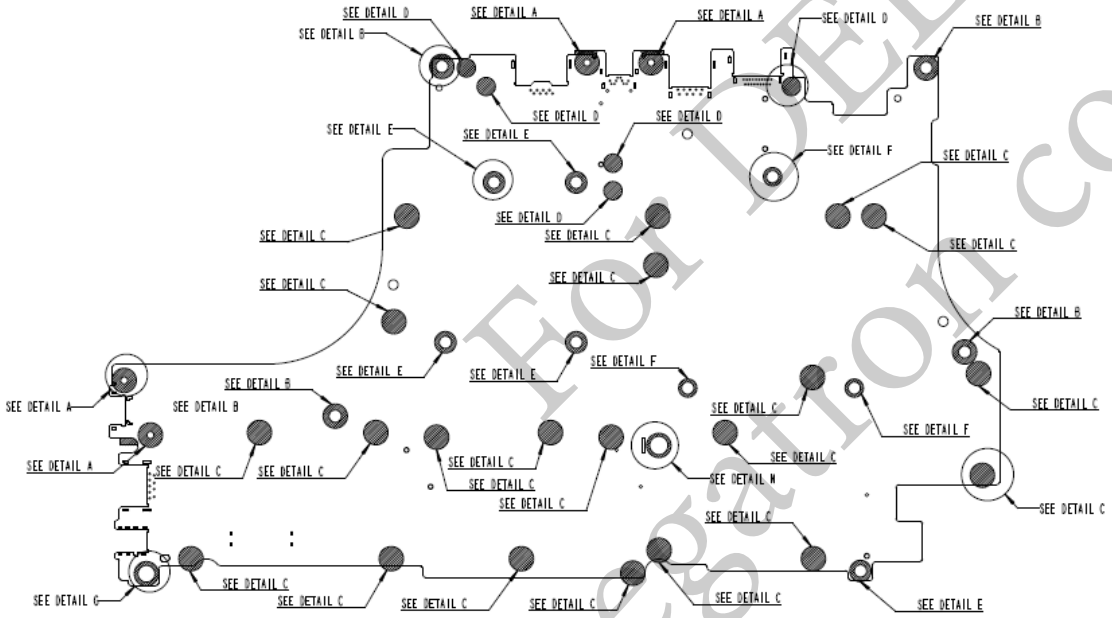
H4748 C315D157 NOBOM
H4747 C315D157 NOBOM
H4746 C315D157 NOBOM
H4745 C315D157 NOBOM
B

H4744 C315D236 NOBOM N
H4743 C315D217 NOBOM G
H4742 RT374X276B276D157 NOBOM E
H4750 O122x83DO122x83N NOBOM J
H4751 C118D118N NOBOM K

H4753 C315D157 NOBOM
H4754 C315D157 NOBOM M
H4755 CT315BR315X311D91 NOBOM O
H4756 RT339X394RB528D91 NOBOM P
H4757 O39x197DO39x197N NOBOM Q

GND

TOP VIEW



PEGATRON Title : PCB & Label & Screw
Pegatron Corp. Engineer: Travis_Hsieh
Size A3 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 Sheet 47 of 94

Panel power

Supply max 2.5A

+3P3VSB → W=100mils → NOBOM R4852 0Ohm → +3P3VSB_PANEL_IN

change for power drop test - X01/0828

C4834 2.2uF/6.3V; U4800 G5250A1T12U (IN, OUT, GND, DSG, EN); R4859 33Ohm → +3P3V_PANEL_O

+3P3V_PANEL_O → R4835 0Ohm NOBOM → W=100mils → +3P3V_PANEL; C4833 4.7UF/6.3V

+AC_BAT_SYS → W=60mils → L4801 120Ohm/100Mhz → C4808 0.1UF/25V

EMC預留 - X02 10/24

NOBOM R4857 0Ohm → F4800 4A/32V → C4806 2.2UF/25V X5R/+/-10%; C4807 0.1UF/25V; C4809 68PF/50V; C4810 2200PF/50V → +VDD_BL_CONN

NON G-SYNC ; CPU

EDP_TXN0..3, EDP_TXP0..3 → R4800–R4807 0Ohm → /NON_GSYNC

EDP_AUXN, EDP_AUXP, EDP_HPD → R4808–R4810 0Ohm → /NON_GSYNC → EDP_MUX_AUXN, EDP_MUX_AUXP, EDP_MUX_HPD

IFPD_EDP_AUXN, IFPD_EDP_AUXP, IFPD_HPD → R4811–R4813 0Ohm → /GSYNC

IFPD_EDP_TXN0..3, IFPD_EDP_TXP0..3 → R4814–R4821 0Ohm → /GSYNC

EDP_MUX_TXN0..3, EDP_MUX_TXP0..3

G-SYNC ; GPU

LCD_VCC_TEST_EN, ENVDD_PCH → R4853 0Ohm → /NON_GSYNC → D4801 BAT54C; R4836 100KOHM

LCD_VCC_EN_GPU → D4807 SDM20U30-7 → /GSYNC; R4836 100KOHM

L_BKLT_EN_EC → R4854 0Ohm → /NON_GSYNC → D4808 BAT54C → BKLT_IN_EC_D; R4847 100KOHM

LCD_BLEN_GPU

+3P3V → F4801 0.5A/32V → +3P3V_MIC; C4837 0.1UF/6.3V

Follow Vendor comment - X00/0516

+3P3V_CAM; C4805 0.1UF/6.3V

R4851 0Ohm NOBOM

eDP CONNECTOR

FPC_CON_40P

LCD_DBC; USBP5_RD_R, USBN5_RD_R; DMIC_CLK1, DMIC_DATA1

EDP_MUX_TXP0..3, EDP_MUX_TXN0..3 → C4813–C4826 0.1UF/6.3V → EDP_TXP0_C..EDP_TXP3_C, EDP_TXN0_C..EDP_TXN3_C

EDP_MUX_AUXP, EDP_MUX_AUXN → C4832, C4830 0.1UF/6.3V → EDP_AUXP_C, EDP_AUXN_C

EDP_HPD_CON → R4840 NOBOM 0Ohm

CAM_CBL_DET# → +3P3V_MIC

Reserve for Panel Overdrive - X00/0717

PANEL_OVERDRI, CAM_15B_DET#, LCD_TST → R4856, R4828 NOBOM 0Ohm

BIA_PWM_PCH_R → R4834 100KOHM, R4839 100KOHM

+VDD_BL_CONN; C4838 10PF/50V NI

RF預留 - X02 10/24

CON4800

USBP5 → 0OHM RN4800B → USBP5_RD_R

USBN5 → 0OHM RN4800A → USBN5_RD_R

L4800 90ohm 09T090002I00 NI

DMIC_CLK1, DMIC_DATA1 → C4835, C4836 12PF/50V NI → D4804 AZ5125-01J; D4805 AZ5125-01J

+3P3V_PANEL → C4803 0.1UF/6.3V; C4839 10PF/50V NI

PANEL_BKEN_EC → R4858 0Ohm → D4809 SDM20U30-7

BIA_PWM_PCH → D4802 SDM20U30-7 → /NON_GSYNC

LCD_VCC_TEST_EN → D4809 SDM20U30-7

BL_PWM_GPU → D4806 SDM20U30-7 → /GSYNC

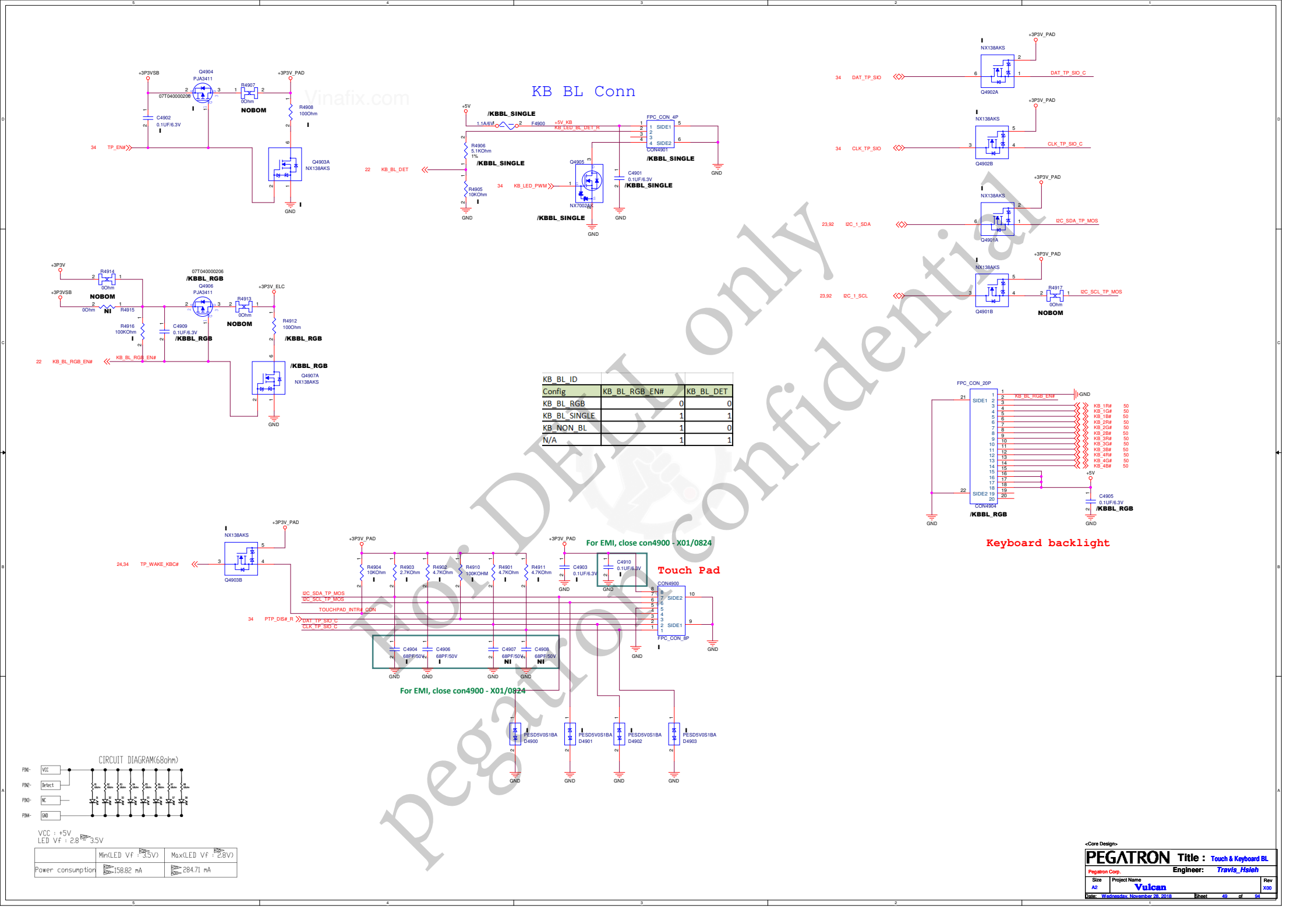
<Core Design>

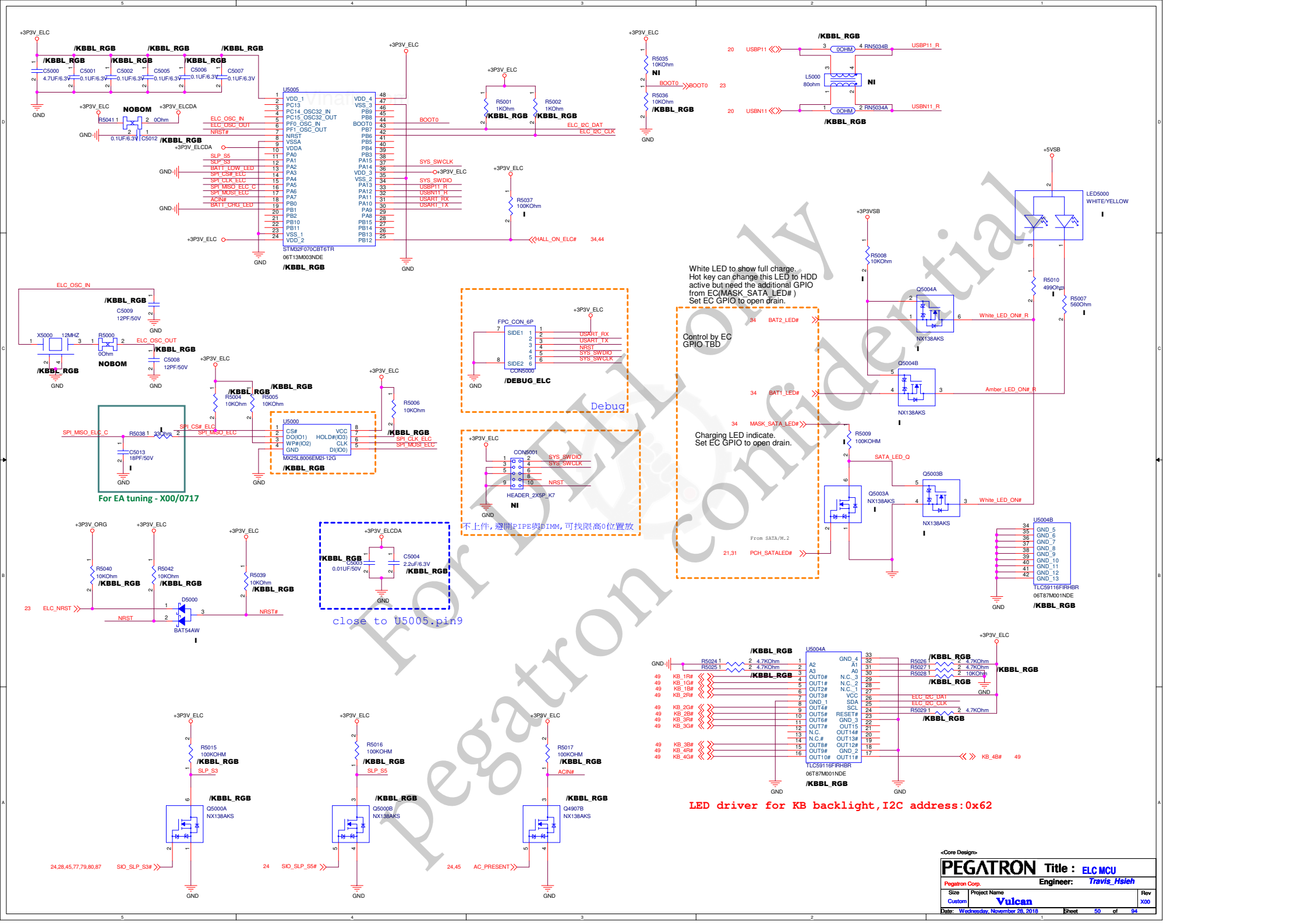
PEGATRON Title : eDP CON.

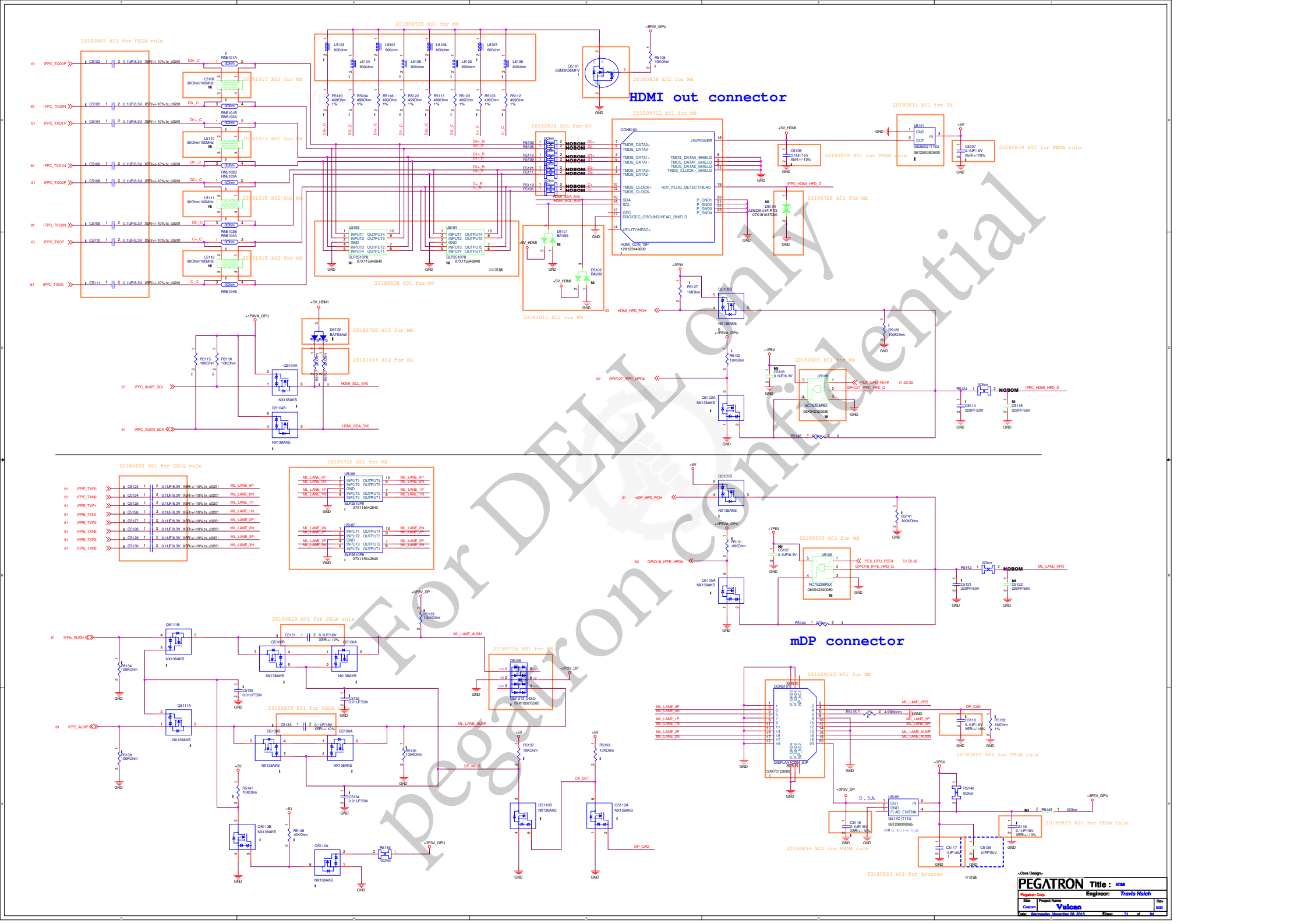
Pegatron Corp. Engineer: Travis_Hsieh

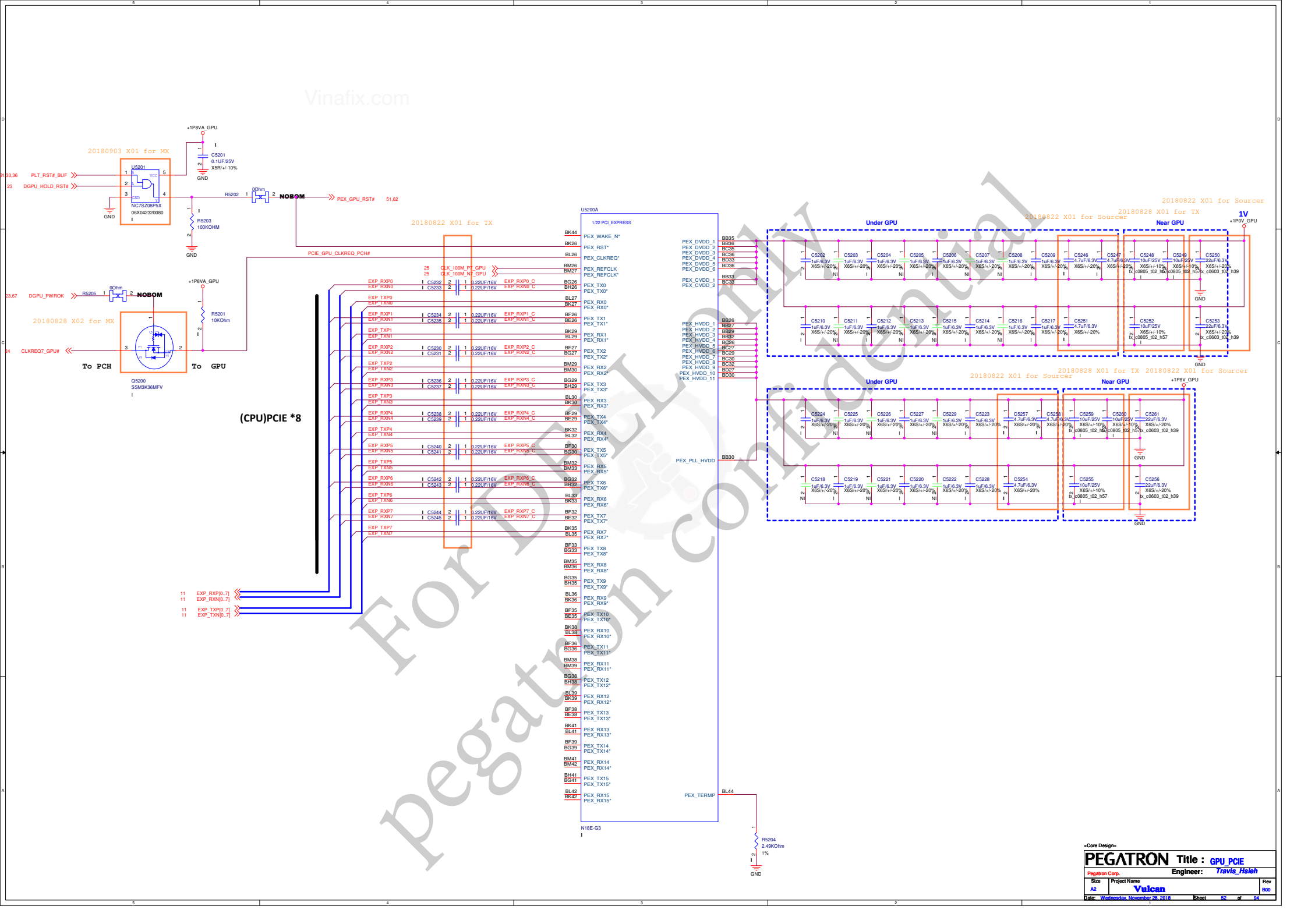
Size A2 | Project Name Vulcan | Rev X00

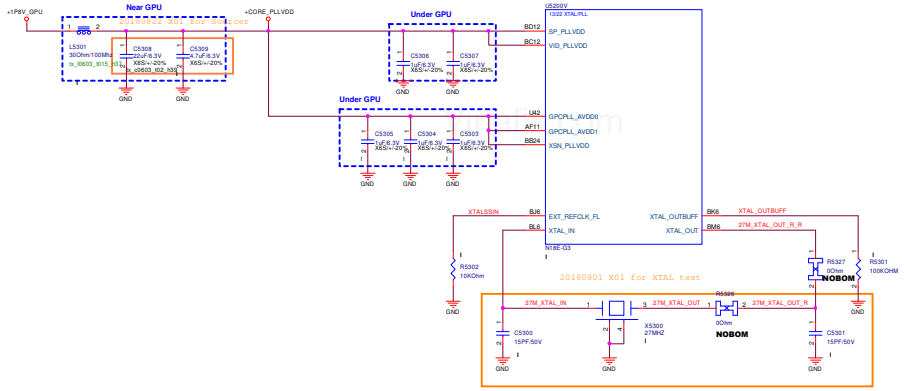
Date: Wednesday, November 28, 2018 Sheet 48 of 94




+3P3V_ELC
/KBBL_RGB
C5000 4.7UF/6.3V
C5001 0.1UF/6.3V
C5002 0.1UF/6.3V
C5005 0.1UF/6.3V
C5006 0.1UF/6.3V
C5007 0.1UF/6.3V
GND
NOBOM
R5041 0Ohm
C5012 0.1UF/6.3V
+3P3V_ELCDA
U5005
STM32F070CBT6TR
06T13M003NDE
ELC_OSC_IN
ELC_OSC_OUT
NRST#
SLP_S5
SLP_S3
BAT1_LOW_LED
SPI_CS#_ELC
SPI_CLK_ELC
SPI_MISO_ELC_C
SPI_MOSI_ELC
ACIN#
BAT1_CHG_LED
BOOT0
SYS_SWCLK
SYS_SWDIO
USBPT1_R
USBN11_R
USART_RX
USART_TX
R5001 1KOhm
R5002 1KOhm
ELC_I2C_DAT
ELC_I2C_CLK
R5037 100KOHm
HALL_ON_ELC#
34,44
R5035 10KOhm
R5036 10KOhm
NI
USBP11
USBN11
0OHM
RN5034B
RN5034A
L5000 80ohm
USBP11_R
USBN11_R
X5000 12MHZ
R5000 0Ohm
C5009 12PF/50V
C5008 12PF/50V
ELC_OSC_OUT
U5000
MX25L8006EM2I-12G
R5004 10KOhm
R5005 10KOhm
R5006 10KOhm
R5038 33Ohm
C5013 18PF/50V
SPI_MISO_ELC_C
SPI_CS#_ELC
SPI_MISO_ELC
SPI_CLK_ELC
SPI_MOSI_ELC
For EA tuning - X00/0717
FPC_CON_6P
CON5000
/DEBUG_ELC
Debug
CON5001
HEADER_2X5P_K7
SYS_SWDIO
SYS_SWCLK
NRST
不上件，避開PIPE與DIMM，可找限高0位置放
+3P3V_ORG
R5040 10KOhm
R5042 10KOhm
R5039 10KOhm
D5000
BAT54AW
ELC_NRST
NRST#
+3P3V_ELCDA
C5003 0.01UF/50V
C5004 2.2uF/6.3V
close to U5005.pin9
+5VSB
LED5000
WHITE/YELLOW
+3P3VSB
R5008 10KOhm
R5010 499Ohm
R5007 560Ohm
Q5004A
Q5004B
NX138AKS
White_LED_ON#_R
Amber_LED_ON#_R
White_LED_ON#
BAT2_LED#
BAT1_LED#
MASK_SATA_LED#
SATA_LED_Q
R5009 100KOHM
Q5003A
Q5003B
PCH_SATALED#
From SATA/M.2
White LED to show full charge.
Hot key can change this LED to HDD active but need the additional GPIO from EC(MASK_SATA_LED#)
Set EC GPIO to open drain.
Control by EC GPIO TBD
Charging LED indicate.
Set EC GPIO to open drain.
U5004B
TLC59116FIRHBR
06T87M001NDE
U5004A
R5024 4.7KOhm
R5025 4.7KOhm
R5026 4.7KOhm
R5027 4.7KOhm
R5028 10KOhm
R5029 4.7KOhm
KB_1R#
KB_1G#
KB_1B#
KB_2R#
KB_2G#
KB_2B#
KB_3R#
KB_3G#
KB_3B#
KB_4R#
KB_4G#
KB_4B#
LED driver for KB backlight,I2C address:0x62
R5015 100KOHM
R5016 100KOHM
R5017 100KOHM
SLP_S3
SLP_S5
ACIN#
Q5000A
Q5000B
Q4907B
24,28,45,77,79,80,87
SIO_SLP_S3#
24
SIO_SLP_S5#
24,45
AC_PRESENT
For DELL only
pegatron confidential
<Core Design>
PEGATRON
Title : ELC MCU
Engineer: Travis_Hsieh
Pegatron Corp.
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 50 of 94




20180903 X01 for MX
+1P8VA_GPU
C5201
0.1UF/25V
X5R/+/-10%
GND
U5201
NC7SZ08P5X
06X042320080
PLT_RST#_BUF
DGPU_HOLD_RST#
R5202
0Ohm
NOBOM
PEX_GPU_RST#
R5203
100KOHM
20180822 X01 for TX
PCIE_GPU_CLKREQ_PCH#
20180828 X02 for MX
DGPU_PWROK
R5205
R5201
10KOHM
CLKREQ7_GPU#
To PCH
To GPU
Q5200
SSM3K36MFV
(CPU)PCIE *8
U5200A
1/22 PCI_EXPRESS
N18E-G3
R5204
2.49KOhm
1%
20180822 X01 for Sourcer
20180828 X01 for TX
Under GPU
Near GPU
1V
+1P0V_GPU
+1P8V_GPU
For DELL only
pegatron confidential



Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

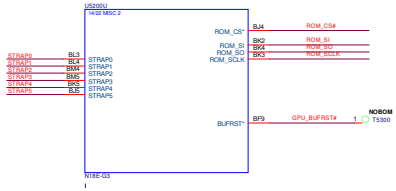
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

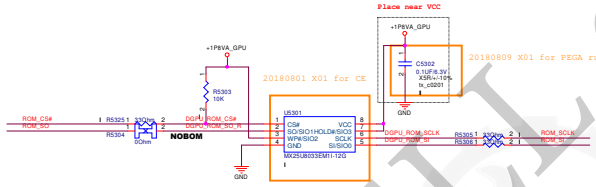
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Straps 需確認strap及ROM(Memory 還未確定)

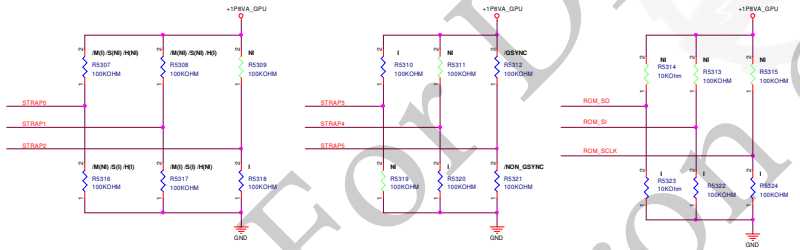




Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx2Chx16	1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.

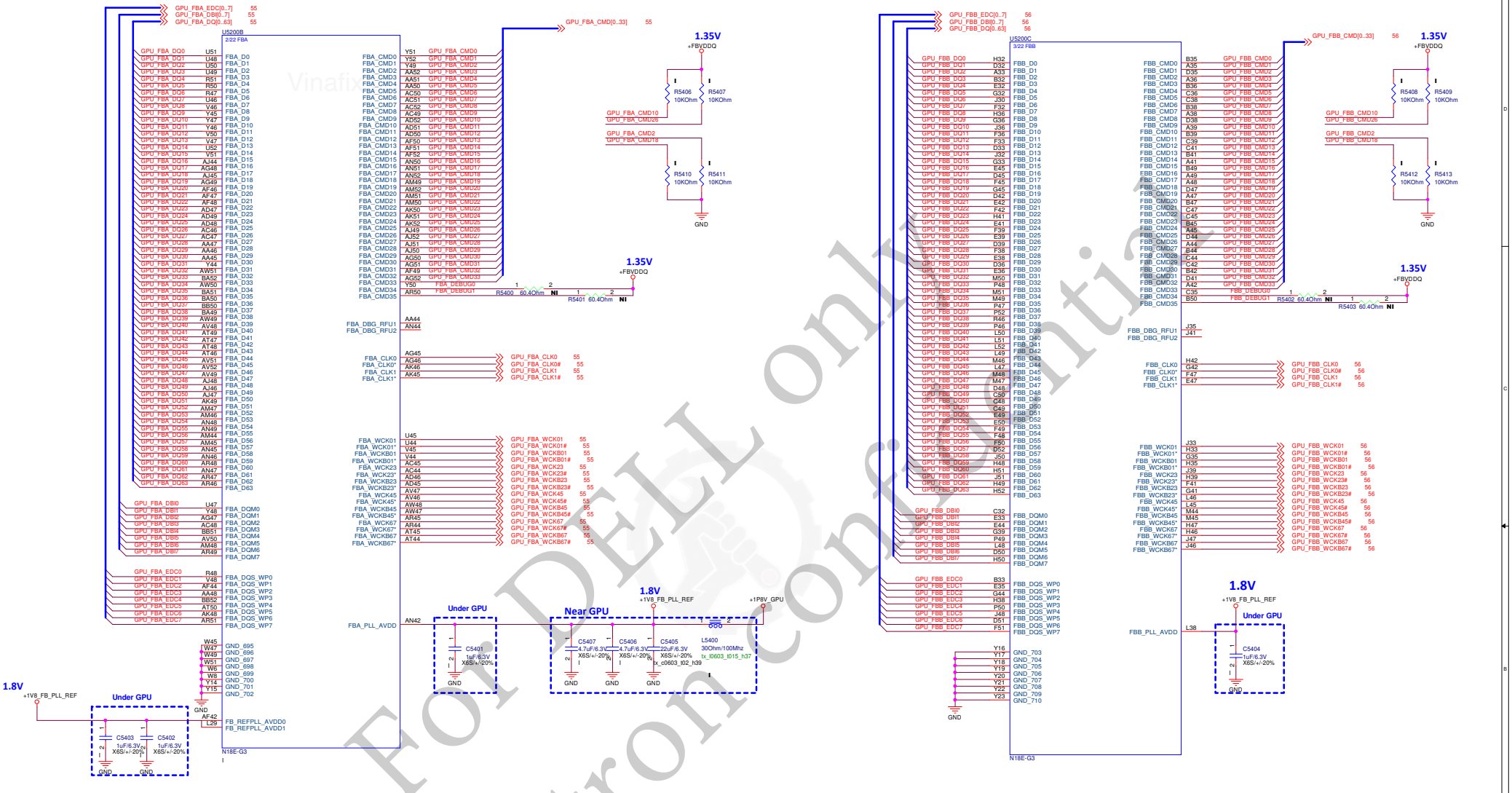
Need NV check



Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate
			Hynix	H56C8H24MJR-S2C	M-die	0x2	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

<Core Design>
PEGATRON Title : GPU-Xtal & Straps
Pegatron Corp. Engineer: Travis_Hsieh
Size: Custom | Project Name: Vulcan | Rev: B00
Date: Wednesday, November 28, 2018 Sheet 53 of 94



<Core Design>

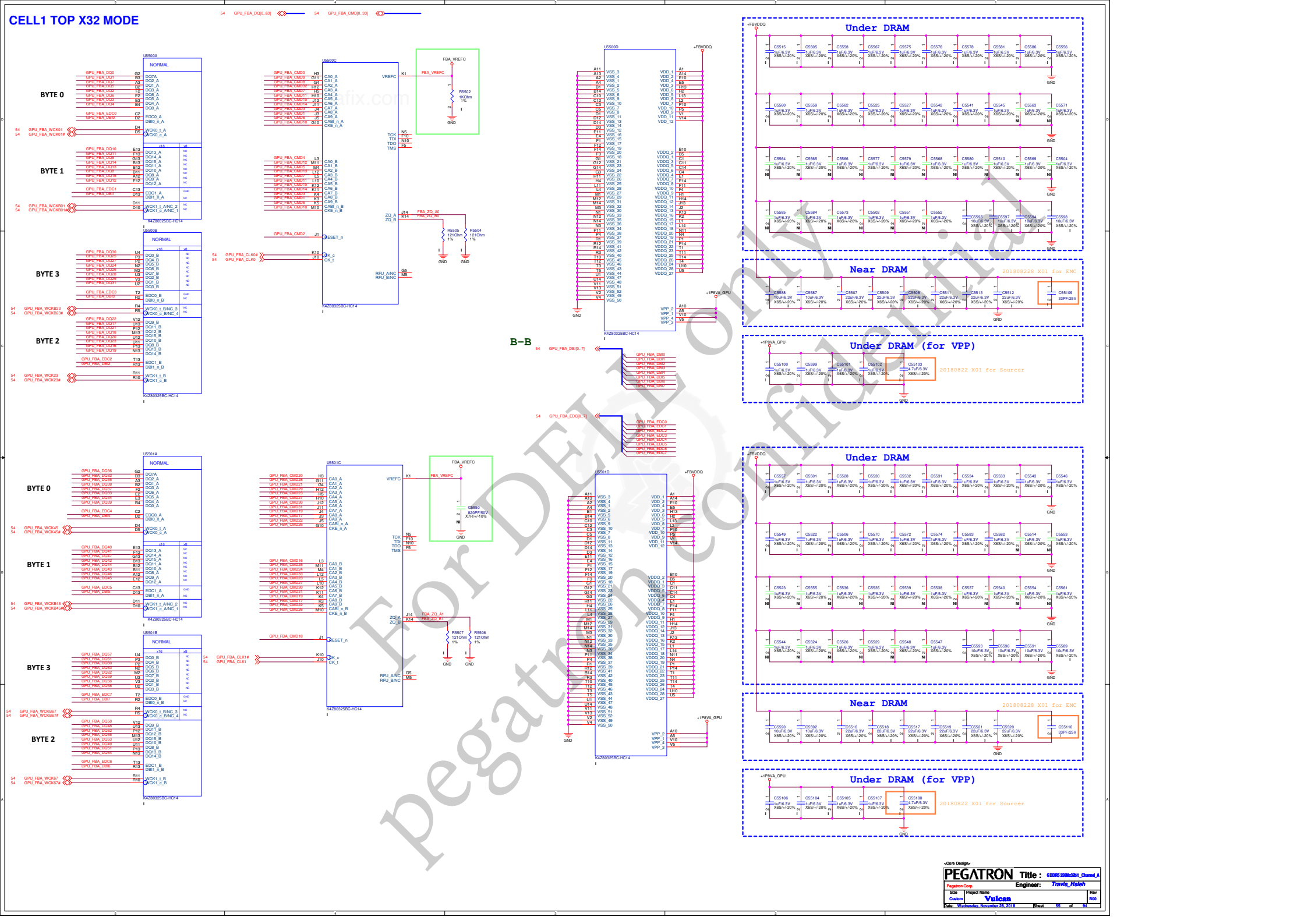
PEGATRON Title : GPU-BUFFER PARTITION A/B

Pegatron Corp. Engineer: Travis_Hsieh

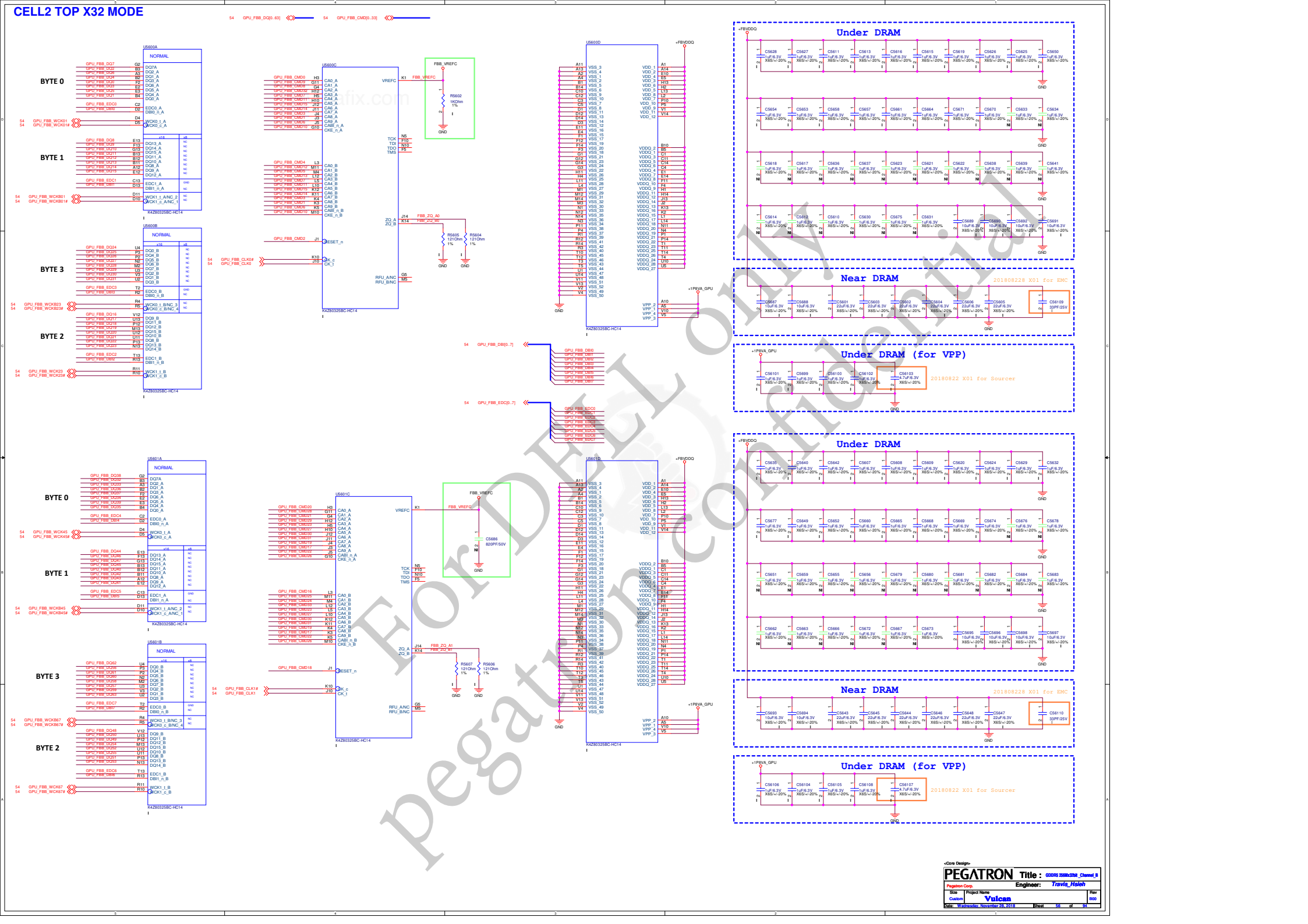
Size	Project Name	Rev
A2	Vulcan	B00

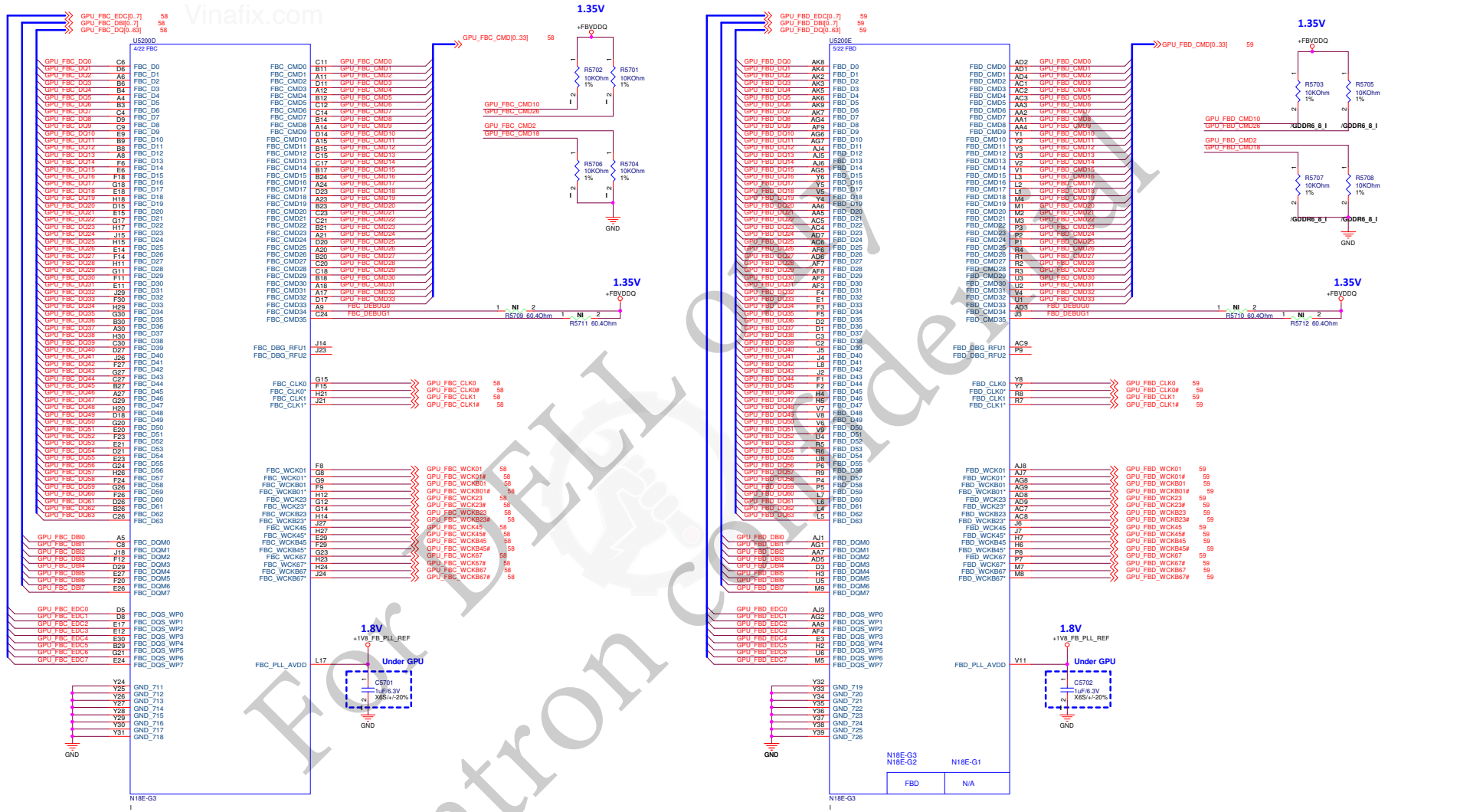
Date: Wednesday, November 28, 2018 Sheet 54 of 84

CELL1 TOP X32 MODE



CELL2 TOP X32 MODE





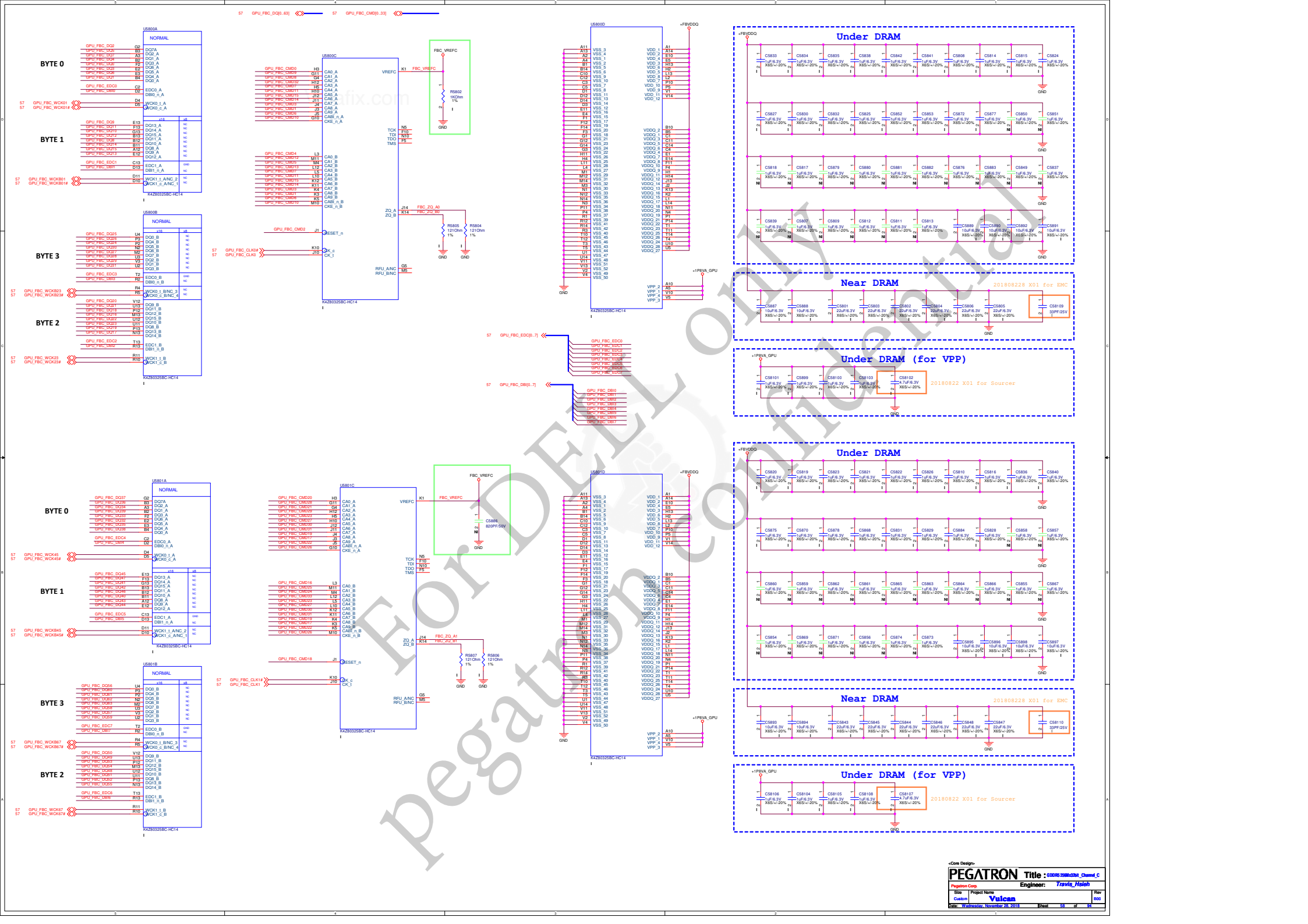
<Core Design>

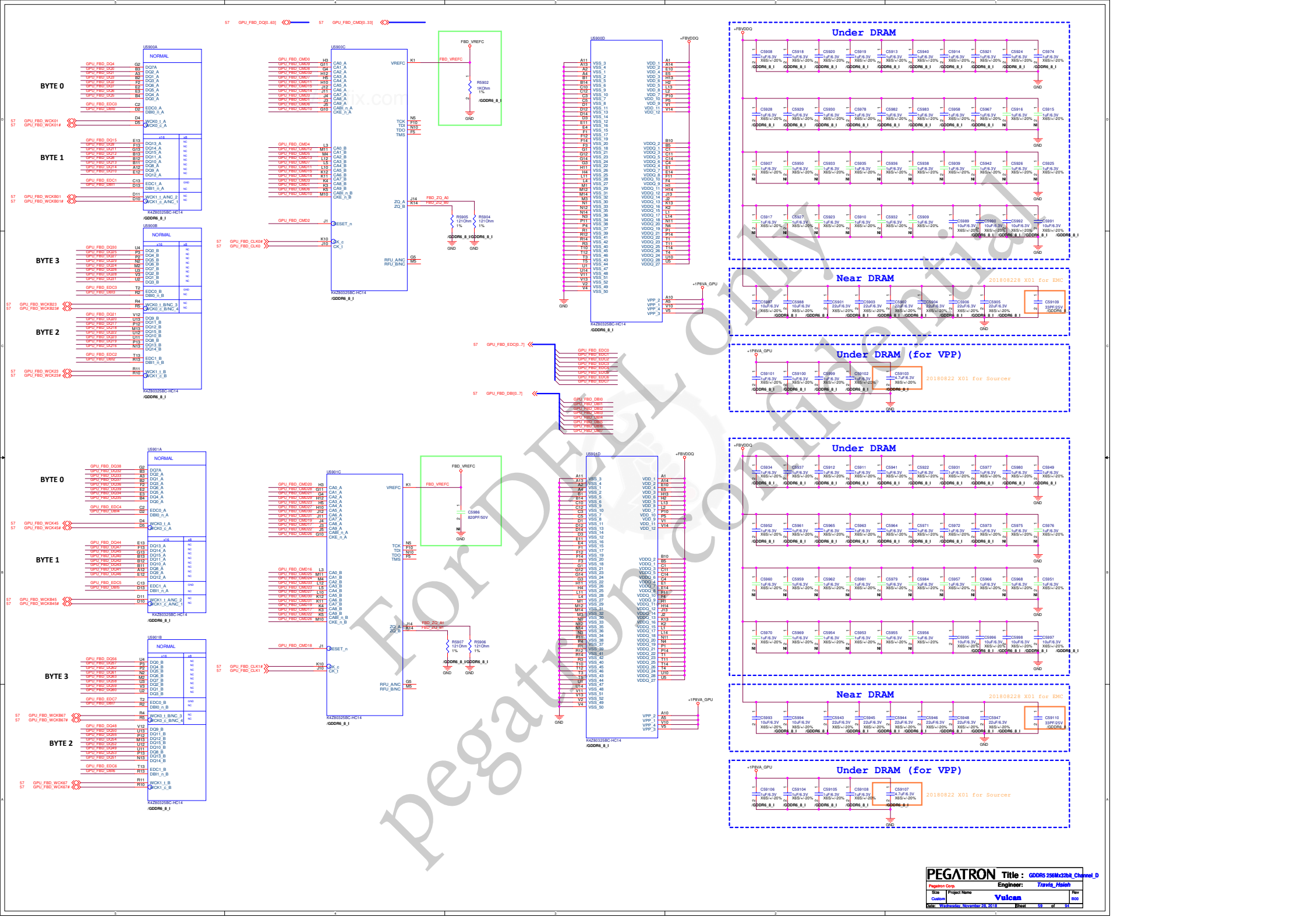
PEGATRON Title : GPU-BUFFER PARTITION C/D

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 57 of 94


BYTE 0
BYTE 1
BYTE 3
BYTE 2
Under DRAM
Near DRAM
Under DRAM (for VPP)
201808228 X01 for EMC
20180822 X01 for Sourcer
PEGATRON
Title : DDDR5 256Mx32bit_Channel_C
Engineer: Travis_Hsieh
Vulcan
Wednesday, November 28, 2018
For DELL only
pegatron confidential

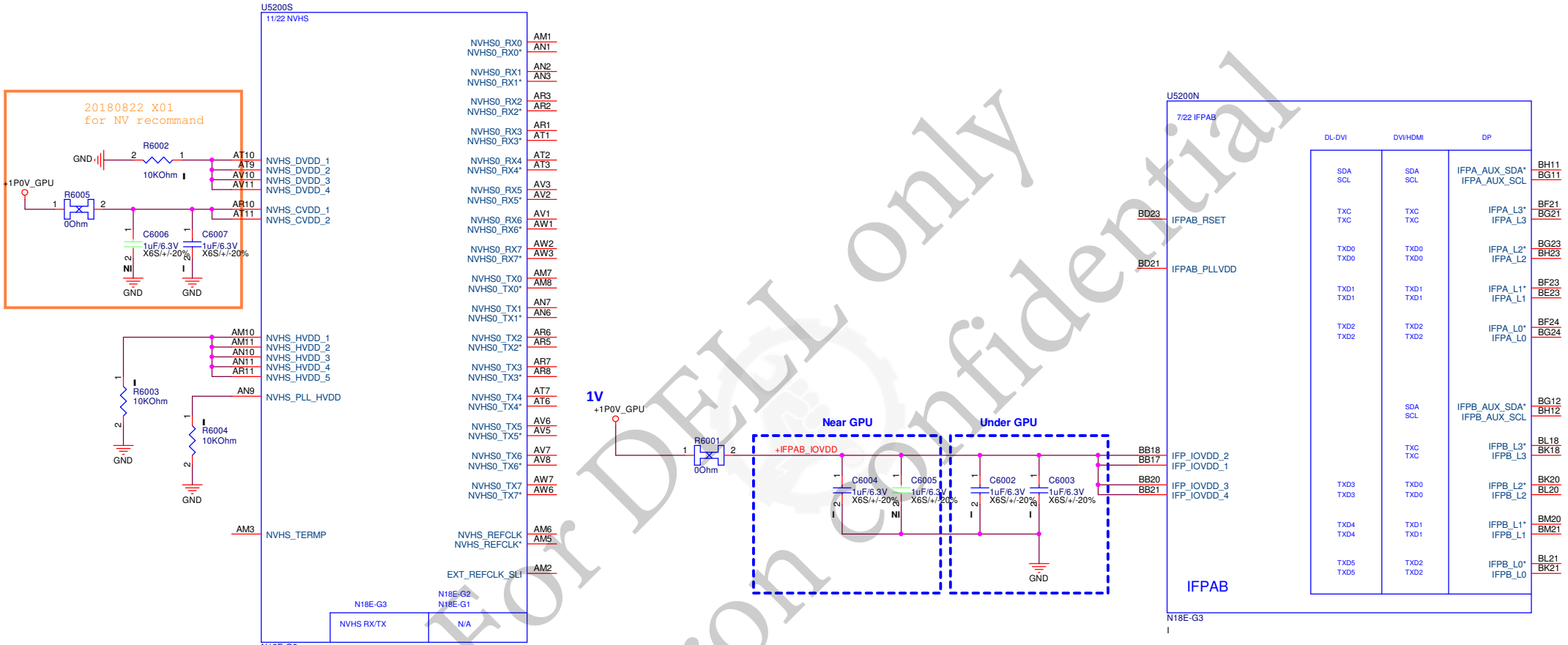


PEGATRON Title : GDDR5 256Mx32bit_Channel_D

Pegatron Corp. Engineer: Travis_Hsieh

Size: Custom | Project Name: Vulcan | Rev: B00

Date: Wednesday, November 28, 2018 | Sheet 59 of 94



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GPU_MIO

Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A3	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 60 of 94

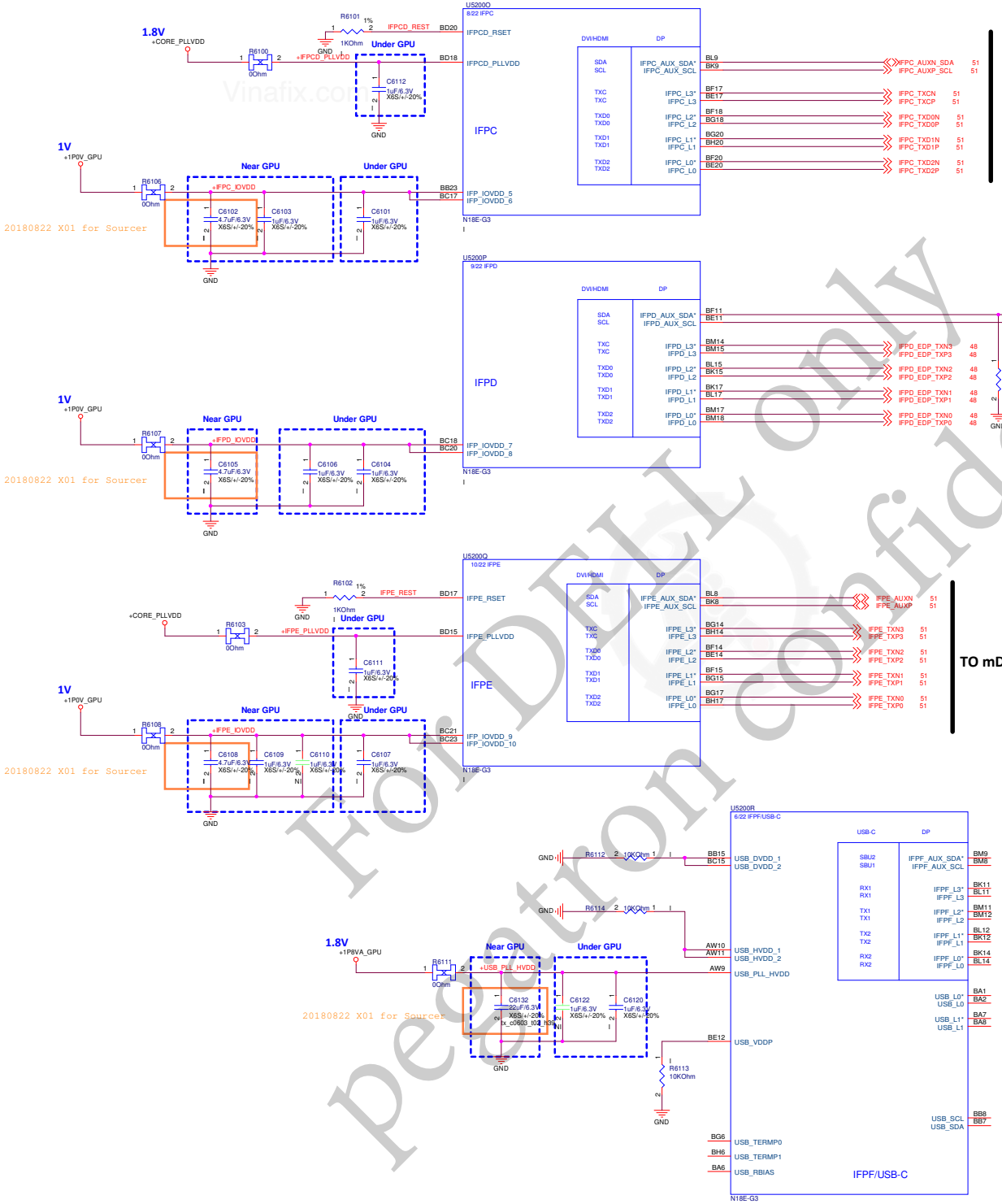


Table 9.6 HDMI Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA

Table 9.11 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFP_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA
IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

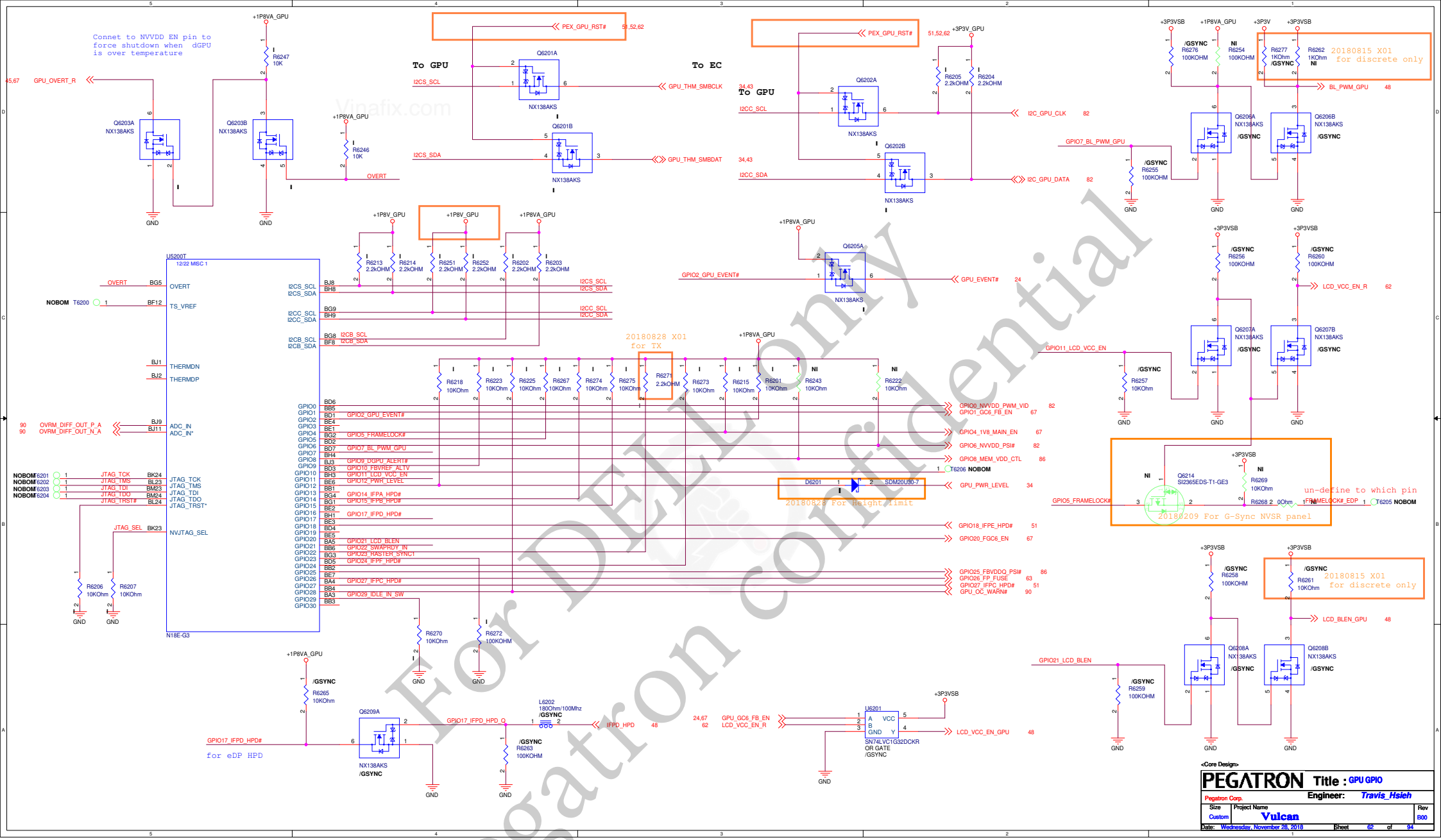
<Core Design>

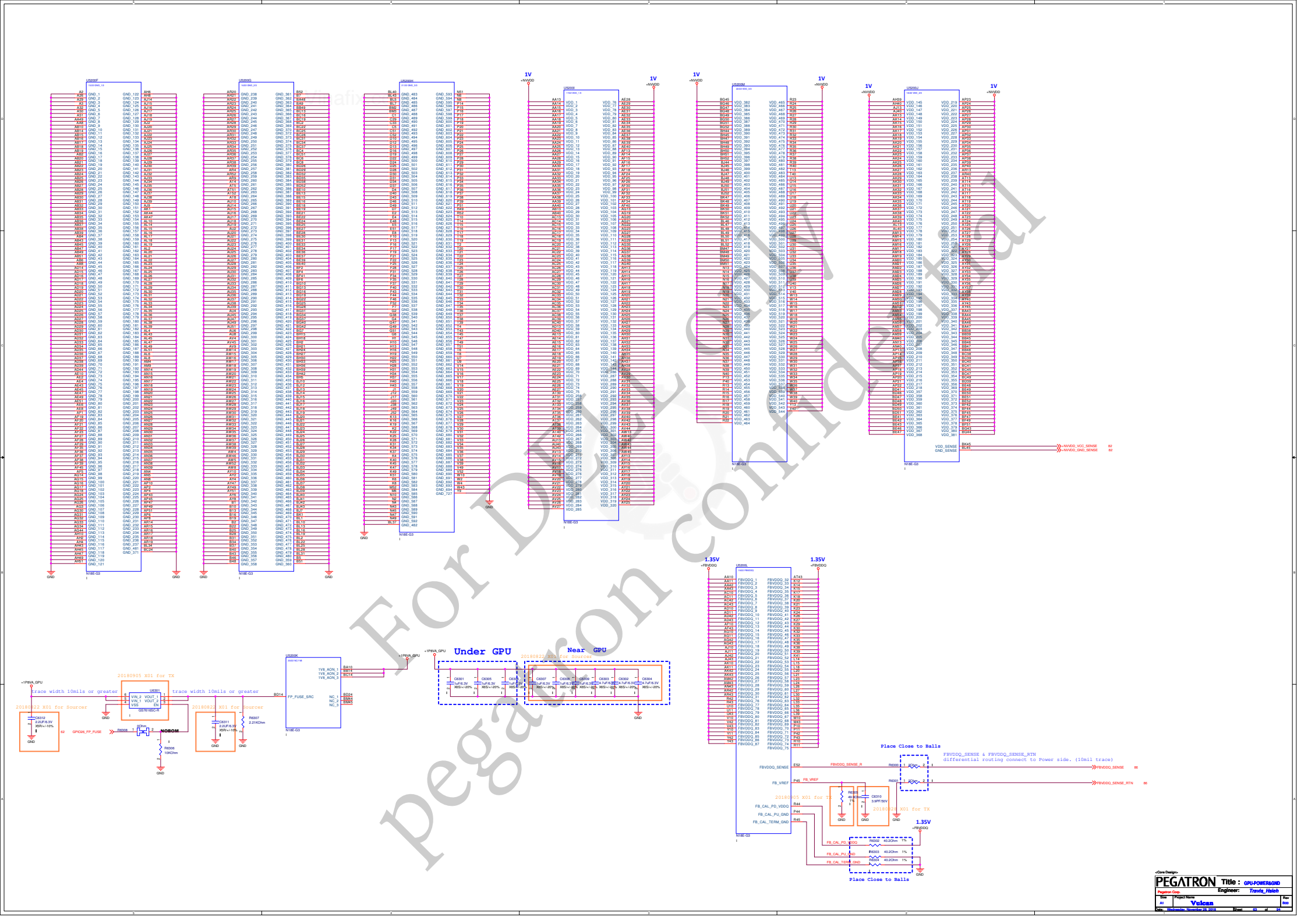
PEGATRON Title : GPU mini DP/HDMI/MUX

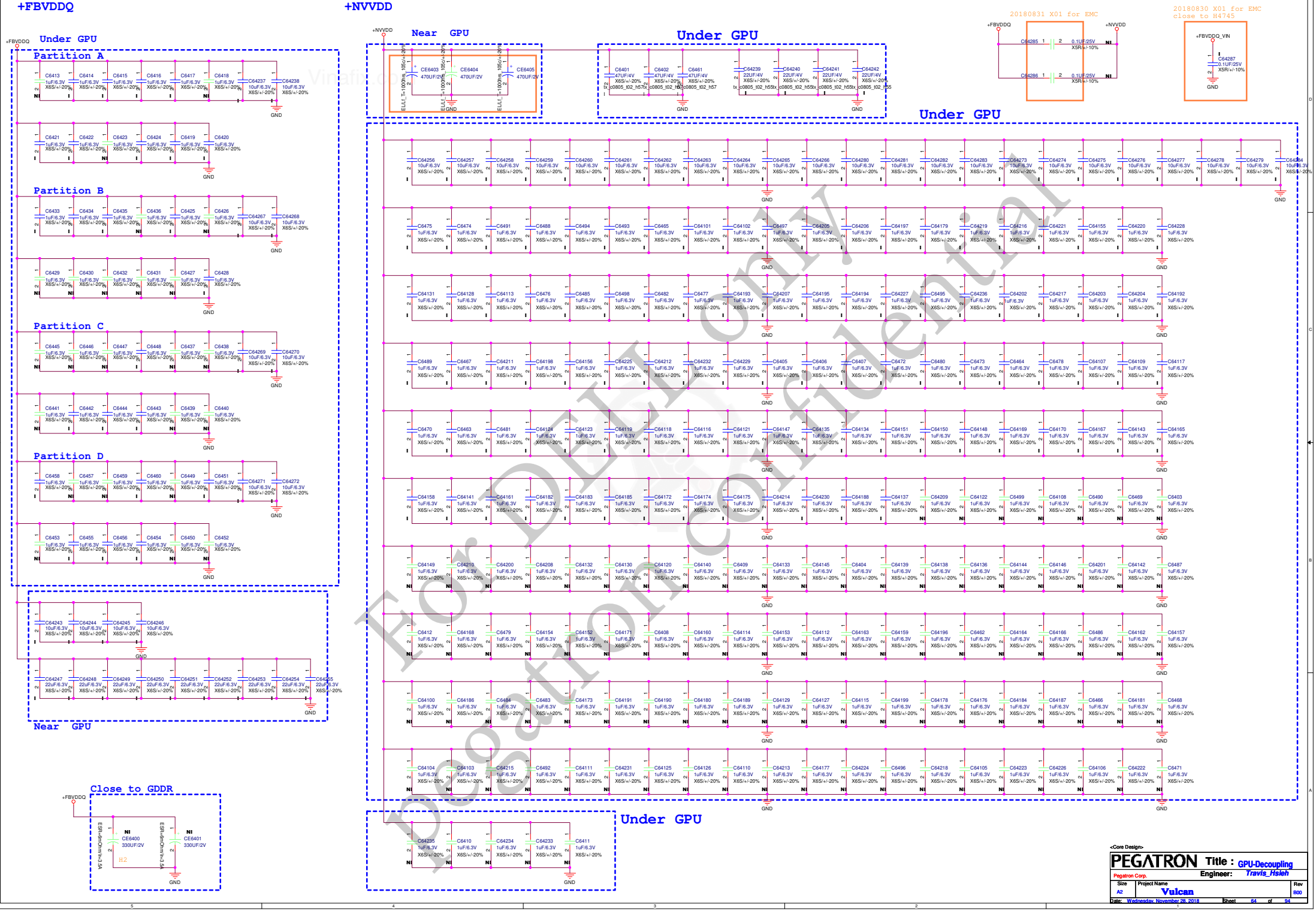
Pegatron Corp. Engineer: Travis_Hsieh

Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 61 of 94







<Core Design>

PEGATRON Title : GPU-Decoupling

Pegatron Corp. Engineer: Travis_Hsieh

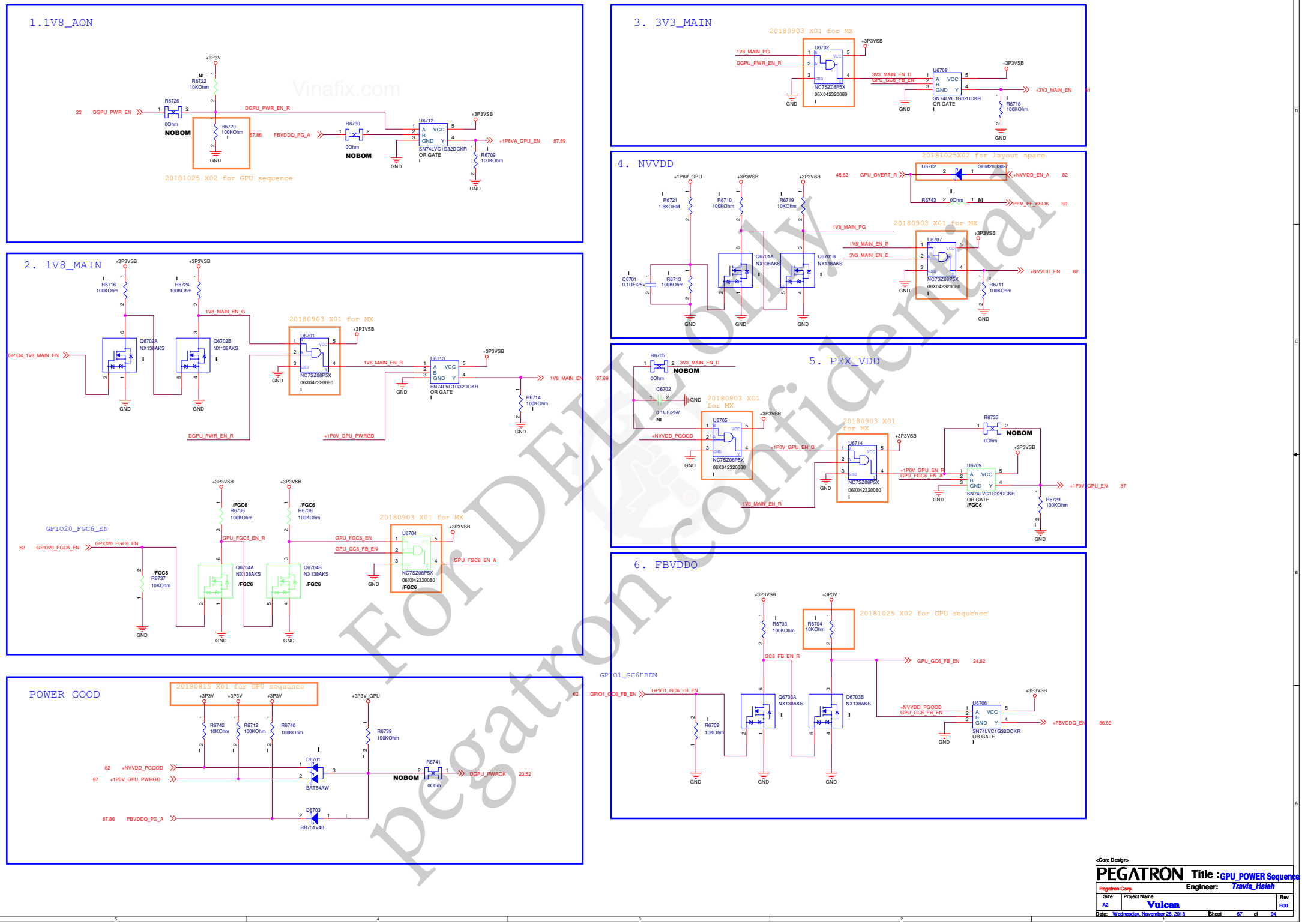
Size	Project Name	Rev
A2	Vulcan	B00

Date: Wednesday, November 28, 2018 Sheet 64 of 94

PEGATRON	Title : TYPE-C_PD		
Pegatron Corp.	Engineer: Travis_Hsieh		
Size: C	Project Name: Vulcan		Rev: B00
Date: Wednesday, November 28, 2018	Sheet 65 of 94		

PEGATRON DT-MB RESTRICTED SECRET

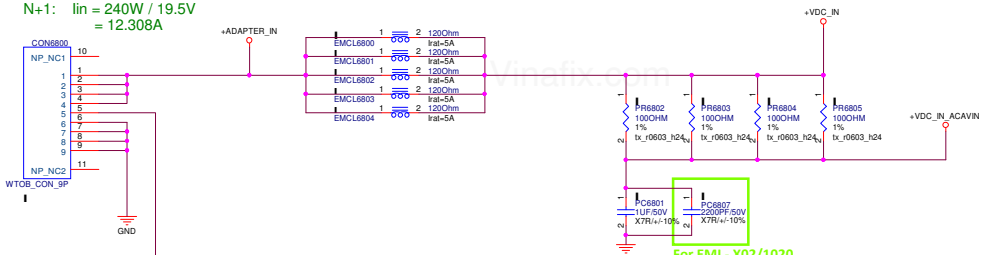
PEGATRON	Title : Type-C MUX	
Pegatron Corp.	Engineer: Travis_Hsieh	
Size: Custom	Project Name: Vulcan	Rev: 800
Date: Wednesday, November 28, 2018	Sheet 68 of 94	


1.1V8_AON
20181025 X02 for GPU sequence
2. 1V8_MAIN
20180903 X01 for MX
GPIO20_FGC6_EN
3. 3V3_MAIN
20180903 X01 for MX
4. NVVDD
20181025X02 for layout space
20180903 X01 for MX
5. PEX_VDD
20180903 X01 for MX
6. FBVDDQ
20181025 X02 for GPU sequence
POWER GOOD
20180815 X01 for GPU sequence
NOBOM
Vinafix.com
For DELL Only
pegatron confidential

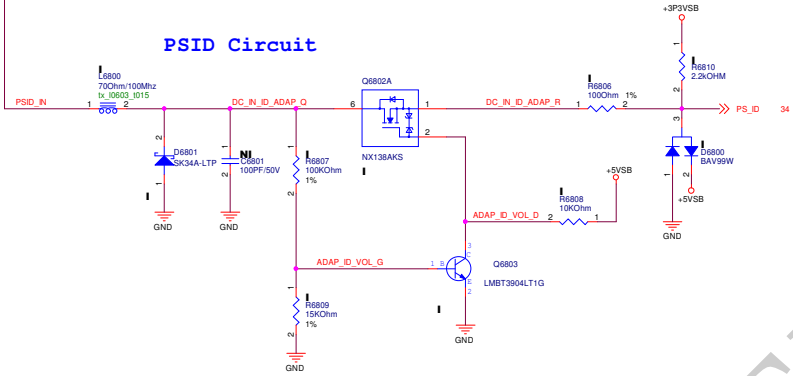
DC-IN connector

N : Iin = 180W / 19.5V
= 9.231A

N+1: Iin = 240W / 19.5V
= 12.308A

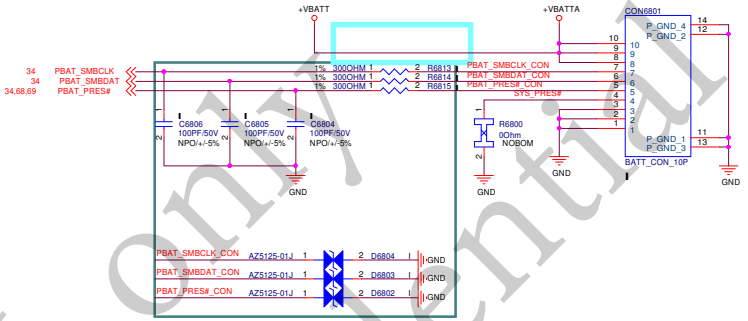


PSID Circuit



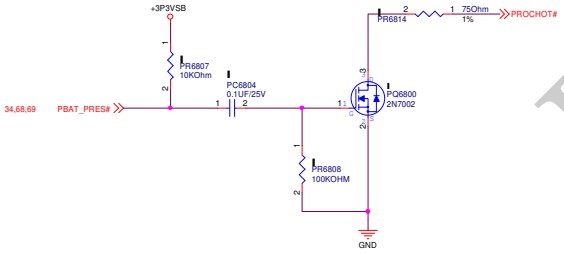
Remove JP6800 and JP6801

Battery Pack connector

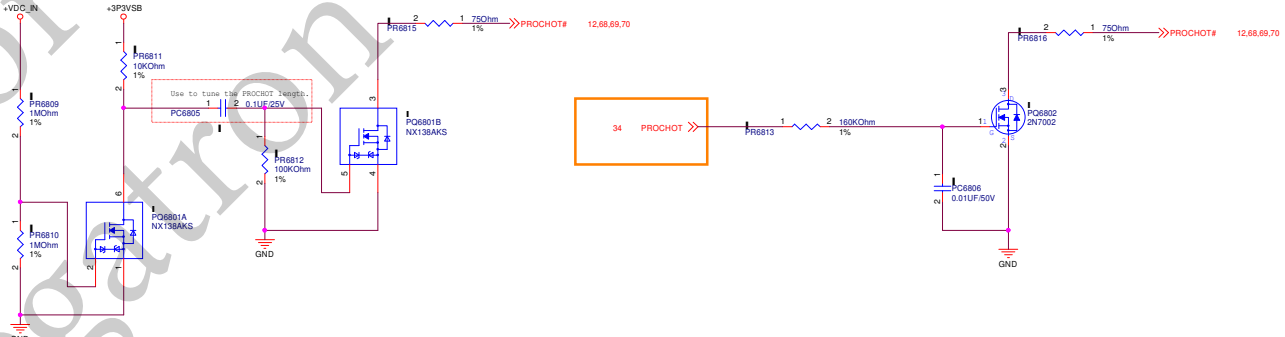


For Battery damage EC issue - X01/0824

Adapter Protection Circuit



Battery Protection Circuit



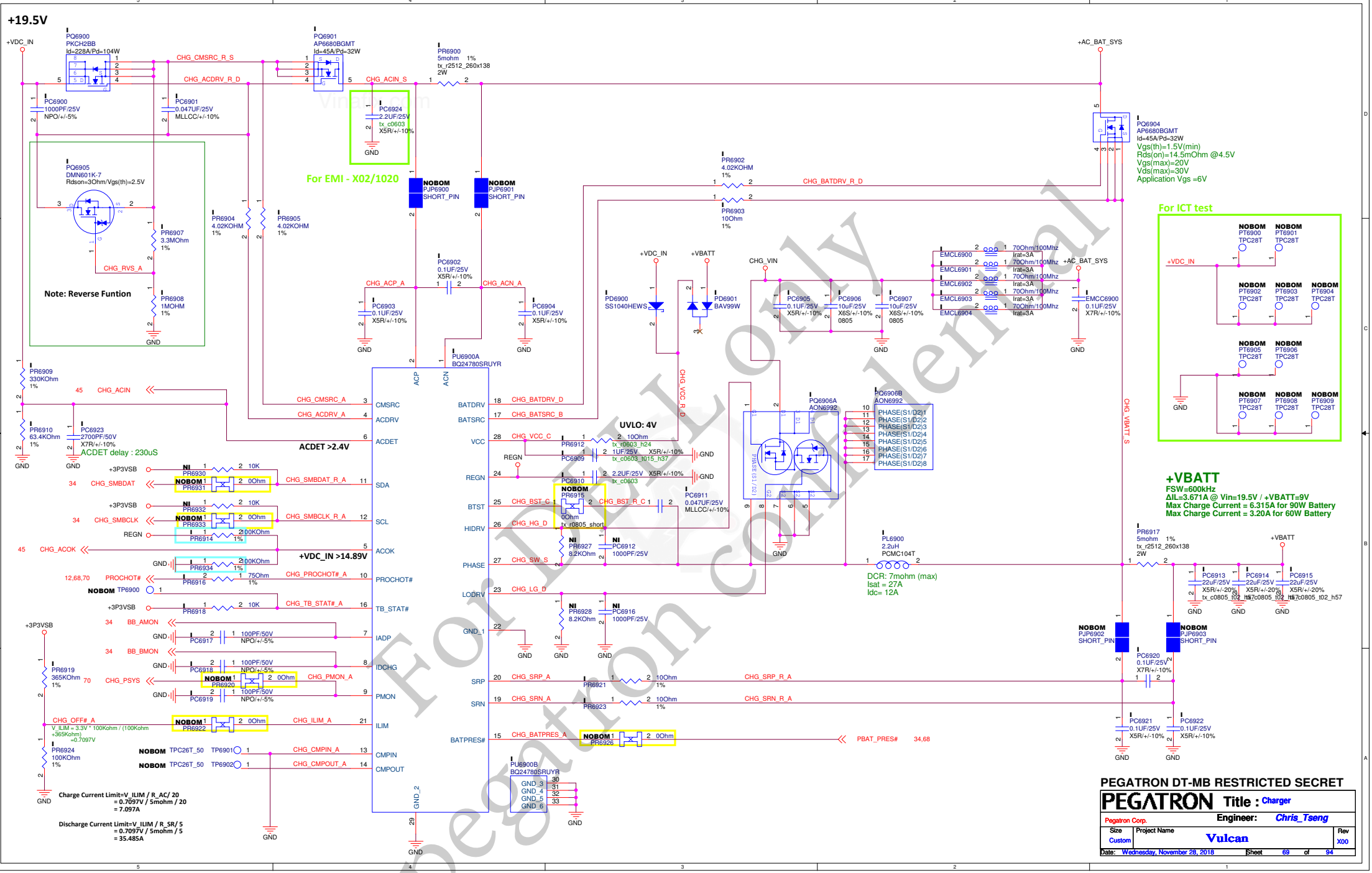
<Core Design>

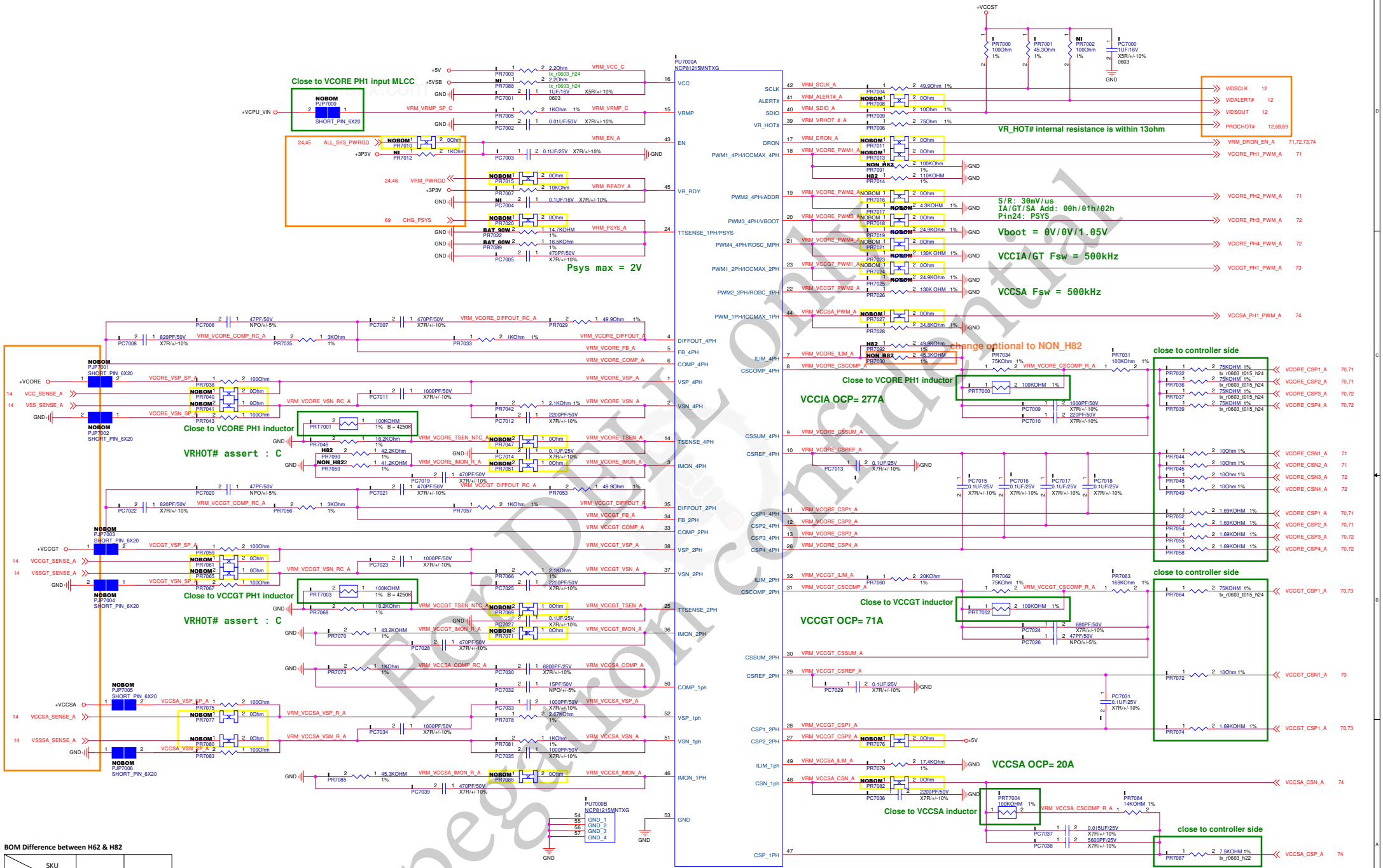
PEGATRON Title : DC_IN

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A2	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 68 of 94



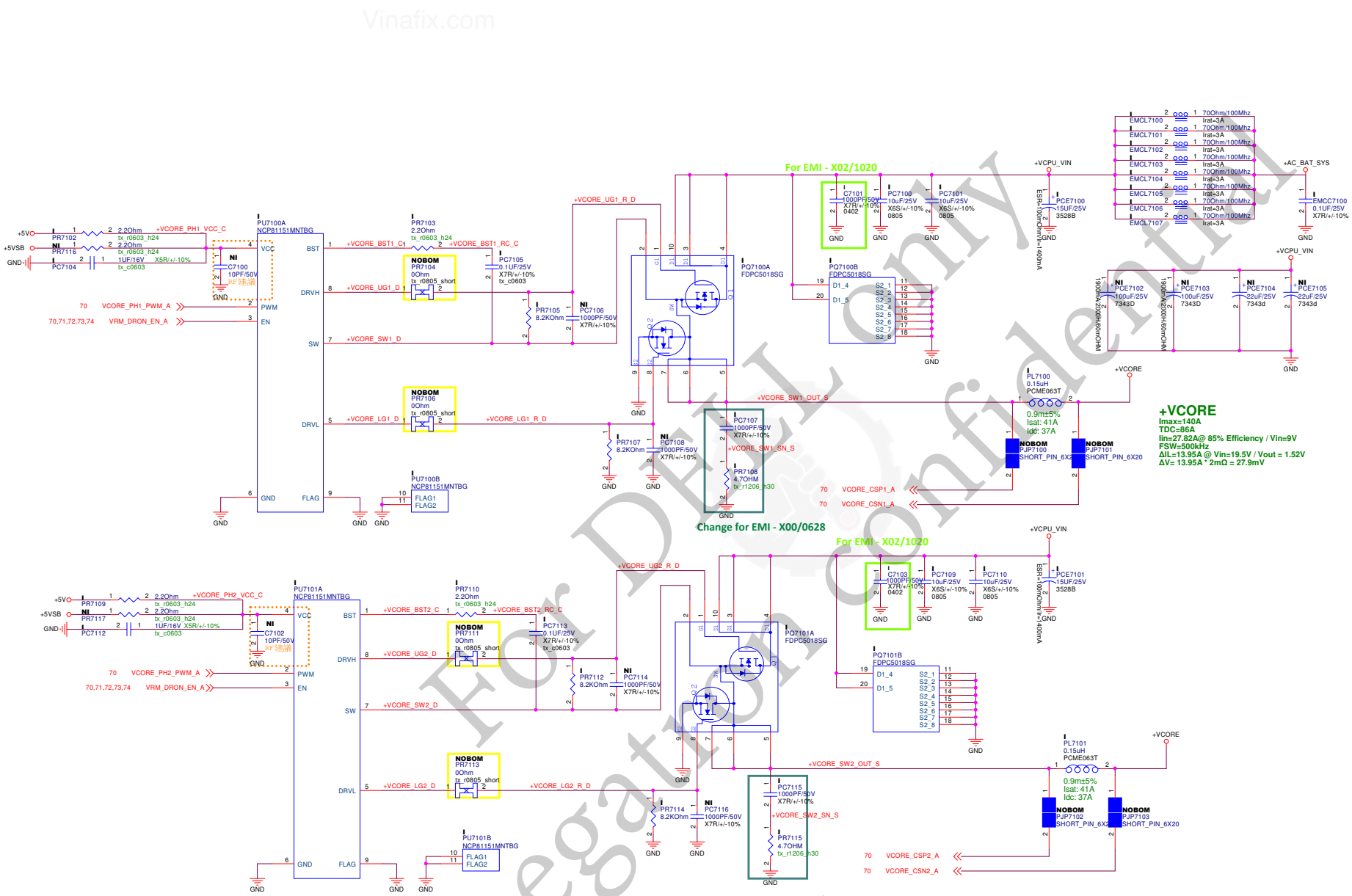


BOM Difference between H62 & H82

SKU / Part Reference	H62	H82
PR7050 / PR7090	41.2KΩ	42.2KΩ
PR7014 / PR7091	110KΩ	100KΩ
PR7030 / PR7092	45.3KΩ (OCP = 252A)	49.9KΩ (OCP = 277A)

<Core Design>

PEGATRON Title : VR CONTROLLER
Pegatron Corp. Engineer: Chris_Tseng
Size A2 | Project Name Vulcan | Rev X00
Date: Wednesday, November 28, 2018 | Sheet 70 of 94



OWNER	+VCORE OC Point	Low Limit	High Limit
Atticus	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)
Terry	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)

I_Low Limit = I_DVID + Io_Cout
= 26A + (30mV/uS) * 1748uF
= 78.44A

※ Controller will shut down after 50uS when 184.99A ≤ Iout < 277.49A
Controller will shut down immediately when Iout trigger 277.49A

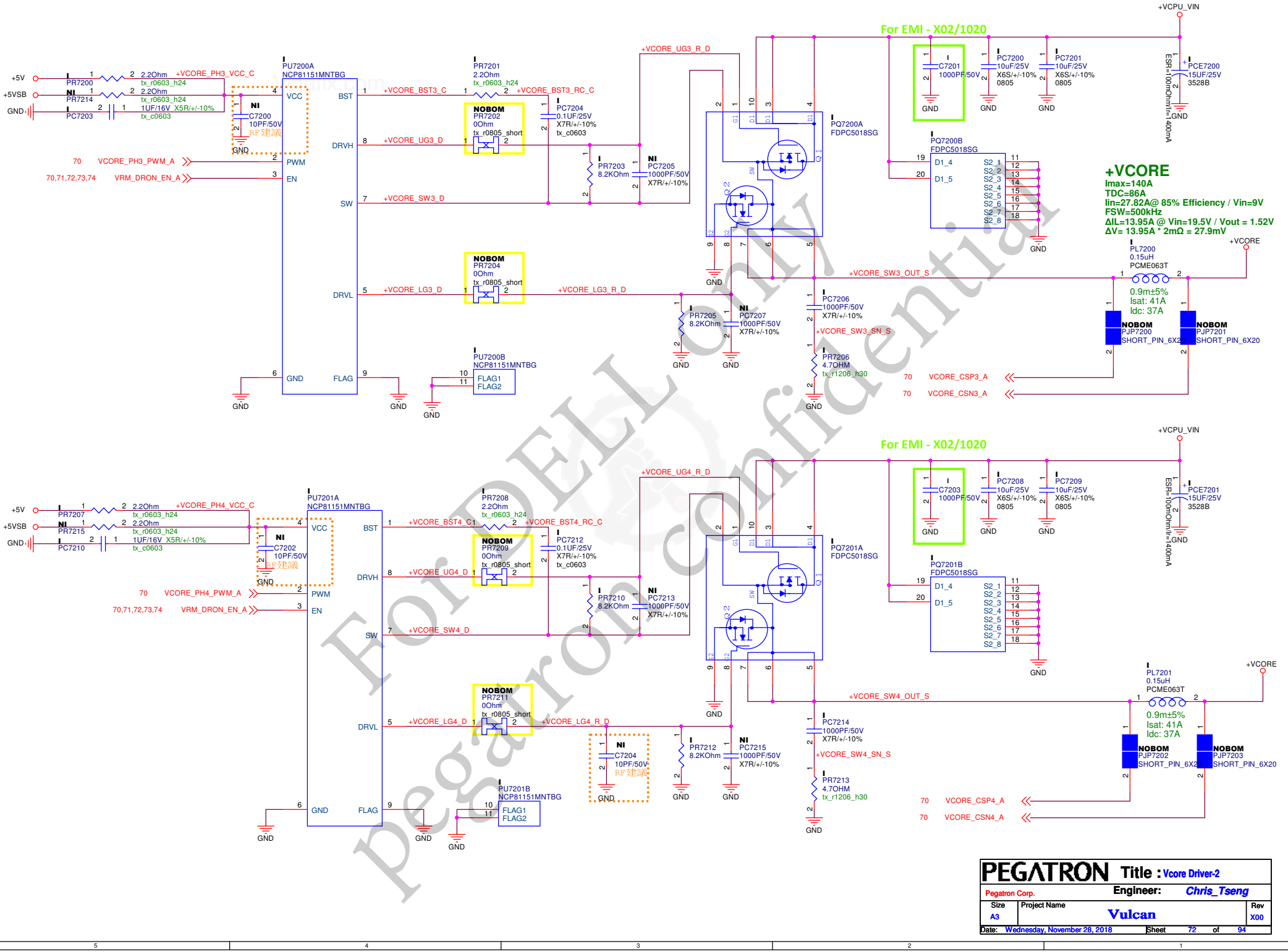
PEGATRON DT-MB RESTRICTED SECRET

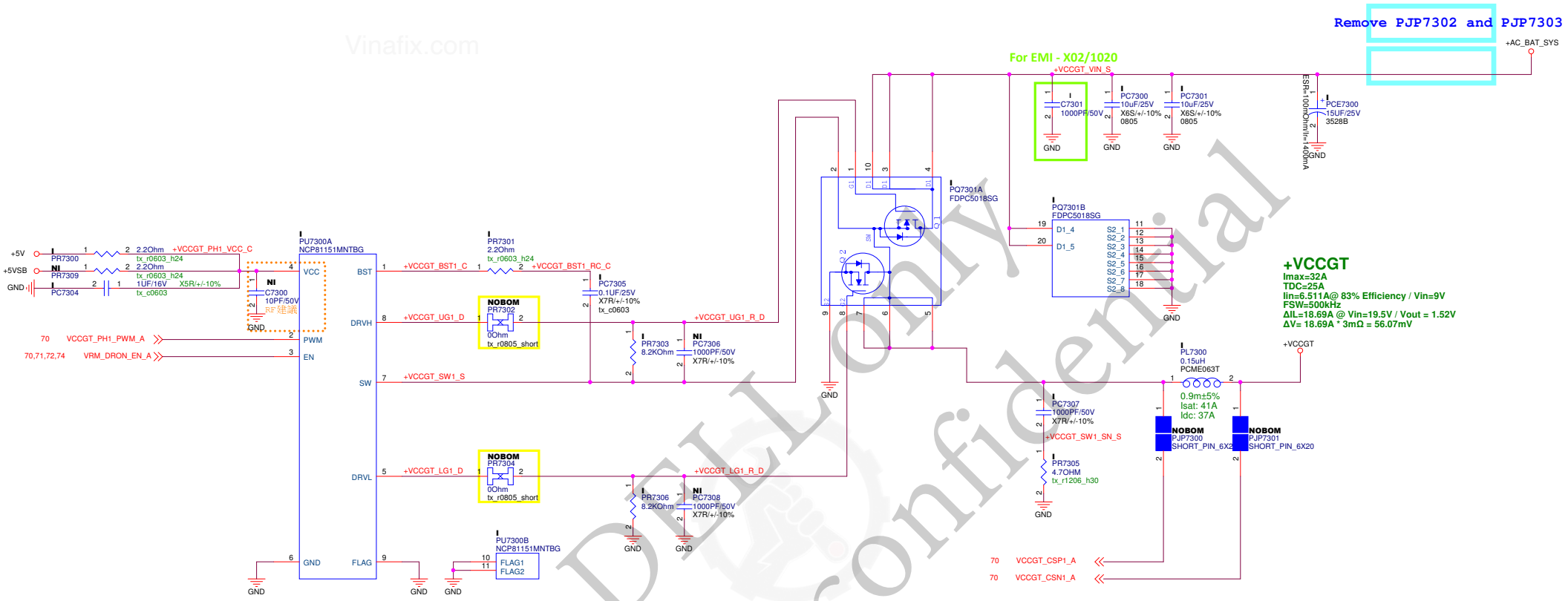
PEGATRON Title : Vcore Driver-1

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 71 of 94





+VCCGT
Imax=32A
TDC=25A
Iin=6.511A@ 83% Efficiency / Vin=9V
FSW=500kHz
ΔIL=18.69A @ Vin=19.5V / Vout = 1.52V
ΔV= 18.69A * 3mΩ = 56.07mV

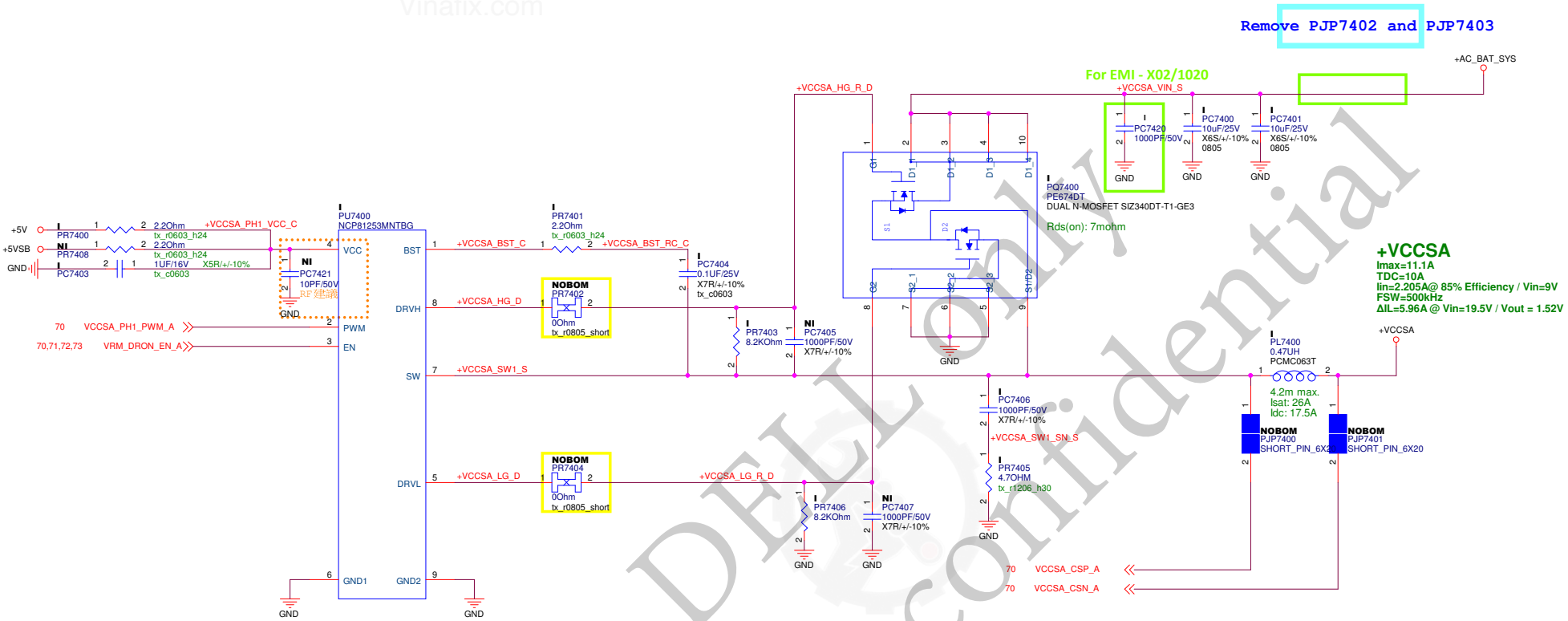
OWNER	+VCCGT OC Point	Low Limit	High Limit
Atticus	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A
Terry	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A

I_Low Limit = I_DVID + Io_Cout
= 8A + (30mV/uS) * 1156uF
= 42.68A

※ Controller will shut down after 50uS when 47.51A ≤ Iout < 71.27A
Controller will shut down immediately when Iout trigger 71.27A

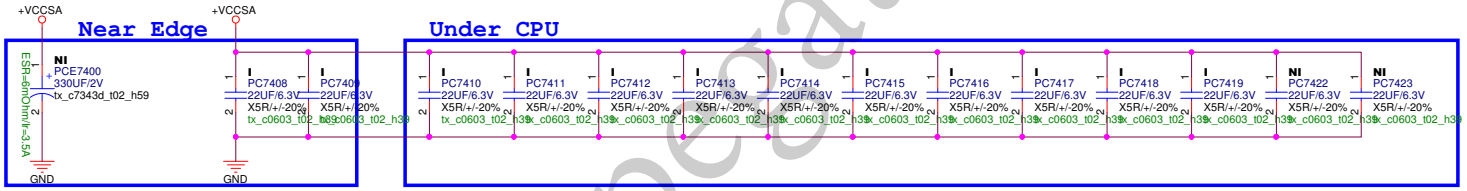
PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON Title : VccGT Driver
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 73 of 94



OWNER	+VCCSA OC Point	Low Limit	High Limit
Atticus	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A
Terry	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A

I_Low Limit = I_DVID + Io_Cout
= 5A + (30mV/μS) * 265uF
= 12.95A



VCCSA Output CAP

330uF/2V/H=2mm * 1(NI)
22uF/6.3V * 12 (I)
22uF/6.3V * 2 (NI)

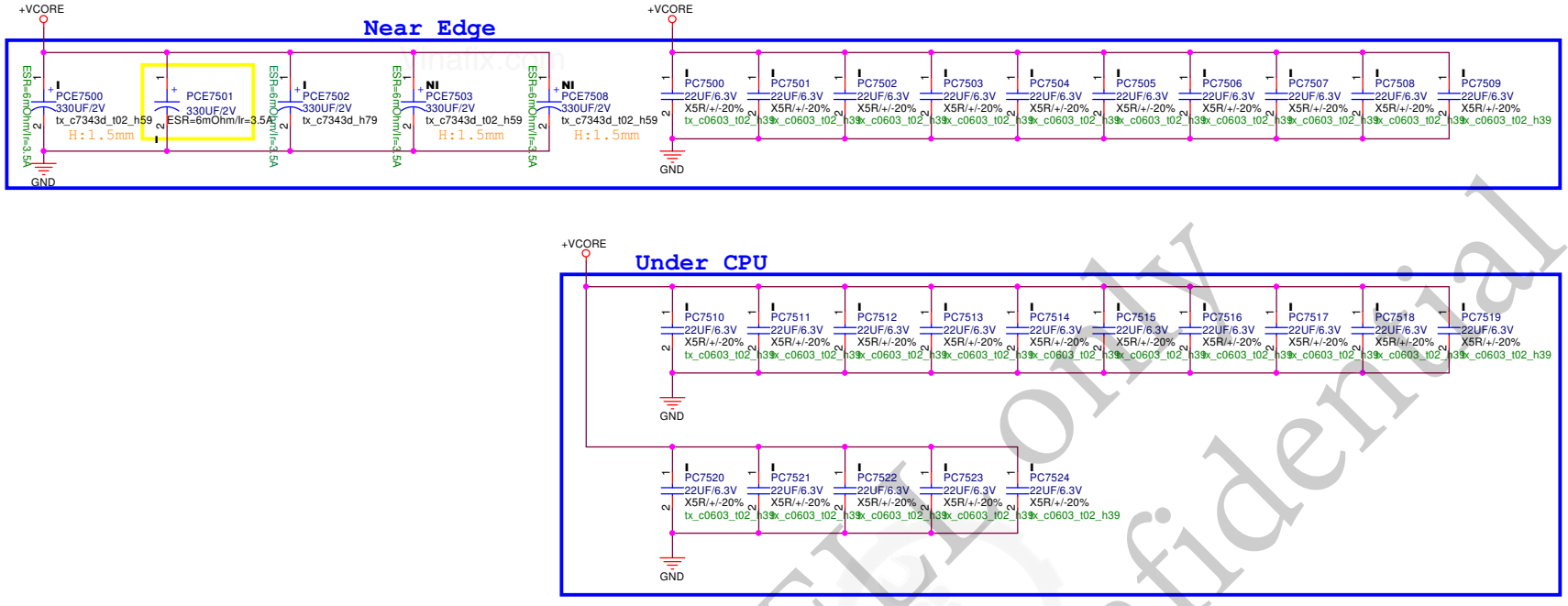
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VccSA Driver

Pegatron Corp. Engineer: Chris_Tseng

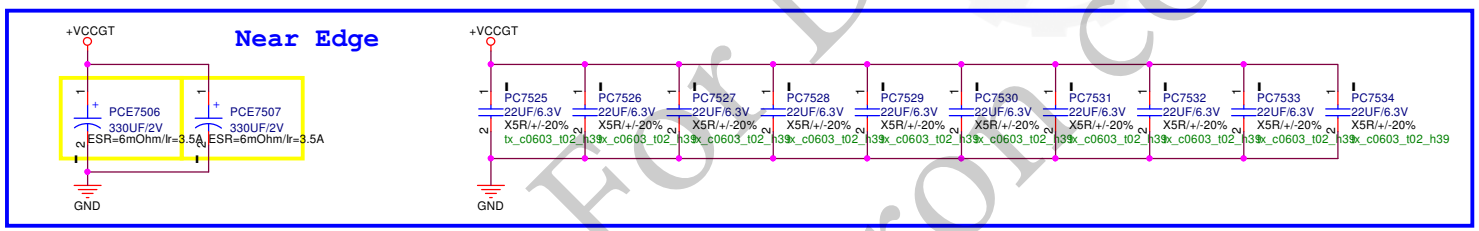
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 74 of 94



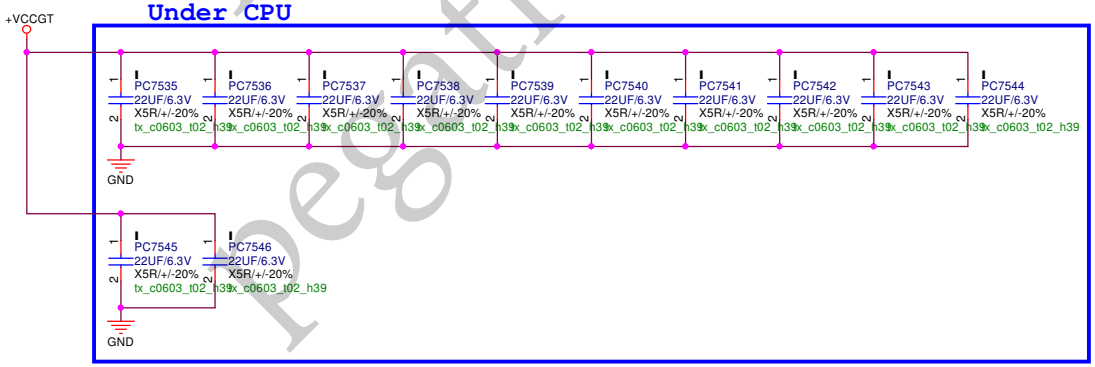
Vcore Output CAP

330uF/2V/H=2mm * 2 (I)
330uF/2V/H=1.5mm * 1(I)
330uF/2V/H=1.5mm * 2(NI)
22uF * 25

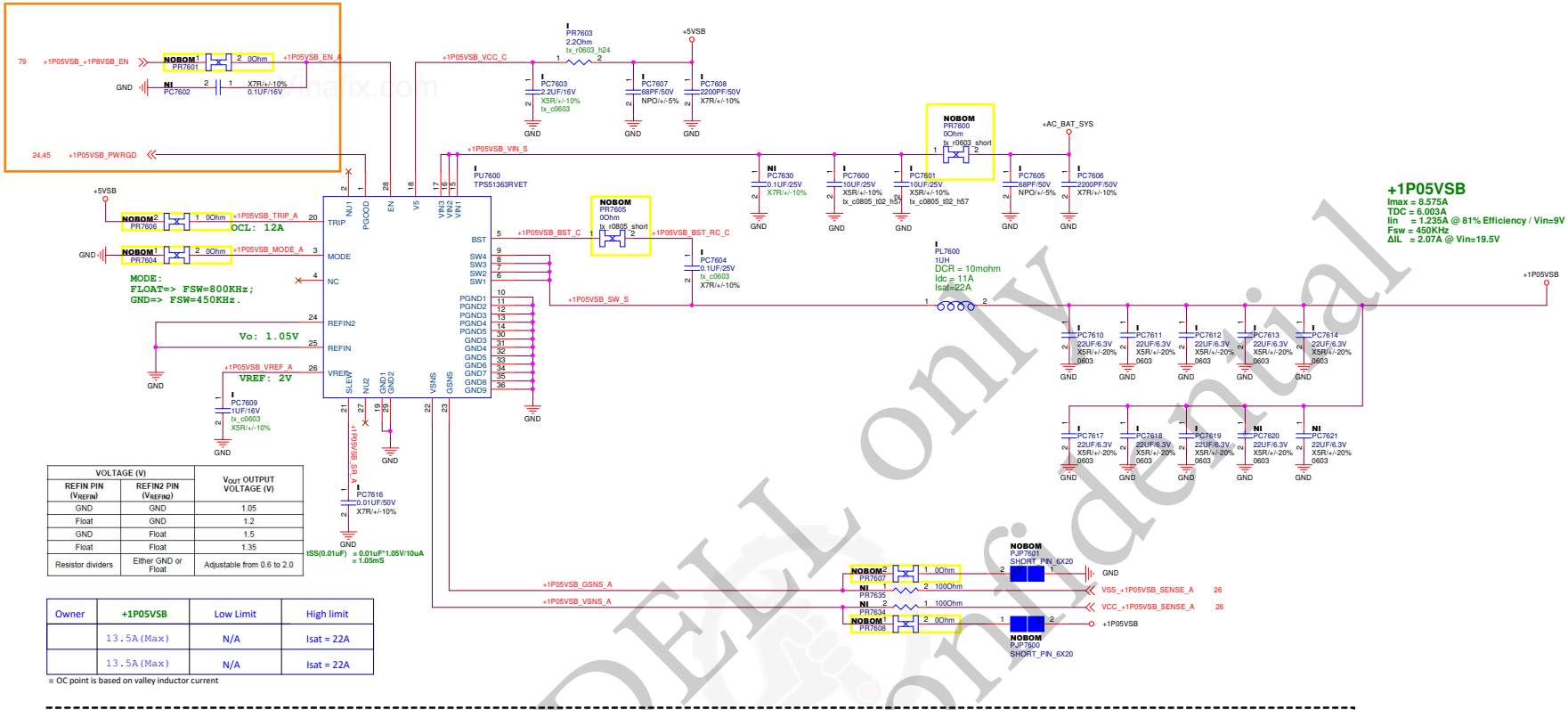


VCCGT Output CAP

330uF/2V/H=2mm * 2 (I)
22uF * 22



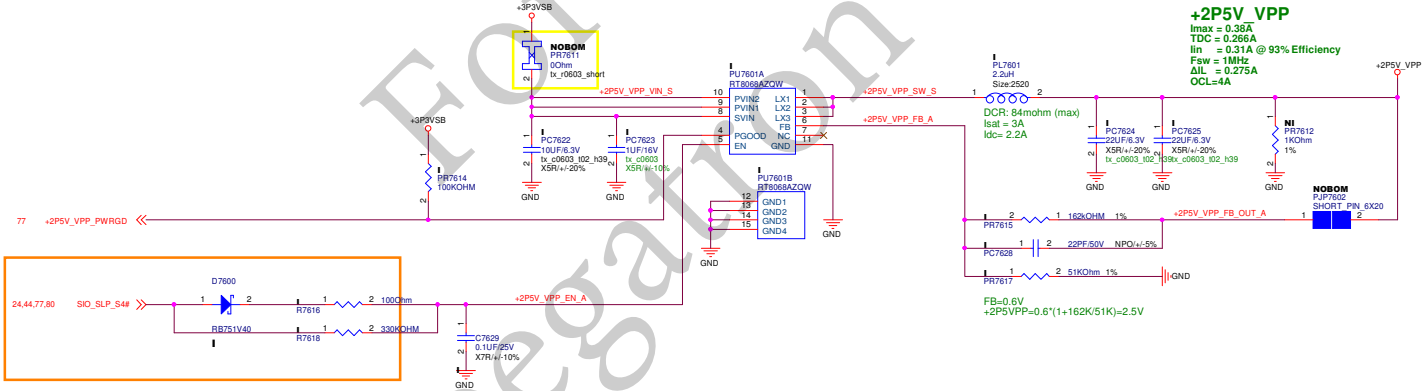
PEGATRON	Title :	Vcore & VccGT CAP
Pegatron Corp.	Engineer:	Chris_Tseng
Size: A3	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 75 of 94	



VOLTAGE (V)		V_{OUT} OUTPUT VOLTAGE (V)
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

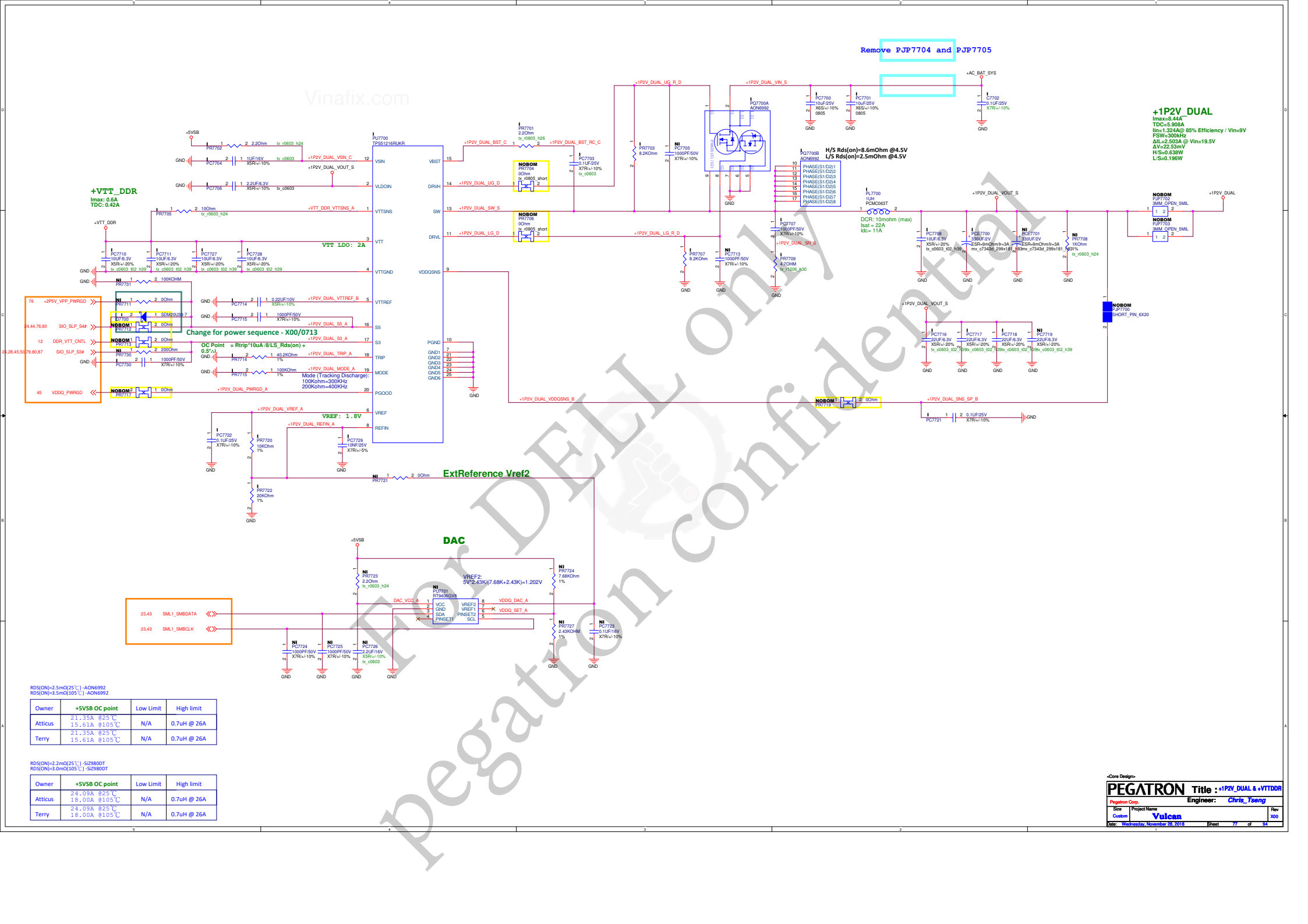
Owner	+1P05VSB	Low Limit	High limit
	13.5A(Max)	N/A	Isat = 22A
	13.5A(Max)	N/A	Isat = 22A

※ OC point is based on valley inductor current



Owner	+2P5V_VPP	Low Limit	High limit
	4.0A	N/A	0.66uH @ 6A
	4.0A	N/A	0.66uH @ 6A

※ OC point is based on peak inductor current



RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992

Owner	+5VSB OC point	Low Limit	High limit
Atticus	21.35A @25℃ 15.61A @105℃	N/A	0.7uH @ 26A
Terry	21.35A @25℃ 15.61A @105℃	N/A	0.7uH @ 26A

RDS(ON)=2.2mΩ(25℃) -SiZ980DT
RDS(ON)=3.0mΩ(105℃) -SiZ980DT

Owner	+5VSB OC point	Low Limit	High limit
Atticus	24.09A @25℃ 18.00A @105℃	N/A	0.7uH @ 26A
Terry	24.09A @25℃ 18.00A @105℃	N/A	0.7uH @ 26A

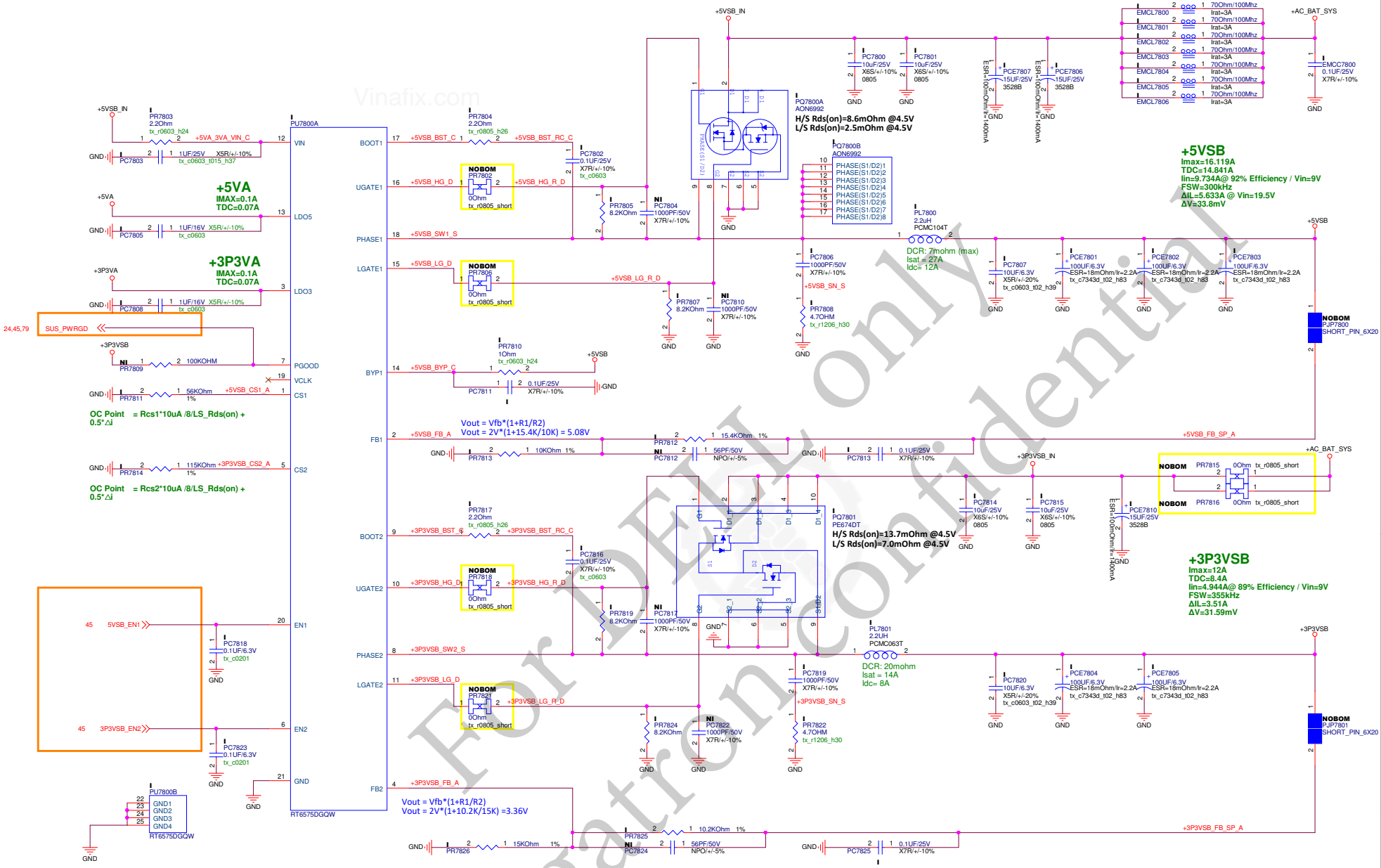
<Core Design>

PEGATRON Title : +1P2V_DUAL & +VTTDDR

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 77 of 94



RDS(ON)=2.5mΩ(25℃) -AON6992
RDS(ON)=3.5mΩ(105℃) -AON6992

Owner	+5VSB OC point	Low Limit	High limit
	30.82A @25℃ 22.82A @105℃	N/A	1.6uH @ 36A
	32.3165A @25℃ 23.89A @105℃	N/A	1.6uH @ 36A

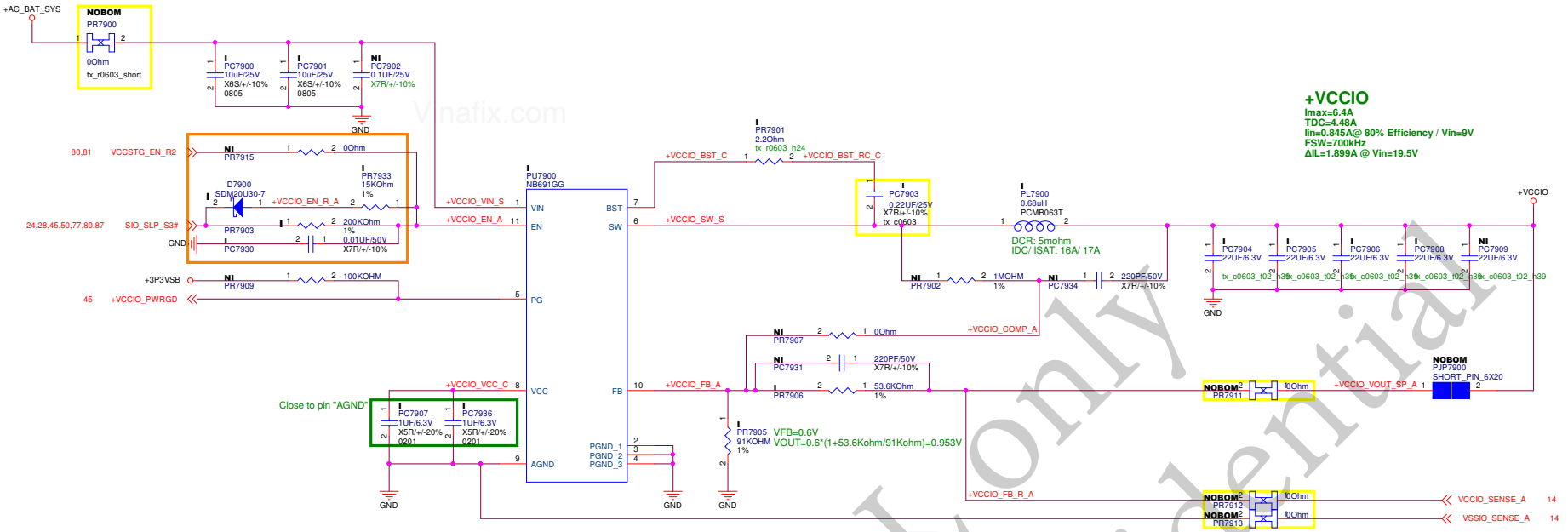
RDS(ON)=7.0mΩ(25℃) -SIZ340DT-T1-GE3
RDS(ON)=9.8mΩ(105℃) -SIZ340DT-T1-GE3

Owner	+3P3VSB OC point	Low Limit	High limit
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A
	22.29A @25C 16.463A @105C	N/A	1.5uH @ 23A

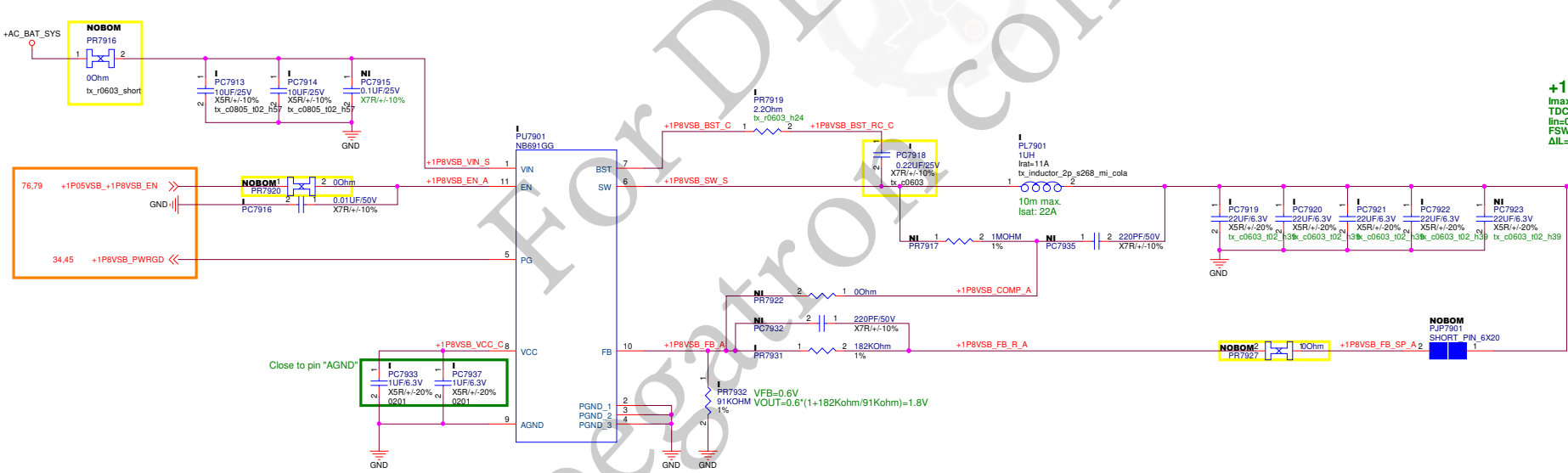
RDS(ON)=2.2mΩ(25℃) -SIZ980DT
RDS(ON)=3.08mΩ(105℃) -SIZ980DT

Owner	+5VSB OC point	Low Limit	High limit
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A
	34.63A @25℃ 25.54A @105℃	N/A	1.6uH @ 36A

PEGATRON Title : +3P3VSB / +5VSB
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 78 of 94



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 17A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 17A



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Atticus	7A (min.) 8A (max.)	N/A	L_Isat = 22A
Terry	7A (min.) 8A (max.)	N/A	L_Isat = 22A

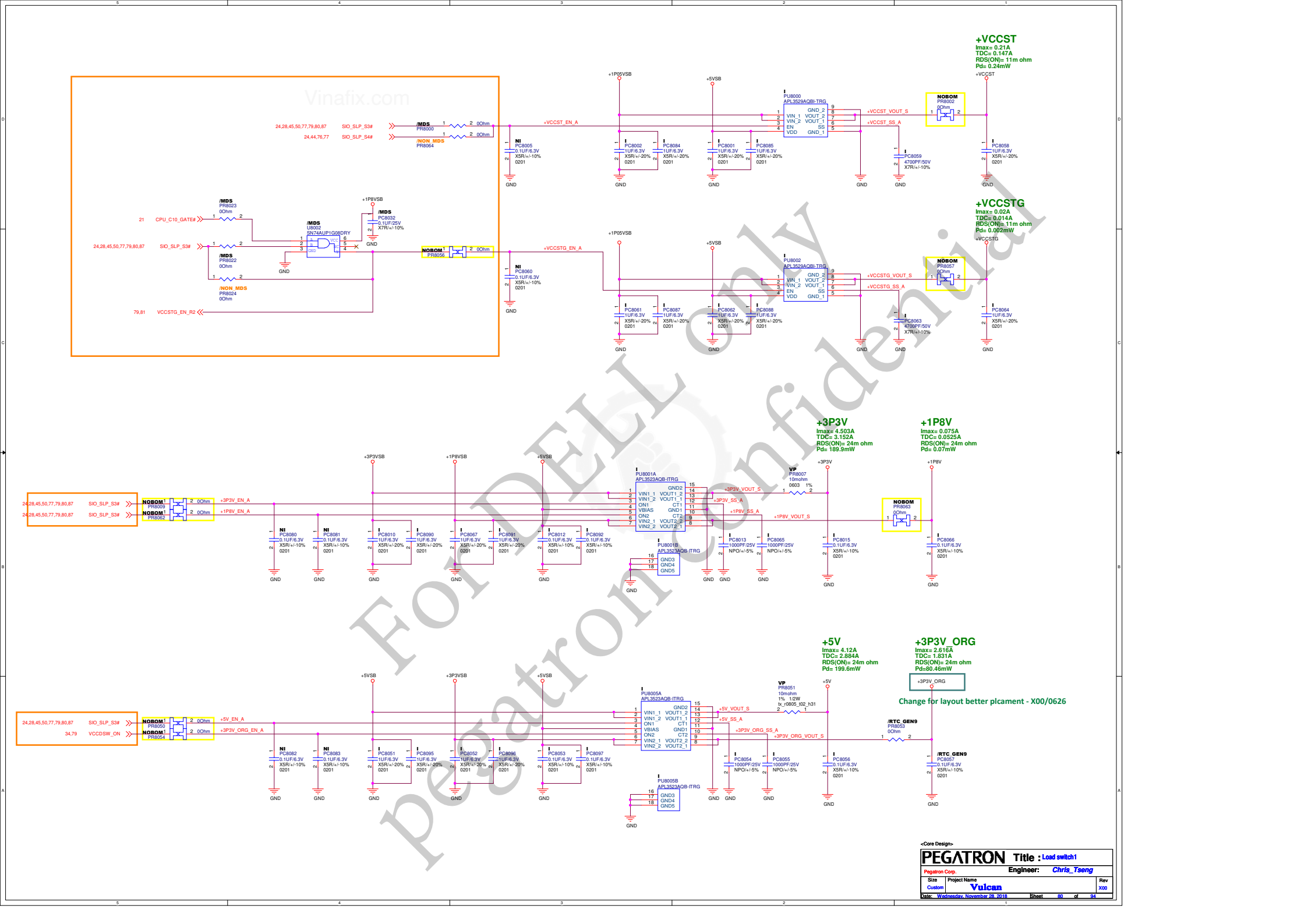
<Core Design>

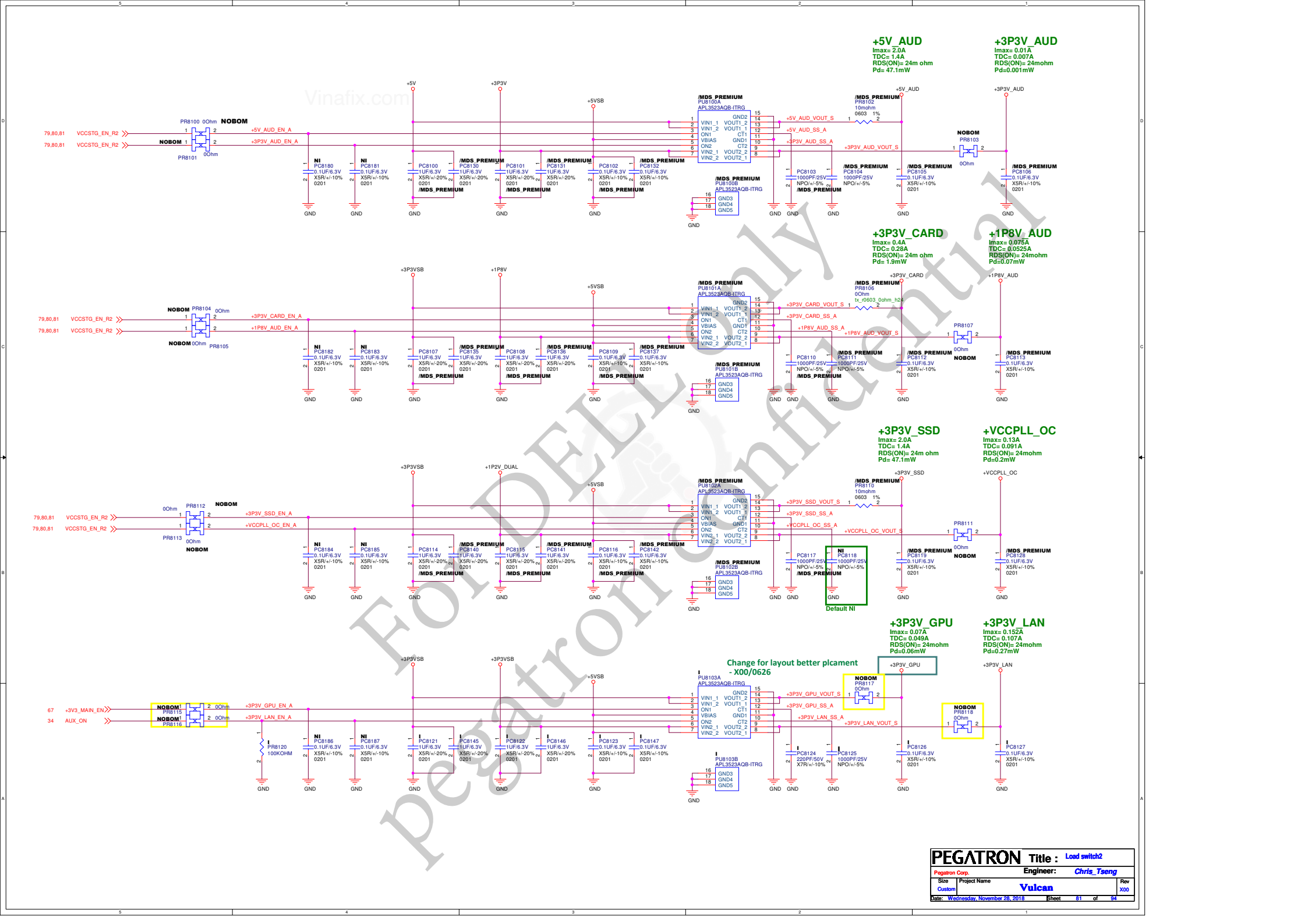
PEGATRON Title : 79.+VCCIO/ +1P8V

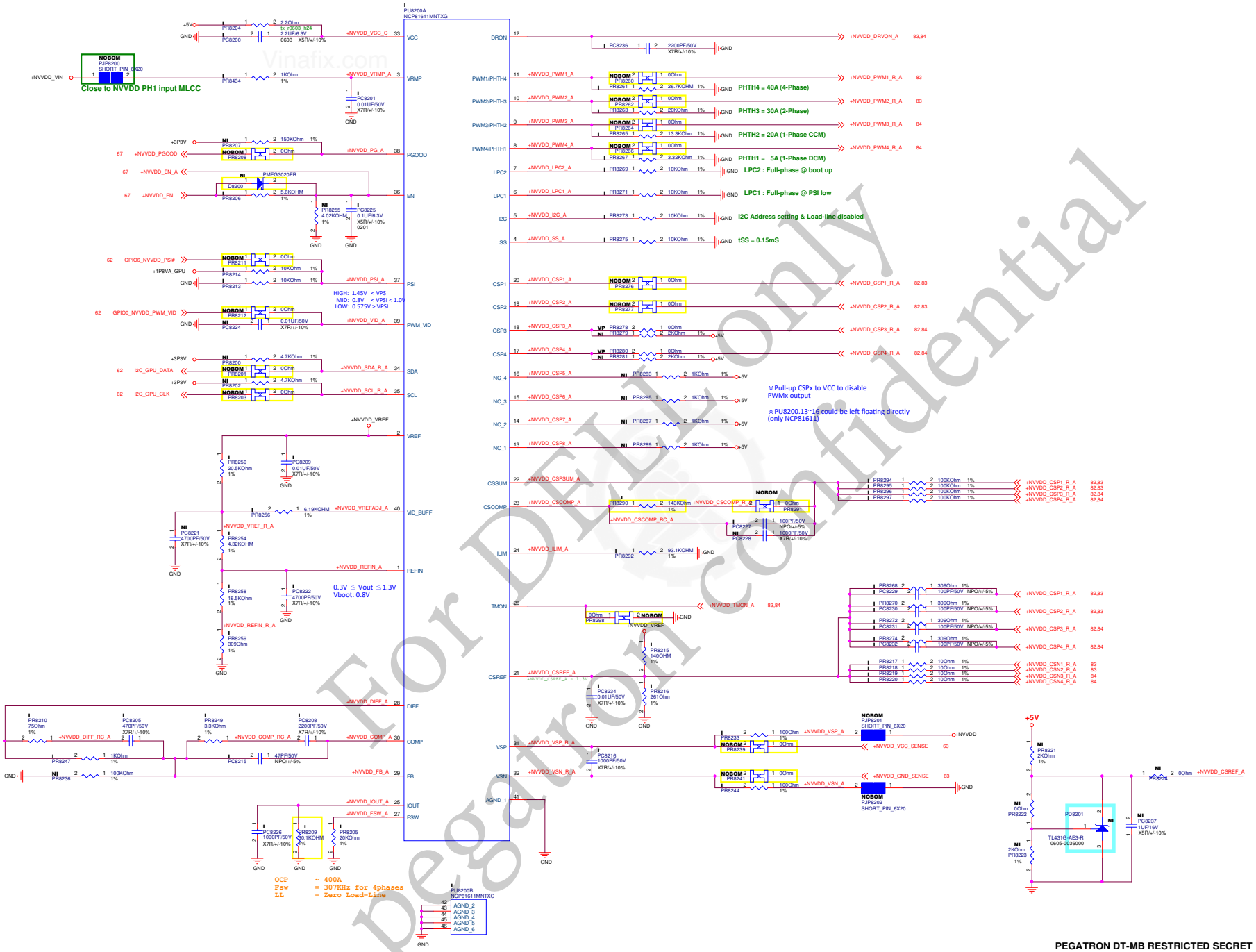
Pegatron Corp. Engineer: Chris_Tseng

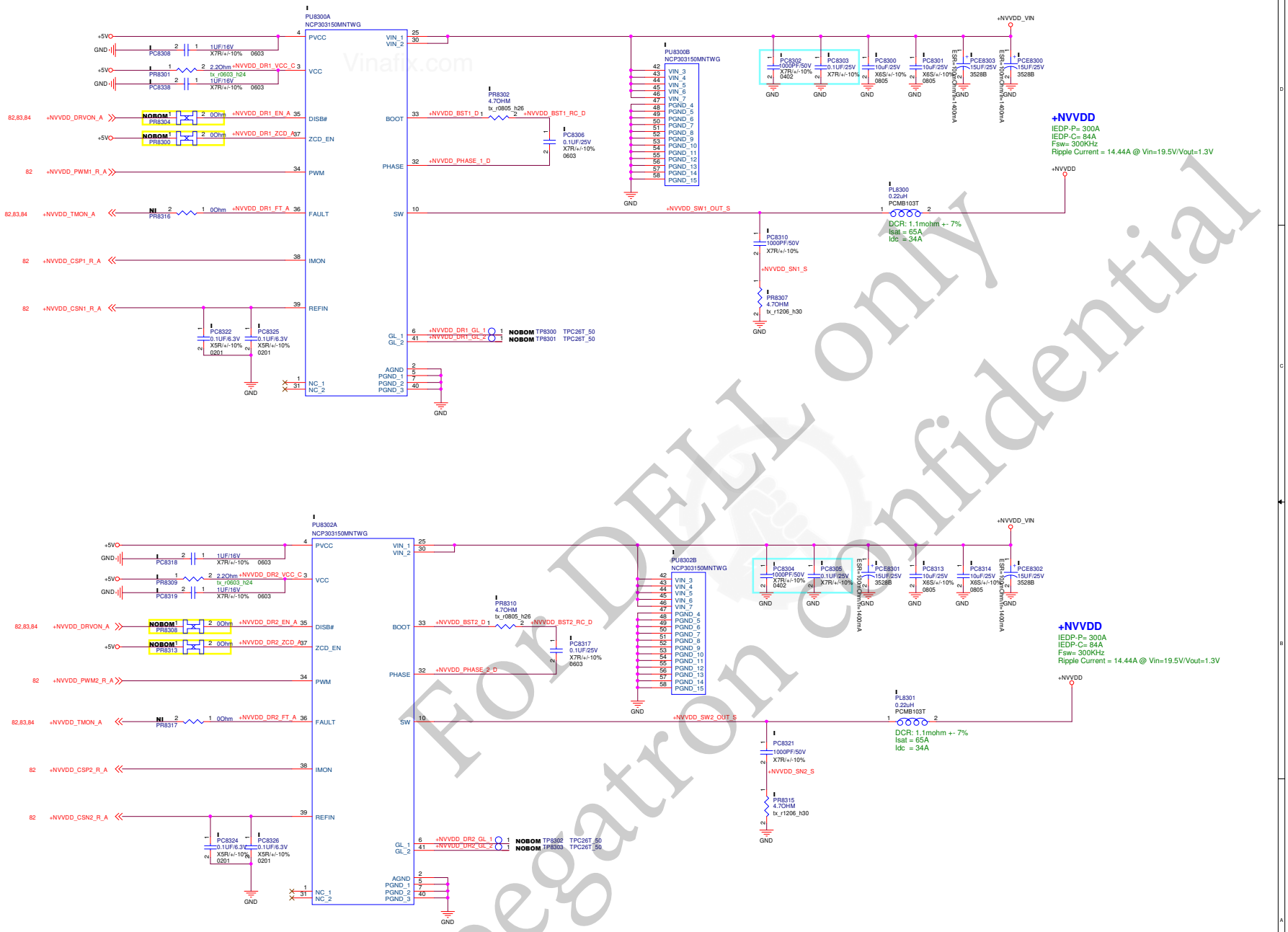
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 79 of 94


+VCCST
Imax= 0.21A
TDC= 0.147A
RDS(ON)= 11m ohm
Pd= 0.24mW
+VCCSTG
Imax= 0.02A
TDC= 0.014A
RDS(ON)= 11m ohm
Pd= 0.002mW
+3P3V
Imax= 4.503A
TDC= 3.152A
RDS(ON)= 24m ohm
Pd= 189.9mW
+1P8V
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24m ohm
Pd= 0.07mW
+5V
Imax= 4.12A
TDC= 2.884A
RDS(ON)= 24m ohm
Pd= 199.6mW
+3P3V_ORG
Imax= 2.616A
TDC= 1.831A
RDS(ON)= 24m ohm
Pd=80.46mW
Change for layout better plcament - X00/0626
Vinafix.com
For DELL only
pegatron confidential
PEGATRON
Title : Load switch1
Engineer: Chris_Tseng
Pegatron Corp.
Vulcan
Rev X00
Wednesday, November 28, 2018
Sheet 80 of 94


+5V_AUD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW
+3P3V_AUD
Imax= 0.01A
TDC= 0.007A
RDS(ON)= 24mohm
Pd=0.001mW
+3P3V_CARD
Imax= 0.4A
TDC= 0.28A
RDS(ON)= 24m ohm
Pd= 1.9mW
+1P8V_AUD
Imax= 0.075A
TDC= 0.0525A
RDS(ON)= 24mohm
Pd=0.07mW
+3P3V_SSD
Imax= 2.0A
TDC= 1.4A
RDS(ON)= 24m ohm
Pd= 47.1mW
+VCCPLL_OC
Imax= 0.13A
TDC= 0.091A
RDS(ON)= 24mohm
Pd=0.2mW
+3P3V_GPU
Imax= 0.07A
TDC= 0.049A
RDS(ON)= 24mohm
Pd=0.06mW
+3P3V_LAN
Imax= 0.152A
TDC= 0.107A
RDS(ON)= 24mohm
Pd=0.27mW
Change for layout better plcament
- X00/0626
Default NI
For DELL only
pegatron confidential
PEGATRON Title : Load switch2
Pegatron Corp.
Engineer: Chris_Tseng
Size Custom
Project Name Vulcan
Rev X00
Date: Wednesday, November 28, 2018
Sheet 81 of 94





PEGATRON DT-MB RESTRICTED SECRET

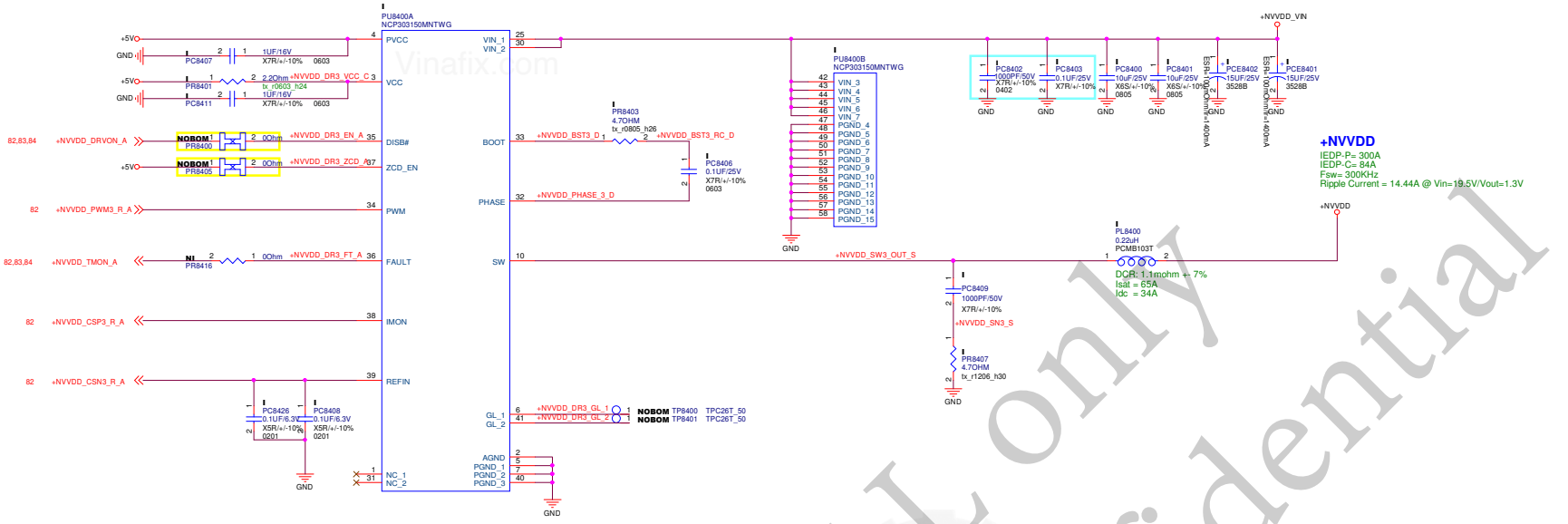
<Core Design>

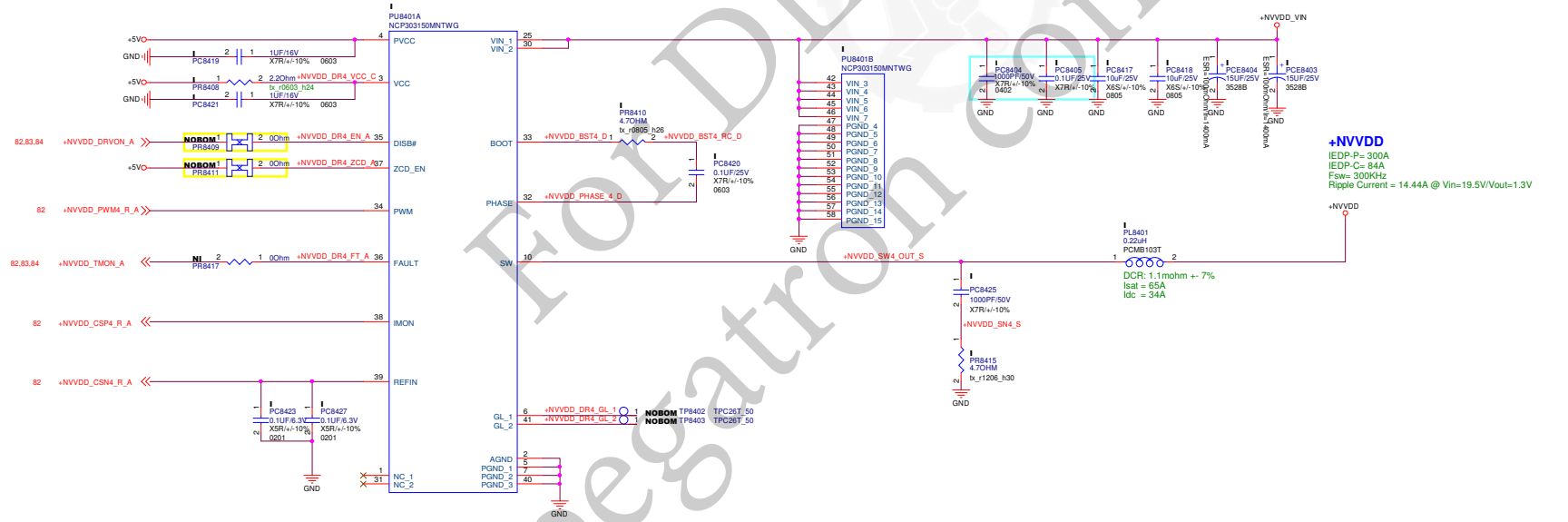
PEGATRON Title : +NVDD Driver /Cap

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 83 of 94





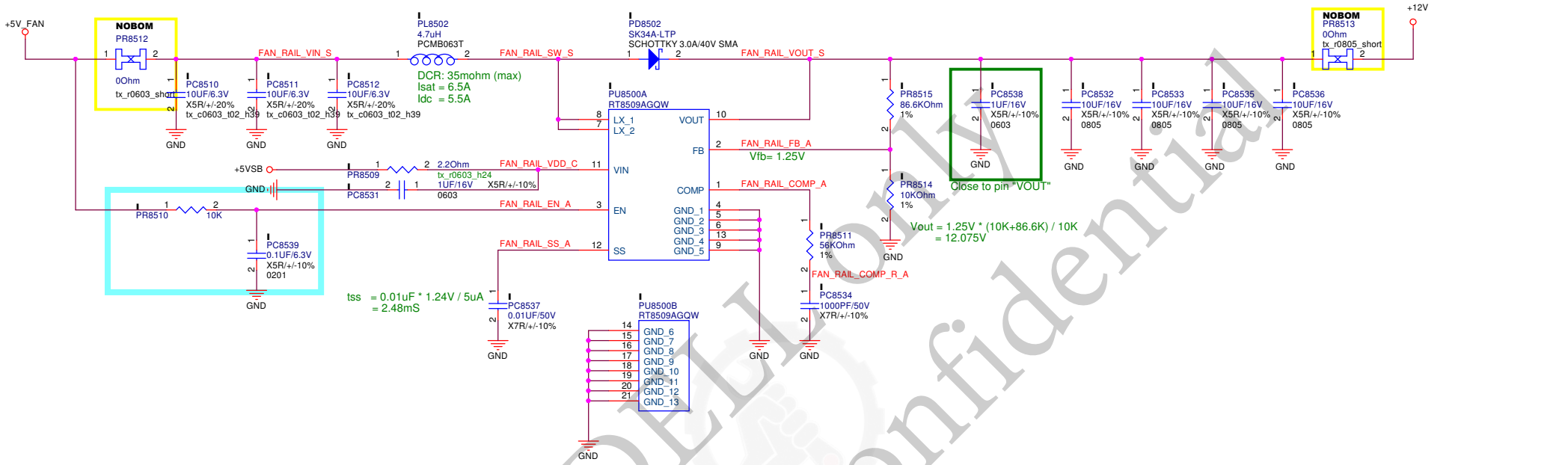
<Core Design>

PEGATRON Title : +NVVDD Driver-2

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 84 of 94



Owner	+12V OC point	Low Limit	High limit
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A
	4.5A(Min)/5.0A(Typ.)	N/A	3.25uH @ 8A

※ OC point is based on peak inductor current

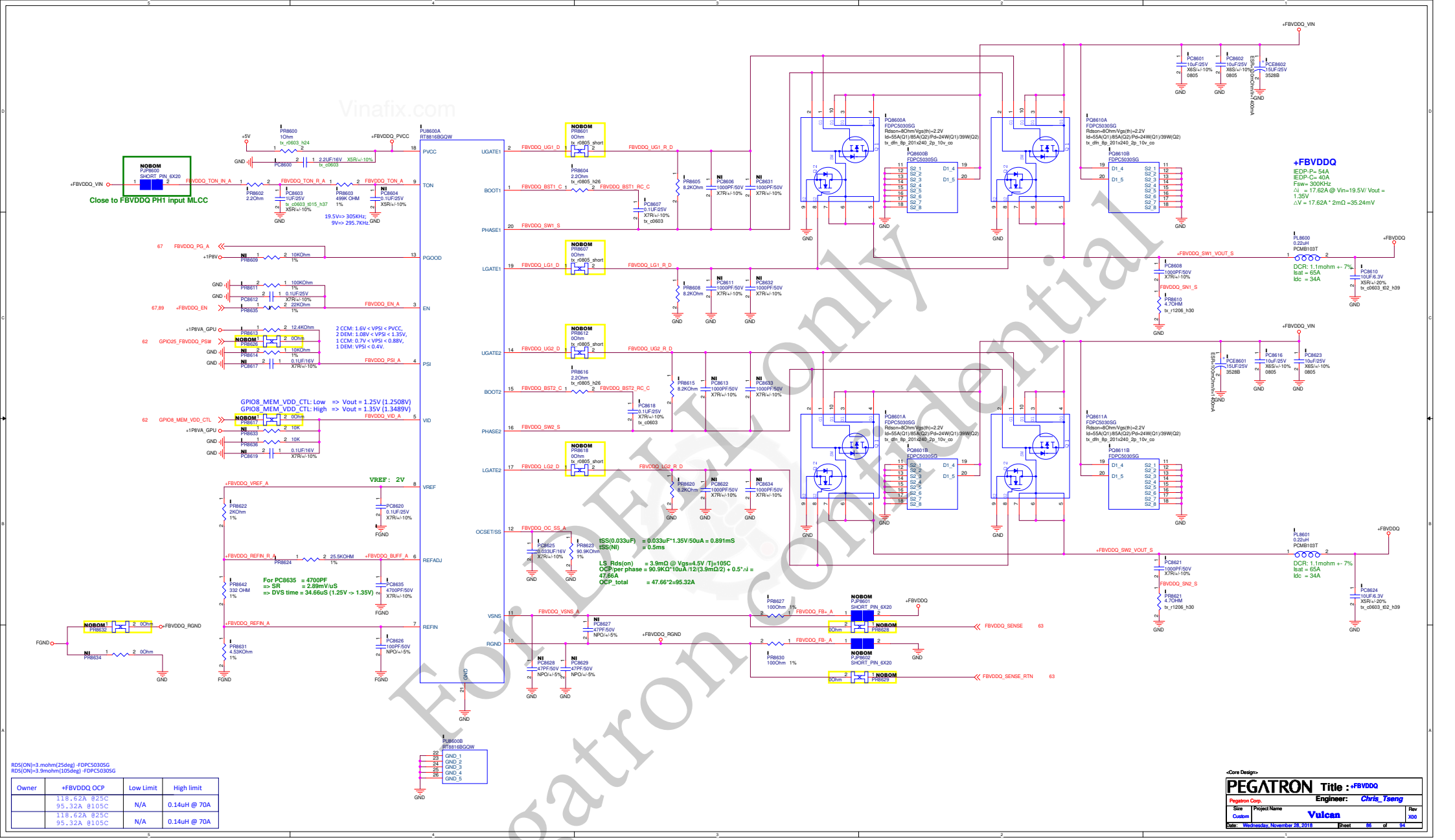
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +12V

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 85 of 94



RDS(ON)=3.mohm(25deg) -FDPC5030SG
RDS(ON)=3.9mohm(105deg) -FDPC5030SG

Owner	+FBVDDQ OCP	Low Limit	High limit
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A

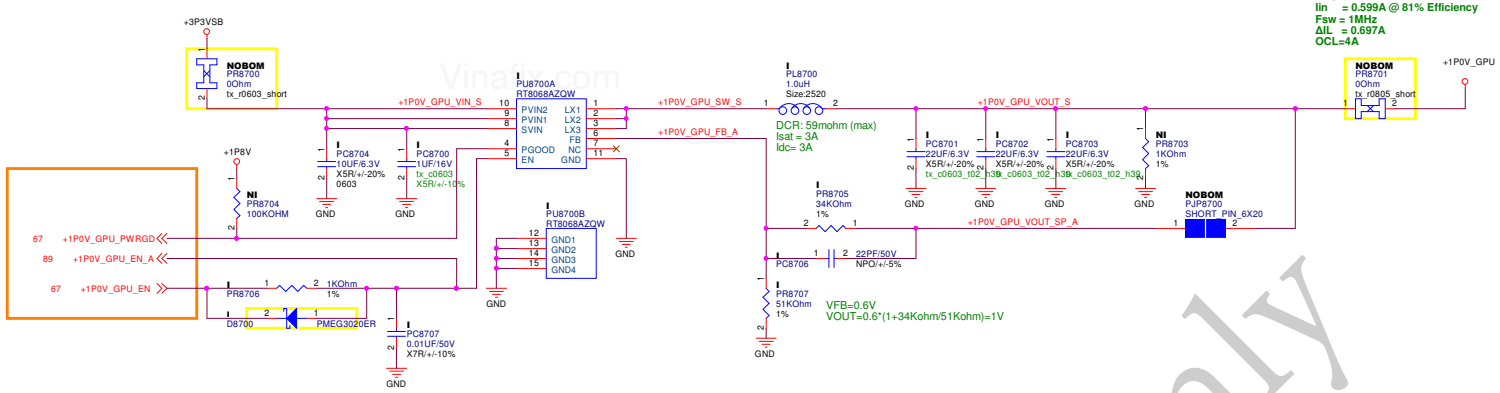
<Core Design>

PEGATRON Title : +FBVDDQ

Pegatron Corp. Engineer: Chris_Tseng

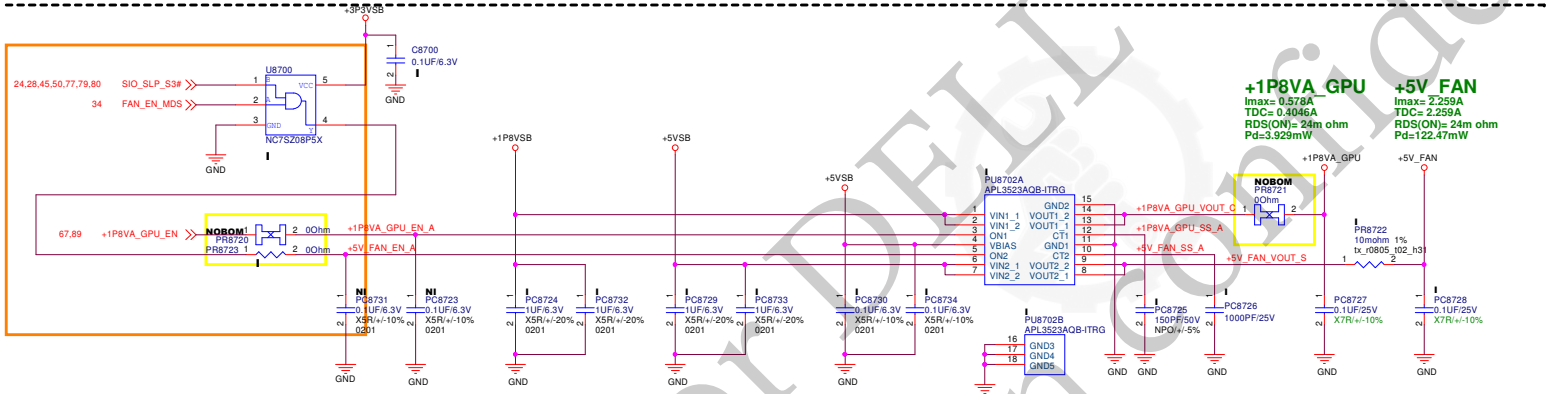
Size	Project Name	Rev
Custom	Vulcan	X00

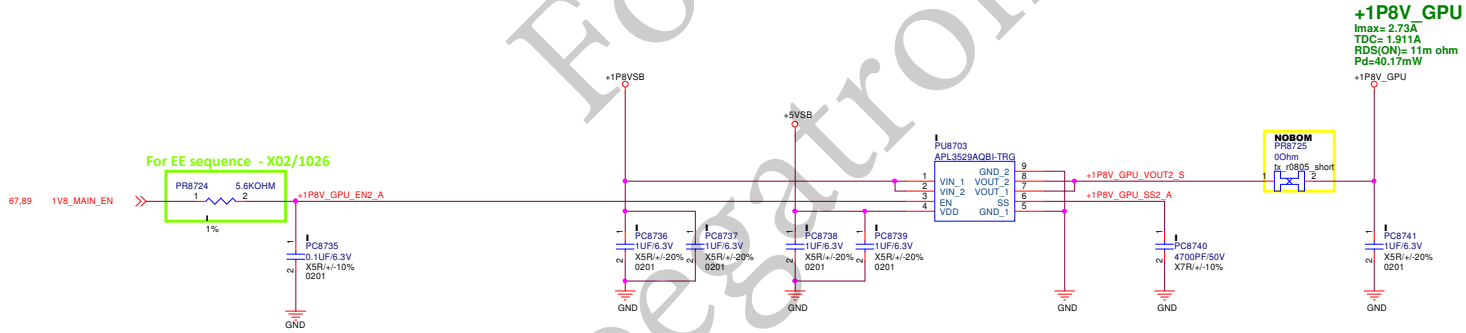
Date: Wednesday, November 28, 2018 Sheet 86 of 94



Owner	+1P0V_GPU	Low Limit	High limit
Atticus	4.0A	N/A	0.44uH @ 6A
Terry	4.0A	N/A	0.44uH @ 6A

※ OC point is based on peak inductor current





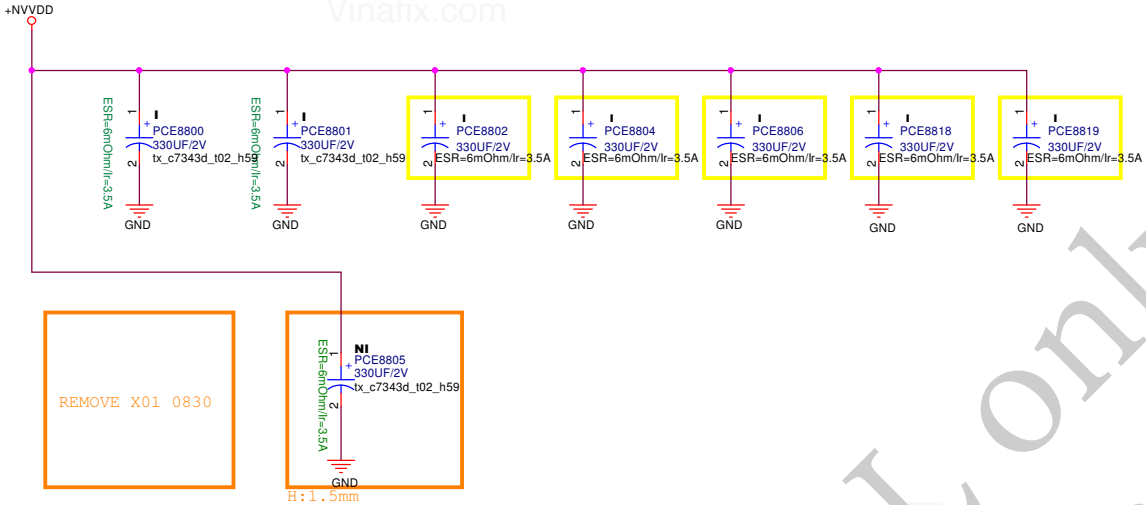
<Core Design>

PEGATRON Title : +1P0V_GPU/+1P8V_GPU & LDO

Pegatron Corp. Engineer: Chris_Tseng

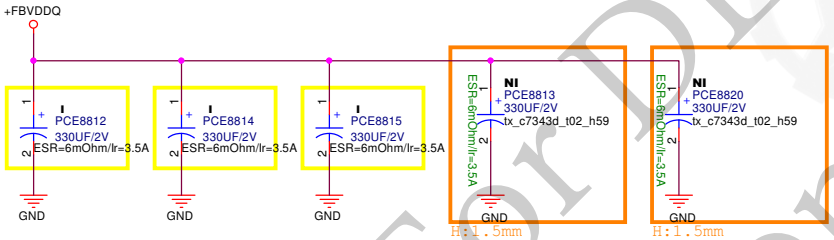
Size	Project Name	Rev
Custom	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 87 of 94



+NVVDD Output CAP(w/ +NVVDDS)

330uF/2V/H=2mm * 7 (I)
330uF/2V/H=1.5mm * 2(NI)



+FBVDDQ Output CAP

330uF/2V/H=2mm * 3 (I)
330uF/2V/H=1.5mm * 2(NI)

<Core Design>

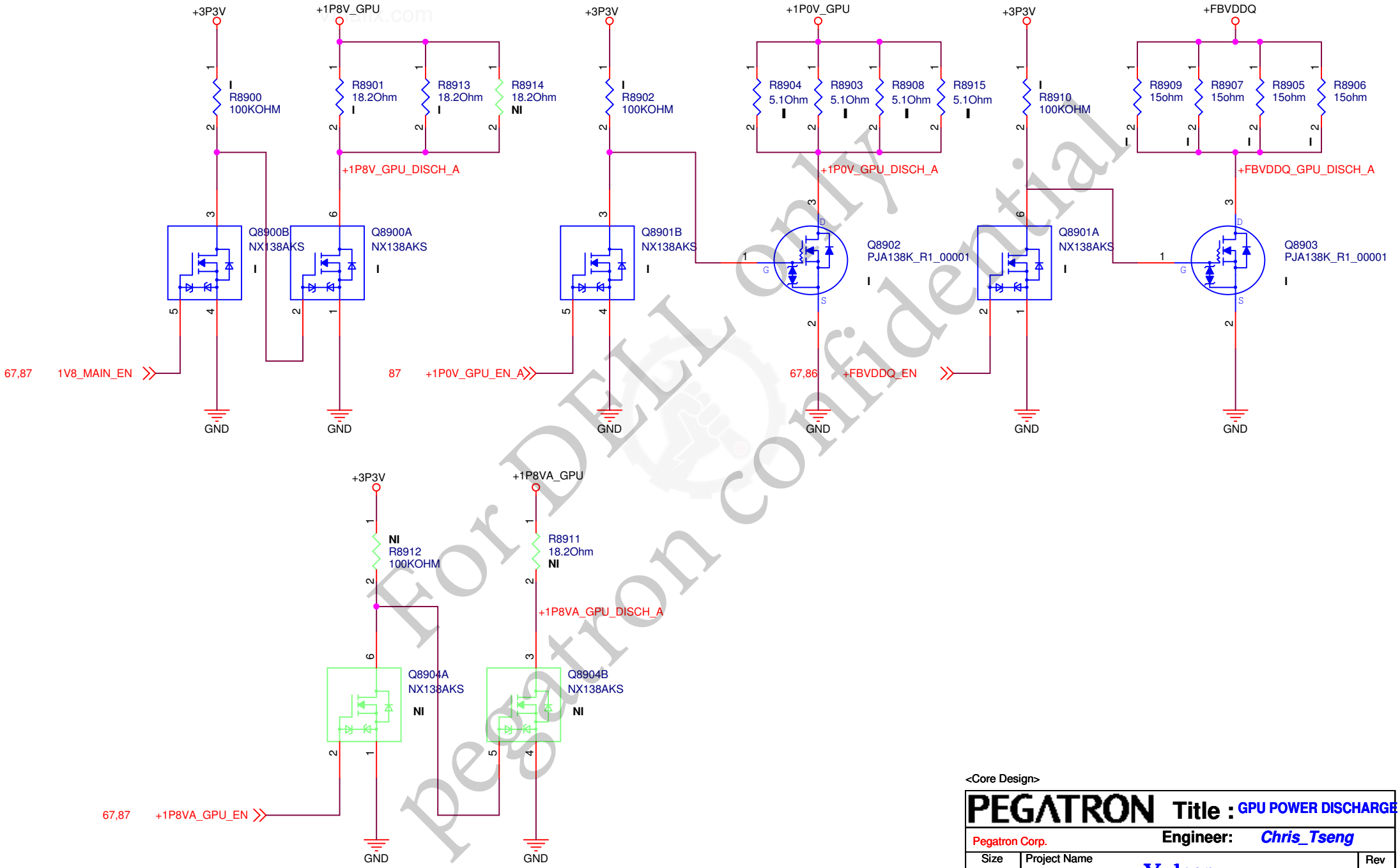
PEGATRON Title : GPU_POWER_CAP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 88 of 94

GPU POWER DISCHARGE



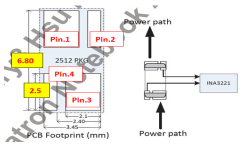
<Core Design>

PEGATRON Title : GPU POWER DISCHARGE

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A4	Vulcan	B00

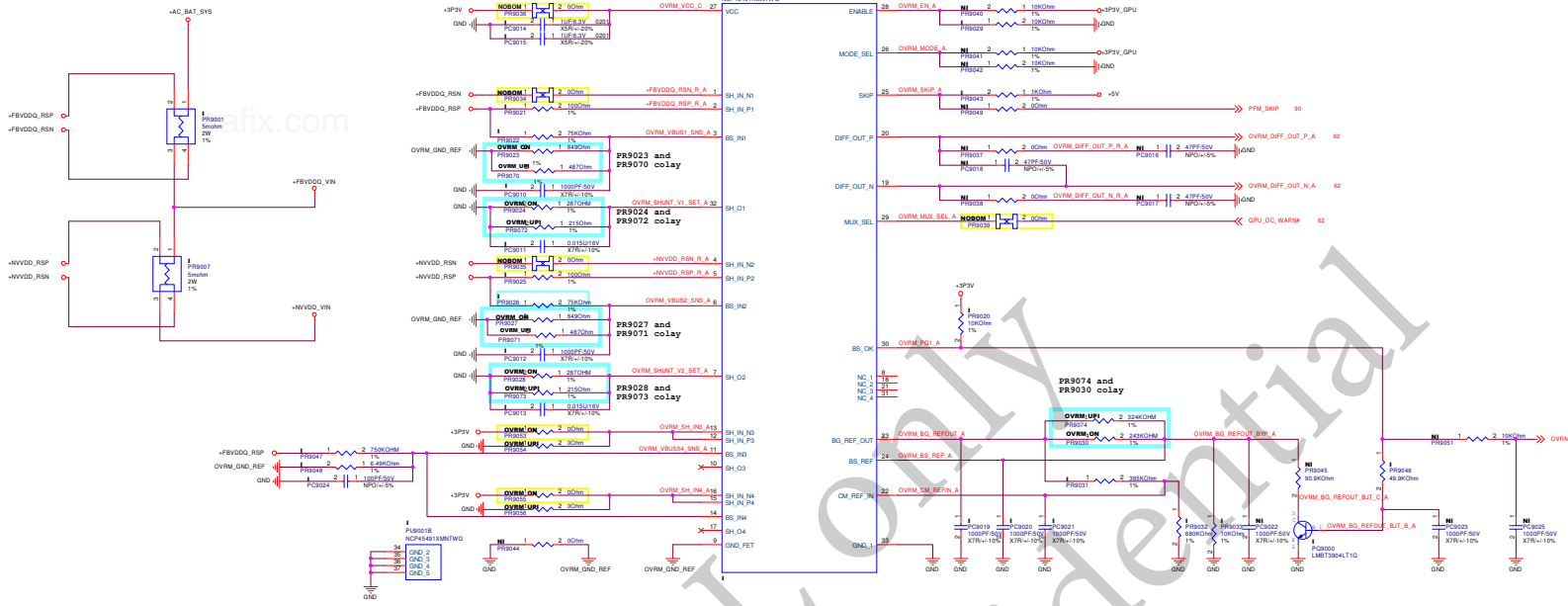
Date: Wednesday, November 28, 2018 Sheet 89 of 94



+AC_BAT_SYS (GPU power only)

Input Current: 12A @19V (1ms moving average)
Input Current: 10A @19V (5ms moving average)
Input Current : 4.21A @19V (1s movingi average)

Input Current: 25.33A @9V (1ms moving average)
Input Current: 21.11A @9V (5ms moving average)
Input Current : 8.89A @9V (1s movingi average)



OnSemi		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9023	PR9027	PR9024	PR9028	PR9030	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	649Ω	649Ω	287Ω	287Ω	243kΩ	75kΩ	75kΩ	1.0nF	1.0nF

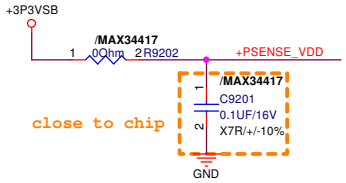
uPI		R954	R924	R977	R923	R950	R953	R952	C841	C836
		PR9070	PR9071	PR9072	PR9073	PR9074	PR9022	PR9026	PC9010	PC9012
N18E-G3 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G2 MAX-Q	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G1 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF
N18E-G0 MAX-P	80W	487Ω	487Ω	215Ω	215Ω	324kΩ	75kΩ	75kΩ	1.0nF	1.0nF

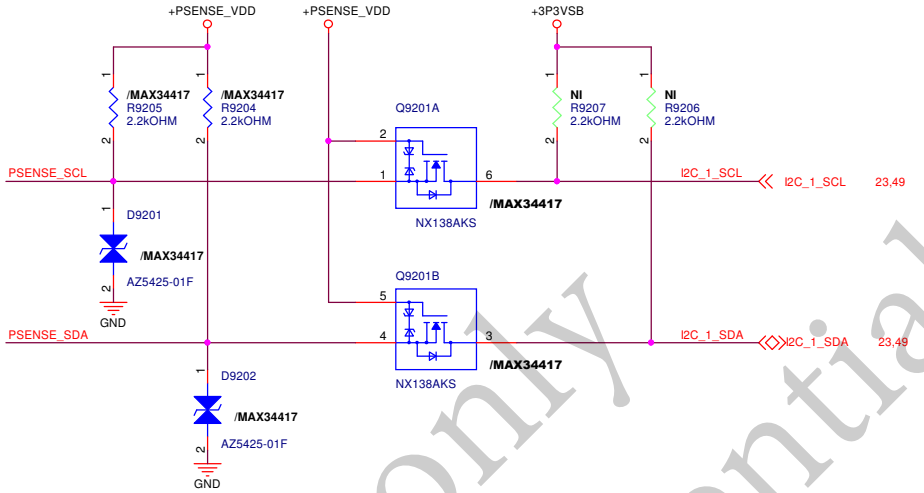
<Core Design>
PEGATRON Title : Power sense
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Vulcan | Rev: X00
Date: Wednesday, November 28, 2018 | Sheet 60 of 66

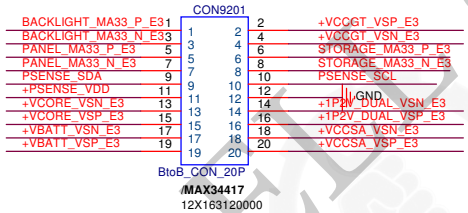
<Core Design>

PEGATRON	Title : RESERVE	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: A2	Project Name: Vulcan	Rev: X00
Date: Wednesday, November 28, 2018	Sheet 91 of 94	

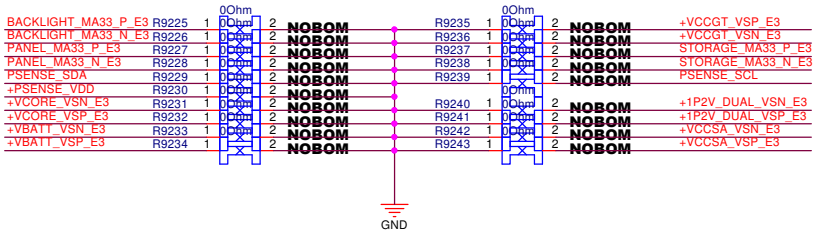
POWER SENSE







VCCGT		SSD/HDD				VDDQ		VCCSA	
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19
PANEL Backlight		PANEL Logic				VCORE		Battery	



	Chip Channel	Connector pin	Item	Location	Sense Resistor	Note
Sensor 1 [10h]	1	P1+/-	CPU_VCCGT	PR7307 (10m ohm) PR7308 (10m ohm)	5m ohm (0x05)	VCCGT
	2	P2+/-	STORAGE	R3109 (10m ohm)	10m ohm (0x0A)	SSD
				R3216 (10m ohm)		HDD(SATA)
	3	P3+/-	DISPLAY_CTLR	R4852 (10m ohm)	10m ohm (0x0A)	Panel Logic
	4	P4+/-	DISPLAY_BACKLIGHT	R4800 (10m ohm)	10m ohm (0x0A)	Panel Backlight
Sensor 2 [1Eh]	1	P5+/-	STYSTEM	R6811 (5m ohm)	5m ohm (0x05)	Battery
	2	P6+/-	CPU_VCORE	PR7100 (10m ohm) PR7101 (10m ohm)	5m ohm (0x05)	VCORE
	3	P7+/-	CPU_VDDQ	PR7700 (10m ohm)	10m ohm (0x0A)	VDDQ
	4	P8+/-	CPU_VCCSA	PR7407 (10m ohm)	10m ohm (0x0A)	VCCSA

<Core Design>

PEGATRON Title : POWER SENSE MAX34417

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 92 of 94

<Core Design>

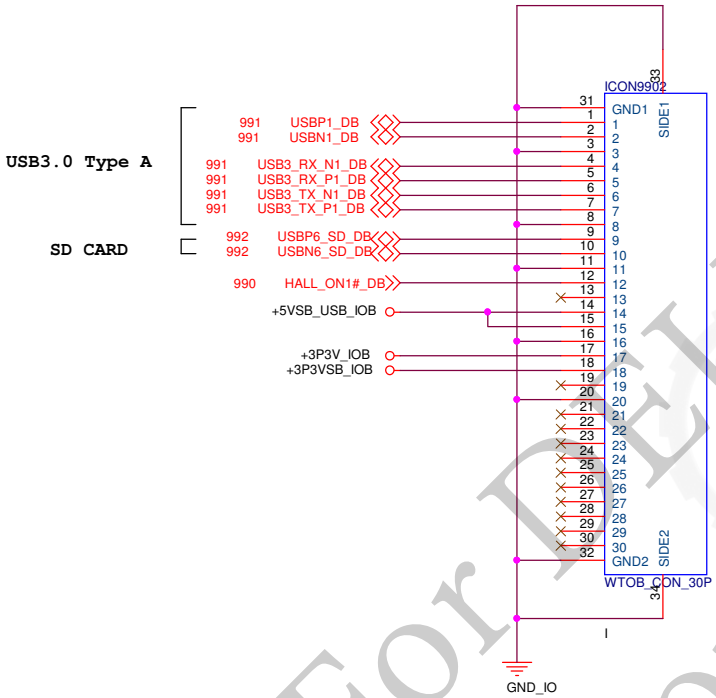
PEGATRON Title : RESERVE

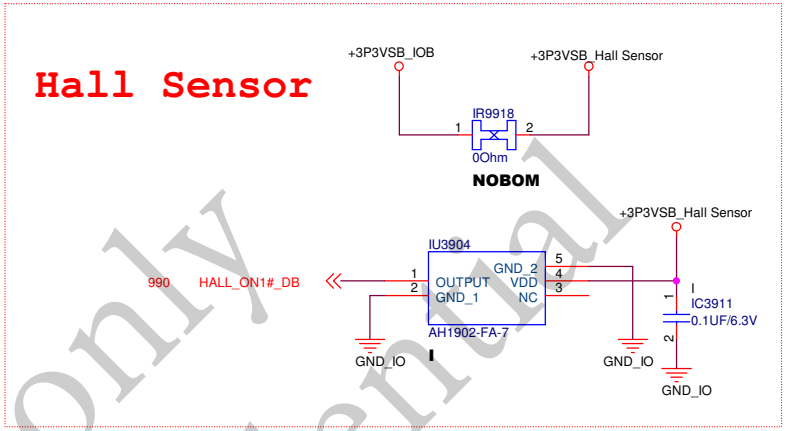
Pegatron Corp. Engineer: Chris_Tseng

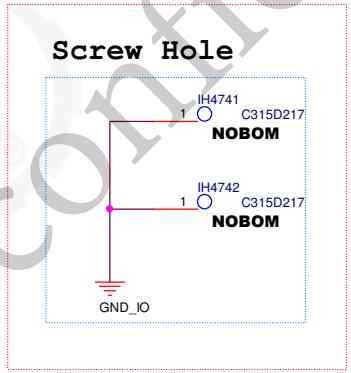
Size	Project Name	Rev
A3	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 94 of 94

990.IO port/Hall sensor







<Core Design>

PEGATRON Title : IO port/Hall sensor

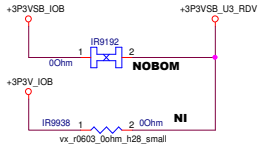
Pegatron Corp. Engineer: Alex_Tsai

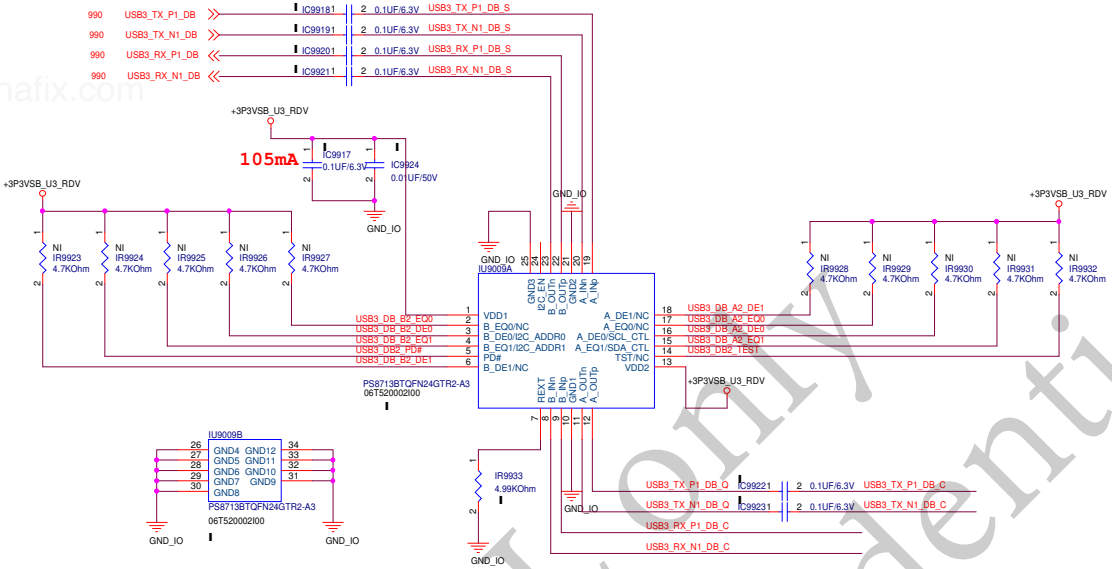
Size	Project Name	Rev
B	Vulcan	X00

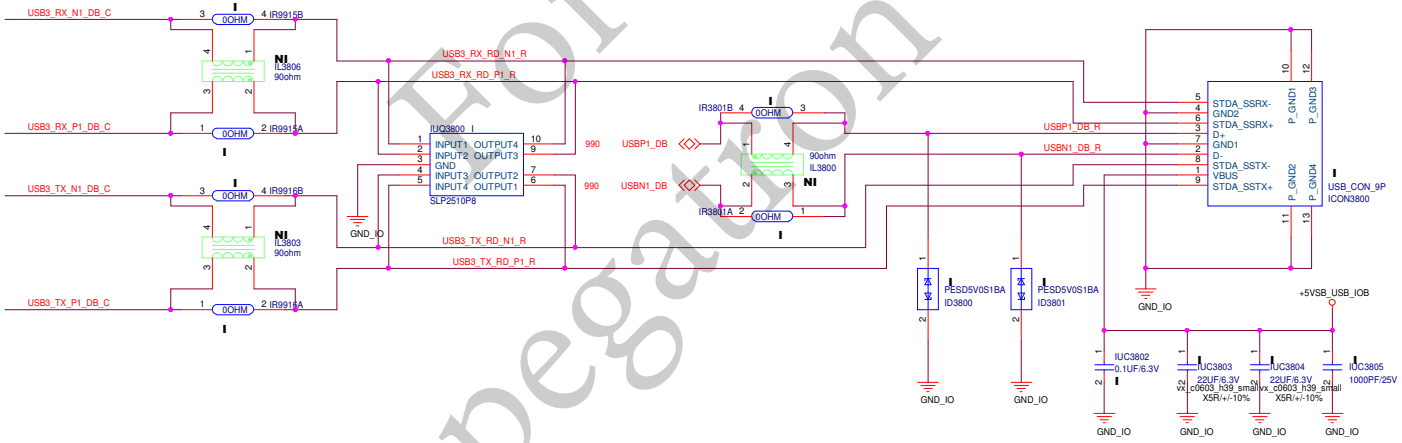
Date: Wednesday, November 28, 2018 Sheet 990 of 94

991.USB PORT

Imax: 105mA







<Core Design>

PEGATRON Title : USB DB PORT

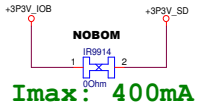
Pegatron Corp. Engineer: Alex_Tsai

Size	Project Name	Rev
C	Vulcan	X00

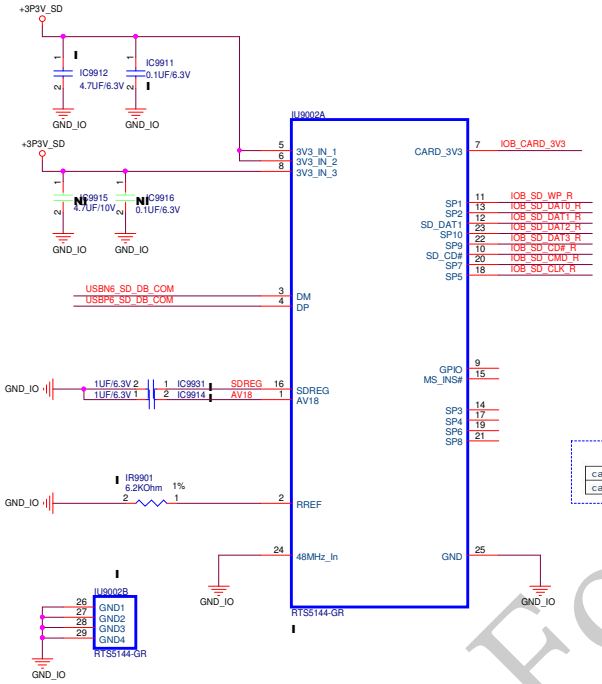
Date: Wednesday, November 28, 2018 Sheet 991 of 94

992.Card_reader_RTS5144-GR

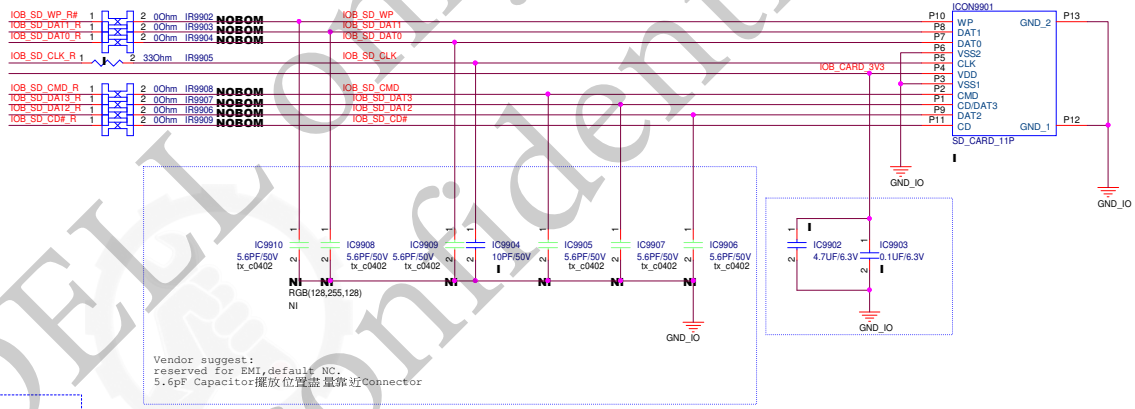
POWER



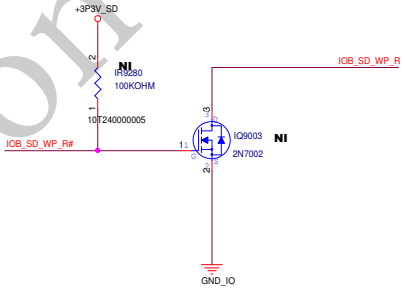
Imax: 400mA

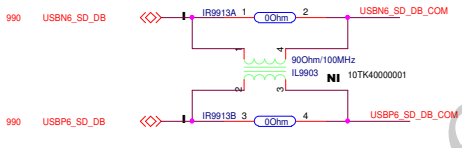


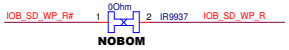
WITHOUT CARD		CARD INSERTED:LOCK		CARD INSERTED:UNLOCK	
W/P	GND	W/P	GND	W/P	GND
C/D	VSS1 P3	C/D	VSS1 P3	C/D	VSS1 P3



card lock	SD_WP pin high
card unlock	SD_WP pin low







<Core Design>

PEGATRON Title : Card_reader_RTS5144GR

Pegatron Corp. Engineer: Alex_Tsai

Size	Project Name	Rev
C	Vulcan	X00

Date: Wednesday, November 28, 2018 Sheet 992 of 94