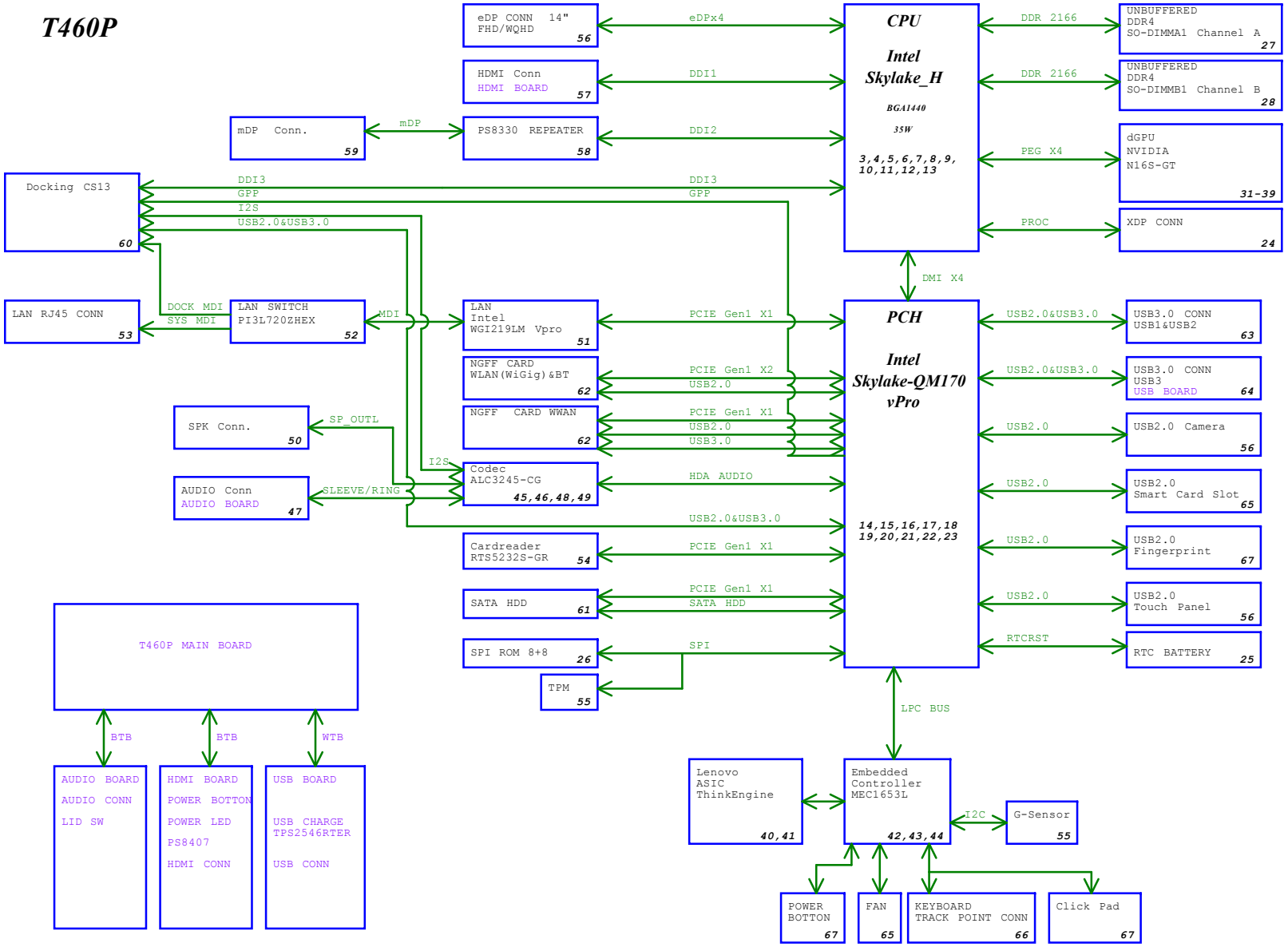
T460P



Page:03~13==>CPU SKL-H
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Page:24=====>XDP CONNECTOR
Page:25=====>RTC BATTERY
Page:26=====>SPI FLASH
Page:27~28==>DDR4 MEMORY
Page:31~39==>N16S-GT
Page:40~41==>THINK ENGINE
Page:42~44==>MEC1653L
Page:45~50==>AUDIO ALC3245-CG
Page:51~53==>LAN WGI219LM
Page:54=====>CARD_READER RTS5232S-GR
Page:55=====>THERMAL SENSOR/G SENSOR/TPM
Page:56=====>eDP/CMOS/LOGO-LED CONN.
Page:57=====>HDMI BTB CONN.
Page:58=====>PS8330B REPEATER DP
Page:59=====>MINI-DP CONN.
Page:60=====>CS13 DOCKING CONN.
Page:61=====>SATA HDD CONN.
Page:62=====>WLAN/WWAN/SIM CONN.
Page:63=====>USB3 P1/2 CONN.
Page:64=====>USB3 P3 CONN.
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Page:84=====>DC/DC IMVP8
Page:85=====>DC/DC VCCPUCORE
Page:86=====>DC/DC VCCGFXCORE_I
Page:87=====>DC/DC VCCSA
Page:88=====>CPU PROCESSOR DECOUPLING
Page:89=====>DC/DC VCCCPUIO
Page:90=====>DC/DC VCC1R0_SUS
Page:91=====>DC/DC VCC1R2A/VCC0R6B
Page:92=====>DC/DC VCC2R5A
Page:93=====>DC/DC GFXCORE_D
Page:94=====>DC/DC VCC1R5VIDEO
Page:95=====>DC/DC VCC1R05VIDEO_PLL

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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	Suspend-to-Disk (STD)
	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	Soft Off
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
	S5 EC OFF	M-OFF	ON	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

Schematics Mark Definition

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device		Address
CH-A	DDR DIMM1	1001 0000b
CH-B	DDR DIMM2	1001 0010b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1%	+-2%	+-3%	+-5%	+-10%	+-20%	+-30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	+50, -20%	-30% ~ 10%

ZZZ1 PCB@ — BT463 DA80000Z600

ZZZ2 X76_VSE2G@ — K4W4G1646E-BC1A X7608112001

ZZZ3 X76_VME2G@ — MT41J256M16HA-093G X7608112002

ZZZ4 X76_VHC2G@ — H5TC4G63CFR-N0C X7608112003

BOM Structure Table

BOM Structure	NOTE
DEBUG@	For EE DEBUG
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
GC6@	For GC6 function
NGC6@	NON GC6 function
ME@	ME Connector
EMC@	For EMI Solution
RF@	For RF Solution
VSE2G@	For SAMSUNG VRAM Setting
VME2G@	For Micron VRAM Setting
VHC2G@	For RF HYNIX VRAM Setting
X76_VSE2G@	K4W4G1646E-BC1A x4 + 24.9K
X76_VME2G@	MT41J256M16HA-093G x4 +10k
X76_VHC2G@	H5TC4G63CFR-N0C x4 +30.1k
CS@	For CURRENT SENSE
UMA@	For UMA
DIS@	For DIS
UC1@	For CPU

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Title: Blank

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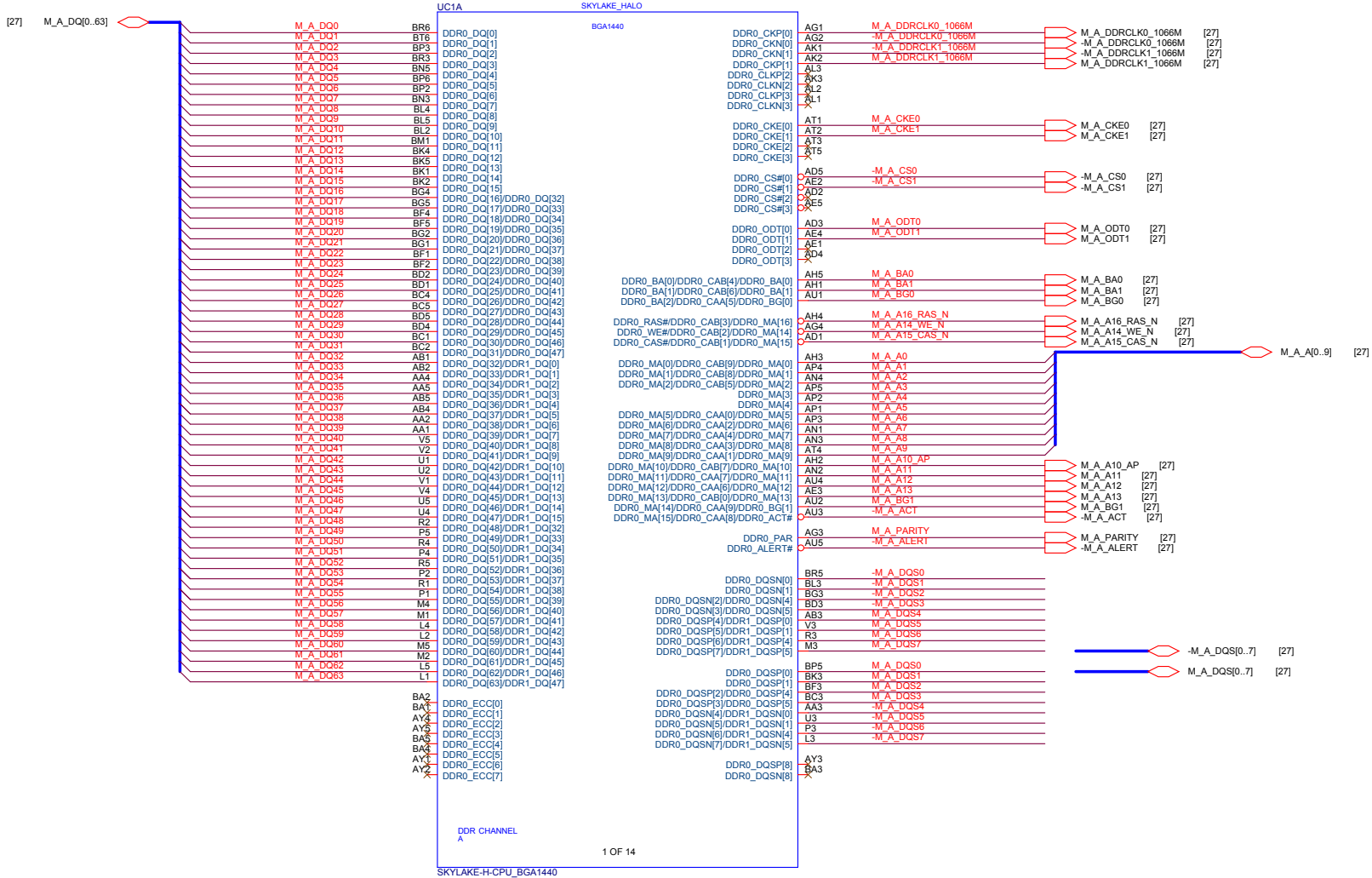

DDR4 INTERLEAVE IMPLEMENTATION

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Title	CPU SKL-H : DDR4 CH-A
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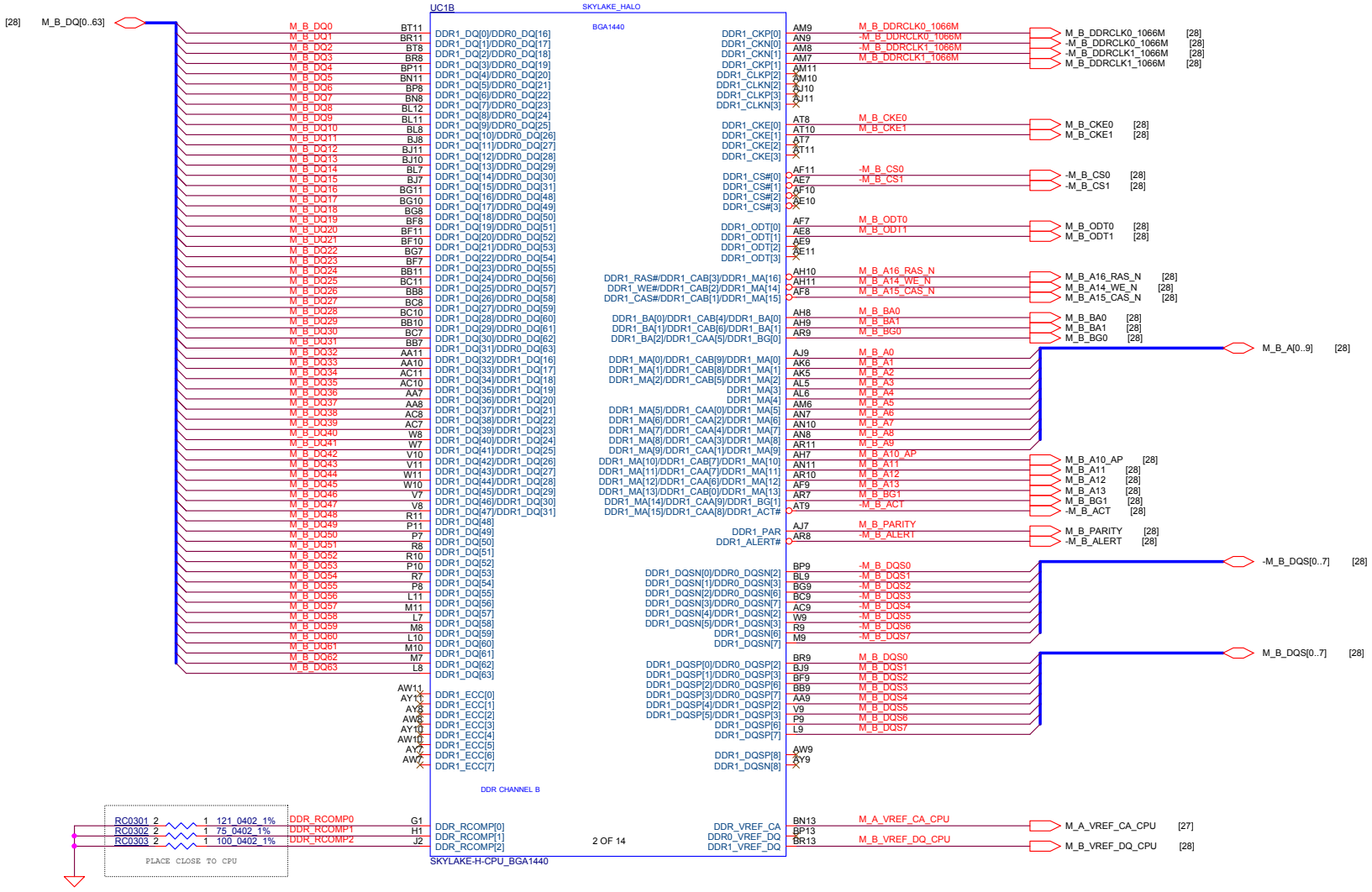

DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_DQ : Connected to VREF_CA on DIMM CH-B

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Title: CPU SKL-H : DDR4 CH-B

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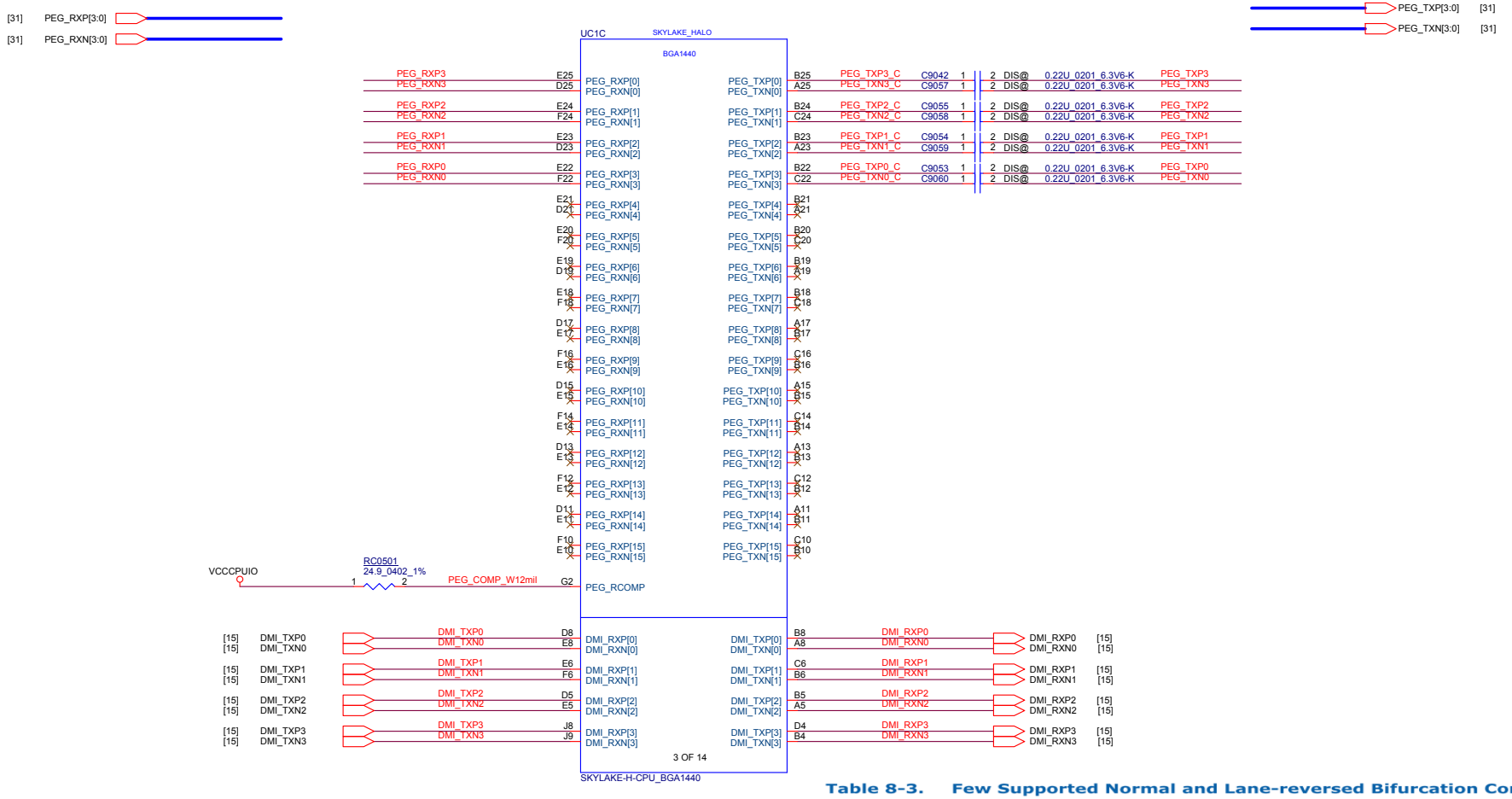

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro-cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Title			
CPU SKL-H : PEG/DMI			
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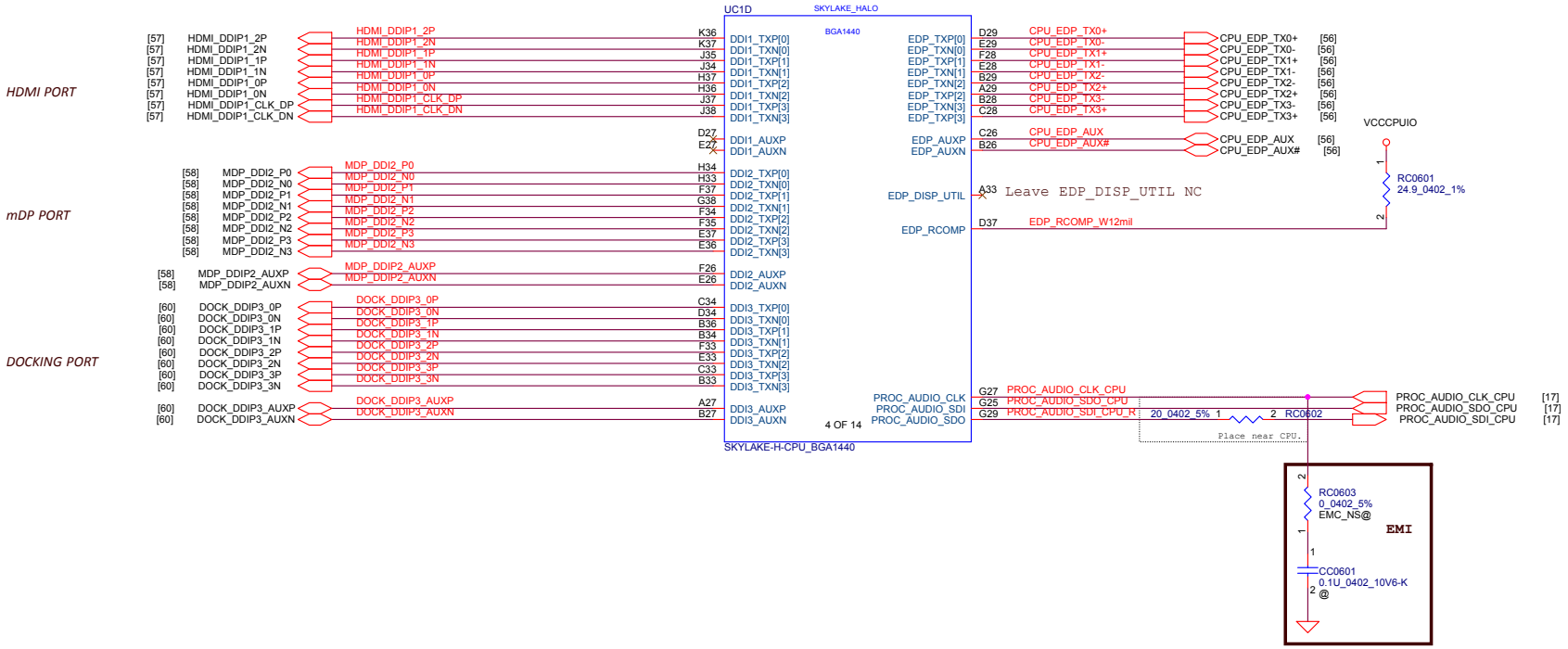

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Title: CPU SKL-H : DDI/EDP

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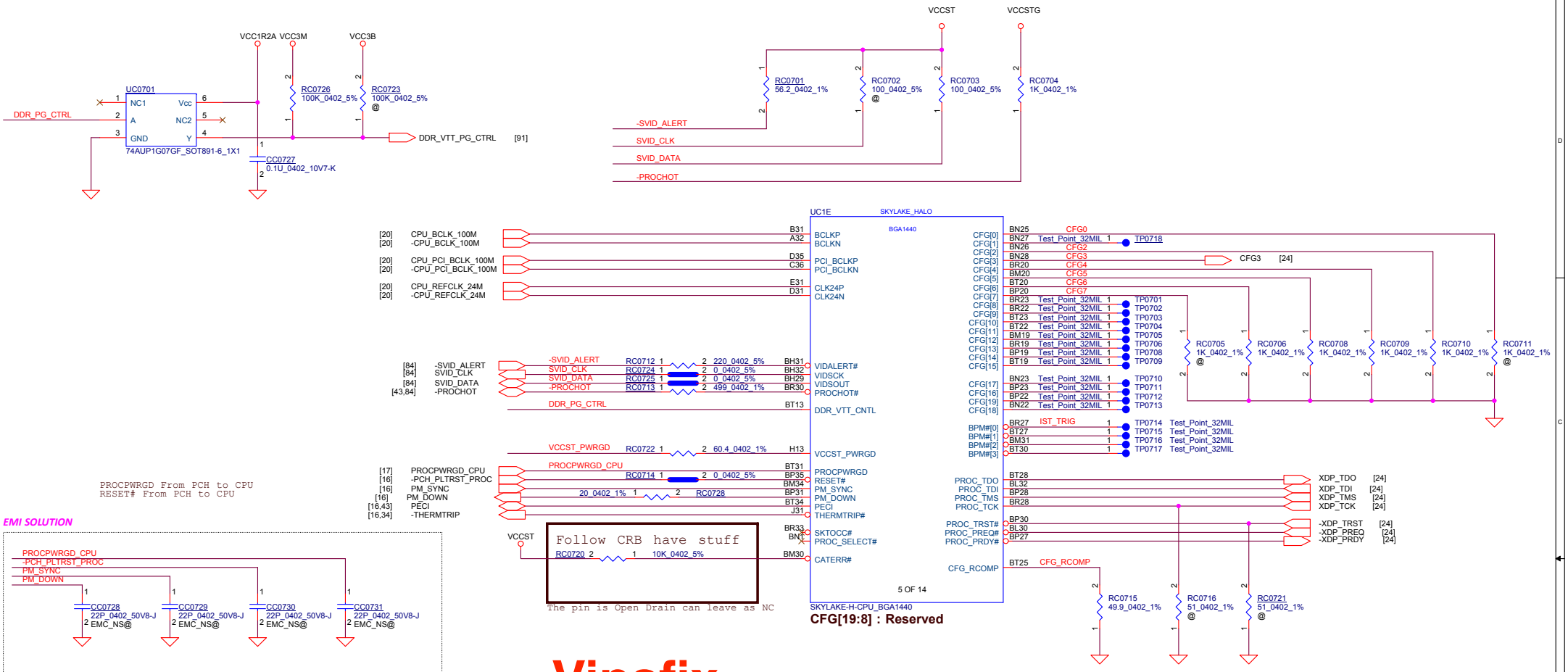

Vinafix

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
- 1 : No Stall <---------- LOGIC
- 0 : Stall

CFG[2] : PEG Static Lane Reversal
- 1 : Normal Operation
- 0 : Lane Reversal <---------- LOGIC

CFG[4] : eDP enable
- 1 : Disabled
- 0 : Enabled <---------- LOGIC

CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:2(CONFIRM BIOS)
- 00 : 1x4 <---------- LOGIC

CFG[7] : PEG Training(CONFIRM BIOS)
- 1 : PEG Train immediately following RESET# deassertion <---------- LOGIC
- 0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

For x16 Reversal Lanes - CFG[6/5/2] setting is 110
For x4 Reversal Lanes - CFG[6/5/2] setting is 000
For x4 Normal Lanes - CFG[6/5/2] setting is 001

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Title: CPU SKL-H : MISC/CLK/JTAG/CFG

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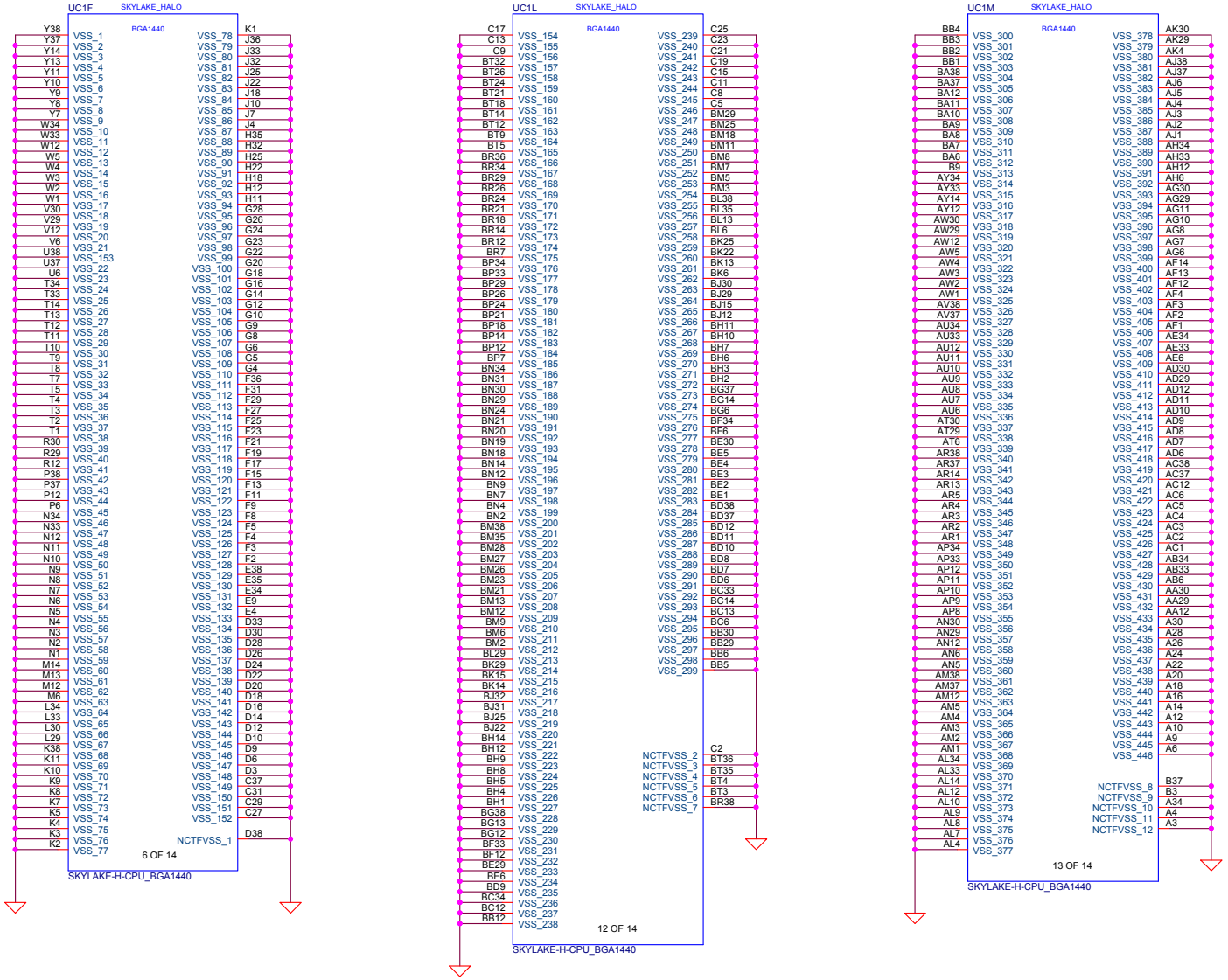

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: CPU SKL-H : GND

Size	Document Number	Rev
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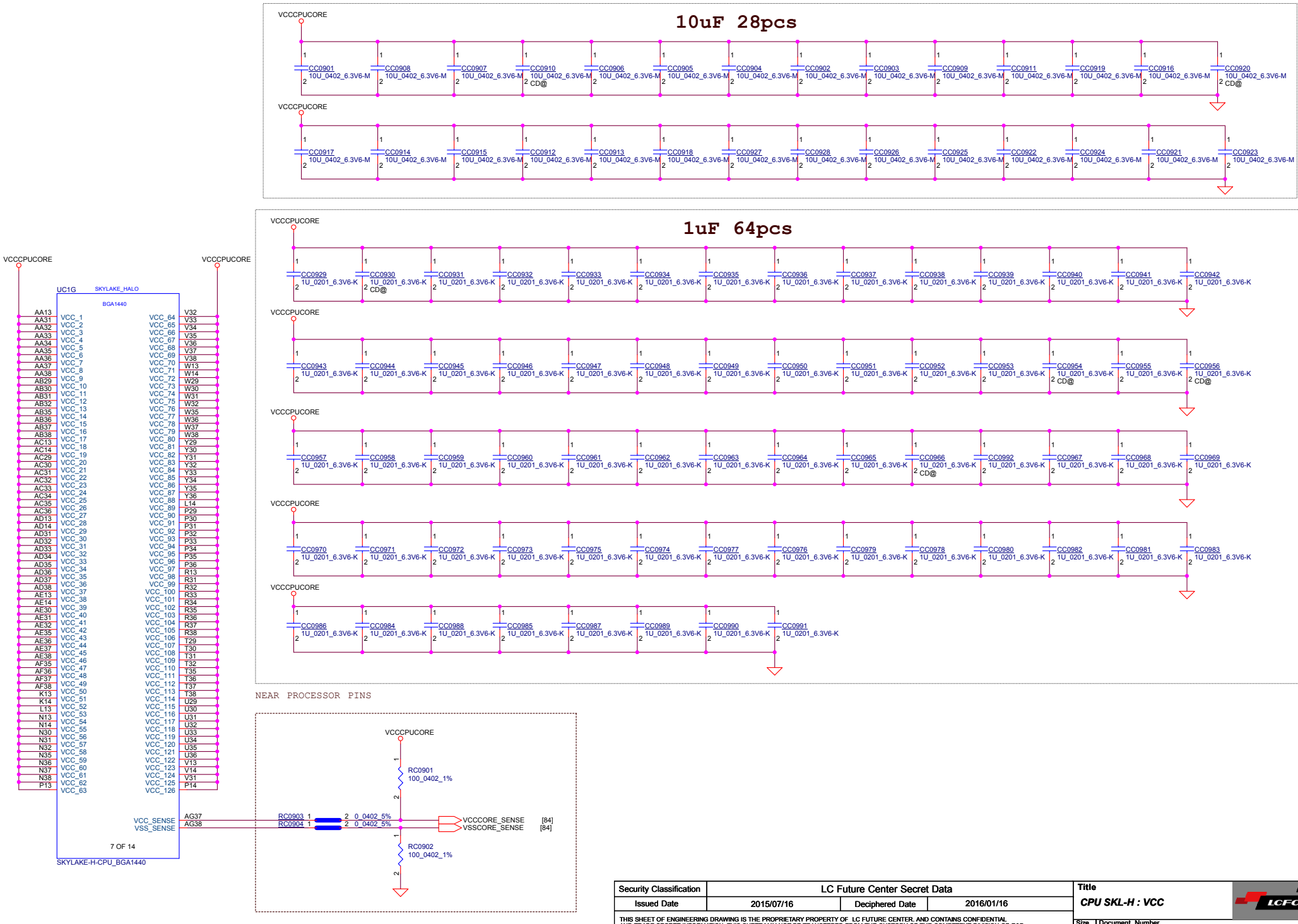

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Title: CPU SKL-H : VCC

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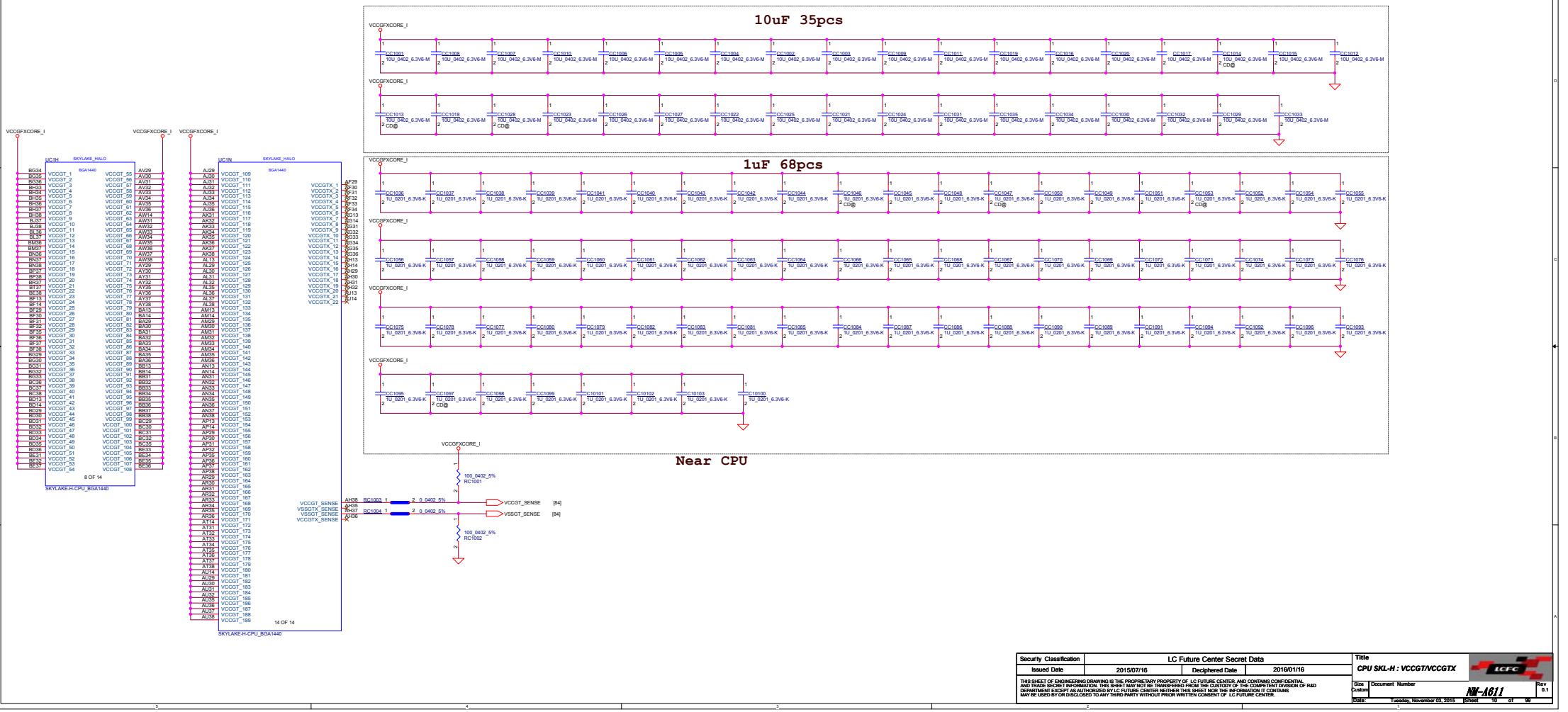

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Title	CPU SKL-H : VCCGT/VCCGTX		
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VCCSA DECOUPLING

VCCSA

10uF 7pcs

CC1125 10U_0402_6.3V6-M
CC1130 10U_0402_6.3V6-M
CC1129 10U_0402_6.3V6-M
CC1131 10U_0402_6.3V6-M
CC1128 10U_0402_6.3V6-M
CC1127 10U_0402_6.3V6-M
CC1126 10U_0402_6.3V6-M

VCCSA

1uF 3pcs

CC1133 1U_0402_6.3V6-K
CC1132 1U_0402_6.3V6-K
CC1134 1U_0402_6.3V6-K

VDDQ DECOUPLING

VCC1R2A

10uF 10pcs

CC1111 10U_0402_6.3V6-M
CC1112 10U_0402_6.3V6-M
CC1113 10U_0402_6.3V6-M
CC1114 10U_0402_6.3V6-M
CC1115 10U_0402_6.3V6-M
CC1116 10U_0402_6.3V6-M
CC1117 10U_0402_6.3V6-M
CC1118 10U_0402_6.3V6-M
CC1119 10U_0402_6.3V6-M
CC1120 10U_0402_6.3V6-M

VCC1R2A

22uF 4pcs

CC1121 22U_0603_6.3V6M
CC1122 22U_0603_6.3V6M
CC1123 22U_0603_6.3V6M
CC1124 22U_0603_6.3V6M

VCCSA

VCC1R2A

UC1I SKYLAKE_HALO BGA1440

J30	VCCSA_1	VDDQ_1	AA6
K29	VCCSA_2	VDDQ_2	AE12
K30	VCCSA_3	VDDQ_3	AF5
K31	VCCSA_4	VDDQ_4	AF6
K32	VCCSA_5	VDDQ_5	AG5
K33	VCCSA_6	VDDQ_6	AG9
K34	VCCSA_7	VDDQ_7	AJ12
K35	VCCSA_8	VDDQ_8	AL11
L31	VCCSA_9	VDDQ_9	AP6
L32	VCCSA_10	VDDQ_10	AP7
L35	VCCSA_11	VDDQ_11	AR12
L36	VCCSA_12	VDDQ_12	AR6
L37	VCCSA_13	VDDQ_13	AT12
L38	VCCSA_14	VDDQ_14	AW6
M29	VCCSA_15	VDDQ_15	AY6
M30	VCCSA_16	VDDQ_16	J5
M31	VCCSA_17	VDDQ_17	J6
M32	VCCSA_18	VDDQ_18	K12
M33	VCCSA_19	VDDQ_19	K6
M34	VCCSA_20	VDDQ_20	L12
M35	VCCSA_21	VDDQ_21	L6
M36	VCCSA_22	VDDQ_22	R6
		VDDQ_23	T6
		VDDQ_24	W6
		VDDQC	Y12
		VCCPLL_OC_1	BH13
		VCCPLL_OC_2	G11
		VCCST	H30
		VCCSTG_1	H29
		VCCSTG_2	G30
		VCCPLL_1	H28
		VCCPLL_2	J28
		VCCSA_SENSE	M38
		VSSSA_SENSE	M37
		VCCIO_SENSE	H14
		VSSIO_SENSE	J14
AG12	VCCIO_1		
G15	VCCIO_2		
G17	VCCIO_3		
G19	VCCIO_4		
G21	VCCIO_5		
H15	VCCIO_6		
H16	VCCIO_7		
H17	VCCIO_8		
H19	VCCIO_9		
H20	VCCIO_10		
H21	VCCIO_11		
H26	VCCIO_12		
H27	VCCIO_13		
J15	VCCIO_14		
J16	VCCIO_15		
J17	VCCIO_16		
J19	VCCIO_17		
J20	VCCIO_18		
J21	VCCIO_19		
J26	VCCIO_20		
J27	VCCIO_21		

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SKYLAKE-H-CPU_BGA1440

VDDQC : Memory Control Clock Power

VCCPLL_OC : CPU digital PLL power rails

VCCPCUIO

CC1108 10U_0603_6.3V6-M
CC1109 10U_0603_6.3V6-M
CC1110 10U_0603_6.3V6-M

VCC1R2A

CC1107 10U_0603_6.3V6-M

VCC1R2A

CC1105 1U_0402_6.3V6-K
CC1106 1U_0402_6.3V6-K

VCCST

CC1101 1U_0402_6.3V6-K

VCCSTG

CC1102 1U_0402_6.3V6-K
CC1103 1U_0402_6.3V6-K

VCCST

CC1104 1U_0402_6.3V6-K

RC1115 0_0402_5%
RC1116 0_0402_5%

VCCPCUIO

RC1111 100_0402_1%
RC1113 100_0402_1%

VCCSA

RC1112 100_0402_1%
RC1114 100_0402_1%

VCCSA_SENSE [84]
VSSSA_SENSE [84]
VCCCPUIO_SENSE [89]
VSSCPUIO_SENSE [89]

RESISTORS CLOSE TO CPU PINS

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Title: CPU SKL-H : VCCSA/VCCIO/VDDQ

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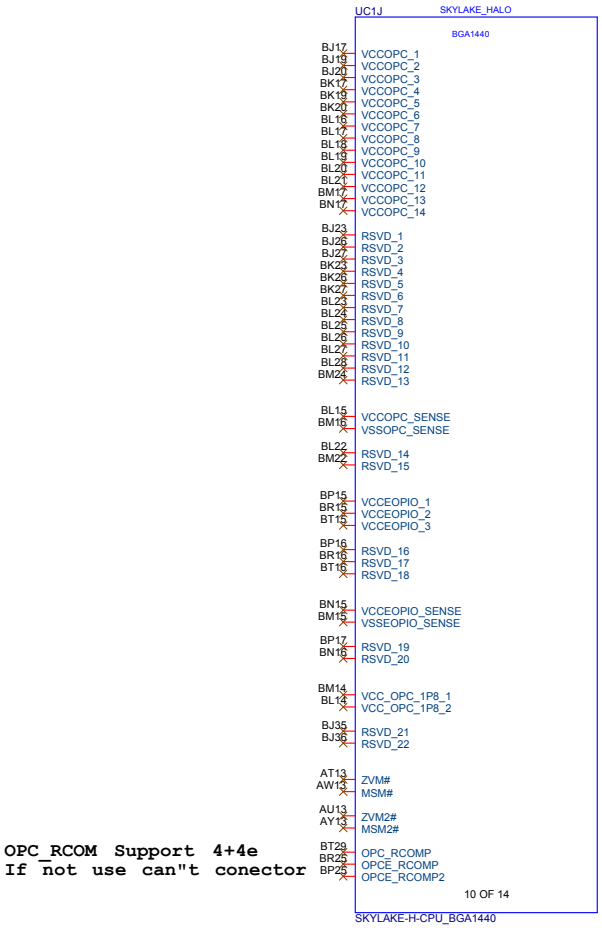

OPC_RCOM Support 4+4e
If not use can"t conector

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Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: CPU SKL-H : VCCOPC/RSVD

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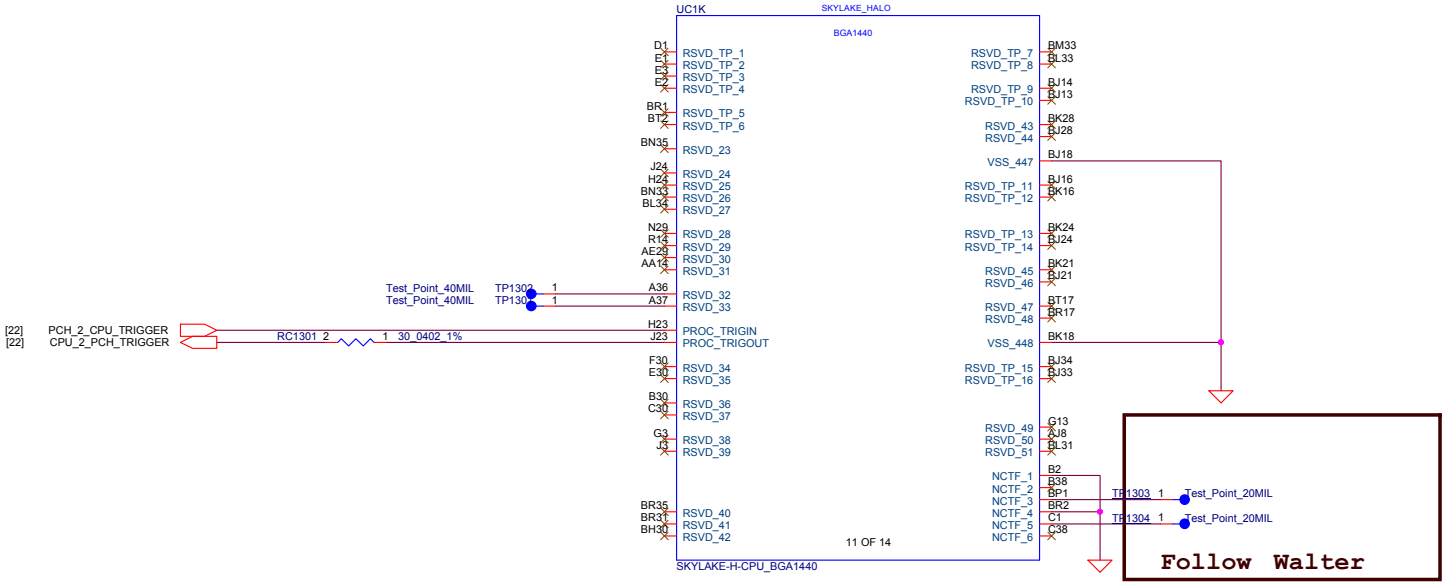

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Title: CPU SKL-H : RSVD

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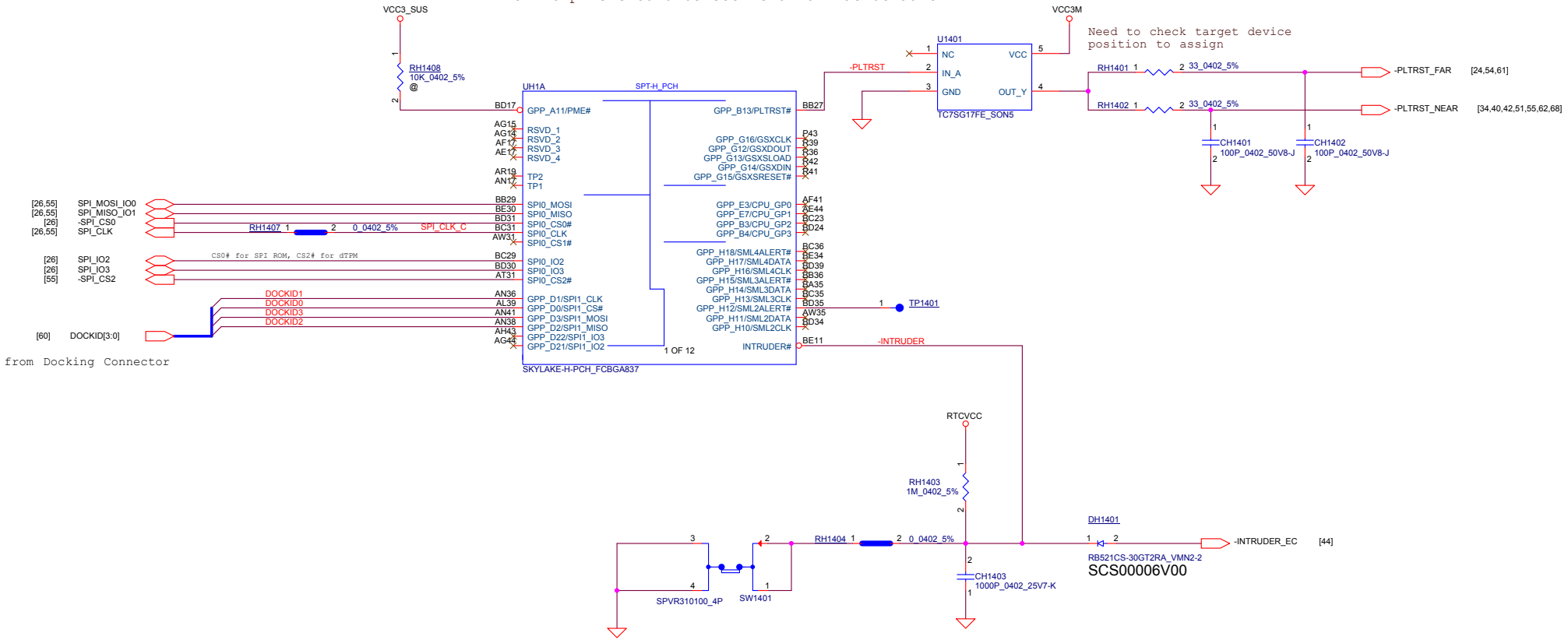
All of NC pins should be set "GPO LOW" as default



DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

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Title: PCH SKL-H : SPI

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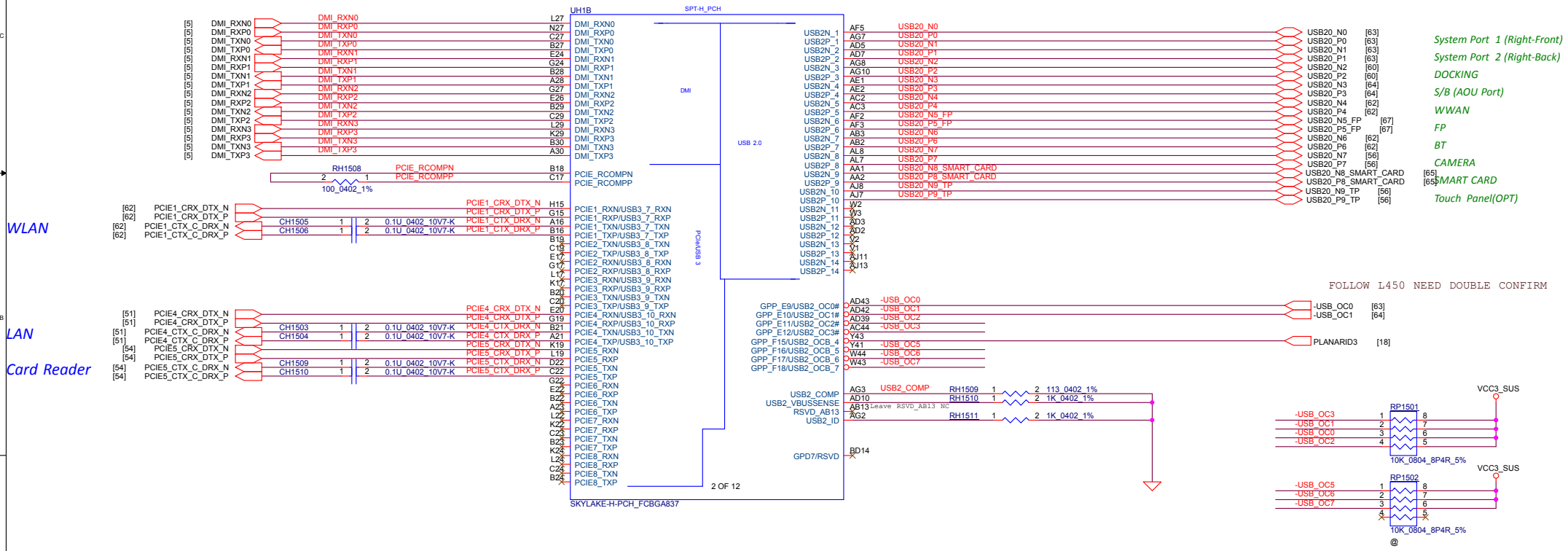
USB2.0	Port Assignment	OC#
USB2 #1	USB Port 1	OC0
USB2 #2	USB Port 2	OC0
USB2 #3	Docking USB2.0 port	
USB2 #4	USB AOU port	OC1
USB2 #5	WWAN	
USB2 #6	Finger printer	
USB2 #7	BT	
USB2 #8	Camera	
USB2 #9	Smart Card reader	
USB2 #10	Touch panel (Option)	
USB2 #11		
USB2 #12		
USB2 #13		
USB2 #14		



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Title: PCH SKL-H : DMI/PCIE/USB

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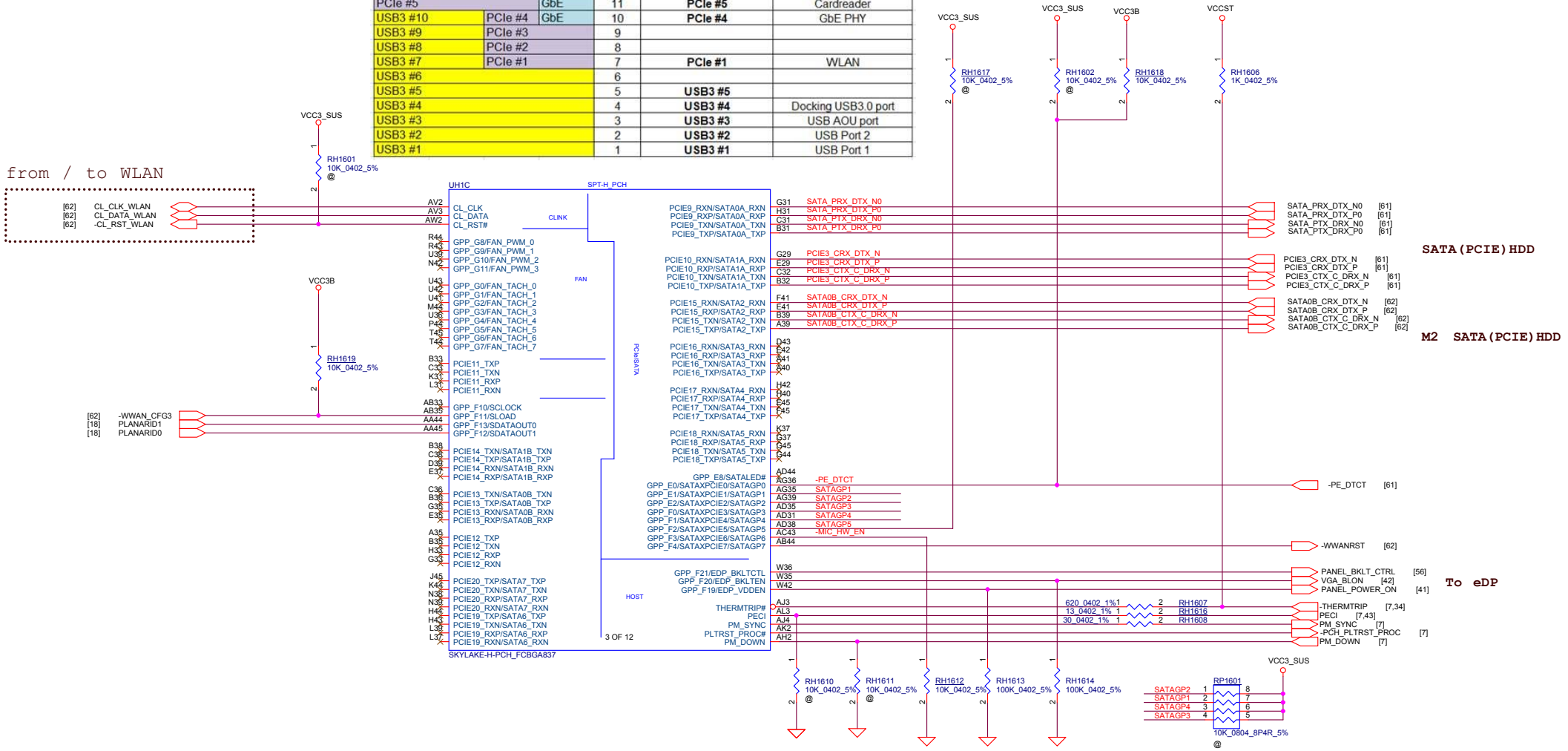
Flexible I/O			Port#	Configuration	Port Assignment
PCIe #20			26		
PCIe #19			25		
PCIe #18	SATA #5		24		
PCIe #17	SATA #4		23		
PCIe #16	SATA #3		22	**SATA #3**	M.2 Type B connector
PCIe #15	SATA #2		21	**SATA #2**	M.2 Type B connector
PCIe #14	SATA #1		20		
PCIe #13	SATA #0	GbE	19		
PCIe #12		GbE	18		
PCIe #11			17		
PCIe #10	SATA #1		16	**PCIe #10**	SATA-Express connector
PCIe #9	SATA #0	GbE	15	**SATA #0/PCIe #9**	SATA-Express connector
PCIe #8			14		
PCIe #7			13		
PCIe #6			12		
PCIe #5		GbE	11	**PCIe #5**	Cardreader
USB3 #10	PCIe #4	GbE	10	**PCIe #4**	GbE PHY
USB3 #9	PCIe #3		9		
USB3 #8	PCIe #2		8		
USB3 #7	PCIe #1		7	**PCIe #1**	WLAN
USB3 #6			6		
USB3 #5			5	**USB3 #5**	
USB3 #4			4	**USB3 #4**	Docking USB3.0 port
USB3 #3			3	**USB3 #3**	USB AOU port
USB3 #2			2	**USB3 #2**	USB Port 2
USB3 #1			1	**USB3 #1**	USB Port 1



Notes:

1. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
2. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: *PCH SKL-H : SATA/PCIE*

Size	Document Number	Rev
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TABLE : Functional Strap

HDA_SDO Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confldentlality
LOW	Disable ME Crypto TLS(Default)

PLACE ON BOTTOM SIDE

TEST PAD
BOTTOM SIDE
DO NOT MOVE AFTER FIX

20140730: As of now, we cannot get information about these pins from SKL-H RVP and other documents. We need to confirm about them later.

FOLLOW WALTER CONNECTER TO GBE

Pullups on SMB are located in SMBUS Switch page.

important

LPC is selected for EC. (Default)
This PD is insurance in case internal PD doesn't work well.

INTEL FAE ADVICE

RH1739 Pull up 150K follow MOW

TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Owerride)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : AUDIO/SMBUS/JTAG

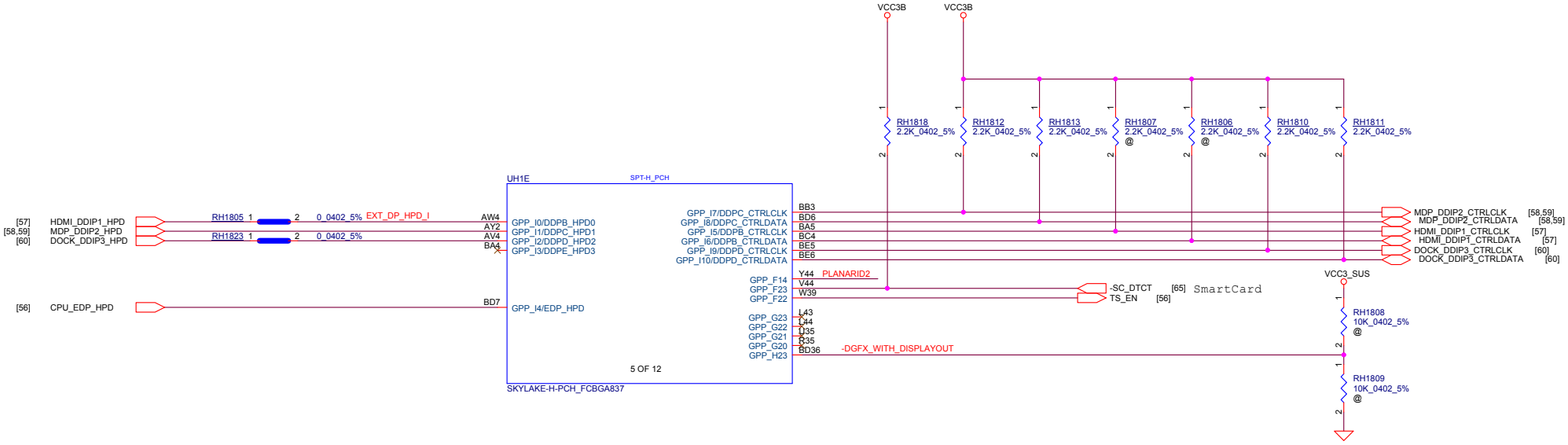
Size: Custom | Document Number: NM-A611 | Rev: 0.1

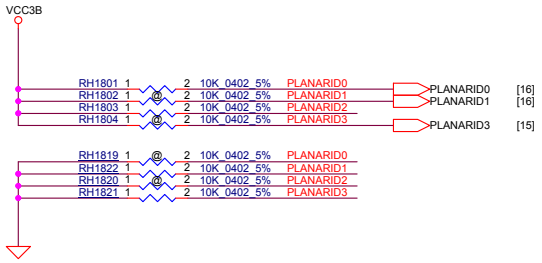
Date: Tuesday, November 03, 2015 | Sheet 17 of 99

to be confirm on SDV

RH1816 1 @ 2 100K_0402_5% HDMI_DDIP1_HPD
RH1814 NODPRE@1 2 100K_0402_5% MDP_DDIP2_HPD
RH1817 1 2 100K_0402_5% DOCK_DDIP3_HPD
RH1815 1 2 100K_0402_5% CPU_EDP_HPD

DDIP2_HPD : PS8330 has Int.PD 150K

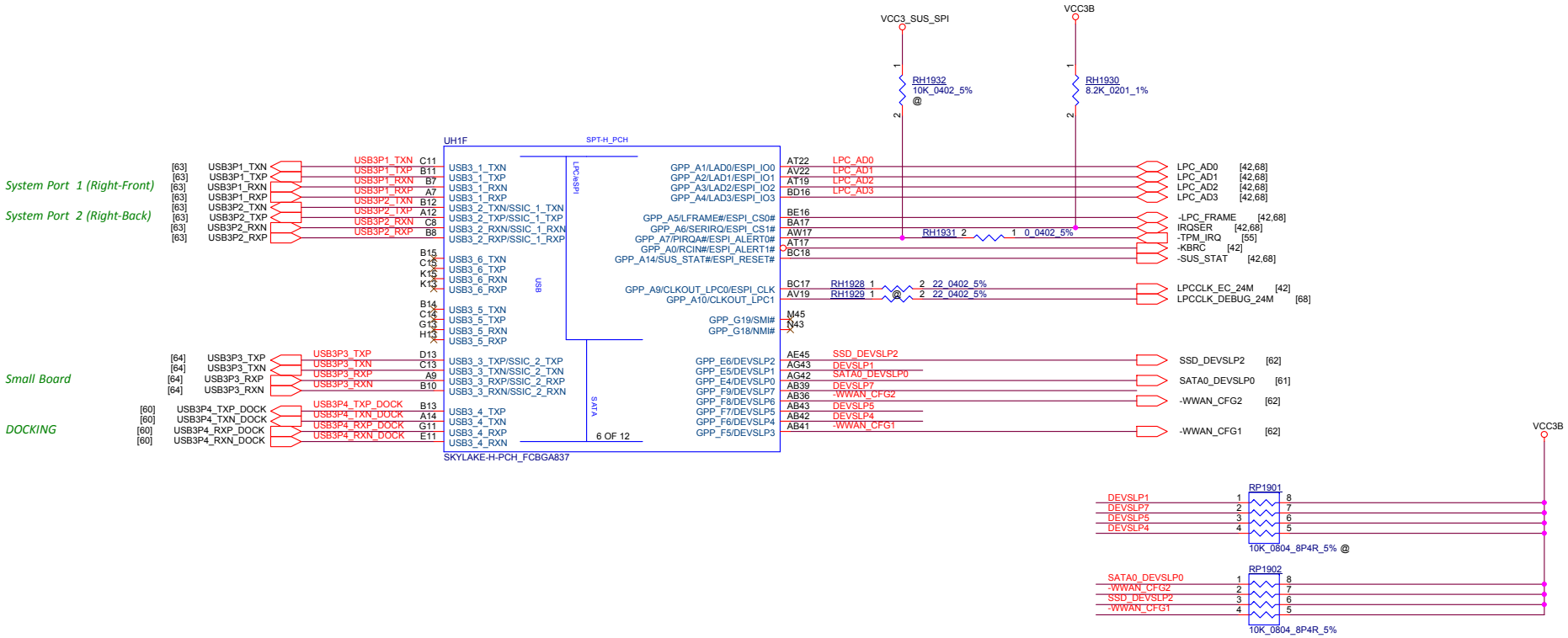




TABLE

	PLANAR ID			
	3	2	1	0
SDV	0	0	0	0
FVT	0	0	0	1
FVT2	0	0	1	0
SIT	0	0	1	1
SWG FVT	0	1	0	0
SWG SIT UMA SVT	0	1	0	1

Title		
PCH SKL-H : DDI CONTROL		
Size: Custom	Document Number: NM-A611	Rev: 0.1
Date: Tuesday, November 03, 2015	Sheet 18 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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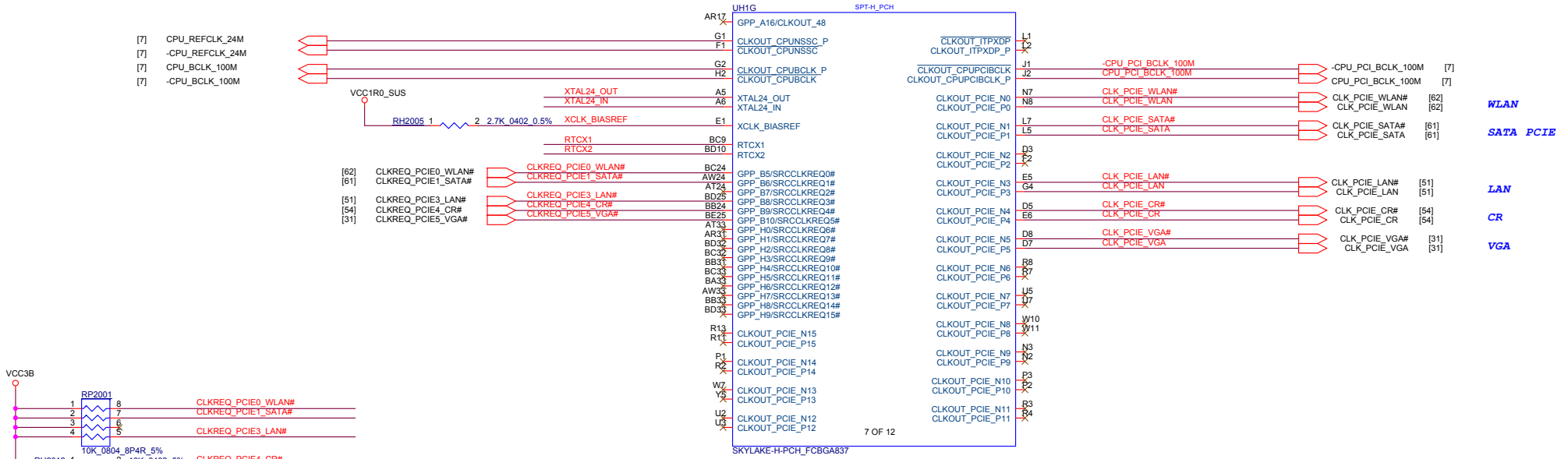
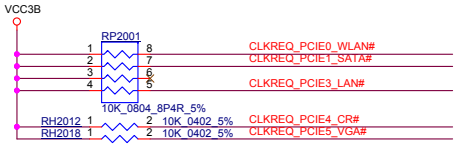
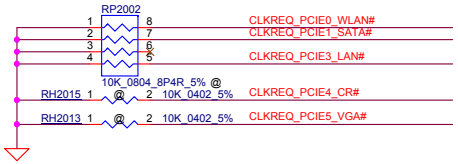
Title: **PCH SKL-H : USB3/LPC**

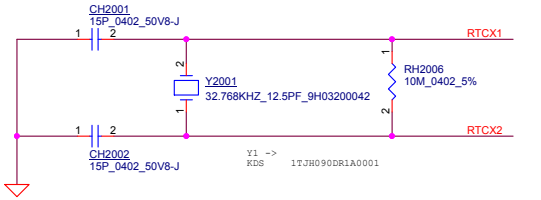
Size	Document Number	Rev
Custom	NM-A611	0.1

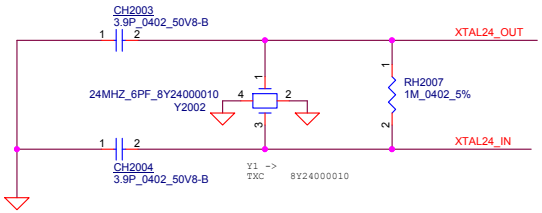
Date: Tuesday, November 03, 2015 Sheet 19 of 99











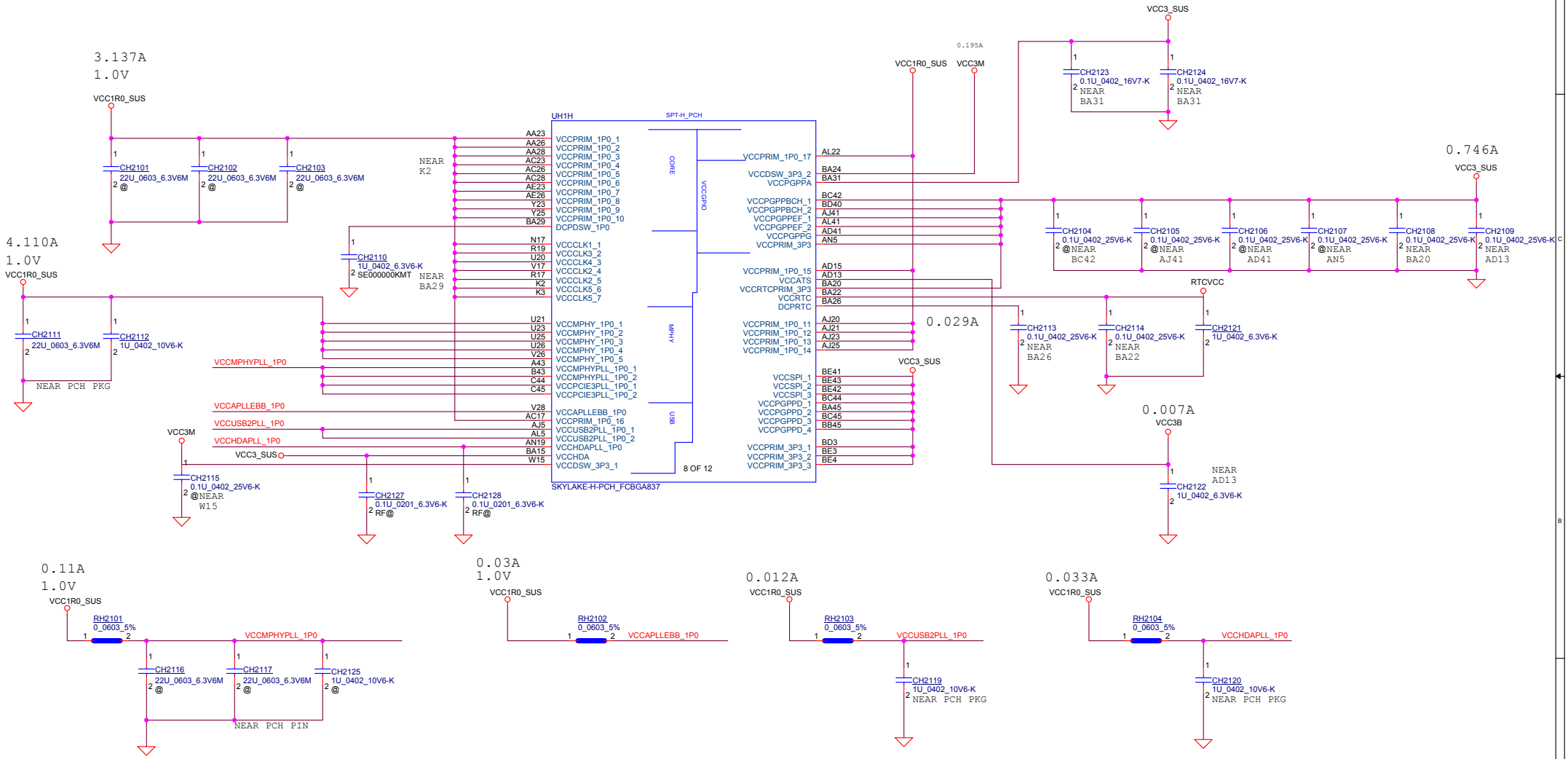
PCIE Clock Assignment
Clock 0 : WLAN
Clock 1 : SATA
Clock 3 : Giga LAN
Clock 4 : CARD READER
Clock 5 : GPU N16S-GT

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : CLK

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 20 of 99



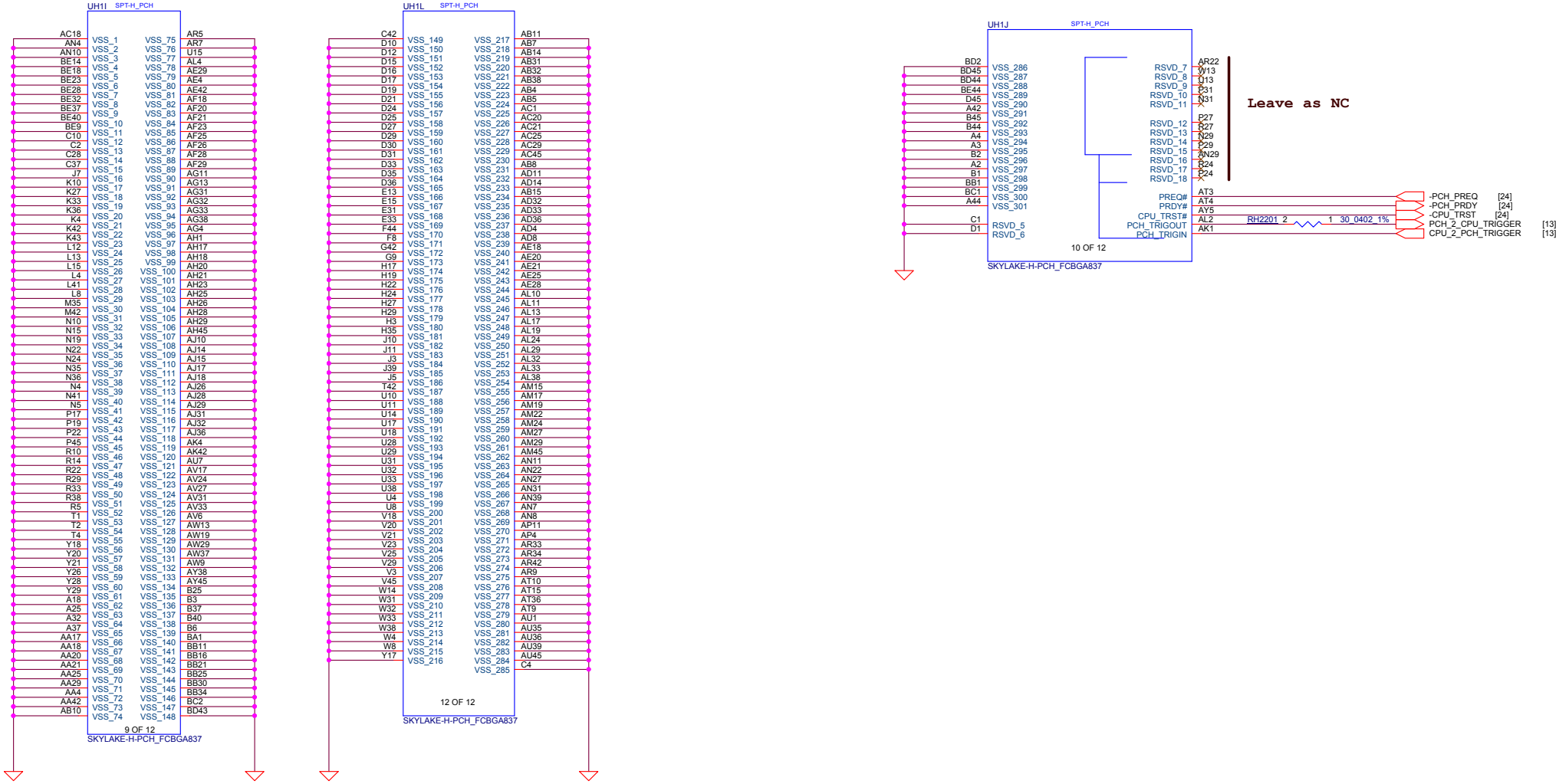
Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **PCH SKL-H : POWER**

Size	Document Number	Rev
Custom	T460P	0.1

NM-A611

Date: Tuesday, November 03, 2015 Sheet 21 of 99

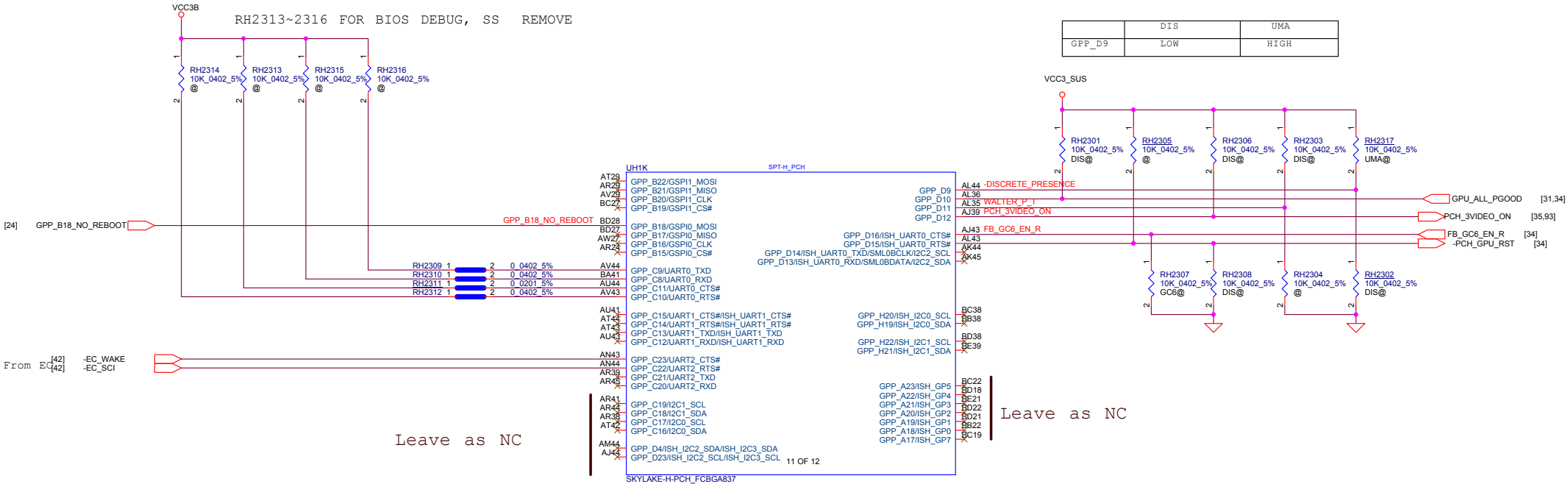


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : GND/RSVD

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 22 of 99



	DIS	UMA
GPP_D9	LOW	HIGH

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : GSPI/UART/I2C

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 23 of 99

R2420,R2422,R2423,R2407,R2410,R2413,R2415,R2401 NEAR BY PCH

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

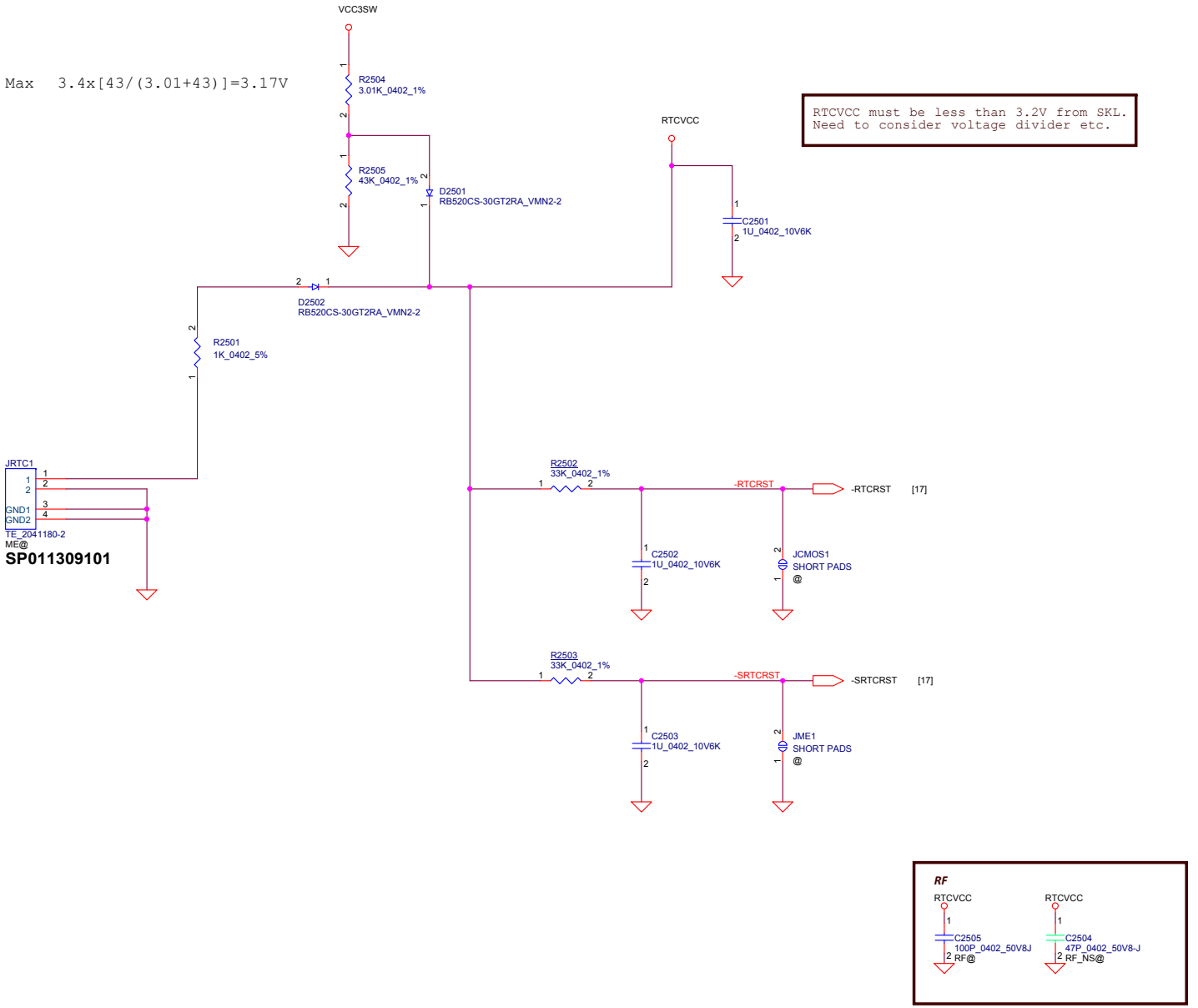
GPP_B18/GSPI0_MOSI (No Reboot)		R2406
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **XDP CONNECTOR**

Size	Document Number	Rev
Custom	T460P	0.1
Date: Tuesday, November 03, 2015	Sheet 24 of 99	NM-A611



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

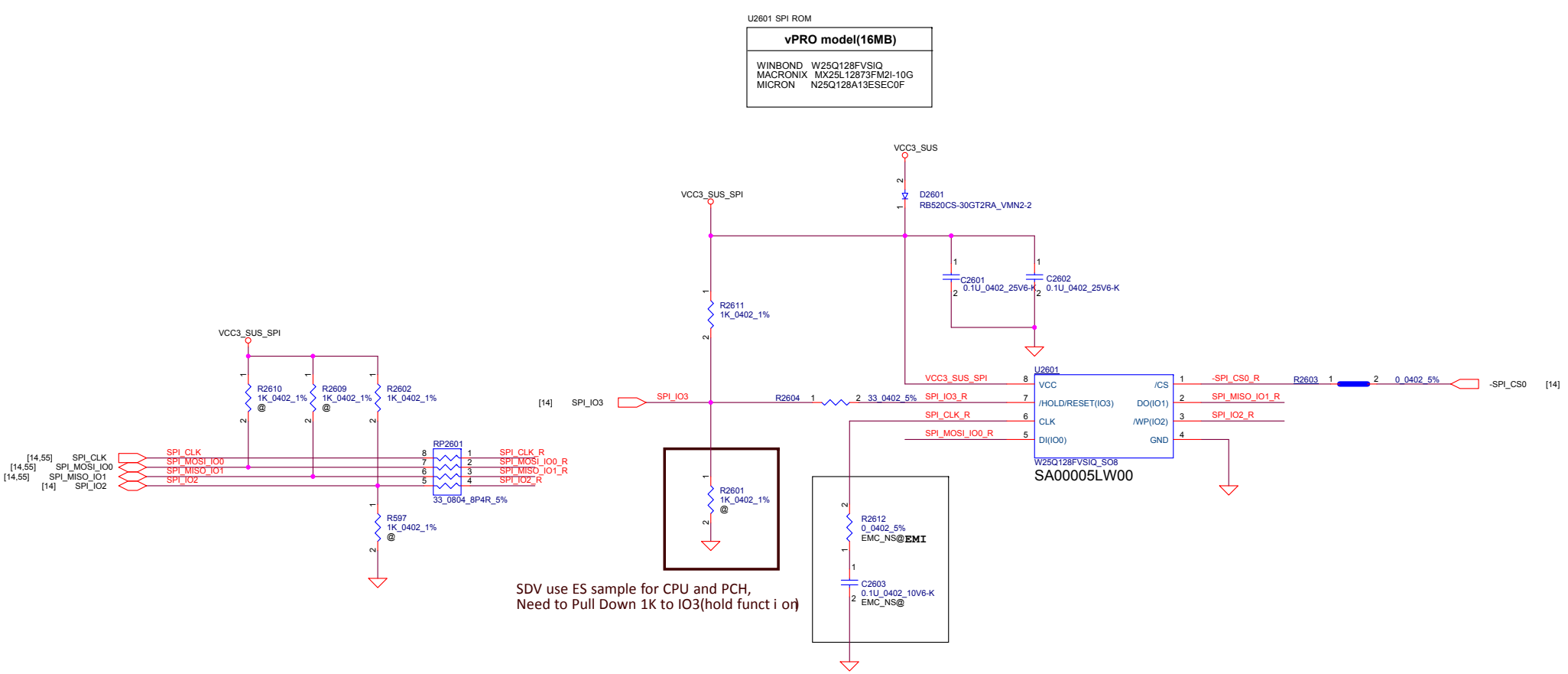
Title: **RTC BATTERY**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 25 of 99

U2601 SPI ROM

vPRO model(16MB)
WINBOND W25Q128FVSIQ MACRONIX MX25L12873FM2I-10G MICRON N25Q128A13ESEC0F



SDV use ES sample for CPU and PCH,
Need to Pull Down 1K to IO3(hold funct i on)

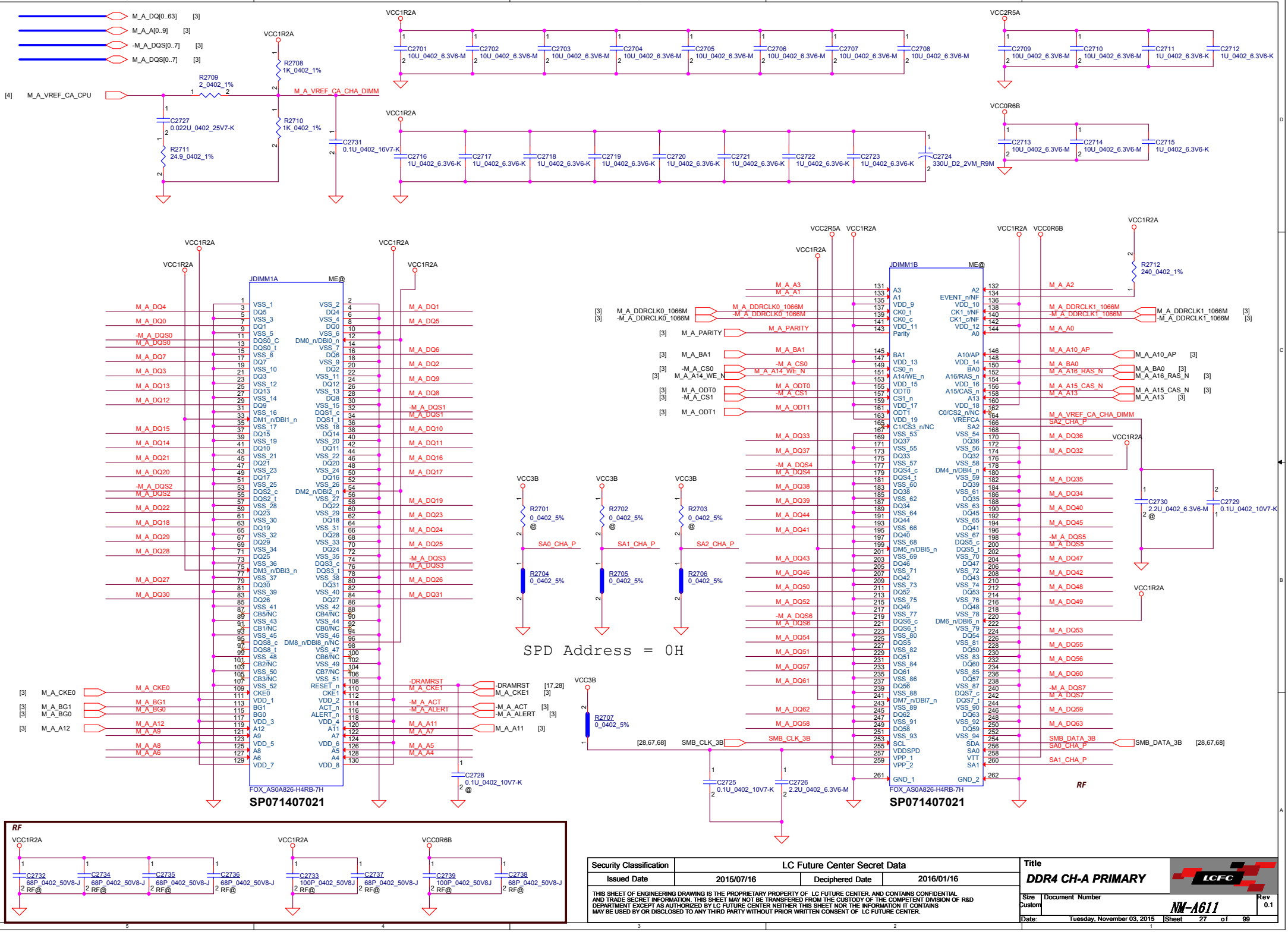
Vinafix

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: SPI FLASH

Size	Document Number	Rev
Custom	NM-A611	0.1

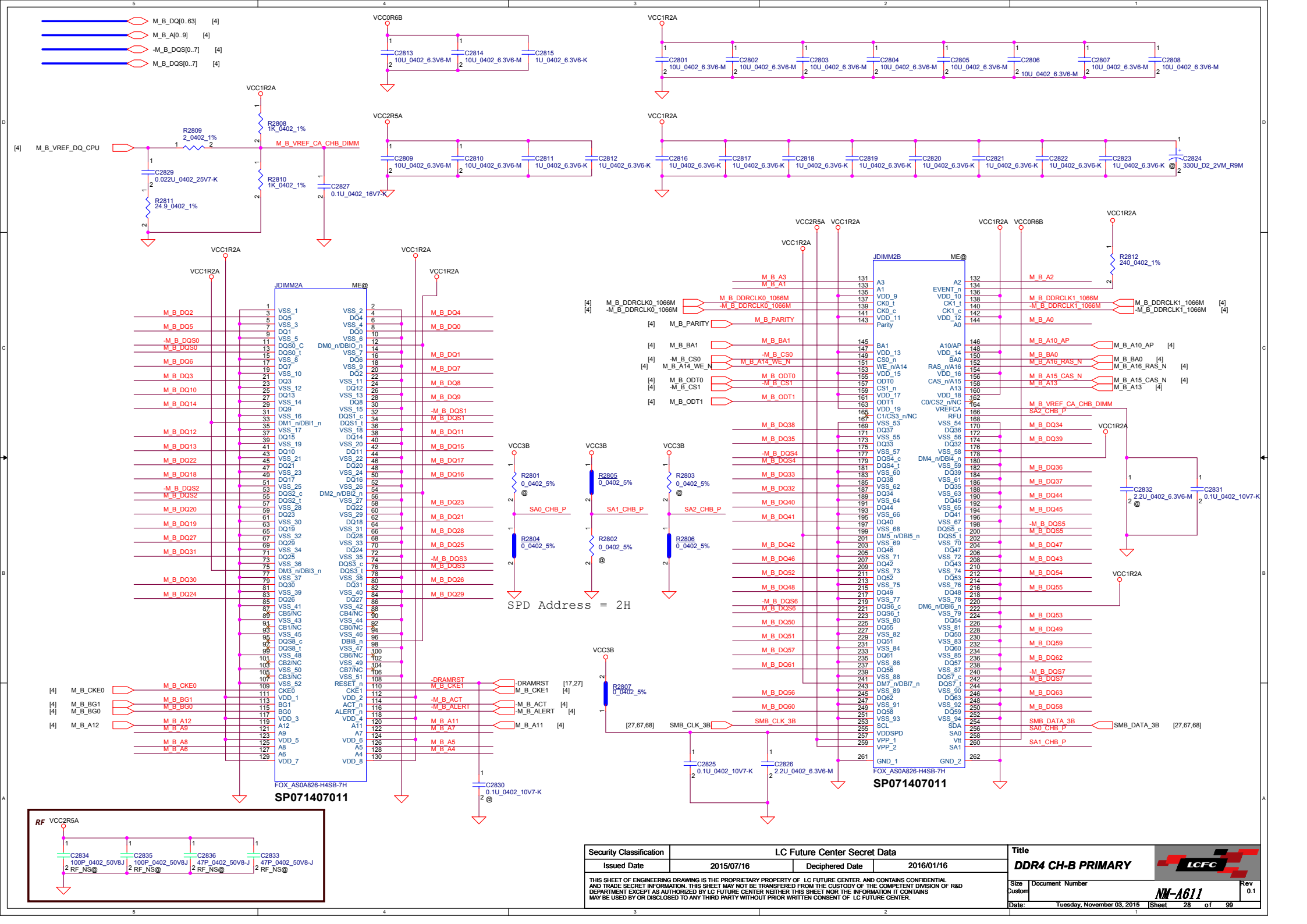
Date: Tuesday, November 03, 2015 Sheet 26 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **DDR4 CH-A PRIMARY**

Size: Custom	Document Number: NM-A611	Rev: 0.1
Date: Tuesday, November 03, 2015	Sheet 27 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **DDR4 CH-B PRIMARY**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 28 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title

Size	Document Number	Rev
Custom	NM-A611	0.1

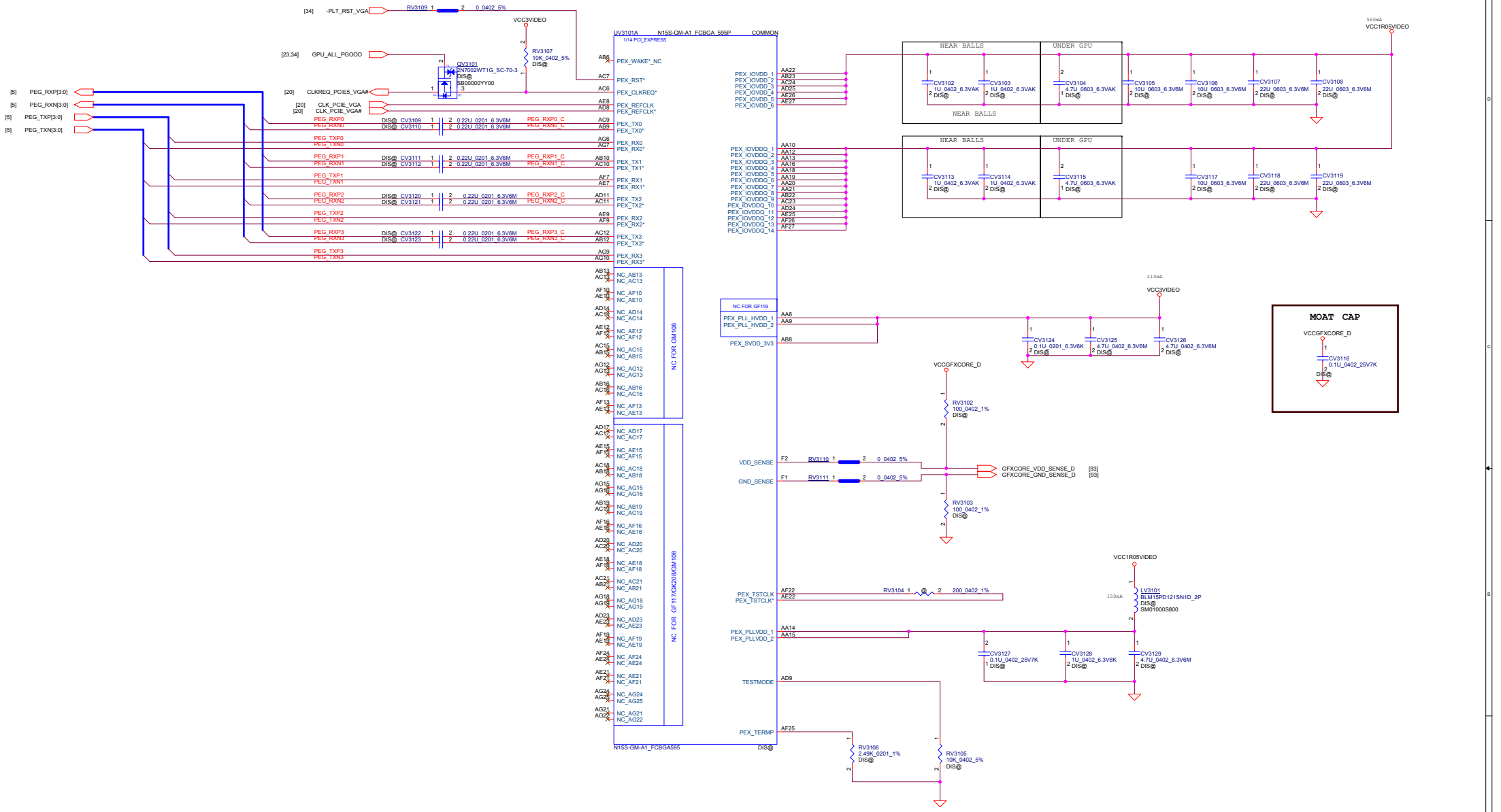
Date: Tuesday, November 03, 2015 Sheet 29 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 30 of 99

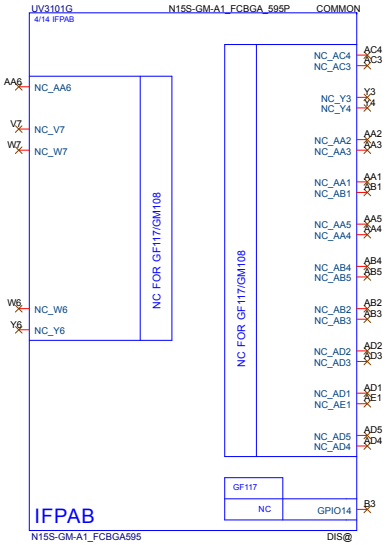


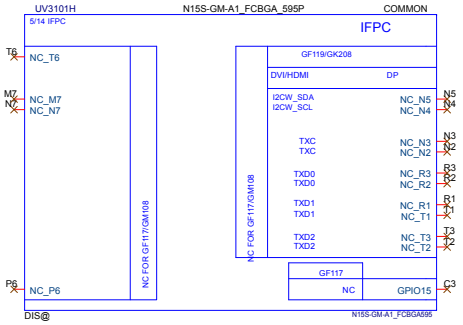
Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

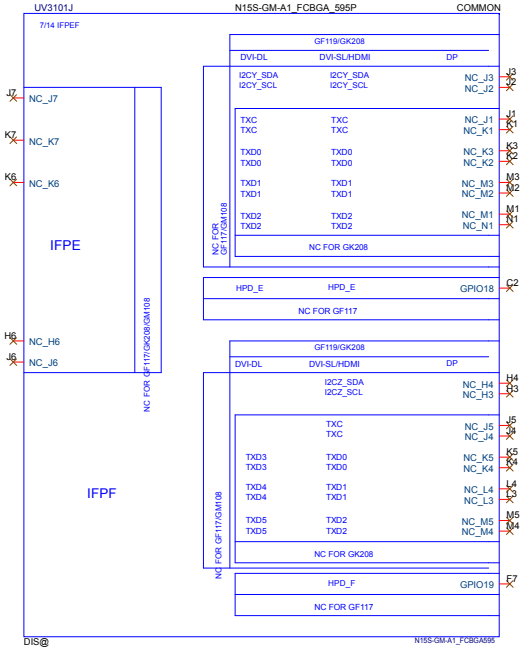
Title: **N16S-GT(1/6) PEG I/F**

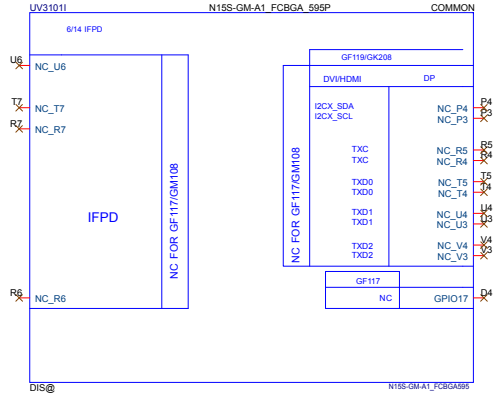
Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 31 of 99









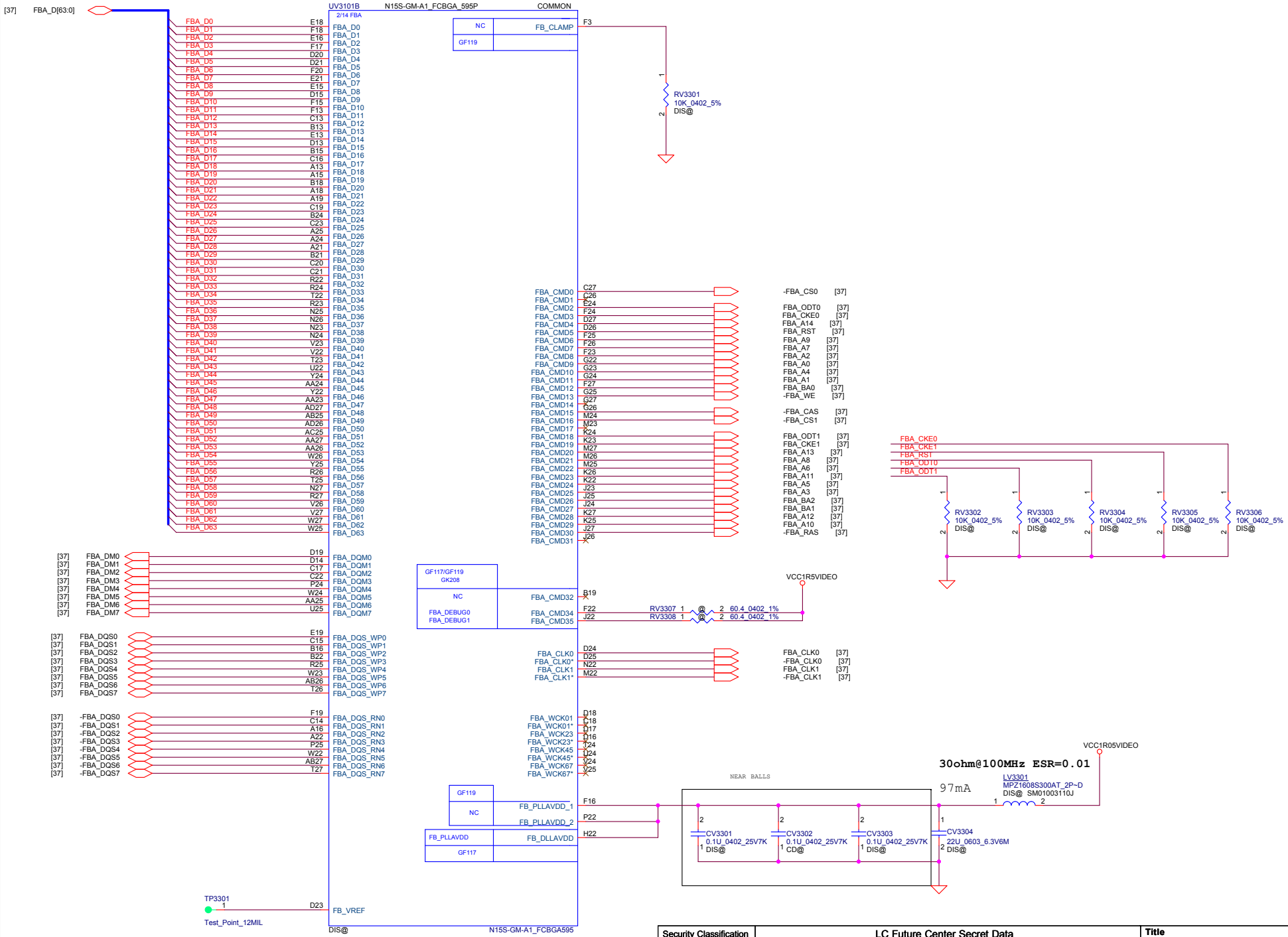
CB_1_SWG_SDV_EC006

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: *N16S-GT(2/6) DIGITAL OUT I/F*

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 32 of 99

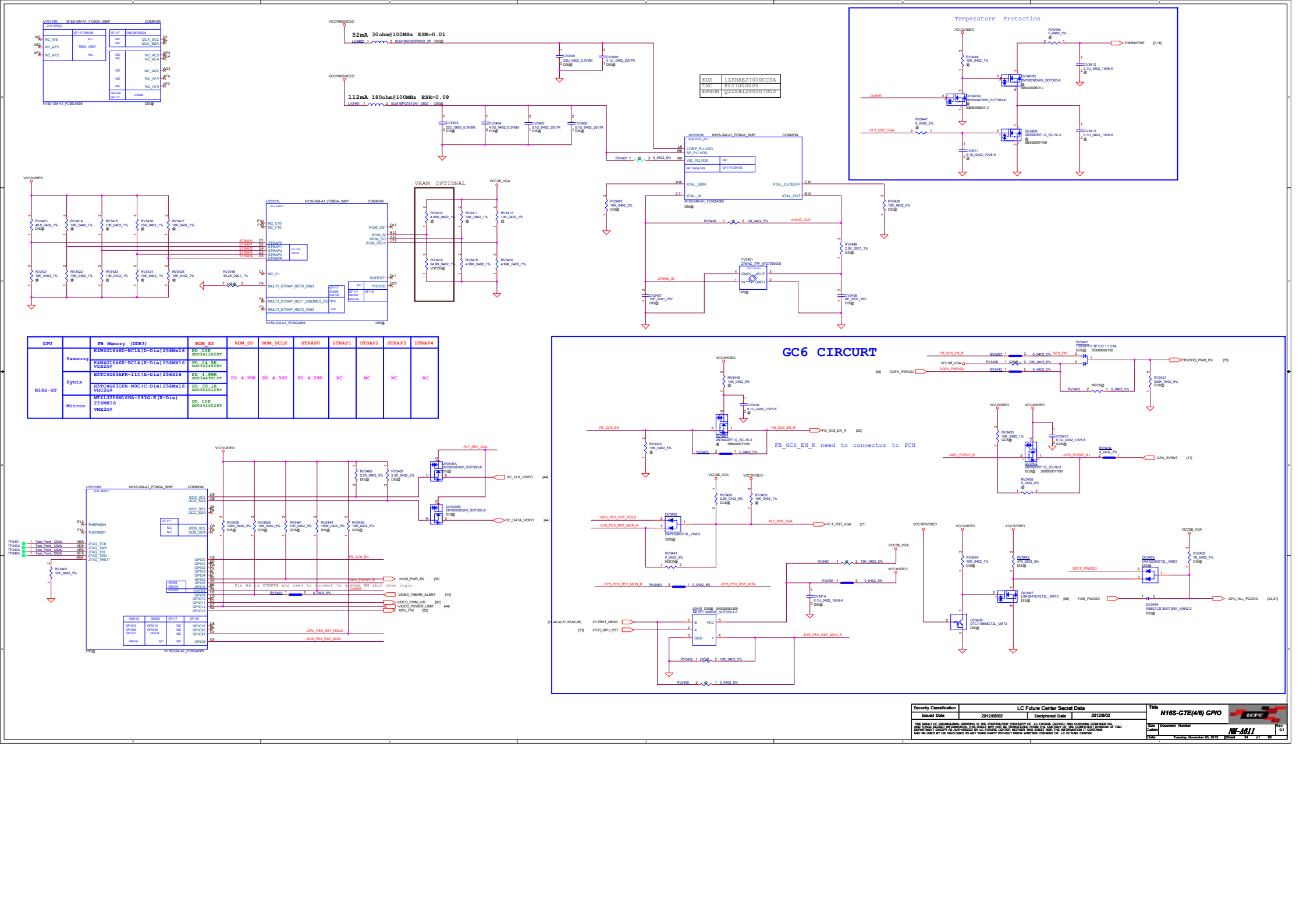


Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: N16S-GT(3/6) VRAM I/F

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 33 of 99



GPU		FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GT	Samsung	K4W4G1646D-BC1A(D-Die)256Mx16	PD 15K SD03415028	PD 4.99K	PD 4.99K	PU 4.99K	NC	NC	NC	NC
		K4W4G1646E-BC1A(E-Die)256Mx16 VSE2G8	PD 24.9K SD03424928							
	Hynix	H5TC4G63AFR-11C(A-Die)256X16 VHC2G8	PD 4.99K SD03449910							
		H5TC4G63CFR-N0C(C-Die)256Mx16 VHC2G8	PD 30.1K SD03430128							
	Micron	MT41J256M16HA-093G:E(E-Die) 256MX16 VME2G8	PD 10K SD03410028							

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: N16S-GTE(4/6) GPIO

Size	Document Number	Rev
Custom	NKE-A811	0.1

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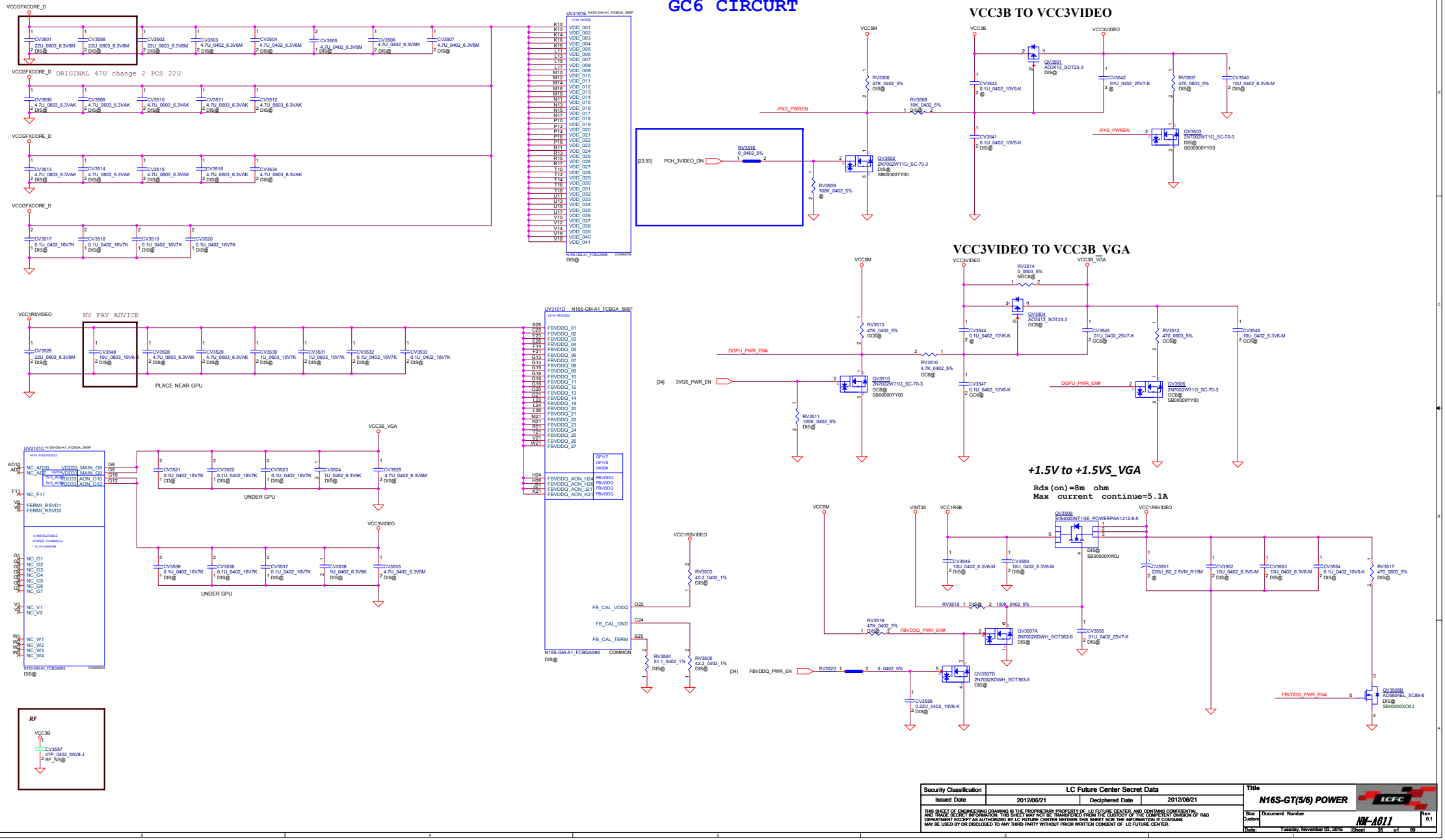
GC6 CIRCURT



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

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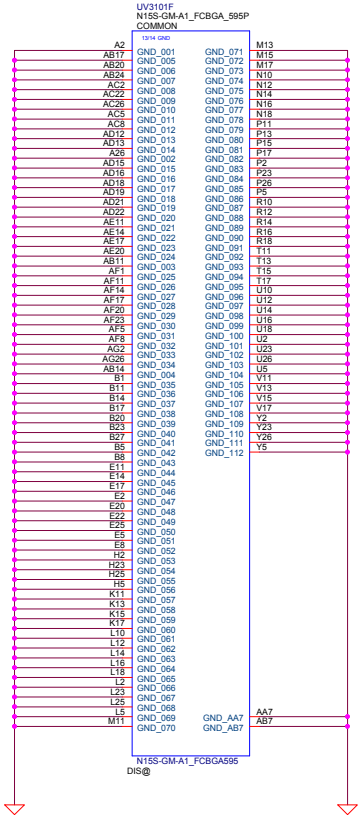
Title: N16S-GT(5/6) POWER

Size: Custom | Document Number: NM-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 35 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: **N16S-GT(6/6) GND**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 36 of 99

FB CMD mapping Mode D-N14x

TABLE
DDR3 VIDEO MEMORY

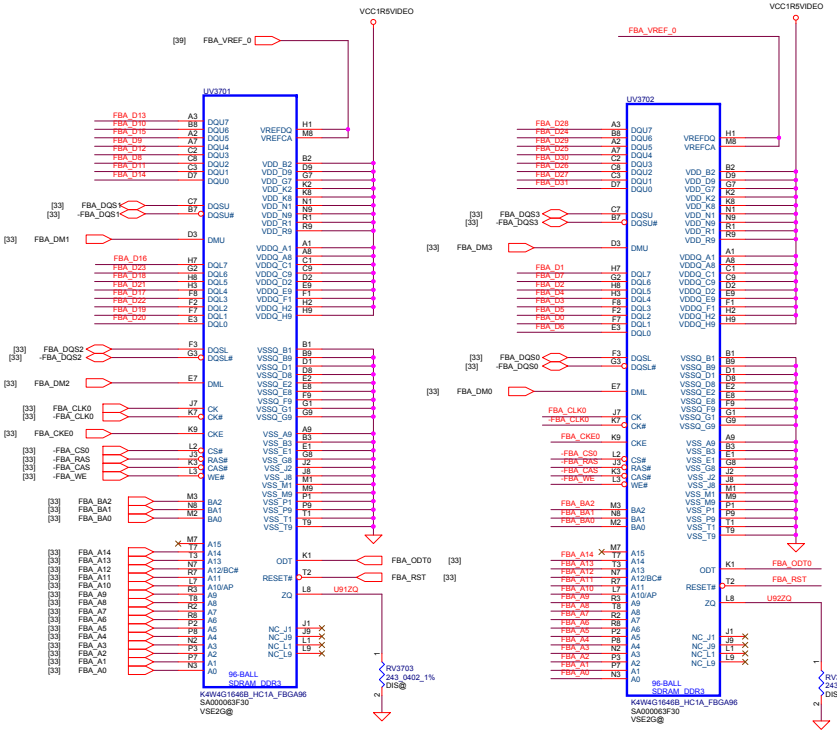
	Micron 4GBITS (256Mx16)	HYNIX 4GBITS(256Mx16)	SAMSUNG 4GBITS(256Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
UV3701 UV3702 UV3703 UV3704	MT41J256M16HA-093G:E(E-Die) 256MX16 SA000060I00	H5TC4G63AFR-11C (A-Die)256X16 SA00005YL10	K4W4G1646D-BC1A (D-Die)256Mx16 SA000063F00	K4W4G1646E-BC1A (E-Die)256MX16(LCFC USE) SA000063F30	H5TC4G63CFR-N0C(C-Die) 256Mx16(LCFC USE) SA00007DU00
BOM Structure	VME2G@	VHA2G@	VSD2G@	VSE2G@	VHC2G@

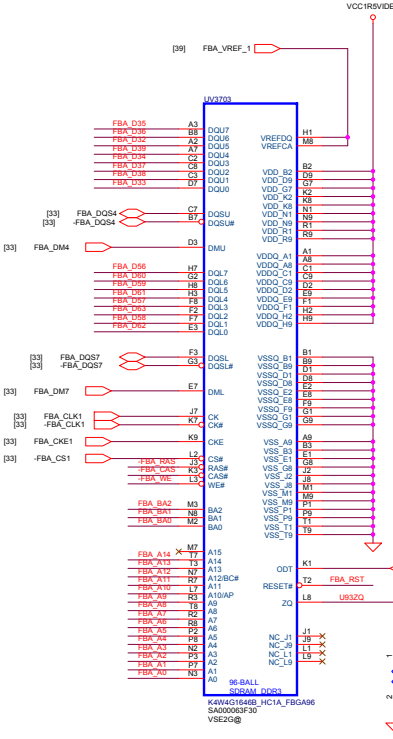
* FOR SDV

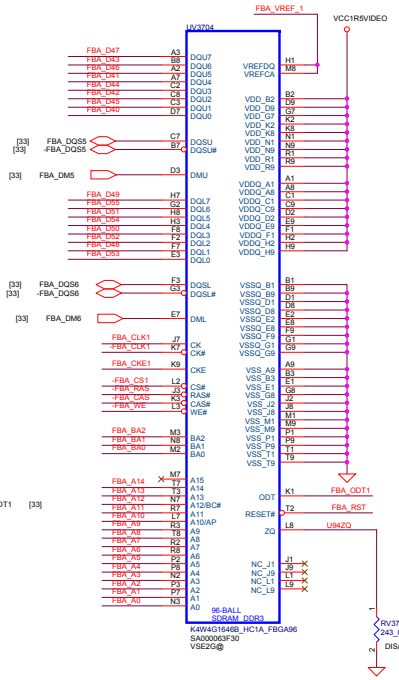
[33] FBA_D[63:0]

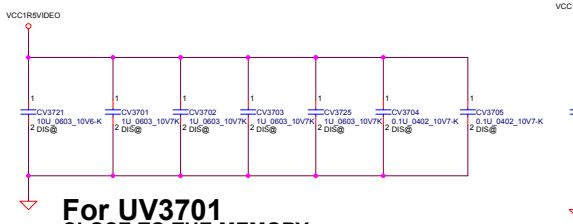
FBA_CLK0 — RV3702 162_0402_1% DIS@ — -FBA_CLK0

FBA_CLK1 — RV3701 162_0402_1% DIS@ — -FBA_CLK1

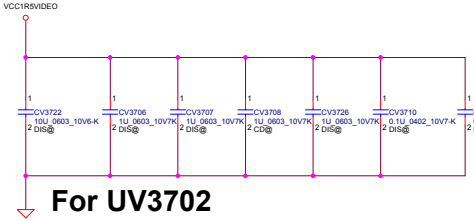




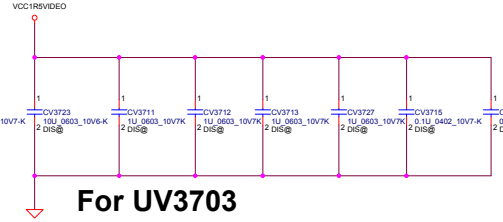




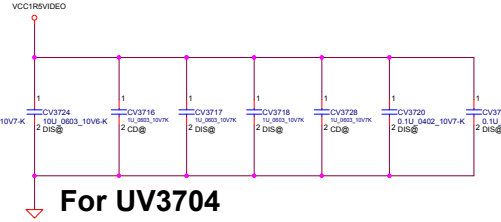
For UV3701
CLOSE TO THE MEMORY



For UV3702
CLOSE TO THE MEMORY



For UV3703
CLOSE TO THE MEMORY



For UV3704
CLOSE TO THE MEMORY

Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: N16S-GT VRAM CHANNEL-A

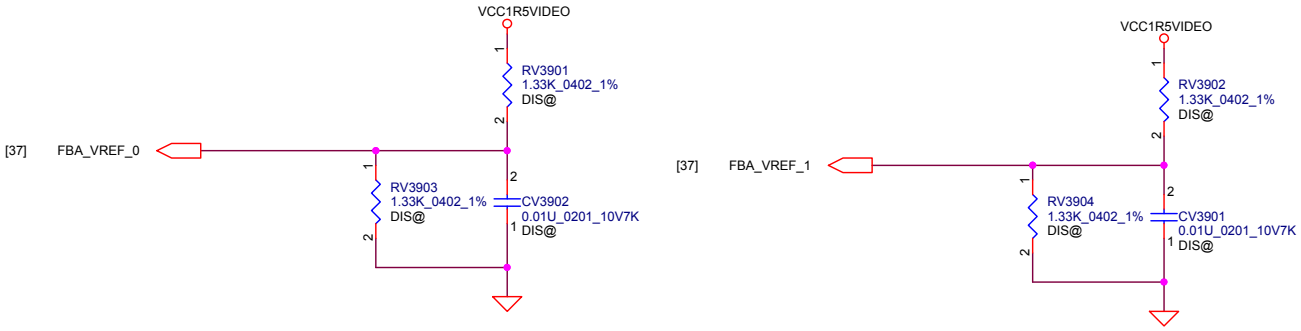
Size: Custom | Document Number: NW-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 37 of 99

Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/08/21	Deciphered Date	2012/08/21	N16S-GT VRAM CHANNEL-A

Size	Document Number	Rev
	NW-A011	0.1

Date: Tuesday, November 05, 2013 Sheet 38 of 57

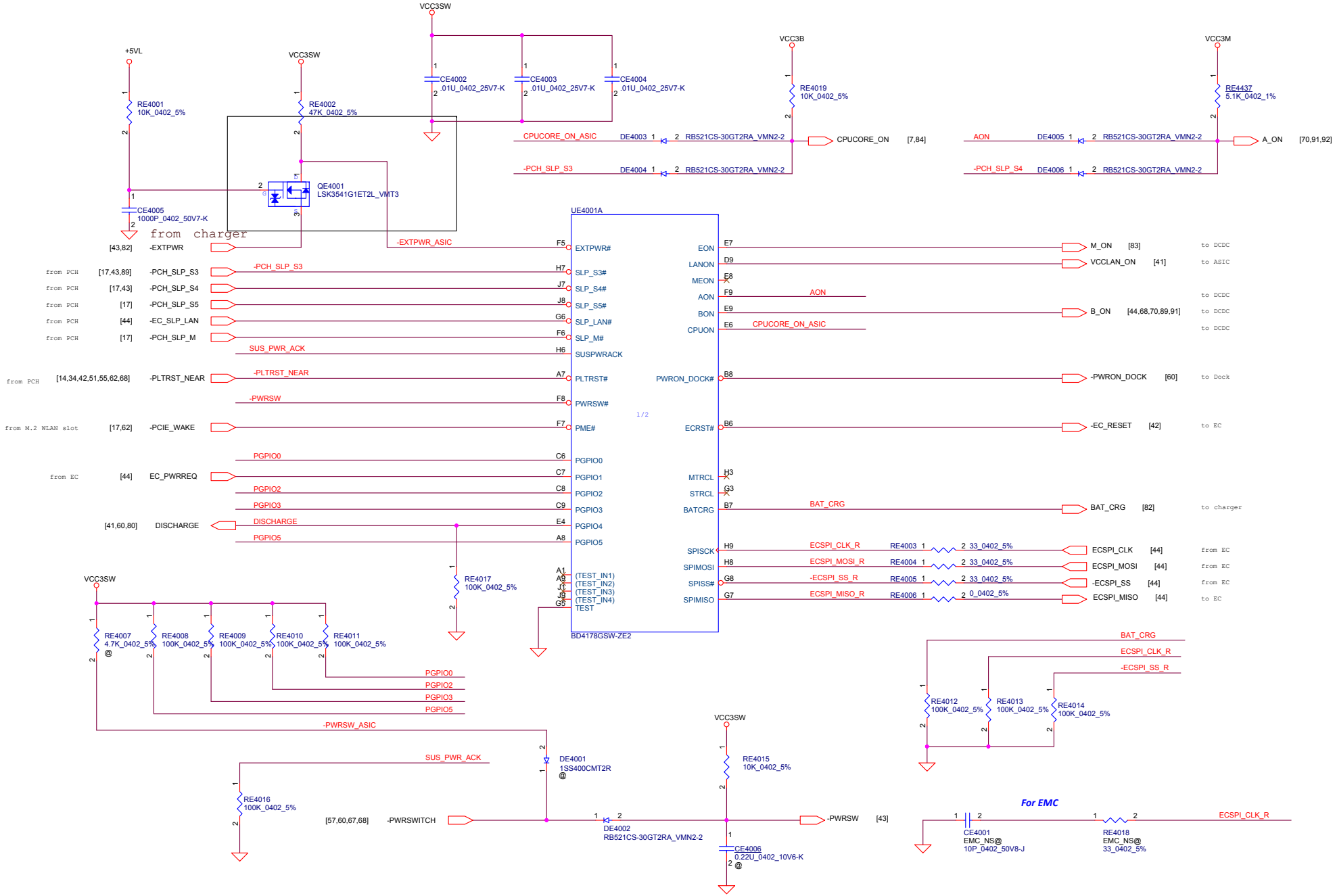


Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **N16S-GT MEMORY TERMINATION**

Size	Document Number	Rev
B	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 39 of 99

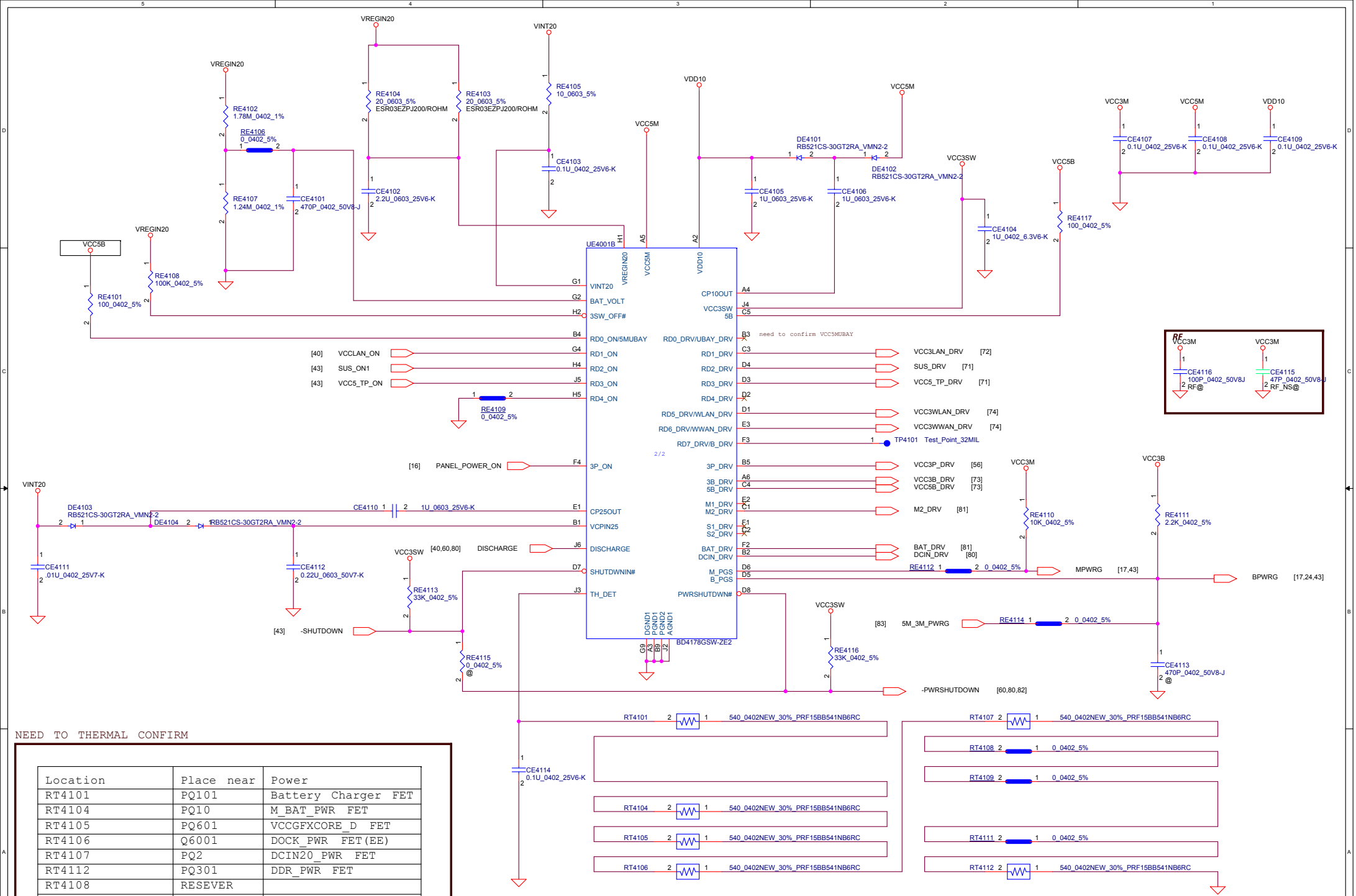


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: THINK ENGINE 2(1/2)

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 40 of 99



NEED TO THERMAL CONFIRM

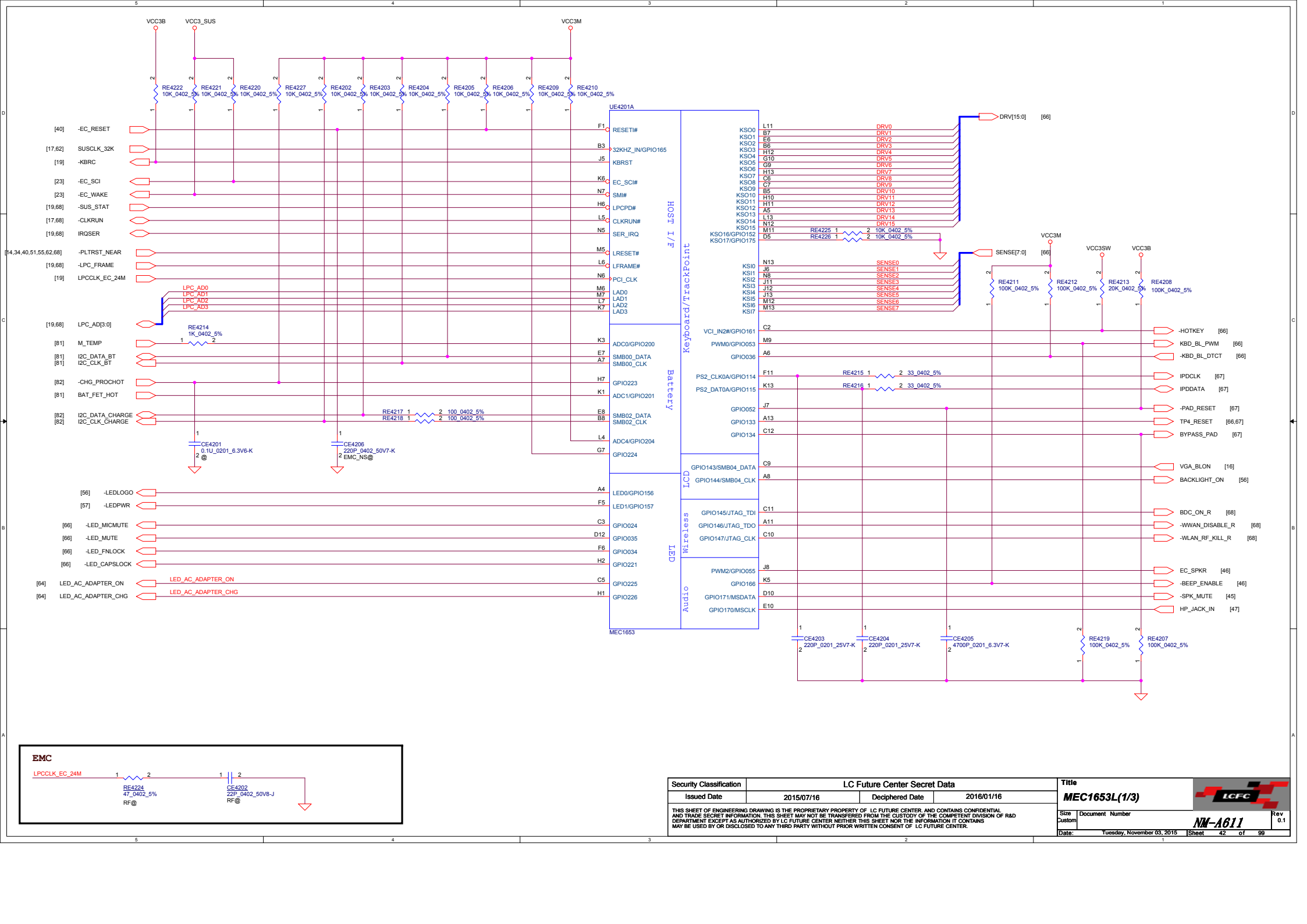
Location	Place near	Power
RT4101	PQ101	Battery Charger FET
RT4104	PQ10	M_BAT_PWR FET
RT4105	PQ601	VCCGFXCORE_D FET
RT4106	Q6001	DOCK_PWR FET(EE)
RT4107	PQ2	DCIN20_PWR FET
RT4112	PQ301	DDR_PWR FET
RT4108	RESEVER	
RT4109	RESEVER	
RT4111	RESEVER	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

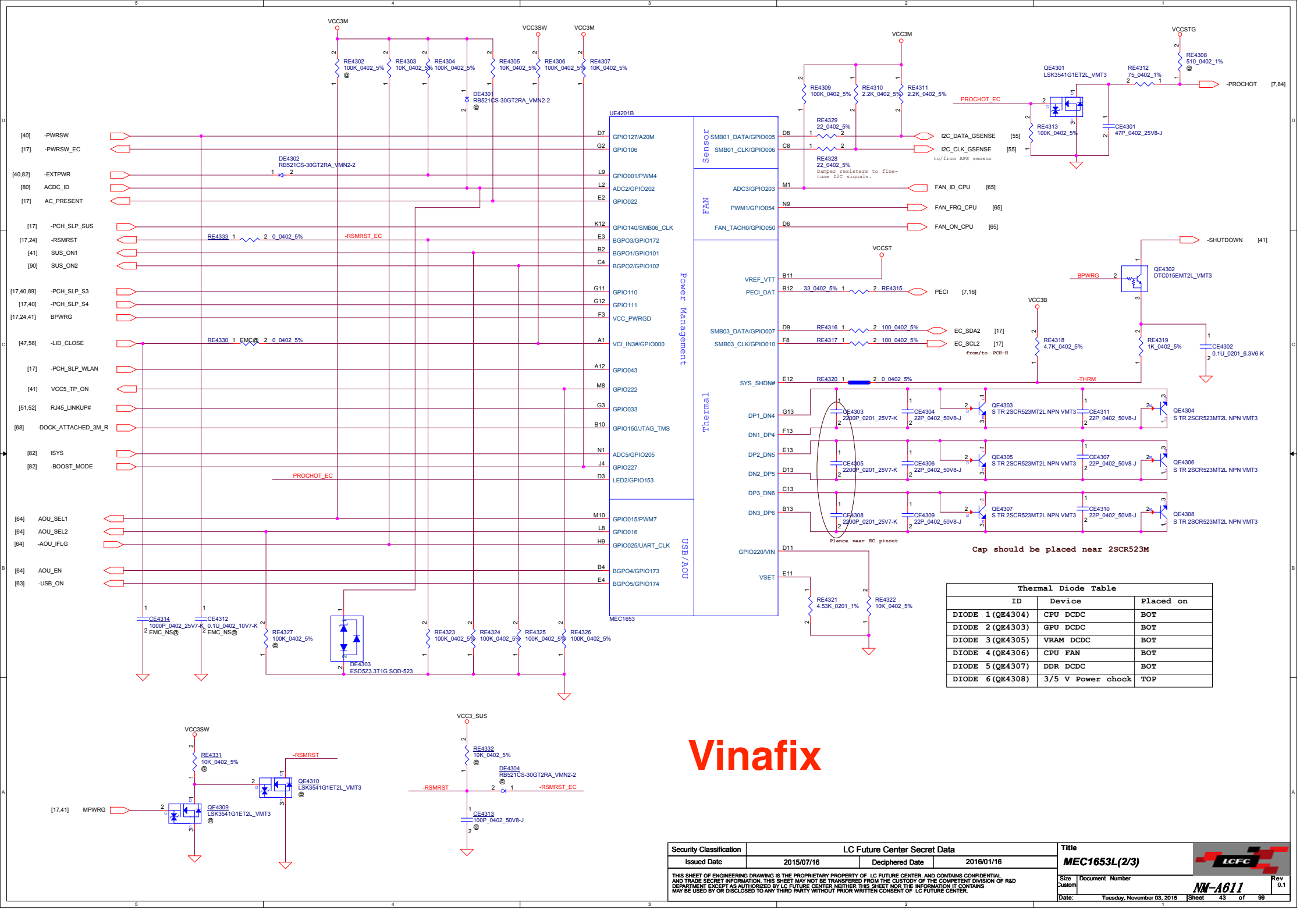
Title: THINK ENGINE 2(2/2)

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 41 of 99



Title		
MEC1653L(1/3)		
Size: Custom	Document Number: NM-A611	Rev: 0.1
Date: Tuesday, November 03, 2015	Sheet 42 of 99	

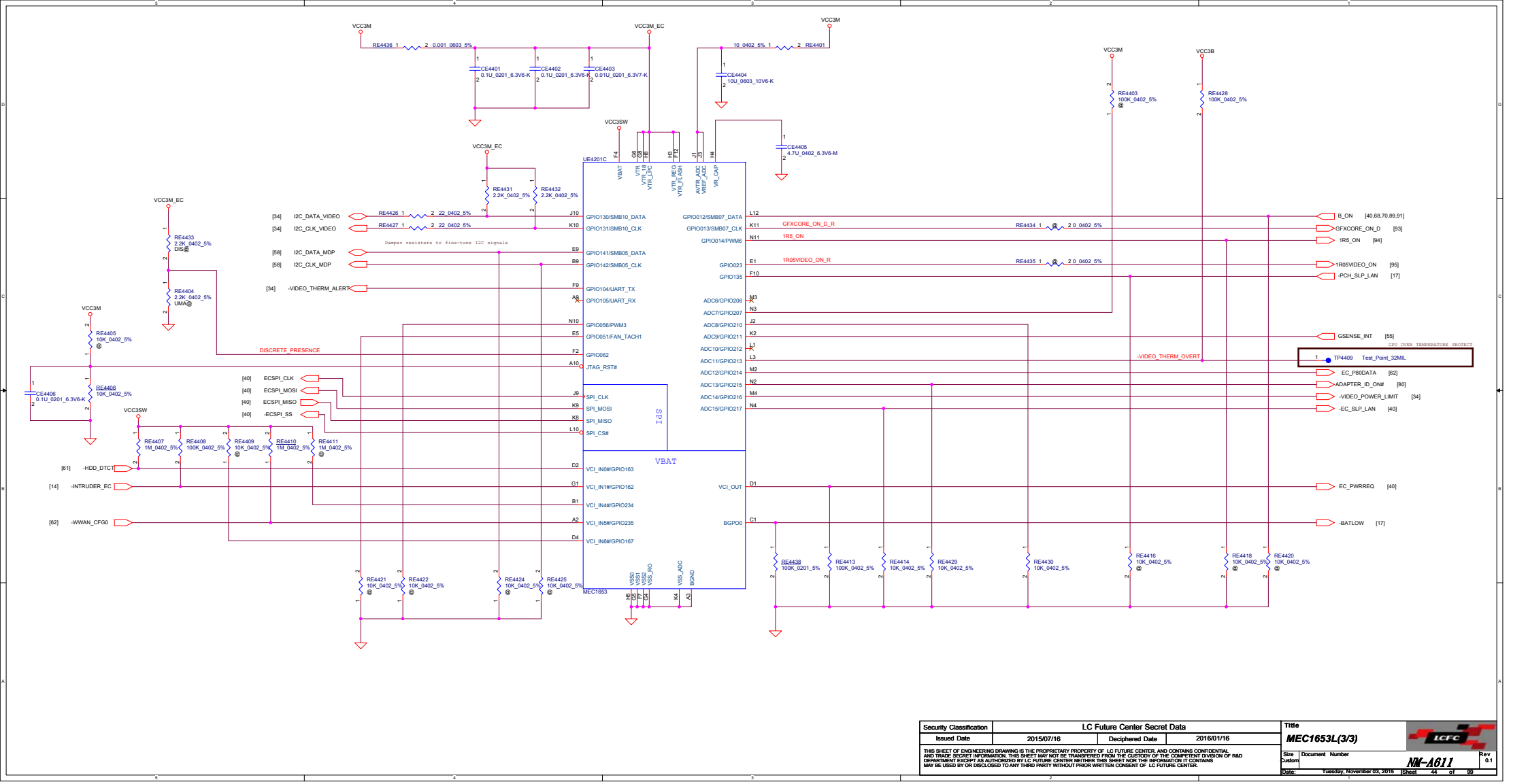


Thermal Diode Table		
ID	Device	Placed on
DIODE 1(QE4304)	CPU DCDC	BOT
DIODE 2(QE4303)	GPU DCDC	BOT
DIODE 3(QE4305)	VRAM DCDC	BOT
DIODE 4(QE4306)	CPU FAN	BOT
DIODE 5(QE4307)	DDR DCDC	BOT
DIODE 6(QE4308)	3/5 V Power chock	TOP

Vinafix

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title	MEC1653L(2/3)		
Size Custom	Document Number	NM-A611	Rev 0.1
Date: Tuesday, November 03, 2015	Sheet 43 of 99		

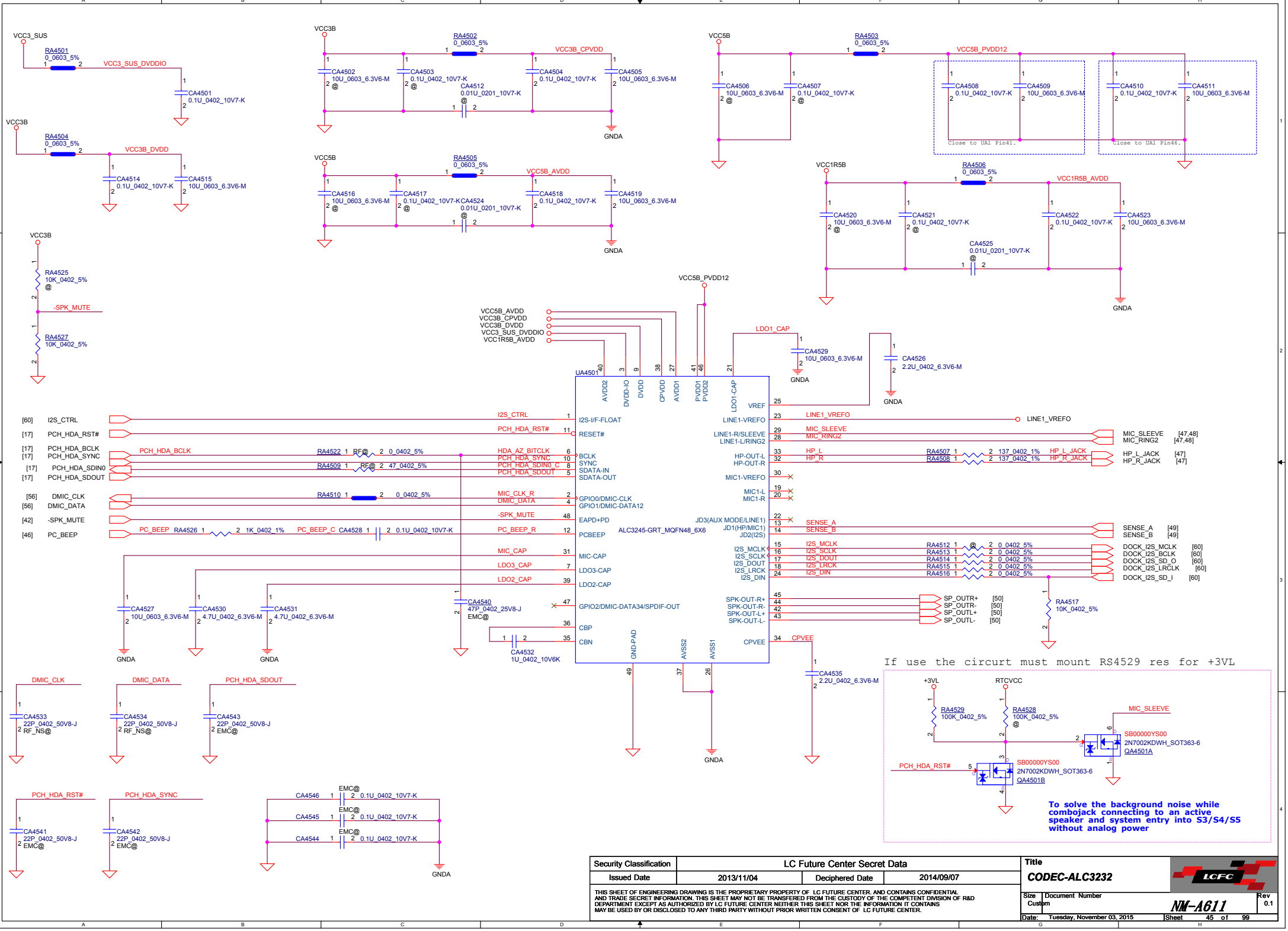


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **MEC1653L(3/3)**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 44 of 99



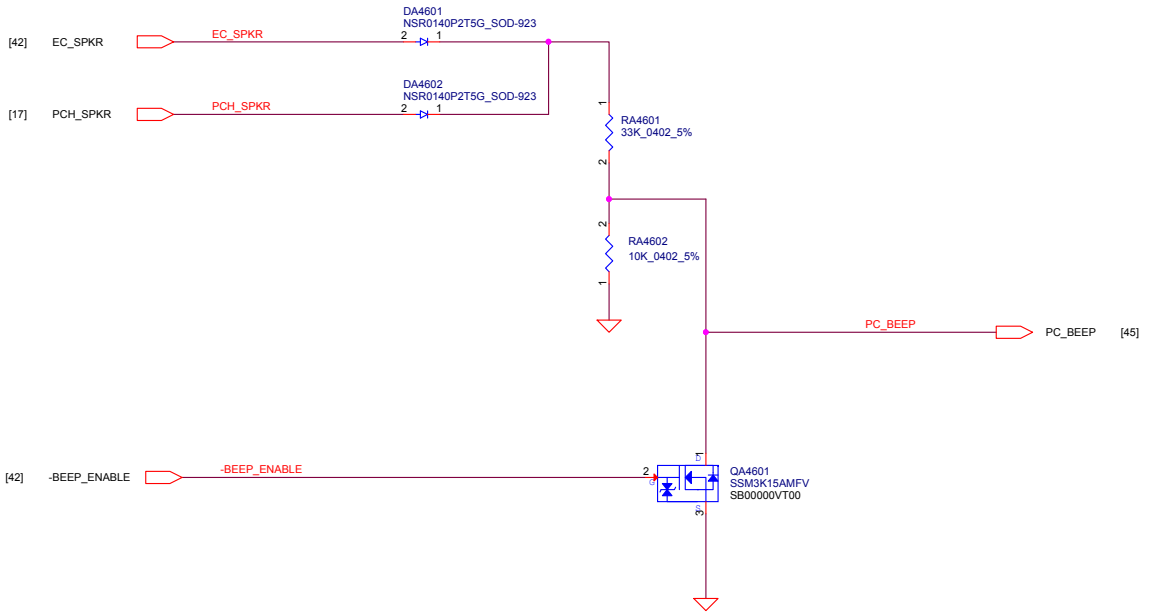
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: CODEC-ALC3232

Size: Custom | Document Number: NM-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 45 of 99

PC-BEEP

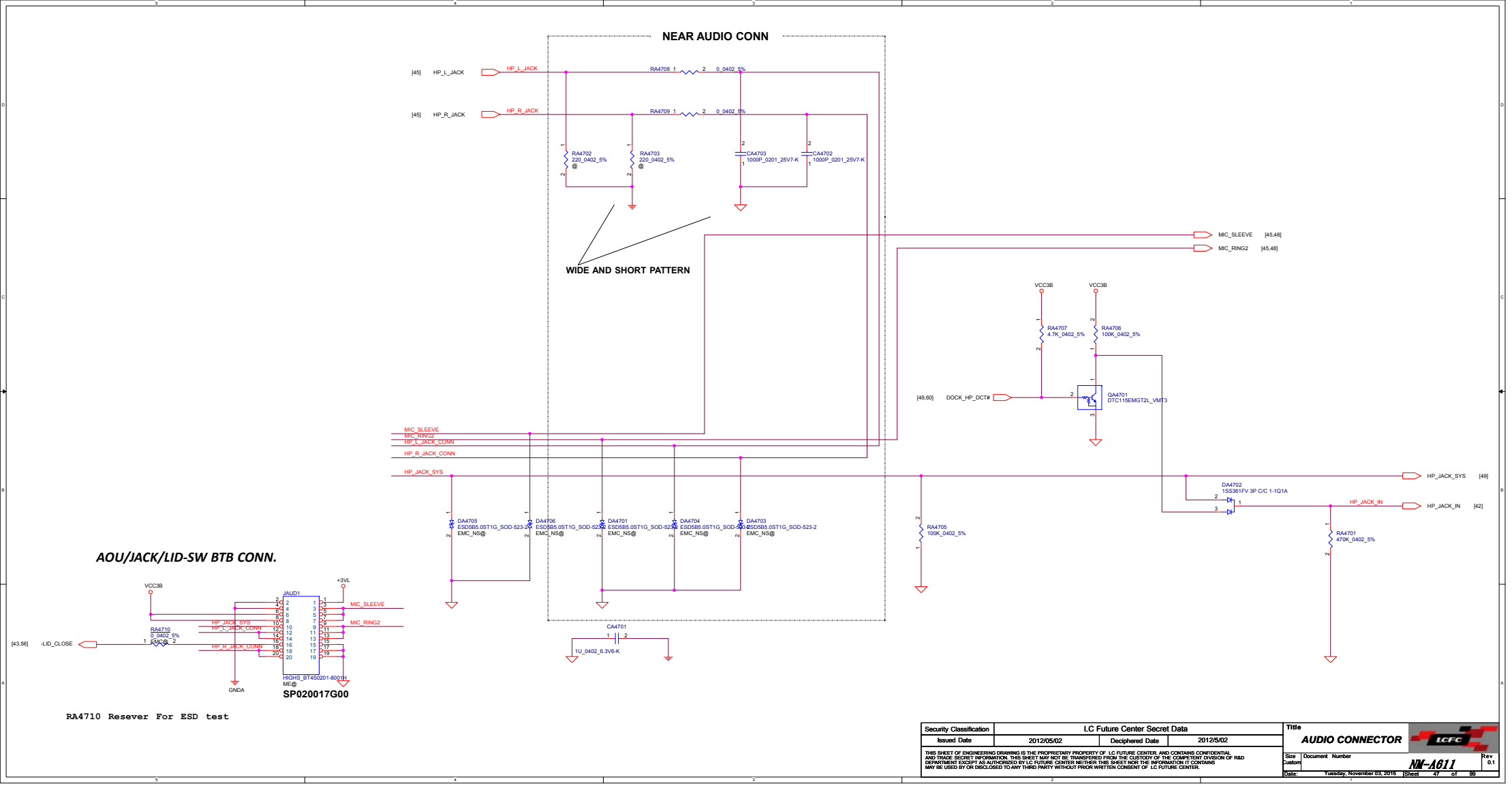


Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO BEEP**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 46 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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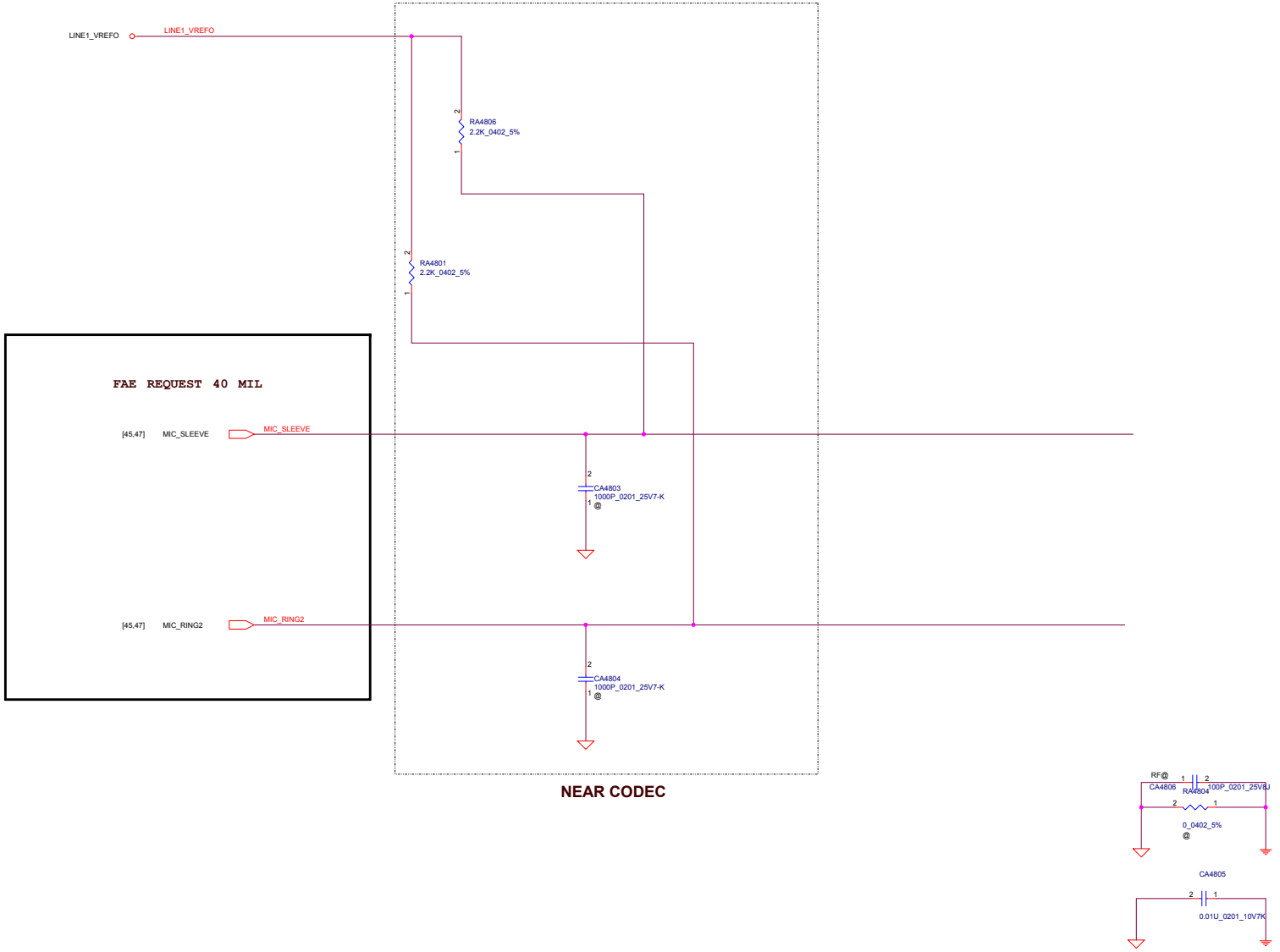
Title: **AUDIO CONNECTOR**

Size	Document Number	Rev
Custom	NM-A611	0.1

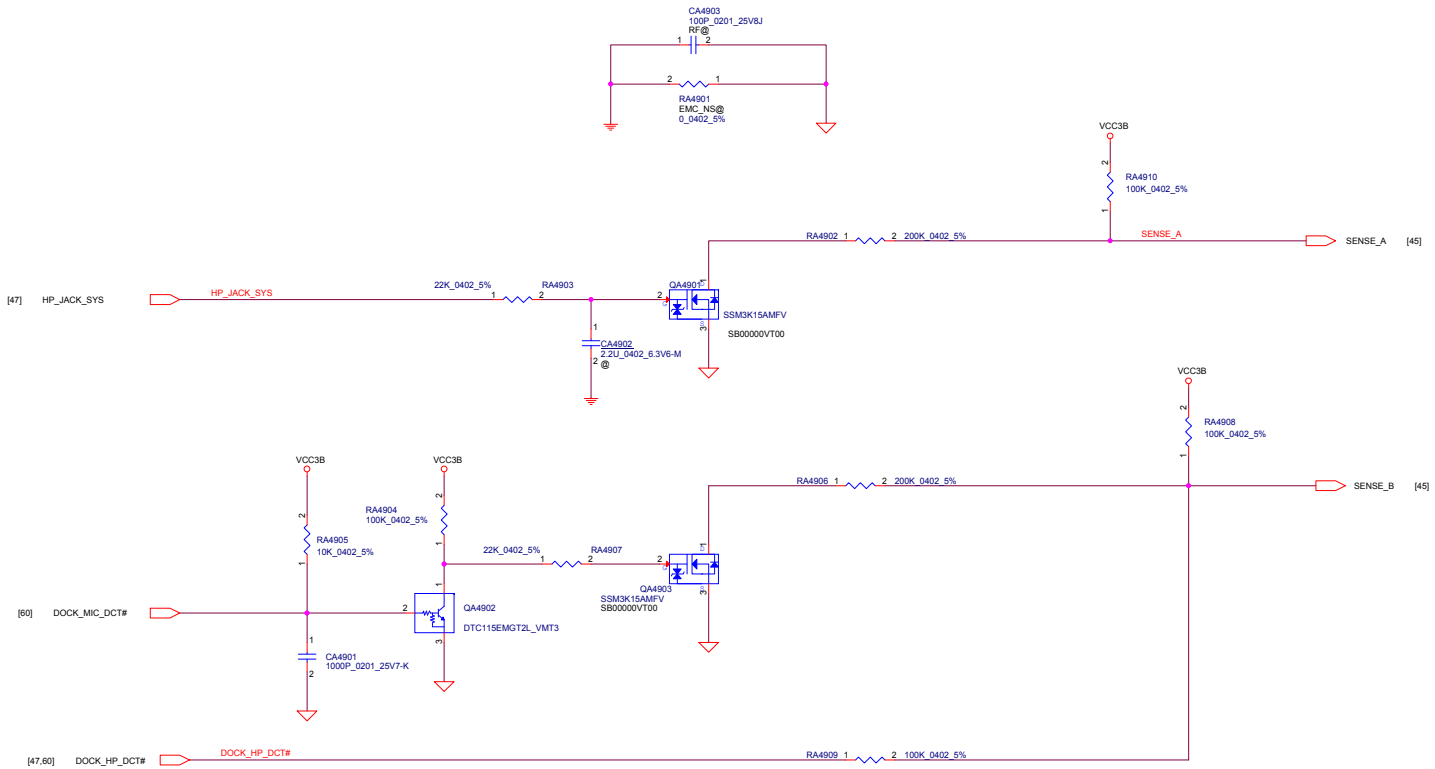
Date: Tuesday, November 03, 2015 Sheet 47 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: AUDIO EXT MIC I/F

Size: Custom	Document Number: T460P	Rev: 0.1
	NM-A611	
Date: Tuesday, November 03, 2015	Sheet 48 of 99	



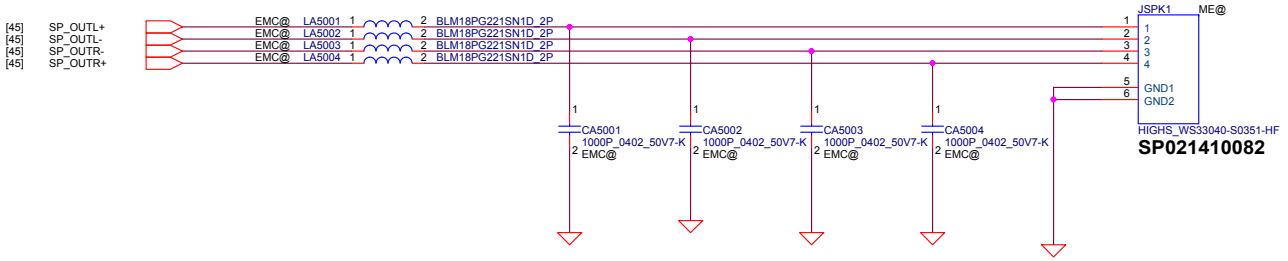
Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO JACK SENSE**

Size	Document Number	Rev
Custom	C NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 49 of 99

SPEAKER CONN.



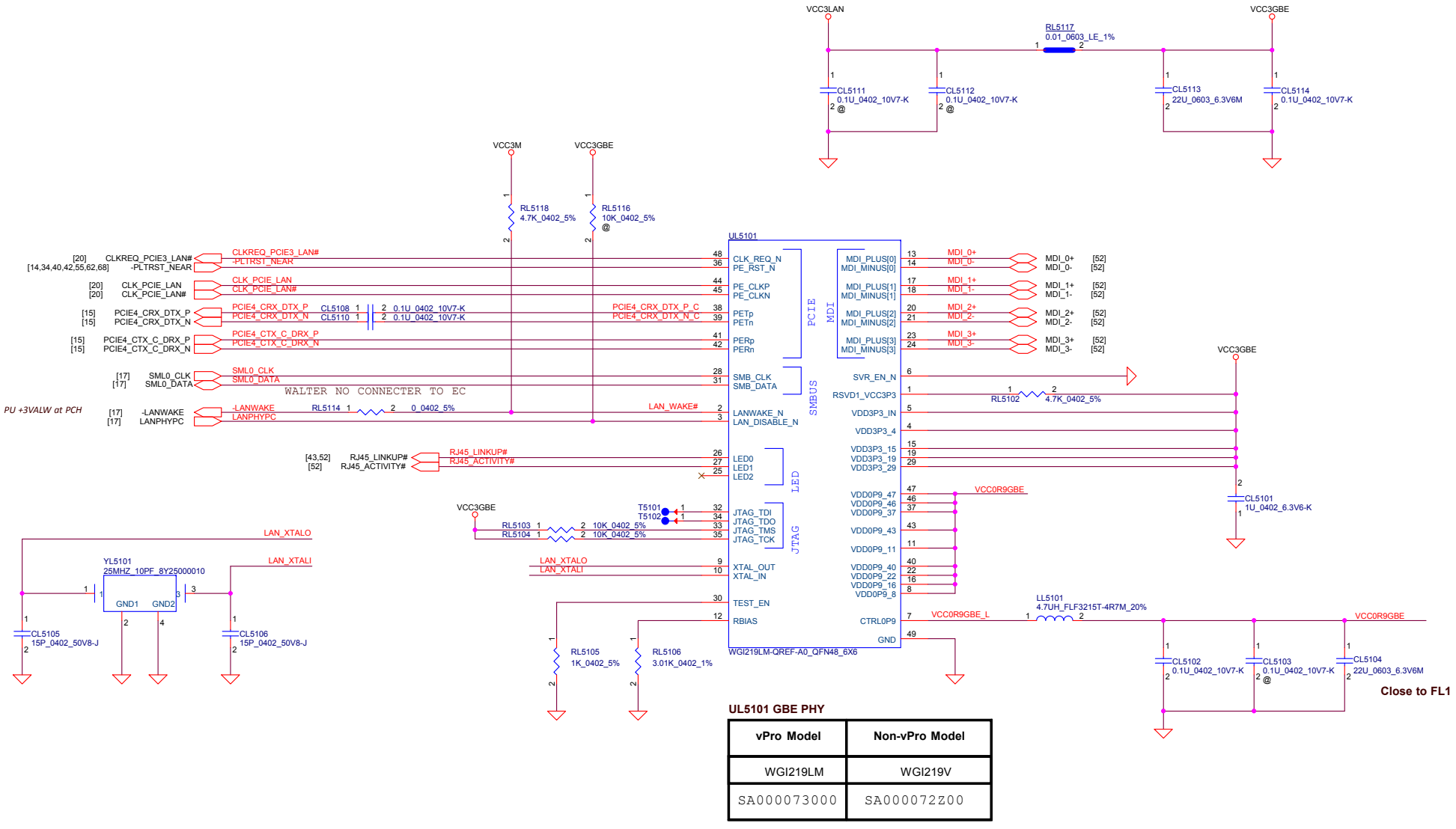
PLACE, NEAR SPEAKER CONNECTOR

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO SPEAKER**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 50 of 99



UL5101 GBE PHY

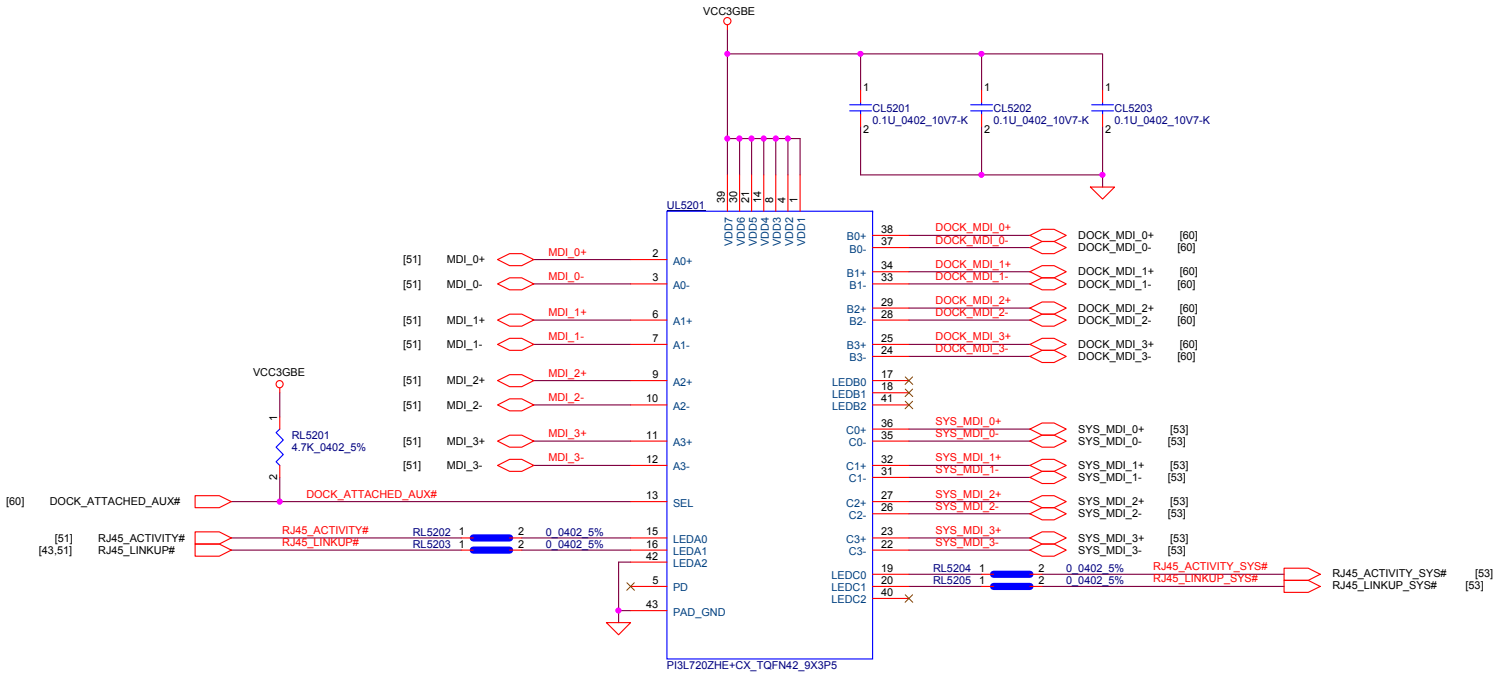
vPro Model	Non-vPro Model
WGI219LM	WGI219V
SA000073000	SA000072Z00

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **GBE LAN PHY**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 51 of 99



UL5201

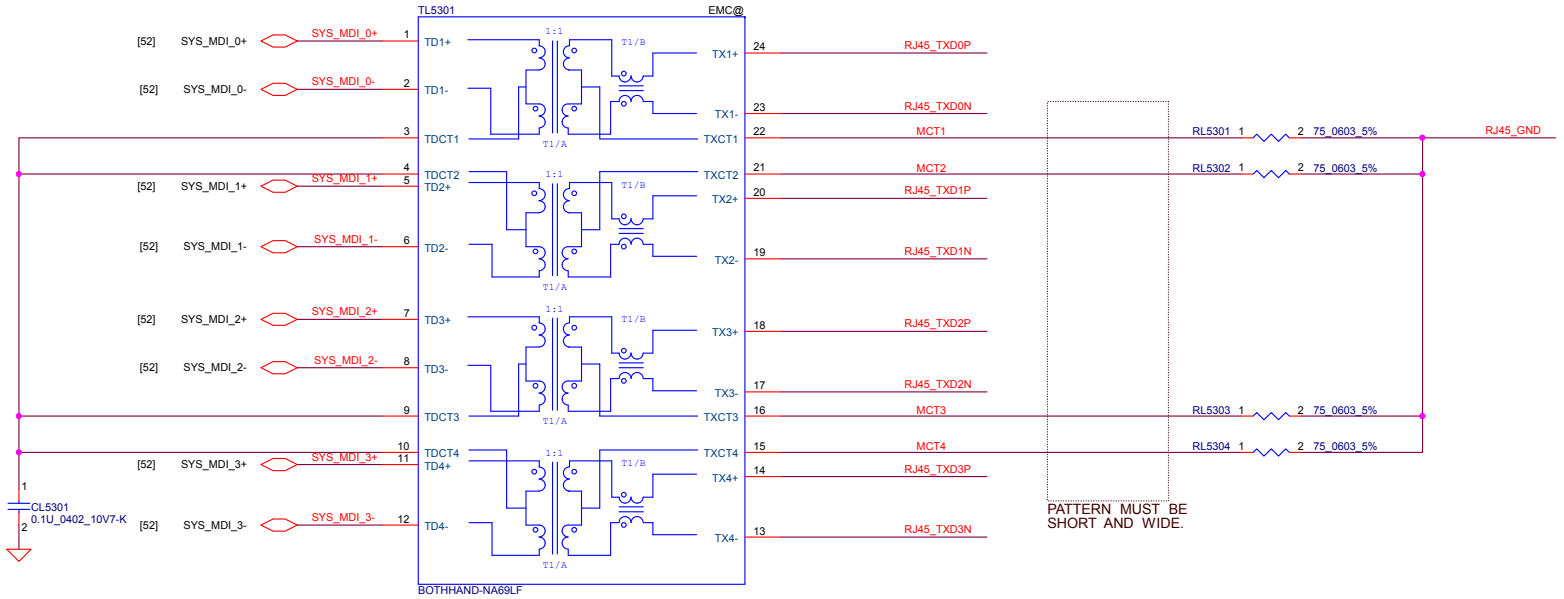
Vendor	P/N	NOTE
Pericom	PI3L720ZHE, SA00003B20J	Main Source
ONSemi	NCN7201 , SA00005TF00	2nd Source (FVT)

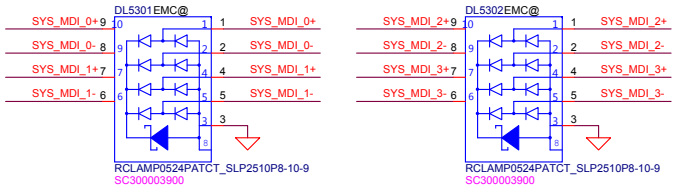
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: GBE LAN SWITCH

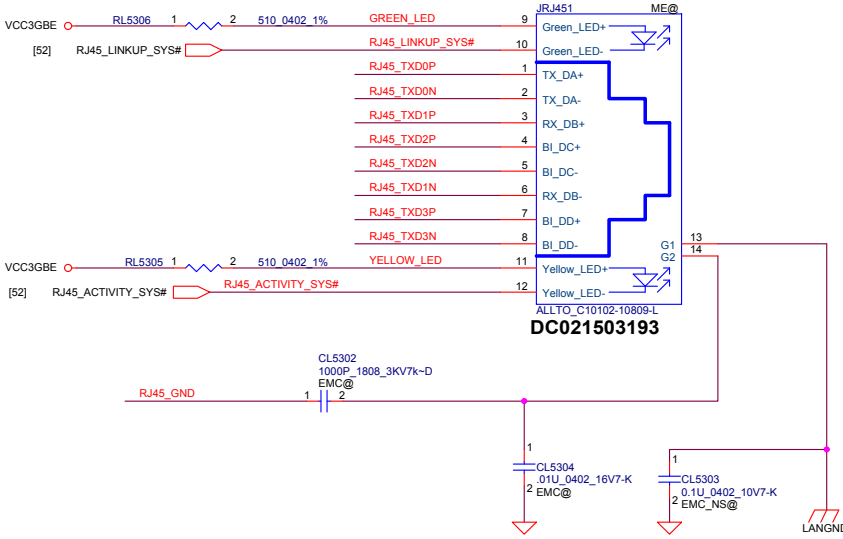
Size: Custom | Document Number: NM-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 52 of 99



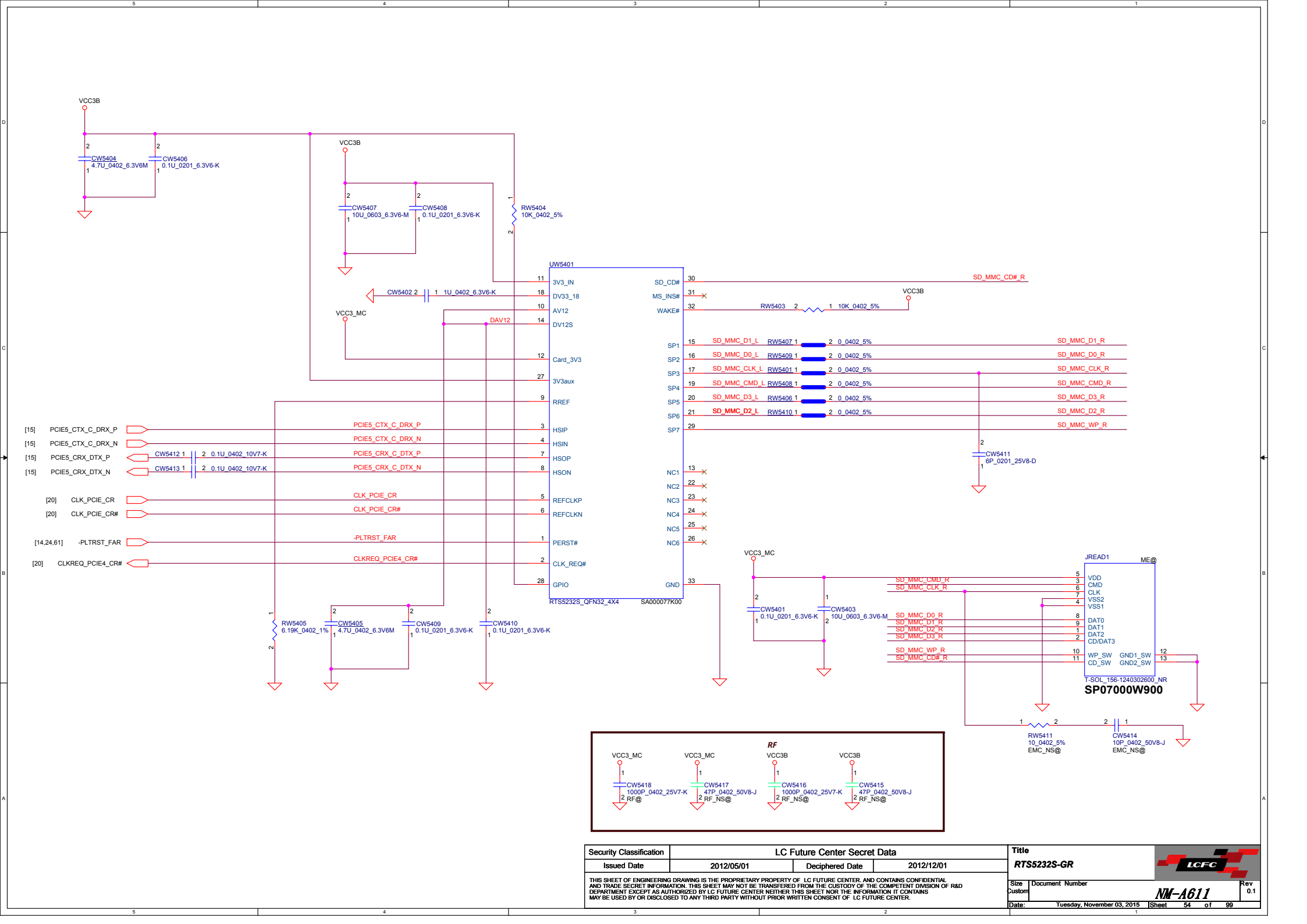


RJ-45 Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	RJ45 CONN.		
Size	Document Number		Rev
Custom	NM-A611		0.1
Date:	Tuesday, November 03, 2015	Sheet	53 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

Title: RTS5232S-GR

Size: Custom | Document Number: NM-A611 | Rev: 0.1

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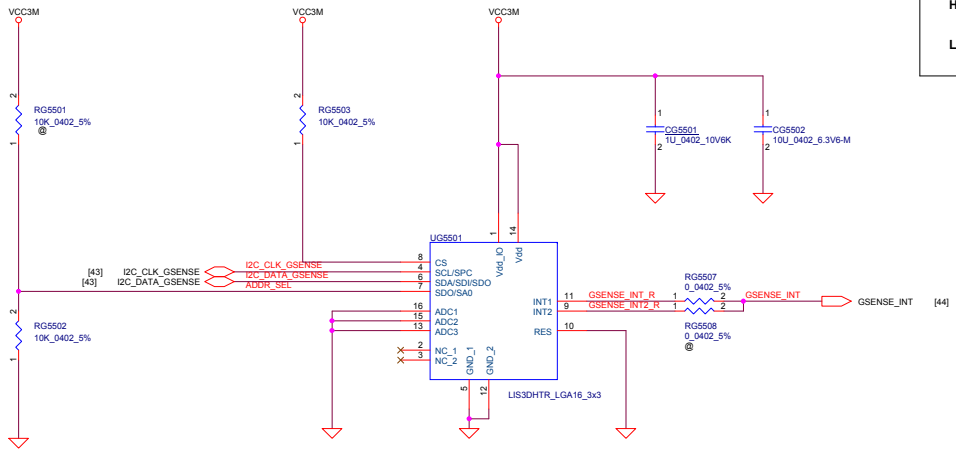
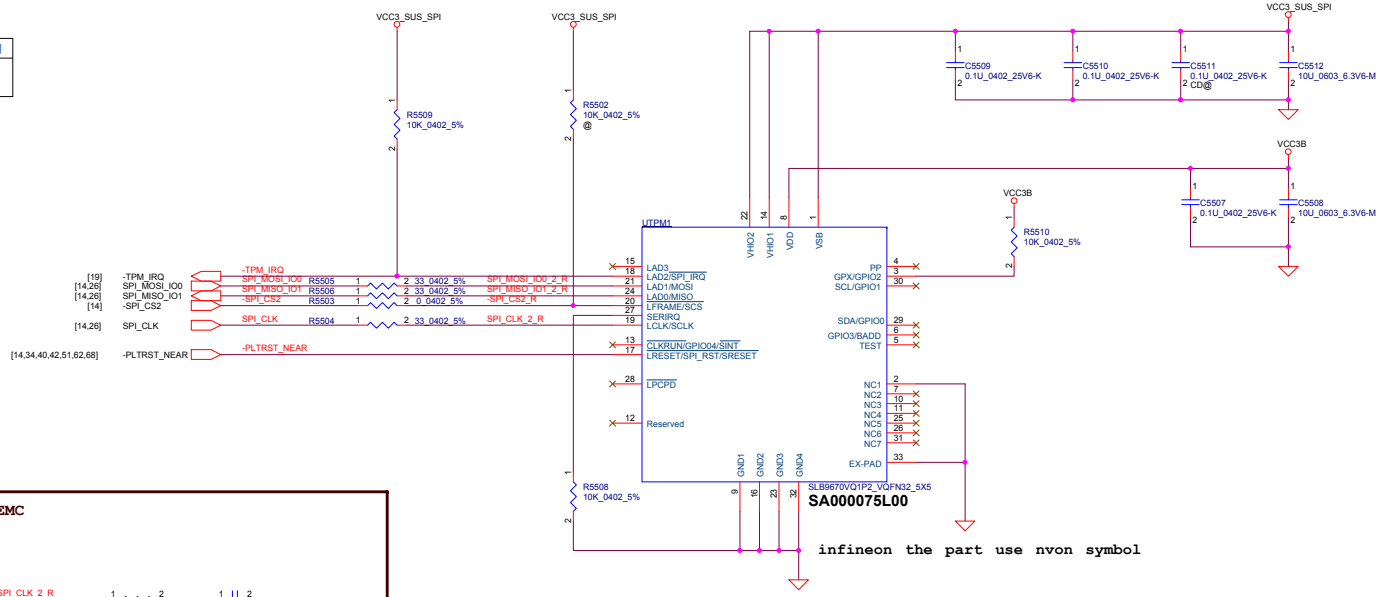
APS G-Sensor

TABLE	
CS	Mode Selection
H	I2C Mode
L	SPI Mode



TPM IC

TPM Pin8	+3VS	VCC3_SUS_SPI
S3~S5 current	120uA	330uA



infineon the part use nvon symbol

EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

Title			
G SENSOR/TPM			
Size: Custom	Document Number: NM-A611		Rev: 0.1
Date: Tuesday, November 03, 2015	Sheet 55 of 99		

eDP/CMOS/LOGO-LED CONN.

Rds(on)=32m ohm
Max current continue=257 mA

VCC3M
VCC3P
Q5601
TPCF8002_2-3U1A
R5608 47_0402_5%
R5609 100_0402_5%
D5602 RB521CS-30GT2RA_VMN2-2
[41] VCC3P_DRV
C5619 0.068U_0402_25V
R5610 47K_0402_5%

VINT20
C5627 0.01U_0402_25V7K
C5628 0.1U_0402_25
C5629 1UF_25V_0603

VCC3P
C5624 1U_0402_10V6K
C5625 0.1U_0402_25V6-K
C5626 .01U_0402_25V7-K

VINT20
2A, 80 mil
R5604 0.01_0603_LE_1%
R5613 0.01_0603_LE_1%
C5603 4.7U_0805_25V6-K

eDP TO BE CONFIRM

VCC3B
VCC3P
R5615 100K_0402_5%
R5611 10K_0402_5%

+LEDVDD W= 80 mil
VCC3B_DMIC W= 40 mil
VCC3B_CMOS
VCC3P W= 60 mil
VCC3M_LOGO

R5603 100K_0402_5%
R5605 0.01_0603_LE_1%
R5601 0.01_0603_LE_1%
R5606 1K_0402_5%

[42] -LEDLOGO
[42] BACKLIGHT_ON
[16] PANEL_BKLT_CTRL
R5617 0_0402_5%
R5618 0_0402_5%

[45] DMIC_DATA
[45] DMIC_CLK
R5619 EMC@ 33_0402_5%
R5612 EMC@ 33_0402_5%

[15] USB20_N7
[15] USB20_P7
L5601 EMC@ EXC24CH900U_4P SM070003X00
USB20_N7_CMOS
USB20_P7_CMOS

[6] CPU_EDP_AUX#
[6] CPU_EDP_AUX
[18] CPU_EDP_HPD
C5604 0.1U_0402_10V7-K
C5605 0.1U_0402_10V7-K
CPU_EDP_AUX#_CON
CPU_EDP_AUX_CON

[6] CPU_EDP_TX0-
[6] CPU_EDP_TX0+
C5608 0.1U_0402_10V7-K
C5609 0.1U_0402_10V7-K
CPU_EDP_TX0-_CON
CPU_EDP_TX0+_CON

[6] CPU_EDP_TX1-
[6] CPU_EDP_TX1+
C5606 0.1U_0402_10V7-K
C5607 0.1U_0402_10V7-K
CPU_EDP_TX1-_CON
CPU_EDP_TX1+_CON

[6] CPU_EDP_TX2-
[6] CPU_EDP_TX2+
C5621 0.1U_0402_10V7-K
C5620 0.1U_0402_10V7-K
CPU_EDP_TX2-_CON
CPU_EDP_TX2+_CON

[6] CPU_EDP_TX3-
[6] CPU_EDP_TX3+
C5623 0.1U_0402_10V7-K
C5622 0.1U_0402_10V7-K
CPU_EDP_TX3-_CON
CPU_EDP_TX3+_CON

[15] USB20_N9_TP
[15] USB20_P9_TP
L5602 EMC@ EXC24CH900U_4P SM070003X00
USB20_N9_TP_R
USB20_P9_TP_R

[18] TS_EN
[43,47] -LID_CLOSE
D5603 DAP222MGT2L_VMD3

VCC3B
VCC3P
R5614 1 2 0.01_0603_LE_1%
R5616 1 @ 2 0.01_0603_LE_1%
VCC3B_TS

JEDP1 ME@
I-PEX_20525-040E-01
SP011408042

C5633 22P_0402_50V8-J 2 EMC@
C5632 1000P_0402_25V7-K 2 EMC_NS@
C5630 1000P_0402_25V7-K 2 @
D5601 PESD5V0U2BT_SOT23-3 EMC@
C5631 22P_0402_50V8-J 2 EMC@

RF
+LEDVDD
C5610 100P_0402_50V8J 2 RF@
C5611 47P_0402_50V8-J 2 RF_NS@
VCC3B_CMOS
C5612 100P_0402_50V8J 2 RF@
C5613 47P_0402_50V8-J 2 RF_NS@

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: eDP/CMOS/LOGO-LED CONN.
Size: Custom
Document Number: NM-A611
Rev: 0.1
Date: Tuesday, November 03, 2015
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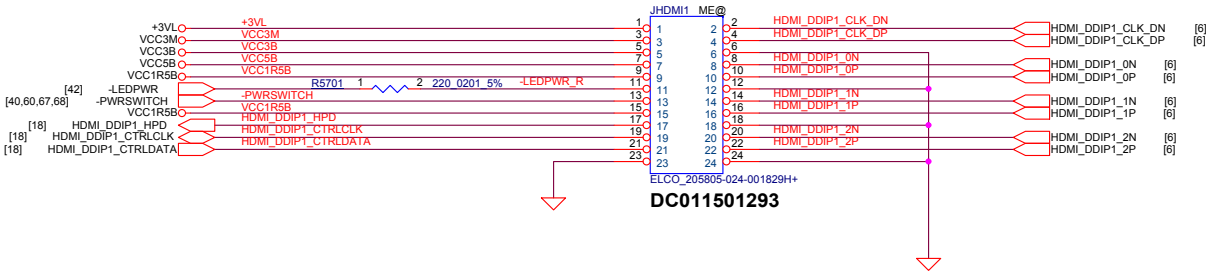
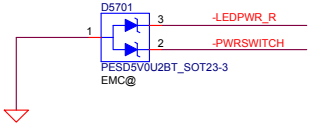
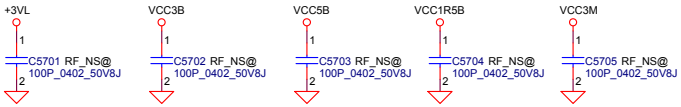
M/B TO HDMI/B BTB CONN.





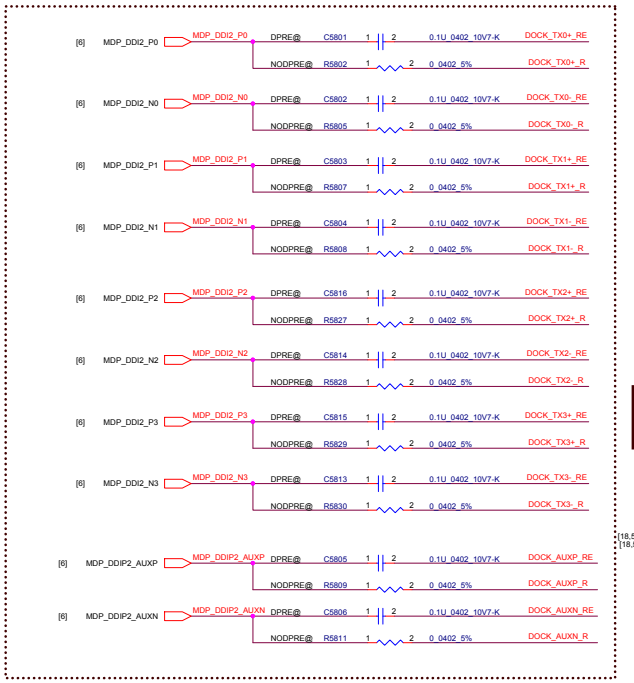


Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

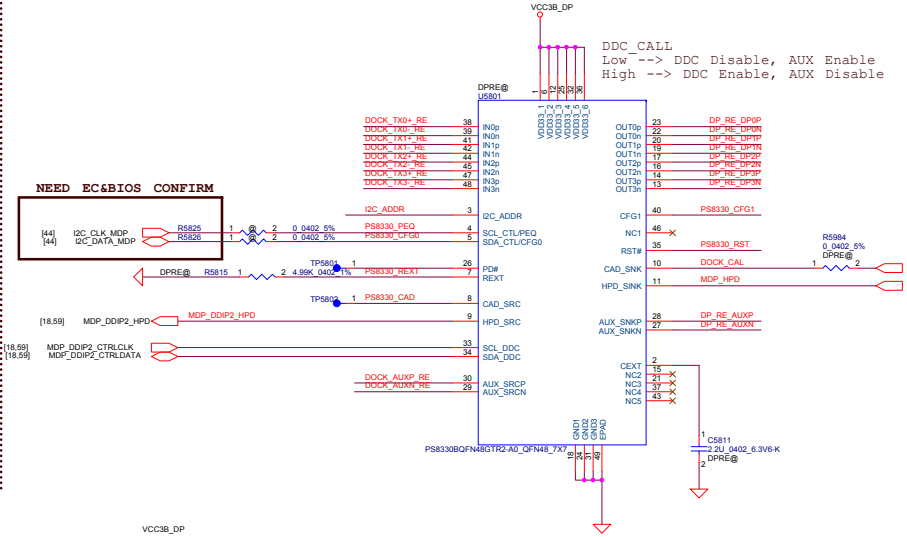
Title: HDMI BTB CONN.

Size	Document Number	Rev
Custom	NM-A611	0.1

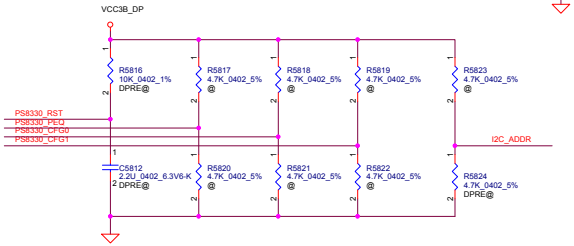
Date: Tuesday, November 03, 2015 Sheet 57 of 99

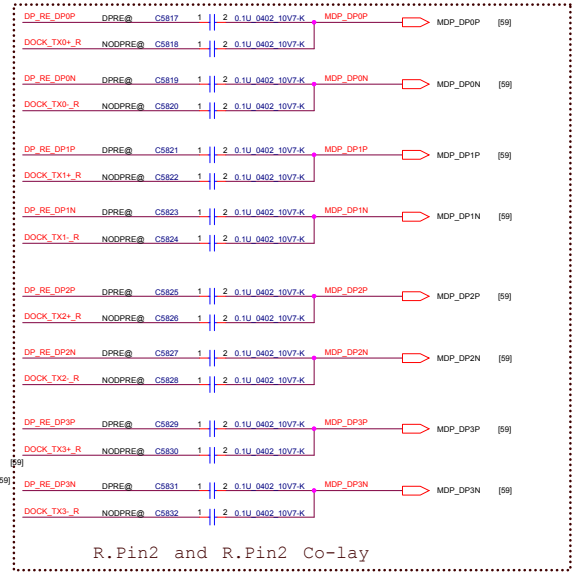


Cap.Pin1 and R.Pin1 Co-lay

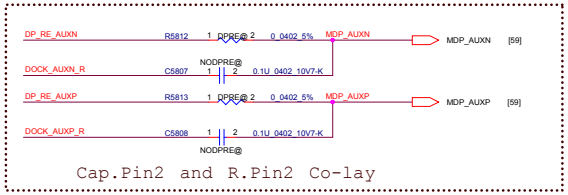


NEED EC&BIOS CONFIRM





R.Pin2 and R.Pin2 Co-lay



Cap.Pin2 and R.Pin2 Co-lay

DP AUX : From Repeator don't need cap, but PCH.

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: PS8330B REPEATER

Size	Document Number	Rev
Custom	NM-A611	0.1

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[58] MDP_DP0N
[58] MDP_DP0P
MDP_DP0N
MDP_DP0P

[58] MDP_DP1N
[58] MDP_DP1P
MDP_DP1N
MDP_DP1P

[58] MDP_DP2N
[58] MDP_DP2P
MDP_DP2N
MDP_DP2P

[58] MDP_DP3N
[58] MDP_DP3P
MDP_DP3N
MDP_DP3P

[58] DVI_DONGLE
[58] MDP_HPD
DVI_DONGLE
MDP_HPD

[58] MDP_AUXP
[58] MDP_AUXN
MDP_AUXP
MDP_AUXN

R5922 1 2 DPRE@ 0_0201_5% MDP_DDIP2_HPD_R
R5925 1 2 DPRE@ 0_0201_5% DP_AUXP_CONN_R
R5926 1 2 DPRE@ 0_0201_5% DP_AUXN_CONN_R
R5930 1 2 NODPRE@ 0_0201_5% MDP_AUXP_L
R5931 1 2 NODPRE@ 0_0201_5% MDP_AUXN_L

PIN1 COLAY

VCC5B

C5920 0.1U_0201_25V6-K 2 NODPRE@

U5902 NODPRE@
CBT3257ABQ_DHVQFN16_2P5X3P5

Vcc	16	
1B1	2	MDP_AUXP_L
1B2	3	MDP_AUXN_L
2B1	5	
2B2	6	
3B1	11	
3B2	10	
4B1	14	
4B2	13	
1A	4	MDP_AUXP_R
2A	7	MDP_AUXN_R
3A	9	MDP_DDIP2_HPD_R
4A	12	
OE	15	
S	1	DVI_DONGLE
GND	8	
T-PAD	17	

PIN2 COLAY

DP_AUXP_CONN_R
DP_AUXN_CONN_R
R5934 1 2 DPRE@ 0_0201_5%
R5935 1 2 DPRE@ 0_0201_5%
MDP_AUXP_R
MDP_AUXN_R
R5932 1 2 NODPRE@ 0_0201_5%
R5933 1 2 NODPRE@ 0_0201_5%
DP_AUXP_CONN
DP_AUXN_CONN

[18,58] MDP_DDIP2_CTRLCLK
[18,58] MDP_DDIP2_CTRLDATA

[18,58] MDP_DDIP2_HPD
MDP_DDIP2_HPD
Q5901 2N7002WT1G_SC-70-3 @ SB00000YY00
R5927 100K_0402_5% @
MDP_DDIP2_HPD_L
R5923 1 2 NODPRE@ 0_0201_5%

OE	S	Result
L	L	nA1 to nB1.
L	H	nA1 to nB2.
H	X	Swtich off.

SA00005V10J

JMDP1 ME@
ALLTO_C17727-120A9-L

MDP_DDIP2_HPD_R	2	HOT_PLUG	
DP_AUXP_CONN	16	AUX_CH_P	
DP_AUXN_CONN	18	AUX_CH_N	
MDP_DP3P	10	LANE3_P	
MDP_DP3N	12	LANE3_N	
MDP_DP2P	15	LANE2_P	
MDP_DP2N	17	LANE2_N	
MDP_DP1P	9	LANE1_P	
MDP_DP1N	11	LANE1_N	
MDP_DP0P	3	LANE0_P	
MDP_DP0N	5	LANE0_N	
		DP_PWR	20
		GND6	19
		GND5	14
		CONFIG2	6
		CONFIG1	4
		GND4	13
		GND3	8
		GND2	7
		GND1	1
		GND7	21
		GND8	22
		GND9	23
		GND10	24

DC021503181

VCC3B_MINIDP
C5916 0.1U_0402_10V7-K
R5905 5.1M_0402_5%
DVI_DONGLE
C5917 0.1U_0402_25V6-K EMC@
R5906 1M_0402_5%
VCC3B
RF_NS@ C5919 100P_0402_50V8J
VCC5B
RF_NS@ C5918 100P_0402_50V8J

VCC3B
R5904 1 2 100K_0402_5% DP_AUXN_CONN
R5903 1 2 100K_0402_5% DP_AUXP_CONN

EMC (ESD solut i on)

D5901 EMC@
MDP_DP0N 1 10 9 MDP_DP0N
MDP_DP0P 2 9 8 MDP_DP0P
MDP_DP3P 4 7 7 MDP_DP3P
MDP_DP3N 5 6 6 MDP_DP3N
3 8
RCLAMP0524PATCT_SLP2510P8-10-9
SC300003900

D5902 EMC@
MDP_DP2N 1 10 9 MDP_DP2N
MDP_DP2P 2 9 8 MDP_DP2P
MDP_DP1N 4 7 7 MDP_DP1N
MDP_DP1P 5 6 6 MDP_DP1P
3 8
RCLAMP0524PATCT_SLP2510P8-10-9
SC300003900

D5903 EMC@
DP_AUXN_CONN 1 10 9 DP_AUXN_CONN
DP_AUXP_CONN 2 9 8 DP_AUXP_CONN
MDP_DDIP2_HPD_R 4 7 7 MDP_DDIP2_HPD_R
5 6 6
3 8
RCLAMP0524PATCT_SLP2510P8-10-9
SC300003900

NEAR DP CONN

VCC3B
VCC3B_MINIDP

Rds(on)=110m ohm
Max current continue=500 mA

U5901
G5250M1T1U_SOT23-5
SA000078Z00
IN 5
OUT 1
GND 2
EN 4
OC# 3

C5912 10U_0603_6.3V6-M
C5913 0.1U_0402_25V6-K EMC@
C5914 10U_0603_6.3V6-M
C5915 4.7U_0603_10V6-K
R5911 0.01_0603_LE_1%

Typ. 500mA, Max 1.5A

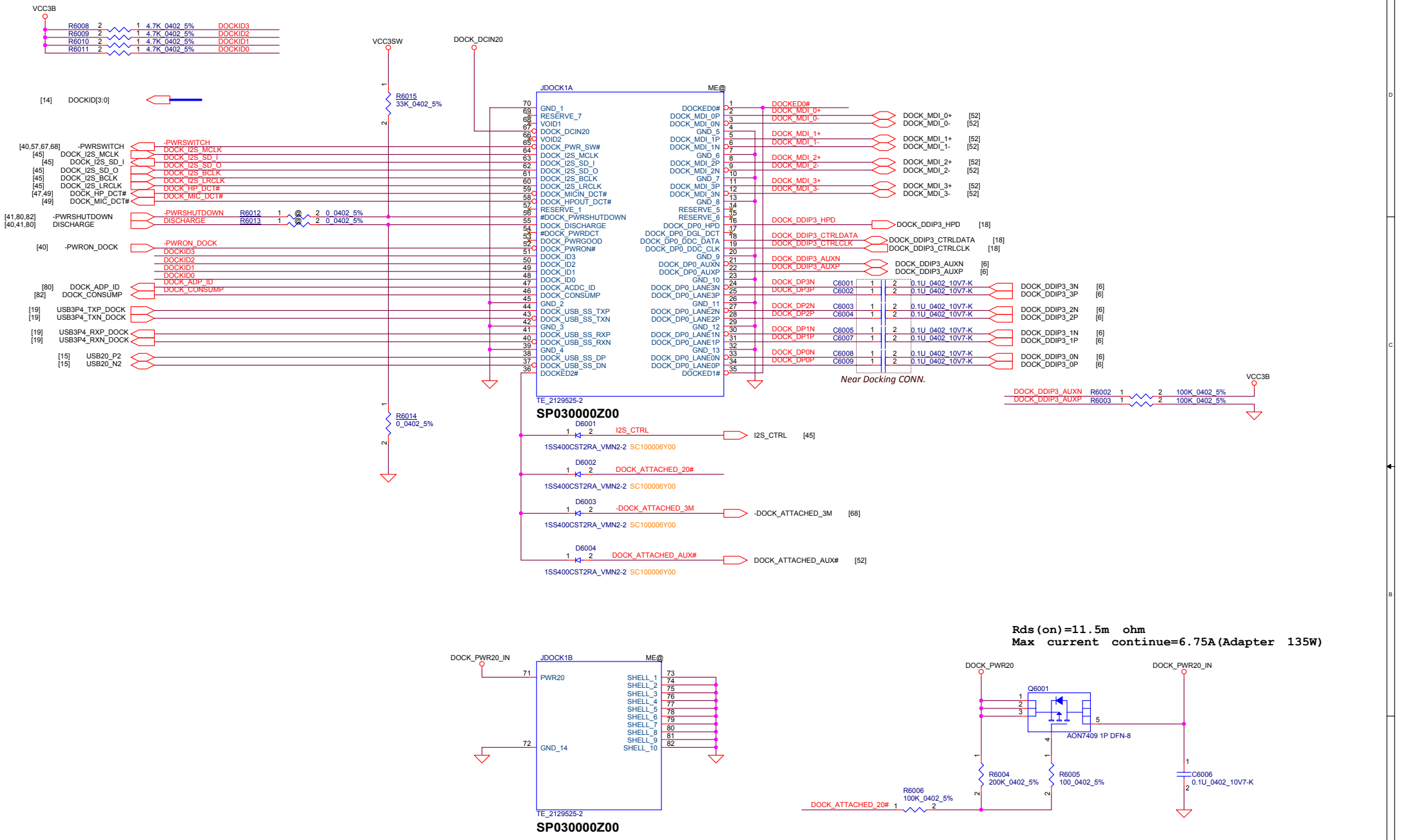
NEAR DP CONN

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: *MINI-DP/CONN.*

Size: Custom | Document Number: NM-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 59 of 99



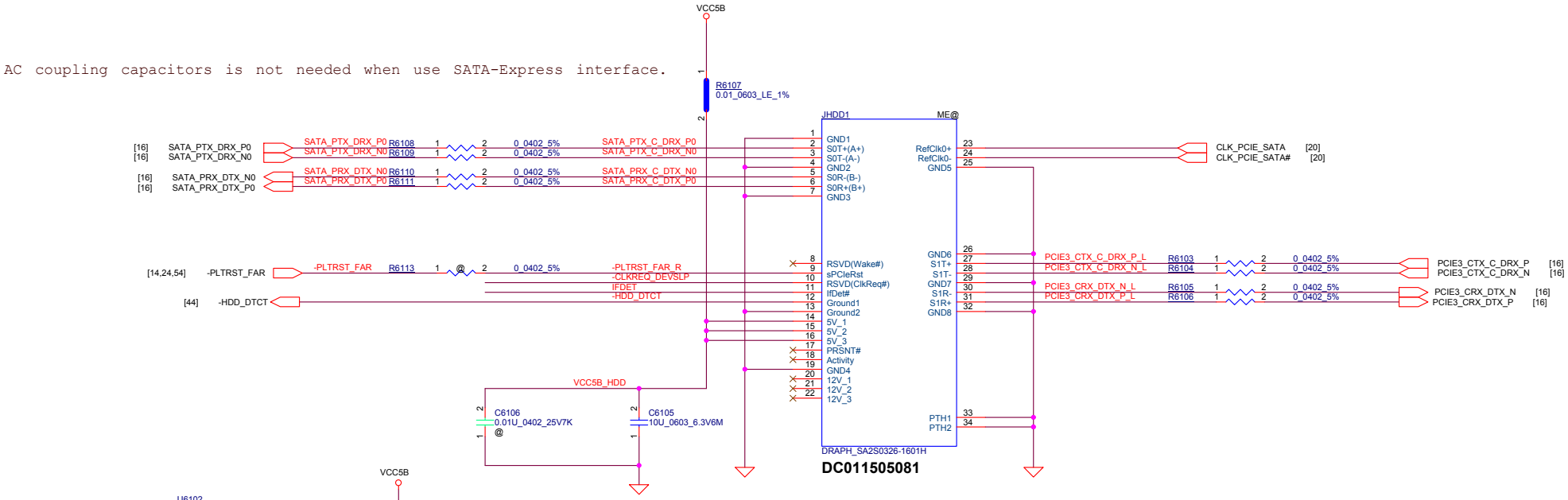
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

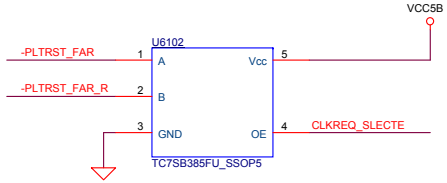
Title: **DOCKING CONN.**

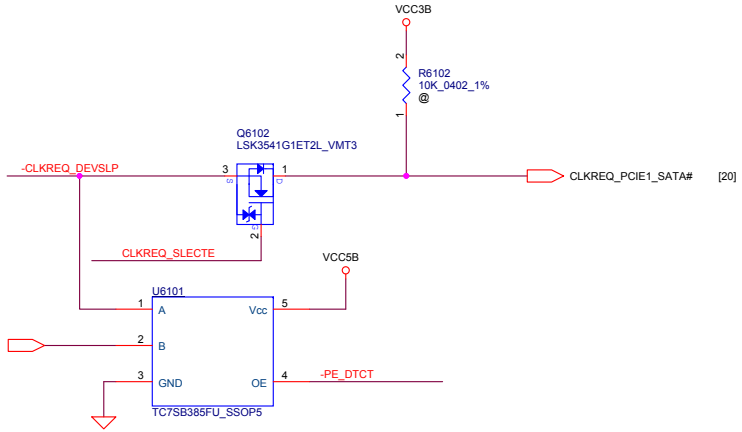
Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 60 of 99

AC coupling capacitors is not needed when use SATA-Express interface.

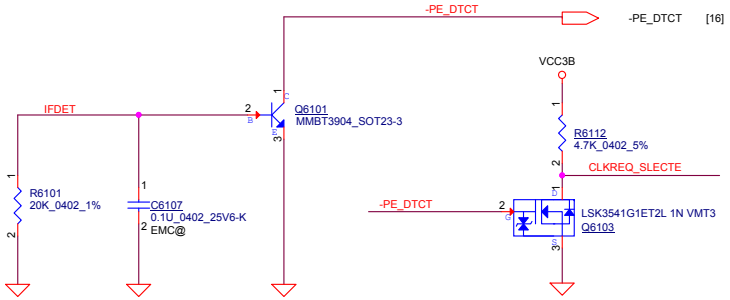






Input	Function
OE	
L	Disconnect
H	A port = B port

IFDET
SATA Device GND
PCIe Device 5K PU to Vsource



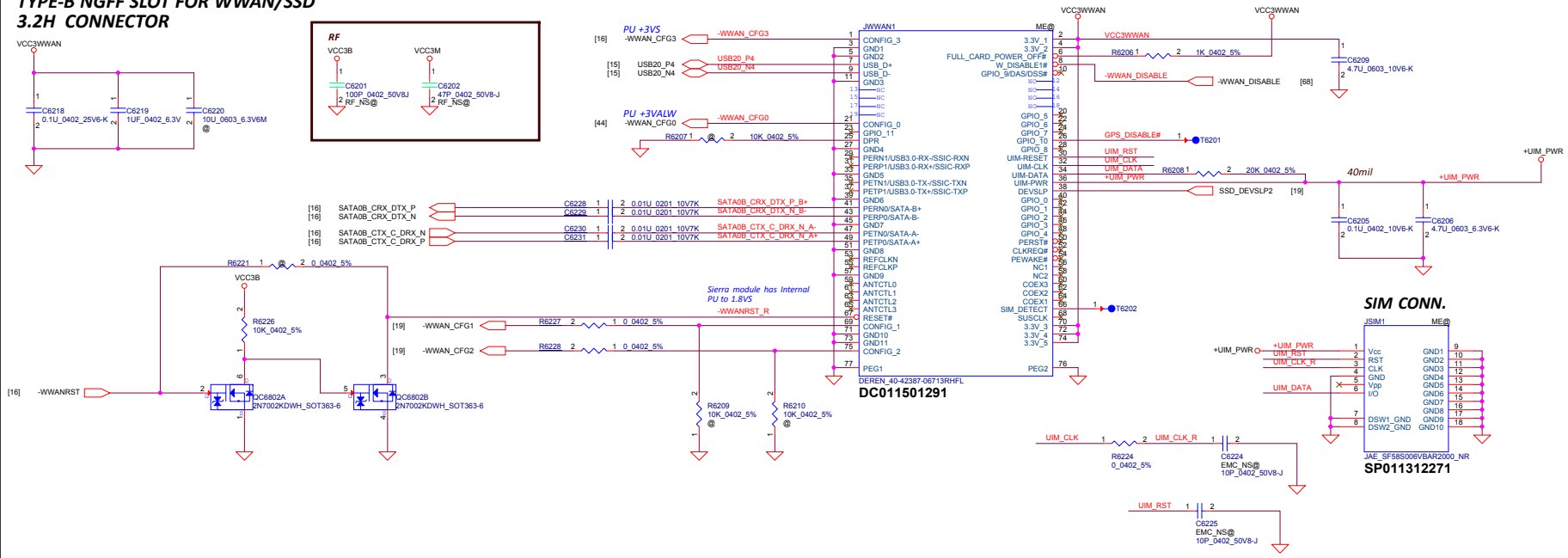
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: SATA HDD CONN.

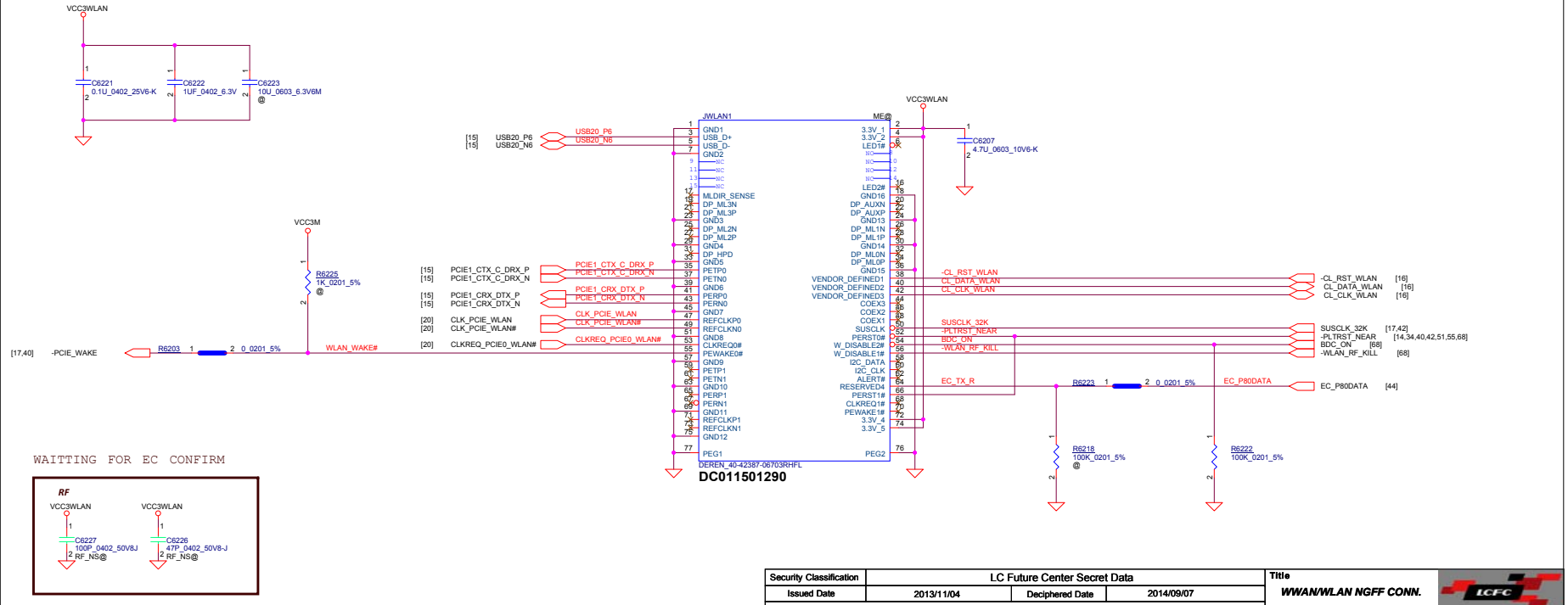
Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 61 of 99

TYPE-B NGFF SLOT FOR WWAN/SSD
3.2H CONNECTOR



TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



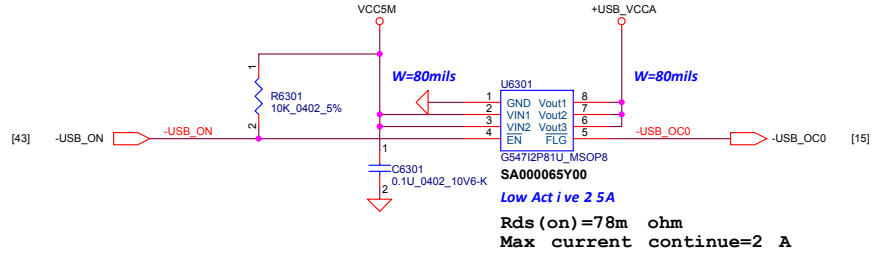
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: WWAN/WLAN NGFF CONN.

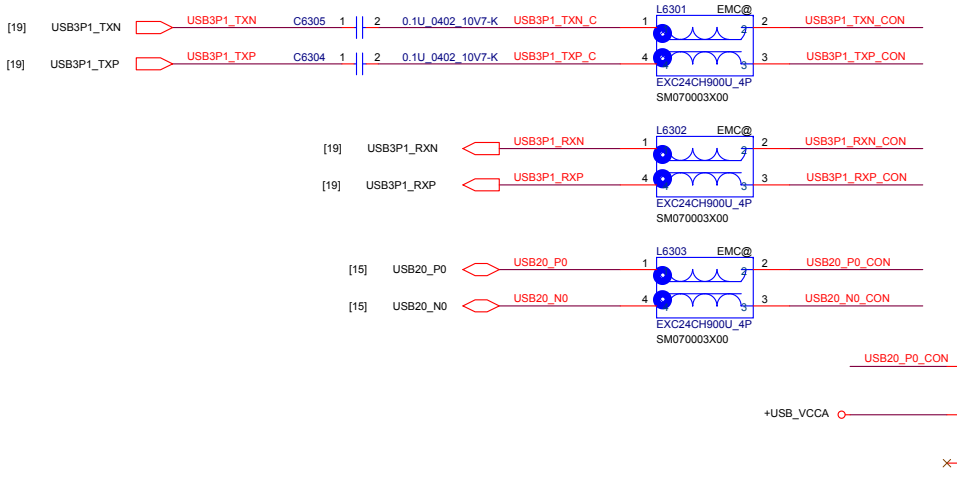
Size: Custom | Document Number: NM-A611 | Rev: 0.1

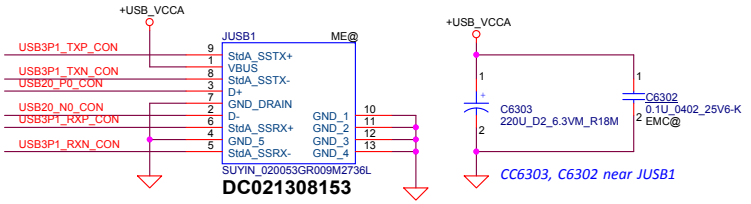
Date: Tuesday, November 03, 2015 | Sheet 62 of 99

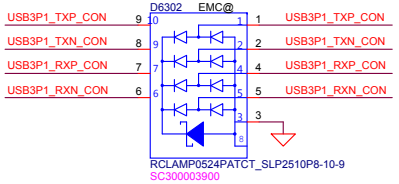
USB POWER SWITCH



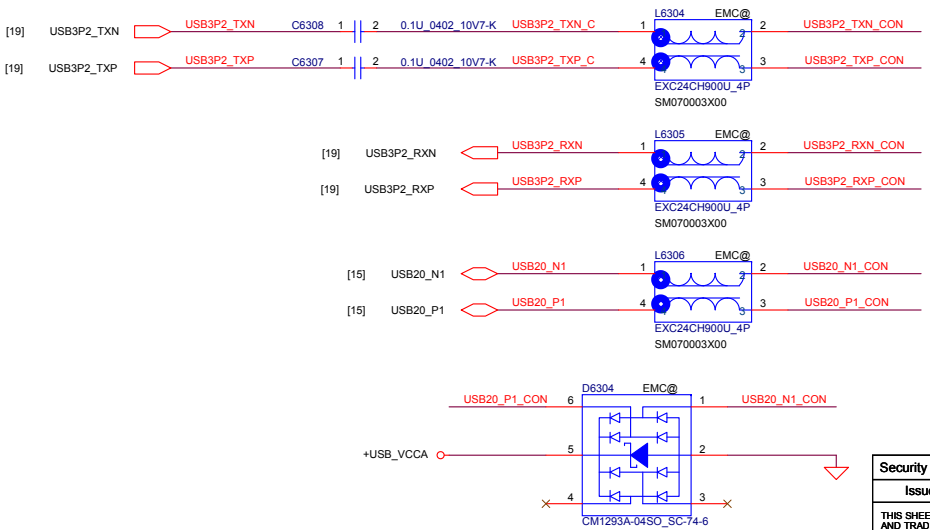
On Board (Right-Front)

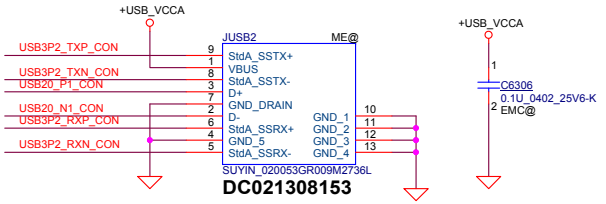


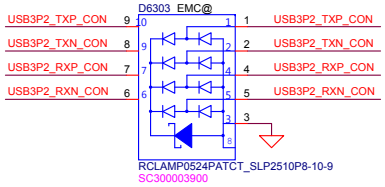




On Board (Right-Back)







Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: **USB3 P1/2 CONN.**

Size	Document Number	Rev
Custom	NM-A611	0.1

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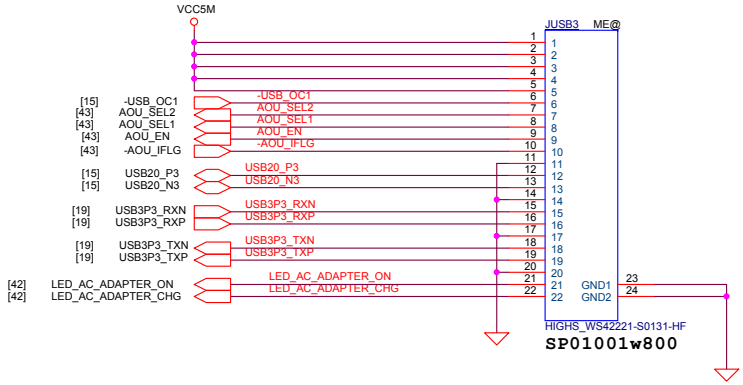
*

MB PIN number	MB PIN name	SB board pin name	SB PIN number
pin1~5	VCC5M	VCC5M	pin1~5
pin6	-USB_OC1	-USB_OC1	pin6
pin7	AOU_SEL2	AOU_SEL2	pin7
pin8	AOU_SEL1	AOU_SEL1	pin8
pin9	AOU_EN	AOU_EN	pin9
pin10	-AOU_IFLG	-AOU_IFLG	pin10
pin11	GND	GND	pin11
pin12	USB20_P3	USB20_P3	pin12
pin13	USB20_N3	USB20_N3	pin13
pin14	GND	GND	pin14
pin15	USB3P3_RXN	USB3P3_RXN	pin19
pin16	USB3P3_RXP	USB3P3_RXP	pin18
pin17	GND	GND	pin17
pin18	USB3P3_TXN	USB3P3_TXN	pin16
pin19	USB3P3_TXP	USB3P3_TXP	pin15
pin20	GND	GND	pin20
pin21	LED_AC_ADAPTER_ON	LED_AC_ADAPTER_ON	pin21
pin22	LED_AC_ADAPTER_CHG	LED_AC_ADAPTER_CHG	pin22

*

USB board and MB board is wire to board connector.
Due to USB board layout issue so pin define can* meet
MB

USB LEFT PORT

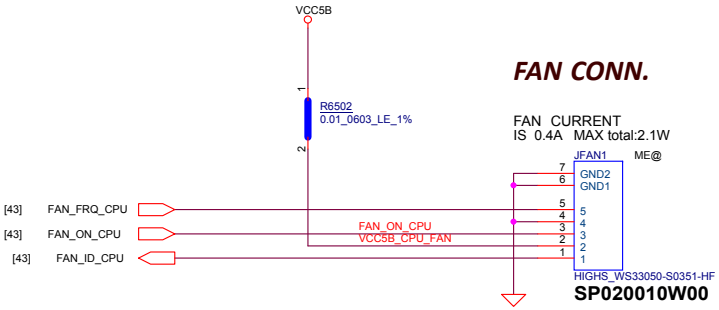


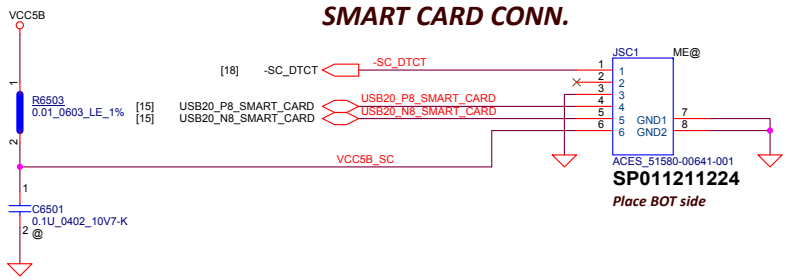
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: *USB3 P3 CONN.*

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 64 of 99



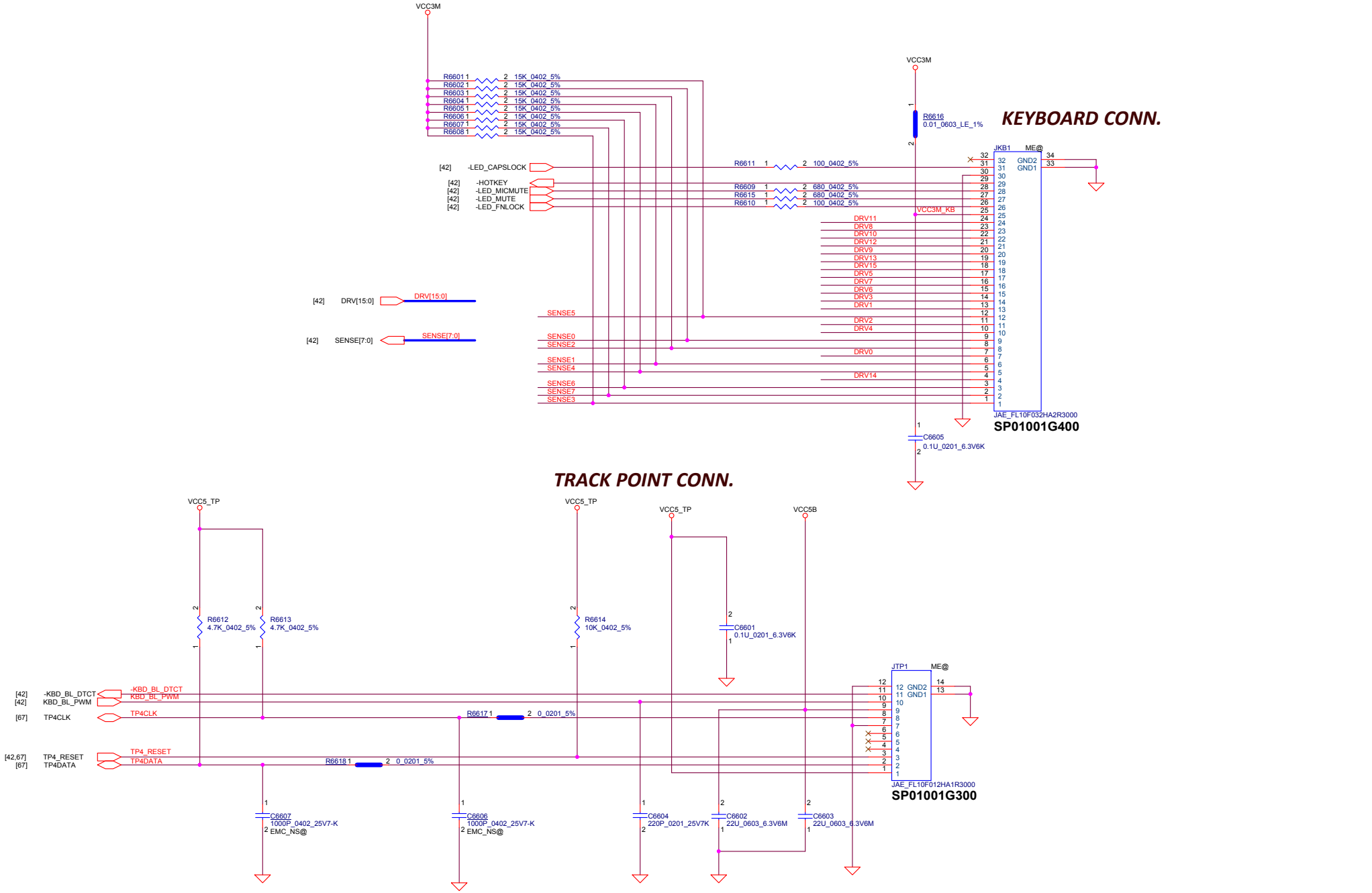


Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: FAN/SC CONN

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 65 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: KEYBOARD/TRACK POINT

Size	Document Number	Rev
Custom	NM-A611	0.1

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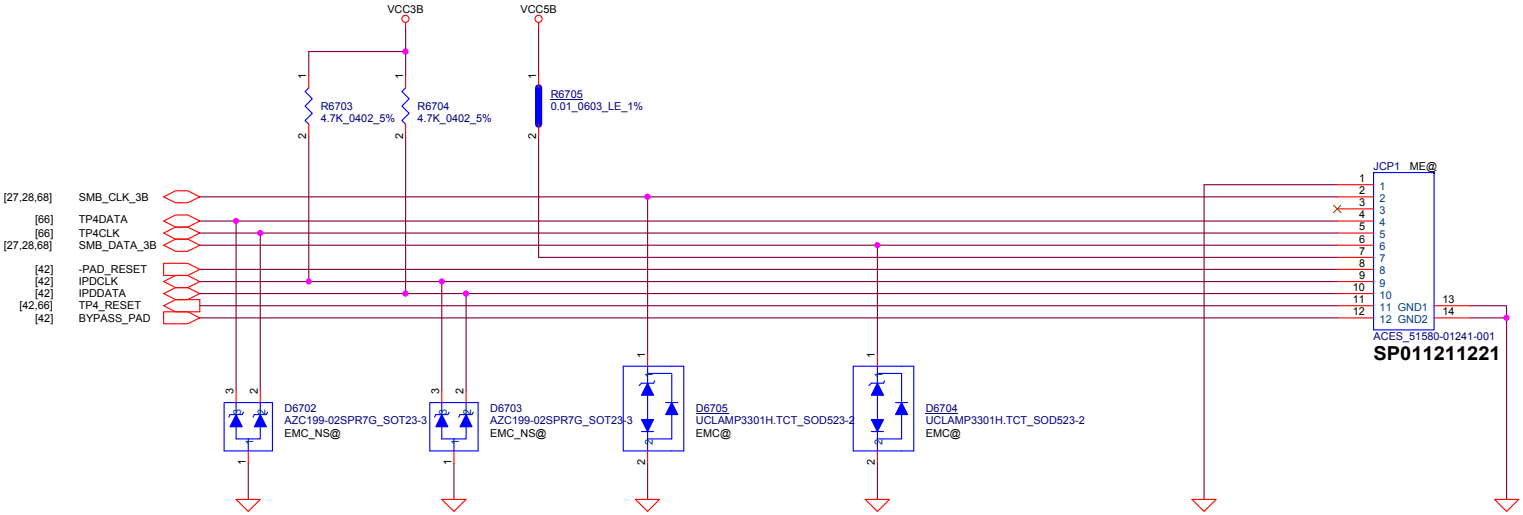
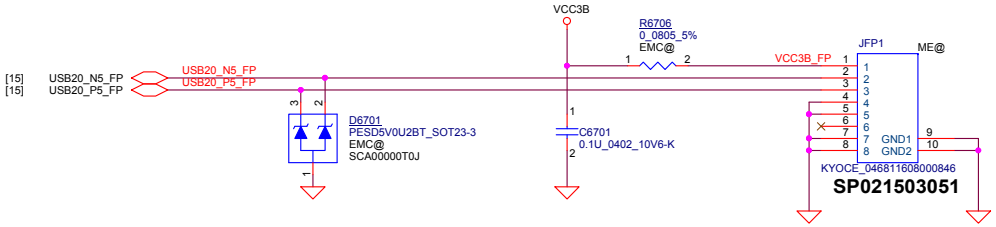
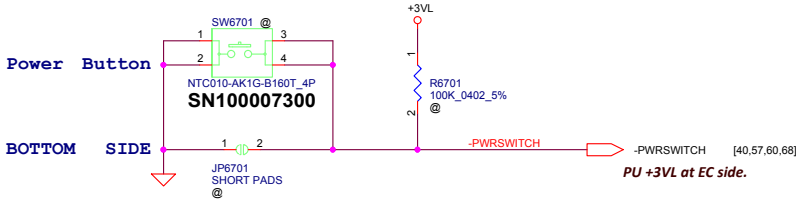
Click Pad



FingerPrint CONN.



PWRBTN FOR DEBUG



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: Click Pad/FPR/PBTN

Size	Document Number	Rev
Custom	NM-A611	0.1

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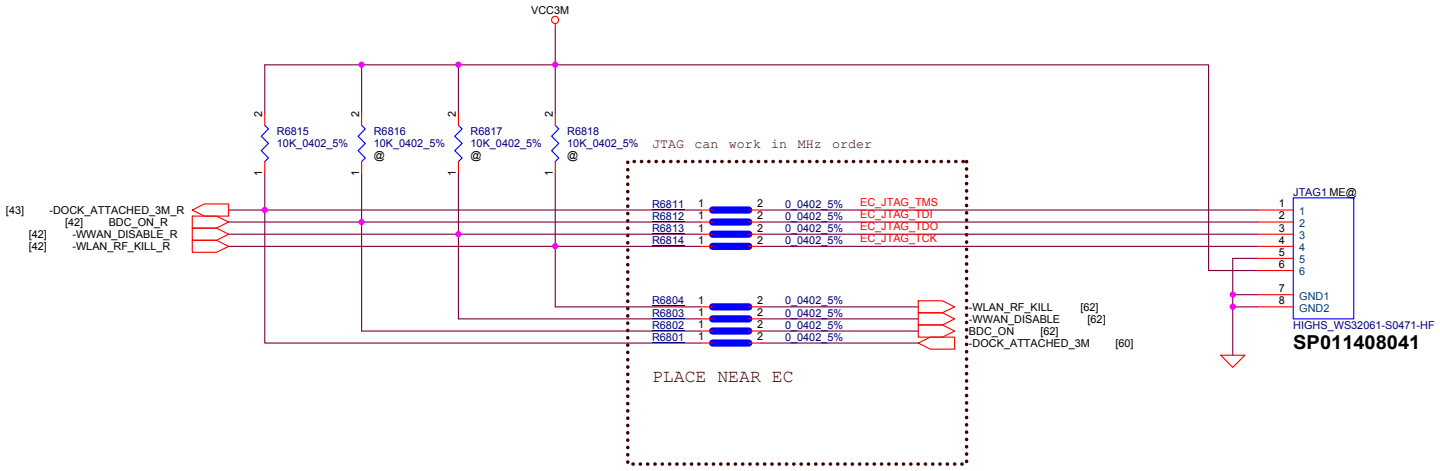
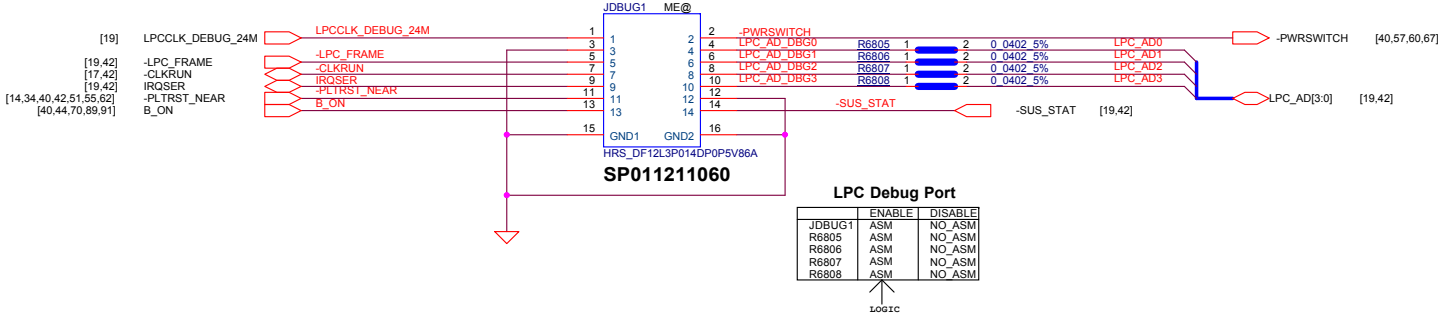
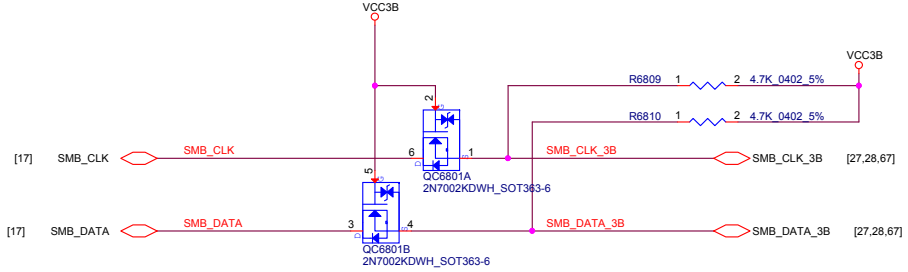




LPC Debug Port

	ENABLE	DISABLE
JDBUG1	ASM	NO_ASM
R6805	ASM	NO_ASM
R6806	ASM	NO_ASM
R6807	ASM	NO_ASM
R6808	ASM	NO_ASM

LOGIC



EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **SMBUS SWITCH/LPC DEBUG**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 68 of 99

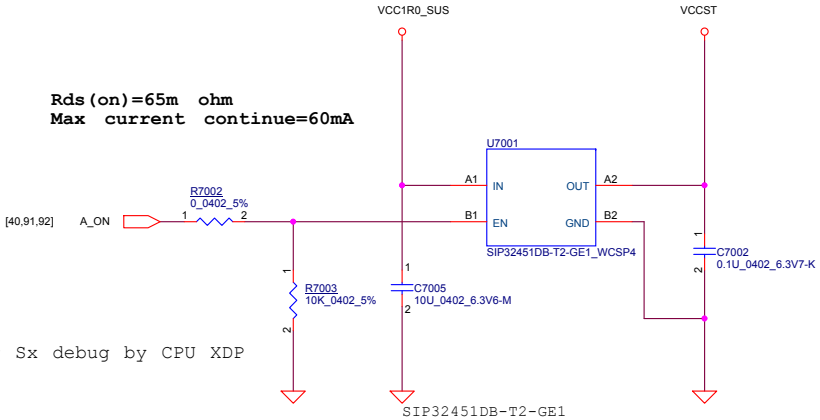
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/12/31

Title

EMC

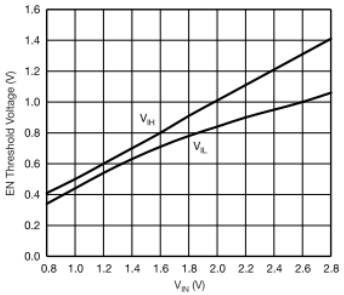
Size	Document Number	Rev
Custom	NM-A611	0.1

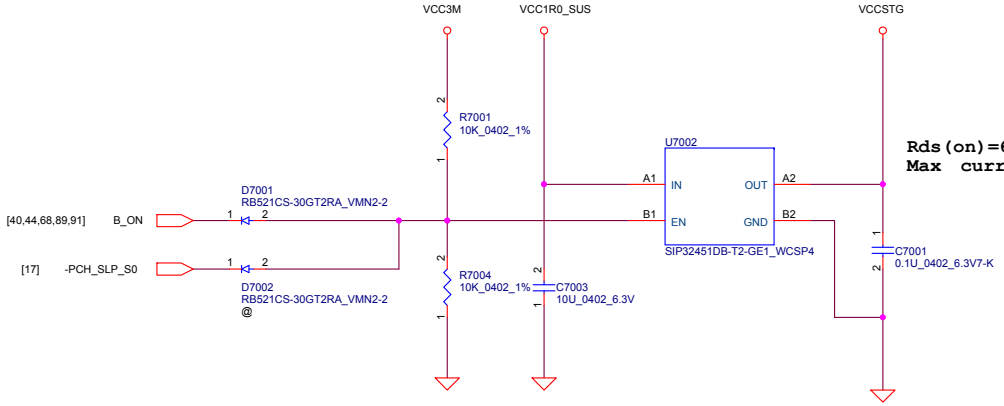
Date: Tuesday, November 03, 2015 Sheet 69 of 99



For Sx debug by CPU XDP

SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V





SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

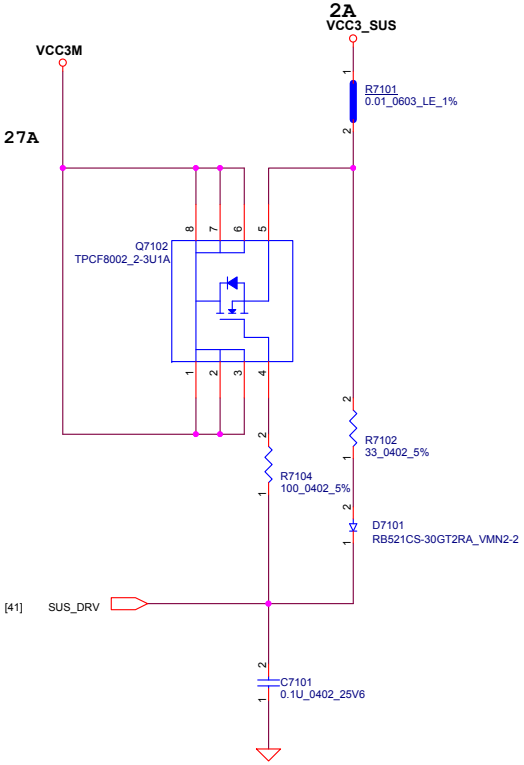
Title: LOAD SW VCCST/VCCSTG

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 70 of 99

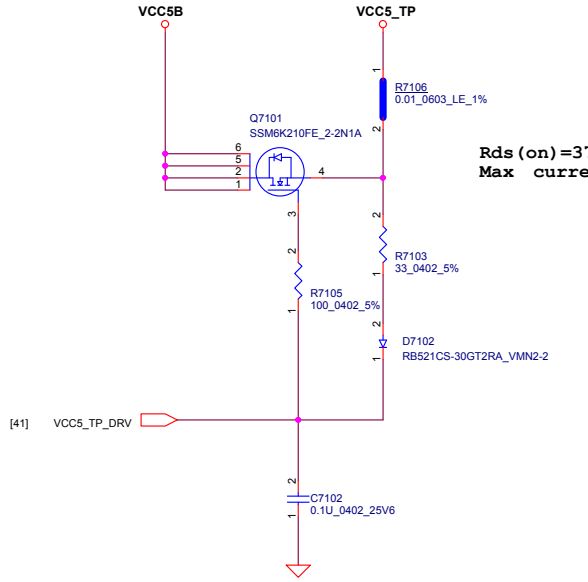
2A

Rds(on)=65m ohm
Max current continue=4.27A



15mA

Rds(on)=371m ohm
Max current continue=15mA

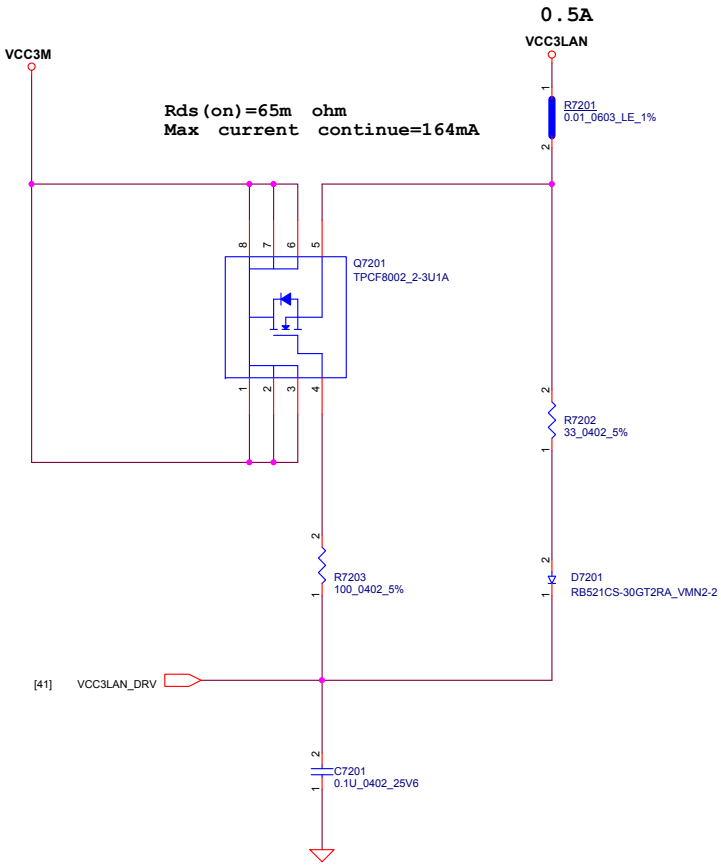


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW PCH SUS/TRACK POINT

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 71 of 99

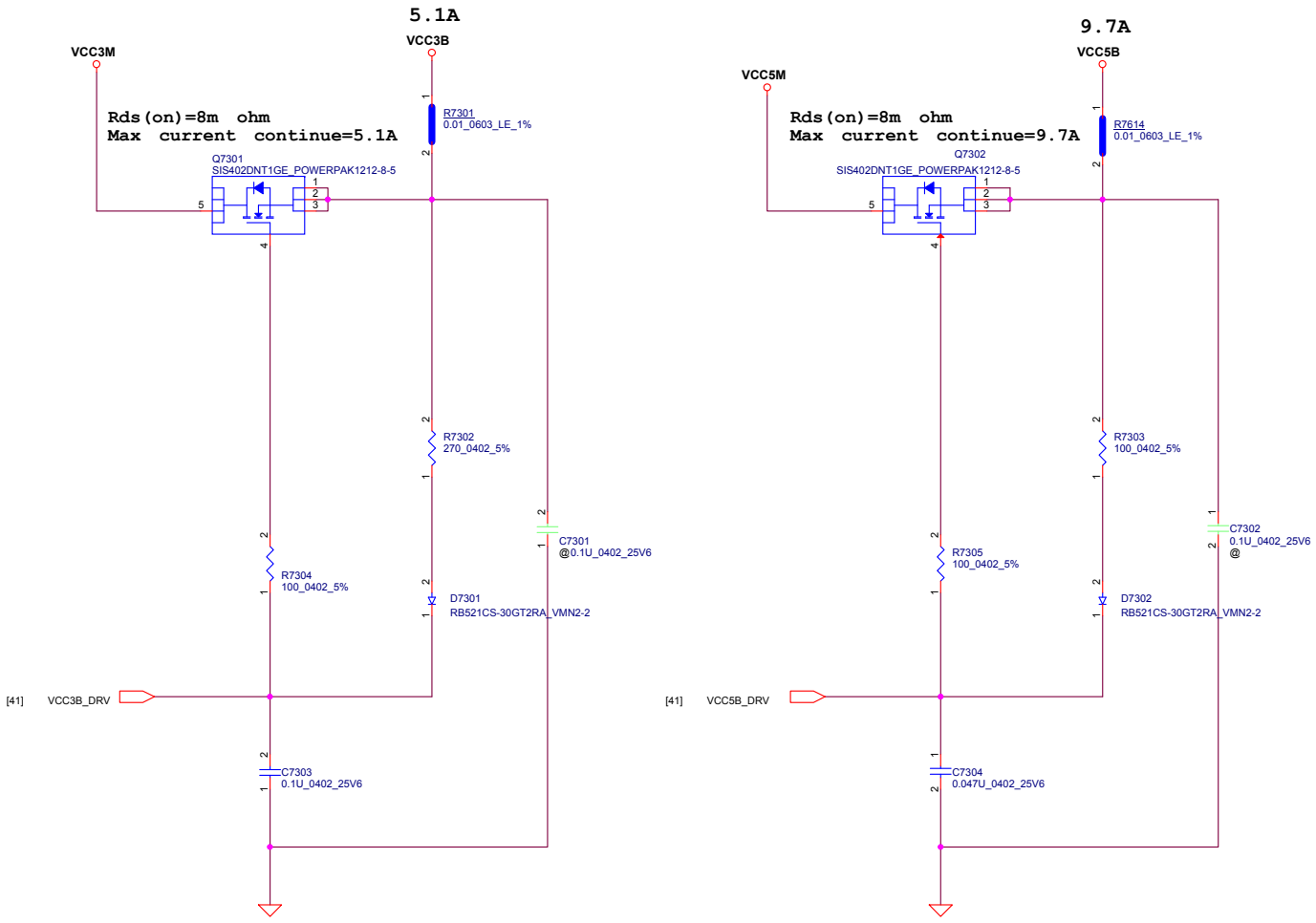


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW LAN

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 72 of 99

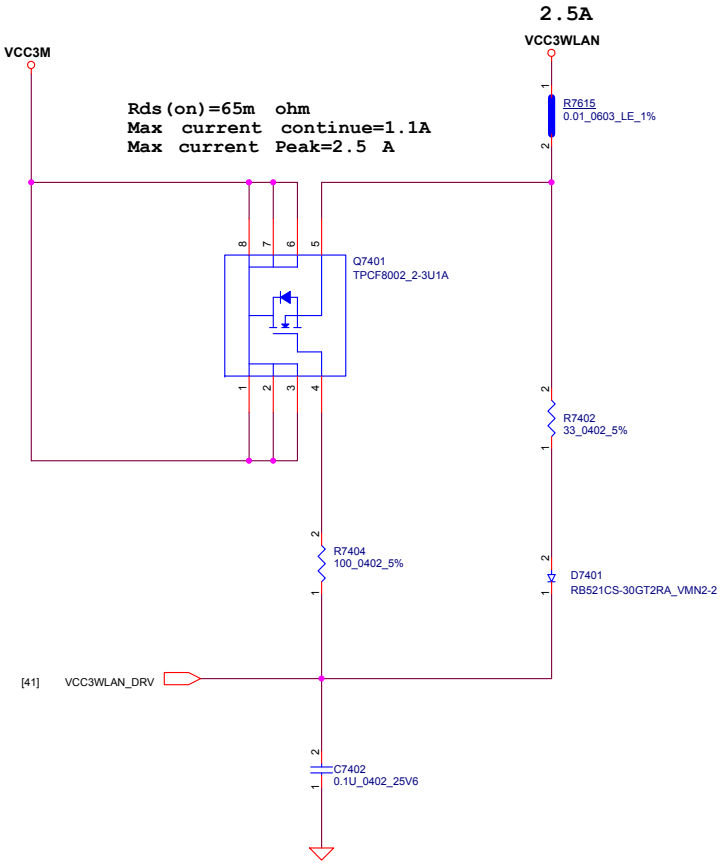


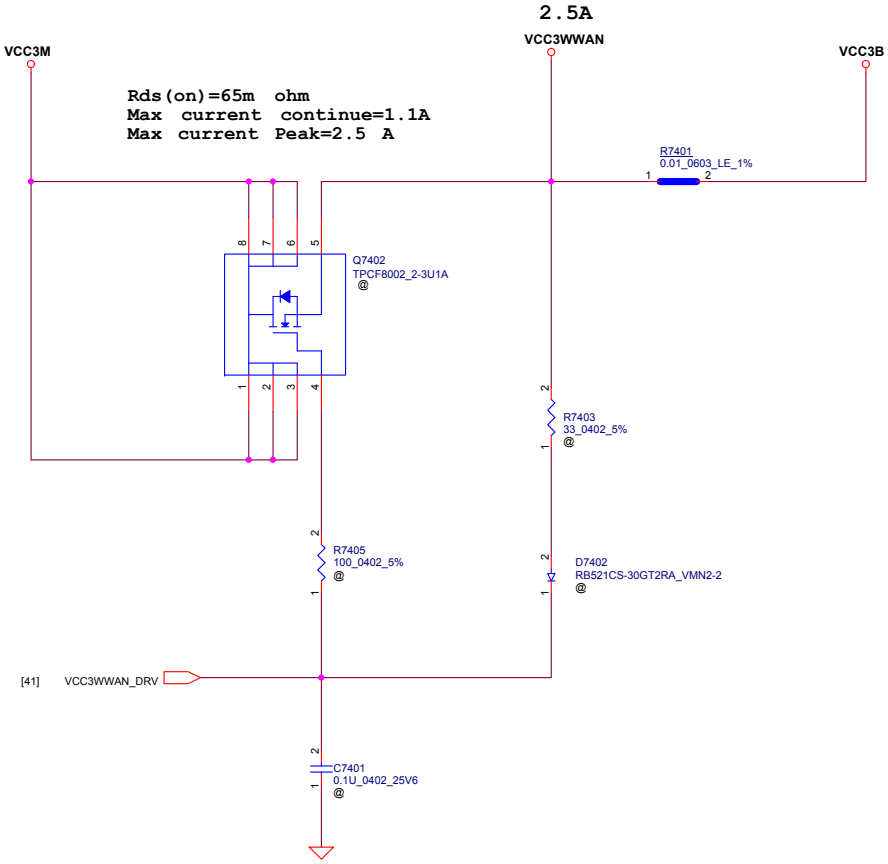
Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW B

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 73 of 99





Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW WWAN&WLAN

Size: Custom | Document Number: NM-A611 | Rev: 0.1

Date: Tuesday, November 03, 2015 | Sheet 74 of 99

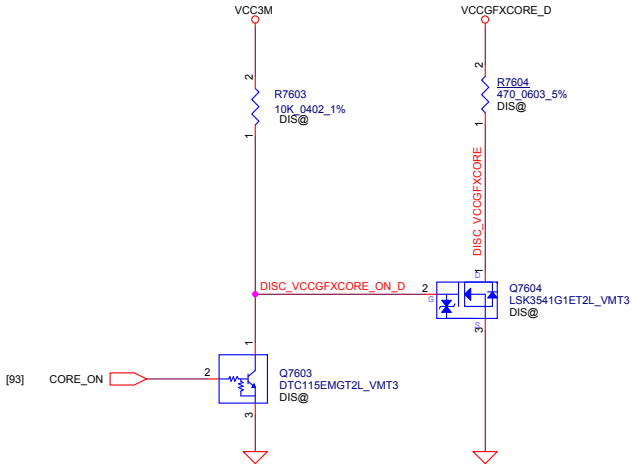
Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

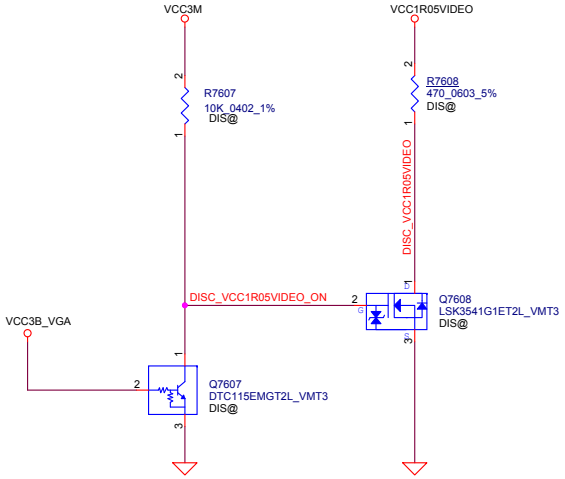
Title

LOAD SW VIDEO&FBVDD

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 75 of 99





Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DISCHARGE CIRCUIT VIDEO

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 76 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title

LCFC

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 77 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title

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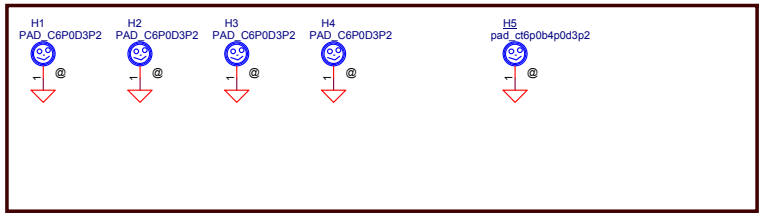
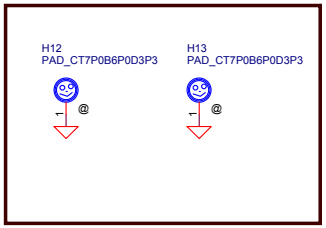
Screw Hole

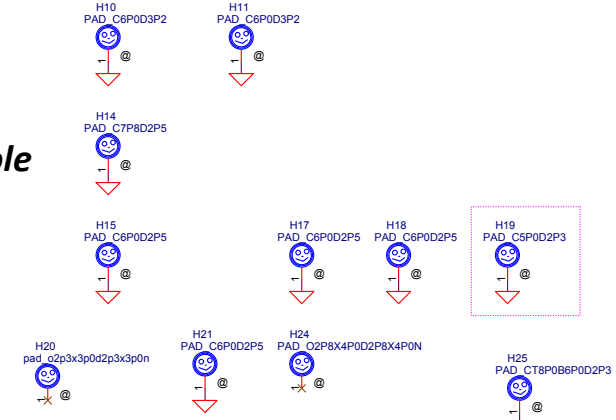
For CPU and GPU



AUDIO SCREW



For ME GND hole



For ME hole

PCB Fedical Mark PAD

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/12/31

Title: SCREW HOLE

Size	Document Number	Rev
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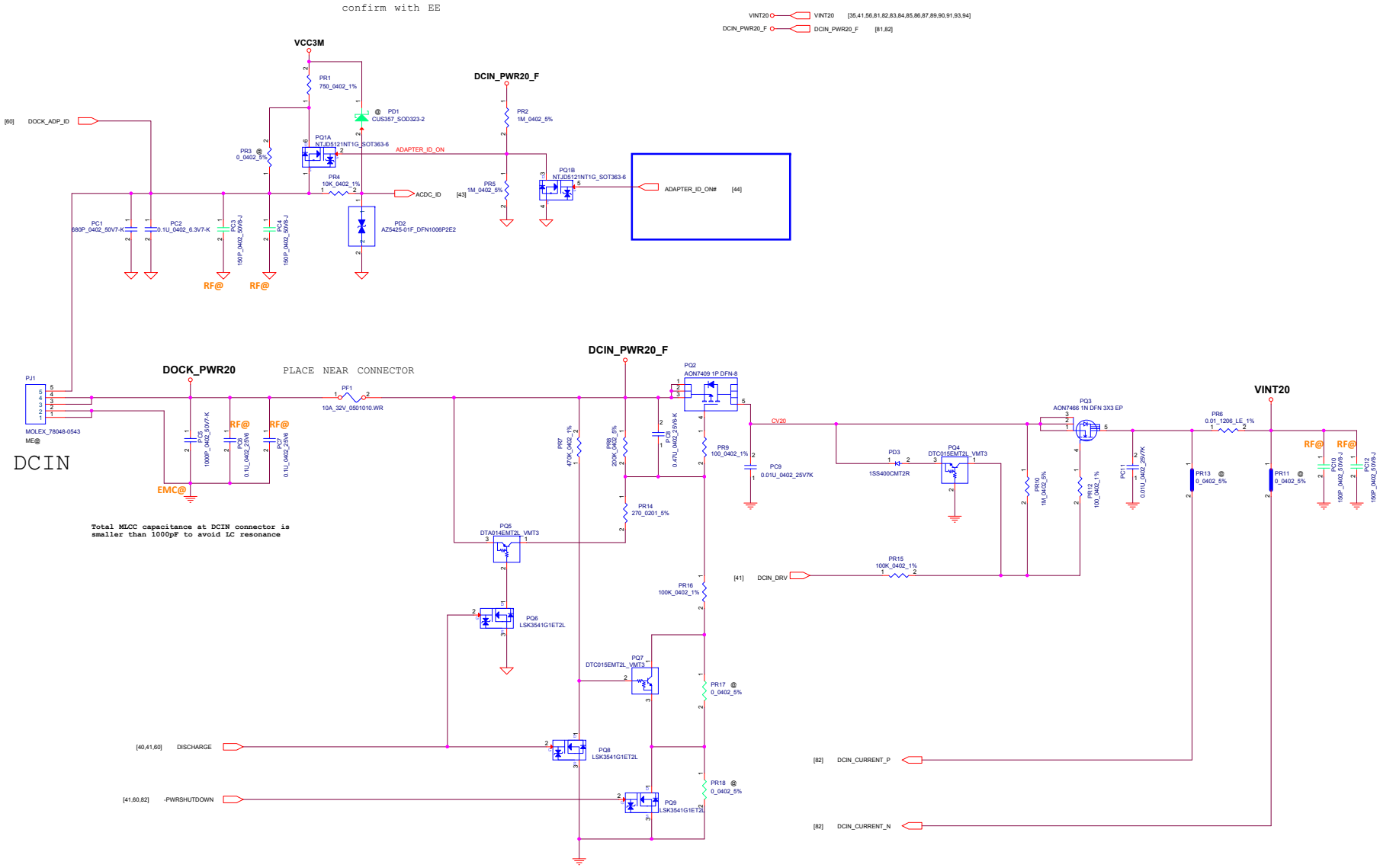

TABLE

PEAK SHIFT	YES	NO
PR17	NO-ASM	ASM
PR7	ASM	NO-ASM
PQ8	ASM	NO-ASM
PQ7	ASM	NO-ASM

LOGIC

Security Classification	LC Future Center Secret Data	
Issued Date	Deciphered Date	

Title: DC-IN

Size: Custom | Document Number: NM-A611 | Rev: 0.1

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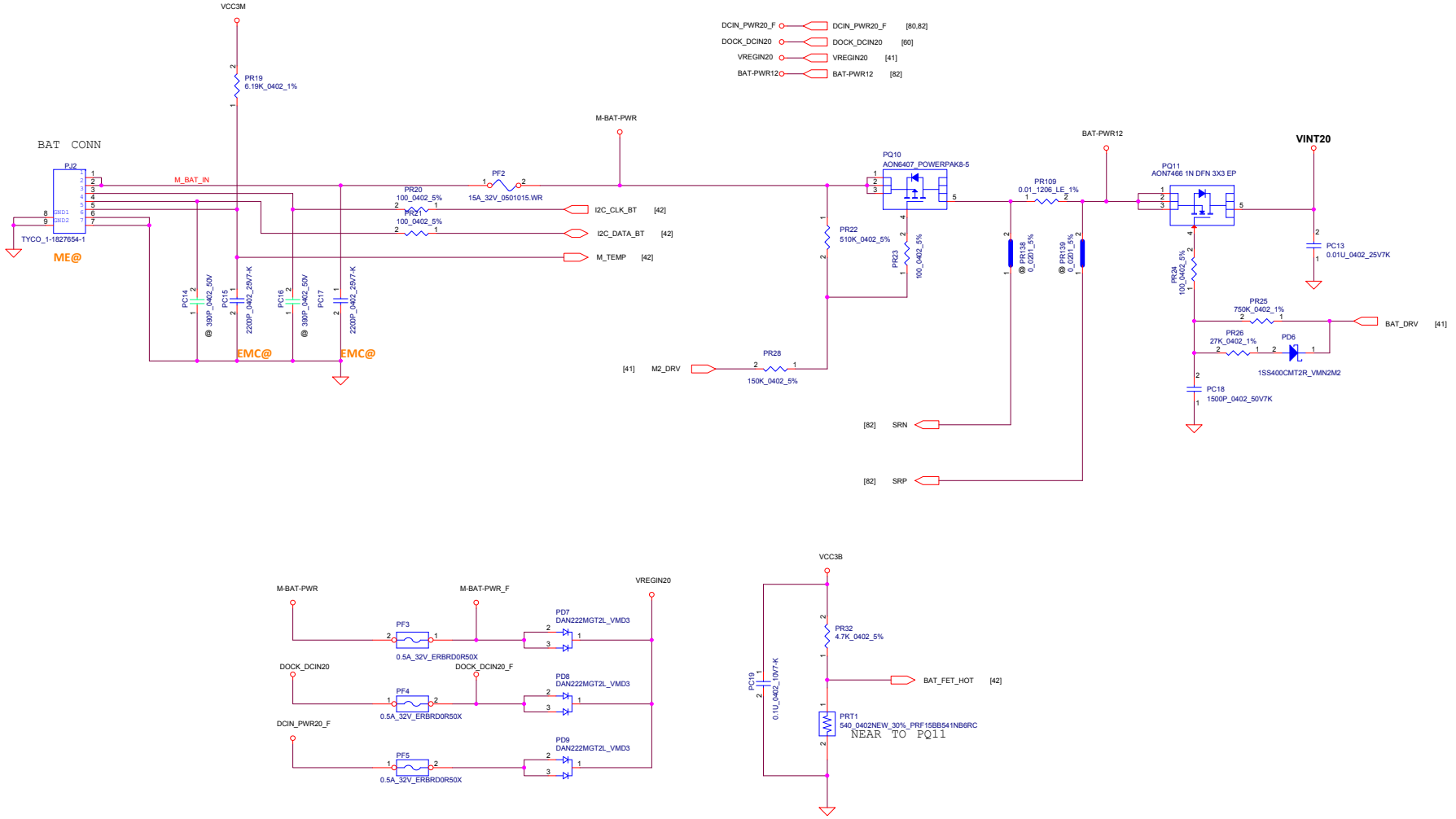
Payton Common

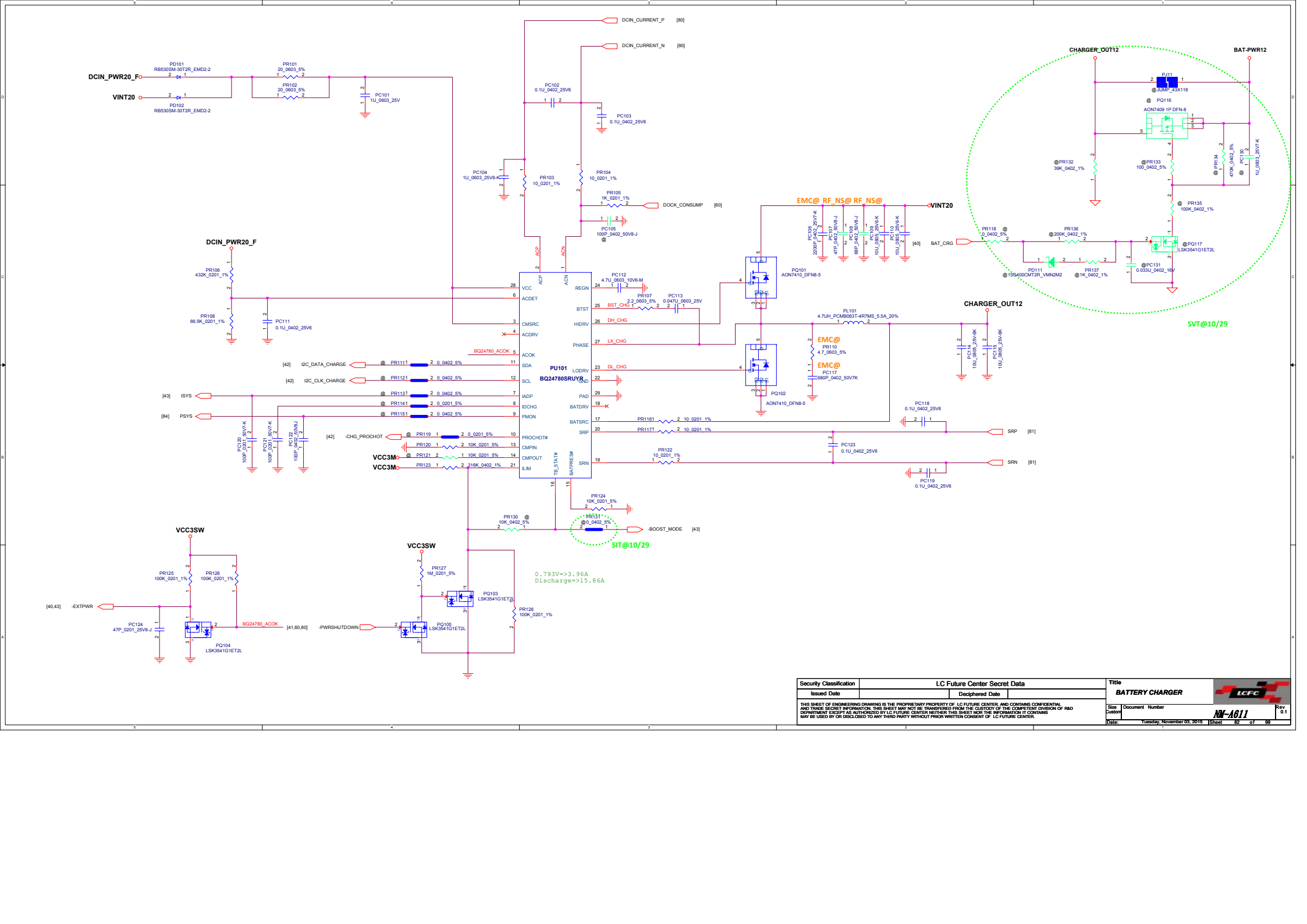


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: **BATTERY INPUT**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 81 of 99



Security Classification	LC Future Center Secret Data	
Issued Date		Deciphered Date

Title	BATTERY CHARGER	
Size: Custom	Document Number: NM-A611	Rev: 0.1
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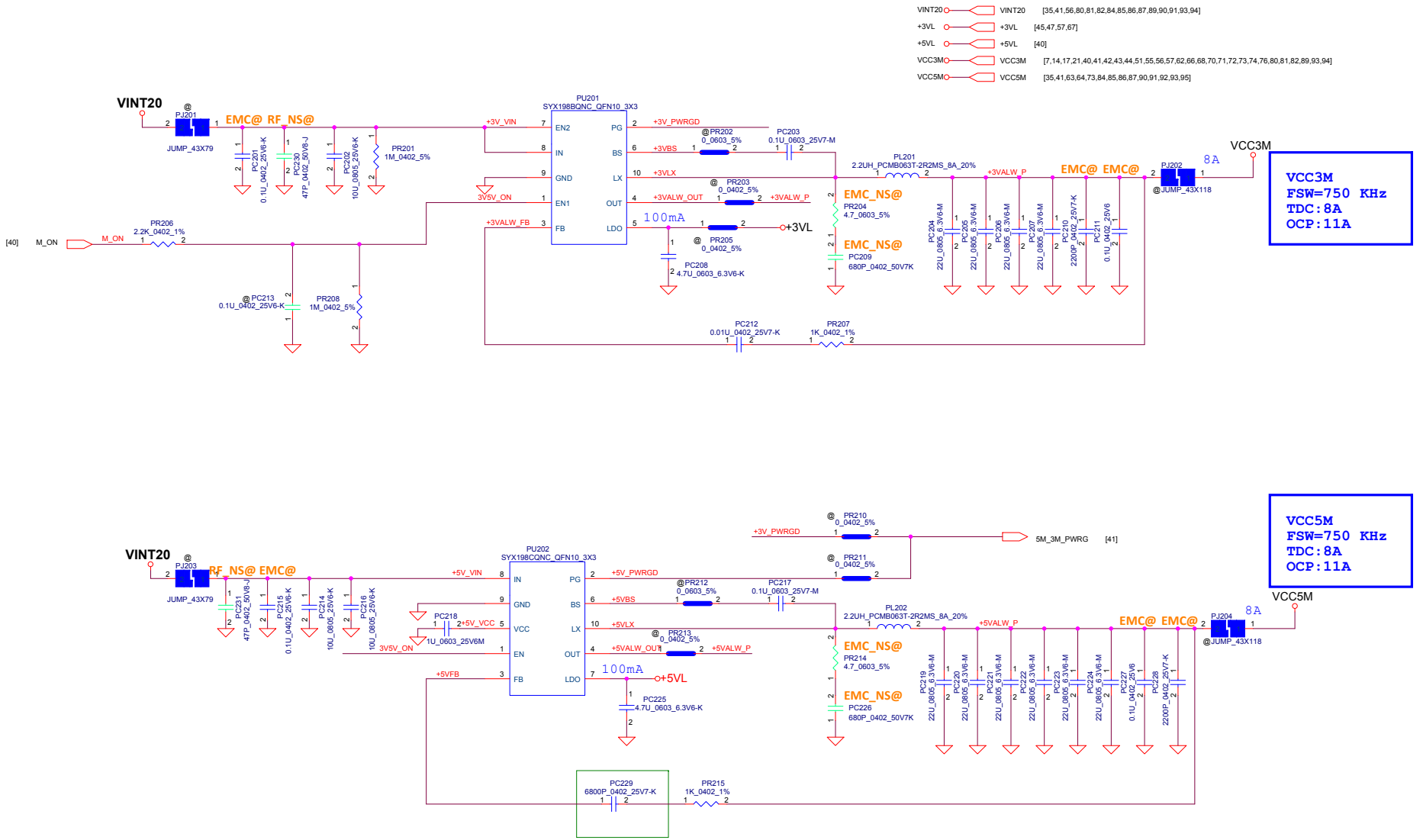

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: 3VALWP/5VALWP

Size: Custom | Document Number: NM-A611 | Rev: 0.1

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Support Skylake H-line 42 processor only

PR464	Vboot for Core/GT
24.9Kohm	0V
169Kohm	1.05V

SVT@10/29

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

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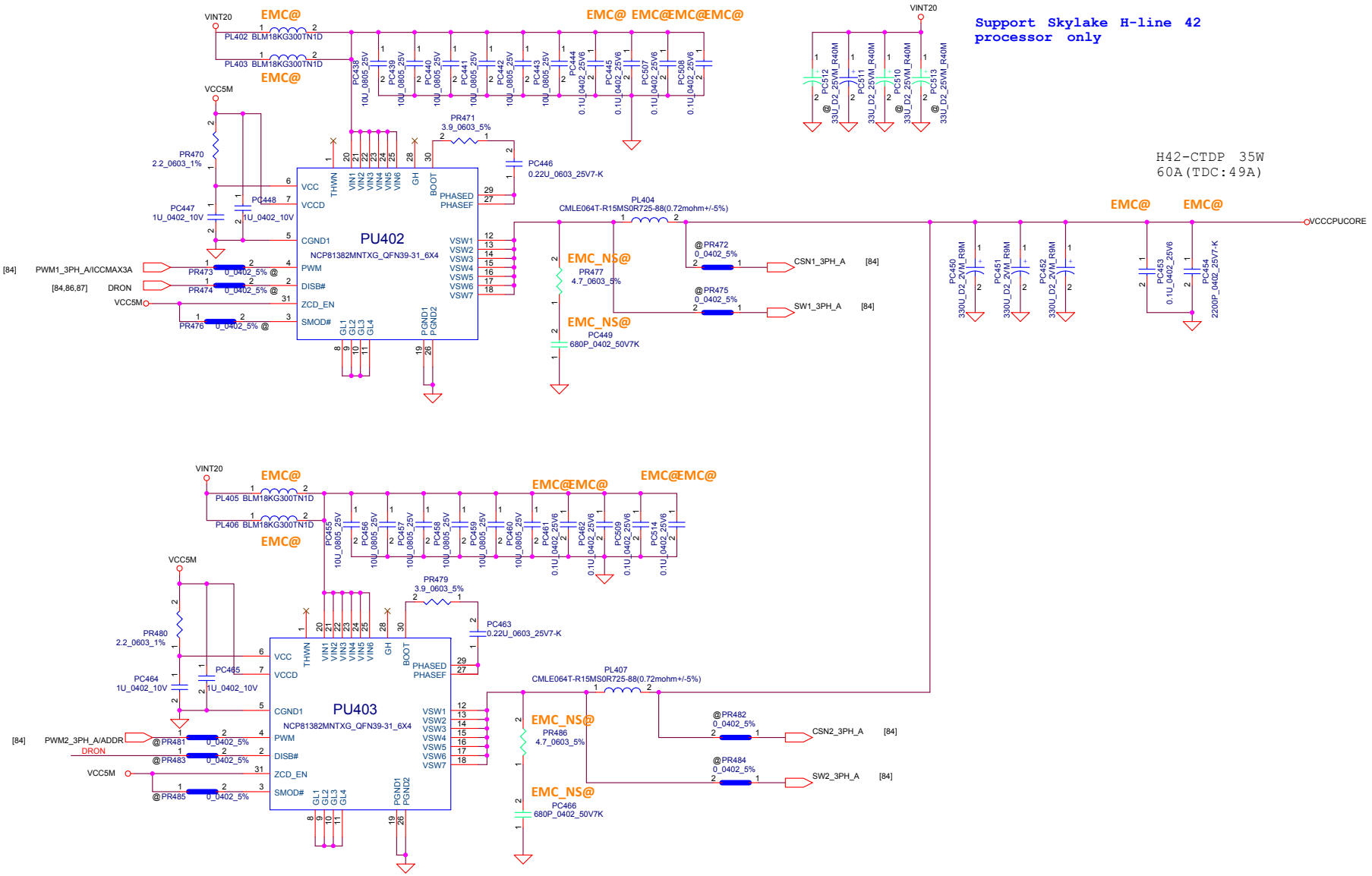
Title	DC/DC IMVP8		
Size: Custom	Document Number: NM-A611		Rev: 0.1
Date: Tuesday, November 03, 2015	Sheet 84 of 99		



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

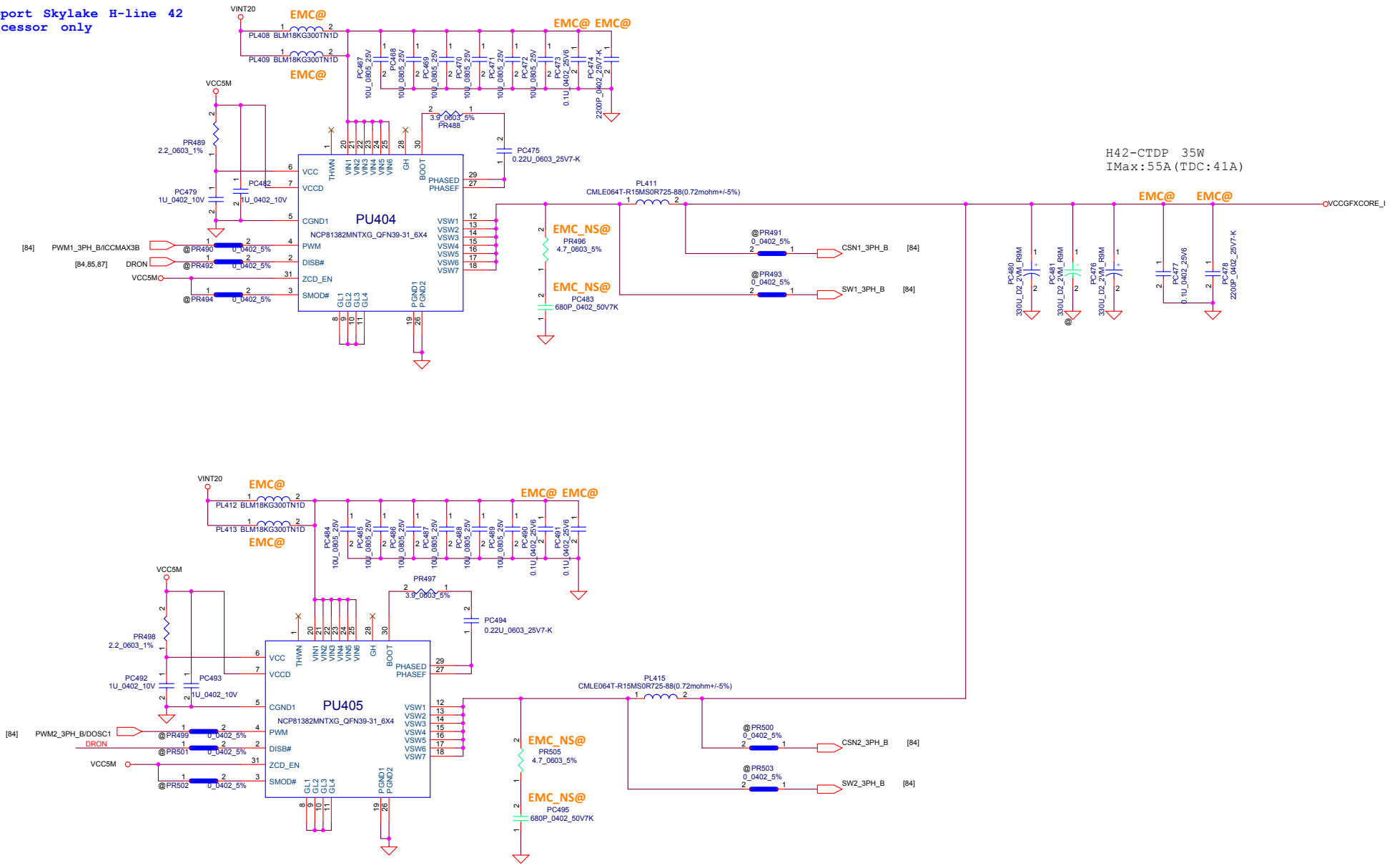
Title: DC/DC VCCPUCORE

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 85 of 99

Walter Unique

Support Skylake H-line 42 processor only



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

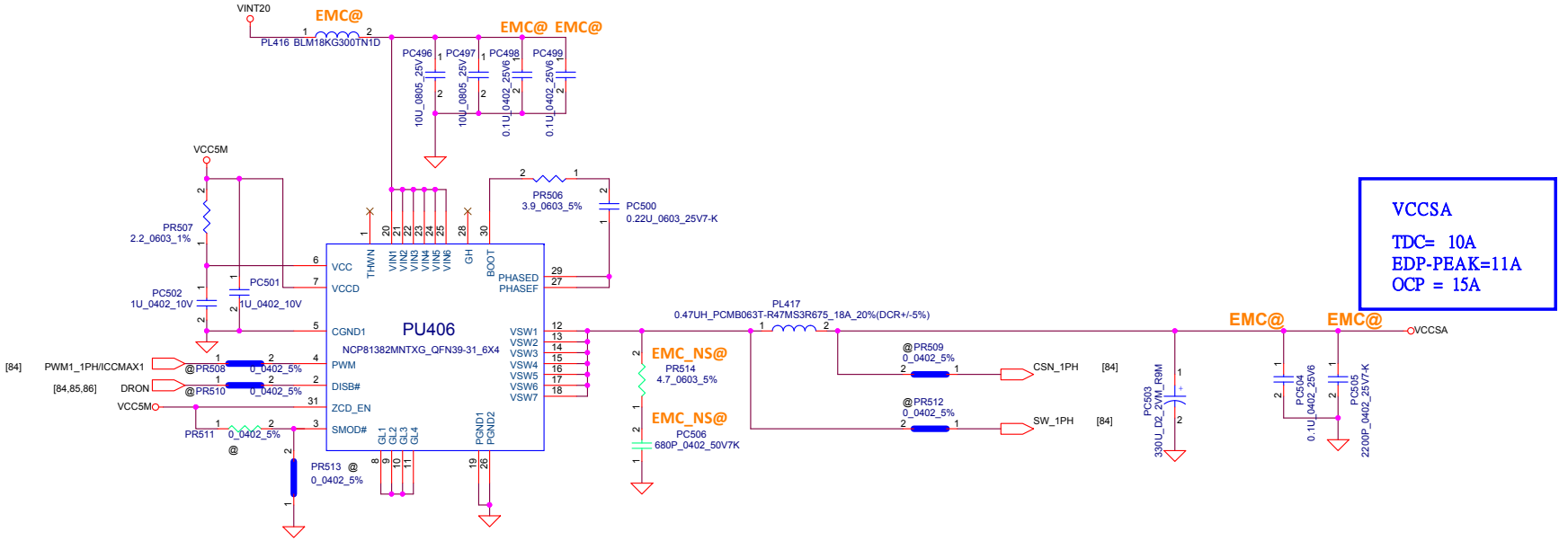
Title: **DC/DC VCCGFXCORE_I**

Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Tuesday, November 03, 2015 Sheet 86 of 99

Walter Unique

Support Skylake H-line 42 processor only



VCCSA

TDC= 10A
EDP-PEAK=11A
OCP = 15A

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCCSA

Size	Document Number	Rev
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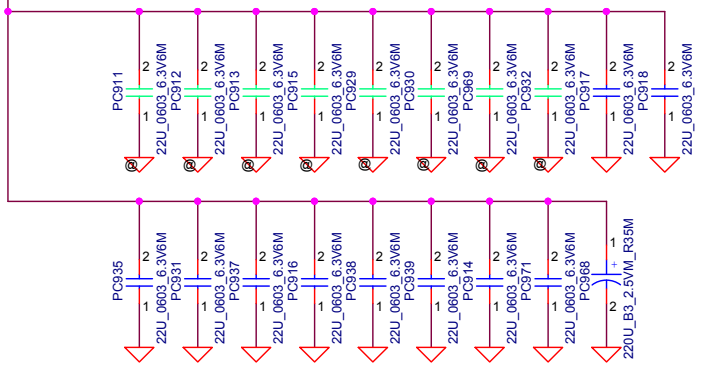
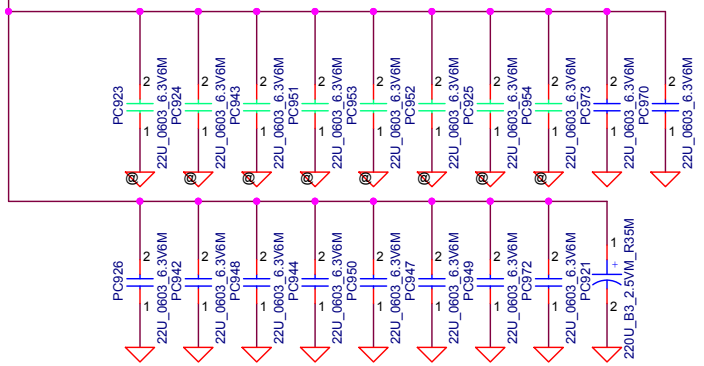
VCCCPUCORE

VCCCPUCORE
22uF 10pcs + 220uF/3528 1pcs



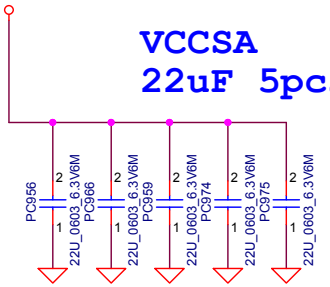
VCCGFXCORE_I

VCCGFXCORE_I
22uF 10pcs + 220uF/3528 1pcs

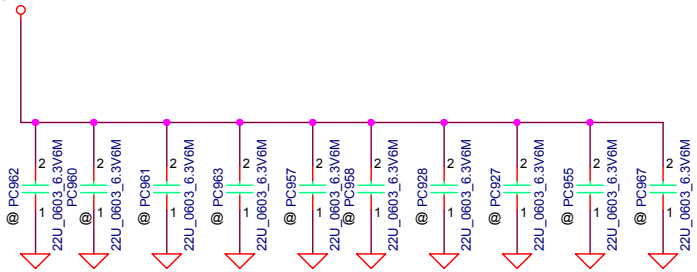


VCCSA

VCCSA
22uF 5pcs



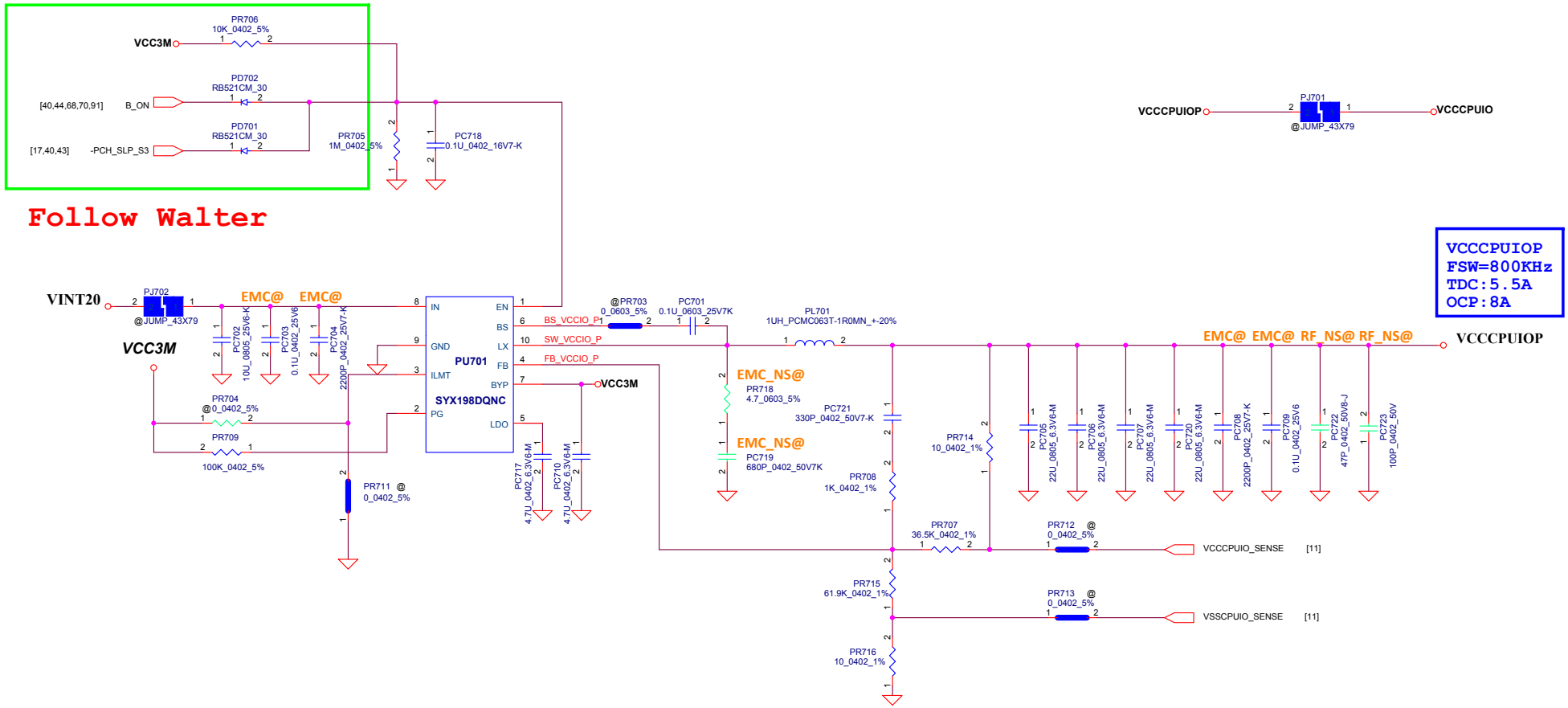
VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
B	NM-A611	0.1
Date: Tuesday, November 03, 2015	Sheet 88 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCCCPUIO

Size	Document Number	Rev
Custom	NM-A611	0.1

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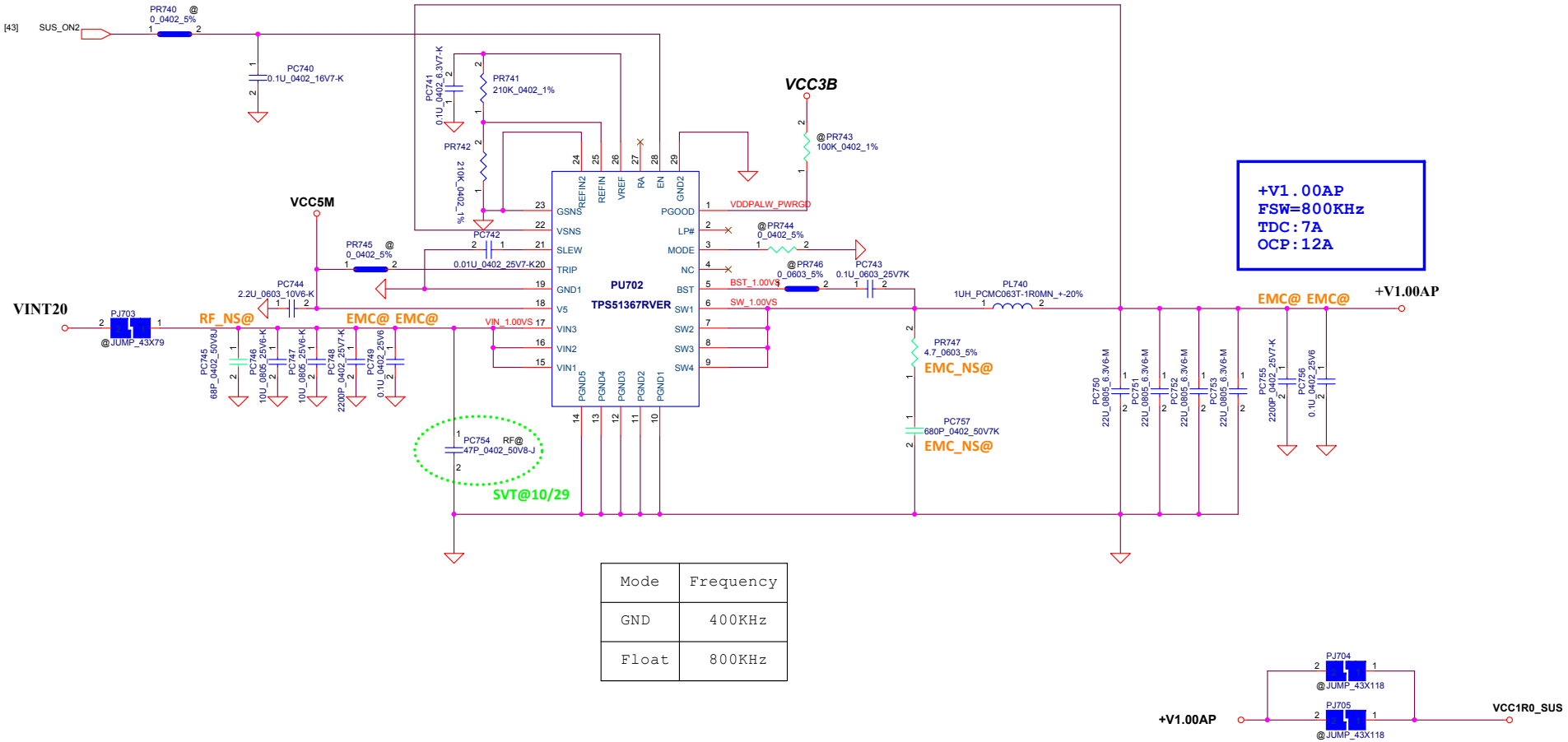

Mode	Frequency
GND	400KHz
Float	800KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCC1R0_SUS

Size: Custom	Document Number: NM-A611	Rev: 0.1
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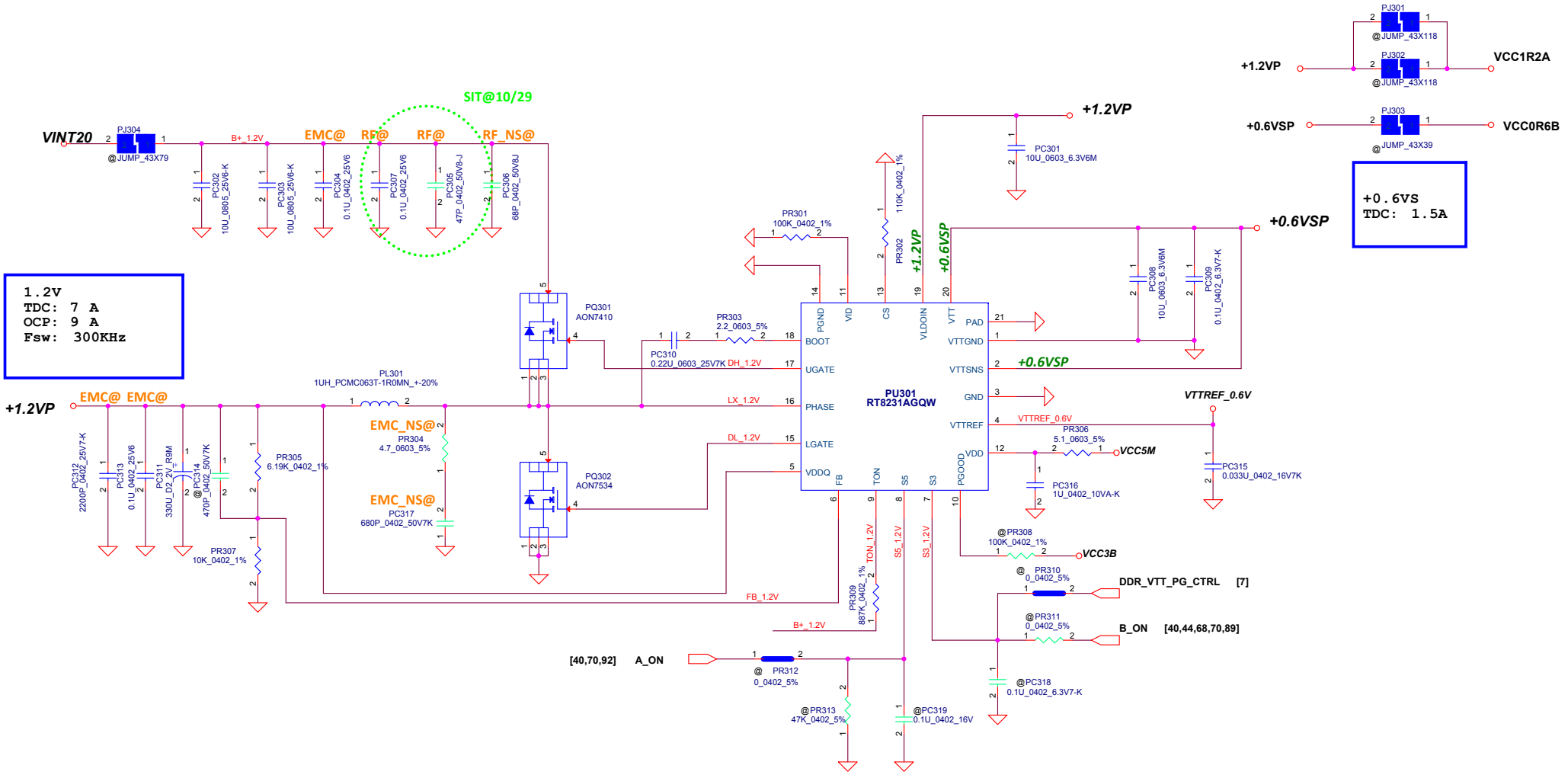

Title		
+1.35V/+0.675VS		
Size: Custom	Document Number: NM-A611	Rev: 0.1
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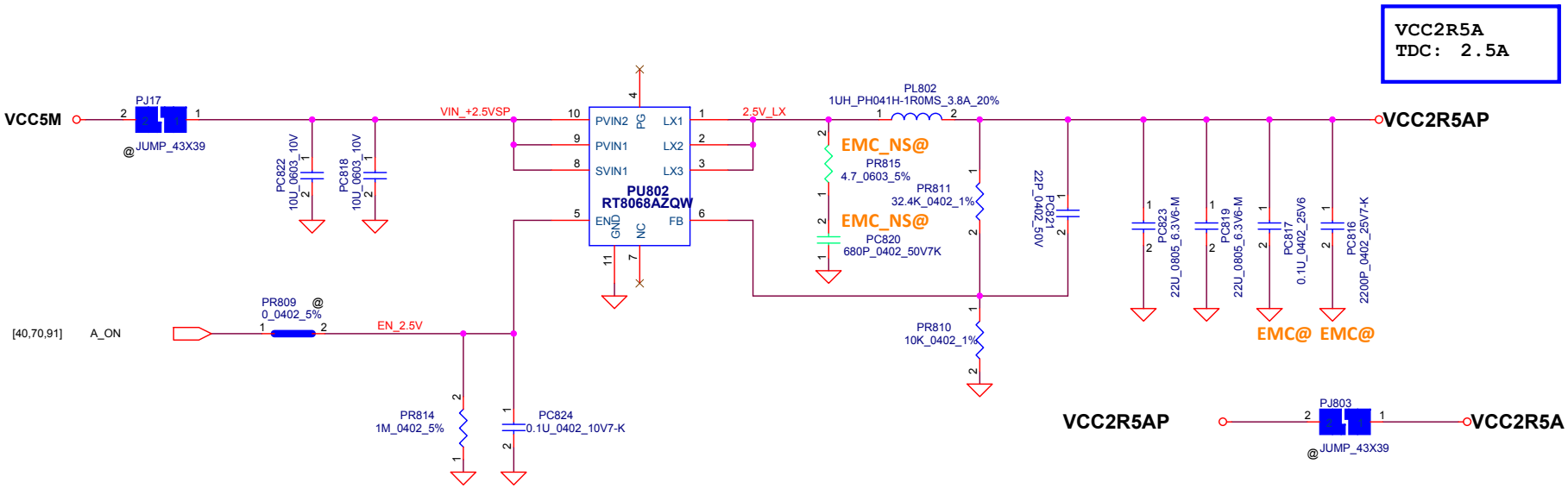

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: DC/DC VCC2R5A

Size	Document Number	Rev
B	NM-A611	0.1

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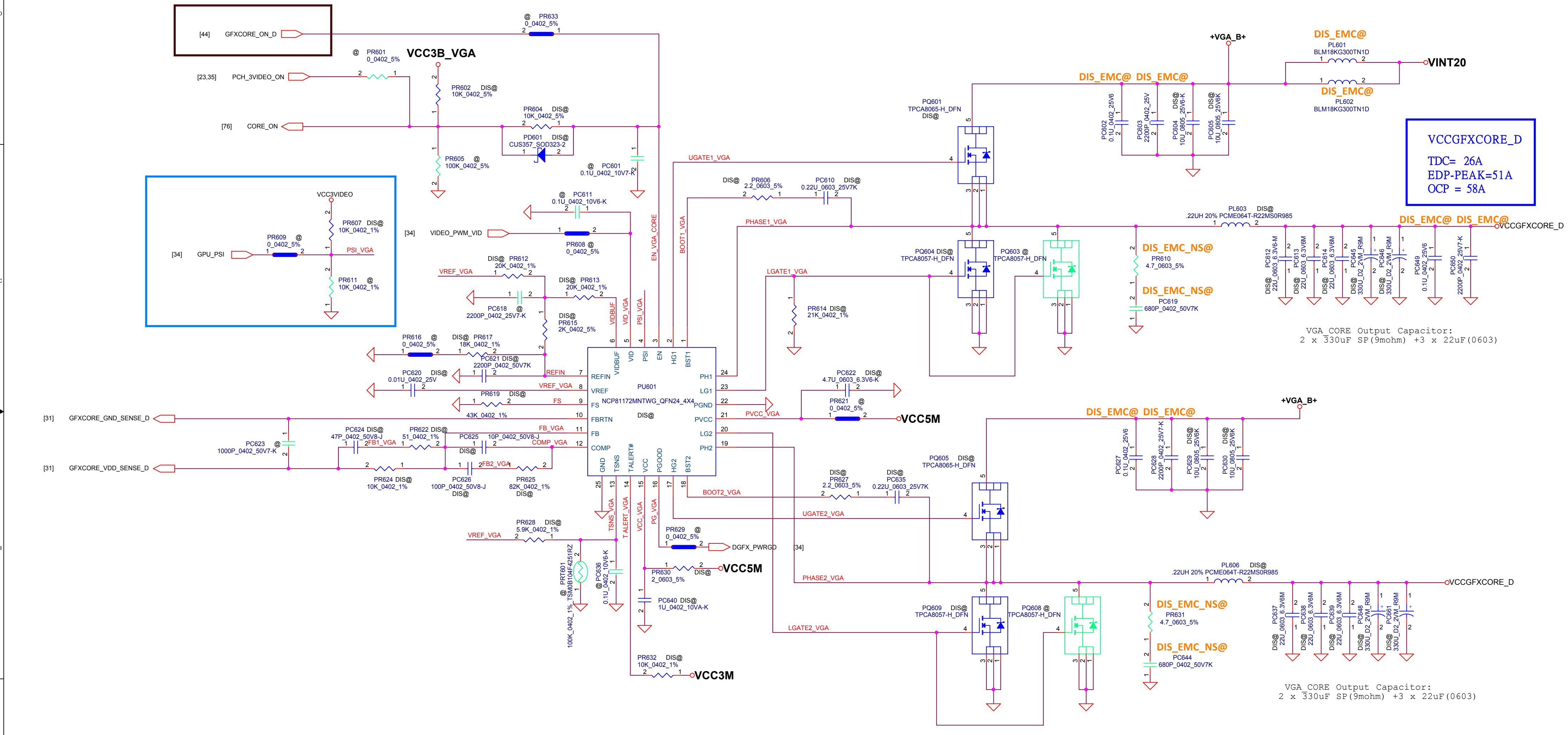

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: PWR-VGA_CORE(NCP81174)

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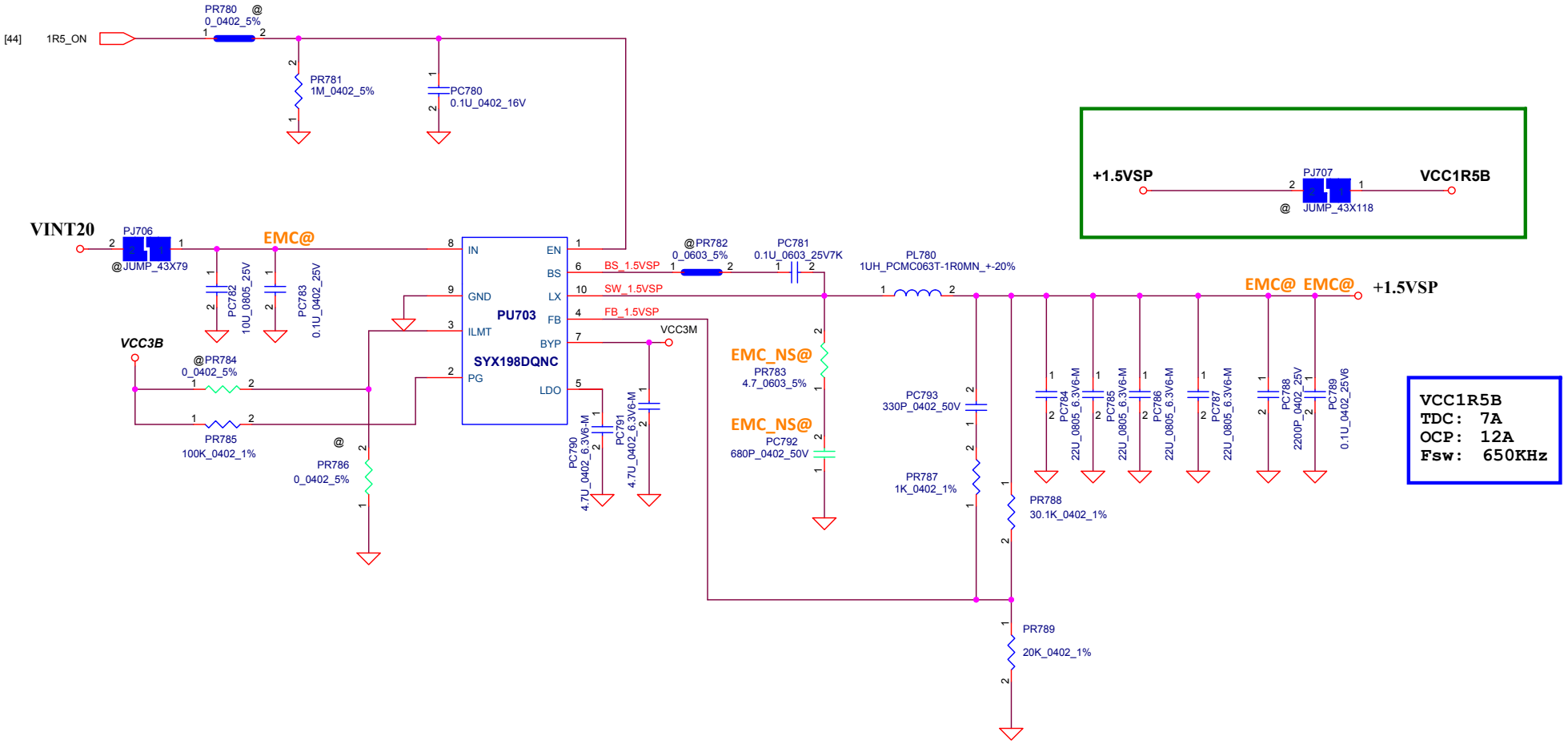

Title			
+1.5VS			
Size B	Document Number NM-A611		Rev 0.1
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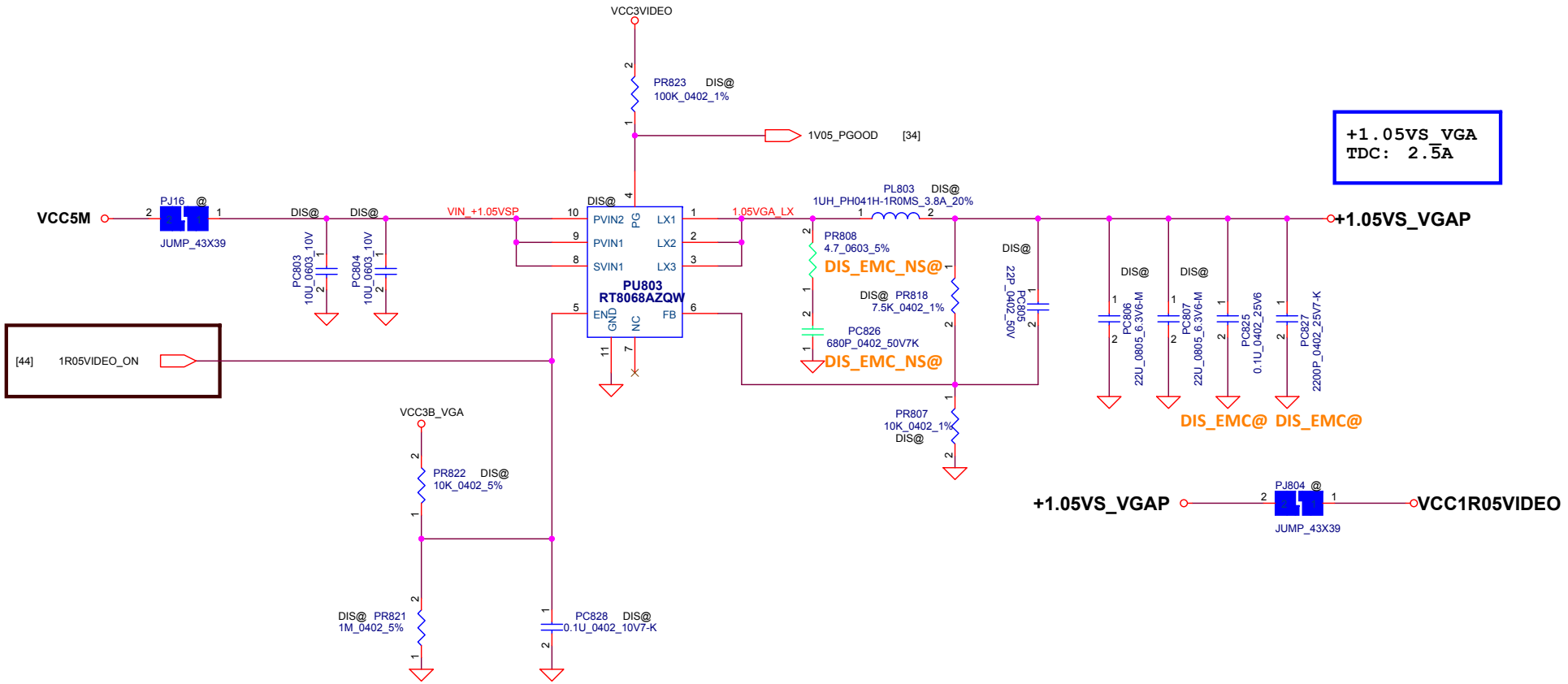

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: PWR-+1.05ALW

Size	Document Number	Rev
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+0.6VSP	+0.6VSP	[91]
+1.05VS_VGAP	+1.05VS_VGAP	[95]
+1.2VP	+1.2VP	[91]
+1.5VSP	+1.5VSP	[94]
+V1.00AP	+V1.00AP	[90]
BAT-PWR12	BAT-PWR12	[81,82]
DCIN_PWR20_F	DCIN_PWR20_F	[80,81,82]
DOCK_DCIN20	DOCK_DCIN20	[60,81]
DOCK_DCIN20_F	DOCK_DCIN20_F	[81]
DOCK_PWR20	DOCK_PWR20	[60,80]
M-BAT-PWR	M-BAT-PWR	[81]
M-BAT-PWR_F	M-BAT-PWR_F	[81]
VCC2R5AP	VCC2R5AP	[92]
VCC3P	VCC3P	[56]
VTTREF_0.6V	VTTREF_0.6V	[91]

VINT20	VINT20	[35,41,56,80,81,82,83,84,85,86,87,89,90,91,93,94]
+3VL	+3VL	[45,47,57,67,83]
+5VL	+5VL	[40,83]
VCC3M	VCC3M	[7,14,17,21,40,41,42,43,44,51,55,56,57,62,66,68,70,71,72,73,74,76,80,81,82,83,89,93,94]
VCC3_SUS	VCC3_SUS	[7,14,15,16,17,18,21,23,24,26,42,43,45,71]
VCC3B	VCC3B	[7,16,17,18,19,20,21,23,24,27,28,35,40,41,42,43,44,45,47,49,54,55,56,57,58,59,60,61,62,67,68,73,74,81,84,90,91,94]
VCC5M	VCC5M	[35,41,63,64,73,83,84,85,86,87,90,91,92,93,95]
VCC5B	VCC5B	[41,45,57,59,61,65,66,67,71,73]
VCCCPUCORE	VCCCPUCORE	[9,85,88]
VCCGFXCORE_I	VCCGFXCORE_I	[10,86,88]
VCCSA	VCCSA	[11,87,88]
VCCST	VCCST	[7,11,16,24,43,70,84]
VCCSTG	VCCSTG	[7,11,43,70]
VCCCPUIO	VCCCPUIO	[5,6,11,89]
RTCVCC	RTCVCC	[14,21,25,45]
VCC0R6B	VCC0R6B	[27,28,91]
VCC3SW	VCC3SW	[25,40,41,42,43,44,60,82]
VCC1R2A	VCC1R2A	[7,11,17,27,28,91]
VCC1R5B	VCC1R5B	[35,45,57,94]
VCC2R5A	VCC2R5A	[27,28,92]
VCC1R0_SUS	VCC1R0_SUS	[7,20,21,24,70,90]
VDD10	VDD10	[41]

VCCGFXCORE_D	VCCGFXCORE_D	[31,35,76,93]
VCC3VIDEO	VCC3VIDEO	[31,34,35,93,95]
VCC3B_VGA	VCC3B_VGA	[34,35,76,93,95]
VCC1R05VIDEO	VCC1R05VIDEO	[31,33,34,76,95]
VCC1R5VIDEO	VCC1R5VIDEO	[33,34,35,37,39]

VCC3_SUS_SPI	VCC3_SUS_SPI	[19,26,55]
VCC5B_AVDD	VCC5B_AVDD	[45]
VCC5B_PVDD12	VCC5B_PVDD12	[45]
VCC3_SUS_DVDDIO	VCC3_SUS_DVDDIO	[45]
VCC3B_CPVDD	VCC3B_CPVDD	[45]
VCC3B_DVDD	VCC3B_DVDD	[45]
VCC3B_DP	VCC3B_DP	[58]
VCC3B_MINIDP	VCC3B_MINIDP	[59]
VCC3GBE	VCC3GBE	[51,52,53]
VCC3LAN	VCC3LAN	[51,72]
VCC3M_EC	VCC3M_EC	[44]
VCC3WWAN	VCC3WWAN	[62,74]
VCC3WLAN	VCC3WLAN	[62,74]
VCC5_TP	VCC5_TP	[66,71]
VCC3_MC	VCC3_MC	[54]
VCC1R5B_AVDD	VCC1R5B_AVDD	[45]
+UIM_PWR	+UIM_PWR	[62]
+USB_VCCA	+USB_VCCA	[63]
LINE1_VREFO	LINE1_VREFO	[45,48]

NOTE

1:NEED FIX SYMBOL
LV3301,LV3402,UL5201,U3401

2:NEED APPLY PART NUMBER
LV3101==>FROM BLM18PG121SN1D TO BLM15PD121SN1

3:10 OHM ALREADY CHANGE 470 OHM
RV3465,R7604,R7608

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: POWER NET NAME

Size: Custom	Document Number: NM-A611	Rev: 0.1
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