LCFC Confidential

DY510/DY511 M/B Schematics Document

Intel Kabylake H-Processor with DDR4 + NV N17E-G1 GPU

MB NM-B163

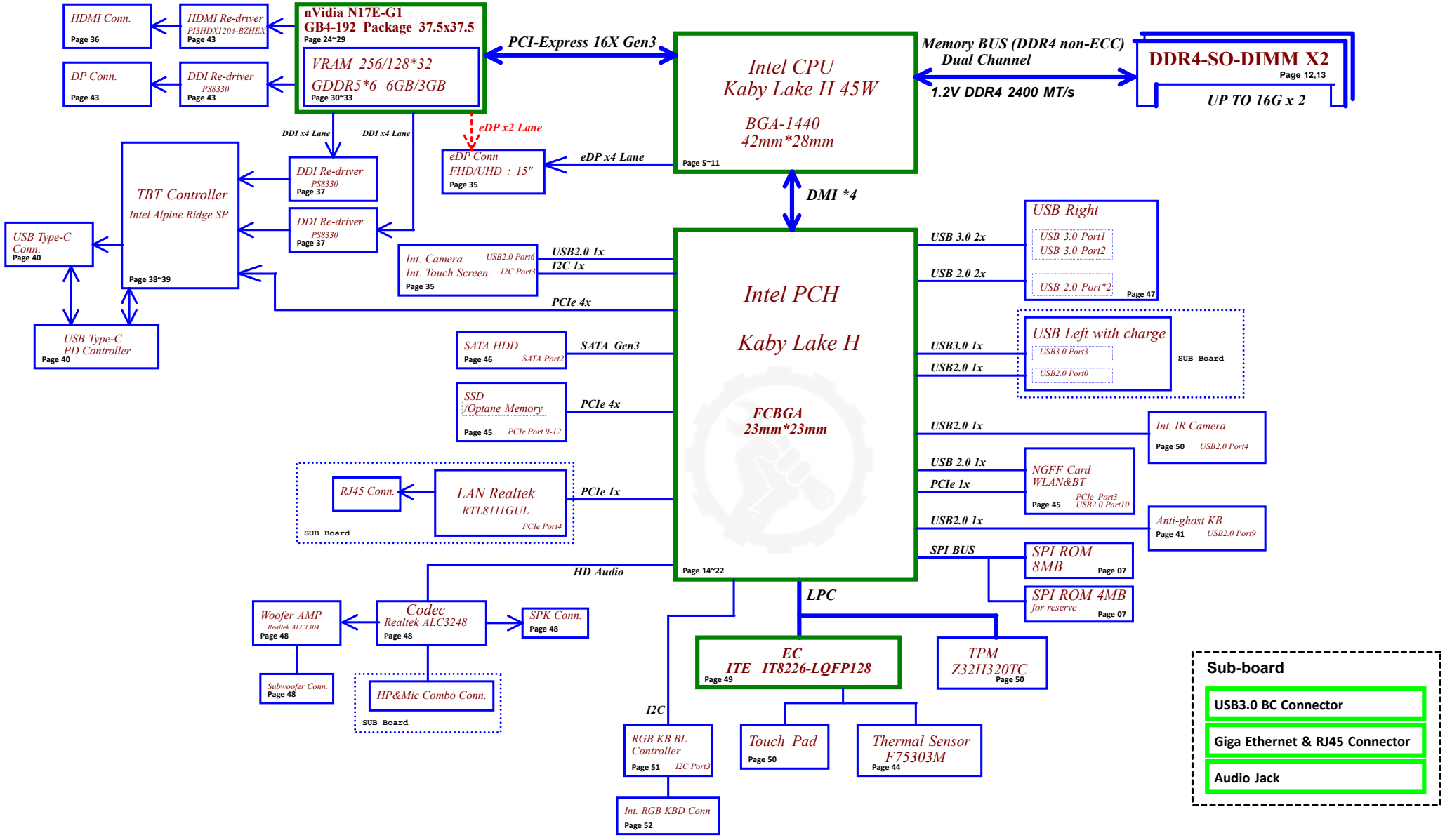
2016-12-12

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title	Cover Page		
Size: Custom	Document Number: DY510/DY511 N17E-G1		Rev: 1.0
Date: Monday, December 19, 2016	Sheet 1 of 75		

LCFC confidential



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: Block Diagram

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 2 of 75

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD NVVDDS +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB2.0 Port table

Port	Function
1	Right USB2.0
2	Left USB3.0
3	Left USB3.0
4	IR Camera
5	Touch Screen
6	Camera
7	
8	XBOX Module
9	Anti-ghost KB
10	Reserved for debug
11	Bluetooth
12	
13	
14	

USB3.0 Port table

Port	Function
1	Left USB3.0
2	Left USB3.0
3	
4	
5	
6	

SATA 3.0 Port table

Port	Function
0	M.2 SSD SATA Gen3
1	HDD SATA Gen3
2	
3	
4	
5	
6	
7	

PCIe 3.0 Port table

Port	Function
1	
2	Cardreader
3	WLAN
4	LAN
5	Thunderbolt
6	Thunderbolt
7	Thunderbolt
8	Thunderbolt
9	SSD
10	SSD
11	SSD
12	SSD
13	
14	
15	
16	
17	
18	
19	

BOM Structure Table

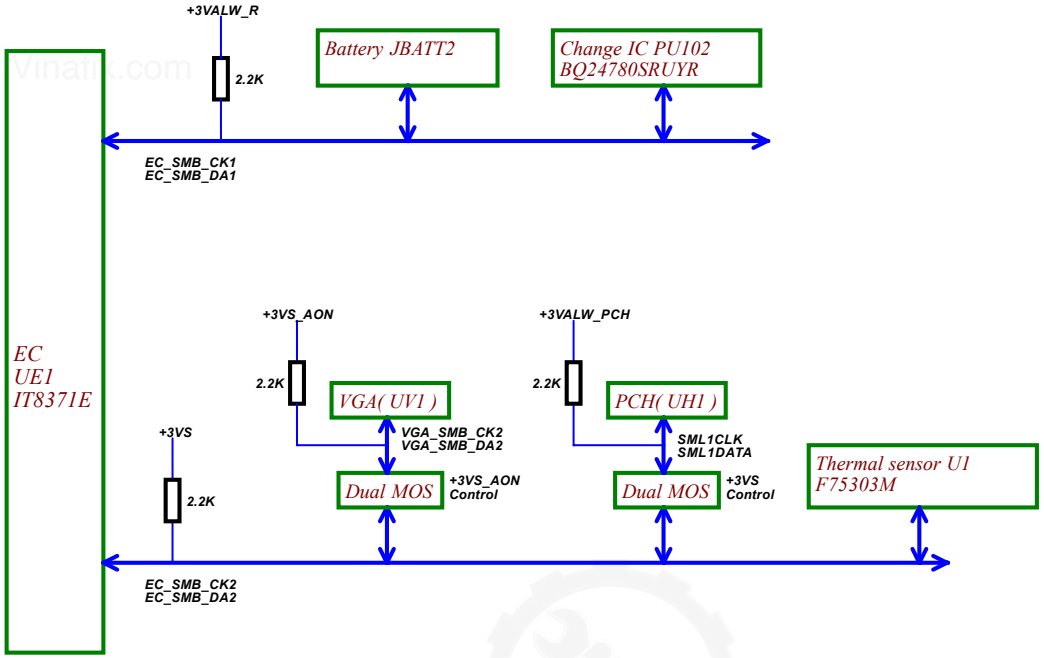
BOM Structure	BTO Item
@	Not stuff
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
ME@	ME part(connector, hole)
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
OPT@	For GPU part
TS@	For support touch panel sku part
TPM@	For support TPM sku part
U31@	For support USB re-driver part
IR@	For support IR camera sku part
RGB@	For support RGB KB Backlight sku part
N_KBL@	For normal KB Backlight sku part Non RGB KB Backlight
AG@	For support Anti-ghost KB sku part
N_KB@	For normal KB sku part Non Anti-ghost KB
CD@	Cost down part
XBOX@	For support XBOX Module sku part

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: **Notes List**

Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 3 of 75



SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	V +3VALW_R ReserVe	V +3VALW_R ReserVe	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +3VS_VGA	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X	X	X	V +3VS
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS Reserve	X	V +3VALW_PCH	V +3VS	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +3VALW_BL	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: I2C Block

Size	Document Number	Rev
D	DX510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 4 of 75

[24] PCIE_CRX_GTX_N[0..15]
[24] PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] [24]
PCIE_CTX_C_GRX_P[0..15] [24]

VCCIO
PEG_COMP RC1 1 2 24.9_0402_1%

CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

UC1C SKYLAKE_HALO
BGA1440

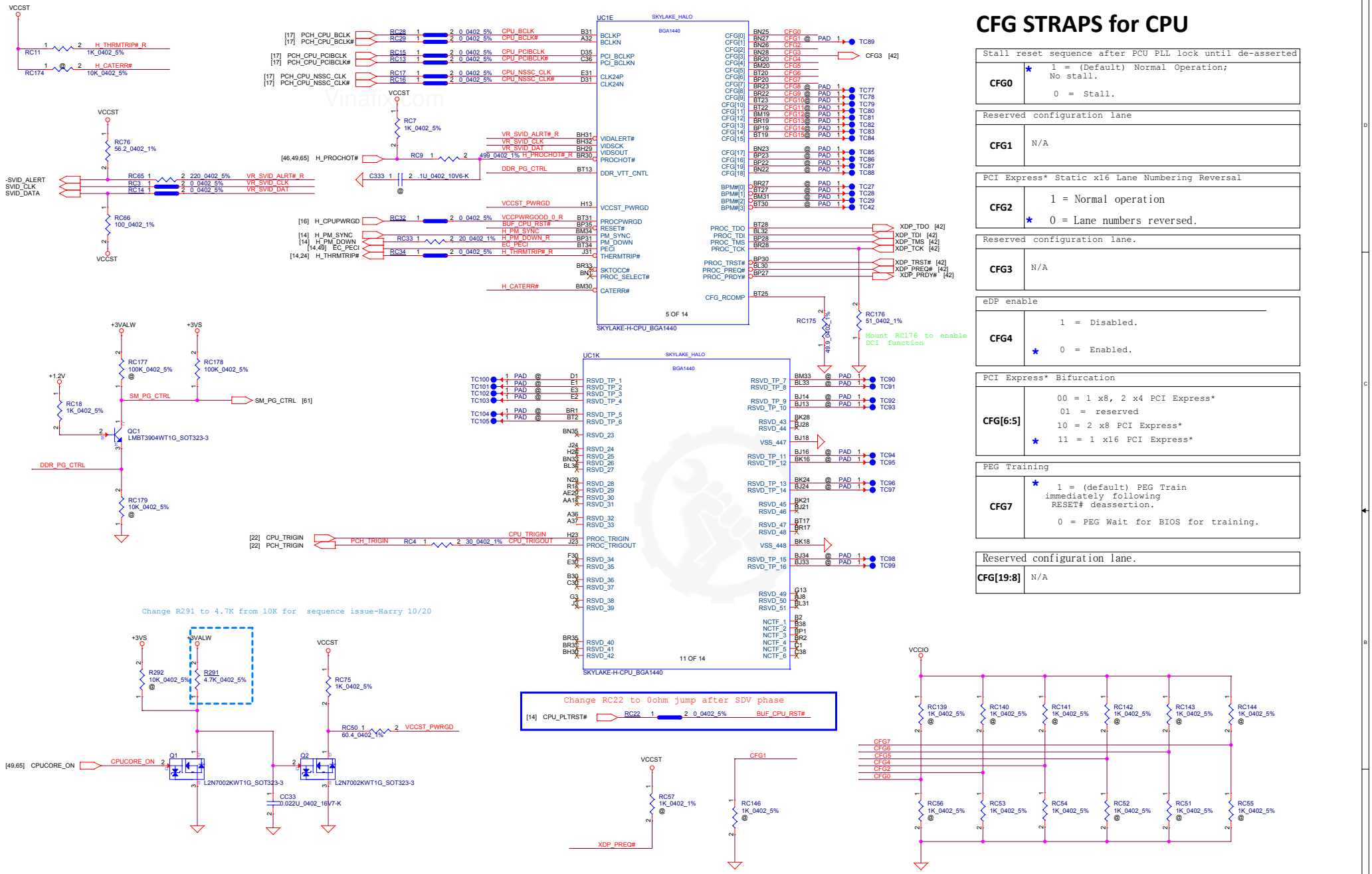
PCIE_CRX_GTX_P15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PCIE_CTX_GRX_P15	OPT@	CC32	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P15
PCIE_CRX_GTX_N15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PCIE_CTX_GRX_N15	OPT@	CC16	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N15
PCIE_CRX_GTX_P14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PCIE_CTX_GRX_P14	OPT@	CC31	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P14
PCIE_CRX_GTX_N14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PCIE_CTX_GRX_N14	OPT@	CC15	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N14
PCIE_CRX_GTX_P13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PCIE_CTX_GRX_P13	OPT@	CC30	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P13
PCIE_CRX_GTX_N13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PCIE_CTX_GRX_N13	OPT@	CC14	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N13
PCIE_CRX_GTX_P12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PCIE_CTX_GRX_P12	OPT@	CC29	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P12
PCIE_CRX_GTX_N12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PCIE_CTX_GRX_N12	OPT@	CC13	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N12
PCIE_CRX_GTX_P11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PCIE_CTX_GRX_P11	OPT@	CC28	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P11
PCIE_CRX_GTX_N11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PCIE_CTX_GRX_N11	OPT@	CC12	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N11
PCIE_CRX_GTX_P10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PCIE_CTX_GRX_P10	OPT@	CC27	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P10
PCIE_CRX_GTX_N10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PCIE_CTX_GRX_N10	OPT@	CC11	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N10
PCIE_CRX_GTX_P9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PCIE_CTX_GRX_P9	OPT@	CC26	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P9
PCIE_CRX_GTX_N9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PCIE_CTX_GRX_N9	OPT@	CC10	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N9
PCIE_CRX_GTX_P8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PCIE_CTX_GRX_P8	OPT@	CC25	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P8
PCIE_CRX_GTX_N8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PCIE_CTX_GRX_N8	OPT@	CC9	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N8
PCIE_CRX_GTX_P7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PCIE_CTX_GRX_P7	OPT@	CC24	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P7
PCIE_CRX_GTX_N7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PCIE_CTX_GRX_N7	OPT@	CC8	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N7
PCIE_CRX_GTX_P6	F16	PEG_RXP[9]	PEG_TXP[9]	C16	PCIE_CTX_GRX_P6	OPT@	CC23	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P6
PCIE_CRX_GTX_N6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PCIE_CTX_GRX_N6	OPT@	CC7	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N6
PCIE_CRX_GTX_P5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PCIE_CTX_GRX_P5	OPT@	CC22	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P5
PCIE_CRX_GTX_N5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PCIE_CTX_GRX_N5	OPT@	CC6	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N5
PCIE_CRX_GTX_P4	F14	PEG_RXP[11]	PEG_TXP[11]	C14	PCIE_CTX_GRX_P4	OPT@	CC21	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P4
PCIE_CRX_GTX_N4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PCIE_CTX_GRX_N4	OPT@	CC5	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N4
PCIE_CRX_GTX_P3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PCIE_CTX_GRX_P3	OPT@	CC20	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P3
PCIE_CRX_GTX_N3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PCIE_CTX_GRX_N3	OPT@	CC4	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N3
PCIE_CRX_GTX_P2	F12	PEG_RXP[13]	PEG_TXP[13]	C12	PCIE_CTX_GRX_P2	OPT@	CC19	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P2
PCIE_CRX_GTX_N2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PCIE_CTX_GRX_N2	OPT@	CC3	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N2
PCIE_CRX_GTX_P1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PCIE_CTX_GRX_P1	OPT@	CC18	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P1
PCIE_CRX_GTX_N1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PCIE_CTX_GRX_N1	OPT@	CC2	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N1
PCIE_CRX_GTX_P0	F10	PEG_RXP[15]	PEG_TXP[15]	C10	PCIE_CTX_GRX_P0	OPT@	CC17	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_P0
PCIE_CRX_GTX_N0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PCIE_CTX_GRX_N0	OPT@	CC1	1	2	0.22U_0402_10V6K	PCIE_CTX_C_GRX_N0
PEG_COMP	G2	PEG_RCOMP									

[19] DMI_CRX_PTX_P0	DMI_CRX_PTX_P0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0 [19]
[19] DMI_CRX_PTX_N0	DMI_CRX_PTX_N0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0 [19]
[19] DMI_CRX_PTX_P1	DMI_CRX_PTX_P1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1 [19]
[19] DMI_CRX_PTX_N1	DMI_CRX_PTX_N1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1 [19]
[19] DMI_CRX_PTX_P2	DMI_CRX_PTX_P2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2 [19]
[19] DMI_CRX_PTX_N2	DMI_CRX_PTX_N2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2 [19]
[19] DMI_CRX_PTX_P3	DMI_CRX_PTX_P3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3 [19]
[19] DMI_CRX_PTX_N3	DMI_CRX_PTX_N3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3 [19]

3 OF 14
SKYLAKE-H-CPU_BGA1440

Security Classification	LC Future Center Secret Data		Title	CPU (1/7) DMI,PEG
Issued Date	2015/02/26	Deciphered Date 2016/02/26		

Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0
Date: Monday, December 19, 2016	Sheet 5 of 75	



CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. ★ 0 = Enabled.

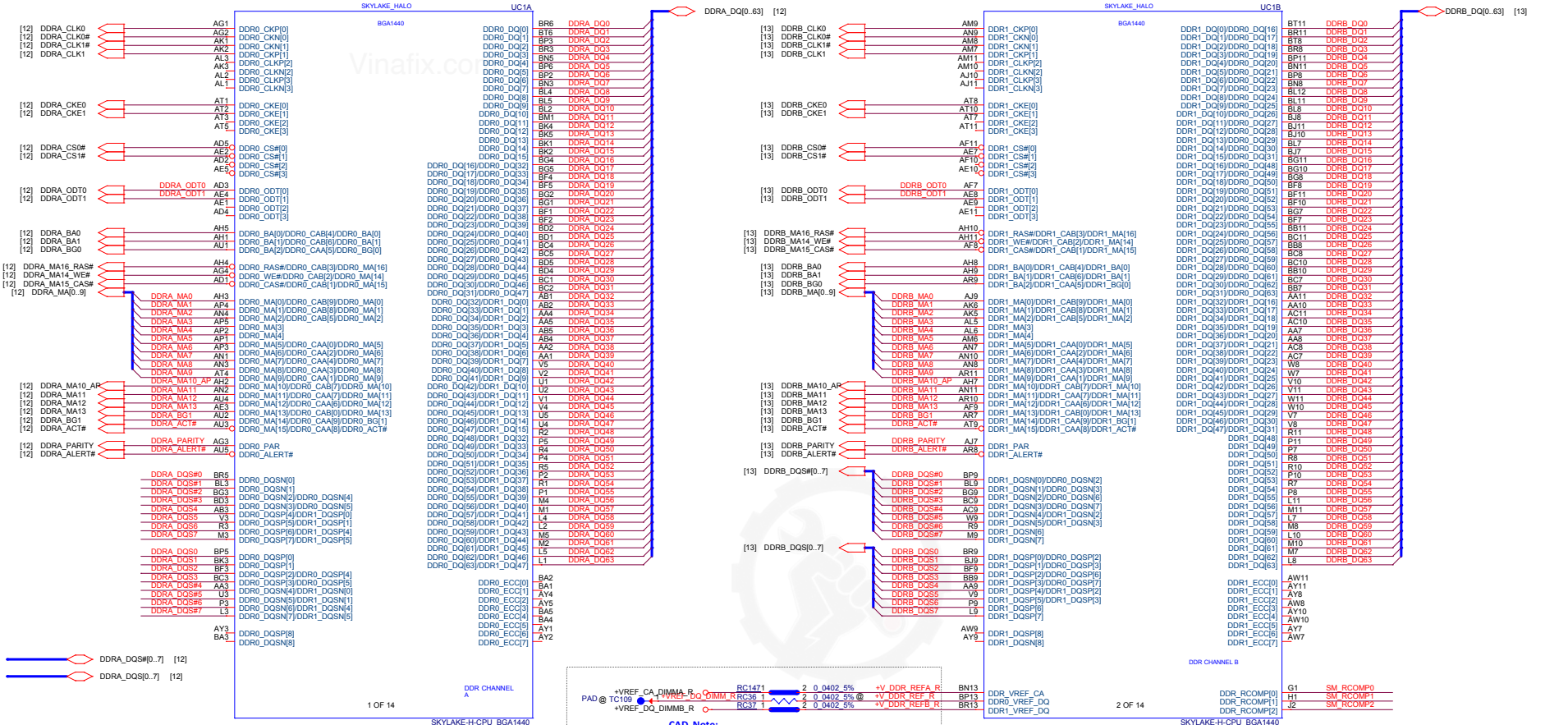
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* ★ 11 = 1 x16 PCI Express*

PEG Training	
CFG7	★ 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.

Reserved configuration lane.	
CFG[19:8]	N/A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	CPU (2/7) PM, XDP, CLK, CFG		
Size C	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 6 of 75		



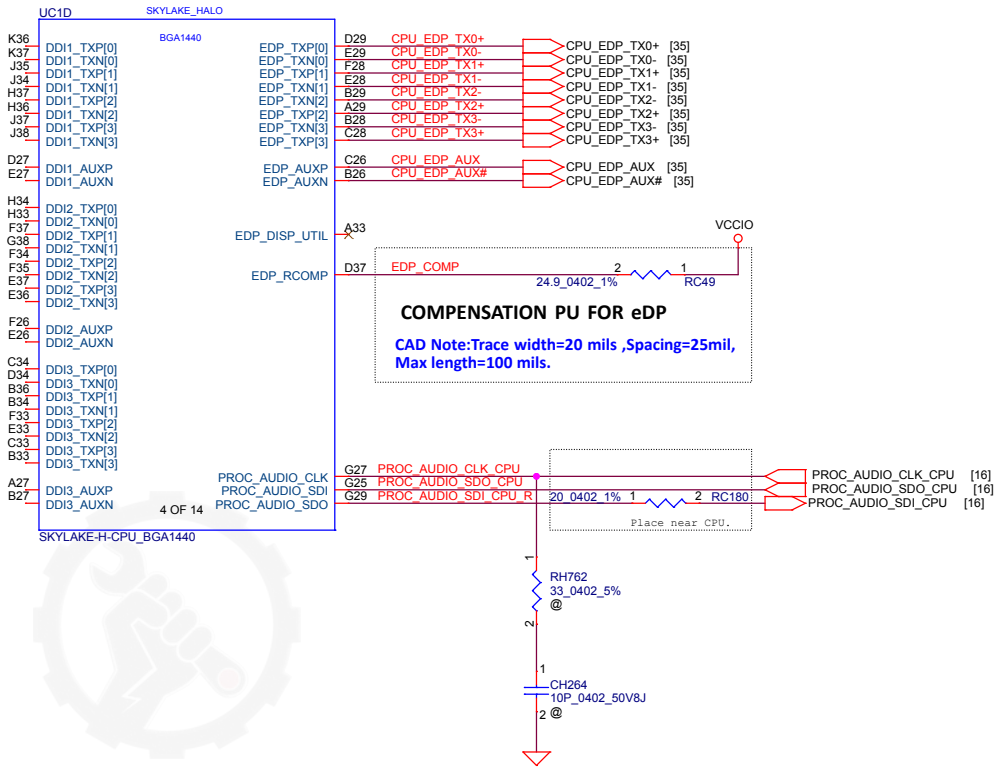
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 7 of 75

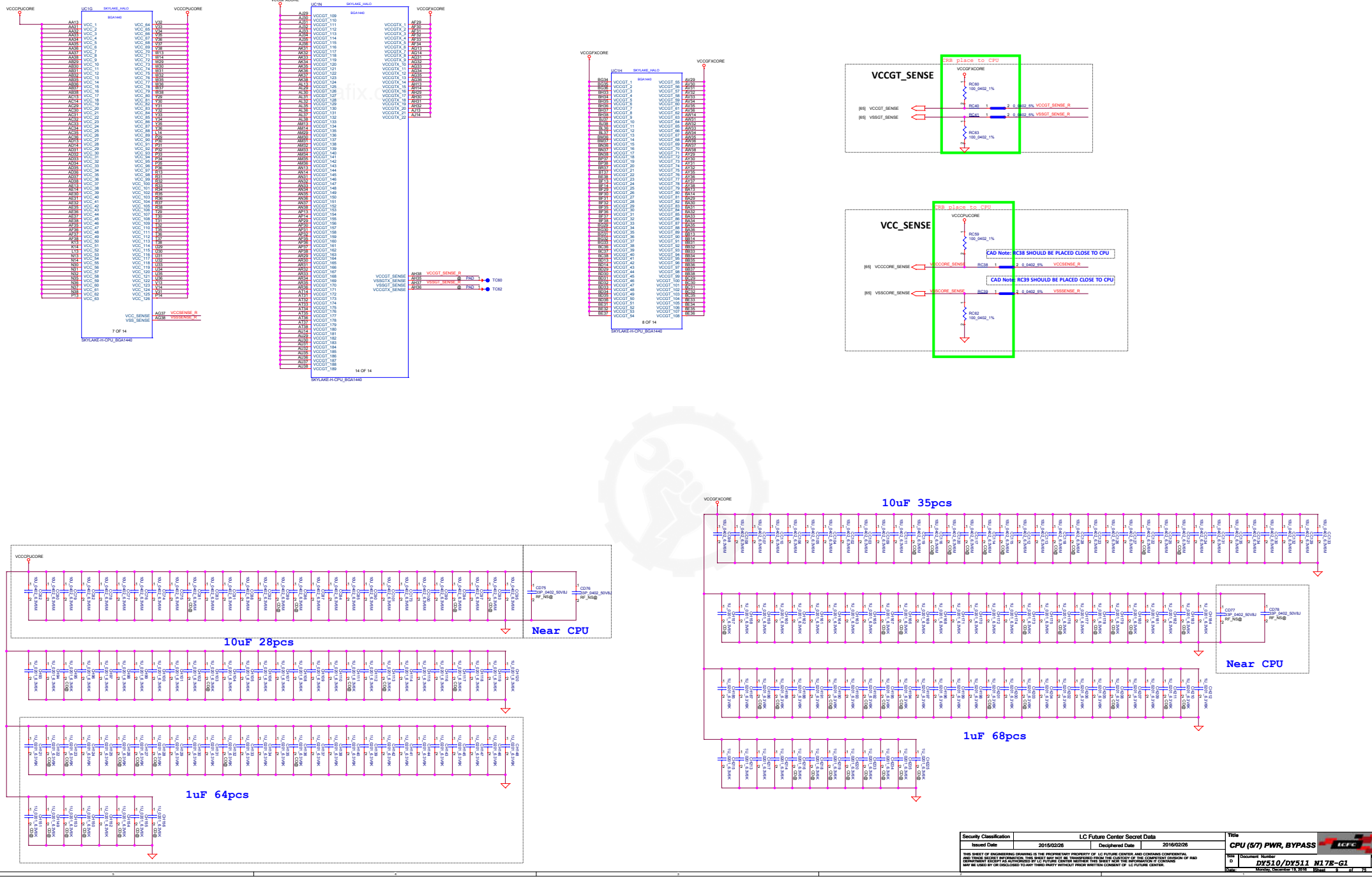


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 8 of 75



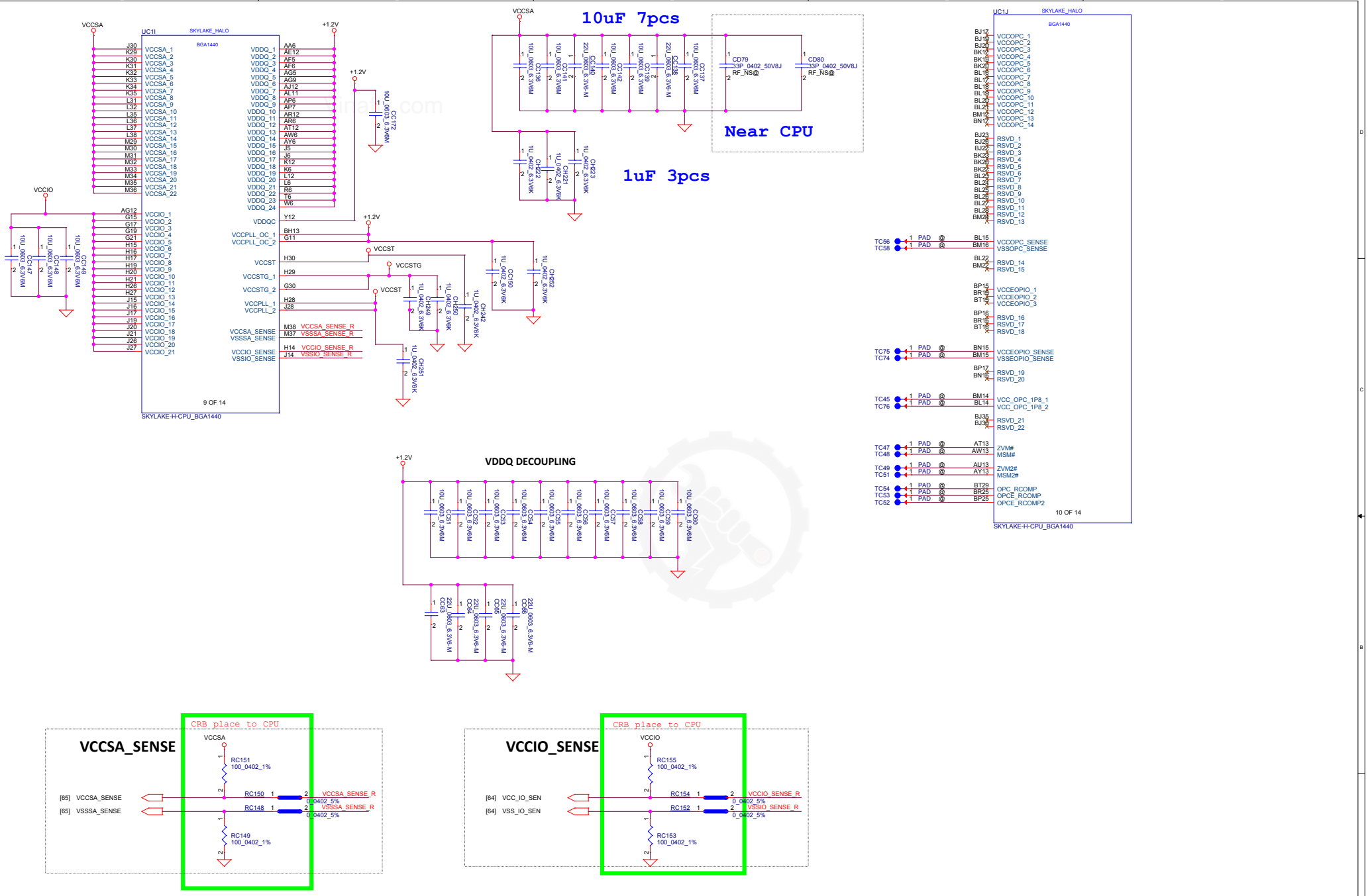
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: CPU (5/7) PWR, BYPASS

Size: D | Document Number: DY510/DY511 N17B-G1 | Rev: 1.0

Date: Monday, December 19, 2016 | Sheet 9 of 75

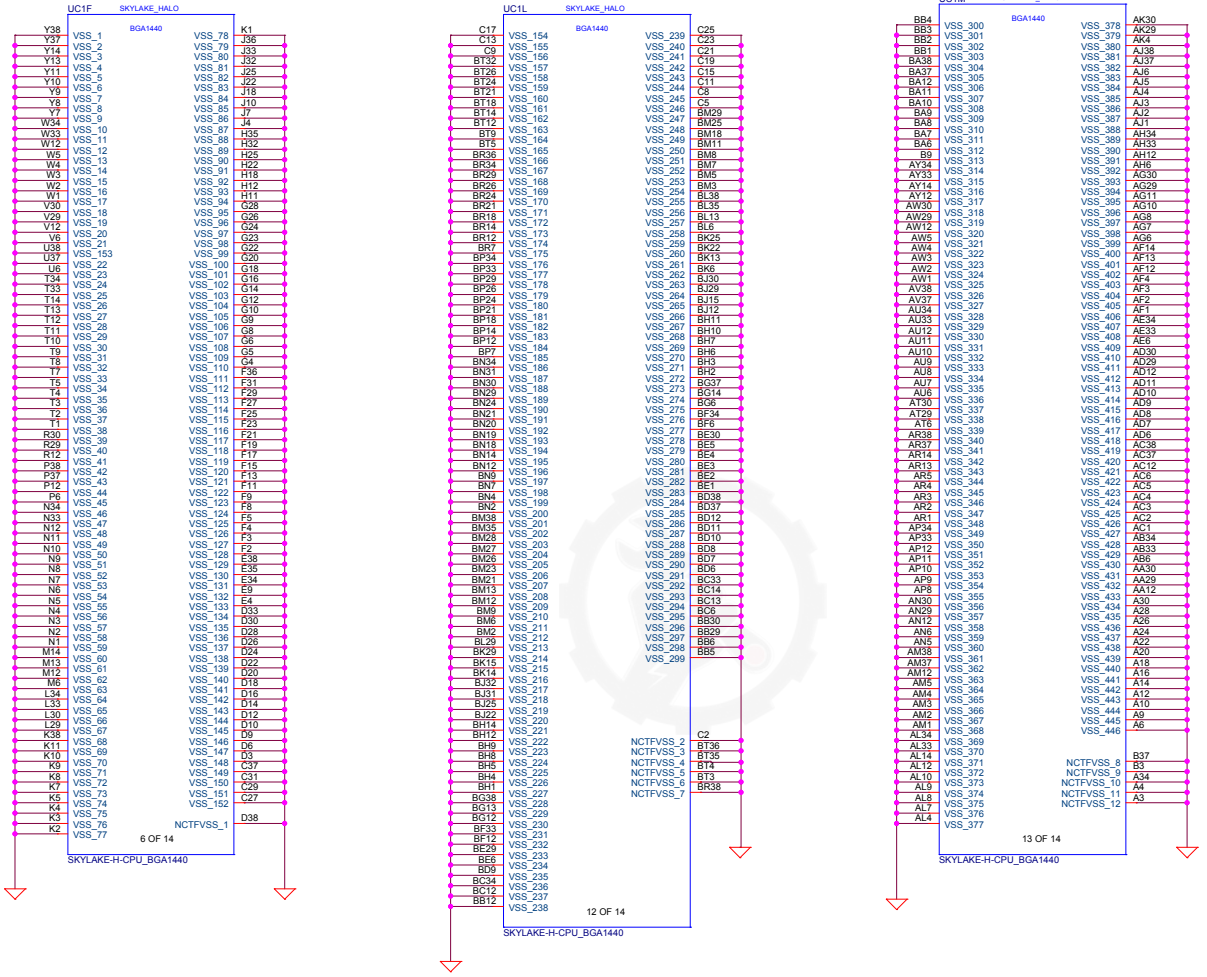


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (6/7) PWR, BYPASS

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 | Sheet 10 of 75



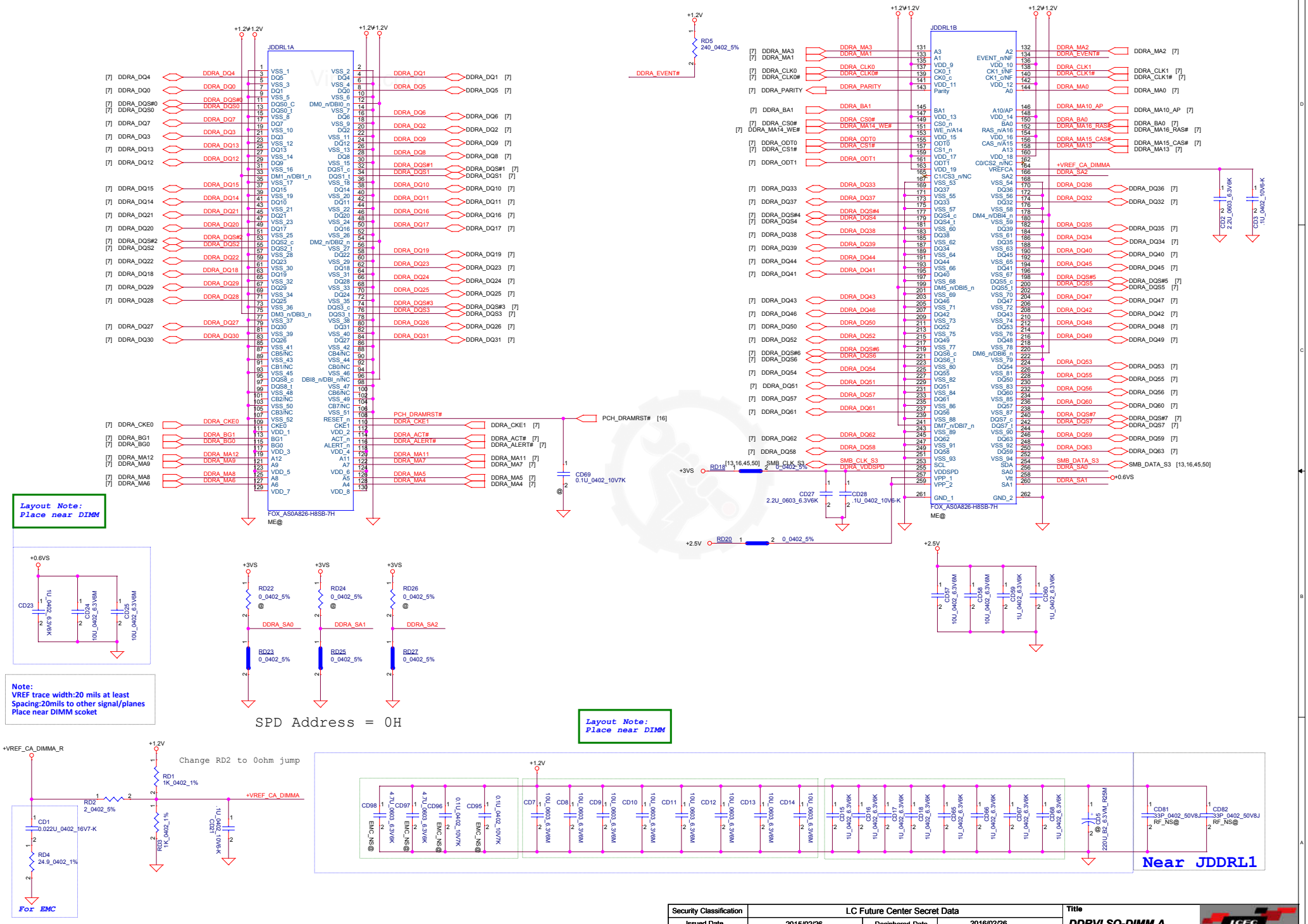
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (6/7) PWR, VSS

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 | Sheet 11 of 75

DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

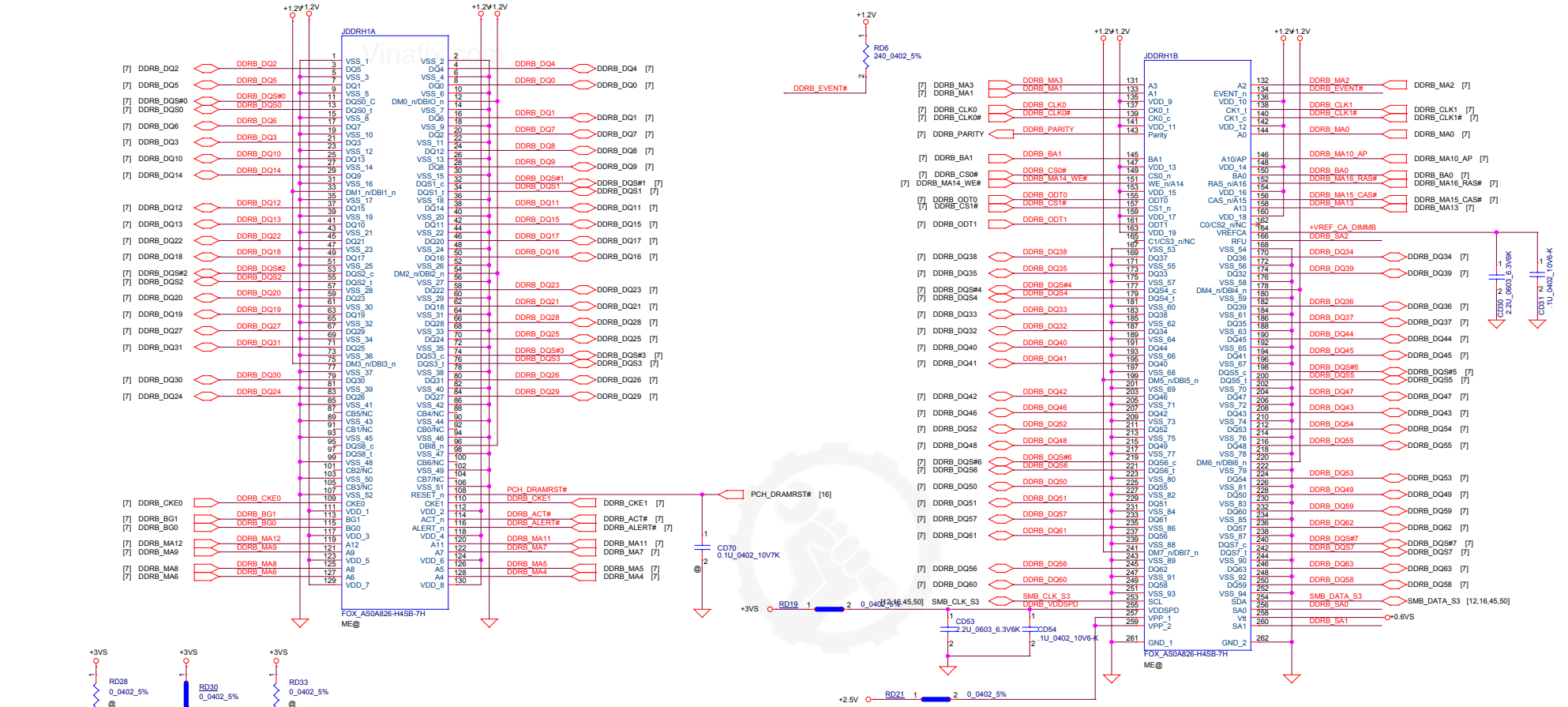
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

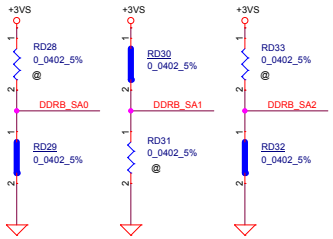
Title: DDRVI SO-DIMM A

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 | Sheet 12 of 75

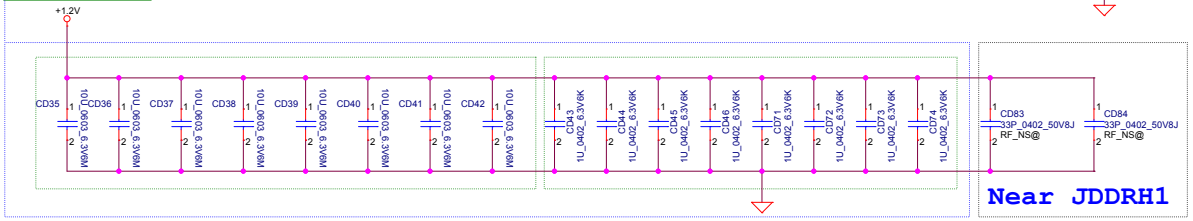
DDR4 SO-DIMM B



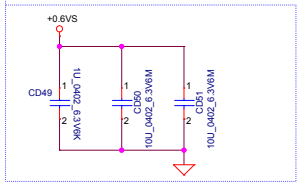


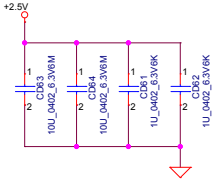
SPD Address = 2H

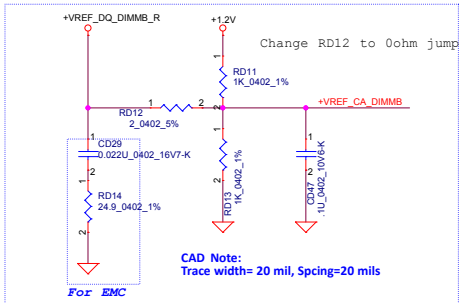
Layout Note:
Place near DIMM



Layout Note:
Place near DIMM

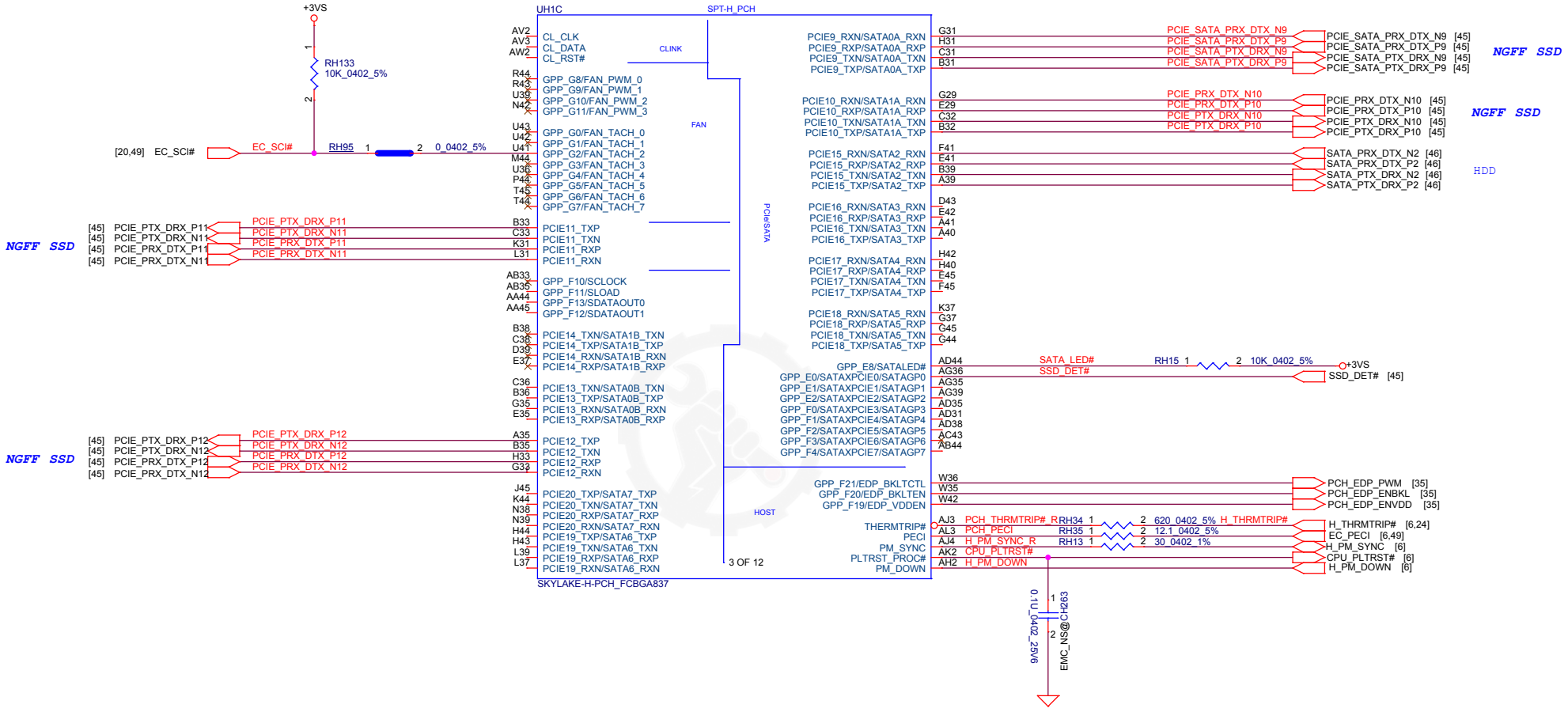






Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	DDRVI SO-DIMM B		
Size C	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 13 of 75		

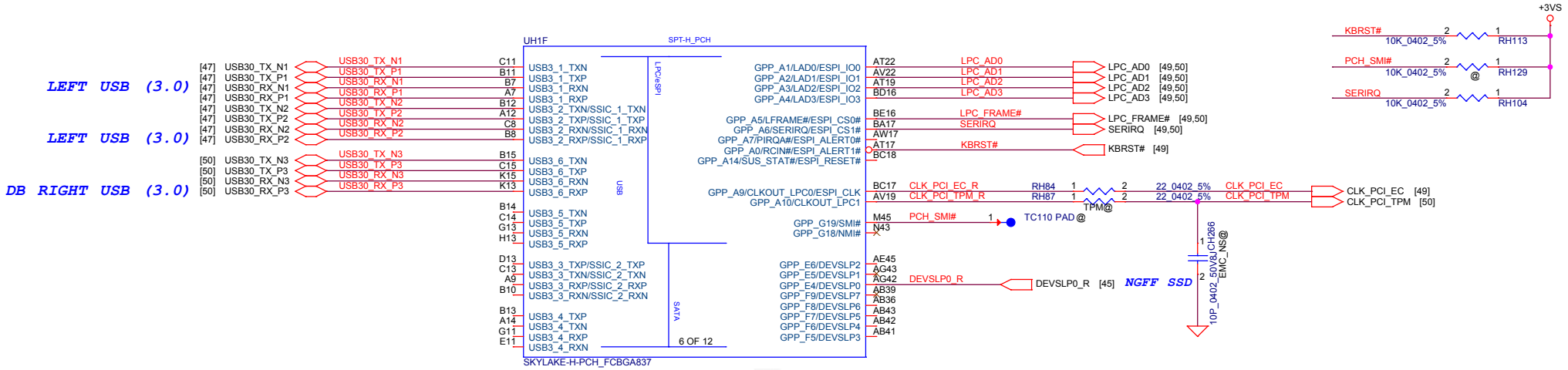


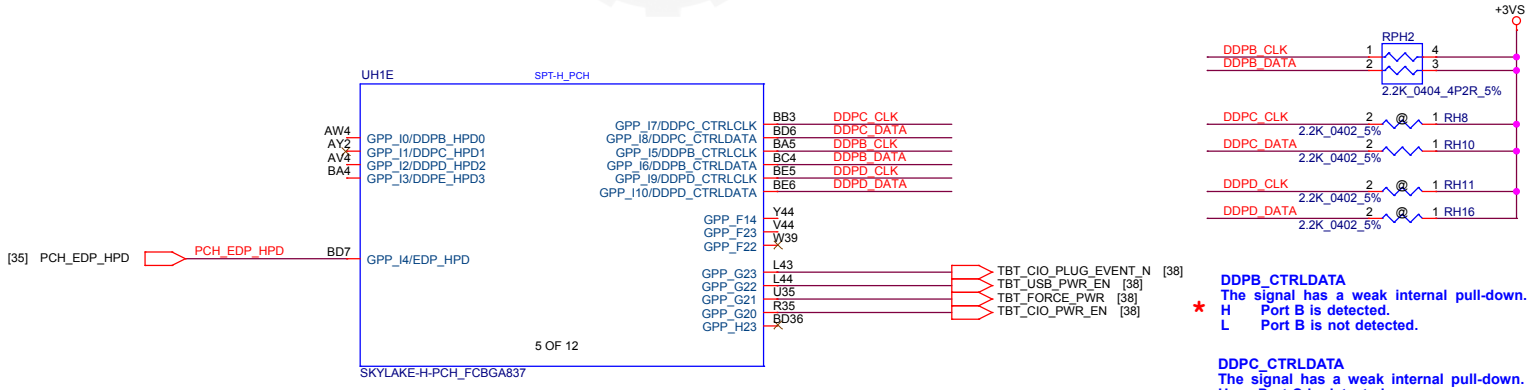
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (1/9) PCIe/SATA/GPPFG

Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 14 of 75





DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
L Port C is not detected. (Default)

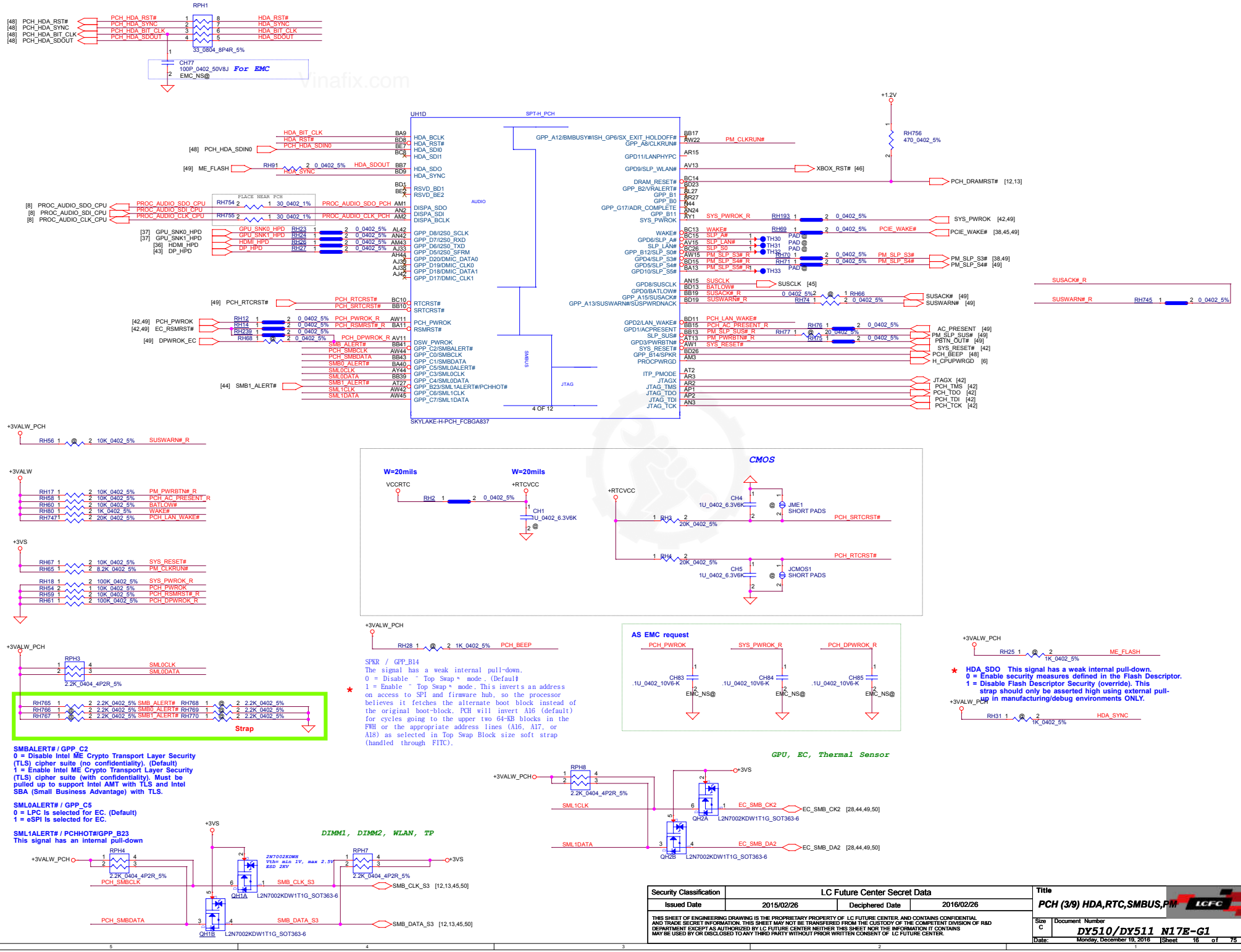
DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
L Port D is not detected. (Default)

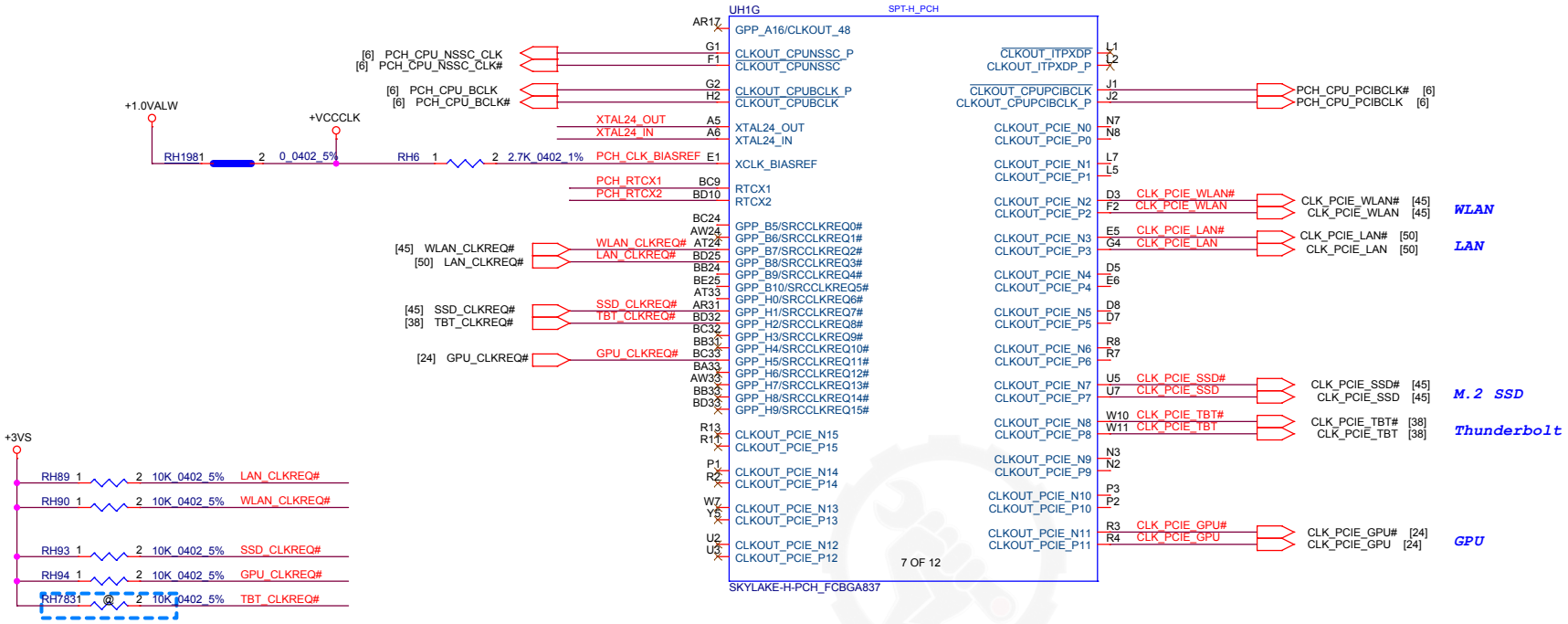
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (2/9) USB3/GPPAEFGHI

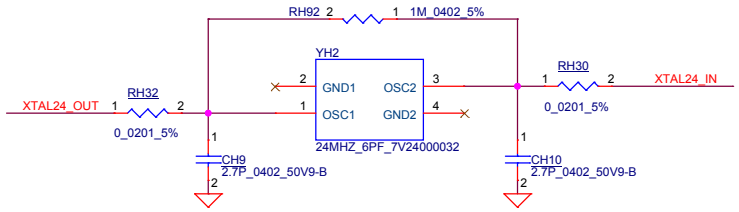
Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

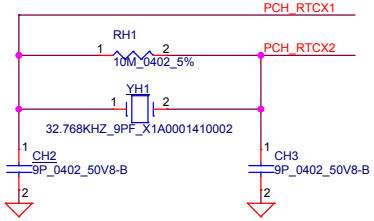
Date: Monday, December 19, 2016 Sheet 15 of 75


RPH1
33_0804_8P4R_5%
CH77
100P_0402_50V8J
For EMC
EMC_NS@
UH1D
SPT-H_PCH
SKYLAKE-H-PCH_FCBGA837
4 OF 12
AUDIO
SMBUS
JTAG
PLACE_NEAR_PCH
RH754
RH755
RH91
RH23
RH24
RH26
RH27
RH12
RH14
RH239
RH68
RH756
470_0402_5%
RH193
RH69
RH70
RH71
RH66
RH74
RH745
RH76
RH77
RH73
RH56
10K_0402_5%
SUSWARN#_R
RH17
RH58
RH60
RH80
RH7471
20K_0402_5%
PM_PWRBTN#_R
PCH_AC_PRESENT_R
BATLOW#
WAKE#
PCH_LAN_WAKE#
RH67
RH65
RH18
RH54
RH59
RH61
8.2K_0402_5%
100K_0402_5%
SYS_RESET#
PM_CLKRUN#
SYS_PWROK_R
PCH_PWROK
PCH_RSMRST#_R
PCH_DPWROK_R
RPH3
2.2K_0404_4P2R_5%
RH765
RH766
RH767
RH768
RH769
RH770
2.2K_0402_5%
SML0CLK
SML0DATA
SMB_ALERT#
SMB0_ALERT#
SMB1_ALERT#
Strap
W=20mils
VCCRTC
RH2
+RTCVCC
CH1
1U_0402_6.3V6K
CMOS
CH4
CH5
JME1
JCMOS1
SHORT PADS
PCH_SRTCRST#
PCH_RTCRST#
RH3
RH4
RH28
PCH_BEEP
SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable " Top Swap " mode. (Default)
1 = Enable " Top Swap " mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).
AS EMC request
PCH_PWROK
SYS_PWROK_R
PCH_DPWROK_R
CH83
CH84
CH85
.1U_0402_10V6-K
EMC_NS@
RH25
ME_FLASH
1K_0402_5%
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
RH31
HDA_SYNC
SMBALERT# / GPP_C2
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
SML0ALERT# / GPP_C5
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.
SML1ALERT# / PCHHOT#/GPP_B23
This signal has an internal pull-down
GPU, EC, Thermal Sensor
RPH8
EC_SMB_CK2
EC_SMB_DA2
QH2A
QH2B
L2N7002KDW1T1G_SOT363-6
DIMM1, DIMM2, WLAN, TP
RPH4
RPH7
QH1A
QH1B
2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV
SMB_CLK_S3
SMB_DATA_S3
PCH_SMBCLK
PCH_SMBDATA
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
PCH (3/9) HDA,RTC,SMBUS,PM
Size
C
Document Number
DY510/DY511 N17E-G1
Rev
1.0
Date:
Monday, December 19, 2016
Sheet
16
of
75



RH783 change to un-stuff-Harry 11/01



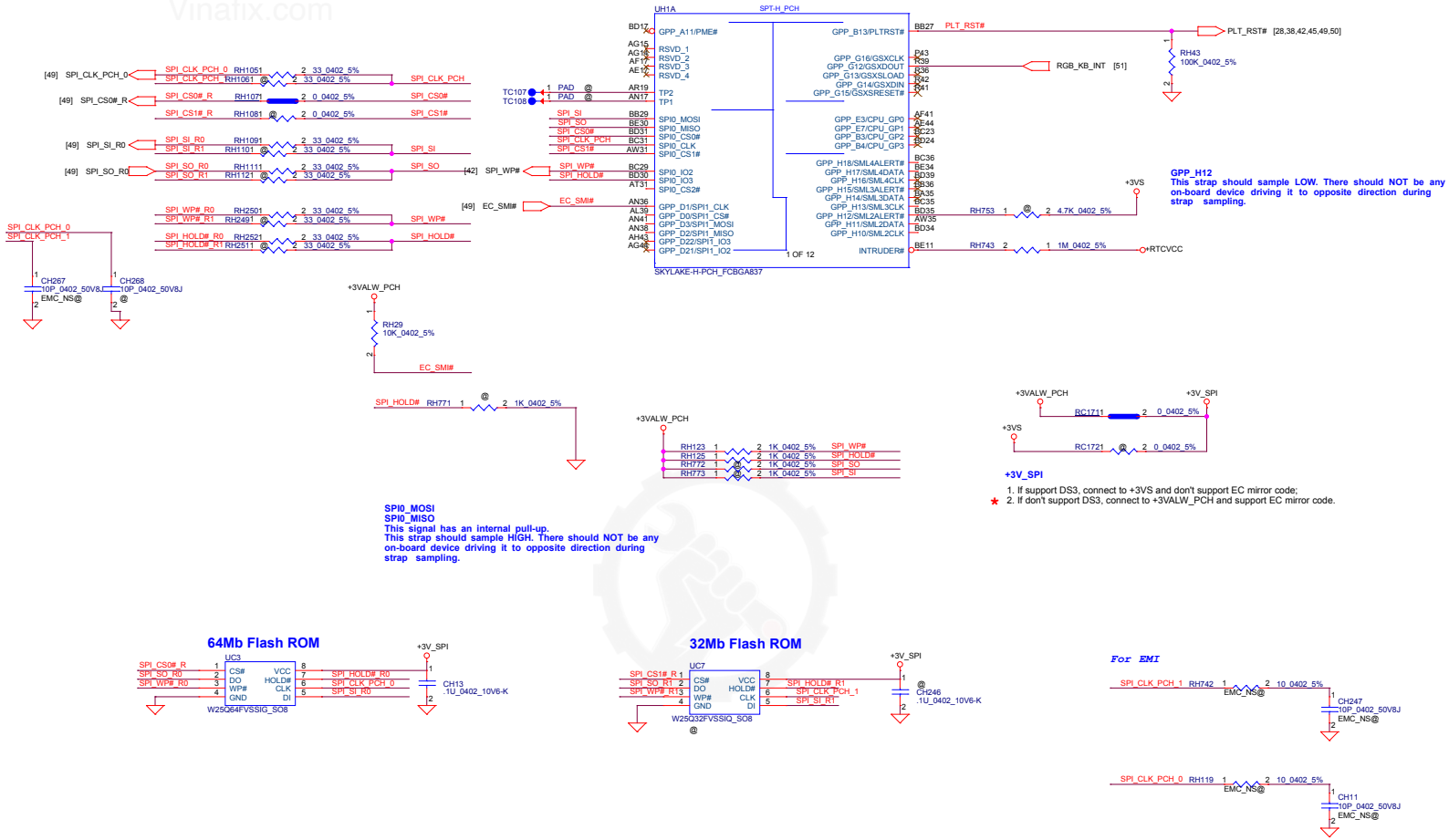


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (3/9) CLOCK,GPPBH

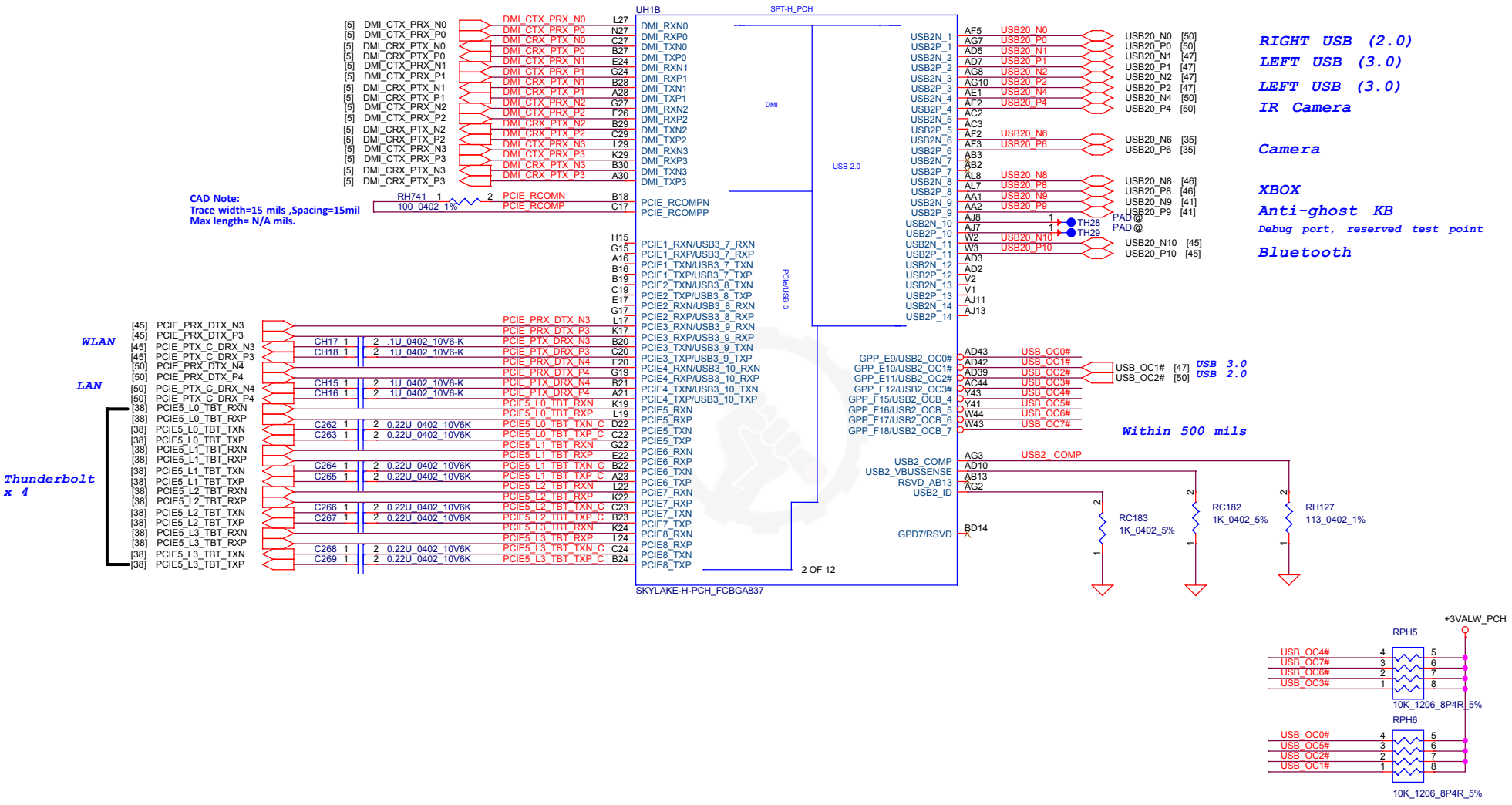
Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 17 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (5/9) SPI,SMBUS,GPPBEGH		
Size A2	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 18 of 75		

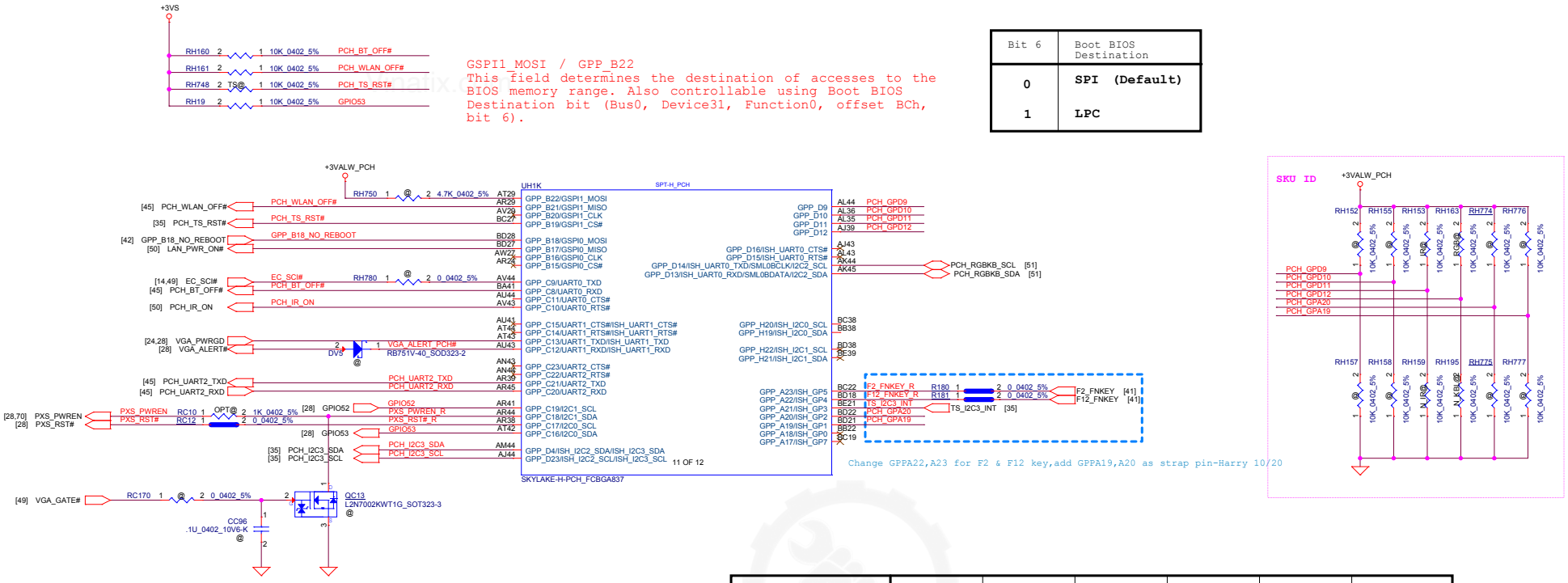


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (5/9) DMI, PCIe, USB2, G

Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 19 of 75



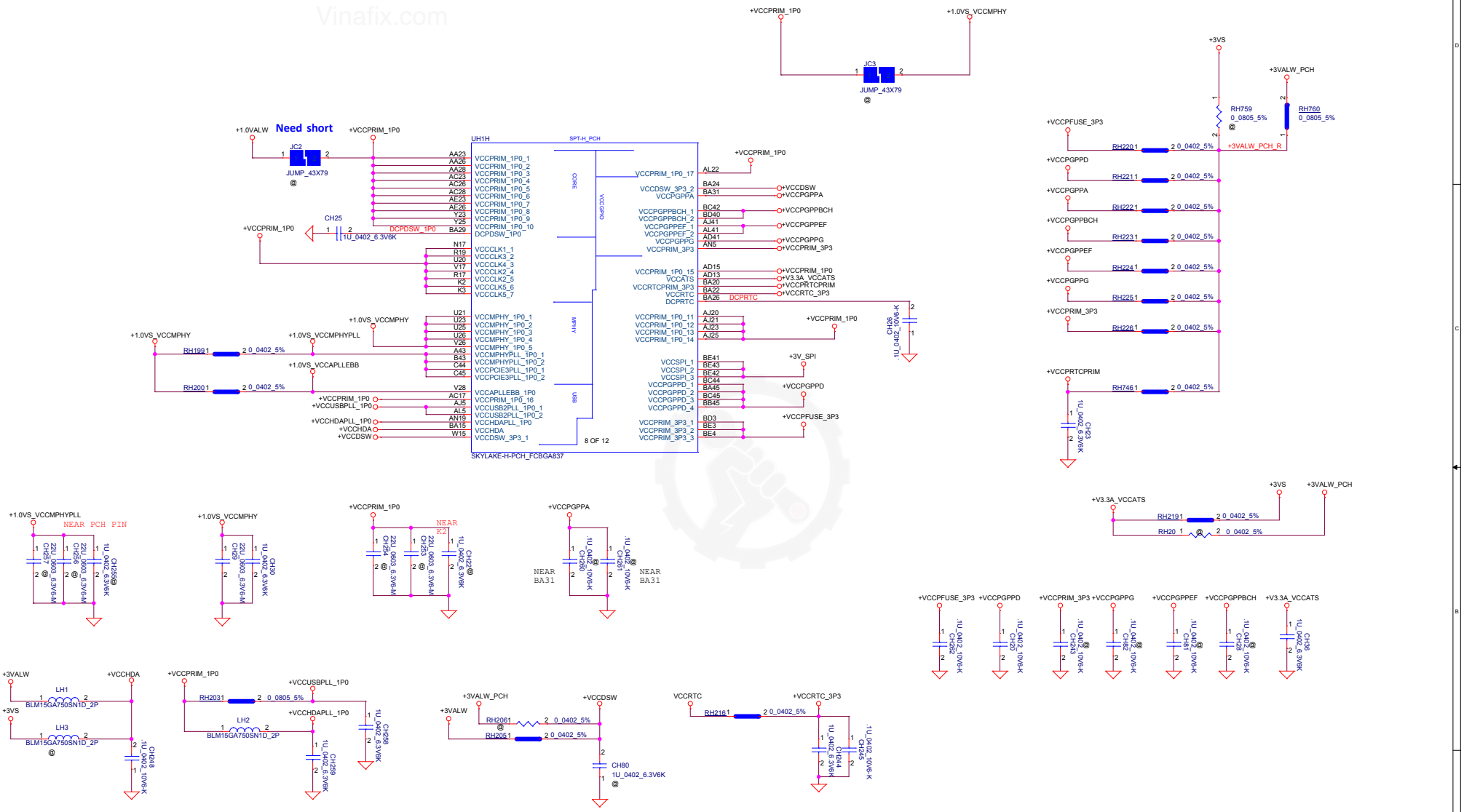
Function	PCH_GPD9	PCH_GPD10	PCH_GPD11	PCH_GPD12	PCH_GPA19	PCH_GPA20
Optane Memory	0	X	X	X	X	X
non-touch	X	1	X	X	X	X
touch	X	0	X	X	X	X
IR Camera	X	X	1	X	X	X
Normal Camera	X	X	0	X	X	X
RGB BL KB	X	X	X	1	X	X
Red BL KB	X	X	X	0	X	X

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 20 of 75

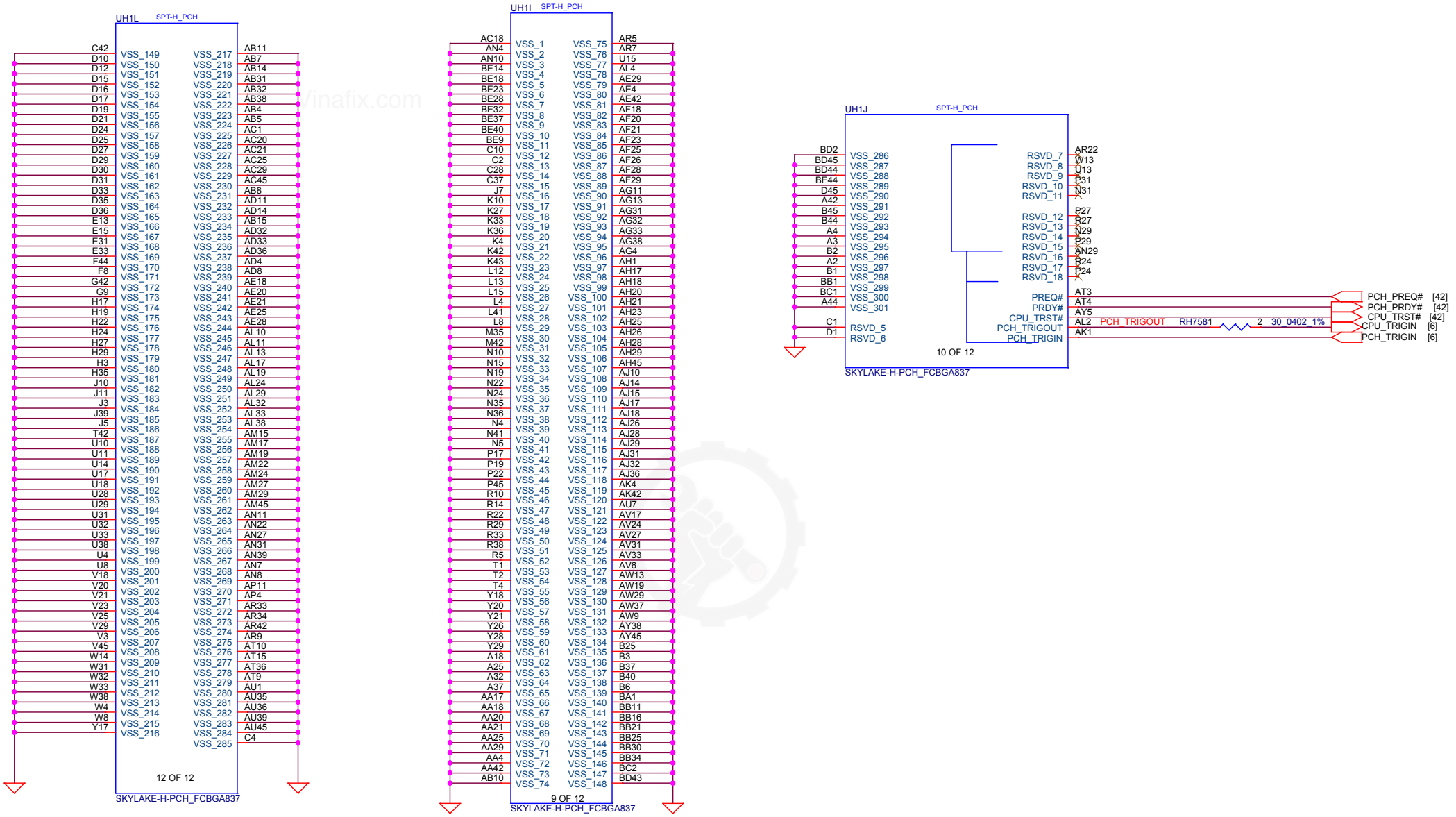


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (7/9) PWR

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 | Sheet 21 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
B	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 22 of 75

N17E-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control	(100K pull Down)
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

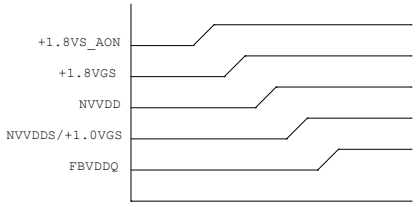
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17E-G1 Power Sequence

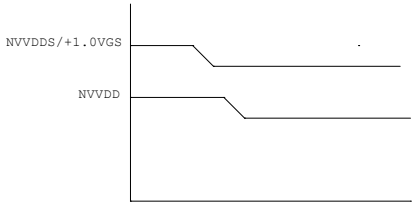


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

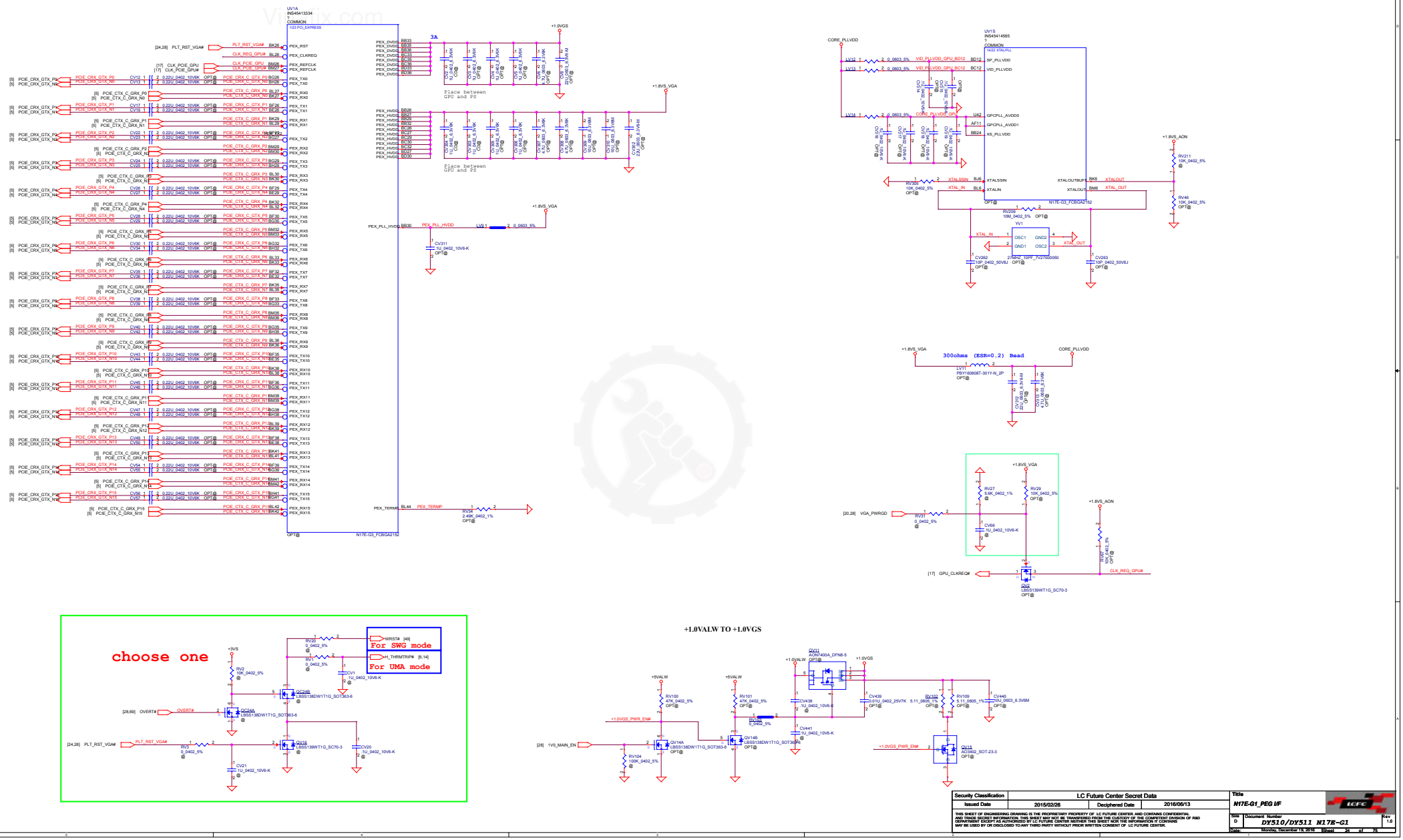
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: VGA Notes List

Size: C | Document Number: DY510/DY511 N17E-G1 | Rev: 1.0

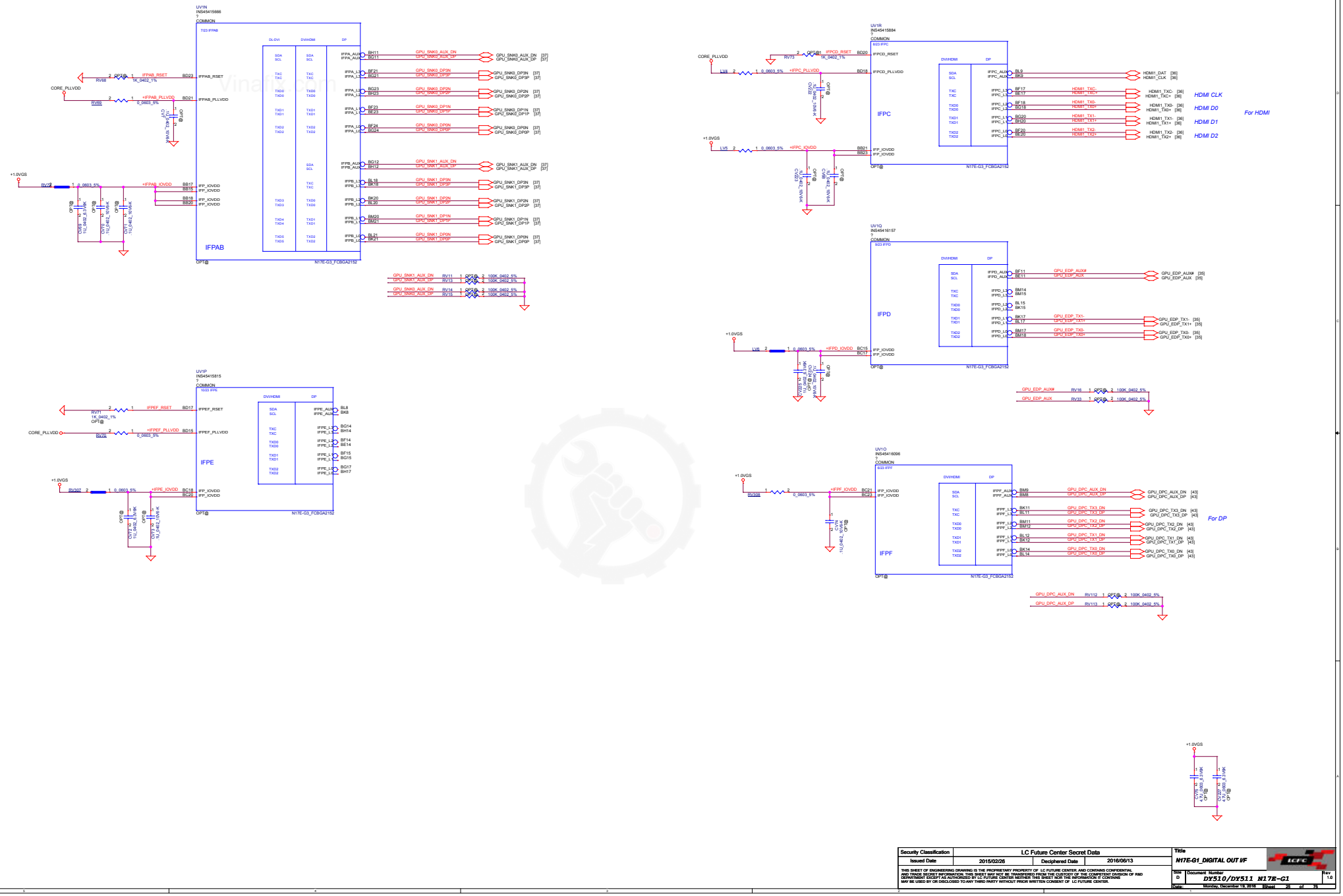
Date: Monday, December 19, 2016 | Sheet 23 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

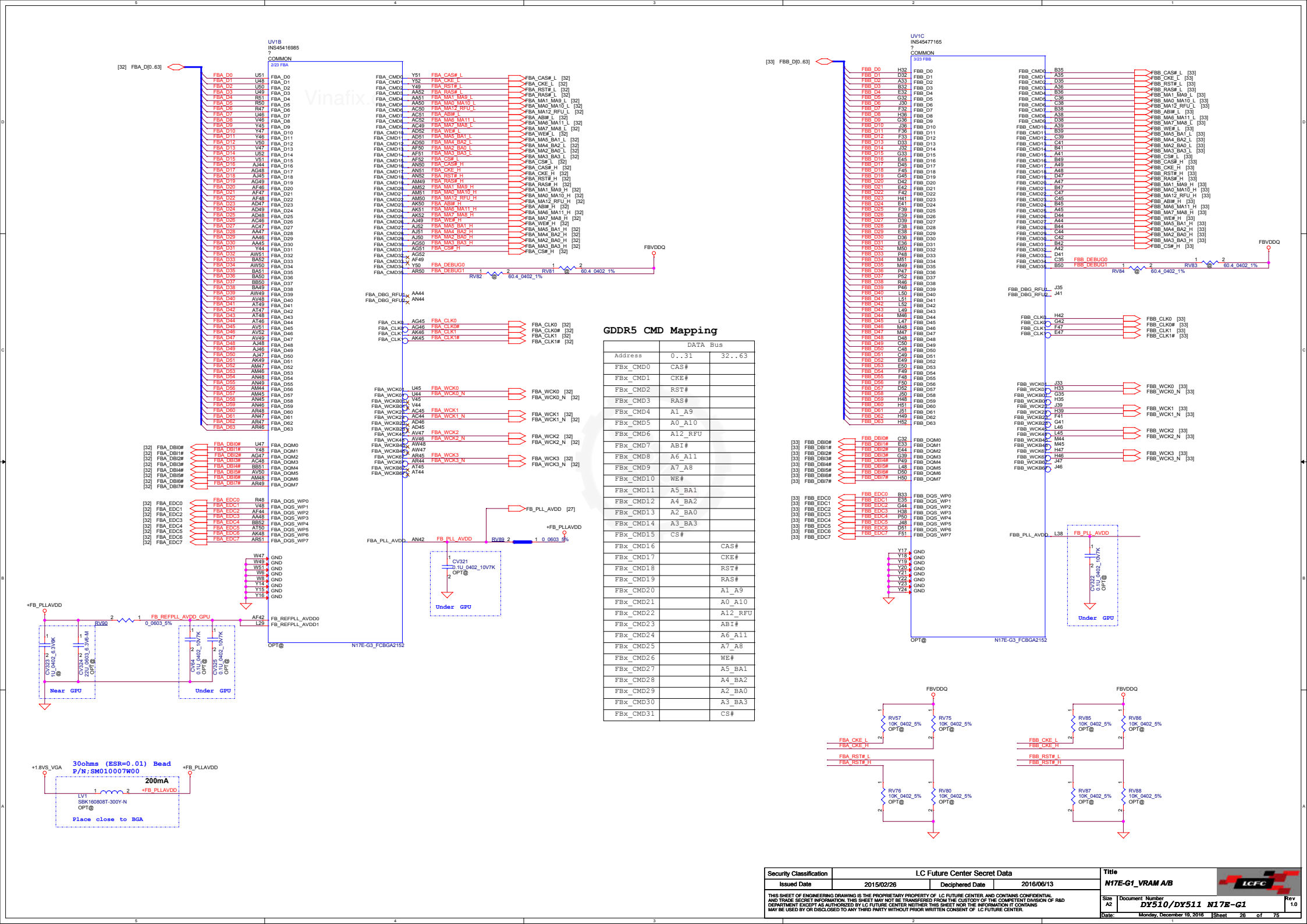
Title	N17E-G1_PEG I/F		
Size D	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 24 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	N17E-G1_DIGITAL OUT I/F
Size	D
Document Number	DY510/DY511 N17E-G1
Rev	1.0
Date	Monday, December 19, 2016
Sheet	25 of 75

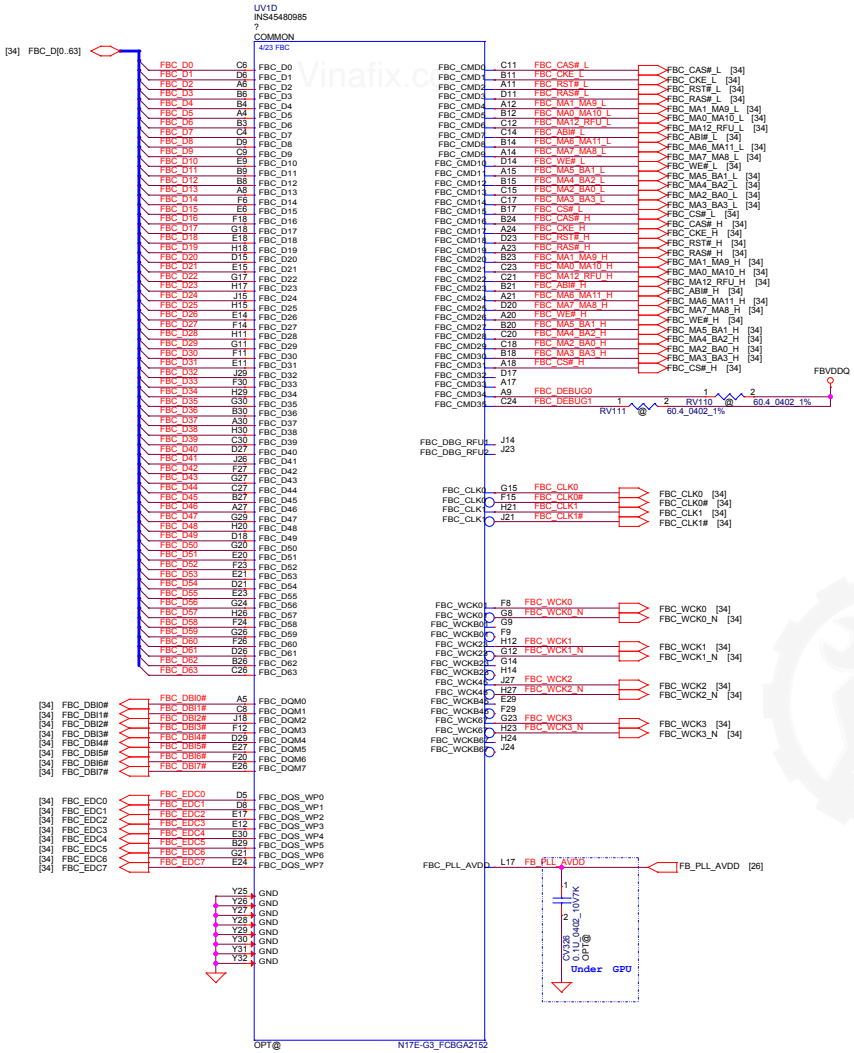


GDDR5 CMD Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CAS#	
FBx_CMD1	CKE#	
FBx_CMD2	RST#	
FBx_CMD3	RAS#	
FBx_CMD4	A1_A9	
FBx_CMD5	A0_A10	
FBx_CMD6	A12_RFU	
FBx_CMD7	ABI#	
FBx_CMD8	A6_A11	
FBx_CMD9	A7_A8	
FBx_CMD10	WE#	
FBx_CMD11	A5_BA1	
FBx_CMD12	A4_BA2	
FBx_CMD13	A2_BA0	
FBx_CMD14	A3_BA3	
FBx_CMD15	CS#	
FBx_CMD16		CAS#
FBx_CMD17		CKE#
FBx_CMD18		RST#
FBx_CMD19		RAS#
FBx_CMD20		A1_A9
FBx_CMD21		A0_A10
FBx_CMD22		A12_RFU
FBx_CMD23		ABI#
FBx_CMD24		A6_A11
FBx_CMD25		A7_A8
FBx_CMD26		WE#
FBx_CMD27		A5_BA1
FBx_CMD28		A4_BA2
FBx_CMD29		A2_BA0
FBx_CMD30		A3_BA3
FBx_CMD31		CS#

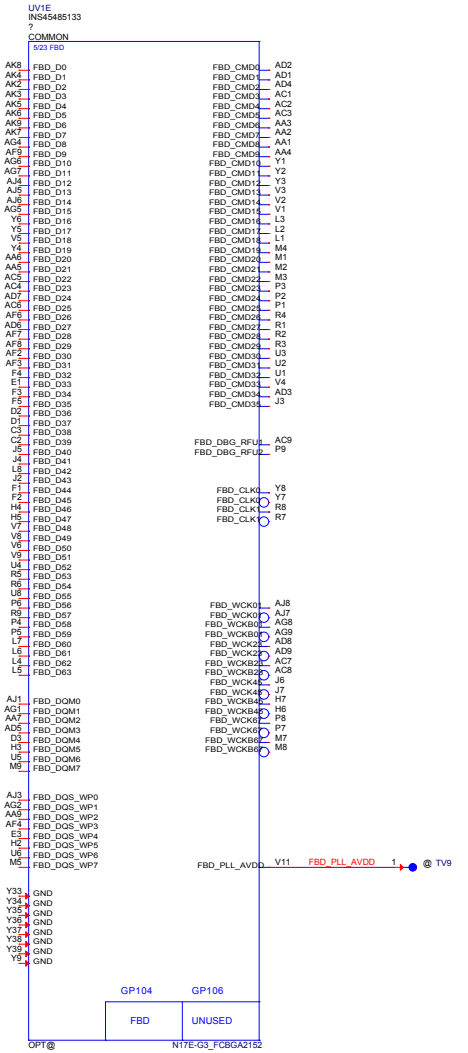
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

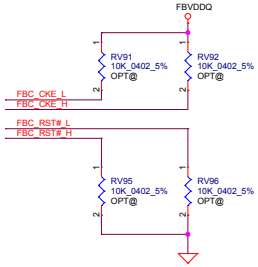
Title	N17E-G1_VRAM A/B		
Size A2	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 26 of 75		



GDDR5 CMD Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CAS#	
FBx_CMD1	CKE#	
FBx_CMD2	RST#	
FBx_CMD3	RAS#	
FBx_CMD4	A1_A9	
FBx_CMD5	A0_A10	
FBx_CMD6	A12_RFU	
FBx_CMD7	ABI#	
FBx_CMD8	A6_A11	
FBx_CMD9	A7_A8	
FBx_CMD10	WE#	
FBx_CMD11	A5_BA1	
FBx_CMD12	A4_BA2	
FBx_CMD13	A2_BA0	
FBx_CMD14	A3_BA3	
FBx_CMD15	CS#	
FBx_CMD16		CAS#
FBx_CMD17		CKE#
FBx_CMD18		RST#
FBx_CMD19		RAS#
FBx_CMD20		A1_A9
FBx_CMD21		A0_A10
FBx_CMD22		A12_RFU
FBx_CMD23		ABI#
FBx_CMD24		A6_A11
FBx_CMD25		A7_A8
FBx_CMD26		WE#
FBx_CMD27		A5_BA1
FBx_CMD28		A4_BA2
FBx_CMD29		A2_BA0
FBx_CMD30		A3_BA3
FBx_CMD31		CS#



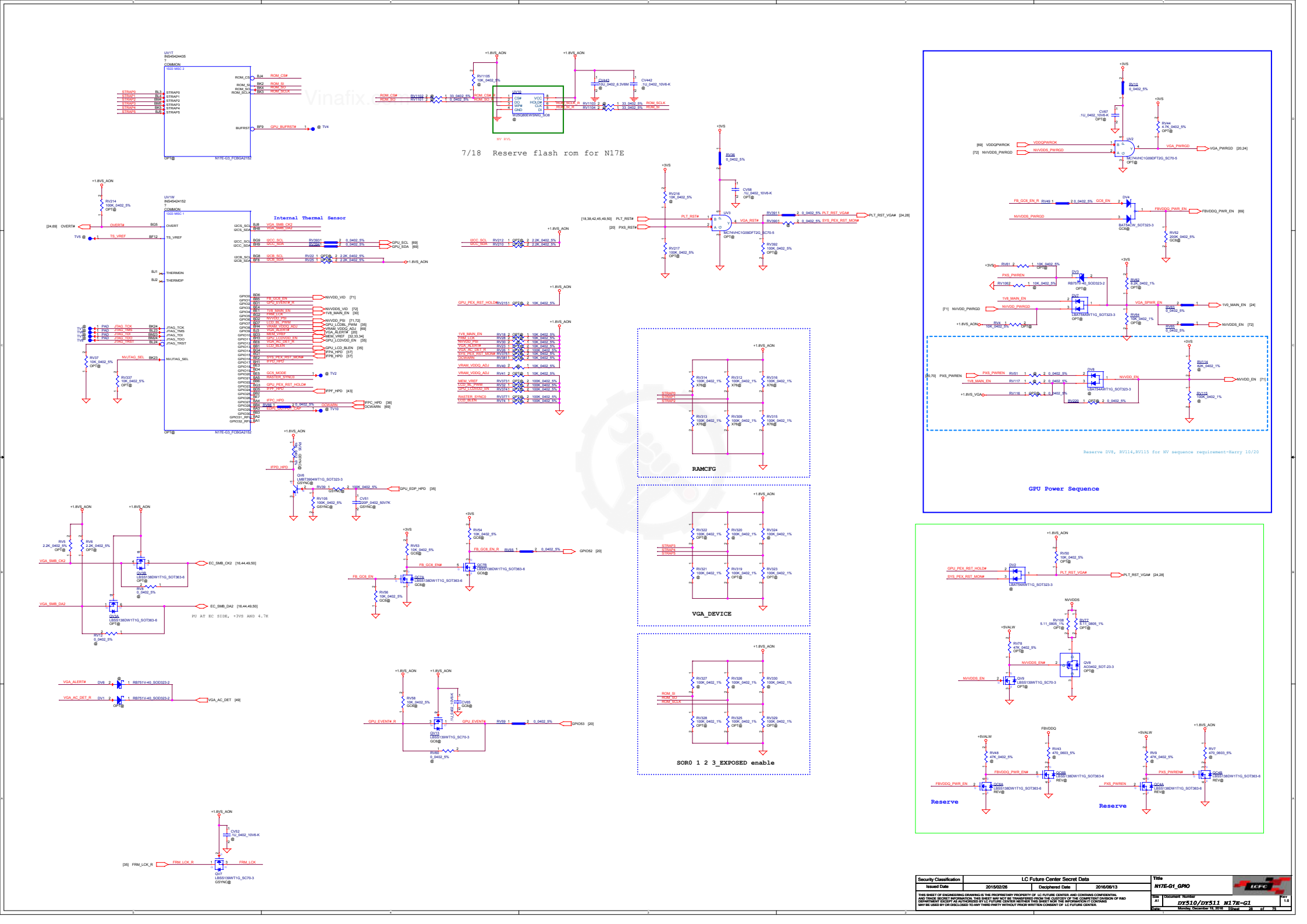


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *N17E-G1_VRAM C/D*

Size	Document Number	Rev
A2	*DY510/DY511 N17E-G1*	1.0

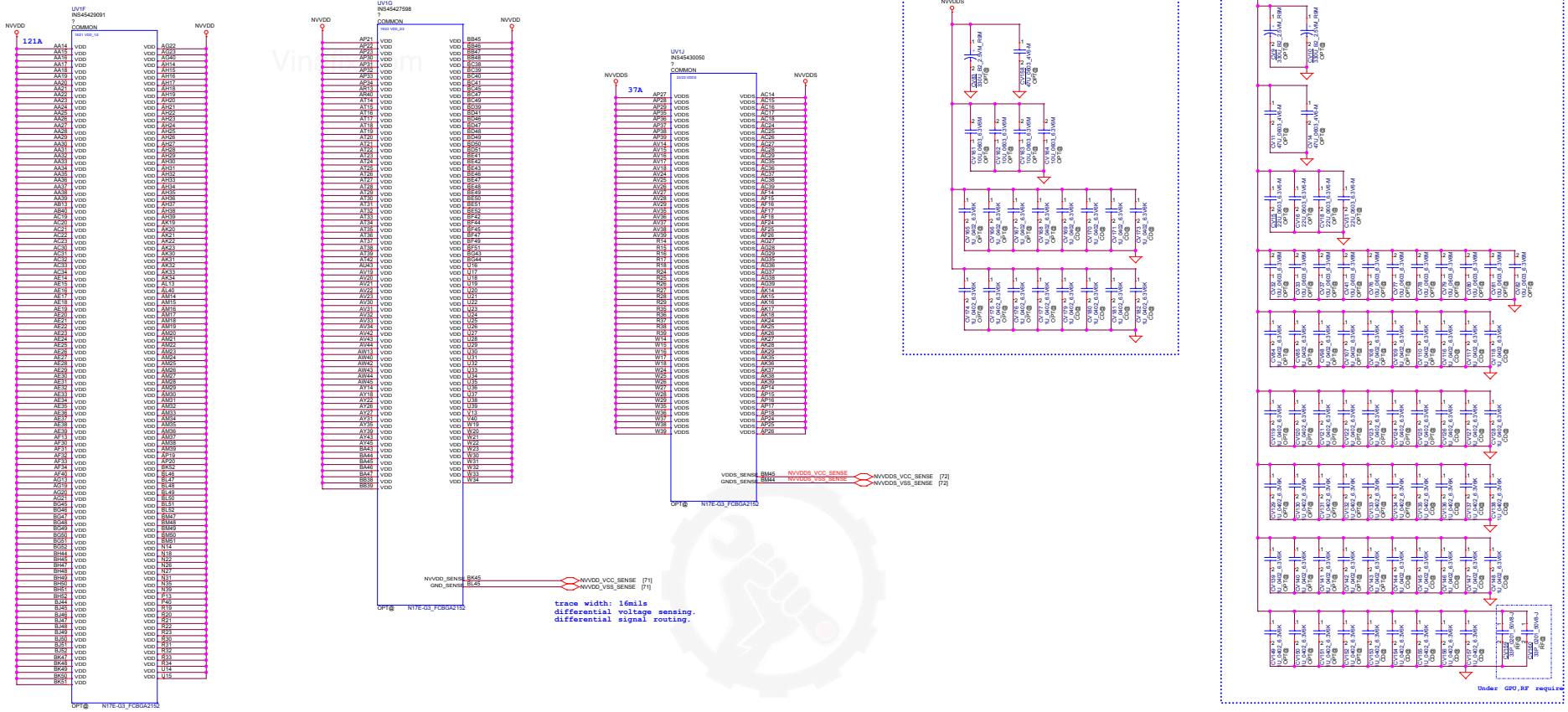
Date: Monday, December 19, 2016 Sheet 27 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

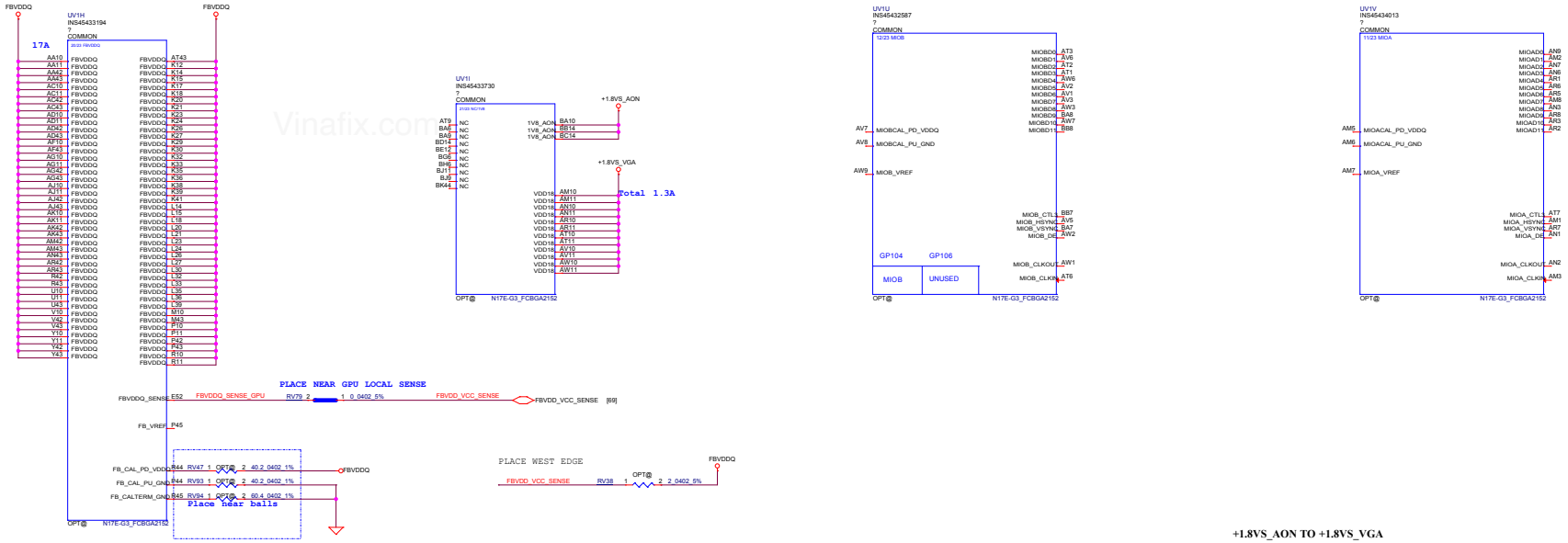
Title	N17E-G1_GPIO
Size	A1
Document Number	DY510/DY511 N17E-G1
Rev	1.0
Date	Monday, December 19, 2016
Sheet	28 of 75

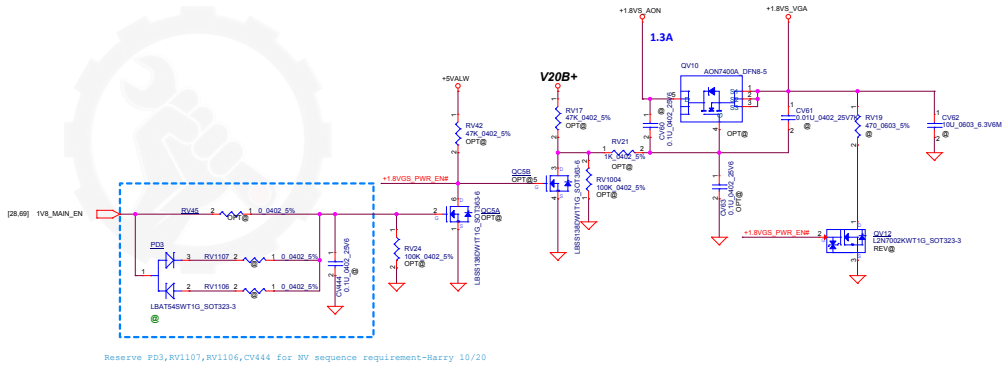


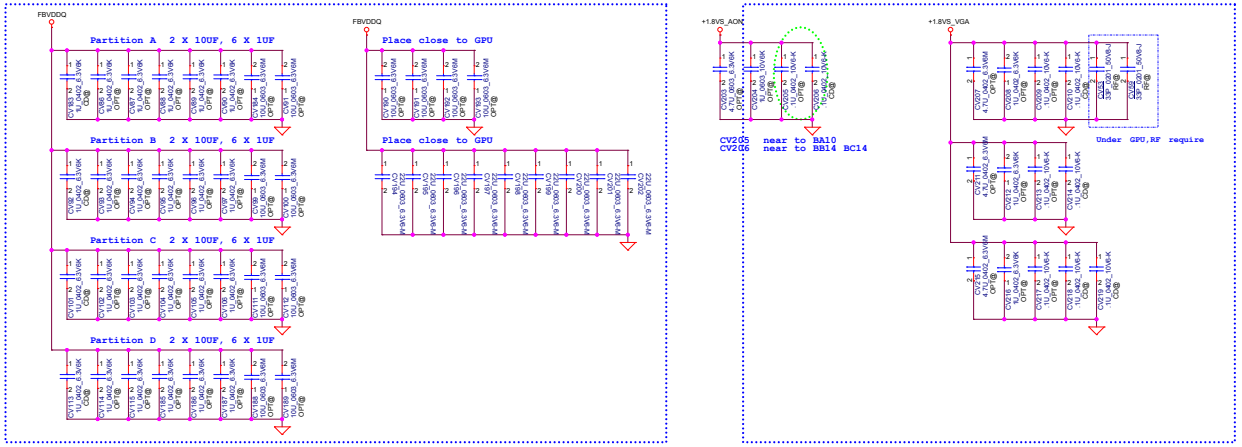
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: **N17E-G1_POWER CORE**

Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0
Date: Monday, December 19, 2016	Sheet 29 of 75	







Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

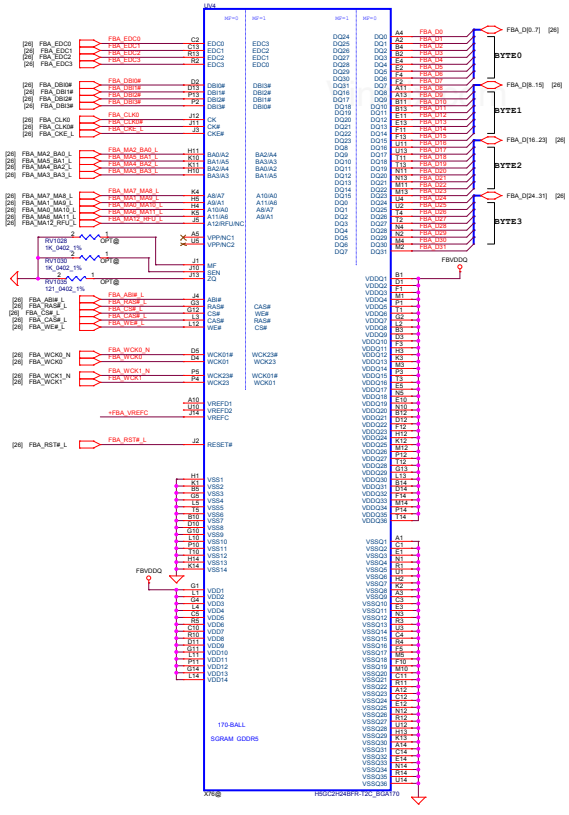
Title	N17E-G1_POWER VDDQ		
Size	Document Number		Rev
Custom	DX510/DY511 N17E-G1		1.0
Date:	Monday, December 19, 2016	Sheet	30 of 75

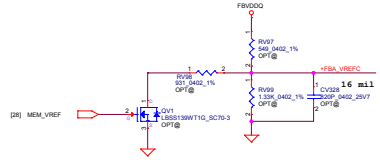
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

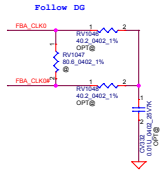
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D EXCEPT AS AUTHORIZED BY LC FUTURE CENTER MANAGEMENT. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

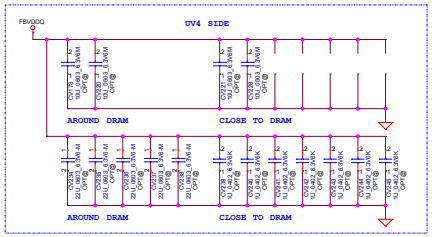
Title	N17E-G1_GND		
Size	Document Number		Rev
Custom	DY510/DY511 N17E-G1		1.0
Date:	Monday, December 19, 2016	Sheet 31 of 75	

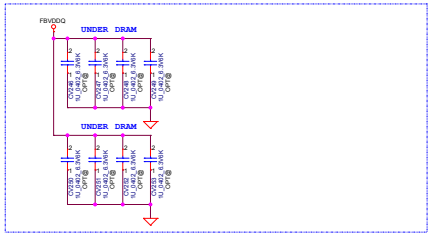
Memory - Lower 32 bits



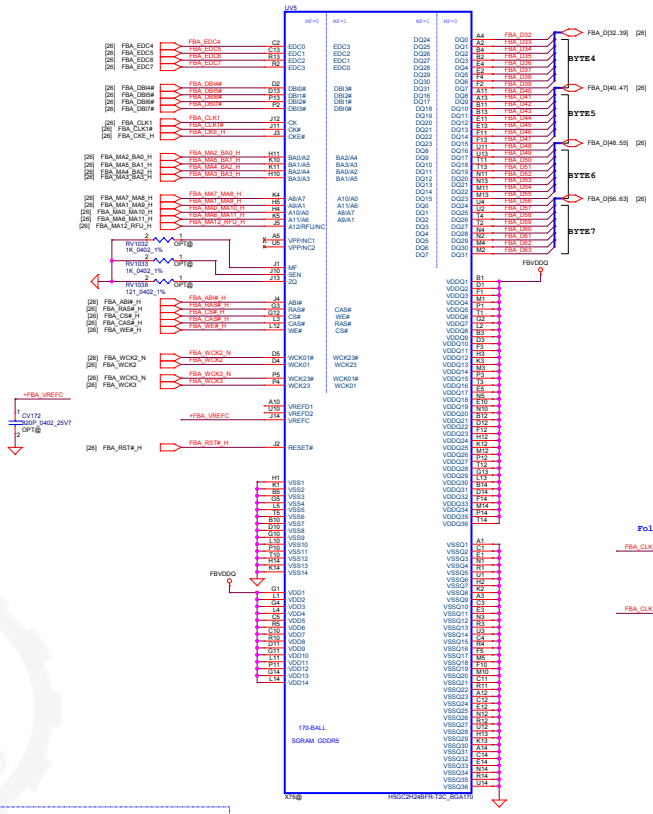


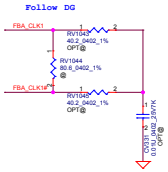


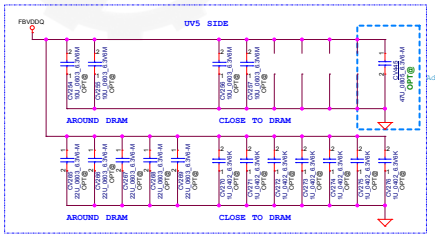


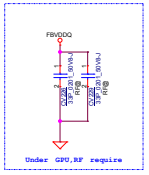


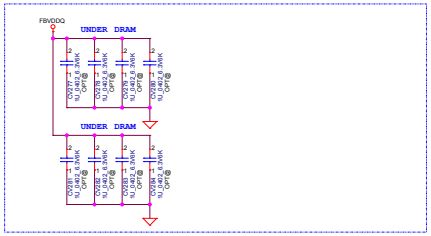
Memory - Upper 32 bits







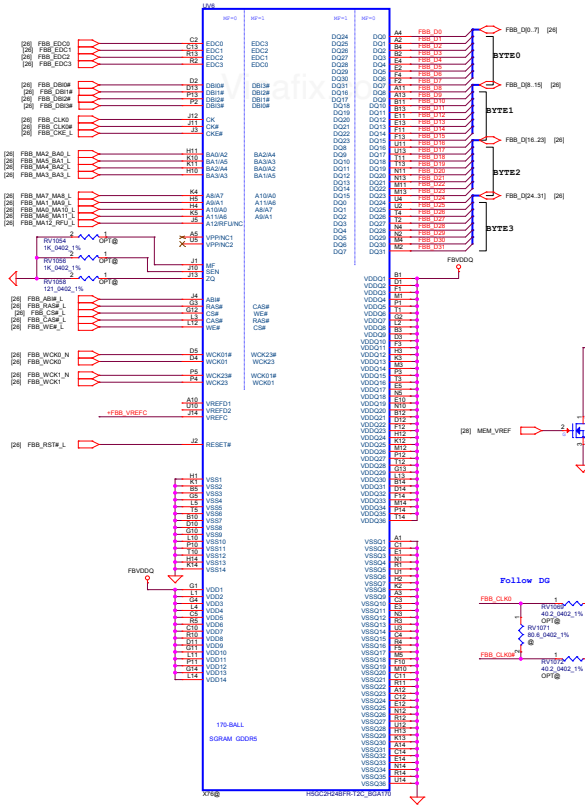


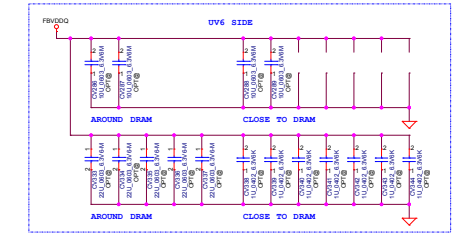


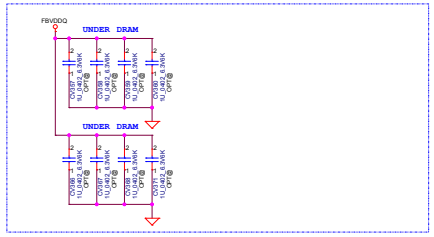
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title	N17E-G1_VRAM A		
Size	Document Number		Rev
D	DY510/DY511 N17E-G1		1.0
Date: Monday, December 19, 2016	Sheet 32 of 75		

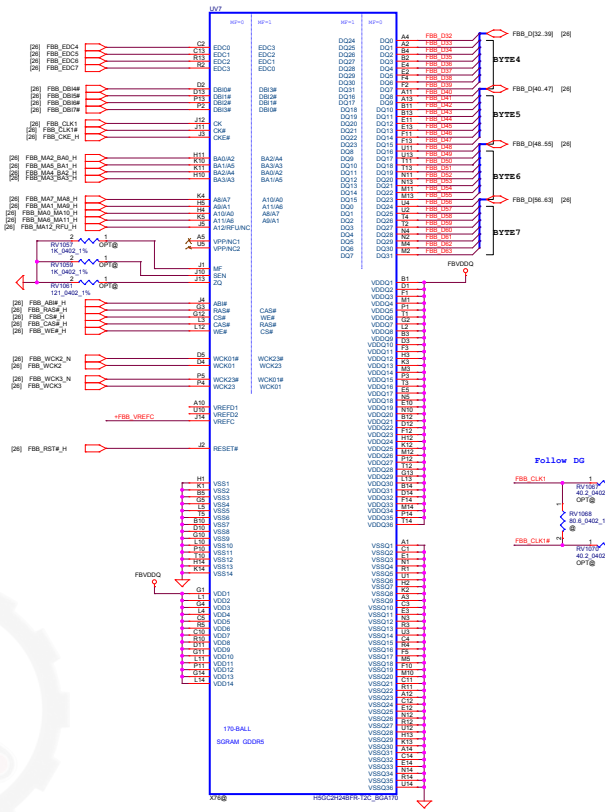
Memory - Lower 32 bits

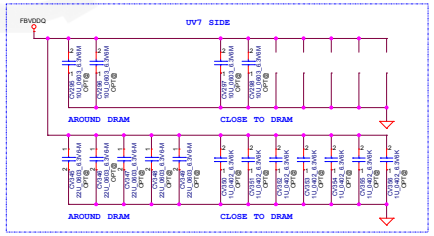


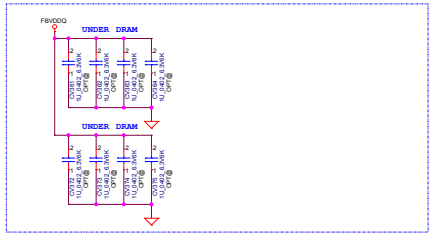




Memory - Upper 32 bits







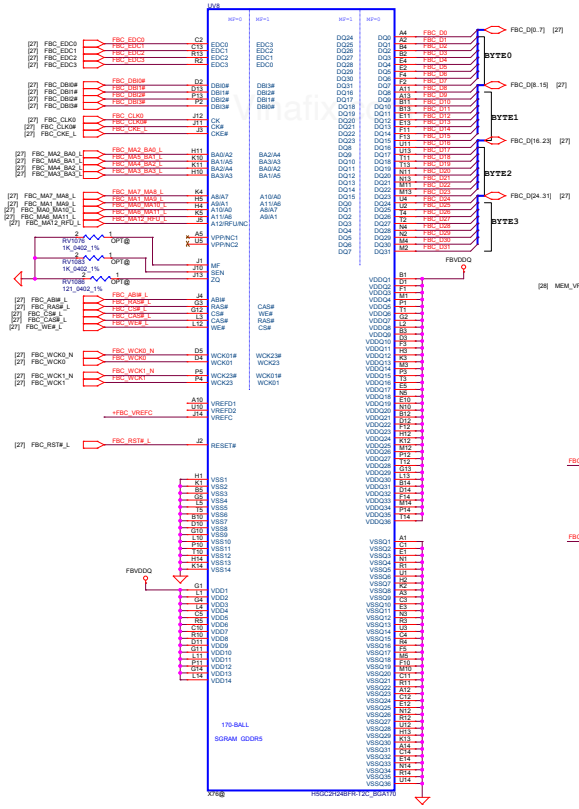
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

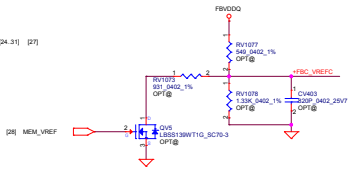
Title: N17E-G1_VRAM B

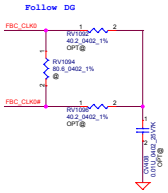
Size: D | Document Number: DY510/DY511 N17E-G1 | Rev: 1.0

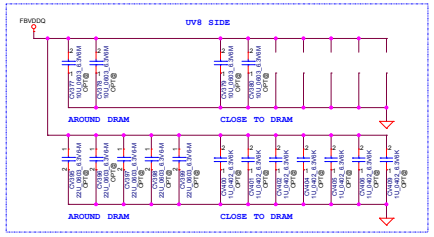
Date: Monday, December 19, 2016 | Sheet 33 of 75

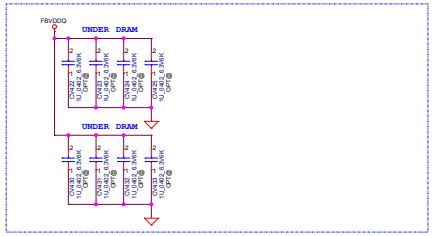
Memory Partition C - Lower 32 bits



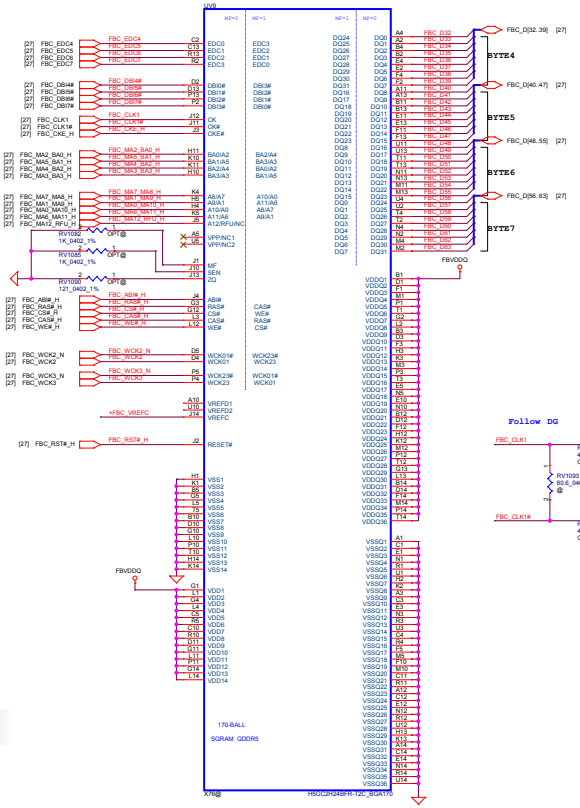


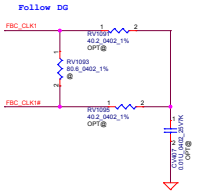


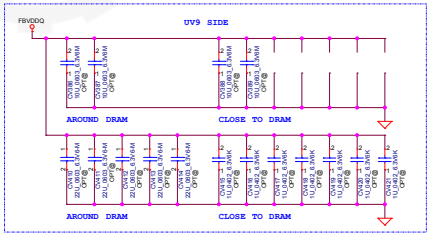


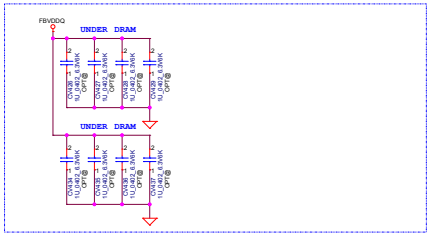


Memory Partition C - Upper 32 bits







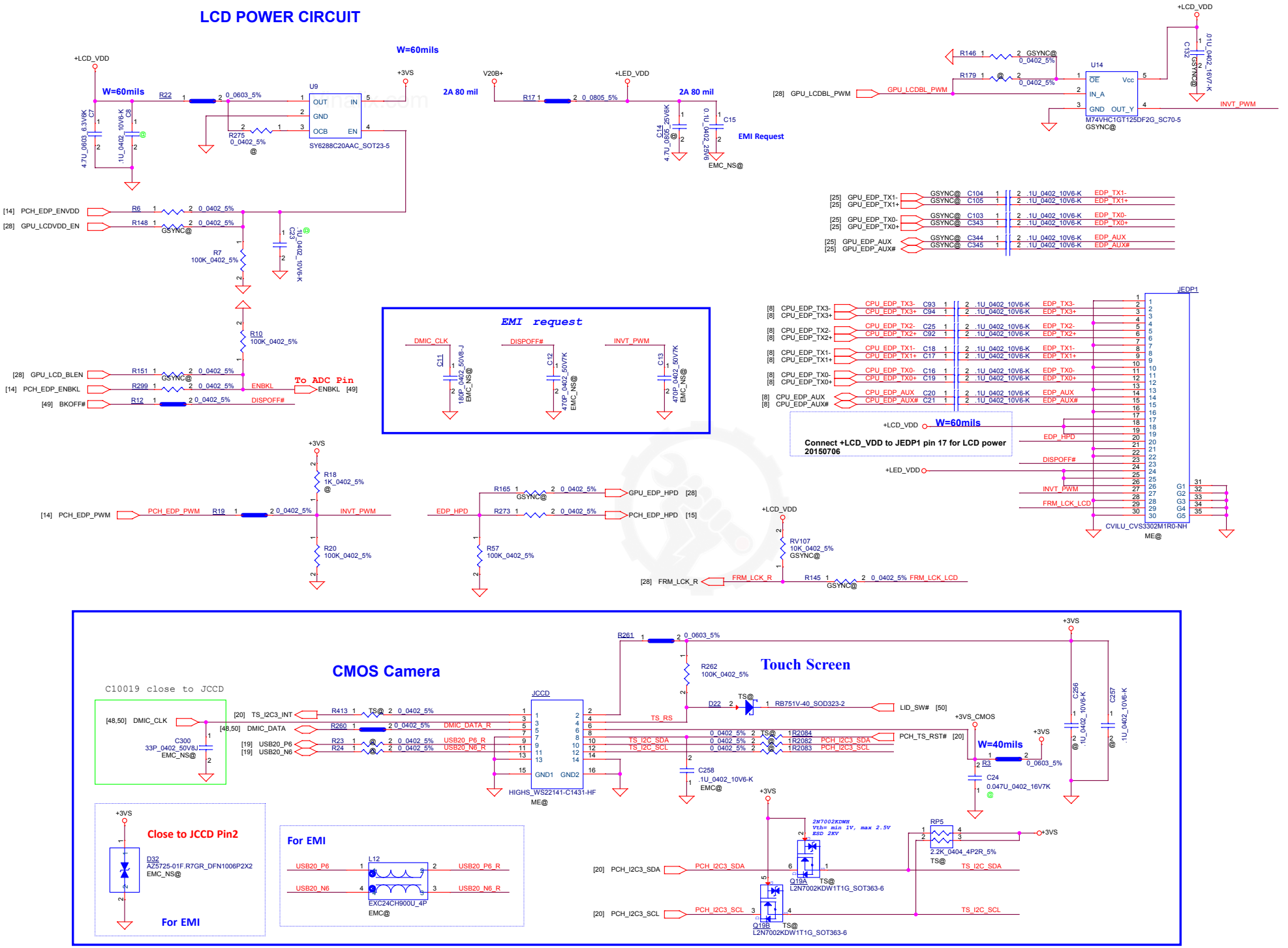


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	N17E-G1_VRAM C	
Size D	Document Number DY510/DY511 N17E-G1	Rev 1.0
Date: Monday, December 19, 2016	Sheet 34 of 75	

LCD POWER CIRCUIT

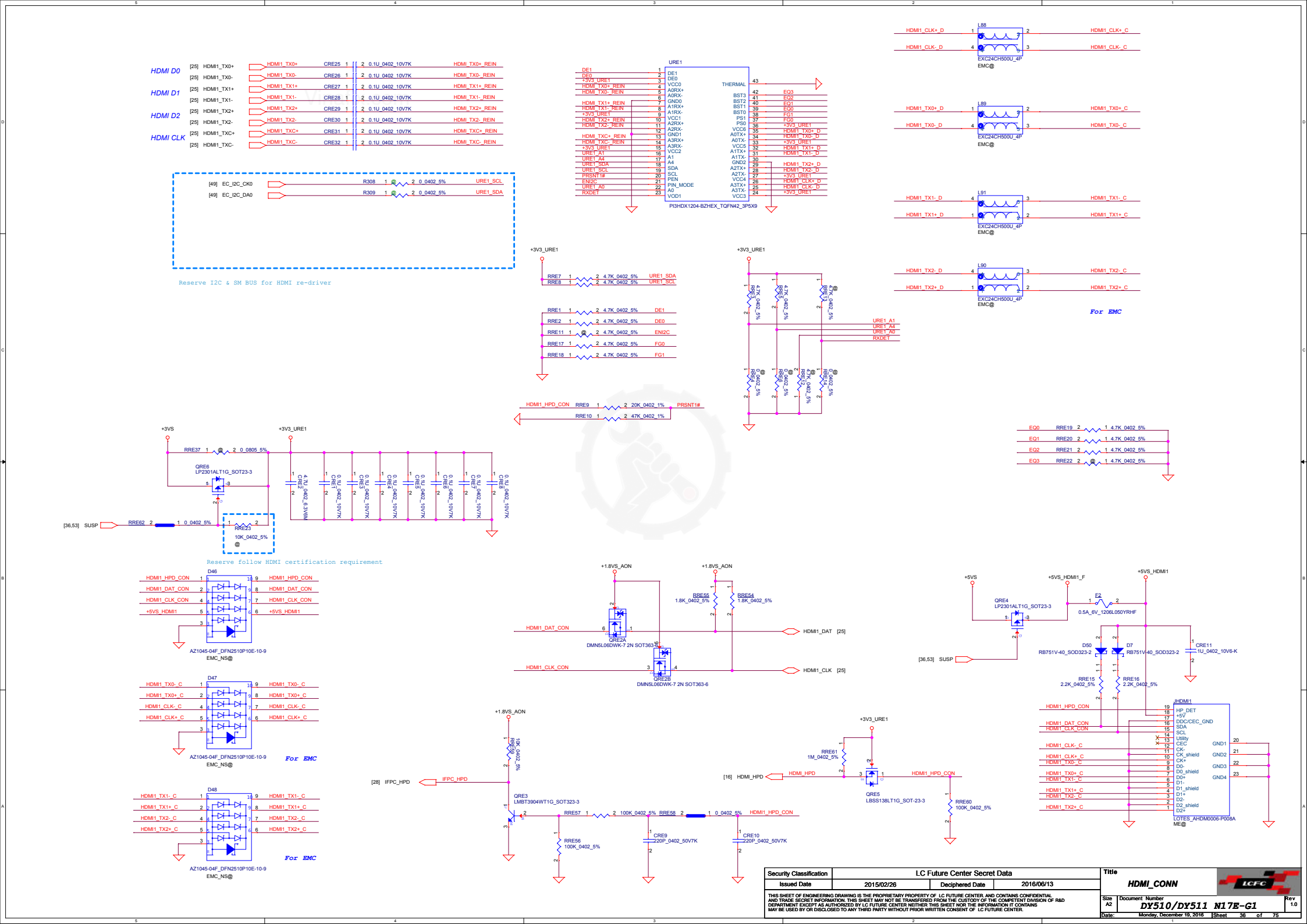


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: eDP/ CMOS/Touch screen

Size: Custom | Document Number: DY510/DY511 N17E-G1 | Rev: 1.0

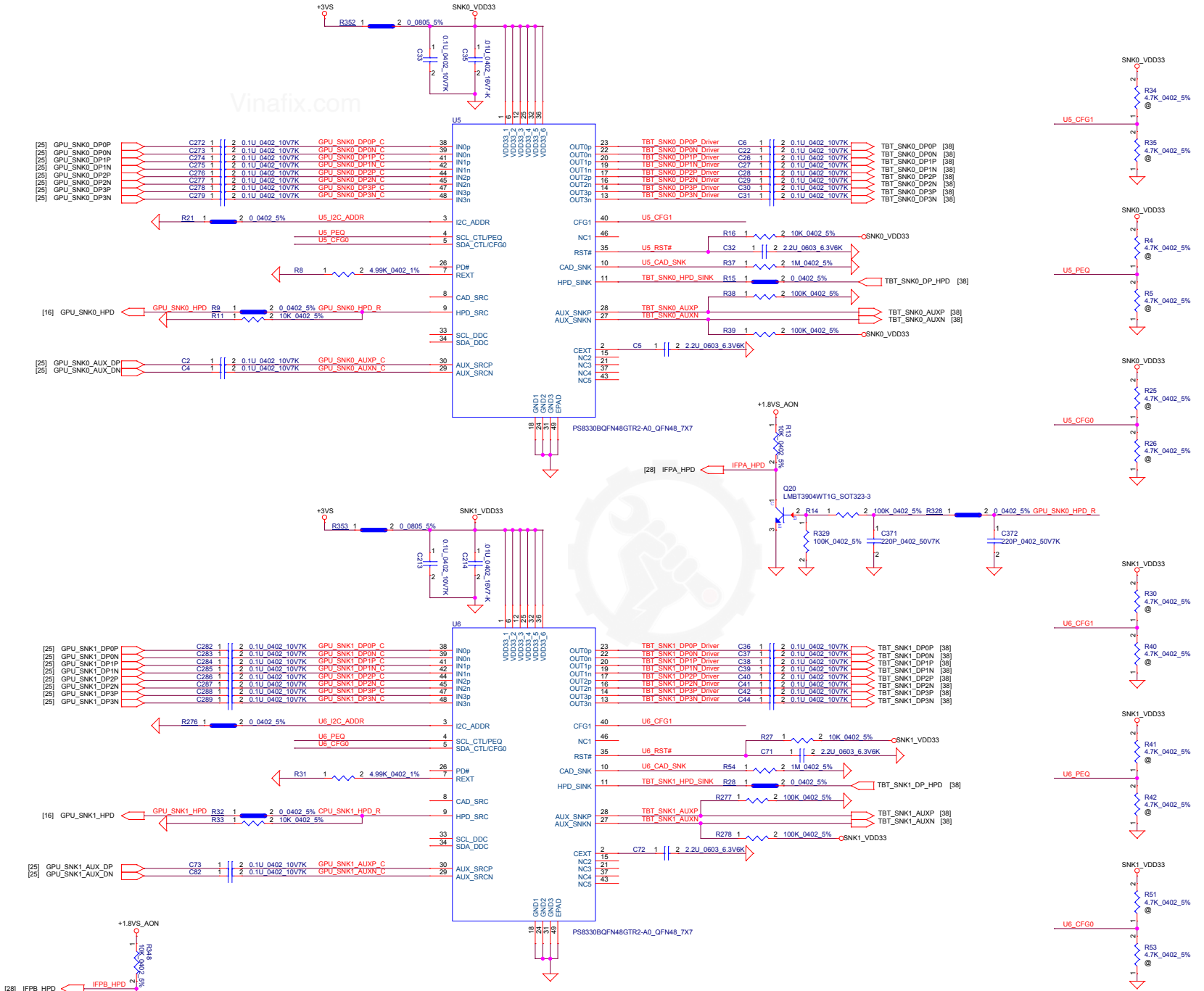
Date: Monday, December 19, 2016 | Sheet 35 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	HDMI_CONN		
Size A2	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 36 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

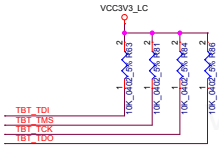
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: DDI Redriver PS8330

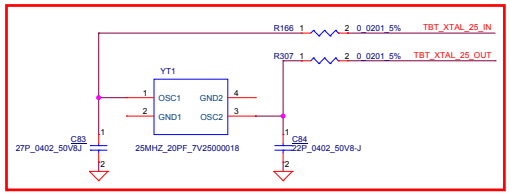
Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 37 of 75

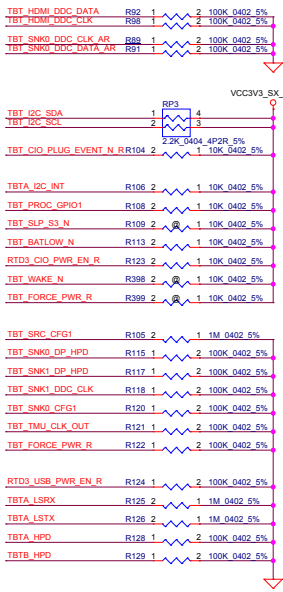
JTAG

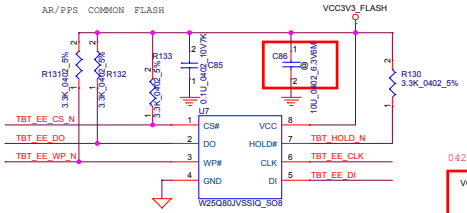


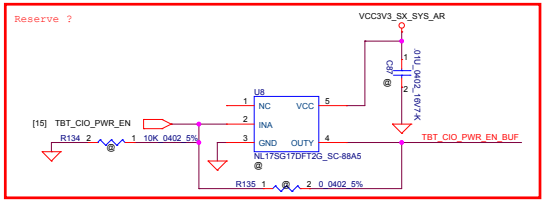
XTAL

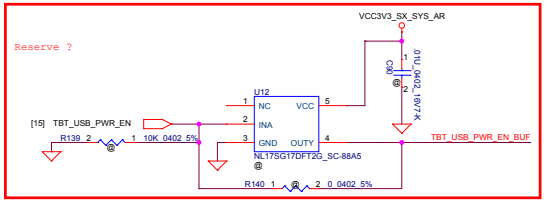


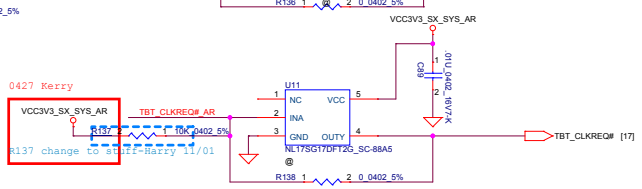
GPIO

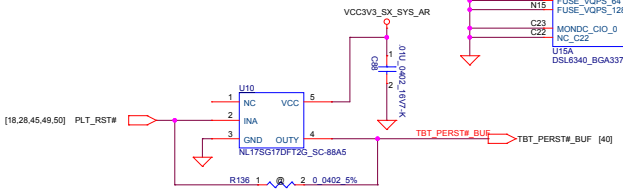


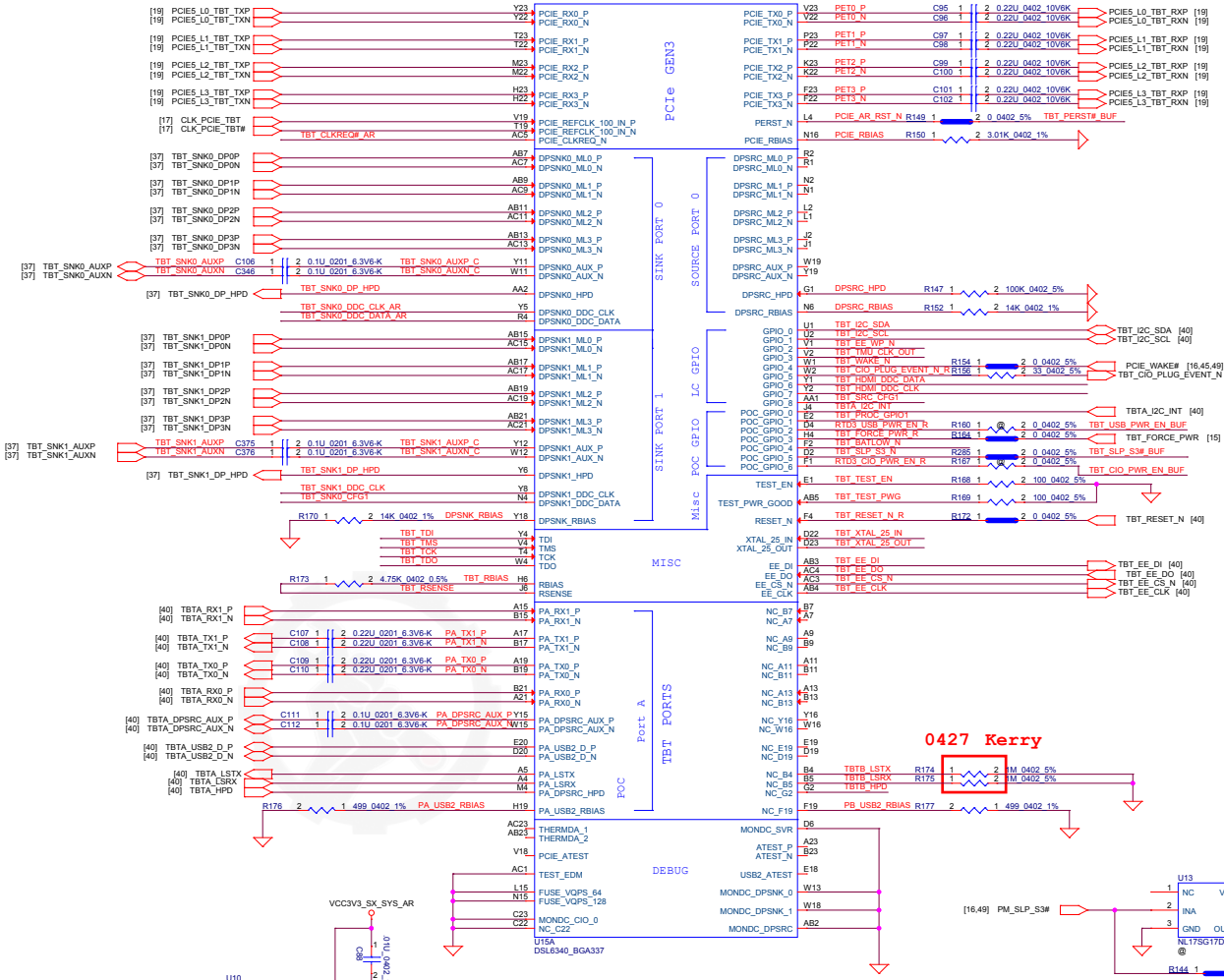










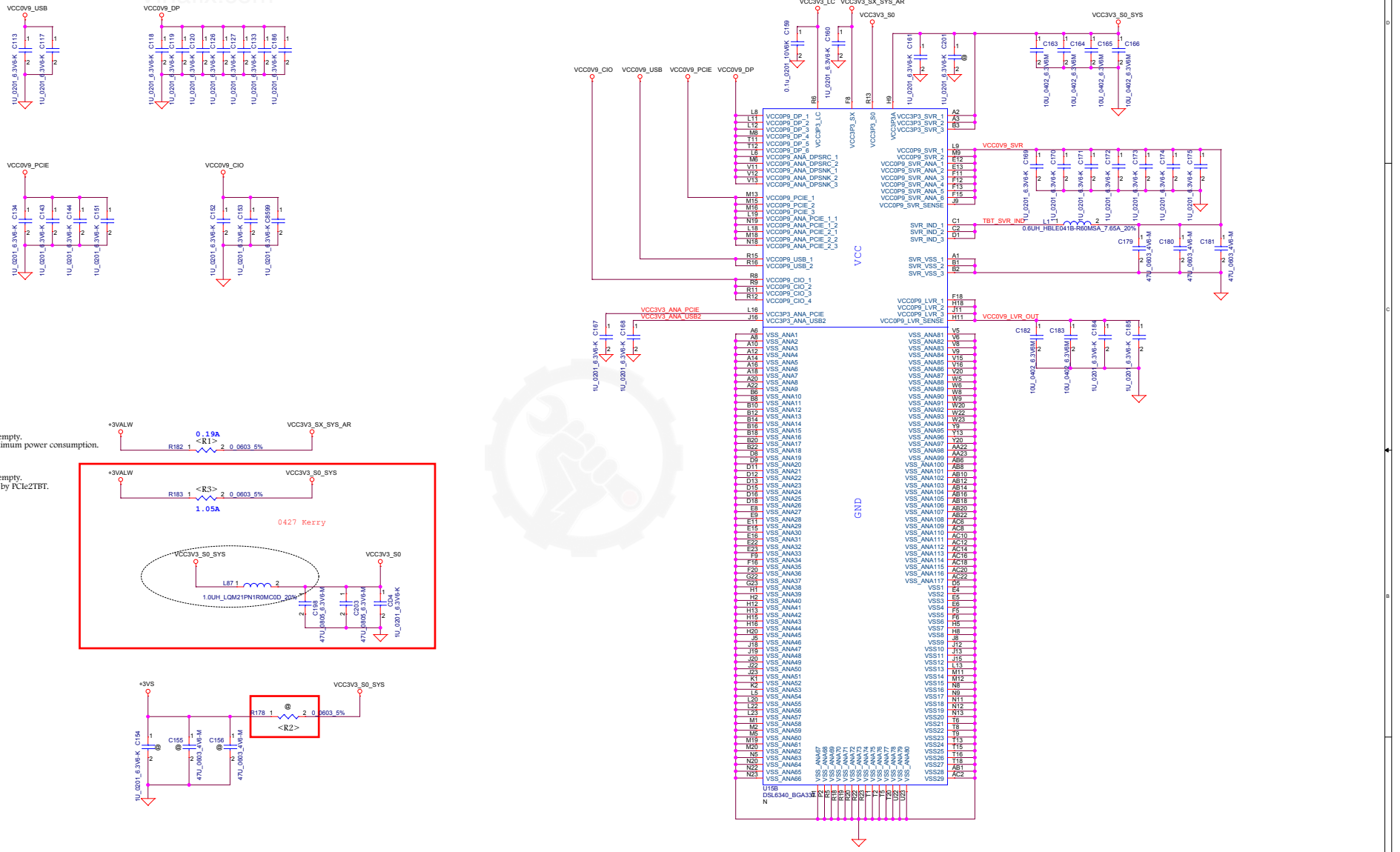


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **USB TYPE-C Controller**

Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 38 of 75



Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

40KHz LC Filter to
reduce VCC3v3_S0_TBT
ripple

L (LQM18PN1R0MFHD):
RDC < 0.2Ohm
IDC > 0.2A

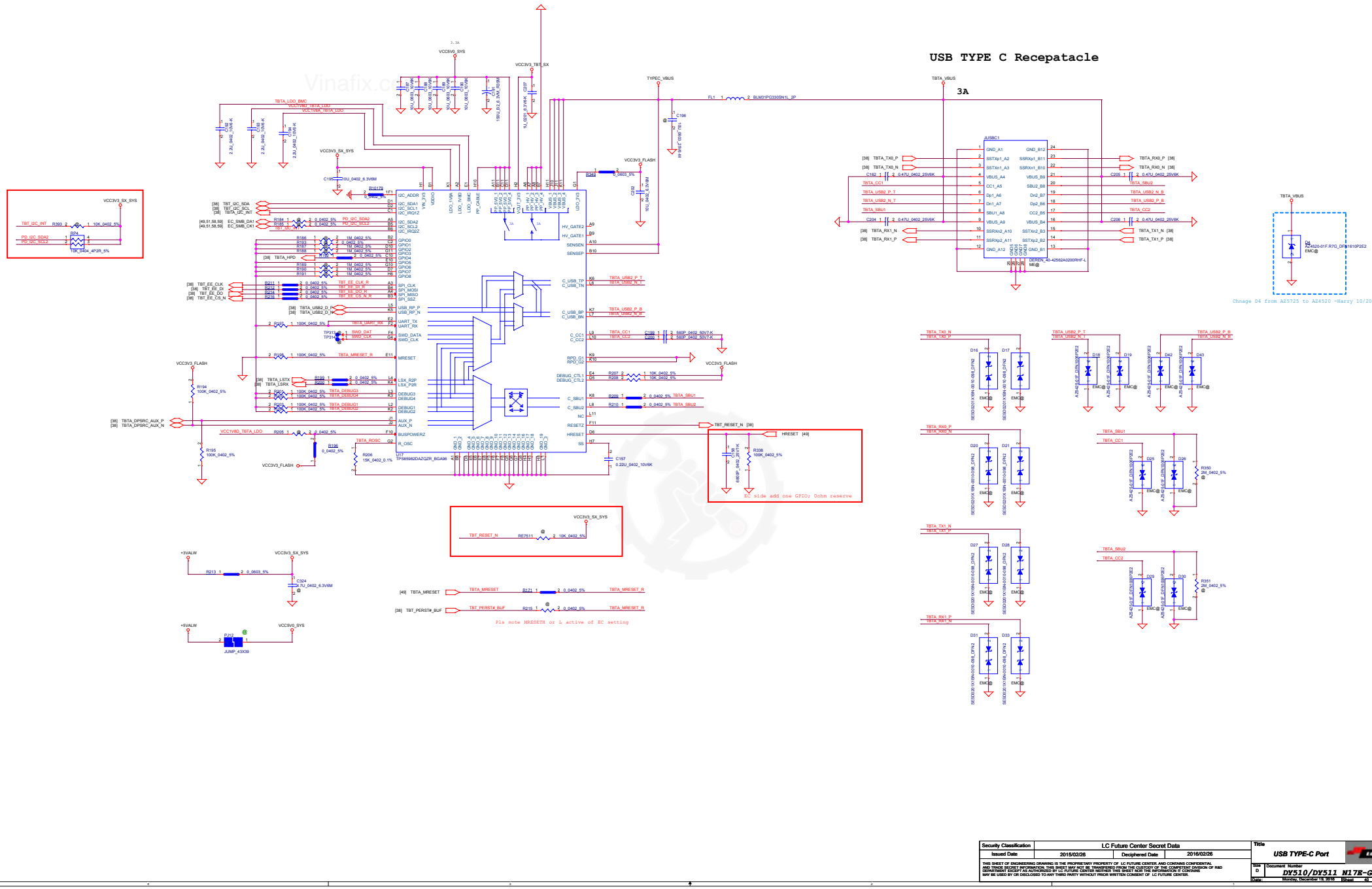
C (GRM188R60J476ME15):
Need to notice the capacitance at 3.3 Vdc

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **USB TYPE-C Controller**

Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0

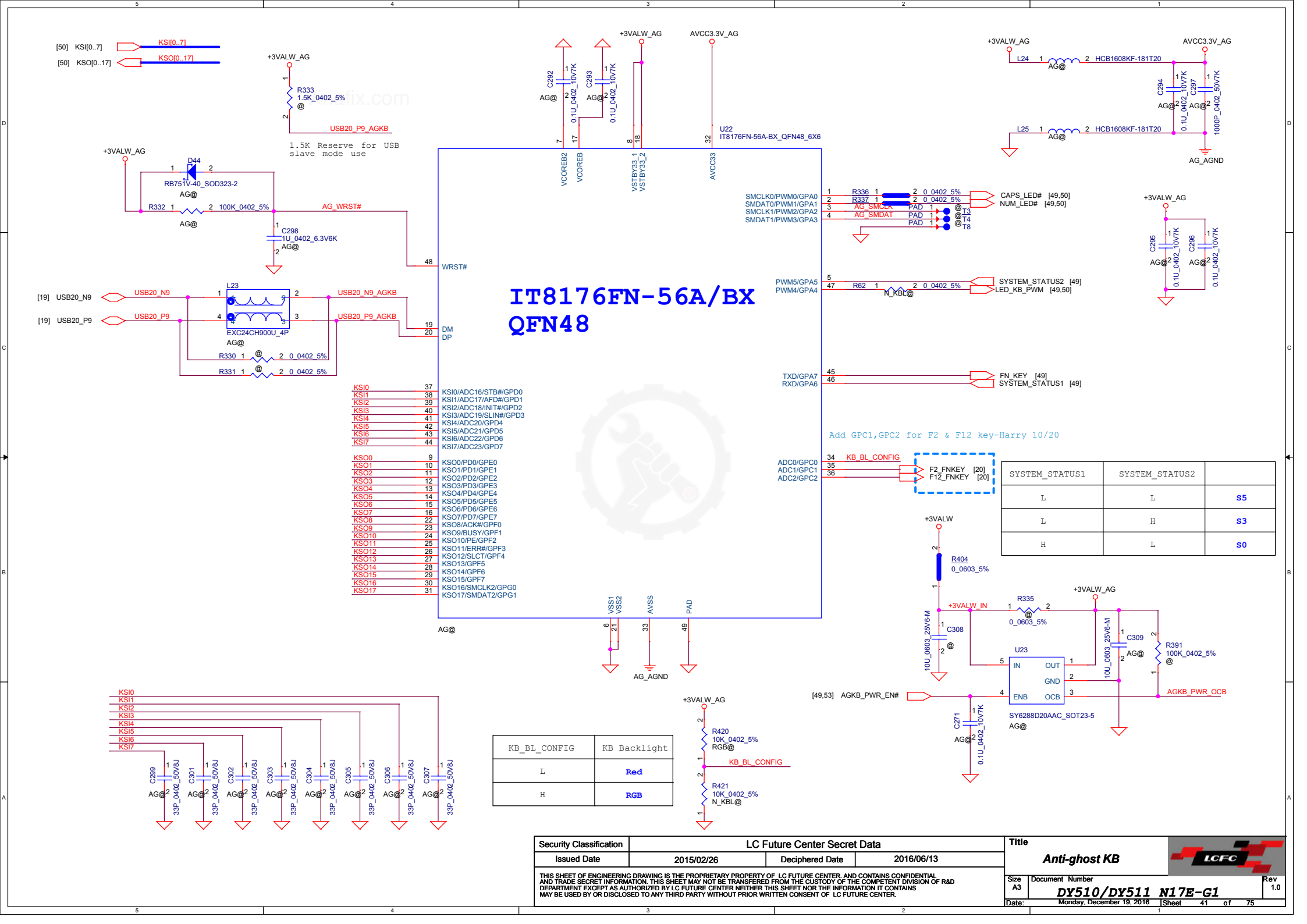
Date: Monday, December 19, 2016 Sheet 39 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	USB TYPE-C Port		
Size	Document Number		Rev
D	DY510/DY511 N17B-G1		1.0
Date:	Monday, December 19, 2016	Sheet	40 of 75



SYSTEM_STATUS1	SYSTEM_STATUS2	
L	L	S5
L	H	S3
H	L	S0

KB_BL_CONFIG	KB Backlight
L	Red
H	RGB

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: **Anti-ghost KB**

Size	Document Number	Rev
A3	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 41 of 75

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

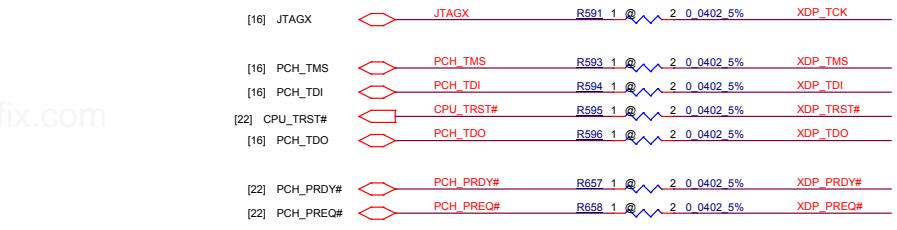
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

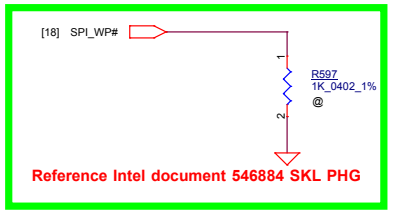
LOGIC

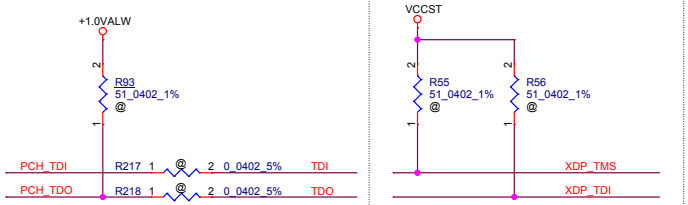
TABLE : Functional Strap

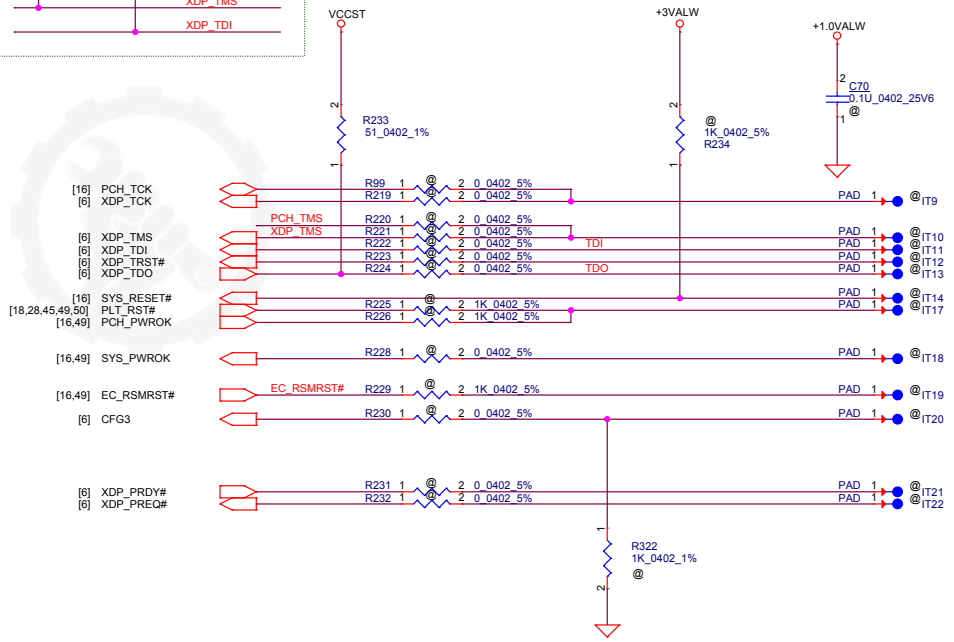
GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

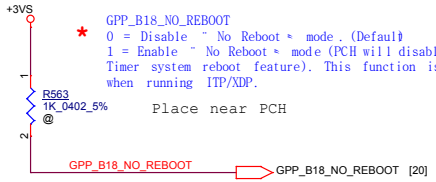
LOGIC









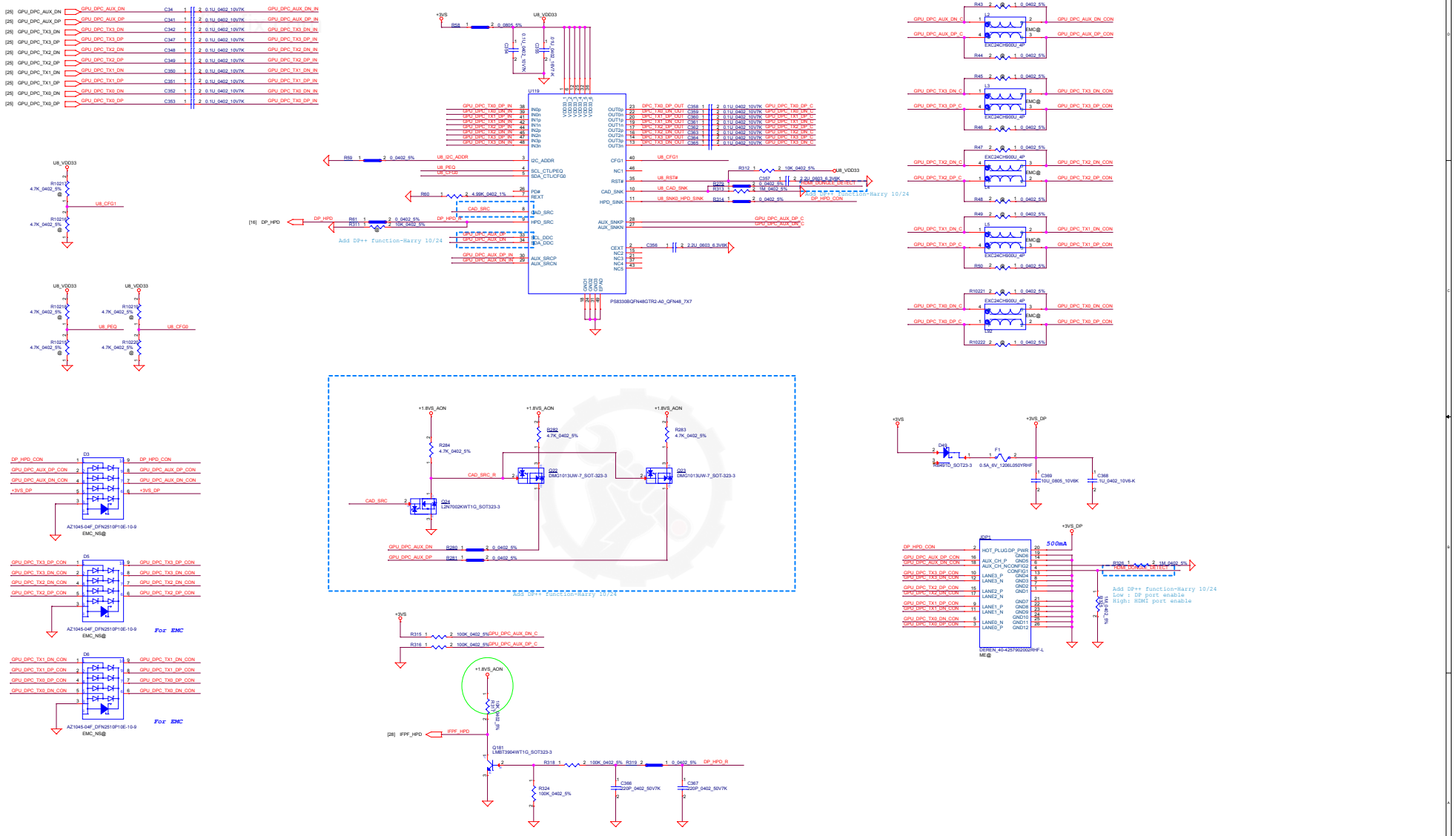


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: XDP

Size: Custom | Document Number: DY510/DY511 N17E-G1 | Rev: 1.0

Date: Monday, December 19, 2016 | Sheet 42 of 75

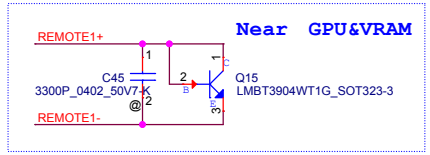


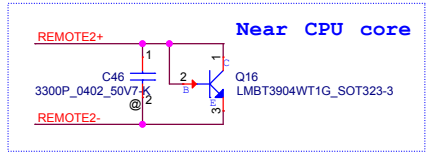
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

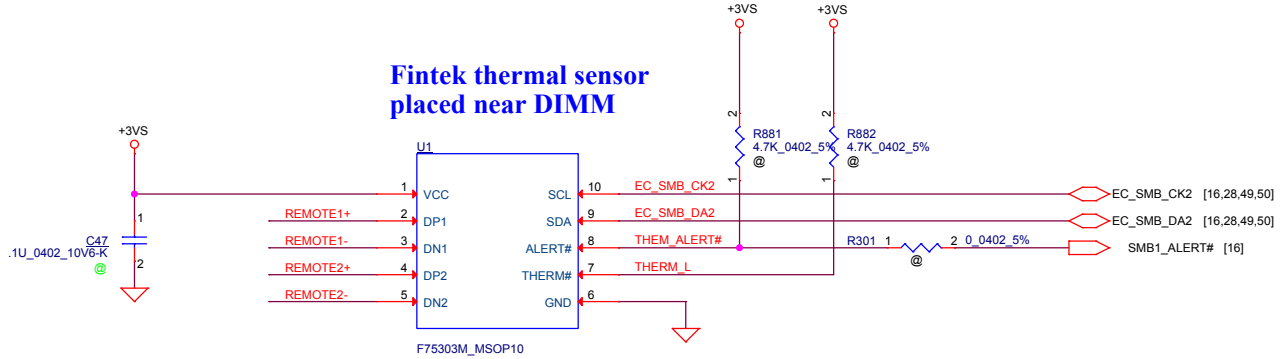
Title	DP		
Size	Document Number		Rev
D	DY510/DY511 N17E-G1		1.0
Date: Monday, December 19, 2016	Sheet 43 of 75		

REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



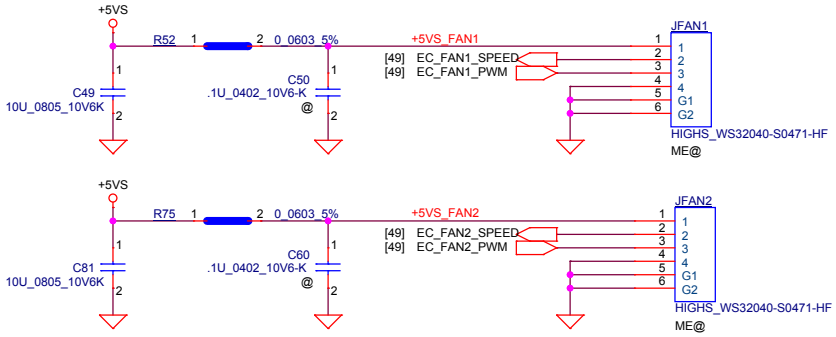


Fintek thermal sensor placed near DIMM



FAN Conn

Address 1001_101xb



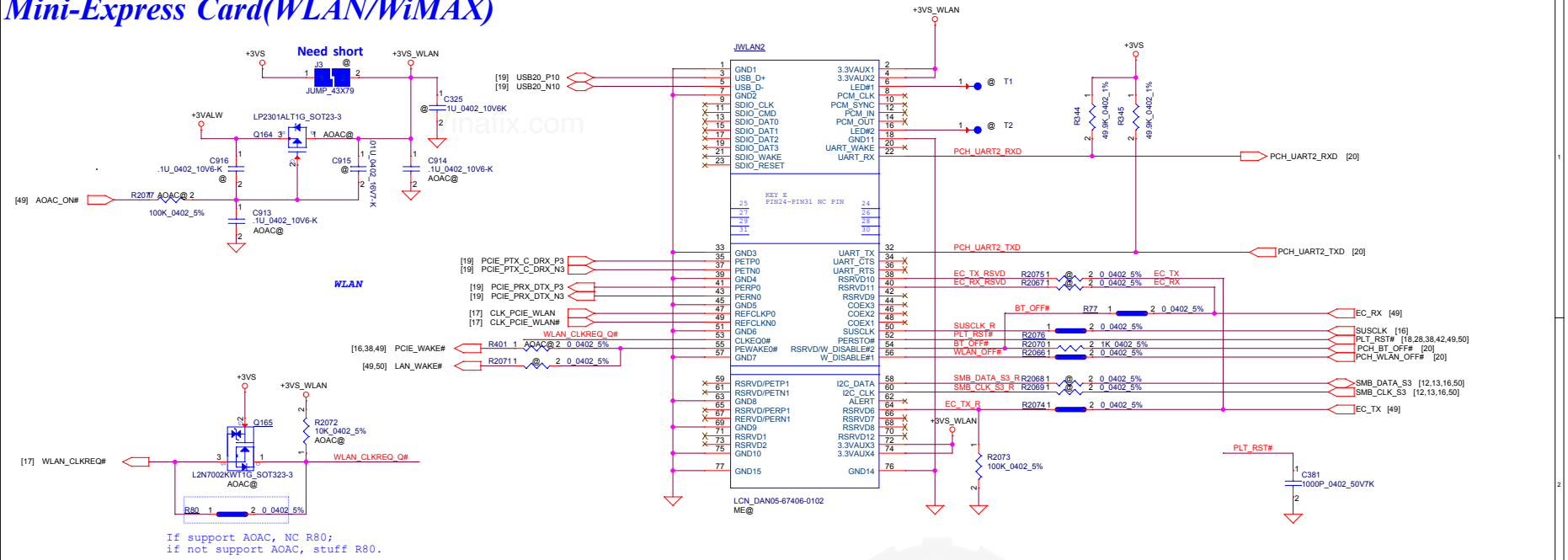
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: Thermal sensor/FAN CONN

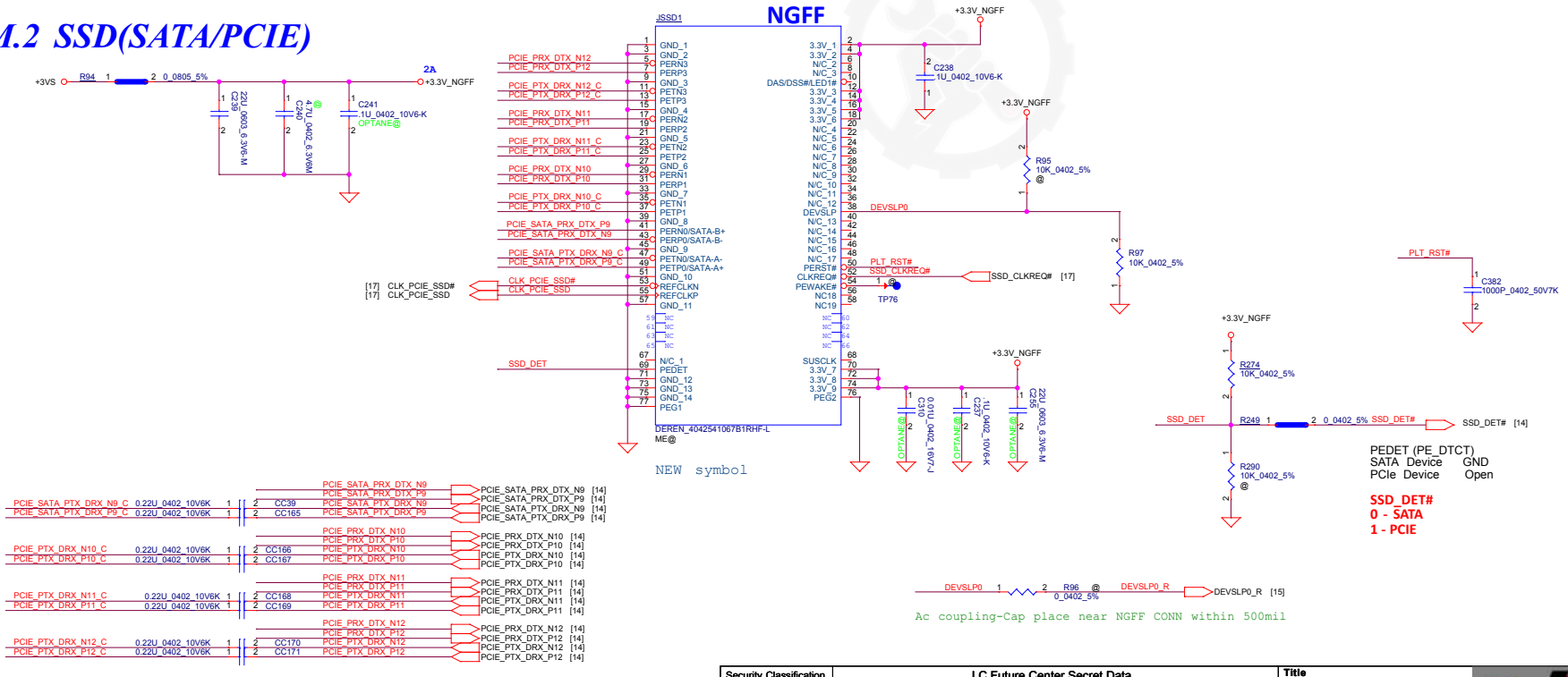
Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0

Date: Monday, December 19, 2016 Sheet 44 of 75

Mini-Express Card(WLAN/WiMAX)



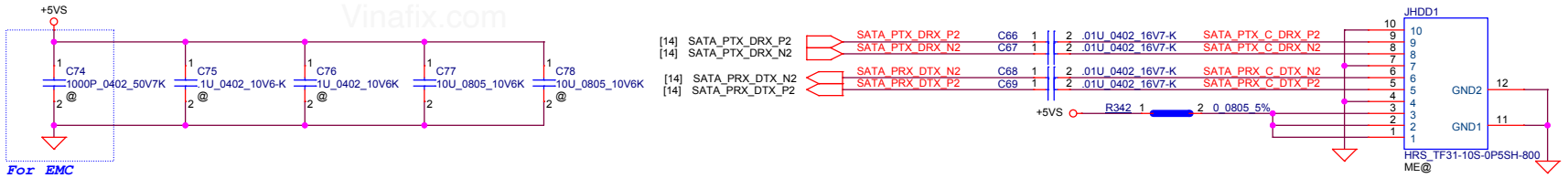
M.2 SSD(SATA/PCIE)



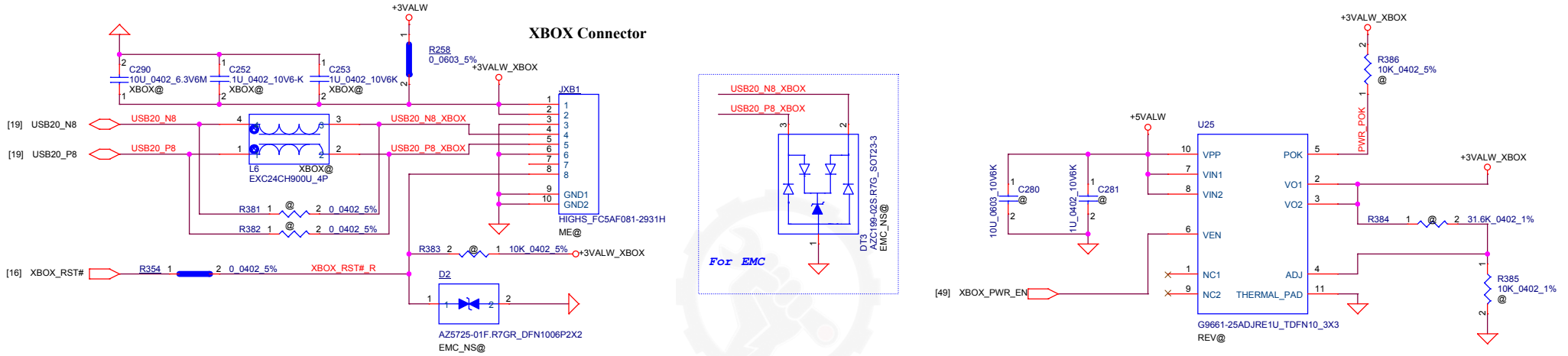
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

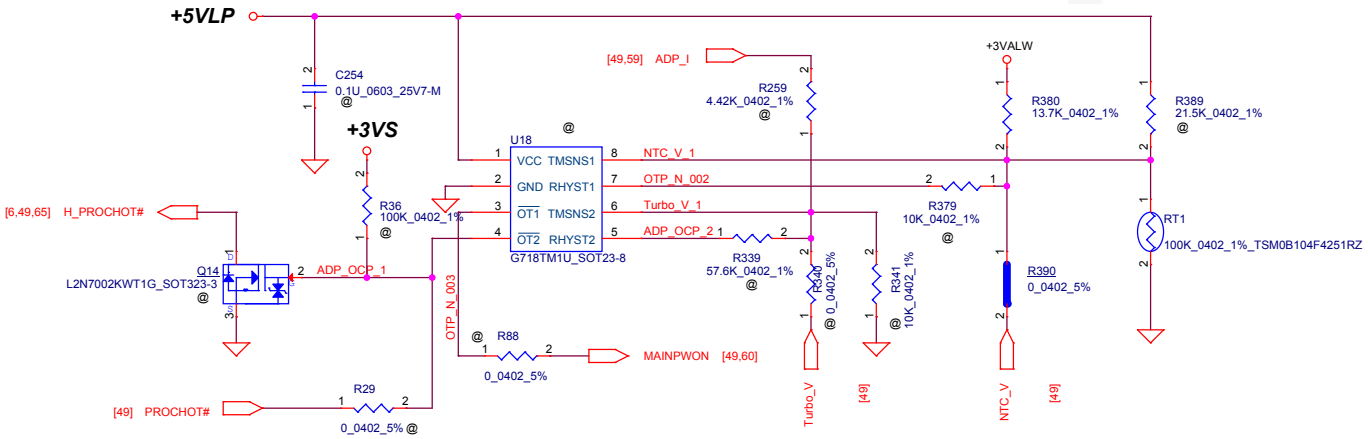
Title	NGFF WLAN		
Size: Custom	Document Number: DY510/DY511 N17E-G1		Rev: 1.0
Date: Monday, December 19, 2016	Sheet 45 of 75		

SATA HDD Conn.



XBOX Connector





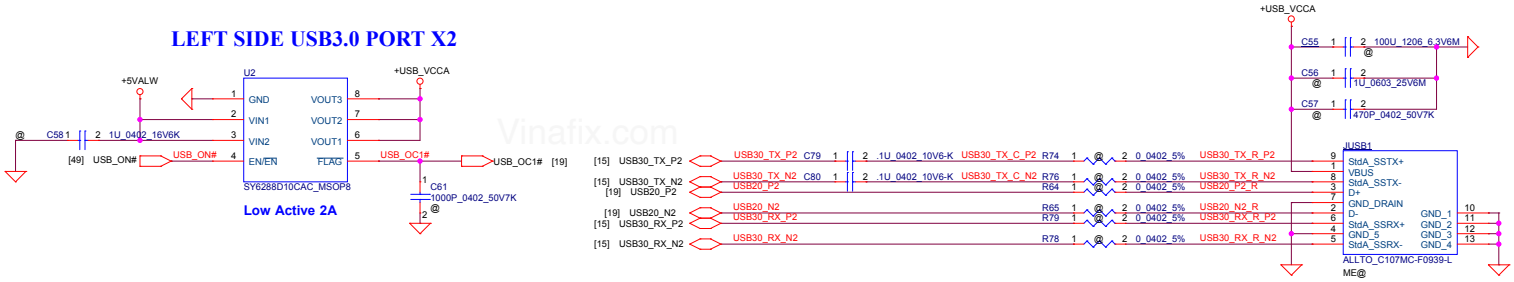
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

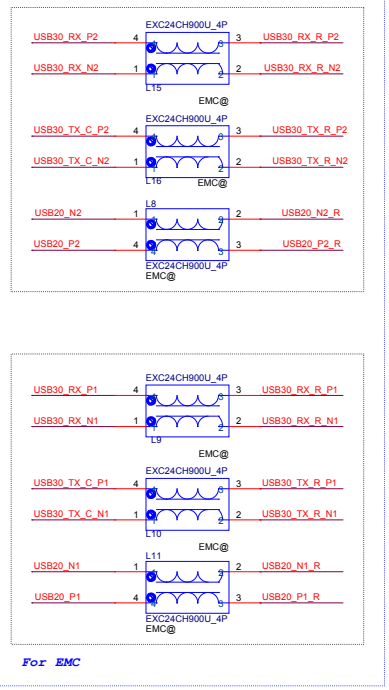
Title: **HDD/XBOX CONN**

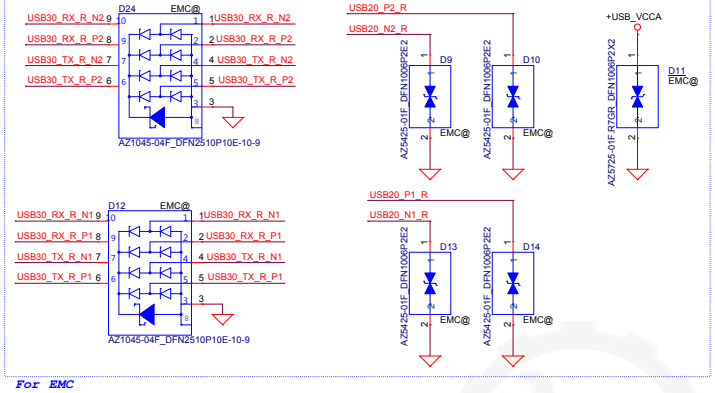
Size	Document Number	Rev
Custom	DY510/DY511 N17E-G1	1.0

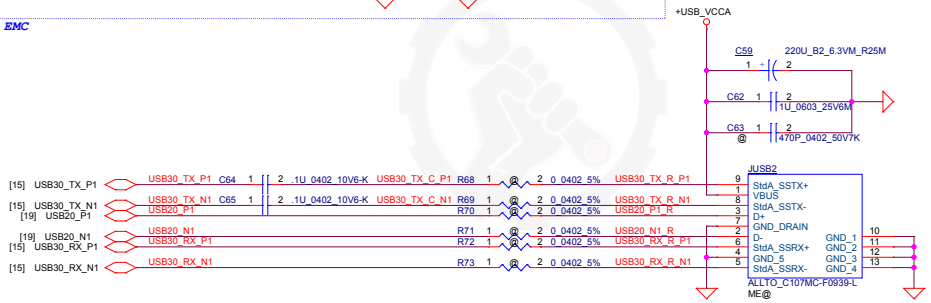
Date: Monday, December 19, 2016 Sheet 46 of 75

LEFT SIDE USB3.0 PORT X2



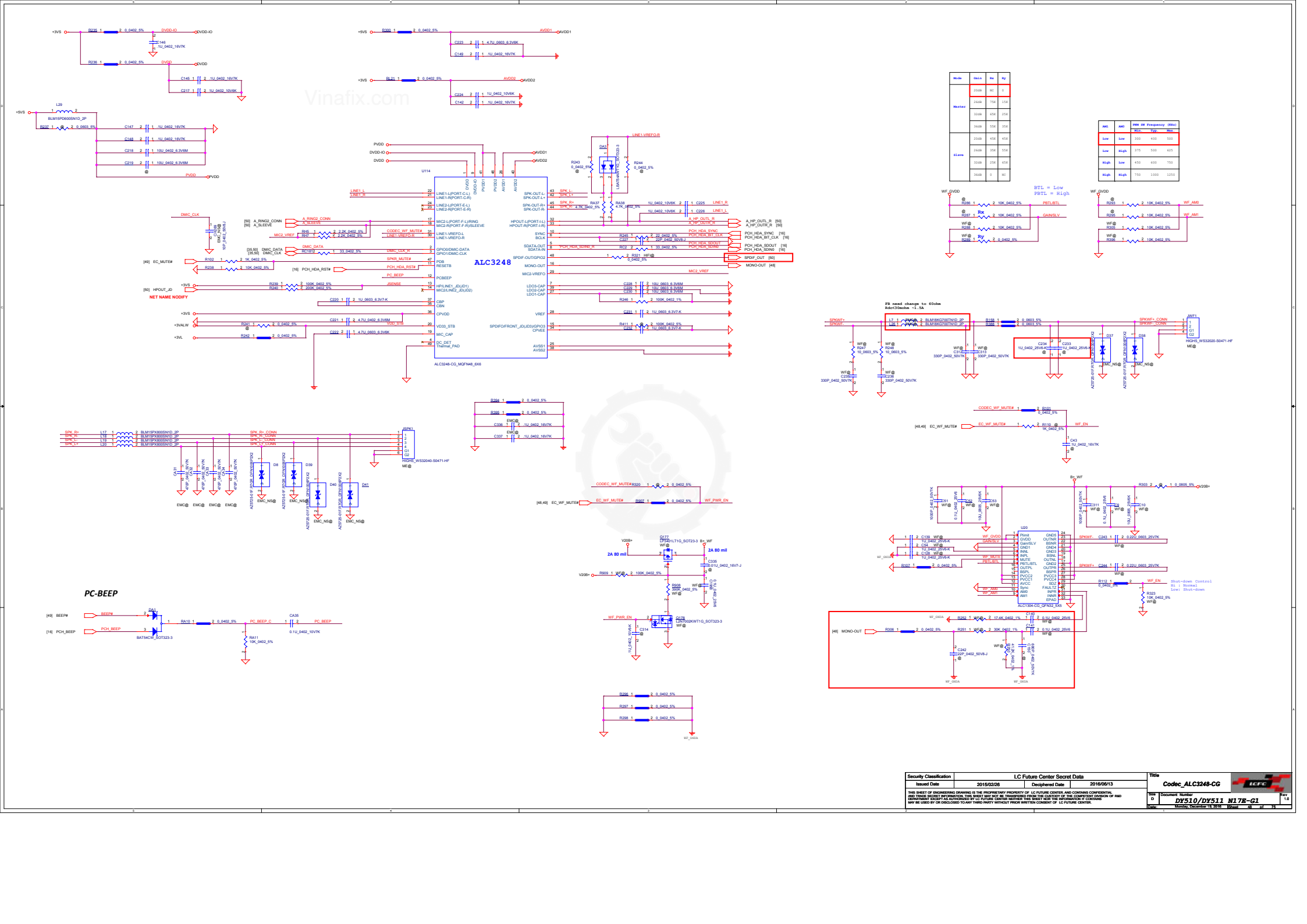






Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title	USB2.0/USB3.0 PORT (LEFT)		
Size C	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 47 of 75		



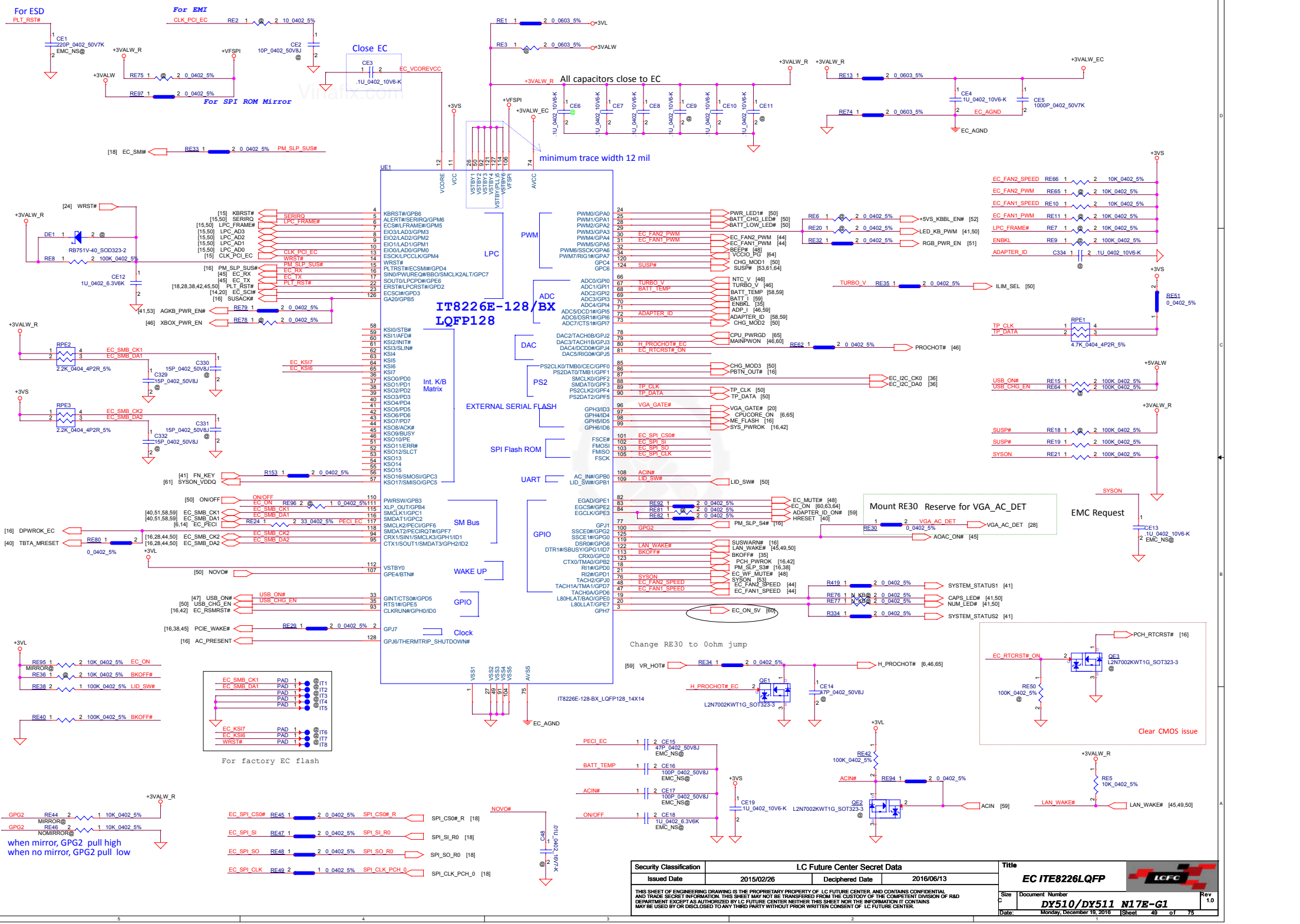
Mode	Gain	Rx	Ry
Master	20dB	8K	0
	24dB	75K	15K
	32dB	45K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	24dB	35K	55K
	32dB	25K	65K
	36dB	0	8K

AM0	AM1	PWM SW Frequency (KHz)		
		Min.	Typ.	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

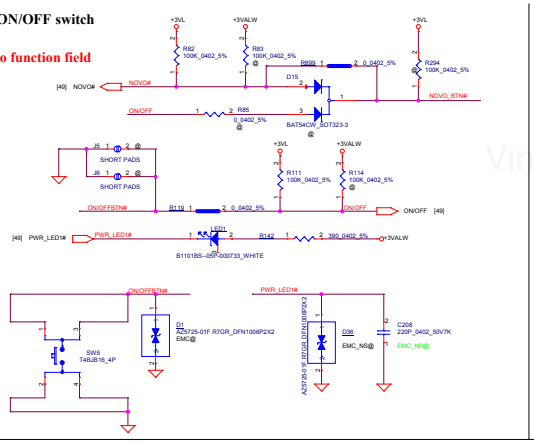
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

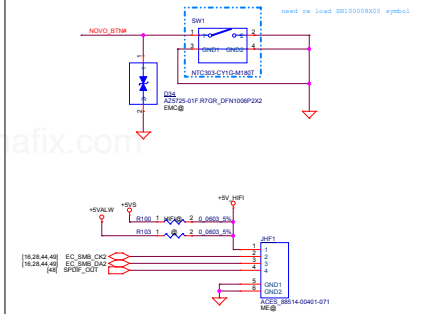
Title	Codec_ALC3248-CG		
Size D	Document Number DY510/DY511 N17B-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 48 of 75		


For ESD
For EMI
Close EC
For SPI ROM Mirror
All capacitors close to EC
minimum trace width 12 mil
IT8226E-128/BX
LQFP128
UE1
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
WAKE UP
GPIO
Clock
Int. K/B Matrix
Mount RE30 Reserve for VGA_AC_DET
EMC Request
Change RE30 to 0ohm jump
Clear CMOS issue
For factory EC flash
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
IT8226E-128-BX_LQFP128_14X14
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/06/13
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
EC ITE8226LQFP
Size
C
Document Number
DY510/DY511 N17E-G1
Rev
1.0
Date:
Monday, December 19, 2016
Sheet
49
of
75

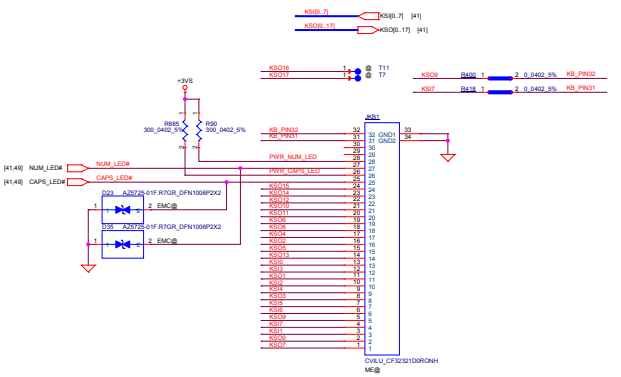
ON/OFF switch

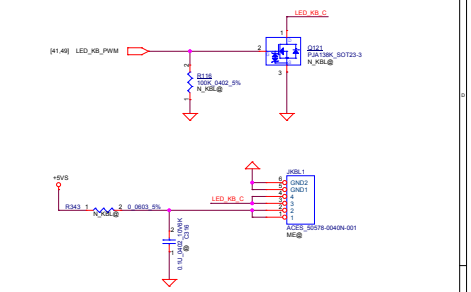
No function field



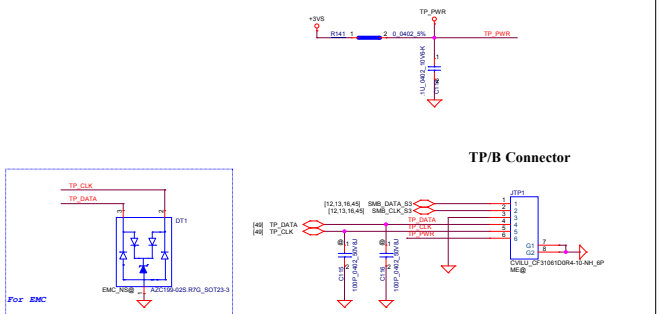


K/B Connector

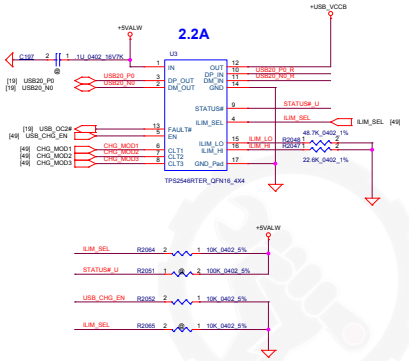




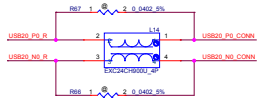
TP/B Connector



USB charger



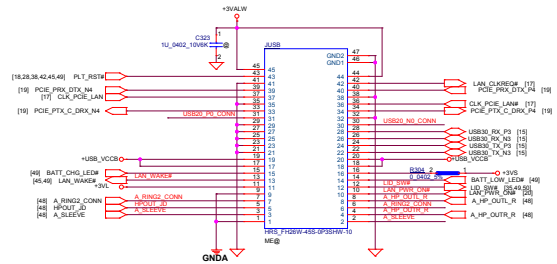
Right Side USB2.0 Port X 1 (USB/B)



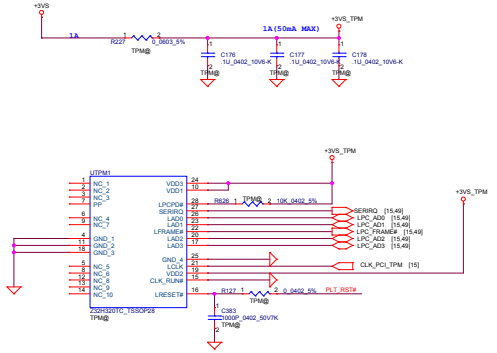
	Pin Number	6	7	8	4
	Pin Name	CTL1	CTL2	CTL3	ILM_SEL
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

SDP2 (No Discharge from/to CDP)
SDP1(Discharge from/to any charging state including CDP)

USB I/O Connector

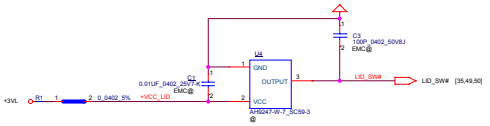


TPM

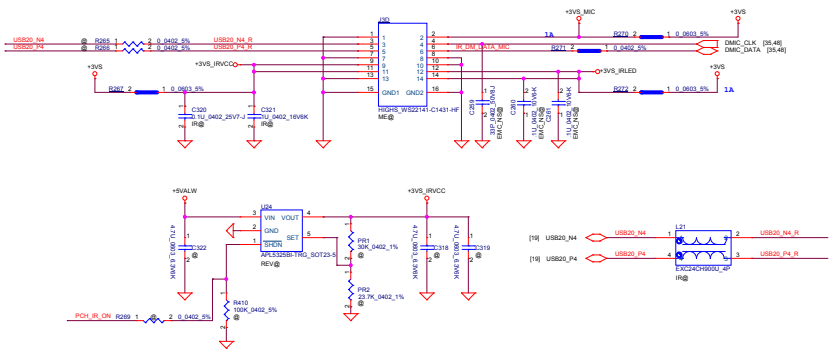


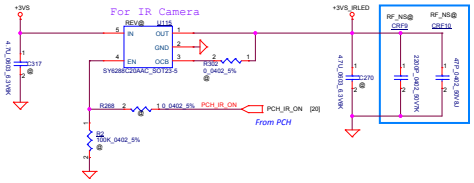
LID Hall Sensor

No function field



IR Camera

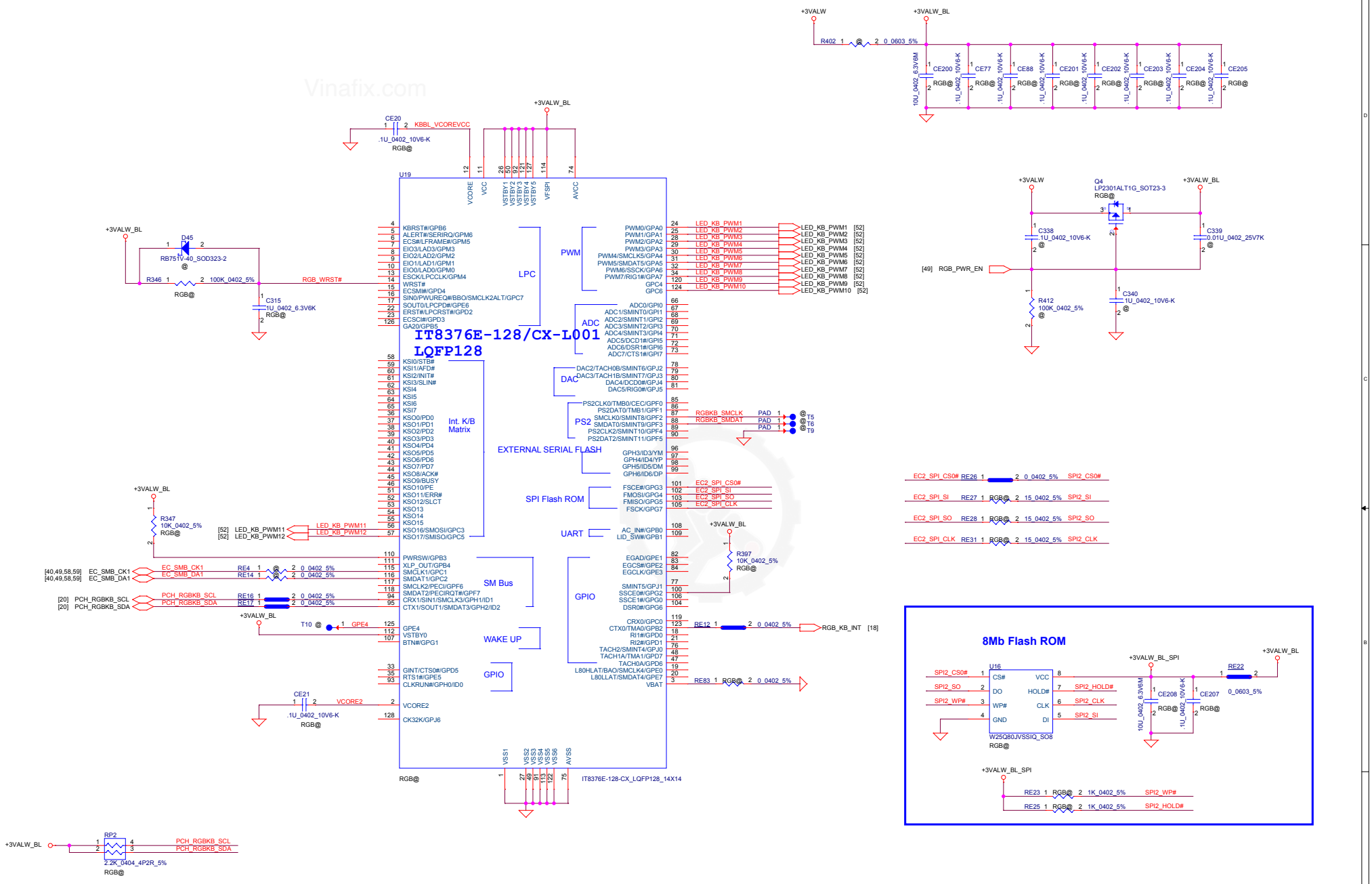




Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	KBD/PWR/IO/LED/TP Conn.		
Size D	Document Number DY510/DY511 N17B-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 50 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

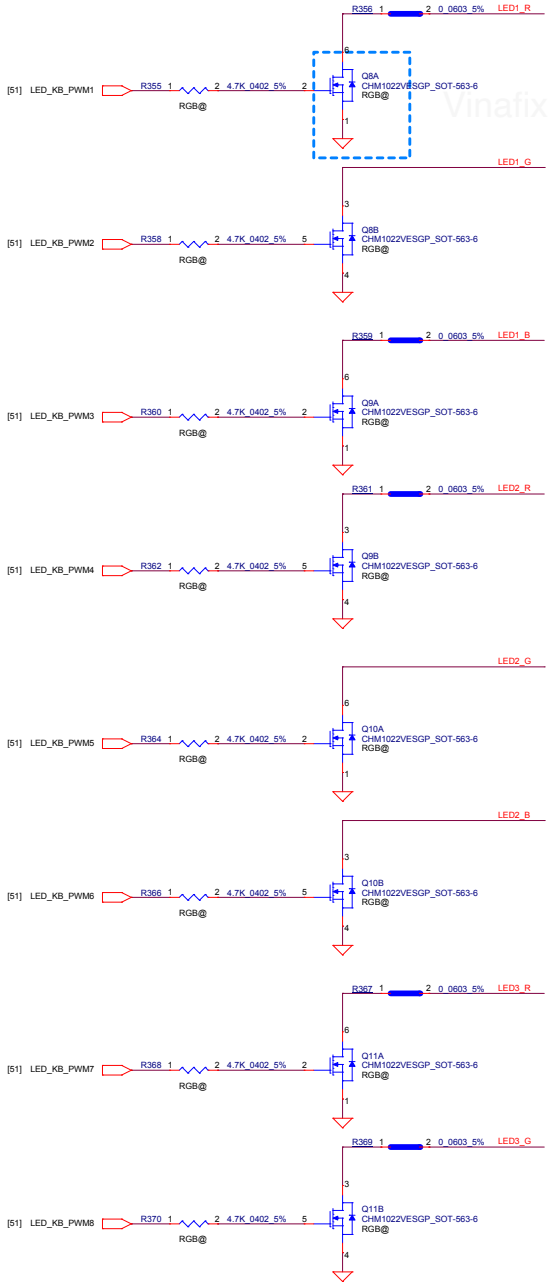
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

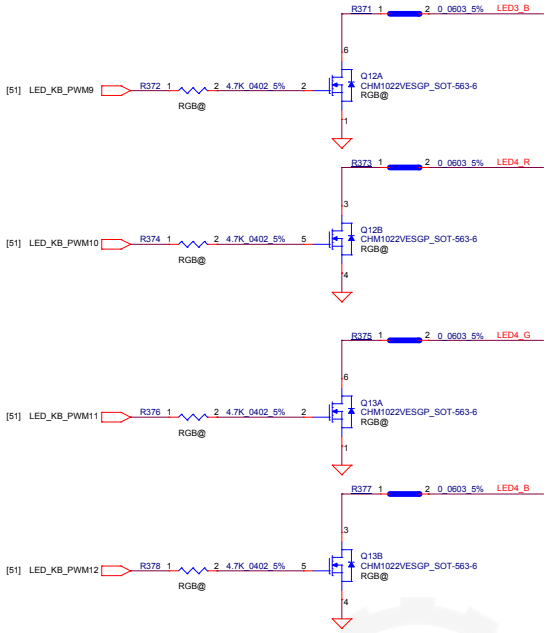
Title: **RGB KBD LED Controller**

Size	Document Number	Rev
C	DY510/DY511 N17E-G1	1.0

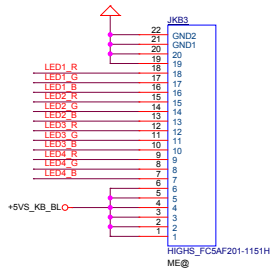
Date: Monday, December 19, 2016 Sheet 51 of 75

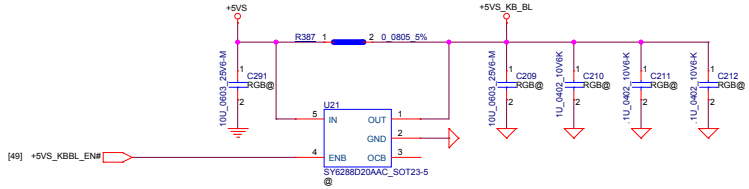
need reload symbol for SB000018E00
-Harry 10/20





RGB KB BL CONN.



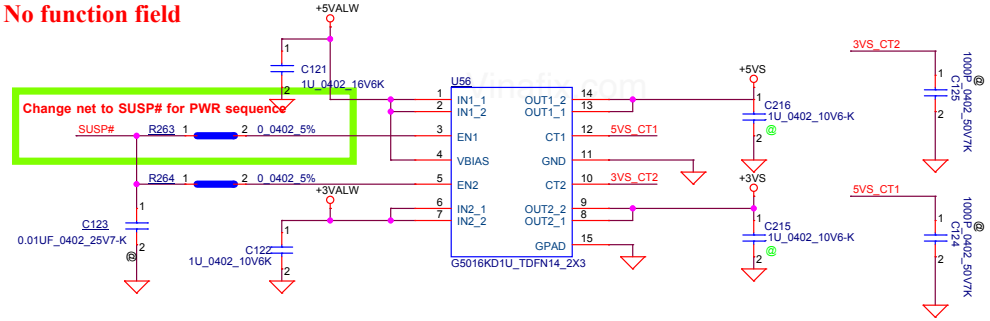


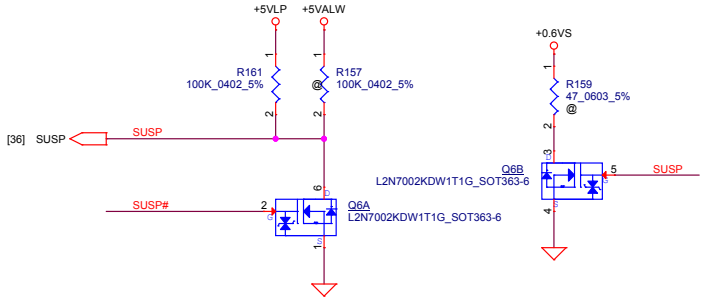
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title	RGB KBD LED CONN		
Size A2	Document Number DY510/DY511 N17E-G1		Rev 1.0
Date: Monday, December 19, 2016	Sheet 52 of 75		

+5VALW to +5VS

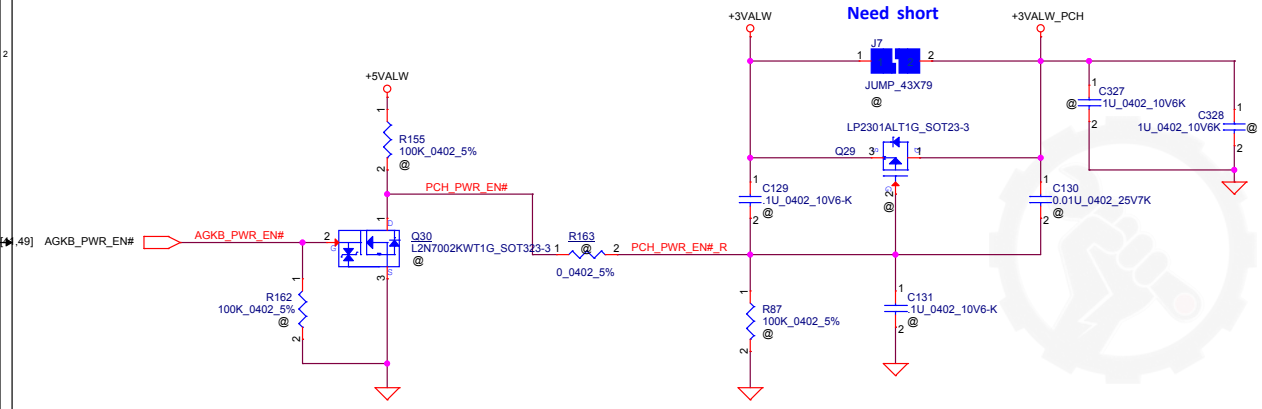
No function field

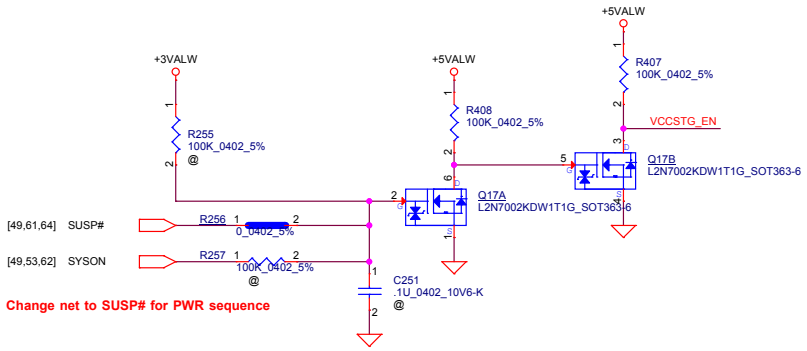


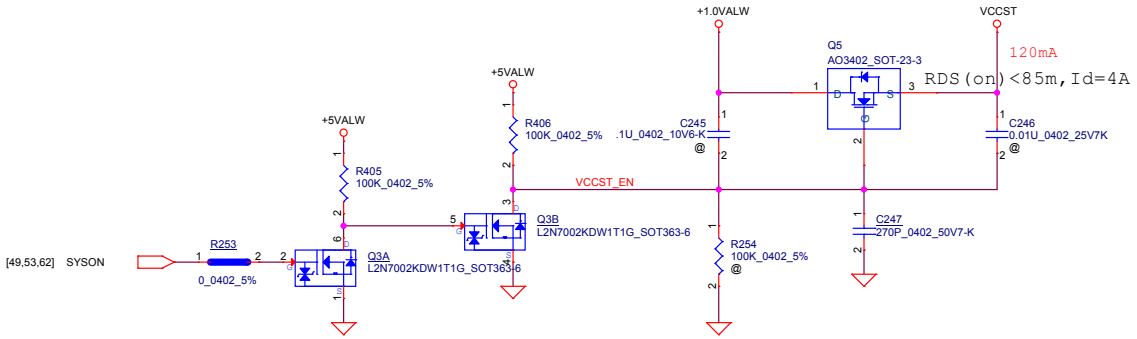


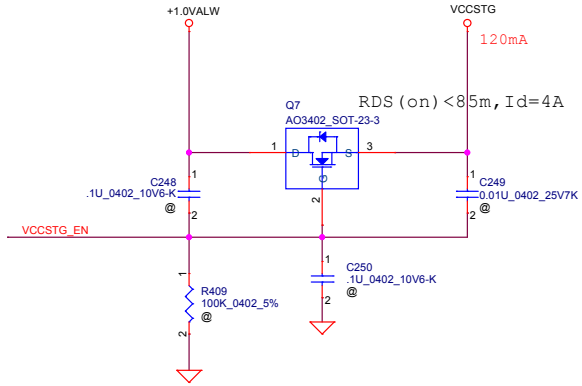
LP2301ALT1G
Rds=110mohm @
VGS=4.5V,ID=2.8A
VGS(th)=1V Max

Need short









Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/06/13

Title: *DC V TO VS INTERFACE*

Size	Document Number	Rev
Custom	*DY510/DY511 N17E-G1*	1.0

Date: Monday, December 19, 2016 Sheet 53 of 75

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

Virtual symbol

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 54 of 75

H1 HOLEA PAD_C5P5D2P3
H2 HOLEA PAD_C4P0D4P0N
H3 HOLEA pad_ct6p0d2p5
H4 HOLEA pad_ct8p0d5p5
H5 HOLEA pad_ct6p0d2p5
H6 HOLEA PAD_O2P1X2P6D2P1X2P6N
H7 HOLEA PAD_C4P0D4P0N
H8 HOLEA PAD_CT6P0B5P5D2P3
H9 HOLEA PAD_C4P0D4P0N
H10 HOLEA pad_ct6p0b5p0d2p3
H11 HOLEA pad_ct8p0d6p0
H12 HOLEA pad_c6p5d6p5n
H13 HOLEA PAD_C4P0D4P0N
H14 HOLEA PAD_C4P0D4P0N

H19 HOLEA pad_c5p5d5p5n
H18 HOLEA pad_ct6p0d2p5
H23 HOLEA pad_c2p1d2p1n
H15 HOLEA pad_shapet6p5x10p25cb5p0d2p3
H16 HOLEA PAD_C4P0D4P0N
H17 HOLEA PAD_C4P0D4P0N
H20 HOLEA pad_ct6p0b5p0d2p3
H21 HOLEA PAD_CT6P0B5P5D2P3
H22 HOLEA pad_c5p5d5p5n
H24 HOLEA PAD_C5P5D2P3
H25 HOLEA PAD_C5P5D2P3
H26 HOLEA PAD_O2P1X2P6D2P1X2P6N

SH9 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH15 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P

SO-DIMM Shielding

SH1 ME@ SPRING_FINGER_6.2X1.64
SH2 ME@ SPRING_FINGER_6.2X1.64
SH3 ME@ SPRING_FINGER_6.2X1.64
SH4 ME@ SPRING_FINGER_6.2X1.64
SH6 ME@ SPRING_FINGER_6.2X1.64

USB3.0 Shielding

NVVDD C135 .1U_0402_10V6-K EMC_NS@
+3VS C136 .1U_0402_10V6-K EMC_NS@
+5VALW C137 .1U_0402_10V6-K EMC_NS@
+3VALW C138 .1U_0402_10V6-K EMC_NS@

For EMC

FD1 FD2 FD3 FD4 FD5 FD6

+3VS C326 4.7U_0402_6.3V6M @

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

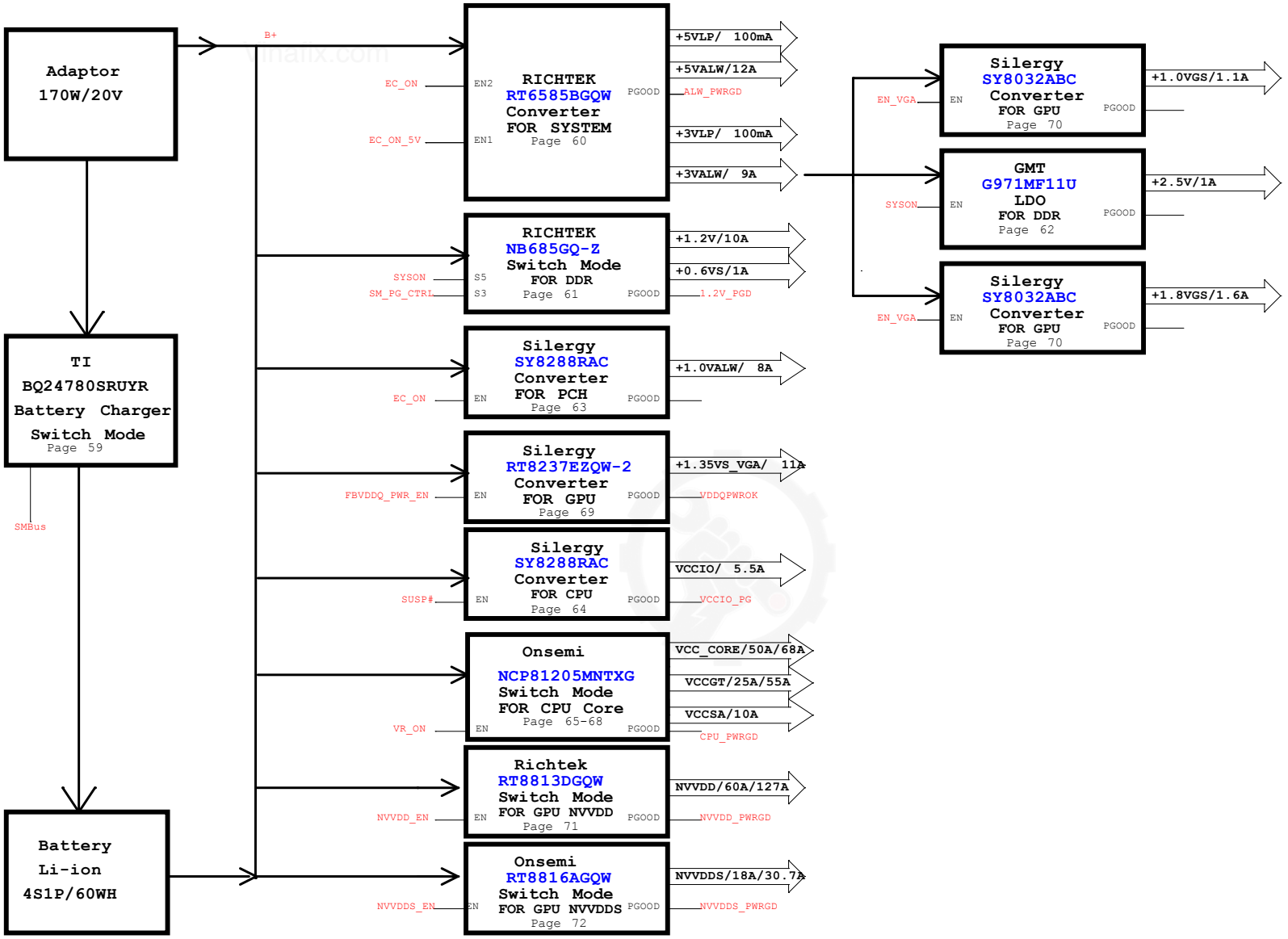
Title: ***Hole***

Size B	Document Number: ***DY510/DY511***	Rev 1.0
Date: Monday, December 19, 2016	Sheet 55 of 75	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size: D	Document Number: ***DX510/DX511***	Rev: 1.0
Date: Monday, December 19, 2016	Sheet 58 of 75	

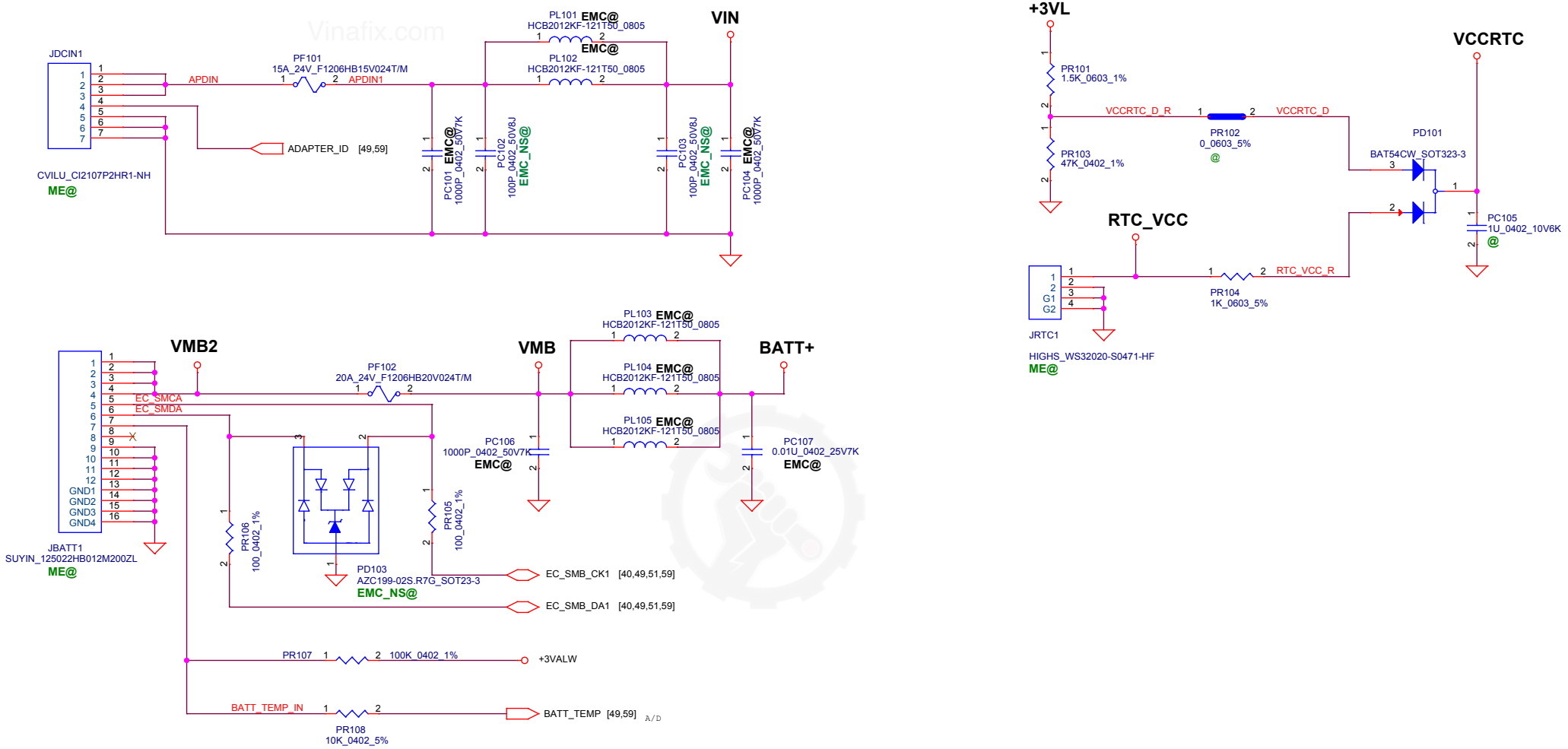


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **Power Diagram**

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 57 of 75

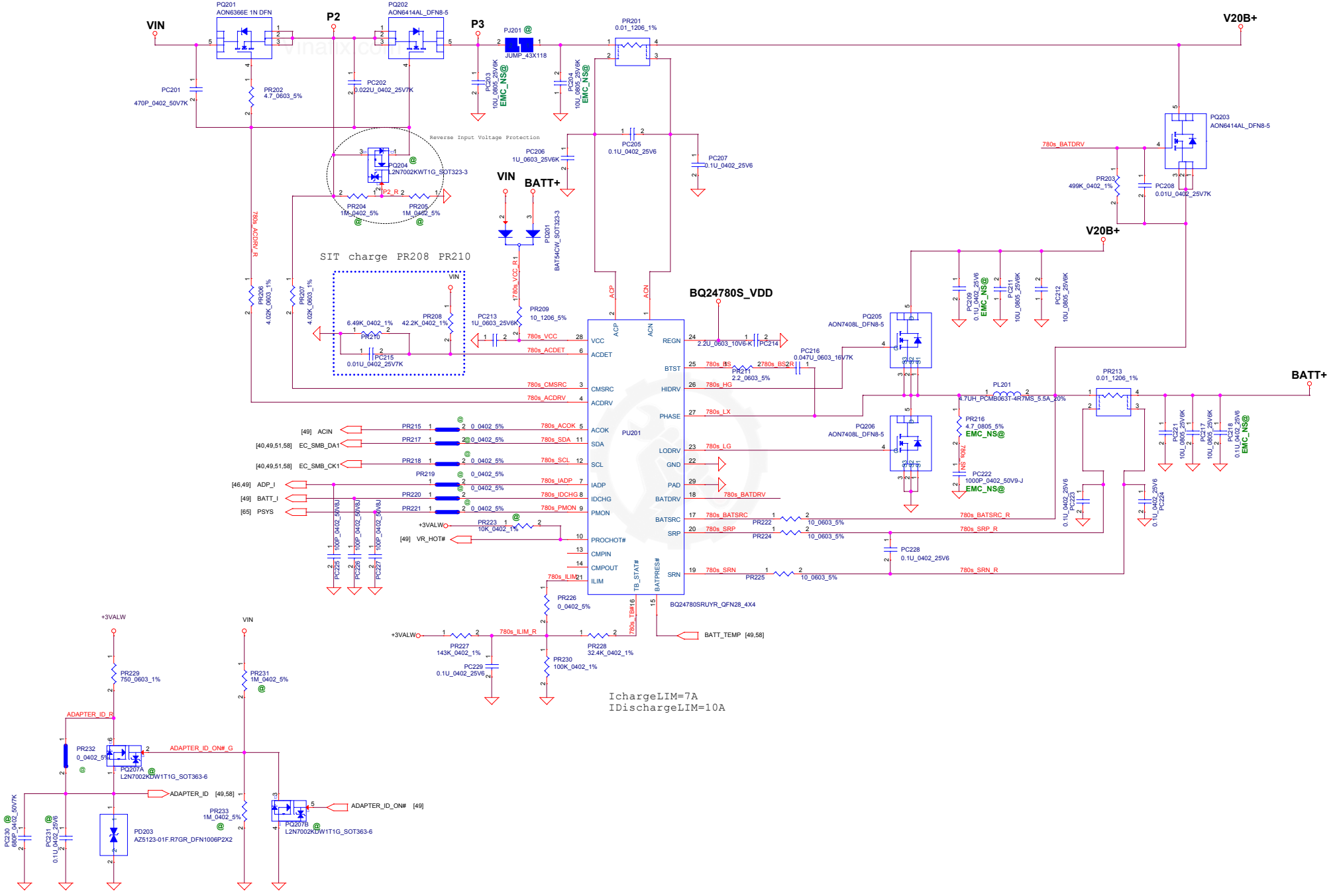


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-DCIN /BATT/ RTC CONN

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 58 of 75

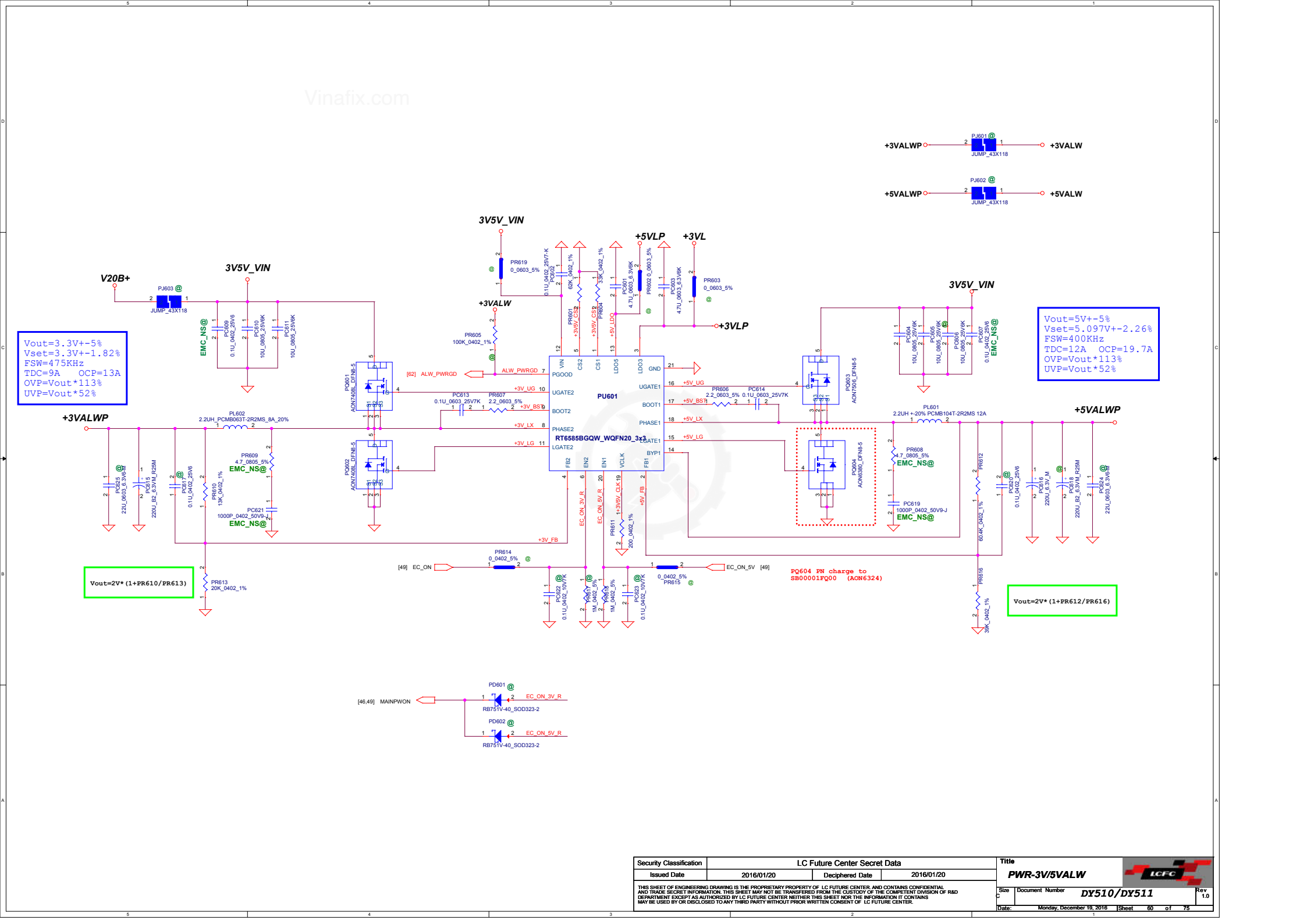


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-Charger

Size: Custom | Document Number: DY510/DY511 | Rev: 1.0

Date: Monday, December 19, 2016 | Sheet 59 of 75

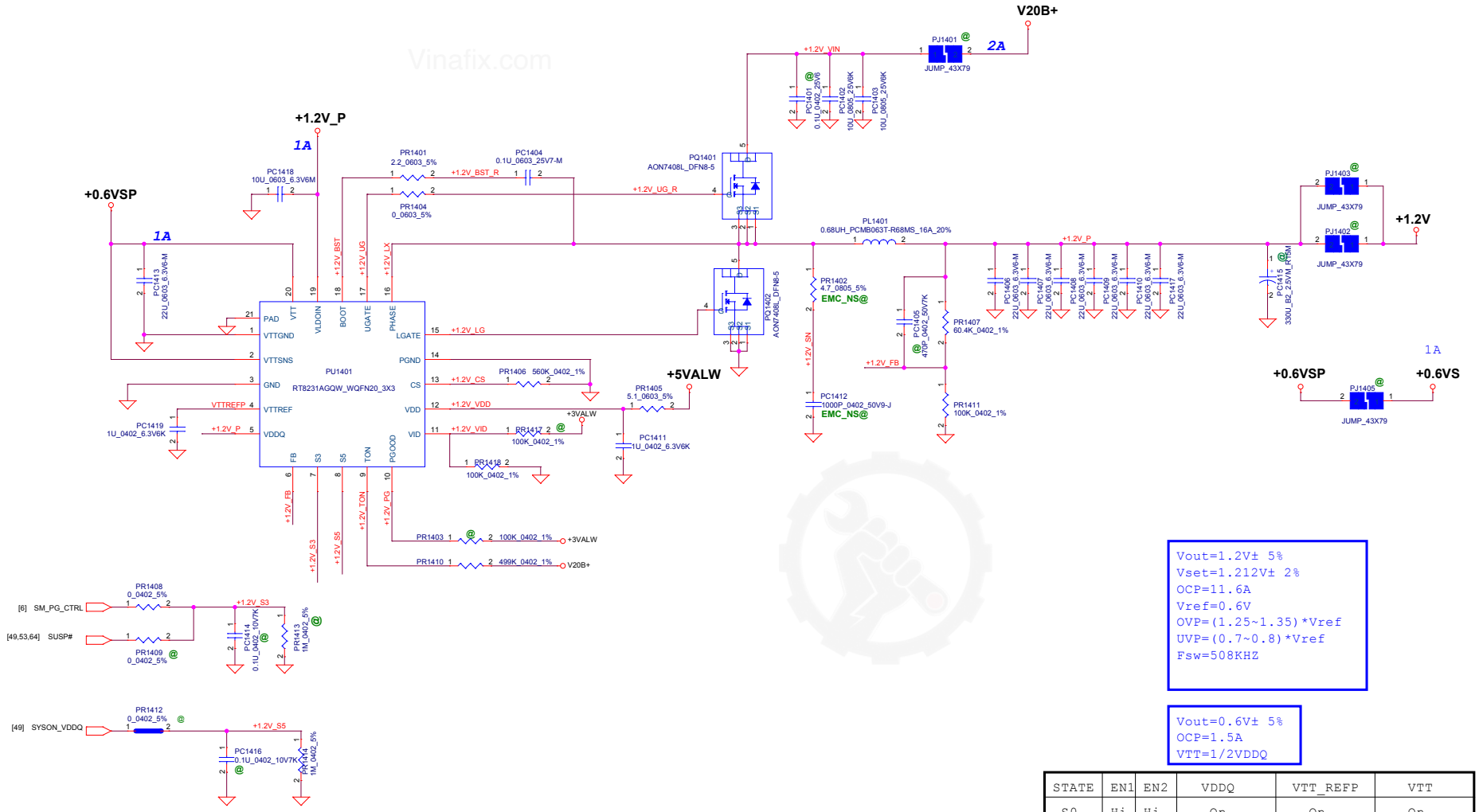


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-3V/5VALW**

Size	Document Number	Rev
C	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 60 of 75



Vout=1.2V± 5%
Vset=1.212V± 2%
OCP=11.6A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=508KHZ

Vout=0.6V± 5%
OCP=1.5A
VTT=1/2VDDQ

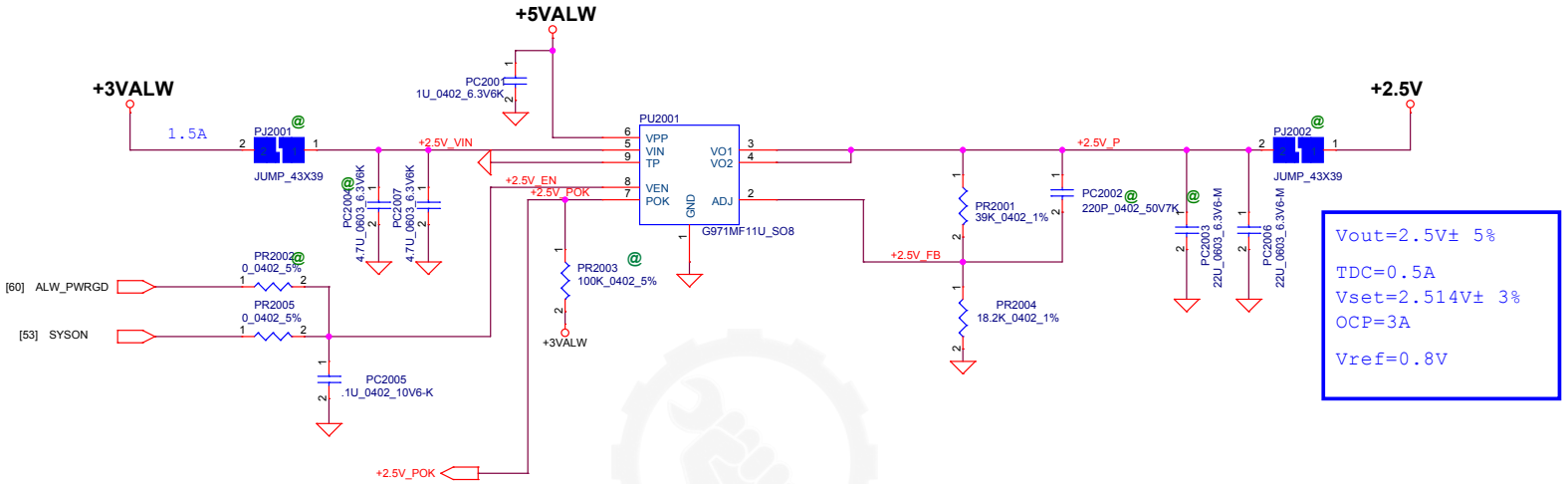
STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Title: PWR-VDDQ/VTT

Size	Document Number	Rev
C	DZ510/DY512	1.0

Date: Monday, December 19, 2016 Sheet 61 of 75

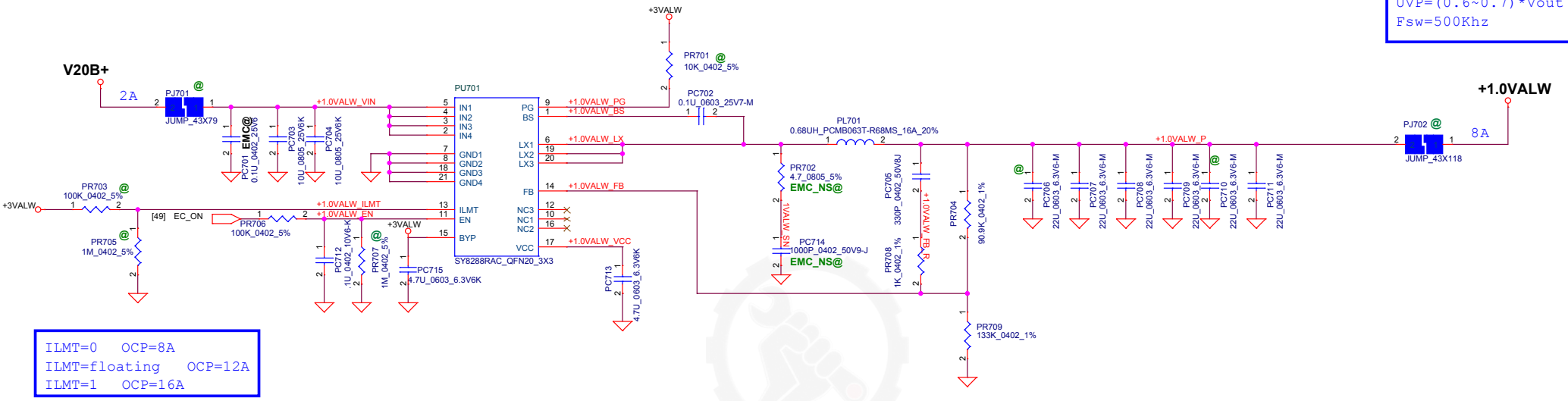


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: ***PWR-2.5V***

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 62 of 75



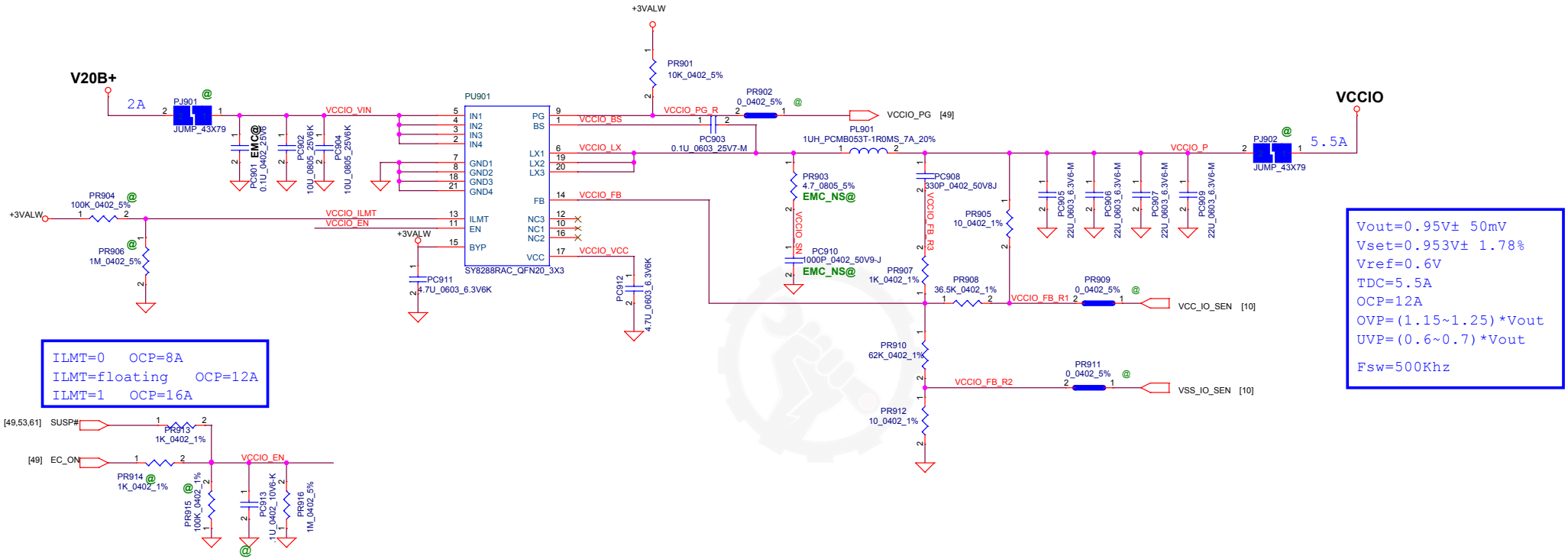
Vout=1.00V± 3%
Vset=1.01V± 1.88%
Vref=0.6V
TDC=8A
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz

ILMT=0 OCP=8A
ILMT=floating OCP=12A
ILMT=1 OCP=16A

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-1.0VALW**

Size: Custom	Document Number: DY510/DY511	Rev: 1.0
Date: Monday, December 19, 2016	Sheet 63 of 75	

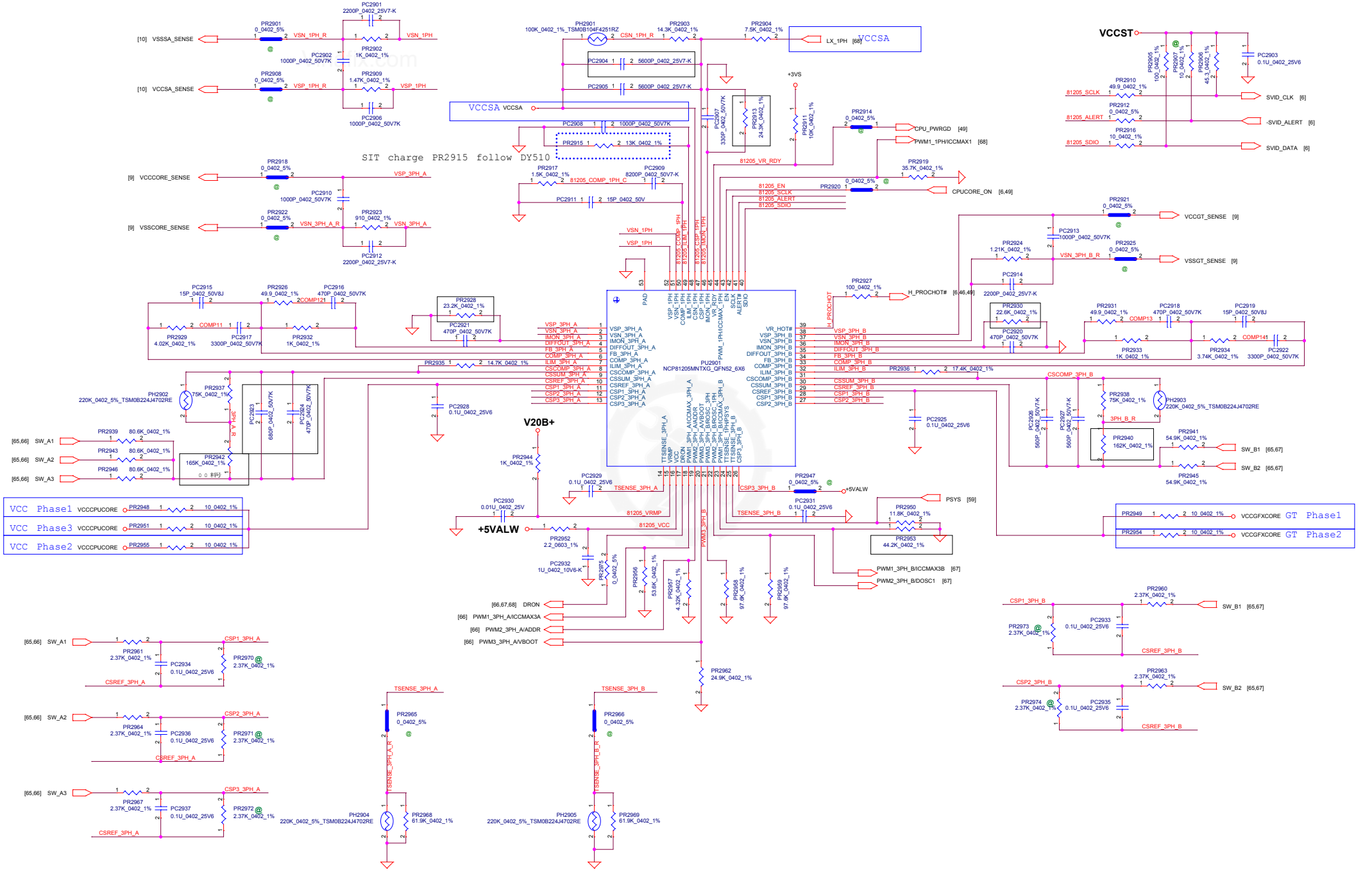


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-VCCIO**

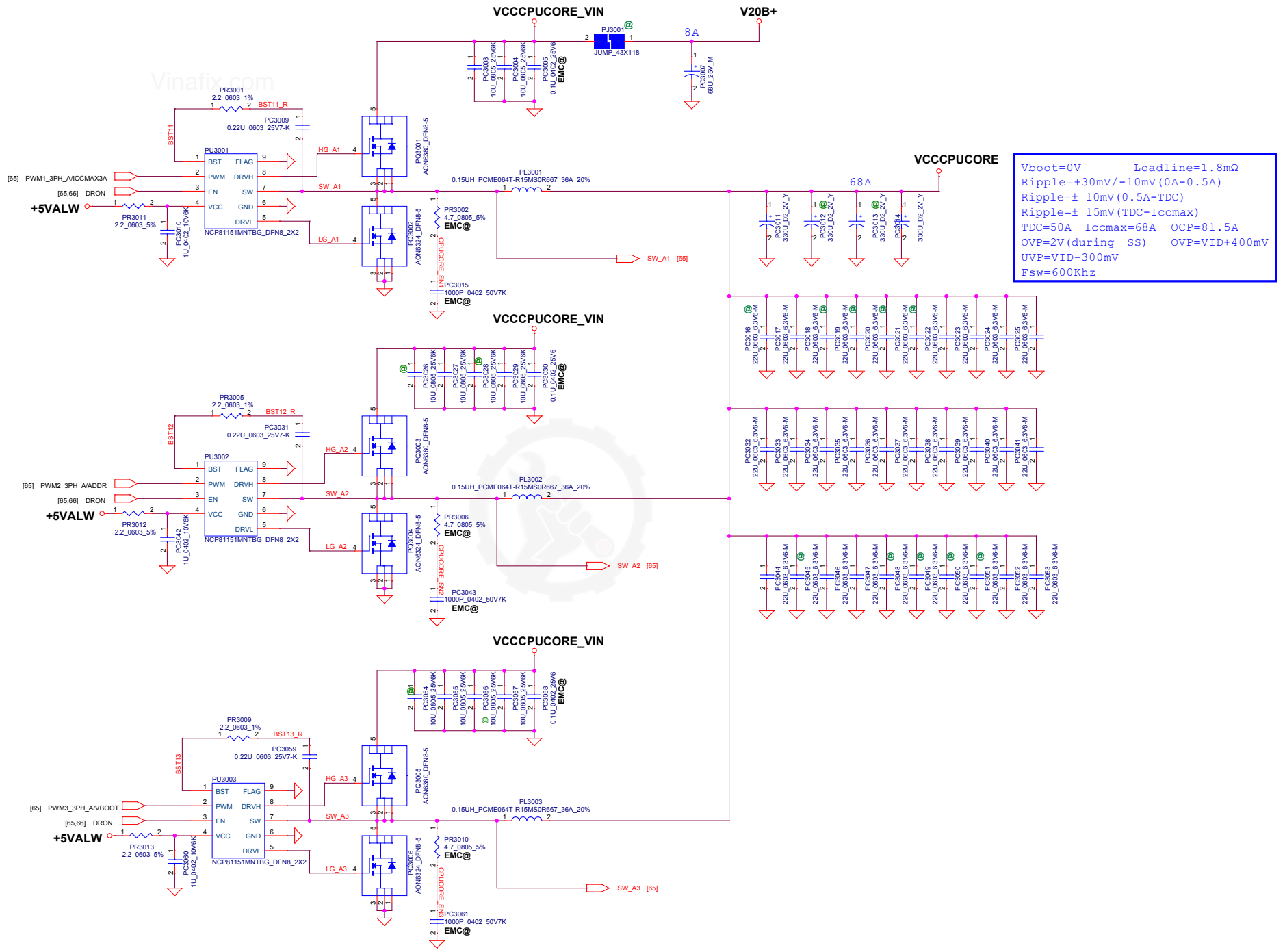
Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 64 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-CPUCORE(NCP81205)		
Size	Document Number	DY510/DY511	Rev 1.0
Custom			
Date:	Monday, December 19, 2016	Sheet	65 of 75

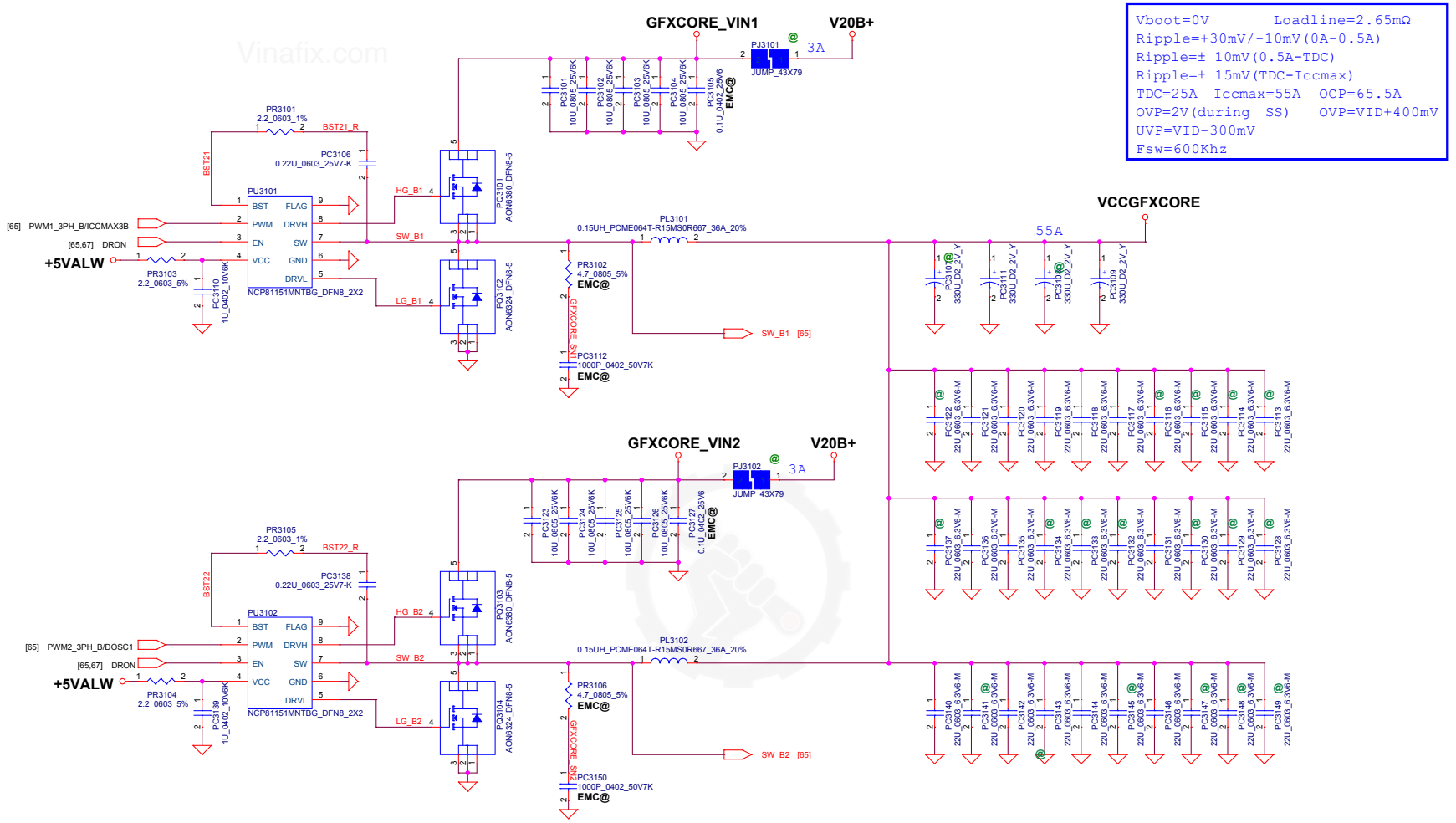


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-CPUCORE**

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 66 of 75



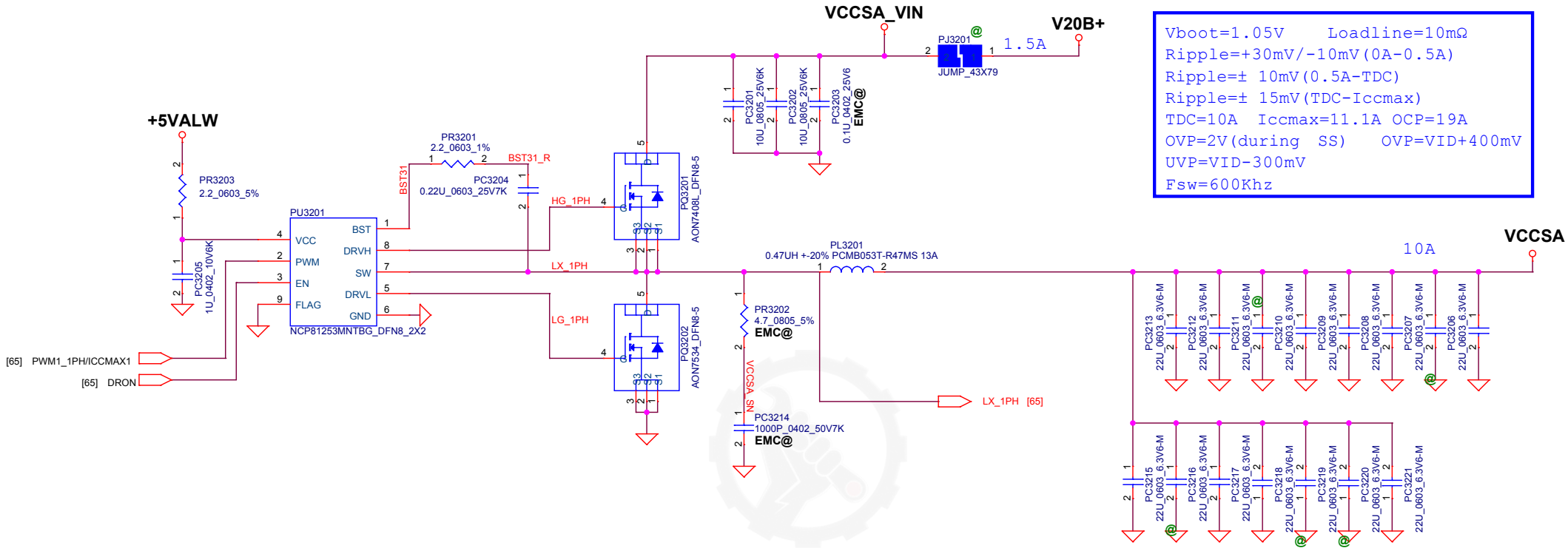
Vboot=0V Loadline=2.65mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=25A Iccmax=55A OCP=65.5A
OVP=2V(during SS) OVP=VID+400mV
UVP=VID-300mV
Fsw=600Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-VCCGFXCORE

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 67 of 75



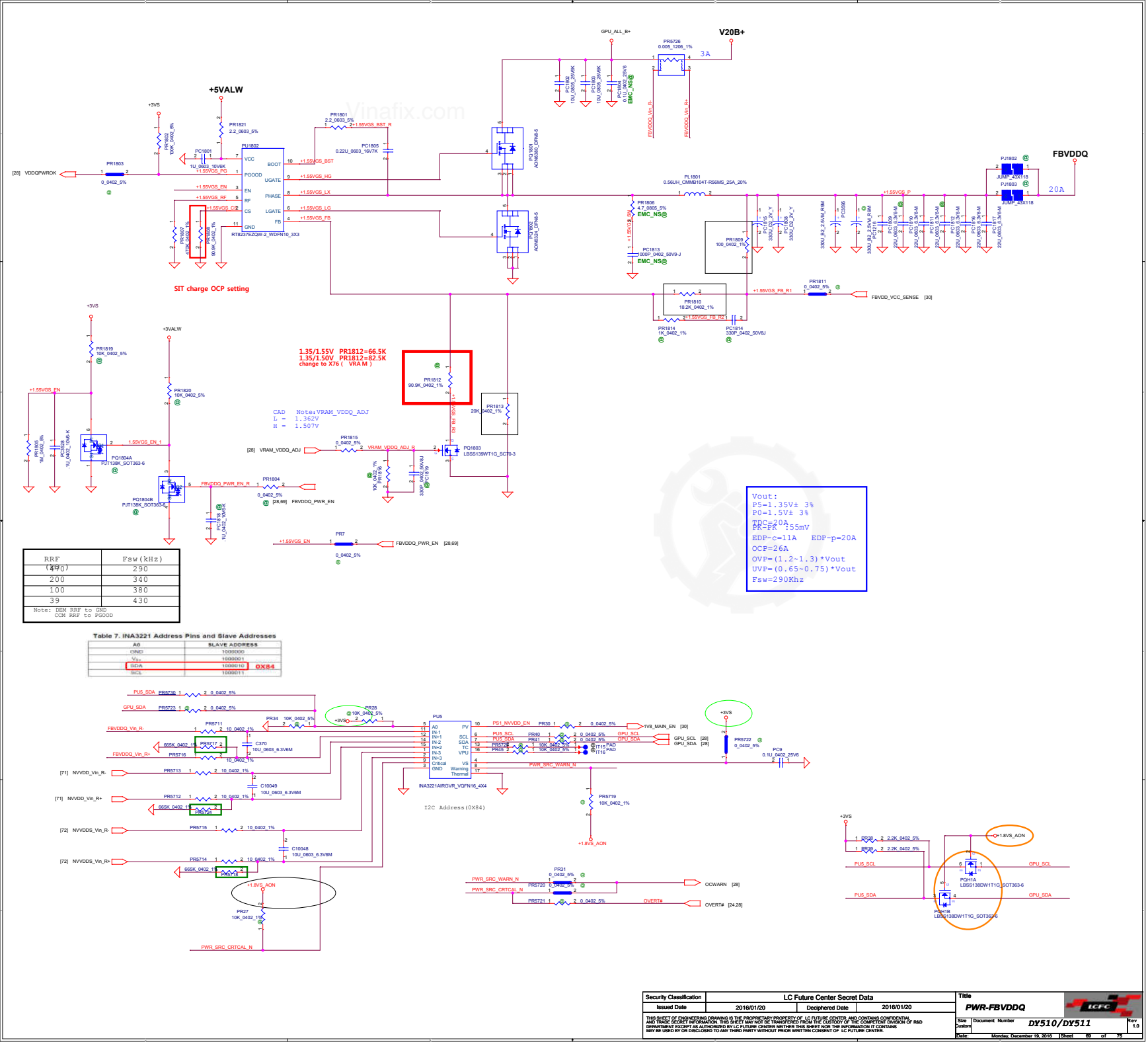
22u-0603 Power 12PCS, 2PCS change to CC140 CC138

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-VCCSA**

Size	Document Number	Rev
B	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 68 of 75



RRF (470)	Fsw(kHz)
200	340
100	380
39	430

Note: DEM RRF to GND
CCM RRF to PGOOD

Table 7. INA3221 Address Pins and Slave Addresses

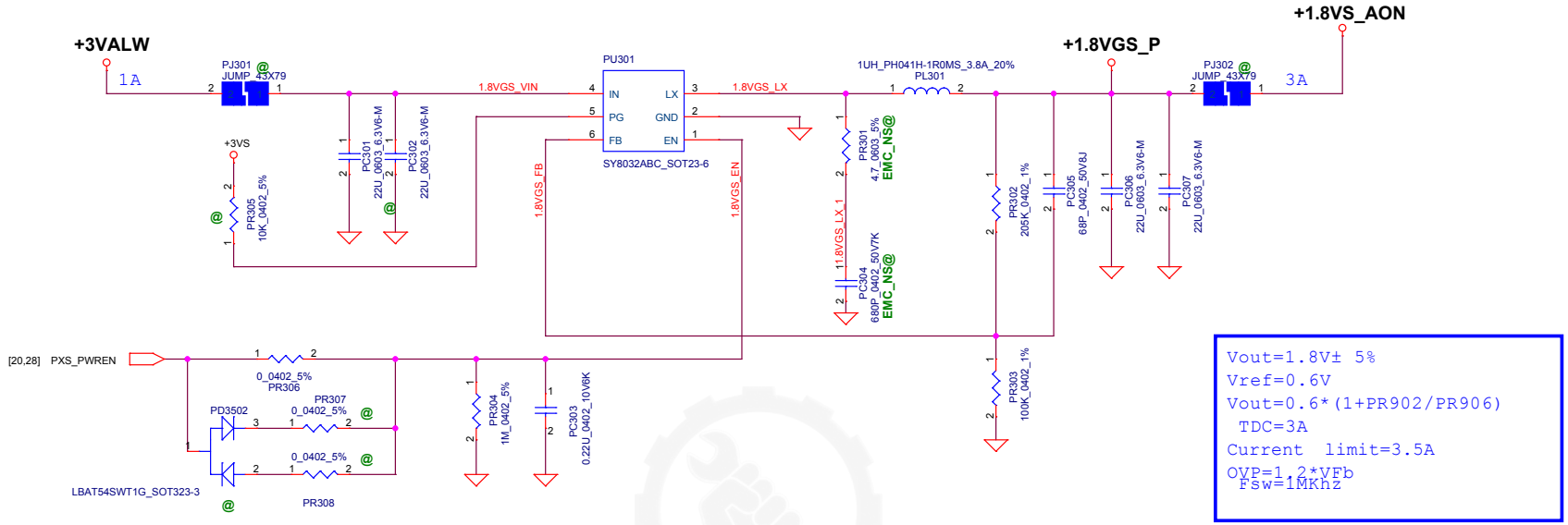
A0	SLAVE ADDRESS
GND	1000000
V_{S+}	1000001
SDA	1000010 0X84
SCL	1000011

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-FBVDDQ

Size: Custom | Document Number: DY510/DY511 | Rev: 1.0

Date: Monday, December 19, 2016 | Sheet 69 of 75



Title	PWR-1.8VGS		
Size: Custom	Document Number: DY510/DY511		Rev: 1.0
Date: Monday, December 19, 2016	Sheet 70 of 75		

PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR5816	6.19
R2(KΩ)	PR5811	20.5
R3(KΩ)	PR5815	4.32
R4(KΩ)	PR5813	16.5
R5(KΩ)	PR5818	0.309
C(nF)	PC5838	4.7

PSI Level	Power Mode	Phase Configuration
PSI<0.4V	PSH	1Phase DEM
0.8V<PSI<1V	PS0	1Phase FCCM
1.4V<PSI<5.5V	PS1	3Phase FCCM

Vboot=0.8V
Ripple=± 20mV
TDC=60A Iccmax=127AOCP= 154A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=345KHz

VR Remote Sense - Tie to GPU sense points

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

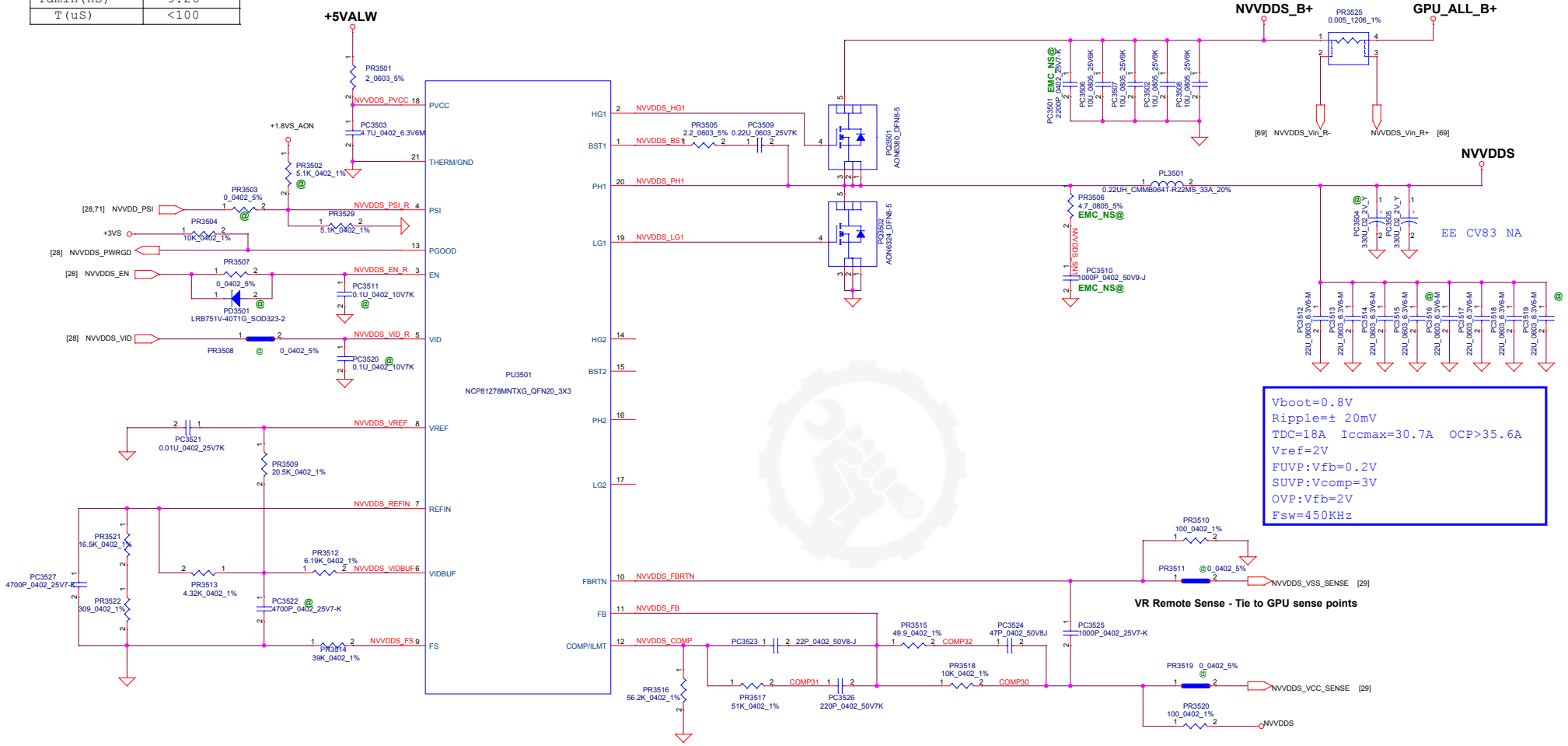
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	PWR-NVVDD		
Size	Document Number		Rev
D	DZ510/DY512		1.0
Date: Monday, December 19, 2016	Sheet 71 of 75		

PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR9440	6.19
R2(KΩ)	PR9434	20.5
R3(KΩ)	PR9436	4.32
R4(KΩ)	PR9437	16.5
R5(KΩ)	PR9431	0.309
C(nF)	PC1277	4.7

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2Phase Auto CCM/DCM
High	PS0	2Phase FCCM
Intermediate	PS1	2Phase Auto CCM
Low	PS2	1Phase Auto CCM/DCM



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-NVVDDS		
Size	Document Number	DY510/DY511	Rev 1.0
C			
Date:	Monday, December 19, 2016	Sheet	72 of 75

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

PWR-VGA_CORE(NCP81174)

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, December 19, 2016 Sheet 73 of 75

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size: D	Document Number: ***DY510/DY511***	Rev: 1.0
Date: Monday, December 19, 2016	Sheet 74 of 75	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size: D	Document Number: ***DY510/DY511***	Rev: 1.0
Date: Monday, December 19, 2016	Sheet 75 of 75	