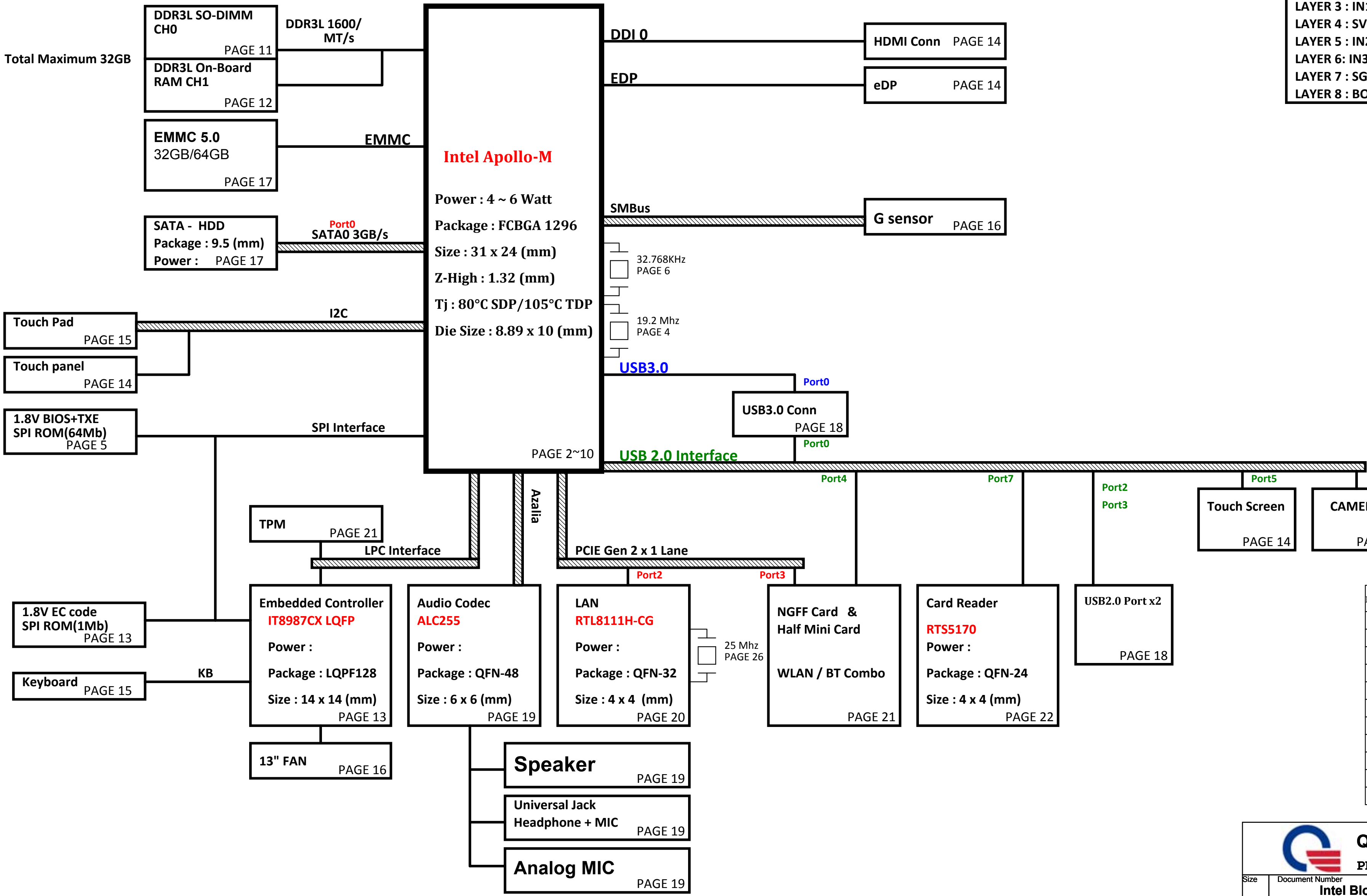
01

EJ-11/13 ZHP/ZSP (11 and 13")

Intel Apollo Platform Block Diagram



PCB 8L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : SVCC
- LAYER 5 : IN2(Low)
- LAYER 6: IN3(High)
- LAYER 7 : SGND
- LAYER 8 : BOT

BOM option	Note
EM@	EMMC
TPS@	Touch Screen
GS@	G-Sensor
AC@	IOAC
NAC@	Non-IOAC
VL@	LED Backlight
DB@	Debug Conn.
*TSI@	Touch Screen I2C
TPM@	DTPM

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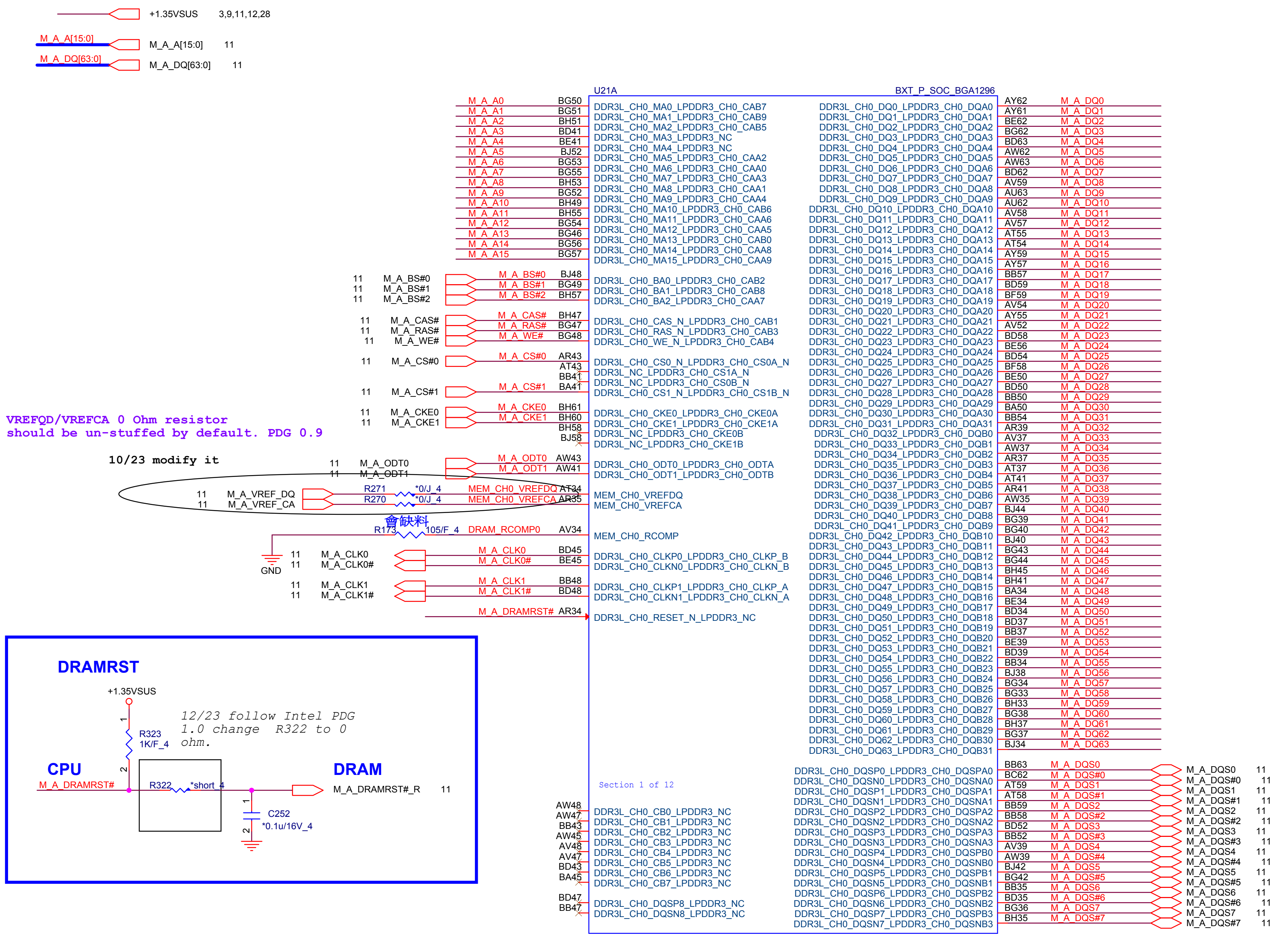
PROJECT : ZHP/ZSP

Size | Document Number: Intel Block Diagram | Rev 1A

Date: Tuesday, July 26, 2016 | Sheet 1 of 36

02



Configuration	Speed (MT/s)	Channels	Raw Card	Maximum Total Capacity (GB)
SODIMM	1333/1600/1867	2	A(2Rx16) C(1Rx16) B(1Rx8) F(2Rx8)	32

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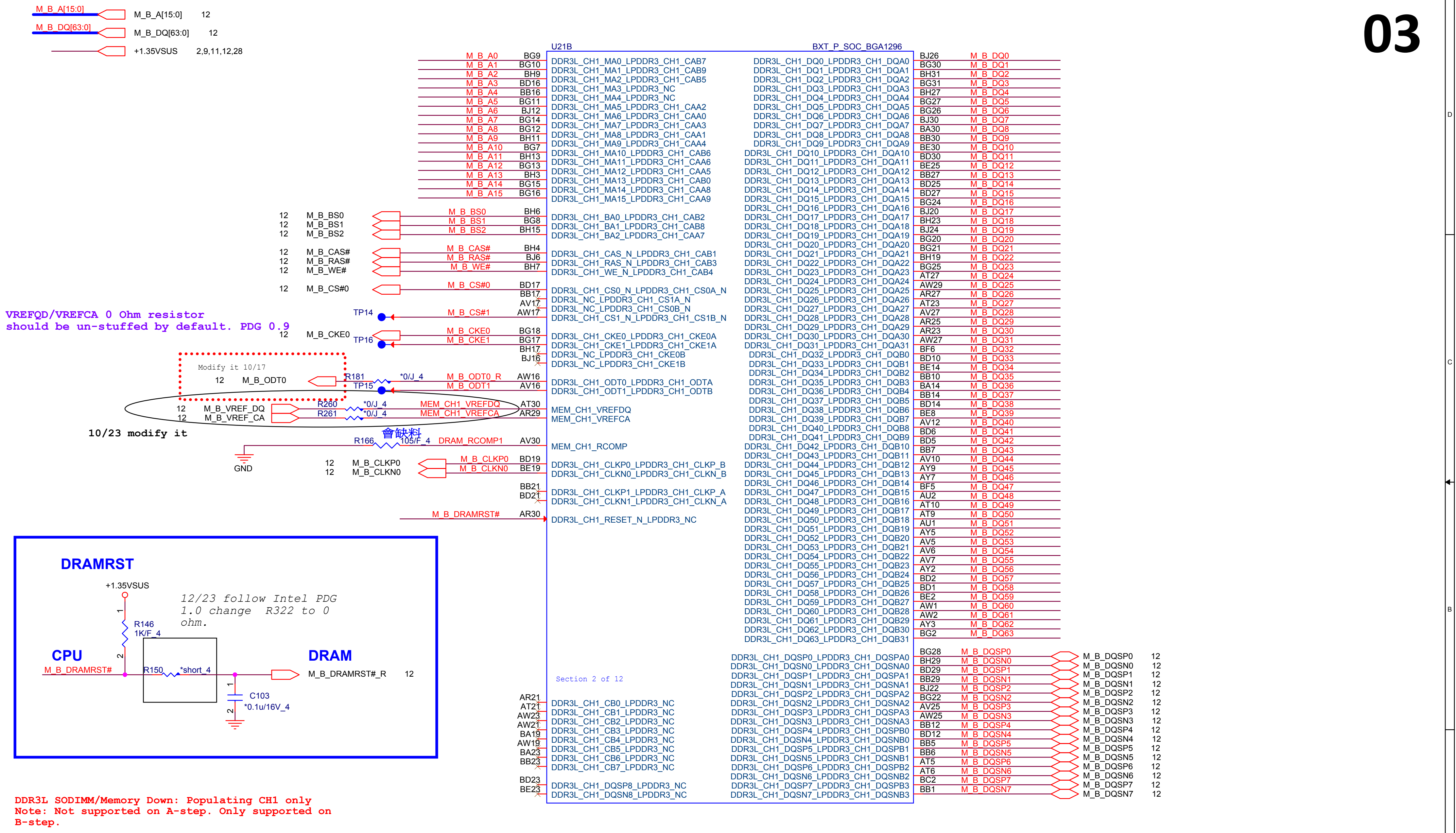
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A

Date: Tuesday, July 26, 2016 Sheet 2 of 36

03



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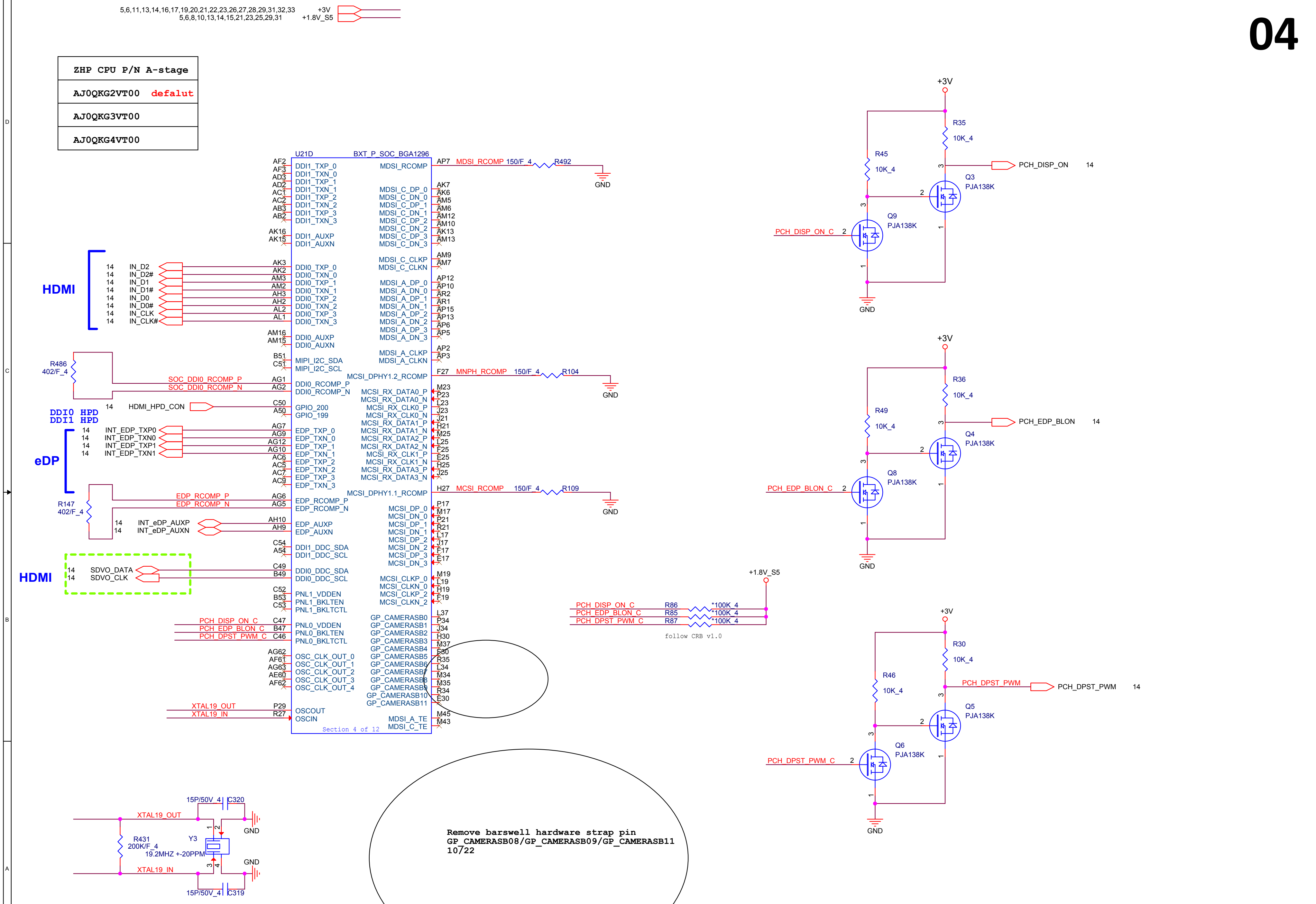
PROJECT : ZHP/ZSP

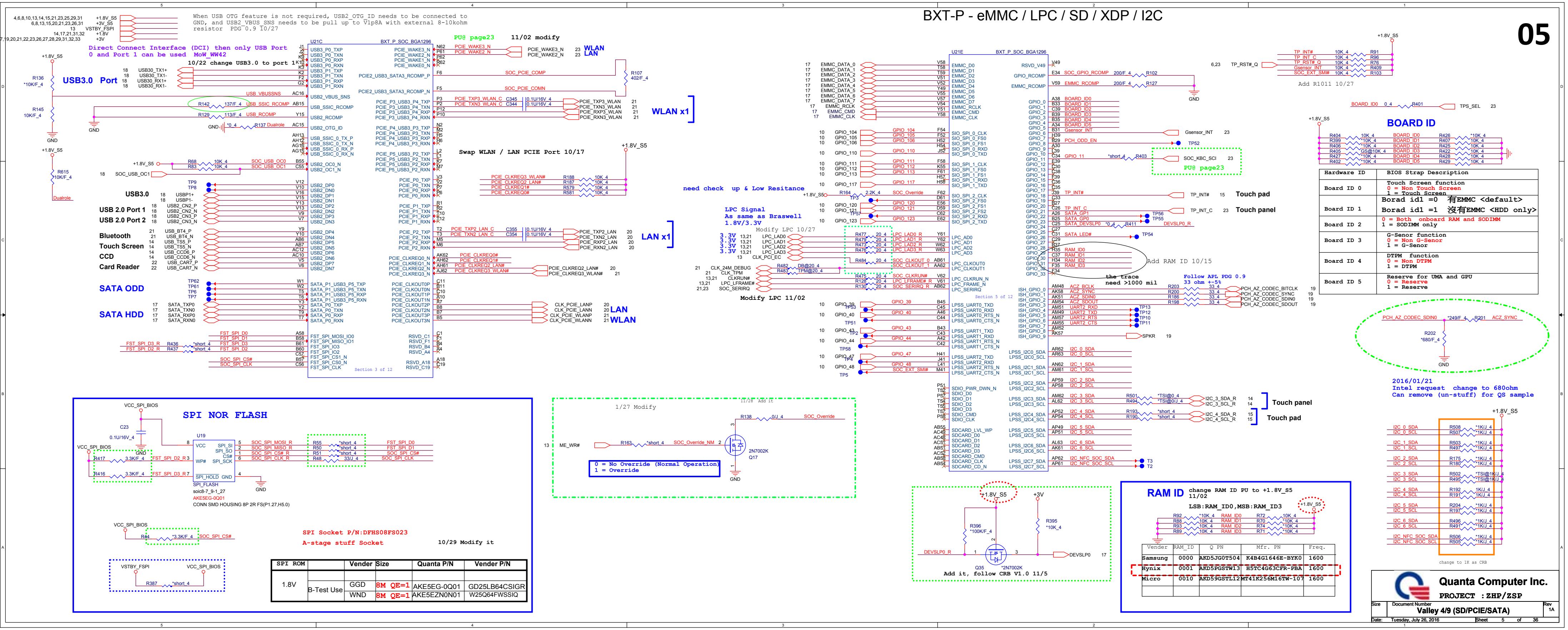
Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

Date: Tuesday, July 26, 2016 Sheet 3 of 36

ZHP CPU P/N A-stage
AJ0QKG2VT00 defalut
AJ0QKG3VT00
AJ0QKG4VT00



2nd source:BG619200014 (TXC)



Hardware ID	BIOS Strap Description
Board ID 0	Touch Screen function 0 = Non Touch Screen 1 = Touch Screen
Board ID 1	Borad id1 =0 有EMMC <default> Borad id1 =1 沒有EMMC <HDD only>
Board ID 2	0 = Both onboard RAM and SODIMM 1 = SODIMM only
Board ID 3	G-Senor function 0 = Non G-Senor 1 = G-Senor
Board ID 4	DTPM function 0 = Non DTPM 1 = DTPM
Board ID 5	Reserve for UMA and GPU 0 = Reserve 1 = Reserve

SPI ROM		Vender	Size	Quanta P/N	Vender P/N
1.8V	B-Test Use	GGD	8M QE=1	AKE5EG-0Q01	GD25LB64CSIGR
		WND	8M QE=1	AKE5EZN0N01	W25Q64FWSSIQ

Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Samsung	0000	AKD5JG0T504	K4B4G1646E-BYK0	1600
Hynix	0001	AKD5PGSTW13	H5TC4G63CFR-PBA	1600
Micro	0010	AKD59GSTL12	MT41K256M16TW-107	1600

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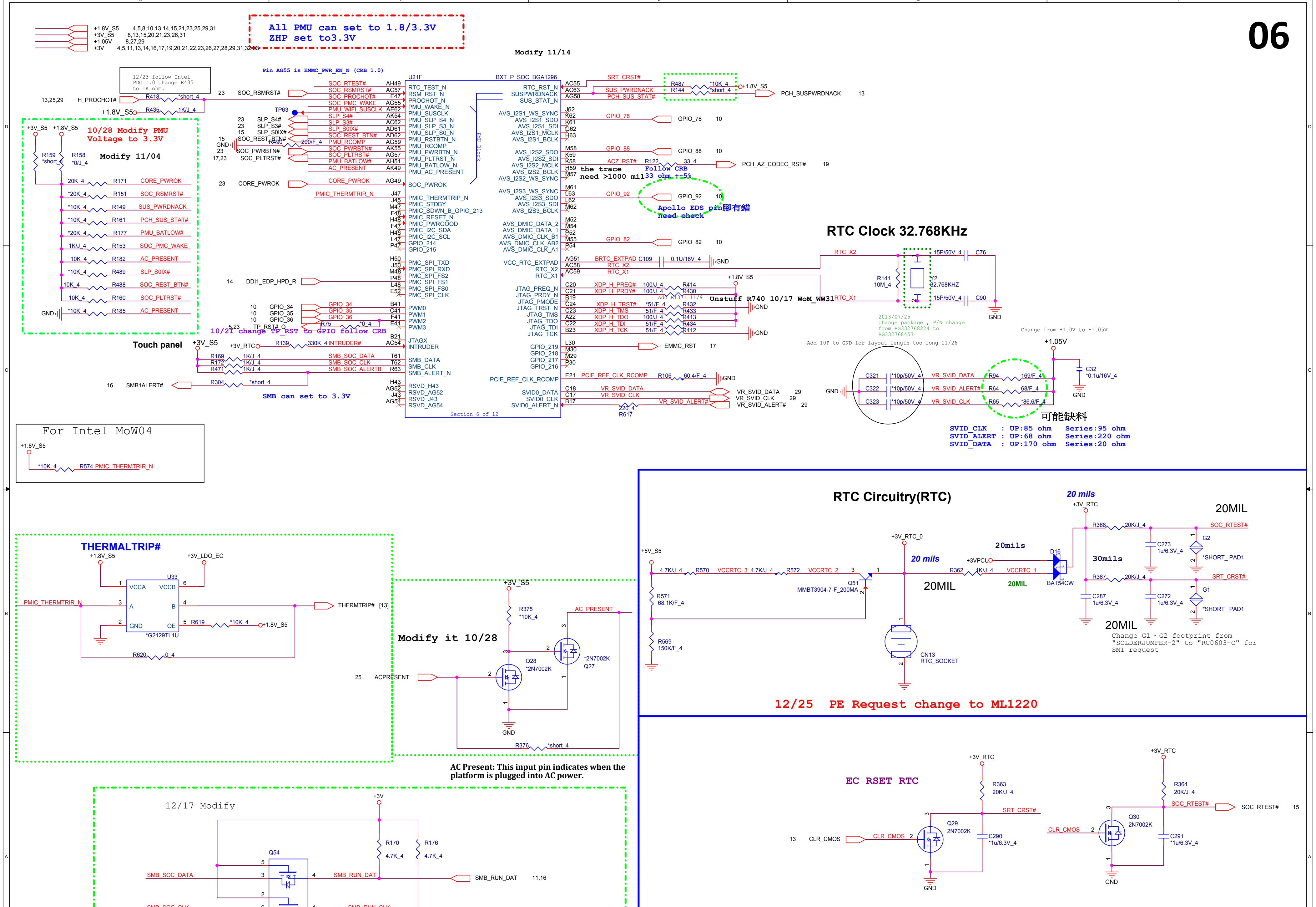
PROJECT : ZHP/ZSP

Size | Document Number: Valley 4/9 (SD/PCIE/SATA) | Rev 1A

Date: Tuesday, July 26, 2016 | Sheet 5 of 36

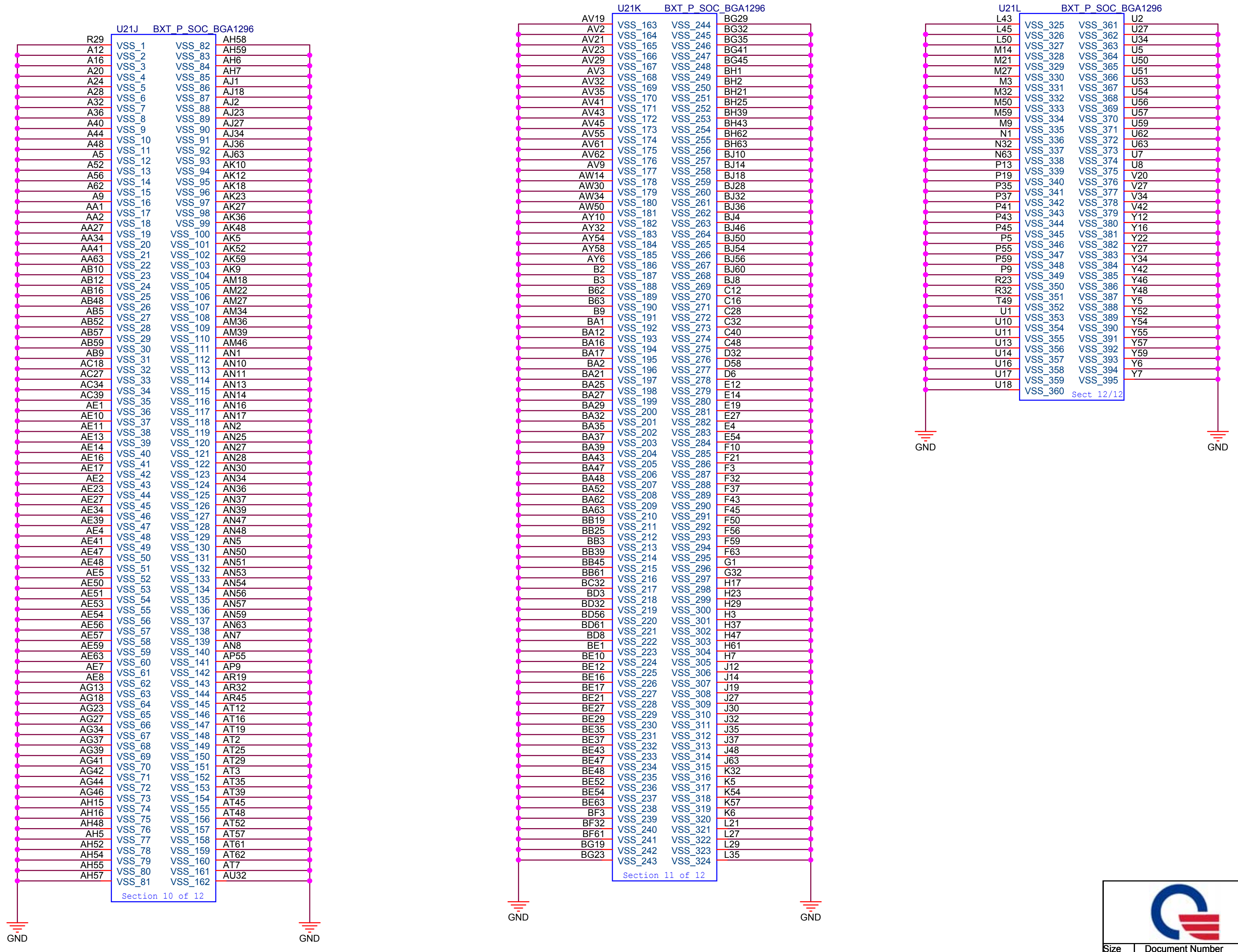


Quanta Computer Inc.

PROJECT : ZHP/ZSP

Document Number: Valley 6/9 (USB/LPC/I2C) — Rev 1A

Date: Tuesday, July 26, 2016 — Sheet 6 of 36



Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 7/9 (Power 1)	1A

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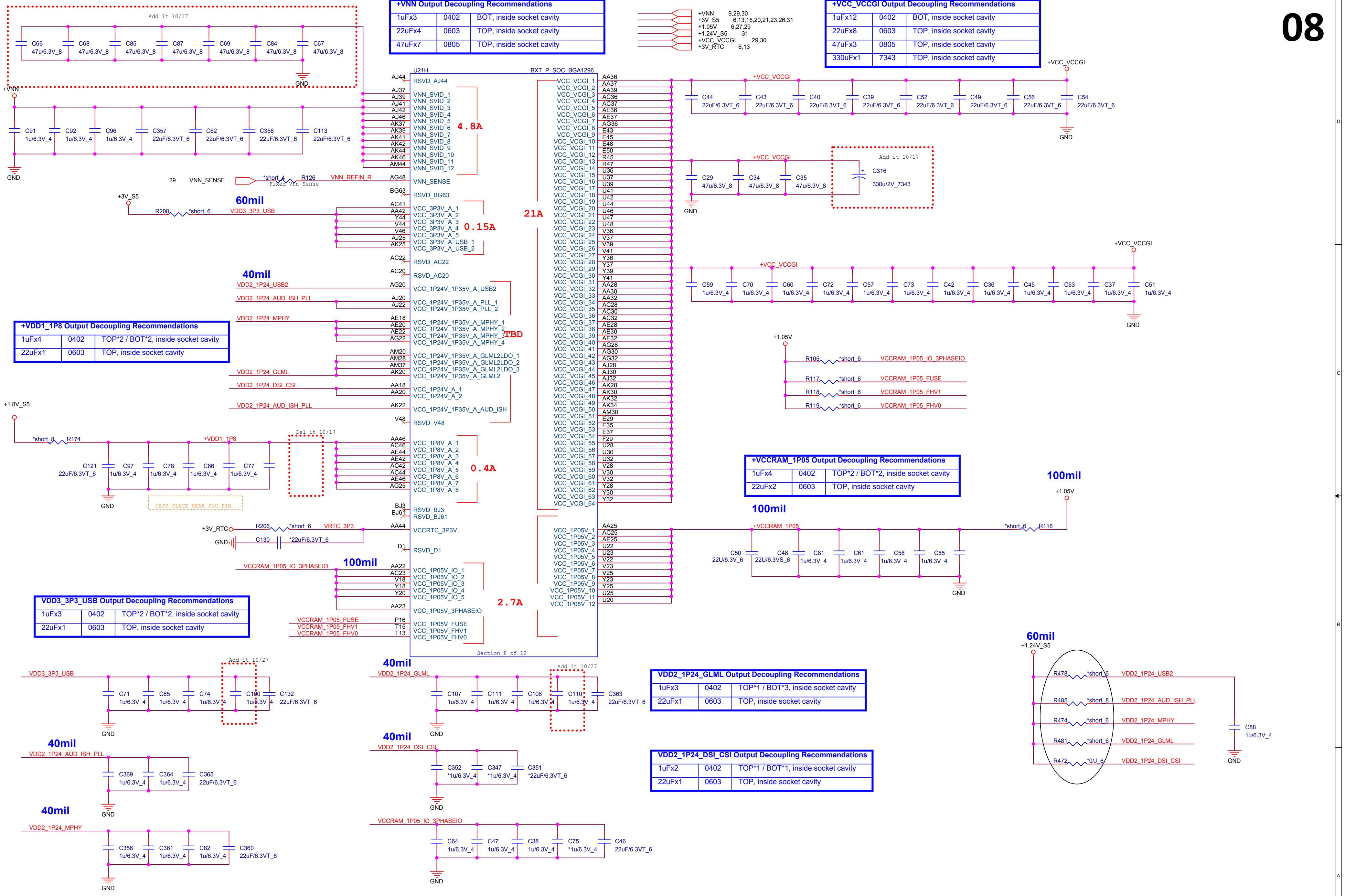
08



+VNN Output Decoupling Recommendations		
1uFx3	0402	BOT, inside socket cavity
22uFx4	0603	TOP, inside socket cavity
47uFx7	0805	TOP, inside socket cavity

+VCC_VCCGI Output Decoupling Recommendations		
1uFx12	0402	BOT, inside socket cavity
22uFx8	0603	TOP, inside socket cavity
47uFx3	0805	TOP, inside socket cavity
330uFx1	7343	TOP, inside socket cavity

+VDD1_1P8 Output Decoupling Recommendations		
1uFx4	0402	TOP*2 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

+VCCRAM_1P05 Output Decoupling Recommendations		
1uFx4	0402	TOP*2 / BOT*2, inside socket cavity
22uFx2	0603	TOP, inside socket cavity

VDD3_3P3_USB Output Decoupling Recommendations		
1uFx3	0402	TOP*2 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

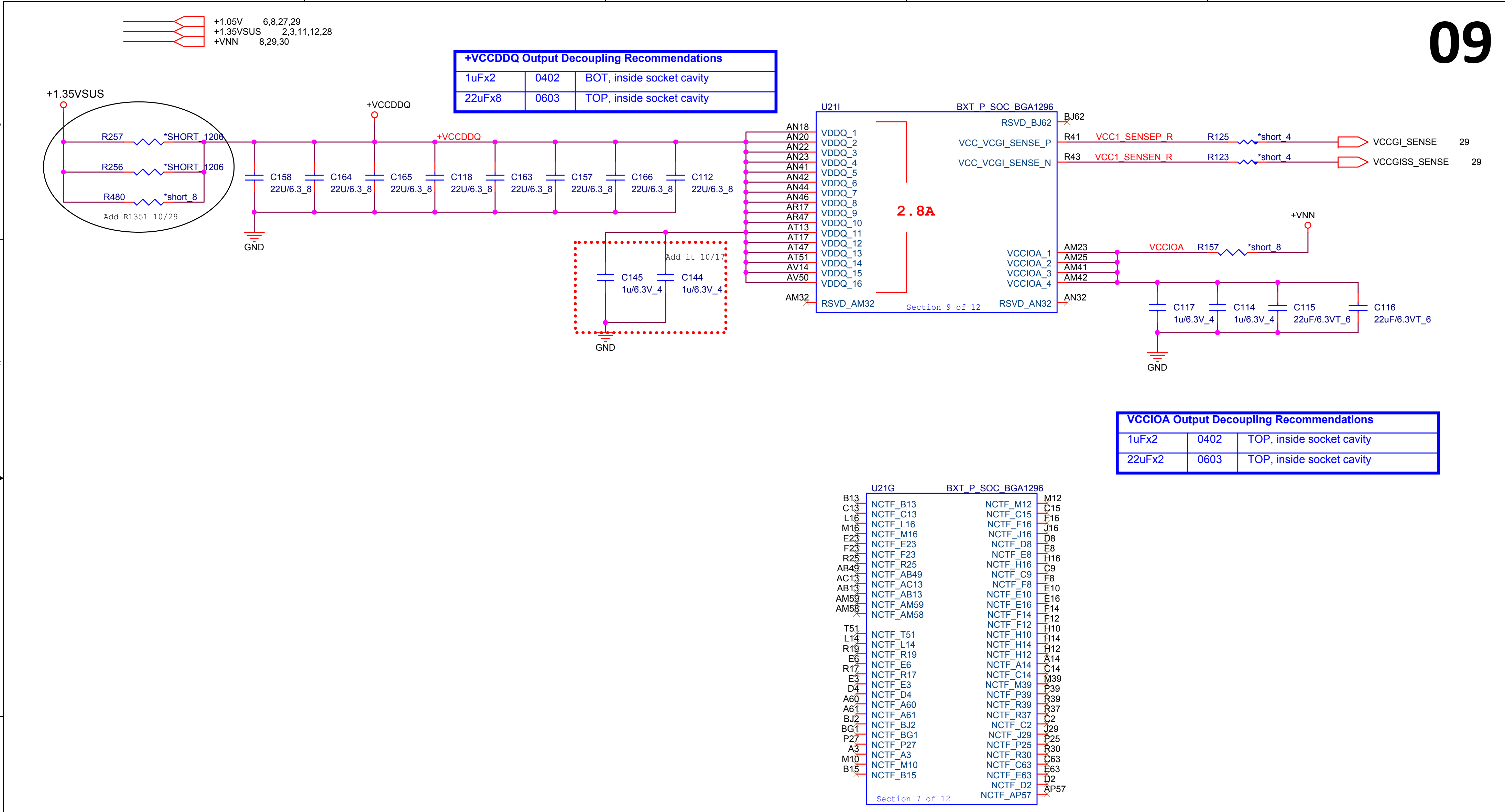
VDD2_1P24_GLML Output Decoupling Recommendations		
1uFx3	0402	TOP*1 / BOT*3, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_DSI_CSI Output Decoupling Recommendations		
1uFx2	0402	TOP*1 / BOT*1, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_AUD_ISH_PLL Output Decoupling Recommendations		
1uFx2	0402	TOP*1 / BOT*1, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VCCRAM_1P05_IO_3PHASEIO Output Decoupling Recommendations		
1uFx4	0402	TOP*2 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_MPHY Output Decoupling Recommendations		
1uFx3	0402	TOP*1 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity



+VCCDDQ Output Decoupling Recommendations

1uFx2	0402	BOT, inside socket cavity
22uFx8	0603	TOP, inside socket cavity

VCCIOA Output Decoupling Recommendations

1uFx2	0402	TOP, inside socket cavity
22uFx2	0603	TOP, inside socket cavity

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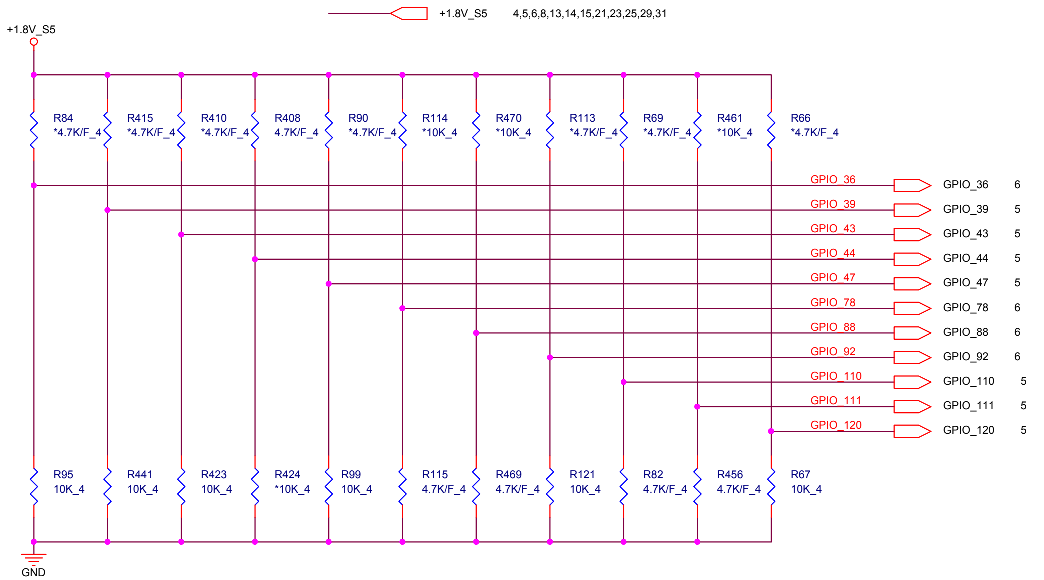
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Tuesday, July 26, 2016 Sheet 9 of 36

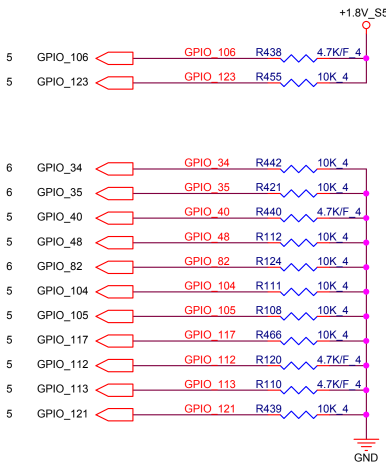


Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = Disable 1 = Enable

Note: This strap will only be used for B-step.
For A-step this rails should only be set at 1.24V

B Stage change to 3.3V

Hardware Strap to enable boot from SPI
If the platform design wants to have BIOS Boot form SPI then please ensure you have the following setting for hardware strap:
GPIO_43 = 0 [Disable eMMC boot]
GPIO_44 = 1 [Enable SPI Boot]
MoW_WW36



Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_40/GPIO_48/GPIO_104/GPIO_105/GPIO_112/GPIO_113/GPIO_117/GPIO_121 PD
GPIO_106/GPIO_123 PU

Quanta Computer Inc.
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Hardware Strap	1A

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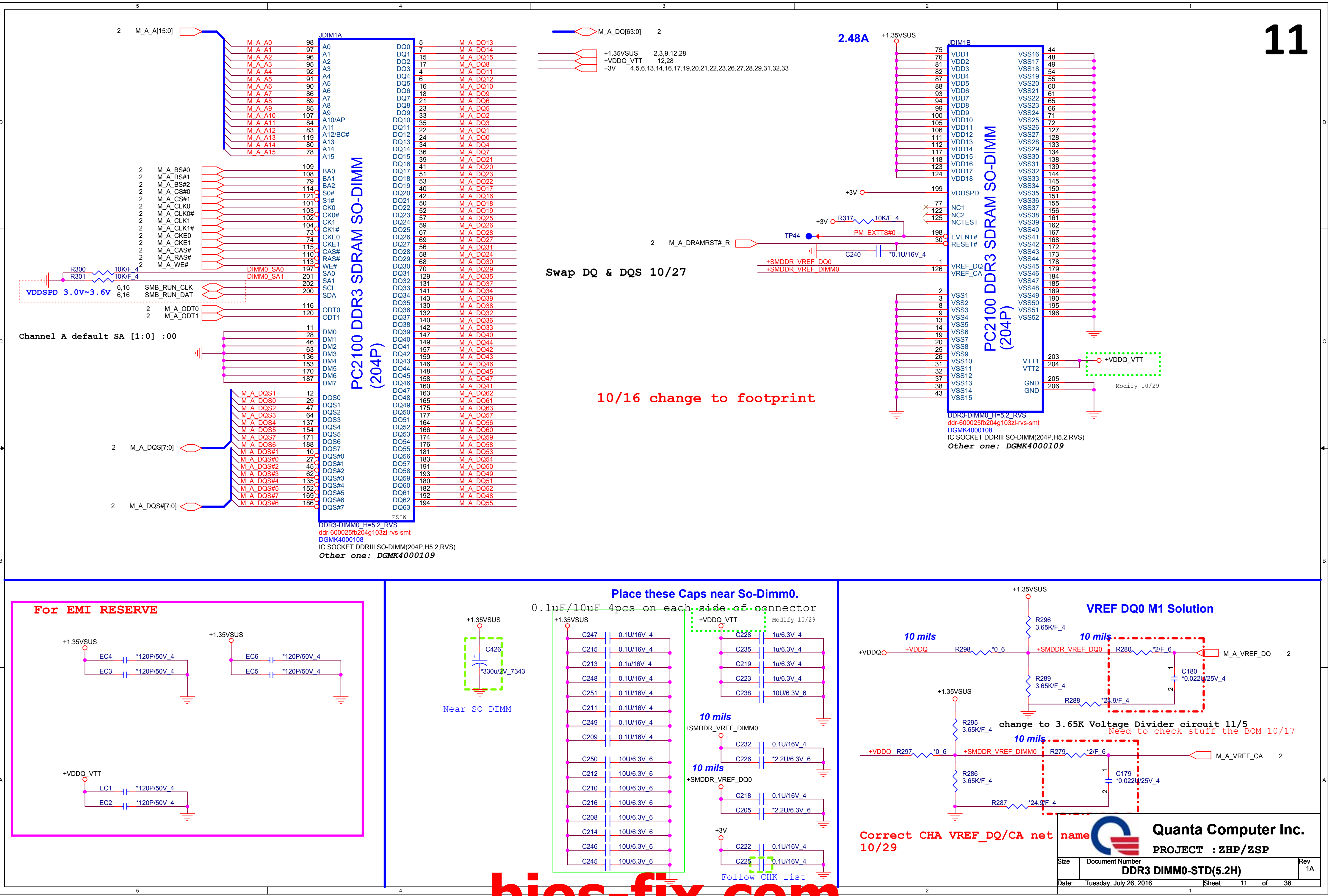
11
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
M_A_A[15:0]
M_A_DQ[63:0]
M_A_DQS[7:0]
M_A_DQS#[7:0]
VDDSPD 3.0V~3.6V
Channel A default SA [1:0] :00
DDR3-DIMM0_H=5.2_RVS
ddr-600025fb204g103zl-rvs-smt
DGMK4000108
IC SOCKET DDRIII SO-DIMM(204P,H5.2,RVS)
Other one: DGMK4000109
Swap DQ & DQS 10/27
2.48A
+1.35VSUS
JDIM1B
10/16 change to footprint
Modify 10/29
For EMI RESERVE
Place these Caps near So-Dimm0.
0.1uF/10uF 4pcs on each side of connector
Near SO-DIMM
Follow CHK list
VREF DQ0 M1 Solution
10 mils
change to 3.65K Voltage Divider circuit 11/5
Need to check stuff the BOM 10/17
Correct CHA VREF_DQ/CA net name 10/29
Quanta Computer Inc.
PROJECT : ZHP/ZSP
DDR3 DIMM0-STD(5.2H)
Rev 1A
Date: Tuesday, July 26, 2016
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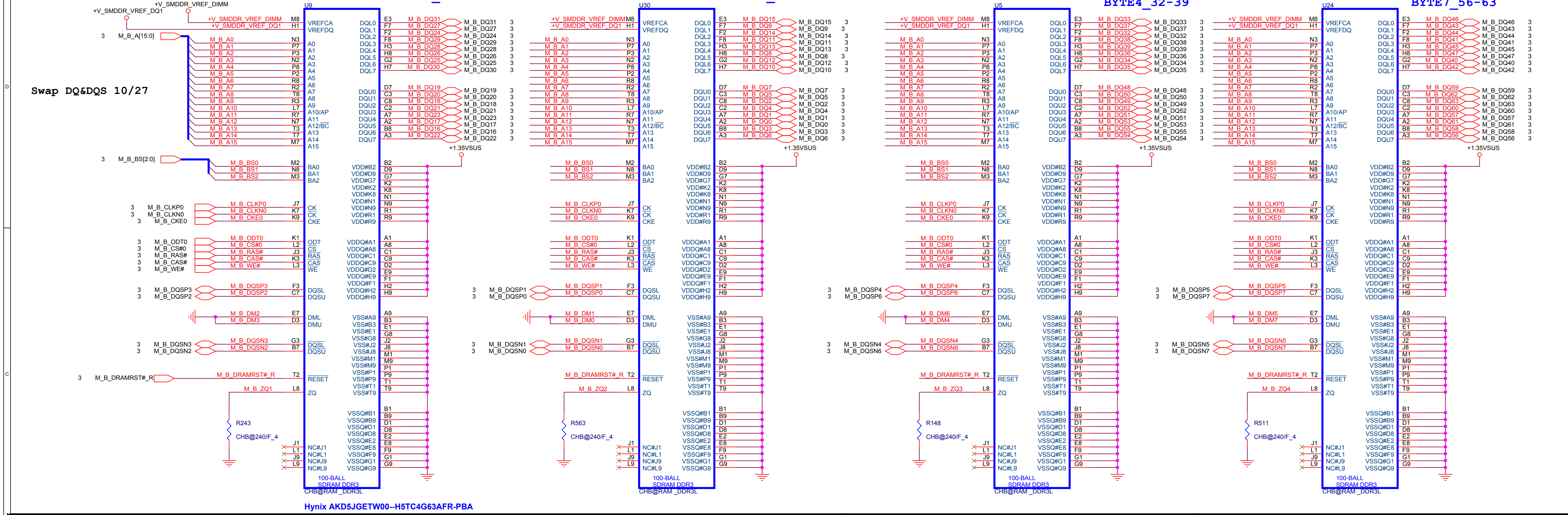
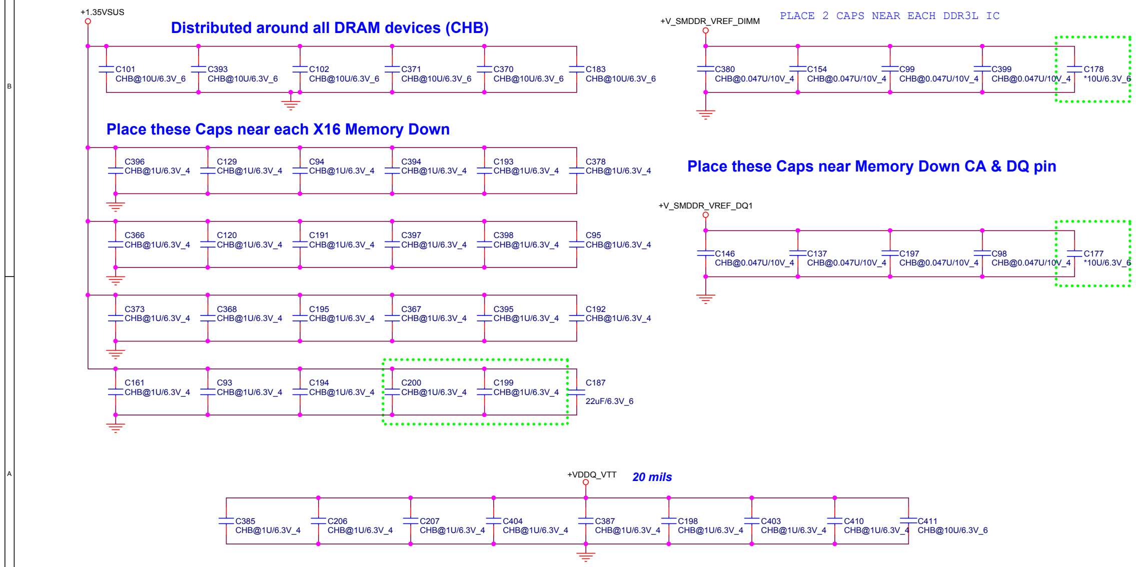
On board memory(OBM)

DDR3L MEMORY CHANNEL B

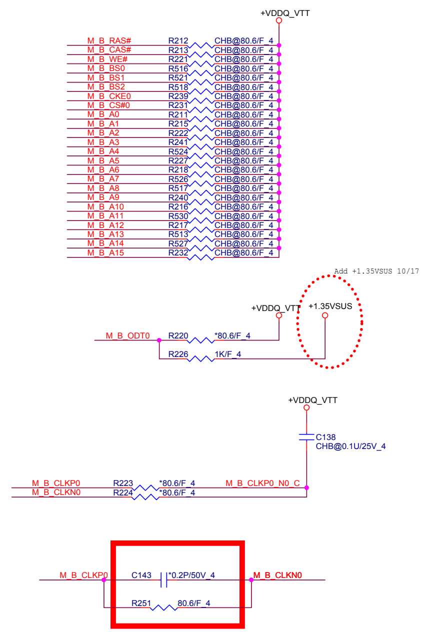
Swap DQ&DQS 10/27



DE-CAPS FOR MEMORY CHANNEL B

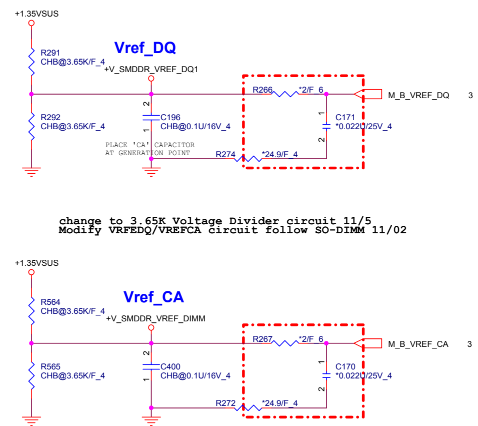


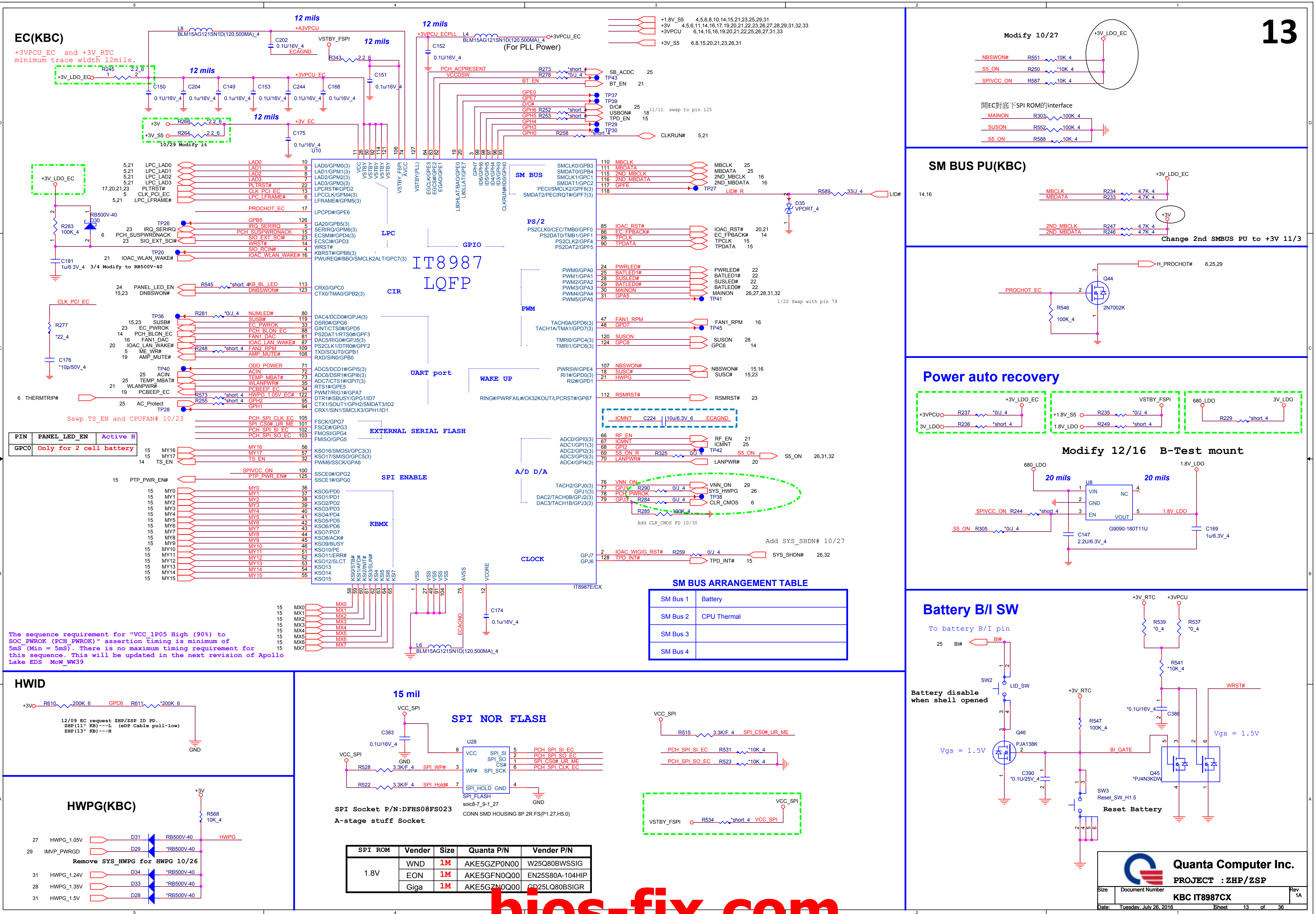
VTT TERMINATIONS



VREF_DQ CIRCUIT

VREF_CA CIRCUIT





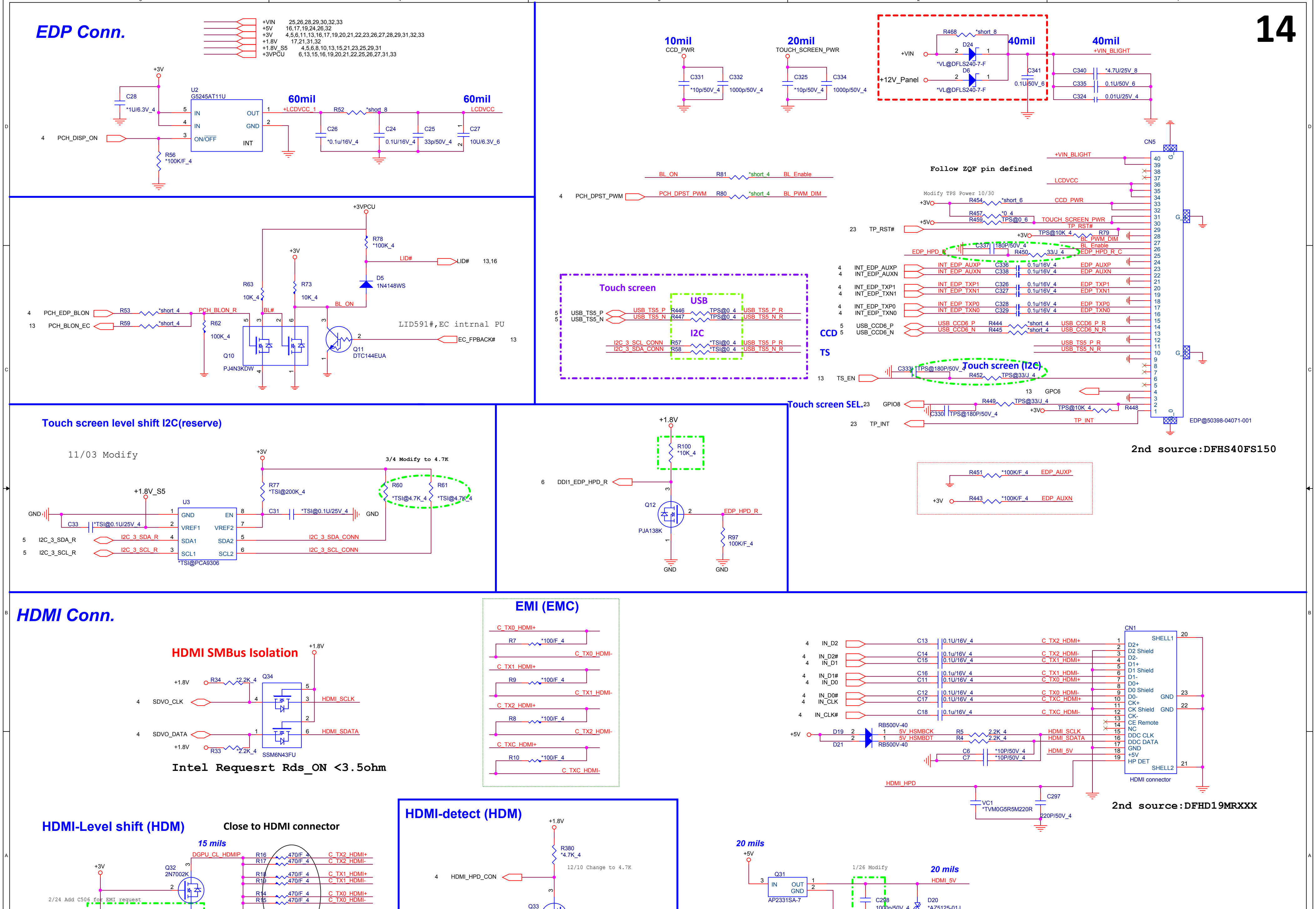
PIN	PANEL_LED_EN	Active H
GPC0	Only for 2 cell battery	

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU Thermal
SM Bus 3	
SM Bus 4	

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	1M	AKE5GZP0N00	W25Q80BWSSIG
	EON	1M	AKE5GFN0Q00	EN25S80A-104HIP
	Giga	1M	AKE5GZN0Q00	GD25LQ80BSIGR

Quanta Computer Inc.
PROJECT : ZHP/ZSP
Document Number: KBC IT8987CX
Rev 1A
Date: Tuesday, July 26, 2016 Sheet 13 of 36



Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	LCD/HDMI/Camera	1A
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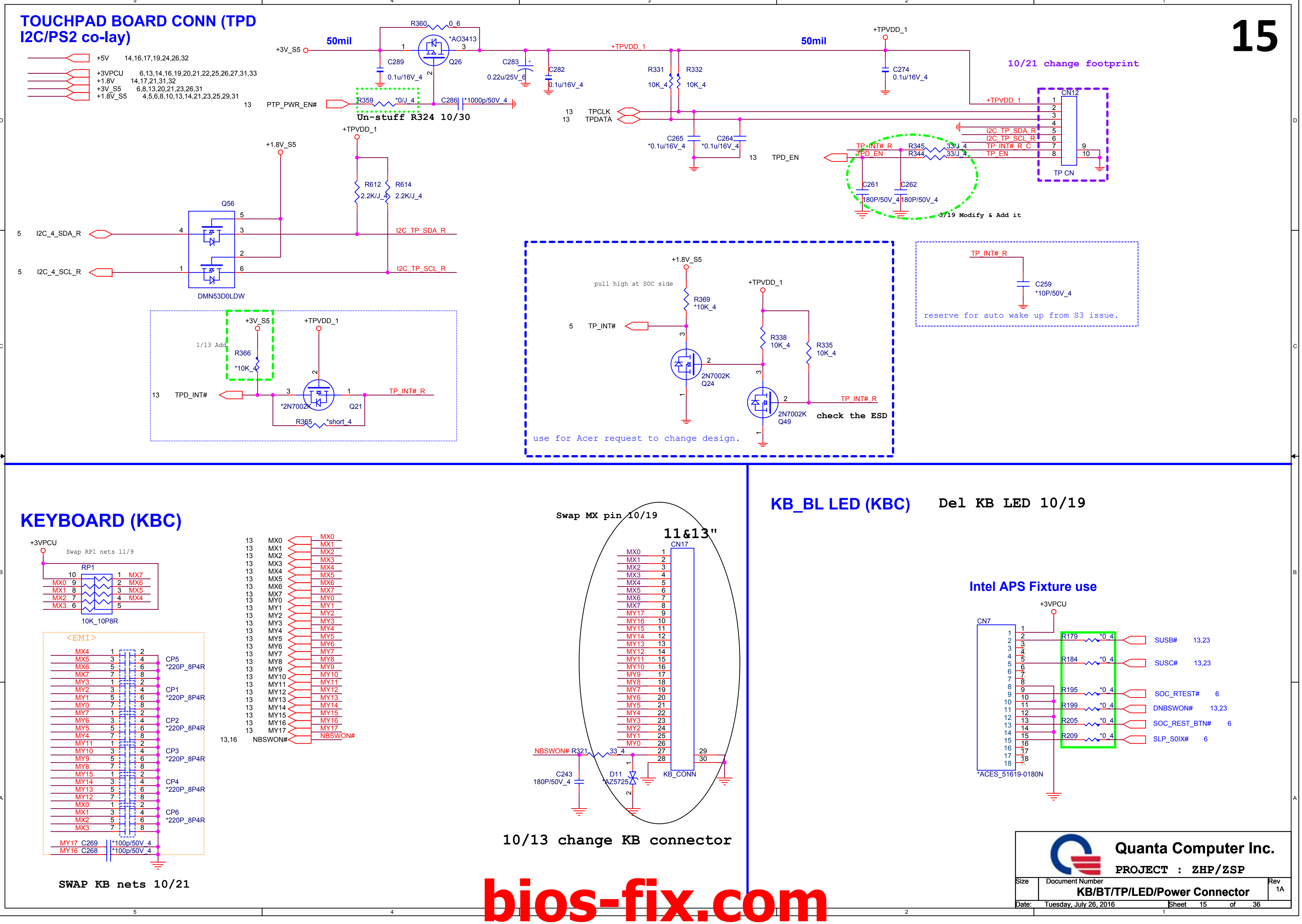
15
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)
+5V 14,16,17,19,24,26,32
+3VPCU 6,13,14,16,19,20,21,22,25,26,27,31,33
+1.8V 14,17,21,31,32
+3V_S5 6,8,13,20,21,23,26,31
+1.8V_S5 4,5,6,8,10,13,14,21,23,25,29,31
50mil
50mil
R360 0_6
*AO3413
Q26
C289 0.1u/16V_4
C283 0.22u/25V_6
C282 0.1u/16V_4
+TPVDD_1
R331 10K_4
R332 10K_4
C274 0.1u/16V_4
10/21 change footprint
13 PTP_PWR_EN#
R359 *0/J_4
C286 *1000p/50V_4
Un-stuff R324 10/30
13 TPCLK
13 TPDATA
C265 *0.1u/16V_4
C264 *0.1u/16V_4
13 TPD_EN
CN12
TP CN
I2C_TP_SDA_R
I2C_TP_SCL_R
TP_INT#_R_C
TP_EN
R345 33/J_4
R344 33/J_4
C261 180P/50V_4
C262 180P/50V_4
3/19 Modify & Add it
+1.8V_S5
R612 2.2K/J_4
R614 2.2K/J_4
Q56
DMN53D0LDW
5 I2C_4_SDA_R
5 I2C_4_SCL_R
I2C_TP_SDA_R
I2C_TP_SCL_R
1/13 Add
R366 *10K_4
13 TPD_INT#
*2N7002K
Q21
TP_INT#_R
R365 *short_4
pull high at SOC side
R369 *10K_4
5 TP_INT#
2N7002K Q24
R338 10K_4
R335 10K_4
2N7002K Q49
TP_INT#_R
check the ESD
use for Acer request to change design.
C259 *10P/50V_4
reserve for auto wake up from S3 issue.
KEYBOARD (KBC)
+3VPCU
Swap RP1 nets 11/9
RP1
10K_10P8R
<EMI>
CP5 *220P_8P4R
CP1 *220P_8P4R
CP2 *220P_8P4R
CP3 *220P_8P4R
CP4 *220P_8P4R
CP6 *220P_8P4R
MY17 C269 *100p/50V_4
MY16 C268 *100p/50V_4
SWAP KB nets 10/21
13,16 NBSWON#
Swap MX pin 10/19
11&13"
CN17
KB_CONN
NBSWON# R321 33_4
C243 180P/50V_4
D11 *AZ5725
10/13 change KB connector
KB_BL LED (KBC)
Del KB LED 10/19
Intel APS Fixture use
+3VPCU
CN7
*ACES_51619-0180N
R179 *0_4 SUSB# 13,23
R184 *0_4 SUSC# 13,23
R195 *0_4 SOC_RTEST# 6
R199 *0_4 DNBSWON# 13,23
R205 *0_4 SOC_REST_BTN# 6
R209 *0_4 SLP_S0IX# 6
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Document Number
KB/BT/TP/LED/Power Connector
Rev 1A
Date: Tuesday, July 26, 2016
Sheet 15 of 36
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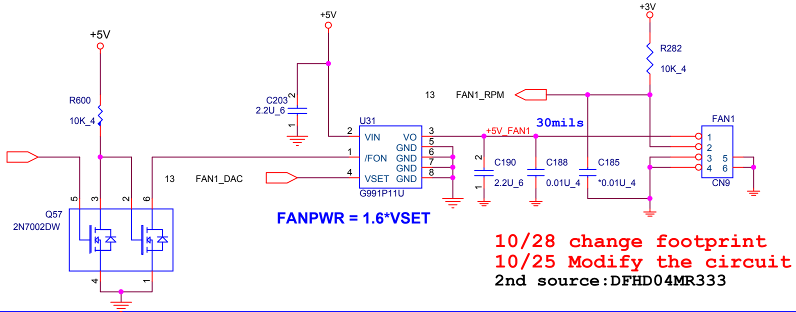
CPU FAN CTRL(THM)

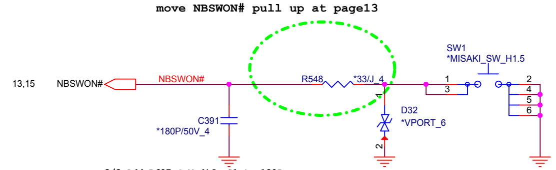


FANPWR = 1.6*VSET

10/28 change footprint
10/25 Modify the circuit
2nd source:DFHD04MR333

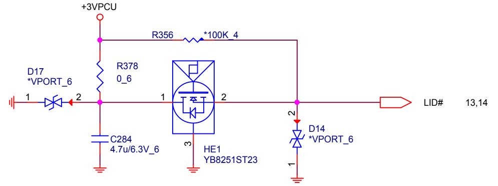
Power Switch. (FSW)

move NBSWON# pull up at page13



3/3 Add R697 & Modify C1 to 180P

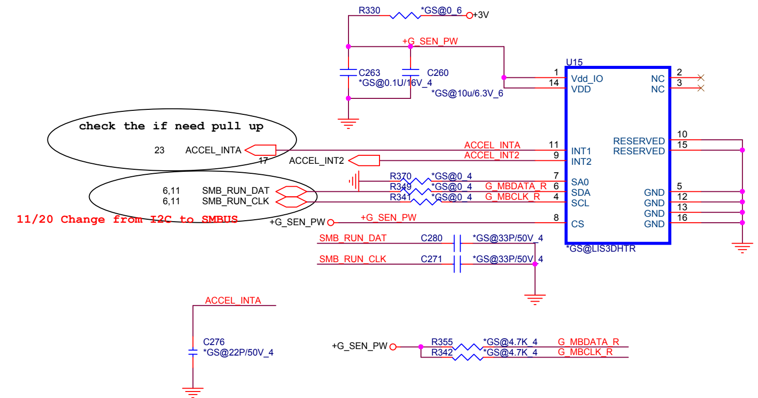
Hall Sensor (HSR)



1st：YB8251000-- YBT
2nd：AL001691000 -- OCS

Modify 10/31

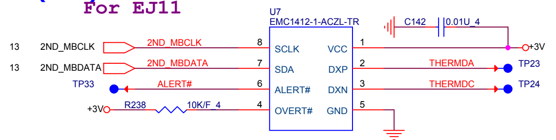
G-sensor(GRS)



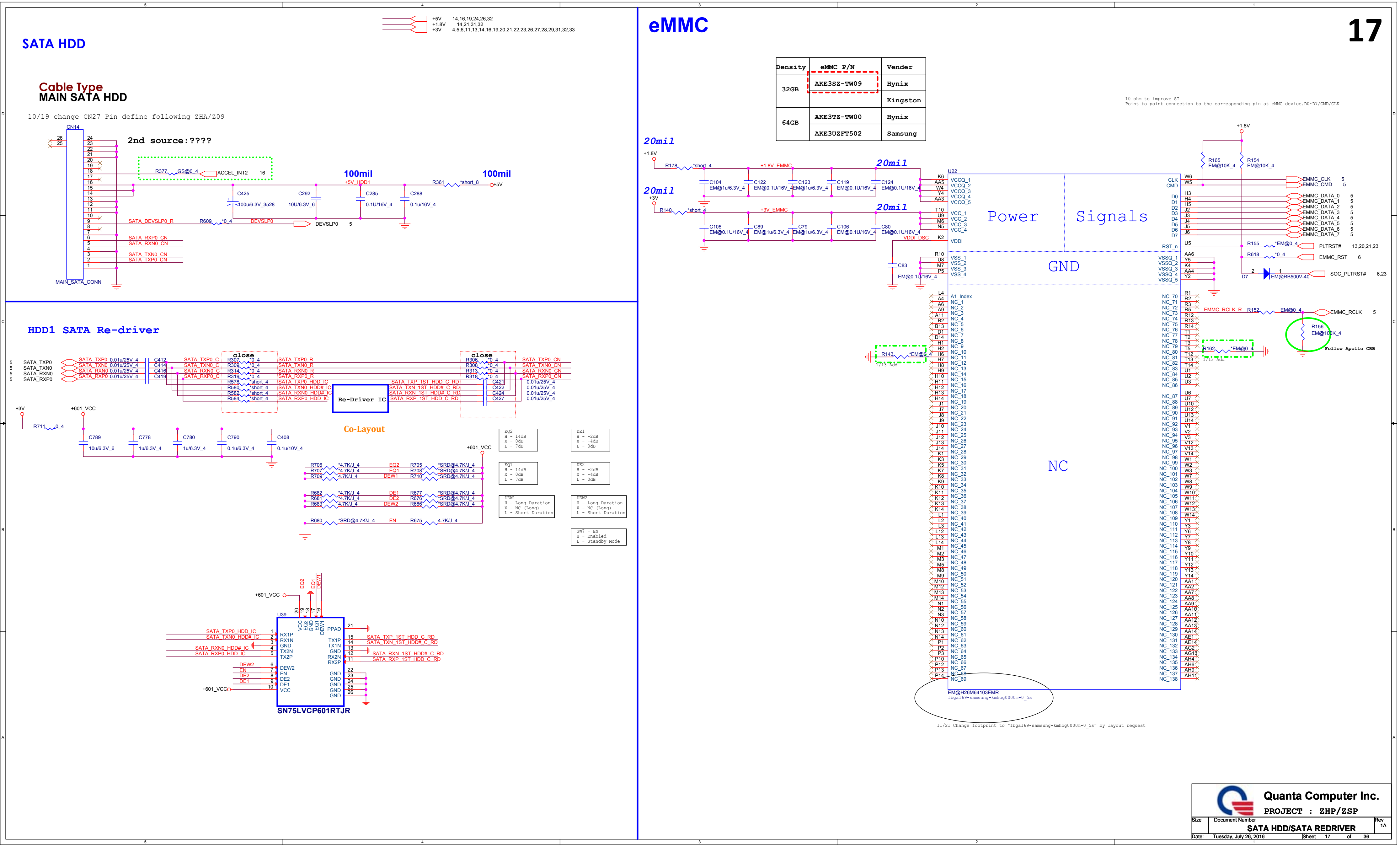
11/20 Change from I2C to SMBUS

CPU Thermal sensor(THS) / MB Local TEMP (THM)

For EJ11



Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)



Density	eMMC P/N	Vender
32GB	AKE3SZ-TW09	Hynix
		Kingston
64GB	AKE3TZ-TW00	Hynix
	AKE3UZFT502	Samsung

Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	SATA HDD/SATA REDRIVER	1A

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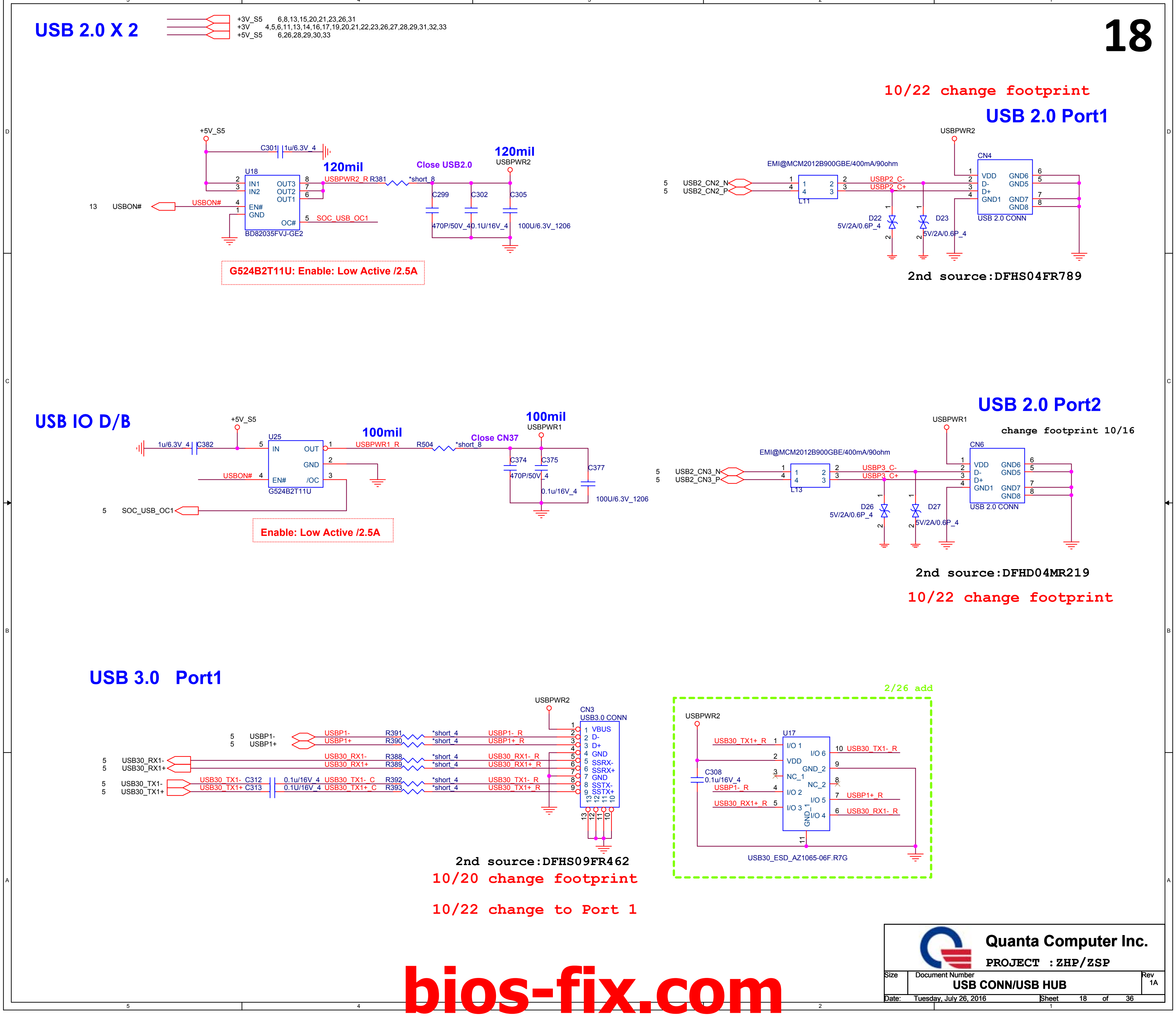
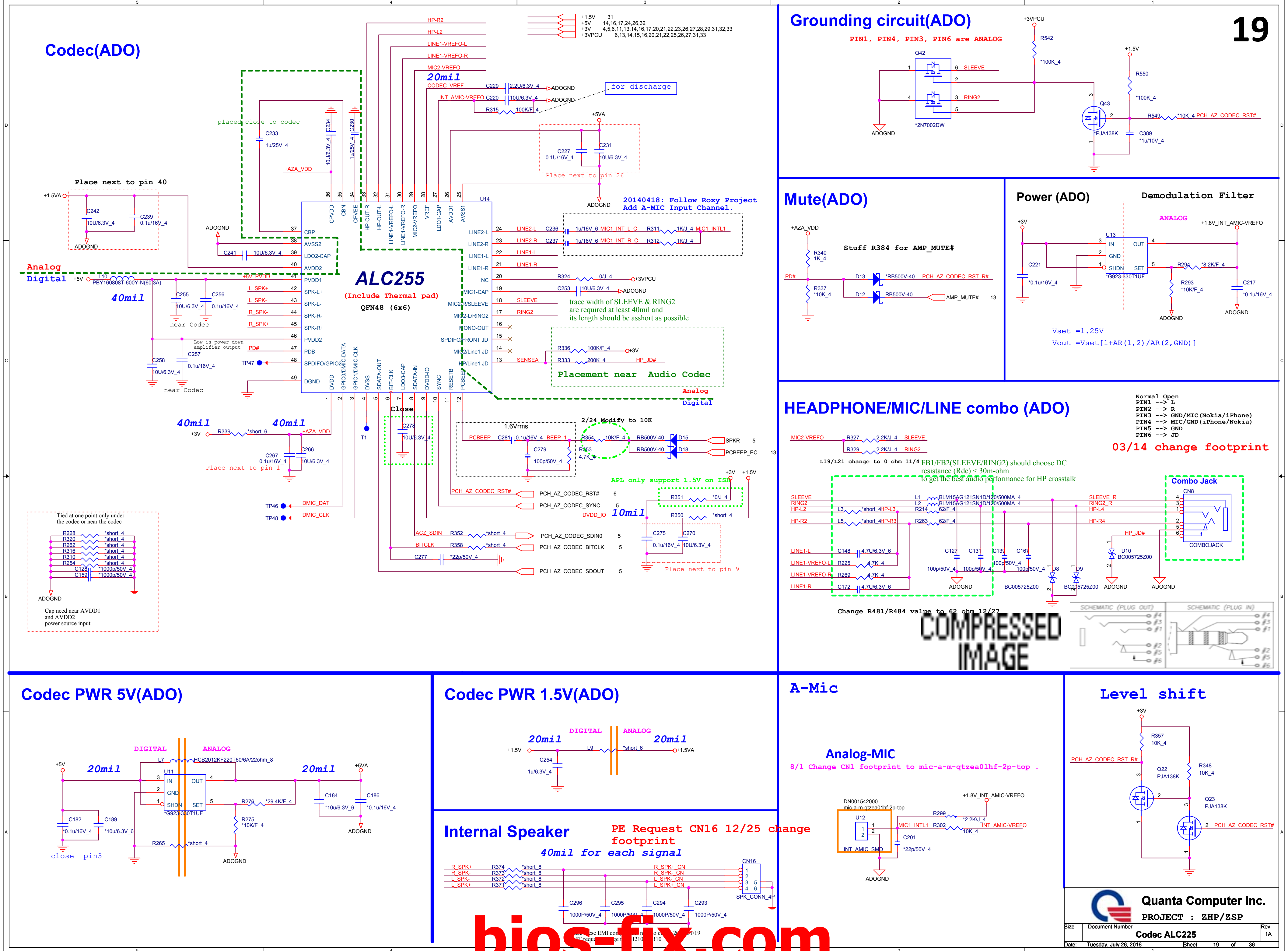
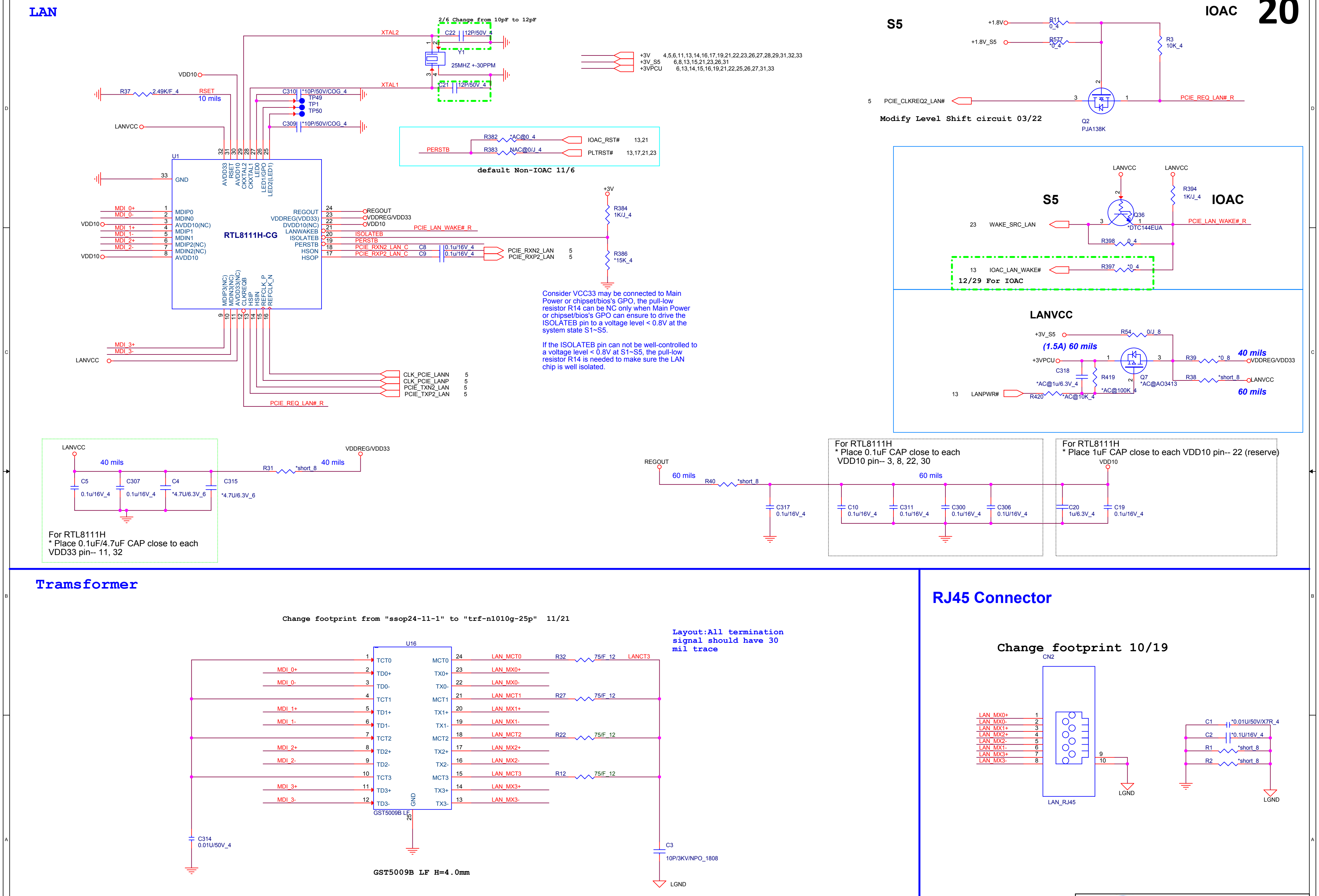


USB 2.0 X 2
+3V_S5 6,8,13,15,20,21,23,26,31
+3V 4,5,6,11,13,14,16,17,19,20,21,22,23,26,27,28,29,31,32,33
+5V_S5 6,26,28,29,30,33
18
10/22 change footprint
USB 2.0 Port1
+5V_S5
C301 1u/6.3V_4
U18
IN1
IN2
EN#
GND
OUT3
OUT2
OUT1
OC#
BD82035FVJ-GE2
120mil
USBPWR2_R R381 *short_8
Close USB2.0
120mil
USBPWR2
C299
C302
C305
470P/50V_4
0.1U/16V_4
100U/6.3V_1206
13 USBON#
USBON#
SOC_USB_OC1
G524B2T11U: Enable: Low Active /2.5A
USBPWR2
EMI@MCM2012B900GBE/400mA/90ohm
CN4
VDD
D-
D+
GND1
GND5
GND6
GND7
GND8
USB 2.0 CONN
5 USB2_CN2_N
5 USB2_CN2_P
L11
USBP2_C-
USBP2_C+
D22 5V/2A/0.6P_4
D23 5V/2A/0.6P_4
2nd source:DFHS04FR789
USB IO D/B
+5V_S5
1u/6.3V_4 C382
U25
IN
OUT
GND
EN#
/OC
G524B2T11U
100mil
USBPWR1_R
R504 *short_8
Close CN37
100mil
USBPWR1
C374
C375
C377
470P/50V_4
0.1u/16V_4
100U/6.3V_1206
USBON#
5 SOC_USB_OC1
Enable: Low Active /2.5A
USB 2.0 Port2
USBPWR1
change footprint 10/16
EMI@MCM2012B900GBE/400mA/90ohm
CN6
VDD
D-
D+
GND1
GND6
GND5
GND7
GND8
USB 2.0 CONN
5 USB2_CN3_N
5 USB2_CN3_P
L13
USBP3_C-
USBP3_C+
D26 5V/2A/0.6P_4
D27 5V/2A/0.6P_4
2nd source:DFHD04MR219
10/22 change footprint
USB 3.0 Port1
USBPWR2
CN3
USB3.0 CONN
VBUS
D-
D+
GND
SSRX-
SSRX+
GND
SSTX-
SSTX+
5 USBP1-
5 USBP1+
5 USB30_RX1-
5 USB30_RX1+
5 USB30_TX1-
5 USB30_TX1+
USBP1- R391 *short_4 USBP1-_R
USBP1+ R390 *short_4 USBP1+_R
USB30_RX1- R388 *short_4 USB30_RX1-_R
USB30_RX1+ R389 *short_4 USB30_RX1+_R
USB30_TX1-_C312 0.1u/16V_4 USB30_TX1-_C R392 *short_4 USB30_TX1-_R
USB30_TX1+ C313 0.1U/16V_4 USB30_TX1+_C R393 *short_4 USB30_TX1+_R
2nd source:DFHS09FR462
10/20 change footprint
10/22 change to Port 1
2/26 add
USBPWR2
U17
I/O 1
VDD
NC_1
I/O 2
I/O 3
GND_1
I/O 6
GND_2
NC_2
I/O 5
I/O 4
C308 0.1u/16V_4
USB30_TX1+_R
USBP1-_R
USB30_RX1+_R
USB30_TX1-_R
USBP1+_R
USB30_RX1-_R
USB30_ESD_AZ1065-06F.R7G
Quanta Computer Inc.
PROJECT :ZHP/ZSP
Size
Document Number
USB CONN/USB HUB
Rev
1A
Date: Tuesday, July 26, 2016
Sheet 18 of 36


19
Codec(ADO)
ALC255
(Include Thermal pad)
QFN48 (6x6)
U14
Place next to pin 40
placed close to codec
Place next to pin 26
20140418: Follow Roxy Project
Add A-MIC Input Channel.
for discharge
20mil
40mil
10mil
Analog
Digital
near Codec
Low is power down amplifier output
trace width of SLEEVE & RING2
are required at least 40mil and
its length should be asshort as possible
Placement near Audio Codec
Place next to pin 1
Close
1.6Vrms
2/24 Modify to 10K
APL only support 1.5V on ISP
Place next to pin 9
Tied at one point only under
the codec or near the codec
Cap need near AVDD1
and AVDD2
power source input
Grounding circuit(ADO)
PIN1, PIN4, PIN3, PIN6 are ANALOG
Mute(ADO)
Stuff R384 for AMP_MUTE#
Power (ADO)
Demodulation Filter
Vset =1.25V
Vout =Vset[1+AR(1,2)/AR(2,GND)]
HEADPHONE/MIC/LINE combo (ADO)
Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC(Nokia/iPhone)
PIN4 --> MIC/GND(iPhone/Nokia)
PIN5 --> GND
PIN6 --> JD
03/14 change footprint
L19/L21 change to 0 ohm 11/4
FB1/FB2(SLEEVE/RING2) should choose DC
resistance (Rdc) < 30m-ohm
to get the best audio performance for HP crosstalk
Combo Jack
COMBOJACK
Change R481/R484 value to 62 ohm 12/27
COMPRESSED IMAGE
Codec PWR 5V(ADO)
DIGITAL
ANALOG
close pin3
Codec PWR 1.5V(ADO)
Internal Speaker
PE Request CN16 12/25 change footprint
40mil for each signal
A-Mic
Analog-MIC
8/1 Change CN1 footprint to mic-a-m-qtzea01hf-2p-top .
Level shift
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Document Number
Codec ALC225
Rev
1A
Date: Tuesday, July 26, 2016
Sheet 19 of 36



Quanta Computer Inc.

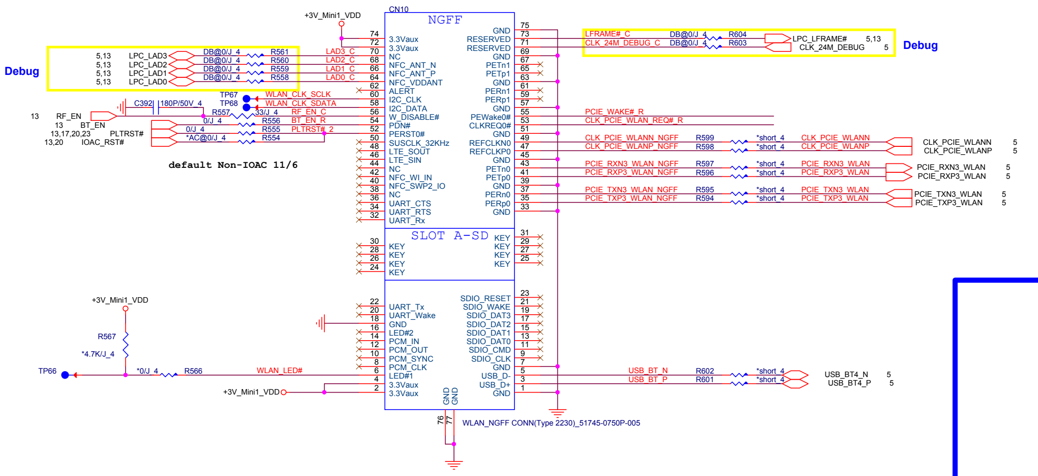
PROJECT : ZHP/ZSP

Size	Document Number	Rev
	LAN	1A

Date: Tuesday, July 26, 2016 Sheet 20 of 36

WLAN

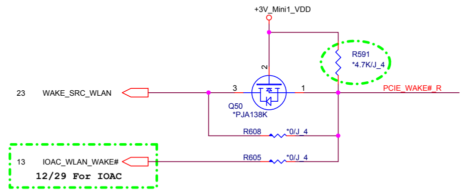
10/20 change footprint



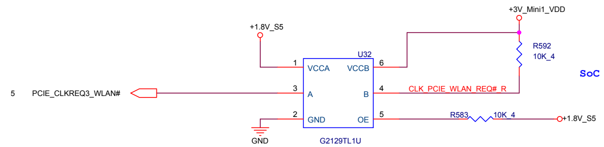
default Non-IOAC 11/6

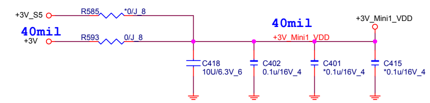
2nd source:DFHS75FR101

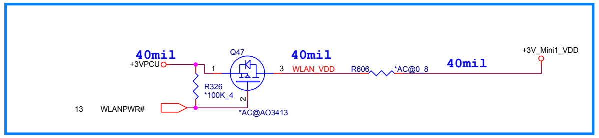
Current Leakage in S5
Dioded Forward max current : 500mA



12/29 For IOAC





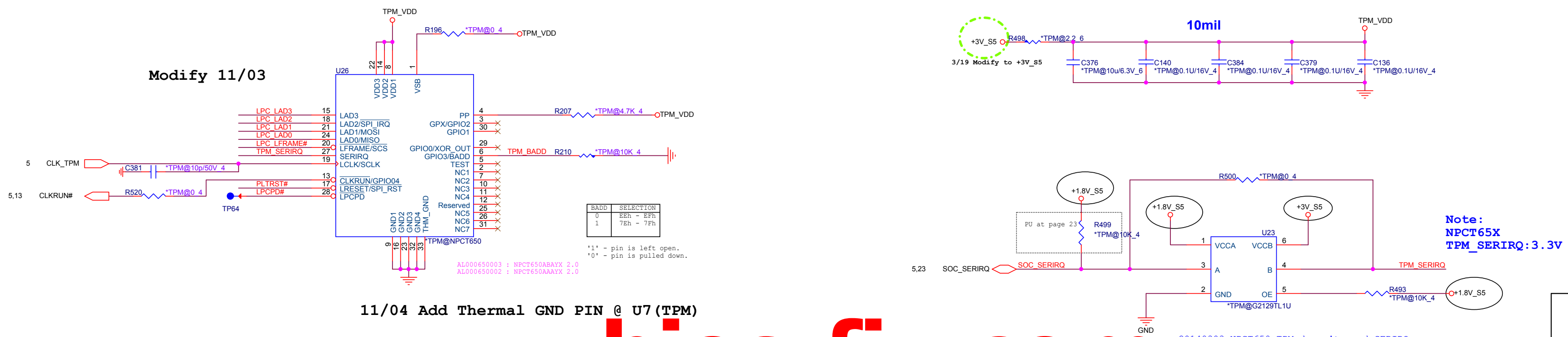


MINI PCI-E

TPM (TPM)

change to QFN type AL000650003
11/03 modify the symbol

Modify 11/03

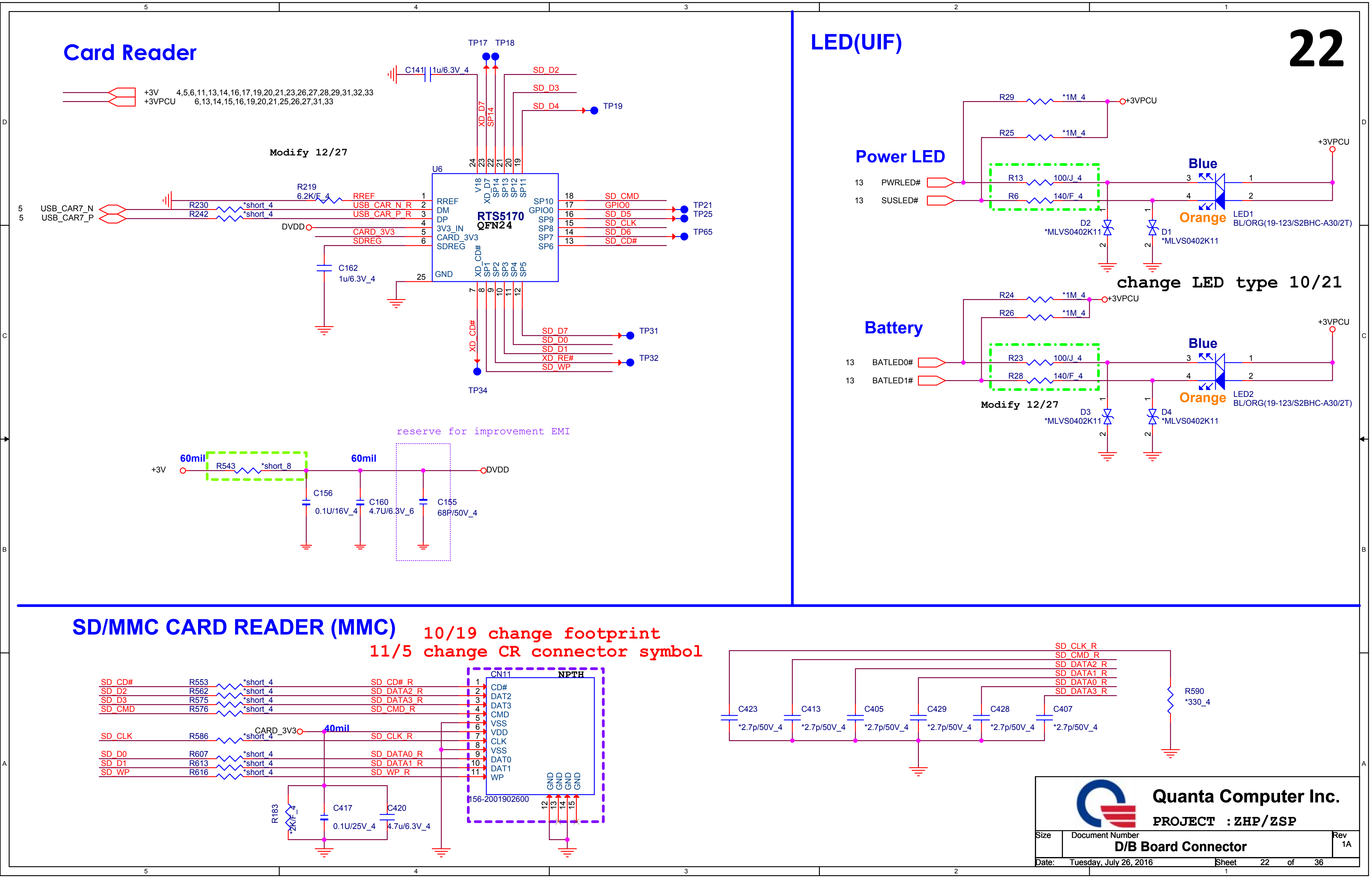


11/04 Add Thermal GND PIN @ U7(TPM)

Note:
NPCT65X
TPM_SERIRQ:3.3V

20140303:NPCT650 TPM doesn't need SERIRQ.

Quanta Computer Inc.
PROJECT :ZHP/ZSP
WiFi & BT & TPM
Rev 1A
Date: Tuesday, July 26, 2016 Sheet 21 of 36



22
Card Reader
+3V 4,5,6,11,13,14,16,17,19,20,21,23,26,27,28,29,31,32,33
+3VPCU 6,13,14,15,16,19,20,21,25,26,27,31,33
Modify 12/27
TP17 TP18
C141 1u/6.3V_4
SD_D2
SD_D3
SD_D4
TP19
XD_D7
SP14
U6
RTS5170
QFN24
R219 6.2K/F_4
RREF
R230 *short_4 USB_CAR_N_R
R242 *short_4 USB_CAR_P_R
5 USB_CAR7_N
5 USB_CAR7_P
DVDD
CARD_3V3
SDREG
C162 1u/6.3V_4
RREF DM DP 3V3_IN CARD_3V3 SDREG GND
V18 XD_D7 SP14 SP13 SP12 SP11
SP10 GPIO0 SP9 SP8 SP7 SP6
XD_CD# SP1 SP2 SP3 SP4 SP5
SD_CMD
GPIO0
SD_D5
SD_CLK
SD_D6
SD_CD#
TP21 TP25 TP65
SD_D7
SD_D0
SD_D1
XD_RE#
SD_WP
XD_CD#
TP31 TP32 TP34
reserve for improvement EMI
60mil
60mil
+3V
R543 *short_8
DVDD
C156 0.1U/16V_4
C160 4.7U/6.3V_6
C155 68P/50V_4
LED(UIF)
Power LED
R29 *1M_4 +3VPCU
R25 *1M_4
13 PWRLED#
13 SUSLED#
R13 100/J_4
R6 140/F_4
Blue
Orange
LED1 BL/ORG(19-123/S2BHC-A30/2T)
+3VPCU
D2 *MLVS0402K11
D1 *MLVS0402K11
change LED type 10/21
Battery
R24 *1M_4 +3VPCU
R26 *1M_4
13 BATLED0#
13 BATLED1#
R23 100/J_4
R28 140/F_4
Blue
Orange
LED2 BL/ORG(19-123/S2BHC-A30/2T)
+3VPCU
Modify 12/27
D3 *MLVS0402K11
D4 *MLVS0402K11
SD/MMC CARD READER (MMC)
10/19 change footprint
11/5 change CR connector symbol
SD_CD# R553 *short_4 SD_CD#_R
SD_D2 R562 *short_4 SD_DATA2_R
SD_D3 R575 *short_4 SD_DATA3_R
SD_CMD R576 *short_4 SD_CMD_R
SD_CLK R586 *short_4 SD_CLK_R
CARD_3V3 40mil
SD_D0 R607 *short_4 SD_DATA0_R
SD_D1 R613 *short_4 SD_DATA1_R
SD_WP R616 *short_4 SD_WP_R
R183 *2K/F_4
C417 0.1U/25V_4
C420 4.7u/6.3V_4
CN11 NPTH
CD# DAT2 DAT3 CMD VSS VDD CLK VSS DAT0 DAT1 WP
GND GND GND GND
156-2001902600
SD_CLK_R SD_CMD_R SD_DATA2_R SD_DATA1_R SD_DATA0_R SD_DATA3_R
C423 *2.7p/50V_4
C413 *2.7p/50V_4
C405 *2.7p/50V_4
C429 *2.7p/50V_4
C428 *2.7p/50V_4
C407 *2.7p/50V_4
R590 *330_4
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size
Document Number
D/B Board Connector
Rev 1A
Date: Tuesday, July 26, 2016
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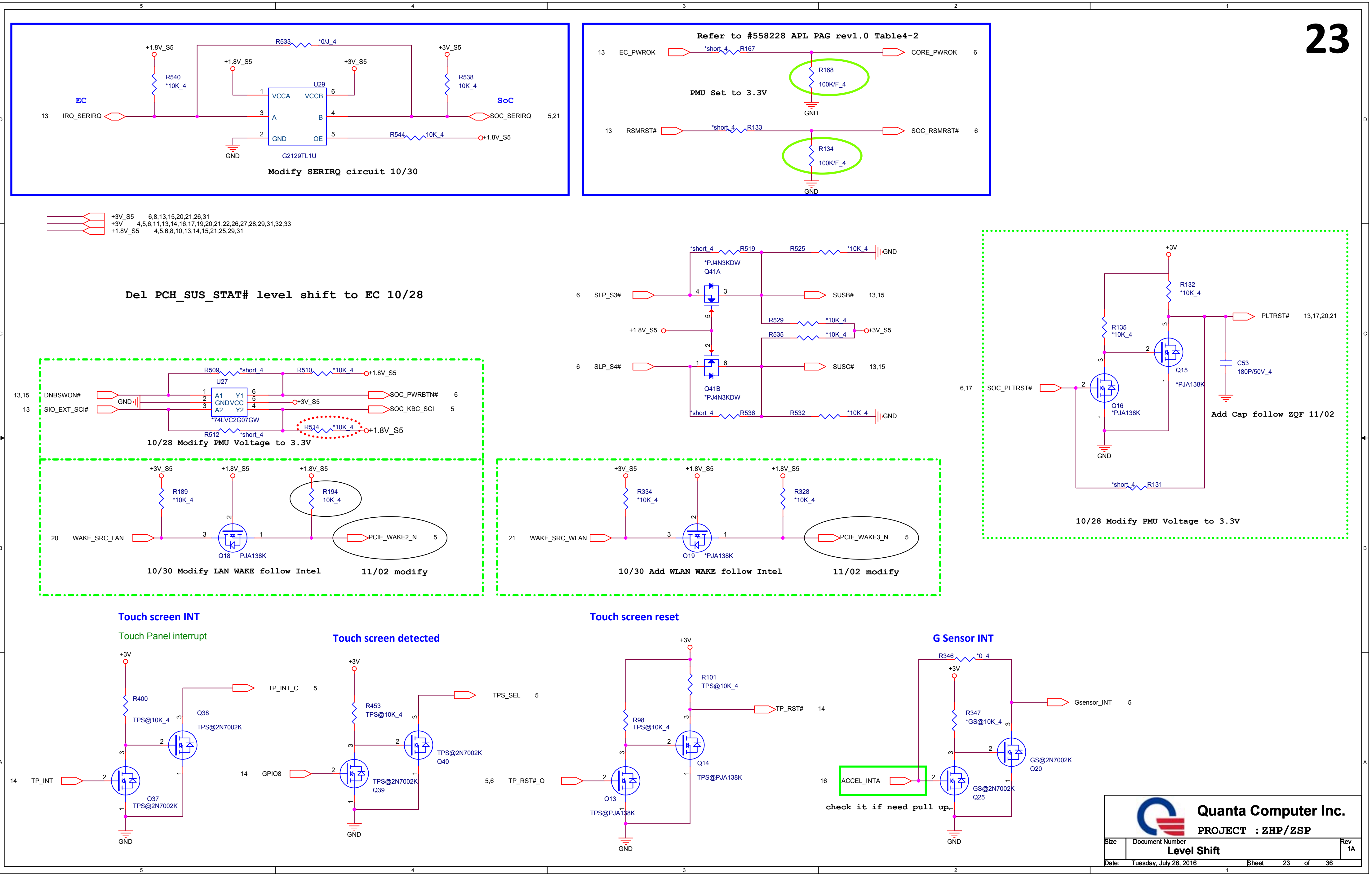
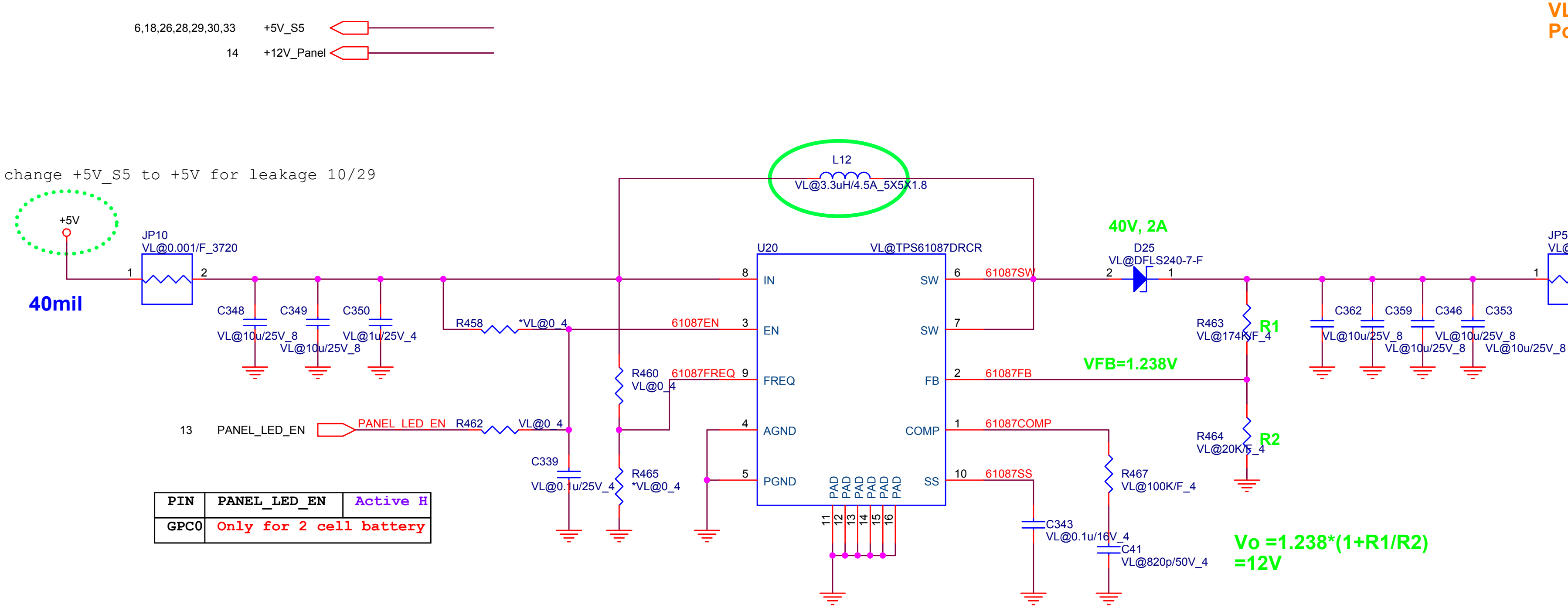

EC
13 IRQ_SERIRQ
+1.8V_S5
R540 *10K_4
R533 *0/J_4
+1.8V_S5
+3V_S5
U29
VCCA VCCB
A B
GND OE
G2129TL1U
R544 10K_4 +1.8V_S5
+3V_S5
R538 10K_4
SoC
SOC_SERIRQ 5,21
GND
Modify SERIRQ circuit 10/30
Refer to #558228 APL PAG rev1.0 Table4-2
13 EC_PWROK *short_4 R167 CORE_PWROK 6
R168 100K/F_4
PMU Set to 3.3V
GND
13 RSMRST# *short_4 R133 SOC_RSMRST# 6
R134 100K/F_4
GND
+3V_S5 6,8,13,15,20,21,26,31
+3V 4,5,6,11,13,14,16,17,19,20,21,22,26,27,28,29,31,32,33
+1.8V_S5 4,5,6,8,10,13,14,15,21,25,29,31
Del PCH_SUS_STAT# level shift to EC 10/28
*short_4 R519 R525 *10K_4 GND
*PJ4N3KDW Q41A
6 SLP_S3# SUSB# 13,15
+1.8V_S5
R529 *10K_4 +3V_S5
R535 *10K_4
6 SLP_S4# SUSC# 13,15
Q41B *PJ4N3KDW
*short_4 R536 R532 *10K_4 GND
+3V
R132 *10K_4
R135 *10K_4
PLTRST# 13,17,20,21
Q15 *PJA138K
C53 180P/50V_4
6,17 SOC_PLTRST#
Q16 *PJA138K
GND
Add Cap follow ZQF 11/02
*short_4 R131
10/28 Modify PMU Voltage to 3.3V
R509 *short_4 R510 *10K_4 +1.8V_S5
U27
13,15 DNBSWON# SOC_PWRBTN# 6
GND A1 Y1 GND VCC A2 Y2 +3V_S5
13 SIO_EXT_SCI# SOC_KBC_SCI 5
*74LVC2G07GW
R514 *10K_4 +1.8V_S5
R512 *short_4
10/28 Modify PMU Voltage to 3.3V
+3V_S5 +1.8V_S5 +1.8V_S5
R189 *10K_4
R194 10K_4
20 WAKE_SRC_LAN PCIE_WAKE2_N 5
Q18 PJA138K
10/30 Modify LAN WAKE follow Intel
11/02 modify
+3V_S5 +1.8V_S5 +1.8V_S5
R334 *10K_4
R328 *10K_4
21 WAKE_SRC_WLAN PCIE_WAKE3_N 5
Q19 *PJA138K
10/30 Add WLAN WAKE follow Intel
11/02 modify
Touch screen INT
Touch Panel interrupt
+3V
R400 TPS@10K_4
Q38 TPS@2N7002K
TP_INT_C 5
14 TP_INT
Q37 TPS@2N7002K
GND
Touch screen detected
+3V
R453 TPS@10K_4
TPS_SEL 5
14 GPIO8
TPS@2N7002K Q40
TPS@2N7002K Q39
GND
Touch screen reset
+3V
R101 TPS@10K_4
TP_RST# 14
R98 TPS@10K_4
Q14 TPS@PJA138K
5,6 TP_RST#_Q
Q13 TPS@PJA138K
GND
G Sensor INT
R346 *0_4
+3V
R347 *GS@10K_4
Gsensor_INT 5
GS@2N7002K Q20
16 ACCEL_INTA
GS@2N7002K Q25
check it if need pull up.
GND
Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size Document Number Rev
Level Shift 1A
Date: Tuesday, July 26, 2016 Sheet 23 of 36

Panel Spec (TFT-LCD 14")
VLED : 6V~21V (Tpy:12V)
Power Consumption : 3W (MAX)

+12V_Panel
12 Volt +/- 5%
PEAK : 0.35A
Width : 20mil

change +5V_S5 to +5V for leakage 10/29



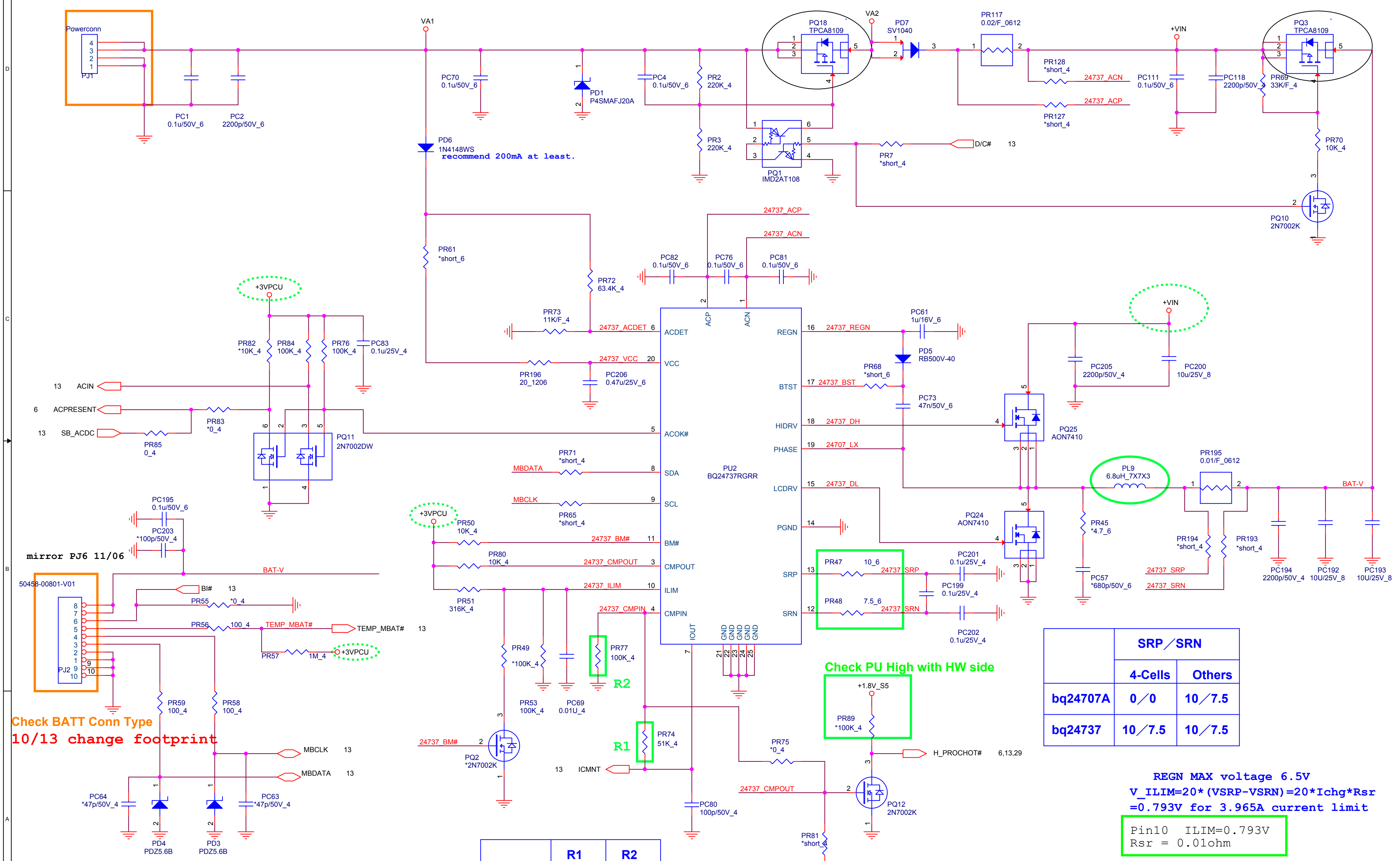
PIN	PANEL_LED_EN	Active H
GPC0	Only for 2 cell battery	

Vo =1.238*(1+R1/R2)
=12V

Quanta Computer Inc.		
PROJECT :		
Size	Document Number DC-DC	Rev 1A
Date: Tuesday, July 26, 2016	Sheet 24 of 36	

Change ADP-IN Pin define 2016/01/11 by SMT Request.

PQ27 / PQ8 change from BAM14130000 (MOS AOL1413) to BAM81090000 (MOS TPCA8109) 11/06



	SRP/SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

	R1	R2
UMA-45W	51K	100K

REGN MAX voltage 6.5V

V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr

=0.793V for 3.965A current limit

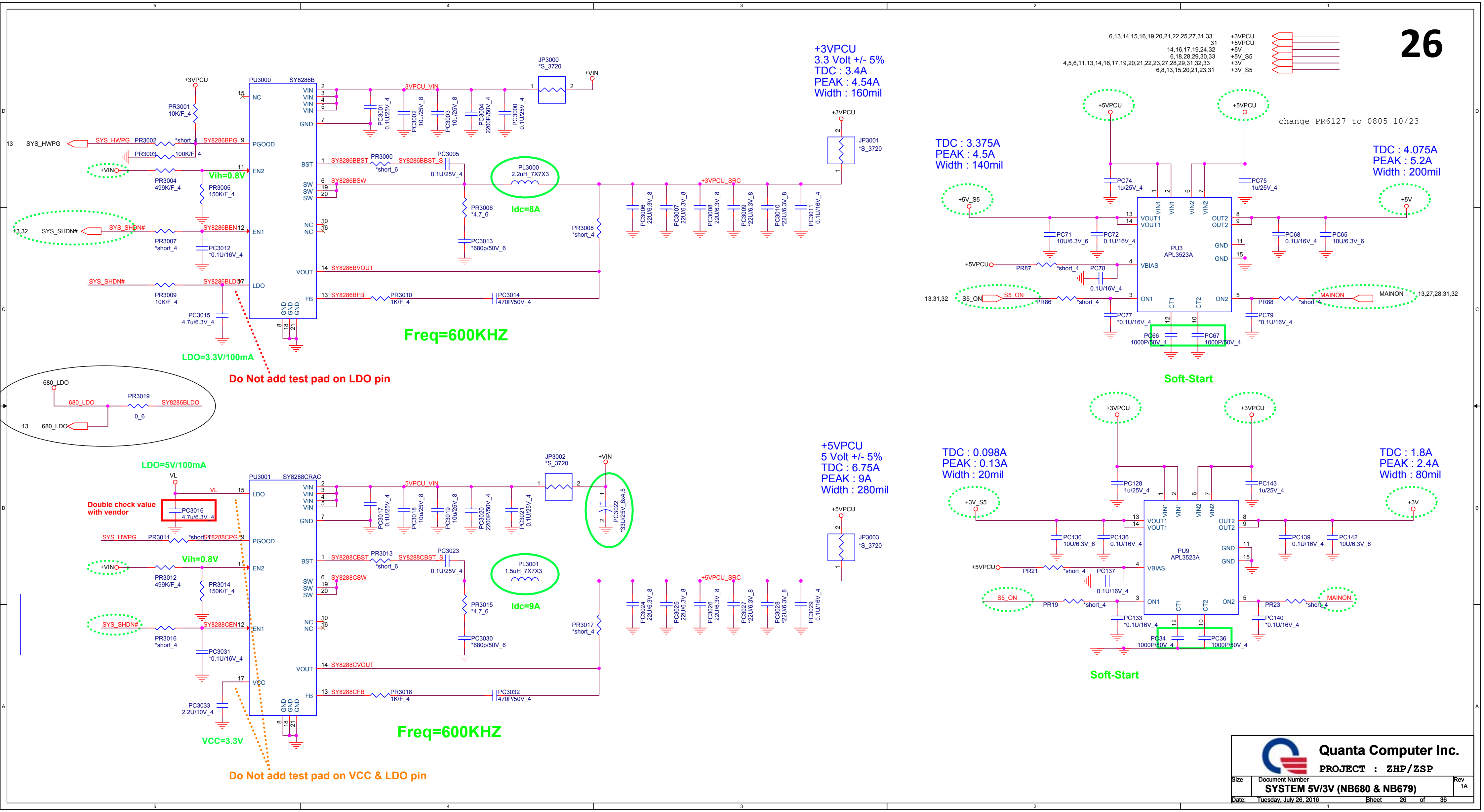
Pin10 ILIM=0.793V

Rsr = 0.01ohm

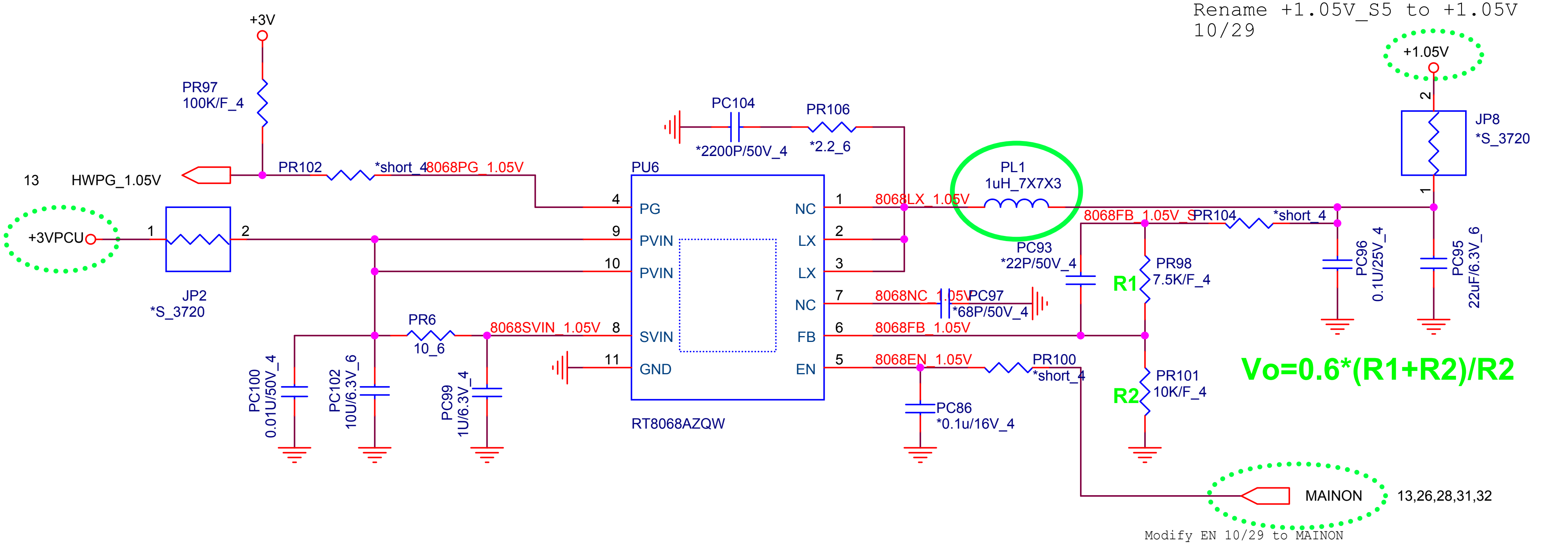
Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	Charger(BQ24737RGRR)	2A
Date: Tuesday, July 26, 2016	Sheet 25 of 36	


26
+3VPCU
3.3 Volt +/- 5%
TDC : 3.4A
PEAK : 4.54A
Width : 160mil
Freq=600KHZ
LDO=3.3V/100mA
Do Not add test pad on LDO pin
Idc=8A
Vih=0.8V
+5VPCU
5 Volt +/- 5%
TDC : 6.75A
PEAK : 9A
Width : 280mil
LDO=5V/100mA
Double check value with vendor
Idc=9A
VCC=3.3V
Do Not add test pad on VCC & LDO pin
TDC : 3.375A
PEAK : 4.5A
Width : 140mil
TDC : 4.075A
PEAK : 5.2A
Width : 200mil
change PR6127 to 0805 10/23
Soft-Start
TDC : 0.098A
PEAK : 0.13A
Width : 20mil
TDC : 1.8A
PEAK : 2.4A
Width : 80mil
Quanta Computer Inc.
PROJECT : ZHP/ZSP
SYSTEM 5V/3V (NB680 & NB679)
Tuesday, July 26, 2016
Sheet 26 of 36

+1.05V_S5
1.05Volt +/- 5%
TDC : 2.025A
PEAK : 2.7A
Width : 100mil



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	+1.05V_S5 (RT8068AZQW)	2A

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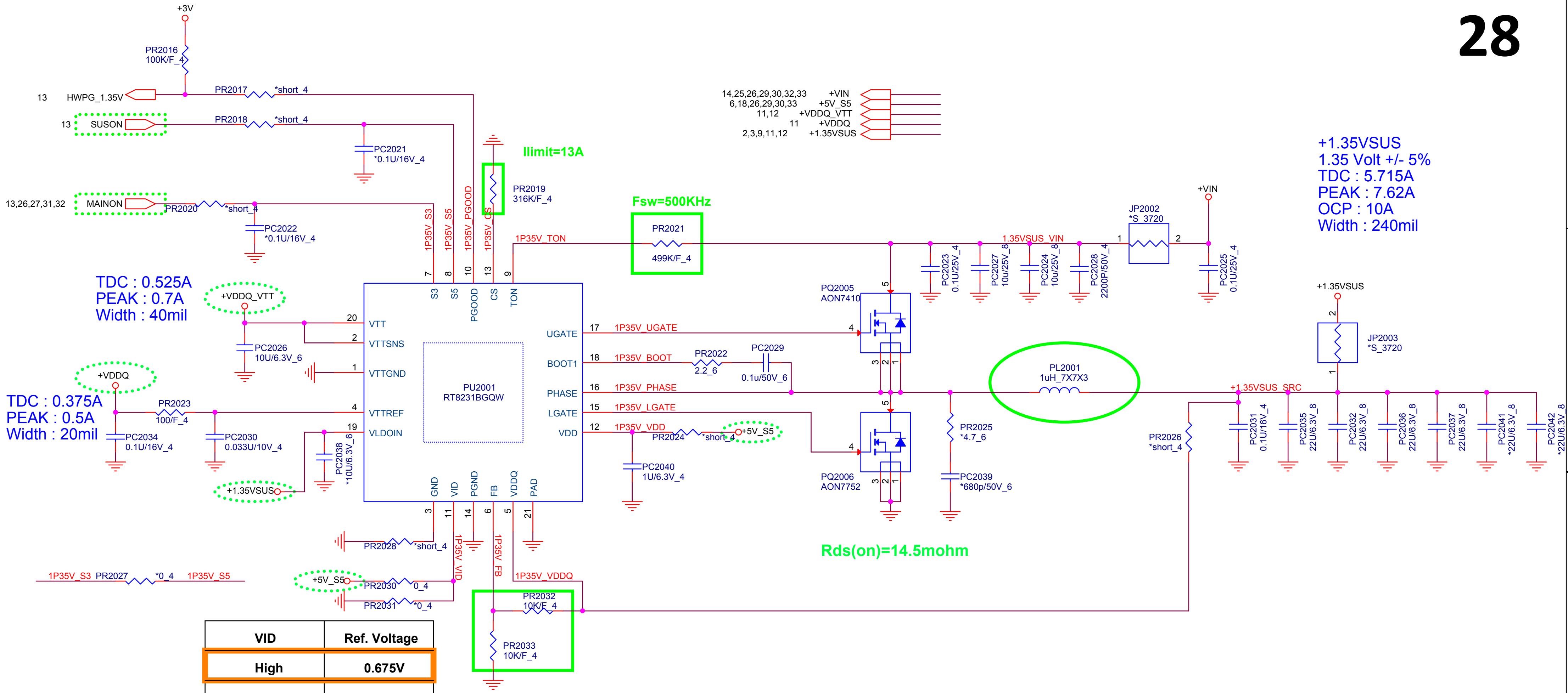


VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=10A
L ripple current
=(19-1.35)*1.35/(1u*500k*19)
=2.508A
Vtrip=10-(2.508/2)*14.5mohm
=126.817mV
Rlimit=126.817mV/5uA*10=253.63Kohm

DDR=1.35V
PR2032=10K/F_4
PR2033=10K/F_4

Quanta Computer Inc.

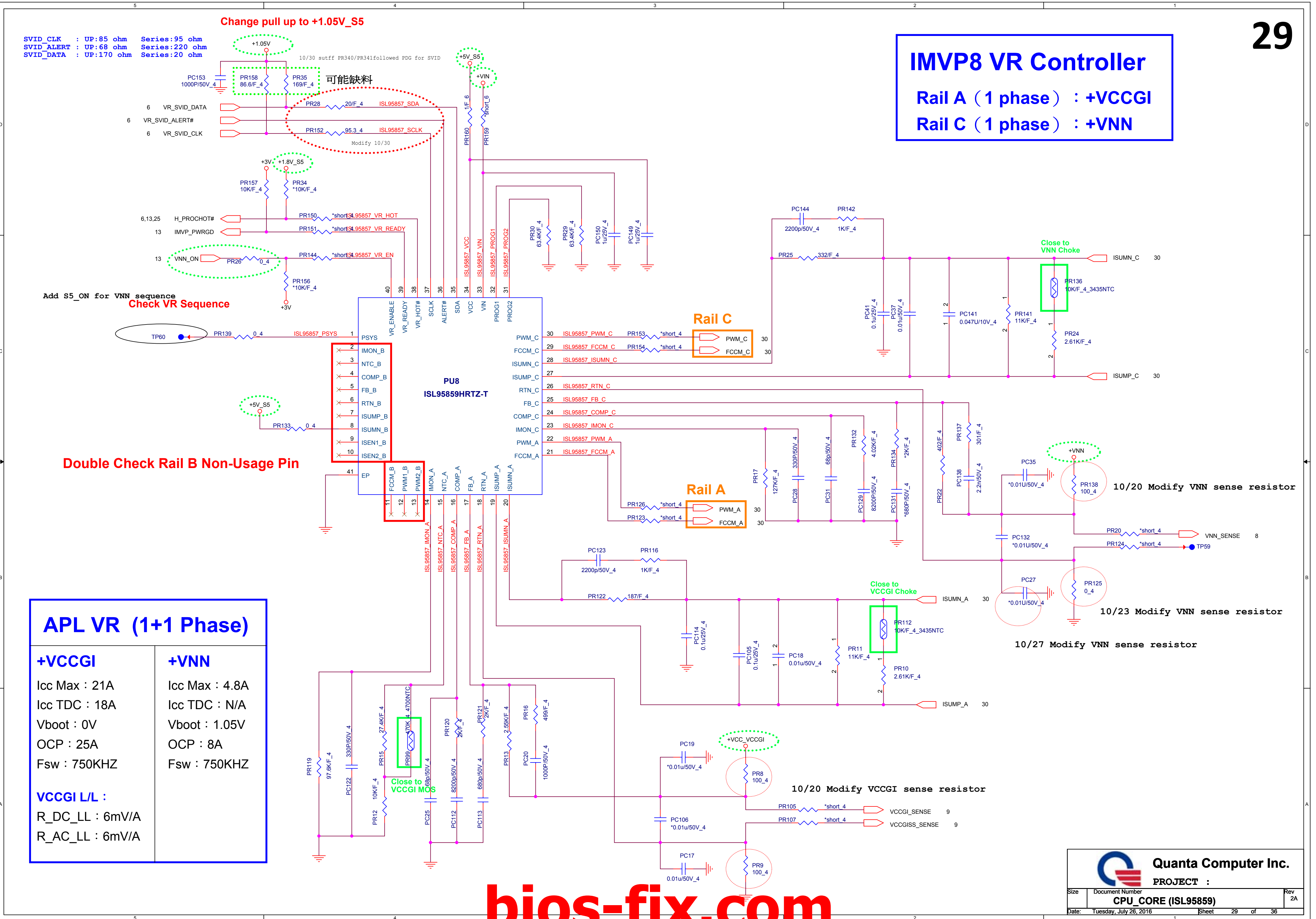
PROJECT :

Size	Document Number	Rev
	DDR3L (RT8231BGQW)	1A

Date: Tuesday, July 26, 2016 Sheet 28 of 36

IMVP8 VR Controller

Rail A（1 phase）：+VCCGI
Rail C（1 phase）：+VNN



APL VR (1+1 Phase)

+VCCGI	+VNN
Icc Max：21A	Icc Max：4.8A
Icc TDC：18A	Icc TDC：N/A
Vboot：0V	Vboot：1.05V
OCP：25A	OCP：8A
Fsw：750KHZ	Fsw：750KHZ

VCCGI L/L：

R_DC_LL：6mV/A

R_AC_LL：6mV/A

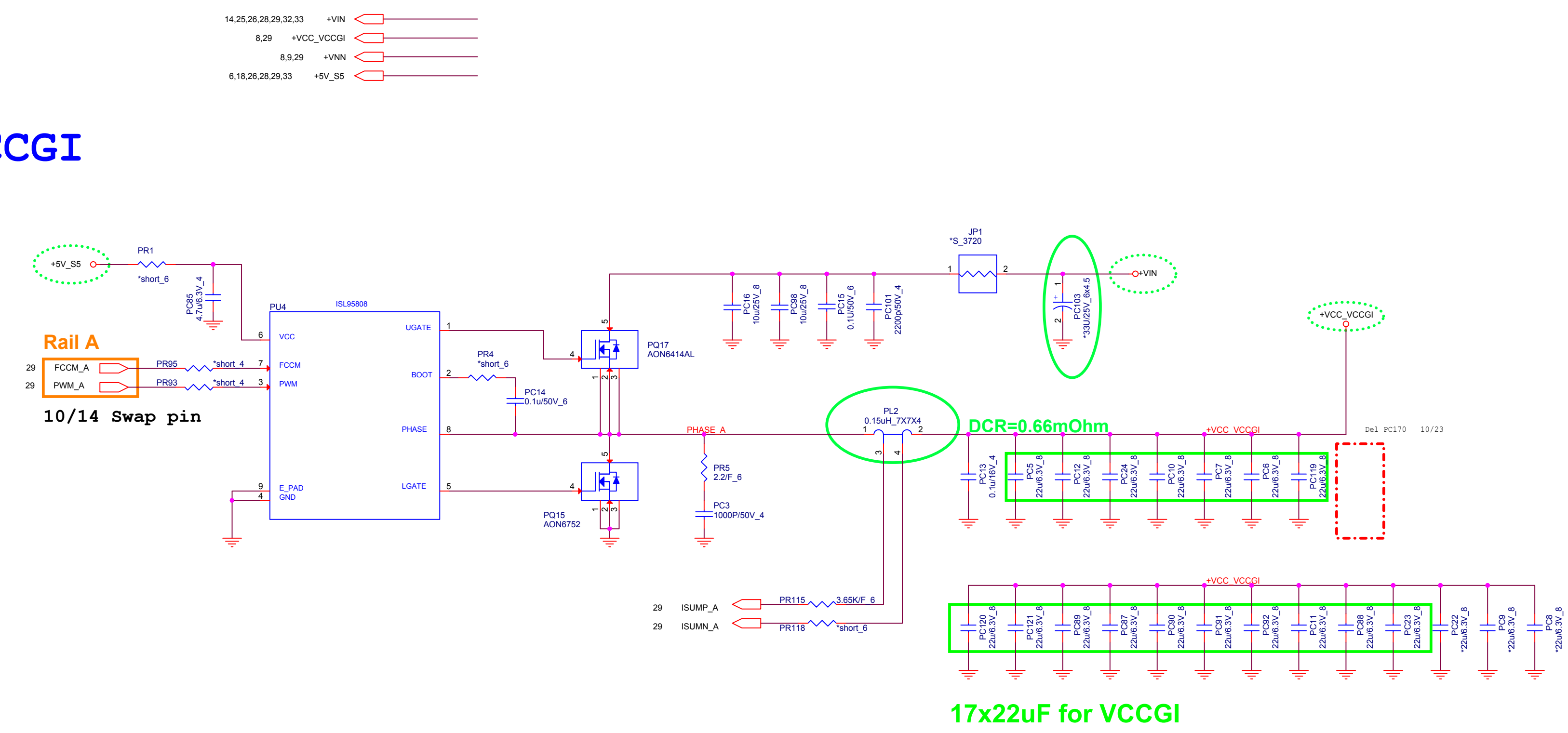
Quanta Computer Inc.

PROJECT :

Size | Document Number: CPU_CORE (ISL95859) | Rev 2A

Date: Tuesday, July 26, 2016 | Sheet 29 of 36

VCCGI

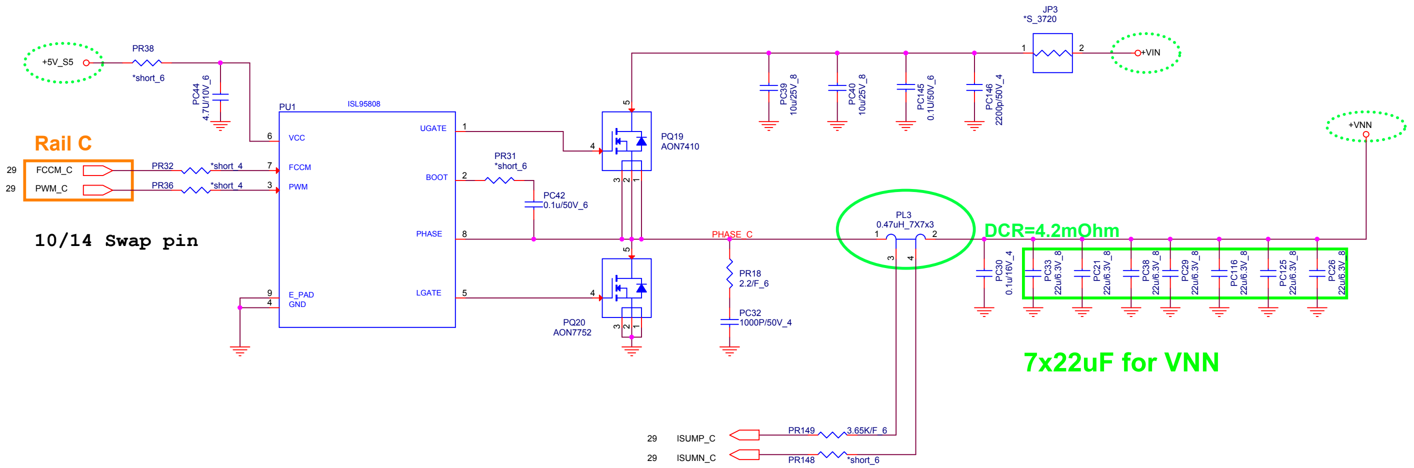


+VCCGI

Icc Max：21A
Icc TDC：18A
Vboot：0V
OCP：25A
Fsw：750KHZ

VCCGI L/L：
R_DC_LL：6mV/A
R_AC_LL：6mV/A

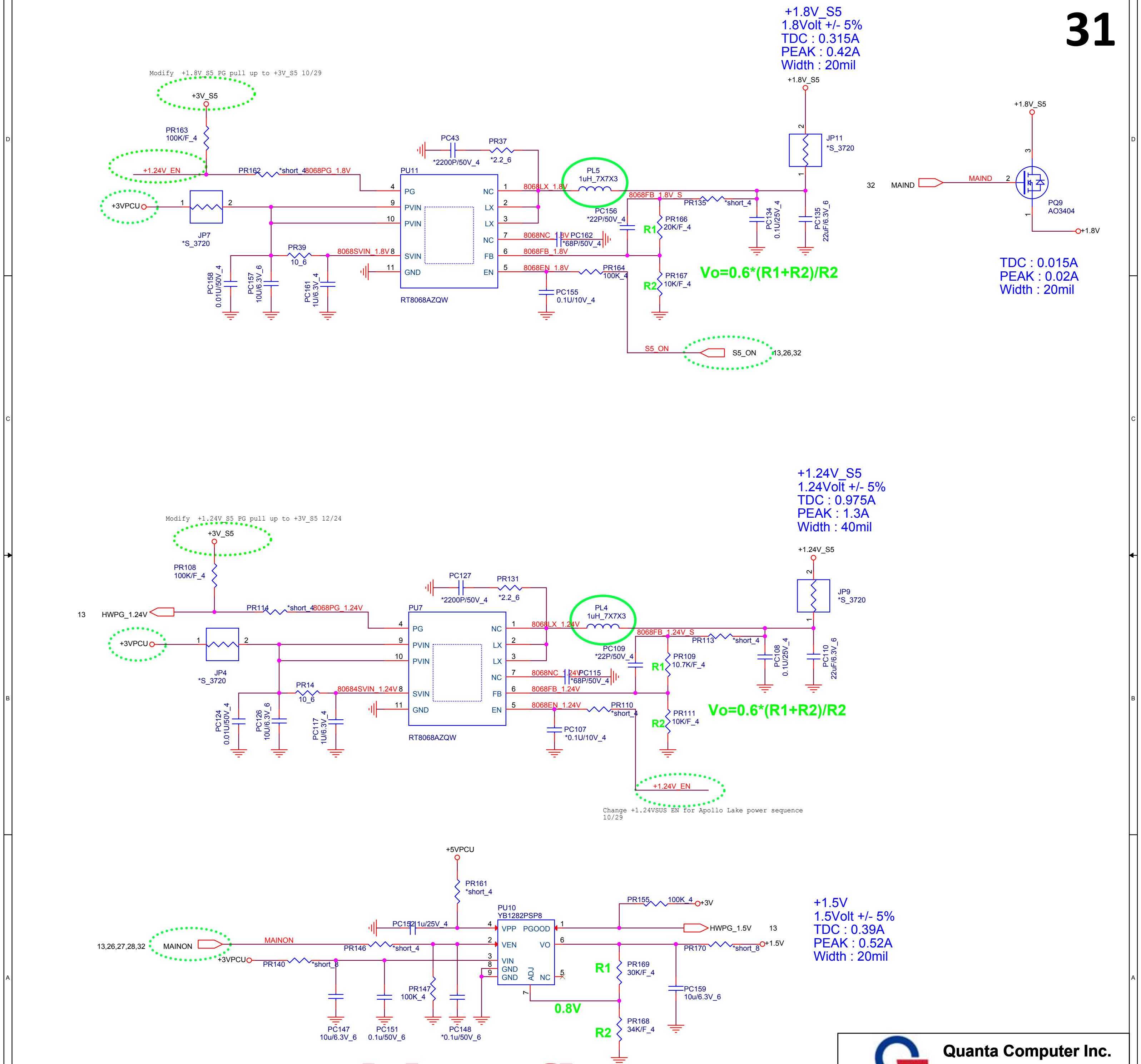
VNN



+VNN

Icc Max：4.8A
Icc TDC：N/A
Vboot：1.05V
OCP：8A
Fsw：750KHZ

Quanta Computer Inc.
PROJECT :
Size | Document Number: +VCCGI / +VNN (ISL95859) | Rev 2A
Date: Tuesday, July 26, 2016 | Sheet 30 of 36

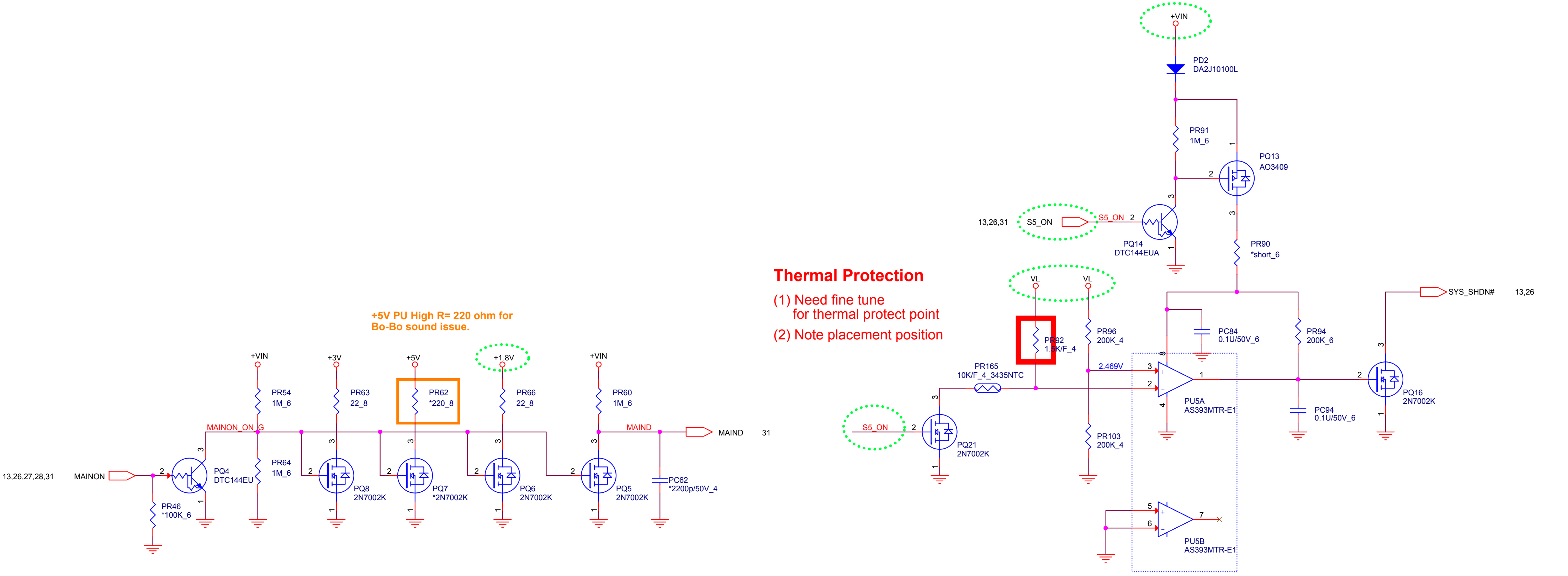


Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	+1.8V_S5 / +1.24VSUS / +1.5V	2A

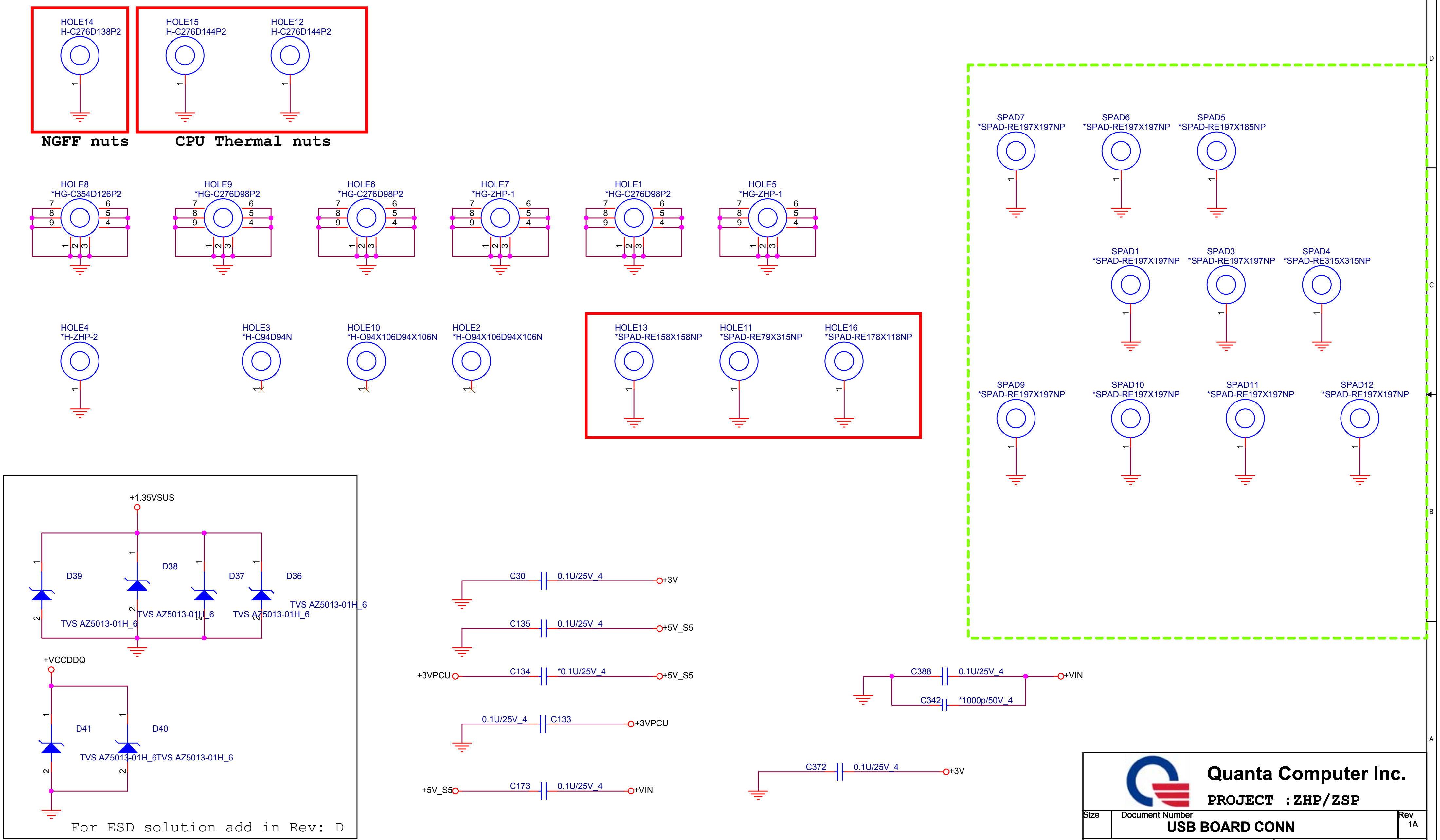
Date: Tuesday, July 26, 2016 Sheet 31 of 36



For EC control thermal protection (output 3.3V)

HOLE(OTH)

Need to check the nuts 10/27



Quanta Computer Inc.

PROJECT : ZHP/ZSP

Size	Document Number	Rev
	USB BOARD CONN	1A

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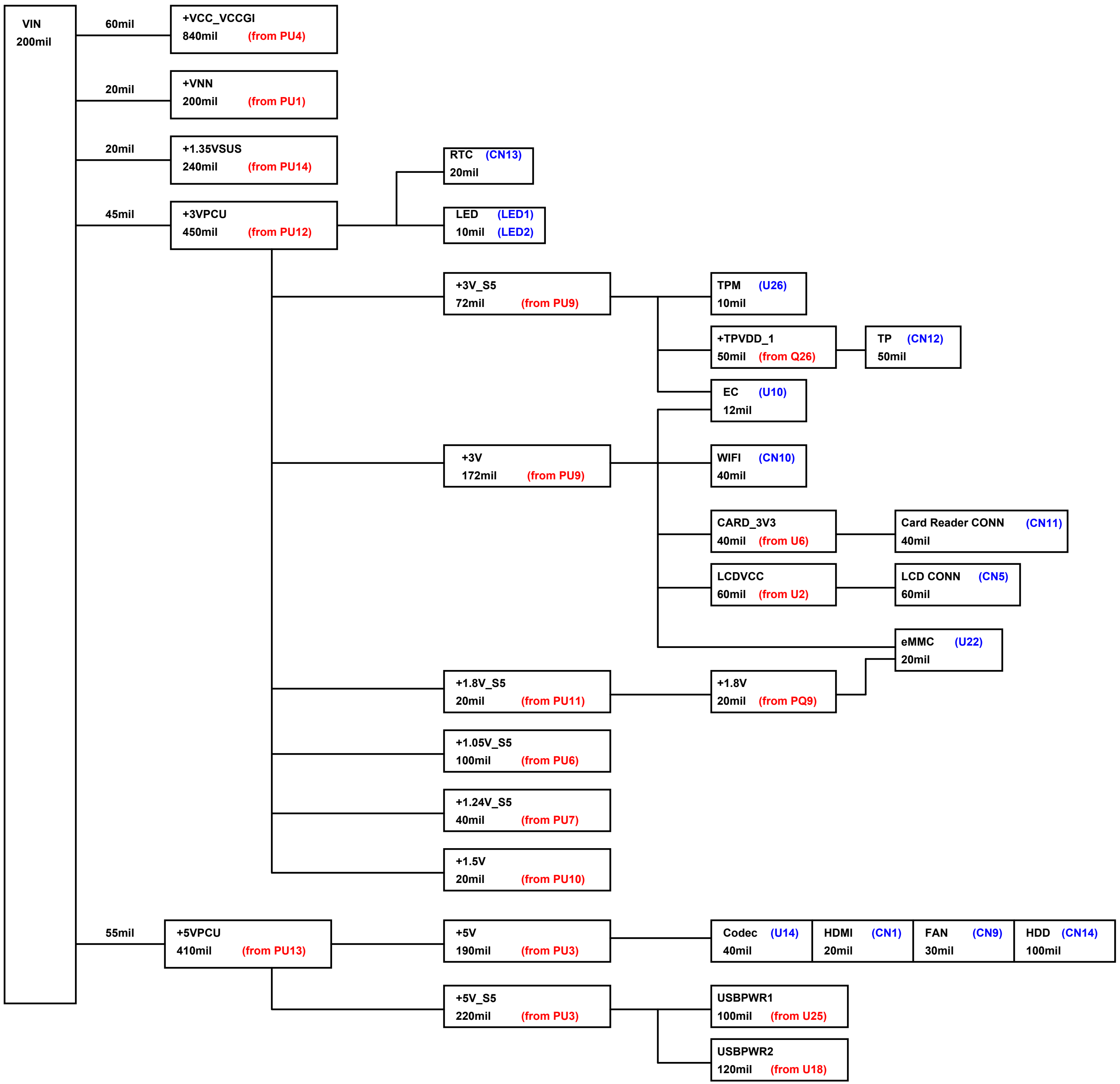
Apollo Power Tree



Quanta Computer Inc.
PROJECT : ZHP/ZSP
Size | Document Number | Rev
Power Sequence | 1A
Date: Tuesday, July 26, 2016 | Sheet 34 of 38

CHANGE LIST

Model	REV	CHANGE LIST
ZHP/ZSP MB	REV.A	1 2015/11/10 REV:A Initial release

REV.A

1 2015/11/12 R64 (68ohm) change EOD part CS06802FB07 to CS06802JB17
2 2015/11/12 PR152 Change CS09532FB08 to CS09532FB00
3 2015/11/12 Stuff R483
4 2015/11/12 R220 modify value *CHB@80.6/F_4
5 2015/11/12 R266, R274, C171, R267, C170, R272 modify value CHB@
6 2015/11/12 U2 change EOL part AL005243001 to AL005245000
7 2015/11/12 Page 6 add text "Pin AG55 is EMMC_PWR_EN_N (CRB 1.0)"
8 2015/11/12 Correct the value and description of R13, R23
9 2015/11/12 Correct the value and description of R6, R28

1 2015/11/13 R142 change CS11372FB09 to CS11372FB25
2 2015/11/13 PR22 change CS14022FB03 to CS14022FB11
3 2015/11/13 PC18, PC181 change EOD part CH31004KB17 to CH31006KB18
4 2015/11/13 PC96, PC108, PC134, PC182, C138 change EOD part CH41002KB93 to CH4104K1B00
5 2015/11/13 C408, C409, C421, C422 change EOD part CH4102K1B03 to CH4104K1B00
6 2015/11/13 PC152 change EOD part CH5103K9901 to CH5103K1900
7 2015/11/13 PR186 change EOD part CS-2003J932 to CS-2003F900
8 2015/11/13 C112, C118, C157, C158, C163, C164, C165, C166 change EOD part CH6221M9A07 to CH6221M9A01

REV.B

1 2015/12/07 Remove PR27, Add R617 220 ohm for A Can't Power on issue.
2. 2015/12/07 Remove R280/R288/R279/R287/R266/R274/R267/R272/C170/C171/C180/C179/R220,
ADD R226 And R251 for memory Down can't work issue.
3. 2015/12/07 remove R75 for can't power on.
4. 2015/12/07 change SW2 to PN: DHPDSA40E00 and Footprint
5. 2015/12/17 change U4 and U33 to Dual 2N7002K for RDC request.
6. 2015/12/17 change C377 from 3528 to 1206 and C27 from 0805 10U to 0603 10U.
7. 2015/12/17 add U21 Pin L30 EMMC Rest to U22
8. 2015/12/25 Change CN13 to support ML1220 for PE Request.
9. 2015/12/25 Change P28 DDR3L Power solution
9. 2016/01/11 Resever 2K for SD-Card VCC
10. 2016/01/11 Change PJ1 ADP-IN Pin define 2016/01/11 by SMT Request.
11. 2016/01/12 R514 remove in B test , for AC/DC change icon issue, Add D35 for Hall IC ESD part by EC side.
12. 2016/01/25 remove R472/C352/C347/C351 int function no need use.
13. 2016/01/25 add EC Pin

REV.C

1.Change Q56 to DMN53D0LDW (Vgs=1.5V)
2.Change Q2 folllow ZRV 雙向.
3.Change PR73 from 10K to 11K by power team request
4.Change PR164 from 63.4K to 100K for power sequence fine tune and PR110 from 4.7K to 0 ohm
5.Add R573 and net "THERMTRIP#" and to conect EC pin4
6.Add R579 and R581 10K PU for PDG 1.2 Request.
7. Remove R136 and R137 , Mount R145 for PDG 1.2 Request.
8. Modify HDMI Q34 to 1.BAM6N430000 for HDMI Issue and Remove R34/R33/R380 /R100
9. G_Sensor issue remove R346
10. Core Power OK R171 change from 20K to 100K, R488 change from 2.7K to 10K.
11. CHange C76 and C78 to 15P for RTC clock issue.

REV.D

1.Add R589 for Acer ESD lesson.

REV.E

1.Change R164 from 100K to 2.2K and R138 from 4.7K to 0 ohm for BIOS SOC_Override functiion.
2.Remove R201 and R201 (HDA SDI I/O pin issue) for QS sample .
3.Follow check list V1.5 to change R171 from 100K to 20K
4.Change Q12/Q33 type to PJA138K (Vgs<=1.5V)
5. Unstuff SW1,C391,R548

0402: R578,R580,R582,R584,R322,R150,R387,R55,R50,R51,R418,R159,R304,R376,R144,R126,R125,R123,R534,
R255,R248,R545,R229,R249,R236,R80,R81,R444,R445,R365,R228,R320,R262,R316,R310,R254,R265,
R352,R358,R350 R601,R602,R594,R595,R596,R597,R598,R599,R242,R230,R553,R562,R575,R576,R586,
R607,R613,R616,R509,R512,R131,
R536,R519,R133,R167,R163,PR71,PR65,PR128,PR127,PR194,PR193,PR81,PR7,PR3002,PR3007,PR3011,
PR3016,PR3017,PR3008,PR87,PR86,PR88,PR21,PR19,PR23,PR102,PR100,PR104,PR2017,PR2018,PR2020,
PR2028,PR2024,PR2026,PR150,PR151,PR144,PR26,PR126,PR123,PR105,PR107,PR20,PR124,PR153,
PR154,PR95,PR93,PR32,PR36,PR162,PR114,PR146,PR161,PR110,PR113,PR135,R224,R193/R190/R403
/R436/R437/R258/R252/R253/R273/R53/R59/L5/L3

0603: R208,R206,R481,R474,R478,R116,R105,R117,R118,R119,R545,L6,PR68,PR61,PR3013,PR3000,
PR159,PR4,PR31,PR1,PR38,PR118,PR148,PR90,R339

0805: R361,R174,R485,R480,R52,R468,R374,R373,R372,R371,R40,R38,R1,R2,R31,R543,PR130,PR143,PR129,
PR145,PR67,PR52,PR78,PR79,PR170,PR140

1206:R257,R256,

3720: JP3000,JP3001,JP3002,JP3003,JP2,JP8,JP2002,JP2003,JP1,JP3,JP11,JP9,JP4

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Model	REV	CHANGE LIST
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ZHP/ZSP MB

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Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF

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	Power Table	1A

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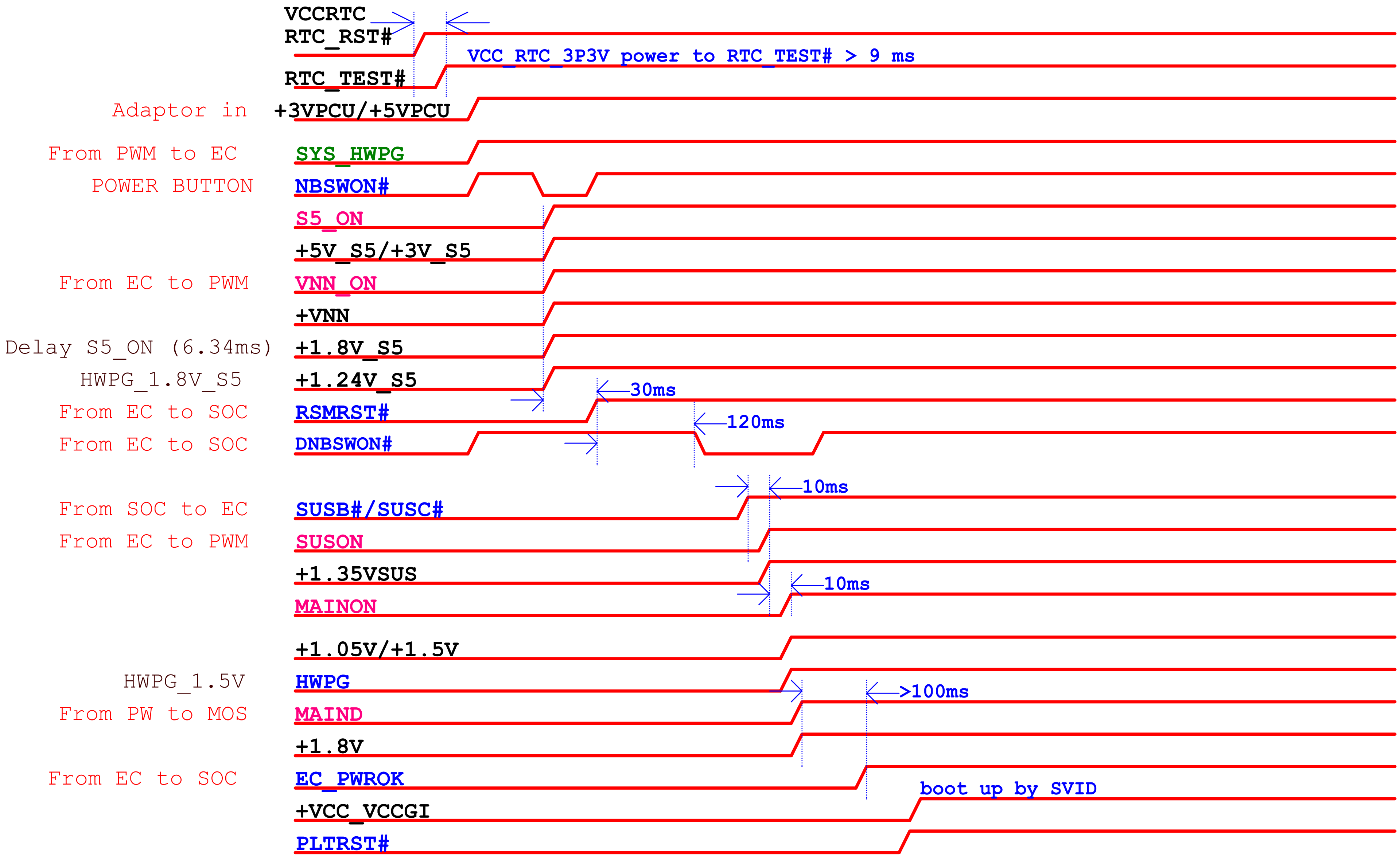

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PROJECT : ZHP/ZSP

Size	Document Number	Rev
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