VDKTE

Rosetta 10ADT/10ADTG

LA-9869P REV 0.3 Schematic

AMD APU RICHLAND FP2 / FCH BOLTON-M3

Sun Pro M2

2013-02-04 Rev 0.3

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: LA-9869P		Rev: 0.3
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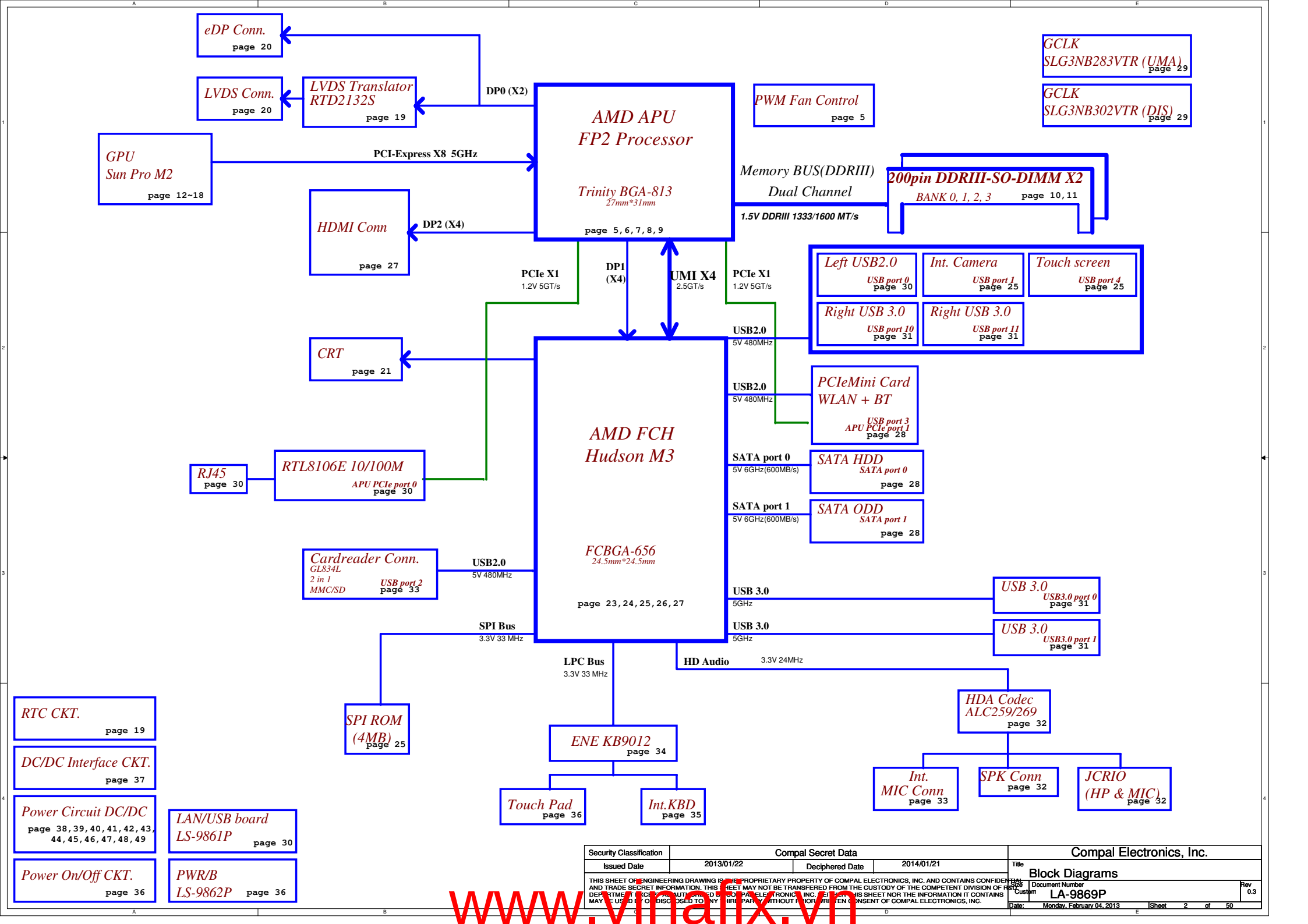

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
Custom	LA-9869P	0.3

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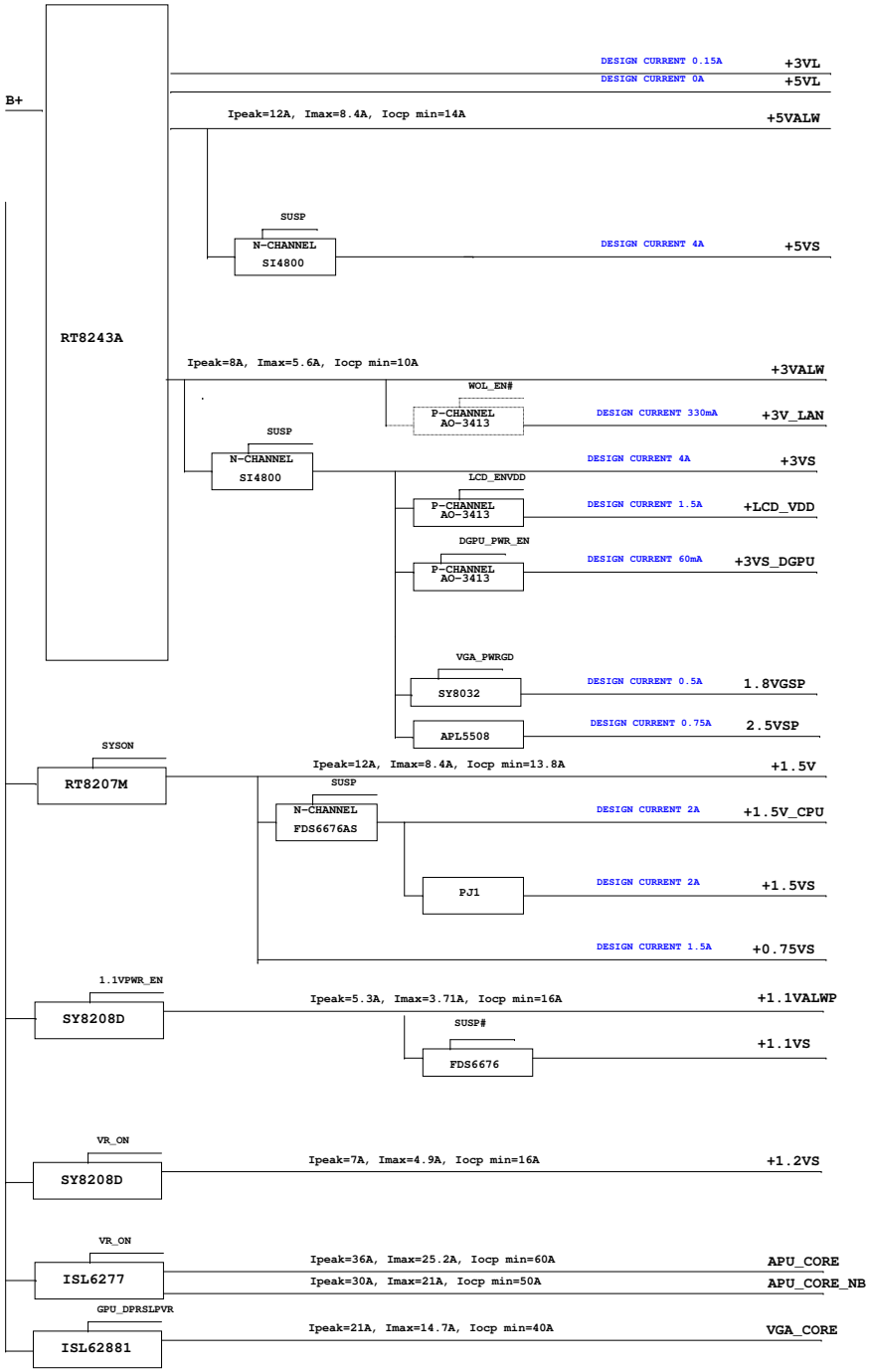

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: Power Tree

Size	Document Number	Rev
	LA-9869P	0.3

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +1.1VALW
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	APU		FCH		GPU	
description			Bolton			
explain	R1	R3	R1	R3	R1	R3
BTO			BOLTONR1@	HUDM3R3@		

Function	3D sensor	KB LED	Clock		UMA/DIS	
description		K			1G	U
explain	G-sensor	KB LED	Green Clock	No Green Clock	DIS	UMA
BTO	GSENSOR@	KBL@	GCLK@	NOGCLK@	VGA@	UMA@

Function	Panel			
description	S	D		
explain	LVDS	eDP		
BTO	LVDS@	IEDP@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	VGA Thermal	82H	1000 0010 b

EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

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Issued Date	2013/01/22	Deciphered Date 2014/01/21	Title: Notes List
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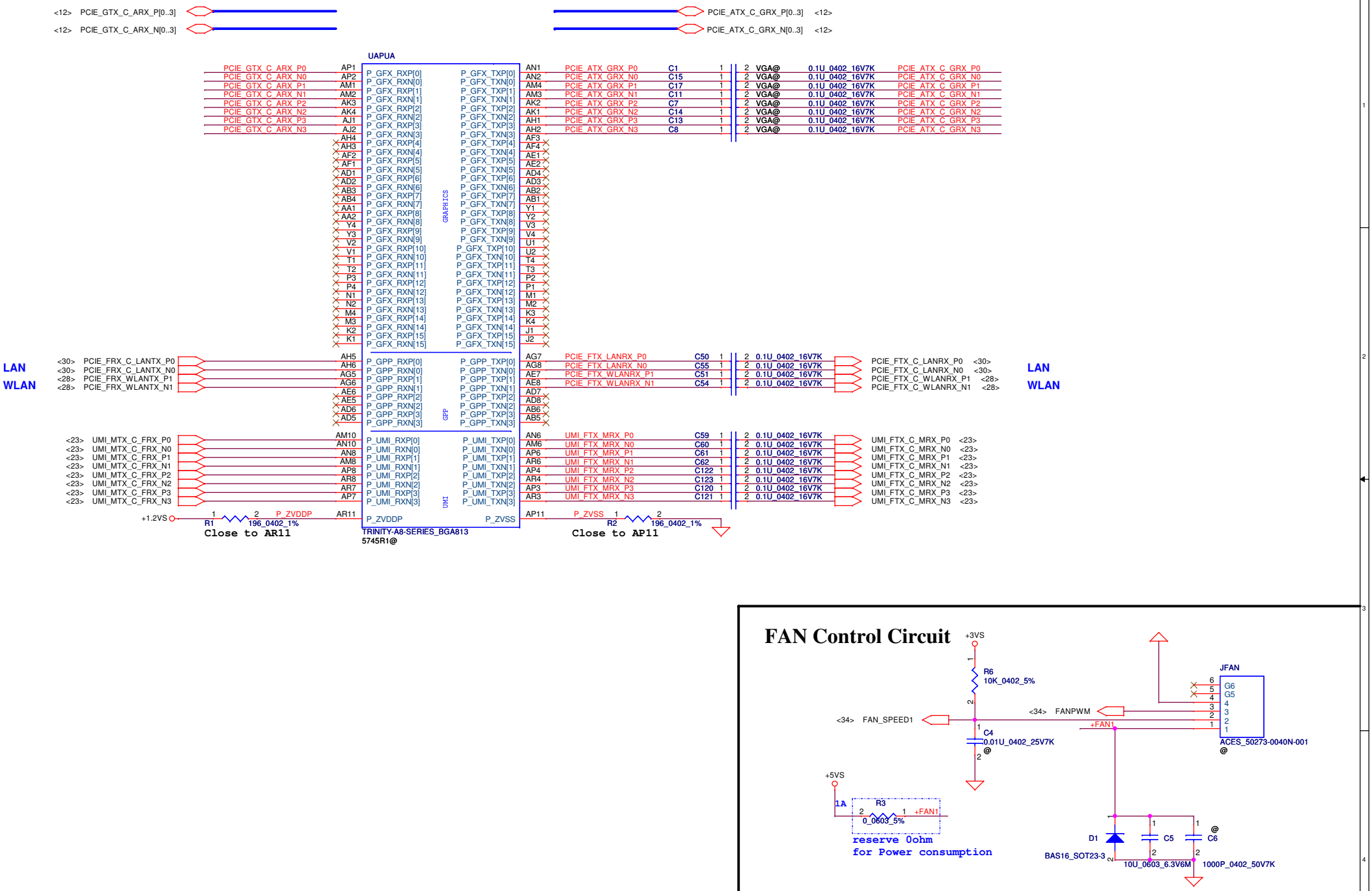

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: AMD Trinity FP2 / GFX / UMI

Size	Document Number	Rev
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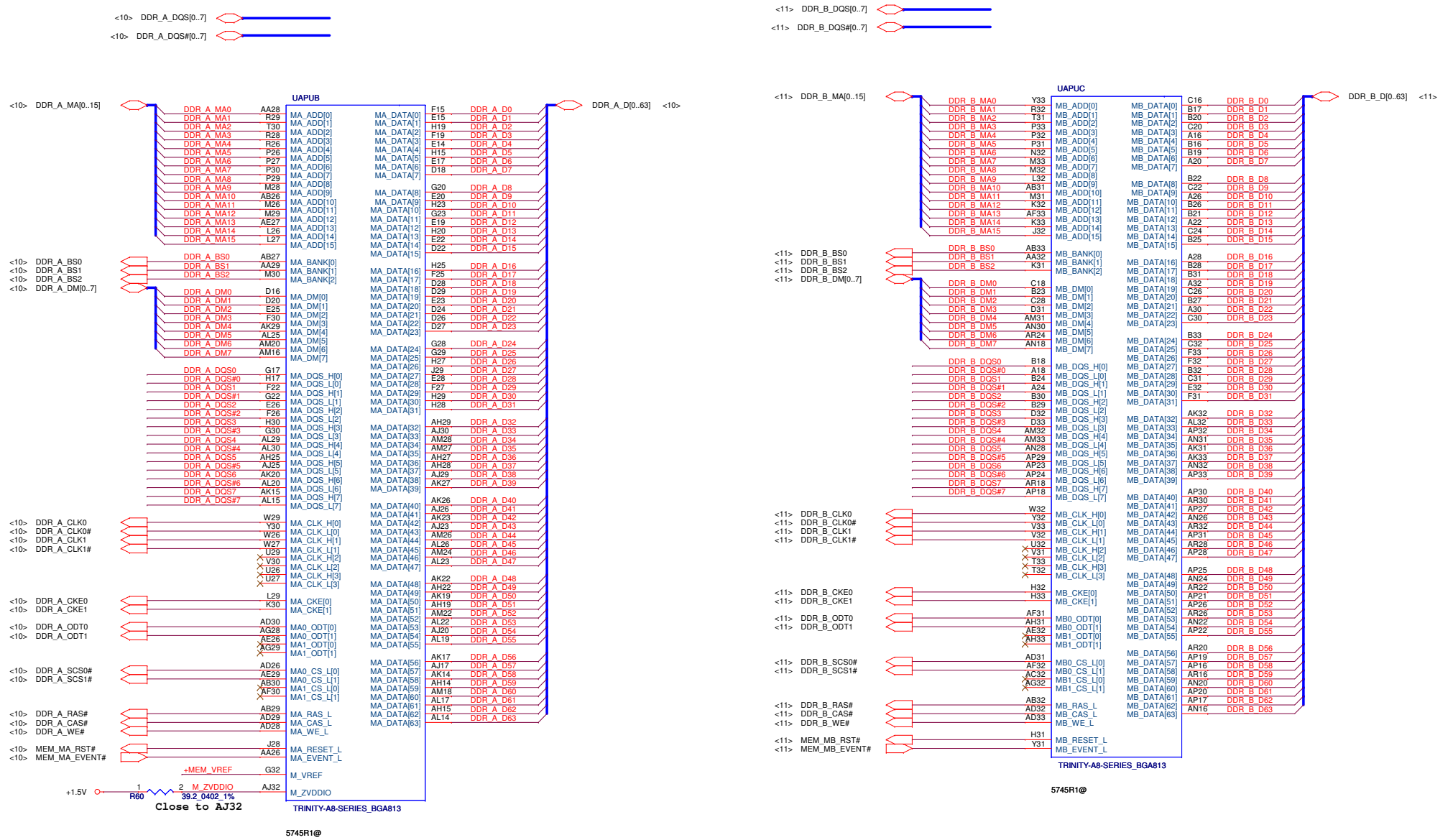

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: AMD Trinity FP2 DDRIII I/F

Size	Document Number	Rev
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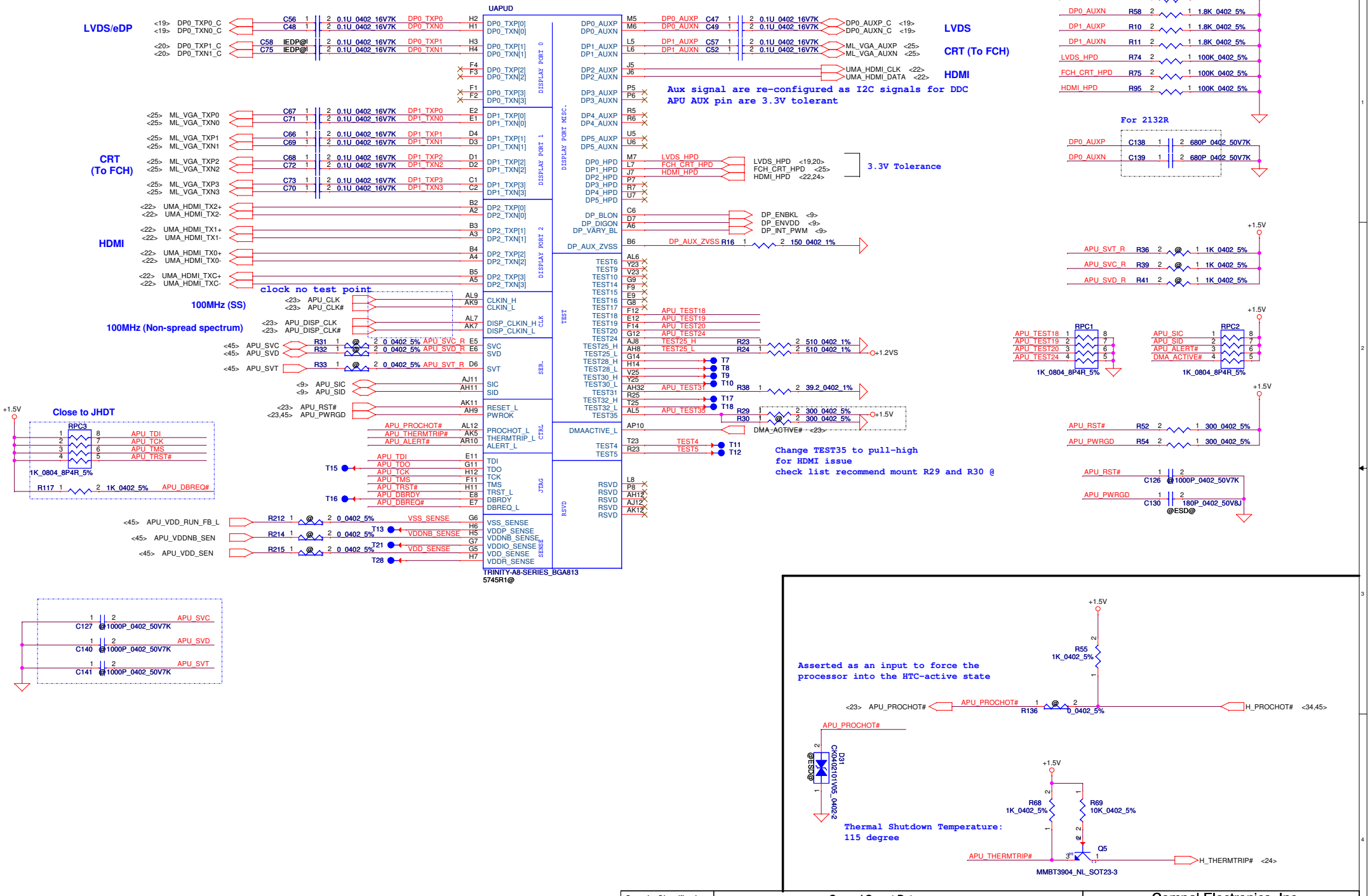

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: AMD Trinity FP2 Display / MISC / HDT

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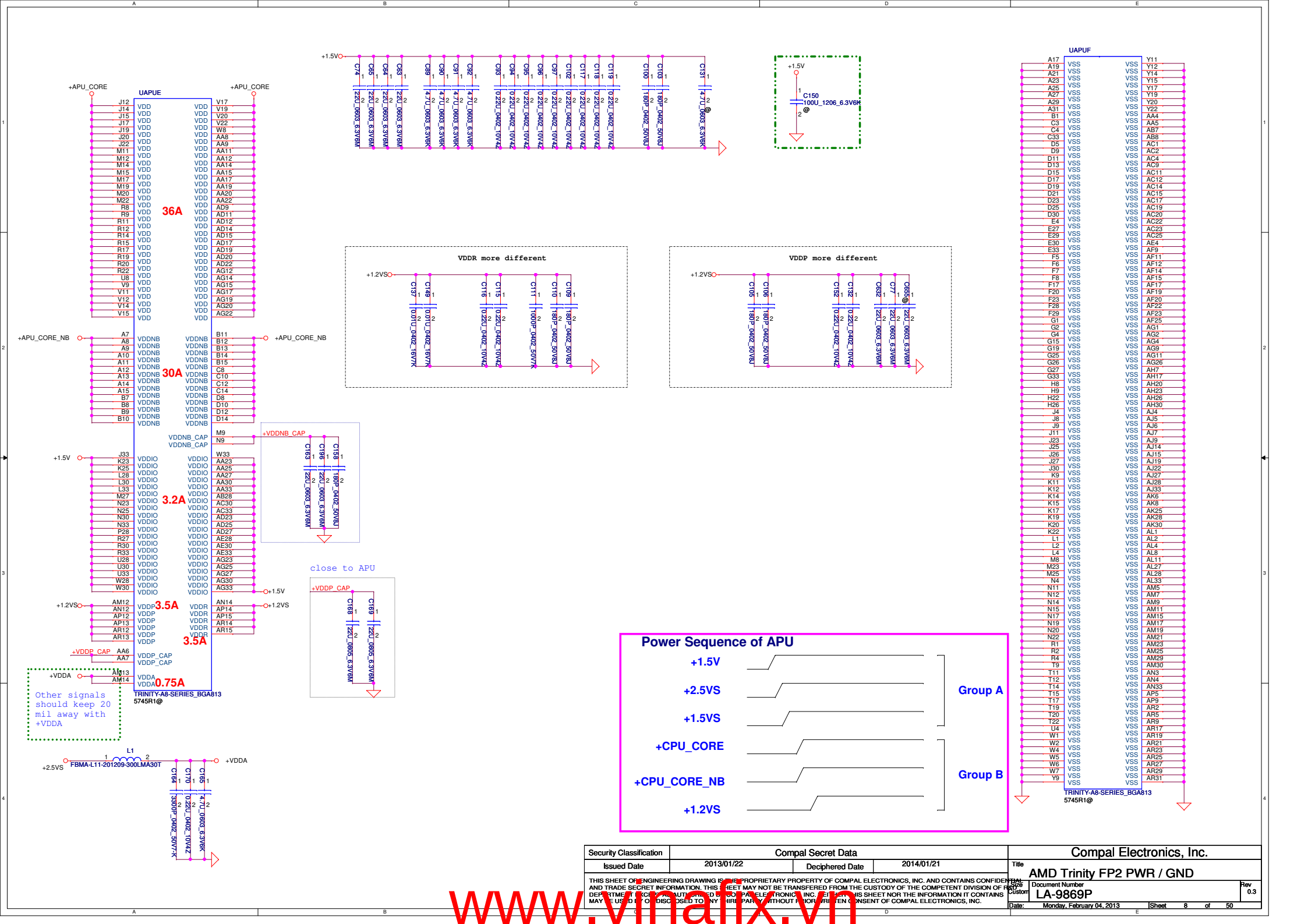

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: AMD Trinity FP2 PWR / GND

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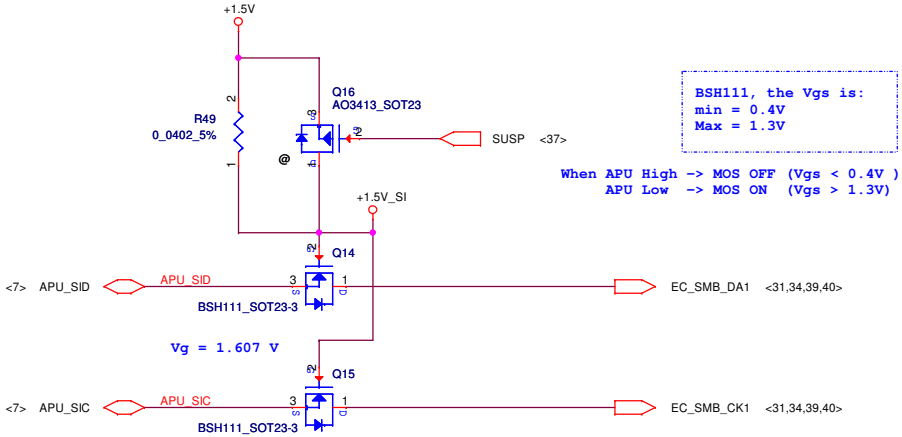
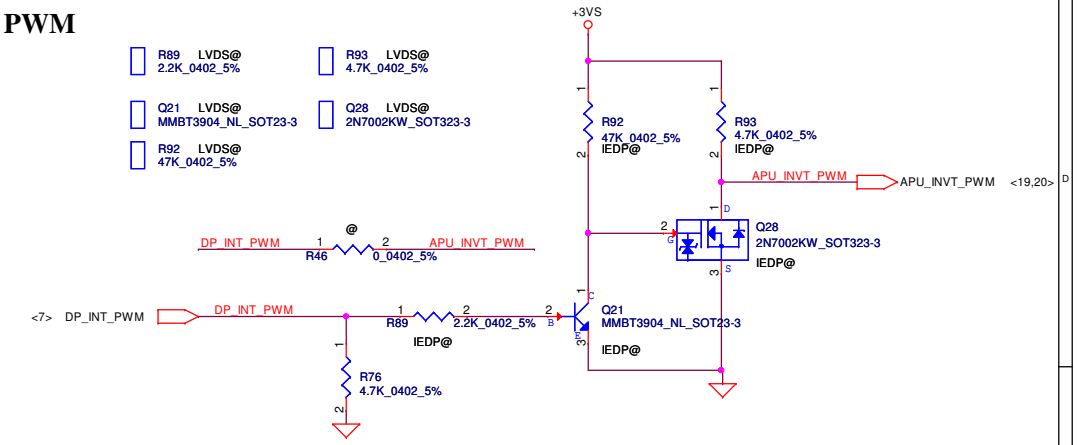
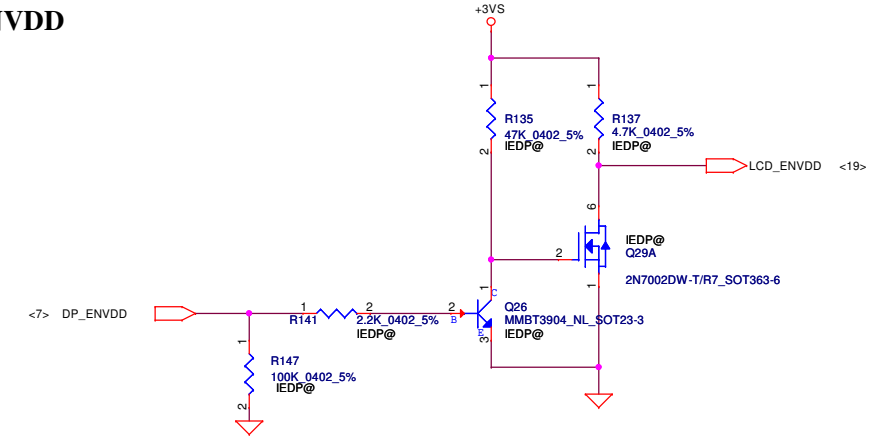
SB-TSI



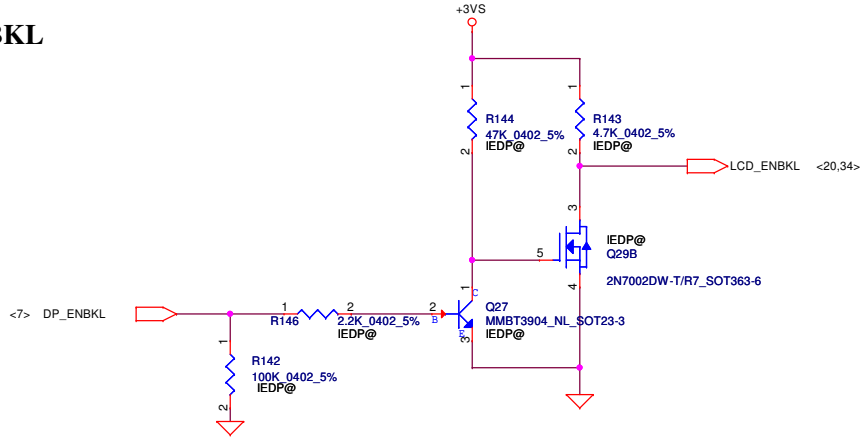
Panel PWM



eDP Panel ENVDD



eDP Panel ENBKL



Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Title: AMD Trinity FP2 Singal Level Shifter

Size	Document Number	Rev
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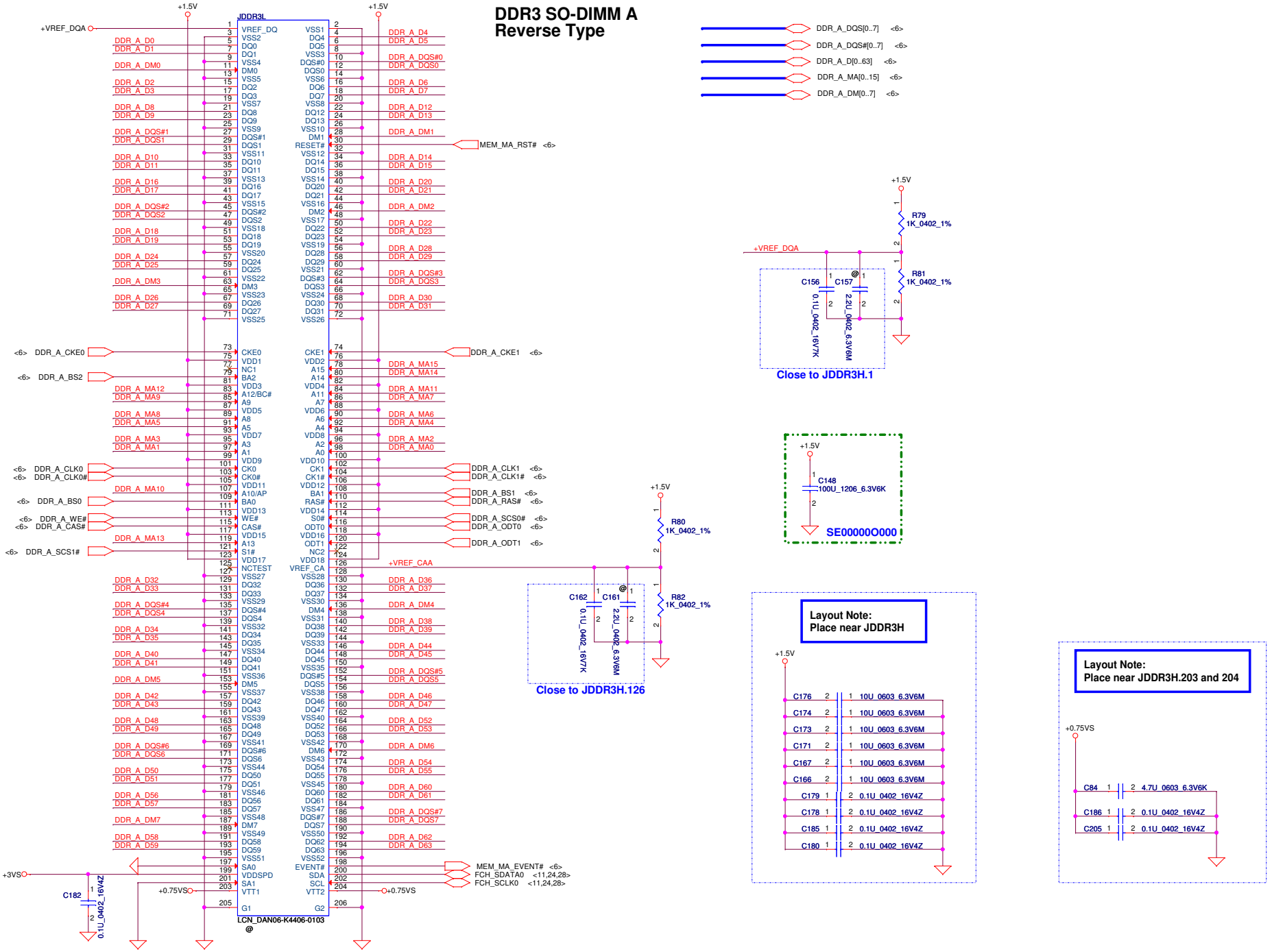
DDR3 SO-DIMM A
Reverse Type



Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM0***

Size	Document Number	Rev
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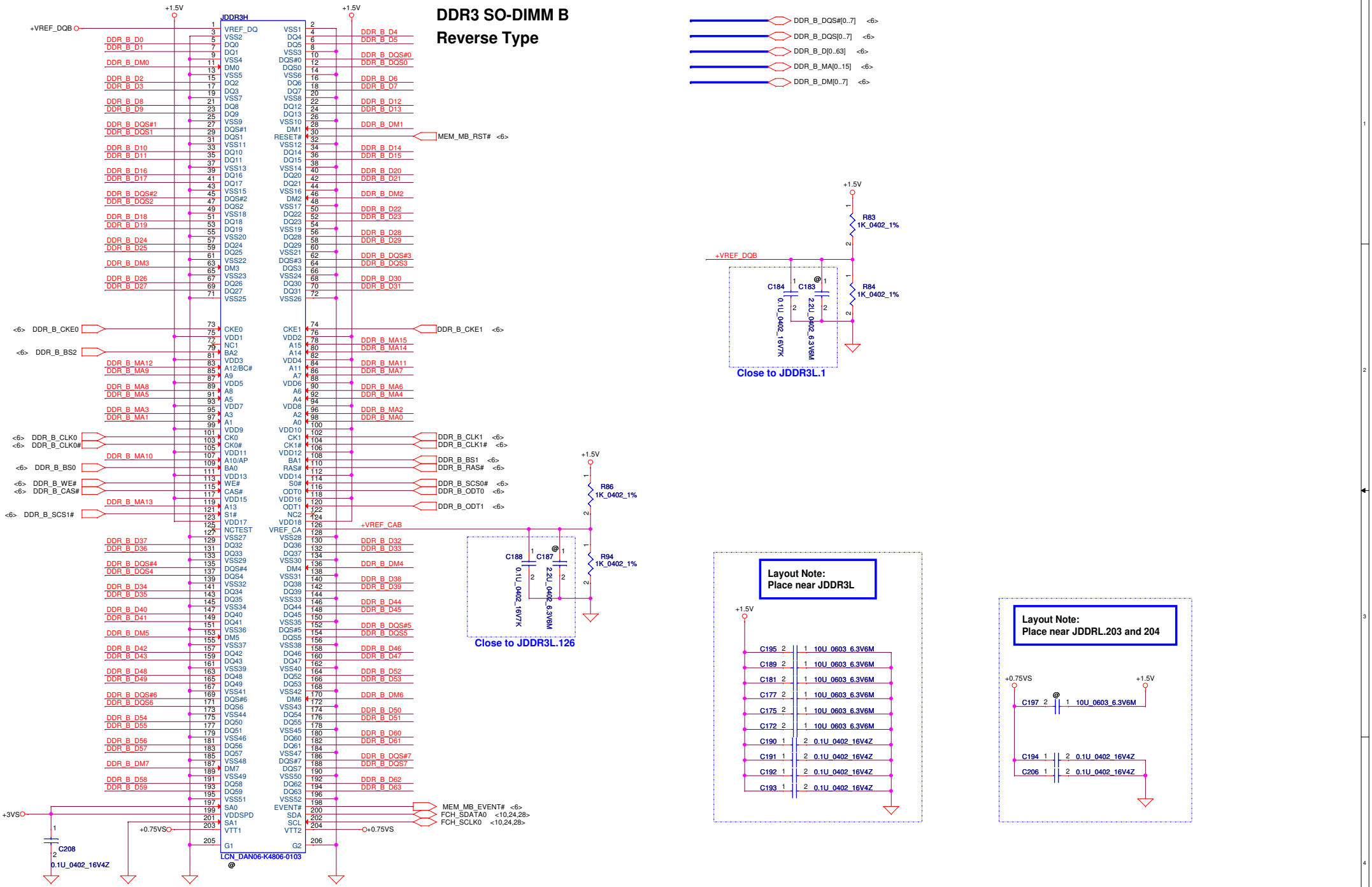
DDR3 SO-DIMM B
Reverse Type



Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM1***

Size	Document Number	Rev
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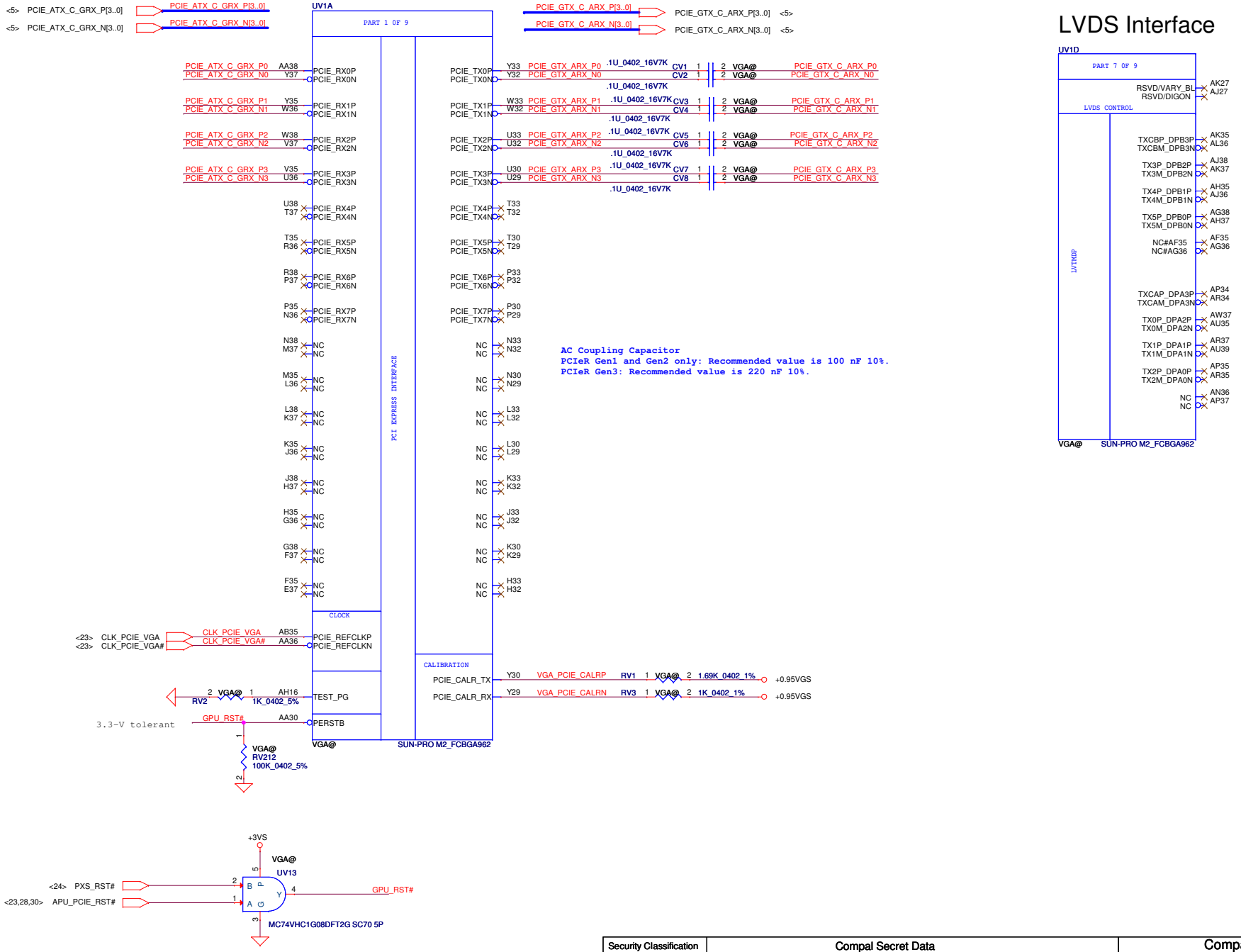

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/22	Deciphered Date 2014/01/21	Title: PCIE/LVDS
Size: B25 Custom	Document Number: LA-9869P		Rev: 0.3
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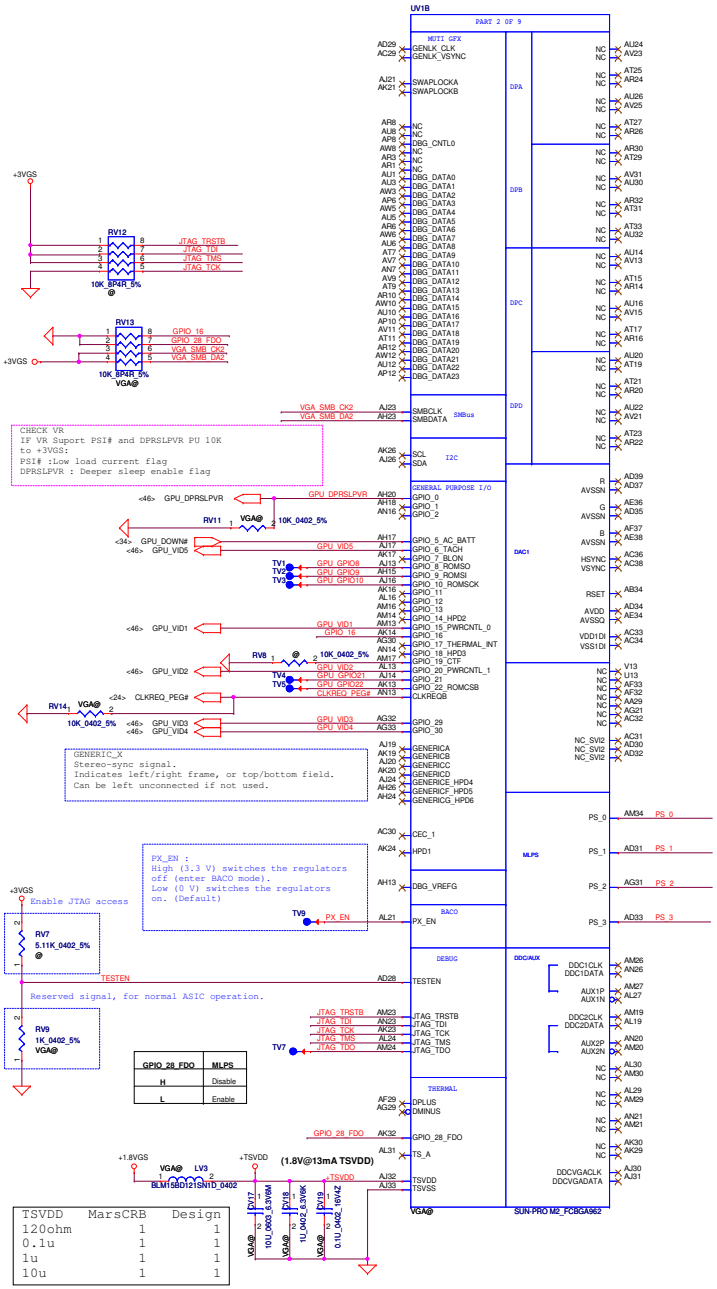


Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Suport PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point.
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109°C by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

MLPS

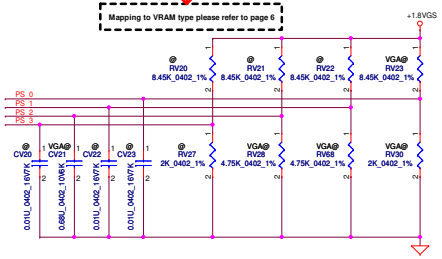
MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

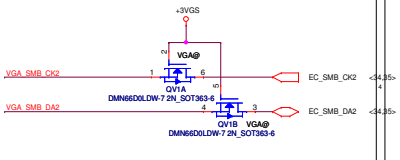
For MEMCLK 1GHZ	Brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHZ	Brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V-1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X





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Compal Electronics, Inc.

Title: Main_MSIC

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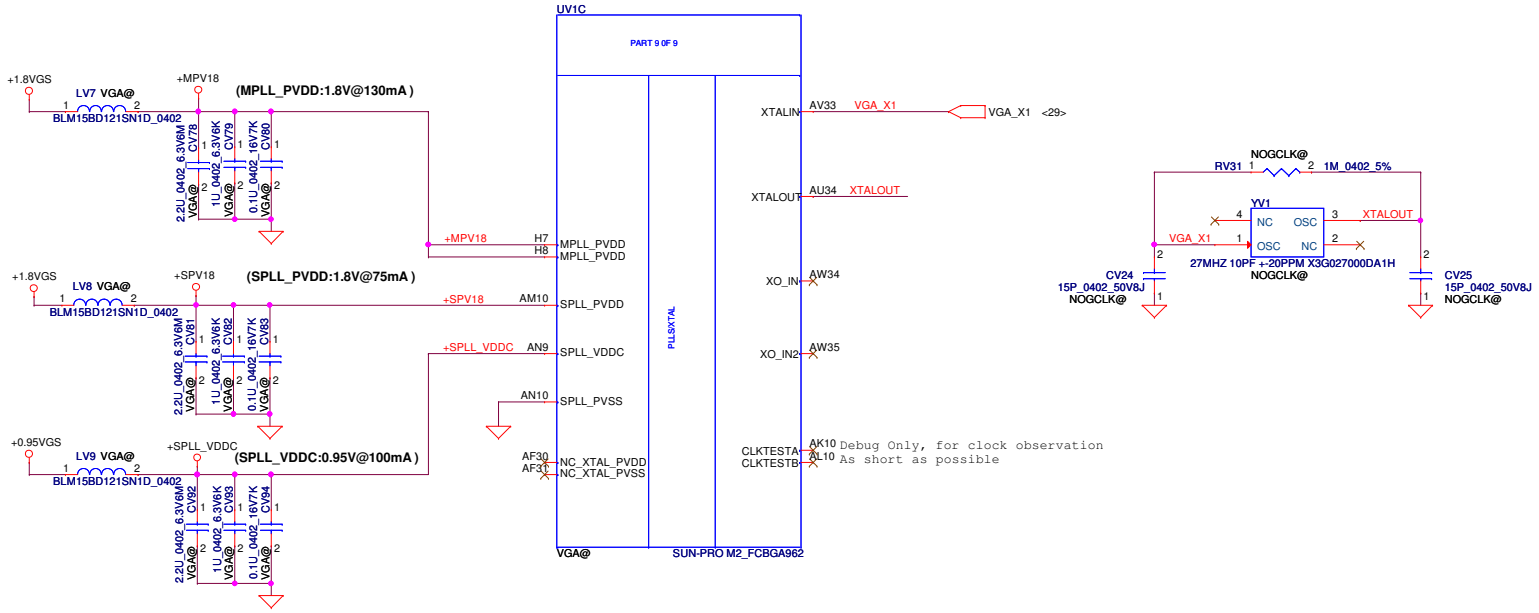
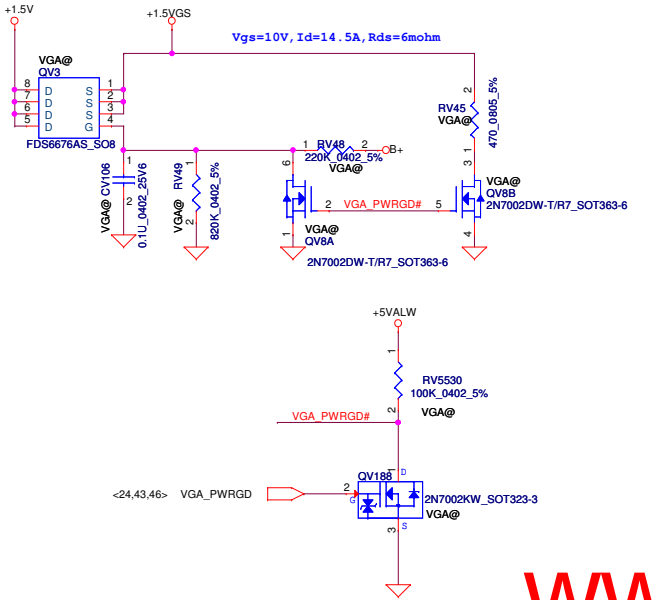
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

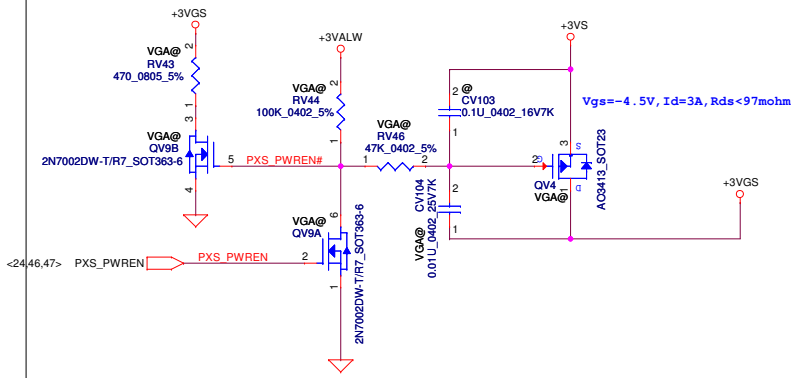
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+1.5V to +1.5VGS



+3VS to +3VGS



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Compal Electronics, Inc.

Title: BACO POWER

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VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

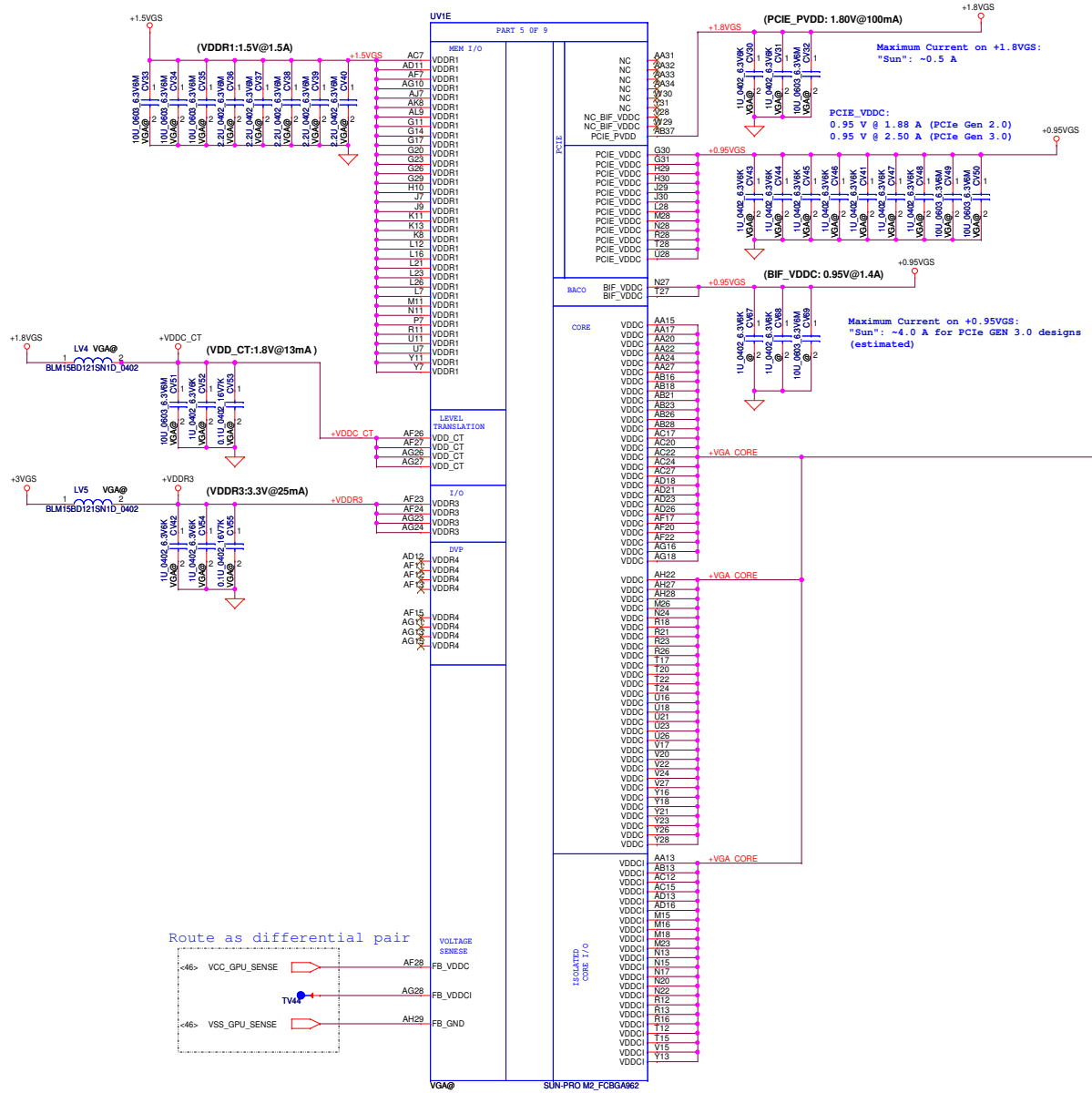
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars check list	Design
120ohm	1	1
1u	3	2
10u	1	0
0.1u	0	1

PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

BIF_VDDC	Mars check list	Design
1u	1	1
10u	1	1



Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

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Title	Power		
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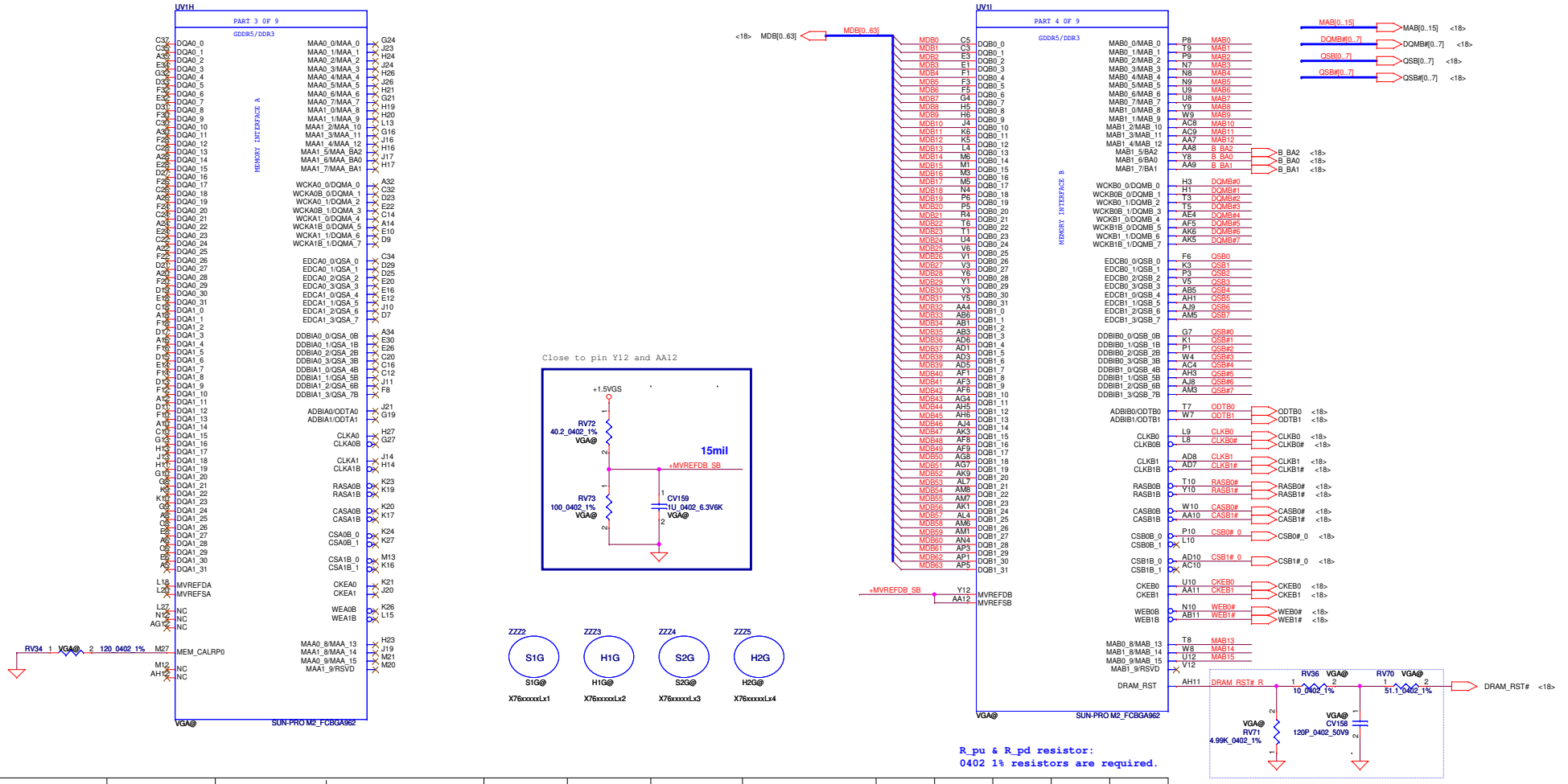


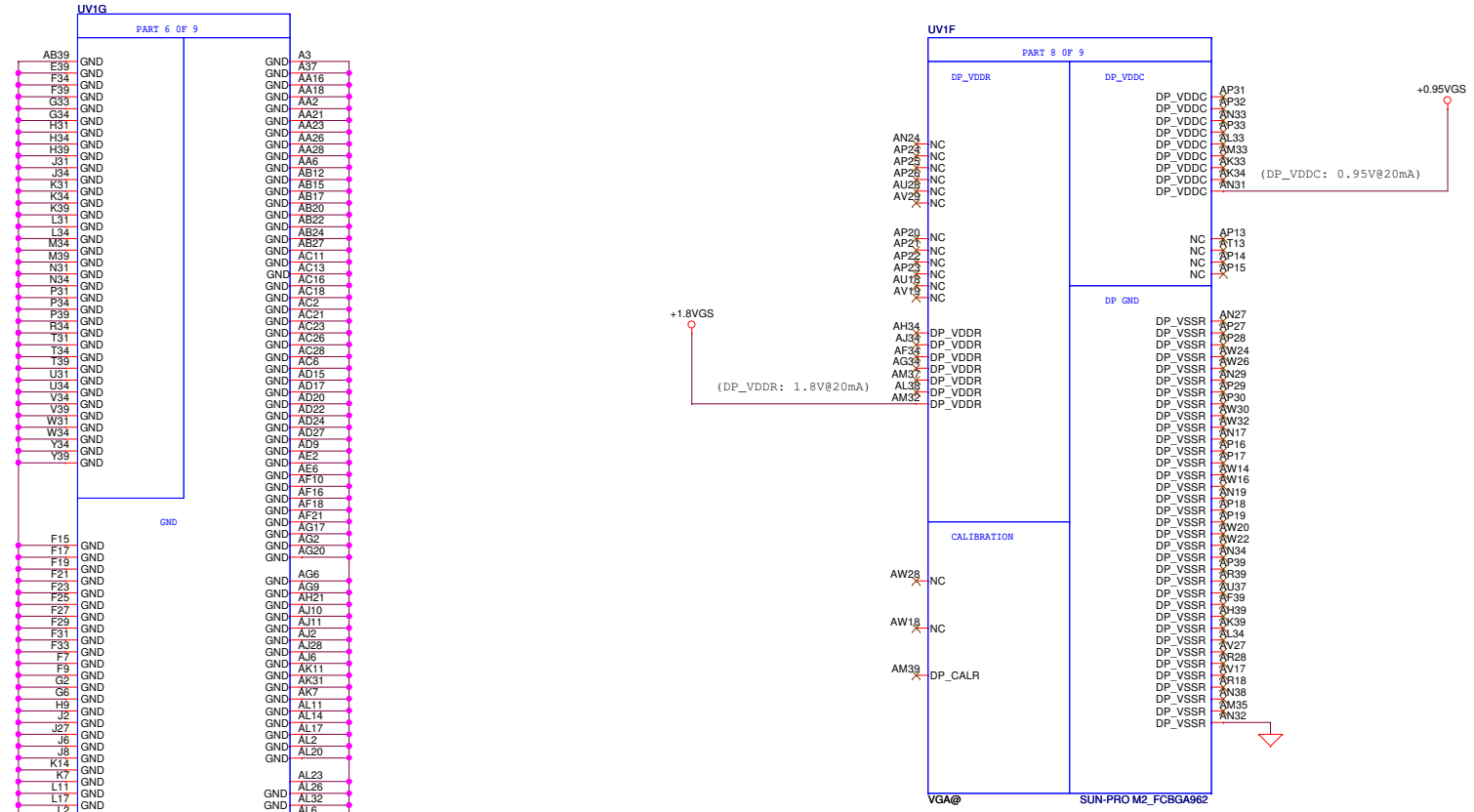
R_pu & R_pd resistor:
0402 1% resistors are required.

Place all these components close to GPU (Within 25mm) and keep all component close to each other

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YOG0	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Hynix	SA000065320	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB10	MT41K128M16JT-107G:K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH40	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

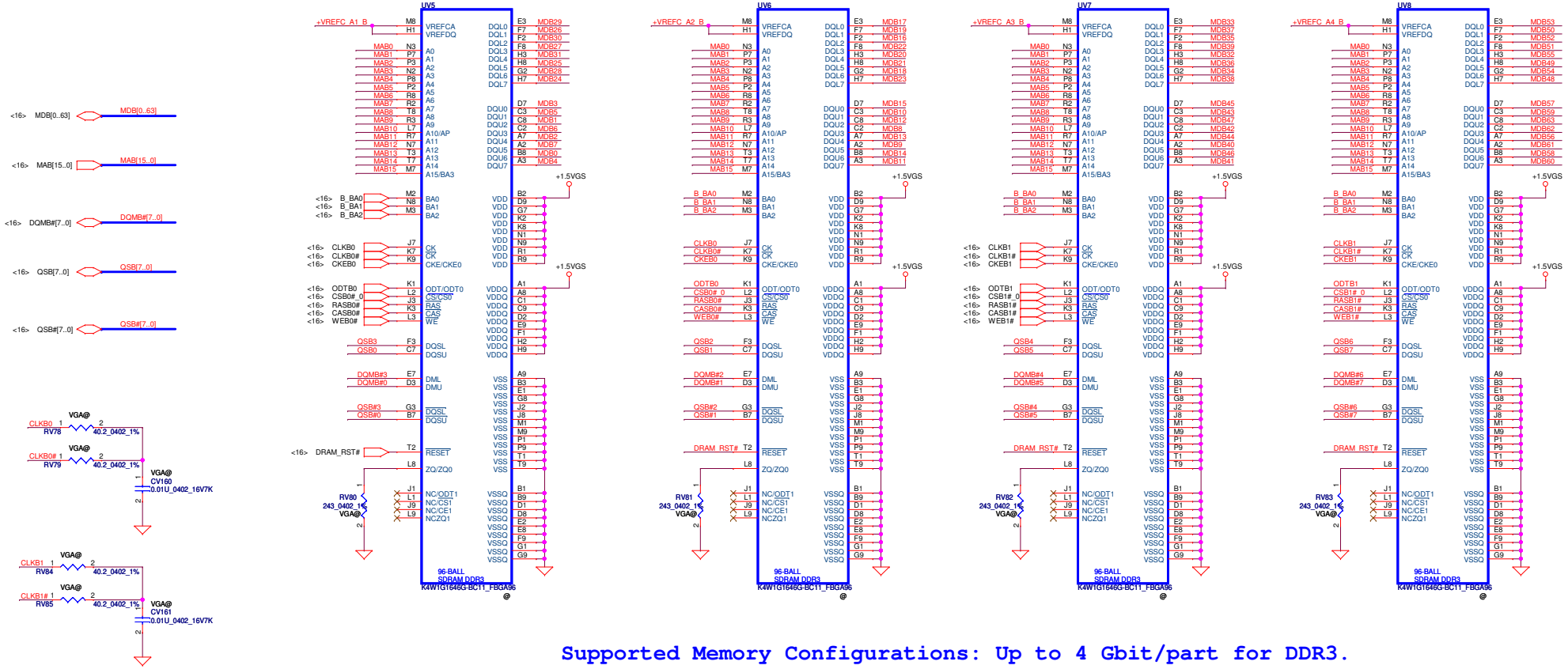
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Title	MEM Interface	
Size C	Document Number LA-9869P	Rev 0.3
Date: Monday, February 04, 2013	Sheet 16 of 50	

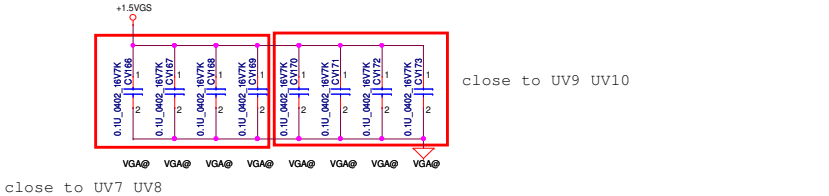


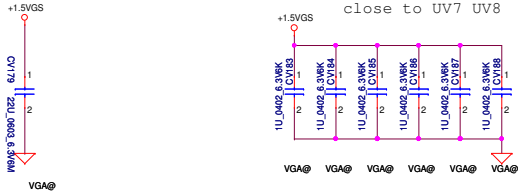
Compal Electronics, Inc.			
Title	PWR_GND		
Size: Custom	Document Number: LA-9869P		Rev: 0.3
Date: Monday, February 04, 2013	Sheet 17 of 50		

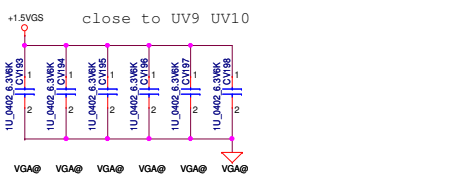
CHANNEL B: 512MB/1024MB DDR3



Supported Memory Configurations: Up to 4 Gbit/part for DDR3.







Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: VRAM Channel B

Size	Document Number	Rev
C	LA-9869P	0.3

Date: Monday, February 04, 2013 | Sheet 18 of 50

SWR / LDO Mode select

	LDO	SWR
2132R	RT24	mount LT3

※ If use 2132R, please select LDO mode as default.

reserve 0ohm
for Power consumption

+3VS — 80mil — LVDS@ RT1 2 0_0603_5% — 80mil — +3VS_RT

Close to Pin3

+DP_V33 — CT1 10U_0603_6.3V6M — CT2 0.1U_0402_16V4Z — CT3 0.1U_0402_16V4Z — LVDS@

Close to LT2 / Close to Pin18

+SWR_VDD — CT4 10U_0603_6.3V6M — CT5 0.1U_0402_16V4Z — CT6 22U_0603_6.3V6M — CT7 0.1U_0402_16V4Z — CT8 0.1U_0402_16V4Z — LVDS@

Close to Pin13

Close to L29

+SWR_V12 — CT9 10U_0603_6.3V6M — CT10 0.1U_0402_16V4Z — CT11 0.1U_0402_16V4Z — CT12 0.1U_0402_16V4Z — LVDS@

Close to Pin27 / Close to Pin7

R476/481/480/482 need to place under UT2
In orfer to reduce sub-trace

DP0_AUXP_C / DP0_AUXN_C — R476 IEDP@ 0_0402_5% — LCD_EDID_CLK
DP0_AUXP_C / DP0_AUXN_C — R481 IEDP@ 0_0402_5% — LCD_EDID_DATA
<7> DP0_AUXP_C
<7> DP0_AUXN_C
DP0_TXP0_C / DP0_TXN0_C — R480 IEDP@ 0_0402_5% — LCD_TXOUT0+
DP0_TXP0_C / DP0_TXN0_C — R482 IEDP@ 0_0402_5% — LCD_TXOUT0-
<7> DP0_TXP0_C
<7> DP0_TXN0_C

Mode Configure

ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
※EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

〈 ※Default mode 〉

+3VS_RT — RT4 @ 4.7K_0402_5% — MIIC_SDA — RT6 LVDS@ 4.7K_0402_5% — PIN30
+3VS_RT — RT12 LVDS@ 4.7K_0402_5% — MIIC_SCL — RT7 @ 4.7K_0402_5% — PIN31

+3VS_RT — LVDS@ LT1 FBMA-L11-201209-221LMA30T_0805 — +DP_V33 — 40mil — DP_V33
+3VS_RT — LVDS@ LT2 FBMA-L11-201209-221LMA30T_0805 — +SWR_VDD — 100mil — SWR_VDD PVCC
+SWR_V12 — 40mil — SWR_LX; 40mil — SWR_VCCK; 40mil — VCCK; 40mil — DP_V12

UT2 RTD2132R

Power / LVDS:
TXEC+ / TXEC- — LCD_TXCLK+ <20> / LCD_TXCLK- <20>
TXE2+ / TXE2- — LCD_TXOUT2+ <20> / LCD_TXOUT2- <20>
TXE1+ / TXE1- — LCD_TXOUT1+ <20> / LCD_TXOUT1- <20>
TXE0+ / TXE0- — LCD_TXOUT0+ <20> / LCD_TXOUT0- <20>

DP_AUX_CH / GPIO:
DP0_AUXP_C / DP0_AUXN_C — AUX_P / AUX_N
DP0_TXP0_C / DP0_TXN0_C — LANE0P / LANE0N
GPIO(PWM OUT) — TL_INVT_PWM — 80mil — +LCD_VDD_R — TL_INVT_PWM <20>
GPIO(Panel_VCC)
GPIO(PWM IN) — APU_INVT_PWM <20,9> / EC_ENBKL <34>
GPIO(BL_EN)

Other:
<34> EC_SMB_CK3 — CIICSCL1 — LVDS EDID MIICSCL1 — LCD_EDID_CLK — LCD_EDID_CLK <20>
<34> EC_SMB_DA3 — CIICSDA1 — LVDS EDID MIICDA1 — LCD_EDID_DATA — LCD_EDID_DATA <20>
<20,7> LVDS_HPD — HPD
ROM — MIICSCL0 — MIIC_SCL; MIICSDA0 — MIIC_SDA
DP_REXT
DP_GND
GND

RT8 12K_0402_1% LVDS@ — Close to Pin8

LVDS@ RTD2132R-VE-CG_QFN32_5X5 SA000069200

LCD_EDID_DATA — RT9 LVDS@ 4.7K_0402_5% — +3VS_RT
LCD_EDID_CLK — RT10 LVDS@ 4.7K_0402_5%

R8 for power consumption
Remove on PVT phase

+LCD_VDD_R — R8 LVDS@ 0_0805_5% — +LCD_VDD
CT13 4.7U_0603_6.3V6K LVDS@ — RT113 100K_0402_5% LVDS@
Close to Panel conn.

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

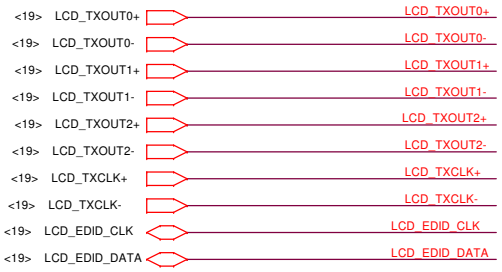
LCD POWER CIRCUIT (For eDP panel only)

+3VS — W=80mils — U18 APL3512ABI-TRG_SOT23-5 (VIN, SS, VOUT, GND, EN) — W=80mils — +LCD_VDD
+LCD_VDD_SS — C2 1500P_0402_50V7K IEDP@
IEDP@ SA00003AR00
R104 IEDP@ 0_0402_5% — Close to Pin15 — LCD_ENVDD <9>
R112 100K_0402_5% IEDP@

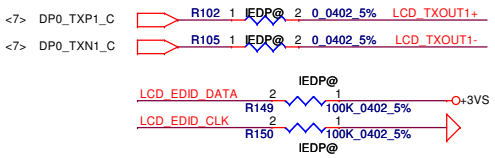
Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

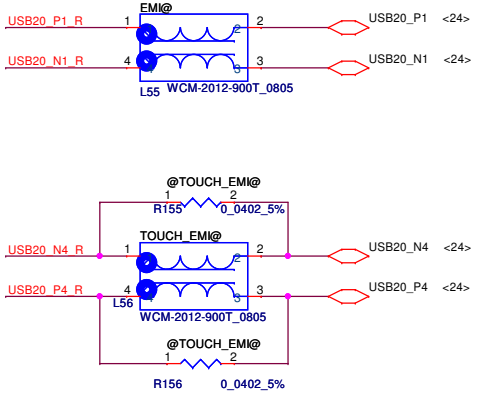
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/22	Deciphered Date 2014/01/21	Title: LVDS Translator - RTD2132S
Size: Custom	Document Number: LA-9869P		Rev: 0.3
Date: Monday, February 04, 2013	Sheet 19 of 50		

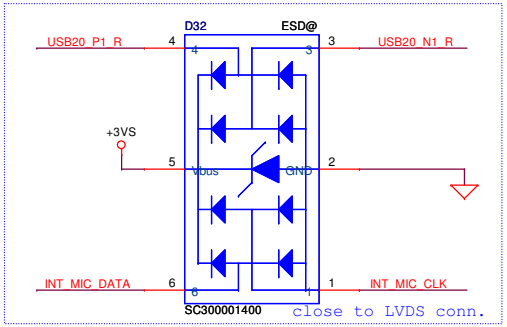
For LVDS 1ch Panel



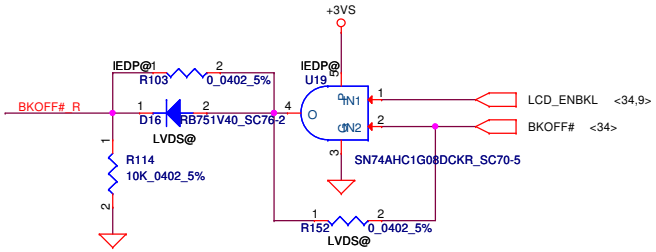
For eDP Panel

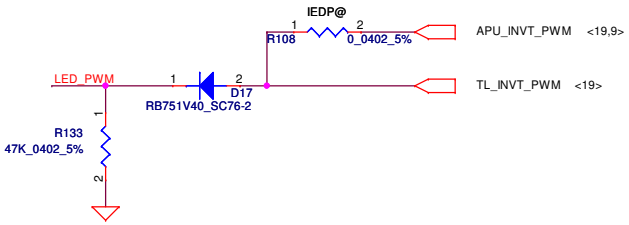


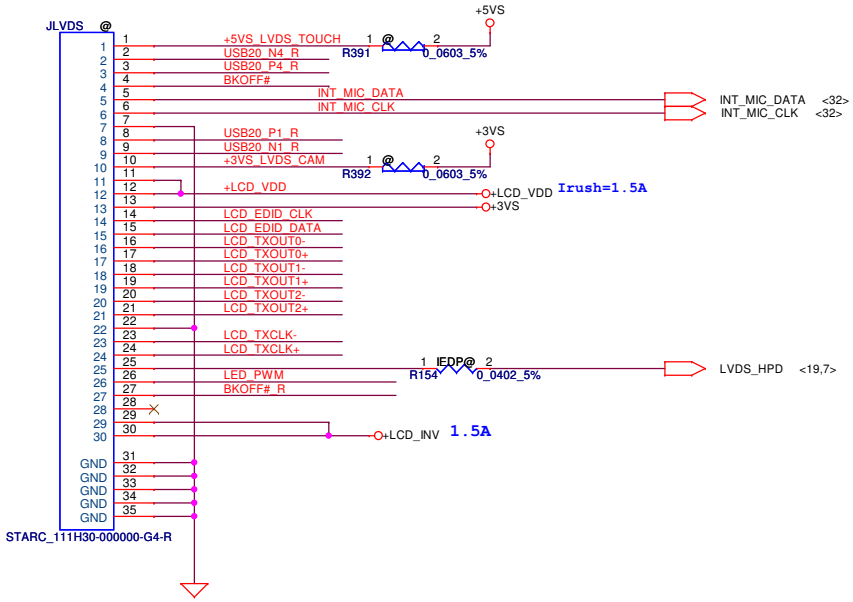




Reserve for eDP panel potience issue







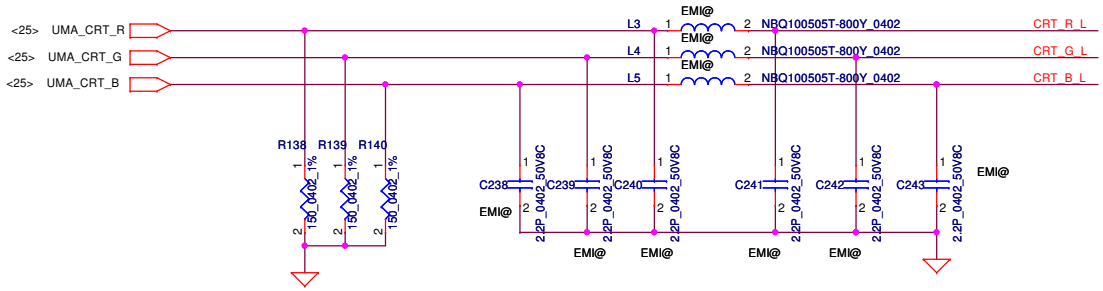
Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

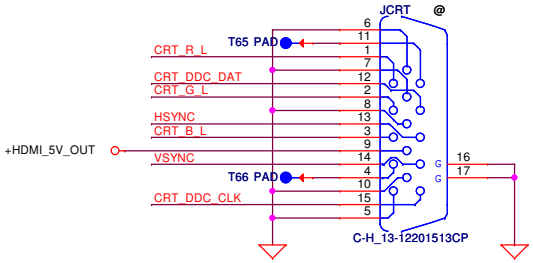
Compal Electronics, Inc.

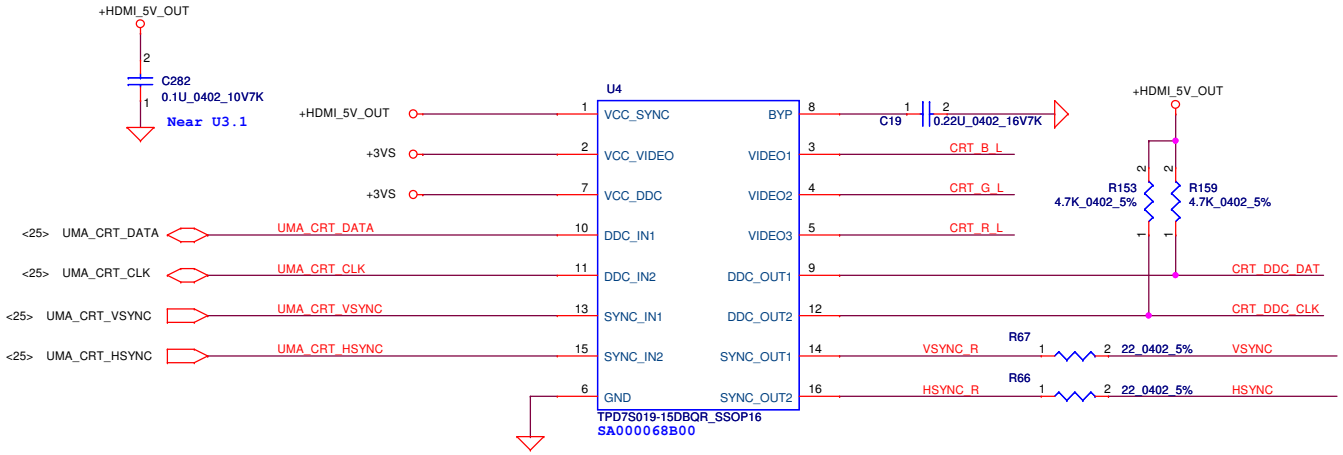
Title: LVDS

Size: Custom | Document Number: LA-9869P | Rev: 0.3

Date: Monday, February 04, 2013 | Sheet 20 of 50







Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: ***CRT***

Size	Document Number	Rev
	LA-9869P	0.3

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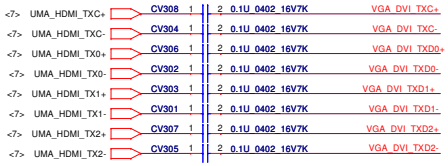
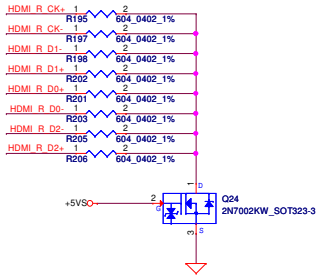
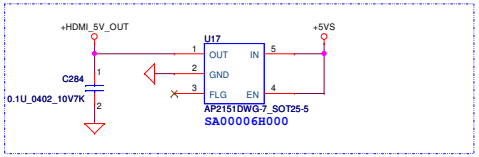




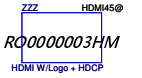
Change R184 and R185 from 2K to 4.7K
for HDMI detect issue on Comal

HDMI POWER CIRCUIT

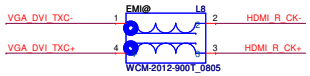
VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A

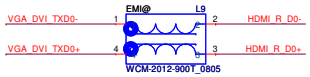


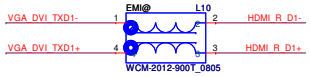
HDMI Royalty

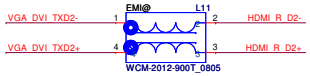


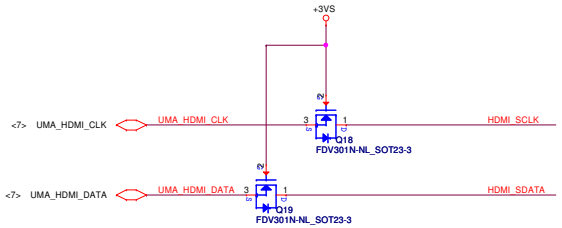
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM



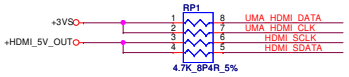


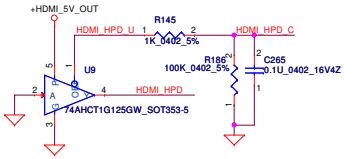




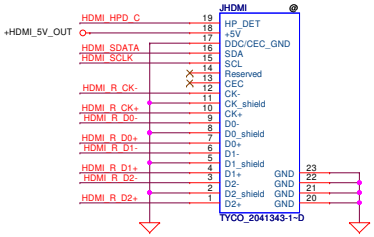


Q18/Q19
Change to FDV301 due to BSH111 EOL





HDMI Connector



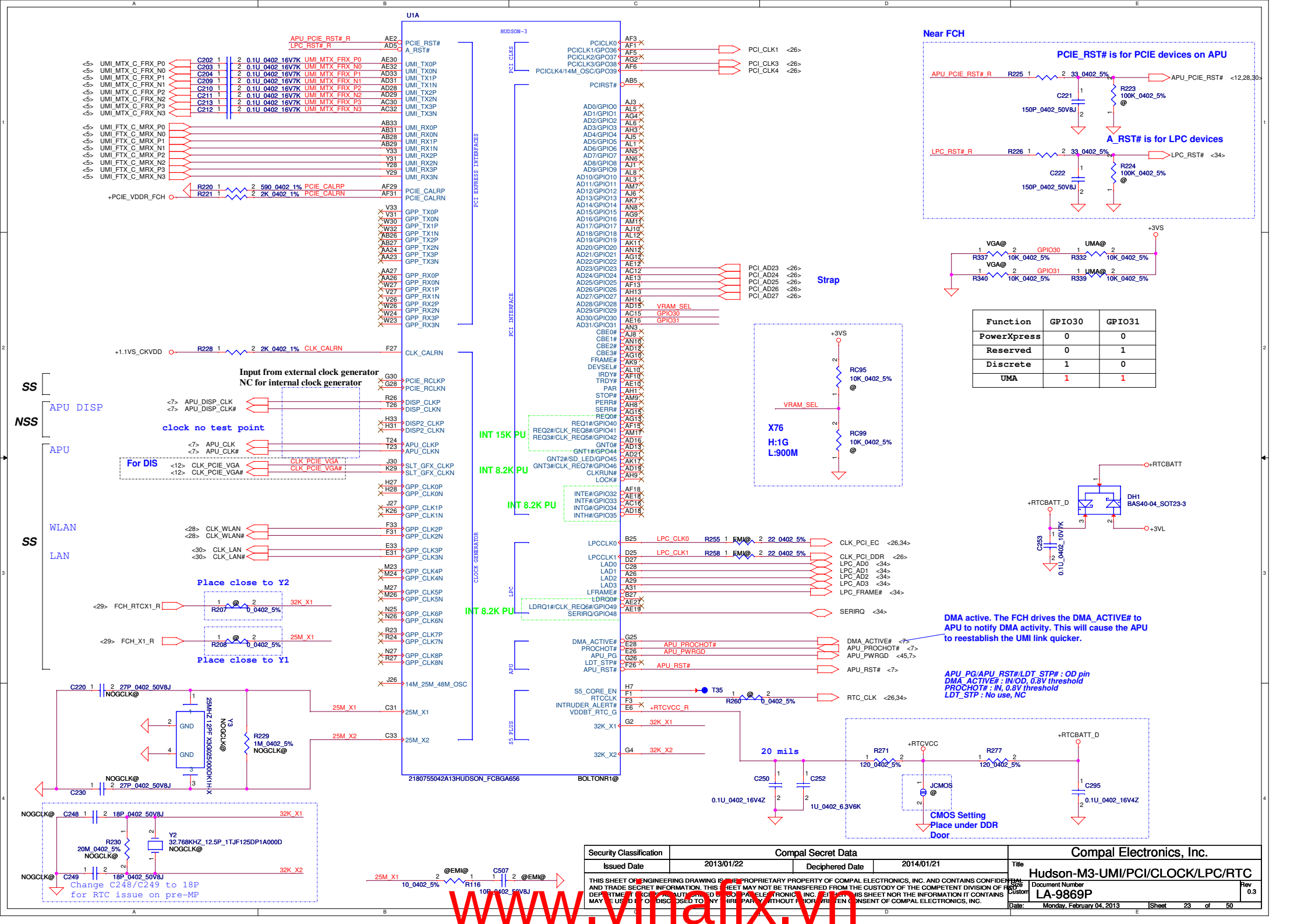
Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: HDMI Conn./CEC

Size: | Document Number: LA-9869P | Rev: 0.3

Date: Monday, February 04, 2013 | Sheet 22 of 50


U1A
HUDSON-3
PCI_CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
S5 PLUIS
2180755042A13HUDSON_FCBGA656
BOLTONR1@
Near FCH
PCIE_RST# is for PCIE devices on APU
APU_PCIE_RST# R
APU_PCIE_RST# <12,28,30>
A_RST# is for LPC devices
LPC_RST# R
LPC_RST# <34>
Strap
VRAM_SEL
X76
H:1G
L:900M
Function | GPIO30 | GPIO31
PowerXpress | 0 | 0
Reserved | 0 | 1
Discrete | 1 | 0
UMA | 1 | 1
Input from external clock generator
NC for internal clock generator
SS
APU DISP
NSS
clock no test point
APU
For DIS
WLAN
SS
LAN
Place close to Y2
Place close to Y1
INT 15K PU
INT 8.2K PU
INT 8.2K PU
INT 8.2K PU
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.
APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
20 mils
CMOS Setting
Place under DDR
Door
Change C248/C249 to 18P
for RTC issue on pre-MP
Security Classification | Compal Secret Data
Issued Date | 2013/01/22 | Deciphered Date | 2014/01/21
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Compal Electronics, Inc.
Title: Hudson-M3-UMI/PCI/CLOCK/LPC/RTC
Size: Custom | Document Number: LA-9869P | Rev: 0.3
Date: Monday, February 04, 2013 | Sheet 23 of 50
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PCIE_RST2# is for PCIE devices on FCH

GEVENT#2~22 INT 10K PU

U1D

HUDSON-3

T50

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO56
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT24/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STA0/GEVENT11#
CLK_REQ8#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

2180755042A13HUDSON_FCBGA656

BOLTONR1@

USB 1.1 MISC
USB 2.0
GPIO
USB OC
HD AUDIO
USB 3.0
EMBEDDED CTRL

INT 15K PD
INT 15K PD
INT 8.2K PU
INT 8.2K PU
INT 8.2K PU
INT 10K PU
INT 10K PU
INT 50K PD
INT 10K PU
INT 10K PU
INT 10K PU
INT 10K PU

USB 3.0-Right 2
USB 3.0-Right 1
Touch
WLAN (BT)
Card reader
Int. Camera
USB-Left 1
USB 3.0-Right 2
USB 3.0-Right 1

Hudson-M2/M3
OHCI (DEV-20, FUN-5)
Hudson-M2
OHCI (DEV-22, FUN-0)
EHCI (DEV-22, FUN-2)
Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)
Hudson-M2/M3
OHCI (DEV-19, FUN-0)
EHCI (DEV-19, FUN-2)
Hudson-M2/M3
OHCI (DEV-18, FUN-0)
EHCI (DEV-18, FUN-2)
<Support Wakeup>
Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

Strap

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

USB_OC2# is for right USB2.0 ports
USB_CHG_OC# is for right USB3.0 ports
USB_OC0# is for right USB3.0 ports

For ESD request

For FCH internal debug use

For DIS

Place R425 and C363
close to FCH for ESD

Security Classification: Compal Secret Data
Issued Date: 2013/01/22
Deciphered Date: 2014/01/21

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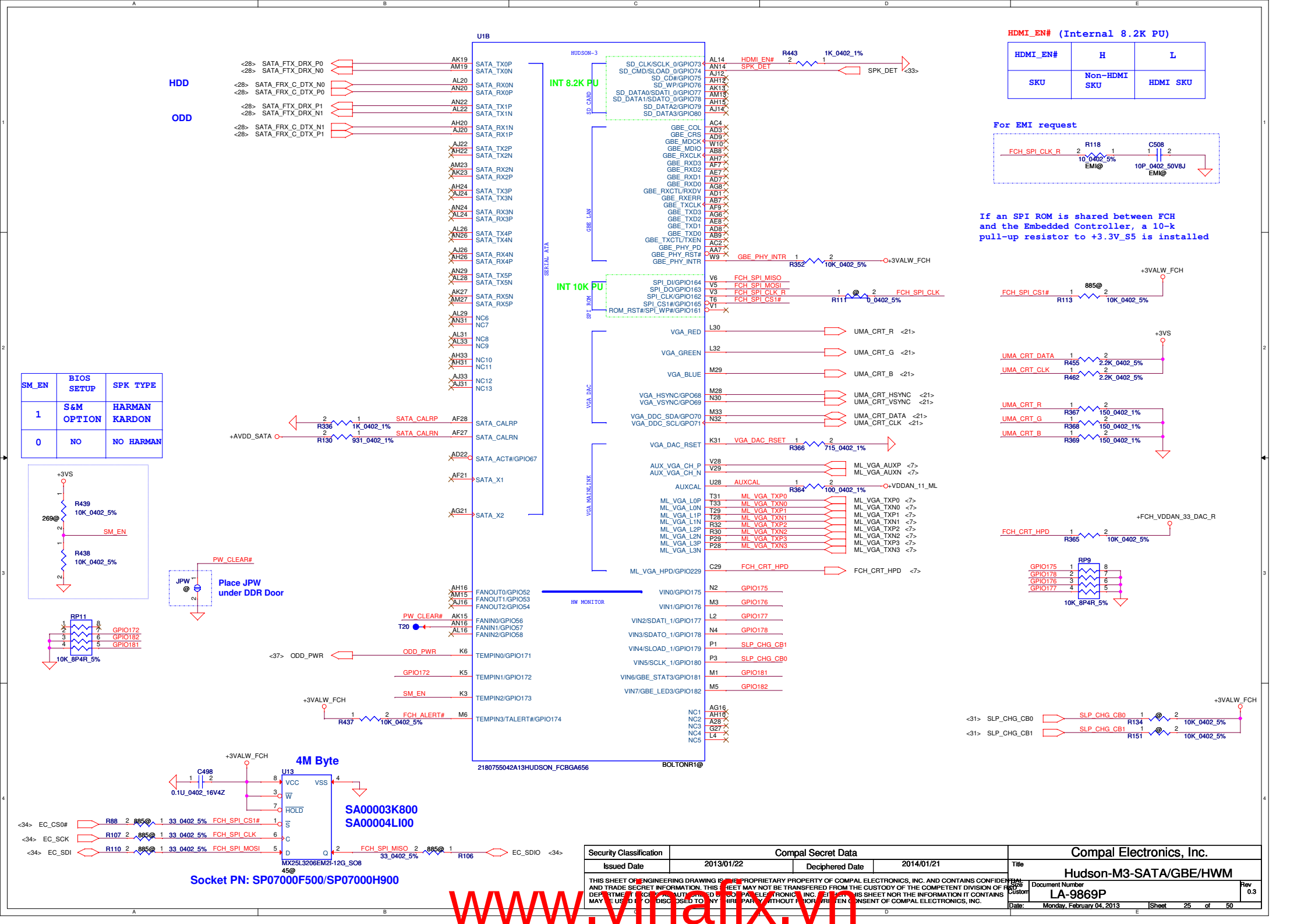
Compal Electronics, Inc.

Title: Hudson-M3-ACPI/USB/EC

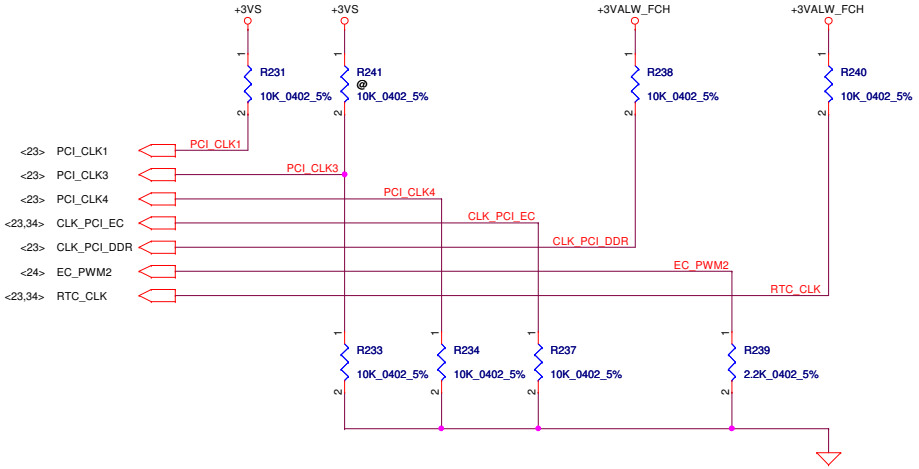
Size: Custom | Document Number: LA-9869P | Rev: 0.3

Date: Monday, February 04, 2013 | Sheet 24 of 50



STRAP PINS

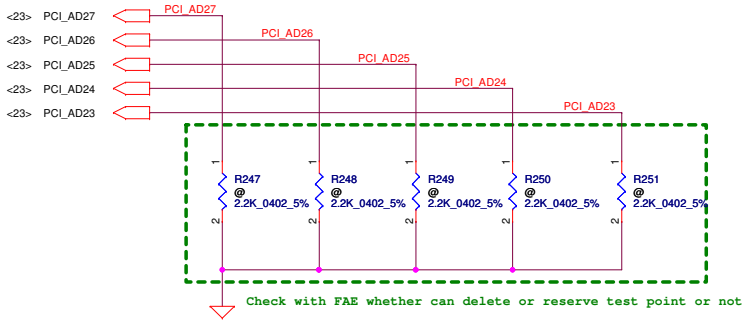
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

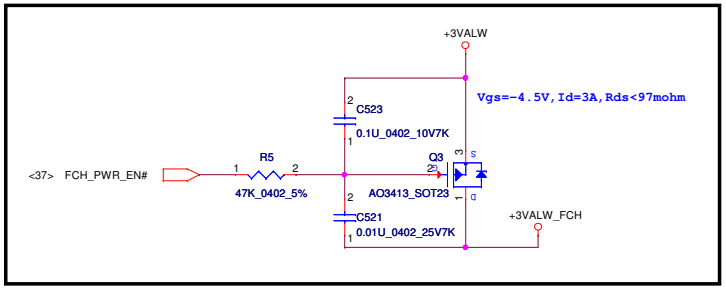


DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.

Title: Hudson-M3-STRAP

Size: Custom | Document Number: LA-9869P | Rev: 0.3

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reserve 0ohm
for Power consumption

reserve 0ohm
for Power consumption

VDDPL_33_SSUSB_S
For Hudson M3 USB3.0 only
For Hudson M2, connect to GND

LDO_CAP: Internally generated 1.8V
supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI

U1C

HUDSON-3

U1E

HUDSON-3

GROUND

2180755042A13HUDSON_FCBGA656

BOLTONR1@

No more than two balls sharing any single via.
Note: Use of a single via per ball is preferred.

Connect to GND through a dedicated via

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

reserve 0ohm
for Power consumption

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Issued Date	2013/01/22	Deciphered Date	2014/01/21

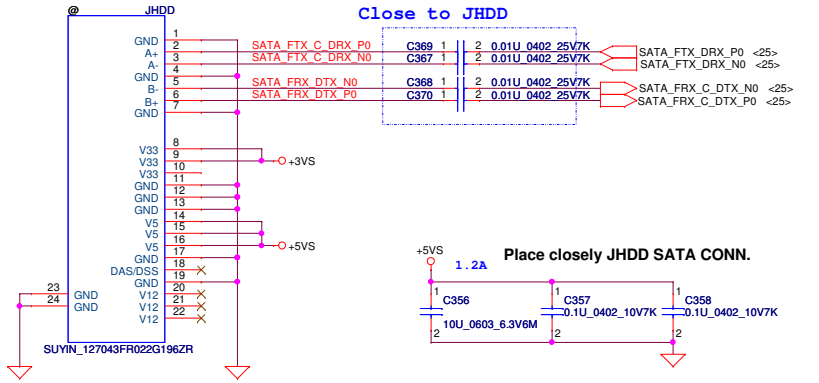
Compal Electronics, Inc.

Title: Hudson-M3-POWER/GND

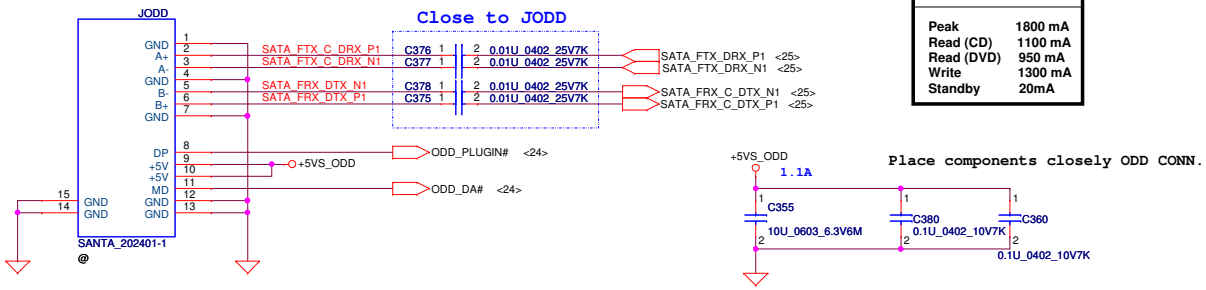
Size: Custom | Document Number: LA-9869P | Rev: 0.3

Date: Monday, February 04, 2013 | Sheet 27 of 50

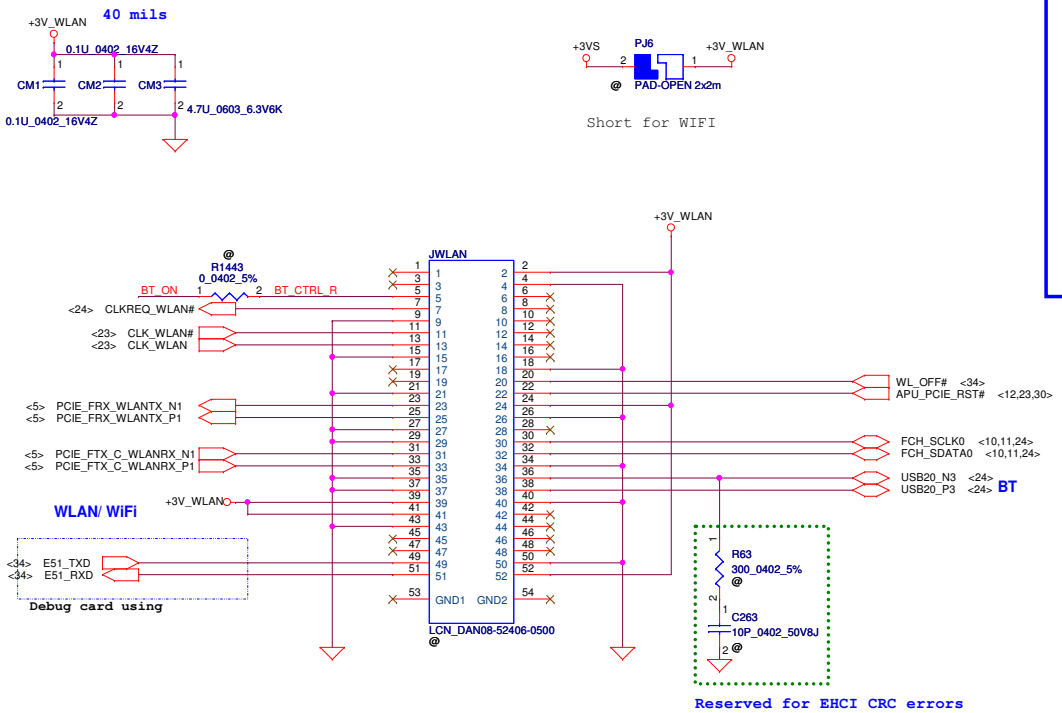
SATA HDD Conn.



SATA ODD Conn



Slot 1 Half PCIe Mini Card-WLAN



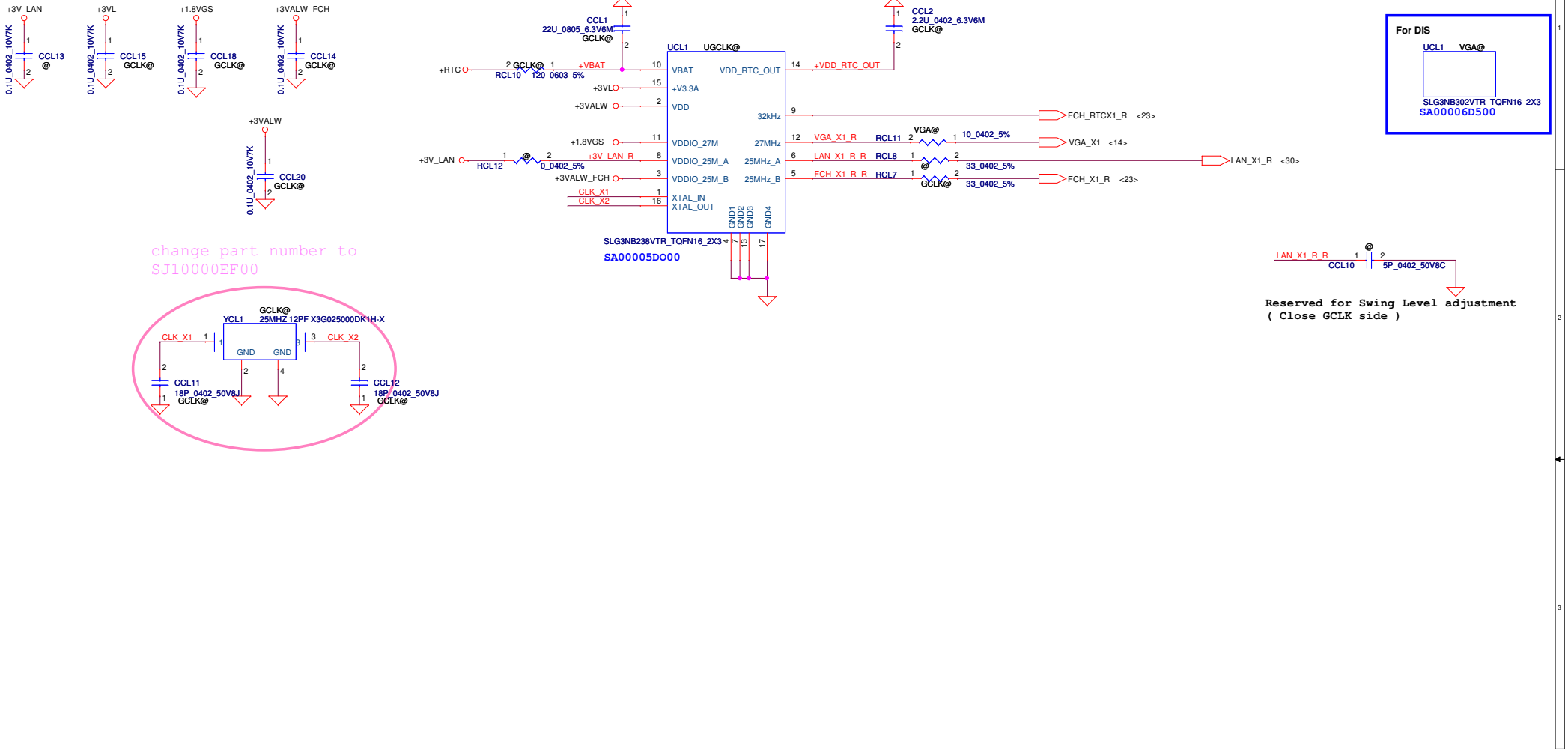
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.	
Title	SATA-HDD/ODD/USB
Size	Document Number: LA-9869P
Rev	0.3
Date:	Monday, February 04, 2013
Sheet	28 of 50

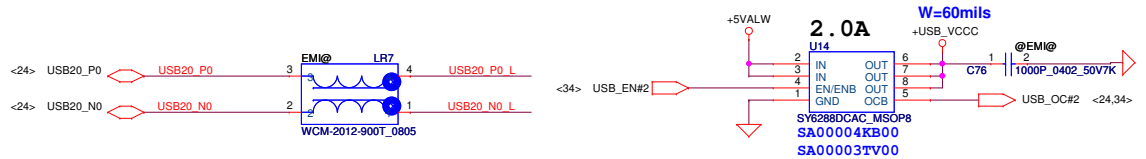
Green Clock Generator



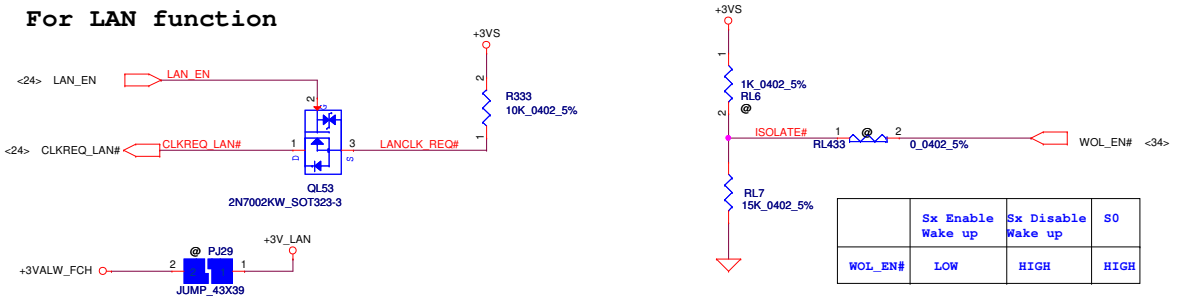
Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Title	PCIe-WLAN/GCLK		
Size	Document Number	LA-9869P	Rev 0.3
Date: Monday, February 04, 2013	Sheet 29 of 50		

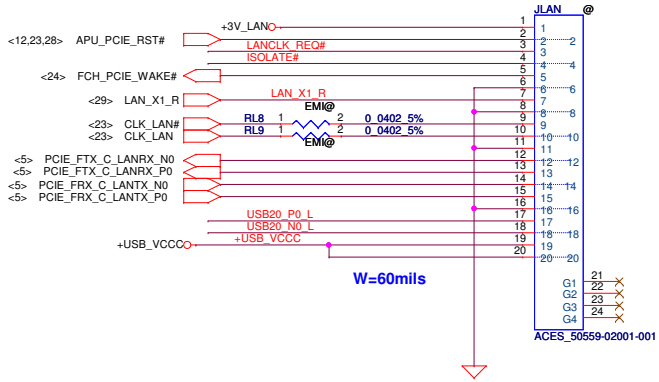
Left USB 2.0 x 1



For LAN function



	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

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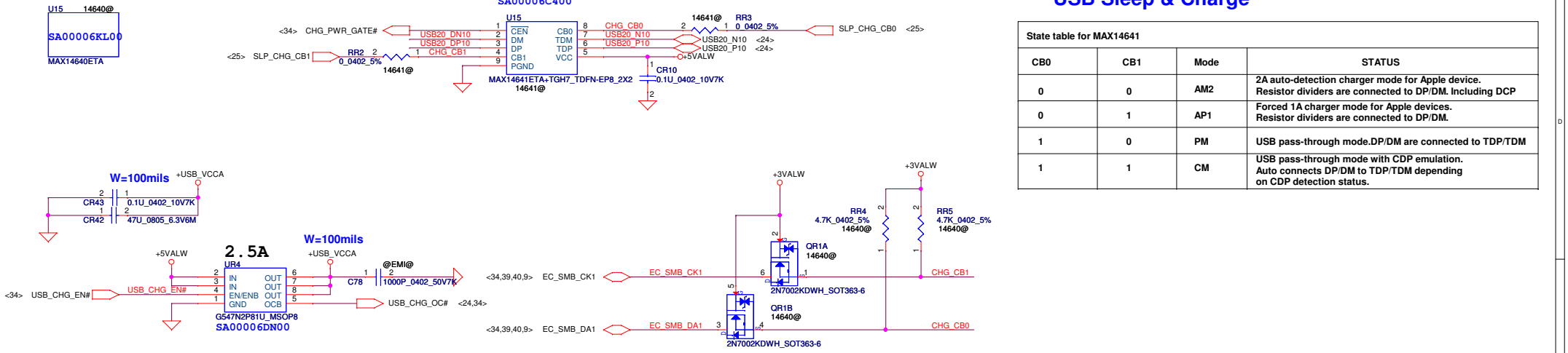
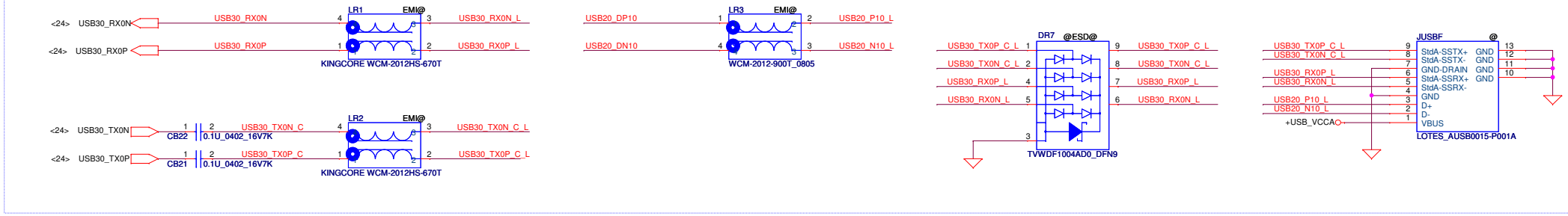
Compal Electronics, Inc.			
Title: PCIe-LAN-RTL8105E/8111F			
Size: Custom	Document Number: LA-9869P		Rev: 0.3
Date: Monday, February 04, 2013	Sheet 30 of 50		

USB Sleep & Charge

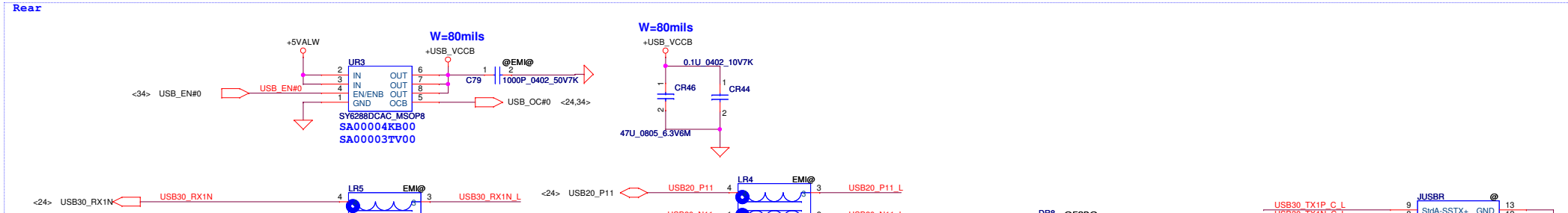
State table for MAX14641			
CB0	**CB1**	**Mode**	**STATUS**
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



Front with S&C



Rear



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Issued Date	2013/01/22	Deciphered Date	2014/01/21

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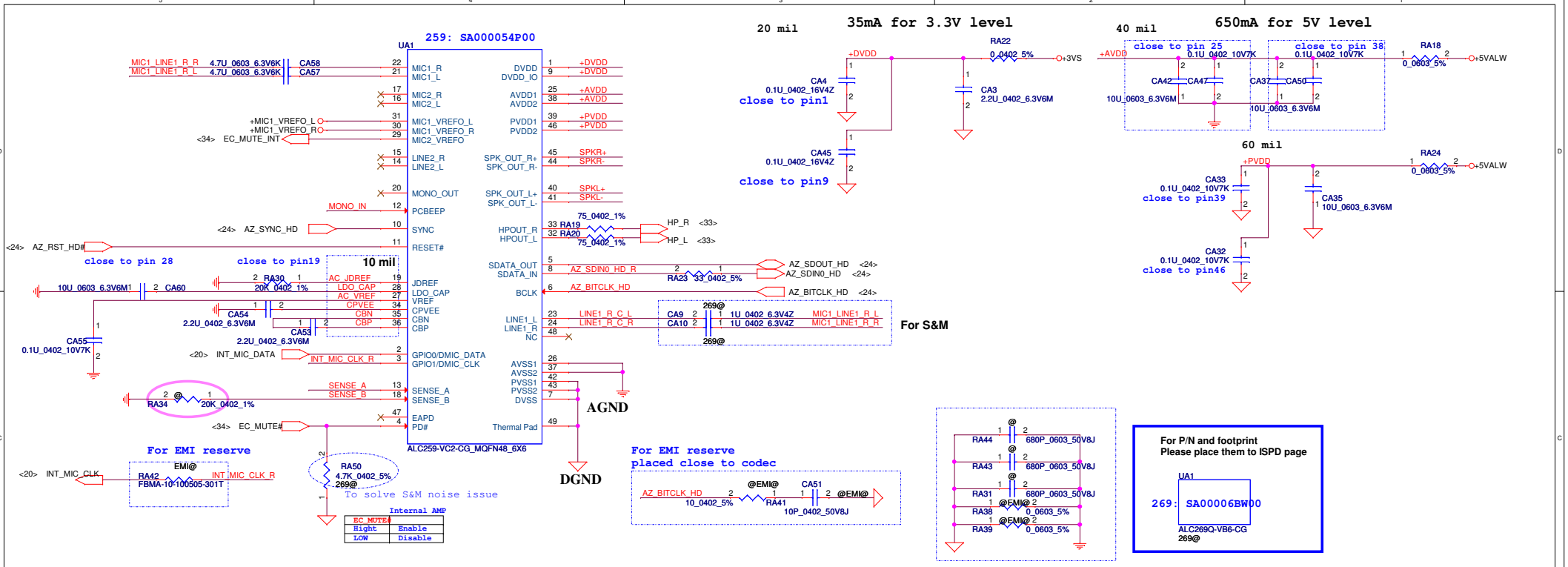
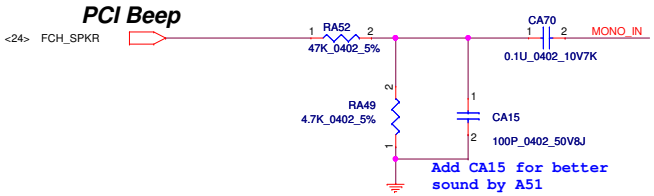
Title: USB3.0

Size: Custom | Document Number: LA-9869P | Rev: 0.3

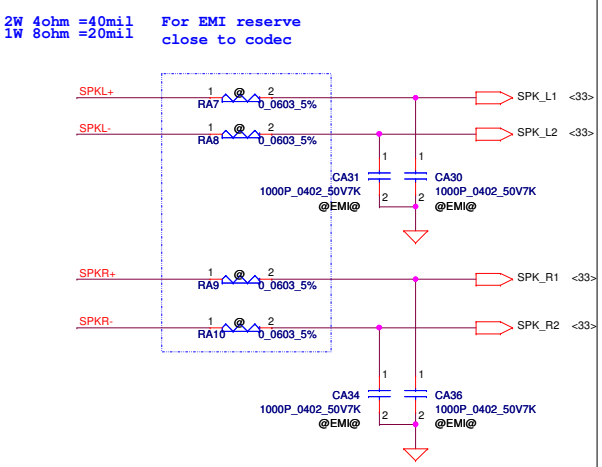
Date: Monday, February 04, 2013 | Sheet 31 of 50



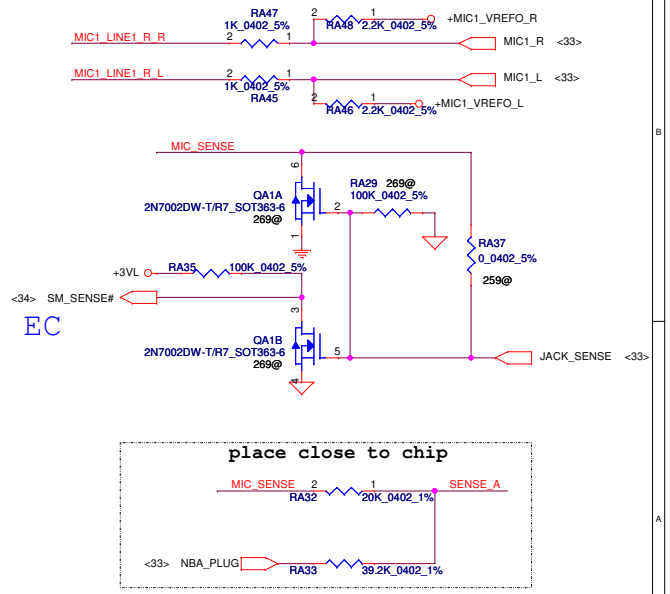
Beep sound



SPK



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

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Compal Electronics, Inc.

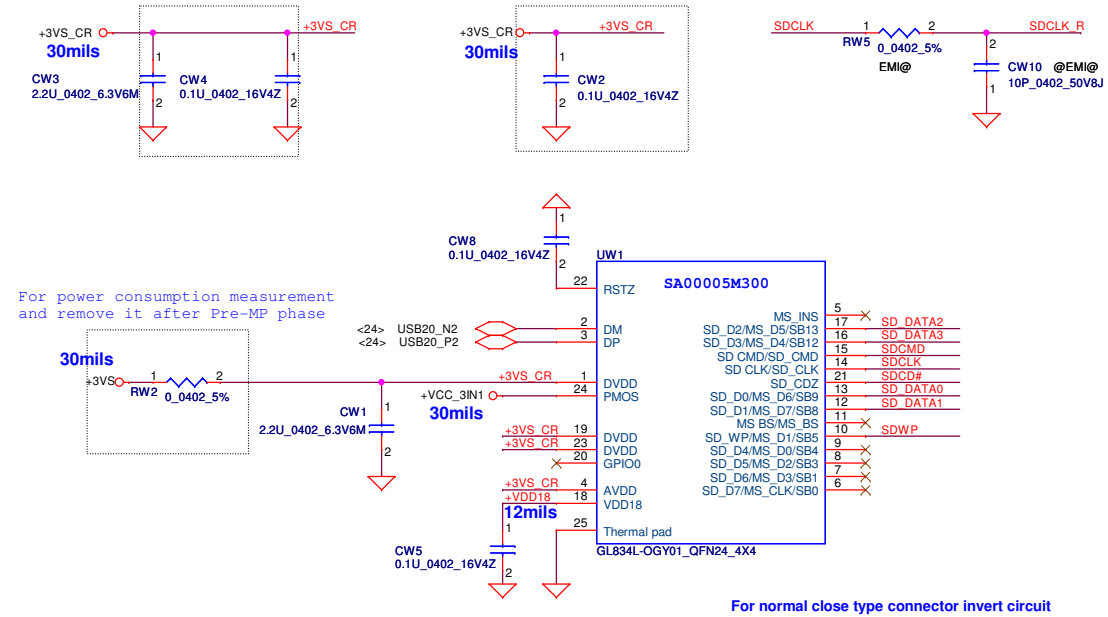
Title: Cover Sheet

Size: Custom	Document Number	Rev: 0.3
Date: Monday, February 04, 2013	Sheet 32 of 50	

Card reader

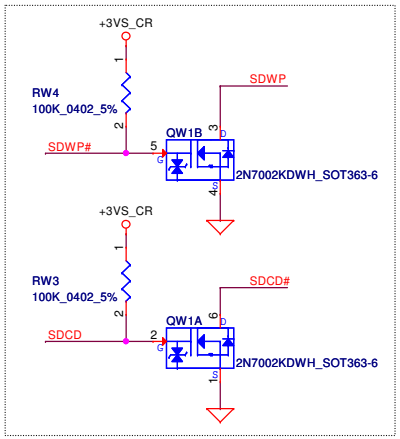
please close the pin4 of UW1

please close the pin19 of UW1



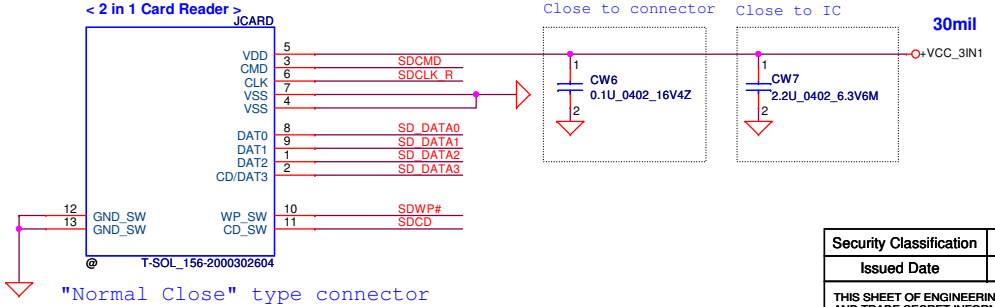
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

For normal close type connector invert circuit



	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

< 2 in 1 Card Reader >

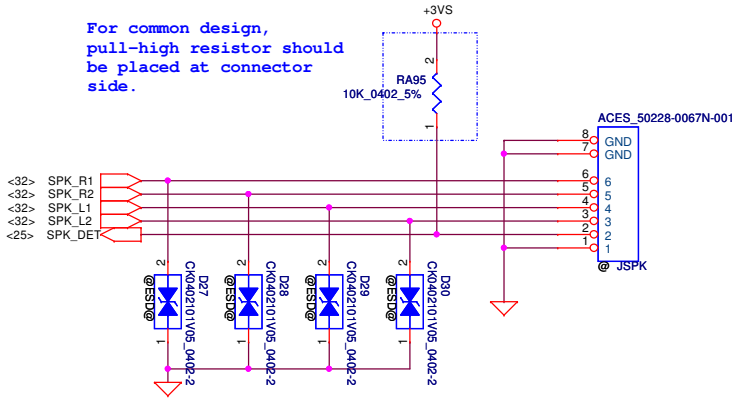


"Normal Close" type connector

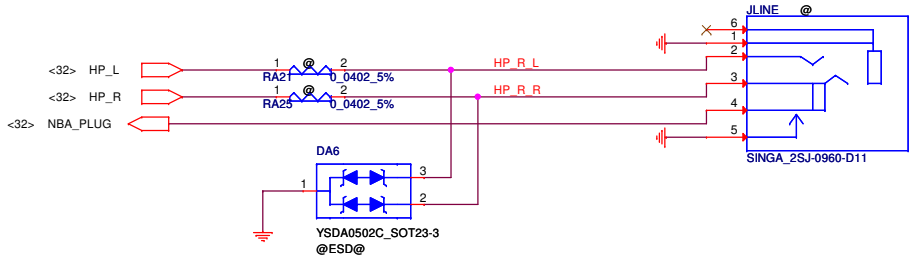
SPK CONN.

	Non-Harman detection	
SPK_DET0	0	ONKYO
	1	Non-Brand

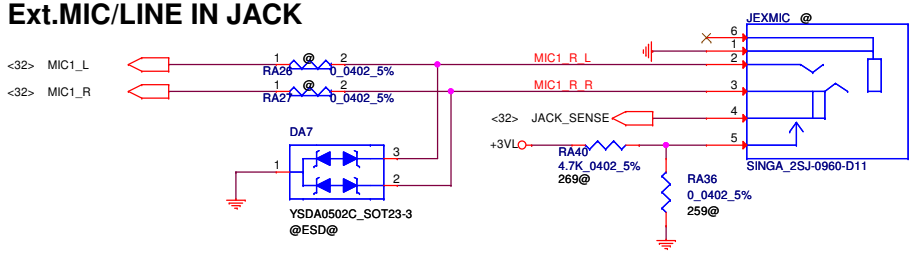
Please check SPK_DET pull high 10K to +3VS



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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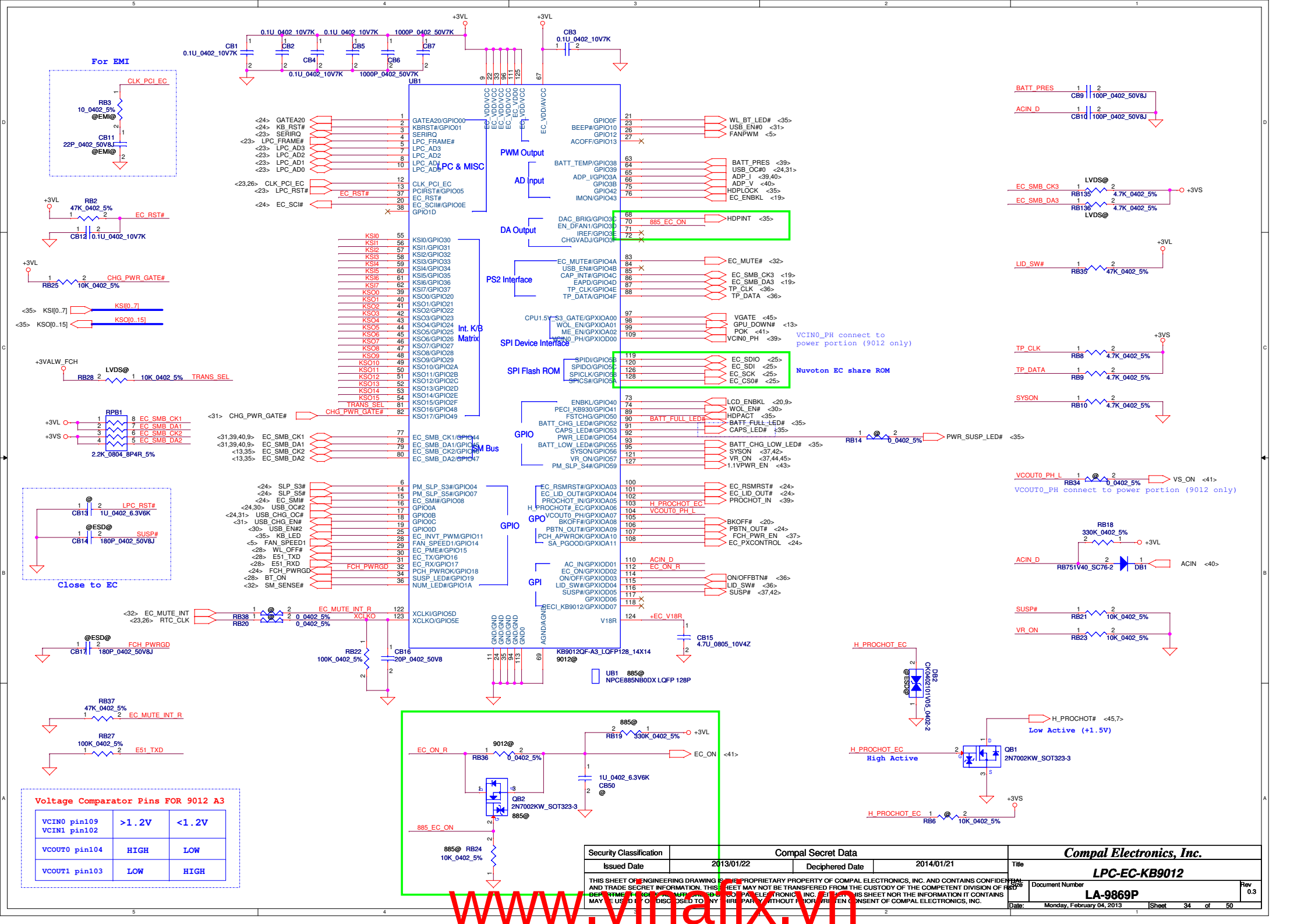
Compal Electronics, Inc.

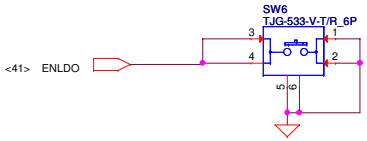
Title: CR & Audio Conn.

Size | Document Number: LA-9869P | Rev: 0.3

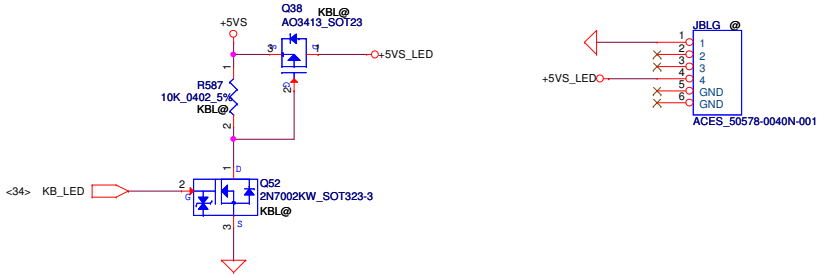
Date: Monday, February 04, 2013 | Sheet 33 of 50


For EMI
UB1
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Nuvoton EC share ROM
VCIN0_PH connect to power portion (9012 only)
VCOUT0_PH connect to power portion (9012 only)
Close to EC
Low Active (+1.5V)
High Active
Voltage Comparator Pins FOR 9012 A3
VCIN0 pin109
VCIN1 pin102
>1.2V
<1.2V
VCOUT0 pin104
HIGH
LOW
VCOUT1 pin103
LOW
HIGH
KB9012QF-A3_LQFP128_14X14
9012@
UB1 885@
NPCE885NB0DX LQFP 128P
Security Classification
Compal Secret Data
Issued Date
2013/01/22
Deciphered Date
2014/01/21
Compal Electronics, Inc.
Title
LPC-EC-KB9012
Size
Document Number
LA-9869P
Rev
0.3
Date:
Monday, February 04, 2013
Sheet
34
of
50
www.vinafix.vn

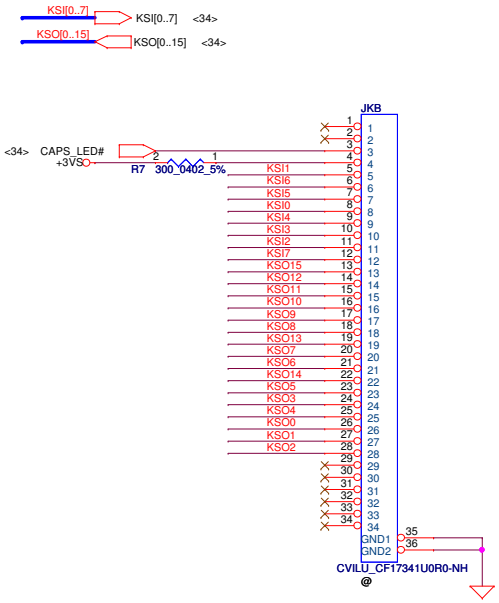
Battery Reset



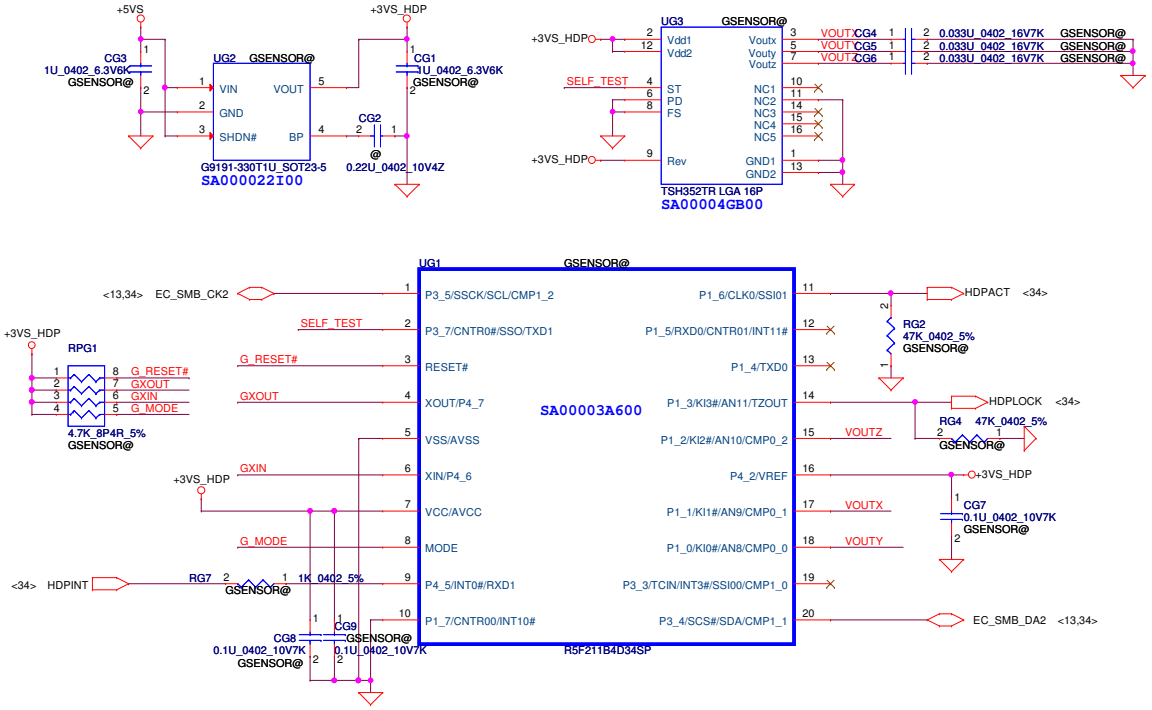
Keyboard LED



NEW KEYBOARD CONN.

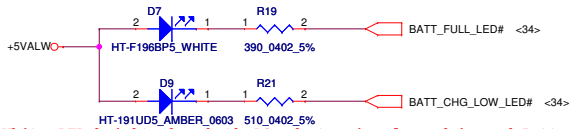


G-SENSOR



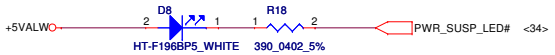
LED

BATT CHARGE(Blink) /FULL LED



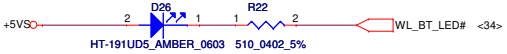
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED(Blink)



White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN LED



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Title: **Debug/KB**

Size: C | Document Number: **LA-9869P** | Rev: 0.3

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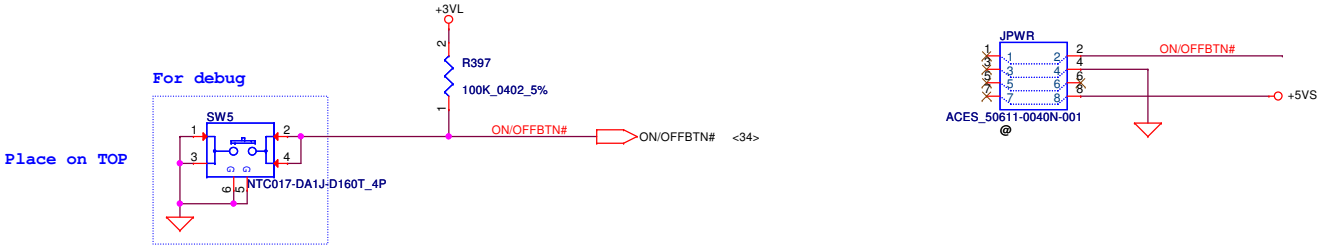
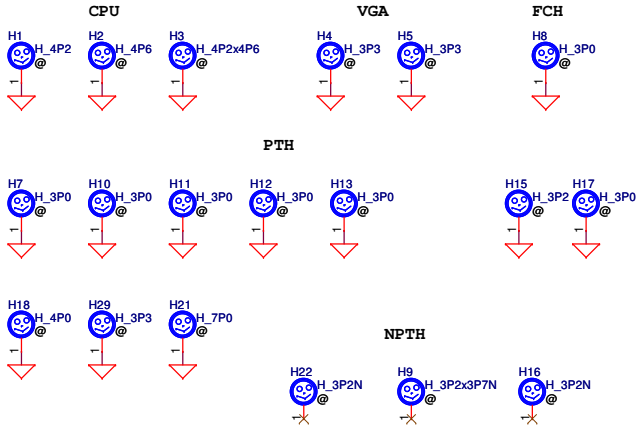
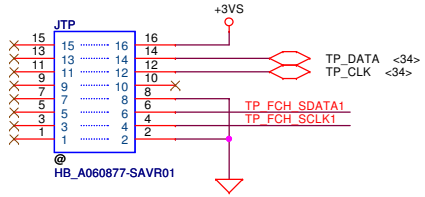
Conn.

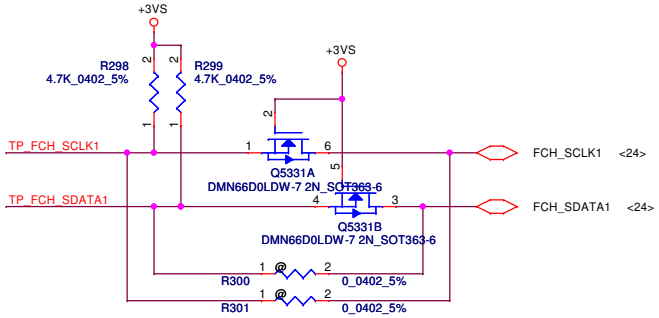


Screw Hole

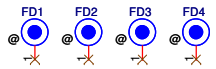


Touchpad Connector

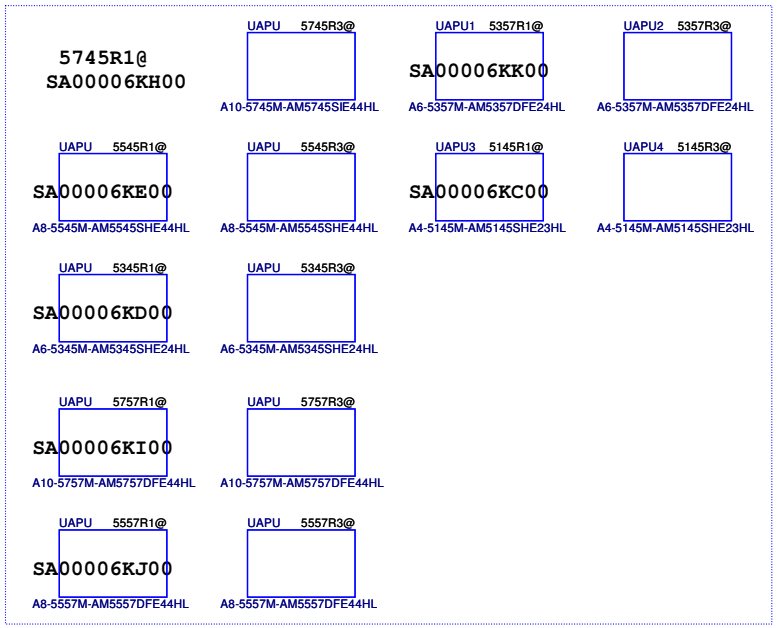


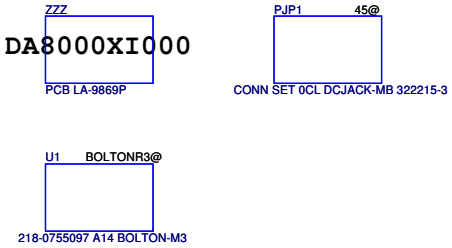


PCB Fedical Mark PAD

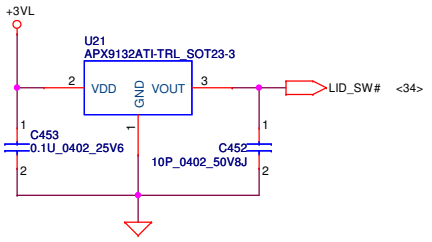


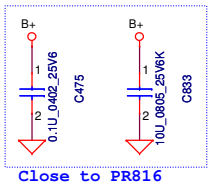
ISPD





Lid SW





Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Title	TP/HDD LED/Screw		
Size	Document Number		Rev
	LA-9869P		0.3
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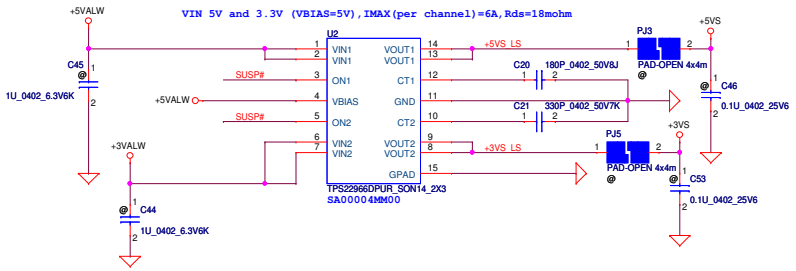
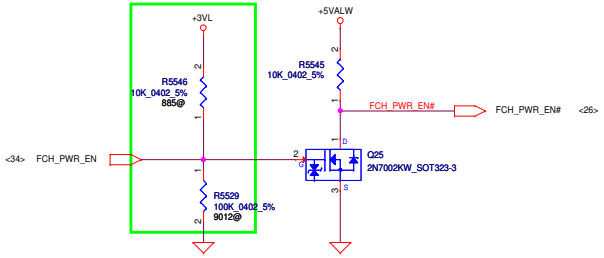
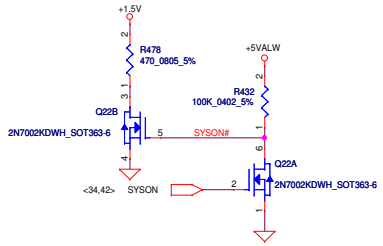
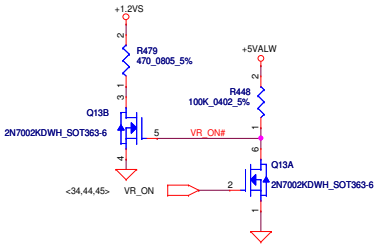
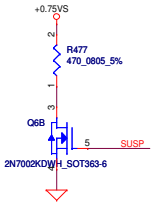
+5VALW TO +5VS
+3VALW TO +3VS
Load switch

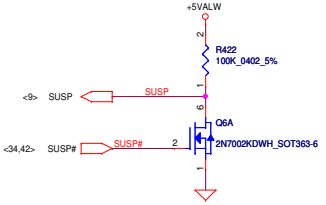




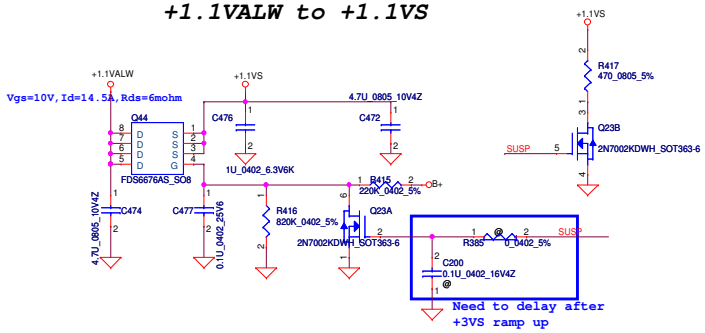




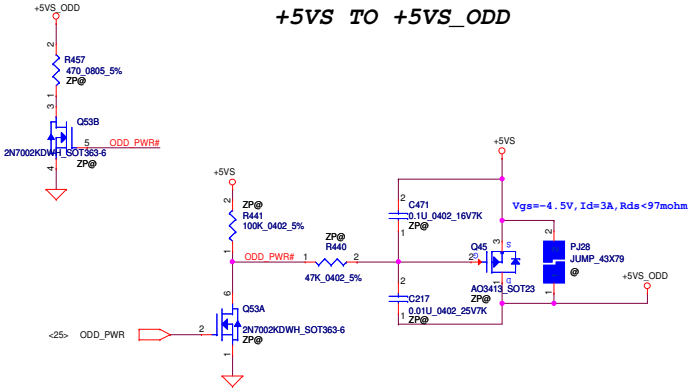




+1.1VALW to +1.1VS



+5VS TO +5VS_ODD



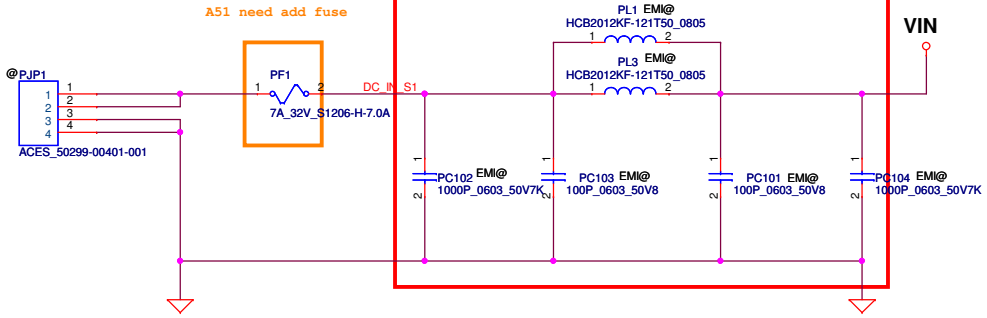
Security Classification	Compal Secret Data		
Issued Date	2013/01/22	Deciphered Date	2014/01/21

Compal Electronics, Inc.			
Title	DC-DC INTERFACE		
Size	Document Number	LA-9869P	Rev 0.3
Date: Monday, February 04, 2013	Sheet 37 of 50		

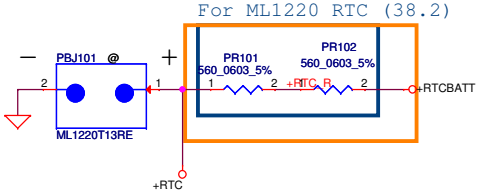
EMI Part (47.1)

Other component (37.1)

A51 need add fuse



For ML1220 RTC (38.2)



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

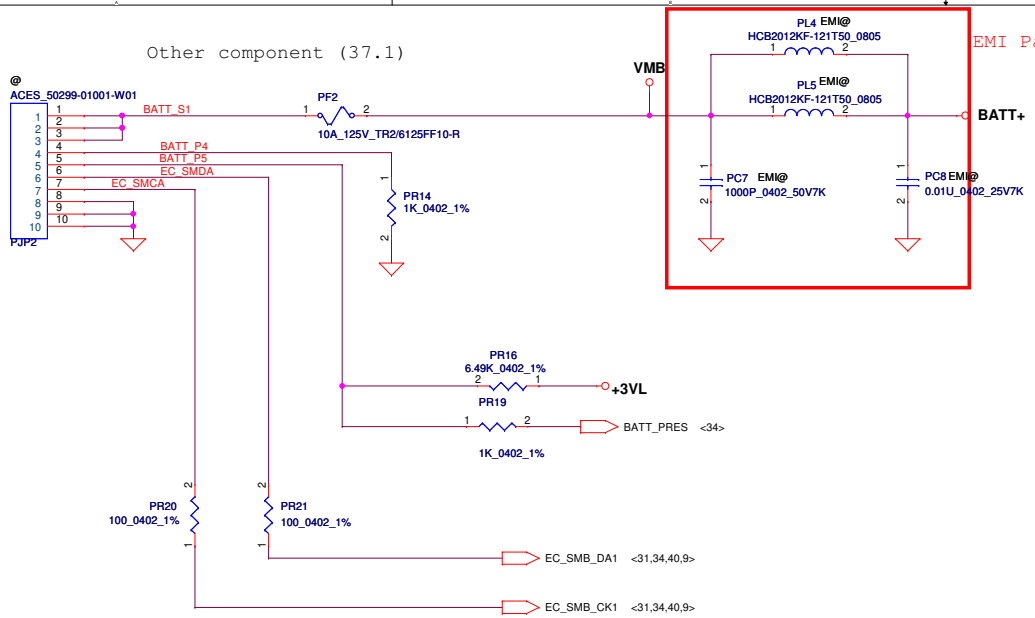
Title: DCIN/PRECHARGE

Size: Custom | Document Number: LA-9869P | Rev: 0.1

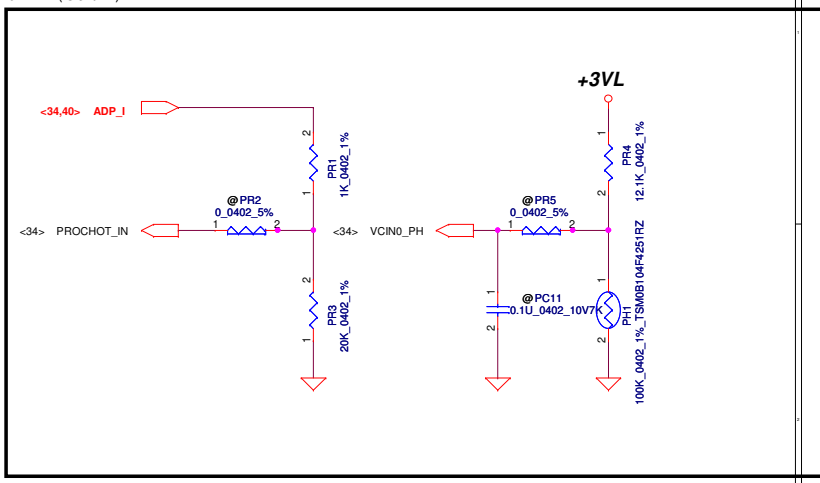
Date: | Sheet 38 of 49

Other component (37.1)

EMI Part (47.1)



OTP (39.7)



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: LA-9869P | Rev: 0.1

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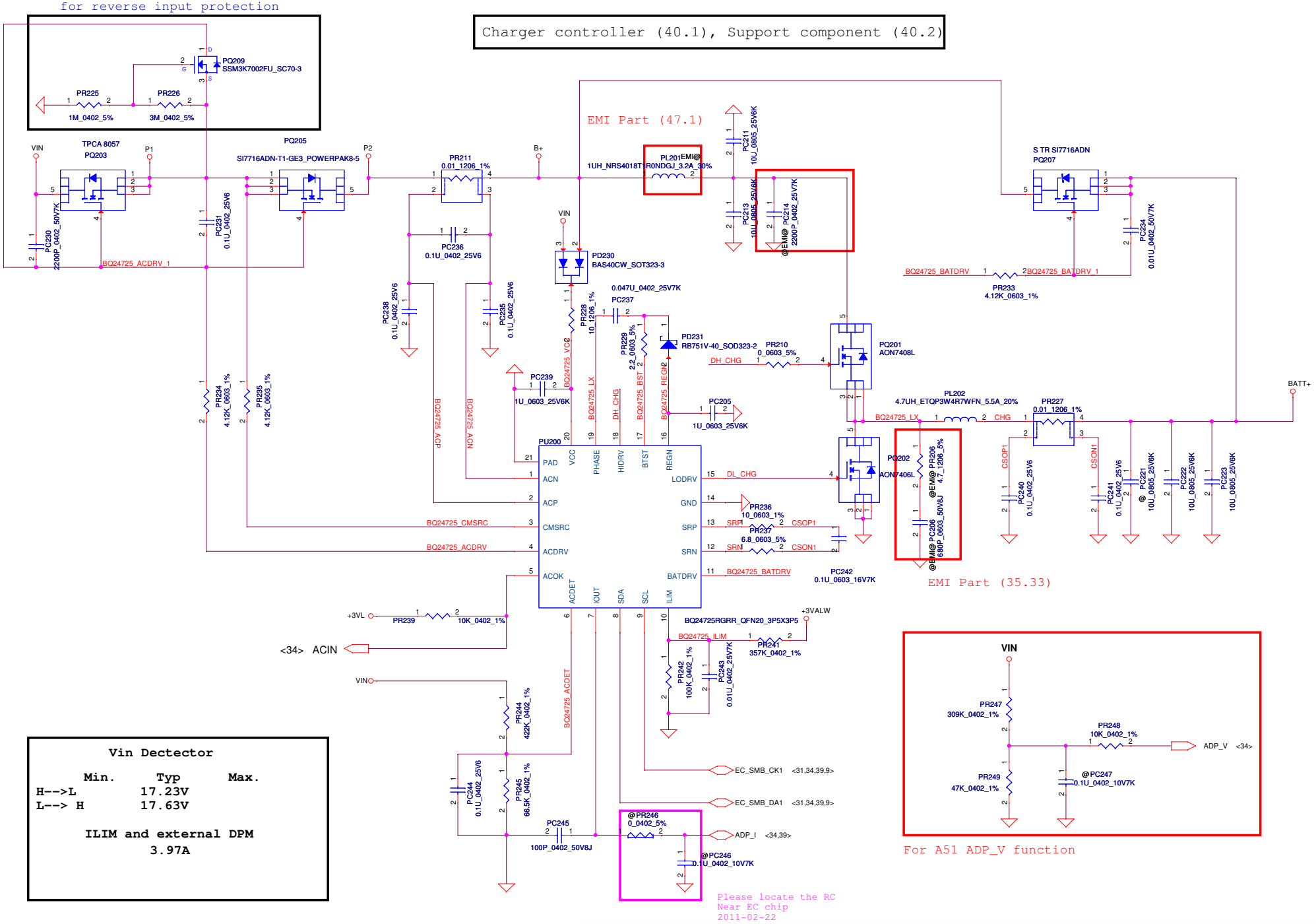
for reverse input protection

Charger controller (40.1), Support component (40.2)



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

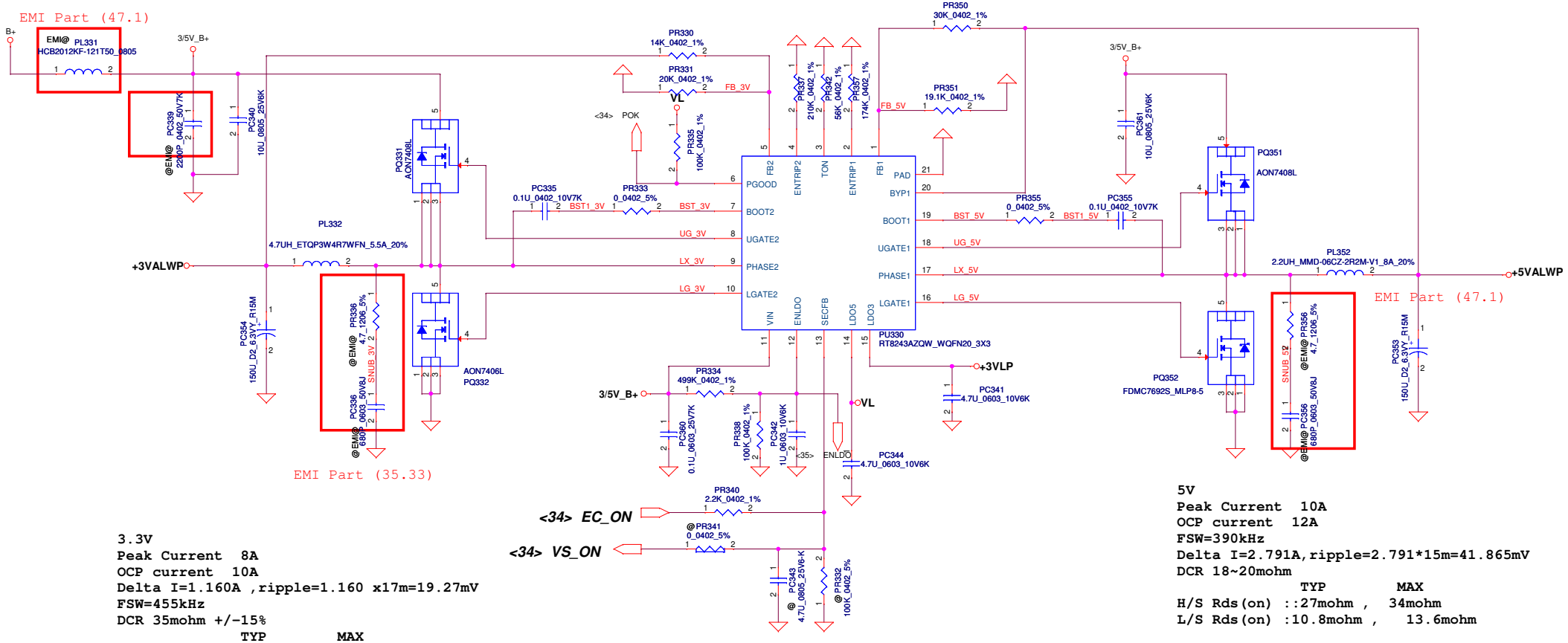
Title: CHARGER

Size: Custom | Document Number | Rev: 0.1

Date: | Sheet 40 of 49

3/5VALW controller (35.1), Support component (35.2)

5V_3.3V controller (35.1), Support component (35.2)



3.3V
Peak Current 8A
OCP current 10A
Delta I=1.160A ,ripple=1.160 x17m=19.27mV
FSW=455kHz
DCR 35mohm +/-15%

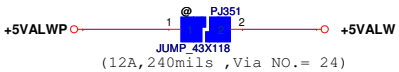
	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:19mohm ,	23.5mohm

5V
Peak Current 10A
OCP current 12A
FSW=390kHz
Delta I=2.791A,ripple=2.791*15m=41.865mV
DCR 18~20mohm

	TYP	MAX
H/S Rds(on)	::27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

(100mA,20mils ,Via NO.= 1)

(8A,160mils ,Via NO.= 16)



(12A,240mils ,Via NO.= 24)

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number | Rev: 0.1

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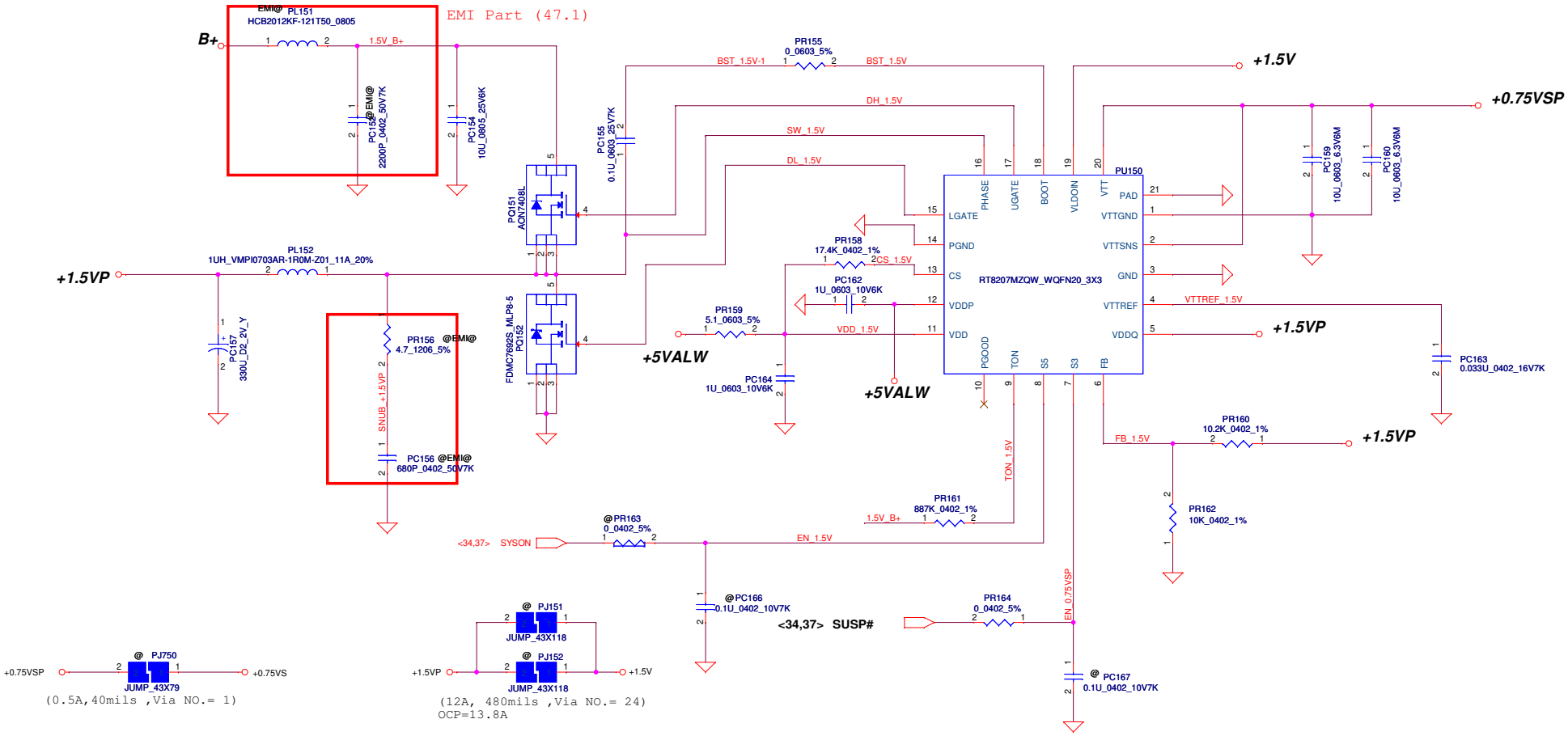
DDR controller (35.3), Support component (35.4)



1.5V
Peak Current 12A
OCP current 13.34A
FSW=300kHz
DCR 8.3 ~ 10mohm

	TYP	MAX
H/S Rds(on)	**:27mohm ,**	**34mohm**
L/S Rds(on)	**:10.8mohm ,**	**13.6mohm**

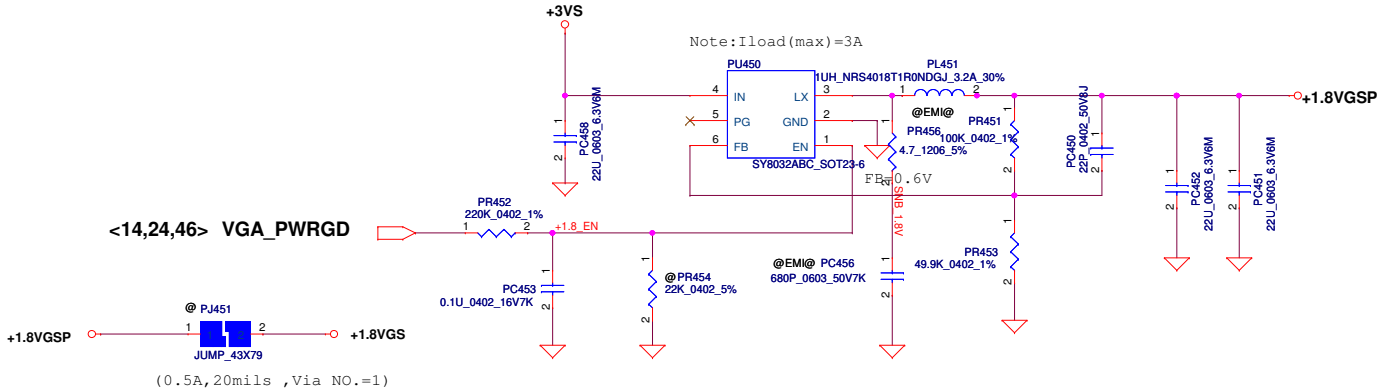
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.	
Title	1.5VP/0.75VSP/1.8VSP
Size: Custom	Document Number: LA-9869P
Rev: 0.1	
Date:	Sheet 42 of 49

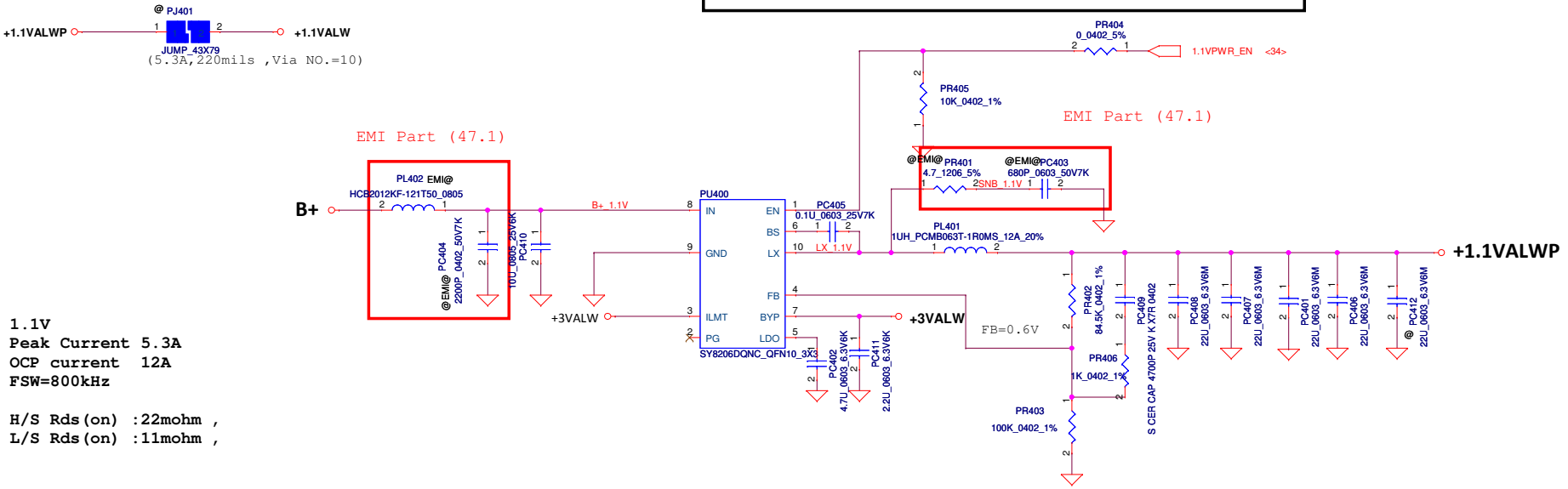
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 0.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

1.1V controller (35.27), Support component (35.28)



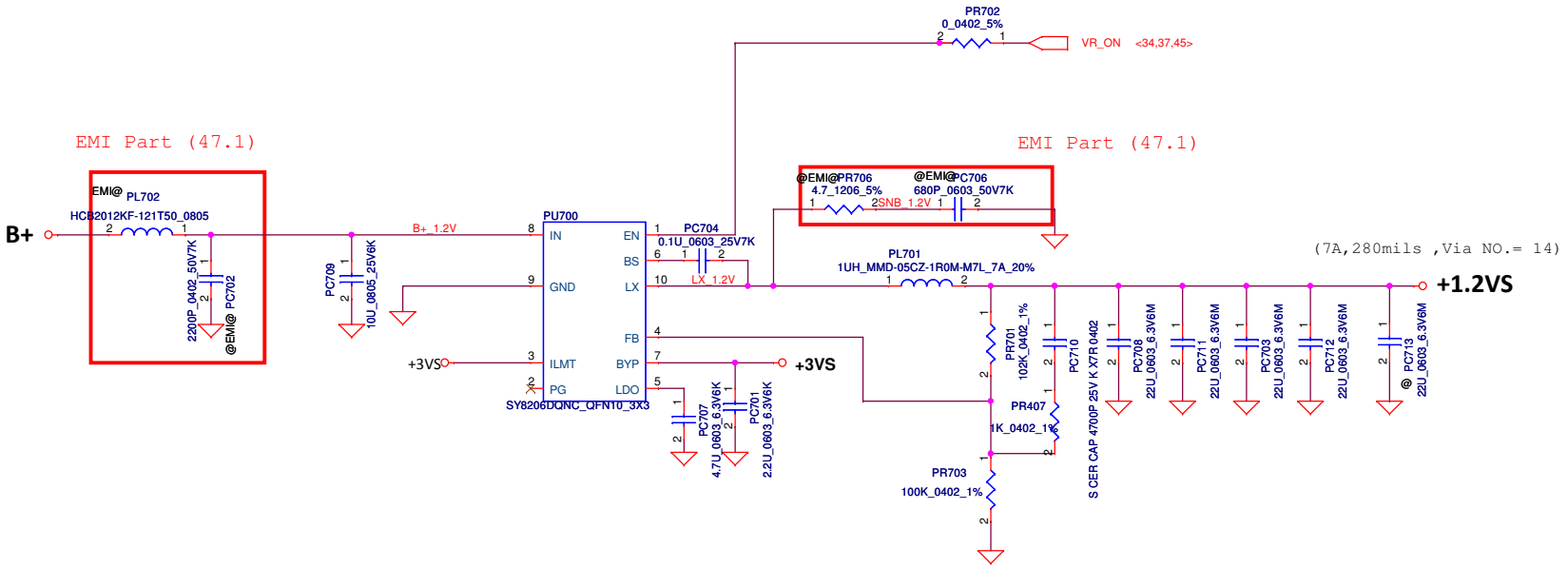
1.1V
Peak Current 5.3A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/06	Deciphered Date	2015/09/06
Title	+1.8VALWP		
Size: Custom	Document Number: LA-9869P		Rev: 0.1
Date: Monday, February 04, 2013	Sheet 43 of 49		

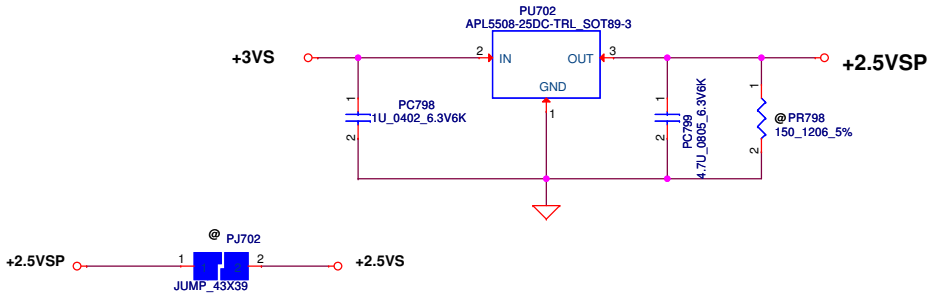
1.2V controller (35.7), Support component (35.8)



1.2V
Peak Current 7A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

2.5V controller (35.13), Support component (35.14)



Security Classification	Compal Secret Data		
Issued Date	2012/09/06	Deciphered Date	2015/09/06

Compal Electronics, Inc.

Title: +1.2VSP/+2.5VSP

Size	Document Number	Rev
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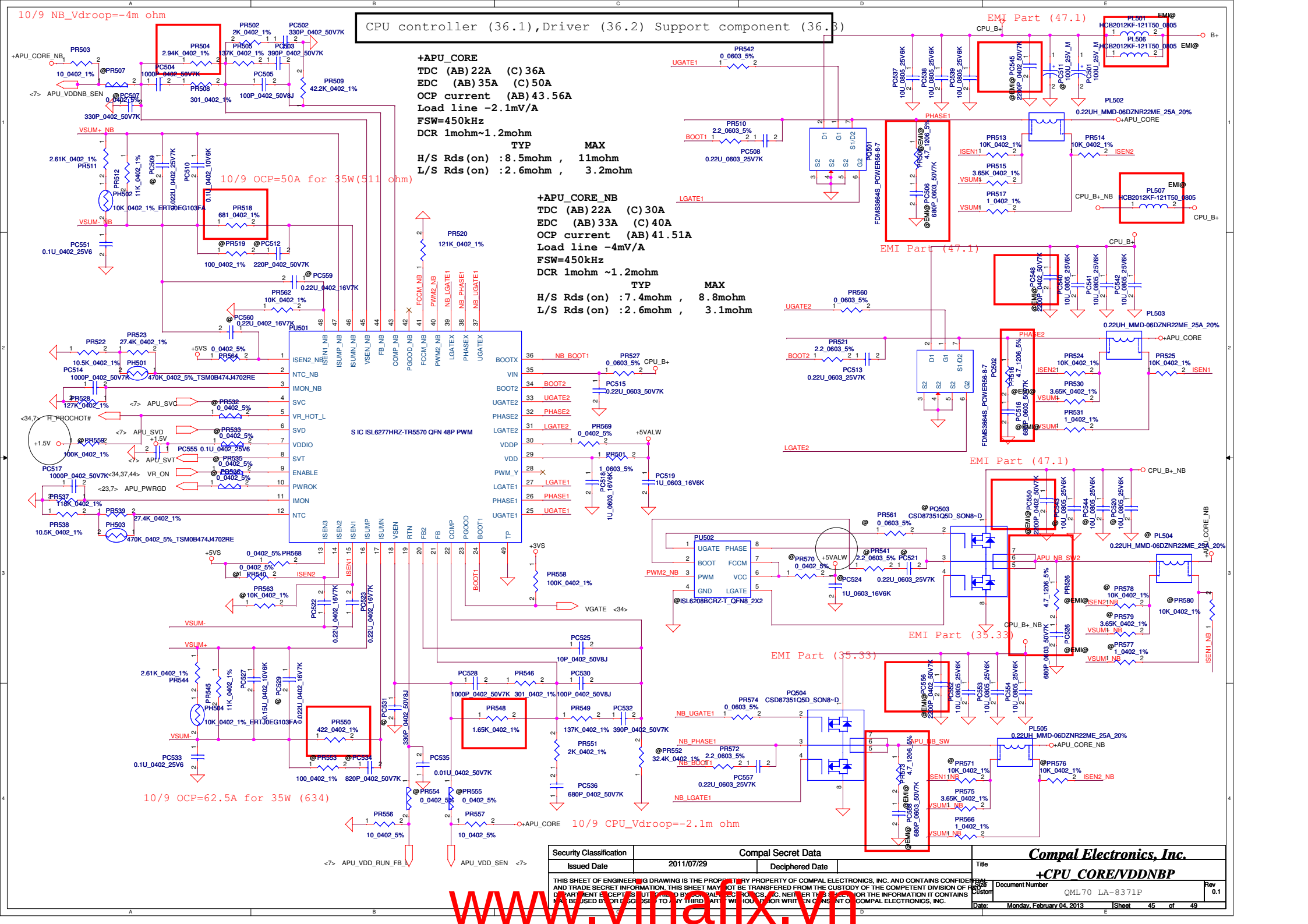
10/9 NB_Vdroop=-4m ohm
CPU controller (36.1),Driver (36.2) Support component (36.3)
+APU_CORE
TDC (AB)22A (C)36A
EDC (AB)35A (C)50A
OCP current (AB)43.56A
Load line -2.1mV/A
FSW=450kHz
DCR 1mohm~1.2mohm
TYP MAX
H/S Rds(on) :8.5mohm , 11mohm
L/S Rds(on) :2.6mohm , 3.2mohm
+APU_CORE_NB
TDC (AB)22A (C)30A
EDC (AB)33A (C)40A
OCP current (AB)41.51A
Load line -4mV/A
FSW=450kHz
DCR 1mohm ~1.2mohm
TYP MAX
H/S Rds(on) :7.4mohm , 8.8mohm
L/S Rds(on) :2.6mohm , 3.1mohm
10/9 OCP=50A for 35W(511 ohm)
10/9 OCP=62.5A for 35W (634)
10/9 CPU_Vdroop=-2.1m ohm
EMI Part (47.1)
EMI Part (35.33)
S IC ISL6277HRZ-TR5570 QFN 48P PWM
PU501
PU502
PQ503
PQ504
PL501
PL502
PL503
PL504
PL505
PL506
PL507
ISL6208BCRZ-T_QFN8_2X2
FDMS3664S_POWER56-8-7
CSD87351Q5D_SON8~D
APU_NB_SW
APU_NB_SW2
Security Classification
Compal Secret Data
Issued Date
2011/07/29
Deciphered Date
Compal Electronics, Inc.
+CPU_CORE/VDDNBP
Document Number
QML70 LA-8371P
Rev
0.1
Date: Monday, February 04, 2013
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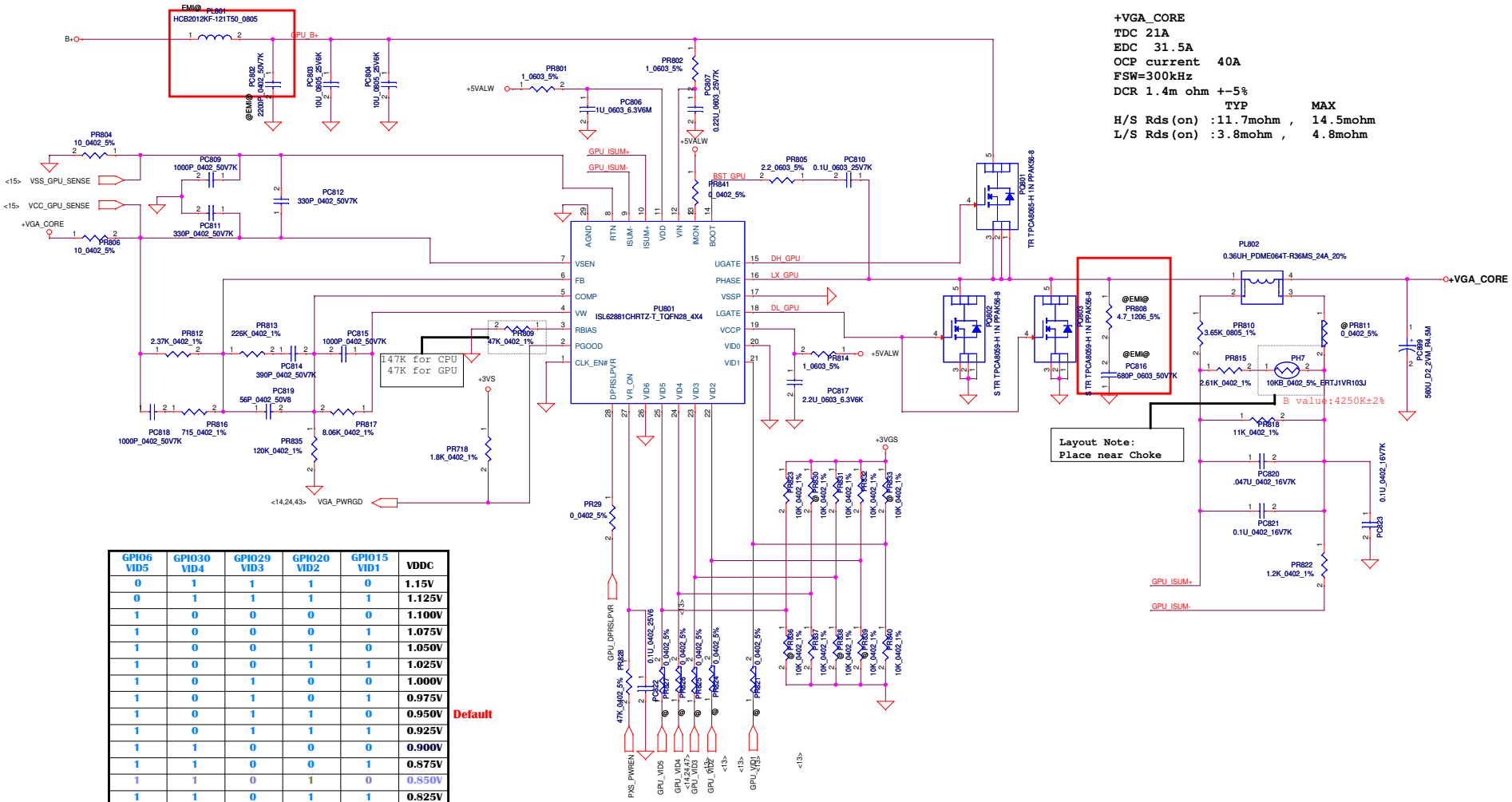
VGA controller (43.1),Driver (43.2) Support component (43.3)

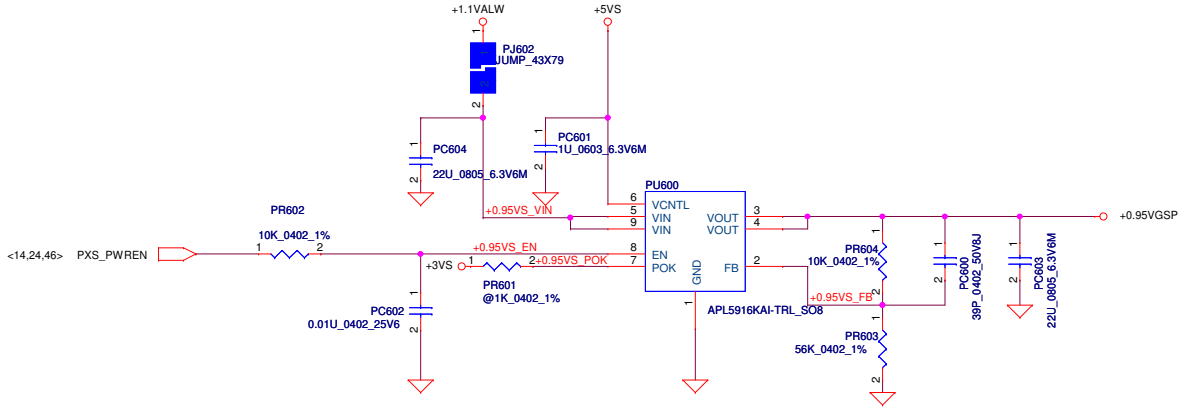
EMI Part (47.1)



GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC	
0	1	1	1	0	1.15V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	Default
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/10	Deciphered Date	2013/07/10
Title	+VPU_COREP		
Size C	Document Number LA-9869P		Rev 0.1
Date: Monday, February 04, 2013	Sheet 46 of 49		

0.95V controller (35.11), Support component (35.12)



(4A,160mils ,Via NO.= 4)

0.95V
Peak Current 4A
OCP current 16A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: +1.5VPCIE/0.935V

Size | Document Number: LA-9869P | Rev: 0.1

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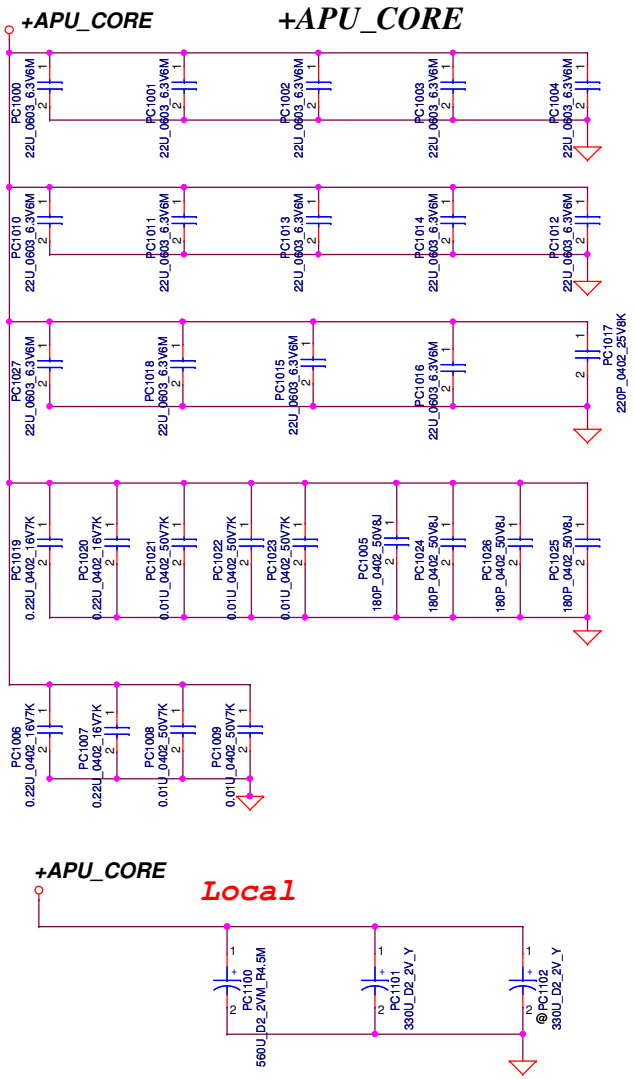
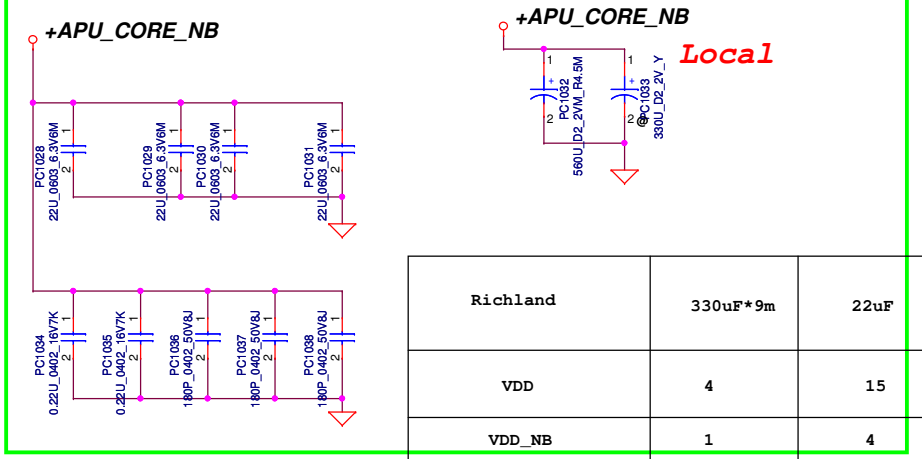
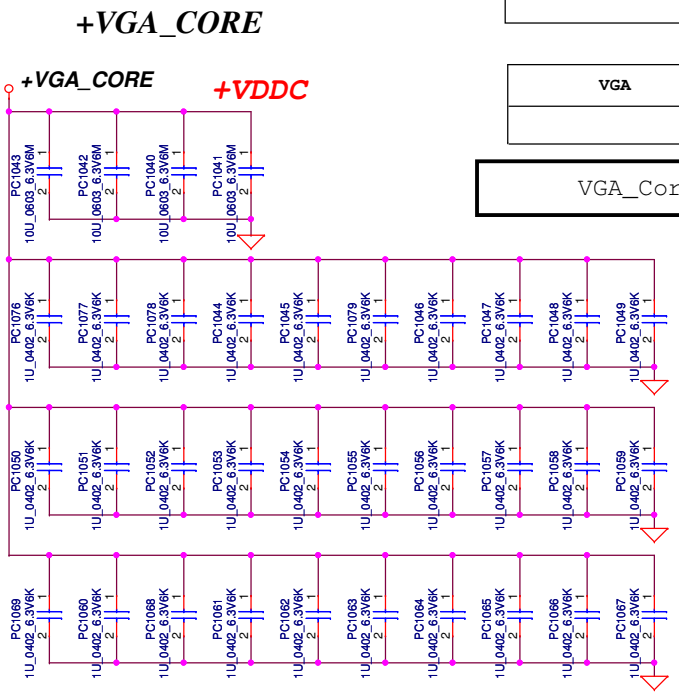
CPU_Core output CAP (Including MLCC) 36.4



GFX output CAP (Including MLCC) 36.5



Richland	330uF*9m	22uF	0.01u	0.22uF	180P
VDD	4	15	5	4	4
VDD_NB	1	4		2	3



VGA	560u x1	10u x 4	1u x30

VGA_Core output CAP (Including MLCC 43.9)

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	LA-8712P	0.1

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Item Reason for change PG# Modify List Date Phase

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT–2012/11/28	P39-PWR-BATTERY CONN / OTP	change PF2 vandor for cost down plane	PWR
2	EVT–2012/11/28	P41-PWR-+3VALW/5VALW	change PR337 235K to 210K & PR5357 156k to 174k	PWR
3	EVT–2012/11/28	P41-PWR-+3VALW/5VALW	Delate PC351 add PC353 150u D2 cap	PWR
4	EVT–2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PC157 220u H=4.5mm to 330u D2 cap H=2mm	PWR
5	EVT–2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PR158 16.2K to 17.4K	PWR
6	EVT–2012/11/28	P50-PWR-CPU_CORE	change the PC1101 560u to 330u	PWR

HW PIR (Product Improve Record)

VDKTE LA-9869P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/12/25

Item	Page	Date	Request	Solution
1)	21	2012/12/04a	For CRT undershoot issue	Add R66 & R67 for CRT issue.
2)	14	2012/12/04a	For VGA_CORE display	unomunt CR103.
3)	22	2012/12/13a	For EMI request	Change L8/L9/L10/L11 part number for EMI requesrt.
4)	34	2012/12/13a	For change EC PIN	Change 1.1VPWR_EN from pin 71 to pin 127 and USB_EN#0 from pin84 to pin 23.
5)	19	2012/12/14a	For LVDS translator	Delete all of RTD2132S components.
6)	31	2012/12/14a	For S&C port wake	Add CHG_PWR_GATE# on U15 pin 1 and connect to EC pin82.
7)	24	2012/12/17a	For leakage with PXS_PWREN	Change Power rail from +3VALW_FCH to +3VALW on R216 pin1
8)	07	2012/12/22a	For leakge	Delete R47, D18.
9)	24	2012/12/22a	For NV suggestion	Add R283 & Q30.
10)	34	2012/12/25a	For S&C port wake	Add RB25.

Compal Electronics, Inc.

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