VDKTE

Rosetta 10ADT/10ADTG

LA-9869P REV 1.0 Schematic

AMD APU RICHLAND FP2 / FCH BOLTON-M3

2013-03-20 Rev 1.0

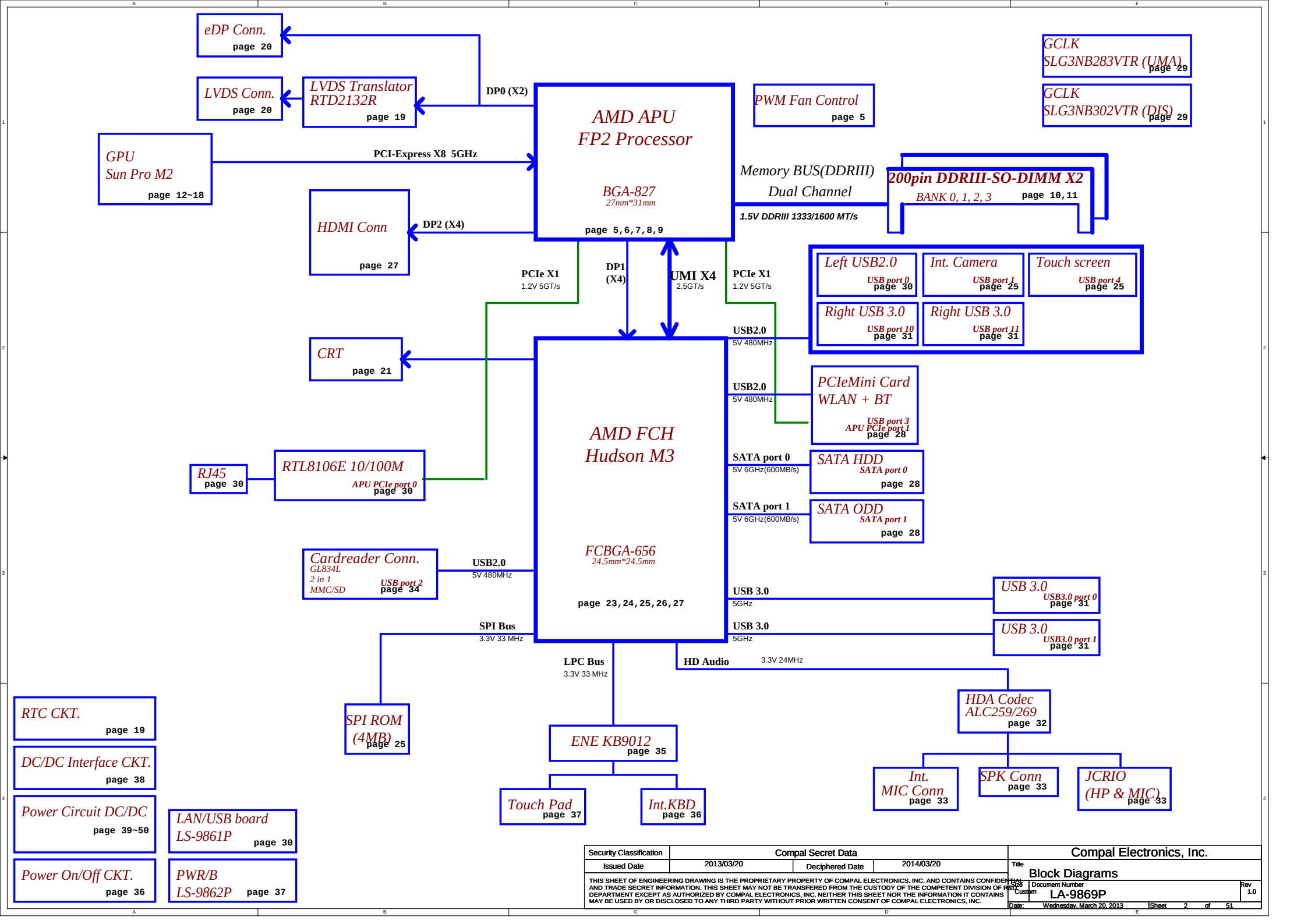
Security Classification	Compal Secret Data		
Issued Date	2013/03/12	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ***Cover Page***

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 1 of 51



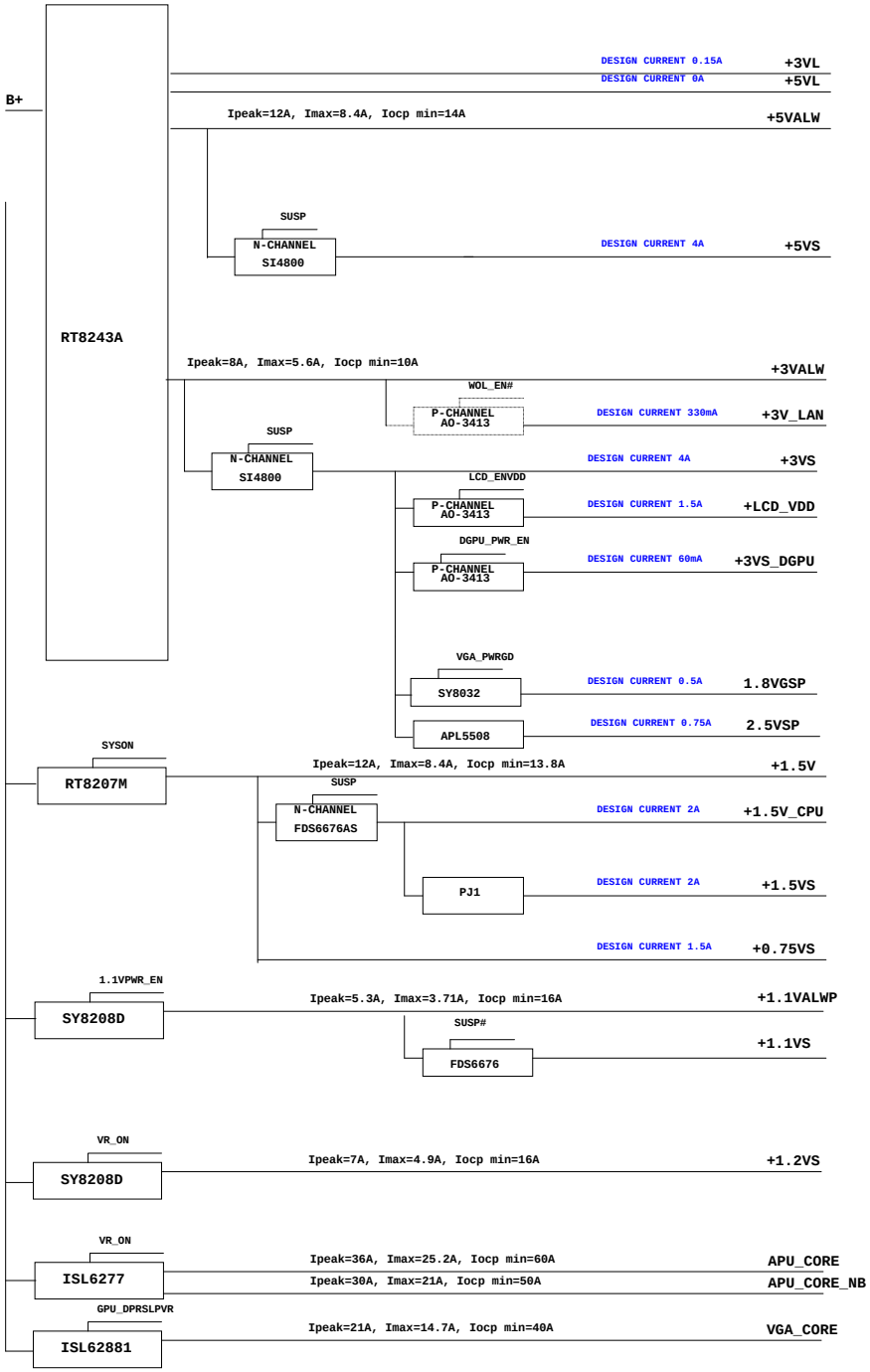
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 2 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.			
Title: Power Tree			
Size	Document Number: LA-9869P		Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 3 of 51		

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +1.1VALW
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	APU		FCH		GPU	
description			Bolton			
explain	R1	R3	R1	R3	R1	R3
BTO			BOLTONR1@	HUDM3R3@		

Function	3D sensor	KB LED	Clock		UMA/DIS	
description		K			1G	U
explain	G-sensor	KB LED	Green Clock	No Green Clock	DIS	UMA
BTO	GSENSOR@	KBL@	GCLK@	NOGCLK@	VGA@	UMA@

Function	Panel			
description	S	D		
explain	LVDS	eDP		
BTO	LVDS@	IEDP@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	VGA Thermal	82H	1000 0010 b

EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date 2014/03/20	Title: Notes List
Size: Custom	Document Number: LA-9869P		Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 4 of 51		

PCIE_GTX_C_ARX_P[0..3]

PCIE_GTX_C_ARX_N[0..3]

PCIE_ATX_C_GRX_P[0..3]

PCIE_ATX_C_GRX_N[0..3]

UAPUA

PCIE_GTX_C_ARX_P0	AP1	P_GFX_RXP[0]	P_GFX_TXP[0]	AN1	PCIE_ATX_GRX_P0	C1	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_P0
PCIE_GTX_C_ARX_N0	AP2	P_GFX_RXN[0]	P_GFX_TXN[0]	AN2	PCIE_ATX_GRX_N0	C15	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_N0
PCIE_GTX_C_ARX_P1	AM1	P_GFX_RXP[1]	P_GFX_TXP[1]	AM4	PCIE_ATX_GRX_P1	C17	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_P1
PCIE_GTX_C_ARX_N1	AM2	P_GFX_RXN[1]	P_GFX_TXN[1]	AM3	PCIE_ATX_GRX_N1	C11	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_N1
PCIE_GTX_C_ARX_P2	AK3	P_GFX_RXP[2]	P_GFX_TXP[2]	AK2	PCIE_ATX_GRX_P2	C7	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_P2
PCIE_GTX_C_ARX_N2	AK4	P_GFX_RXN[2]	P_GFX_TXN[2]	AK1	PCIE_ATX_GRX_N2	C14	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_N2
PCIE_GTX_C_ARX_P3	AJ1	P_GFX_RXP[3]	P_GFX_TXP[3]	AH1	PCIE_ATX_GRX_P3	C13	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_P3
PCIE_GTX_C_ARX_N3	AJ2	P_GFX_RXN[3]	P_GFX_TXN[3]	AH2	PCIE_ATX_GRX_N3	C8	1	2	VGA@	0.1U_0402_16V7K	PCIE_ATX_C_GRX_N3
	AH4	P_GFX_RXP[4]	P_GFX_TXP[4]	AF3							
	AH3	P_GFX_RXN[4]	P_GFX_TXN[4]	AF4							
	AF2	P_GFX_RXP[5]	P_GFX_TXP[5]	AE1							
	AF1	P_GFX_RXN[5]	P_GFX_TXN[5]	AE2							
	AD1	P_GFX_RXP[6]	P_GFX_TXP[6]	AD4							
	AD2	P_GFX_RXN[6]	P_GFX_TXN[6]	AD3							
	AB3	P_GFX_RXP[7]	P_GFX_TXP[7]	AB2							
	AB4	P_GFX_RXN[7]	P_GFX_TXN[7]	AB1							
	AA1	P_GFX_RXP[8]	P_GFX_TXP[8]	Y1							
	AA2	P_GFX_RXN[8]	P_GFX_TXN[8]	Y2							
	Y4	P_GFX_RXP[9]	P_GFX_TXP[9]	V3							
	Y3	P_GFX_RXN[9]	P_GFX_TXN[9]	V4							
	V2	P_GFX_RXP[10]	P_GFX_TXP[10]	U1							
	V1	P_GFX_RXN[10]	P_GFX_TXN[10]	U2							
	T1	P_GFX_RXP[11]	P_GFX_TXP[11]	T4							
	T2	P_GFX_RXN[11]	P_GFX_TXN[11]	T3							
	P3	P_GFX_RXP[12]	P_GFX_TXP[12]	P2							
	P4	P_GFX_RXN[12]	P_GFX_TXN[12]	P1							
	N1	P_GFX_RXP[13]	P_GFX_TXP[13]	M1							
	N2	P_GFX_RXN[13]	P_GFX_TXN[13]	M2							
	M4	P_GFX_RXP[14]	P_GFX_TXP[14]	K3							
	M3	P_GFX_RXN[14]	P_GFX_TXN[14]	K4							
	K2	P_GFX_RXP[15]	P_GFX_TXP[15]	J1							
	K1	P_GFX_RXN[15]	P_GFX_TXN[15]	J2							

GRAPHICS

LAN
WLAN

PCIE_FRX_C_LANTX_P0	AH5	P_GPP_RXP[0]	P_GPP_TXP[0]	AG7	PCIE_FTX_LANRX_P0	C50	1	2	0.1U_0402_16V7K	PCIE_FTX_C_LANRX_P0
PCIE_FRX_C_LANTX_N0	AH6	P_GPP_RXN[0]	P_GPP_TXN[0]	AG8	PCIE_FTX_LANRX_N0	C55	1	2	0.1U_0402_16V7K	PCIE_FTX_C_LANRX_N0
PCIE_FRX_WLANTX_P1	AG5	P_GPP_RXP[1]	P_GPP_TXP[1]	AE7	PCIE_FTX_WLANRX_P1	C51	1	2	0.1U_0402_16V7K	PCIE_FTX_C_WLANRX_P1
PCIE_FRX_WLANTX_N1	AG6	P_GPP_RXN[1]	P_GPP_TXN[1]	AE8	PCIE_FTX_WLANRX_N1	C54	1	2	0.1U_0402_16V7K	PCIE_FTX_C_WLANRX_N1
	AE6	P_GPP_RXP[2]	P_GPP_TXP[2]	AD7						
	AE5	P_GPP_RXN[2]	P_GPP_TXN[2]	AD8						
	AD6	P_GPP_RXP[3]	P_GPP_TXP[3]	AB6						
	AD5	P_GPP_RXN[3]	P_GPP_TXN[3]	AB5						

GPP

LAN
WLAN

UMI_MTX_C_FRX_P0	AM10	P_UMI_RXP[0]	P_UMI_TXP[0]	AN6	UMI_FTX_MRX_P0	C59	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0
UMI_MTX_C_FRX_N0	AN10	P_UMI_RXN[0]	P_UMI_TXN[0]	AM6	UMI_FTX_MRX_N0	C60	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_N0
UMI_MTX_C_FRX_P1	AN8	P_UMI_RXP[1]	P_UMI_TXP[1]	AP6	UMI_FTX_MRX_P1	C61	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_P1
UMI_MTX_C_FRX_N1	AM8	P_UMI_RXN[1]	P_UMI_TXN[1]	AR6	UMI_FTX_MRX_N1	C62	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_N1
UMI_MTX_C_FRX_P2	AP8	P_UMI_RXP[2]	P_UMI_TXP[2]	AP4	UMI_FTX_MRX_P2	C122	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_P2
UMI_MTX_C_FRX_N2	AR8	P_UMI_RXN[2]	P_UMI_TXN[2]	AR4	UMI_FTX_MRX_N2	C123	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_N2
UMI_MTX_C_FRX_P3	AR7	P_UMI_RXP[3]	P_UMI_TXP[3]	AP3	UMI_FTX_MRX_P3	C120	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_P3
UMI_MTX_C_FRX_N3	AP7	P_UMI_RXN[3]	P_UMI_TXN[3]	AR3	UMI_FTX_MRX_N3	C121	1	2	0.1U_0402_16V7K	UMI_FTX_C_MRX_N3

UMI

+1.2VS — 1 — R1 196_0402_1% — 2 — P_ZVDDP — AR11

Close to AR11

P_ZVDDP

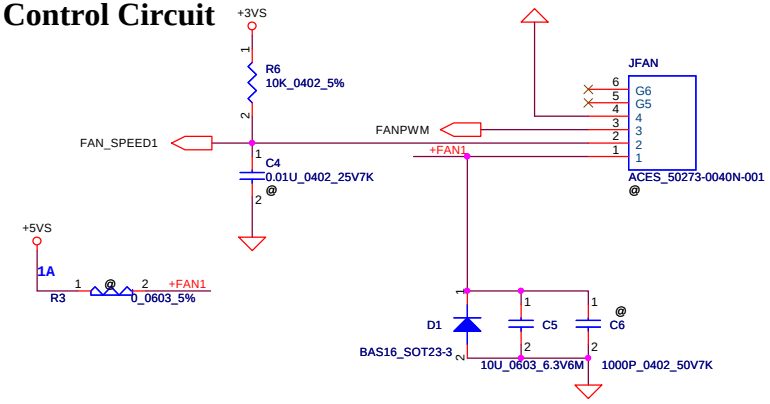
P_ZVSS — AP11 — P_ZVSS — 1 — R2 196_0402_1% — 2

Close to AP11

TRINITY-A8-SERIES_BGA813

5745R1@

FAN Control Circuit



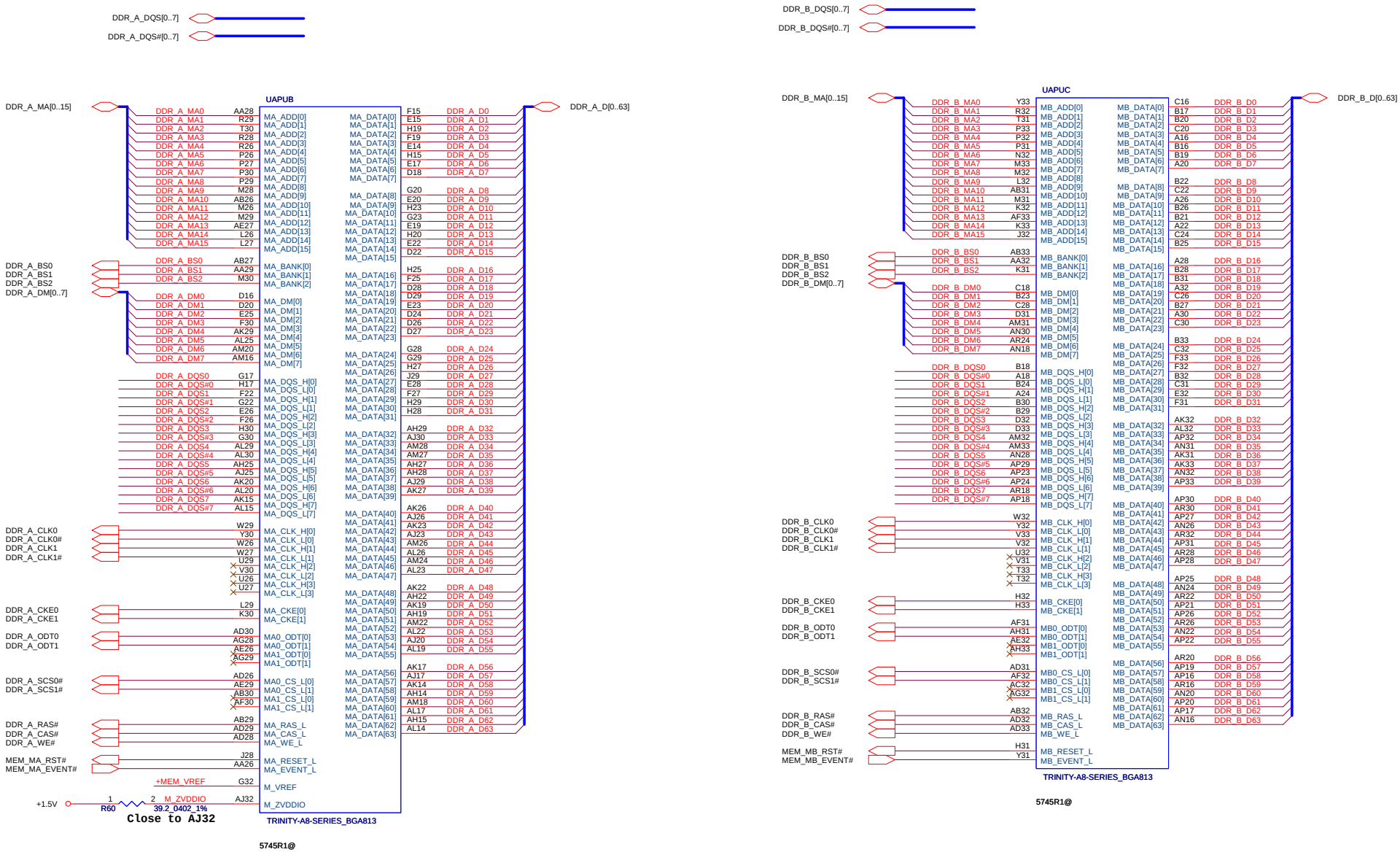
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: AMD Trinity FP2 / GFX / UMI

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 5 of 51



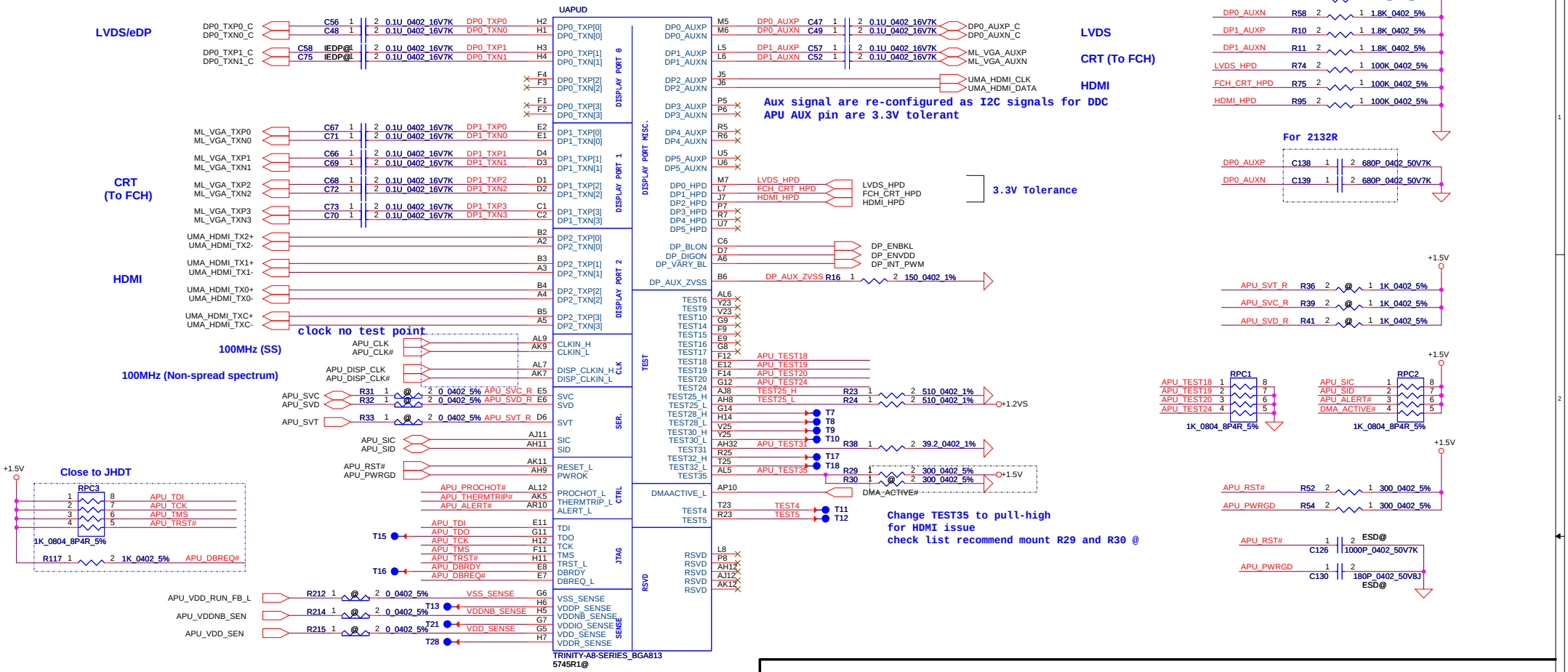
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: AMD Trinity FP2 DDRIII I/F

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 6 of 51



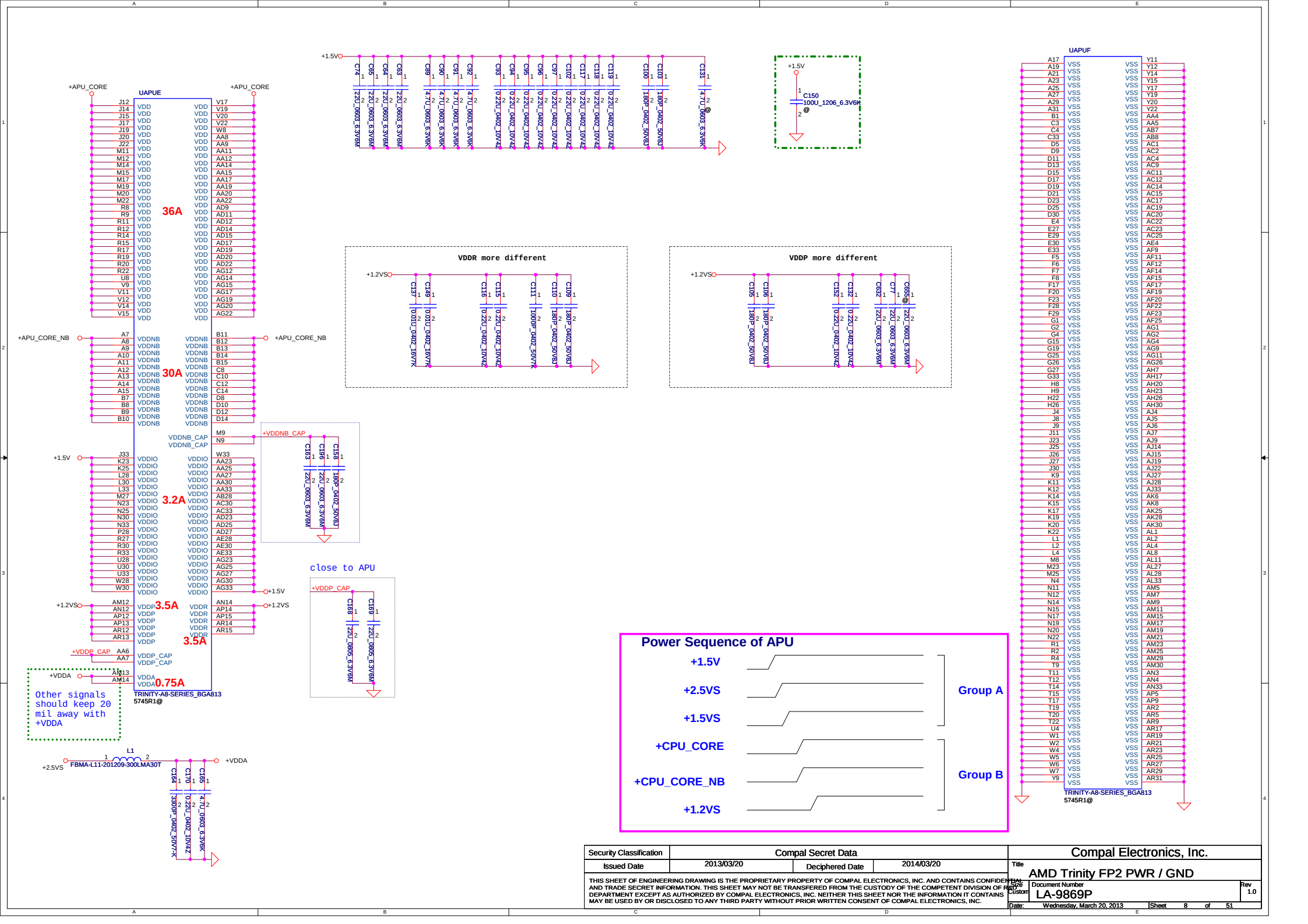
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: AMD Trinity FP2 Display / MISC / HDT

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 7 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

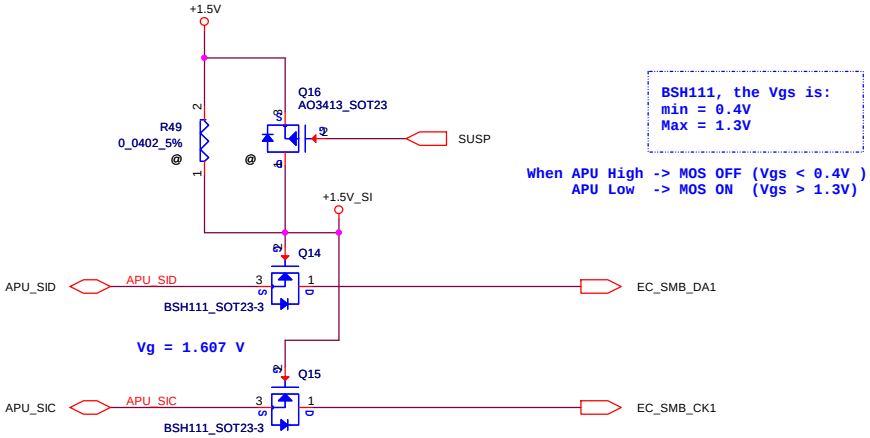
Compal Electronics, Inc.

Title: AMD Trinity FP2 PWR / GND

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 8 of 51

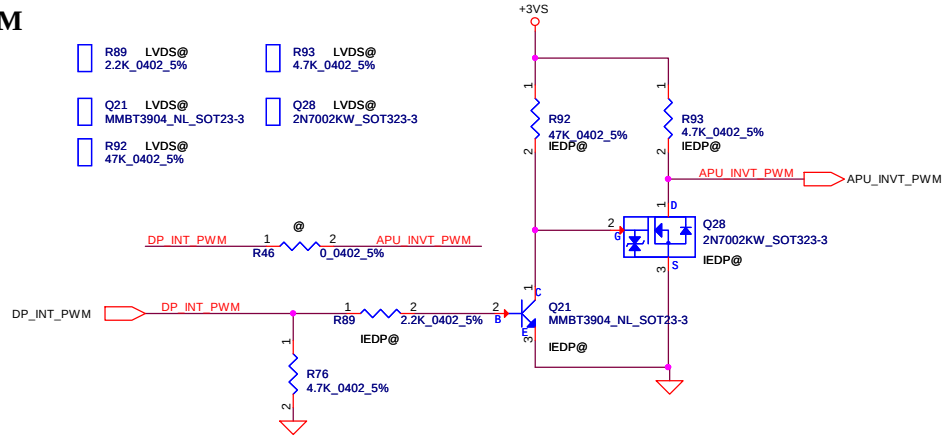
SB-TSI



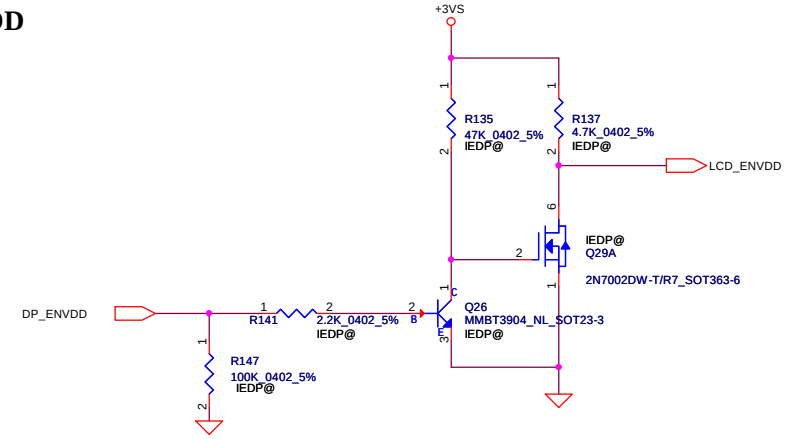
BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

When APU High -> MOS OFF (Vgs < 0.4V)
APU Low -> MOS ON (Vgs > 1.3V)

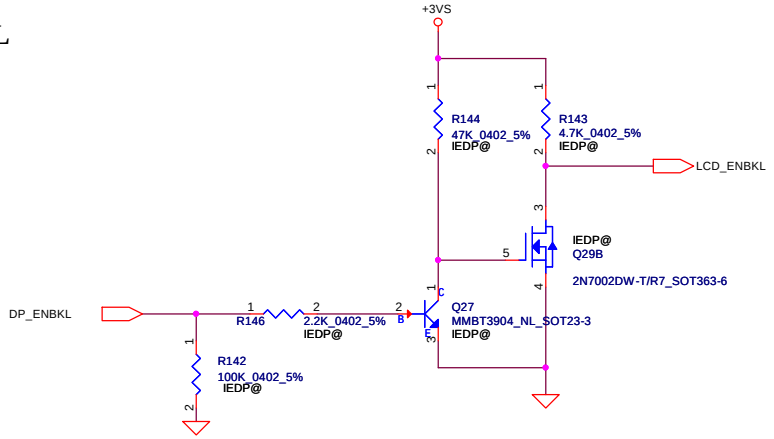
Panel PWM



eDP Panel ENVDD



eDP Panel ENBKL



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Title: AMD Trinity FP2 Singal Level Shifter

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 9 of 51

DDR3 SO-DIMM A
Reverse Type

DDR_A_DQS[0..7]
DDR_A_DQS#[0..7]
DDR_A_D[0..63]
DDR_A_MA[0..15]
DDR_A_DM[0..7]

JDDR3L

+VREF_DQA	1	VREF_DQ	VSS1	2			
DDR_A_D0	3	VSS2	DQ4	4	DDR_A_D4		
DDR_A_D1	5	DQ0	DQ5	6	DDR_A_D5		
	7	DQ1	VSS3	8			
DDR_A_DM0	9	VSS4	DQS#0	10	DDR_A_DQS#0		
	11	DM0	DQS0	12	DDR_A_DQS0		
DDR_A_D2	13	VSS5	VSS6	14			
DDR_A_D3	15	DQ2	DQ6	16	DDR_A_D6		
	17	DQ3	DQ7	18	DDR_A_D7		
DDR_A_D8	19	VSS7	VSS8	20			
DDR_A_D9	21	DQ8	DQ12	22	DDR_A_D12		
	23	DQ9	DQ13	24	DDR_A_D13		
DDR_A_DQS#1	25	VSS9	VSS10	26			
DDR_A_DQS1	27	DQS#1	DM1	28	DDR_A_DM1		
	29	DQS1	RESET#	30	MEM_MA_RST#		
DDR_A_D10	31	VSS11	VSS12	32			
DDR_A_D11	33	DQ10	DQ14	34	DDR_A_D14		
	35	DQ11	DQ15	36	DDR_A_D15		
DDR_A_D16	37	VSS13	VSS14	38			
DDR_A_D17	39	DQ16	DQ20	40	DDR_A_D20		
	41	DQ17	DQ21	42	DDR_A_D21		
DDR_A_DQS#2	43	VSS15	VSS16	44			
DDR_A_DQS2	45	DQS#2	DM2	46	DDR_A_DM2		
	47	DQS2	VSS17	48			
DDR_A_D18	49	VSS18	DQ22	50	DDR_A_D22		
DDR_A_D19	51	DQ18	DQ23	52	DDR_A_D23		
	53	DQ19	VSS19	54			
DDR_A_D24	55	VSS20	DQ28	56	DDR_A_D28		
DDR_A_D25	57	DQ24	DQ29	58	DDR_A_D29		
	59	DQ25	VSS21	60			
DDR_A_DM3	61	VSS22	DQS#3	62	DDR_A_DQS#3		
	63	DM3	DQS3	64	DDR_A_DQS3		
DDR_A_D26	65	VSS23	VSS24	66			
DDR_A_D27	67	DQ26	DQ30	68	DDR_A_D30		
	69	DQ27	DQ31	70	DDR_A_D31		
	71	VSS25	VSS26	72			
DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1		
	75	VDD1	VDD2	76			
	77	NC1	A15	78	DDR_A_MA15		
DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14		
	81	VDD3	VDD4	82			
DDR_A_MA12	83	A12/BC#	A11	84	DDR_A_MA11		
DDR_A_MA9	85	A9	A7	86	DDR_A_MA7		
	87	VDD5	VDD6	88			
DDR_A_MA8	89	A8	A6	90	DDR_A_MA6		
DDR_A_MA5	91	A5	A4	92	DDR_A_MA4		
	93	VDD7	VDD8	94			
DDR_A_MA3	95	A3	A2	96	DDR_A_MA2		
DDR_A_MA1	97	A1	A0	98	DDR_A_MA0		
	99	VDD9	VDD10	100			
DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1		
DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1#		
	105	VDD11	VDD12	106			
DDR_A_MA10	107	A10/AP	BA1	108	DDR_A_BS1		
DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#		
	111	VDD13	VDD14	112			
DDR_A_WE#	113	WE#	S0#	114	DDR_A_SCS0#		
DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0		
	117	VDD15	VDD16	118			
DDR_A_MA13	119	A13	ODT1	120	DDR_A_ODT1		
DDR_A_SCS1#	121	S1#	NC2	122			
	123	VDD17	VDD18	124			
	125	NCTEST	VREF_CA	126	+VREF_CAA		
	127	VSS27	VSS28	128			
DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36		
DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37		
	133	VSS29	VSS30	134			
DDR_A_DQS#4	135	DQS#4	DM4	136	DDR_A_DM4		
DDR_A_DQS4	137	DQS4	VSS31	138			
	139	VSS32	DQ38	140	DDR_A_D38		
DDR_A_D34	141	DQ34	DQ39	142	DDR_A_D39		
DDR_A_D35	143	DQ35	VSS33	144			
	145	VSS34	DQ44	146	DDR_A_D44		
DDR_A_D40	147	DQ40	DQ45	148	DDR_A_D45		
DDR_A_D41	149	DQ41	VSS35	150			
	151	VSS36	DQS#5	152	DDR_A_DQS#5		
DDR_A_DM5	153	DM5	DQS5	154	DDR_A_DQS5		
	155	VSS37	VSS38	156			
DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46		
DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47		
	161	VSS39	VSS40	162			
DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52		
DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53		
	167	VSS41	VSS42	168			
DDR_A_DQS#6	169	DQS#6	DM6	170	DDR_A_DM6		
DDR_A_DQS6	171	DQS6	VSS43	172			
	173	VSS44	DQ54	174	DDR_A_D54		
DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55		
DDR_A_D51	177	DQ51	VSS45	178			
	179	VSS46	DQ60	180	DDR_A_D60		
DDR_A_D56	181	DQ56	DQ61	182	DDR_A_D61		
DDR_A_D57	183	DQ57	VSS47	184			
	185	VSS48	DQS#7	186	DDR_A_DQS#7		
DDR_A_DM7	187	DM7	DQS7	188	DDR_A_DQS7		
	189	VSS49	VSS50	190			
DDR_A_D58	191	DQ58	DQ62	192	DDR_A_D62		
DDR_A_D59	193	DQ59	DQ63	194	DDR_A_D63		
	195	VSS51	VSS52	196			
	197	SA0	EVENT#	198	MEM_MA_EVENT#		
	199	VDDSPD	SDA	200	FCH_SDATA0		
	201	SA1	SCL	202	FCH_SCLK0		
+0.75VS	203	VTT1	VTT2	204	+0.75VS		
	205	G1	G2	206			

LCN_DAN06-K4406-0103
@

+3VS
C182 1 2 0.1U_0402_16V4Z

+1.5V
R79 1K_0402_1%
R81 1K_0402_1%
+VREF_DQA
C156 0.1U_0402_16V7K
C157 2.2U_0402_6.3V6M
Close to JDDR3H.1

+1.5V
C148 100U_1206_6.3V6K
SE00000O000

+1.5V
R80 1K_0402_1%
R82 1K_0402_1%
+VREF_CAA
C162 0.1U_0402_16V7K
C161 2.2U_0402_6.3V6M
Close to JDDR3H.126

Layout Note:
Place near JDDR3H

+1.5V
C176 10U_0603_6.3V6M
C174 10U_0603_6.3V6M
C173 10U_0603_6.3V6M
C171 10U_0603_6.3V6M
C167 10U_0603_6.3V6M
C166 10U_0603_6.3V6M
C179 0.1U_0402_16V4Z
C178 0.1U_0402_16V4Z
C185 0.1U_0402_16V4Z
C180 0.1U_0402_16V4Z

Layout Note:
Place near JDDR3H.203 and 204

+0.75VS
C84 4.7U_0603_6.3V6K
C186 0.1U_0402_16V4Z
C205 0.1U_0402_16V4Z

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

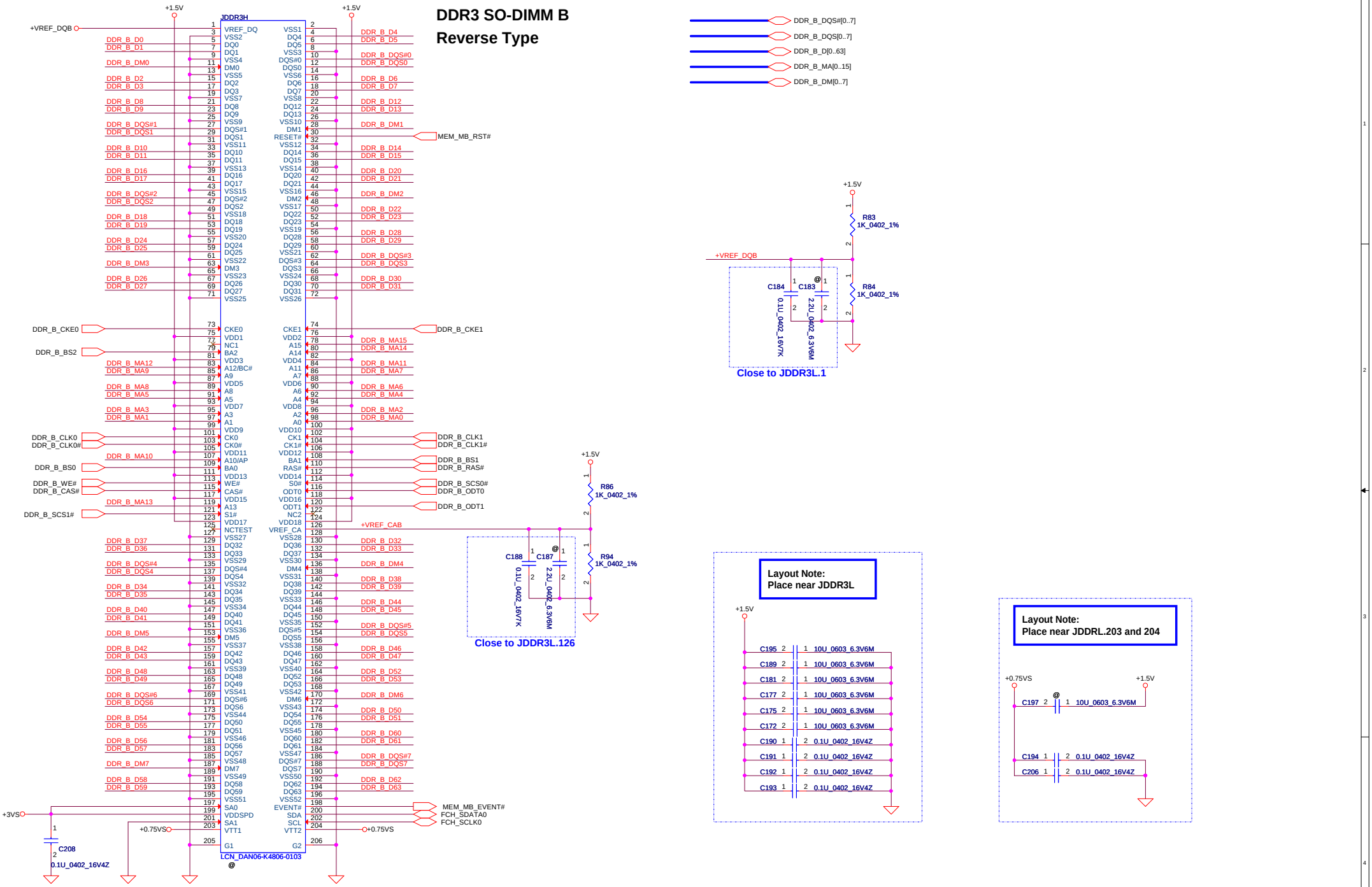
Compal Electronics, Inc.

Title: ***DDRIII-SODIMM0***

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 10 of 51

DDR3 SO-DIMM B
Reverse Type



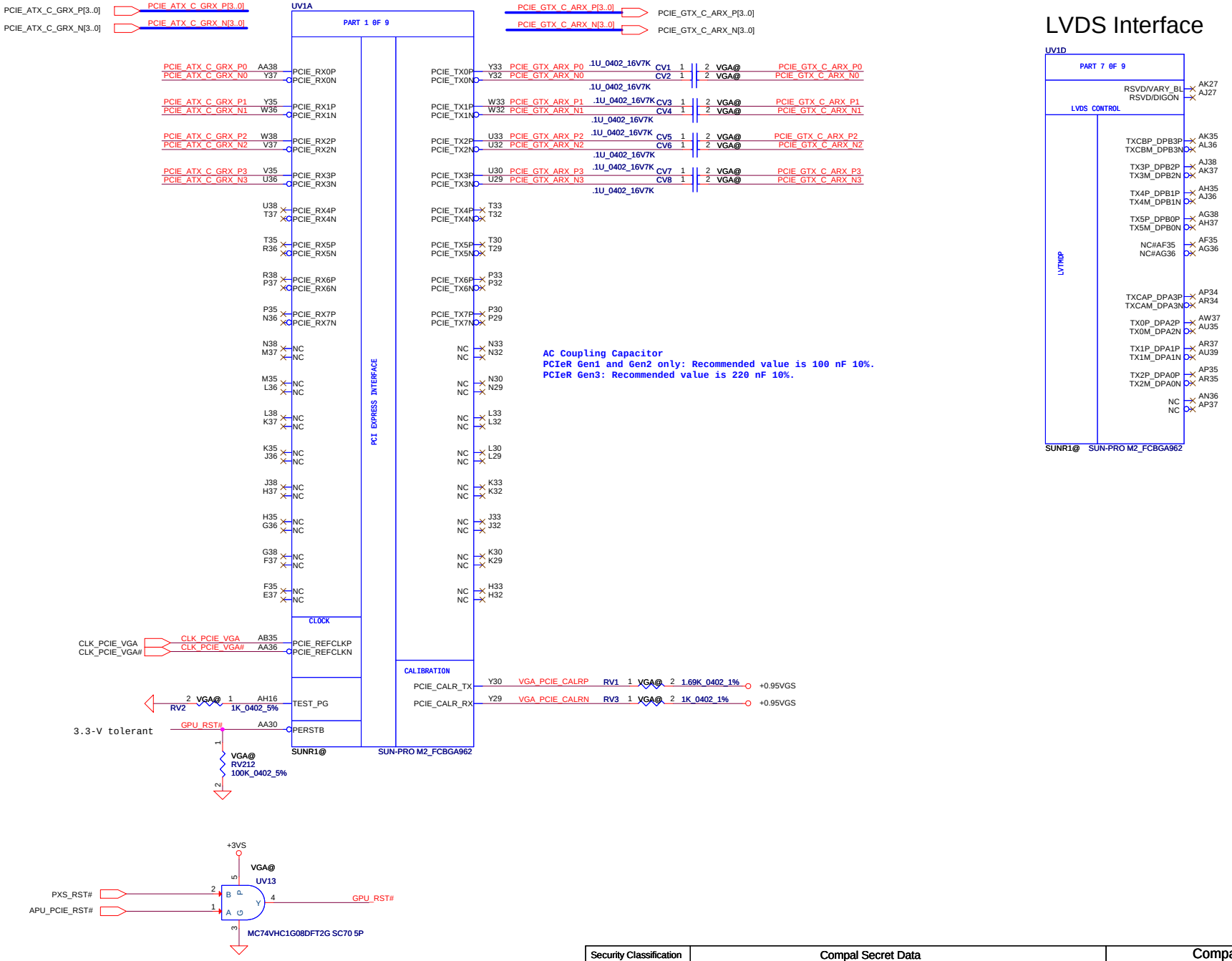
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM1***

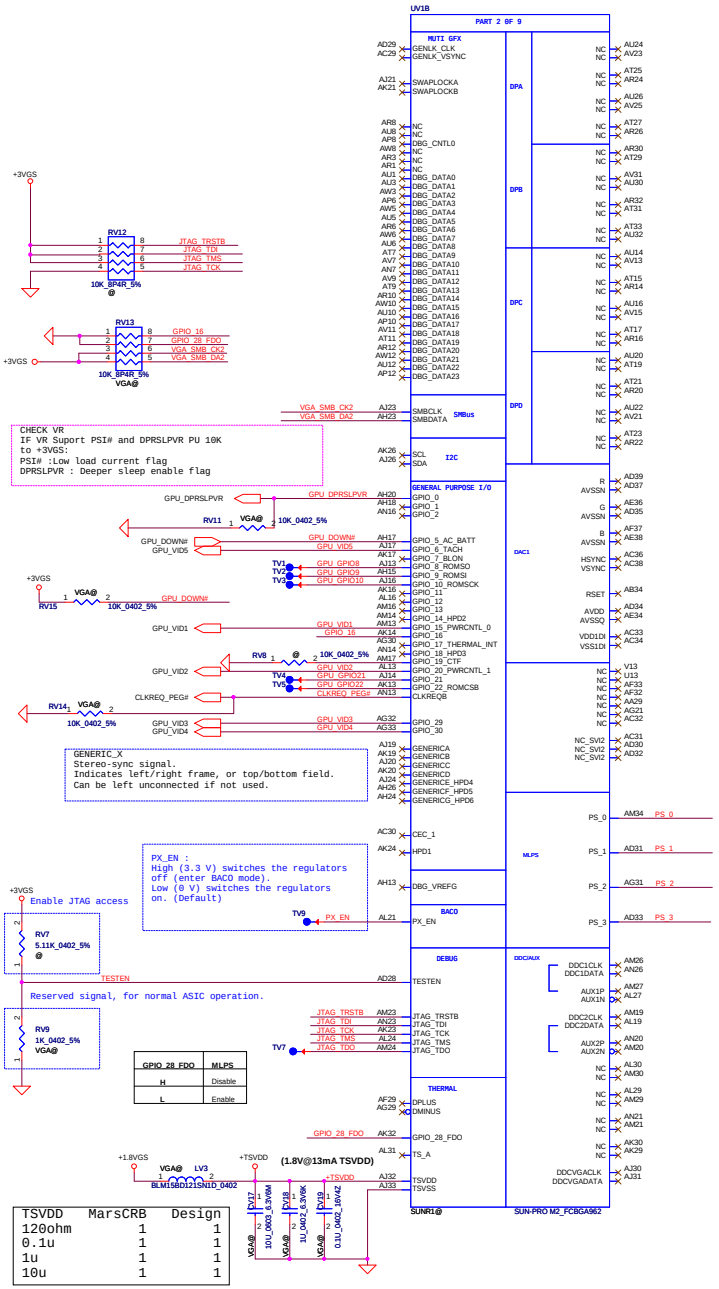
Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 11 of 51



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date 2014/03/20	Title: PCIE/LVDS

Size: Custom	Document Number: LA-9869P		Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 12 of 51		



Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Suport PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point.
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109℃ by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_ CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[0] AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

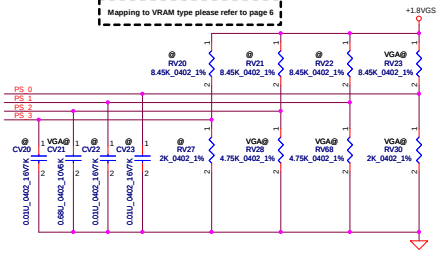
For MEMCLK 1GHZ	Brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

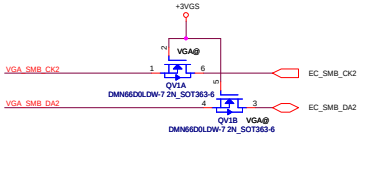
For MEMCLK 900MHZ	Brand	Description	Comment	PS_3[3:1]	R_pu (ohm)	R_pd (ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V-1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 6





Security Classification	Compal Secret Data	
Issued Date	2013/03/20	Deciphered Date 2014/03/20

Compal Electronics, Inc.

Title: Main_MSIC

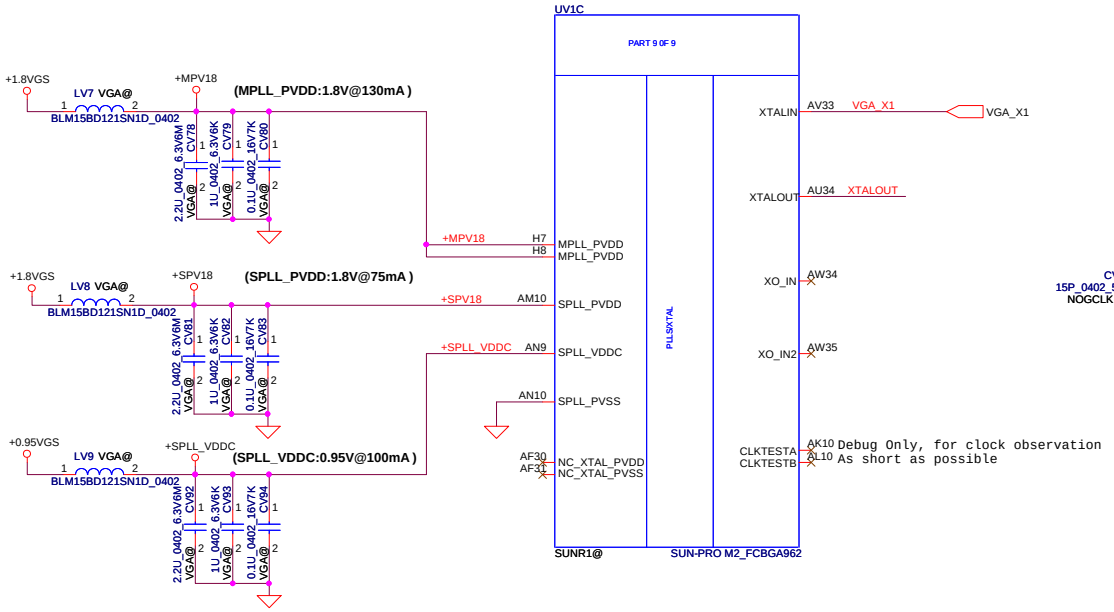
Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 13 of 51

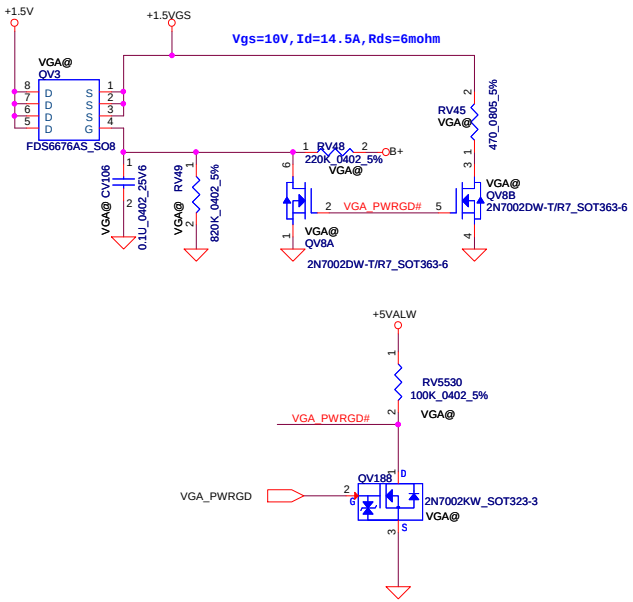
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

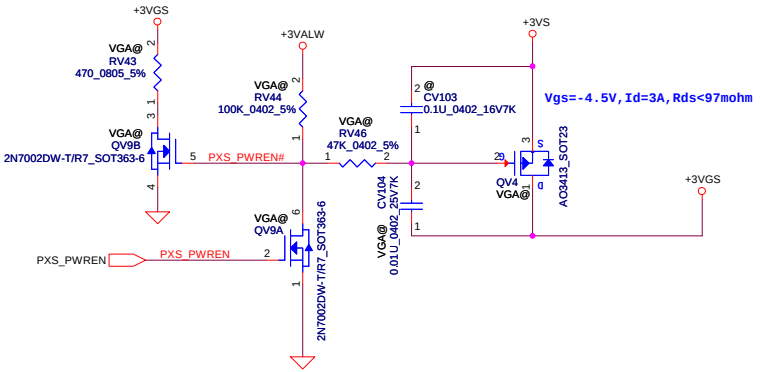
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+1.5V to +1.5VGS



+3VS to +3VGS



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: BACO POWER

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 14 of 51

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

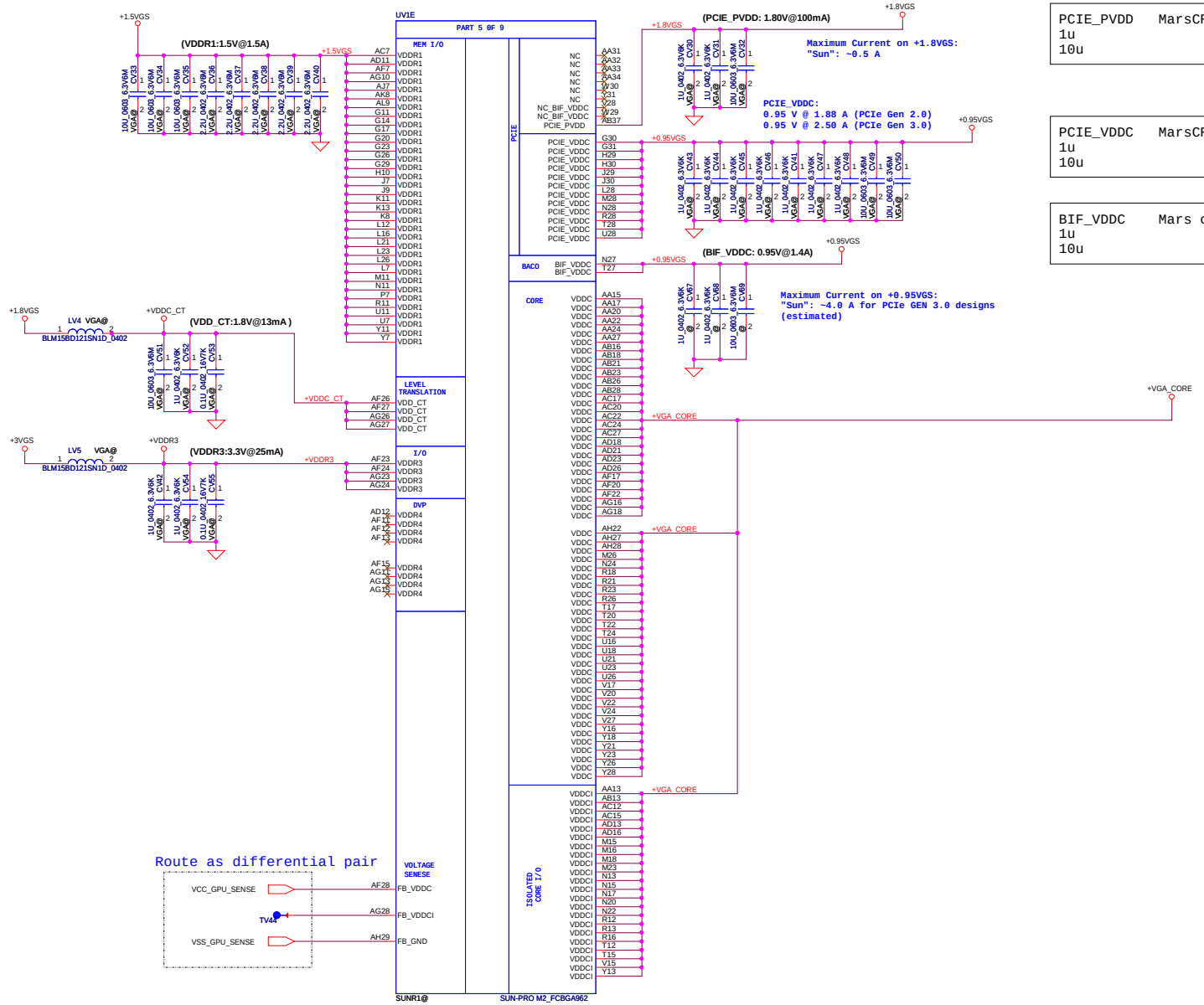
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars check list	Design
120ohm	1	1
1u	3	2
10u	1	0
0.1u	0	1

PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

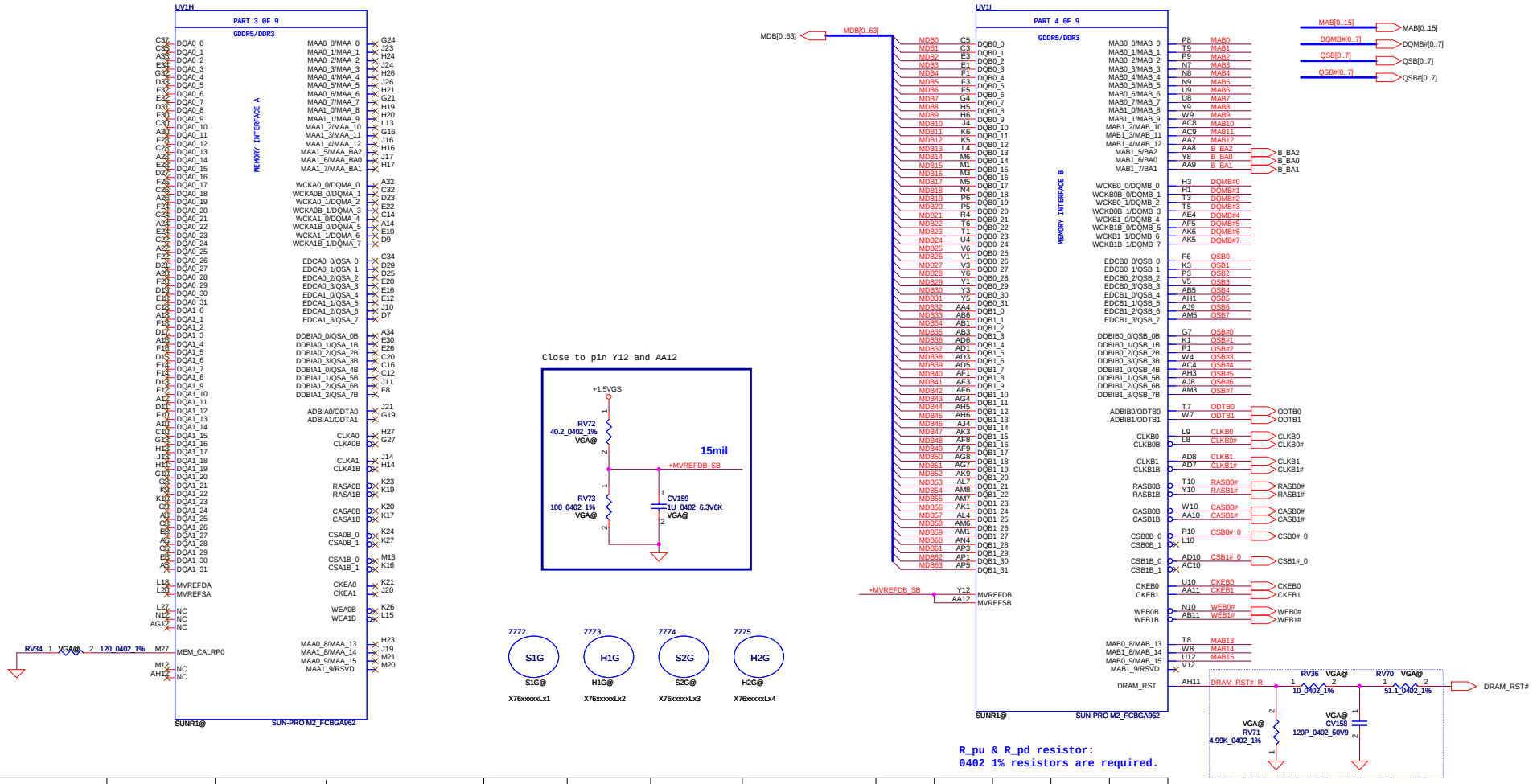
BIF_VDDC	Mars check list	Design
1u	1	1
10u	1	1



Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Title	Power		
Size C	Document Number LA-9869P		Rev 1.0
Date: Wednesday, March 20, 2013	Sheet 15 of 51		

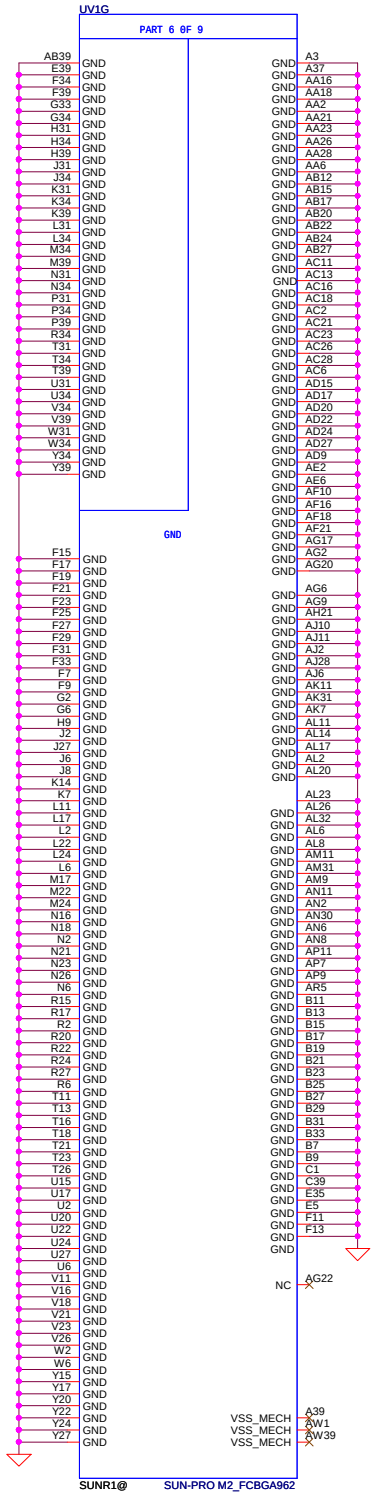


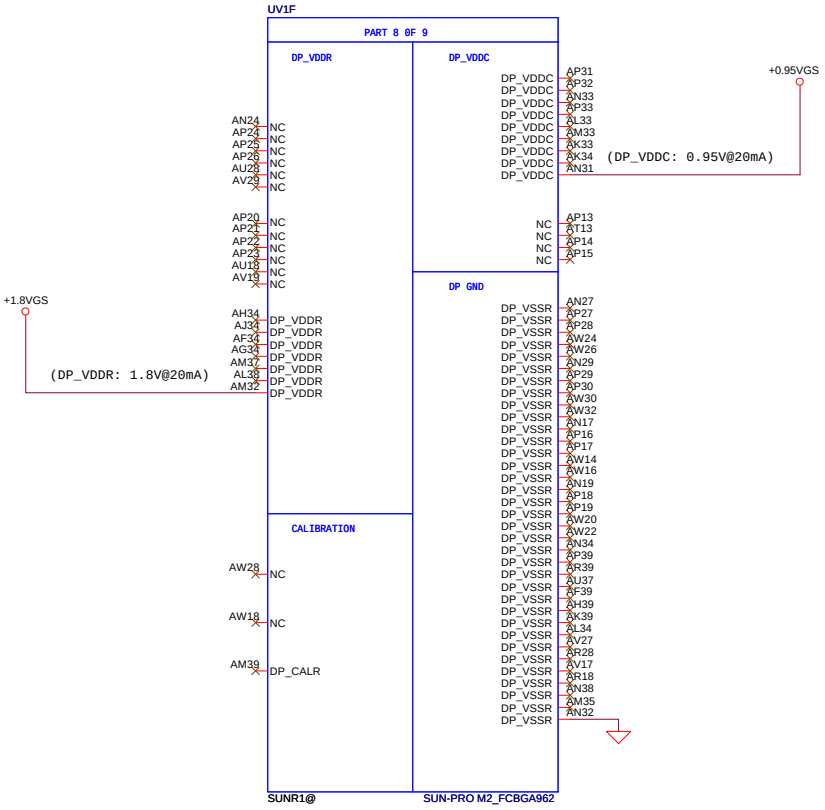
R_pu & R_pd resistor:
0402 1% resistors are required.

Place all these components close to GPU (Within 25mm) and keep all component close to each other

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YOG0	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Hynix	SA000065320	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M2	64bit	Micron	SA00005XB10	MT41K128M16JT-107G:K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH40	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	0	RV20 3.4K	RV27 10K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date	2014/03/20
Title	MEM Interface		
Size C	Document Number LA-9869P		Rev 1.0
Date: Wednesday, March 20, 2013	Sheet 16 of 51		





Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

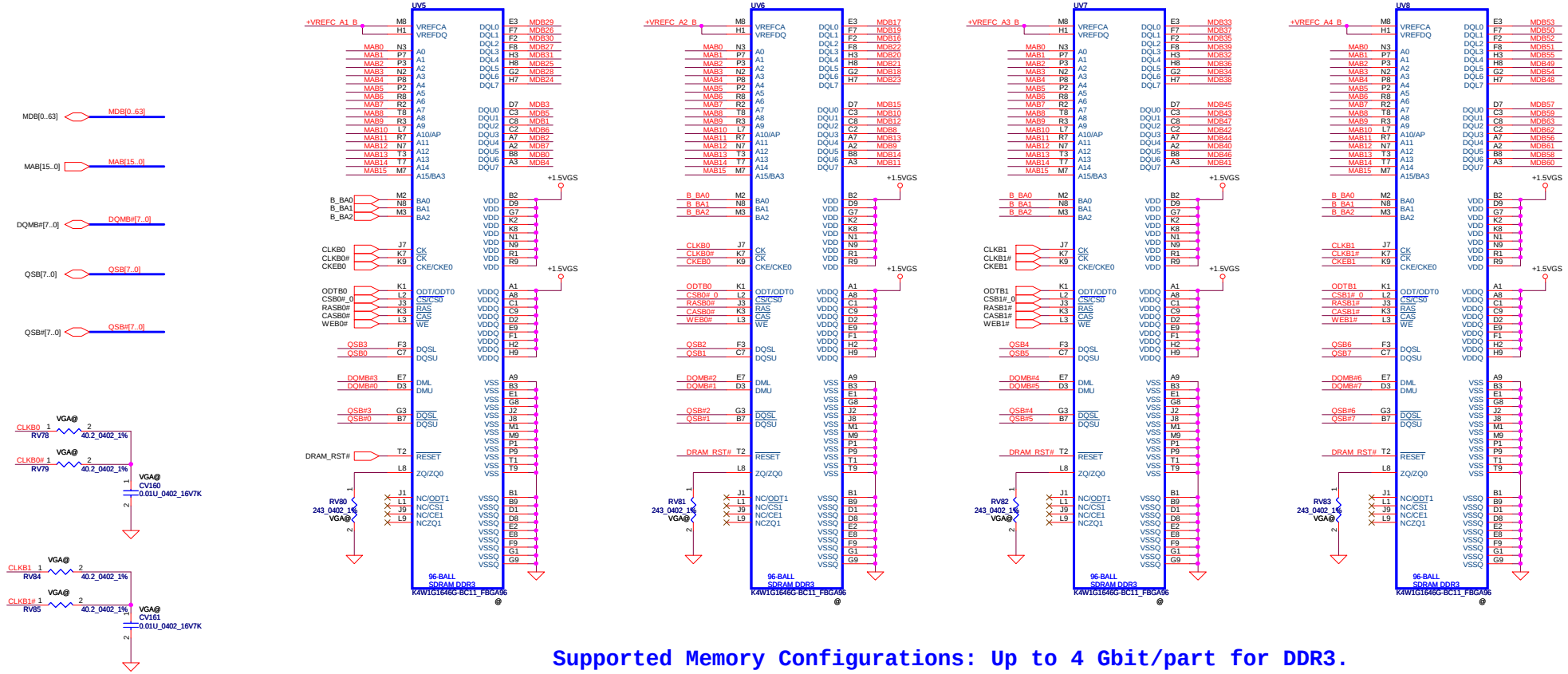
Compal Electronics, Inc.

Title: PWR_GND

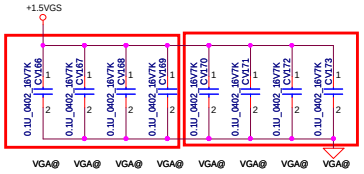
Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 17 of 51

CHANNEL B: 512MB/1024MB DDR3

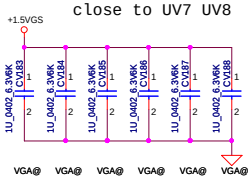


Supported Memory Configurations: Up to 4 Gbit/part for DDR3.

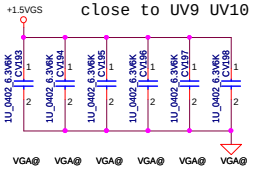


close to UV9 UV10

close to UV7 UV8



close to UV7 UV8



close to UV9 UV10

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: VRAM Channel B

Size	Document Number	Rev
C	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 18 of 51

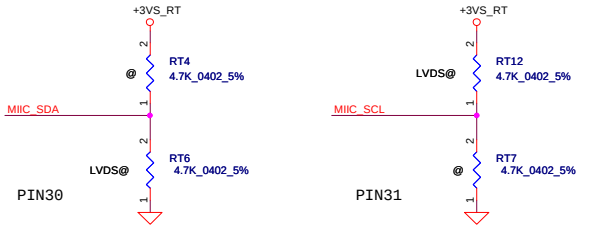
SWR / LDO Mode select

	LDO	SWR
2132R	RT24	

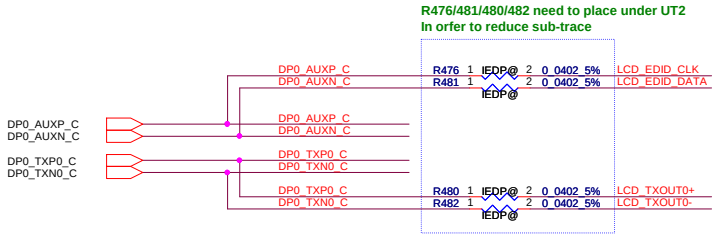
※ If use 2132R, please select LDO mode as default.

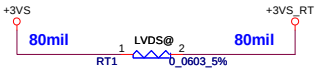
Mode Configure

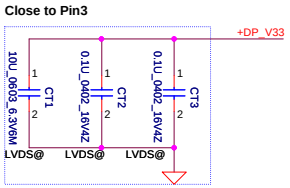
```
  ROM only  mode : PIN 30 4.7k pull low,  Pin 31 4.7k pull high.
※EP mode         : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
  EEPROM         : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

〈 ※Default mode 〉
```

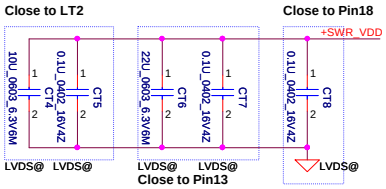


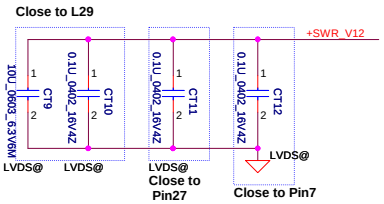
R476/481/480/482 need to place under UT2
In orfer to reduce sub-trace

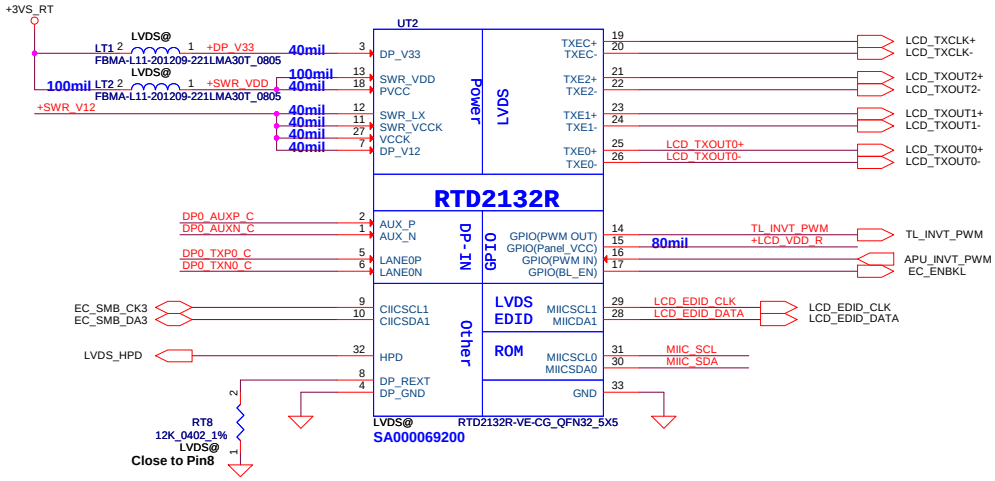


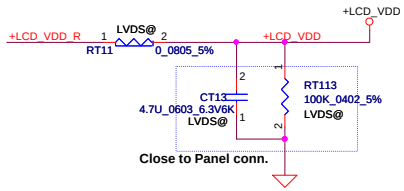












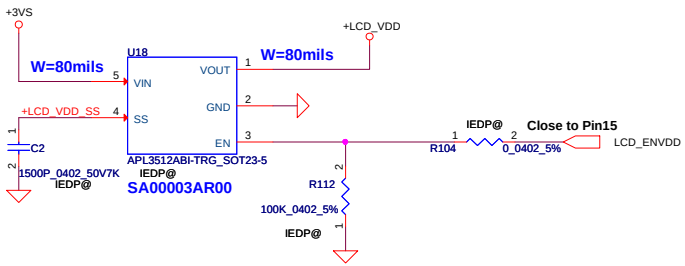
	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

LCD POWER CIRCUIT (For eDP panel only)



Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date 2014/03/20	Title: LVDS Translator - RTD2132S
			Size: Custom; Document Number: LA-9869P; Rev: 1.0
			Date: Wednesday, March 20, 2013; Sheet 19 of 51

For LVDS 1ch Panel

LCD_TXOUT0+ → LCD_TXOUT0+
LCD_TXOUT0- → LCD_TXOUT0-
LCD_TXOUT1+ → LCD_TXOUT1+
LCD_TXOUT1- → LCD_TXOUT1-
LCD_TXOUT2+ → LCD_TXOUT2+
LCD_TXOUT2- → LCD_TXOUT2-
LCD_TXCLK+ → LCD_TXCLK+
LCD_TXCLK- → LCD_TXCLK-
LCD_EDID_CLK → LCD_EDID_CLK
LCD_EDID_DATA → LCD_EDID_DATA

For eDP Panel

DP0_TXP1_C → R102 1 IEDP@ 2 0_0402_5% → LCD_TXOUT1+
DP0_TXN1_C → R105 1 IEDP@ 2 0_0402_5% → LCD_TXOUT1-

LCD_EDID_DATA → R149 IEDP@ 100K_0402_5% → +3VS
LCD_EDID_CLK → R150 IEDP@ 100K_0402_5% → +3VS

Reserve for eDP panel potience issue

+3VS
IEDP@1 R103 2 0_0402_5%
IEDP@ U19 SN74AHC1G08DCKR_SC70-5
BKOFF#_R → D16 RB751V40_SC76-2 LVDS@ → R114 10K_0402_5%
IN1 → LCD_ENBKL
IN2 → BKOFF#
R152 0_0402_5% LVDS@

1.5A

+LCD_INV → L2 EMI@ FBMA-L11-201209-221LMA30T_0805 → B+

IEDP@ R108 0_0402_5% → APU_INVT_PWM
LED_PWM → D17 RB751V40_SC76-2 → TL_INVT_PWM
R133 47K_0402_5%

USB20_P1_R → EMI@ L55 WCM-2012-900T_0805 → USB20_P1
USB20_N1_R → EMI@ L55 WCM-2012-900T_0805 → USB20_N1

TOUCH_EMI@ R155 0_0402_5%
USB20_N4_R → @TOUCH_EMI@ L56 WCM-2012-900T_0805 → USB20_N4
USB20_P4_R → @TOUCH_EMI@ L56 WCM-2012-900T_0805 → USB20_P4
TOUCH_EMI@ R156 0_0402_5%

D32 ESD@ SC300001400 close to LVDS conn.
USB20_P1_R ↔ USB20_P1_R
USB20_N1_R ↔ USB20_N1_R
+3VS → VBUS
GND
INT_MIC_DATA ↔ INT_MIC_DATA
INT_MIC_CLK ↔ INT_MIC_CLK

JLVDS_@ STARC_111H30-000000-G4-R

+5VS_LVDS_TOUCH → R391 0_0603_5% → +5VS
USB20_N4_R
USB20_P4_R
BKOFF#
INT_MIC_DATA → INT_MIC_DATA
INT_MIC_CLK → INT_MIC_CLK
USB20_P1_R
USB20_N1_R
+3VS_LVDS_CAM → R392 0_0603_5% → +3VS
+LCD_VDD → +LCD_VDD **Irush=1.5A**
+3VS
LCD_EDID_CLK
LCD_EDID_DATA
LCD_TXOUT0-
LCD_TXOUT0+
LCD_TXOUT1-
LCD_TXOUT1+
LCD_TXOUT2-
LCD_TXOUT2+
LCD_TXCLK-
LCD_TXCLK+
LED_PWM
BKOFF#_R
R154 IEDP@ 0_0402_5% → LVDS_HPD
+LCD_INV **1.5A**
GND GND GND GND GND

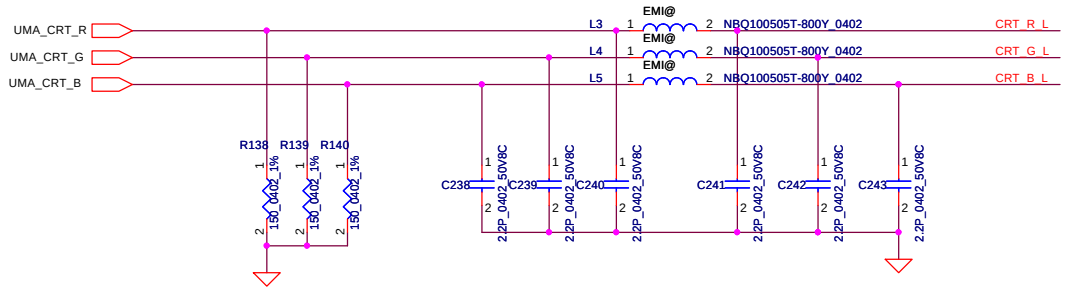
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

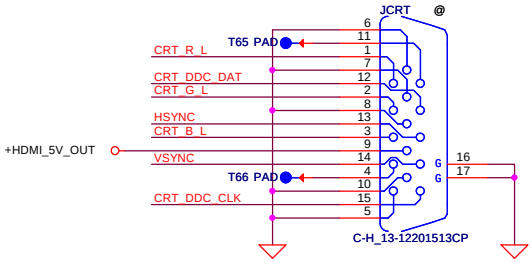
Compal Electronics, Inc.

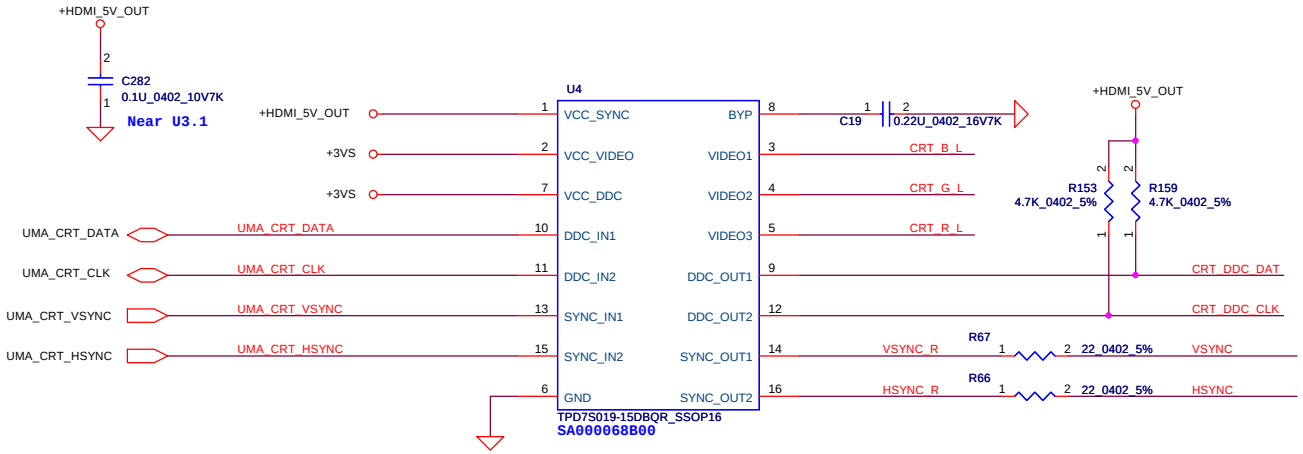
Title: ***LVDS***

Size: Custom | Document Number: **LA-9869P** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 20 of 51







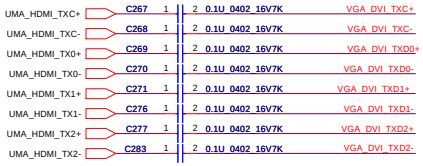
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

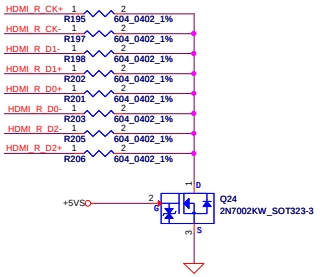
Compal Electronics, Inc.

Title: ***CRT***

Size	Document Number	Rev
	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 21 of 51

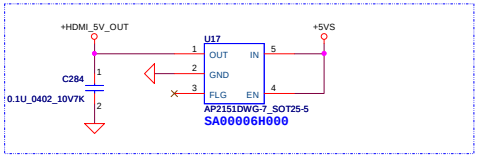




Change R184 and R185 from 2K to 4.7K for HDMI detect issue on Comal

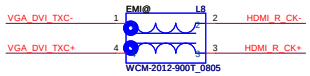
HDMI POWER CIRCUIT

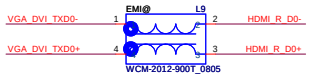
VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A

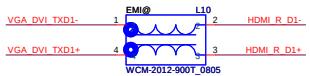


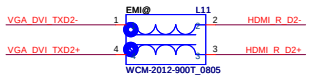
HDMI Royalty

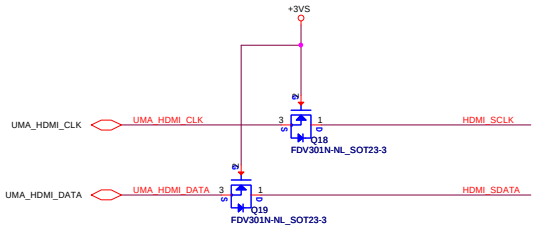
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM



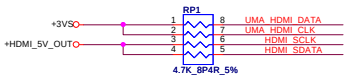


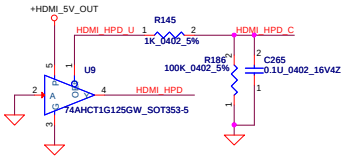




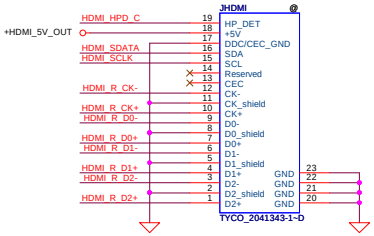


Q18/Q19
Change to FDV301 due to BSH111 EOL





HDMI Connector



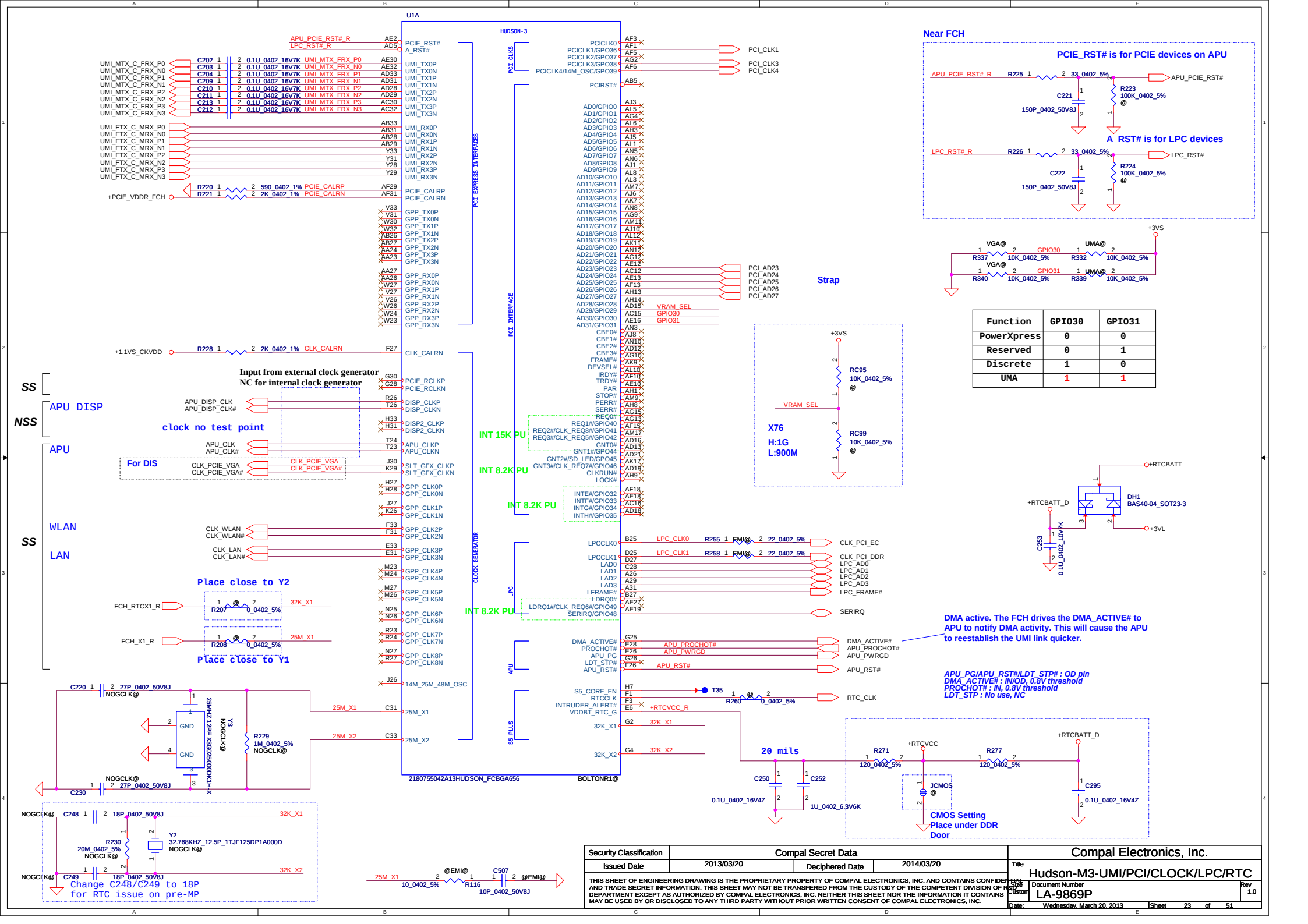
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: *HDMI Conn./CEC*

Size: | Document Number: **LA-9869P** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 22 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: Hudson-M3-UMI/PCI/CLOCK/LPC/RTC

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 23 of 51

PCIE_RST2# is for PCIE devices on FCH

GEVENT#2~22 INT 10K PU

U1D

HUDSON-3

T50

PCIE_RST2#/GEVENT4#
RII#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GENERIC#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STA0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226

2180755042A13HUDSON_FCBGA656

BOLTONR1@

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

USB MISC
USB 1.1
ACPI / WAKE UP EVENTS
USB 2.0
@10
USB OC
HD AUDIO
USB 3.0
EMBEDDED CTRL

INT 15K PD
INT 15K PD
INT 8.2K PU
INT 8.2K PU
INT 8.2K PU
INT 10K PU
INT 10K PU
INT 50K PD
INT 10K PU
INT 10K PU
INT 10K PU
INT 10K PU

USB_RCOMP R329 1 2 11.8K_0402_1%

Hudson-M2/M3
OHCI (DEV-20, FUN-5)

Hudson-M2
OHCI (DEV-22, FUN-0)
EHCI (DEV-22, FUN-2)

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

USB 3.0-Right 2
USB20_P11
USB20_N11
USB 3.0-Right 1
USB20_P10
USB20_N10

Hudson-M2/M3
OHCI (DEV-19, FUN-0)
EHCI (DEV-19, FUN-2)

Touch
WLAN (BT)
Card reader
Int. Camera
USB-Left 1
USB20_P4
USB20_N4
USB20_P3
USB20_N3
USB20_P2
USB20_N2
USB20_P1
USB20_N1
USB20_P0
USB20_N0

Hudson-M2/M3
OHCI (DEV-18, FUN-0)
EHCI (DEV-18, FUN-2)
<Support Wakeup>

C16 USBSS_CALRP R330 1 2 1K_0402_1%
A16 USBSS_CALRN R334 1 2 1K_0402_1%
+FCH_VDD_11_SSUSB_S

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

USB 3.0-Right 2
USB30_TX1P
USB30_TX1N
USB30_RX1P
USB30_RX1N
USB 3.0-Right 1
USB30_TX0P
USB30_TX0N
USB30_RX0P
USB30_RX0N

RP8
GPIO193
GPIO194
GPIO195
GPIO196
10K_8P4R_5%

Strap
EC_PWM2

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

For DIS
VGA_PWRGD
LAN_EN
CLKREQ_PEG#
ODD_DA# FCH

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off
For DIS

USB_OC2# is for right USB2.0 ports
USB_CHG_OC# is for right USB3.0 ports
USB_OC0# is for right USB3.0 ports

ODD_PLUGIN#
USB_OC#2
USB_CHG_OC#
USB_OC#0

For ESD request

AZ_BITCLK_HD
AZ_SDOUT_HD
AZ_SDIN0_HD
AZ_SYNC_HD
AZ_RST_HD#
HDA_BITCLK
HDA_SDOUT
HDA_SYNC
HDA_RST#

RP12
H_THERMTRIP#
USB_OC#0
USB_CHG_OC#
USB_OC#2
10K_8P4R_5%

For DIS
PXS_RST#
PXS_PWREN

For FCH internal debug use
TEST0
TEST1
TEST2

EC_LID_OUT#
FCH_PCIE_WAKE#
FCH_SCLK1
FCH_SDATA1
PXS_PWREN
EC_RSMRST#
HDA_BITCLK
PXS_RST#

RP10
AZ_SDIN1_HD
AZ_SDIN3_HD
AZ_SDIN2_HD
AZ_SDIN0_HD
10K_8P4R_5%

For DIS
Q5530A
2N7002KDWH_SOT363-6
Q5530B
2N7002KDWH_SOT363-6
PXS_PWREN
10K_0402_5%
+3VALW
R216
EC_PXCONTROL

Place R425 and C363
close to FCH for ESD

Q32
2N7002KW_SOT323-3
ODD_DA# FCH
R425 0_0402_5%
ODD_DA# Q
R311 10K_0402_5%
ODD_DA#

HDMI_HPD
Q30
2N7002KW_SOT323-3
HDMI_HPD_FCH
R283 10K_0402_5%

ESD@
C505 1000P_0402_50V7K
FCH_PWRGD

R279 10K_0402_5%
WD_PWRGD

R295 0_0402_5%
R129 100K_0402_5%

R320 EMI@ 33_0402_5%
R321 33_0402_5%
R322 33_0402_5%
R323 33_0402_5%

C503 180P_0402_50V8J
C504 180P_0402_50V8J
ESD@
PXS_RST#
ODD_DA# FCH

R282 100K_0402_5%
R281 10K_0402_5%
R288 2.2K_0402_5%
R289 2.2K_0402_5%
R290 2.2K_0402_5%
R292 2.2K_0402_5%
R293 2.2K_0402_5%
R296 10K_0402_5%

R286 2.2K_0402_5%
R287 2.2K_0402_5%
R291 8.2K_0402_5%
R284 8.2K_0402_5%

R297 10K_0402_5%
R280 2.2K_0402_5%
R324 10K_0402_5%
R269 1K_0402_5%

Security Classification: Compal Secret Data
Issued Date: 2013/03/20
Deciphered Date: 2014/03/20

Compal Electronics, Inc.

Title: Hudson-M3-ACPI/USB/EC

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 24 of 51

HDD

ODD

U1B

HUDSON-3

SATA_FTX_DRX_P0 / SATA_FTX_DRX_N0 → AK19 / AM19 SATA_TX0P / SATA_TX0N

SATA_FRX_C_DTX_N0 / SATA_FRX_C_DTX_P0 → AL20 / AN20 SATA_RX0N / SATA_RX0P

SATA_FTX_DRX_P1 / SATA_FTX_DRX_N1 → AN22 / AL22 SATA_TX1P / SATA_TX1N

SATA_FRX_C_DTX_N1 / SATA_FRX_C_DTX_P1 → AH20 / AJ20 SATA_RX1N / SATA_RX1P

AJ22 / AH22 SATA_TX2P / SATA_TX2N

AM23 / AK23 SATA_RX2N / SATA_RX2P

AH24 / AJ24 SATA_TX3P / SATA_TX3N

AN24 / AL24 SATA_RX3N / SATA_RX3P

AL26 / AN26 SATA_TX4P / SATA_TX4N

AJ26 / AH26 SATA_RX4N / SATA_RX4P

AN29 / AL28 SATA_TX5P / SATA_TX5N

AK27 / AM27 SATA_RX5N / SATA_RX5P

AL29 / AN31 NC6 / NC7

AL31 / AL33 NC8 / NC9

AH33 / AH31 NC10 / NC11

AJ33 / AJ31 NC12 / NC13

SERIAL ATA

+AVDD_SATA → R336 2 1 1K_0402_1% SATA_CALRP AF28 SATA_CALRP

+AVDD_SATA → R130 2 1 931_0402_1% SATA_CALRN AF27 SATA_CALRN

AD22 SATA_ACT#/GPIO67

AF21 SATA_X1

AG21 SATA_X2

INT 8.2K PU

SD_CLK/SCLK_0/GPIO73 AL14 HDMI_EN# R443 2 1 1K_0402_1%

SD_CMD/SLOAD_0/GPIO74 AN14 SPK_DET → SPK_DET

SD_CD#/GPIO75 AJ12

SD_WP/GPIO76 AH12

SD_DATA0/SDATI_0/GPIO77 AK13

SD_DATA1/SDATO_0/GPIO78 AM13

SD_DATA2/GPIO79 AH15

SD_DATA3/GPIO80 AJ14

SD_CARD

GBE_COL AC4

GBE_CRS AD3

GBE_MDCK AD9

GBE_MDIO W10

GBE_RXCLK AB8

GBE_RXD3 AH7

GBE_RXD2 AF7

GBE_RXD1 AE7

GBE_RXD0 AD7

GBE_RXCTL/RXDV AG8

GBE_RXERR AD1

GBE_TXCLK AB7

GBE_TXD3 AF9

GBE_TXD2 AG6

GBE_TXD1 AE8

GBE_TXD0 AD8

GBE_TXCTL/TXEN AB9

GBE_PHY_PD AC2

GBE_PHY_RST# AA7

GBE_PHY_INTR W9 → GBE_PHY_INTR R352 1 2 10K_0402_5% +3VALW_FCH

GBE_LAN

INT 10K PU

SPI_DI/GPIO164 V6 FCH_SPI_MISO

SPI_DO/GPIO163 V5 FCH_SPI_MOSI

SPI_CLK/GPIO162 V3 FCH_SPI_CLK_R R111 1 @ 2 0_0402_5% FCH_SPI_CLK

SPI_CS1#/GPIO165 T6 FCH_SPI_CS1#

ROM_RST#/SPI_WP#/GPIO161 V1

SPI_ROM

VGA_RED L30 → UMA_CRT_R

VGA_GREEN L32 → UMA_CRT_G

VGA_BLUE M29 → UMA_CRT_B

VGA_HSYNC/GPO68 M28 → UMA_CRT_HSYNC

VGA_VSYNC/GPO69 N30 → UMA_CRT_VSYNC

VGA_DDC_SDA/GPO70 M33 → UMA_CRT_DATA

VGA_DDC_SCL/GPO71 N32 → UMA_CRT_CLK

VGA_DAC_RSET K31 → VGA_DAC_RSET R366 1 2 715_0402_1%

VGA_DAC

AUX_VGA_CH_P V28 → ML_VGA_AUXP

AUX_VGA_CH_N V29 → ML_VGA_AUXN

AUXCAL U28 → AUXCAL R364 1 2 100_0402_1% +VDDAN_11_ML

ML_VGA_L0P T31 → ML_VGA_TXP0

ML_VGA_L0N T33 → ML_VGA_TXN0

ML_VGA_L1P T29 → ML_VGA_TXP1

ML_VGA_L1N T28 → ML_VGA_TXN1

ML_VGA_L2P R32 → ML_VGA_TXP2

ML_VGA_L2N R30 → ML_VGA_TXN2

ML_VGA_L3P P29 → ML_VGA_TXP3

ML_VGA_L3N P28 → ML_VGA_TXN3

VGA_MAINLINK

ML_VGA_HPD/GPIO229 C29 → FCH_CRT_HPD

FCH_CRT_HPD

AH16 / AM15 / AJ16 FANOUT0/GPIO52 / FANOUT1/GPIO53 / FANOUT2/GPIO54

HW MONITOR

VIN0/GPIO175 N2 GPIO175

VIN1/GPIO176 M3 GPIO176

VIN2/SDATI_1/GPIO177 L2 GPIO177

VIN3/SDATO_1/GPIO178 N4 GPIO178

VIN4/SLOAD_1/GPIO179 P1 SLP_CHG_CB1

VIN5/SCLK_1/GPIO180 P3 SLP_CHG_CB0

VIN6/GBE_STAT3/GPIO181 M1 PANEL_SEL

VIN7/GBE_LED3/GPIO182 M5 GPIO182

PW_CLEAR# → JPW @ 1 2

PW_CLEAR# AK15 / AN16 / AL16 FANIN0/GPIO56 / FANIN1/GPIO57 / FANIN2/GPIO58

PW_CLEAR# → T20

ODD_PWR → ODD_PWR K6 TEMPIN0/GPIO171

GPIO172 K5 TEMPIN1/GPIO172

SM_EN K3 TEMPIN2/GPIO173

+3VALW_FCH → R437 1 2 10K_0402_5% FCH_ALERT# M6 TEMPIN3/TALERT#/GPIO174

AG16 / AH10 / A28 / G27 / L4 NC1 / NC2 / NC3 / NC4 / NC5

2180755042A13HUDSON_FCBGA656

BOLTONR1@

+3VS → R439 269@ 10K_0402_5% SM_EN → R438 10K_0402_5%

RP11 GPIO172 GPIO182 10K_8P4R_5%

SM_EN	BIOS SETUP	SPK TYPE
1	S&M OPTION	HARMAN KARDON
0	NO	NO HARMAN

Place JPW under DDR Door

4M Byte

+3VALW_FCH → C498 1 2 0.1U_0402_16V4Z

U13

VCC 8 VSS 4

W 3

HOLD 7

S 1

C 6

D 5

Q 2

EC_CS0# → R88 2 885@ 1 33_0402_5% FCH_SPI_CS1#

EC_SCK → R107 2 885@ 1 33_0402_5% FCH_SPI_CLK

EC_SDI → R110 2 885@ 1 33_0402_5% FCH_SPI_MOSI

FCH_SPI_MISO 2 885@ 1 33_0402_5% R106 → EC_SDIO

MX25L3206EM2I-12G_SO8

SA00003K800

SA00004LI00

Socket PN: SP07000F500/SP07000H900

+3VALW_FCH → R285 10K_0402_5% IEDP@

PANEL_SEL → R294 10K_0402_5% LVDS@

HDMI_EN# (Internal 8.2K PU)

HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

For EMI request

FCH_SPI_CLK_R → R118 2 1 10_0402_5% EMI@ → C508 1 2 10P_0402_50V8J EMI@

If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed

+3VALW_FCH → FCH_SPI_CS1# R113 1 885@ 2 10K_0402_5%

+3VS → UMA_CRT_DATA R455 2.2K_0402_5%

+3VS → UMA_CRT_CLK R462 2.2K_0402_5%

UMA_CRT_R R367 150_0402_1%

UMA_CRT_G R368 150_0402_1%

UMA_CRT_B R369 150_0402_1%

+FCH_VDDAN_33_DAC_R → FCH_CRT_HPD R365 10K_0402_5%

RP9 GPIO175 GPIO178 GPIO176 GPIO177 10K_8P4R_5%

+3VALW_FCH → SLP_CHG_CB0 R134 @ 10K_0402_5%

+3VALW_FCH → SLP_CHG_CB1 R151 @ 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

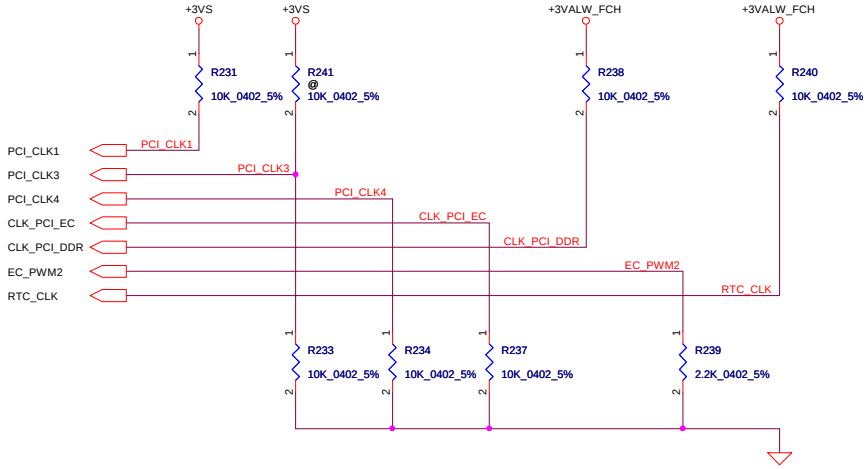
Title: Hudson-M3-SATA/GBE/HWM

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 25 of 51

STRAP PINS

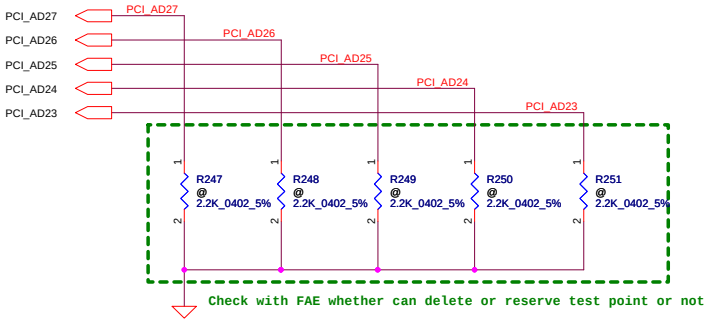
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

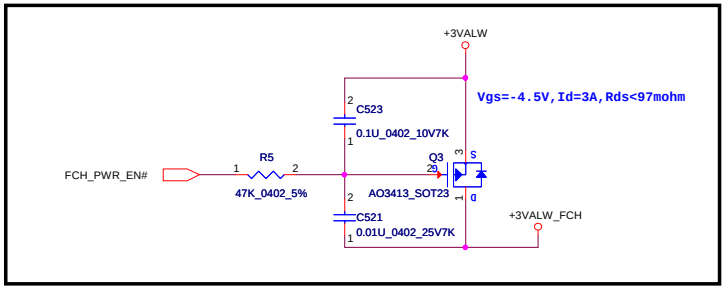


DEBUG STRAPS

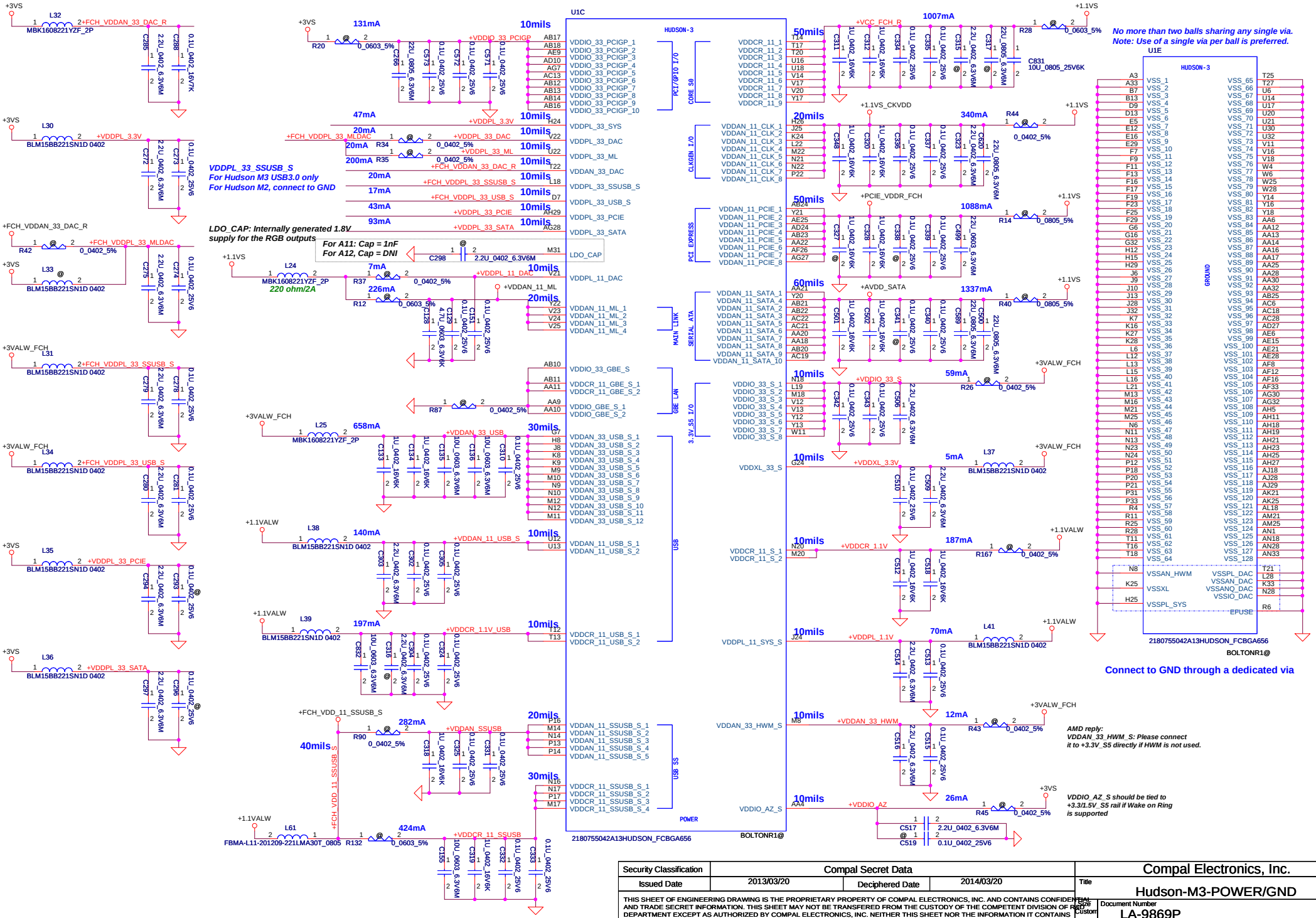
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





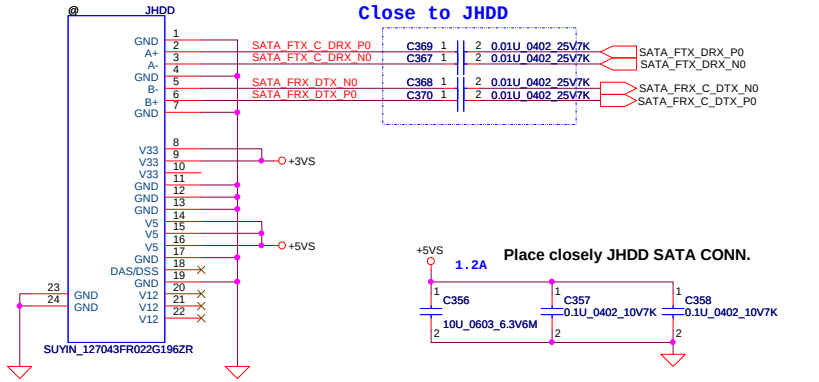
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date 2014/03/20	Title: Hudson-M3-STRAP
			Size: Custom; Document Number: LA-9869P; Rev: 1.0
			Date: Wednesday, March 20, 2013; Sheet 26 of 51



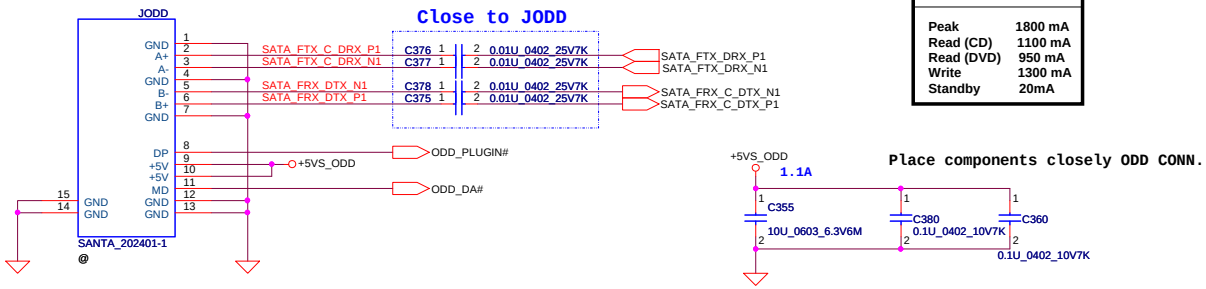
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.			
Title: Hudson-M3-POWER/GND			
Size: Custom	Document Number: LA-9869P		Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 27 of 51		

SATA HDD Conn.

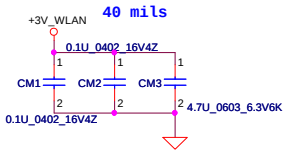


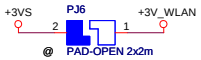
SATA ODD Conn



Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

Slot 1 Half PCIe Mini Card-WLAN



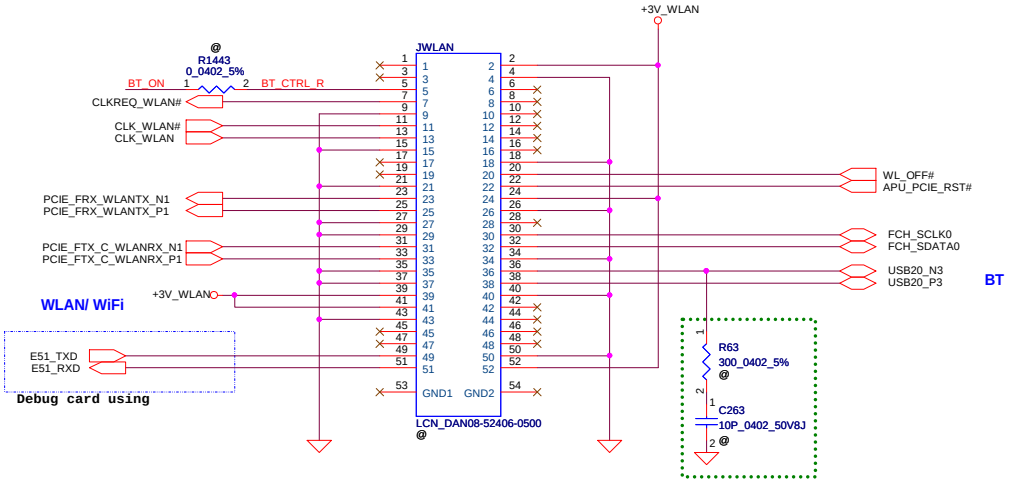


Short for WIFI

For isolate BT_CTRL and Compal Debug Card.

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

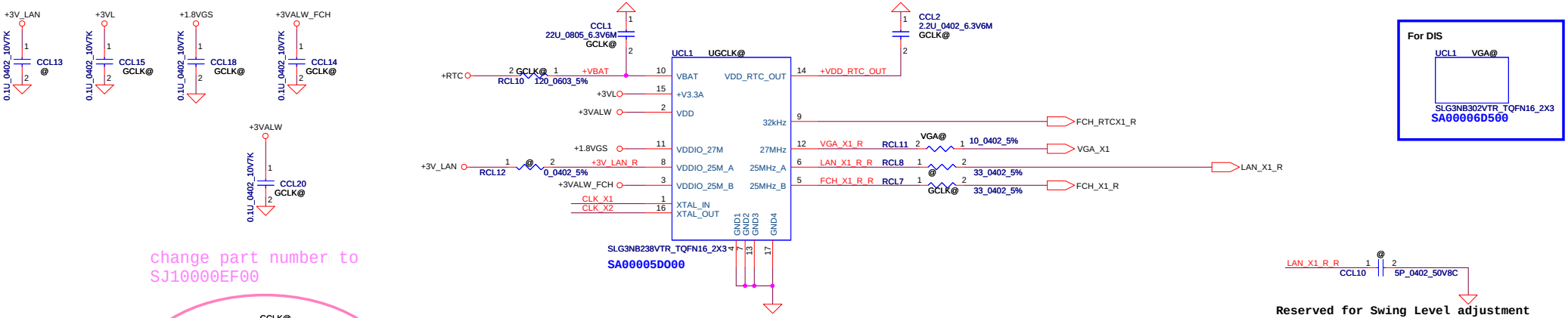
Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

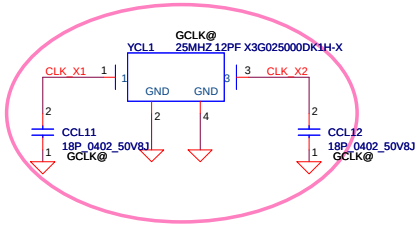
Size | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 28 of 51

Green Clock Generator



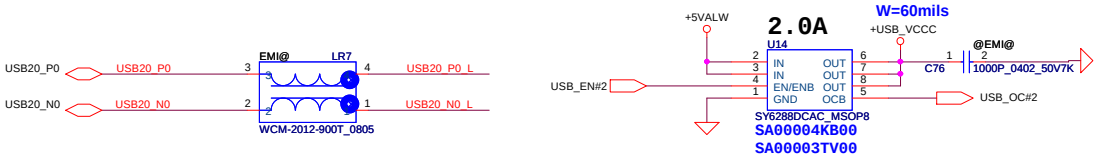
change part number to
SJ10000EF00



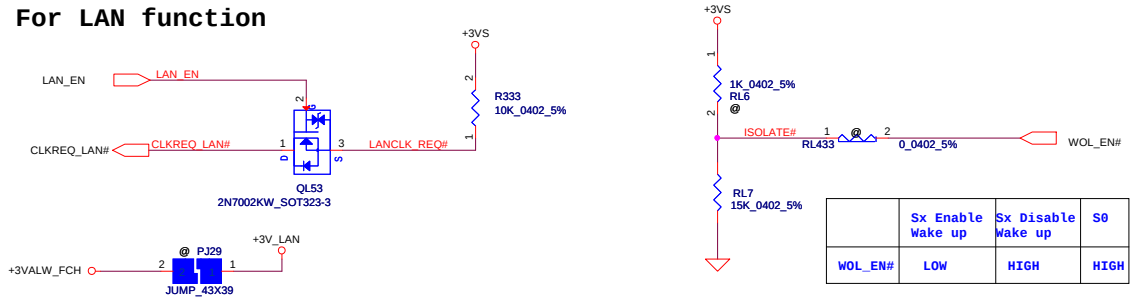
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Title	PCIe-WLAN/GCLK		
Size	Document Number		Rev
	LA-9869P		1.0
Date:	Wednesday, March 20, 2013	Sheet	29 of 51

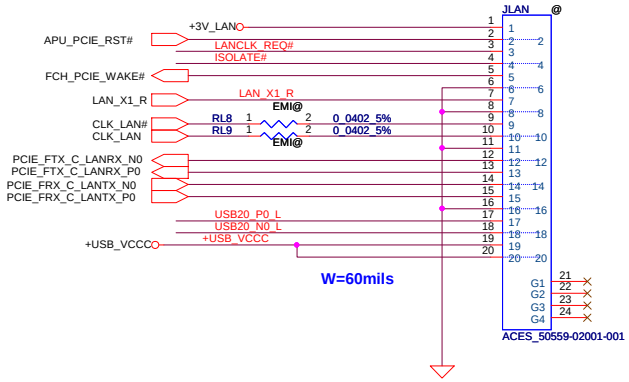
Left USB 2.0 x 1



For LAN function



	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

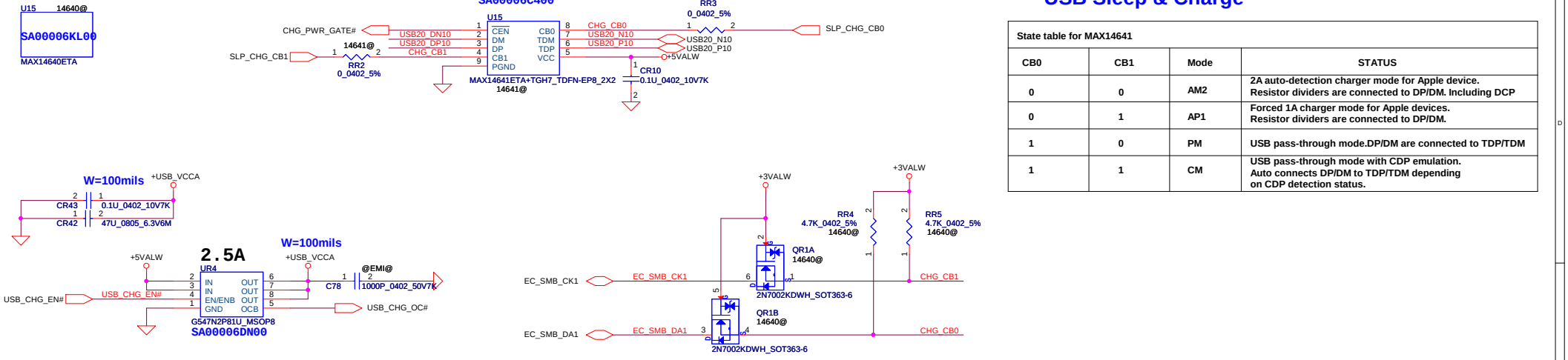
Title: PCIe-LAN-RTL8105E/8111F

Size: Custom | Document Number: LA-9869P | Rev: 1.0

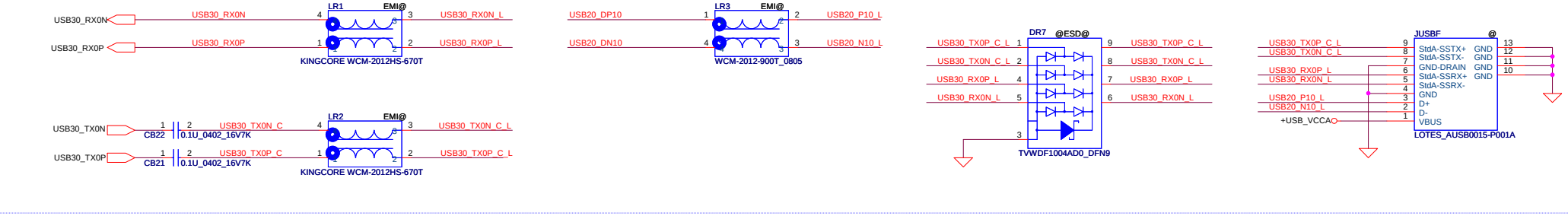
Date: Wednesday, March 20, 2013 | Sheet 30 of 51

USB Sleep & Charge

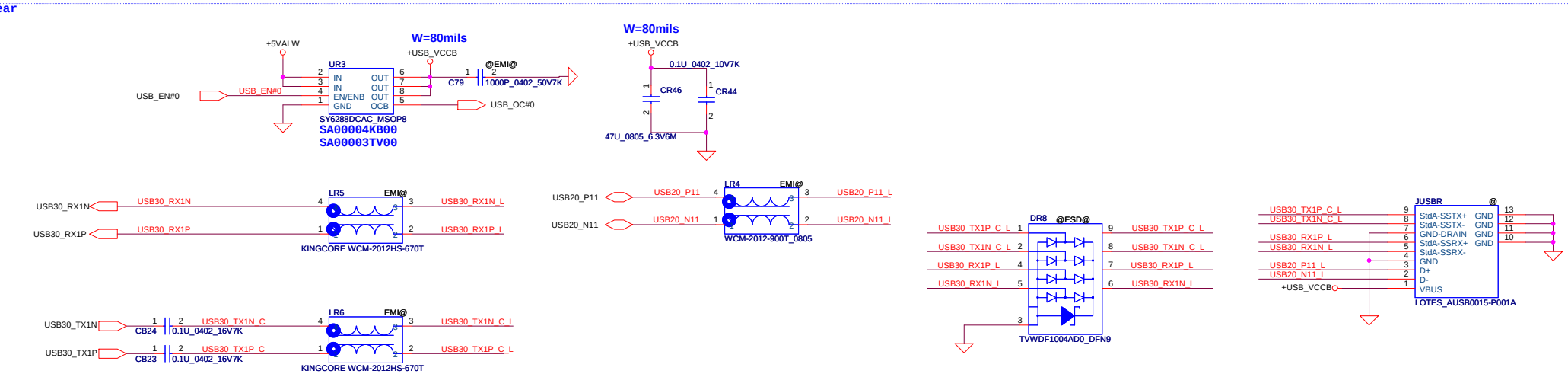
State table for MAX14641			
CB0	**CB1**	**Mode**	**STATUS**
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



Front with S&C



Rear



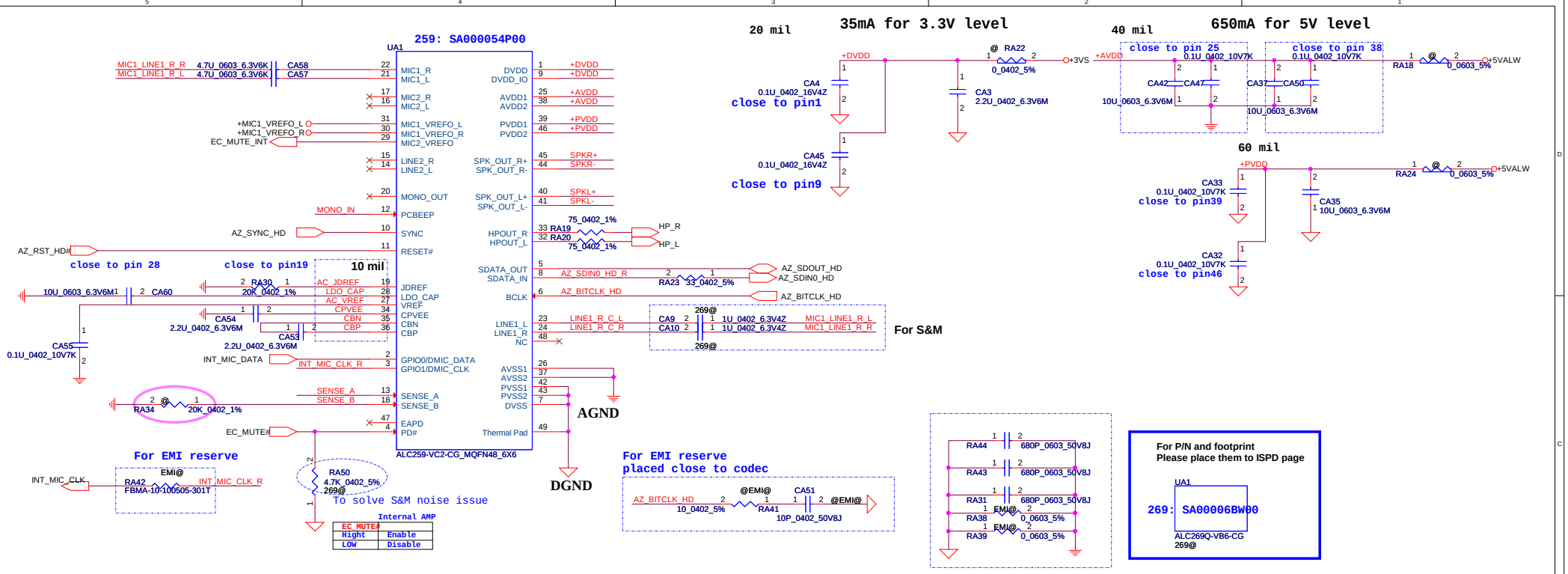
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

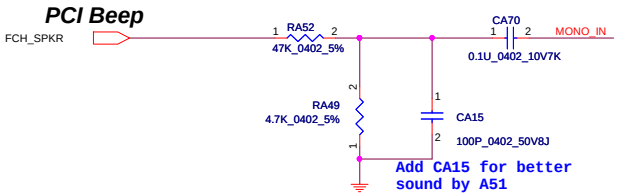
Title: **USB3.0**

Size: Custom | Document Number: **LA-9869P** | Rev: 1.0

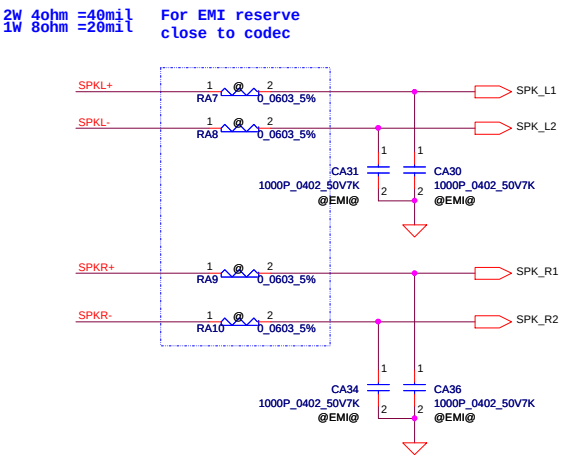
Date: Wednesday, March 20, 2013 | Sheet 31 of 51



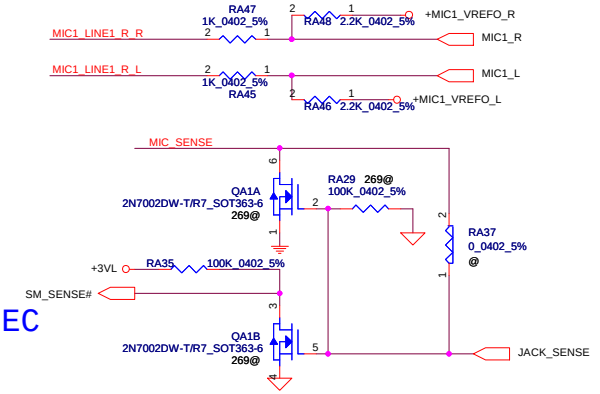
Beep sound



SPK



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: **Cover Sheet**

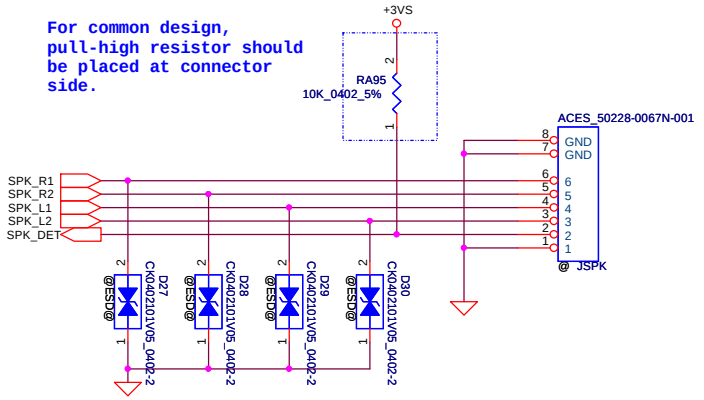
Size	Document Number	Rev
Custom		1.0

Date: Wednesday, March 20, 2013 | Sheet 32 of 51

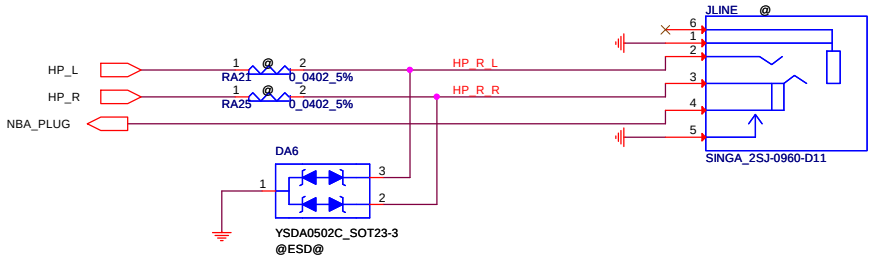
SPK CONN.

	Non-Harman detection	
SPK_DET0	0	ONKYO
	1	Non-Brand

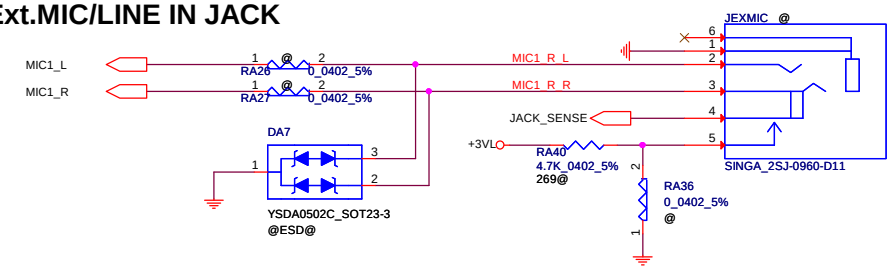
Please check SPK_DET pull high 10K to +3VS



HeadPhone/LINE Out JACK

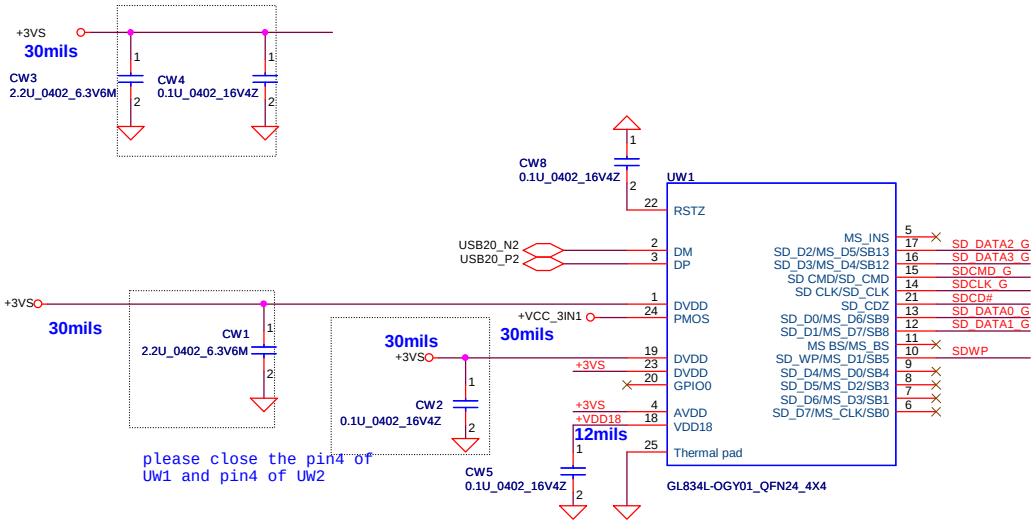


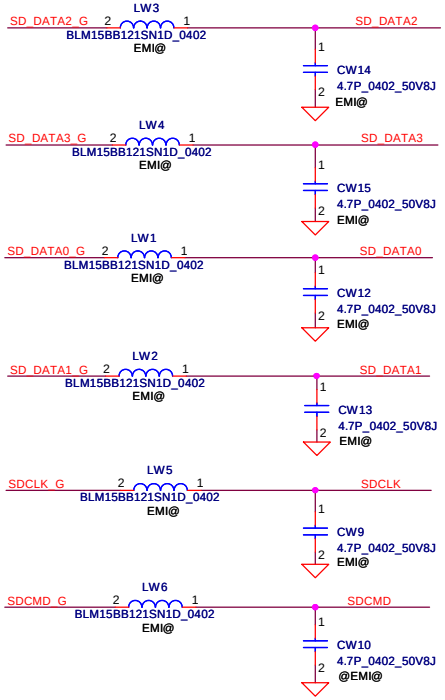
Ext.MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

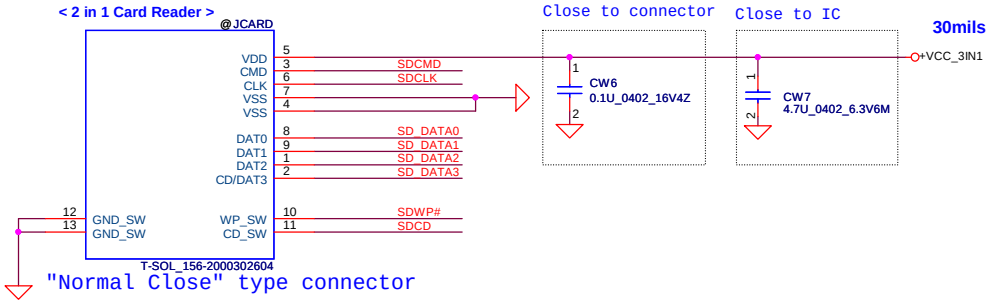
Compal Electronics, Inc.			
Title	CR & Audio Conn.		
Size	Document Number	LA-9869P	Rev 1.0
Date:	Wednesday, March 20, 2013	Sheet 33 of 51	





	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

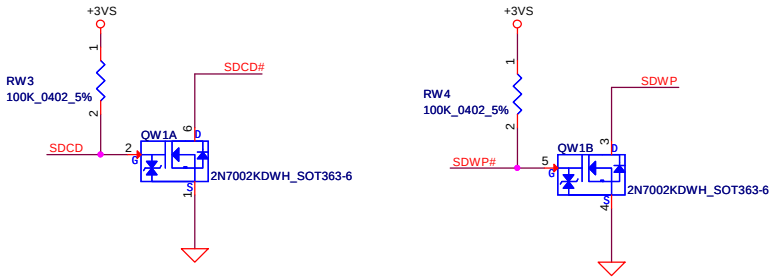
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



"Normal Close" type connector

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



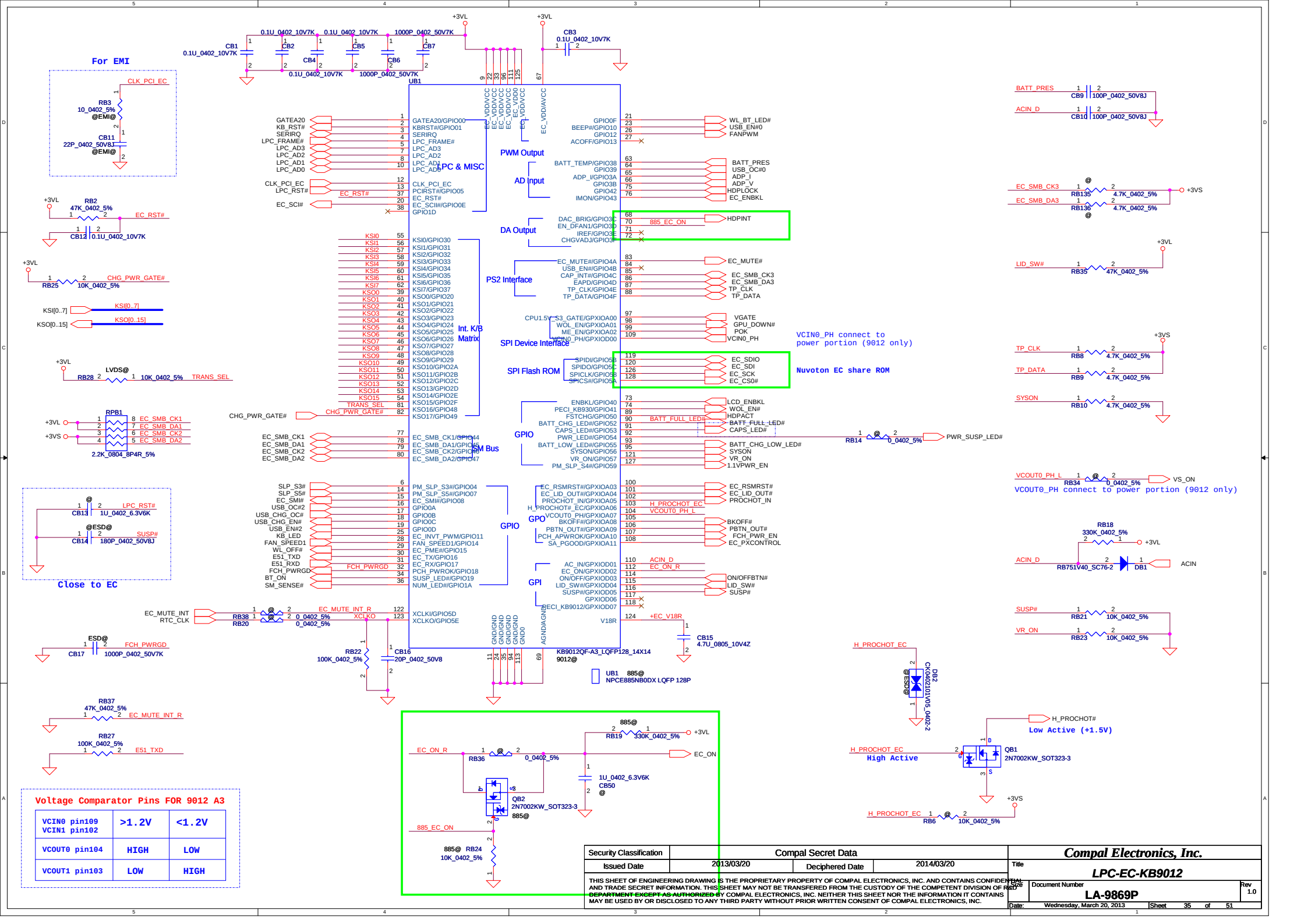
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: **USB-CardReader GL834L/RTS5170**

Size	Document Number	Rev
B	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 34 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

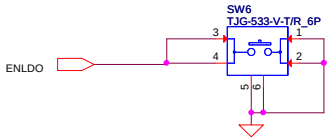
Compal Electronics, Inc.

Title: LPC-EC-KB9012

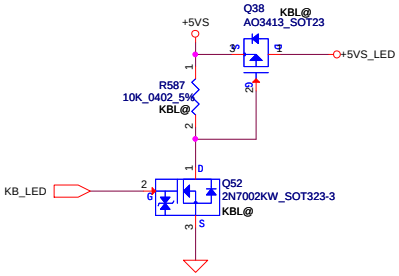
Size: | Document Number: LA-9869P | Rev: 1.0

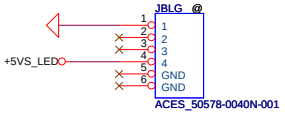
Date: Wednesday, March 20, 2013 | Sheet 35 of 51

Battery Reset

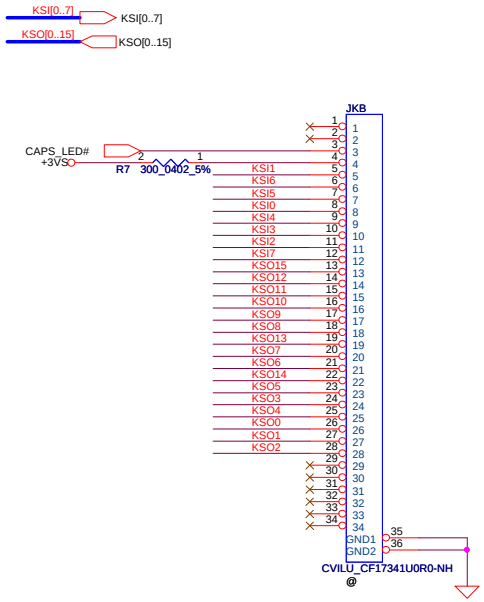


Keyboard LED

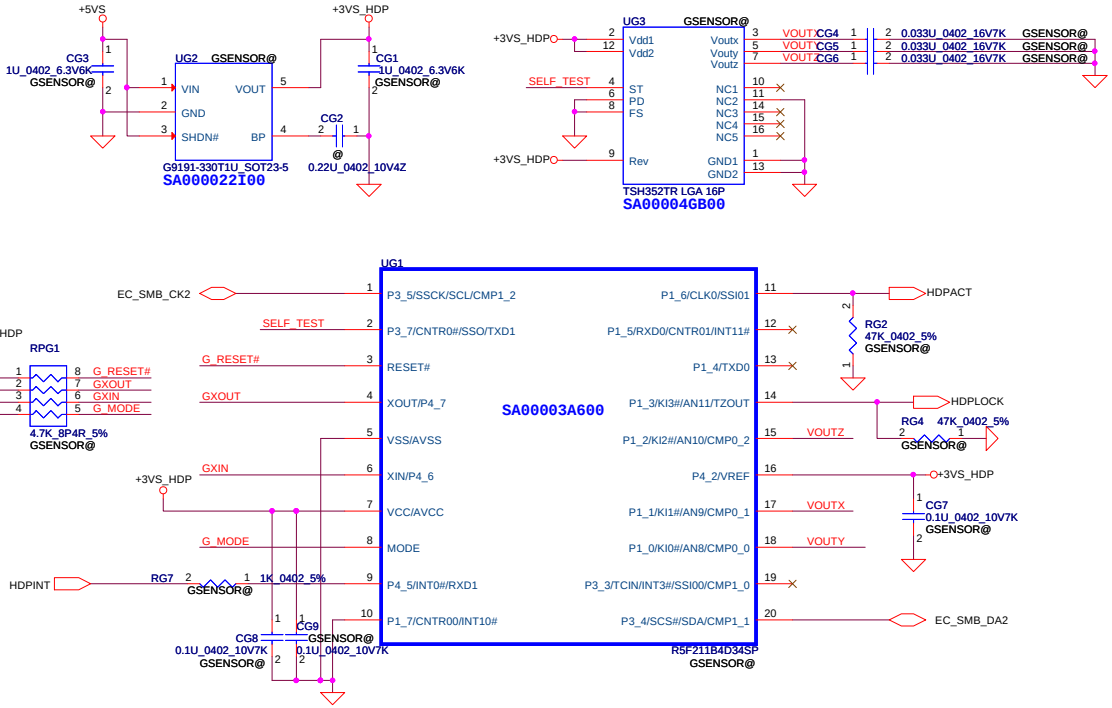




NEW KEYBOARD CONN.

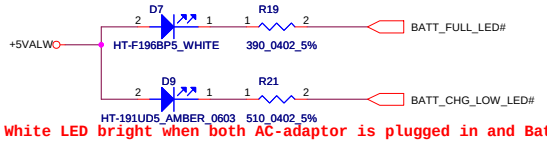


G-SENSOR



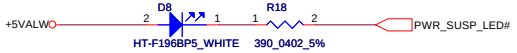
LED

BATT CHARGE(Blink) /FULL LED



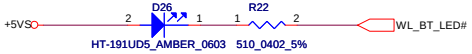
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED(Blink)



White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN LED



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

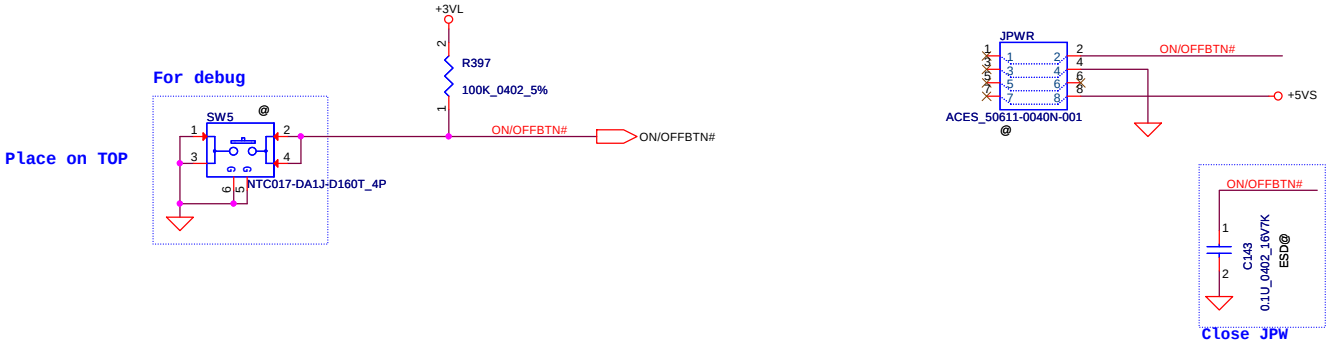
Compal Electronics, Inc.

Title: Debug/KB

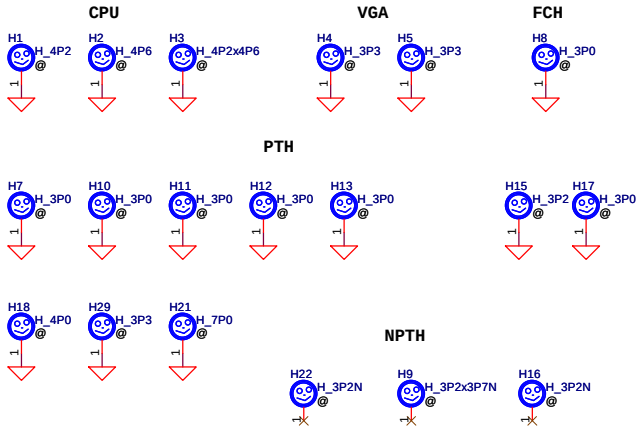
Size | Document Number: LA-9869P | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 36 of 51

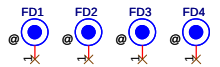
Conn.



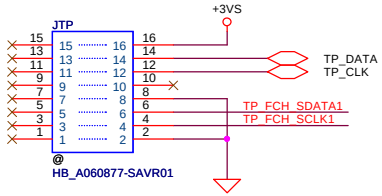
Screw Hole

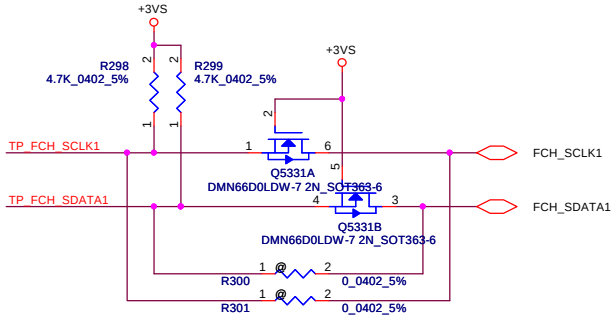


PCB Fedical Mark PAD

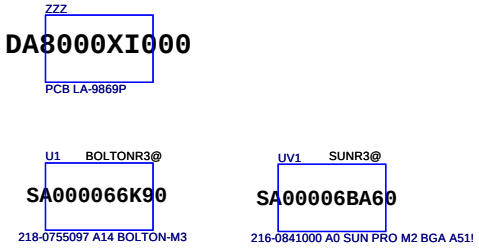


Touchpad Connector

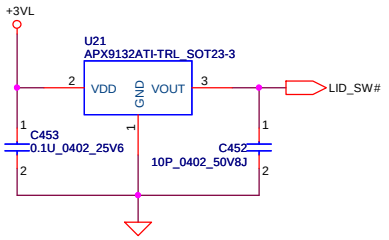


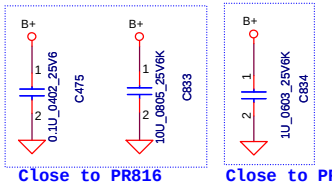


ISPD



Lid SW

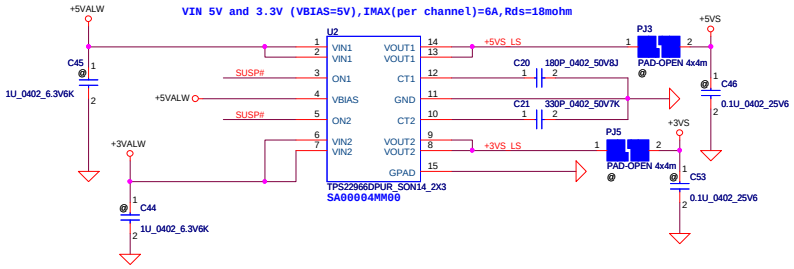


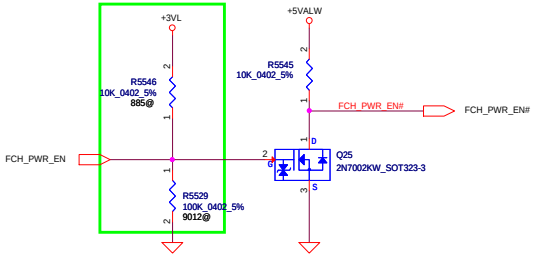


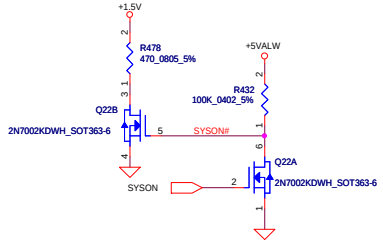
Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

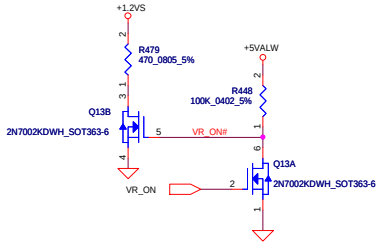
Title	TP/HDD LED/Screw		
Size	Document Number		Rev
	LA-9869P		1.0
Date:	Wednesday, March 20, 2013	Sheet	37 of 51

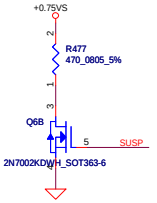
+5VALW TO +5VS
+3VALW TO +3VS
Load switch

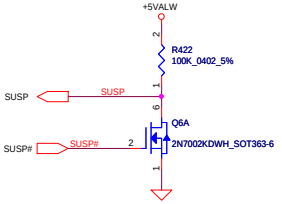




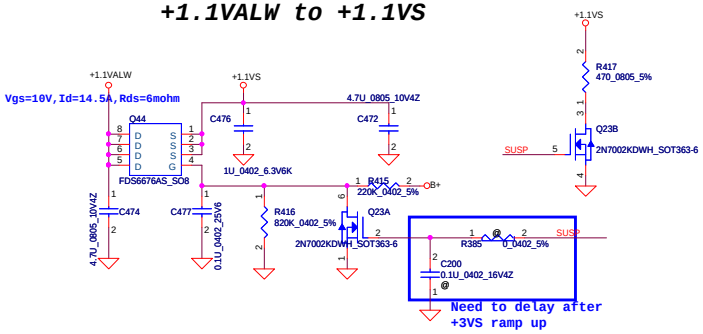




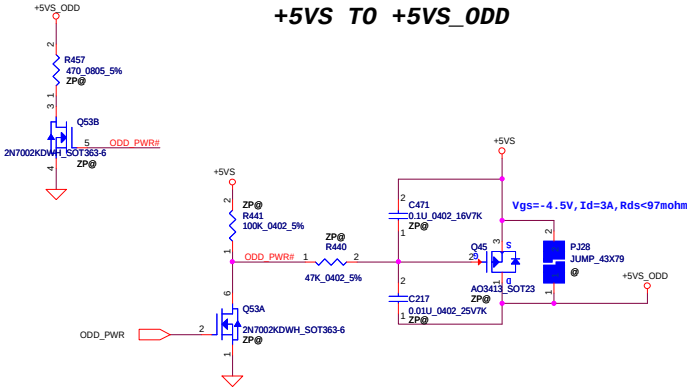




+1.1VALW to +1.1VS



+5VS TO +5VS_ODD



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: **DC-DC INTERFACE**

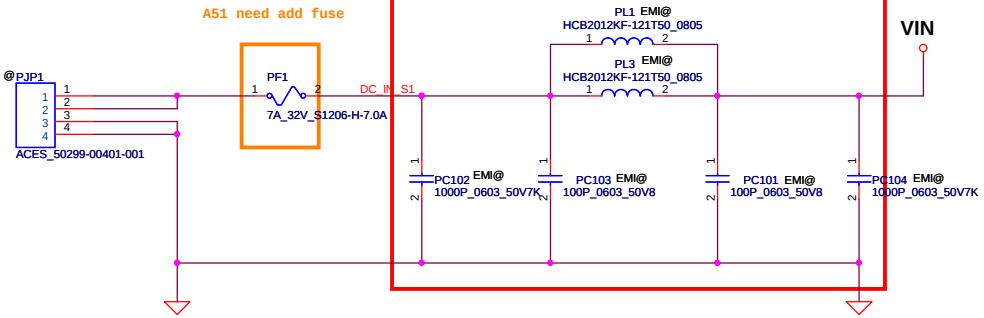
Size	Document Number	Rev
	LA-9869P	1.0

Date: Wednesday, March 20, 2013 | Sheet 38 of 51

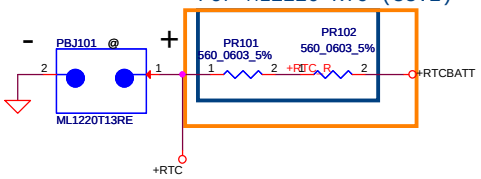
Other component (37.1)

A51 need add fuse

EMI Part (47.1)



For ML1220 RTC (38.2)



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

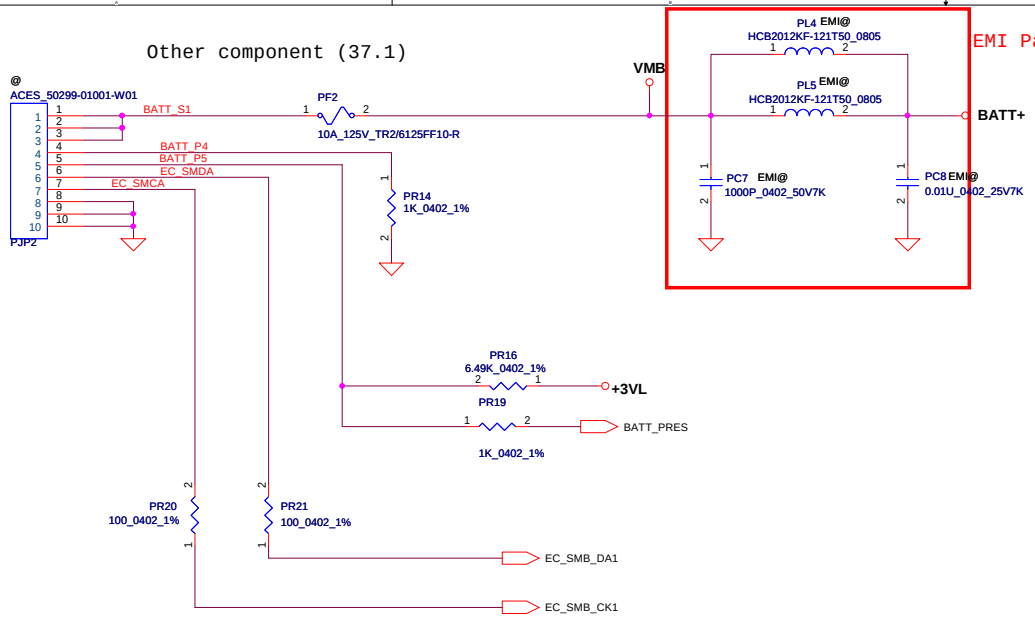
Compal Electronics, Inc.

Title: *DCIN/PRECHARGE*

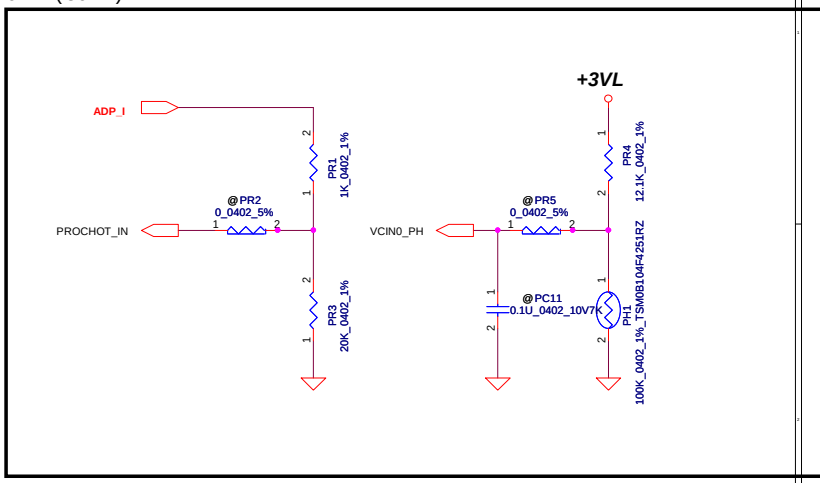
Size	Document Number	Rev
Custom	*LA-9869P*	1.0

Date: | Sheet 39 of 51

Other component (37.1)



OTP (39.7)



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: LA-9869P | Rev: 1.0

Date: | Sheet 40 of 51

Charger controller (40.1), Support component (40.2)

for reverse input protection

PQ209 SSM3K7002FU_SC70-3
PR225 1M_0402_5%
PR226 3M_0402_5%

EMI Part (47.1)

VIN
TPCA 8057 PQ203
PQ205 SI7716ADN-T1-GE3_POWERPAK8-5
P1
P2
B+
PR211 0.01_1206_1%
PL201 EMI@ 1UH_NRS4018T1R0NDGJ_3.2A_30%
PC211 10U_0805_25V6K
PC213 10U_0805_25V6K
PC214 @EMI@ 2200P_0402_25V7K
PC230 2200P_0402_50V7K
PC231 0.1U_0402_25V6
PC234 0.01U_0402_50V7K
PC236 0.1U_0402_25V6
PC238 0.1U_0402_25V6
PC235 0.1U_0402_25V6
PD230 BAS40CW_SOT323-3
PR228 10_1206_1%
PC237 0.047U_0402_25V7K
PD231 RB751V-40_SOD323-2
PR229 2.2_0603_5%
PC239 1U_0603_25V6K
PC205 1U_0603_25V6K
PR234 4.12K_0603_1%
PR235 4.12K_0603_1%
BQ24725_ACDRV_1
BQ24725_VCC
BQ24725_LX
DH_CHG
BQ24725_BST
BQ24725_REGN
BQ24725_ACP
BQ24725_ACN

S TR SI7716ADN PQ207
BQ24725_BATDRV_1
PR233 4.12K_0603_1%

PQ201 AON7408L
DH_CHG
PR210 @ 0_0603_5%

PL202 4.7UH_ETQP3W4R7WFN_5.5A_20%
PR227 0.01_1206_1%
BATT+
BQ24725_LX
CHG
CSOP1
CSON1
PC240 0.1U_0402_25V6
PC241 0.1U_0402_25V6
PC221 @ 10U_0805_25V6K
PC222 10U_0805_25V6K
PC223 10U_0805_25V6K

PQ202 AON7406L
PR206 @EMI@ 4.7_1206_5%
PC206 @EMI@ 680P_0603_50V8J

PU200 BQ24725RGRR_QFN20_3P5X3P5
PAD
ACN
ACP
CMSRC
ACDRV
ACOK
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRP
SRN
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
PR236 10_0603_1%
PR237 6.8_0603_5%
PC242 0.1U_0603_16V7K
BQ24725_CMSRC
BQ24725_ACDRV
BQ24725_BATDRV
DL_CHG
SRP
SRN
CSOP1
CSON1

EMI Part (35.33)

+3VL
PR239 10K_0402_1%
+3VALW
ACIN
BQ24725_ILIM
PR241 357K_0402_1%
PR242 100K_0402_1%
PC243 0.01U_0402_25V7K

VIN
PR244 422K_0402_1%
PC244 0.1U_0402_25V6
PR245 66.5K_0402_1%
PC245 100P_0402_50V8J
@PR246 0_0402_5%
@PC246 0.1U_0402_10V7K
BQ24725_ACDET
EC_SMB_CK1
EC_SMB_DA1
ADP_I

VIN
PR247 309K_0402_1%
PR248 10K_0402_1%
ADP_V
PR249 47K_0402_1%
@PC247 0.1U_0402_10V7K

For A51 ADP_V function

Please locate the RC
Near EC chip
2011-02-22

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

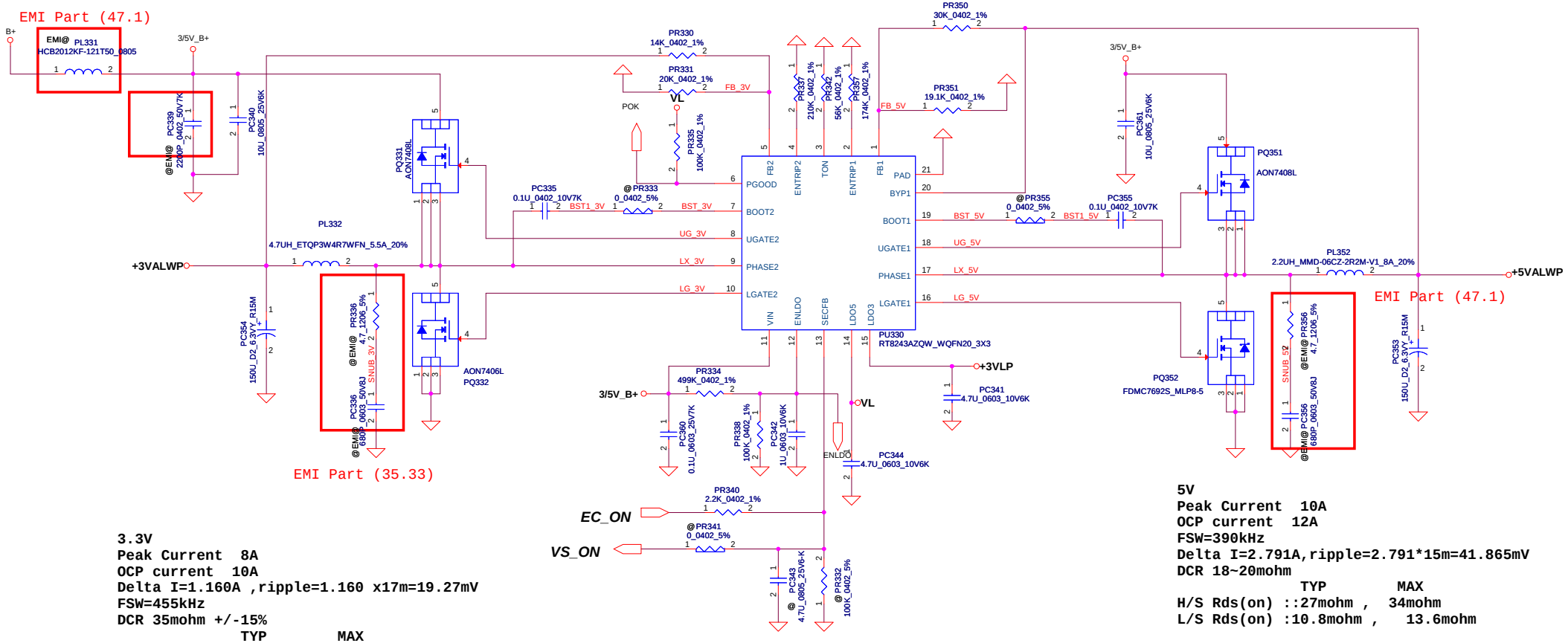
Title: CHARGER

Size: Custom | Document Number | Rev: 1.0

Date: | Sheet 41 of 51

3/5VALW controller (35.1), Support component (35.2)

5V_3.3V controller (35.1), Support component (35.2)



3.3V
Peak Current 8A
OCP current 10A
Delta I=1.160A ,ripple=1.160 x17m=19.27mV
FSW=455kHz
DCR 35mohm +/-15%

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:19mohm ,	23.5mohm

5V
Peak Current 10A
OCP current 12A
FSW=390kHz
Delta I=2.791A,ripple=2.791*15m=41.865mV
DCR 18~20mohm

	TYP	MAX
H/S Rds(on)	::27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

(100mA,20mils ,Via NO.= 1)

(8A,160mils ,Via NO.= 16)

(12A,240mils ,Via NO.= 24)

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

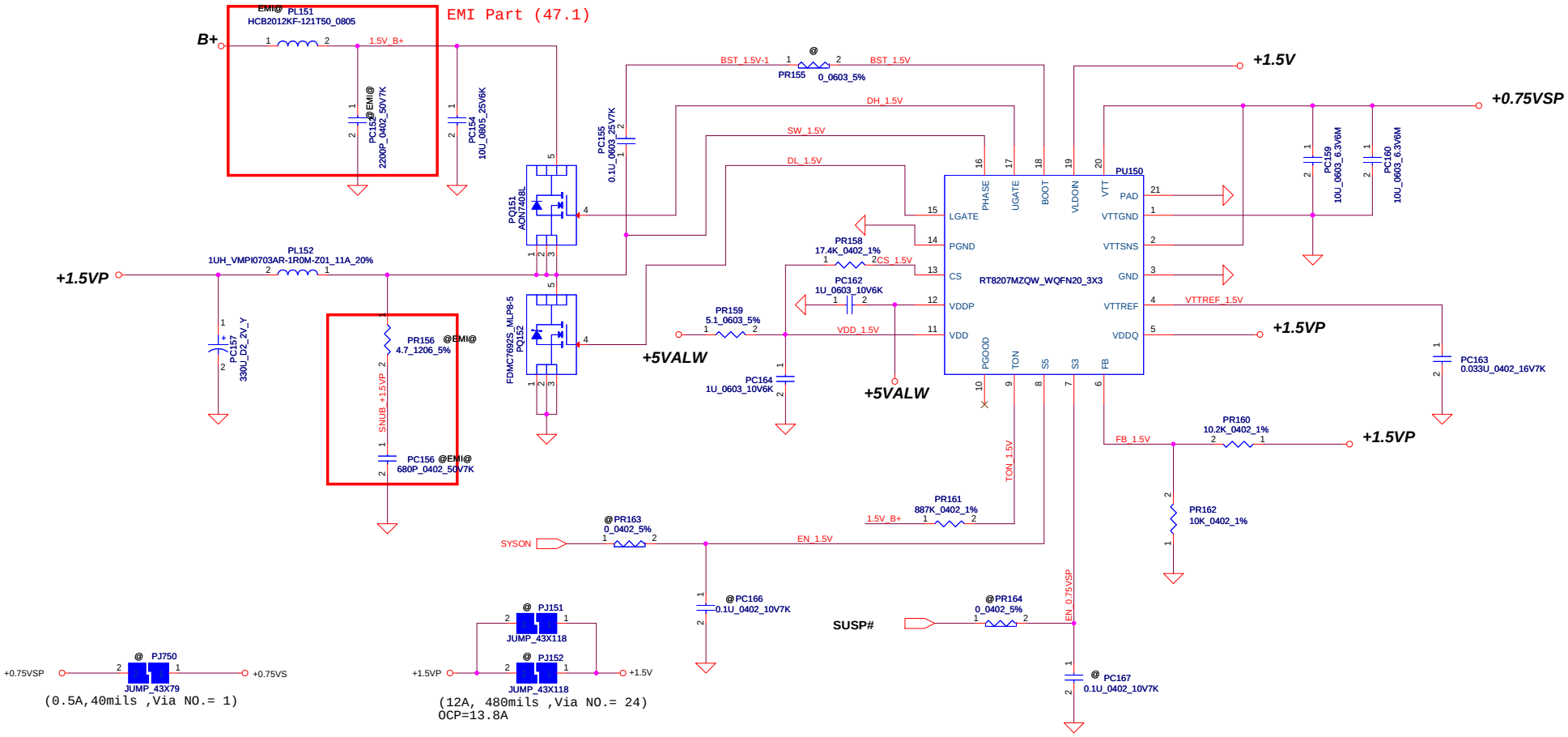
Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size: Custom | Document Number | Rev: 1.0

Date: | Sheet 42 of 51

DDR controller (35.3), Support component (35.4)



1.5V
Peak Current 12A
OCP current 13.34A
FSW=300kHz
DCR 8.3 ~ 10mohm

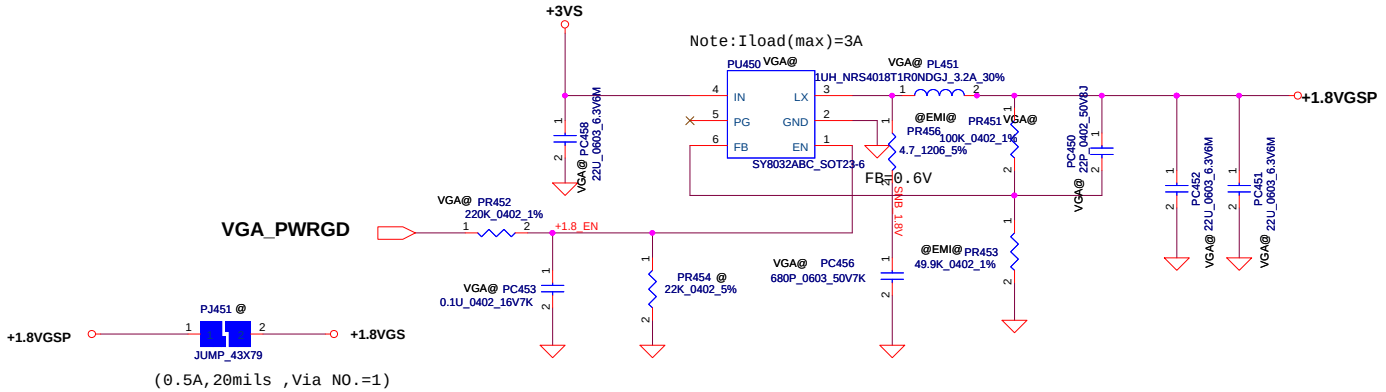
	TYP	MAX
H/S Rds(on)	**:27mohm ,**	**34mohm**
L/S Rds(on)	**:10.8mohm ,**	**13.6mohm**

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date 2014/03/20	Title: 1.5VP/0.75VSP/1.8VSP
			Size: Custom; Document Number: LA-9869P; Rev: 1.0
			Date: ; Sheet 43 of 51

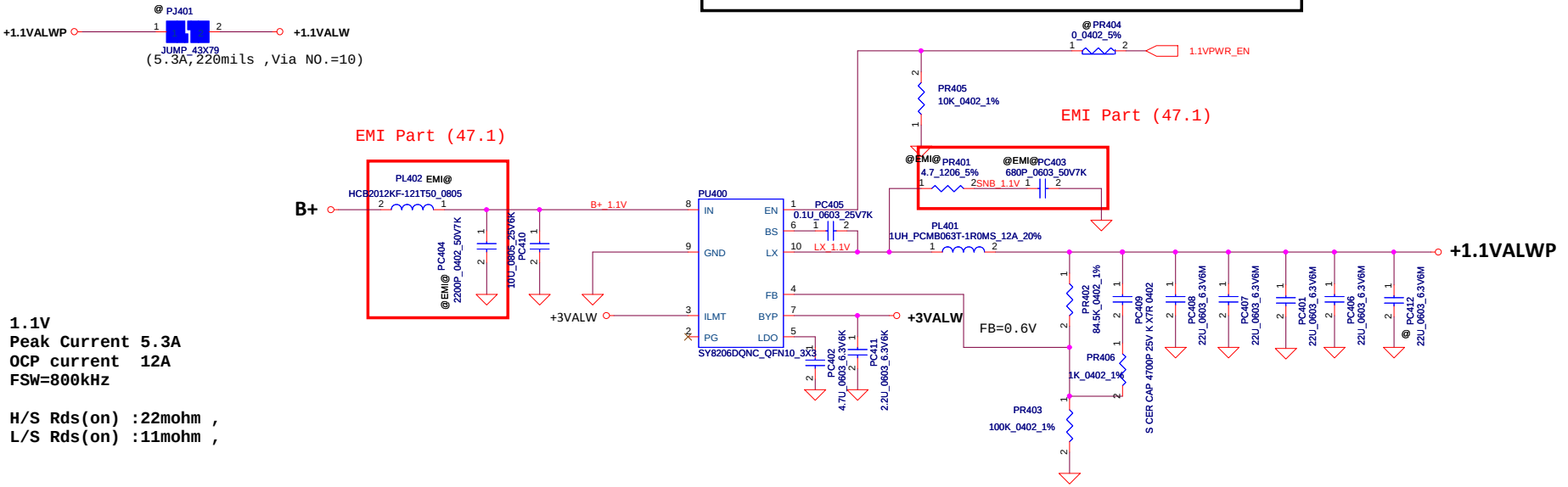
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 0.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

1.1V controller (35.27), Support component (35.28)



1.1V
Peak Current 5.3A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

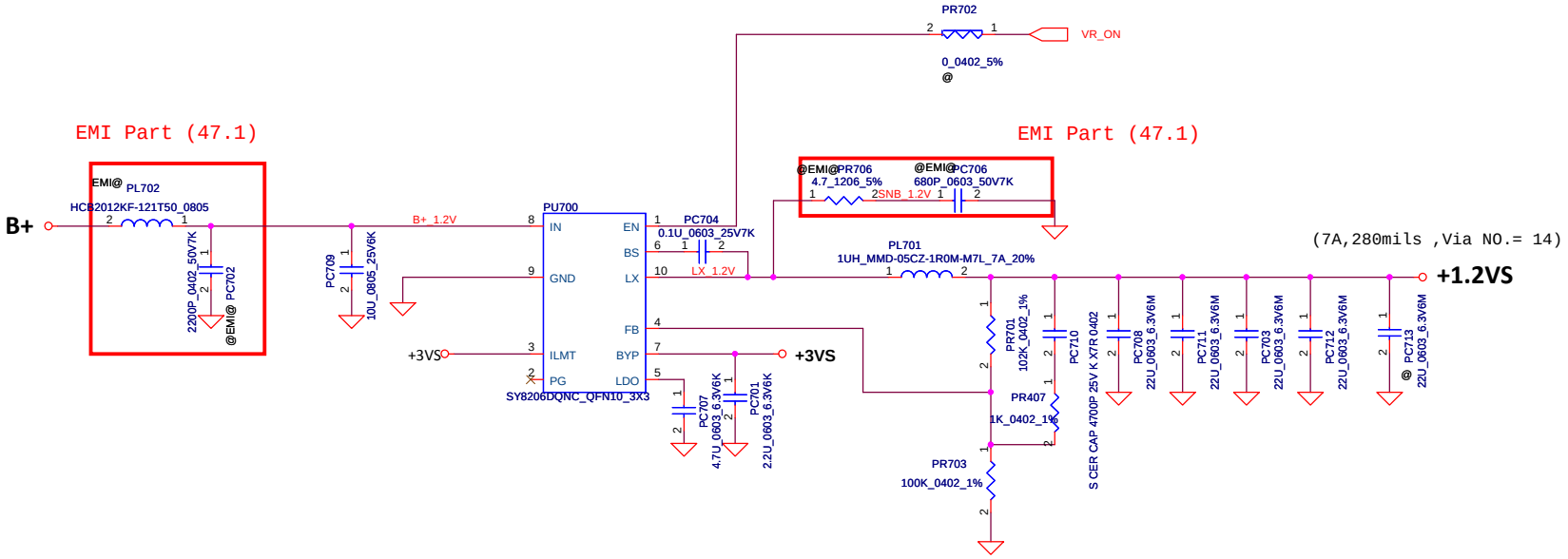
Compal Electronics, Inc.

Title: *+1.8VALWP*

Size: Custom | Document Number: *LA-9869P* | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 44 of 51

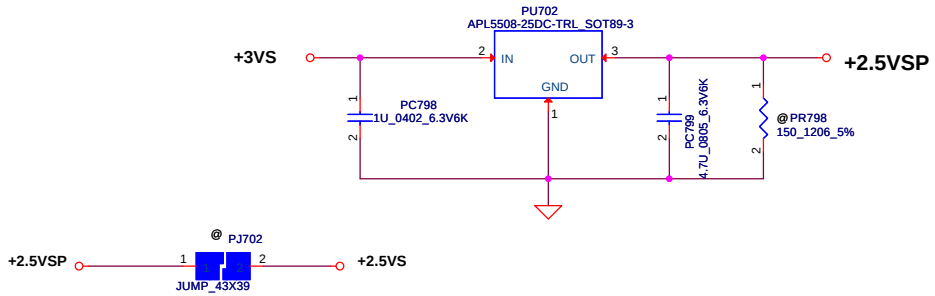
1.2V controller (35.7), Support component (35.8)



1.2V
Peak Current 7A
OCP current 12A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

2.5V controller (35.13), Support component (35.14)



Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	2014/03/20

Compal Electronics, Inc.

Title: +1.2VSP/+2.5VSP

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 45 of 51

CPU controller (36.1),Driver (36.2) Support component (36.3)

10/9 NB_Vdroop=-4m ohm

+APU_CORE
TDC (AB)22A (C)36A
EDC (AB)35A (C)50A
OCP current (AB)43.56A
Load line -2.1mV/A
FSW=450kHz
DCR 1mohm~1.2mohm

	TYP	MAX
H/S Rds(on) :	8.5mohm ,	11mohm
L/S Rds(on) :	2.6mohm ,	3.2mohm

10/9 OCP=50A for 35W(511 ohm)

+APU_CORE_NB
TDC (AB)22A (C)30A
EDC (AB)33A (C)40A
OCP current (AB)41.51A
Load line -4mV/A
FSW=450kHz
DCR 1mohm ~1.2mohm

	TYP	MAX
H/S Rds(on) :	7.4mohm ,	8.8mohm
L/S Rds(on) :	2.6mohm ,	3.1mohm

EMI Part (47.1)

EMI Part (47.1)

EMI Part (47.1)

EMI Part (35.33)

EMI Part (35.33)

10/9 OCP=62.5A for 35W (634)

10/9 CPU_Vdroop=-2.1m ohm

S IC ISL6277HRZ-TR5570 QFN 48P PWM

Security Classification	Compal Secret Data	
Issued Date	2013/03/20	Deciphered Date

Compal Electronics, Inc.

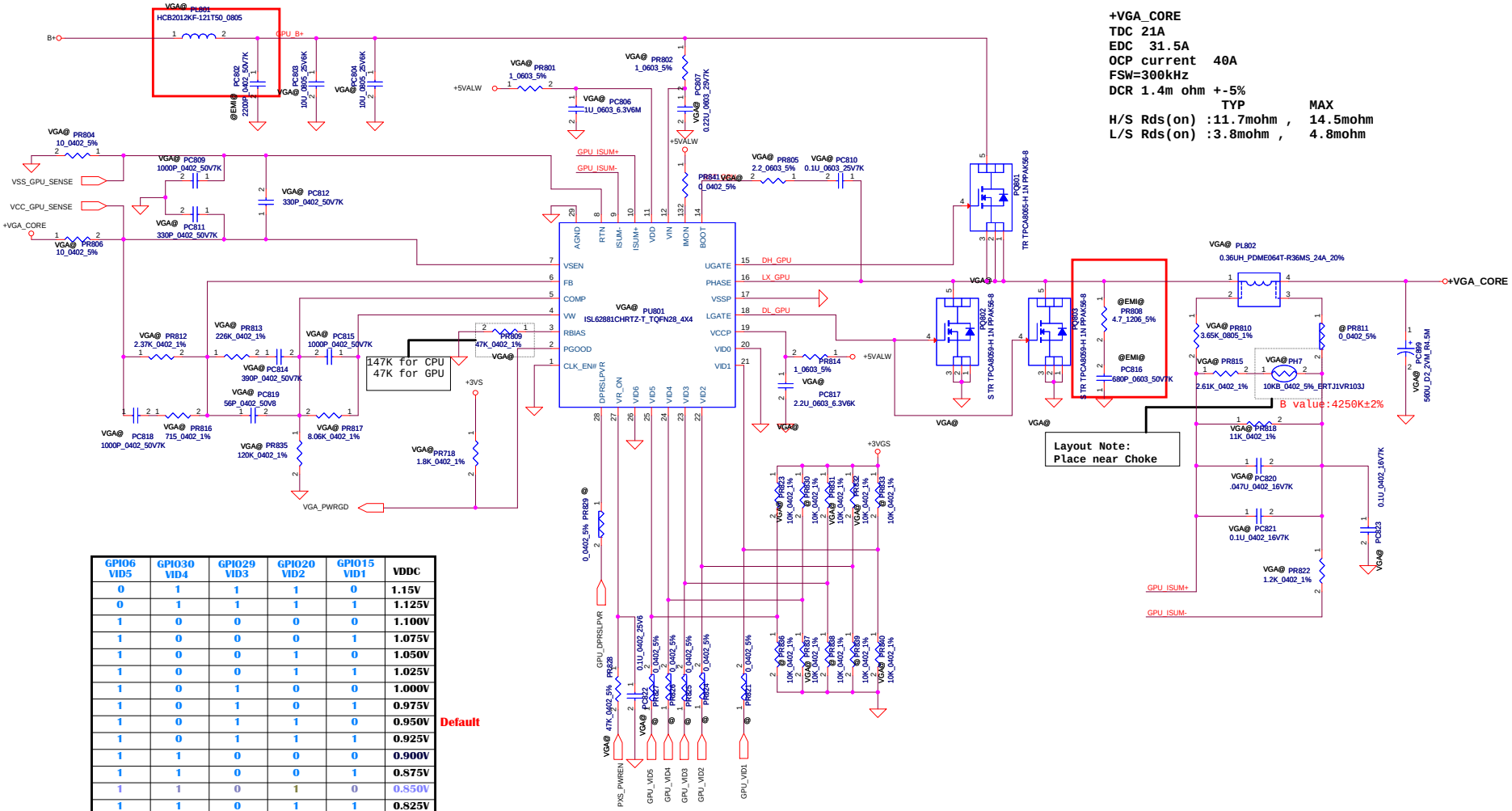
Title: +CPU_CORE/VDDNBP

Size	Document Number	Rev
Custom	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 46 of 51

VGA controller (43.1),Driver (43.2) Support component (43.3)

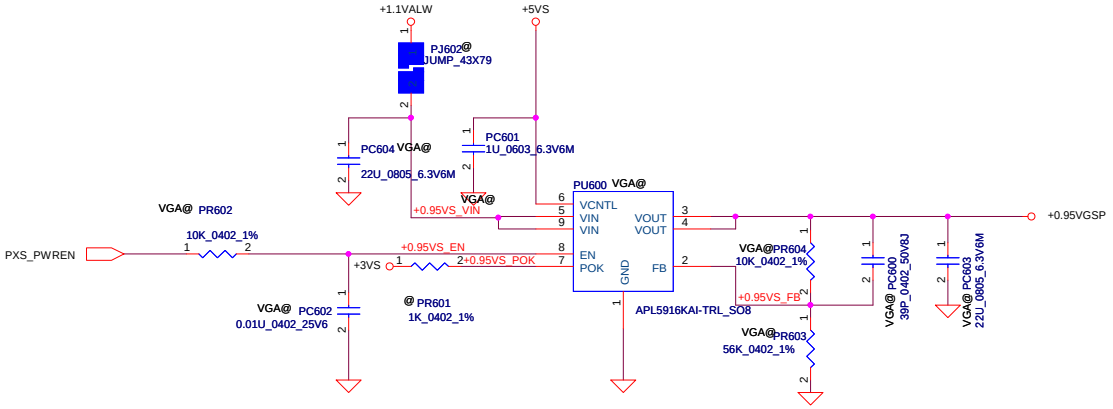
EMI Part (47.1)



GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC	
0	1	1	1	0	1.15V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	Default
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/20	Deciphered Date	2014/03/20
Title	+VPU_COREP		
Size C	Document Number LA-9869P		Rev 1.0
Date: Wednesday, March 20, 2013	Sheet 47 of 51		

0.95V controller (35.11), Support component (35.12)



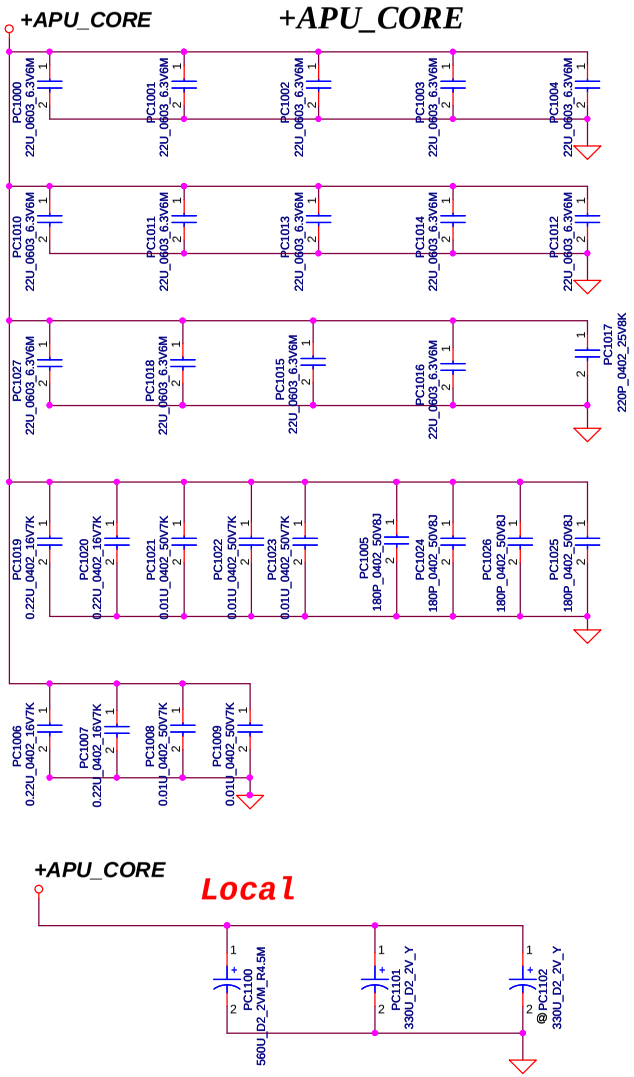
(4A,160mils ,Via NO.= 4)

0.95V
Peak Current 4A
OCP current 16A
FSW=800kHz

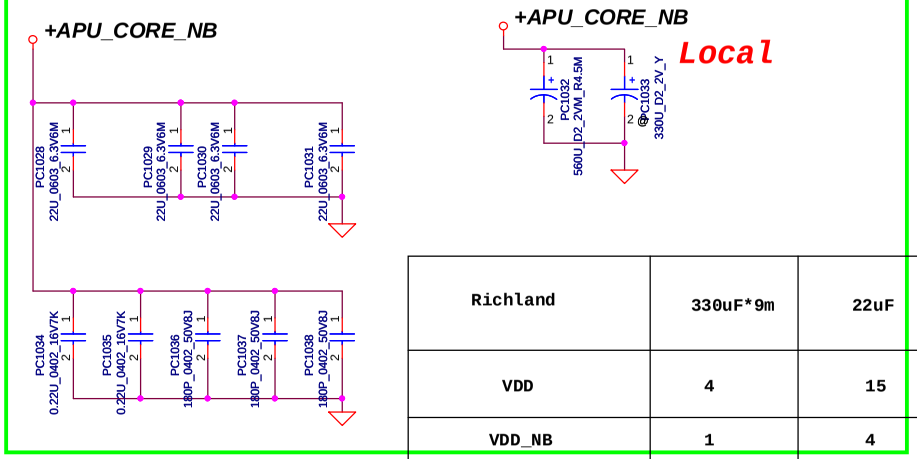
H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

Compal Electronics, Inc.		
Title: +1.5VPCIE/0.935V		
Size	Document Number: LA-9869P	Rev: 1.0
Date: Wednesday, March 20, 2013	Sheet 48 of 51	

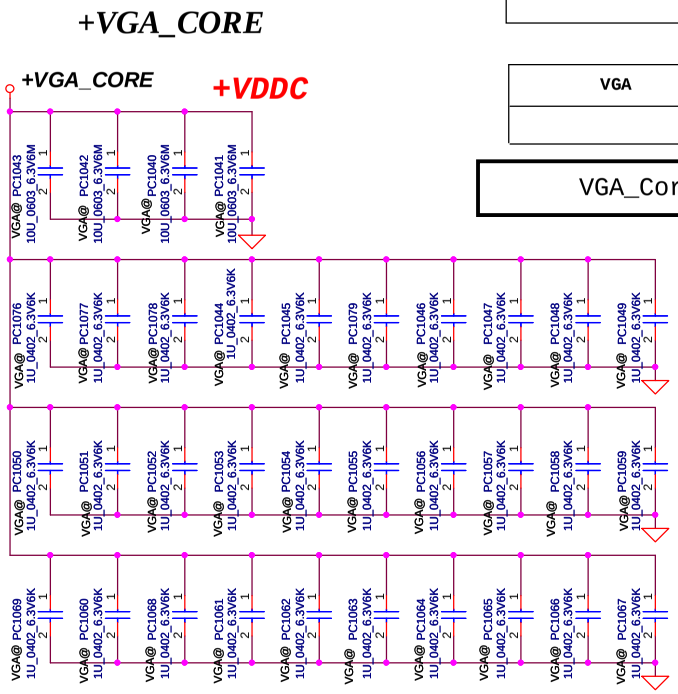
CPU_Core output CAP (Including MLCC) 36.4



GFX output CAP (Including MLCC) 36.5



Richland	330uF*9m	22uF	0.01u	0.22uF	180P
VDD	4	15	5	4	4
VDD_NB	1	4		2	3



VGA	560u x1	10u x 4	1u x30

VGA_Core output CAP (Including MLCC 43.9)

Security Classification	Compal Secret Data		
Issued Date	2013/03/20	Deciphered Date	

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	LA-9869P	1.0

Date: Wednesday, March 20, 2013 Sheet 49 of 51

Item Reason for change PG# Modify List Date Phase

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT–2012/11/28	P39-PWR-BATTERY CONN / OTP	change PF2 vandor for cost down plane	PWR
2	EVT–2012/11/28	P41-PWR-+3VALW/5VALW	change PR337 235K to 210K & PR5357 156k to 174k	PWR
3	EVT–2012/11/28	P41-PWR-+3VALW/5VALW	Delate PC351 add PC353 150u D2 cap	PWR
4	EVT–2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PC157 220u H=4.5mm to 330u D2 cap H=2mm	PWR
5	EVT–2012/11/28	P43-PWR_+1.8VSGP/+1.1VALWP	change PR158 16.2K to 17.4K	PWR
6	EVT–2012/11/28	P50-PWR-CPU_CORE	change the PC1101 560u to 330u	PWR

HW PIR (Product Improve Record)

VDKTE LA-9869P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/12/25

Item	Page	Date	Request	Solution
1)	21	2012/12/04a	For CRT undershoot issue	Add R66 & R67 for CRT issue.
2)	14	2012/12/04a	For VGA_CORE display	unomunt CR103.
3)	22	2012/12/13a	For EMI request	Change L8/L9/L10/L11 part number for EMI requesrt.
4)	34	2012/12/13a	For change EC PIN	Change 1.1VPWR_EN from pin 71 to pin 127 and USB_EN#0 from pin84 to pin 23.
5)	19	2012/12/14a	For LVDS translator	Delete all of RTD2132S components.
6)	31	2012/12/14a	For S&C port wake	Add CHG_PWR_GATE# on U15 pin 1 and connect to EC pin82.
7)	24	2012/12/17a	For leakage with PXS_PWREN	Change Power rail from +3VALW_FCH to +3VALW on R216 pin1
8)	07	2012/12/22a	For leakge	Delete R47, D18.
9)	24	2012/12/22a	For NV suggestion	Add R283 & Q30.
10)	34	2012/12/25a	For S&C port wake	Add RB25.

VDKTE LA-9869P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3
GERBER-OUT DATE: 2013/02/04

Item	Page	Date	Request	Solution
1)	24	2013/01/21a	For AMD suggestion	Update R288/R289 from 10K to 2.2K.
2)	22	2013/01/21a	For HDMIleakage issue	Change R571 to +3VS power rail.
3)	34	2013/01/21a	For Audio noise	Add EC_MUTE_INT (GPIO5D) and add RB38(0 ohm) and RB37 (4.7K PD)
4)	20	2013/01/21a	For layout routing	SWAP L56.
5)	20	2013/01/21a	For EMI request	Add R155/156.
6)	13	2013/01/28a	For Safety	Add GPU_DOWN# connect to EC.
7)	25	2013/01/29a	For EMI request	Add C508(10P)/R118(0 ohm) with FCH_SPI_CLK_R.
8)	33	2013/01/30a	For ESD request	Reserve D27~D30 on SPK.
9)	07	2013/01/30a	For ESD request	Reserve D31 on APU_PROCHOT#.
10)	20	2013/01/30a	For ESD request	Add D32 on Int mic clk/data and USB.
11)	34	2013/01/30a	For ESD request	Reserve DB2 on H_PROCHOT_EC.
12)	36	2013/01/31a	For move JTP	SWAP JTP
13)	24	2013/02/01a	For ESD request	Add 1000p C505 on FCH_PWRGD.
14)	34	2013/02/01a	For ESD request	Add 1000p CB17 on FCH_PWRGD.
15)	34	2013/02/04a	For PWR	Add GPIO pin 99 of EC for power.