Compal Confidential

C5PRH MB Schematic Document

LA-E921P

Rev:1.A

2017.03.29

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.		
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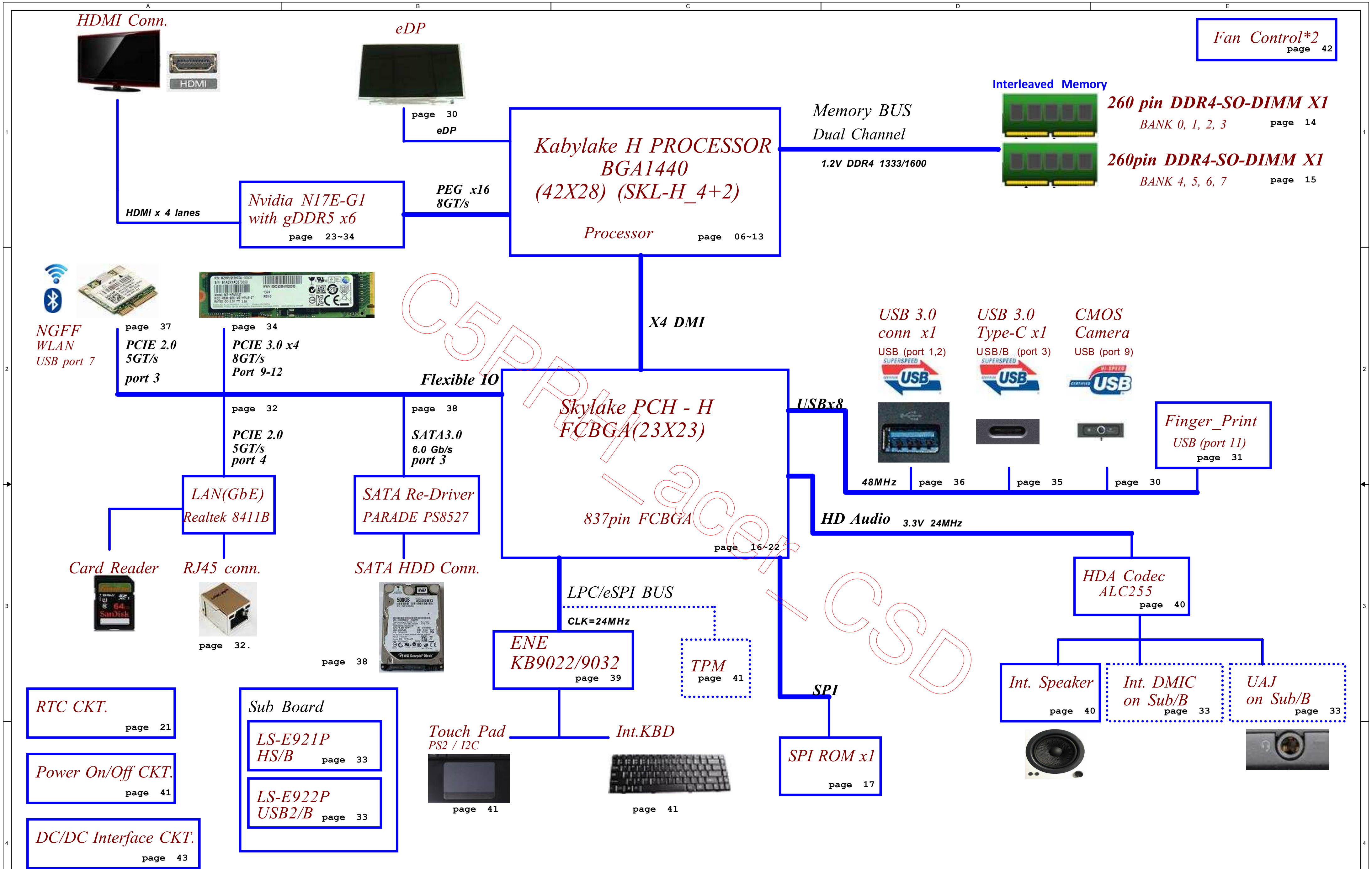
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Title: **Block Diagrams**

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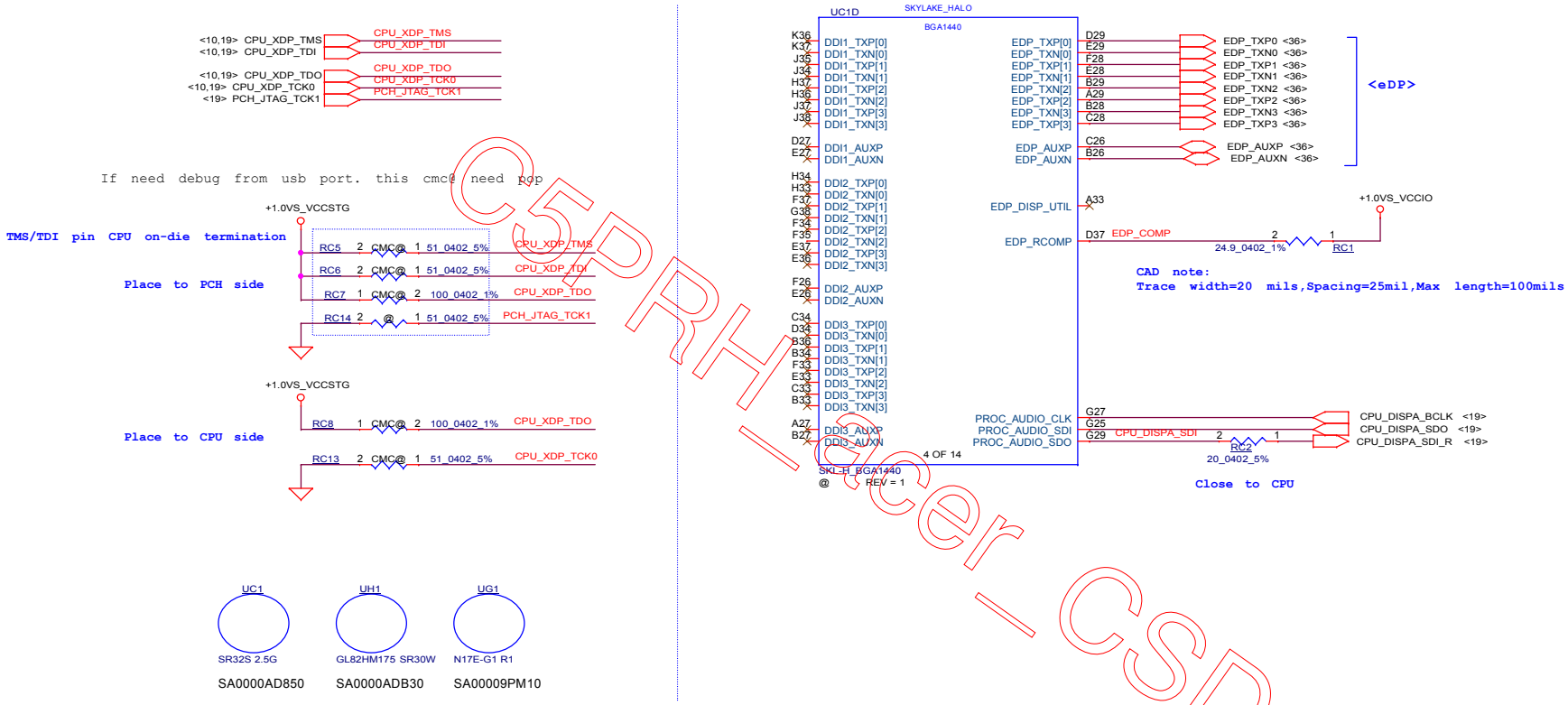

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Title: SKL-H(1/9)DDI,EDP

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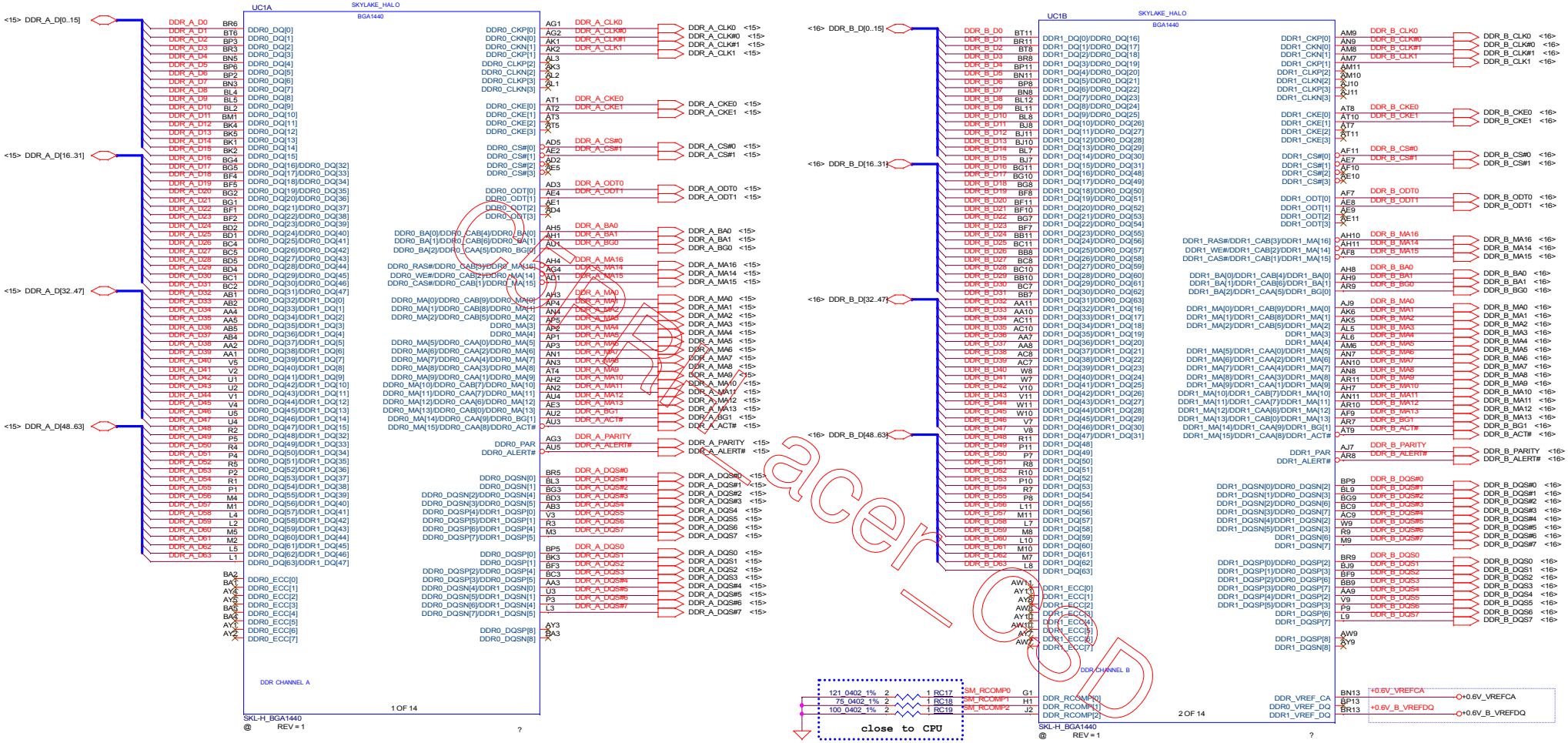
Interleaved Memory



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Title: **SKL-H(2/9)DDRIII**

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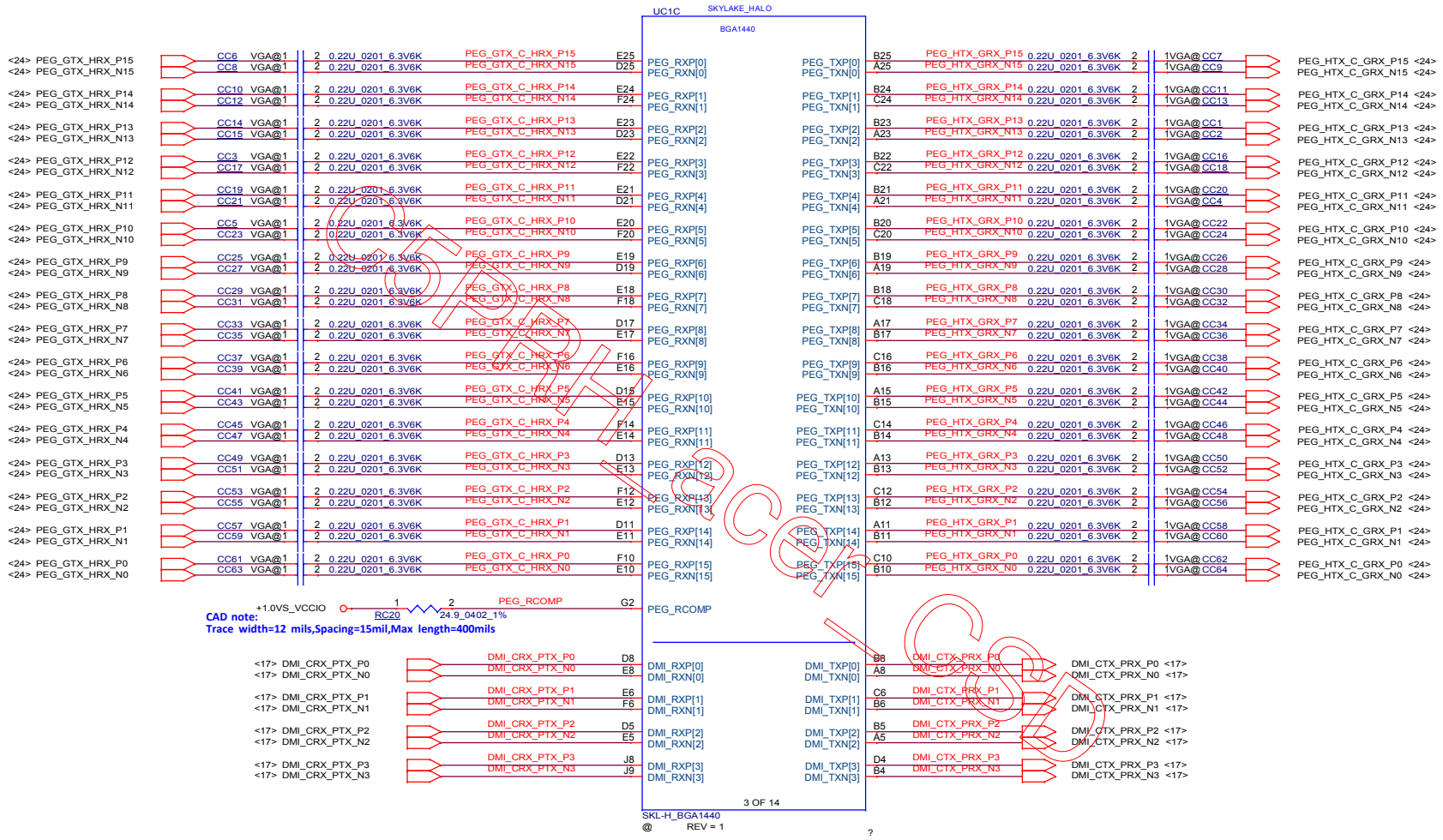

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Title: **SKL-H(3/9) PEG,DMI**

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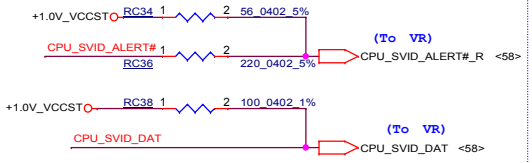
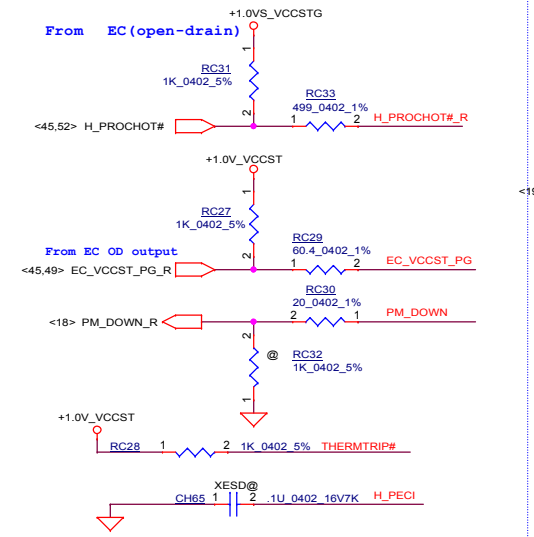
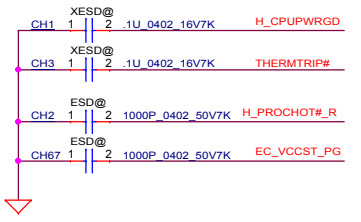
SVID Alert / Data

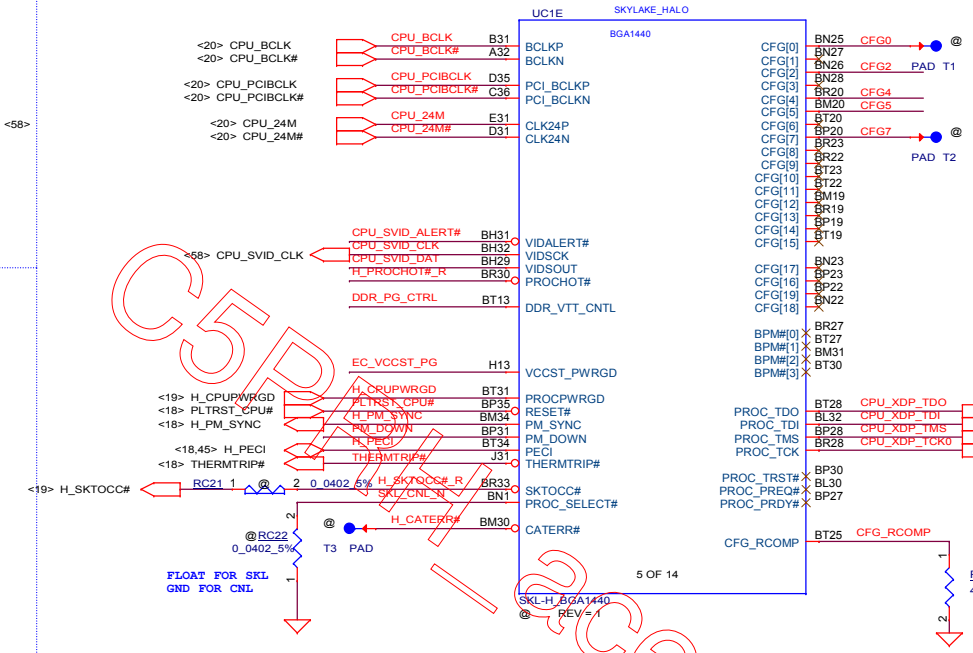
Place the PU resistors close to CPU

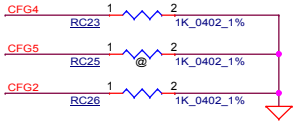




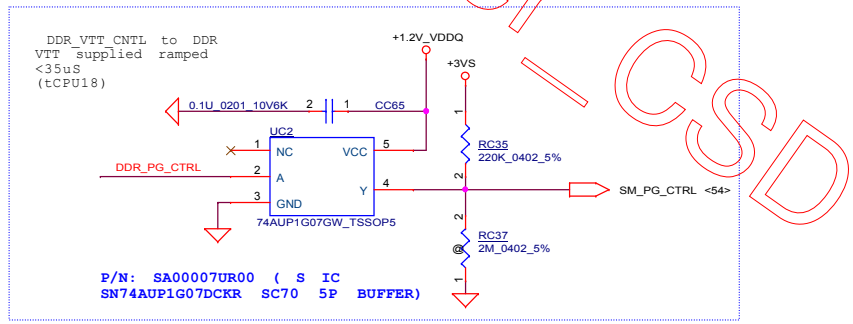


ESD Reserve ,pleace close to cpu





PCIE pore assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 reverse *	1	1	0
2 x 8	1	0	1
2 x 8 reverse	1	0	0
1 x 8 + 2 x 4	0	0	1
1x8+2x4 reverse	0	0	0



Reference SKL EDS 0.85 Table 6-8

CFG signals internal PH default value = 1

	Description
CFG[0] *	Stall reset sequence after PCU PLL lock until de-asserted – 1 = (Default) Normal Operation; No stall. – 0 = Stall.
CFG[4] *	Enable eDP – 1 = Disabled. – 0 = Enabled.
CFG[7] *	PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]	Reserved configuration lane.

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Title: SKL-H(4/9)CLK,GPIO

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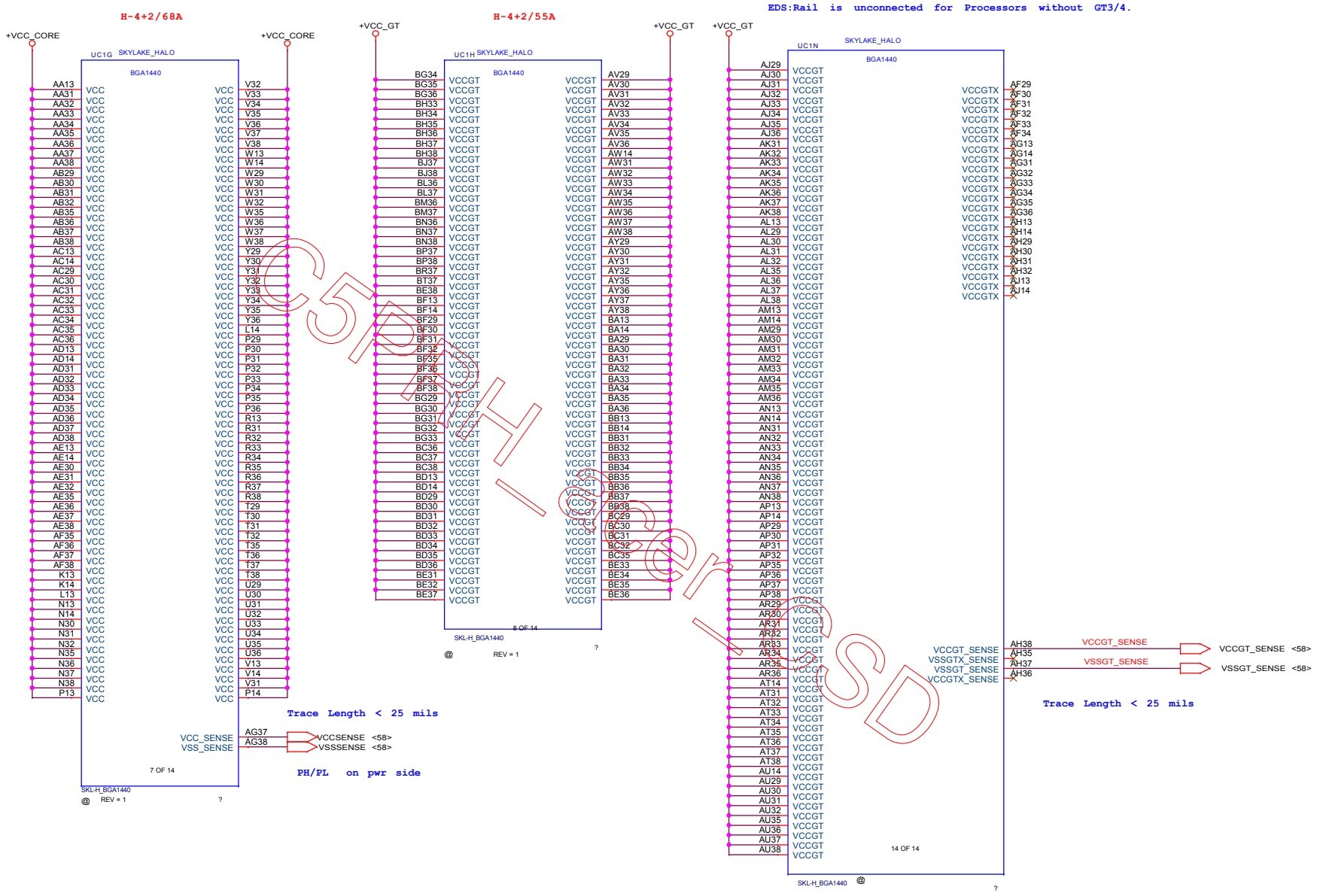

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Title: SKL-H(5/9)Power,SVID

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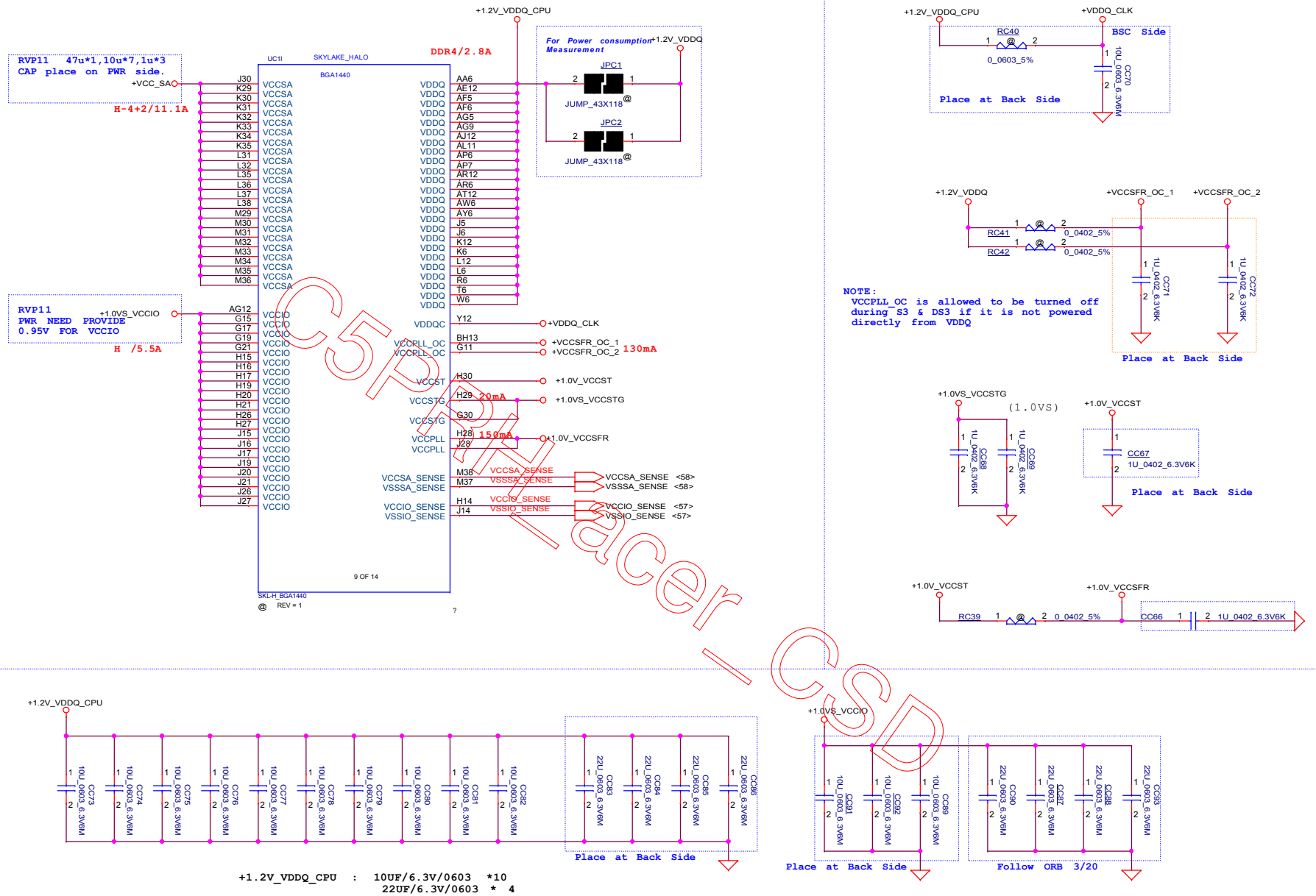

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Title: SKL-H(6/9)POWER			
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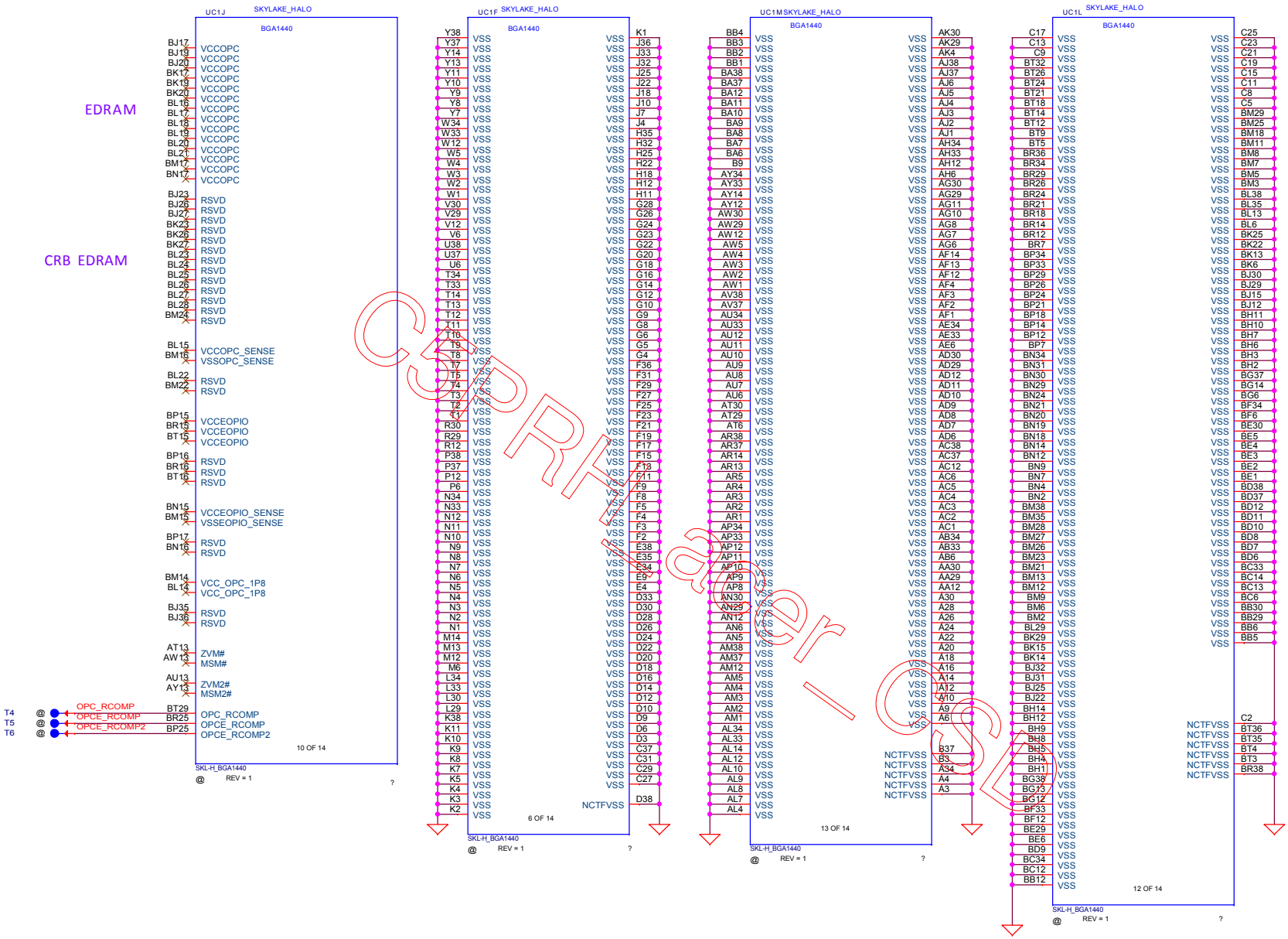

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Title: SKL-H(8/9)GND

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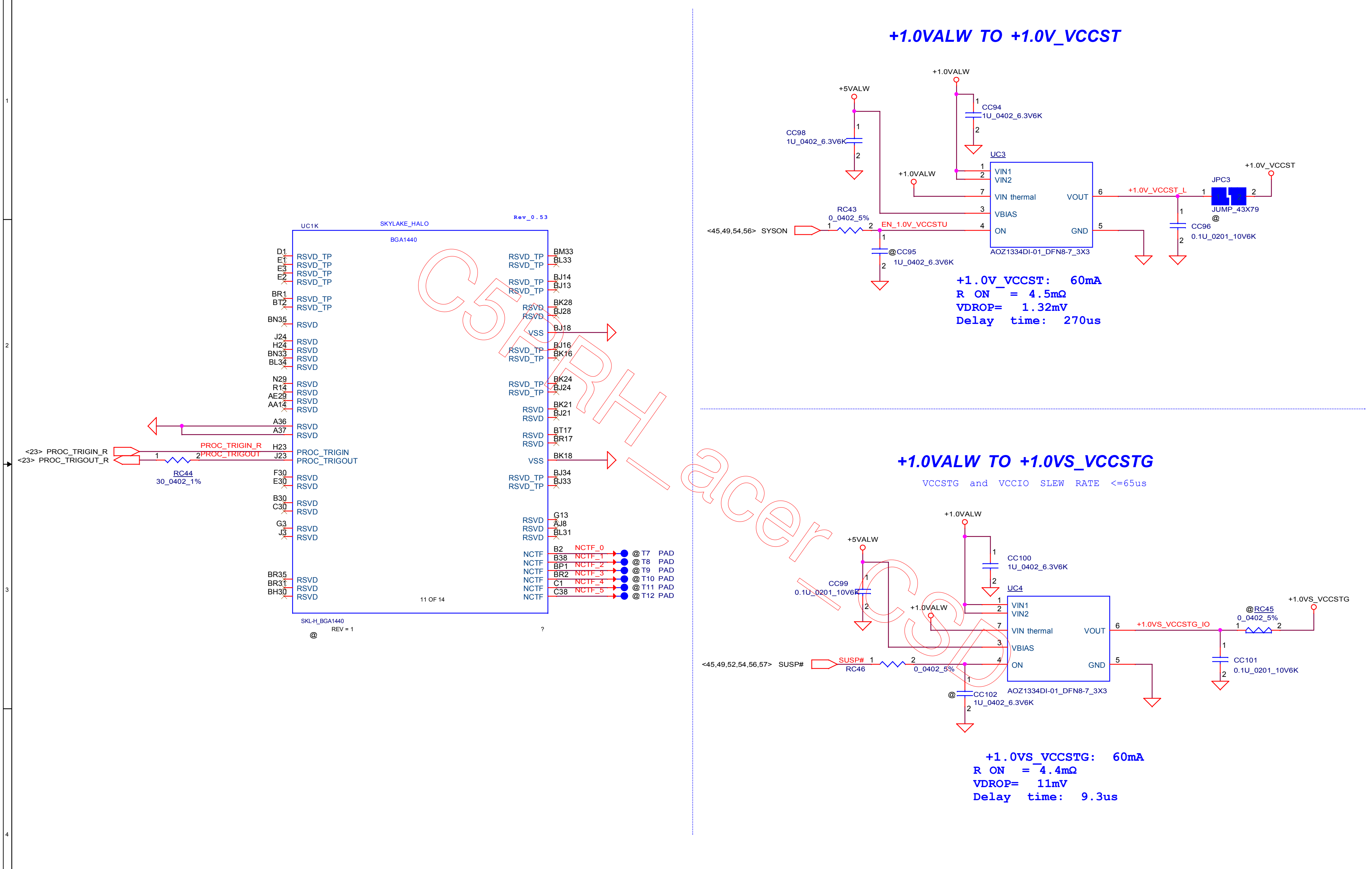

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Issued Date	2016/12/15	Deciphered Date 2017/12/15	Title: SKL-H(9/9)RSVD
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Reverse Type-4H

2-3A to 1 DIMMs/channel

<8> DDR_A_DQS#[0..7]
<8> DDR_A_D[0..63]
<8> DDR_A_DQS[0..7]

<8> DDR_A_MA[0..16]

<8> DDR_A_BA0 — DDR_A_BA0
<8> DDR_A_BA1 — DDR_A_BA1
<8> DDR_A_BG0 — DDR_A_BG0
<8> DDR_A_BG1 — DDR_A_BG1

<8> DDR_A_CLK0 — DDR_A_CLK0
<8> DDR_A_CLK#0 — DDR_A_CLK#0
<8> DDR_A_CLK1 — DDR_A_CLK1
<8> DDR_A_CLK#1 — DDR_A_CLK#1

<8> DDR_A_CKE0 — DDR_A_CKE0
<8> DDR_A_CKE1 — DDR_A_CKE1
<8> DDR_A_CS#0 — DDR_A_CS#0
<8> DDR_A_CS#1 — DDR_A_CS#1

<16,19,44> D_CK_SDATA — D_CK_SDATA
<16,19,44> D_CK_SCLK — D_CK_SCLK

<8> DDR_A_ODT0 — DDR_A_ODT0
<8> DDR_A_ODT1 — DDR_A_ODT1

Layout Note:
Place near JDIMM1.164

CPU Side

+0.6V_VREFCA

+1.2V_VDDQ

RD2 2_0402_1%

RD 1K_0402_1%

CD1 0.1U_0201_10V6K

+0.6V_DDRA_VREFCA

CD2 0.022U_0402_16V7K

RD3 1K_0402_1%

CD3 0.1U_0201_10V6K

RD4 24.9_0402_1%

Dimm1 Side

+0.6V_DDRA_VREFCA

#543016 PDG 1.0164
20mils wide & spacing

Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM1

Note:
place caps close to DIMM 4 on each side of DIMM

+1.2V_VDDQ

CD4 1U_0402_6.3V6K
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K
CD7 1U_0402_6.3V6K
CD8 1U_0402_6.3V6K
CD9 1U_0402_6.3V6K
CD10 1U_0402_6.3V6K
CD11 1U_0402_6.3V6K

+1.2V_VDDQ

CD12 0.1U_0201_10V6K
CD13 0.1U_0201_10V6K

+2.5V

CD14 1U_0402_6.3V6K
CD15 1U_0402_6.3V6K
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M

+1.2V_VDDQ

CD18 10U_0603_6.3V6M
CD19 10U_0603_6.3V6M
CD20 10U_0603_6.3V6M
CD21 10U_0603_6.3V6M
CD22 10U_0603_6.3V6M
CD23 10U_0603_6.3V6M
CD24 10U_0603_6.3V6M
CD25 10U_0603_6.3V6M

Follow MA51

CD26 330U_D2_2V_Y

SGA00009S00
330U 2V H1.9
9mohm POLY

Layout Note:
Place near JDIMM1.257/259

<8> DDR_A_ACT#

+1.2V_VDDQ

<8> DDR_A_PARITY
<8> DDR_A_ALERT#

RD5 240_0402_1%

SPD Address for CHANNEL0
Write Adress 0xA0
Read Address 0xA1
SA0=0 ,SA1=0 ,SA2=0

JDIMM1A

DDR_A_CLK0	137	CK0(T)	DQ0	8	DDR_A_D0
DDR_A_CLK#0	139	CK0#(C)	DQ1	7	DDR_A_D1
DDR_A_CLK1	138	CK1(T)	DQ2	20	DDR_A_D2
DDR_A_CLK#1	140	CK1#(C)	DQ3	21	DDR_A_D3
			DQ4	4	DDR_A_D4
DDR_A_CKE0	109	CKE0	DQ5	3	DDR_A_D5
DDR_A_CKE1	110	CKE1	DQ6	16	DDR_A_D6
			DQ7	17	DDR_A_D7
DDR_A_CS#0	149	S0#	DQS0(T)	13	DDR_A_DQS0
DDR_A_CS#1	157	S1#	DQS0#(C)	11	DDR_A_DQS#0
	162	S2#/C0			
	165	S3#/C1	DQ8	28	DDR_A_D8
			DQ9	29	DDR_A_D9
DDR_A_ODT0	155	ODT0	DQ10	41	DDR_A_D10
DDR_A_ODT1	161	ODT1	DQ11	42	DDR_A_D11
			DQ12	24	DDR_A_D12
DDR_A_BG0	115	BG0	DQ13	25	DDR_A_D13
DDR_A_BG1	113	BG1	DQ14	38	DDR_A_D14
DDR_A_BA0	150	BA0	DQ15	37	DDR_A_D15
DDR_A_BA1	145	BA1	DQS1(T)	34	DDR_A_DQS1
			DQS1#(C)	32	DDR_A_DQS#1
DDR_A_MA0	144	A0			
DDR_A_MA1	133	A1	DQ16	50	DDR_A_D16
DDR_A_MA2	132	A2	DQ17	49	DDR_A_D17
DDR_A_MA3	131	A3	DQ18	62	DDR_A_D18
DDR_A_MA4	128	A4	DQ19	63	DDR_A_D19
DDR_A_MA5	126	A5	DQ20	46	DDR_A_D20
DDR_A_MA6	127	A6	DQ21	45	DDR_A_D21
DDR_A_MA7	122	A7	DQ22	58	DDR_A_D22
DDR_A_MA8	125	A8	DQ23	59	DDR_A_D23
DDR_A_MA9	121	A9	DQS2(T)	55	DDR_A_DQS2
DDR_A_MA10	146	A10_AP	DQS2#(C)	53	DDR_A_DQS#2
DDR_A_MA11	120	A11			
DDR_A_MA12	119	A12	DQ24	70	DDR_A_D24
DDR_A_MA13	158	A13	DQ25	71	DDR_A_D25
DDR_A_MA14	151	A14_WE#	DQ26	83	DDR_A_D26
DDR_A_MA15	156	A15_CAS#	DQ27	84	DDR_A_D27
DDR_A_MA16	152	A16_RAS#	DQ28	66	DDR_A_D28
			DQ29	67	DDR_A_D29
DDR_A_ACT#	114	ACT#	DQ30	79	DDR_A_D30
			DQ31	80	DDR_A_D31
DDR_A_PARITY	143	PARITY	DQS3(T)	76	DDR_A_DQS3
DDR_A_ALERT#	116	ALERT#	DQS3#(C)	74	DDR_A_DQS#3
DDR_A_EVENT#	134	EVENT#			
DDR_DRAMRST#_R	108	RESET#	DQ32	174	DDR_A_D32
			DQ33	173	DDR_A_D33
D_CK_SDATA	254	SDA	DQ34	187	DDR_A_D34
D_CK_SCLK	253	SCL	DQ35	186	DDR_A_D35
			DQ36	170	DDR_A_D36
DDR_A_SA2	166	SA2	DQ37	169	DDR_A_D37
DDR_A_SA1	260	SA1	DQ38	183	DDR_A_D38
DDR_A_SA0	256	SA0	DQ39	182	DDR_A_D39
			DQS4(T)	179	DDR_A_DQS4
			DQS4#(C)	177	DDR_A_DQS#4
	92	CB0_NC			
	91	CB1_NC	DQ40	195	DDR_A_D40
	101	CB2_NC	DQ41	194	DDR_A_D41
	105	CB3_NC	DQ42	207	DDR_A_D42
	88	CB4_NC	DQ43	208	DDR_A_D43
	87	CB5_NC	DQ44	191	DDR_A_D44
	100	CB6_NC	DQ45	190	DDR_A_D45
	104	CB7_NC	DQ46	203	DDR_A_D46
	97	DQS8(T)	DQ47	204	DDR_A_D47
	95	DQS8#(C)	DQS5(T)	200	DDR_A_DQS5
			DQS5#(C)	198	DDR_A_DQS#5
	12	DM0#/DBI0#		216	DDR_A_D48
	33	DM1#/DBI1#	DQ48	215	DDR_A_D49
	54	DM2#/DBI2#	DQ49	228	DDR_A_D50
	75	DM3#/DBI3#	DQ50	229	DDR_A_D51
	178	DM4#/DBI4#	DQ51	211	DDR_A_D52
	199	DM5#/DBI5#	DQ52	212	DDR_A_D53
	220	DM6#/DBI6#	DQ53	224	DDR_A_D54
	241	DM7#/DBI7#	DQ54	225	DDR_A_D55
	96	DM8#/DBI8#	DQ55	221	DDR_A_DQS6
			DQS6(T)	219	DDR_A_DQS#6
			DQS6#(C)		
				237	DDR_A_D56
			DQ56	236	DDR_A_D57
			DQ57	249	DDR_A_D58
			DQ58	250	DDR_A_D59
			DQ59	232	DDR_A_D60
			DQ60	233	DDR_A_D61
			DQ61	245	DDR_A_D62
			DQ62	246	DDR_A_D63
			DQ63	242	DDR_A_DQS7
			DQS7(T)	240	DDR_A_DQS#7
			DQS7#(C)		

LOTES_ADDR0206-P001A
CONN@

+1.2V_VDDQ

RD6 470_0402_5%

<19> DDR_DRAMRST# — @RD7 0_0402_5% — DDR_DRAMRST#_R <16>

CD27 XESD@ 0.1U_0201_10V6K

Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

JDIMM1B

+1.2V_VDDQ — +1.2V_VDDQ

+0.6V_DDRA_VREFCA — +3VS_DIMMA — +0.6VS_VTT — +2.5V

	111	VDD1	VDD11	141	
	112	VDD2	VDD12	142	
	117	VDD3	VDD13	147	
	118	VDD4	VDD14	148	
	123	VDD5	VDD15	153	
	124	VDD6	VDD16	154	
	129	VDD7	VDD17	159	
	130	VDD8	VDD18	160	
	135	VDD9	VDD19	163	
	136	VDD10			
	255	VDDSPD	VTT	258	
	164	VREFCA	VPP1	257	
			VPP2	259	
	1	VSS	VSS	99	
	2	VSS	VSS	102	
	5	VSS	VSS	103	
	6	VSS	VSS	106	
	9	VSS	VSS	107	
	10	VSS	VSS	167	
	14	VSS	VSS	168	
	15	VSS	VSS	171	
	18	VSS	VSS	172	
	19	VSS	VSS	175	
	22	VSS	VSS	176	
	23	VSS	VSS	180	
	26	VSS	VSS	181	
	27	VSS	VSS	184	
	30	VSS	VSS	185	
	31	VSS	VSS	188	
	35	VSS	VSS	189	
	36	VSS	VSS	192	
	39	VSS	VSS	193	
	40	VSS	VSS	196	
	43	VSS	VSS	197	
	44	VSS	VSS	201	
	47	VSS	VSS	202	
	48	VSS	VSS	205	
	51	VSS	VSS	206	
	52	VSS	VSS	209	
	56	VSS	VSS	210	
	57	VSS	VSS	213	
	60	VSS	VSS	214	
	61	VSS	VSS	217	
	64	VSS	VSS	218	
	65	VSS	VSS	222	
	68	VSS	VSS	223	
	69	VSS	VSS	226	
	72	VSS	VSS	227	
	73	VSS	VSS	230	
	77	VSS	VSS	231	
	78	VSS	VSS	234	
	81	VSS	VSS	235	
	82	VSS	VSS	238	
	85	VSS	VSS	239	
	86	VSS	VSS	243	
	89	VSS	VSS	244	
	90	VSS	VSS	247	
	93	VSS	VSS	248	
	94	VSS	VSS	251	
	98	VSS	VSS	252	
	262	GND	GND	261	

LOTES_ADDR0206-P001A
CONN@

+0.6VS_VTT

CD28 10U_0402_6.3V6K
CD29 10U_0402_6.3V6K
CD30 10U_0402_6.3V6K
CD31 10U_0402_6.3V6K
CD32 10U_0603_6.3V6M
@CD33 10U_0603_6.3V6M

Place Holder

Layout Note:
Place near JDIMM1.258

+3VS — @RD8 0_0402_5% — +3VS_DIMMA

CD35 0.1U_0201_10V6K
CD36 2.2U_0402_6.3V6M

+0.6V_DDRA_VREFCA

CD37 0.1U_0201_10V6K
CD38 2.2U_0402_6.3V6M

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164 within 200mils

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **DDR4_DIMMA**

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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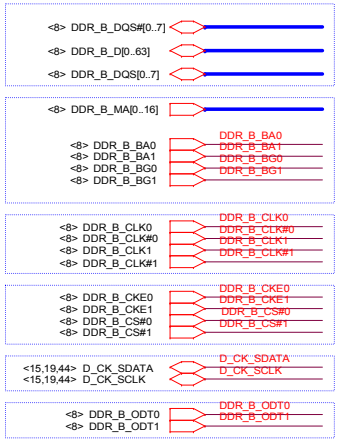
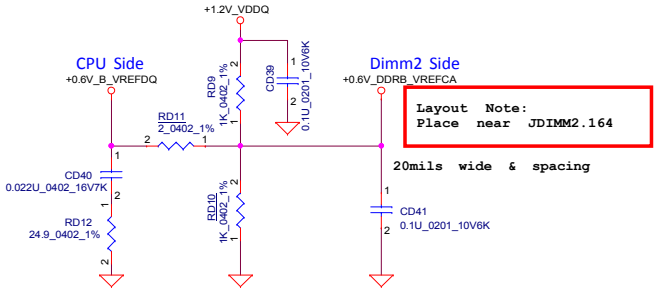
Reverse Type-8H

2-3A to 1 DIMMs/channel





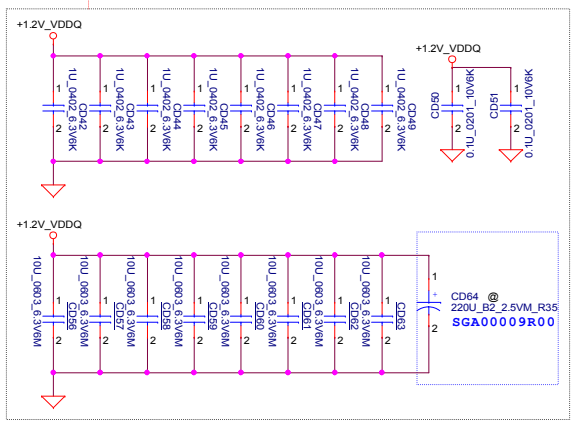
Layout Note:
Place near JDIMM2.164

20mils wide & spacing

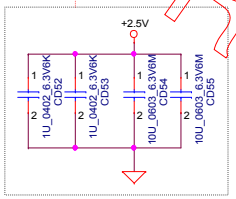
Place near to SO-DIMM connector.

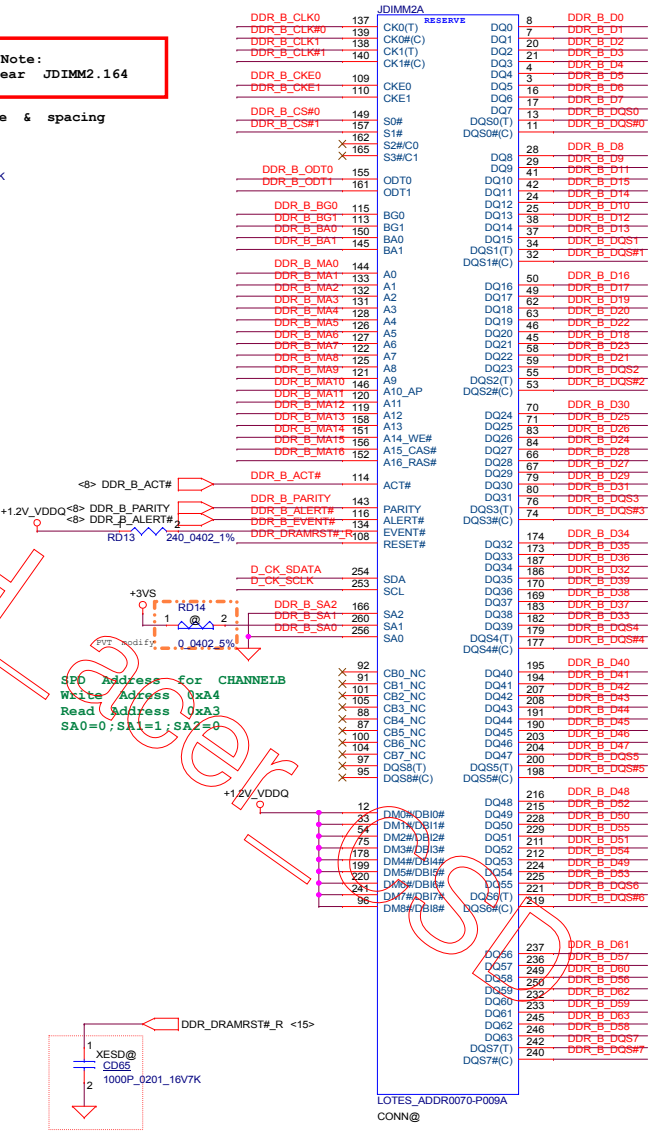
Layout Note:
Place near JDIMM2

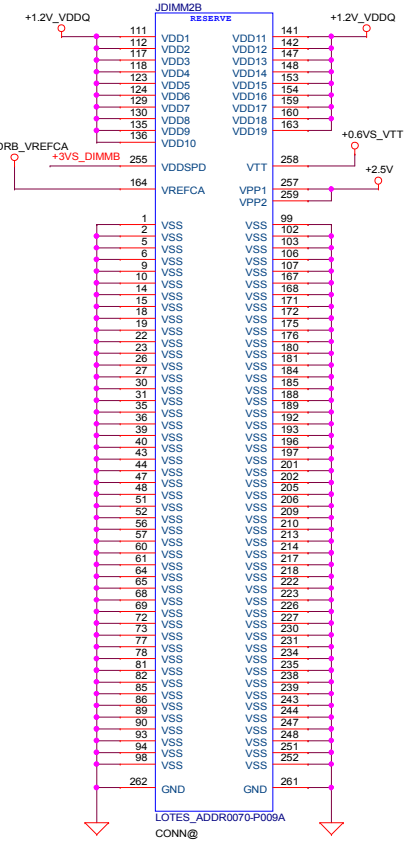
Note:
place caps close to DIMM
4 on each side of DIMM



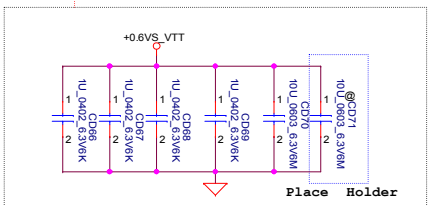
Layout Note:
Place near JDIMM2.257/259

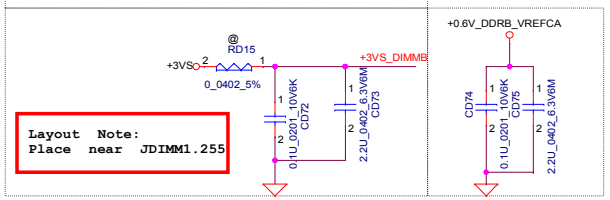






Layout Note:
Place near JDIMM2.258





Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164
within 200mils

Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

SPD Address for CHANNELB
Write Adress 0xA4
Read Address 0xA3
SA0=0;SA1=1;SA2=0

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **DDR4 DIMMB**

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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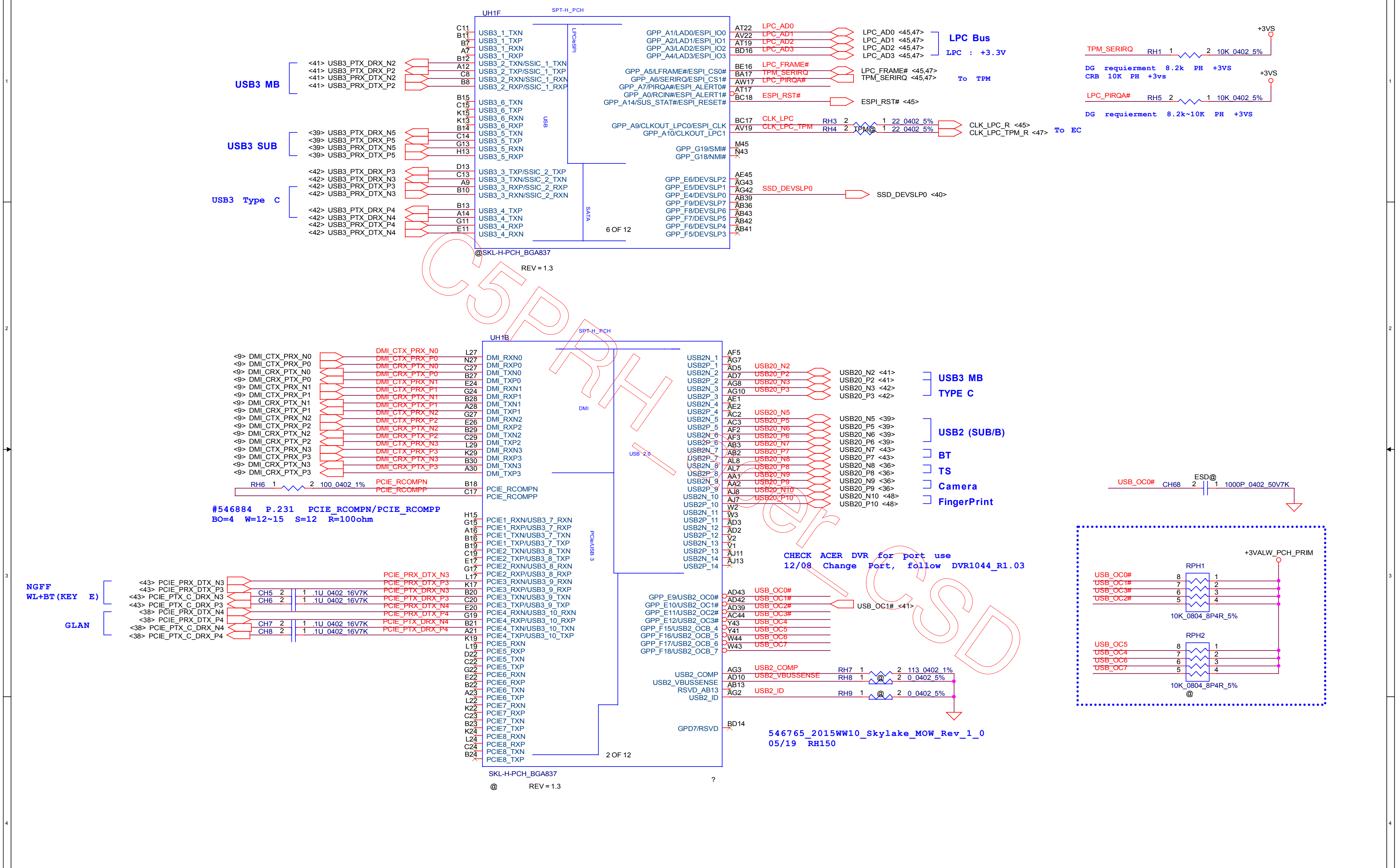

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

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Compal Electronics, Inc.

Title: **PCH(1/7)DMI,PCIE,USB**

Size: Custom — Document Number: **C5PRH M/B LA-E921P** — Rev: 1.A

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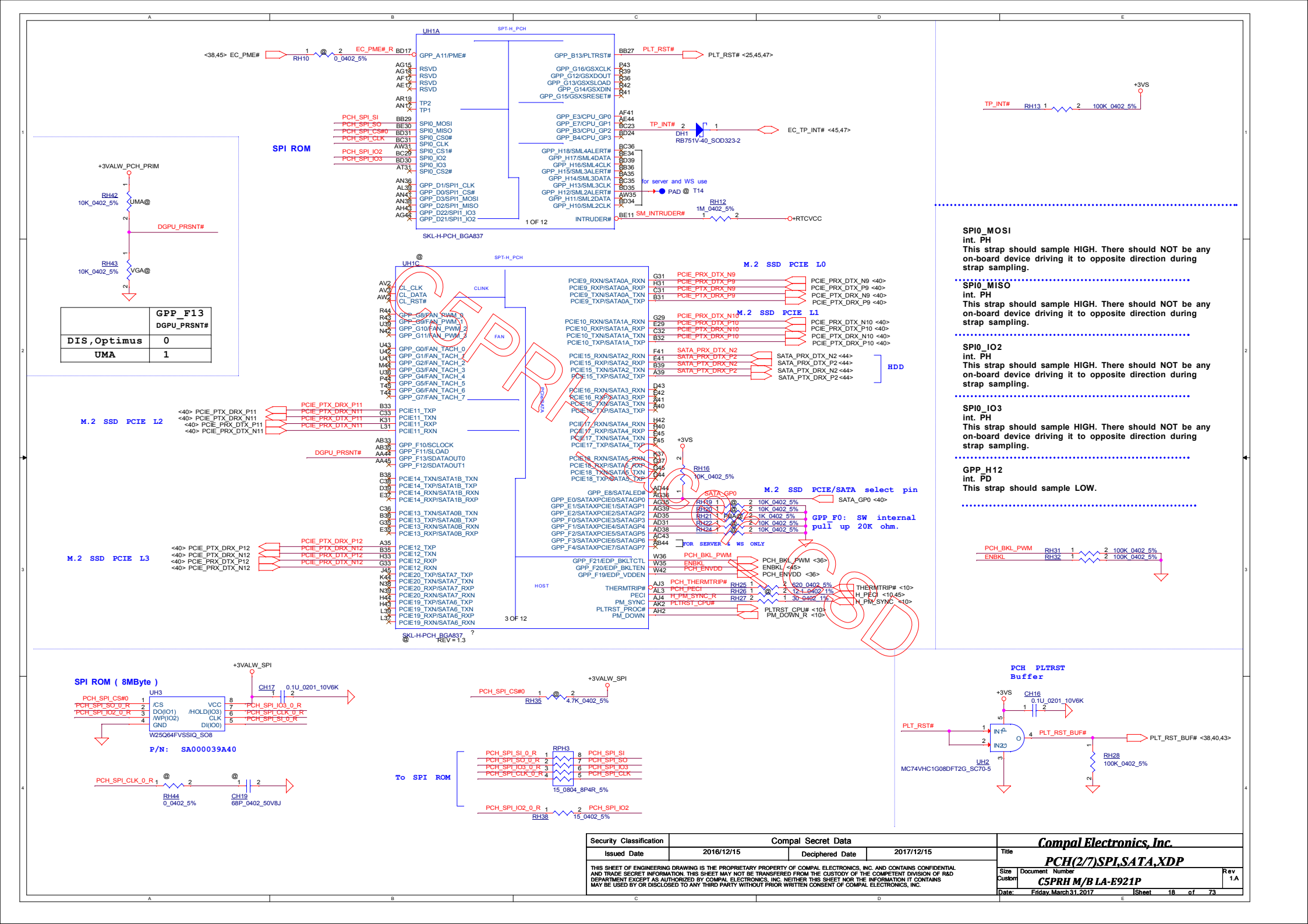
UH1A
SPT-H_PCH
SPI ROM
GPP_F13
DGPU_PRSNT#
DIS,Optimus 0
UMA 1
M.2 SSD PCIE L0
M.2 SSD PCIE L1
M.2 SSD PCIE L2
M.2 SSD PCIE L3
HDD
M.2 SSD PCIE/SATA select pin
GPP_F0: SW internal pull up 20K ohm.
SPI0_MOSI
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3
int. PH
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H12
int. PD
This strap should sample LOW.
SPI ROM (8MByte)
P/N: SA000039A40
To SPI ROM
PCH PLTRST Buffer
Compal Secret Data
Compal Electronics, Inc.
PCH(2/7)SPI,SATA,XDP
C5PRH M/B LA-E921P
Rev 1.A
Friday, March 31, 2017
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2017/12/15
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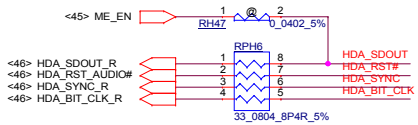
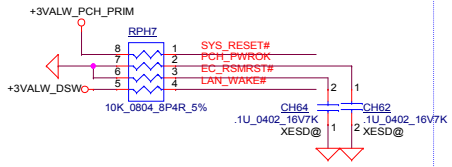
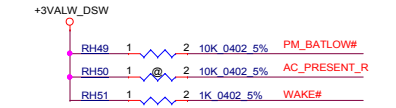
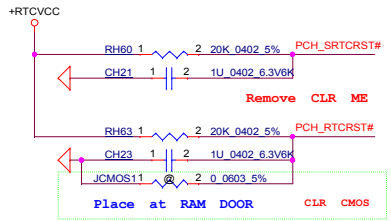
HDA for AUDIO

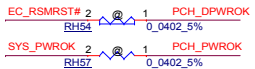


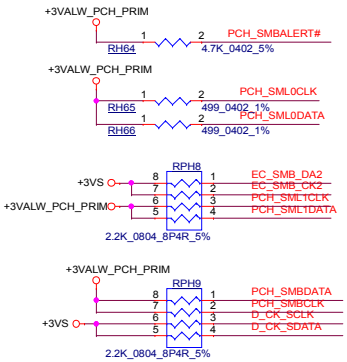




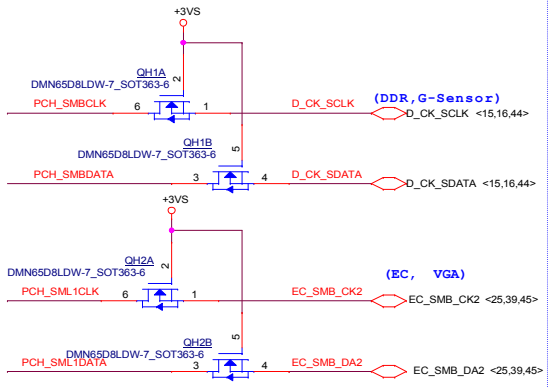
WAKE#
(DSX wake event)
10 KΩ pull-up to Vcc DS W3_3
The pull-up is required even if PCIe* interface is not used on the platform.

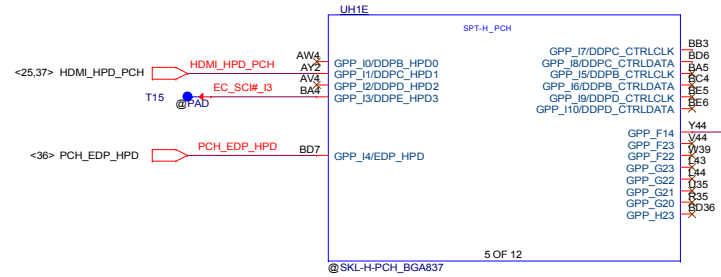


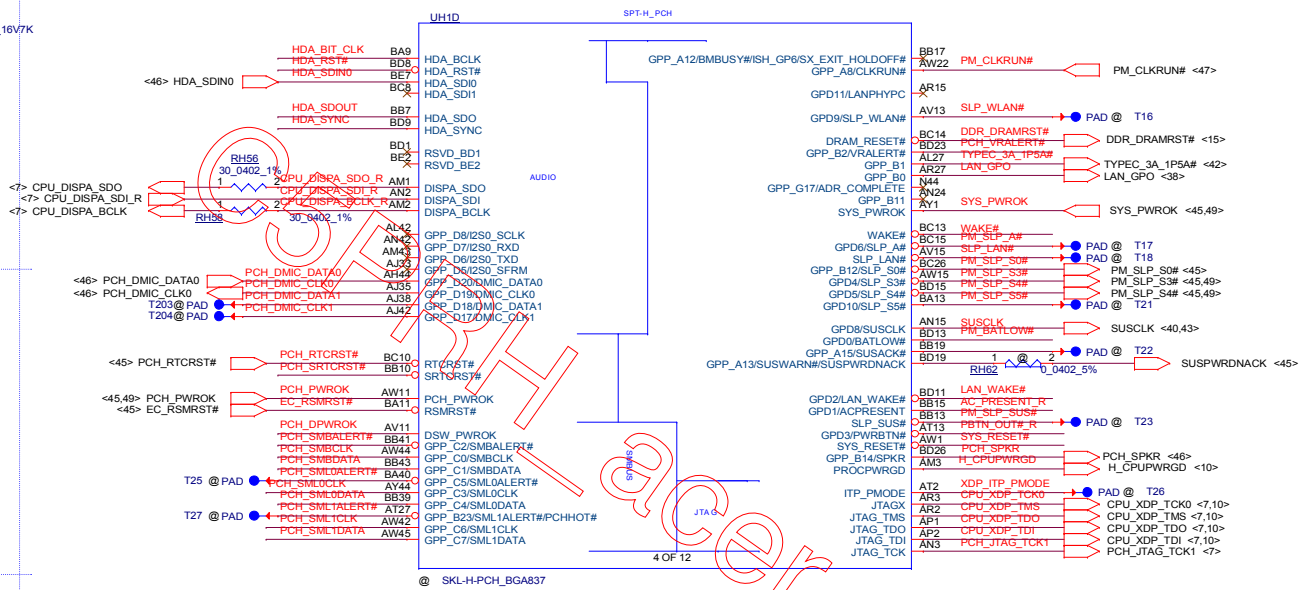


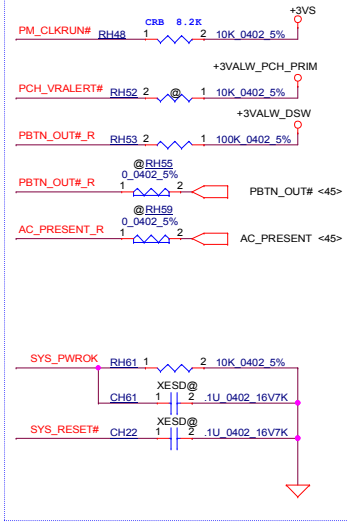


PDG_0_71 requirement PH to +3V_PCH
10/14 Dan









Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

Compal Electronics, Inc.
Title: PCH(3/7)GPIO,SMBUS
Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev: 1.A
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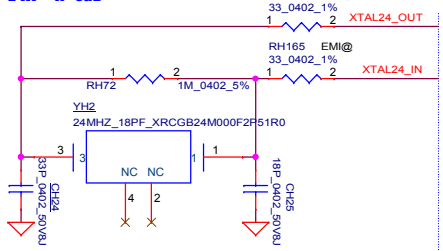
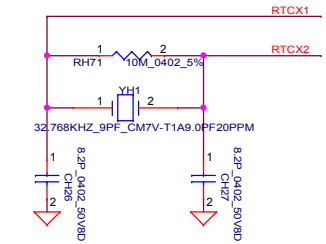
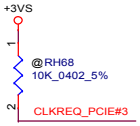
24M X'tal

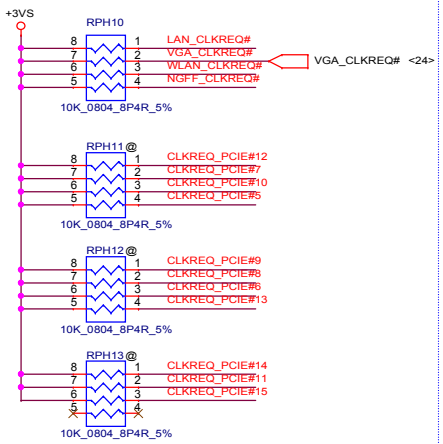


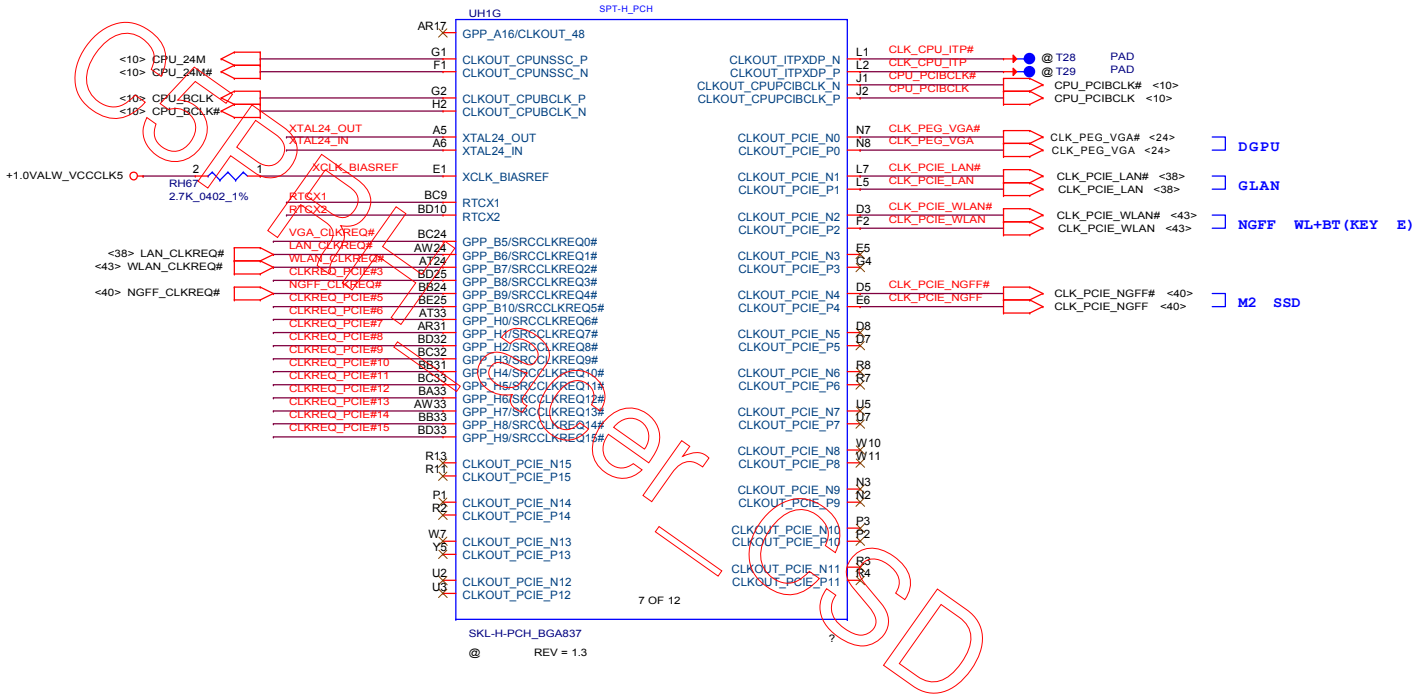
RTC X'tal



P/N: SJ10000Q400 (S CRYSTAL 32.768KHZ 9PF 20PPM 9H03280012)







Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: PCH(4/7)CLK

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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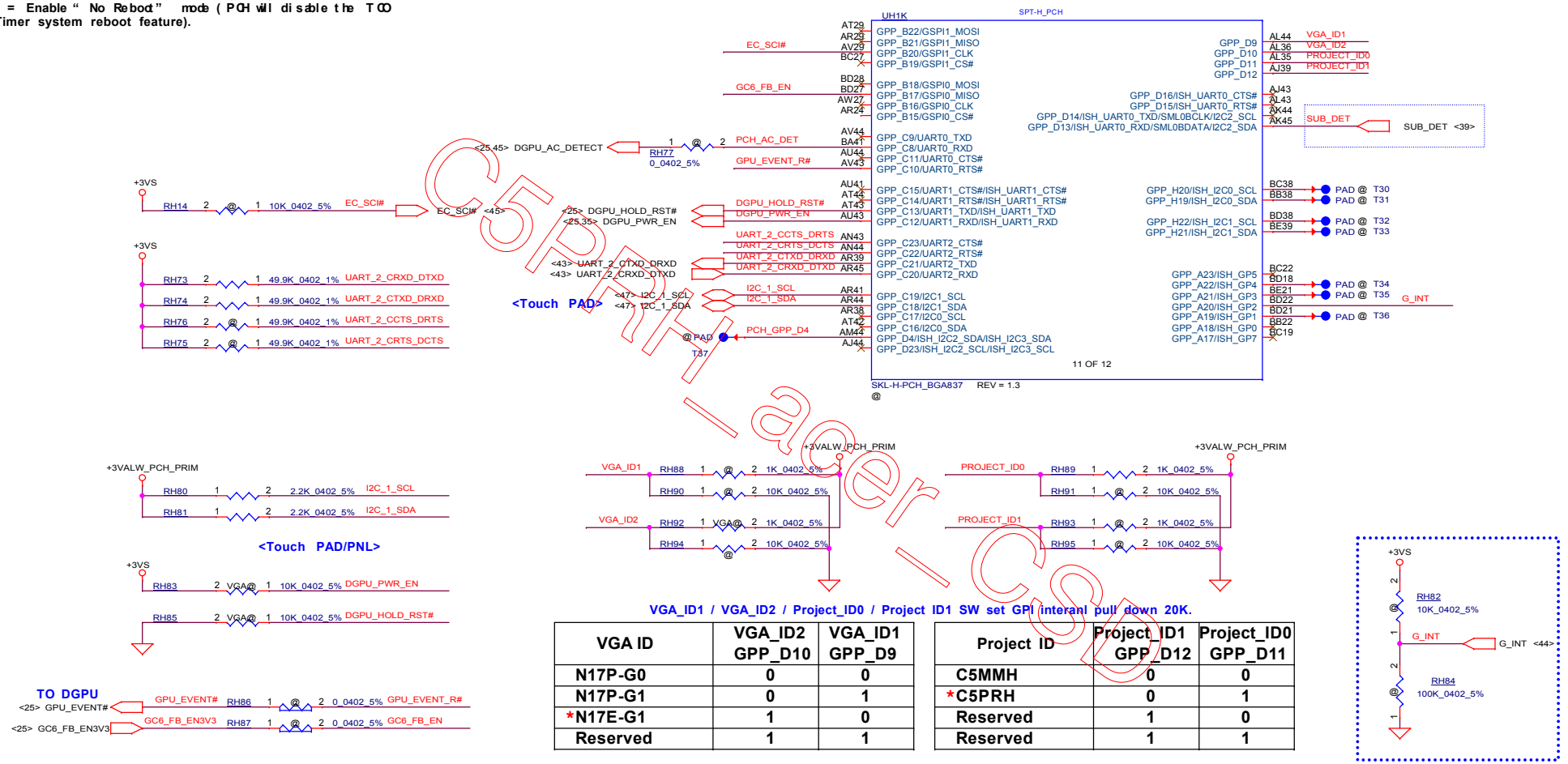
Functional Strap Definitions

GSPI1_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

GSPI0_MOSI / GPP_B18
int. PD
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature).



VGA_ID1 / VGA_ID2 / Project_ID0 / Project ID1 SW set GPI interanl pull down 20K.

VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
N17P-G0	0	0
N17P-G1	0	1
*N17E-G1	1	0
Reserved	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
C5MMH	0	0
*C5PRH	0	1
Reserved	1	0
Reserved	1	1

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: PCH(5/7)UART,I2C,GPIO

Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev: 1.A

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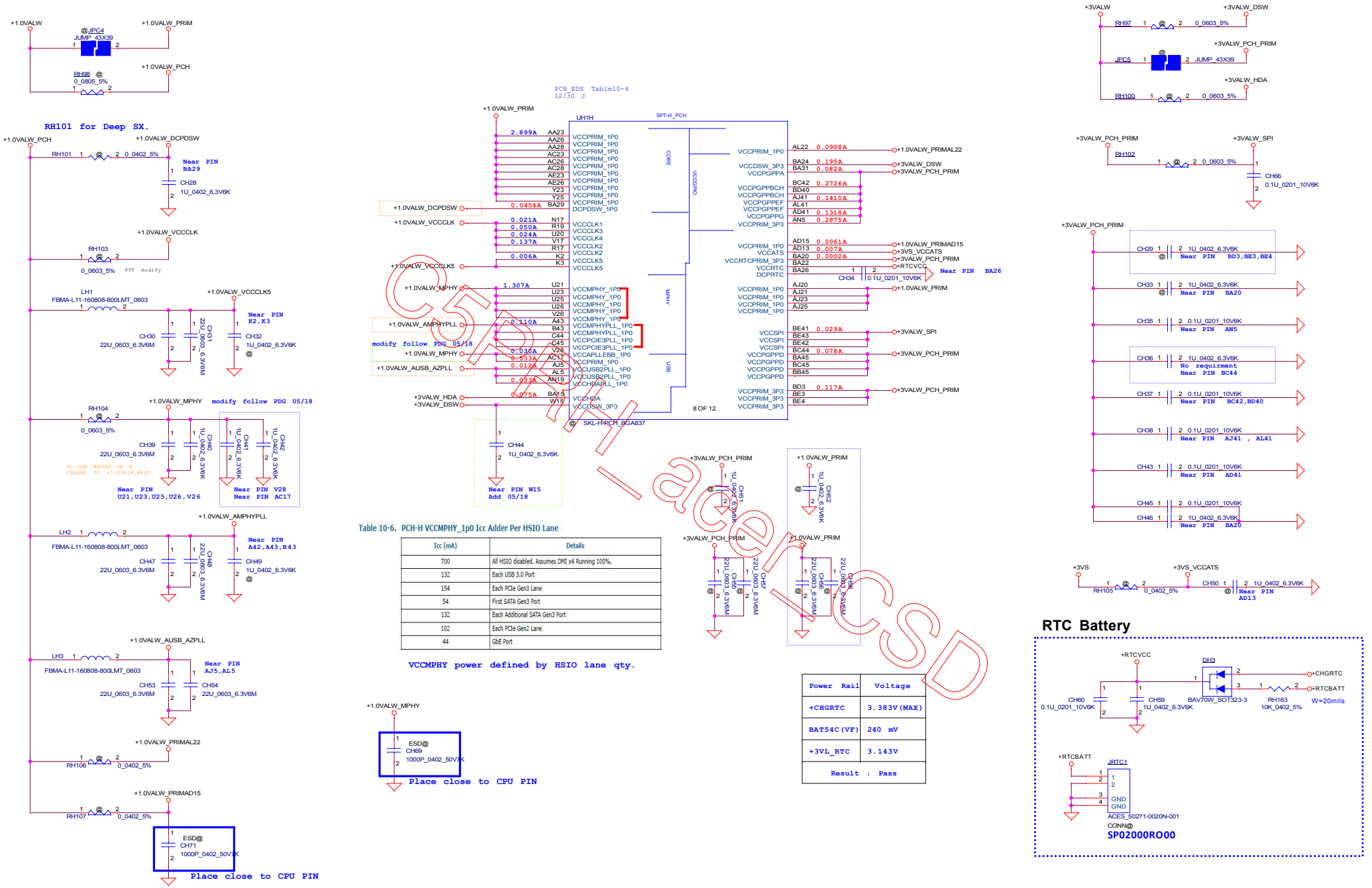
+1.0VALW
@JPC4
JUMP_43X39
+1.0VALW_PRIM
+1.0VALW_PCH
RH98 @ 0_0805_5%
RH101 for Deep SX.
+1.0VALW_PCH
+1.0VALW_DCPDSW
RH101 0_0402_5%
Near PIN BA29
CH28 1U_0402_6.3V6K
+1.0VALW_VCCCLK
RH103 0_0603_5% PVT modify
LH1 FBMA-L11-160808-800LMT_0603
+1.0VALW_VCCCLK5
Near PIN K2,K3
CH30 22U_0603_6.3V6M
CH31 22U_0603_6.3V6M
CH32 1U_0402_6.3V6K @
+1.0VALW_MPHY
modify follow PDG 05/18
RH104 0_0603_5%
CH39 22U_0603_6.3V6M
CH40 1U_0402_6.3V6K
CH41 1U_0402_6.3V6K
CH42 1U_0402_6.3V6K
NO USE MPHYGT ON H CHANGE TO +1.0VALW_MPHY
Near PIN U21,U23,U25,U26,V26
Near PIN V28
Near PIN AC17
+1.0VALW_AMPHYPLL
LH2 FBMA-L11-160808-800LMT_0603
Near PIN A42,A43,B43
CH47 22U_0603_6.3V6M
CH48 22U_0603_6.3V6M
CH49 1U_0402_6.3V6K @
+1.0VALW_AUSB_AZPLL
LH3 FBMA-L11-160808-800LMT_0603
Near PIN AJ5,AL5
CH53 22U_0603_6.3V6M
CH54 22U_0603_6.3V6M
+1.0VALW_PRIMAL22
RH106 0_0402_5%
+1.0VALW_PRIMAD15
RH107 0_0402_5%
ESD@ CH71 1000P_0402_50V7K
Place close to CPU PIN
PCH_EDS Table10-4 12/30 J
UH1H
SPT-H_PCH
2.899A AA23 VCCPRIM_1P0
AA26 VCCPRIM_1P0
AA28 VCCPRIM_1P0
AC23 VCCPRIM_1P0
AC26 VCCPRIM_1P0
AC28 VCCPRIM_1P0
AE23 VCCPRIM_1P0
AE26 VCCPRIM_1P0
Y23 VCCPRIM_1P0
Y25 VCCPRIM_1P0
0.0454A BA29 DCPDSW_1P0
+1.0VALW_DCPDSW
+1.0VALW_VCCCLK
0.021A N17 VCCCLK1
0.050A R19 VCCCLK3
0.024A U20 VCCCLK4
0.137A V17 VCCCLK2
R17 VCCCLK2
0.006A K2 VCCCLK5
K3 VCCCLK5
+1.0VALW_VCCCLK5
+1.0VALW_MPHY
1.307A U21 VCCMPHY_1P0
U23 VCCMPHY_1P0
U25 VCCMPHY_1P0
U26 VCCMPHY_1P0
V26 VCCMPHY_1P0
+1.0VALW_AMPHYPLL
0.110A A43 VCCMPHYPLL_1P0
B43 VCCMPHYPLL_1P0
modify follow PDG 05/18
+1.0VALW_MPHY
C44 VCCPCIE3PLL_1P0
C45 VCCPCIE3PLL_1P0
0.030A V28 VCCAPLLEBB_1P0
0.533A AC17 VCCPRIM_1P0
+1.0VALW_AUSB_AZPLL
0.012A AJ5 VCCUSB2PLL_1P0
AL5 VCCUSB2PLL_1P0
0.033A AN19 VCCHDAPLL_1P0
0.075A BA15 VCCHDA
+3VALW_HDA
+3VALW_DSW
W15 VCCDSW_3P3
@ SKL-H_PCH_BGA837
8 OF 12
CORE
VCCPRIM_1P0
AL22 0.0908A +1.0VALW_PRIMAL22
VCCDSW_3P3
VCCPGPPA
BA24 0.195A +3VALW_DSW
BA31 0.082A +3VALW_PCH_PRIM
VCCPGPPBCH
BC42 0.2726A
BD40
VCCPGPPBCH
AJ41 0.1410A
AL41
VCCPGPPEF
AD41 0.1318A
VCCPGPPG
AN5 0.2875A
VCCPRIM_3P3
VCCPRIM_1P0
AD15 0.0061A +1.0VALW_PRIMAD15
AD13 0.007A +3VS_VCCATS
VCCATS
BA20 0.0002A +3VALW_PCH_PRIM
VCCRTCPRIM_3P3
BA22
VCCRTC
BA26 +RTCVCC
DCPRTC
CH34 0.1U_0201_10V6K
Near PIN BA26
AJ20
AJ21 +1.0VALW_PRIM
AJ23
AJ25
VCCPRIM_1P0
VCCSPI
BE41 0.029A +3VALW_SPI
BE43
VCCSPI
BE42
VCCSPI
BC44 0.078A +3VALW_PCH_PRIM
VCCPGPPD
BA45
VCCPGPPD
BC45
VCCPGPPD
BB45
VCCPGPPD
VCCPRIM_3P3
BD3 0.117A +3VALW_PCH_PRIM
VCCPRIM_3P3
BE3
VCCPRIM_3P3
BE4
MPHY
USB
CH44 1U_0402_6.3V6K
Near PIN W15
Add 05/18
Table 10-6. PCH-H VCCMPHY_1p0 Icc Adder Per HSIO Lane
Icc (mA) | Details
700 | All HSIO disabled. Assumes DMI x4 Running 100%.
132 | Each USB 3.0 Port
154 | Each PCIe Gen3 Lane
54 | First SATA Gen3 Port
132 | Each Additional SATA Gen3 Port
102 | Each PCIe Gen2 Lane
44 | GbE Port
VCCMPHY power defined by HSIO lane qty.
+1.0VALW_MPHY
ESD@ CH69 1000P_0402_50V7K
Place close to CPU PIN
+3VALW_PCH_PRIM
CH51 1U_0402_6.3V6K
+1.0VALW_PRIM
CH52 1U_0402_6.3V6K
+3VALW_PCH_PRIM
CH55 22U_0603_6.3V6M
CH57 22U_0603_6.3V6M
+1.0VALW_PRIM
CH56 22U_0603_6.3V6M
CH58 22U_0603_6.3V6M
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
+3VALW
RH97 0_0603_5%
+3VALW_DSW
+3VALW_PCH_PRIM
JPC5 JUMP_43X39
+3VALW_HDA
RH100 0_0603_5%
+3VALW_PCH_PRIM
RH102 0_0603_5%
+3VALW_SPI
CH66 0.1U_0201_10V6K
+3VALW_PCH_PRIM
CH29 1U_0402_6.3V6K Near PIN BD3,BE3,BE4
CH33 1U_0402_6.3V6K Near PIN BA20
CH35 0.1U_0201_10V6K Near PIN AN5
CH36 1U_0402_6.3V6K No requirment Near PIN BC44
CH37 0.1U_0201_10V6K Near PIN BC42,BD40
CH38 0.1U_0201_10V6K Near PIN AJ41 , AL41
CH43 0.1U_0201_10V6K Near PIN AD41
CH45 0.1U_0201_10V6K
CH46 1U_0402_6.3V6K Near PIN BA20
+3VS
RH105 0_0402_5%
+3VS_VCCATS
CH50 1U_0402_6.3V6K Near PIN AD13
RTC Battery
+RTCVCC
DH3 BAV70W_SOT323-3
+CHGRTC
+RTCBATT
CH60 0.1U_0201_10V6K
CH59 1U_0402_6.3V6K
RH163 10K_0402_5%
W=20mils
+RTCBATT
JRTC1
GND
GND
ACES_50271-0020N-001
CONN@
SP02000RO00
Security Classification
Compal Secret Data
Issued Date
2016/12/15
Deciphered Date
2017/12/15
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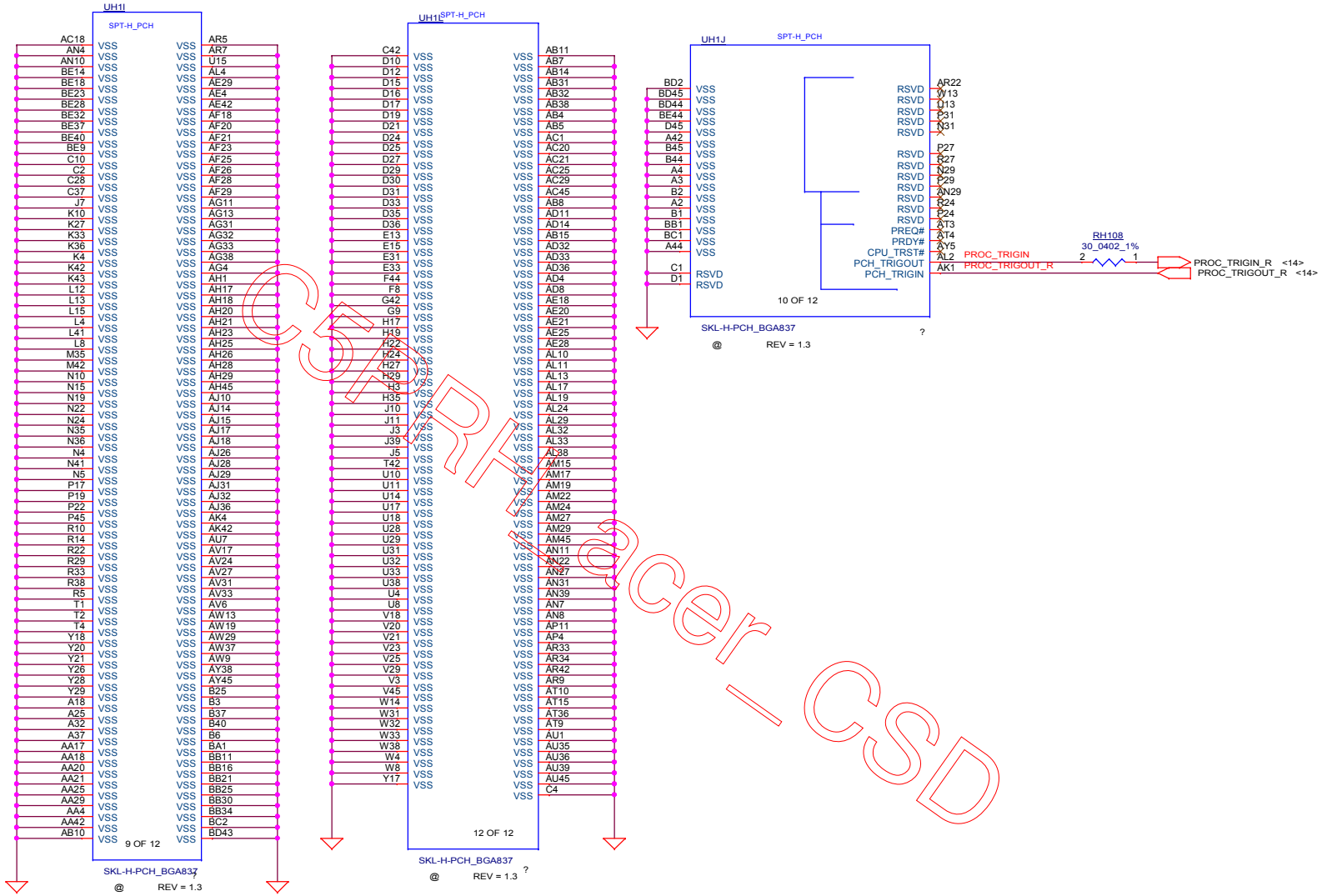
Compal Electronics, Inc.
Title
PCH(6/7)POWER
Size Custom
Document Number
C5PRH M/B LA-E921P
Rev 1.A
Date: Friday, March 31, 2017
Sheet 22 of 73



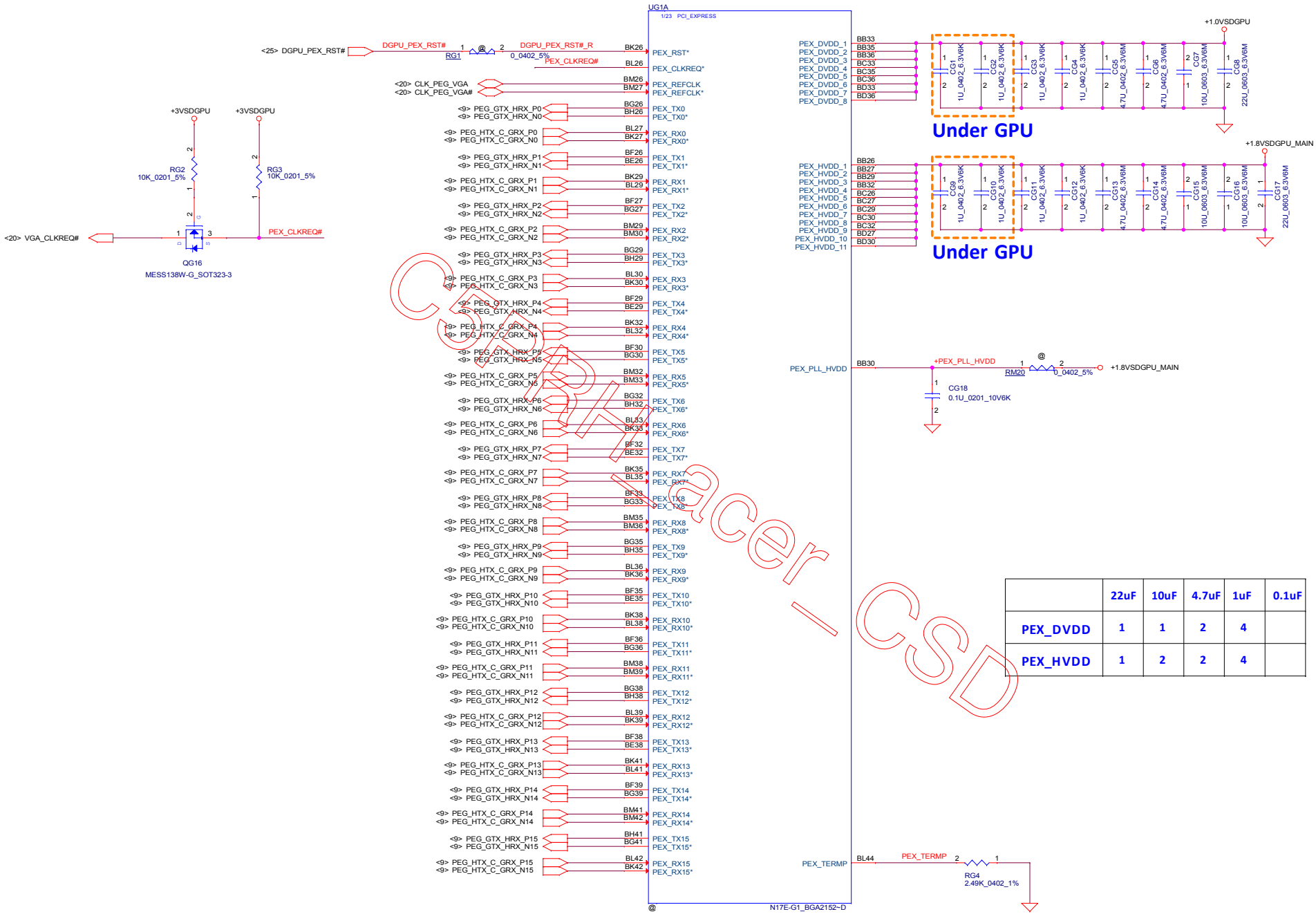
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **PCH(7/7)GND**

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

Date: Friday, March 31, 2017 Sheet 23 of 73



	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

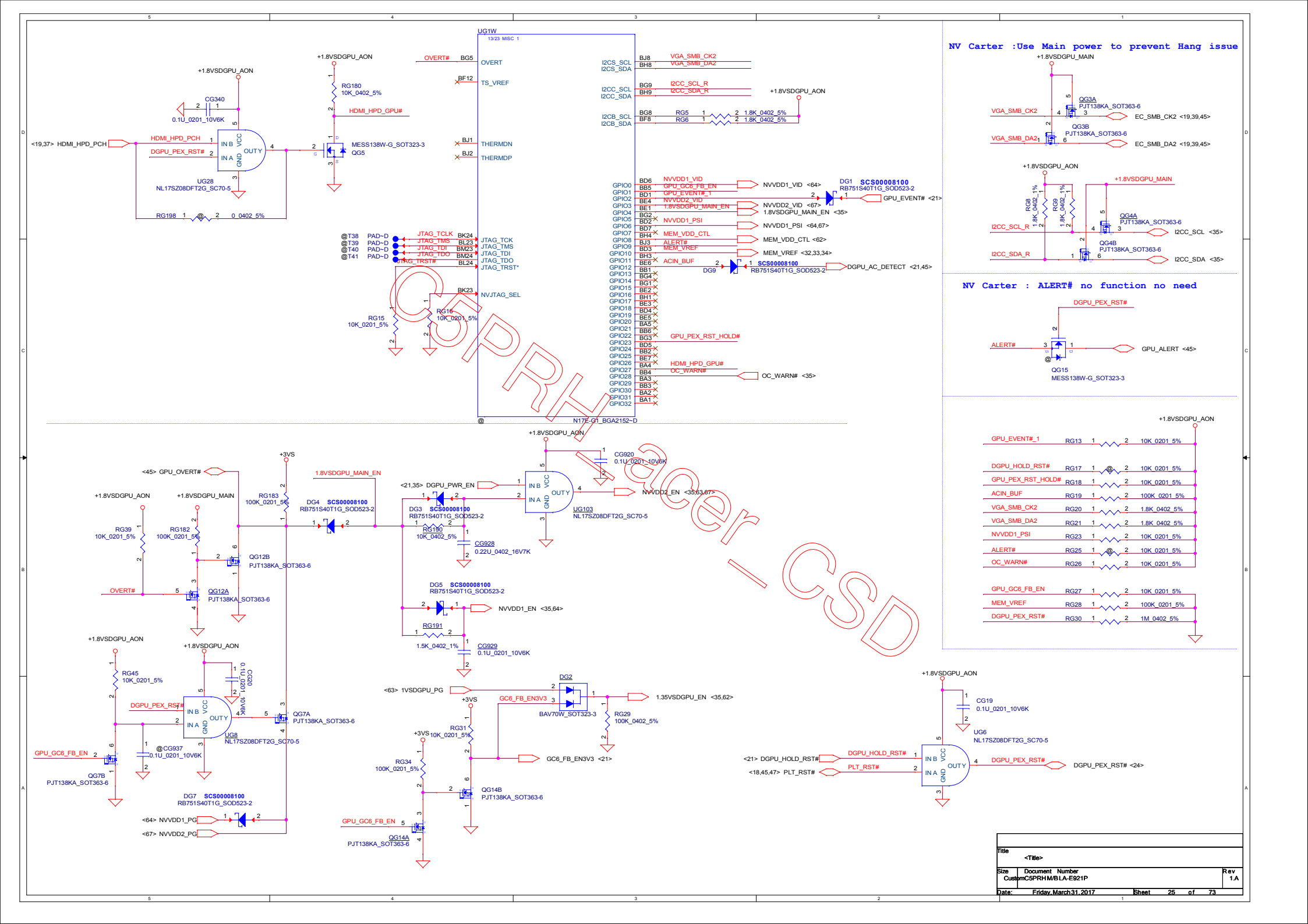
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(1/6) PCIE,GPIO**

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1.A

Date: Friday, March 31, 2017 Sheet 24 of 73


NV Carter :Use Main power to prevent Hang issue
NV Carter : ALERT# no function no need
UG1W
13/23 MISC 1
N17E-G1_BGA2152~D
UG28
NL17SZ08DFT2G_SC70-5
UG103
NL17SZ08DFT2G_SC70-5
UG8
NL17SZ08DFT2G_SC70-5
UG6
NL17SZ08DFT2G_SC70-5
MESS138W-G_SOT323-3
PJT138KA_SOT363-6
RB751S40T1G_SOD523-2
BAV70W_SOT323-3
+1.8VSDGPU_AON
+1.8VSDGPU_MAIN
+3VS
HDMI_HPD_PCH
HDMI_HPD_GPU#
DGPU_PEX_RST#
DGPU_PEX_RST_HOLD#
GPU_GC6_FB_EN
GPU_EVENT#_1
GPU_ALERT <45>
GPU_OVERT# <45>
DGPU_PWR_EN <21,35>
NVVDD1_VID <64>
NVVDD2_VID <67>
NVVDD1_PSI <64,67>
MEM_VDD_CTL <62>
MEM_VREF <32,33,34>
DGPU_AC_DETECT <21,45>
OC_WARN# <35>
NVJTAG_SEL
1.35VSDGPU_EN <35,62>
GC6_FB_EN3V3 <21>
DGPU_HOLD_RST# <21>
PLT_RST# <18,45,47>
DGPU_PEX_RST# <24>
EC_SMB_CK2 <19,39,45>
EC_SMB_DA2 <19,39,45>
I2CC_SCL <35>
I2CC_SDA <35>
NVVDD1_EN <35,64>
NVVDD2_EN <35,63,67>
<64> NVVDD1_PG
<67> NVVDD2_PG
<63> 1VSDGPU_PG
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Document Number
CustomC5PRHM/BLA-E921P
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1.A
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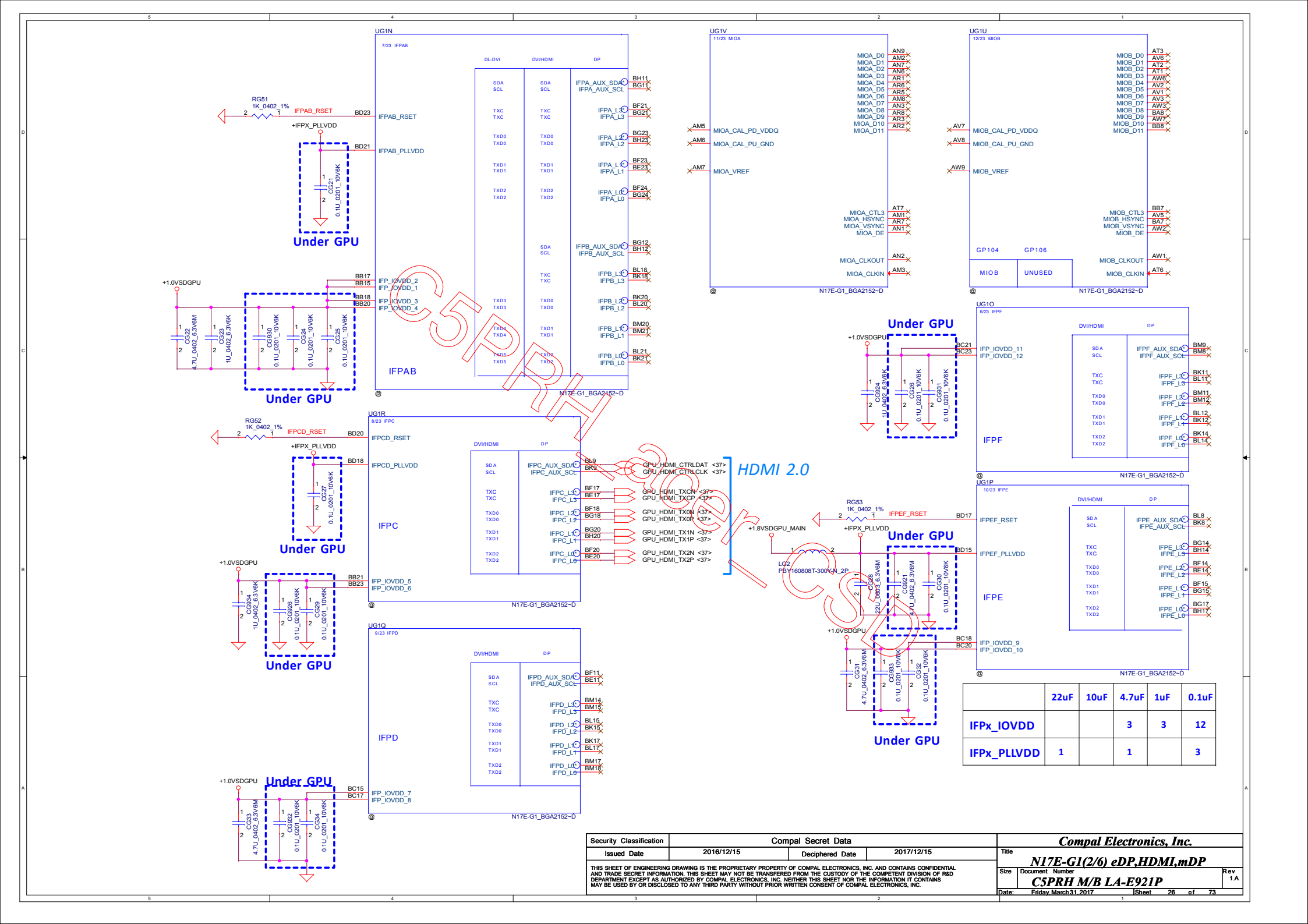


	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			3	3	12
IFPx_PLLVDD	1		1		3

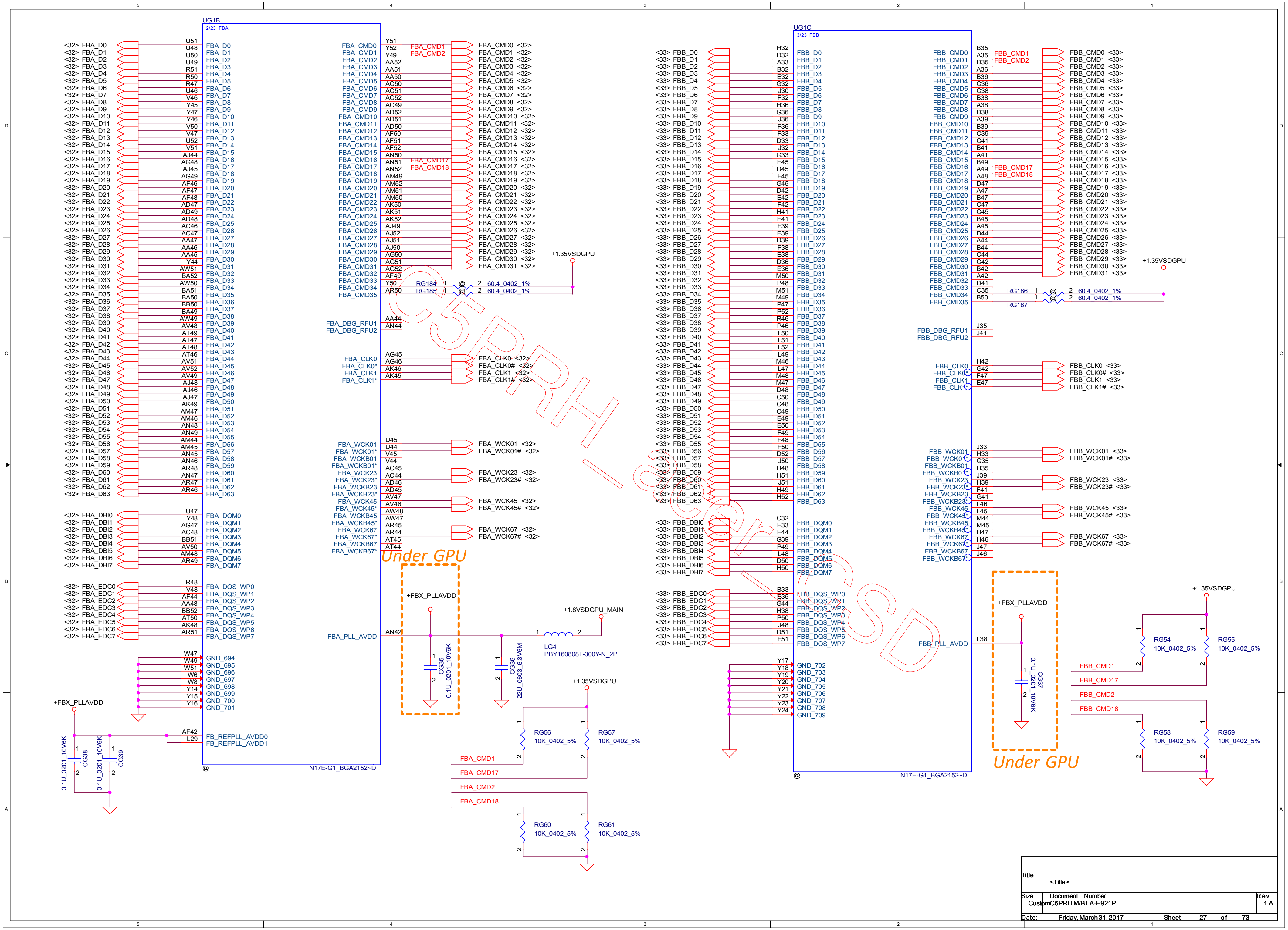
Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: N17E-G1(2/6) eDP,HDMI,mDP

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1A

Date: Friday, March 31, 2017 Sheet 26 of 73


UG1B
2/23 FBA
FBA_D0 … FBA_D63
FBA_DQM0 … FBA_DQM7
FBA_DQS_WP0 … FBA_DQS_WP7
GND_694 GND_695 GND_696 GND_697 GND_698 GND_699 GND_700 GND_701
FB_REFPLL_AVDD0
FB_REFPLL_AVDD1
FBA_CMD0 … FBA_CMD35
FBA_DBG_RFU1
FBA_DBG_RFU2
FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*
FBA_WCK01 FBA_WCK01* FBA_WCKB01 FBA_WCKB01* FBA_WCK23 FBA_WCK23* FBA_WCKB23 FBA_WCKB23* FBA_WCK45 FBA_WCK45* FBA_WCKB45 FBA_WCKB45* FBA_WCK67 FBA_WCK67* FBA_WCKB67 FBA_WCKB67*
FBA_PLL_AVDD
N17E-G1_BGA2152~D
<32> FBA_D0 … <32> FBA_D63
<32> FBA_DBI0 … <32> FBA_DBI7
<32> FBA_EDC0 … <32> FBA_EDC7
FBA_CMD0 <32> … FBA_CMD31 <32>
FBA_CLK0 <32> FBA_CLK0# <32> FBA_CLK1 <32> FBA_CLK1# <32>
FBA_WCK01 <32> FBA_WCK01# <32> FBA_WCK23 <32> FBA_WCK23# <32> FBA_WCK45 <32> FBA_WCK45# <32> FBA_WCK67 <32> FBA_WCK67# <32>
+1.35VSDGPU
RG184 60.4_0402_1%
RG185 60.4_0402_1%
Under GPU
+FBX_PLLAVDD
CG35 0.1U_0201_10V6K
CG36 22U_0603_6.3V6M
+1.8VSDGPU_MAIN
LG4 PBY160808T-300Y-N_2P
CG38 0.1U_0201_10V6K
CG39 0.1U_0201_10V6K
RG56 10K_0402_5%
RG57 10K_0402_5%
RG60 10K_0402_5%
RG61 10K_0402_5%
FBA_CMD1 FBA_CMD17 FBA_CMD2 FBA_CMD18
UG1C
3/23 FBB
FBB_D0 … FBB_D63
FBB_DQM0 … FBB_DQM7
FBB_DQS_WP0 … FBB_DQS_WP7
GND_702 GND_703 GND_704 GND_705 GND_706 GND_707 GND_708 GND_709
FBB_CMD0 … FBB_CMD35
FBB_DBG_RFU1
FBB_DBG_RFU2
FBB_CLK0 FBB_CLK0 FBB_CLK1 FBB_CLK1
FBB_WCK01 FBB_WCK01 FBB_WCKB01 FBB_WCKB01 FBB_WCK23 FBB_WCK23 FBB_WCKB23 FBB_WCKB23 FBB_WCK45 FBB_WCK45 FBB_WCKB45 FBB_WCKB45 FBB_WCK67 FBB_WCK67 FBB_WCKB67 FBB_WCKB67
FBB_PLL_AVDD
N17E-G1_BGA2152~D
<33> FBB_D0 … <33> FBB_D63
<33> FBB_DBI0 … <33> FBB_DBI7
<33> FBB_EDC0 … <33> FBB_EDC7
FBB_CMD0 <33> … FBB_CMD31 <33>
FBB_CLK0 <33> FBB_CLK0# <33> FBB_CLK1 <33> FBB_CLK1# <33>
FBB_WCK01 <33> FBB_WCK01# <33> FBB_WCK23 <33> FBB_WCK23# <33> FBB_WCK45 <33> FBB_WCK45# <33> FBB_WCK67 <33> FBB_WCK67# <33>
RG186 60.4_0402_1%
RG187 60.4_0402_1%
CG37 0.1U_0201_10V6K
RG54 10K_0402_5%
RG55 10K_0402_5%
RG58 10K_0402_5%
RG59 10K_0402_5%
FBB_CMD1 FBB_CMD17 FBB_CMD2 FBB_CMD18
Under GPU
C5PRH_acer_CSD
Title
<Title>
Size Document Number Rev
Custom C5PRH M/B LA-E921P 1.A
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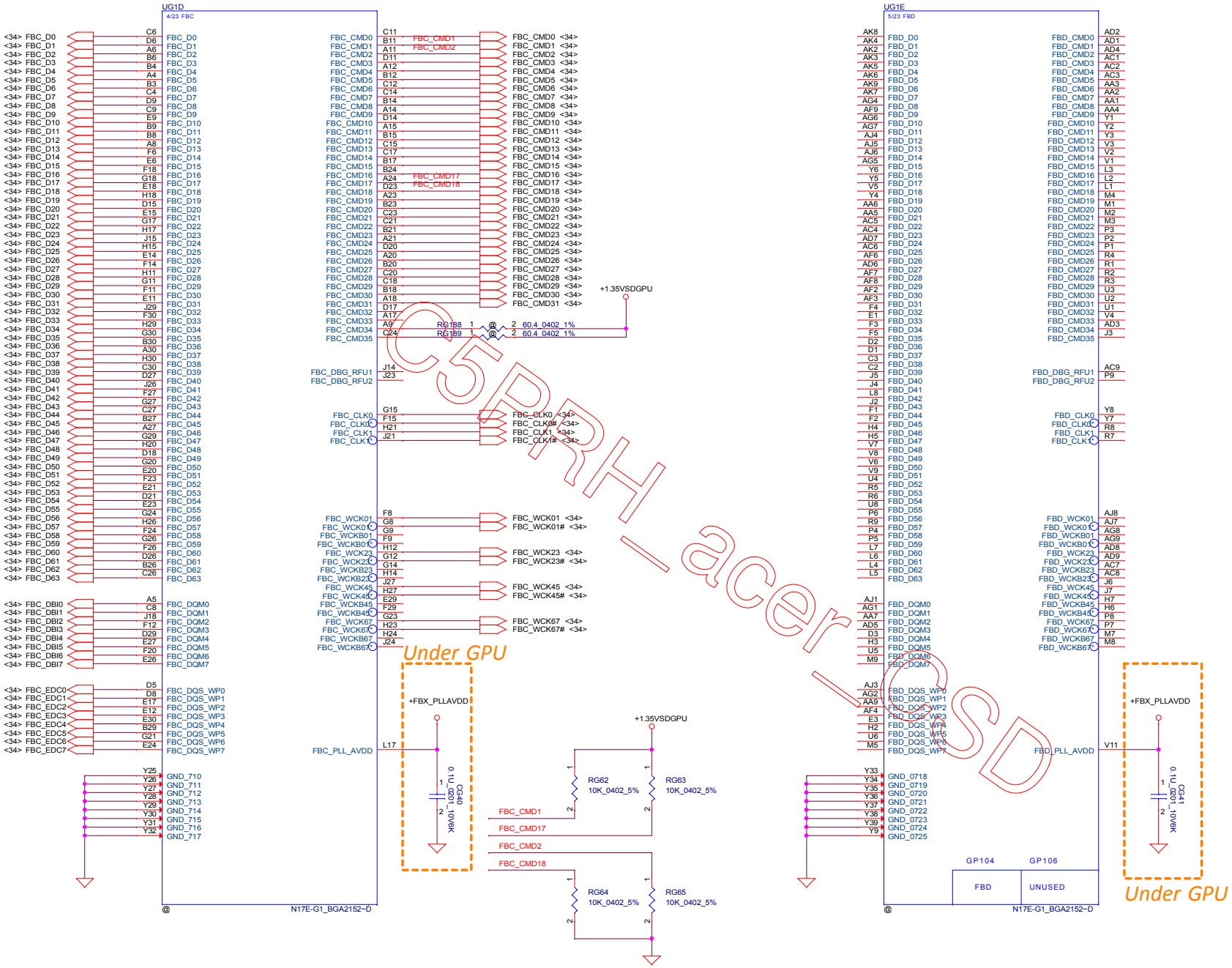

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(3/6) MEM Interface**

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1A

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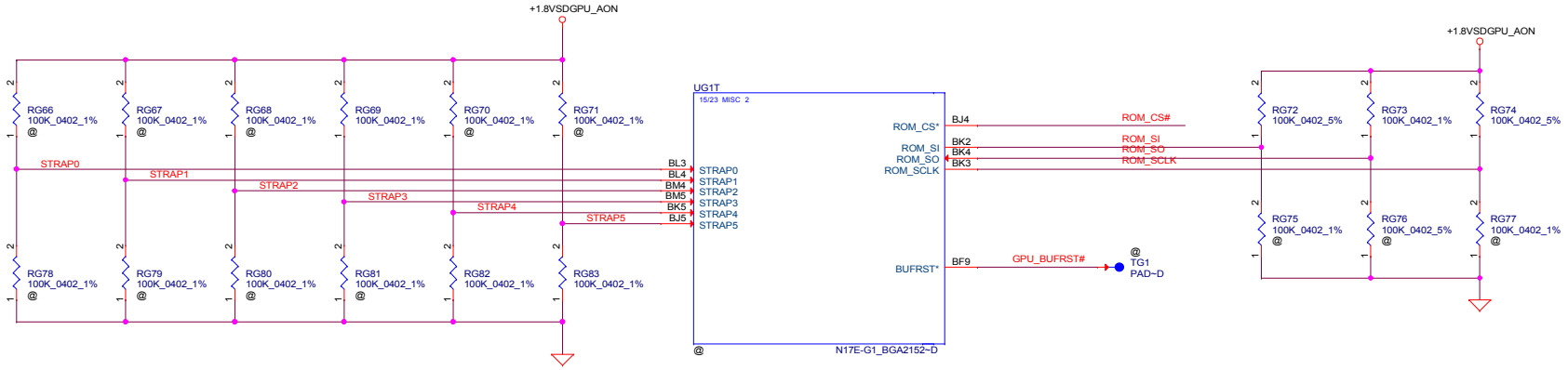

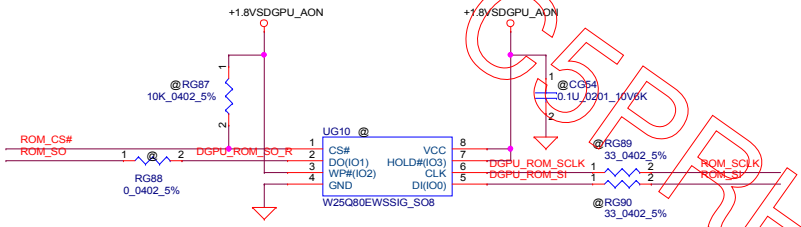

DGPU VBIOS ROM

Table 2. N17E-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V[2]	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production ready
		1.35V and 1.5V[2]	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production ready
		1.35V and 1.55V[2]	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.55V[2]	Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	Full	Post production ready
		1.35V and 1.55V[2]	Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	Full	Post production ready

Notes:
1. For N17E-G1, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-G1 runs WCLK up to 3000 MHz with FBVDD = 1.35V. DVS is required to run WCLK > 3000 MHz.

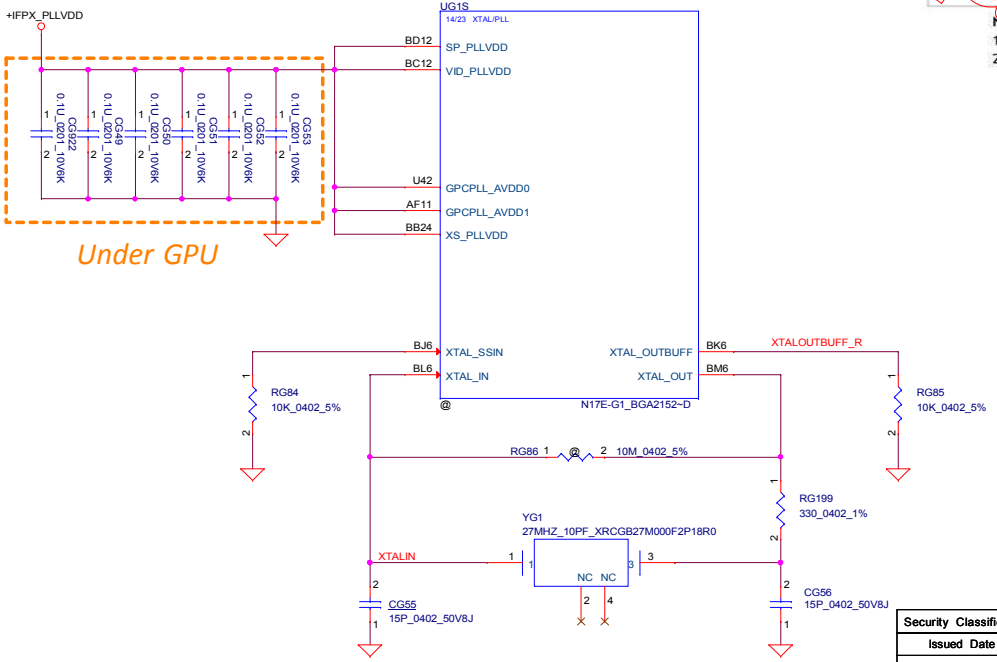

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)

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Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: N17E-G1(6/6) Strap Pin,ROM

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1.A

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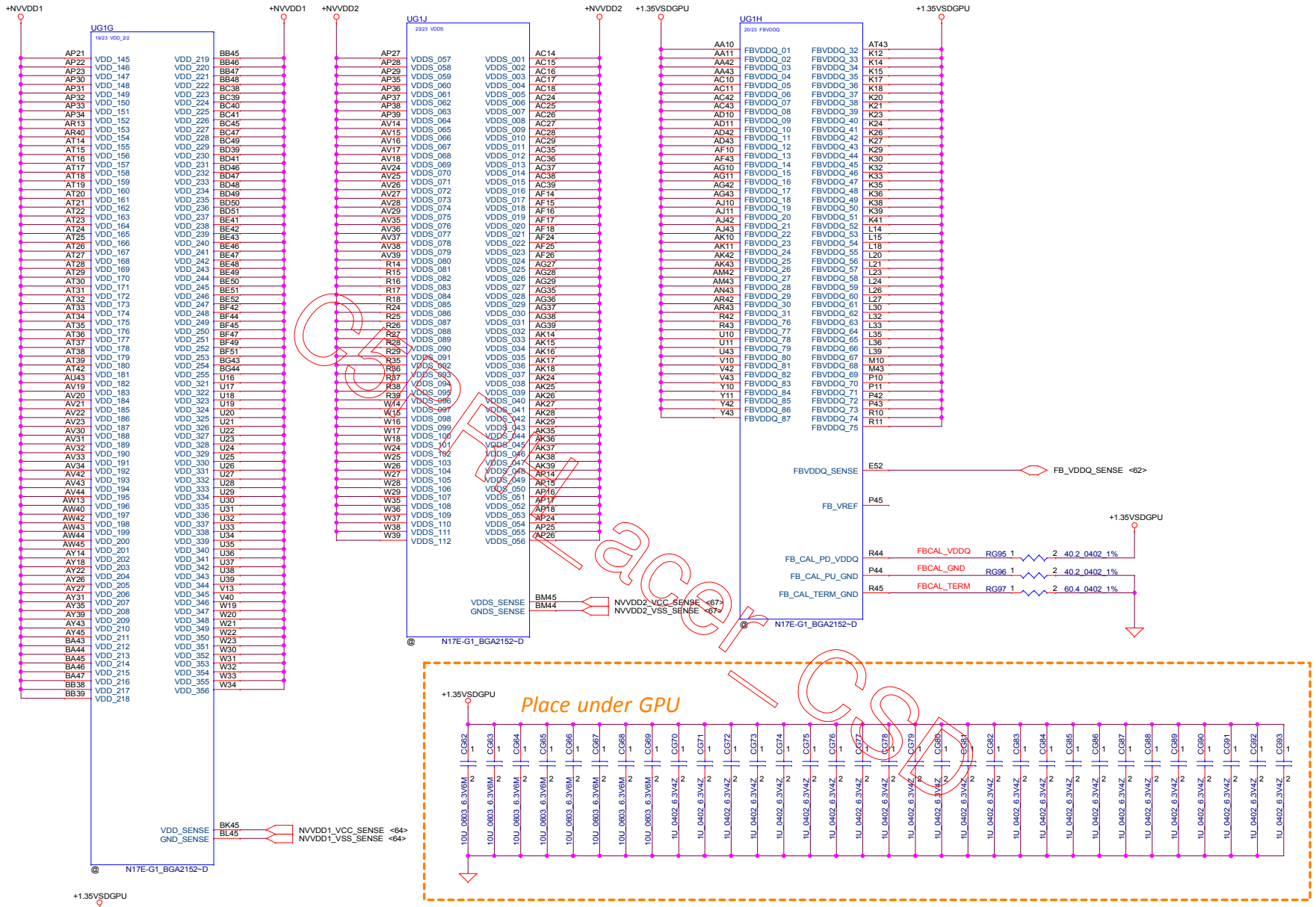

	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ	1	9	13		24	

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: N17E-G1(4/6) Power

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1.A

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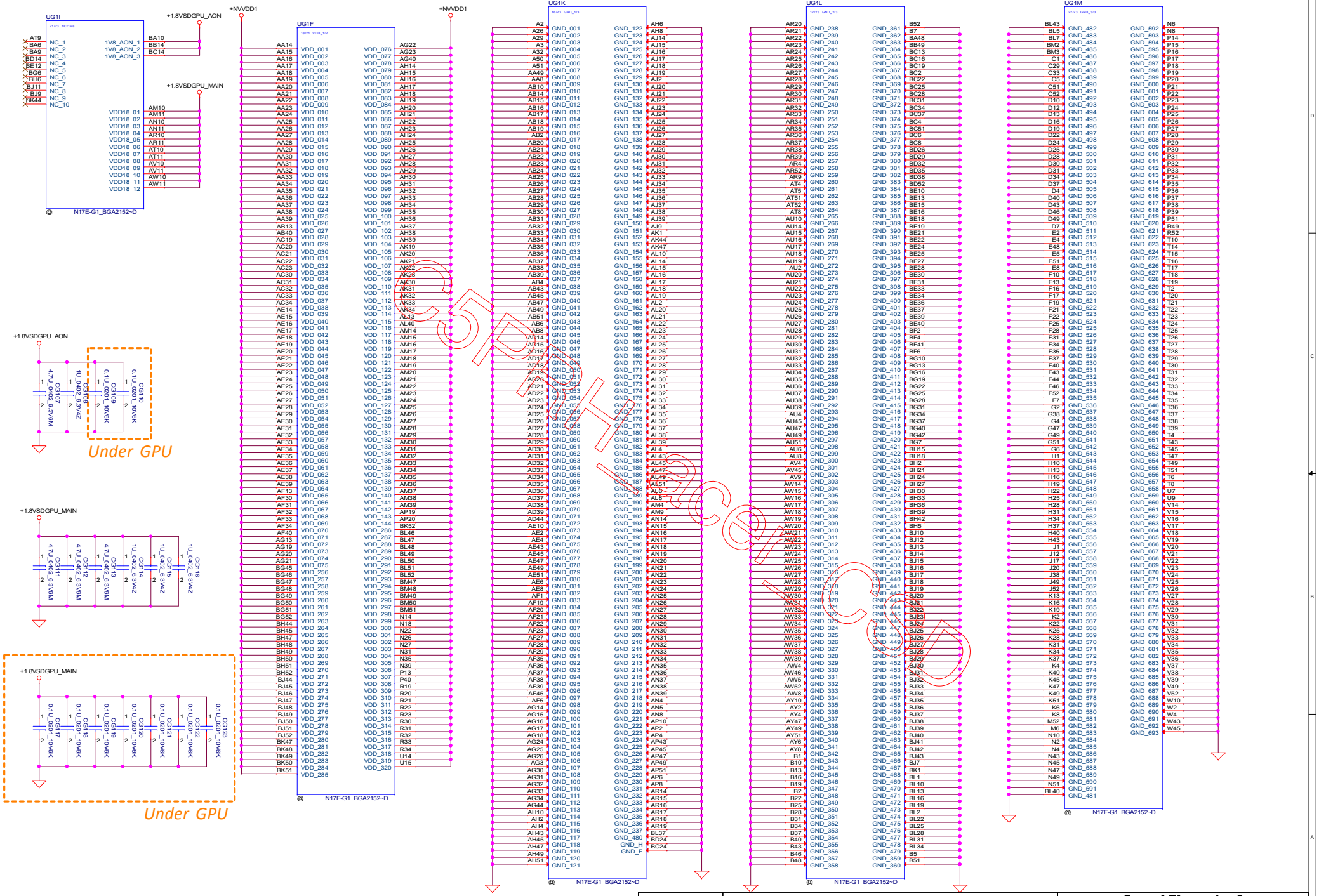

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Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **N17E-G1(5/6) Power,GND**

Size	Document Number	Rev
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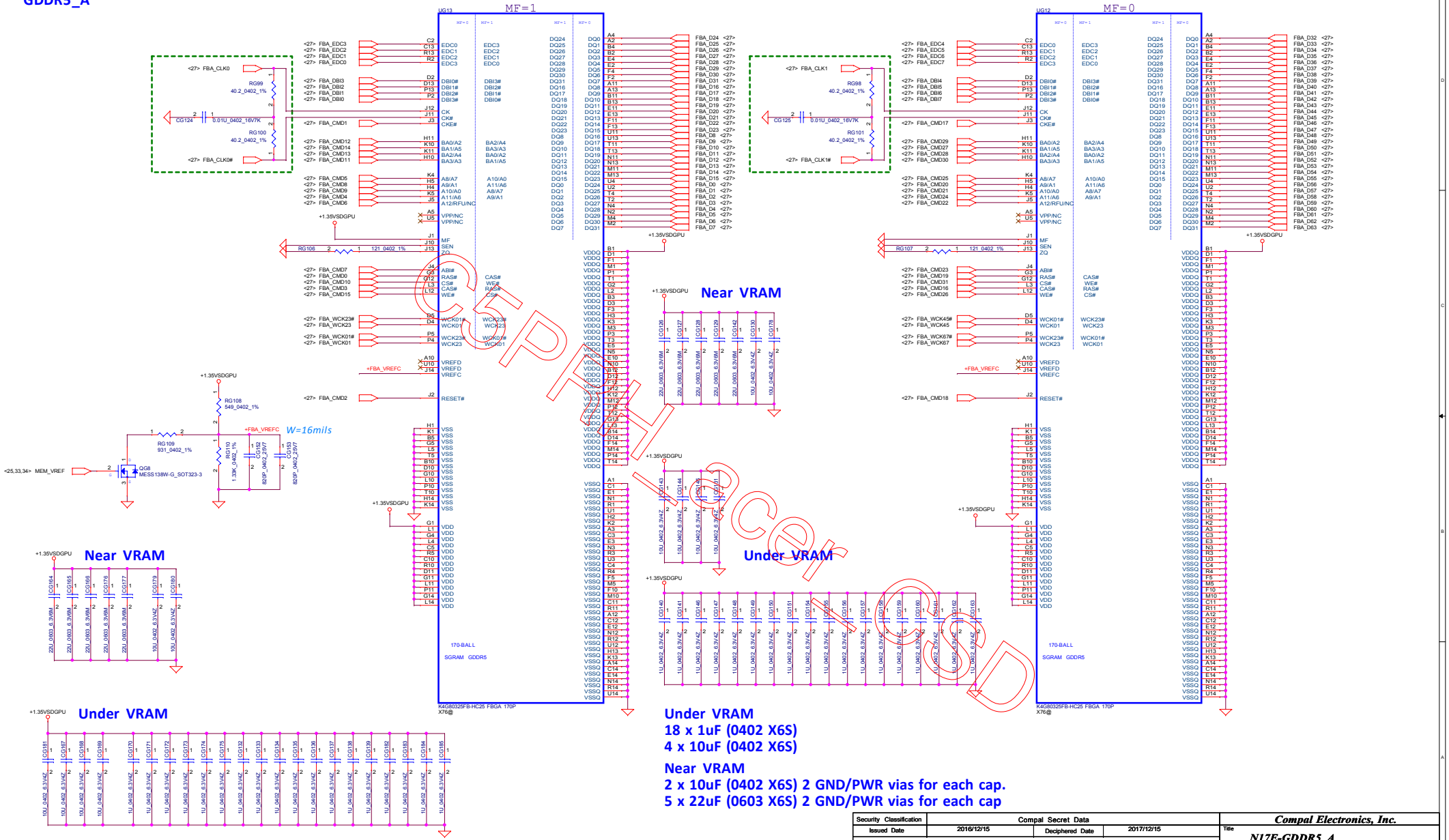
GDDR5_A



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Title: N17E-GDDR5_A			
Size	Document Number: C5PRH M/B LA-E921P		Rev: 1.A
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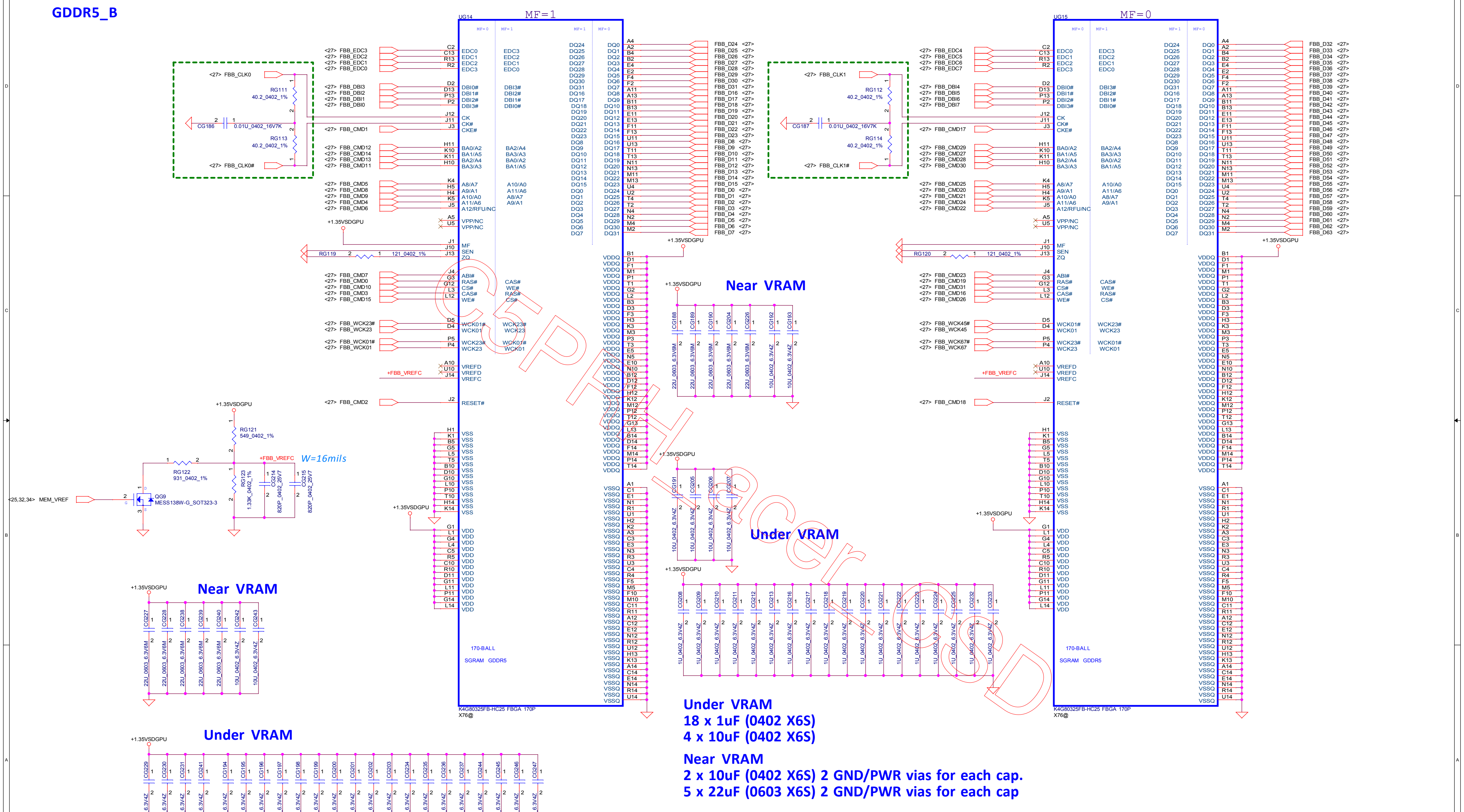

Under VRAM
18 x 1uF (0402 X6S)
4 x 10uF (0402 X6S)

Near VRAM
2 x 10uF (0402 X6S) 2 GND/PWR vias for each cap.
5 x 22uF (0603 X6S) 2 GND/PWR vias for each cap

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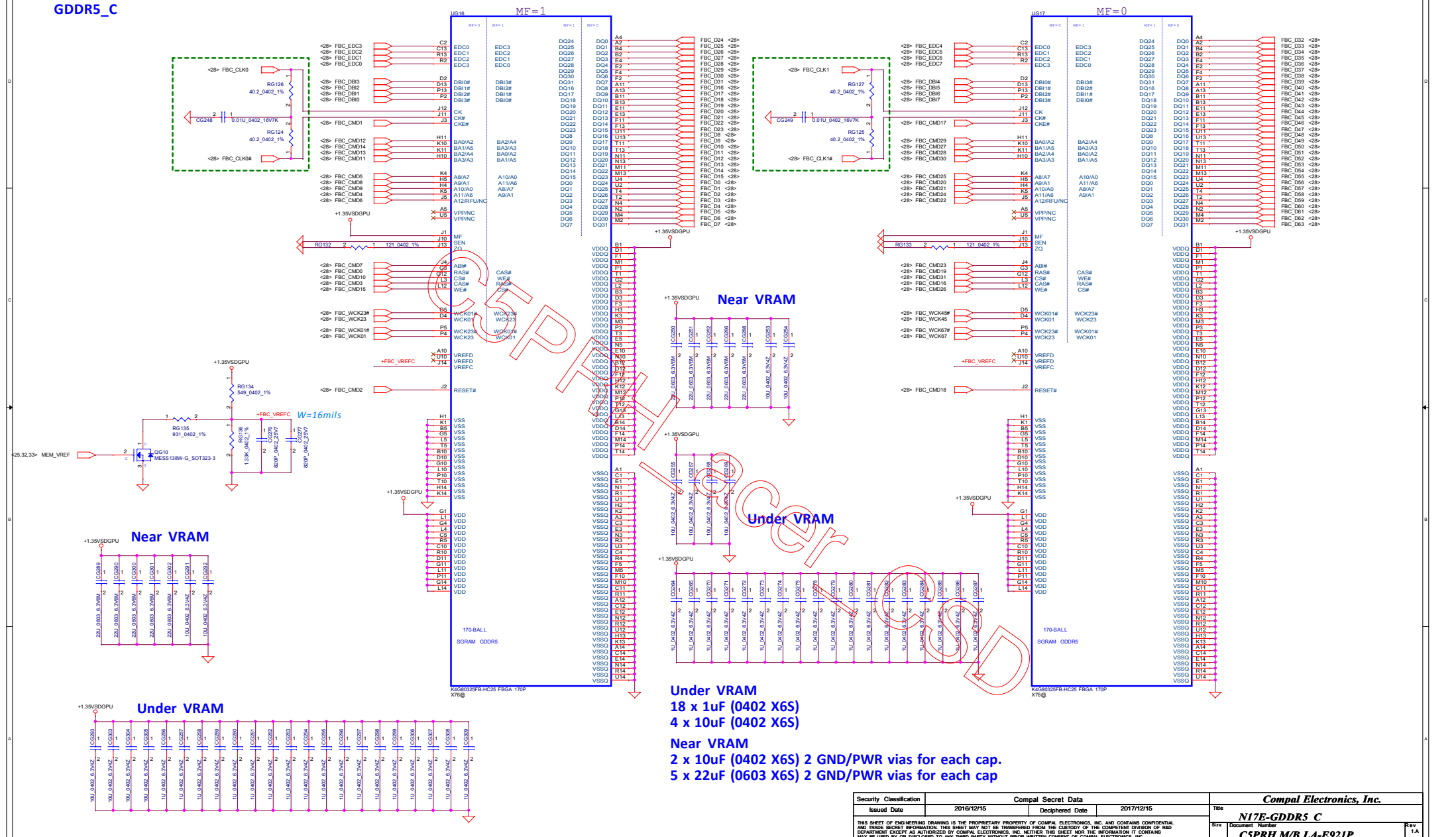
				Size / Document Number: C5PRH M/B LA-E921P / Rev 1.A
				Date: Friday, March 31, 2017 / Sheet 33 of 73



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.			
Title: N17E-GDDR5_C			
Size	Document Number: C5PRH M/B LA-E921P		Rev: 1.A
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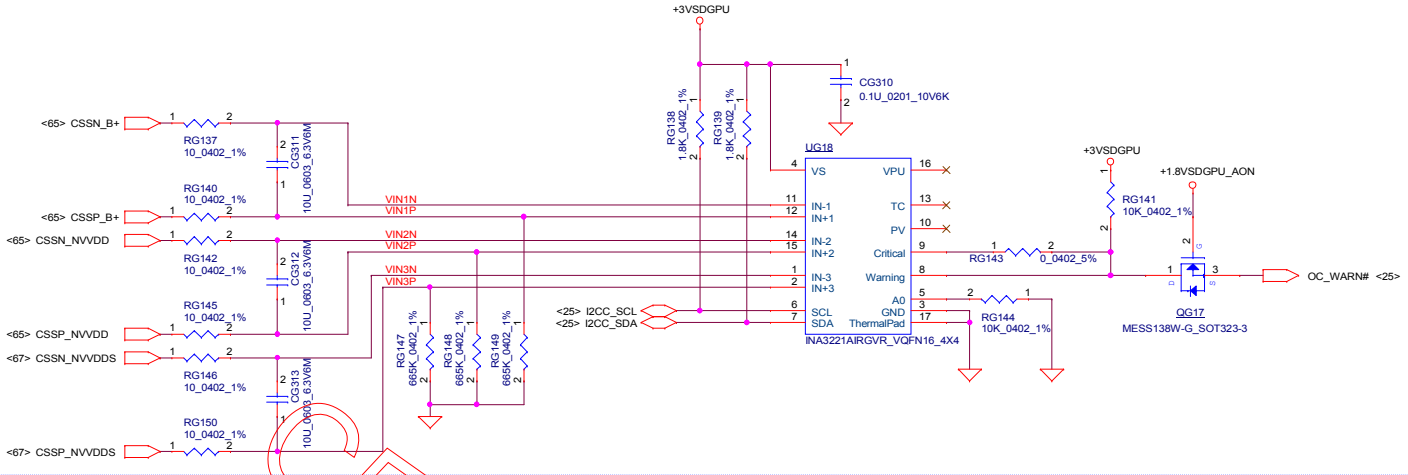
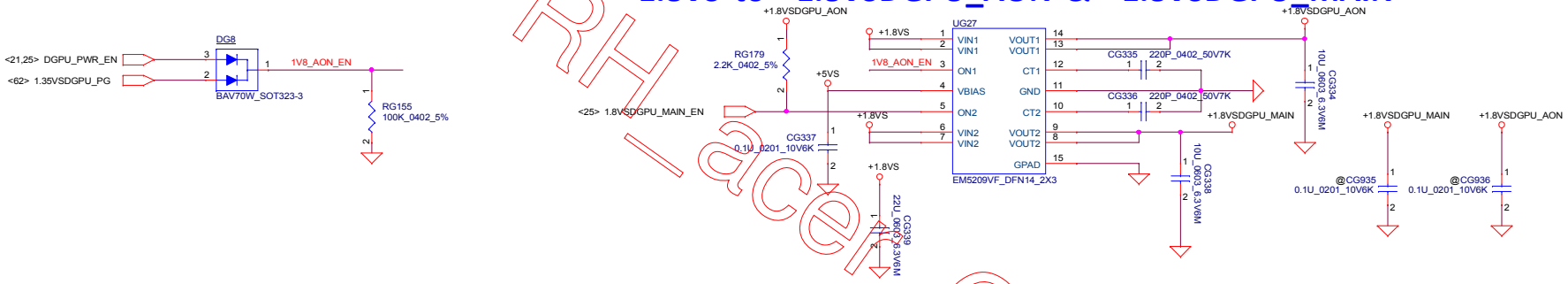
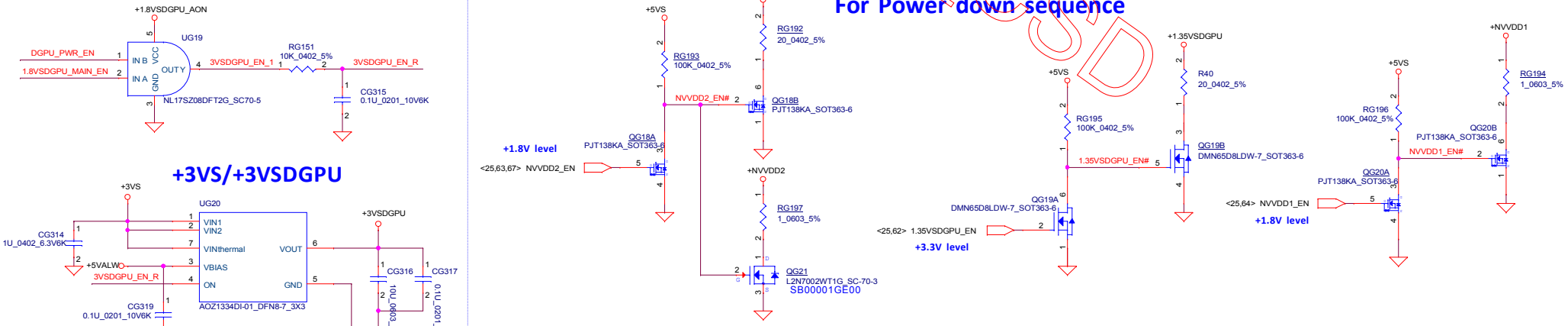


VGA DC inferface

+1.8VS to +1.8VSDGPU_AON & +1.8VSDGPU_MAIN



For Power down sequence



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: GPU power control

Size | Document Number: C5PRH M/B LA-E921P | Rev: 1A

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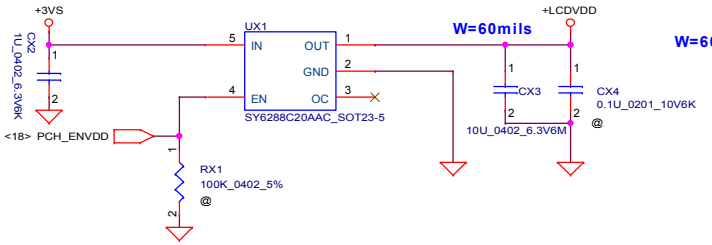
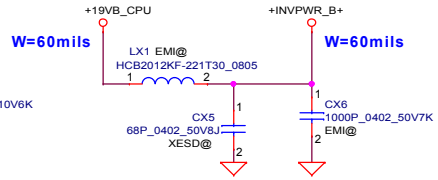
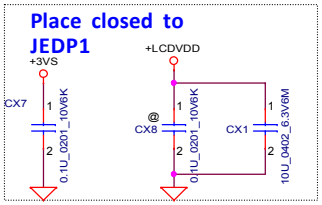
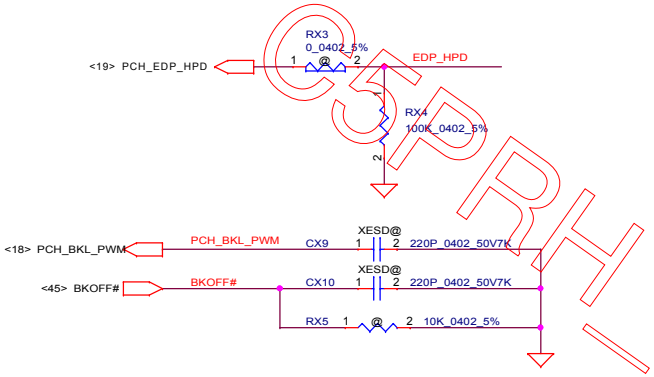
LCD POWER CIRCUIT



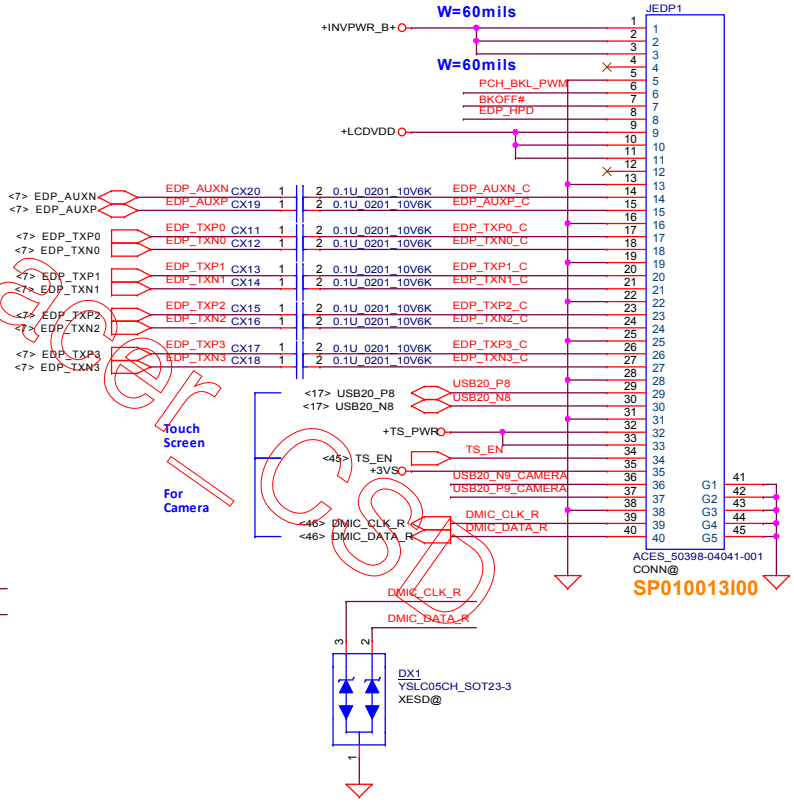
SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04



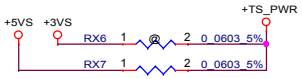




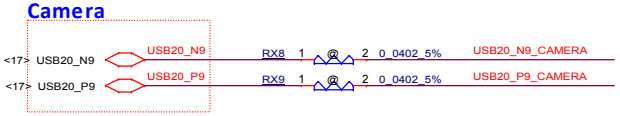
LED PANEL Conn.



USB Touch Screen



Camera



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **eDP CONN.**

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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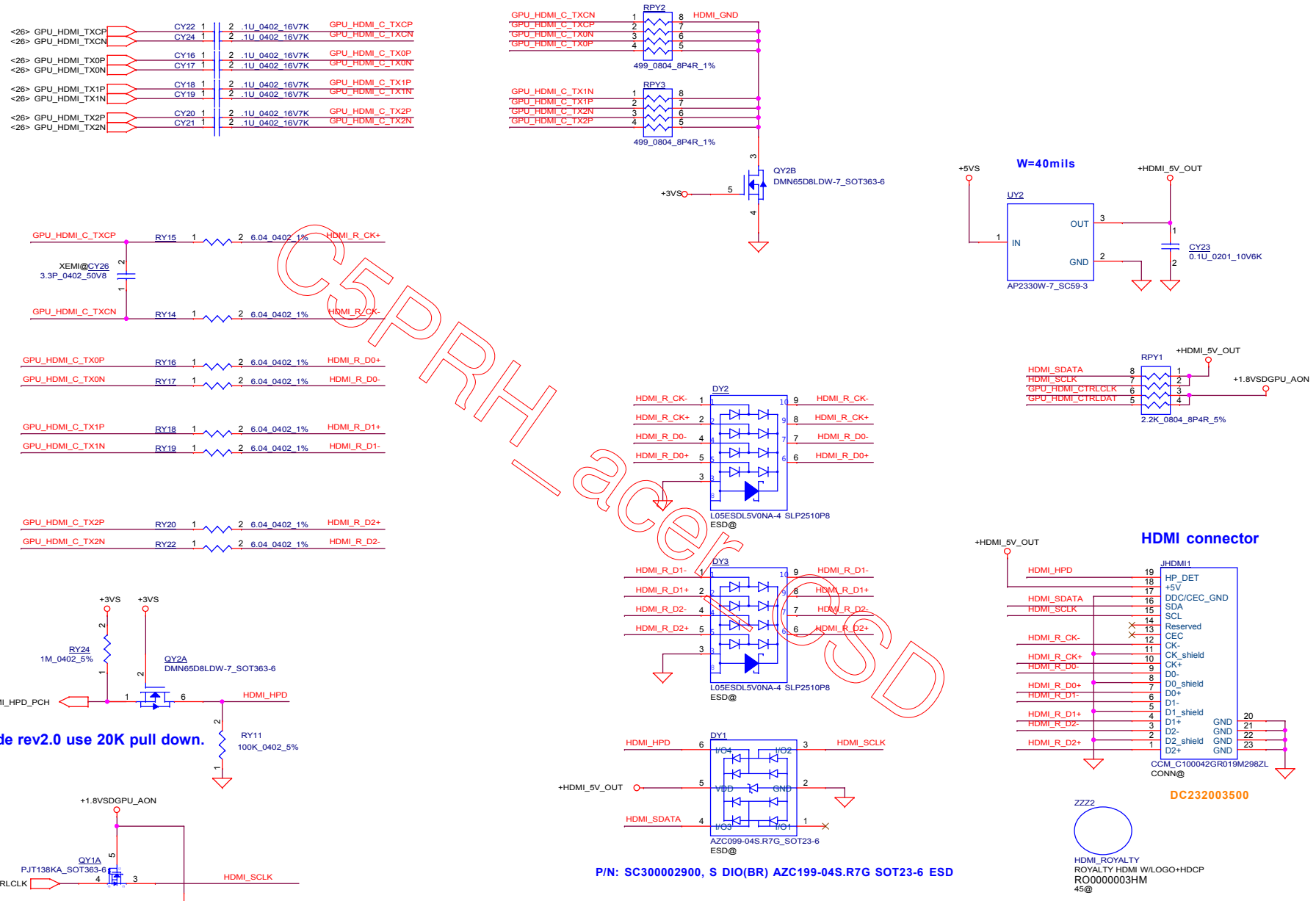

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: **HDMI CONN.**

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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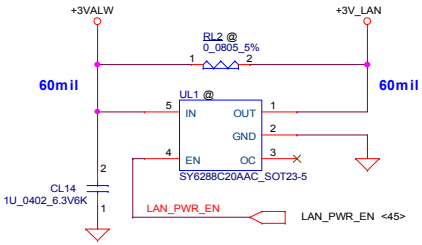
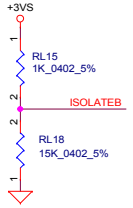
LAN-RTL8411B

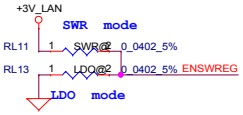


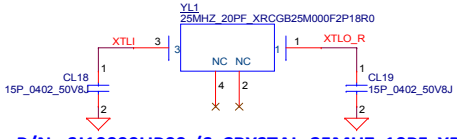
From EC

High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

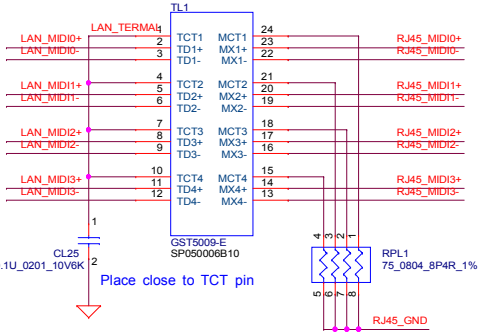
+3V_LAN Rising time must >0.5ms and <100ms

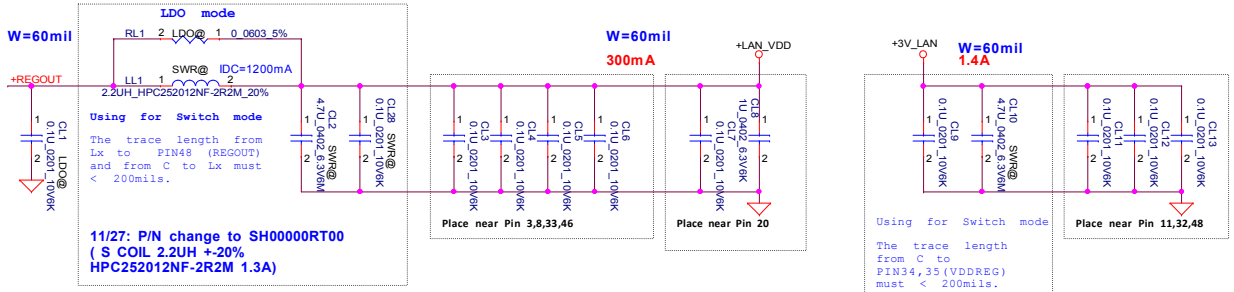






P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

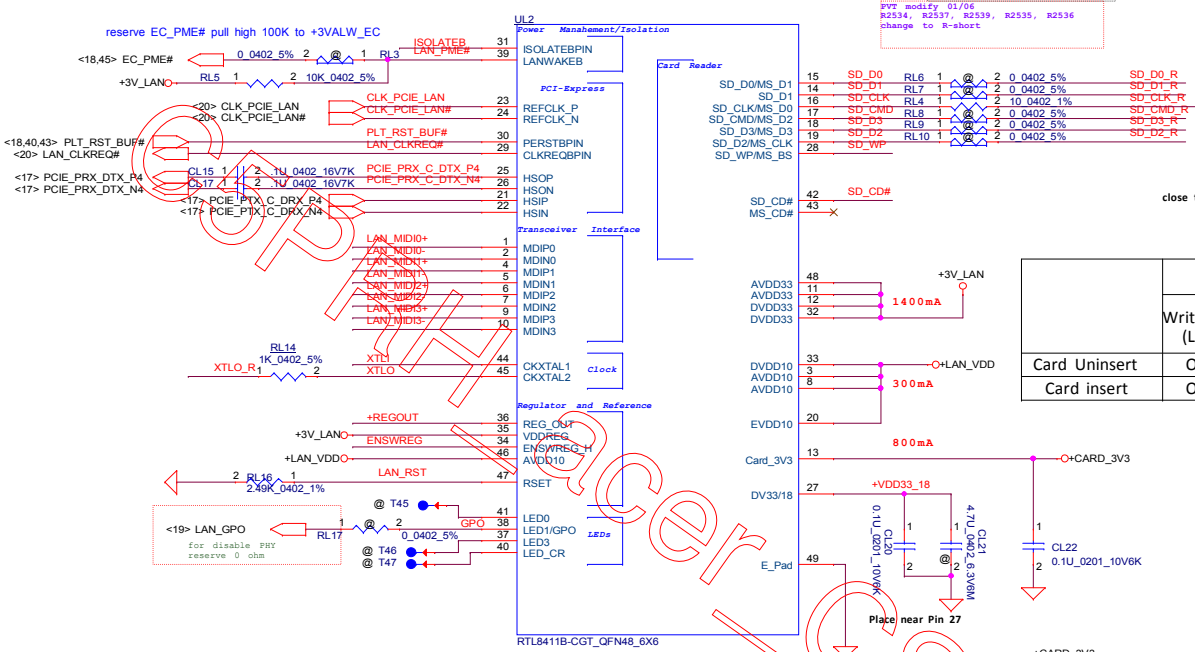




11/27: P/N change to SH00000RT00
(S COIL 2.2UH +-20%
HPC252012NF-2R2M 1.3A)

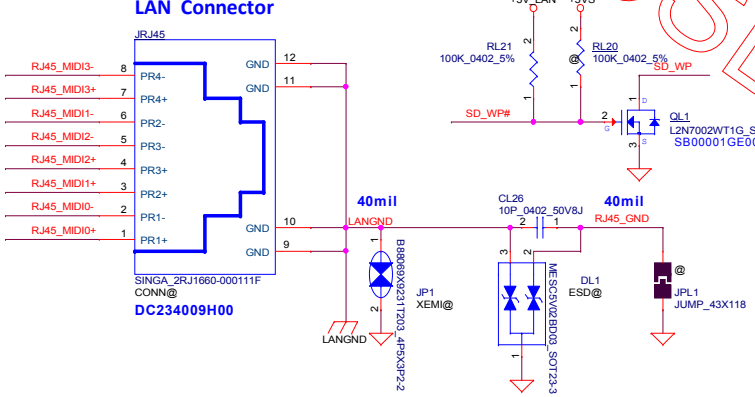
PVT modify 01/06
R2534, R2537, R2539, R2535, R2536
change to R-short

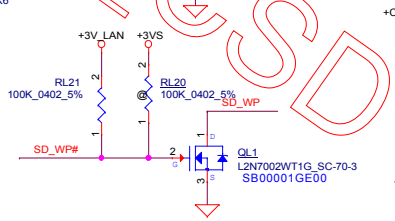
reserve EC_PME# pull high 100K to +3VALW_EC



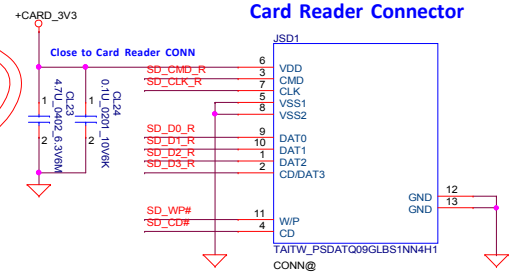
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

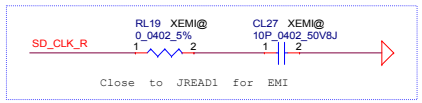
LAN Connector





Card Reader Connector





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Compal Electronics, Inc.	
Title	LAN RTL8411H
Size / Custom	Document Number: C5PRH M/B LA-E921P
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Date:	Friday, March 31, 2017
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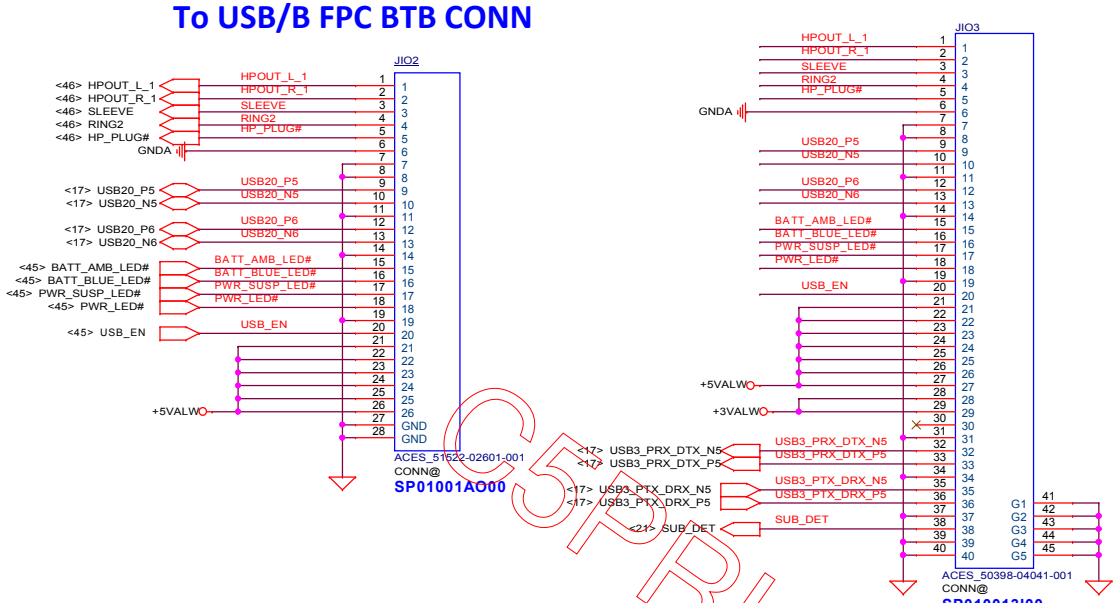
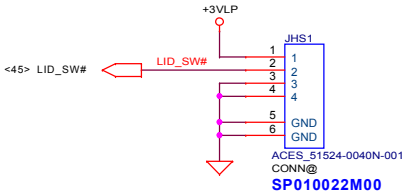
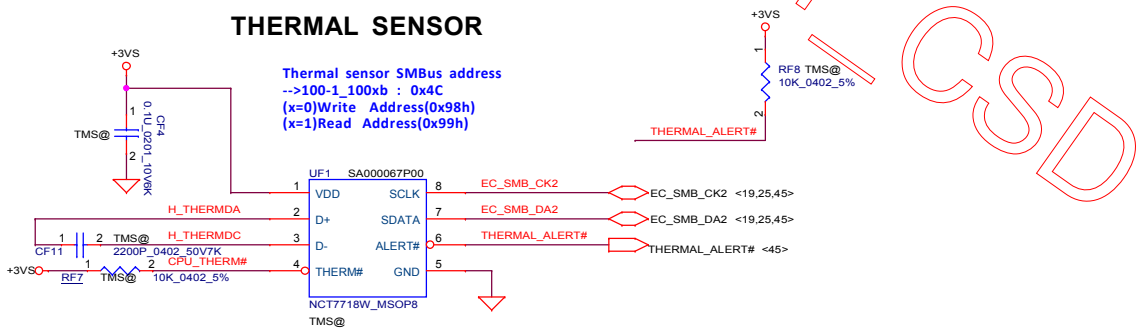
To USB/B FPC BTB CONN



To Hall sensor/B



THERMAL SENSOR



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: FUN/B & LED/B

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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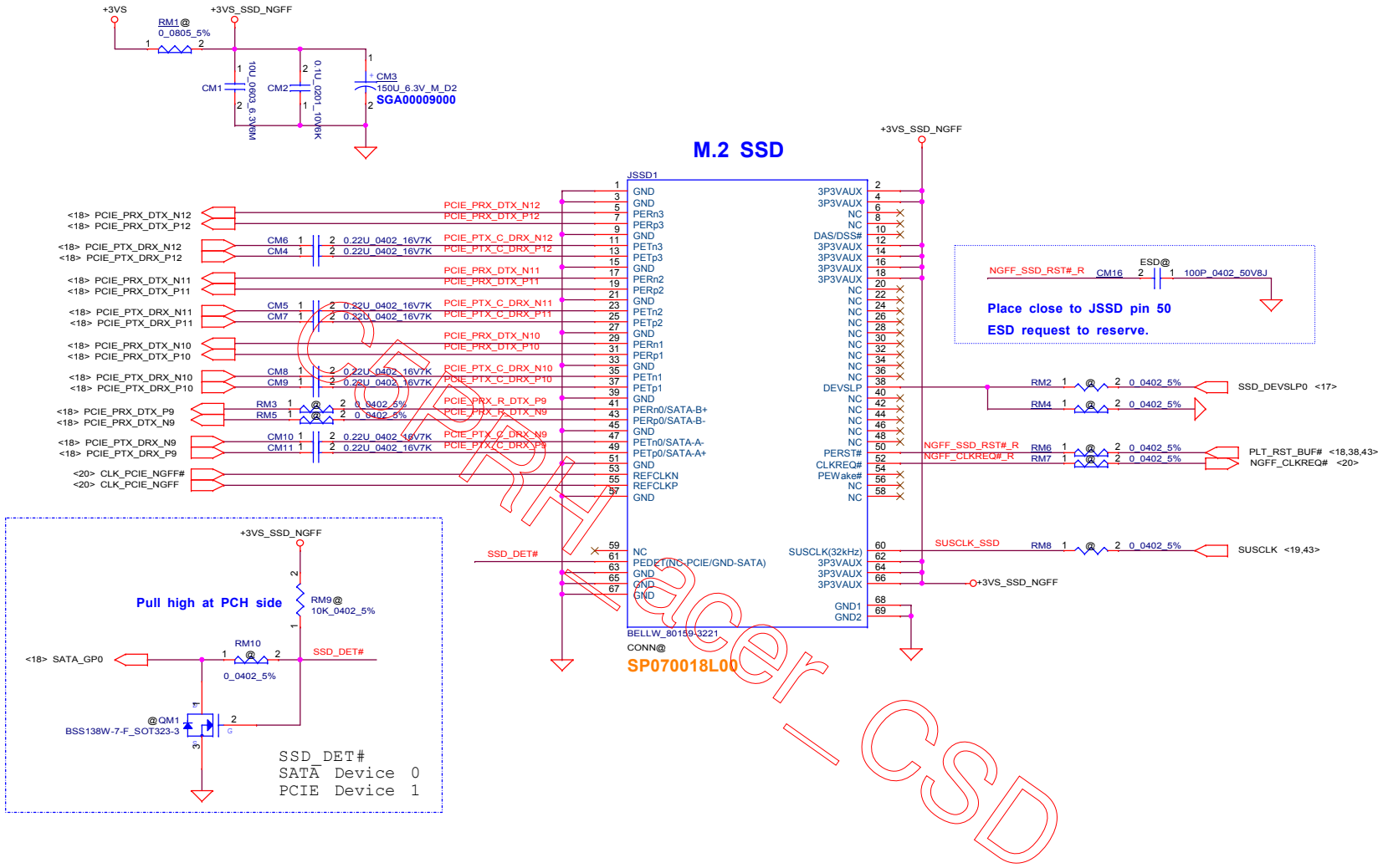

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Compal Electronics, Inc.			
Title: mSATA-SSD			
Size: Custom	Document Number: C5PRH M/B LA-E921P		Rev: 1.A
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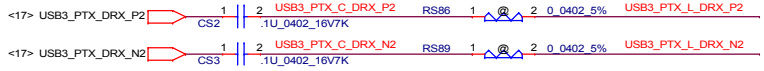
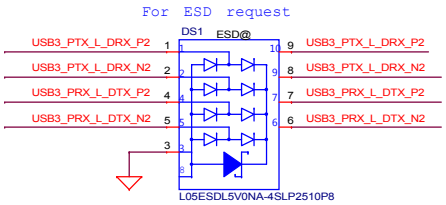
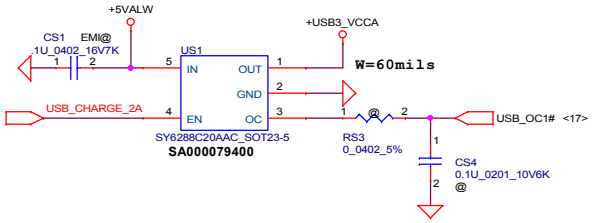
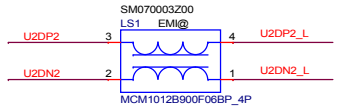
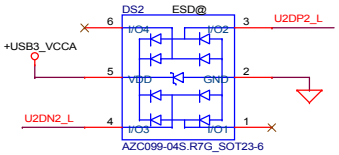
USB3.0

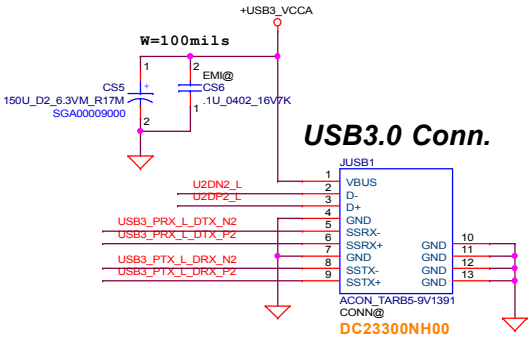


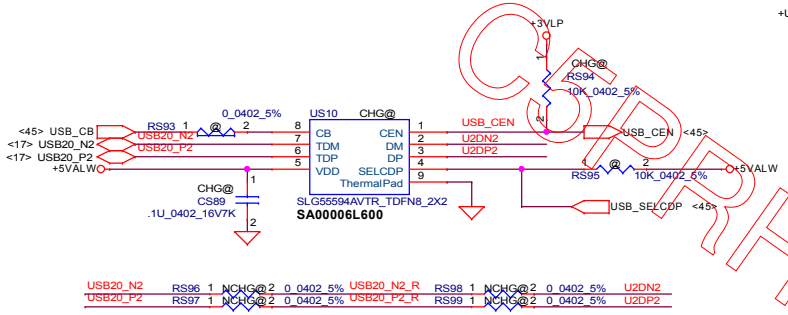












USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.	
Title	USB3.0 Conn/USB Charger
Size: Custom	Document Number: C5PRH M/B LA-E921P
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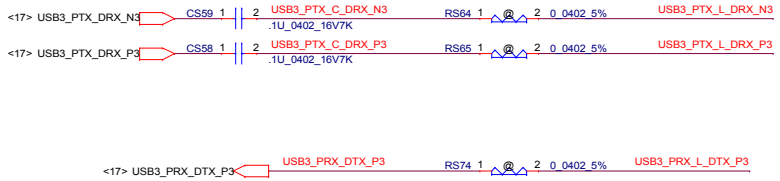
USB3.0 (Port 3)



USB3.0 (Port 4)

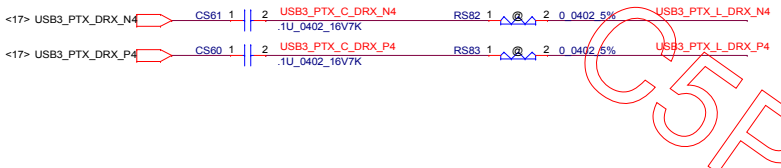
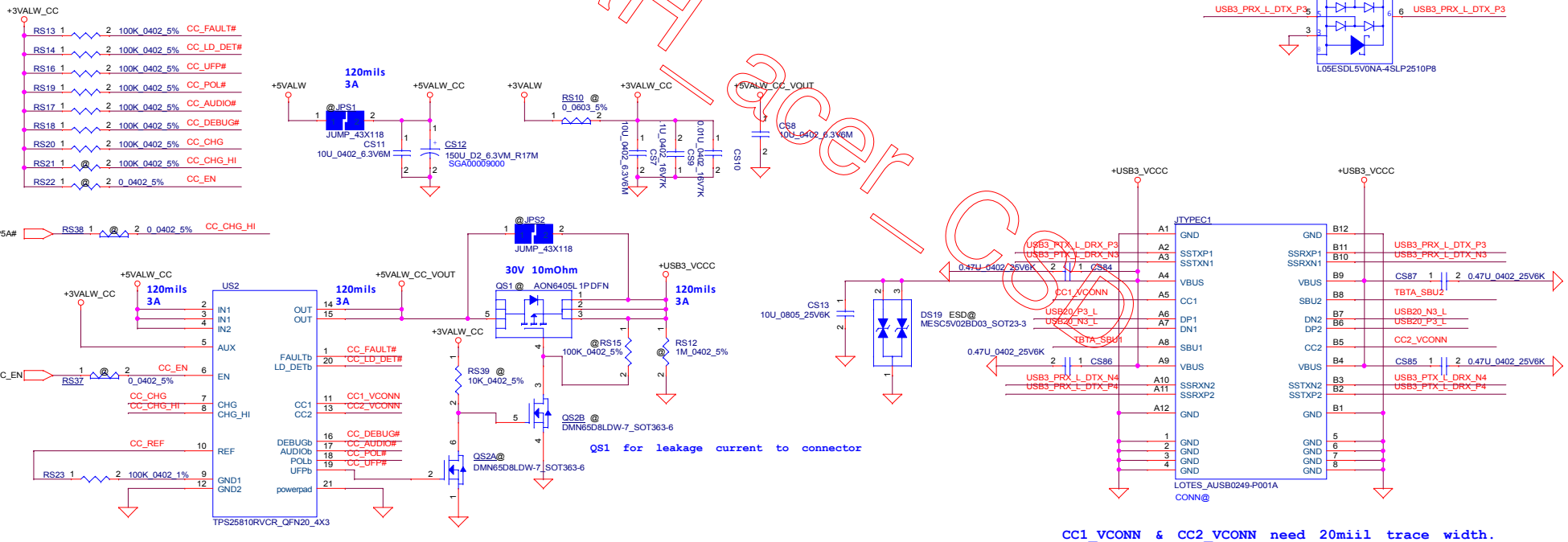


Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: CC+USB TYPE C

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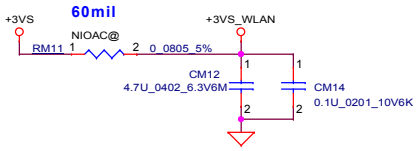
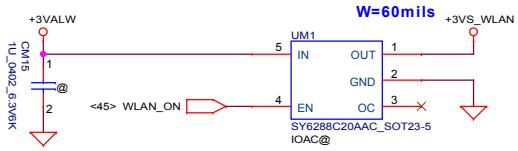
Wireless LAN

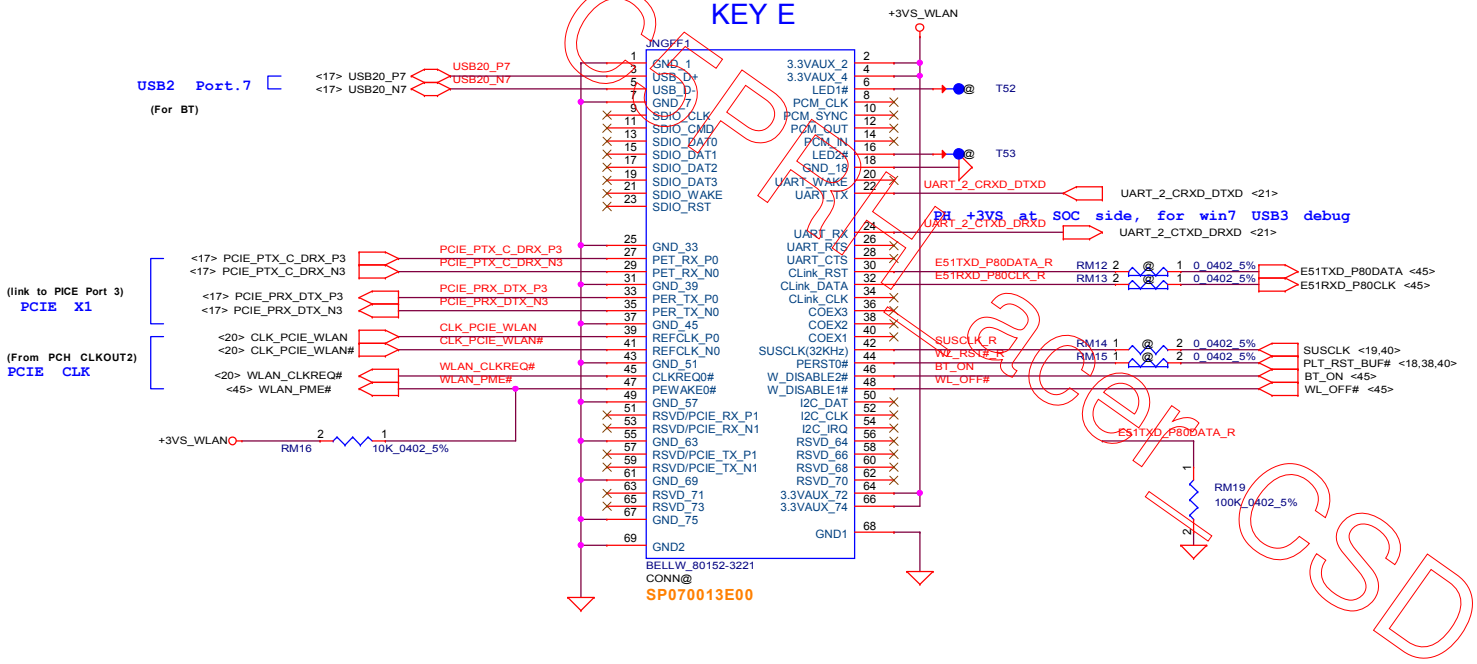




NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I)(I/O)(3.3)	GND	63
60	I2C CLK (O)(O/3.3)	Reserved/PETn1	61
58	I2C DATA (IO)(O/3.3)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(O/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(O/3.3V)	PEWakeO# (IO)(O/3.3V)	55
52	PERST0# (O)(O/3.3V)	CLKREQO# (IO)(O/3.3V)	53
50	SUSCLK(32kHz) (O)(O/3.3V)	GND	51
48	COEX1 (I/O)(O/1.8V)	REFCLKN0	49
46	COEX2(I/O)(O/1.8V)	REFCLKP0	47
44	COEX3(I/O)(O/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(O/1.8V)	PETn0	37
34	UART CTS (I)(O/1.8V)	PETp0	35
32	UART Tx (O)(O/1.8V)	GND	33
	Reserved	Reserved	
22	UART Rx (I)(O/1.8V)	SDIO Reset# (O)(O/1.8V)	23
20	UART Wake# (I)(O/3.3V)	SDIO Wake# (I)(O/1.8V)	21
18	GND	SDIO DAT3(IO)(O/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(O/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(O/1.8V)	SDIO DAT1(IO)(O/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(O/1.8V)	SDIO DAT0(IO)(O/1.8V)	13
10	PCM_SYNC/I2S WS (O)(O/1.8V)	SDIO CMD(IO)(O/1.8V)	11
8	PCM_CLK/I2S SCK (O)(O/1.8V)	SDIO CLK(IO)(O/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

KEY E



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Compal Electronics, Inc.	
Title	M.2 Key E (WLAN)
Size / Document Number	Custom / C5PRH M/B LA-E921P
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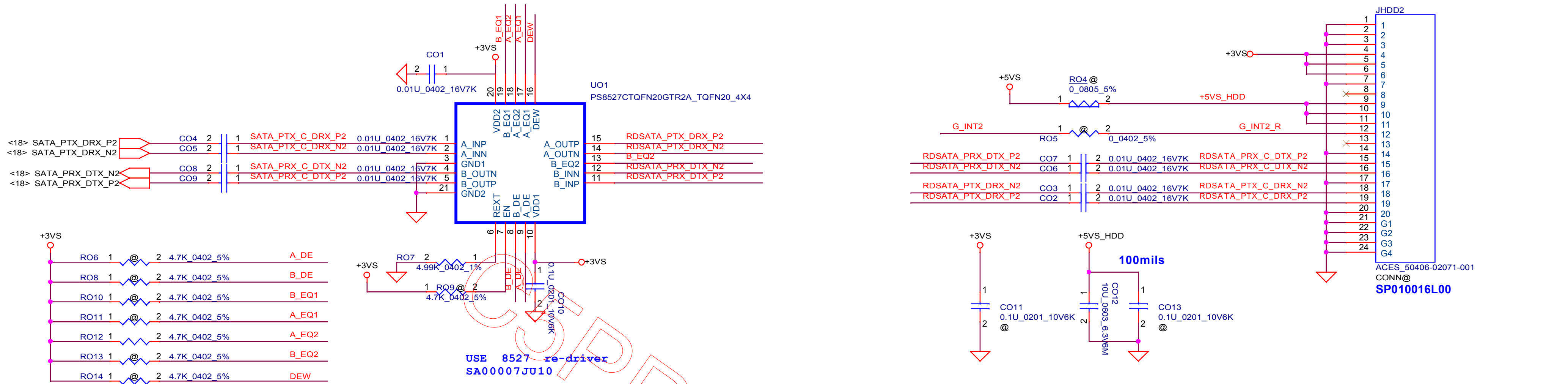
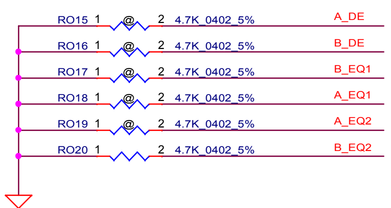
SATA Re-Driver and cable HDD Conn.





Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

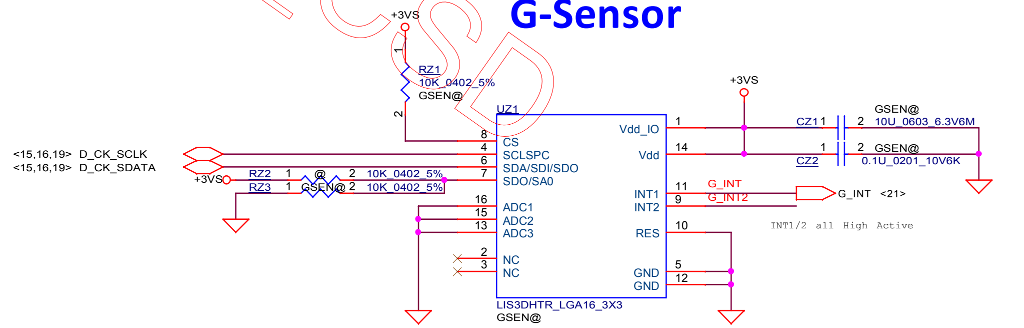
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

G-Sensor



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Compal Electronics, Inc.

Title: HDD/ Re-Driver/ G-sensor

Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev 1.A

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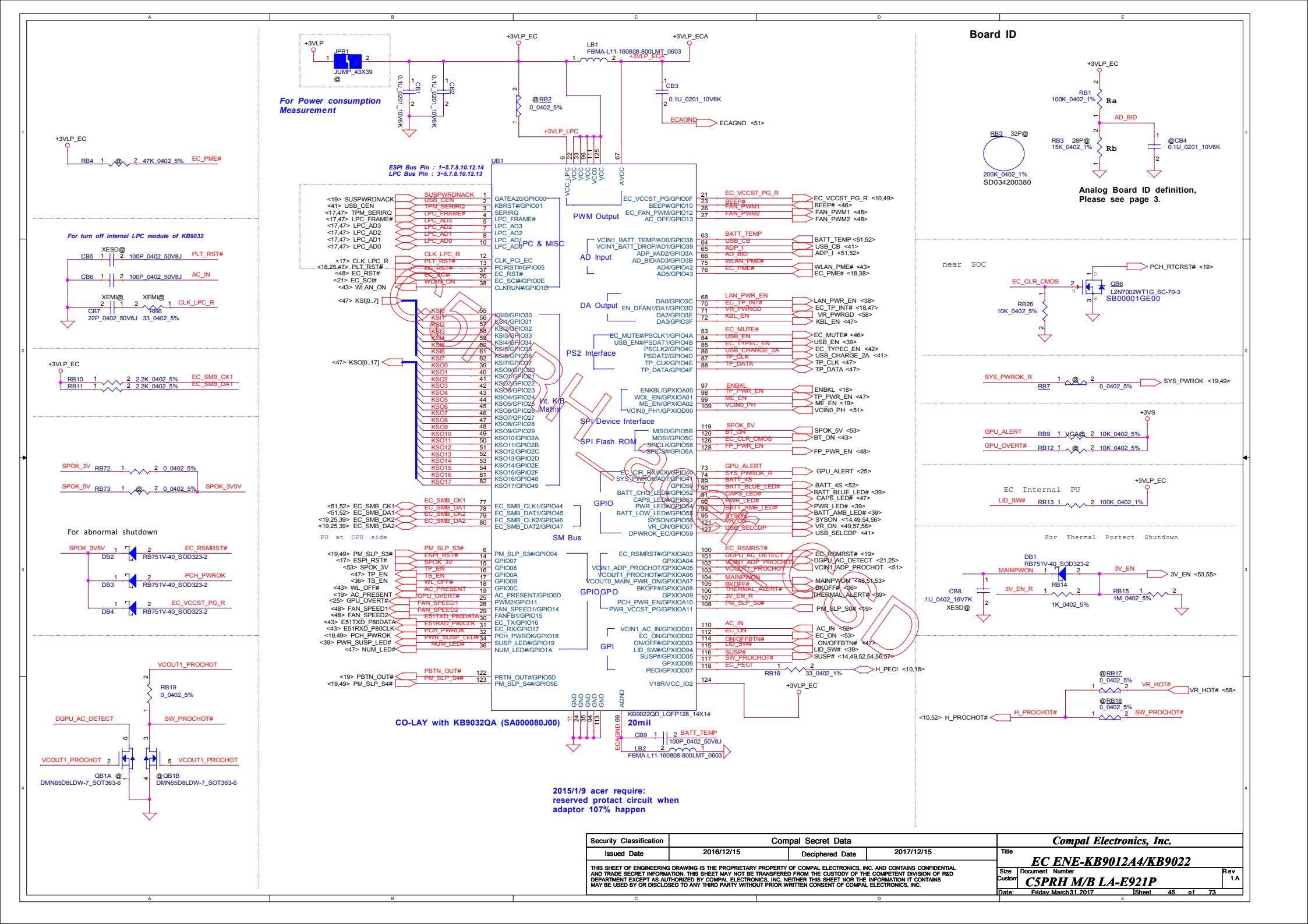
Board ID
Analog Board ID definition, Please see page 3.
For Power consumption Measurement
ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13
UB1
KB9022QD_LQFP128_14X14
20mil
CO-LAY with KB9032QA (SA000080J00)
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
PU at CPU side
For turn off internal LPC module of KB9032
For abnormal shutdown
near SOC
EC Internal PU
For Thermal Portect Shutdown
2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen
Security Classification
Compal Secret Data
Issued Date
2016/12/15
Deciphered Date
2017/12/15
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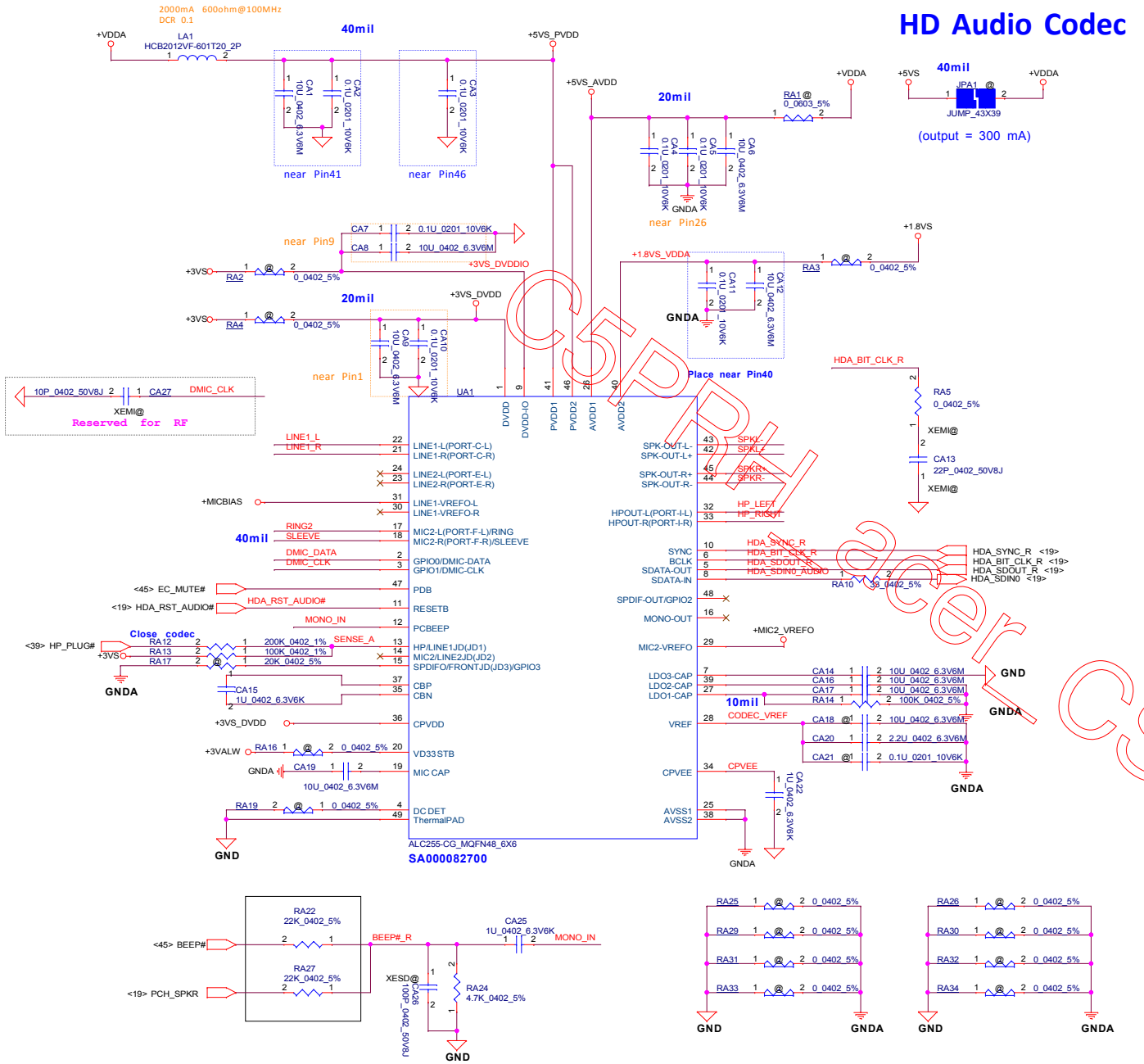
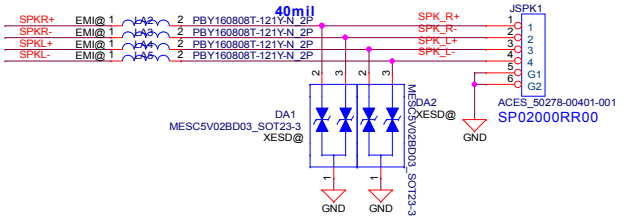
HD Audio Codec

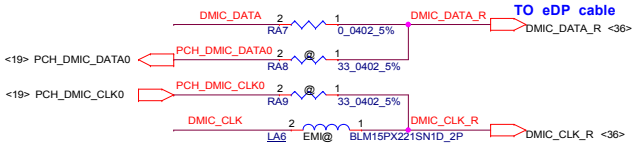


Int. Speaker Conn.

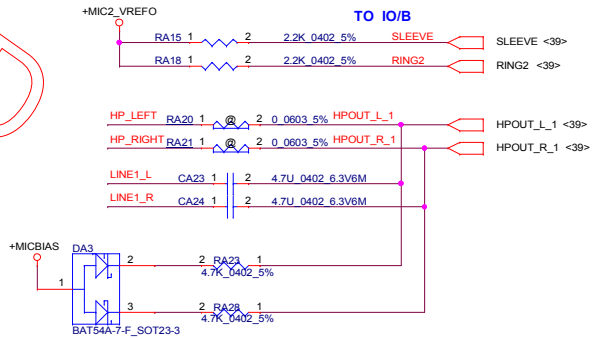


Digital MIC

MIC BOM upload by Audio Team



Headphone Out



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Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: HD Audio Codec ALC255

Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev: 1.A

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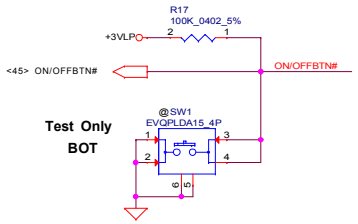
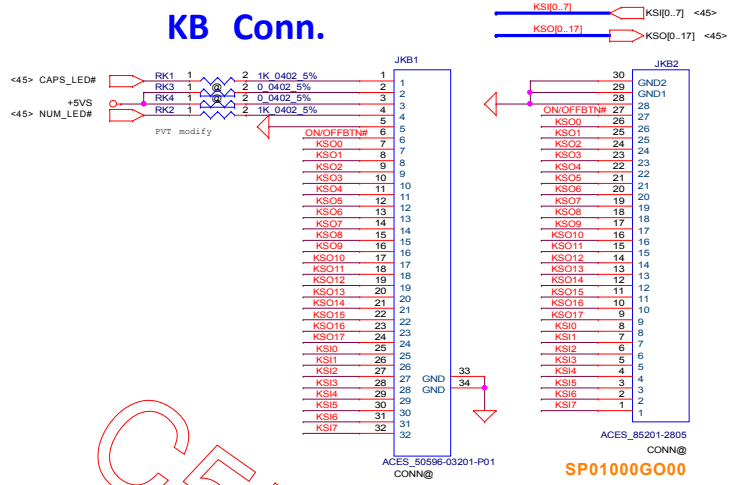
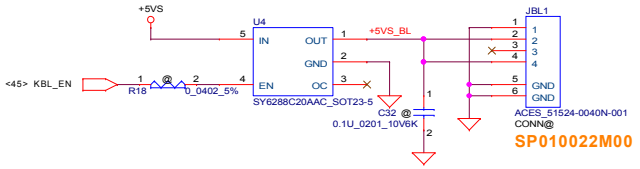
ON/OFF BTN



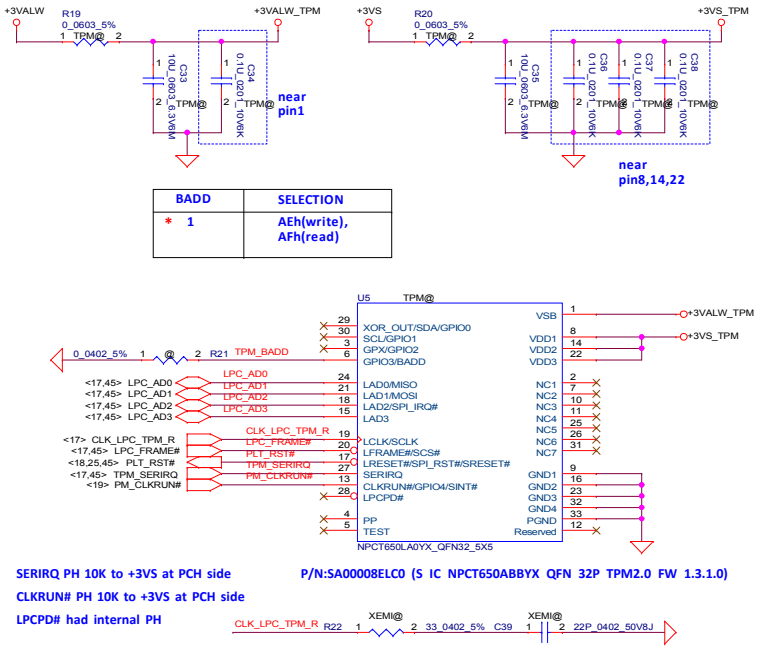
KB Conn.



KB BackLight



TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)

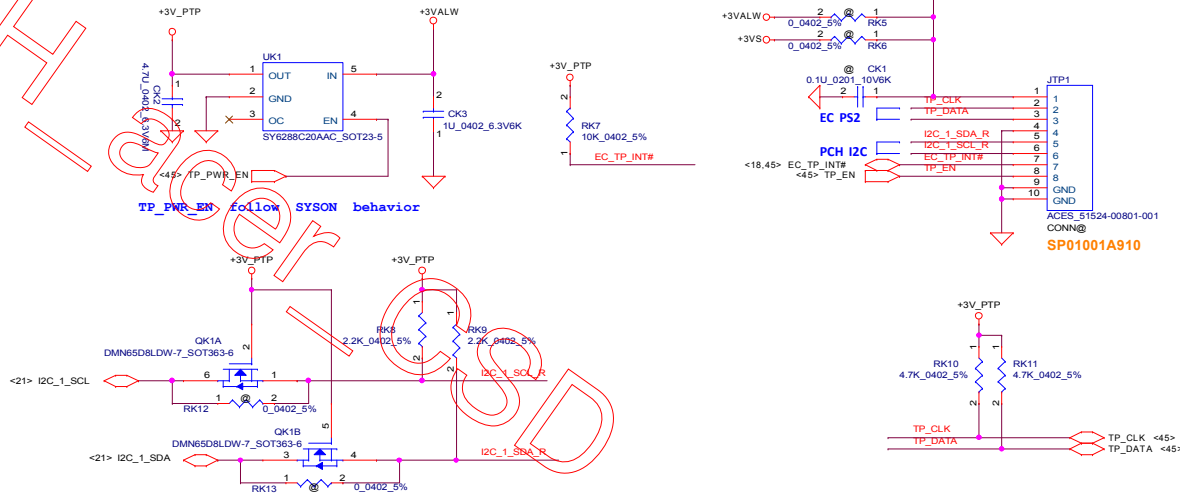
SERIRQ PH 10K to +3VS at PCH side

CLKRUN# PH 10K to +3VS at PCH side

LPCPD# had internal PH

P/N:SA00008ELC0 (S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0)

Touch Pad



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Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: *KB & TP & TPM Connector*

Size: Custom | Document Number: *C5PRH M/B LA-E921P* | Rev: 1.A

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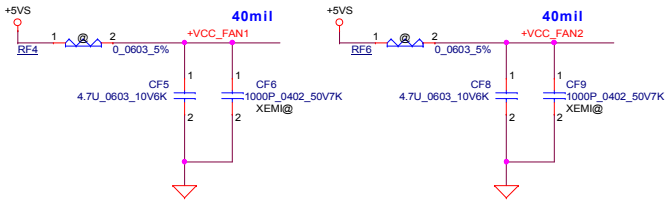
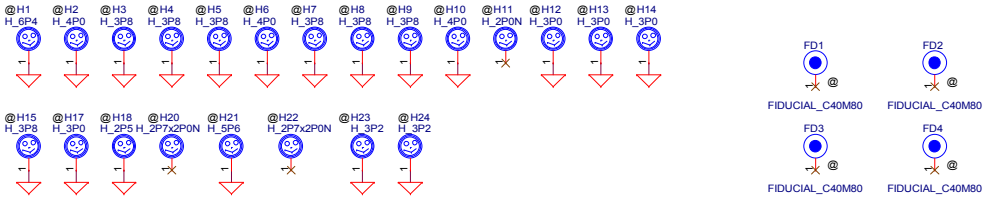
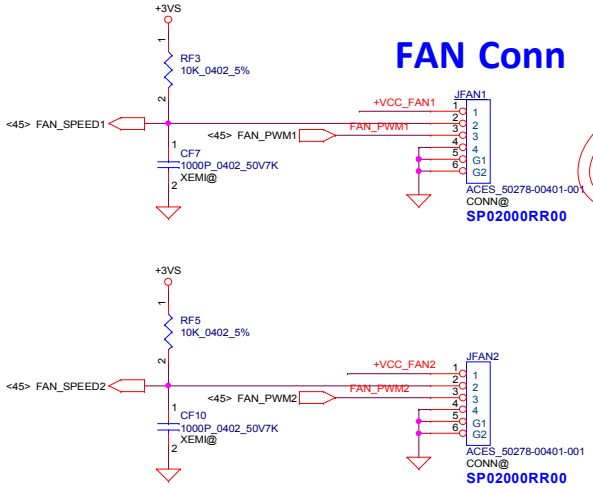


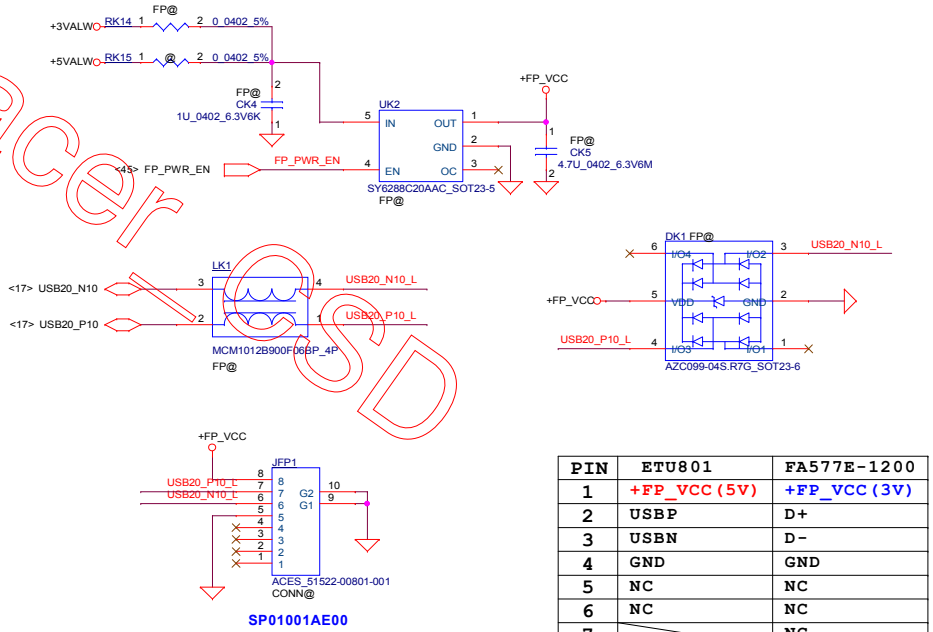
Screw Hole



FAN Conn

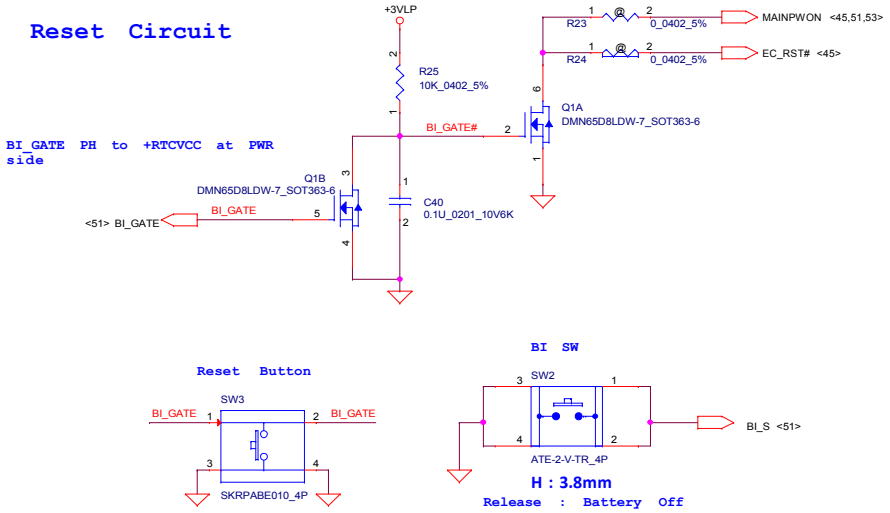


Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Reset Circuit



Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.

Title: FAN & FP & Screw Hole

Size	Document Number	Rev
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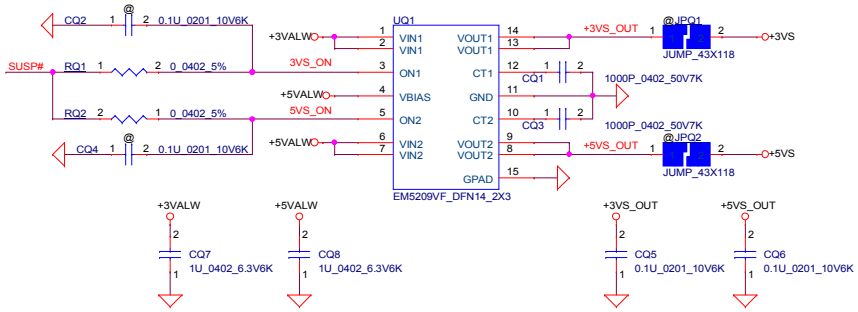
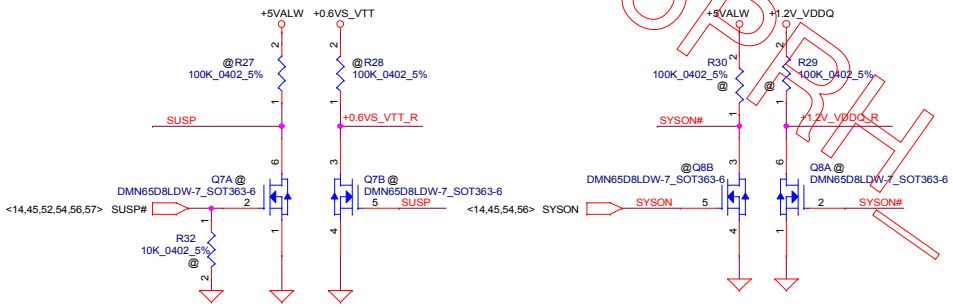
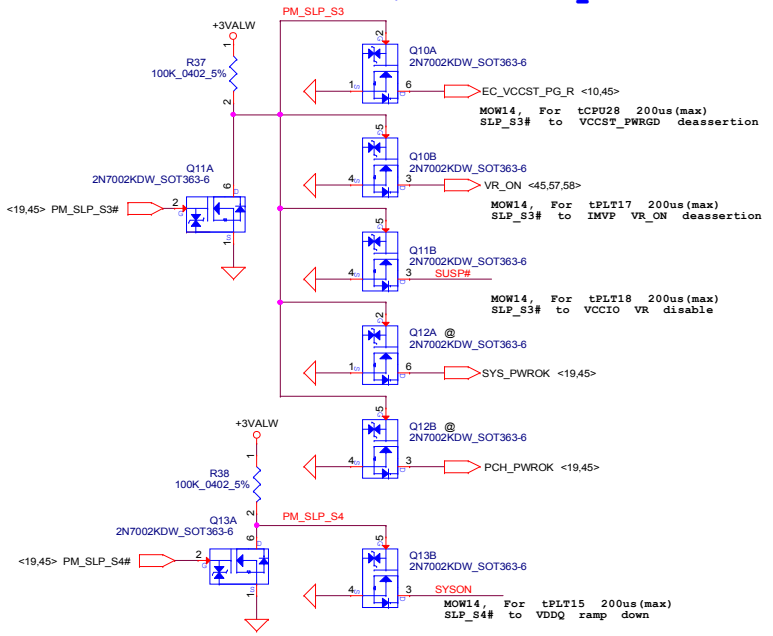
System DC inferface



Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7



For Power ON/Off Sequence



P/N: SB00000ZU00 (S TR DMN65D8LDW-7 2N SOT363-6)

Security Classification	Compal Secret Data		
Issued Date	2016/12/15	Deciphered Date	2017/12/15

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: C5PRH M/B LA-E921P		Rev: 1.A
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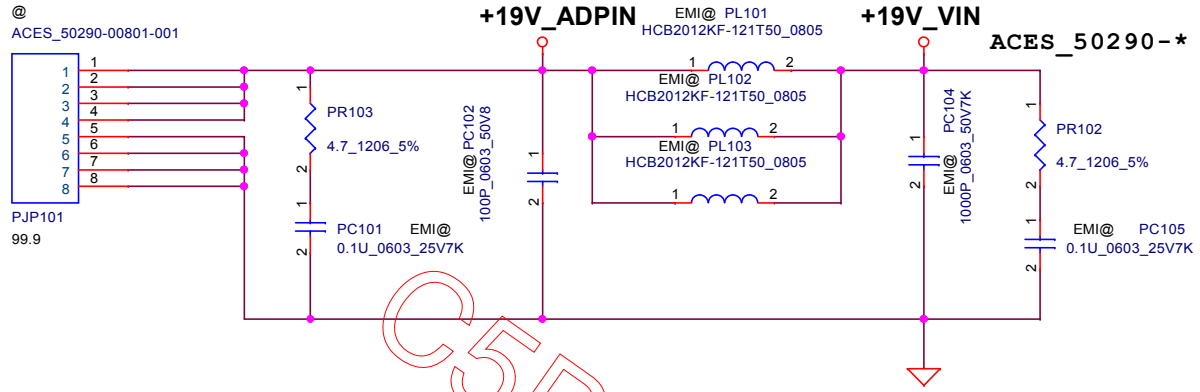
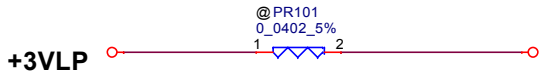
change PL101 PL102 from SM01000C000 to comm part SM01000P200

ACES_50290-*





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DCIN

Size	Document Number	Rev
Custom	C5PRH M/B LA-E921P	1.A

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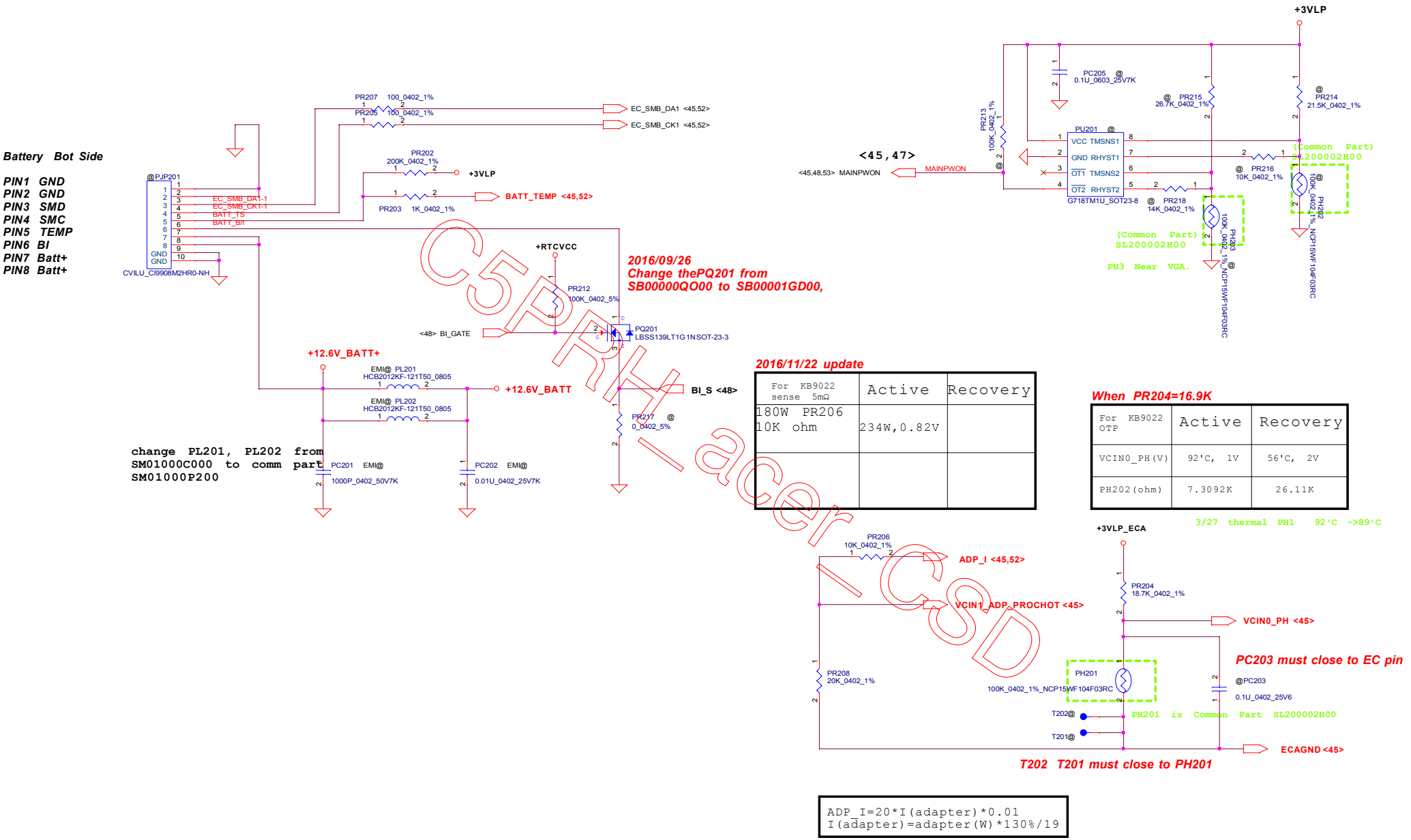


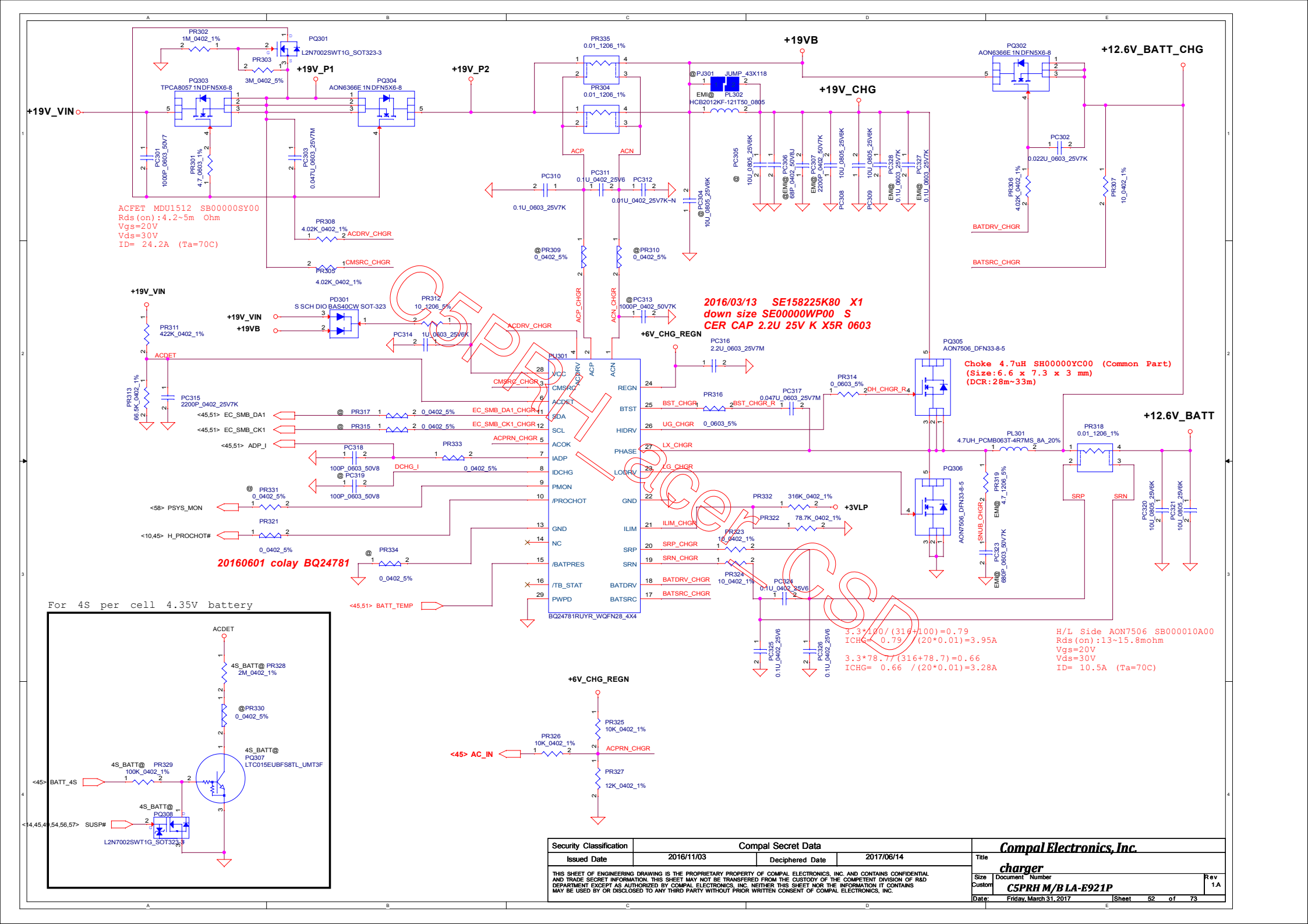
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

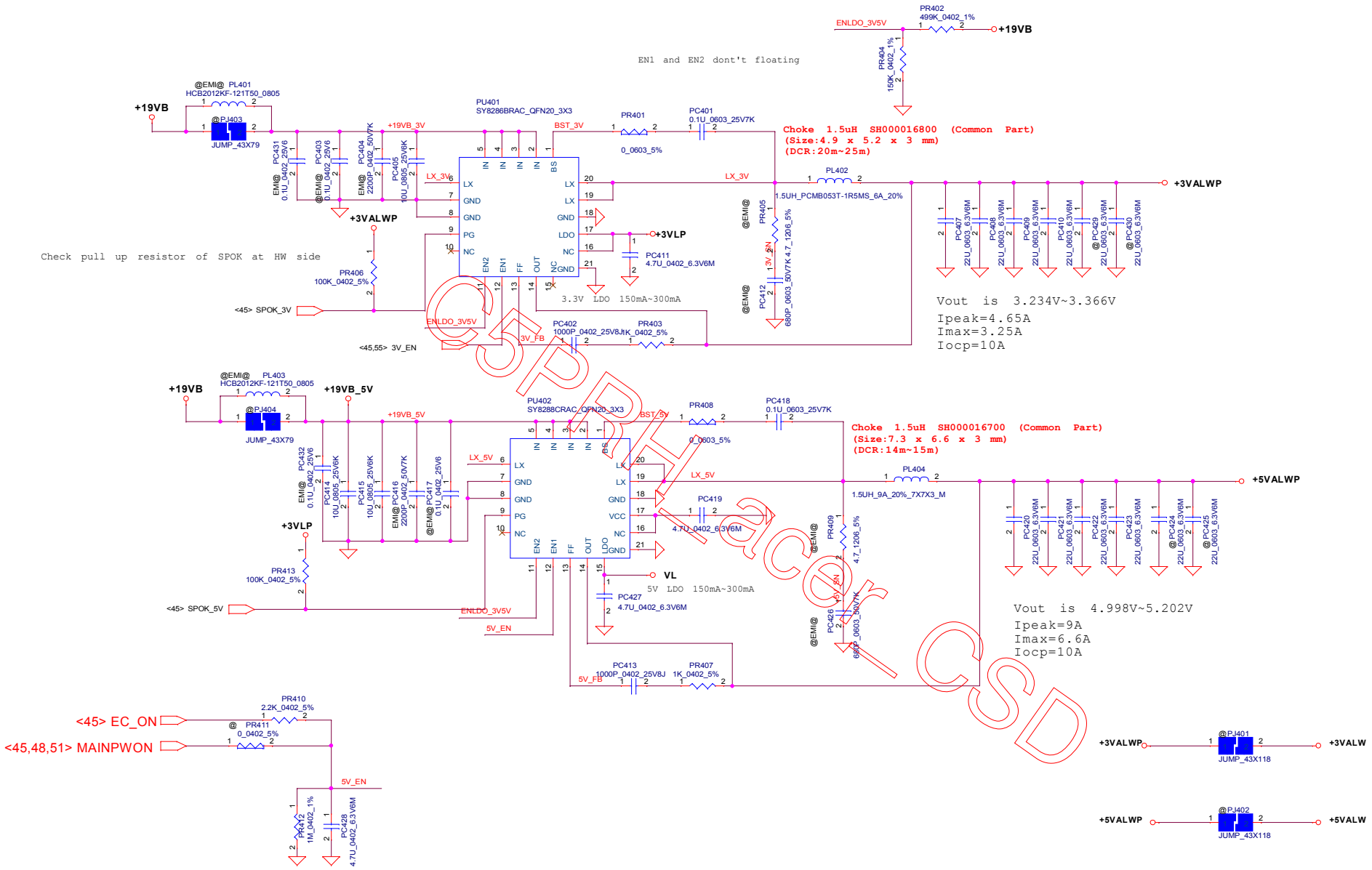
Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev: 1.A

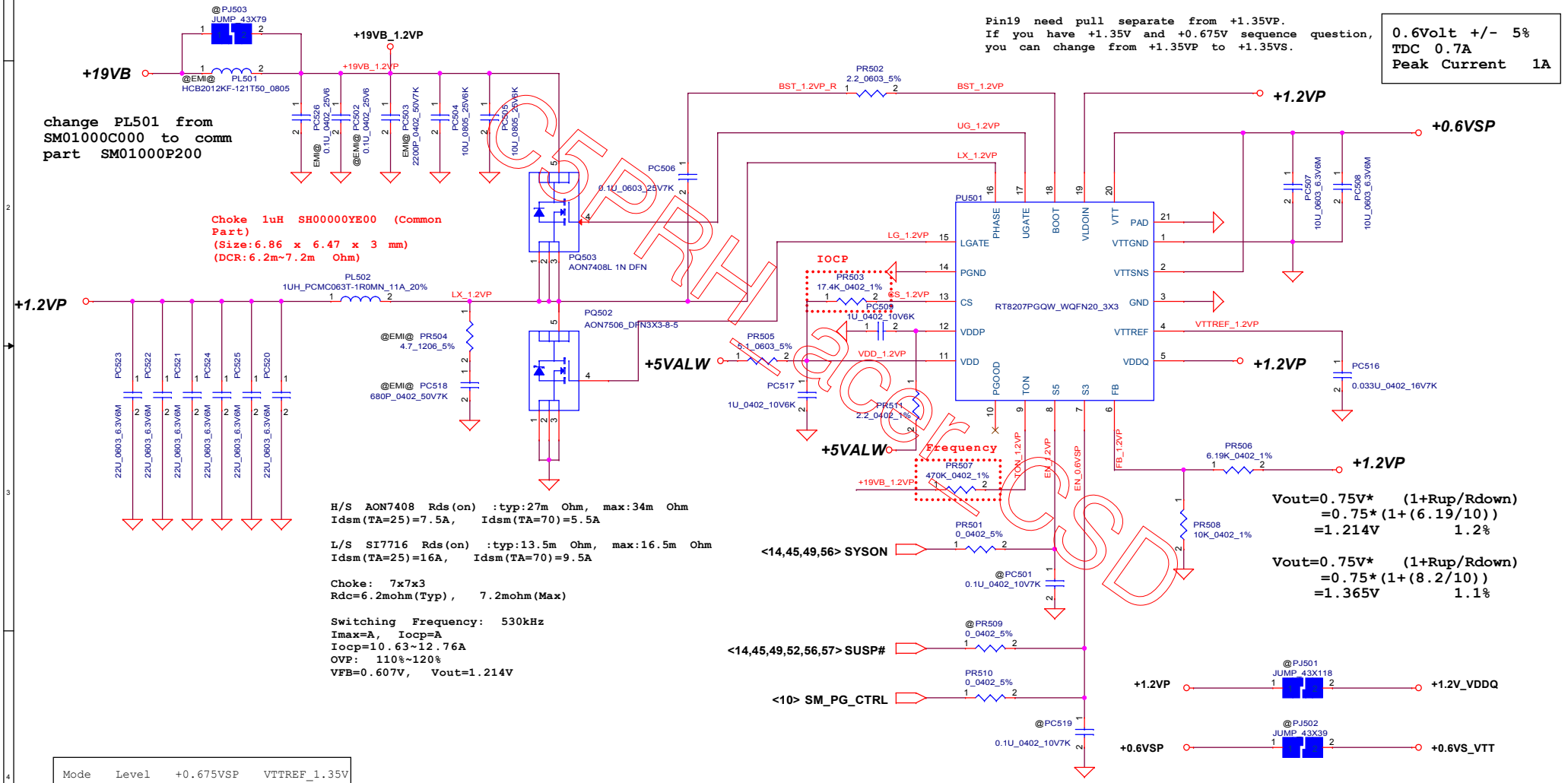
Date: Friday, March 31, 2017 | Sheet 51 of 73





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size	Document Number		Rev
Custom	C5PRH M/B LA-E921P		1.A
Date:	Friday, March 31, 2017	Sheet	53 of 73



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

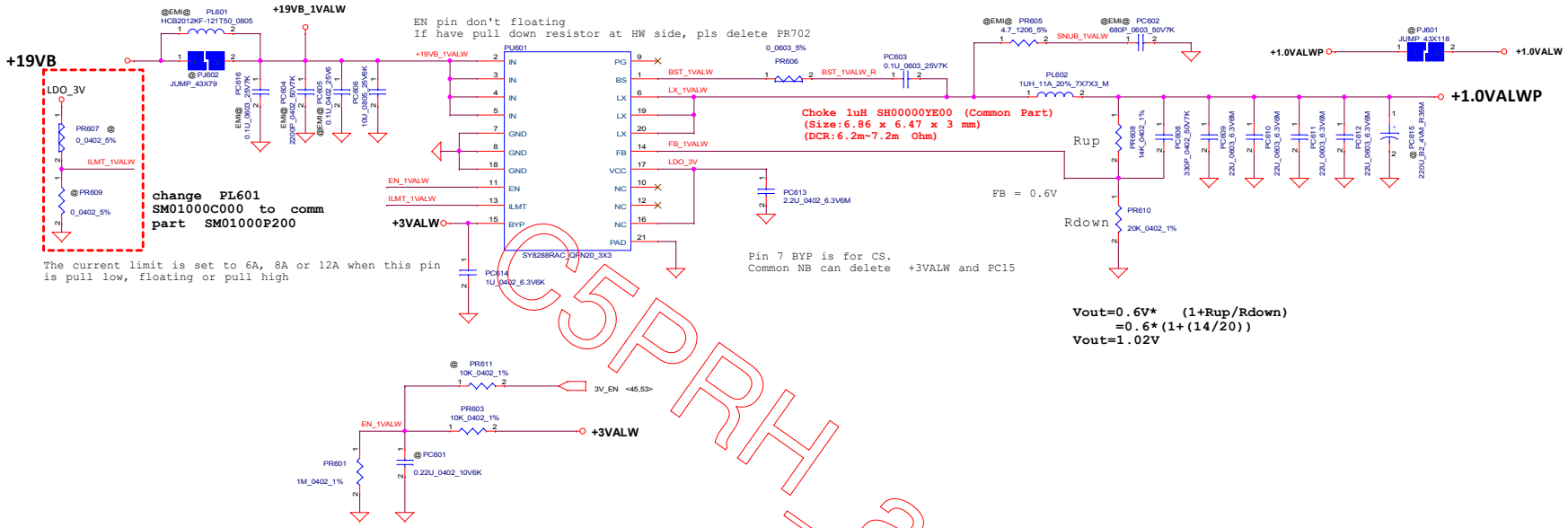
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: C5PRH M/B LA-E921P | Rev: 1.A

Date: Friday, March 31, 2017 | Sheet 54 of 73



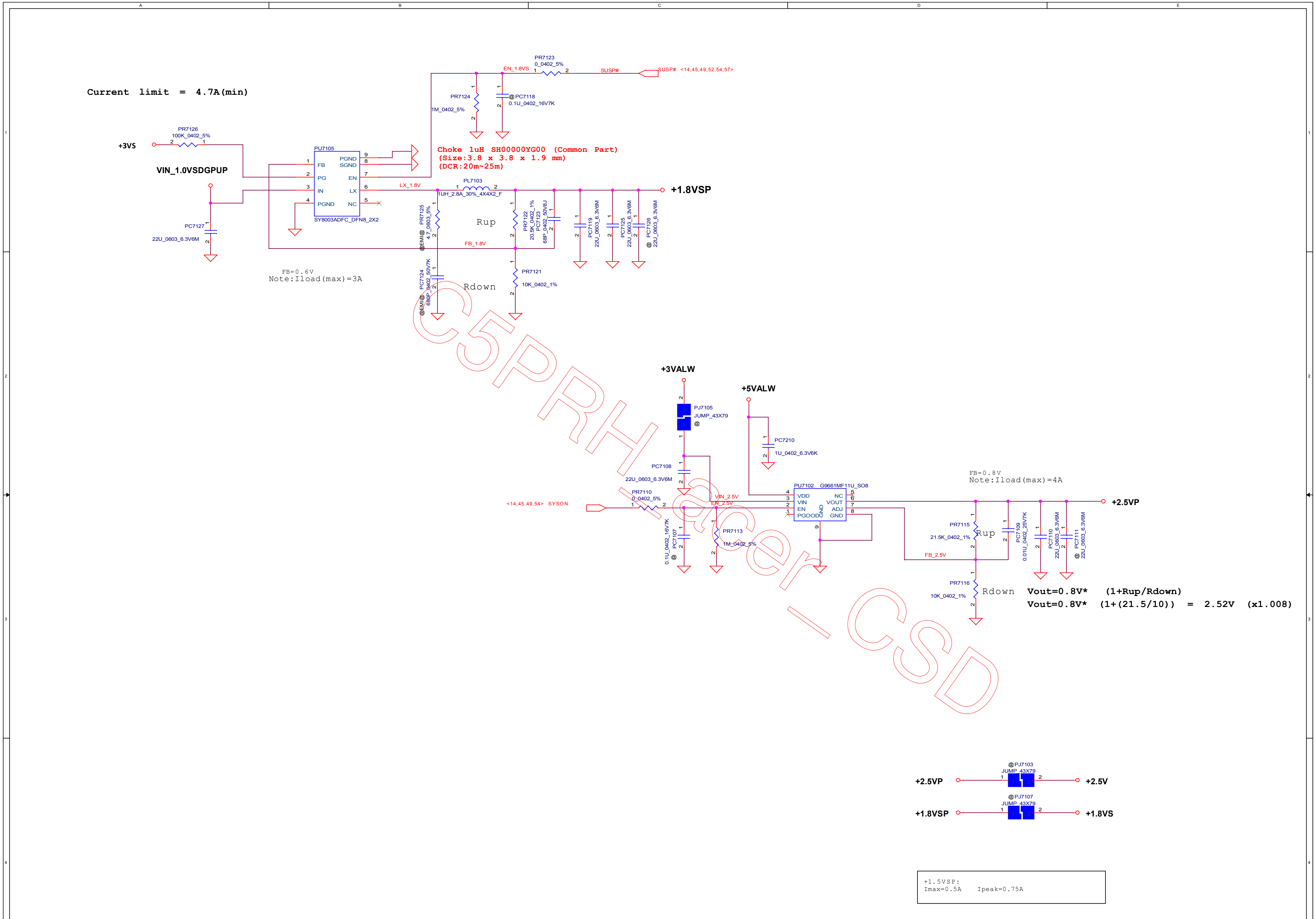
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

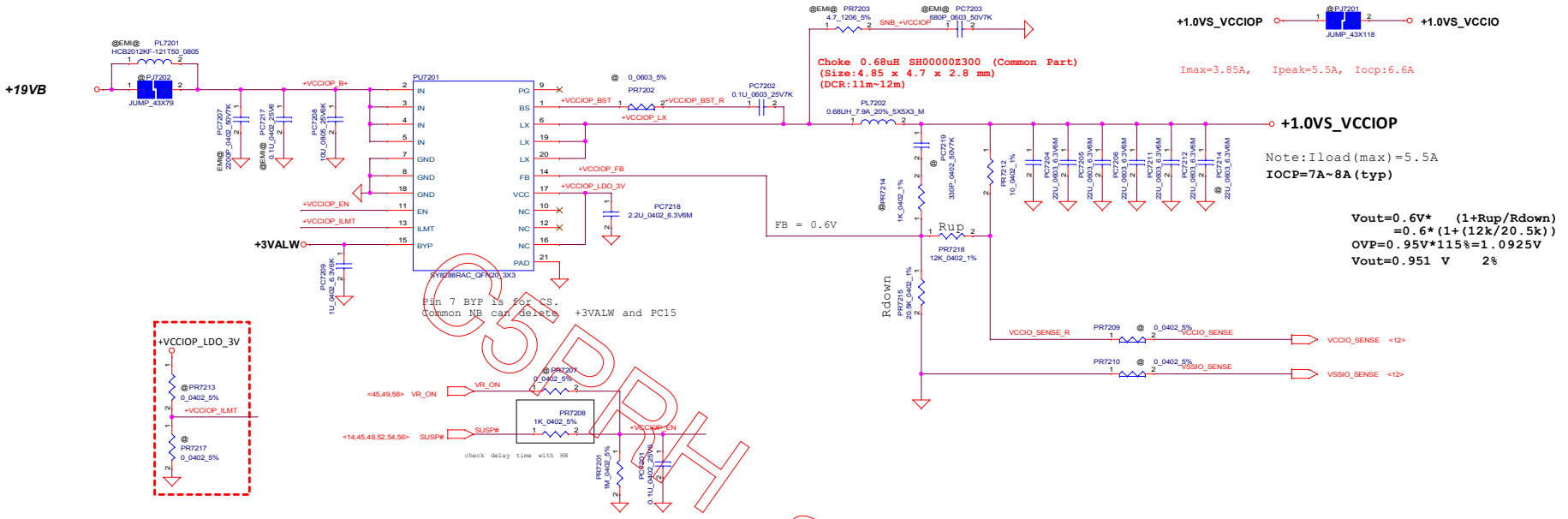
Title: 1V

Size	Document Number	Rev
C	C5PRH M/B LA-E921P	1.A

Date: Friday, March 31, 2017 Sheet 55 of 73



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/11/03	Deciphered Date 2017/06/14	Title: 1.5VS/2.5V
			Size: C Document Number: C5PRH M/B LA-E921P Rev: 1.A
			Date: Friday, March 31, 2017 Sheet 56 of 73



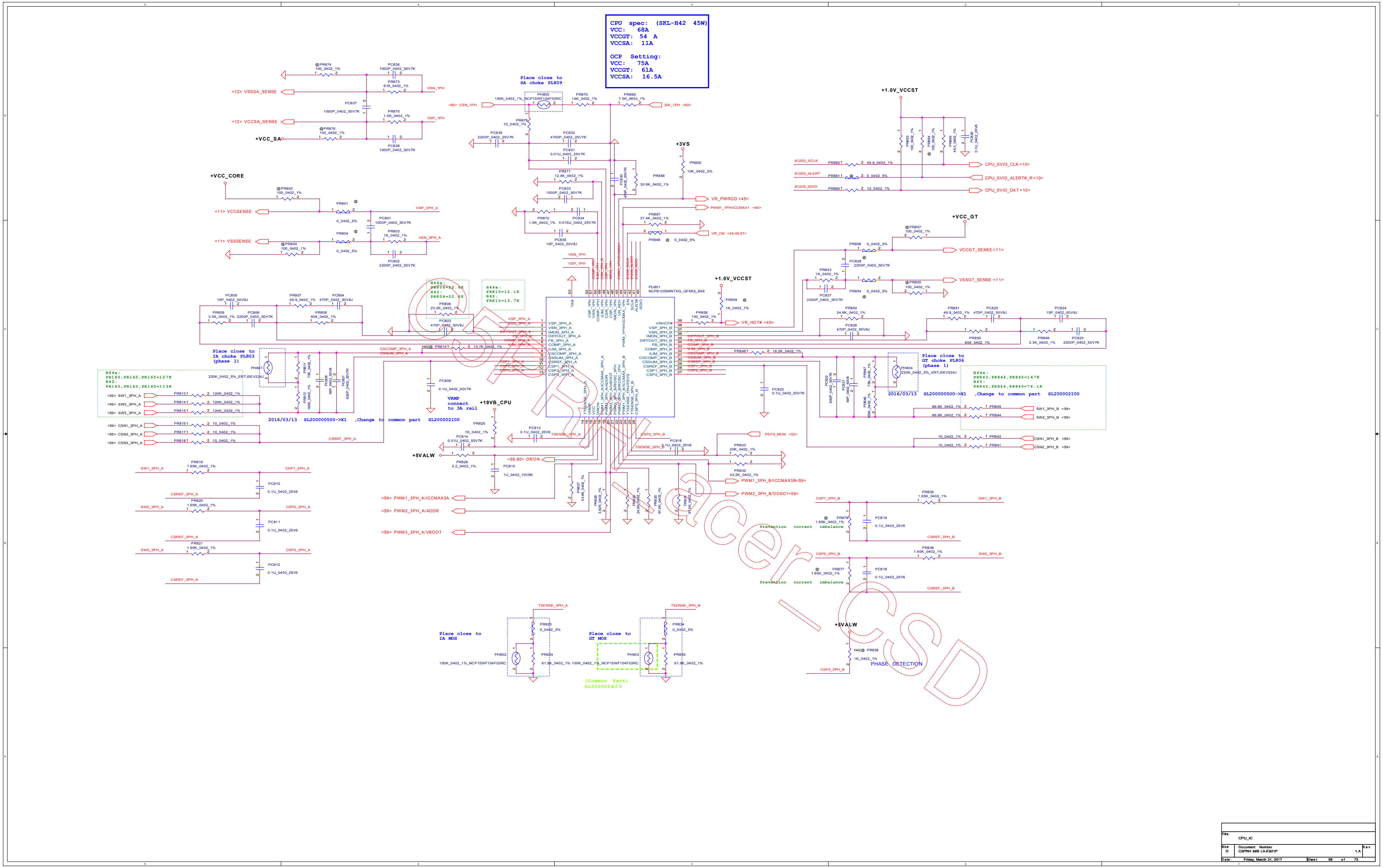
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5PRH M/B LA-E921P

Size	Document Number	Rev
C	1.0VS_VCCIO	1.A

Date: Friday, March 31, 2017 Sheet 67 of 73


CPU spec: (SKL-H42 45W)
VCC: 68A
VCCGT: 54 A
VCCSA: 11A
OCP Setting:
VCC: 75A
VCCGT: 61A
VCCSA: 16.5A
Place close to SA choke PL809
+1.0V_VCCST
+VCC_SA
+VCC_CORE
+3VS
+VCC_GT
+19VB_CPU
+5VALW
<12> VSSSA_SENSE
<12> VCCSA_SENSE
<11> VCCSENSE
<11> VSSSENSE
VCCGT_SENSE <11>
VSSGT_SENSE <11>
CPU_SVID_CLK <10>
CPU_SVID_ALERT#_R <10>
CPU_SVID_DAT <10>
VR_PWRGD <45>
VR_ON <45,49,57>
VR_HOT# <45>
PSYS_MON <52>
PU801
NCP81205MNTXG_QFN52_6X6
Place close to IA choke PL803 (phase 1)
Place close to GT choke PL806 (phase 1)
VRMP connect to 3A rail
2016/03/13 SL200000500->X1 ,Change to common part SL200002I00
Prevention current imbalance
Place close to IA MOS
Place close to GT MOS
(Common Part) SL200002H00
PHASE DETECTION
<59> PWM1_3PH_A/ICCMAX3A
<59> PWM2_3PH_A/ADDR
<59> PWM3_3PH_A/VBOOT
PWM1_3PH_B/ICCMAX3B <59>
PWM2_3PH_B/DOSC1 <59>
CPU_IC
C5PRH M/B LA-E921P
Friday, March 31, 2017
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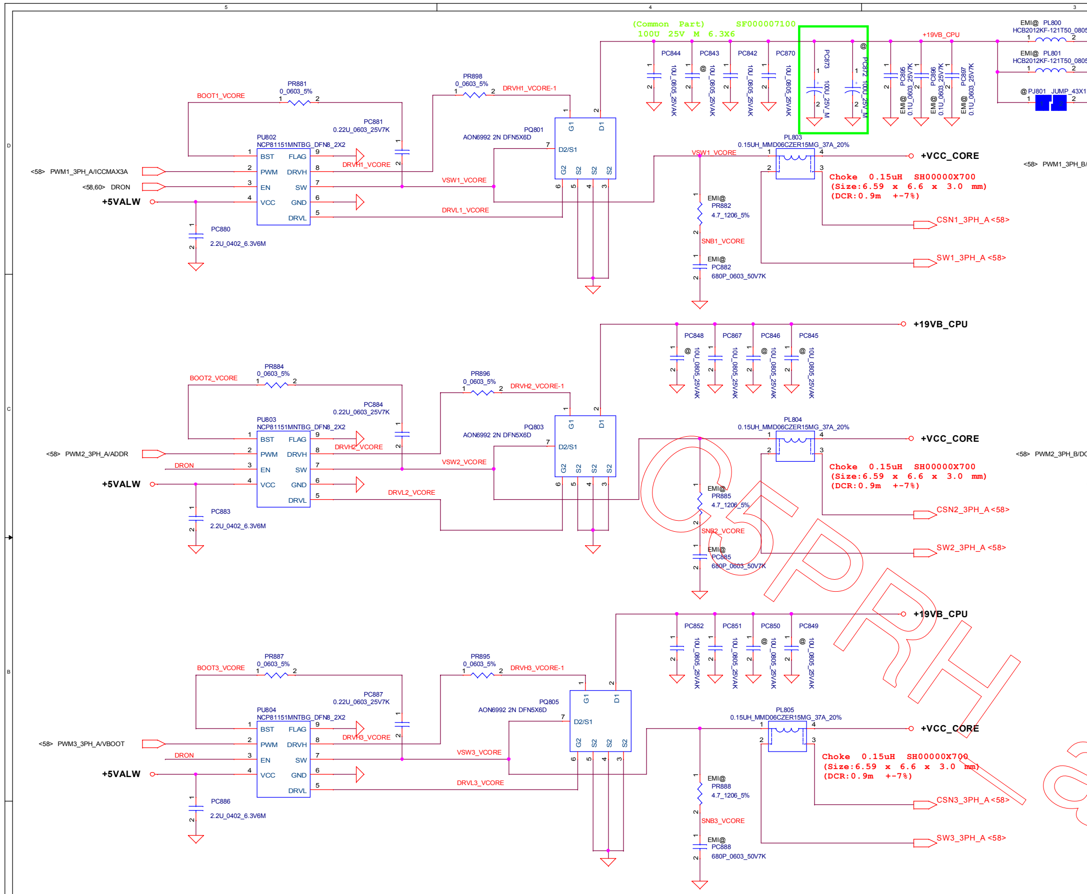
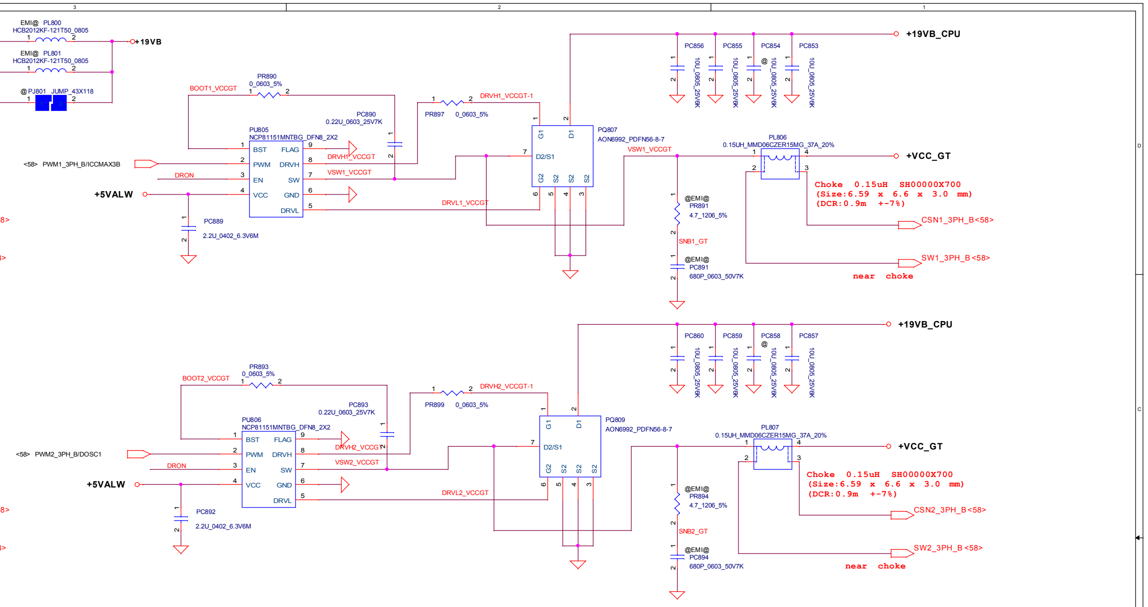




For H-line 42 :
VCC_CORE (LL=1.8m)
FSW = 600kHz
DCR = 0.9m Ohm +/- 7%

I(max)=50A
I(peak)=68A
OCP=75A
Vboot=0V

	TYP	MAX
H/S_AON6428 Rds(on) =	11.3m Ohm ,	14.5m Ohm
L/S_AON6794 Rds(on) =	2.8m Ohm ,	3.5m Ohm

For H-line 42 :
VCC_GT (LL=2.65m)
FSW = 600kHz
DCR = 0.9m Ohm +/- 7%

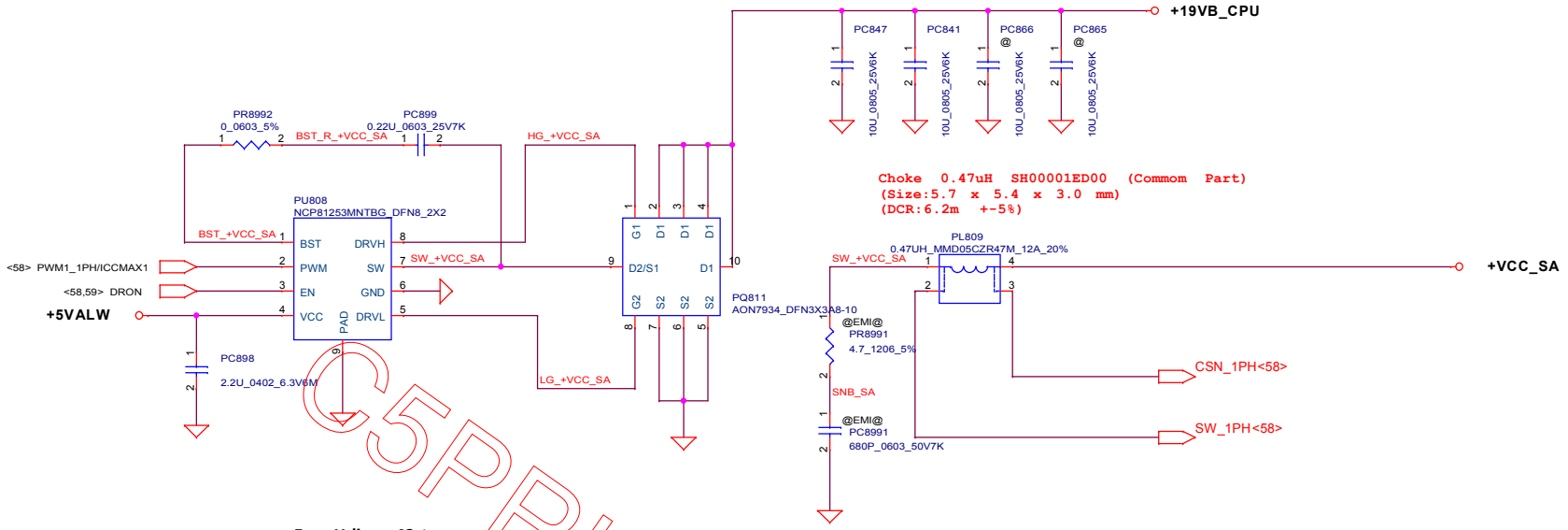
I(max)=25A
I(peak)=55A
OCP=61A
Vboot=0V

DaulMOS MDU5692S	TYP	MAX
H/S Rds(on) =	6.7m Ohm ,	8.5m Ohm
L/S Rds(on) =	2.1m Ohm ,	2.5m Ohm

Function Field :
Drivers - 36.2
Rest of support elements - 36.3
Acoustic Noise B+ Bulk CAP - 37.2

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.
Title: C5PRH M/B LA-E921P
Size: Custom | Document Number: VCC/VCCGT | Rev: 1.A
Date: Friday, March 31, 2017 | Sheet 59 of 73



For H-line 42 :
VCC_SA (LL=10m)
FSW = 600kHz
DCR = 6.2m Ohm +/- 5%

I(max)=10A
I(peak)=11.1A
OCP=16.5A
Vboot=1.05V

DaulMOS AON7934	TYP	MAX
H/S Rds(on) =	12.4m Ohm ,	15.8m Ohm
L/S Rds(on) =	9.1m Ohm ,	11.6m Ohm

Function Field :
Drivers - 36.2
Rest of support elements - 36.3

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: **C5PRH M/B LA-E921P**

Size: Custom | Document Number: **VCCSA** | Rev: 1.A

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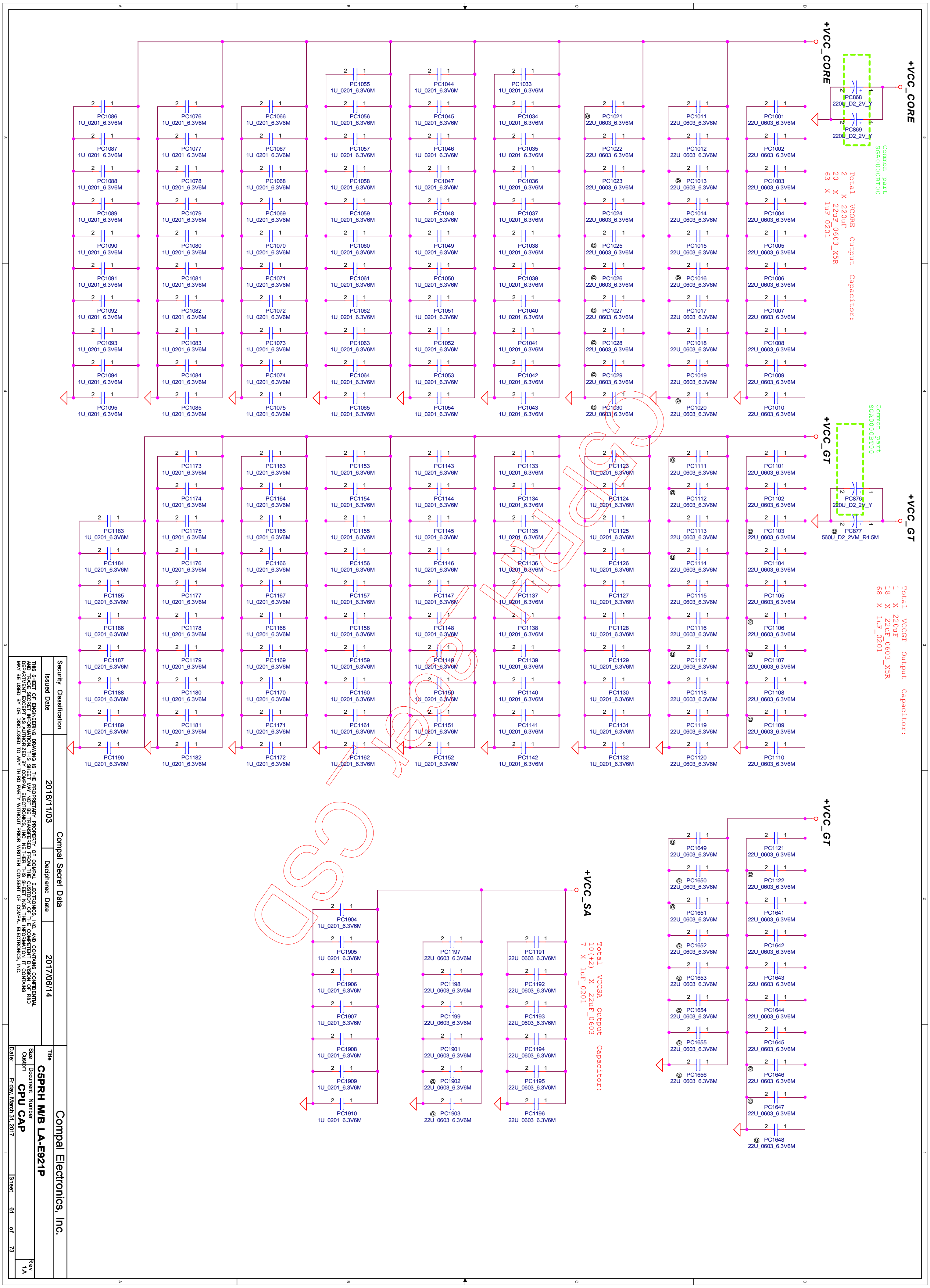

+VCC_CORE
PC868
220U_D2_2V_Y
PC869
220U_D2_2V_Y
Common part
SGA0000BT00
Total VCORE Output Capacitor:
2 X 220uF
20 X 22uF 0603 X5R
63 X 1uF_0201
+VCC_GT
PC876
220U_D2_2V_Y
PC877
560U_D2_2VM_R4.5M
Common part
SGA0000BT00
Total VCCGT Output Capacitor:
1 X 220uF
18 X 22uF 0603 X5R
68 X 1uF_0201
+VCC_SA
Total VCCSA Output Capacitor:
10(+2) X 22uF_0603
7 X 1uF_0201
1U_0201_6.3V6M
22U_0603_6.3V6M
Security Classification
Compal Secret Data
Issued Date
2016/11/03
Deciphered Date
2017/06/14
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Compal Electronics, Inc.
Title
C5PRH M/B LA-E921P
Size
Custom
Document Number
CPU CAP
Rev
1A
Date: Friday, March 31, 2017
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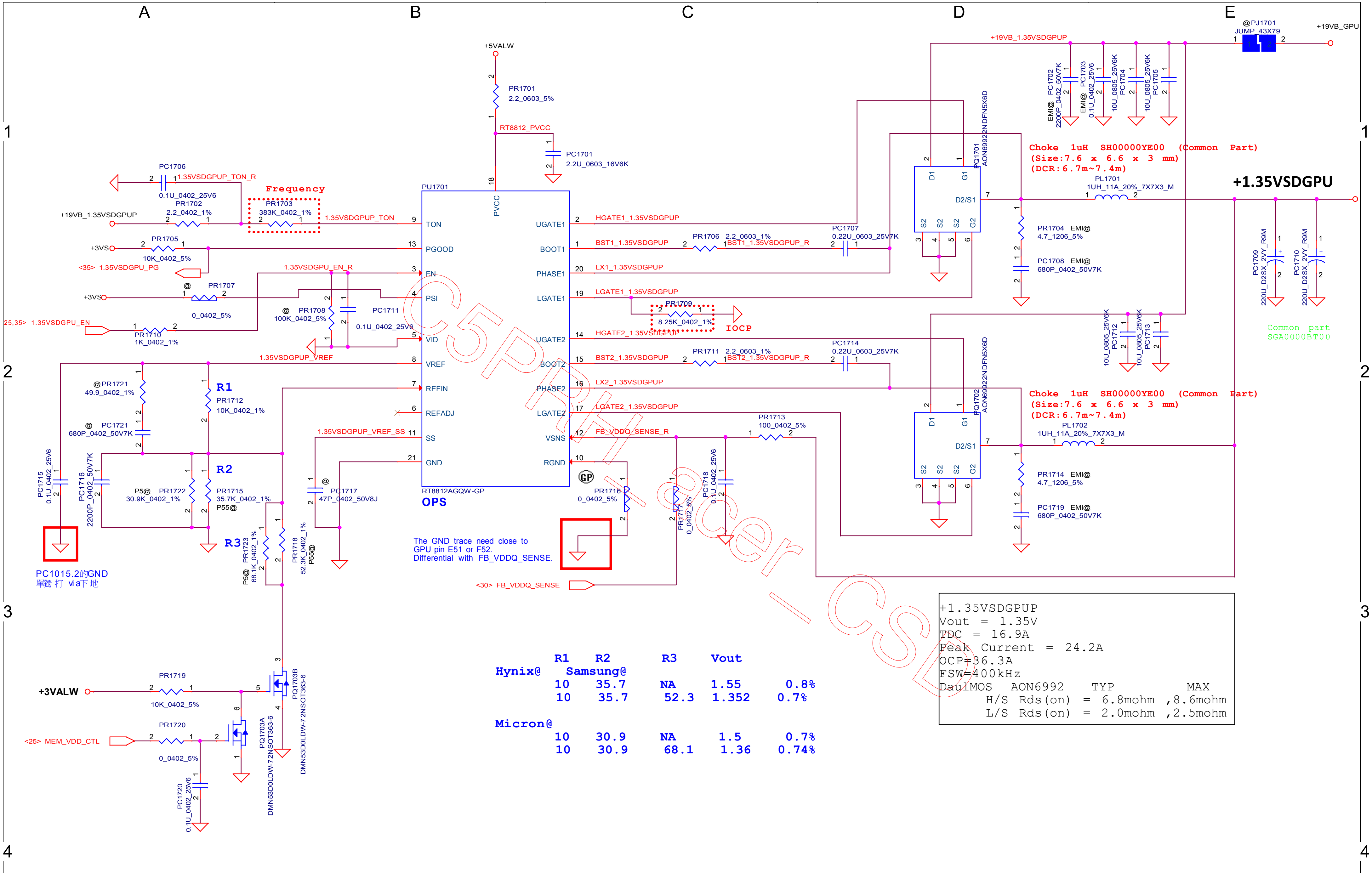


	R1	R2	R3	Vout	
Hynix@	Samsung@				
	10	35.7	NA	1.55	0.8%
	10	35.7	52.3	1.352	0.7%
Micron@					
	10	30.9	NA	1.5	0.7%
	10	30.9	68.1	1.36	0.74%

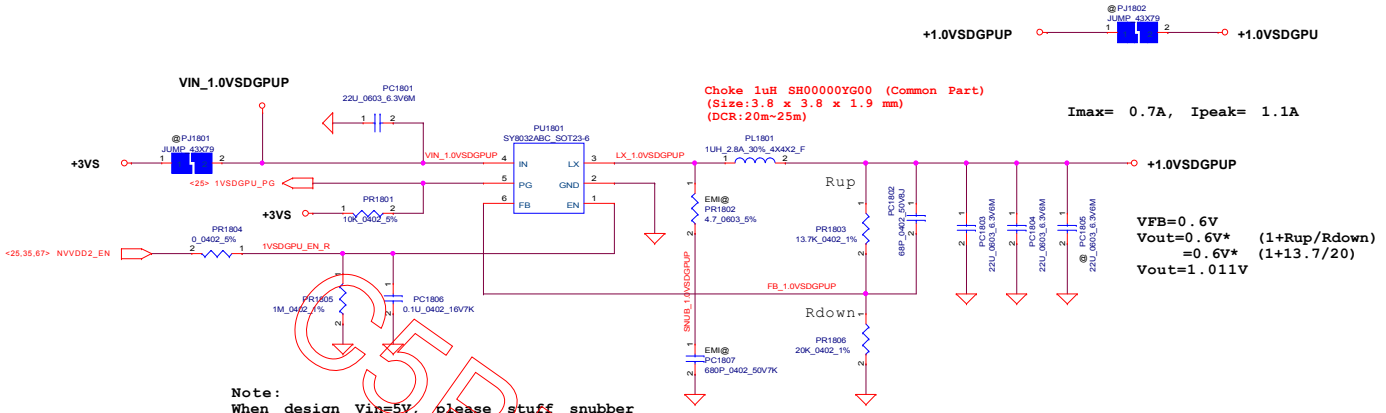
+1.35VSDGPUP
Vout = 1.35V
TDC = 16.9A
Peak Current = 24.2A
OCP=36.3A
FSW=400kHz
DaulMOS AON6992 TYP MAX
H/S Rds(on) = 6.8mohm ,8.6mohm
L/S Rds(on) = 2.0mohm ,2.5mohm

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VRAM

Size A3 | Document Number: C5PRH M/B LA-E921P | Rev 1.A

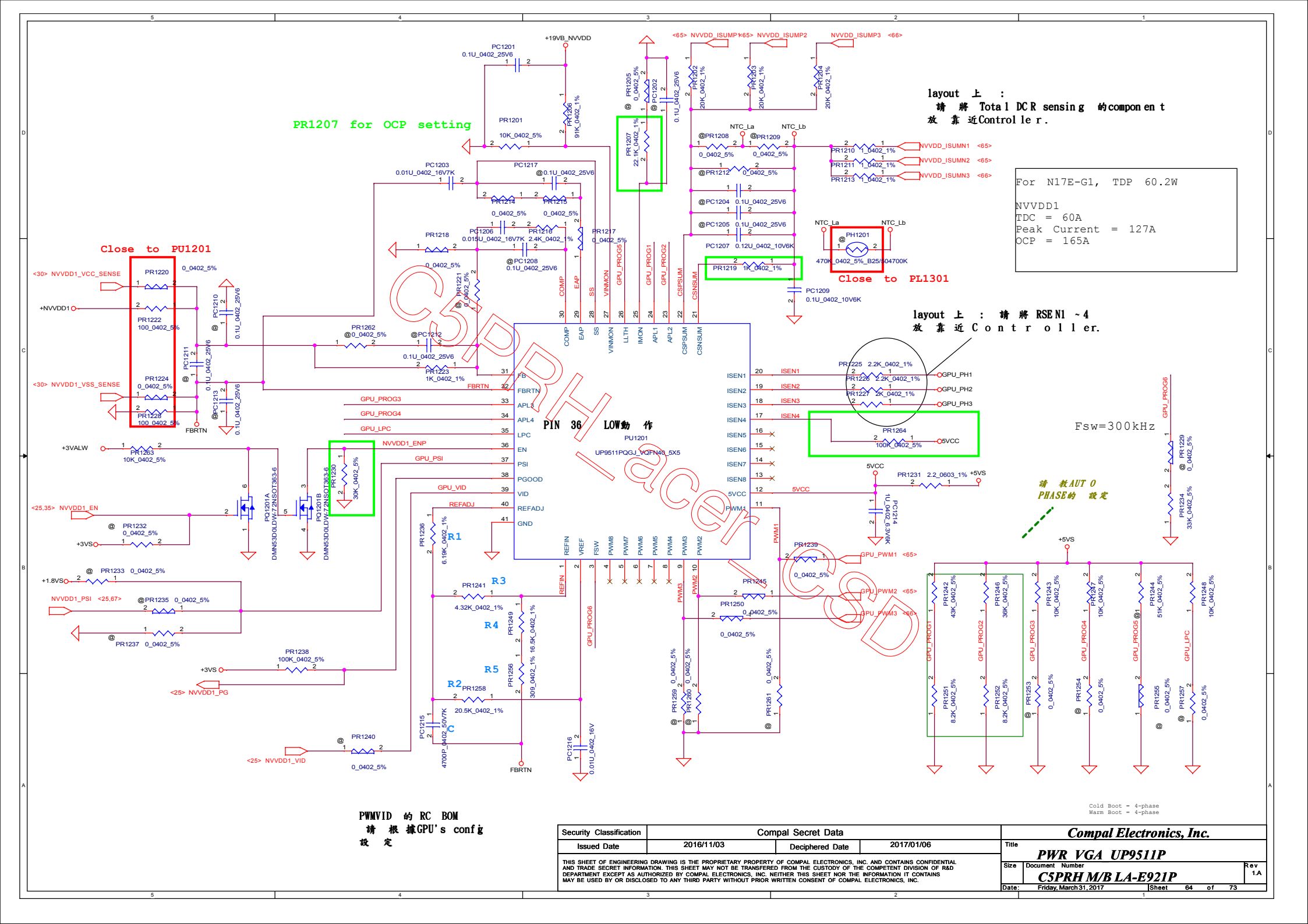


Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title	1.05VSDGPU	
Size: C	Document Number: C5PRH M/B LA-E921P	Rev: 1.A
Date: Friday, March 31, 2017	Sheet 63 of 73	


PR1207 for OCP setting
Close to PU1201
Close to PL1301
PIN 36 LOW動 作
PU1201
UP9511PQGJ_WQFN40_5X5
Fsw=300kHz
layout 上 : 請 將 Total DCR sensing 的component 放 靠 近Controller.
layout 上 : 請 將 RSEN1 ~4 放 靠 近 Controller.
For N17E-G1, TDP 60.2W
NVVDD1
TDC = 60A
Peak Current = 127A
OCP = 165A
請 教AUTO PHASE的 設定
PWMVID 的 RC BOM 請 根 據GPU's config 設 定
Cold Boot = 4-phase
Warm Boot = 4-phase
Security Classification
Compal Secret Data
Issued Date
2016/11/03
Deciphered Date
2017/01/06
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Compal Electronics, Inc.
Title
PWR VGA UP9511P
Size
Document Number
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Rev
1.A
Date: Friday, March 31, 2017
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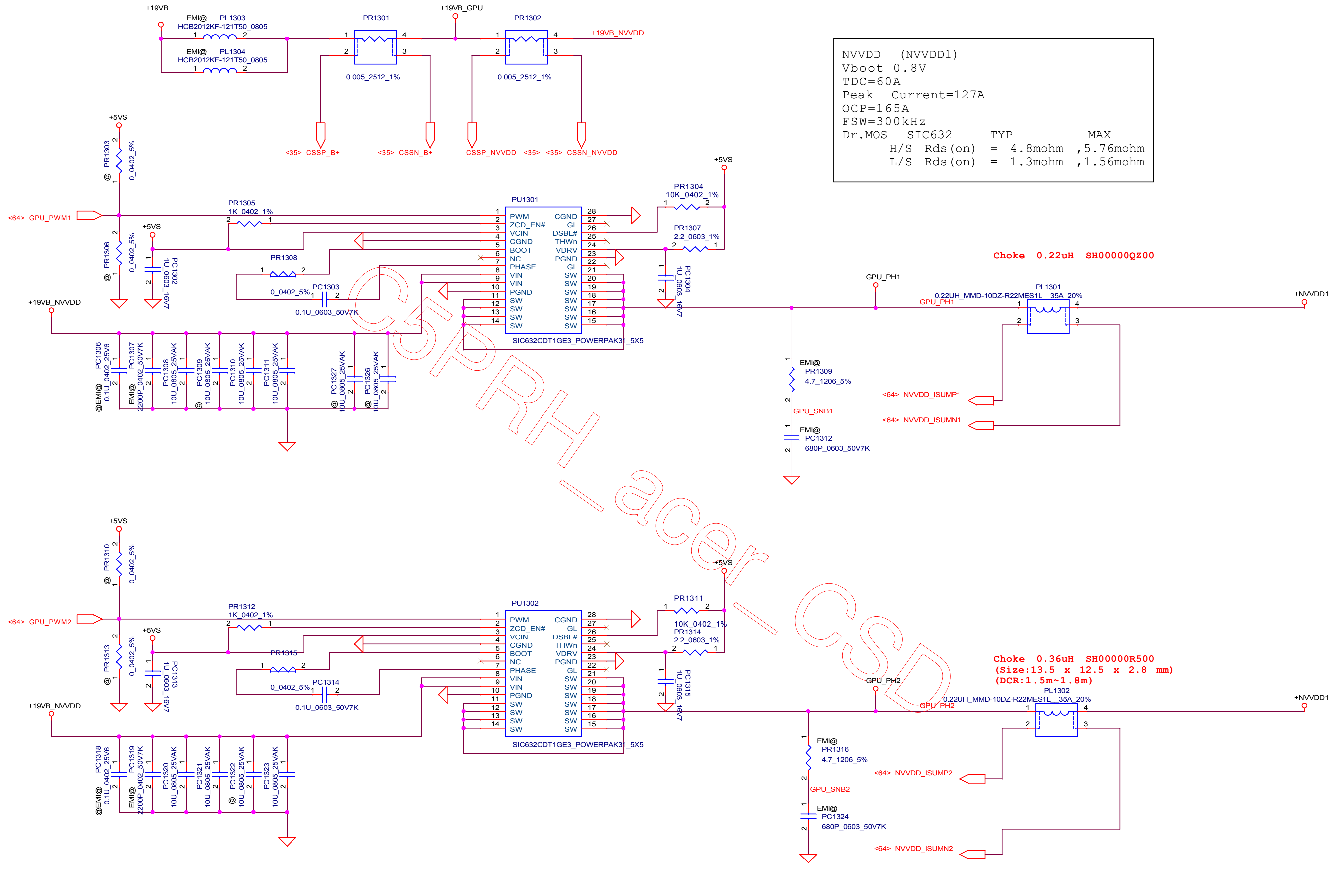
```
NVVDD  (NVVDD1)
Vboot=0.8V
TDC=60A
Peak  Current=127A
OCP=165A
FSW=300kHz
Dr.MOS   SIC632      TYP          MAX
      H/S  Rds(on)  =  4.8mohm  ,5.76mohm
      L/S  Rds(on)  =  1.3mohm  ,1.56mohm
```



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/11/03	Deciphered Date 2017/01/06	Title: PWR +NVVDD1
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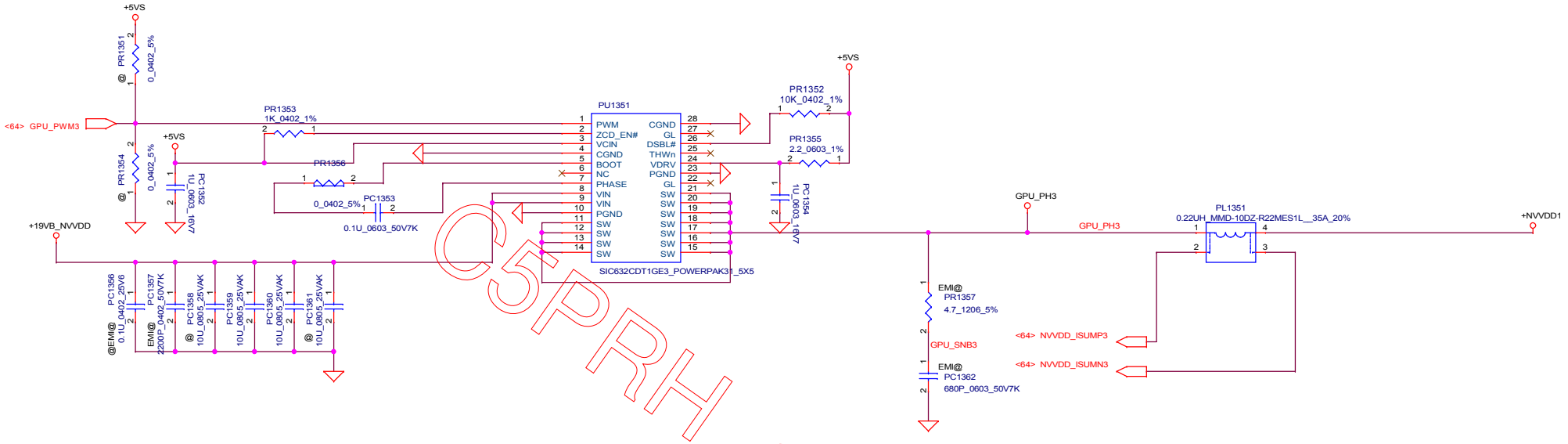
			Date: Friday, March 31, 2017 Sheet 65 of 73



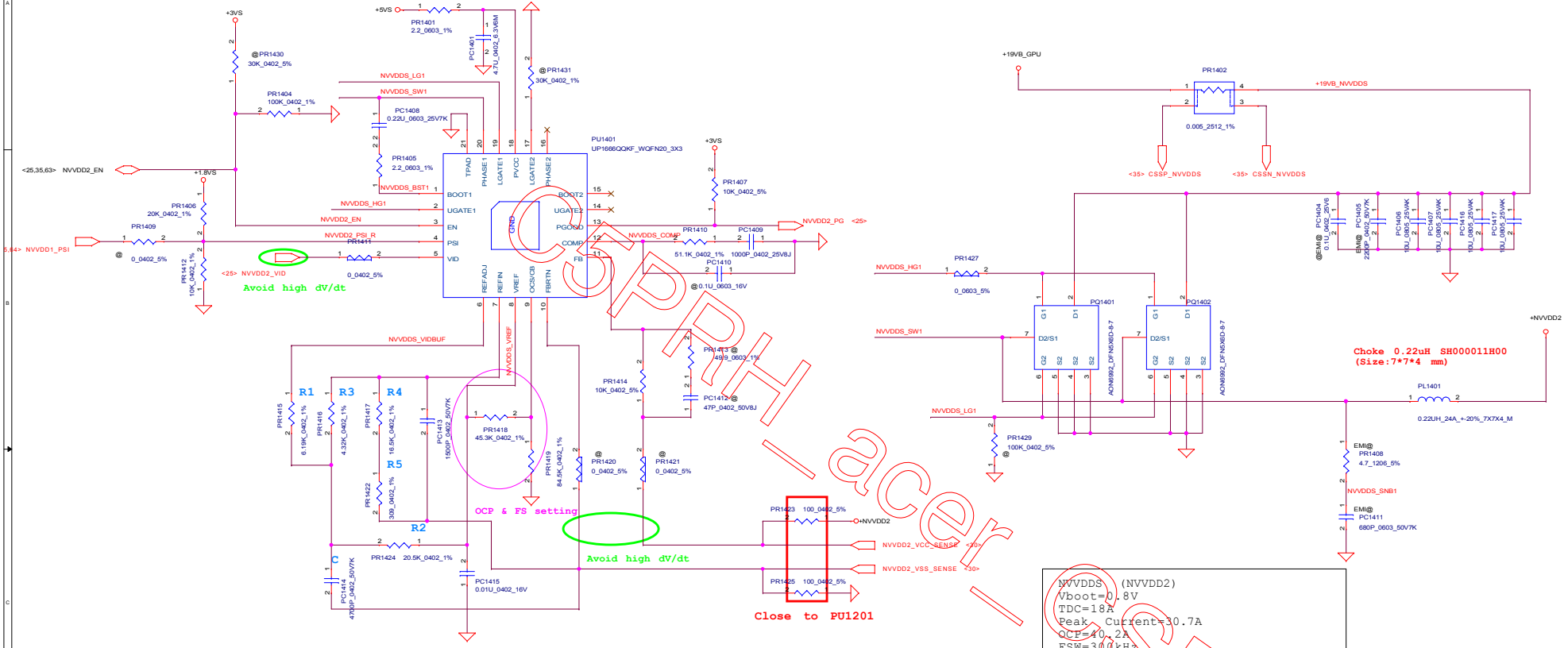
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR +NVVDD1**

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1.A

Date: Friday, March 31, 2017 | Sheet 66 of 73



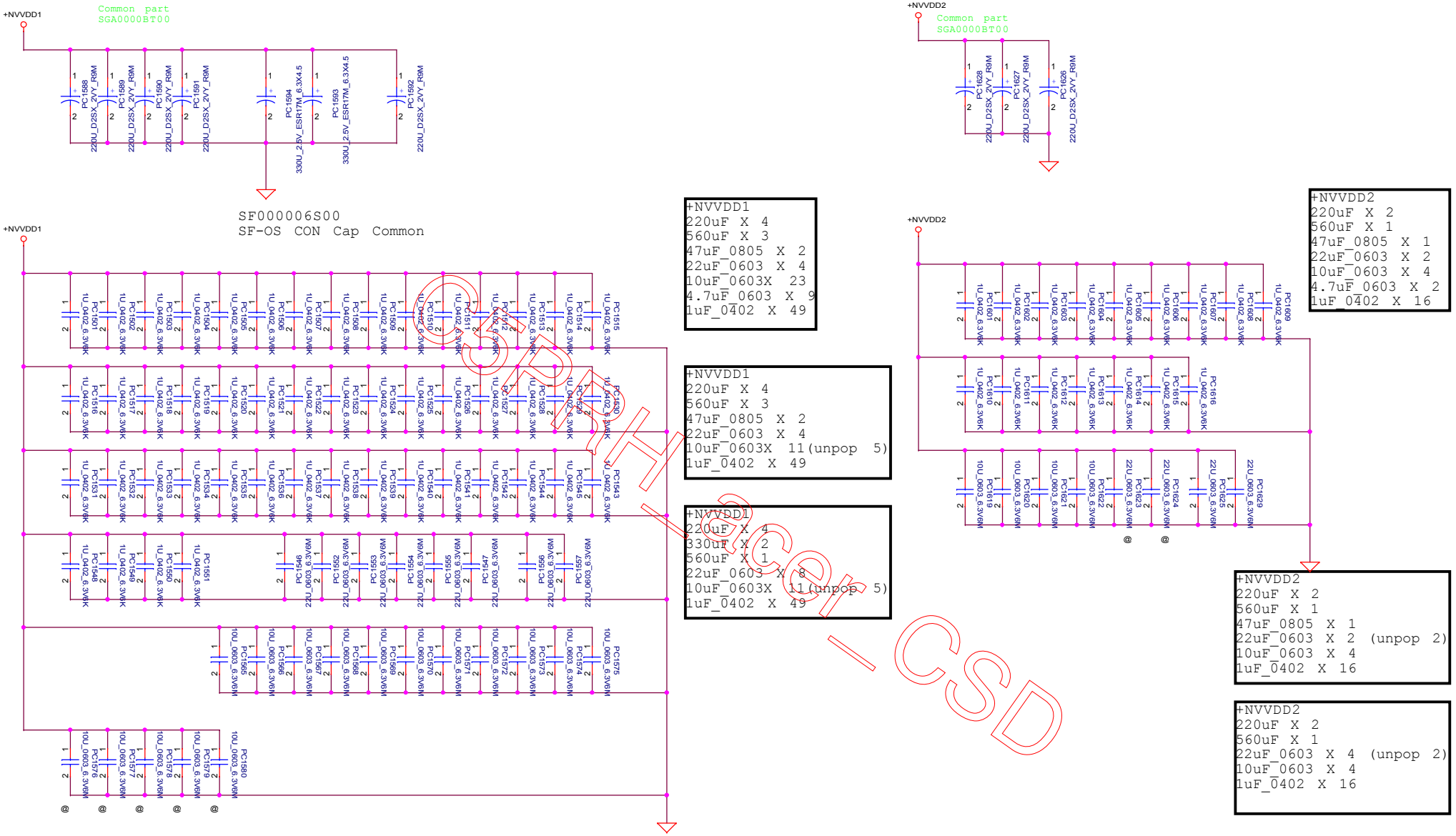
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **PWR +NVVDD2**

Size	Document Number	Rev
	C5PRH M/B LA-E921P	1.A

Date: Friday, March 31, 2017 Sheet 67 of 73



+NVVDD1
220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 23
4.7uF_0603 X 9
1uF_0402 X 49

+NVVDD1
220uF X 4
560uF X 3
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 11(unpop 5)
1uF_0402 X 49

+NVVDD1
220uF X 4
330uF X 2
560uF X 1
22uF_0603 X 8
10uF_0603X 11(unpop 5)
1uF_0402 X 49

+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2
10uF_0603 X 4
4.7uF_0603 X 2
1uF_0402 X 16

+NVVDD2
220uF X 2
560uF X 1
47uF_0805 X 1
22uF_0603 X 2 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16

+NVVDD2
220uF X 2
560uF X 1
22uF_0603 X 4 (unpop 2)
10uF_0603 X 4
1uF_0402 X 16

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