



Special Thanks!

130877

TRALOL

weaver

wins200786

QueenSoft

Mihail_tm

abraziff

iPad 2

Professional Schematic!
A1395, A1396, A1397 (k94ap)
Wites OM Tesla



Special Thanks!

...:Neo:...

~AhmedLeO~

Gecko UK

Mobileinfo

Hobson

Noobfix

DataRus

Kostelectronics

diesel57

D

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820-2875-05 MLB BOTTOM PCB

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB
PVT
REV. A


LAST MODIFIED=Mon Jan 10 13:11:06 2011

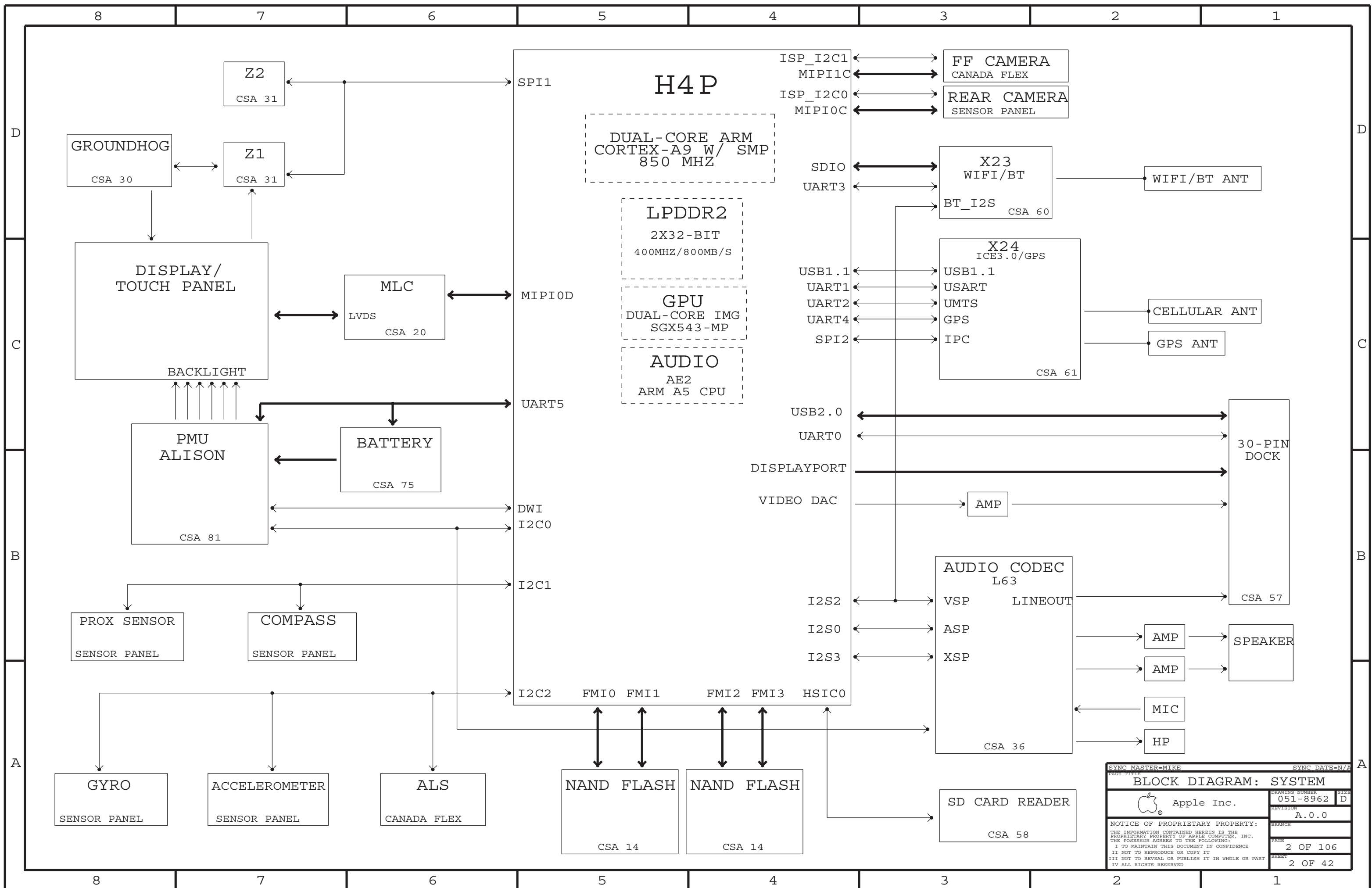
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A	0001052699	PRODUCTION RELEASED	2011-01-10

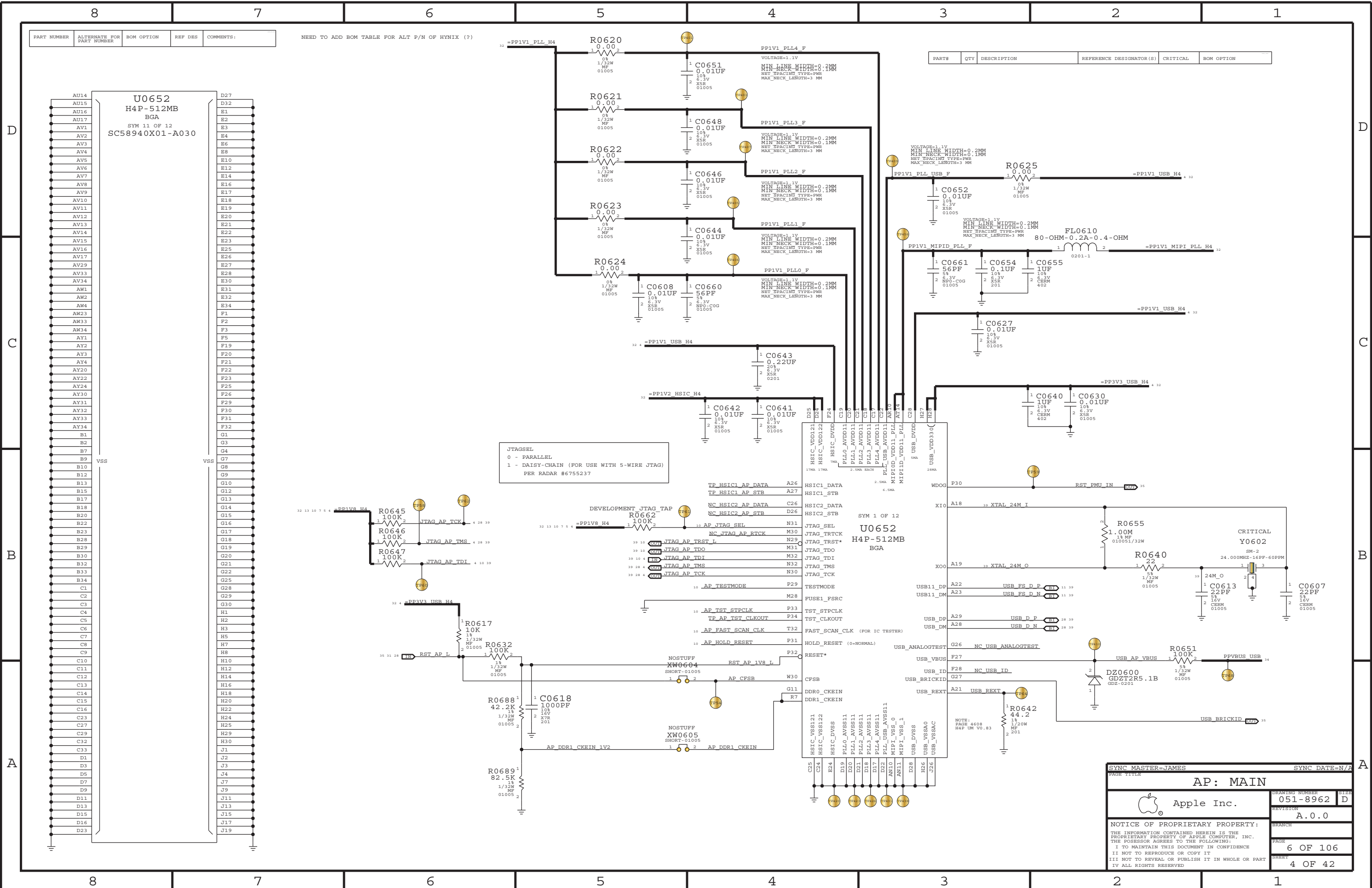
PDF	CSA	CONTENTS	SYNC	MASTER	DATE
1	1	TABLE OF CONTENTS		MIKE	N/A
2	2	BLOCK DIAGRAM: SYSTEM		MIKE	N/A
3	5	BOM TABLE		MIKE	N/A
4	6	AP: MAIN		JAMES	N/A
5	7	AP: I/Os		JAMES	N/A
6	8	AP: NAND		JAMES	N/A
7	9	AP: TV,DP,MIPI		JAMES	N/A
8	10	AP: PWR		JAMES	N/A
9	11	AP: PWR		JAMES	N/A
10	12	AP: MISC & ALIASES		JAMES	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES		JAMES	N/A
12	14	NAND		JONATHAN	N/A
13	17	VIDEO: DISPLAY PORT		JAMES	N/A
14	20	VIDEO: MLC		MIKE	N/A
15	21	VIDEO: MLC ALIASES		MIKE	N/A
16	22	VIDEO: LVDS CONNECTOR		ALEX	N/A
17	30	GRAPE: GROUNDHOG, CONN, BOOST		RAMSIN	N/A
18	31	GRAPE: Z1, Z2		RAMSIN	N/A
19	36	AUDIO: L63 CODEC		LENG	N/A
20	37	AUDIO: SPEAKER AMP		LENG	N/A
21	38	AUDIO: HEADPHONE OUT		LENG	N/A
22	39	AUDIO: BLANK		LENG	N/A
23	42	AUDIO: DETECT/MIC BIAS		LENG	N/A
24	43	AUDIO: HP/MIC FILTERS		LENG	N/A
25	54	CONNECTOR: CANADA FLEX CONN, SENSOR PANEL		MARK B.	N/A
26	55	CONNECTOR: CANADA FLEX FILTERS		MARK B.	N/A
27	56	CONNECTOR: SENSOR PANEL CONNECTOR		MARK B.	N/A
28	57	IO FLEX: DOCK COMPONENTS		JAMES	N/A
29	59	IO FELX: B2B Connector		JAMES	N/A
30	60	CONNECTOR: X23 WIFI/BT		MIKE	N/A
31	61	CONNECTOR: X24 CELLULAR/GPS		MIKE	N/A

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
32	73	POWER: ALIASES		YOSH	N/A
33	75	POWER: BATTERY CONNECTOR		YOSH	N/A
34	81	POWER: PMU		YOSH	N/A
35	82	POWER: PMU		YOSH	N/A
36	83	POWER: 3.3V VR		YOSH	N/A
37	90	DEBUG AND MISC		MIKE	N/A
38	93	FCT/ICT TEST/BRACKETS		MIKE	N/A
39	100	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
40	101	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
41	102	CONSTRAINTS: MLB RULES		MIKE	N/A
42	106	CONSTRAINTS: RF RULES		MIKE	N/A

DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE		CHOPIN MLB	
	Apple Inc.		
	DRAWING NUMBER		SIZE
	051-8962		D
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SHEET		1 OF 42	



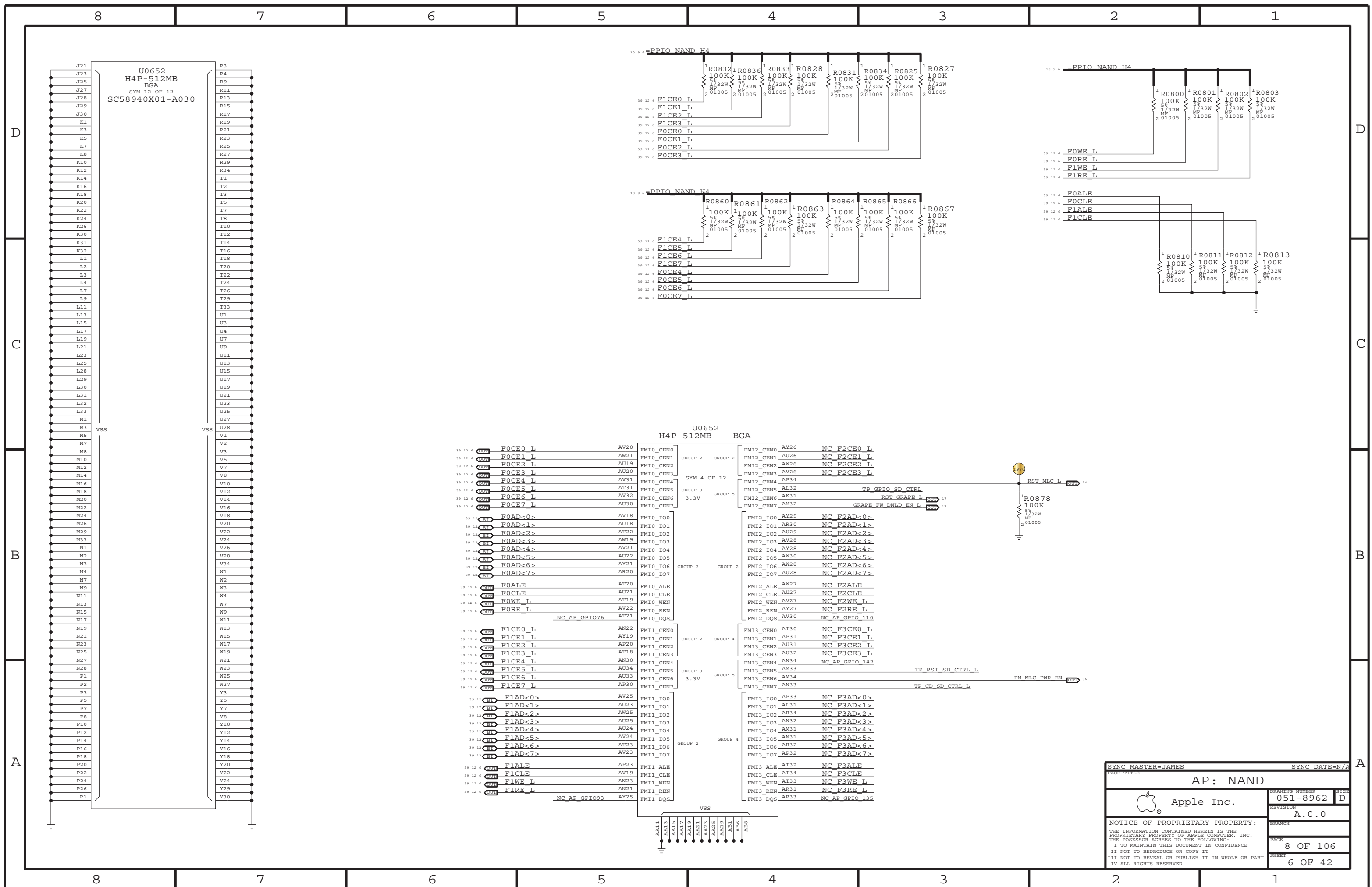


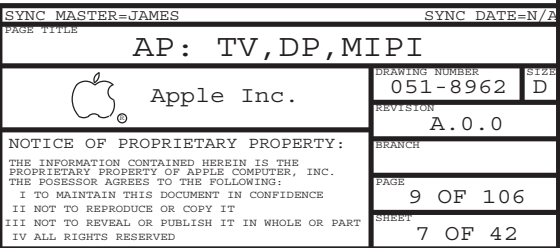
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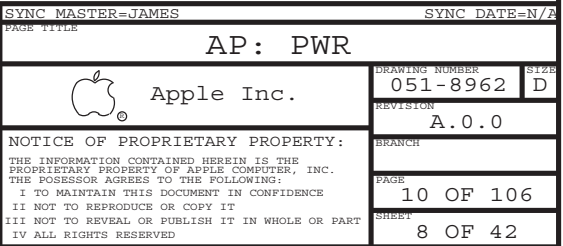
NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

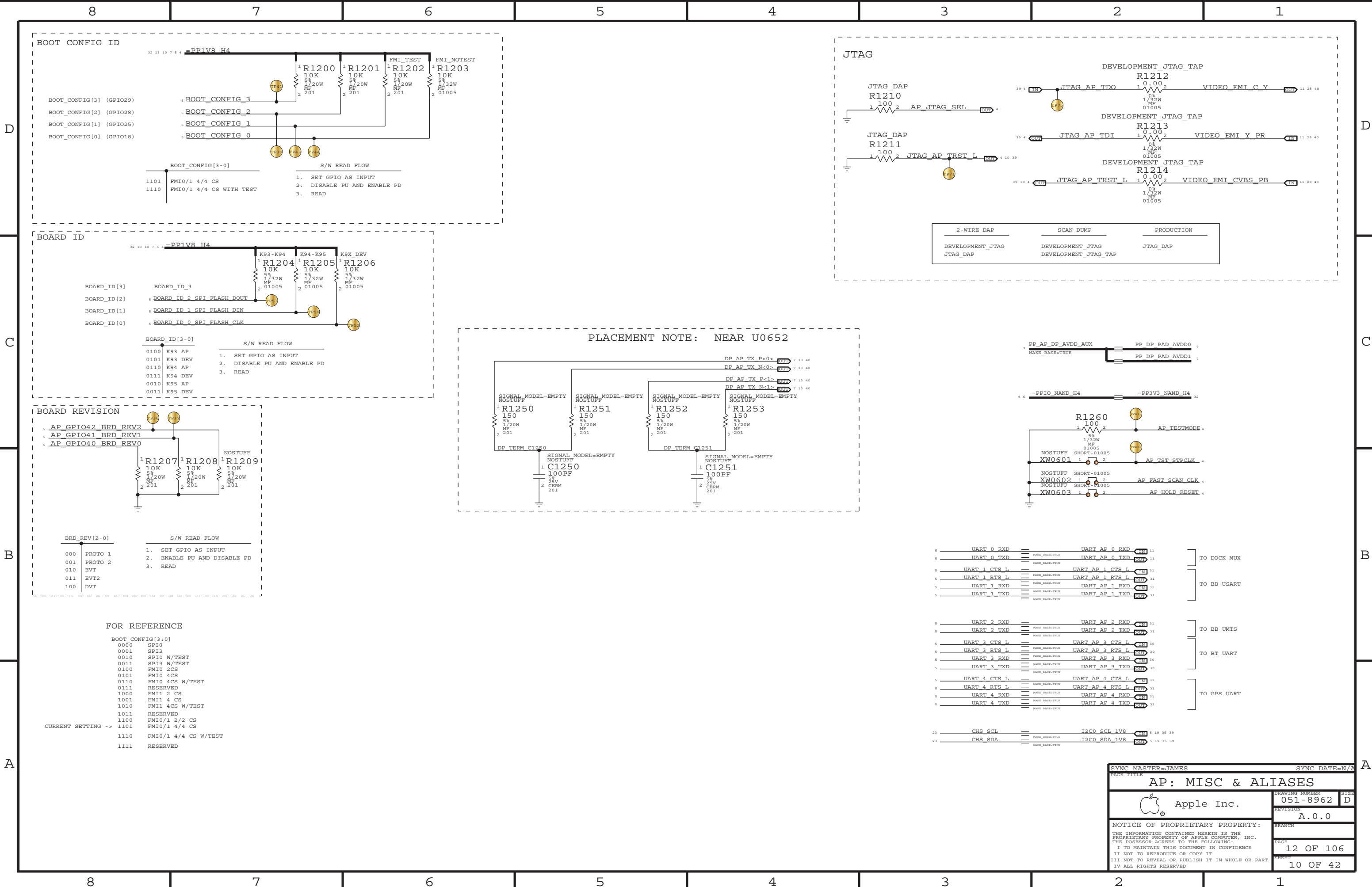
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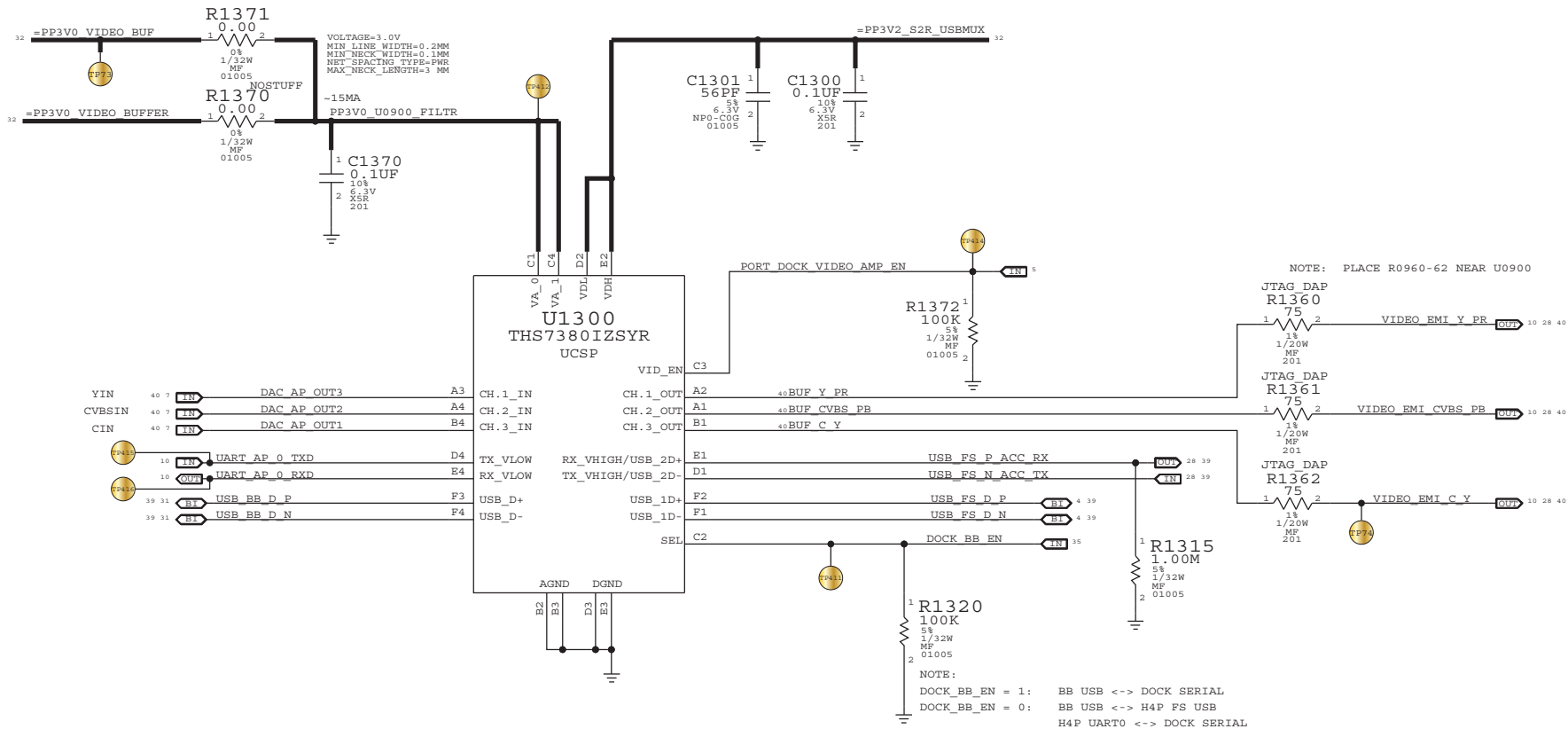





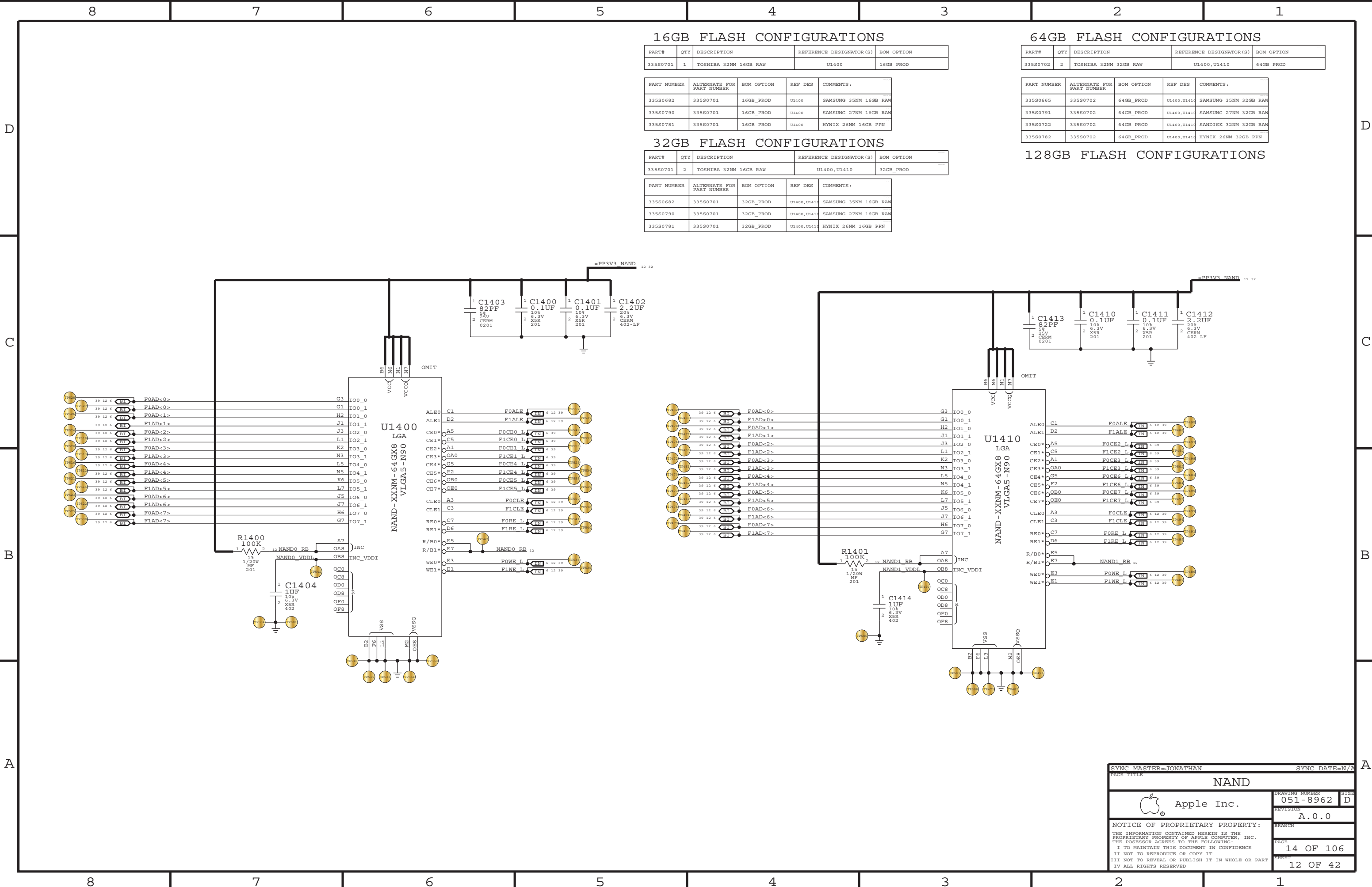




NOTE:
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370



SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE			
AP: VIDEO BUFFER,BB USB MUXES			
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	051-8962		D
	REVISION		
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16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400, U1410	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400, U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400, U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400, U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400, U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400, U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400, U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400, U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400, U1410	HYNIX 26NM 32GB PPN


128GB FLASH CONFIGURATIONS

SYNC MASTER=JONATHAN

SYNC DATE=N/A

PAGE TITLE

NAND

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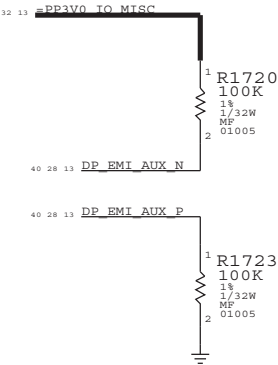
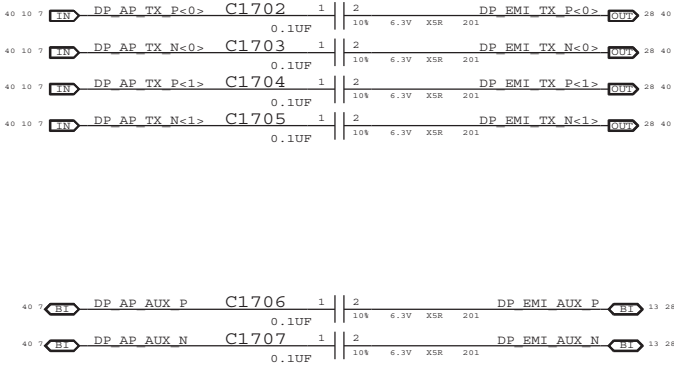
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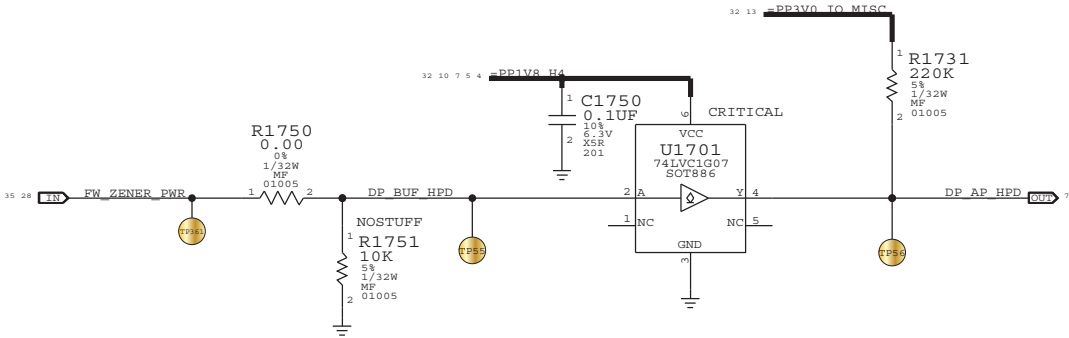
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DISPLAYPORT AC COUPLING



DISPLAYPORT HOT PLUG DETECT

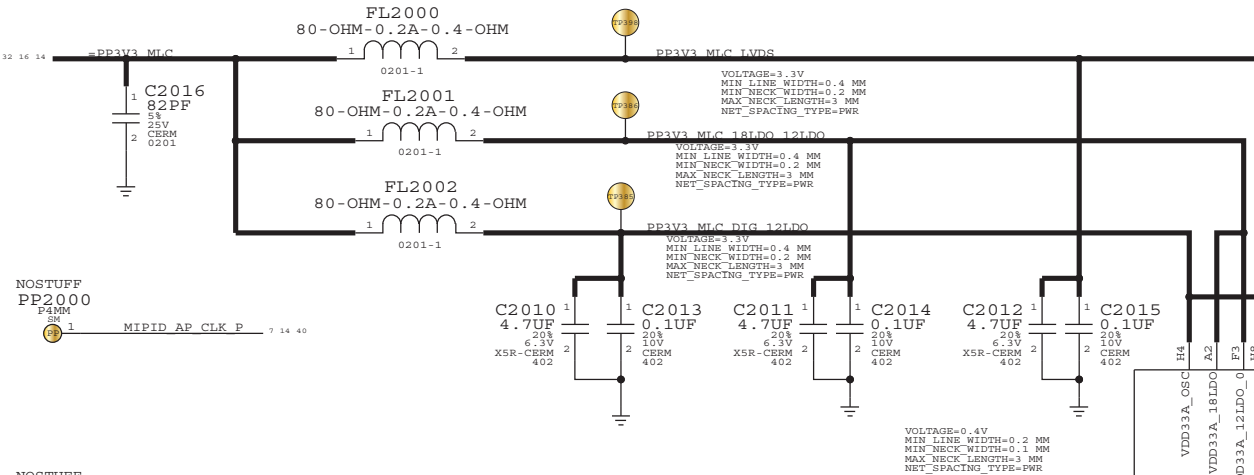
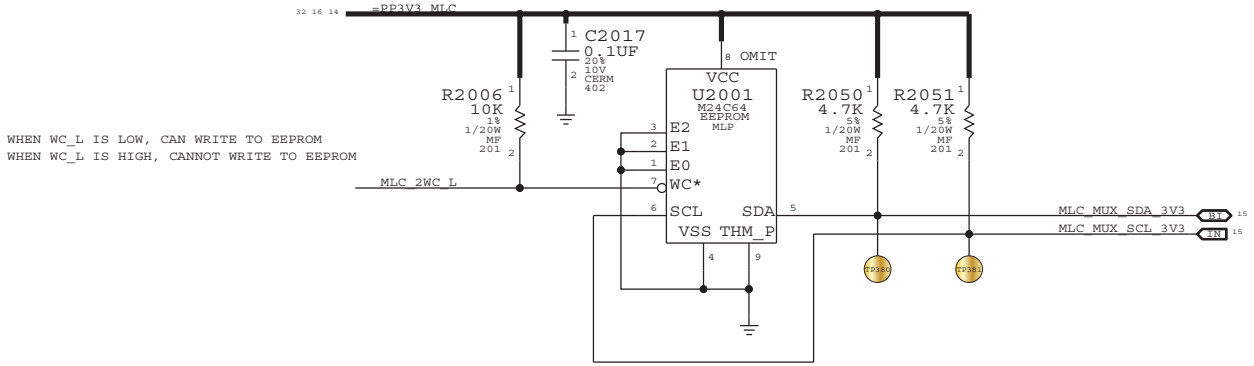


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

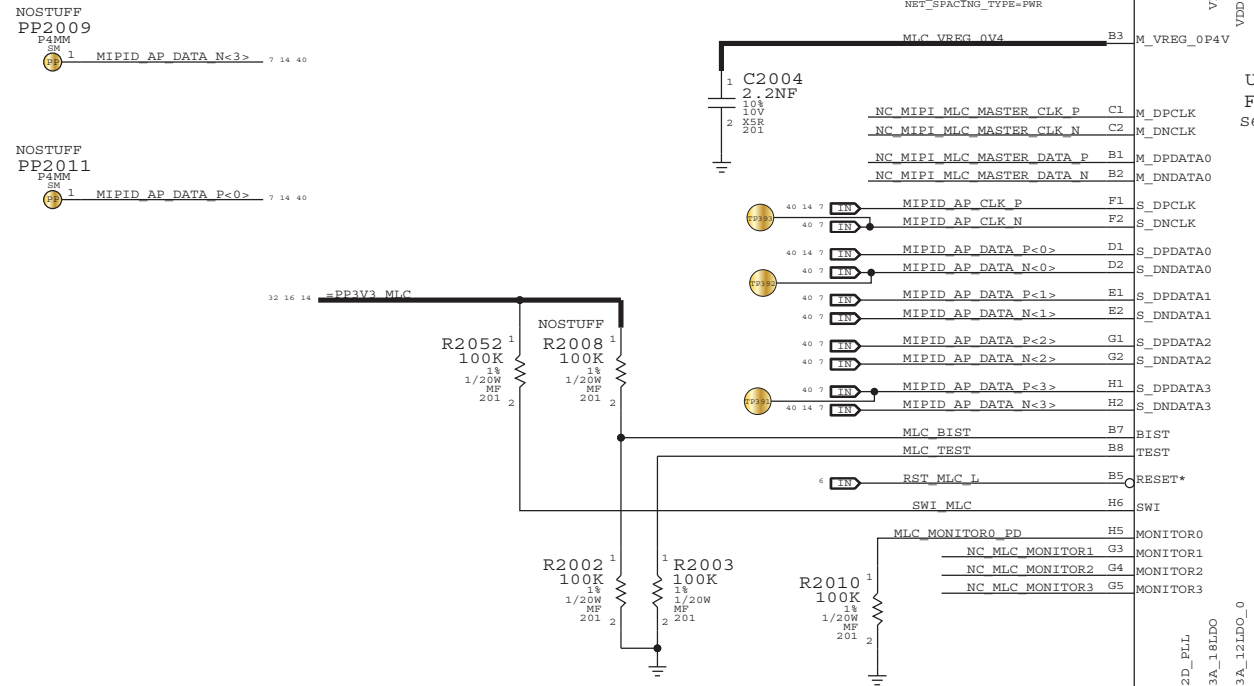
SYNC MASTER=JAMES		SYNC DATE=N/A	
PAGE TITLE			
VIDEO: DISPLAY PORT			
 Apple Inc.	DRAWING NUMBER	051-8962	SIZE D
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		PAGE	17 OF 106
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MLC EEPROM:RAW APN 335S0661

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307



MLC_SCL	MLC_SCL_3V3	15
MLC_SDA	MLC_SDA_3V3	15
EDID_SCL	LVDS_DDC_CLK	16
EDID_SDA	LVDS_DDC_DATA	16
TCLKP	LVDS_CLK_P	16 40
TCLKN	LVDS_CLK_N	16 40
TAP	LVDS_DATA_P<0>	16 40
TAN	LVDS_DATA_N<0>	16 40
TBP	LVDS_DATA_P<1>	16 40
TBN	LVDS_DATA_N<1>	16 40
TCP	LVDS_DATA_P<2>	16 40
TCN	LVDS_DATA_N<2>	16 40
TDP	NC LVDS_DATA_P<3>	
TDN	NC LVDS_DATA_N<3>	
ROUT_LVDS	ROUT_LVDS	
VSYNC	TP_MLC_VSYNC	
PWM	TP_PM_LCD_BKLT_PWM	
PPC	PM_MLC_PPC_OUT	
MONITOR4	NC MLC MONITOR4	
MONITOR5	NC MLC MONITOR5	
MONITOR6	NC MLC MONITOR6	

PAGE TITLE		PAGE NUMBER	
VIDEO: MLC		051-8962	
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SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS (ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
PAGE TITLE VIDEO: LVDS CONNECTOR			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
		REVISION A.0.0	
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LVDS (LCD) CONNECTOR

CABLINE-CA CONNECTOR: 518S0787
NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

VIDEO: LVDS CONNECTOR

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PAGE: 22 OF 106
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LVDS (LCD) CONNECTOR

CABLINE-CA CONNECTOR: 518S0787
NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

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VIDEO: LVDS CONNECTOR

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PAGE: 22 OF 106
SHEET: 16 OF 42

LVDS (LCD) CONNECTOR

CABLINE-CA CONNECTOR: 518S0787
NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

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VIDEO: LVDS CONNECTOR

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PAGE: 22 OF 106
SHEET: 16 OF 42

LVDS (LCD) CONNECTOR

CABLINE-CA CONNECTOR: 518S0787
NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

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VIDEO: LVDS CONNECTOR

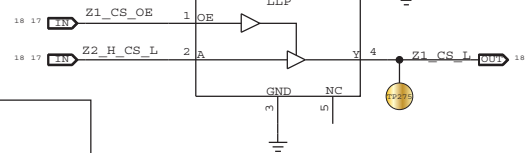
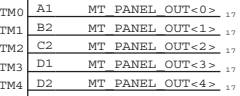
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C



SYNCH MASTER-RAMSN		SYNCH DATE-N/A	
PAGE TITLE			
GRADE: GROUNDHOG, CONN, BOOST			
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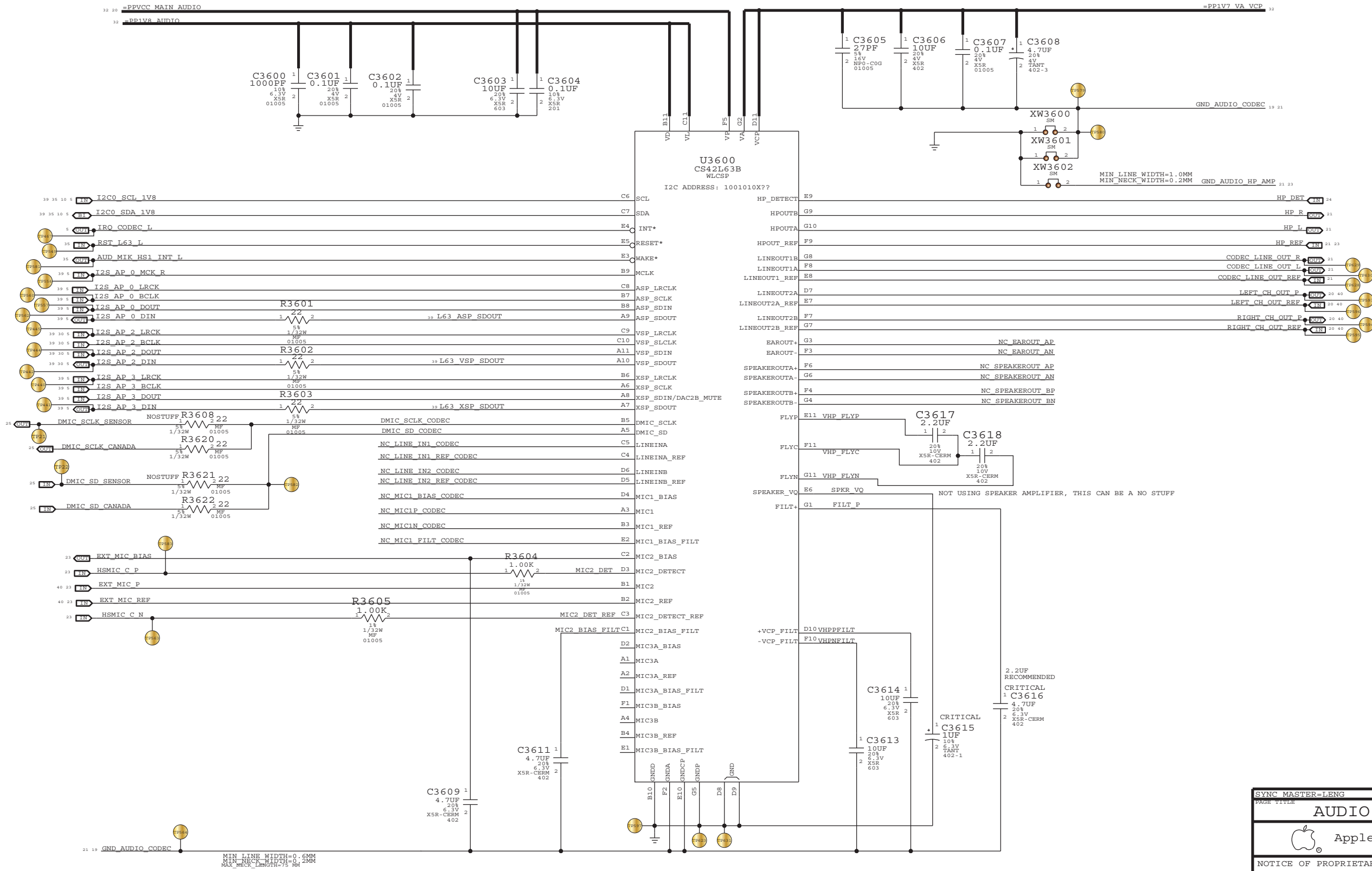
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L63 AUDIO CODEC
APN:338S0940



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: L63 CODEC			
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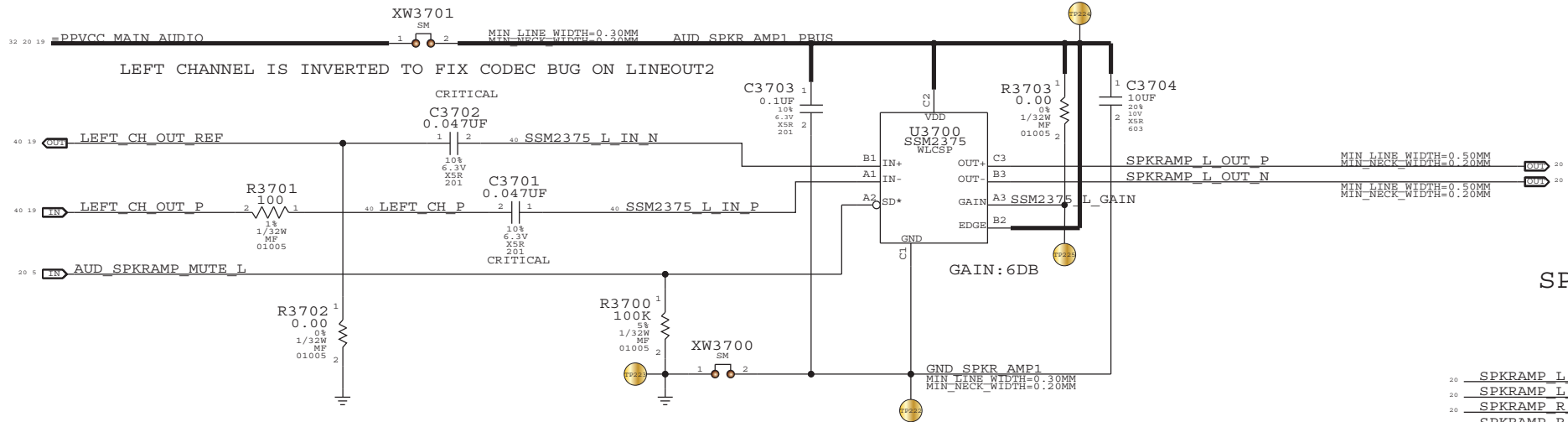
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SPEAKER AMPLIFIER 1

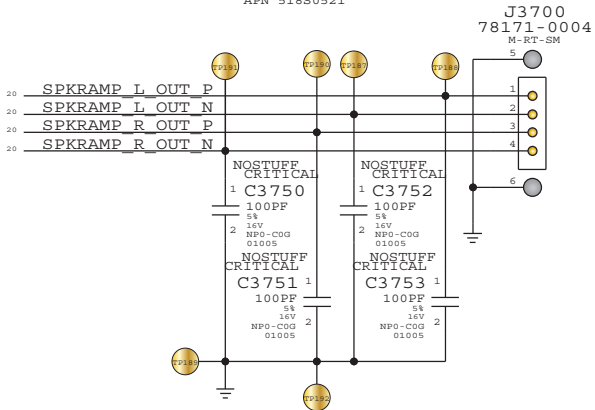
APN:353S2958
TURN ON TIME: 7.5MS
80HZ +/- XXX%
TURN ON DELAY: 20MS



GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT

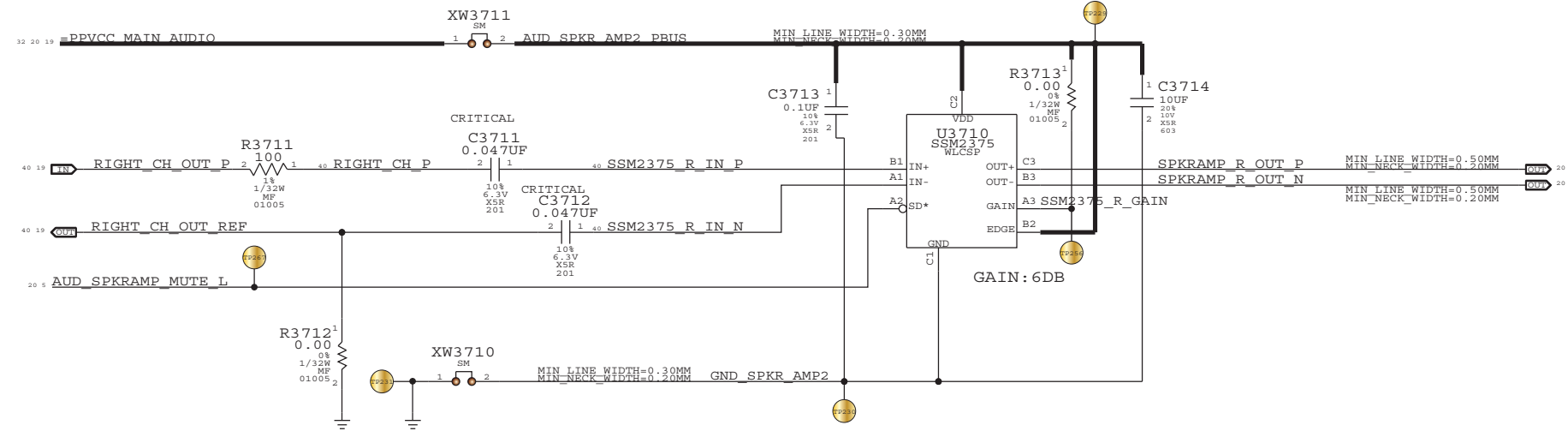
SPEAKER CONNECTOR


APN 518S0521



L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

SPEAKER AMPLIFIER 2



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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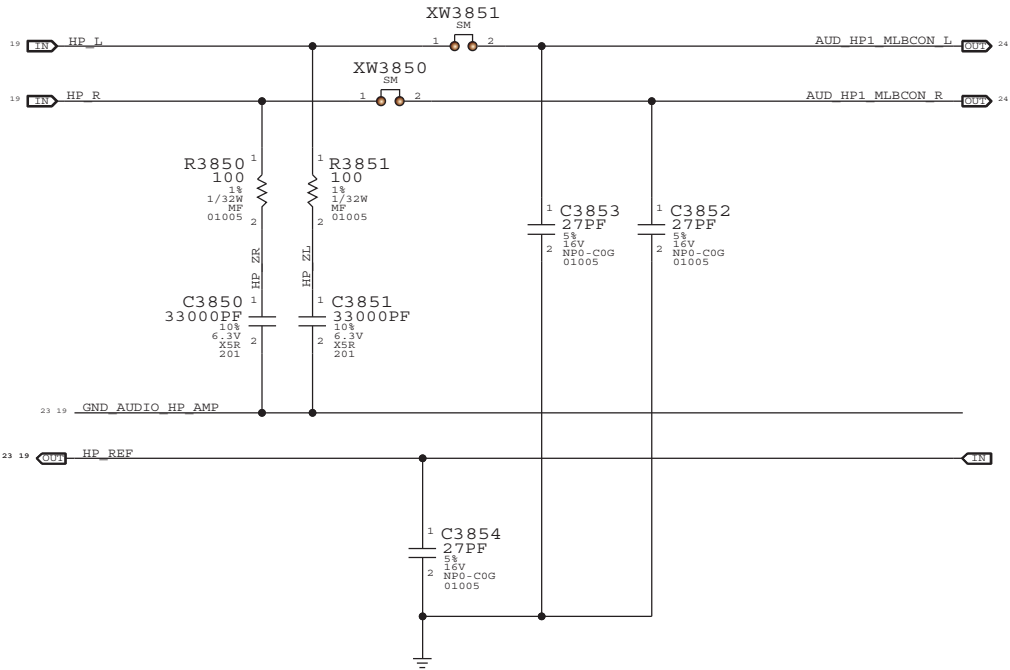
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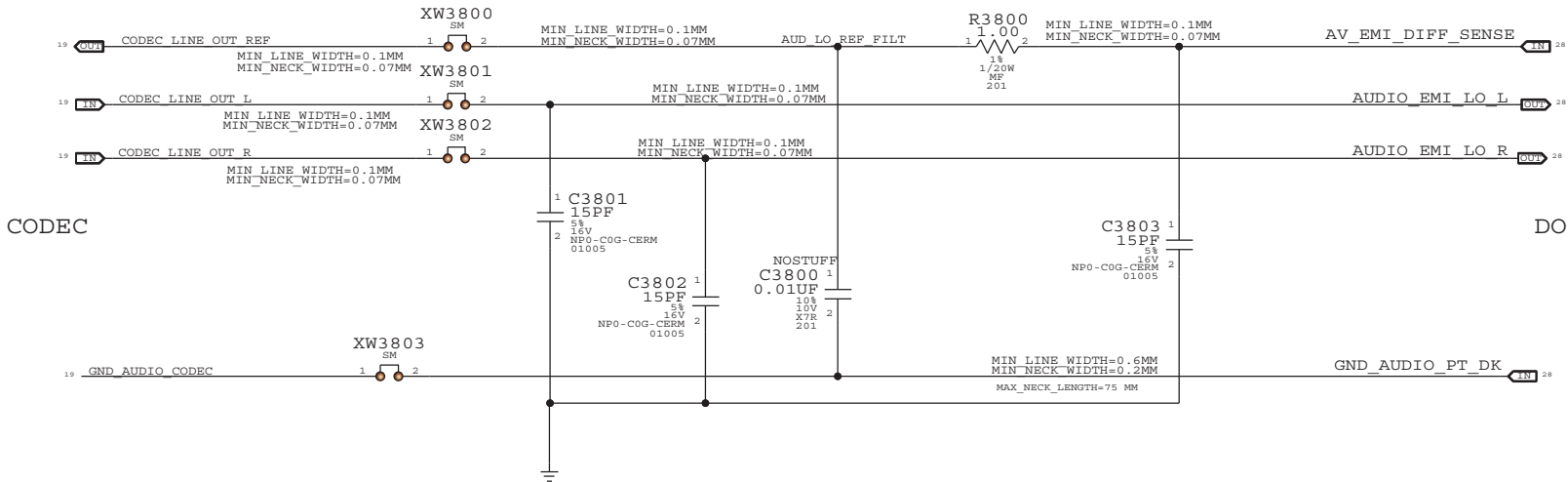
B


A

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: HEADPHONE OUT			
 Apple Inc.		DRAWING NUMBER	051-8962
		SIZE	D
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		BRANCH	
		PAGE	38 OF 106
		SHEET	21 OF 42

D

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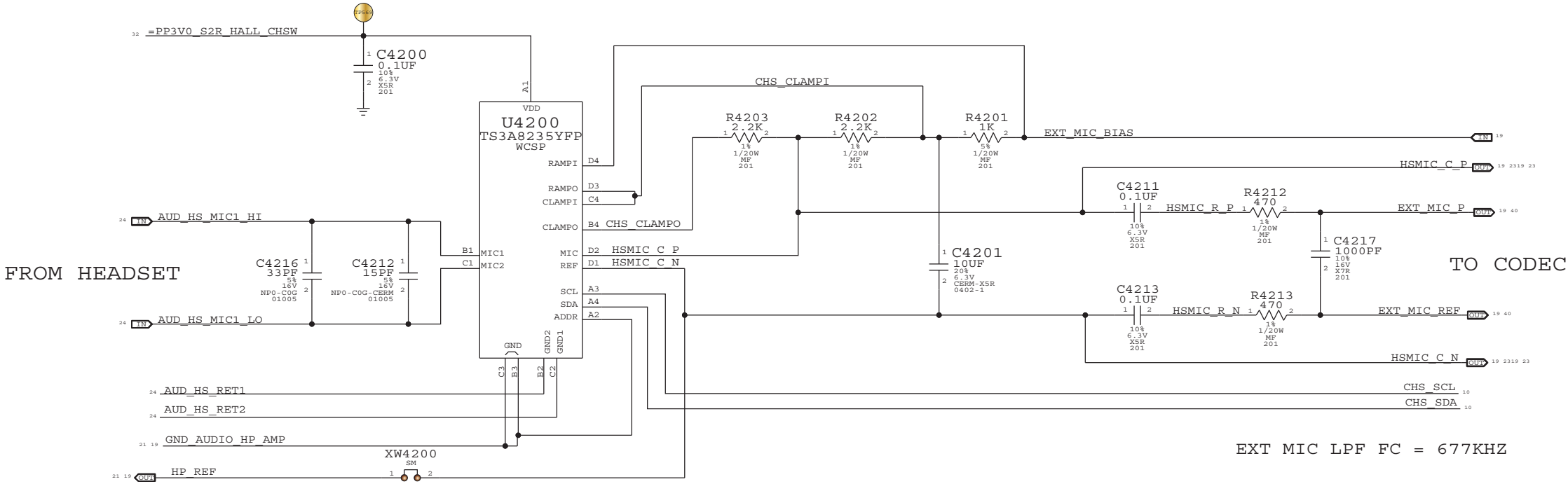
D


C

B

A

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: DETECT/MIC BIAS			
 Apple Inc.		DRAWING NUMBER	051-8962
		REVISION	A.0.0
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		PAGE	42 OF 106
		SHEET	23 OF 42

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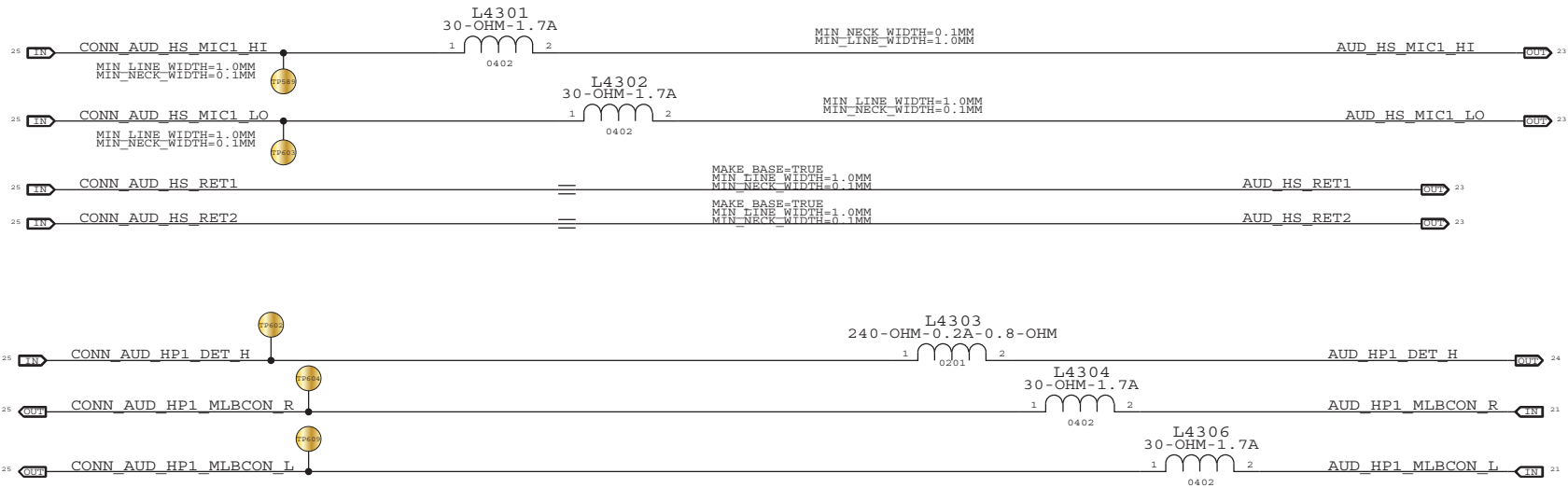
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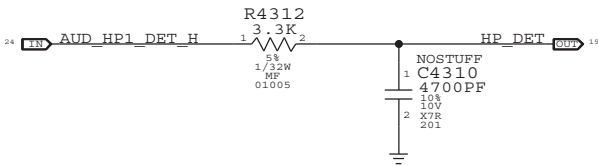
B


A

HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



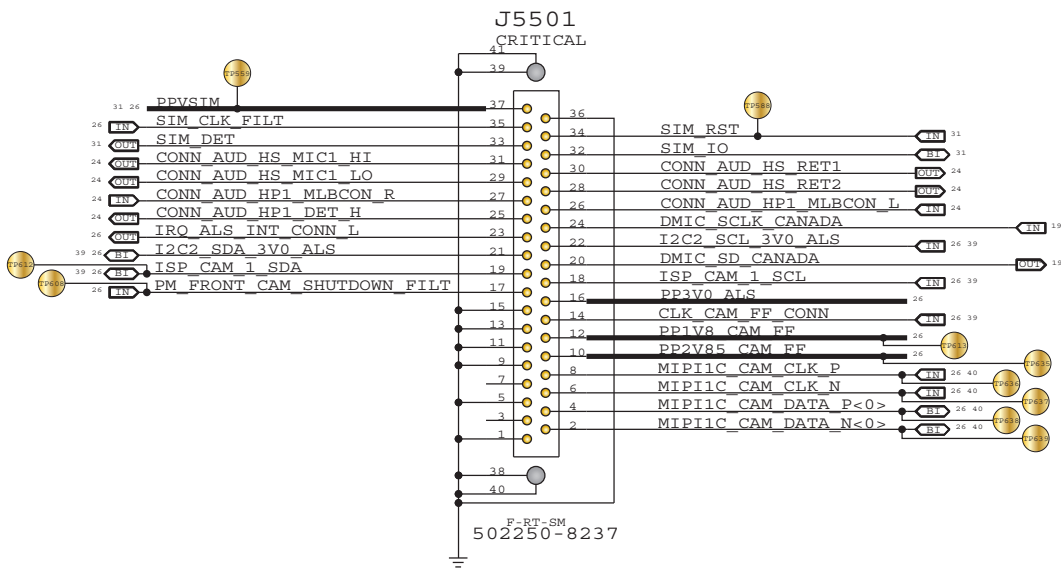
HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE			
AUDIO: HP/MIC FILTERS			
 Apple Inc.		DRAWING NUMBER	051-8962
		SIZE	D
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		BRANCH	
		PAGE	43 OF 106
		SHEET	24 OF 42

CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

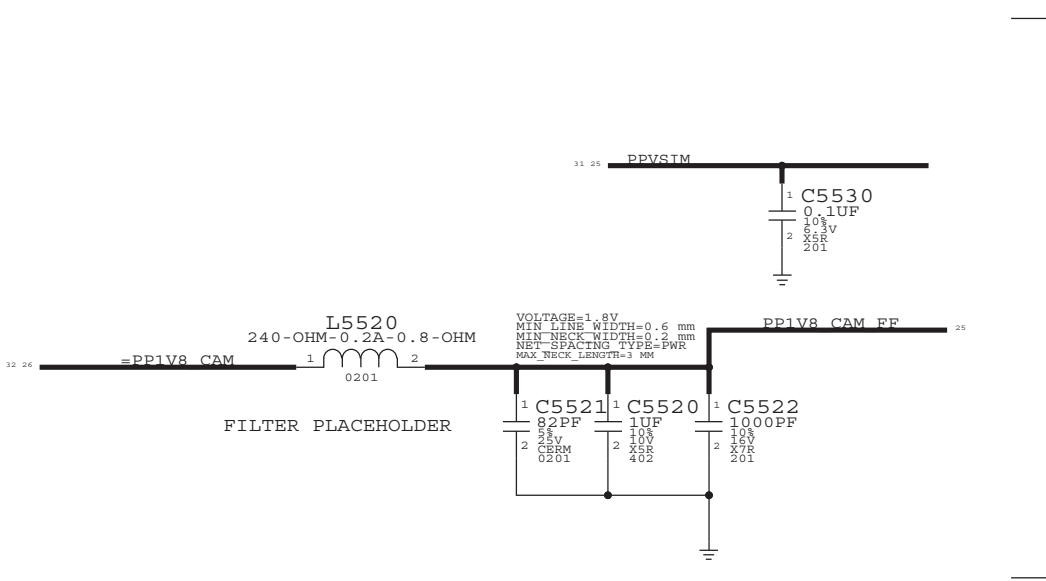
39	27	CLK_CAM_RF_FILT	==	CONN_CLK_CAM_RF_FILT	27	
40	27	MIPIOC_CAM_DATA N<0>	MAKE_BASE+TRUE	==	CONN_MIPIOC_CAM_DATA N<0>	27
40	27	MIPIOC_CAM_DATA P<0>	MAKE_BASE+TRUE	==	CONN_MIPIOC_CAM_DATA P<0>	27
40	27	MIPIOC_CAM_CLK N	MAKE_BASE+TRUE	==	CONN_MIPIOC_CAM_CLK N	27
40	27	MIPIOC_CAM_CLK P	MAKE_BASE+TRUE	==	CONN_MIPIOC_CAM_CLK P	27
7	27	PM_REAR_CAM_SHUTDOWN	MAKE_BASE+TRUE	==	CONN_PM_REAR_CAM_SHUTDOWN	27
27	27	PP1V8_SENSOR_FILT	MAKE_BASE+TRUE	==	CONN_PP1V8_SENSOR_FILT	27
27	27	PP2V85_CAM_REAR	MAKE_BASE+TRUE	==	CONN_PP2V85_CAM_REAR	27
19	27	DMIC_SD_SENSOR	MAKE_BASE+TRUE	==	CONN_DMIC_SD_SENSOR	27
19	27	DMIC_SCLK_SENSOR	MAKE_BASE+TRUE	==	CONN_DMIC_SCLK_SENSOR	27
19	27	ISP_AP_0_SCL	MAKE_BASE+TRUE	==	CONN_ISP_AP_0_SCL	27
19	27	ISP_AP_0_SDA	MAKE_BASE+TRUE	==	CONN_ISP_AP_0_SDA	27
19	27	I2C2_SCL_3V0	MAKE_BASE+TRUE	==	CONN_I2C2_SCL_3V0	27
19	27	I2C2_SDA_3V0	MAKE_BASE+TRUE	==	CONN_I2C2_SDA_3V0	27
19	27	IRQ_ACCEL_INT1_L	MAKE_BASE+TRUE	==	CONN_IRQ_ACCEL_INT1_L	27
19	27	IRQ_ACCEL_INT2_L	MAKE_BASE+TRUE	==	CONN_IRQ_ACCEL_INT2_L	27
19	27	IRQ_GYRO_INT1	MAKE_BASE+TRUE	==	CONN_IRQ_GYRO_INT1	27
19	27	IRQ_GYRO_INT2	MAKE_BASE+TRUE	==	CONN_IRQ_GYRO_INT2	27
19	27	I2C1_SCL_1V8	MAKE_BASE+TRUE	==	CONN_I2C1_SCL_1V8	27
19	27	I2C1_SDA_1V8	MAKE_BASE+TRUE	==	CONN_I2C1_SDA_1V8	27
19	27	IRQ_HALL	MAKE_BASE+TRUE	==	CONN_IRQ_HALL	27
19	27	IRQ_PROX_INT_L	MAKE_BASE+TRUE	==	CONN_IRQ_PROX_INT_L	27
19	27	PP3V0_S2R_HALL_FILT	MAKE_BASE+TRUE	==	CONN_PP3V0_S2R_HALL	27
19	27	ONOFF_L	MAKE_BASE+TRUE	==	CONN_ONOFF_FTR_L	27
19	27	SRL_L	MAKE_BASE+TRUE	==	CONN_SRL_FTR_L	27
19	27	AUD_VOL_UP_L	MAKE_BASE+TRUE	==	CONN_AUD_VOL_UP_FTR_L	27
19	27	AUD_VOL_DOWN_L	MAKE_BASE+TRUE	==	CONN_AUD_VOL_DOWN_FTR_L	27
27	27	PP3V0_OPTICAL_SENS	MAKE_BASE+TRUE	==	CONN_PP3V0_OPTICAL_SENS	27

D

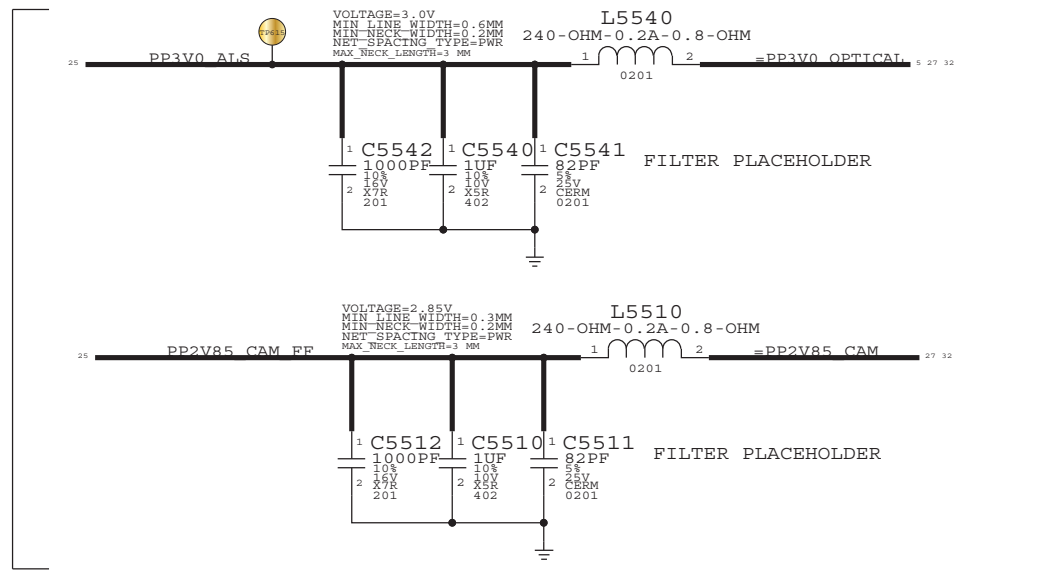
C

D

C



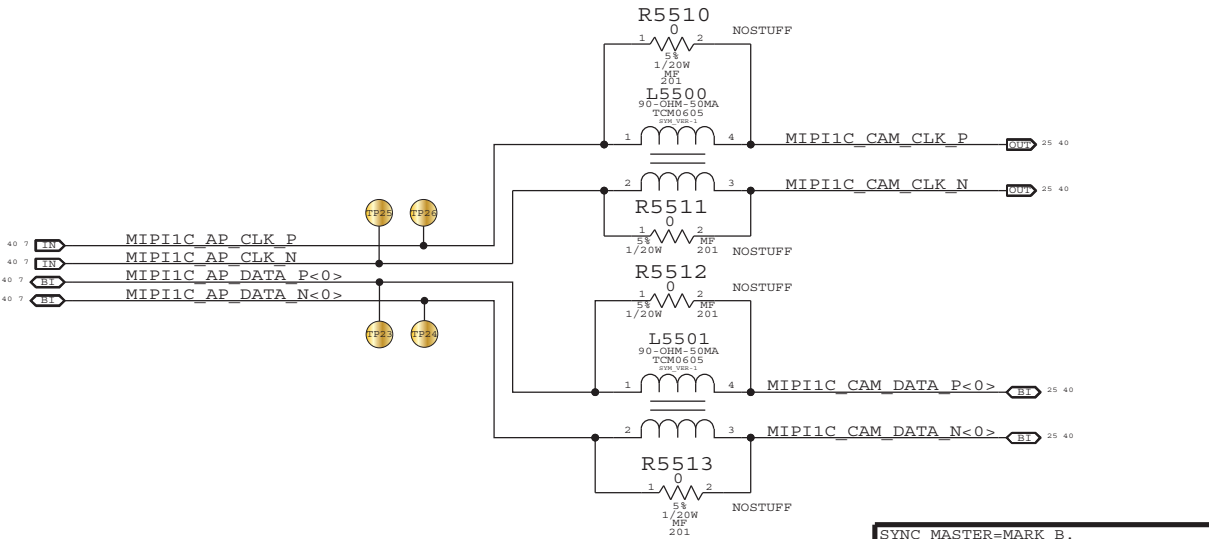
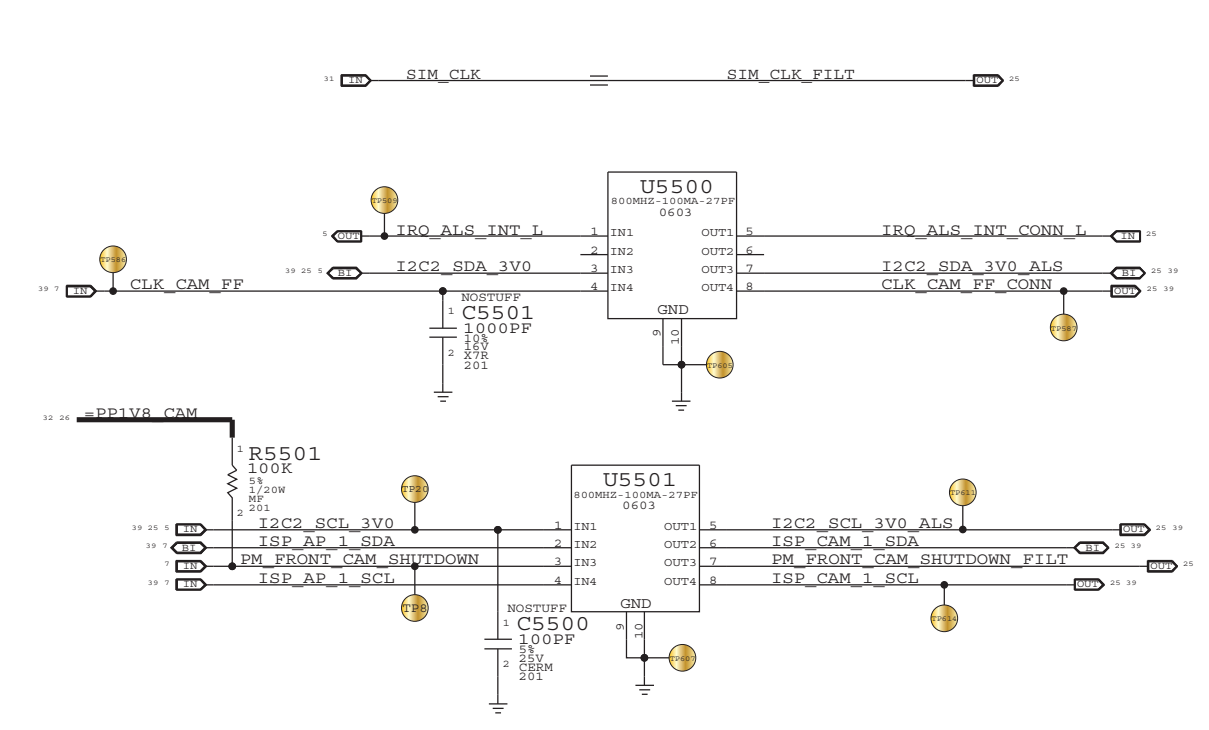
CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS


B

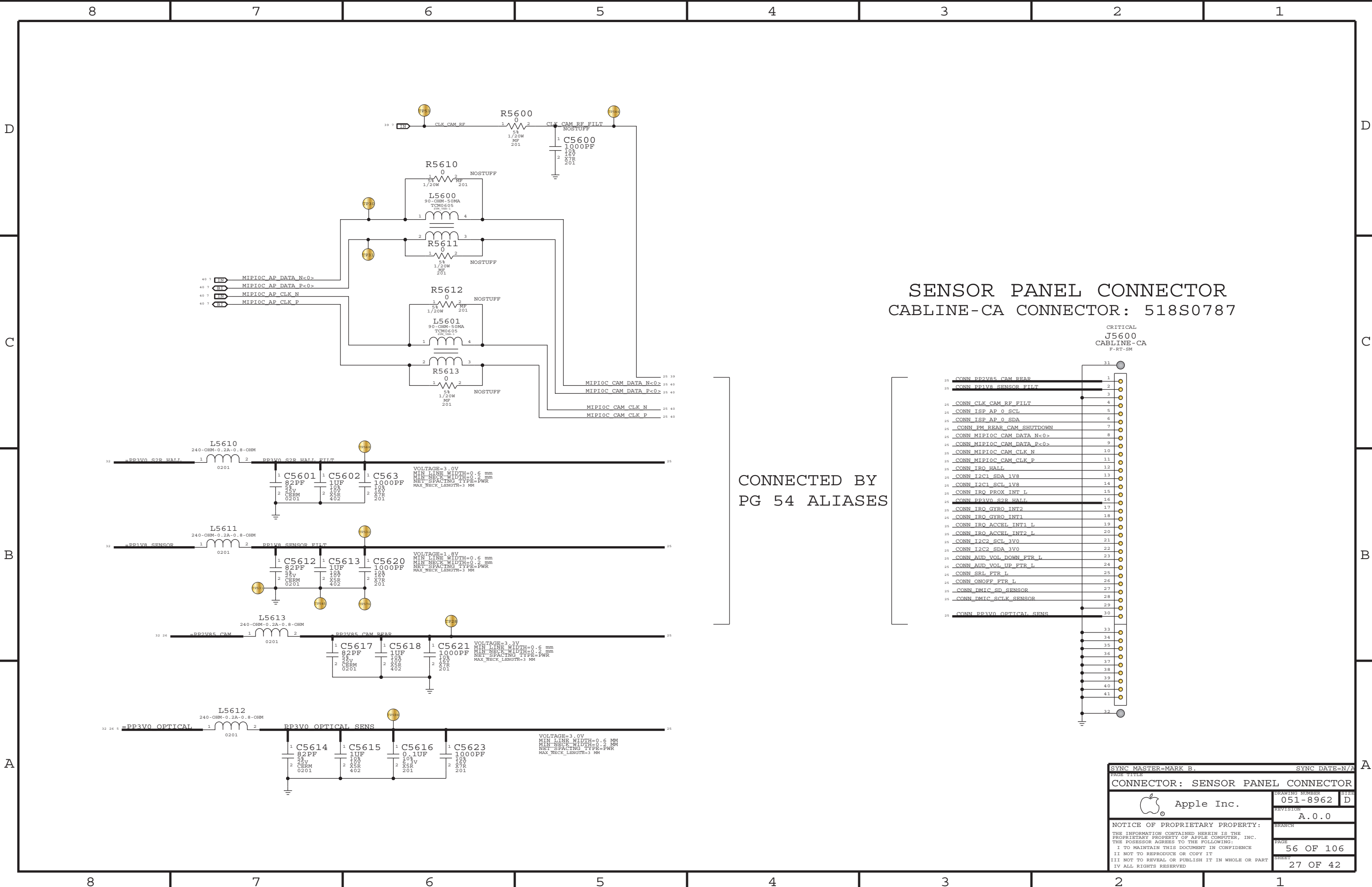
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A


SYNC MASTER=MARK B.		SYNC DATE=N/A	
PAGE TITLE			
CONNECTOR: CANADA FLEX FILTERS			
 Apple Inc.		DRAWING NUMBER	051-8962
		SIZE	D
		REVISION	A.0.0
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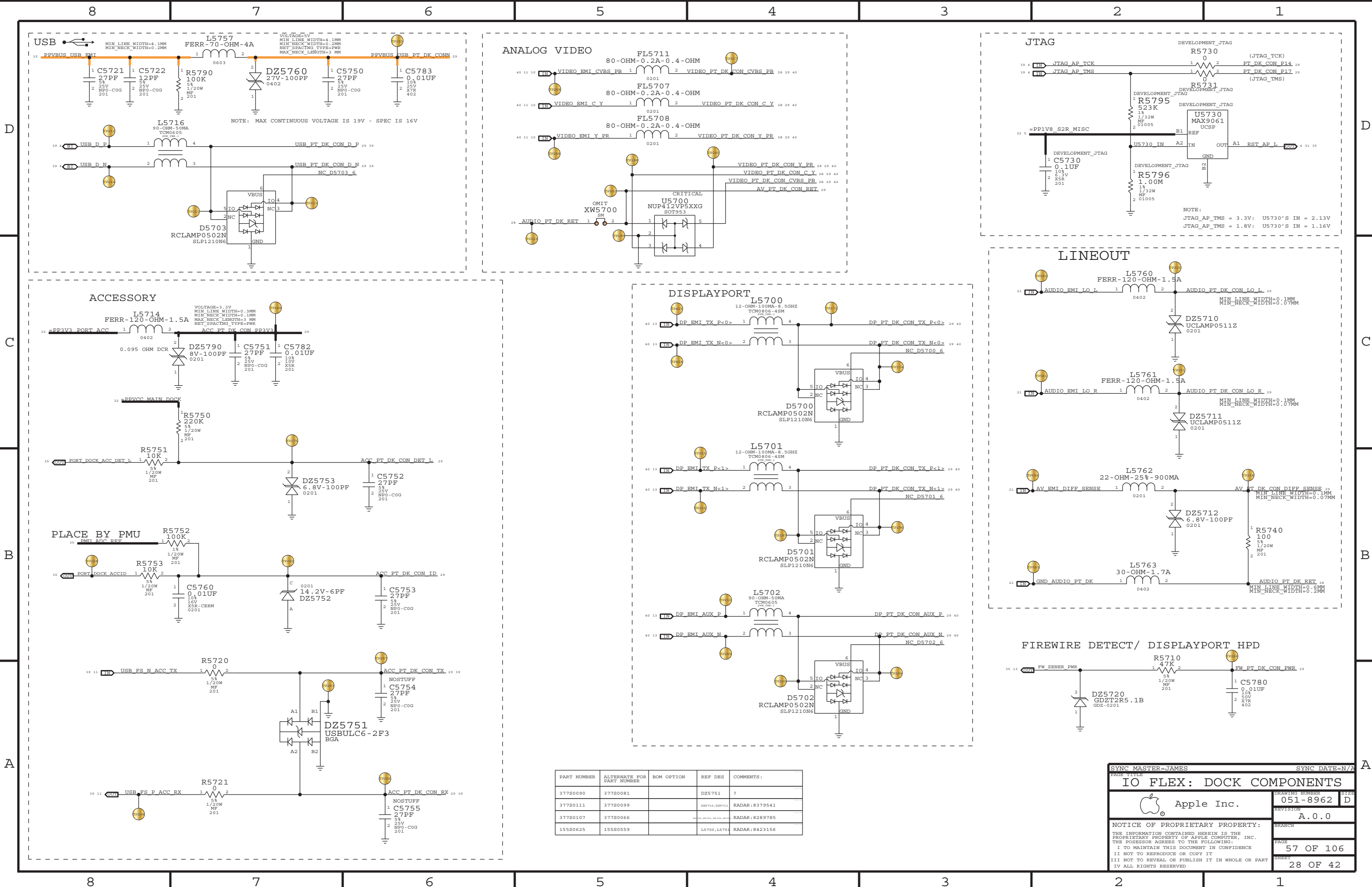


SENSOR PANEL CONNECTOR CABLINE-CA CONNECTOR: 518S0787

CRITICAL
J5600
CABLINE-CA
F-RT-SM

CONN PP2V85 CAM REAR	1
CONN PP1V8 SENSOR FILT	2
CONN CLK CAM RF FILT	3
CONN ISP AP 0 SCL	4
CONN ISP AP 0 SDA	5
CONN PM REAR CAM SHUTDOWN	6
CONN MIPI0C CAM DATA N<0>	7
CONN MIPI0C CAM DATA P<0>	8
CONN MIPI0C CAM CLK N	9
CONN MIPI0C CAM CLK P	10
CONN I2C1 SDA 1V8	11
CONN I2C1 SCL 1V8	12
CONN IRQ PROX INT L	13
CONN PP3V0 S2R HALL	14
CONN IRQ GYRO INT2	15
CONN IRQ GYRO INT1	16
CONN IRQ ACCEL INT1 L	17
CONN IRQ ACCEL INT2 L	18
CONN I2C2 SCL 3V0	19
CONN I2C2 SDA 3V0	20
CONN AUD_VOL_DOWN_FTR L	21
CONN AUD_VOL_UP_FTR L	22
CONN SRL_FTR L	23
CONN ONOFF_FTR L	24
CONN DMIC_SD_SENSOR	25
CONN DMIC_SCLK_SENSOR	26
CONN PP3V0 OPTICAL SENS	27
CONN PP3V0 OPTICAL SENS	28
CONN PP3V0 OPTICAL SENS	29
CONN PP3V0 OPTICAL SENS	30
CONN PP3V0 OPTICAL SENS	31
CONN PP3V0 OPTICAL SENS	32

SYNC MASTER=MARK B.		SYNC DATE=N/A	
PAGE TITLE			
CONNECTOR: SENSOR PANEL CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SHEET
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		A.0.0	
		BRANCH	
		PAGE	56 OF 106
		SHEET	27 OF 42




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710, DZ5711	RADAR: 8379541
377S0107	377S0066		DZ5710, DZ5711, DZ5712	RADAR: 8289785
155S0625	155S0559		L5700, L5701	RADAR: 8423156

SYNC MASTER=JAMES

SYNC DATE=N/A

IO FLEX: DOCK COMPONENTS

 Apple Inc.

DRAWING NUMBER
051-8962

SIZE
D

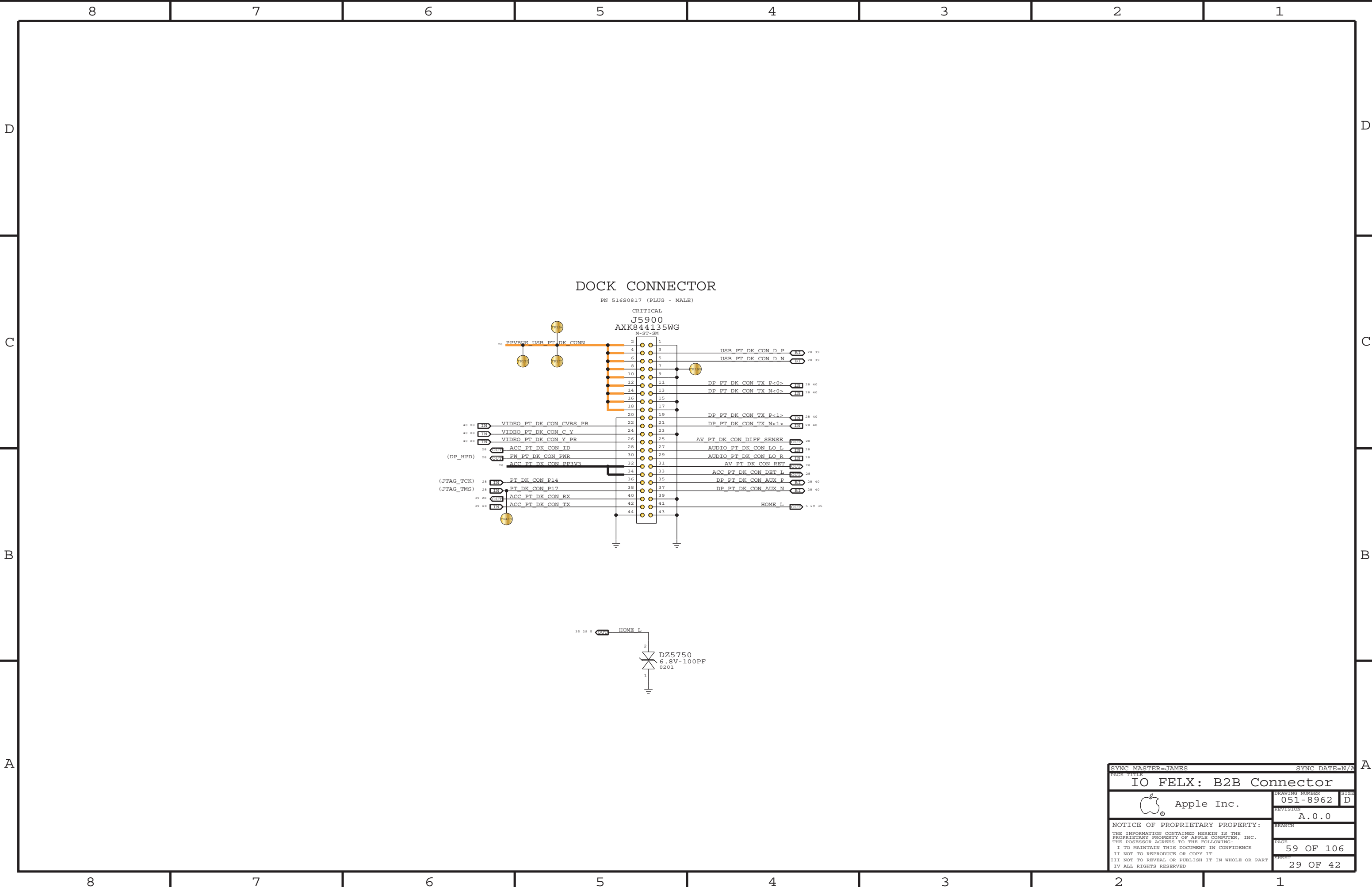
REVISION
A.0.0

BRANCH

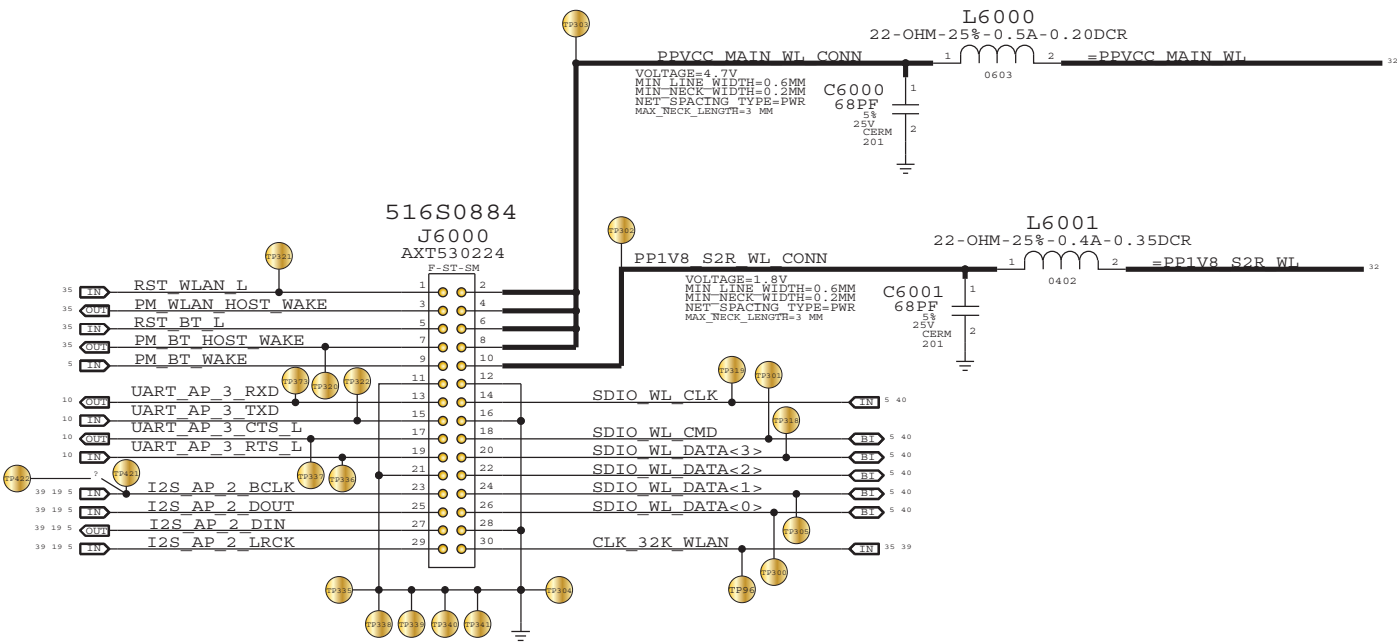
PAGE
57 OF 106

SHEET
28 OF 42

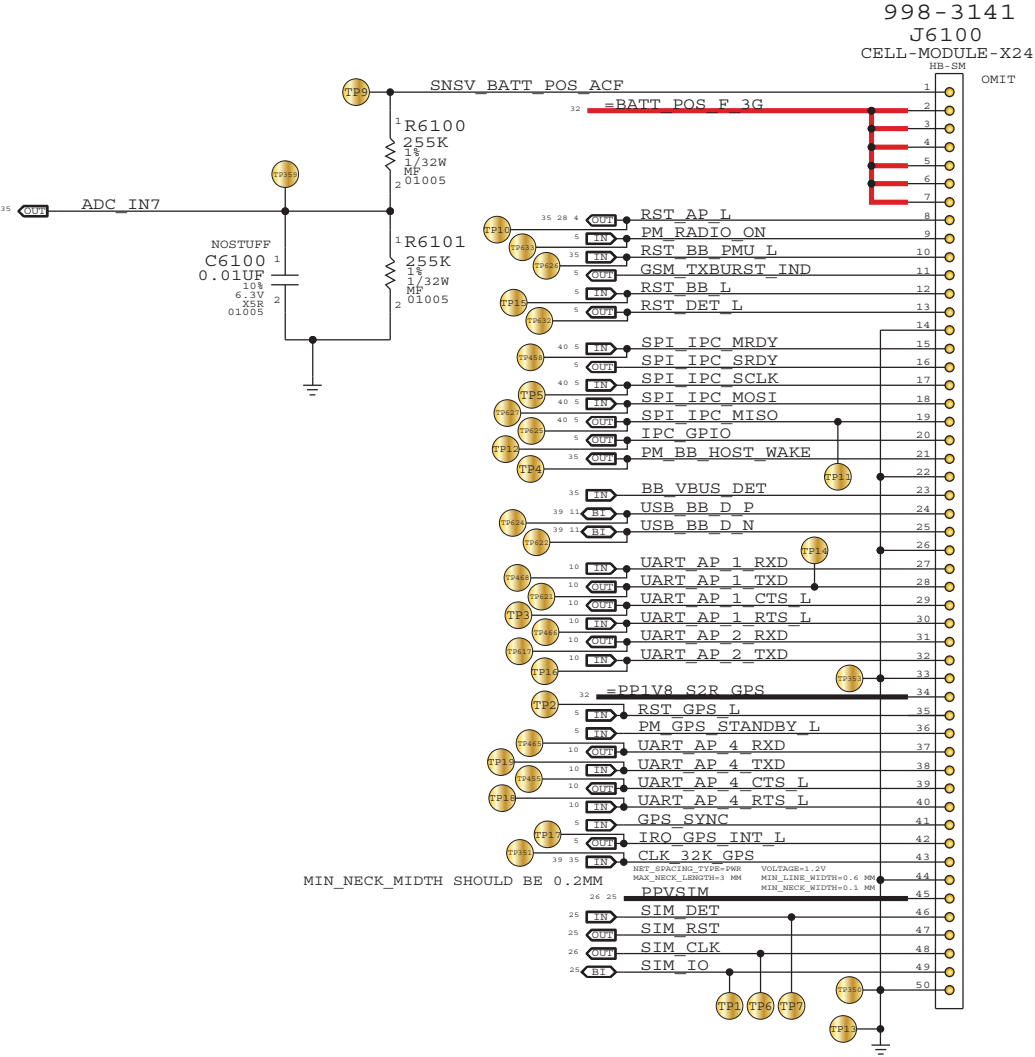
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X23 WIFI/BT CONNECTOR



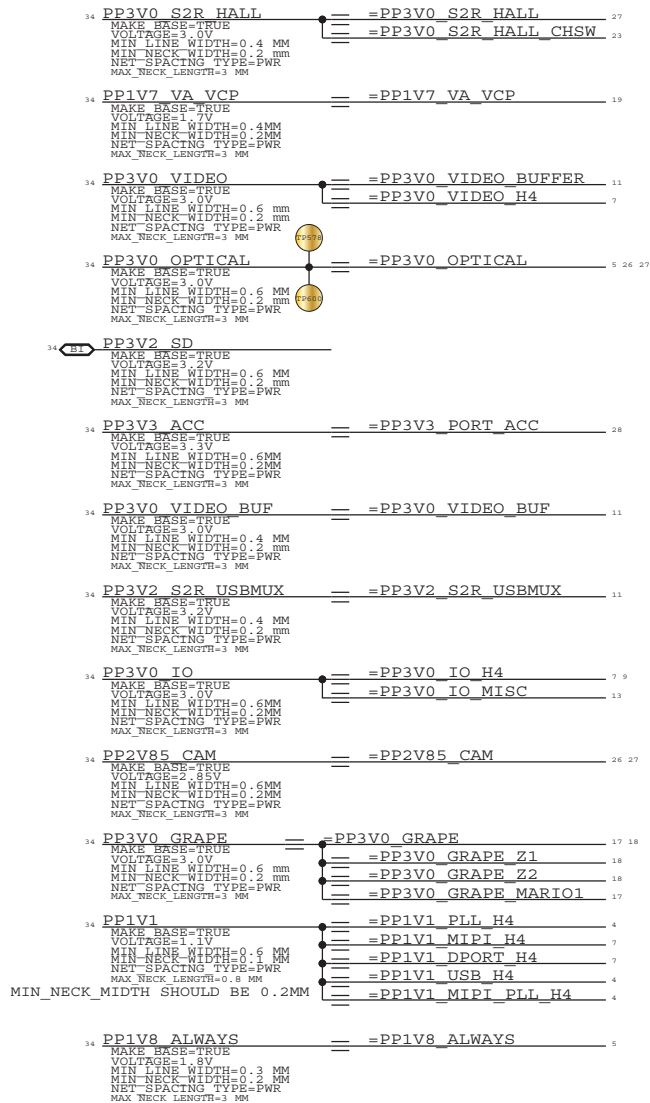
X24 CELLULAR/GPS CONNECTOR



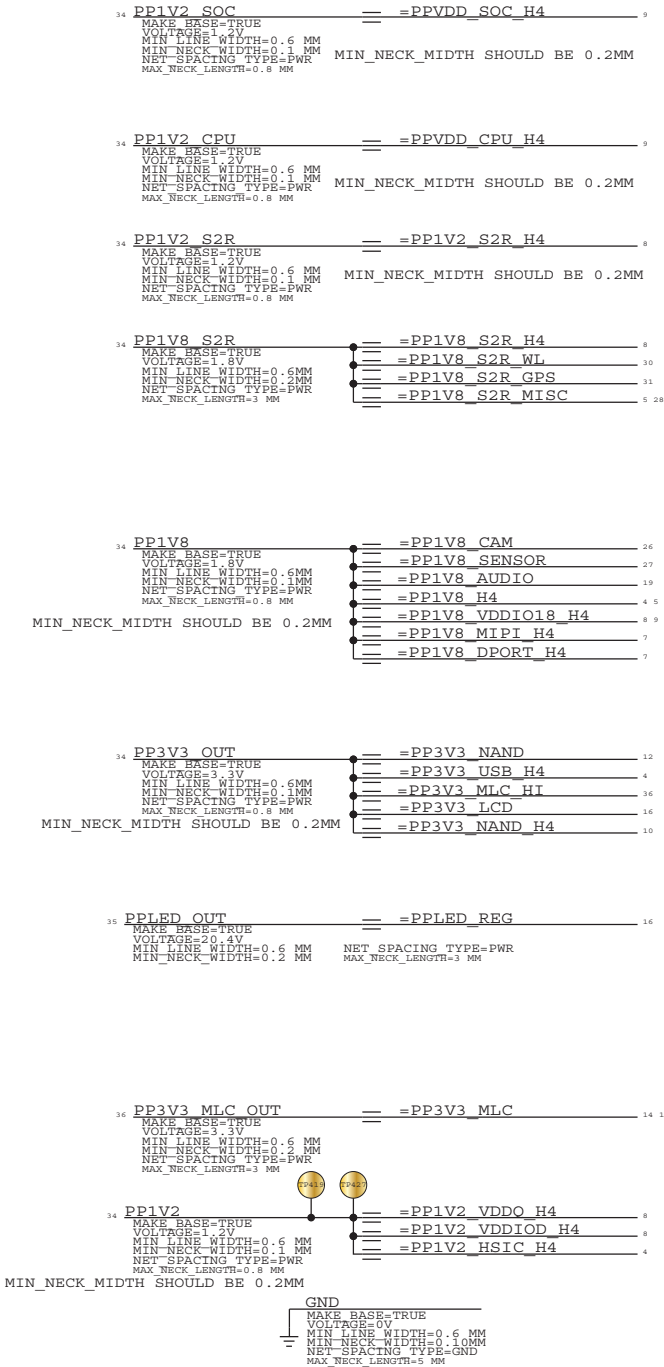
POWER CONN / ALIAS

LDO RAILS

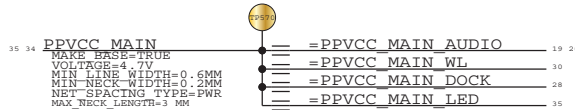
PROGRAMMABLE ON/OFF



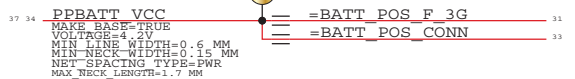
BUCK RAILS



CHARGER MAIN




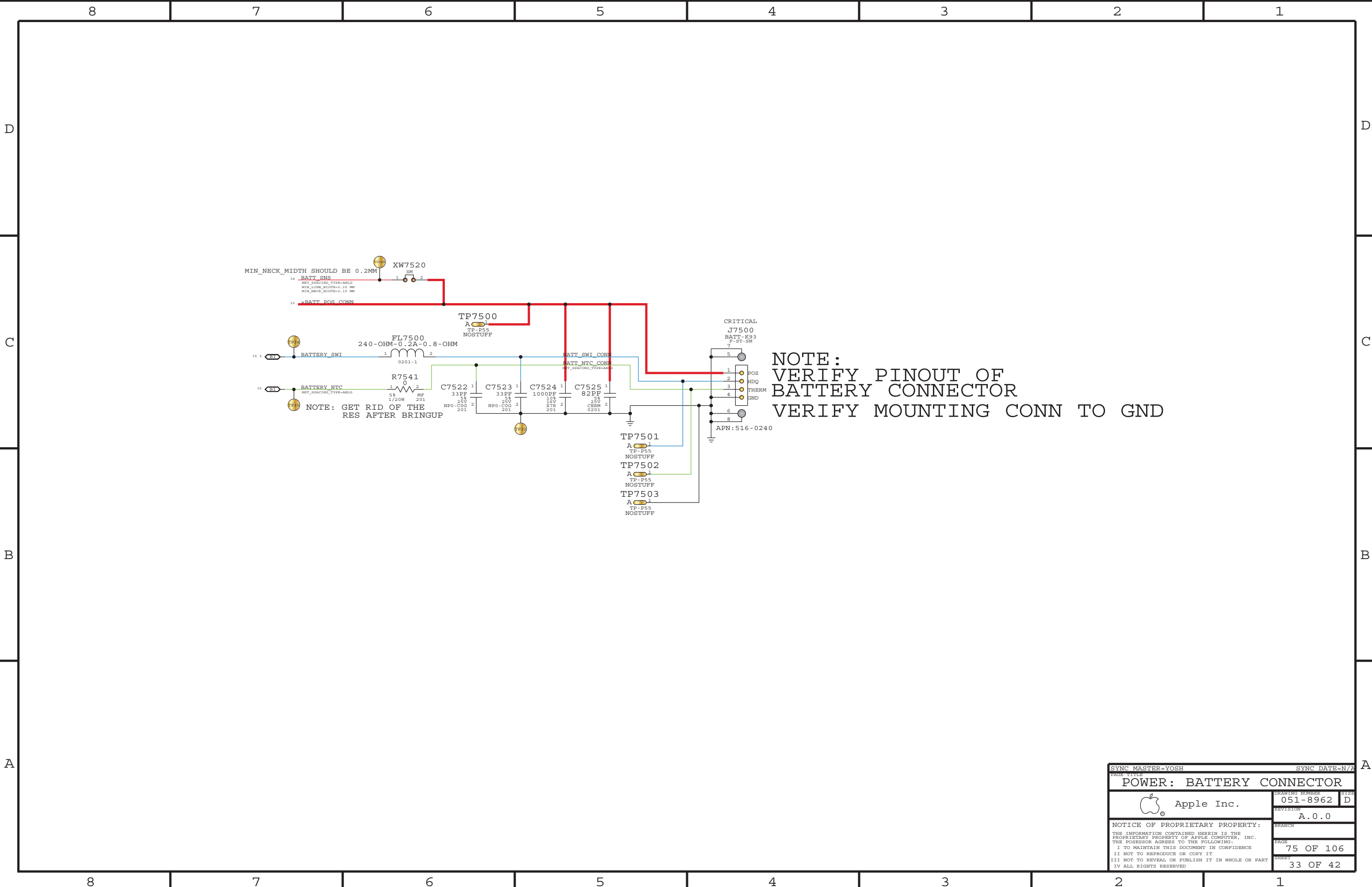
BATTERY



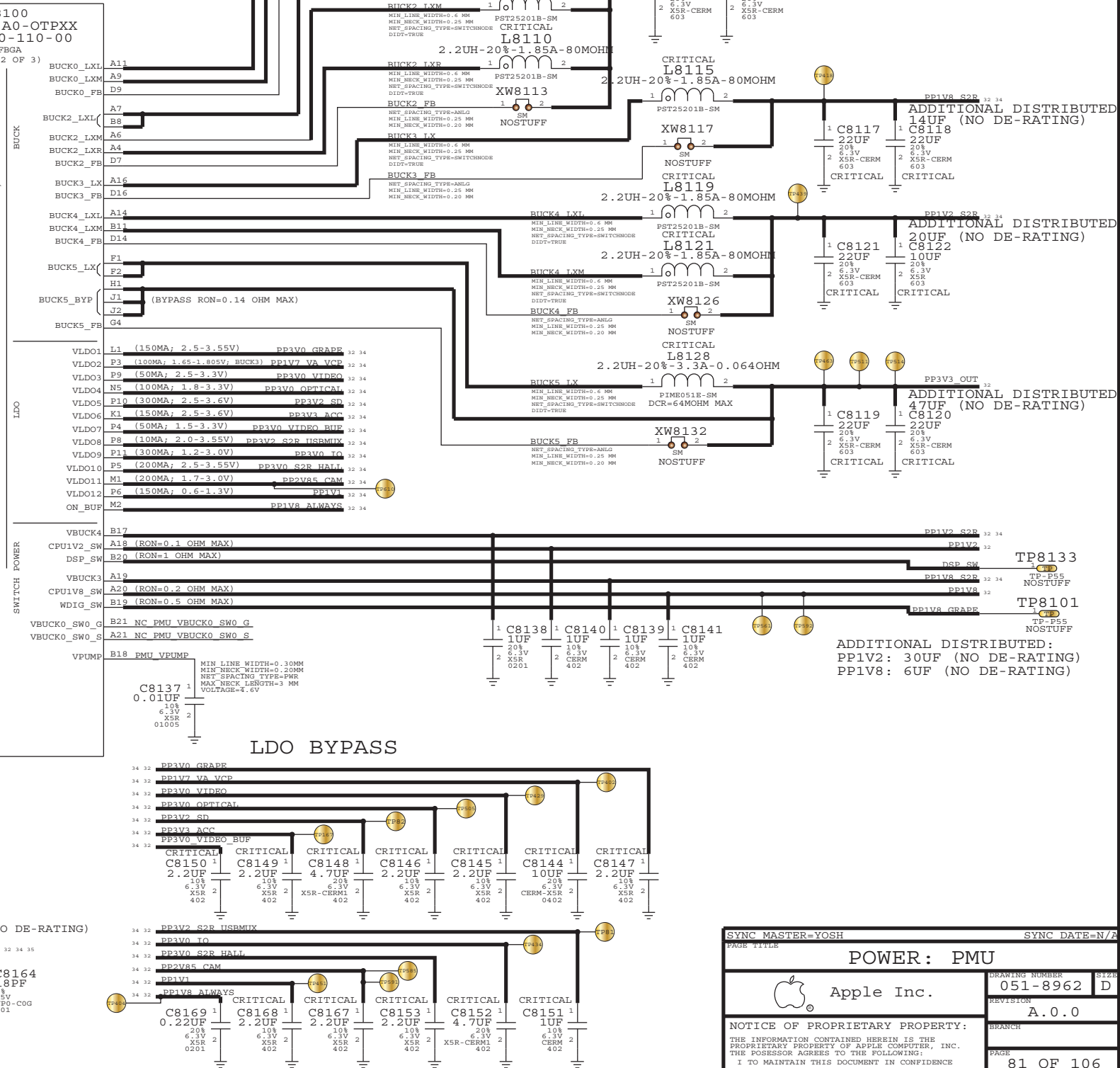
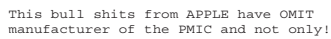
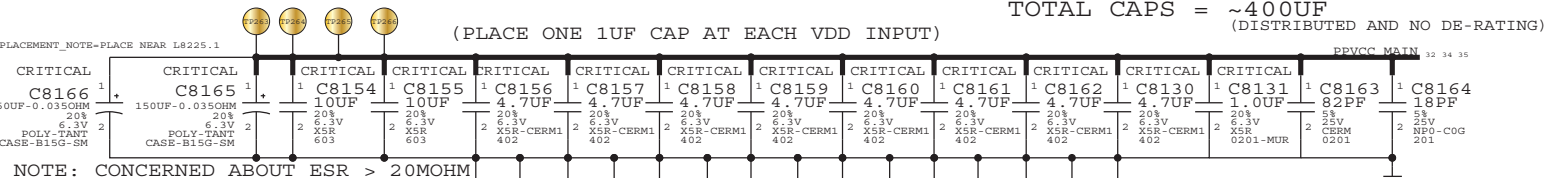
USB POWER INPUT




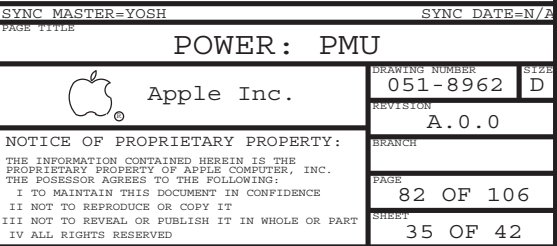
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PAGE TITLE			
POWER: ALIASES			
 Apple Inc.		DRAWING NUMBER	051-8962
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		PAGE	73 OF 106
		SHEET	32 OF 42

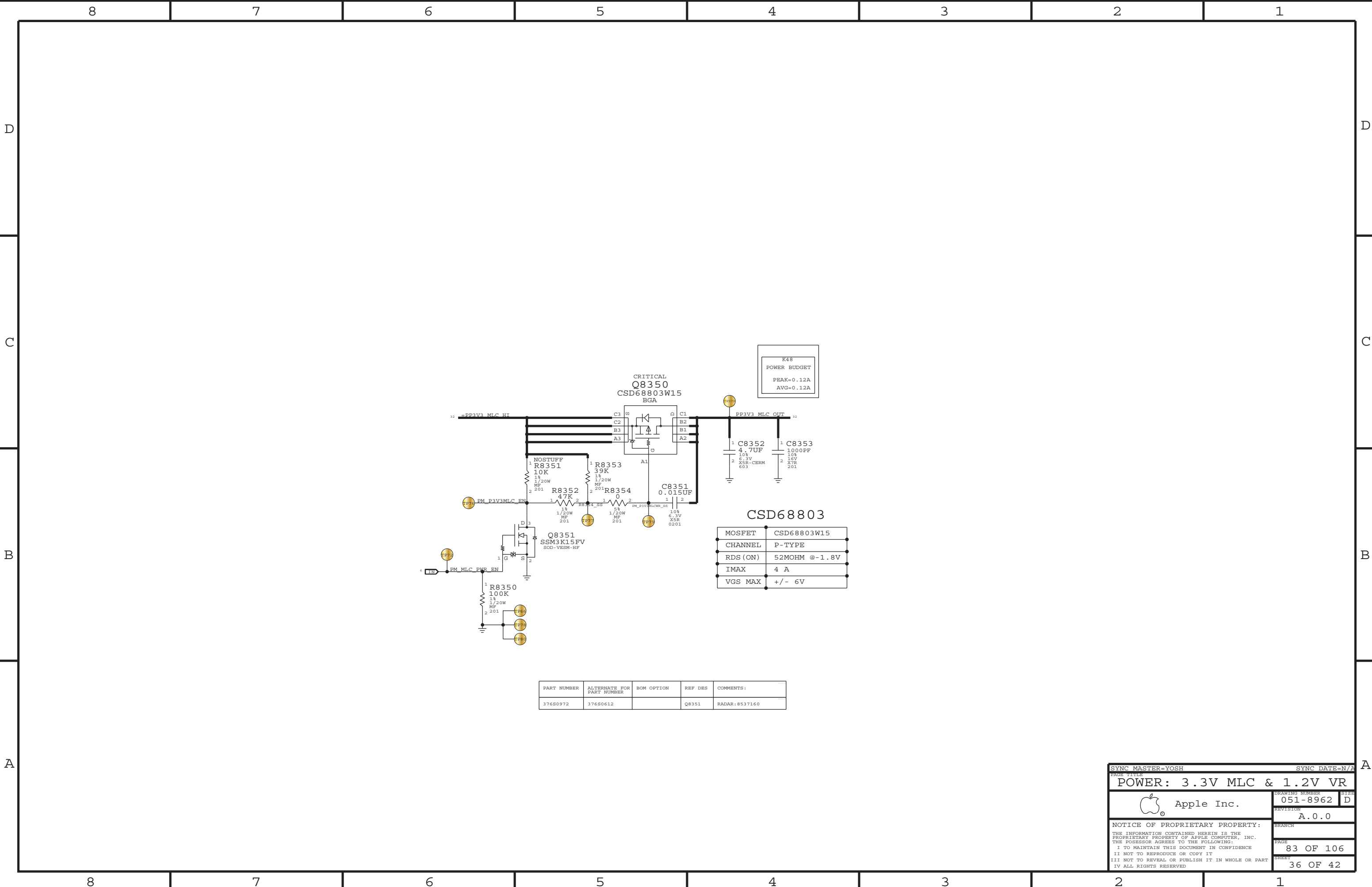


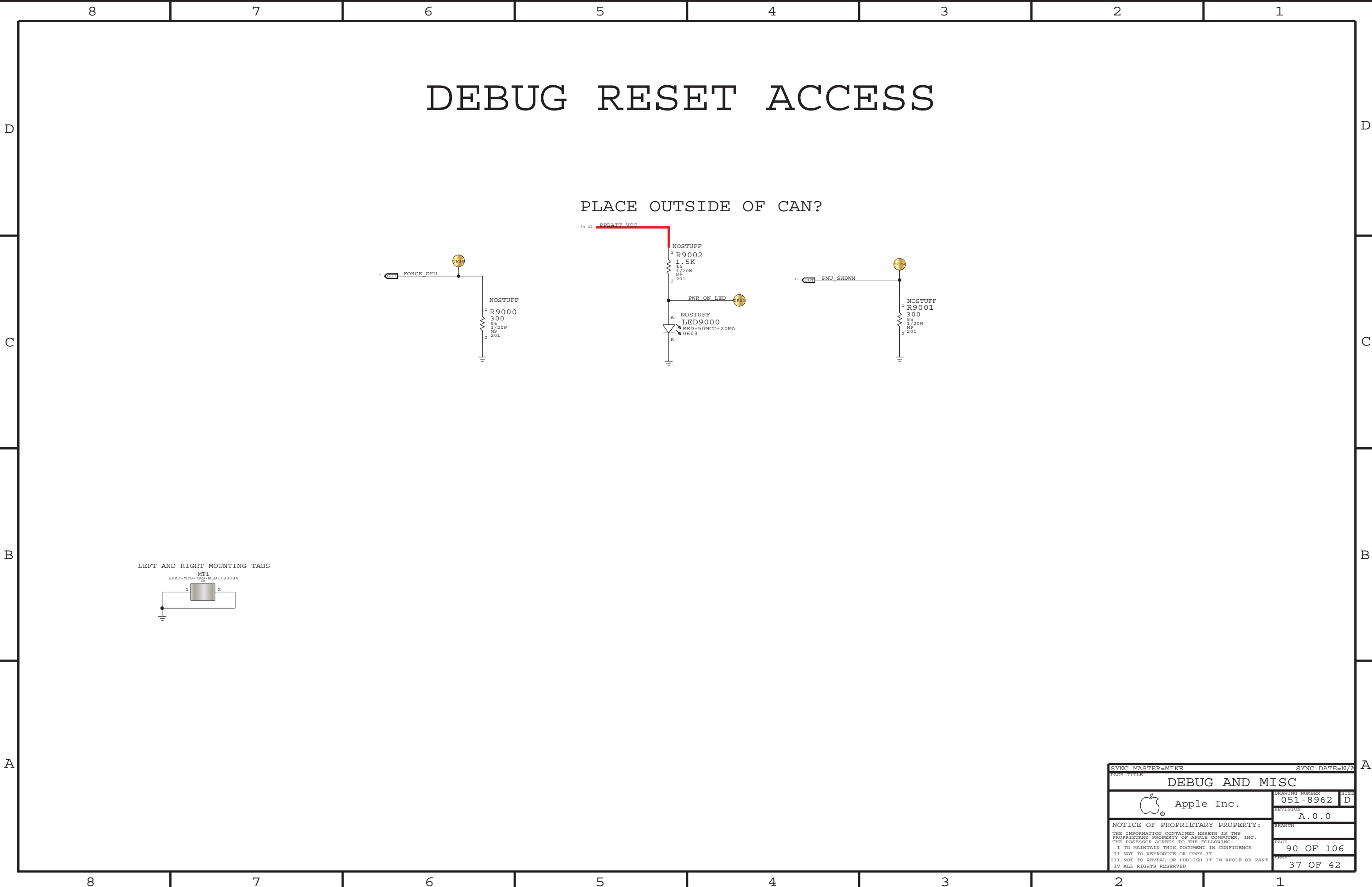
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS :
197S0392	197S0299		Y8138	ALT FOUNDRY



SYNC MASTER-YOSH		SYNC DATE-N/A	
PAGE TITLE			
POWER: PMU			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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		81 OF 106	
		SHEET	
		34 OF 42	









Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000	CLK_50S	CLK	CLK 32K_PMU	10 35
H000	CLK_50S	CLK	CLK 32K_WLAN	30 35
H000	CLK_50S	CLK	CLK 32K_GPS	31 35
H000	CLK_50S	CLK	CLK CAM_FF	7 26
H000	CLK_50S	CLK	CLK CAM_FF_FILT	
H000	CLK_50S	CLK	CLK CAM_FF_CONN	25 26
H000	CLK_50S	CLK	CLK CAM_RF	7 27
H000	CLK_50S	CLK	CLK CAM_RF_FILT	25 27
H000	CLK_50S	CLK	I2S AP_0_MCK	5
H000	CLK_50S	CLK	I2S AP_0_MCK_R	5 19
H000	CLK_50S	CLK	CLK CAM_FF_R	7
H000	CLK_50S	CLK	CLK_CAM_RF_R	7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000	NAND_50S	NAND	F0AD<7...0>	6 12
H000	NAND_50S	NAND	F0CE0_L	6 12
H000	NAND_50S	NAND	F0CE1_L	6 12
H000	NAND_50S	NAND	F0CE2_L	6 12
H000	NAND_50S	NAND	F0CE3_L	6 12
H000	NAND_50S	NAND	F0CE4_L	6 12
H000	NAND_50S	NAND	F0CE5_L	6 12
H000	NAND_50S	NAND	F0CE6_L	6 12
H000	NAND_50S	NAND	F0CE7_L	6 12
H000	NAND_50S	NAND	F0CLE	6 12
H000	NAND_50S	NAND	F0ALE	6 12
H000	NAND_50S	NAND	FORE_L	6 12
H000	NAND_50S	NAND	F0WE_L	6 12
H000	NAND_50S	NAND	F0WP_L	6 12
H000	NAND_50S	NAND	F1AD<7...0>	6 12
H000	NAND_50S	NAND	F1CE0_L	6 12
H000	NAND_50S	NAND	F1CE1_L	6 12
H000	NAND_50S	NAND	F1CE2_L	6 12
H000	NAND_50S	NAND	F1CE3_L	6 12
H000	NAND_50S	NAND	F1CE4_L	6 12
H000	NAND_50S	NAND	F1CE5_L	6 12
H000	NAND_50S	NAND	F1CE6_L	6 12
H000	NAND_50S	NAND	F1CE7_L	6 12
H000	NAND_50S	NAND	F1CLE	6 12
H000	NAND_50S	NAND	F1ALE	6 12
H000	NAND_50S	NAND	F1RE_L	6 12
H000	NAND_50S	NAND	F1WE_L	6 12
H000	NAND_50S	NAND	F1WP_L	
H000	NAND_50S	NAND	F2AD<7...0>	
H000	NAND_50S	NAND	F2CE0_L	
H000	NAND_50S	NAND	F2CE1_L	
H000	NAND_50S	NAND	F2CE2_L	
H000	NAND_50S	NAND	F2CE3_L	
H000	NAND_50S	NAND	F2CLE	
H000	NAND_50S	NAND	F2ALE	
H000	NAND_50S	NAND	F2RE_L	
H000	NAND_50S	NAND	F2WE_L	
H000	NAND_50S	NAND	F2WP_L	
H000	NAND_50S	NAND	F3AD<7...0>	
H000	NAND_50S	NAND	F3CE0_L	
H000	NAND_50S	NAND	F3CE1_L	
H000	NAND_50S	NAND	F3CE2_L	
H000	NAND_50S	NAND	F3CE3_L	
H000	NAND_50S	NAND	F3CLE	
H000	NAND_50S	NAND	F3ALE	
H000	NAND_50S	NAND	F3RE_L	
H000	NAND_50S	NAND	F3WE_L	
H000	NAND_50S	NAND	F3WP_L	

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000		JTAG	JTAG AP_TCK	4 28
H000		JTAG	JTAG AP_TMS	4 28
H000		JTAG	JTAG AP_TDI	4 10
H000		JTAG	JTAG AP_TDO	4 10
H000		JTAG	JTAG AP_TRST_L	4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000	I2C_50S	I2C	I2C1_SDA_1V8	5 25
H000	I2C_50S	I2C	I2C1_SCL_1V8	5 25
H000	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 35
H000	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 35
H000	I2C_50S	I2C	I2C2_SDA_3V0	5 25 26
H000	I2C_50S	I2C	I2C2_SCL_3V0	5 25 26
H000	I2C_50S	I2C	ISP AP_0_SCL	7 25
H000	I2C_50S	I2C	ISP AP_0_SDA	7 25
H000	I2C_50S	I2C	ISP AP_1_SCL	7 26
H000	I2C_50S	I2C	ISP AP_1_SDA	7 26
H000	I2C_50S	I2C	I2C2_SCL_3V0_ALS	25 26
H000	I2C_50S	I2C	I2C2_SDA_3V0_ALS	25 26
H000	I2C_50S	I2C	ISP_CAM_1_SCL	25 26
H000	I2C_50S	I2C	ISP_CAM_1_SDA	25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000		CRYSTAL	XTAL 24M_I	4
H000		CRYSTAL	XTAL 24M_O	4
H000		CRYSTAL	24M_O	4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000		VREF	PPVREF_DDR0_CA	8
H000		VREF	PPVREF_DDR0_DO	8
H000		VREF	PPVREF_DDR1_CA	8
H000		VREF	PPVREF_DDR1_DO	8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000	USB_90D	USB	USB_D_P	4 28
H000	USB_90D	USB	USB_D_N	4 28
H000	USB_90D	USB	USB_PT_DK_CON_D_P	28 29
H000	USB_90D	USB	USB_PT_DK_CON_D_N	28 29
H000	USB_90D	USB	USB_BB_D_P	11 31
H000	USB_90D	USB	USB_BB_D_N	11 31
H000	USB_90D	USB	USB_FS_D_P	4 11
H000	USB_90D	USB	USB_FS_D_N	4 11
H000	USB_90D	USB	USB_FS_N_ACC_TX	11 28
H000	USB_90D	USB	USB_FS_P_ACC_RX	11 28
H000	USB_90D	USB	ACC_PT_DK_CON_TX	28 29
H000	USB_90D	USB	ACC_PT_DK_CON_RX	28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000	I2S_50S	I2S	I2S AP_0_BCLK	5 19
H000	I2S_50S	I2S	I2S AP_0_LRCK	5 19
H000	I2S_50S	I2S	I2S AP_0_DIN	5 19
H000	I2S_50S	I2S	I2S AP_0_DOUT	5 19
H000	I2S_50S	I2S	L63_ASP_SDOUT	19
H000	I2S_50S	I2S	I2S AP_2_BCLK	5 19 30
H000	I2S_50S	I2S	I2S AP_2_LRCK	5 19 30
H000	I2S_50S	I2S	I2S AP_2_DIN	5 19 30
H000	I2S_50S	I2S	I2S AP_2_DOUT	5 19 30
H000	I2S_50S	I2S	L63_VSP_SDOUT	19
H000	I2S_50S	I2S	I2S AP_3_BCLK	5 19
H000	I2S_50S	I2S	I2S AP_3_LRCK	5 19
H000	I2S_50S	I2S	I2S AP_3_DIN	5 19
H000	I2S_50S	I2S	I2S AP_3_DOUT	5 19
H000	I2S_50S	I2S	L63_XSP_SDOUT	19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H000		DWI	DWI AP_CLK	5 35
H000		DWI	DWI AP_DI	5 35
H000		DWI	DWI AP_DO	5 35

SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE		CONSTRAINTS: ASSIGNMENTS	
 Apple Inc.		DRAWING NUMBER	051-8962
		SIZE	D
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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H230	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
H230	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
H230	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
H230	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
H230	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
H230	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
H230	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 10 11 28
H230	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
H230	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
H230	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
H230	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
H230	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H240	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
H240	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
H240	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
H240	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
H240	LVDS_100D	LVDS	LVDS_CLK_P 14 16
H240	LVDS_100D	LVDS	LVDS_CLK_N 14 16
H240	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
H240	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H240	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
H240	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
H240	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
H240	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
H240	DP_100D	DP	DP_AP_AUX_P 7 13
H240	DP_100D	DP	DP_AP_AUX_N 7 13
H240	DP_100D	DP	DP_EMI_TX_P<0> 13 28
H240	DP_100D	DP	DP_EMI_TX_N<0> 13 28
H240	DP_100D	DP	DP_EMI_TX_P<1> 13 28
H240	DP_100D	DP	DP_EMI_TX_N<1> 13 28
H240	DP_100D	DP	DP_EMI_AUX_P 13 28
H240	DP_100D	DP	DP_EMI_AUX_N 13 28
H240	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
H240	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
H240	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
H240	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
H240	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
H240	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H250	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
H250	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
H250	AUDIO	AUDIO	LEFT_CH_P 20
H250	AUDIO	AUDIO	SSM2375_L_IN_P 20
H250	AUDIO	AUDIO	SSM2375_L_IN_N 20
H250	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
H250	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
H250	AUDIO	AUDIO	RIGHT_CH_P 20
H250	AUDIO	AUDIO	SSM2375_R_IN_P 20
H250	AUDIO	AUDIO	SSM2375_R_IN_N 20
H250	AUDIO	AUDIO	EXT_MIC_P 19 23
H250	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H260	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
H260	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R 5 30
H260	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
H260	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H270	SPT_50S	SPT	SPI_GRAPE_MISO 5 31
H270	SPT_50S	SPT	SPI_GRAPE_MOSI 5 31
H270	SPT_50S	SPT	SPI_GRAPE_SCLK 5 31
H270	SPT_50S	SPT	SPI_GRAPE_CS_L 5 31
H270	SPT_50S	SPT	SPI_IPC_MISO 5 31
H270	SPT_50S	SPT	SPI_IPC_MOSI 5 31
H270	SPT_50S	SPT	SPI_IPC_SCLK 5 31
H270	SPT_50S	SPT	SPI_IPC_MRDY 5 31

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
H280	MIPI_100D	MIPT	MIPID_AP_DATA_P<0> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_N<0> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_P<1> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_N<1> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_P<2> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_N<2> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_P<3> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_DATA_N<3> 7 14
H280	MIPI_100D	MIPT	MIPID_AP_CLK_P 7 14
H280	MIPI_100D	MIPT	MIPID_AP_CLK_N 7 14
H280	MIPI_100D	MIPT	MIPIOC_AP_DATA_P<0> 7 27
H280	MIPI_100D	MIPT	MIPIOC_AP_DATA_N<0> 7 27
H280	MIPI_100D	MIPT	MIPIOC_AP_CLK_P 7 27
H280	MIPI_100D	MIPT	MIPIOC_AP_CLK_N 7 27
H280	MIPI_100D	MIPT	MIPIOC_CAM_DATA_P<0> 25 27
H280	MIPI_100D	MIPT	MIPIOC_CAM_DATA_N<0> 25 27
H280	MIPI_100D	MIPT	MIPIOC_CAM_CLK_P 25 27
H280	MIPI_100D	MIPT	MIPIOC_CAM_CLK_N 25 27
H280	MIPI_100D	MIPT	MIPI1C_AP_DATA_P<0> 7 26
H280	MIPI_100D	MIPT	MIPI1C_AP_DATA_N<0> 7 26
H280	MIPI_100D	MIPT	MIPI1C_AP_CLK_P 7 26
H280	MIPI_100D	MIPT	MIPI1C_AP_CLK_N 7 26
H280	MIPI_100D	MIPT	MIPI1C_CAM_DATA_P<0> 25 26
H280	MIPI_100D	MIPT	MIPI1C_CAM_DATA_N<0> 25 26
H280	MIPI_100D	MIPT	MIPI1C_CAM_CLK_P 25 26
H280	MIPI_100D	MIPT	MIPI1C_CAM_CLK_N 25 26

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL8, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL8, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES :


- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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