Compal Confidential

Kabylake-U M/B Schematics Document

Intel ULV Processor with DDR4 SODIMMx2

Date : 2016/05/11

Version : 0.2 (PV phase)

Project : *Diner_Crepe1.1(15")*
BDL50 : LA-D707P

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Title: Cover Page			
Size: Custom	Document Number: LA-D707P		Rev: 0.2
Date: Wednesday, May 11, 2016	Sheet 1	of 60	

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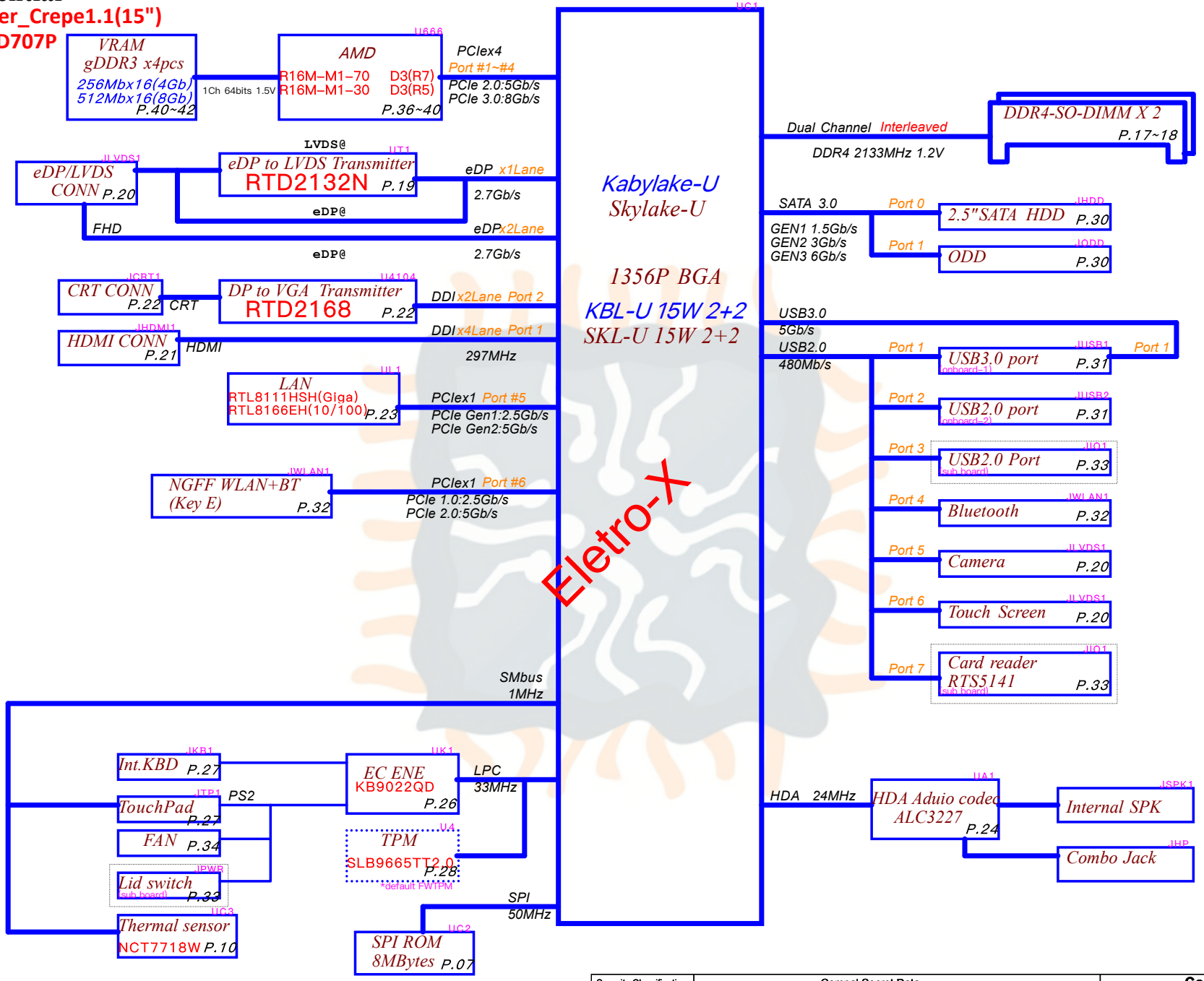
Model Name : Diner_Crepe1.1(15")

File Name : LA-D707P



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Title: Block Diagrams

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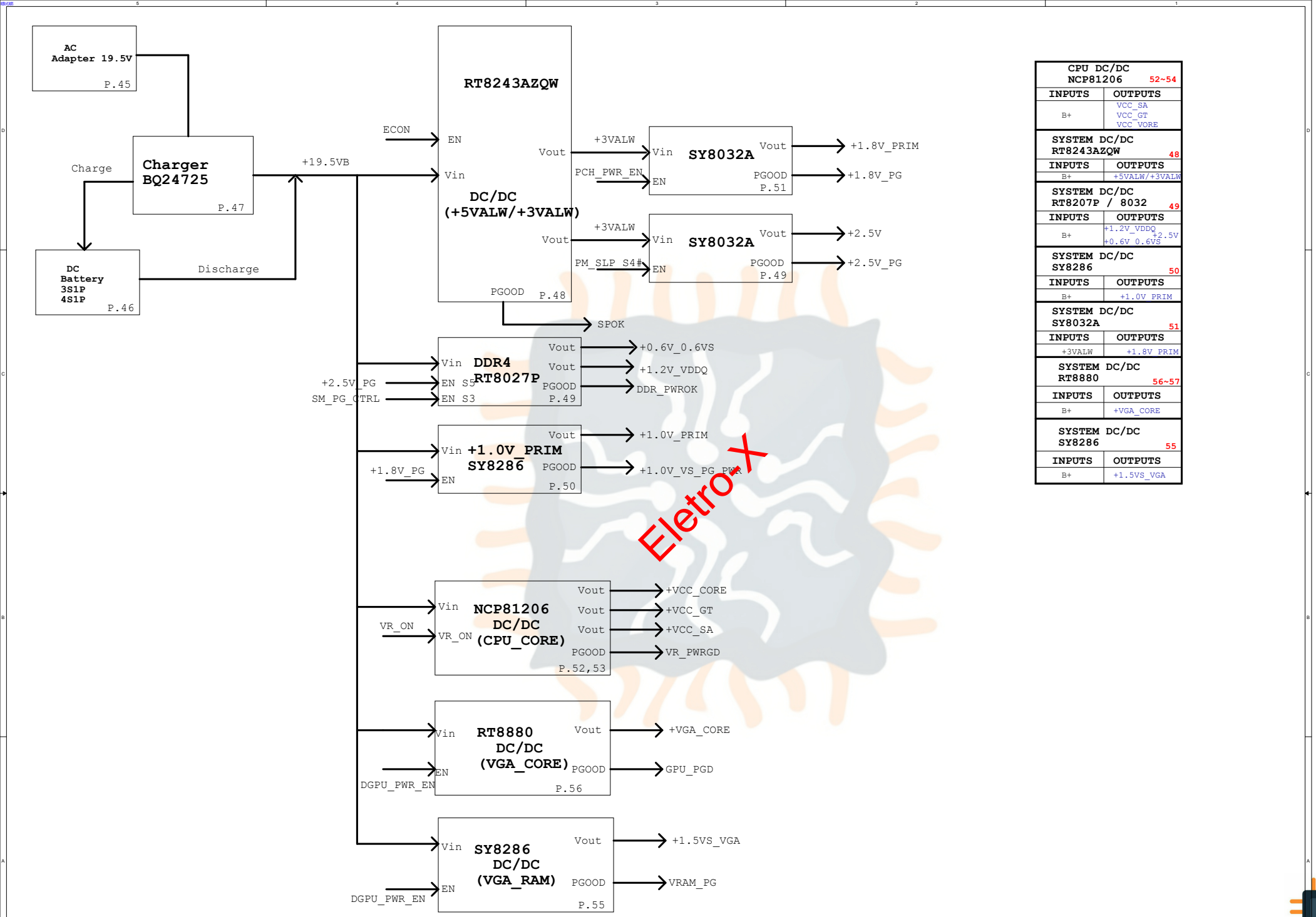


CPU DC/DC NCP81206 52~54	
INPUTS	OUTPUTS
B+	VCC_SA VCC_GT VCC_VORE

SYSTEM DC/DC RT8243AZQW 48	
INPUTS	OUTPUTS
B+	+5VALW/+3VALW

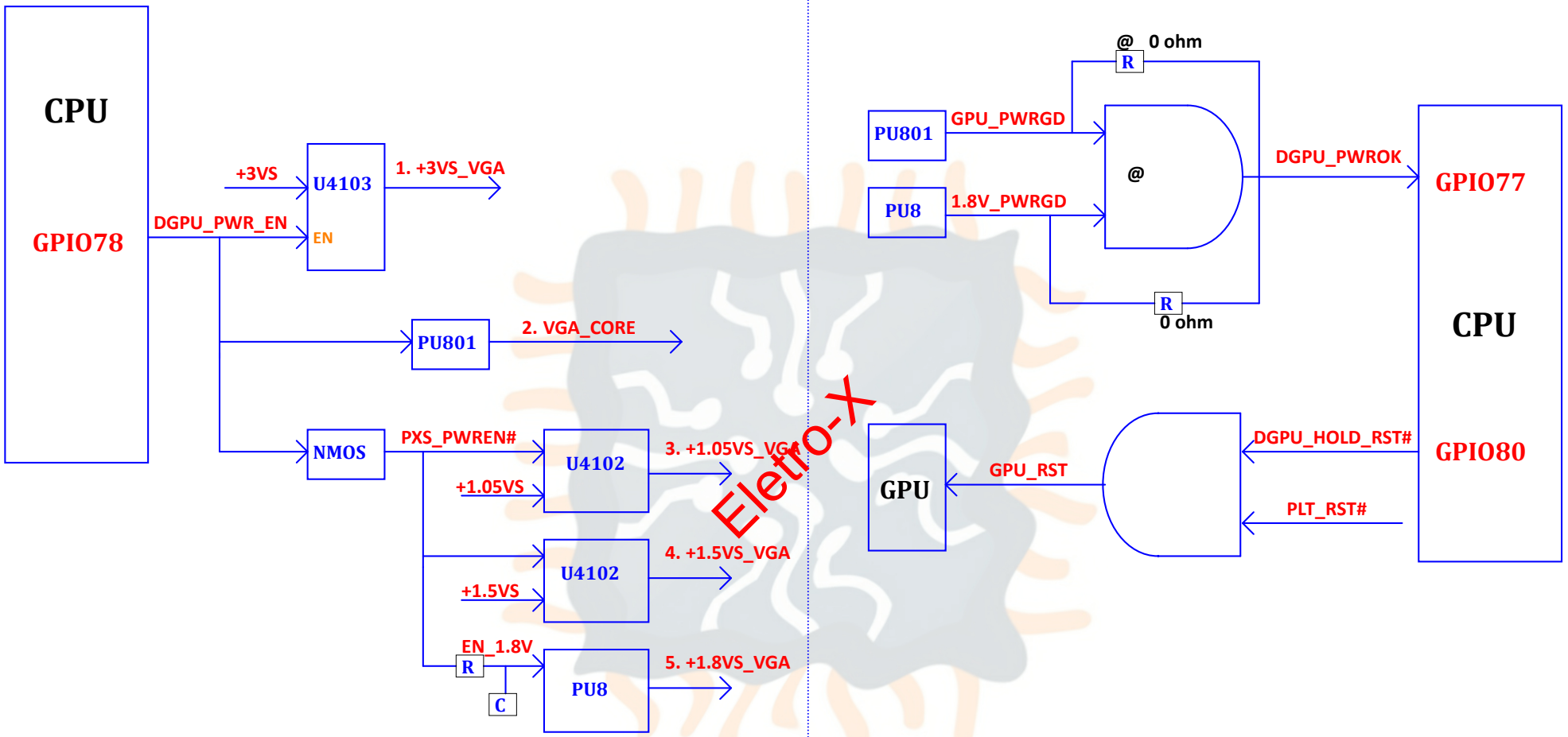
SYSTEM DC/DC RT8207P / 8032 49	
INPUTS	OUTPUTS
B+	+1.2V_VDDQ +2.5V +0.6V_0.6VS

SYSTEM DC/DC SY8286 50	
INPUTS	OUTPUTS
B+	+1.0V_PRIM

SYSTEM DC/DC SY8032A 51	
INPUTS	OUTPUTS
+3VALW	+1.8V_PRIM

SYSTEM DC/DC RT8880 56~57	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8286 55	
INPUTS	OUTPUTS
B+	+1.5VS_VGA



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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Funct i on	Stuf f	Un-Stuf f
DGPU SKU	PX@	
UMA SKU	UMA@	
SPI_IO3(MOW36)	ES@	
Crystal (DIS)	XTALPX@	
Crystal	XTAL@	
Green CLK(UMA)	GCLK@	
Green CLK(DIS)	GCLKPX@	
TPM	TPM@	

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA2
		Touch PAD	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS	ME FW	0x48/0x49	TBC	0x90/0x92
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		DGPU	TBC	TBC	TBC
		PCH	TBC	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C
		PCH	TBC

Power State

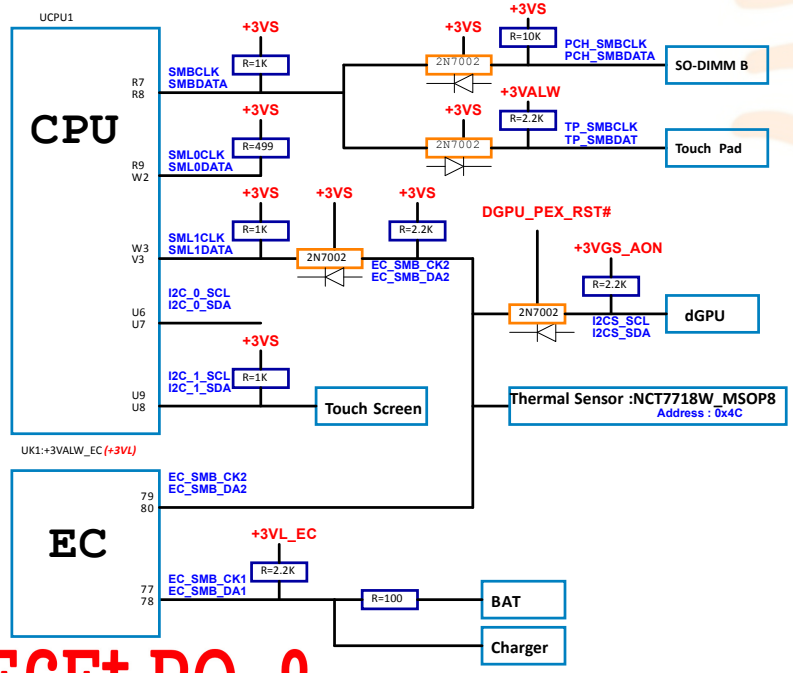
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

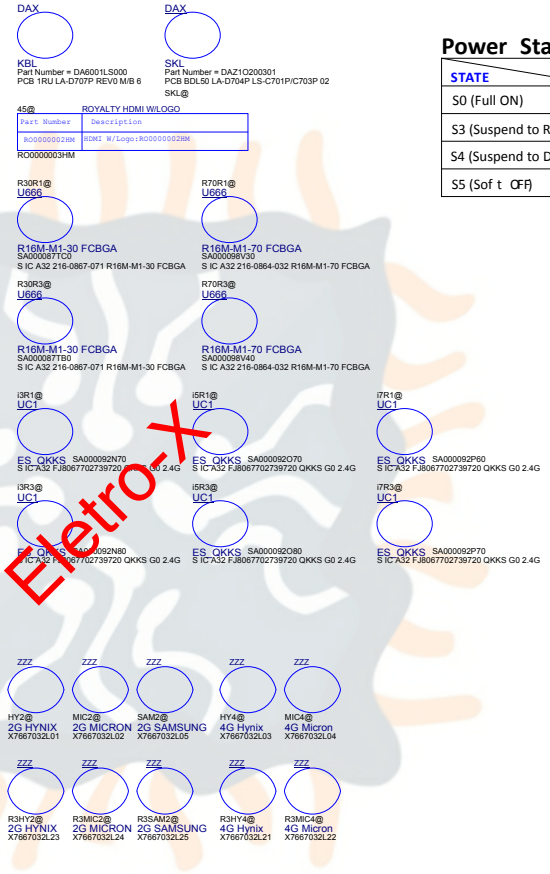
<USB2.0 port>

USB2.0 port	DESTINATION UMA	DESTINATION Dis
1	USB 2.0/3.0	USB 2.0/3.0
2	USB 2.0/3.0	USB 2.0/3.0
3	USB 2.0 OFF BOARD	USB 2.0 OFF BOARD
4	WLAN	WLAN
5	Camera	Camera
6	TOUCH SCREEN	TOUCH SCREEN
7	CR	CR
8		
9		
10		

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION UMA	DESTINATION Dis	CLK
1			1	USB3.0	USB3.0	X
2			2	USB3.0	USB3.0	X
3			3	USB3.0(Charger)	USB3.0(Charger)	X
4			4	USB3.0(IO Board)	USB3.0(IO Board)	X
5	1		5	X	GPU(DIS only)	CLK0
6	2		6	X	GPU(DIS only)	
7	3			X	GPU(DIS only)	
8	4			X	GPU(DIS only)	
9	5			LAN	LAN	CLK1
10	6			WLAN	WLAN	CLK2
11	7	0		2.5"HDD	2.5"HDD	X
12	8	1		ODD	ODD	X
13	9			Card reader(PCI-E)	Card reader(PCI-E)	CLK3
14	10			X	X	X
15	11	1*		X	X	X
16	12	2				X





Load BOM Opt i on Tab l e

BOM Number	Load BOM Opt i on
4519YN32L01(UMA)	
4519YN32L02(DIS)	

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Title: Notes List

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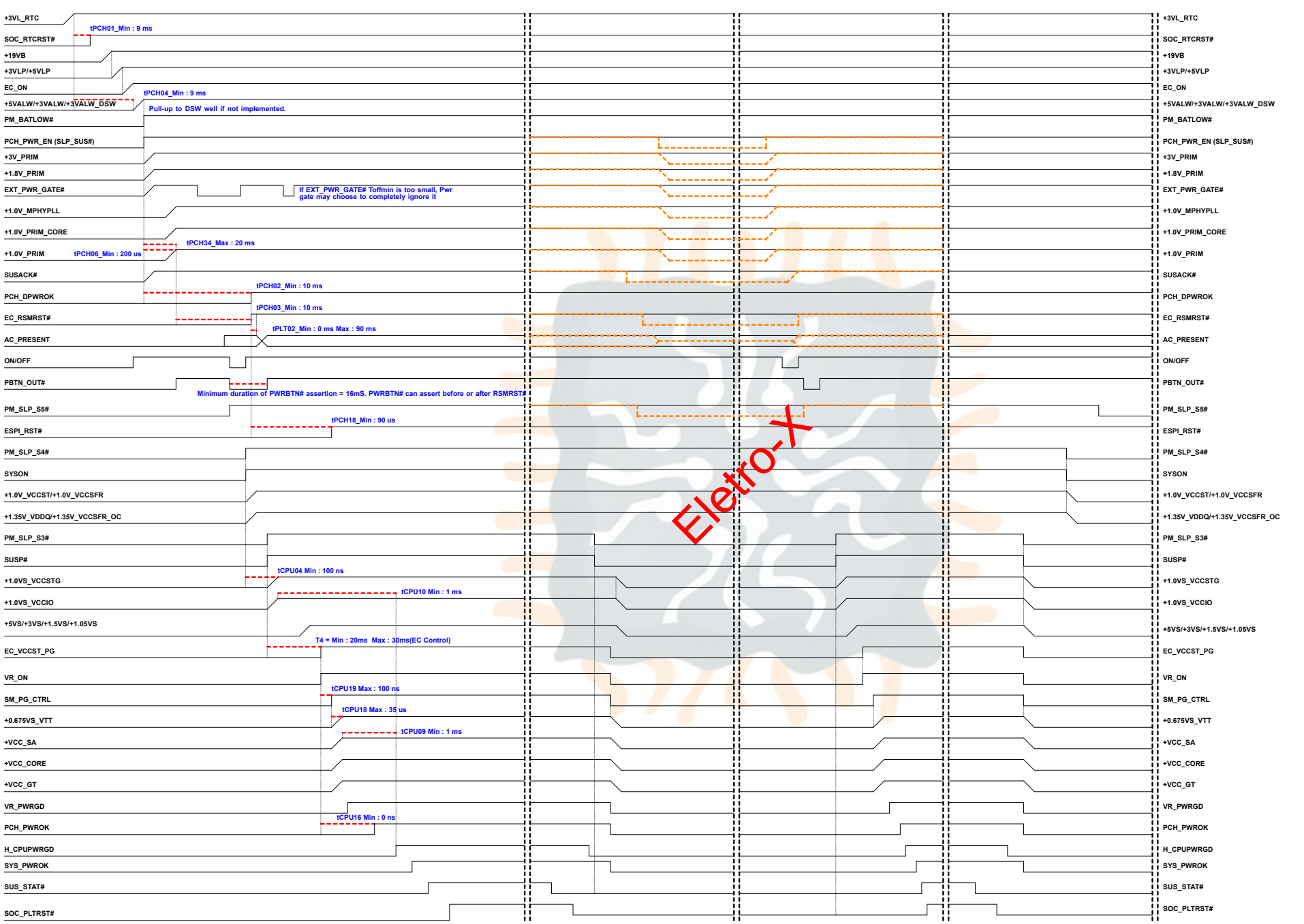
[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



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Issued Date		Deciphered Date	Title: HW Reserve

Size: Custom	Document Number: LA-D707P		Rev: v0.2
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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

<HDMI>

<eDP to CRT>

HDMI DDC (Port B)

<DB> DP port C enable

<eDP>

<DB> Check

UC1A SKL-U Rev_0.53

SKL-U_BGA1356

1 OF 20

COMPENSATION PU FOR eDP

CAD note:
Trace width=20 mils,Spacing=25mil,Max length=100mils

UC1D SKL-U Rev_0.53

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SKL-U_BGA1356

XDP CONN

SD000008H80

SD000008H80

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom | Document Number: LA-D707P | Rev: 1.0

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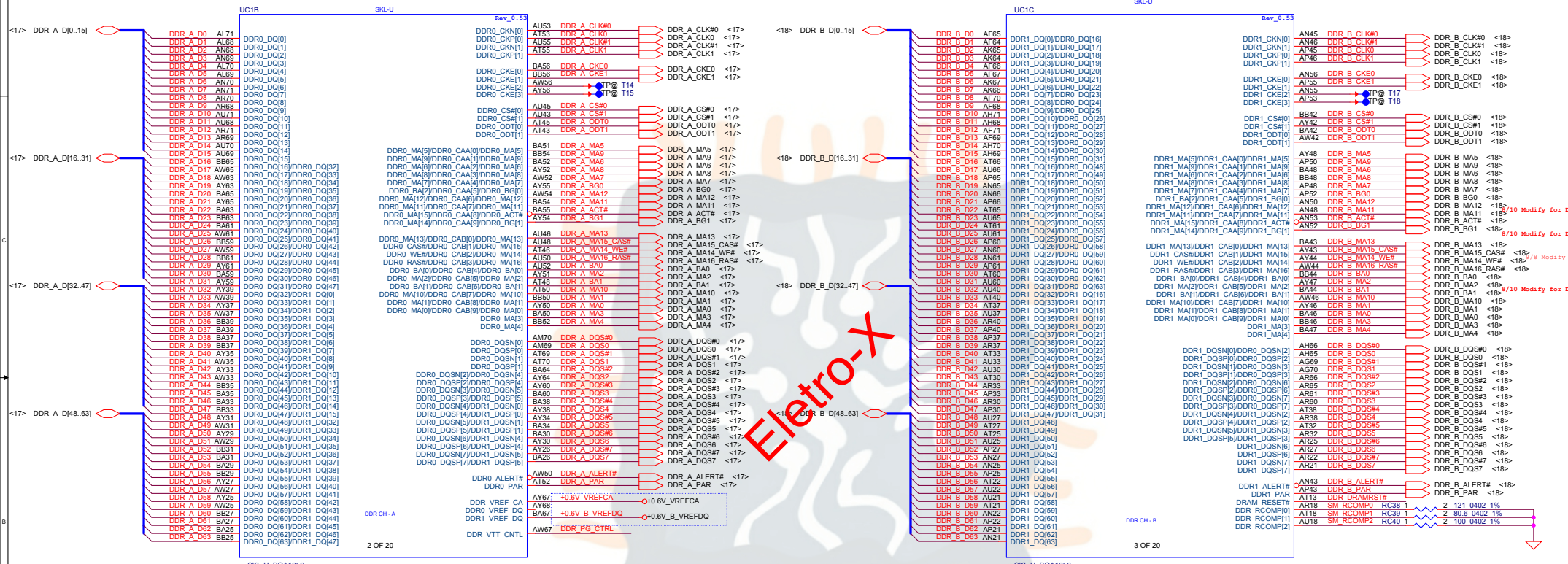
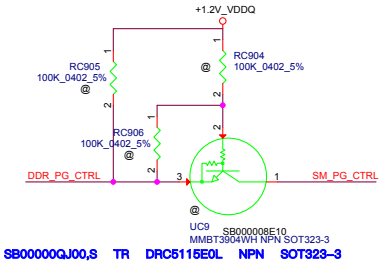
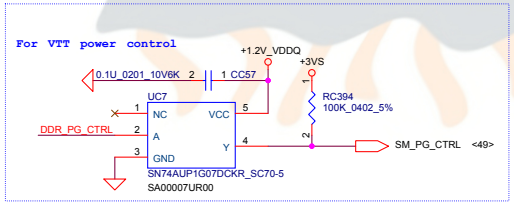
Interleaved Memory

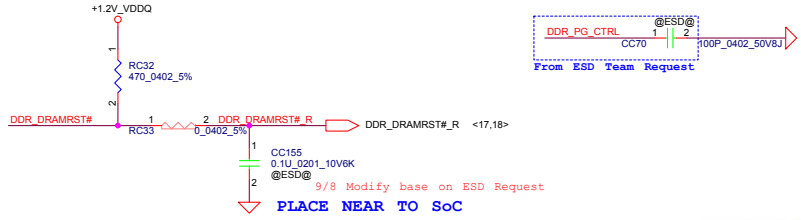
Interleaved Memory

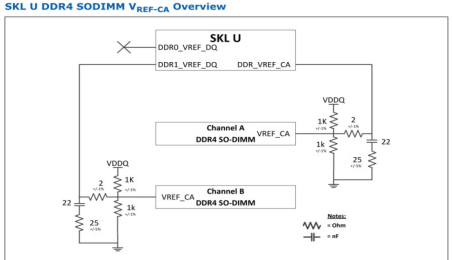
<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)











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Title: SKL-U(2/12)DDRIII			
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ECEtRO-L

SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E
SKL-U
SPI - FLASH
SPI - TOUCH
C LINK
SMBUS, SMLINK
LPC
SKL-U_BGA1356
5 OF 20

PCH_SPI_CLK AV2 SPI0_CLK
PCH_SPI_SO AW3 SPI0_MISO
PCH_SPI_SI AV3 SPI0_MOSI
PCH_SPI_SIO2 AW2 SPI0_IO2
PCH_SPI_SIO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 SMBALERT# TP@ T239
GPP_C3/SML0CLK R9 SML0CLK
GPP_C4/SML0DATA W2 SML0DATA
GPP_C5/SML0ALERT# W1 SML0ALERT#
GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 1 RC902 @ 0_0201_5% 2 SML1ALERT#
TP@ T234

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 LPC_AD0 <26,28>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 LPC_AD1 <26,28>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 LPC_AD2 <26,28>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 LPC_AD3 <26,28>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# LPC_FRAME# <26,28>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT# TP@ T242

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI0 RC387 1 2 22_0402_5% CLK_PCI_LPC <26>
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI1 RC53 1 TPM@2 22_0402_5% CLK_PCI_TPM <28> To EC
GPP_A8/CLKRUN# AW11 PM_CLKRUN# PM_CLKRUN# <26>

12/11_Delete TP

<26> EC_KBRST# EC_KBRST# AW13 GPP_A0/RCIN#
To TPM <26,28> SERIRQ SERIRQ AY11 GPP_A6/SERIRQ
LPC Mode

<SI>un-mount RC53
11/28 CPU side delete EC_PCIE_WAKE#

SMB
(Link to XDP, DDR, TP)
SML1
(Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1% +3V_PRIM
SML1ALERT# RC903 @ 150K_0402_1%
SML0ALERT# RC3602 @ 10K_0402_5%
SMBALERT# EC_KBRST# RPC19 10K_0804_8P4R_5%
+3VS

11/28_Follow Intel check list, add PU res

To SPI ROM U/C2 Source From

RPH11
PCH_SPI_CS0#_R 1 8 EC_SPI_CS0# EC_SPI_CS0# <26>
PCH_SPI_CS0#_R 2 7 PCH_SPI_CS0#
PCH_SPI_SO_R 3 6 EC_SPI_SO EC_SPI_SO <26>
PCH_SPI_SO_R 4 5 PCH_SPI_SO
15_0804_8P4R_5%

RPH12
PCH_SPI_HOLD# 1 8 PCH_SPI_SIO3
PCH_SPI_SI_R 2 7 PCH_SPI_SI
PCH_SPI_SI_R 3 6 EC_SPI_SI EC_SPI_SI <26>
4 5
15_0804_8P4R_5%
PCH_SPI_WP# 2 RC388 15_0402_5% 1 PCH_SPI_SIO2

SPI ROM (8MByte Only)
UC2 +3V_SPI CC8 0.1U_0402_16V7K
PCH_SPI_CS0#_R 1 /CS VCC 8 PCH_SPI_HOLD#
PCH_SPI_SO_R 2 DO(IO1) /HOLD(IO3) 7 PCH_SPI_CLK_R
PCH_SPI_WP# 3 /WP(IO2) CLK 6 PCH_SPI_SI_R
4 GND DI(IO0) 5
W25Q64FVSSIQ_SO8 SA000039A30
PCB Footprint = ACES_91960-0084L_8P-T
Use socket footprint

SPI_ROM:
Main:SA000039A30, S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
2nd :SA00007LA10, S IC FL 64M GD25B64CSIGR SOP 8P SPI ROM
2nd :SA000039300, S IC FL 64M N25Q064A13ESEDFF SOP 8P SPI

RC368 15_0402_5% PCH_SPI_CLK 2 1 PCH_SPI_CLK_R PCH_SPI_CLK_R <26>
EMI@
CC9 10P_0402_50V8J @EMI@

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M M25Q064A13ESECOF SO8W 8P

ENE Fixed Code Block Diagram
CPU
EC
SPI_ROM
M:Master
S : Slave
O : Output
I : Input

+3VS +3VS
RC216 10K_0402_5% RC215 10K_0402_5%
QC1A QC1B
SMBCLK PCH_SMBCLK <17,18,19,22>
SMBDATA PCH_SMBDATA <17,18,19,22>
2N7002DWH_SOT363-6 SB00000I700

+3VS
<Cocoa_1020>
add level shift
2N7002DWH_SOT363-6
SML1CLK QC2A EC_SMB_CK2 <10,19,22,26,37>
SML1DATA QC2B EC_SMB_DA2 <10,19,22,26,37>
SB00000I700

<DB> PWR Rail
+3V_PRIM +3VALW
RC81 10K_0402_5% RC82 10K_0402_5%
SB00000I700
SMBCLK QC7A TP_SMBCLK <27>
SMBDATA QC7B TP_SMBDATA <27>
2N7002DWH_SOT363-6 SB00000I700

11/28_Change PWR rail from +3VS to +3V_PRIM
+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBDATA 3 6
SMBCLK 4 5
1K_0804_8P4R_5%

+3V_SPI
PCH_SPI_SIO2 RC3901 @ 2 1K_0402_1%
PCH_SPI_SIO3 RC3911 @ 2 1K_0402_1%
PCH_SPI_CS0#_R 1 @ 2 RC357 1K_0402_5%

PCH_SPI_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

+3VS_PGPPA
PM_CLKRUN# 1 RC107 2 8.2K_0402_5%
SERIRQ 1 RC122 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

Eletro-X

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Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
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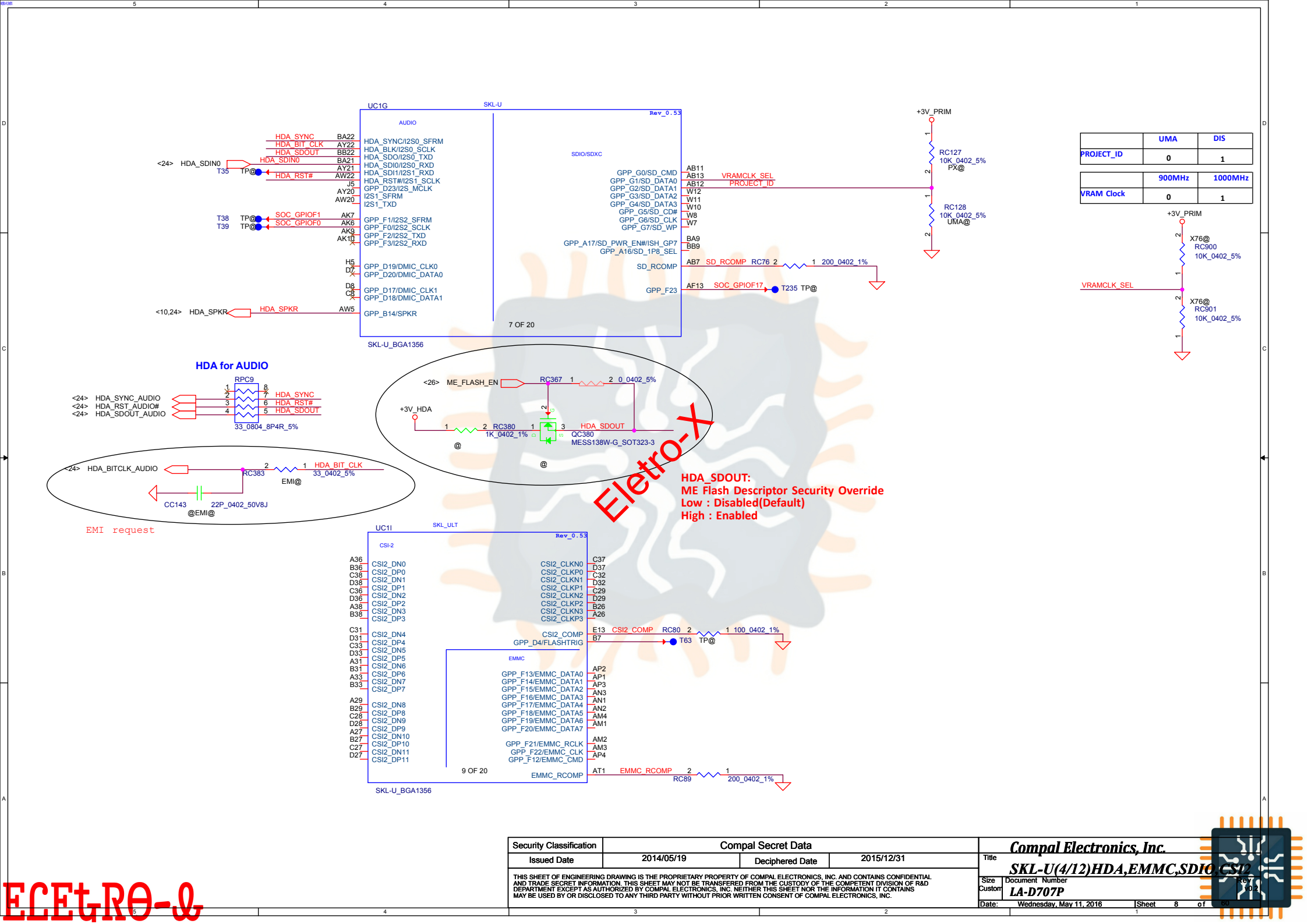
ECEtRO-L



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-D707P | Rev: 1.0

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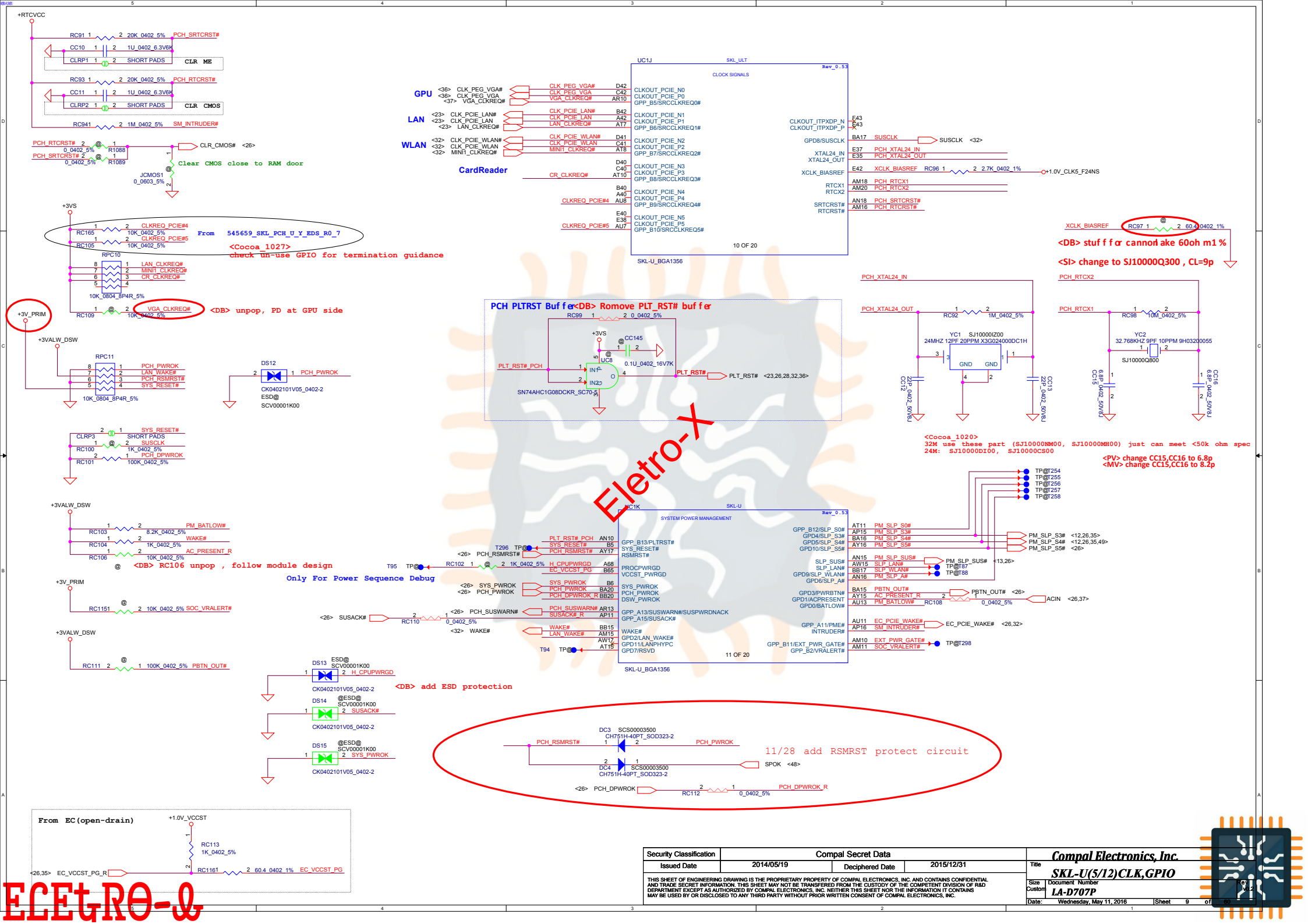

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Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,GPIO		
Size	Document Number		Rev
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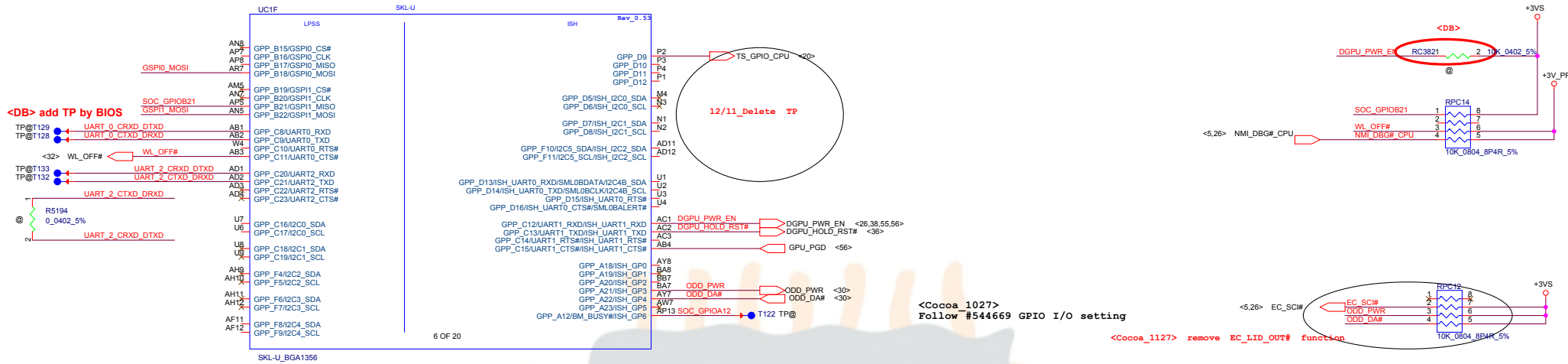


Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

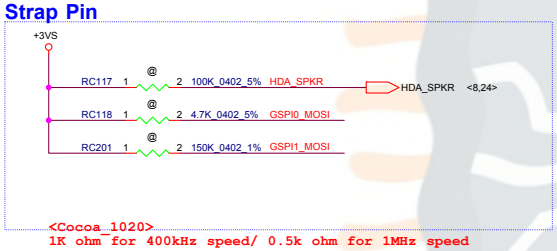
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

1 = LPC Mode

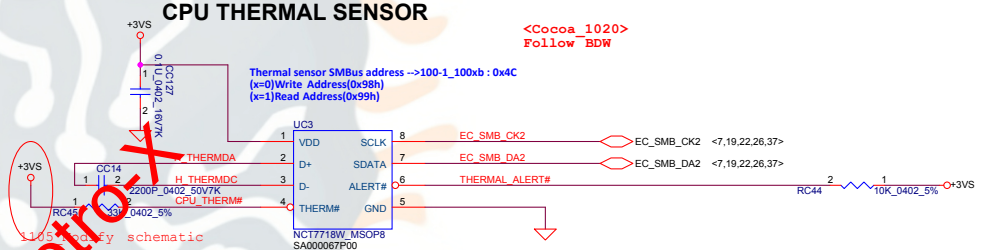
Strap Pin



<Cocoa_1020>
1K ohm for 400kHz speed/ 0.5k ohm for 1MHz speed

CPU THERMAL SENSOR

<Cocoa_1020>
Follow BDW



<DB>
Delete Win7 debug port

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Title	Compal Electronics, Inc.		
	SKL-U(6/12)GPIO		
Size	Document Number		Rev
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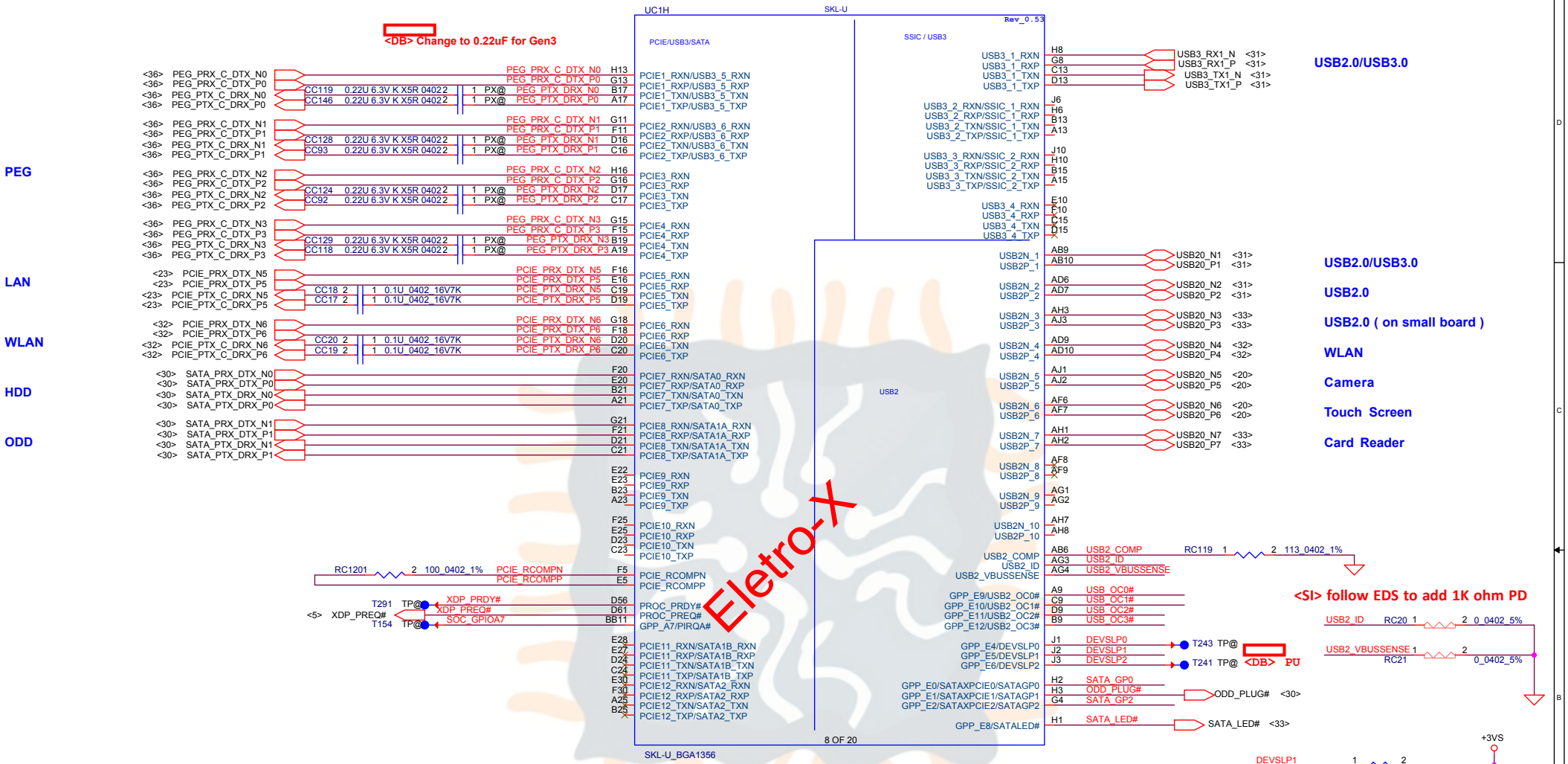
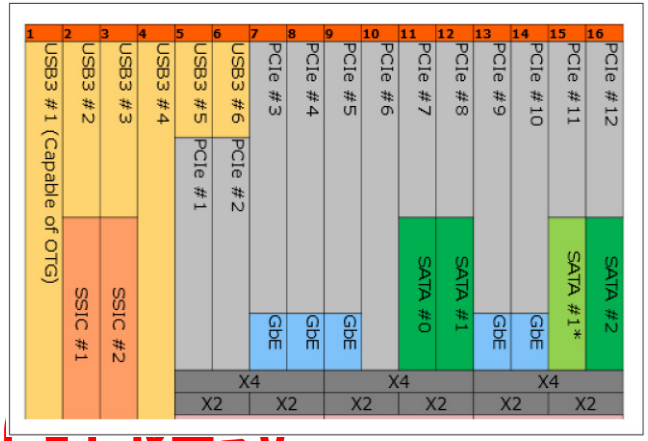


High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NGFF SSD KEY B
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	ODD_PLUG#

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(7/12)PCIE,USB,SATA		
Size	Document Number	Rev	
Custom	LA-D707P	0.3	
Date:	Wednesday, May 11, 2016	Sheet	11 of 60

+1.0V_PRIM TO +1.0V_VCCSTU

1211_Delete jump RC147

1210_Delete jump RC146

I (Max) : 0.04 A(+1.0V_VCCSTU)
RON(Max) : 25 mohm
V drop : 0.001 V

I (Max) : 0.536 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.013 V

<DB> Delete RC145

<Cocoa_1113>
Per 543977_SKL_PDDG_Rev0_91, change CC95 value from 1000pf to 10pf for meet <= 65us timing for +1.0V_VCCSTU power rail.

UC1N SKL-U CPU POWER 3 OF 4 Rev_0.53
SKL-U_BGA1356
14 OF 20

<DB> change +1.35V_VDDQ

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

I (Max) : 3 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V

Imax : 2.77 A

Imax : 3 A

<PV> change short pad

next pin A22

Elero-X

TPS22961DNYR_WSON8

Part Number = SA00007XR00

For Verify S0IX <Cocoa_1027>
connect to EC, check /w EC

RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev1.0

<DB> change +1.35V_VDDQ

RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev0_53

CC47 Follow 543016_SKL_U_Y_PDG_0_9

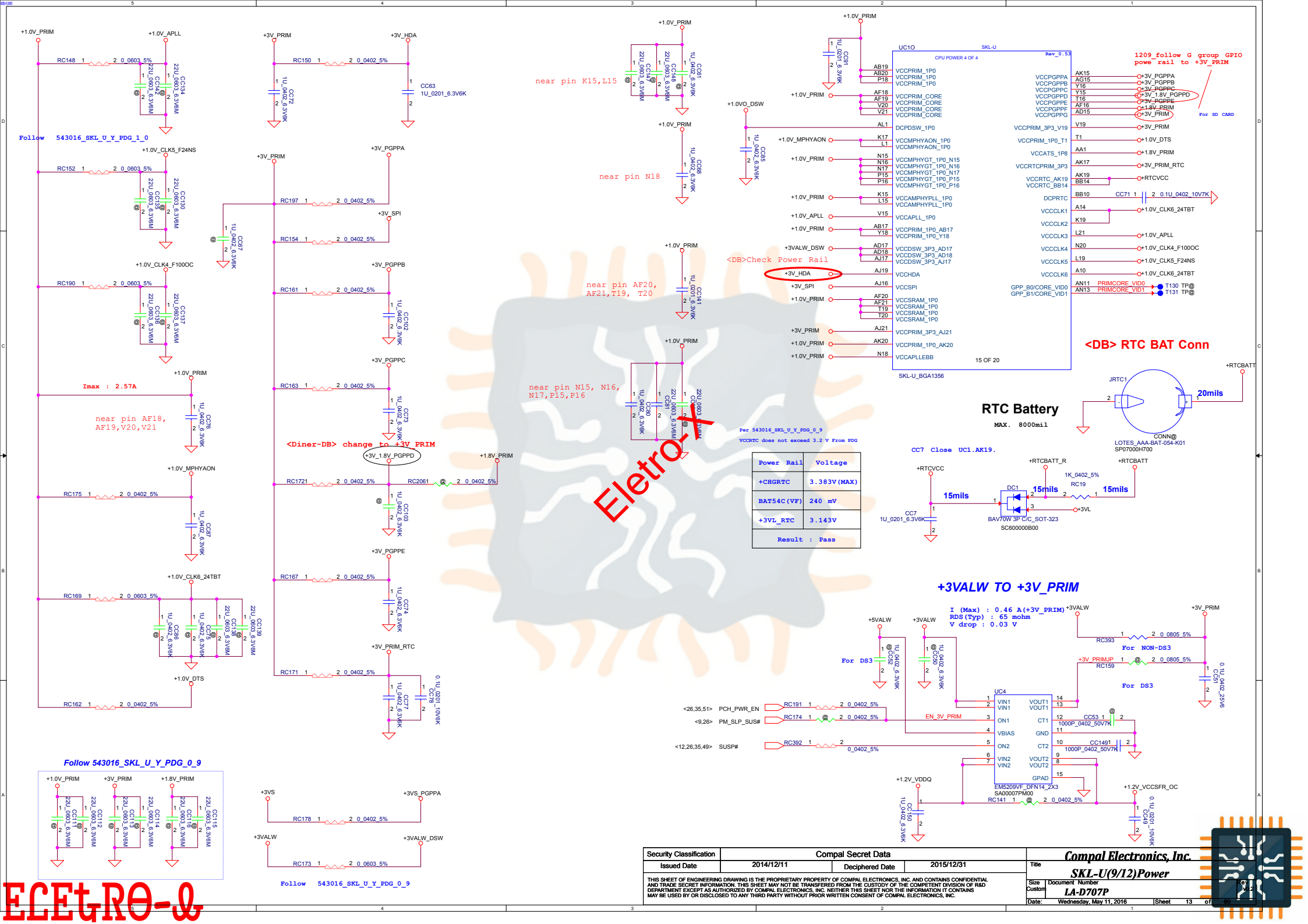
<DB> change +1.35V_VDDQ

+1.35V_VDDQ_CPU : 10UF/6.3V/0603 *6
1UF/6.3V/0402 * 4

Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

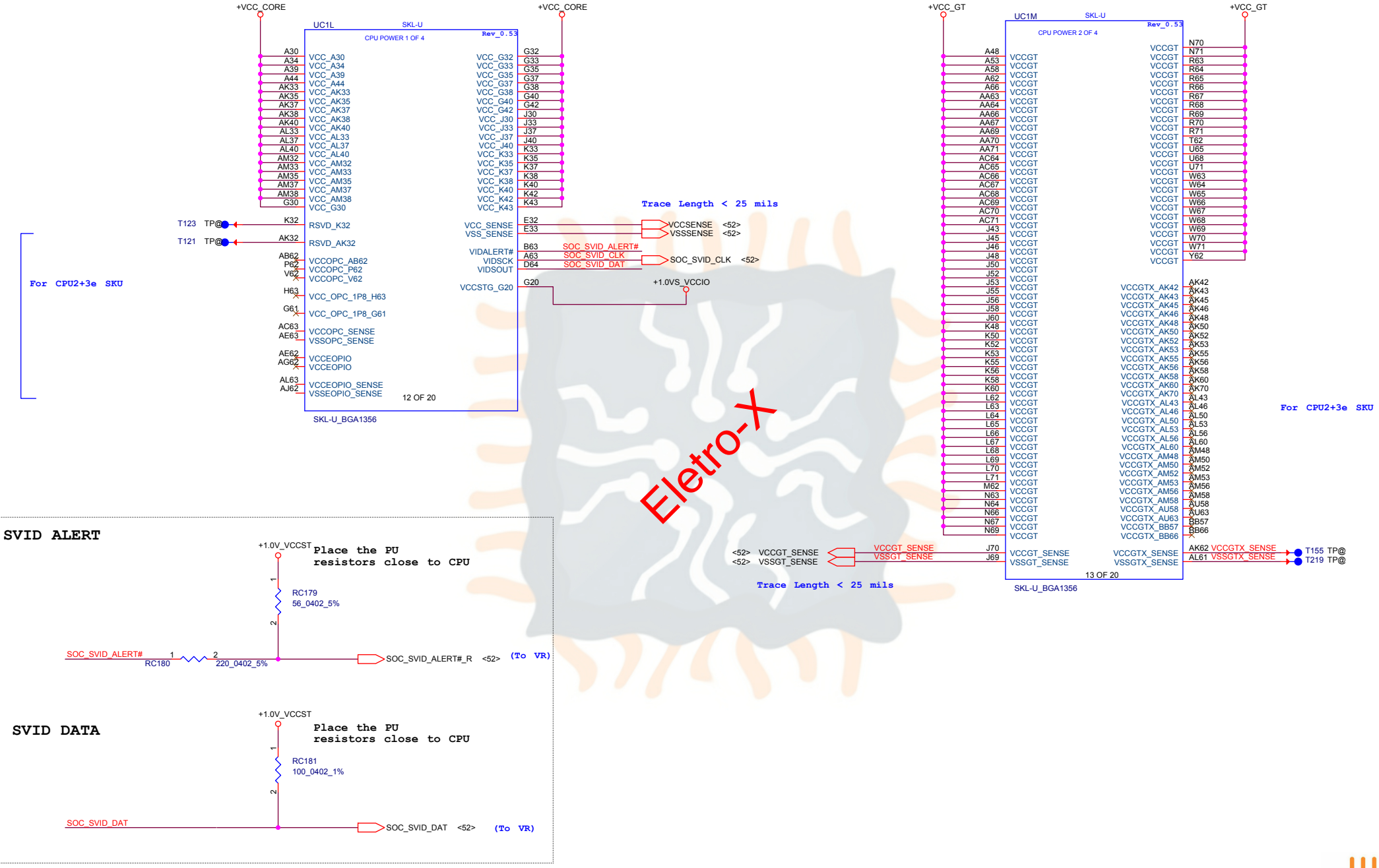
Compal Electronics, Inc.			
Title: SKL-U(8/12)Power			
Size: Custom	Document Number: LA-D707P		Rev: 1.0
Date: Wednesday, May 11, 2016	Sheet 12 of 60		

ECE-R0-L



Security Classification	Compal Secret Data		
Issued Date	2014/12/11	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(9/12)Power		
Size	Document Number	Rev	
Custom	LA-D707P	1.2	
Date:	Wednesday, May 11, 2016	Sheet	13 of 60



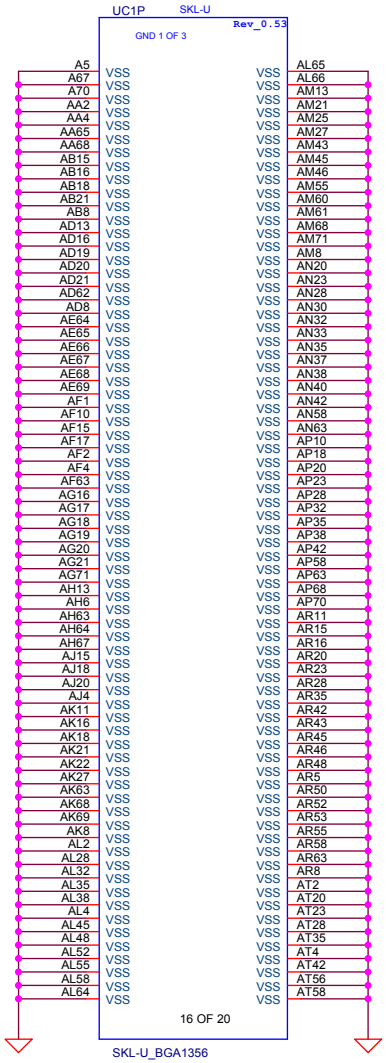
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

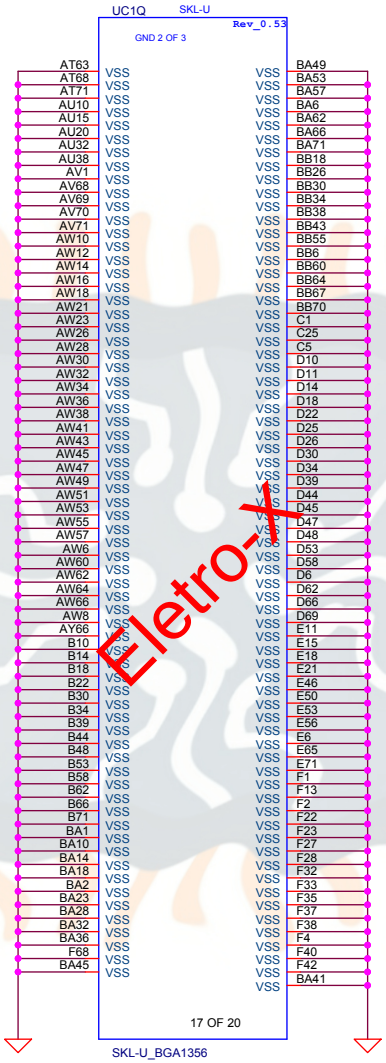
Compal Electronics, Inc.

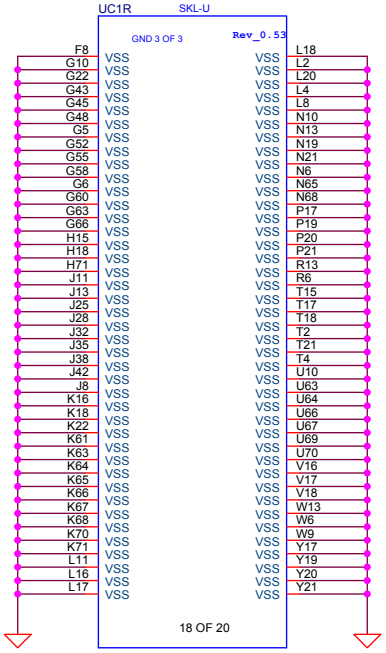
Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 14 of 60







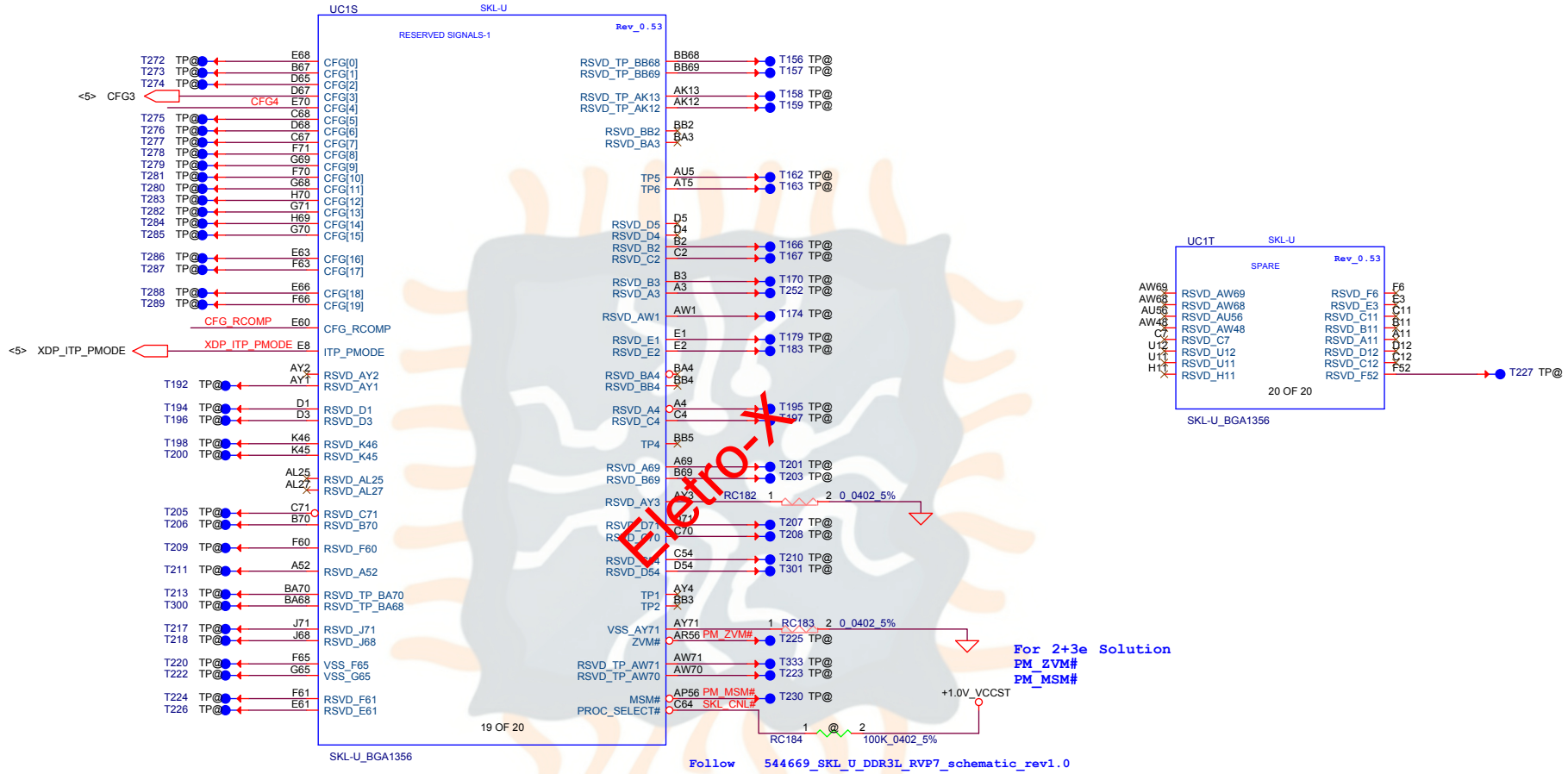
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(11/12)GND

Size	Document Number	Rev
Custom	LA-D707P	1.0

Date: Wednesday, May 11, 2016 Sheet 15 of 60



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.			
Title: SKL-U(12/12)RSVD			
Size: Custom	Document Number: LA-D707P		Rev: 1.0
Date: Wednesday, May 11, 2016	Sheet 16 of 60		

CHANNEL-A

REVERSE TYPE (5.2 mm)

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
PLACE THE CAP near JDIMM1. 164

Layout Note:
Place near JDIMM1

PLACE NEAR TO PIN

PLACE NEAR TO SODIMM

8/26

9/8 Modify

9/8 Modify base on ESD Request

For ECC DIMM

Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Eletro-X

ECEtRO-X

Security Classification	Compal Secret Data		
Issued Date	2015/08/03	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

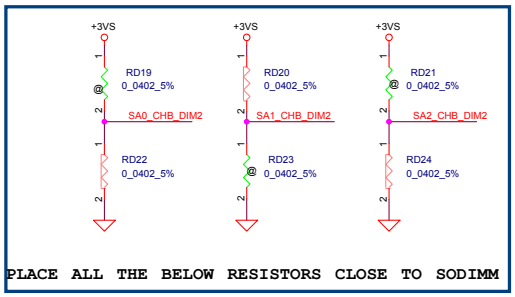
Title: P18-DDRIV_CHA: DIMM0

Size: | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 17 of 60

CHANNEL-B

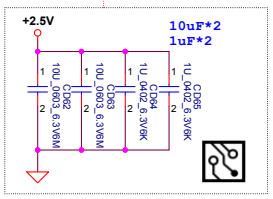
TOP: JDIMM2 CONN Non-ECC DIMM



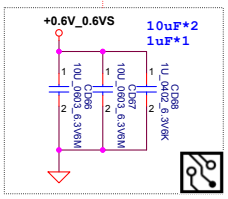
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

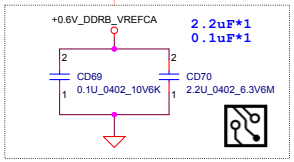
Layout Note:
Place near JDIMM2.257,259

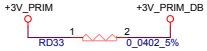


Layout Note:
Place near JDIMM2.258

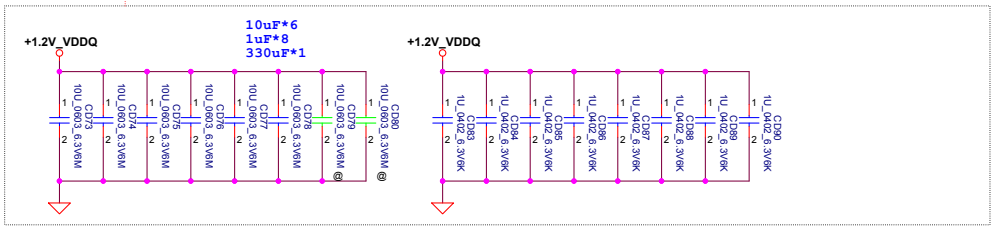


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2



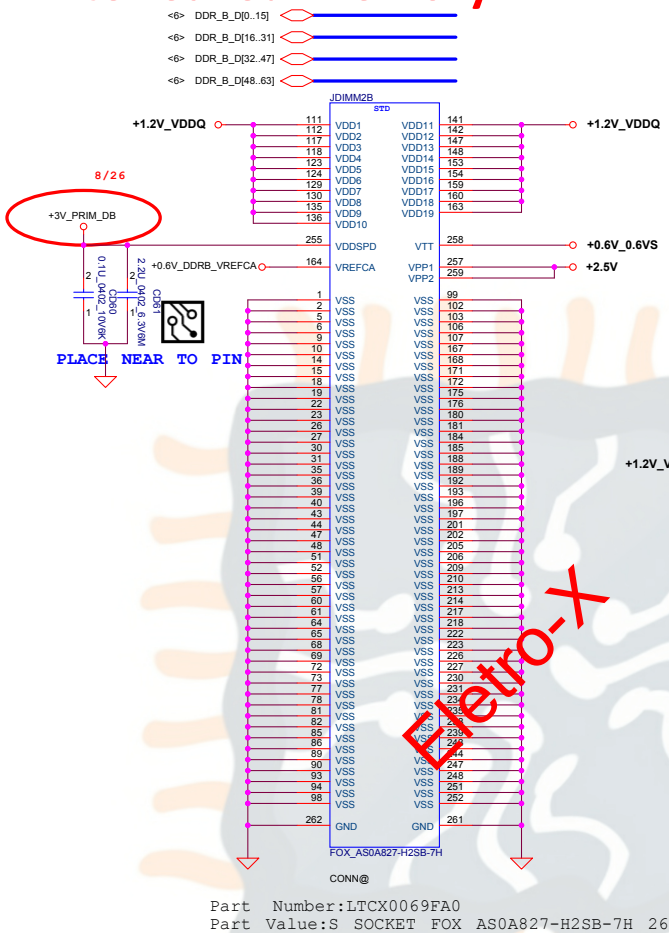


Layout Note:
Place near JDIMM2

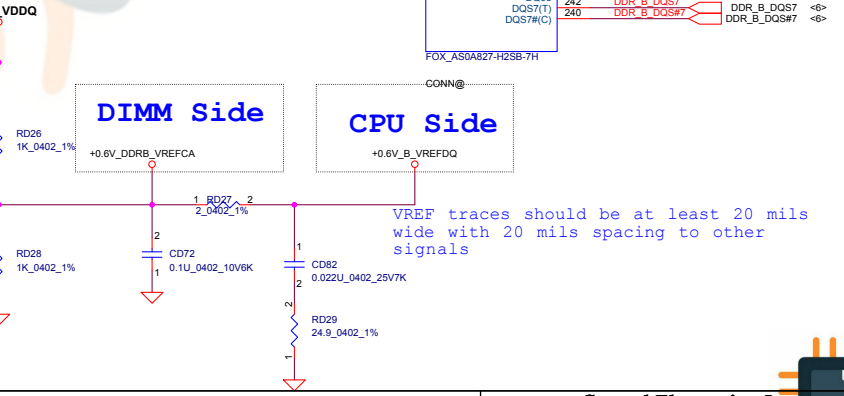


Interleaved Memory

STD (5.2 mm)



Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4



Security Classification	Compal Secret Data		
Issued Date	2015/08/03	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: P19-DDRIV_CHB: DIMM0

Size: | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 18 of 60

<5,6,7,9,10,11,13,17,18,20,21,22,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +3VS +3VS

<CPU CTRL>

<5> EDP_HPD EDP_HPD

RT11 100K_0402_5%

RTD2132 SMBus revrse to PCH

<7,10,22,26,37> EC_SMB_CK2 RT193 1 2 0_0201_5% CIICSCL1
<7,10,22,26,37> EC_SMB_DA2 RT194 1 2 0_0201_5% CIICSDA1
<7,17,18,22> PCH_SMBCLK RT1951 @ 2 0_0201_5%
<7,17,18,22> PCH_SMBDATA RT1961 @ 2 0_0201_5%

Layout notes
CC97~CC102 must closed to connector

<CPU>

<5> EDP_CPU_AUX_C CT102 1 2 .1U_0402_16V7K EDP_CPU_AUX
<5> EDP_CPU_AUX#_C CT101 1 2 .1U_0402_16V7K EDP_CPU_AUX#
<5> EDP_CPU_LANE_P0_C CT98 1 2 .1U_0402_16V7K EDP_CPU_LANE_P0
<5> EDP_CPU_LANE_N0_C CT97 1 2 .1U_0402_16V7K EDP_CPU_LANE_N0
<5> EDP_CPU_LANE_P1_C CT103 1 2 .1U_0402_16V7K EDP_CPU_LANE_P1
<5> EDP_CPU_LANE_N1_C CT100 1 2 .1U_0402_16V7K EDP_CPU_LANE_N1
eDP@

DB phase :
add eDP Lan1 for FHD
20141117

EDP_HPD RT34 1 2 0_0201_5% EDP_HPD_PANEL EDP_HPD_PANEL <20>

Delete BKL_PWM_CPU and DP_INT_PWM
20141113

<CPU by PASS eDP>

0_0804_8P4R_5%
EDP_CPU_LANE_N0 1 8 EDP_LANE_N0
EDP_CPU_LANE_P0 2 7 EDP_LANE_P0
EDP_CPU_AUX 3 6 EDP_AUX
EDP_CPU_AUX# 4 5 EDP_AUX#
RP6 eDP@ SD309000080
2

<eDP to connector>

RP9 eDP@ SD309000080
EDP_AUX 4 5 LCD_CLK LCD_CLK <20>
EDP_AUX# 3 6 LCD_DATA LCD_DATA <20>
EDP_LANE_N0 2 7 LVDS_TXN2_LN0 LVDS_TXN2_LN0 <20>
EDP_LANE_P0 1 8 LVDS_TXP2_LP0 LVDS_TXP2_LP0 <20>
0_0804_8P4R_5%
4

Layout notes
RP6 RP9 RP10 must closed to connector

EDP_CPU_LANE_P1 RT16 1 2 0_0402_5% LVDS_TXP1_LP1 LVDS_TXP1_LP1 <20>
EDP_CPU_LANE_N1 RT17 1 2 0_0402_5% LVDS_TXN1_LN1 LVDS_TXN1_LN1 <20>

DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

<RTS2132>
<EC CTRL>

<26> EC_BKOFF#

RT14 1 @ 2 0_0402_5%
CT24 1 2 @ 0.1U_0402_16V7K
+3VS
UT3
TS_BKOFF#
EC_BKOFF#
B A Y
LVDS@ TC7SH08FUF_SSOP5
EC_TS_BKOFF# <20>
RT12 100K_0402_5% LVDS@
RT15 1 2 0_0402_5%

<LVDS Panel>

PD 100K on LVDS page

Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

Compal Electronics, Inc.

Title: LVDS Translator-RTD2132N

Size: Document Number: LA-D707P Rev: V0.2

Date: Wednesday, May 11, 2016 Sheet 19 of 50

LVDS Power

<SI> change to standard par SA00006Y800 (Different footprint)

+3VS
N6U@ UG1
VIN VOUT GND EN /OC
G524B1T11U_SOT23-5
SA00006Y800
<5> ENVDD_CPU
R172 1 2 0_0402_5%
+LCDVDD
CG2 4.7U_0603_6.3V6K
CG3 0.1U_0402_16V7K
+3VS
RG1 0_0201_5%
CG1 eDP@ 1500P_0402_50V7K
Main SA00006Y800
2nd SA00007U000
3rd SA000079400
UG1 6U@ G524B2T11U SOT-23 SA00007BW00

W=60mils
SM010014520 3000ma
220ohm@100mhz
DCR 0.04
INVPWR_B+
JPHW1@ JUMP_43X79
W=60mils
+19.5VB
@EMI@ C117 680P_0402_50V7K
C118 68P_0402_50V8J
FU1 6U@
FUSE 0438.500WR 0.5A 32V UL/CSA FAST
SP040004X00

<5,6,7,9,10,11,13,17,18,19,21,22,23,24,26,28,32,33,34,35,36,37,38,52,55,56> +3VS
<38,47,48,49,50,53,55,56> +19.5VB
<7,13,23,26,27,30,33,35,48,49,50,51,55> +3VALW

Camera

<11> USB20_N5
<11> USB20_P5
Part Number = SM070003Y00
R170 0_0402_5%
L12 @EMI@
USB20_N5_R
USB20_P5_R
WCM-2012-900T_4P
R171 0_0402_5%

D7 @ESD@ SCA00000U10
USB20_P5_R
USB20_N5_R
PESD5V0U2BT_SOT23-3

LCD/LED PANEL Conn.

C593 2 1 220P_0402_50V7K INVTPWM
C594 2 1 220P_0402_50V7K DISPOFF#

<DB>LA1/LA2 closed to Aduio codec

<24> D_MIC_CLK
<24> D_MIC_DATA
EMI@ SM01000B600
D_MIC_CLK D_MIC_L_CLK
LA1 FBMA-L10-160808-301LMT_2P
D_MIC_DATA D_MIC_L_DATA
R175 0_0402_5%

D3 @ESD@ SCA00000U10
D_MIC_L_CLK
D_MIC_L_DATA
PESD5V0U2BT_SOT23-3

Touch Screen

<DB> for 5V/3V TS option

Touch Screen Power
+3VALW +5VALW
@ RTS2 100K_0402_5%
TS@ RTS3 100K_0402_5%
TS@ RTS1 1K_0402_5%
TS@ QTS1 2N7002K_SOT23
TOUCH_ON# <26>
TS@CTS2 0.047U_0402_16V7K
+VCC_TOUCH_IN
TS@ CTS1 0.1U_0402_16V4Z
TS@ QTS2 S TR LP2301ALT1G 1P SOT-23-3
RG4 @ 0_0402_5% +3VS
RG5 TS@ 0_0402_5% +5VS
@R36 0_0603_5%

<5> BKL_PWM_CPU
R259 0_0402_5%
INVTPWM
LVDS@ R163 100K_0402_5%

<19> EC_TS_BKOFF#
EC_TS_BKOFF# R166 33_0402_5% DISPOFF#
R5176 10K_0402_5%

<10> TS_GPIO_CPU
<26> TS_GPIO_EC
R260 @ 0_0402_5%
R5187 0_0402_5%
TS_GPIO
<PV> Touch GPIO control by EC

CONN@ JLVDS1
STARC_107K40-000001-G2
SP01000XE00
EDP_CPU_LANE_P1 <19> LVDS_TXP1_LP1
EDP_CPU_LANE_N1 <19> LVDS_TXN1_LN1
EDP_CPU_LANE_P0 <19> LVDS_TXP2_LP0
EDP_CPU_LANE_N0 <19> LVDS_TXN2_LN0
EDP_CPU_AUX <19> LCD_CLK
EDP_CPU_AUX# <19> LCD_DATA
+LCDVDD
<19> EDP_HPD_PANEL
Touch screen
USB20_P6_R
USB20_N6_R
DISPOFF#
INVTPWM
TS_GPIO
INVPWR_B+
+VCC_TOUCH
+3VS_CAMERA
Camera
USB20_N5_R
USB20_P5_R
D_MIC_L_CLK
D_MIC_L_DATA

JP@ JPHW4 JUMP_43X39
6U@ FG3 SA00004ZA00
+3VS
+3VS_CAMERA
@ C5221 .1U_0402_16V7K
6U@ C5222 4.7U 6.3V M X5R SE00000SO00
AP2330W-7_SC59-3

+VCC_TOUCH
JP@ JPHW3 JUMP_43X39
TS6U@ FG2 SA00004ZA00
TS6U@ C5223 4.7U 6.3V M X5R SE00000SO00
@ CTS3 0.1U 16V K X7R
+VCC_TOUCH_IN
AP2330W-7_SC59-3

<11> USB20_N6
<11> USB20_P6
Part Number = SM070003Y00
R5175 0_0402_5%
L13 @EMI@
USB20_N6_R
USB20_P6_R
WCM-2012-900T_4P
R173 0_0402_5%

D6
USB20_P6_R
USB20_N6_R
PESD5V0U2BT_SOT23-3
@ESD@ SCA00000U10

Eletro-X

ECEtR0-L

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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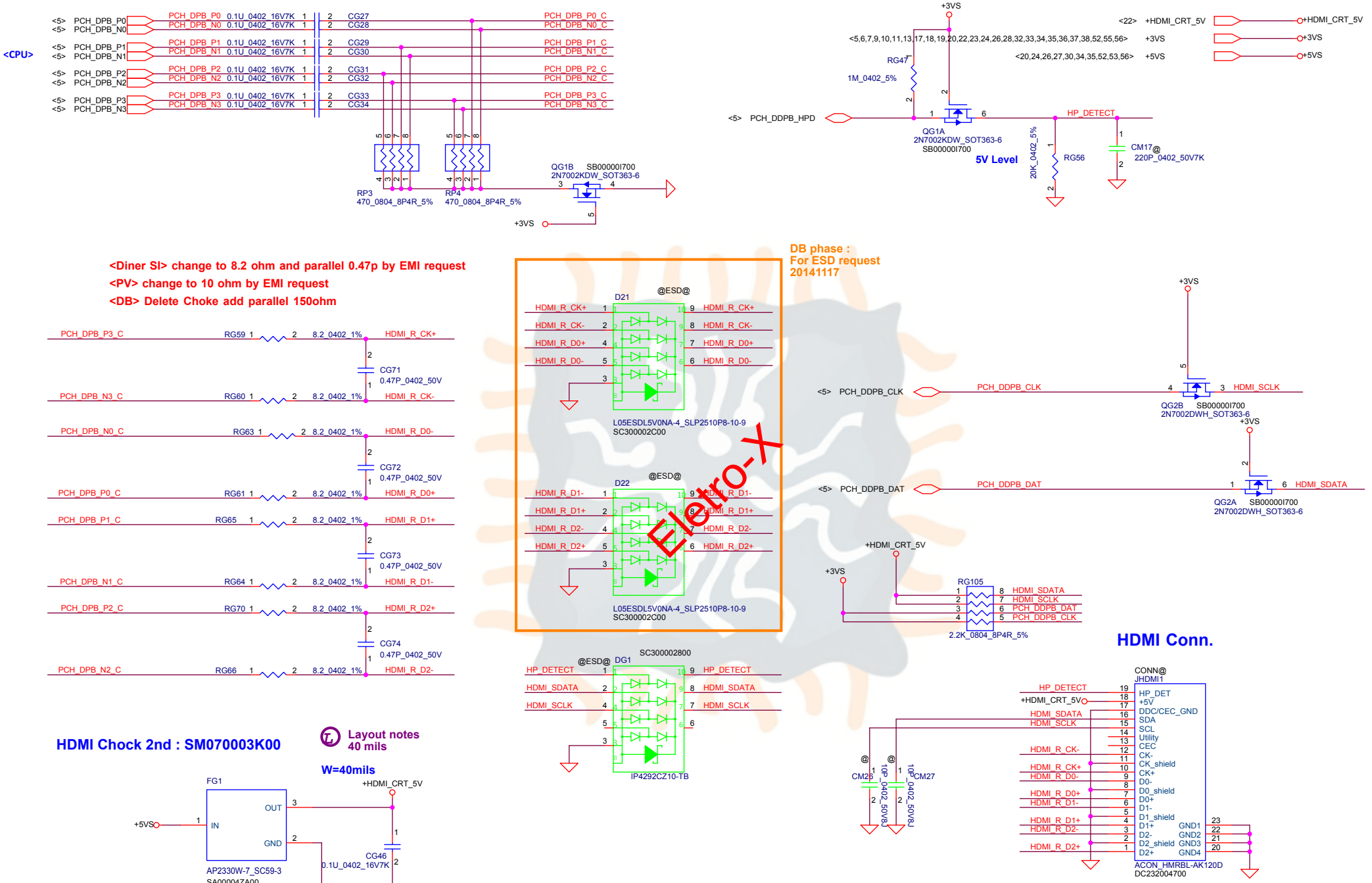
Compal Electronics, Inc.
Title: LVDS Connector
Size: Document Number: LA-C707P Rev: v0.2
Date: Wednesday, May 11, 2016 Sheet 20 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

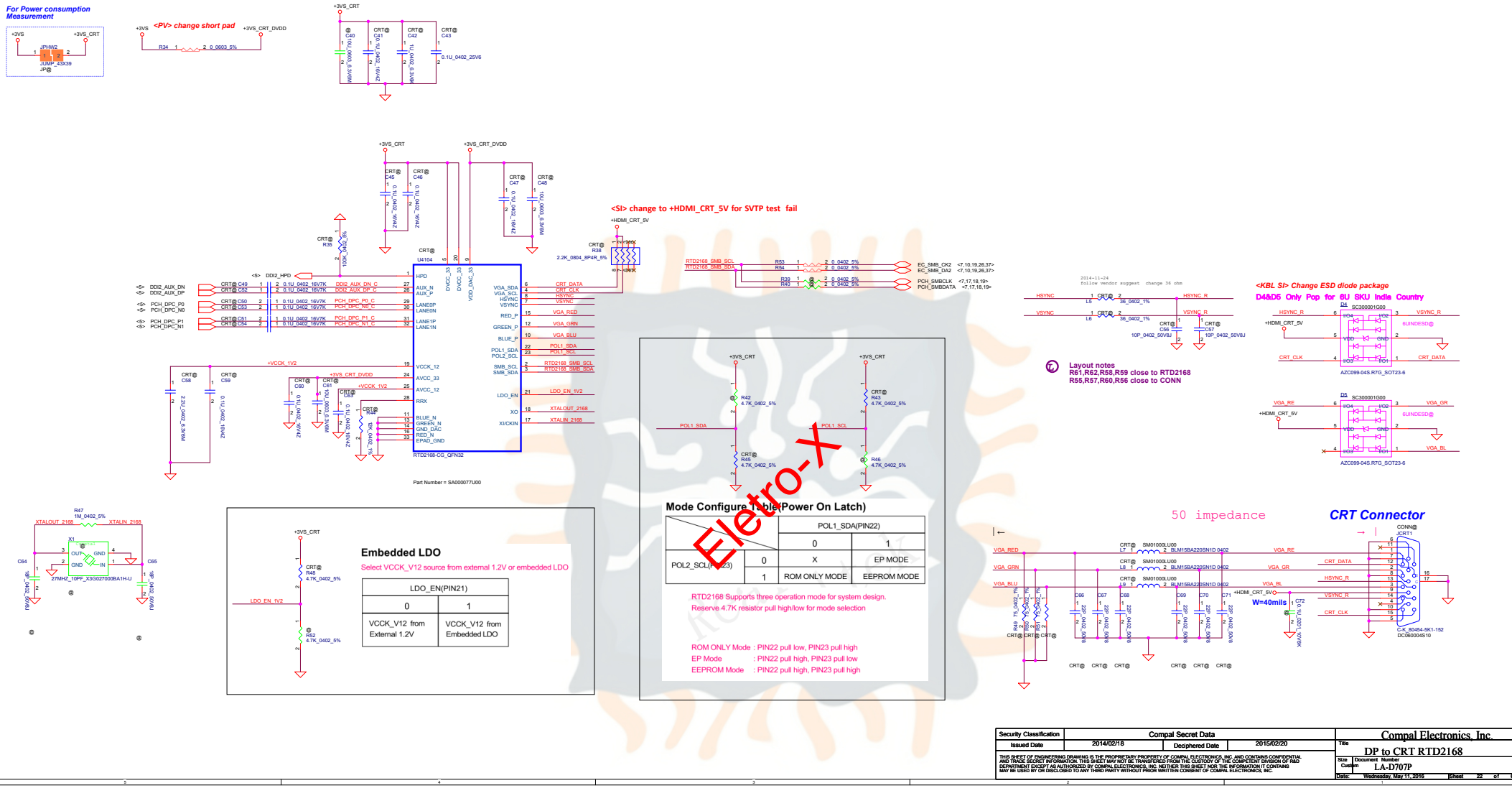
Title: HDMI Conn/Level shift

Size	Document Number	Rev
	LA-D707P	1.0

Date: Wednesday, May 11, 2016 Sheet 21 of 60

ECEtR0-L

DP to CRT converter



Security Classification: Compal Secret Data
Issued Date: 2014/02/18 Deciphered Date: 2015/02/20

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Compal Electronics, Inc.
Title: DP to CRT RTD2168
Size: Custom | Document Number: LA-D707P | Rev: v0.2
Date: Wednesday, May 11, 2016 | Sheet 22 of 60

+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

8/15 Change to LDO Mode

	LDO mode	Switcing mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8,CL23	@	SMT

CL13 & CL15 close UL1 Pin22
CL14 & CL27 close UL1 Pin30

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

Place CL11~CL12 close UL1 Pin 3,8

8151/8166 Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

0923 PV CNG from DP00 to E500

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

EC control 08/17 Add 0ohm

Swap P/N 08/16

SP050005L00 Footprint

(SA000063500) 8166GSH 10/100
(SA000084T00) 8111HSH-CG Giga

2016-03-03:Change Single Source
(SP050008V00) 10/100
(SP050008Y00) Giga

11/18 modify vendor review results

11/15 change CONN.

11/17 reserver for ESD request

powe rail need to check

powe rail need to check

CR RTS5237S move to S/B

Eletro-X

ECEtR0-L

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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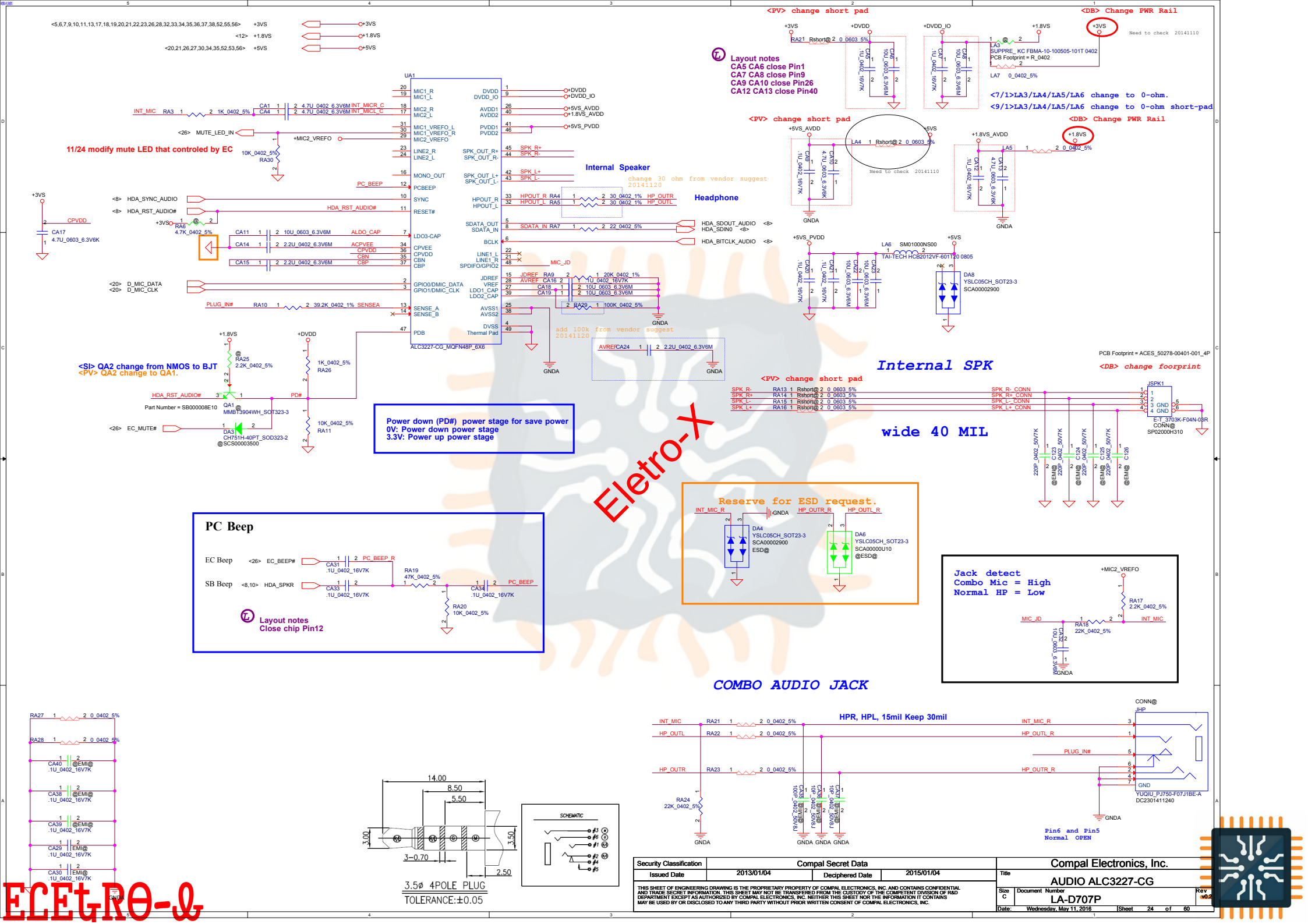
Compal Electronics, Inc.

Title: LAN 8151/8166_ CR RTS5238

Size: | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 23 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.			
Title	AUDIO ALC3227-CG		
Size C	Document Number LA-D707P		Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 24 of 60		

EC Board ID (UMA, Dis, phase) control table

RK4	DB	SI	PV	MV	Note
UMA	15Kohm	27Kohm	43Kohm	75Kohm	
Dis	20Kohm	33Kohm	56Kohm	100Kohm	

Current

DB_UMA_15kohm:SD034150280, S RES 1/16W 15K +-1% 0402
DB_DIS_20kohm:SD034200280, S RES 1/16W 20K +-1% 0402
SI_UMA_27kohm:SD034270280, S RES 1/16W 27K +-1% 0402
SI_DIS_33kohm:SD034330280, S RES 1/16W 33K +-1% 0402
PV_UMA_43kohm:SD034430280, S RES 1/16W 43K +-1% 0402
PV_DIS_56kohm:SD034560280, S RES 1/16W 56K +-1% 0402
MV_UMA_75kohm:SD034750280, S RES 1/16W 75K +-1% 0402
MV_DIS_100kohm:SD034100380, S RES 1/16W 100K +-1% 0402

<PV> change short pad

<SI> un-mount RC , Internal PU in 9022

Board ID control

Reserve EC_CLR_CMOS for clear CMOS
(2016-03-04 : Confirm intel platform not support EC Clear CMOS function)

<SI> EC request to add RK9

<DB> for leakage of LED light

For Solve tPCH04(Min 9ms) Sequence Timing

CC128 RC369 place near EC Side

EMI request

Elerov

UK1 KB9022QD_LQFP128_14X14

20mil

2014-11-25
Reserve for co-lay Nuvoton NPCE388N

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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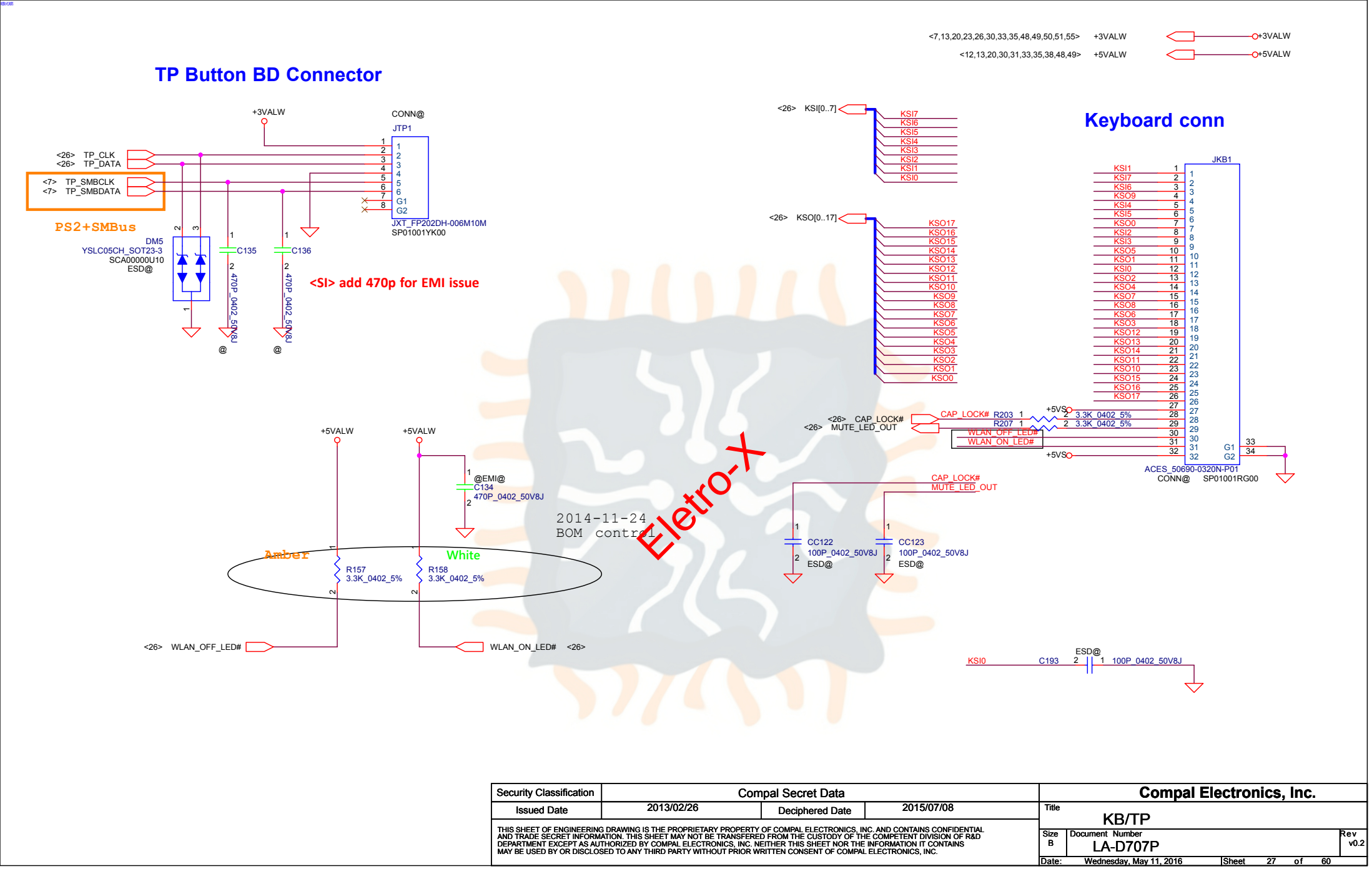
Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | Document Number: LA-D707P | Rev: 0.4

Date: Wednesday, May 11, 2016 | Sheet 2 of 60

ECEtR0-L

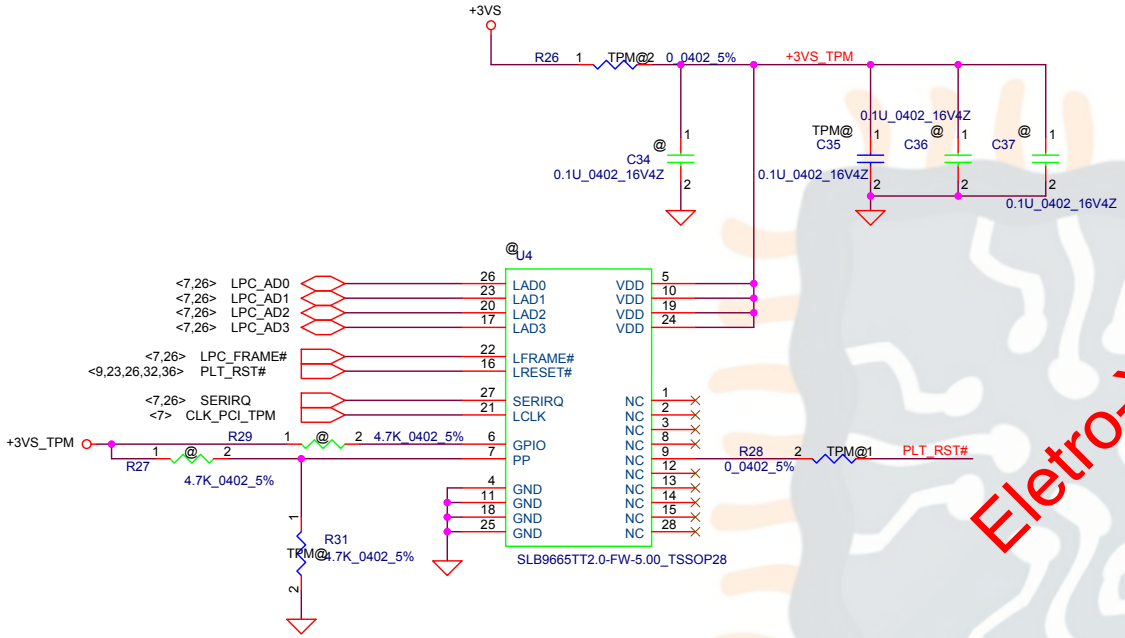


Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

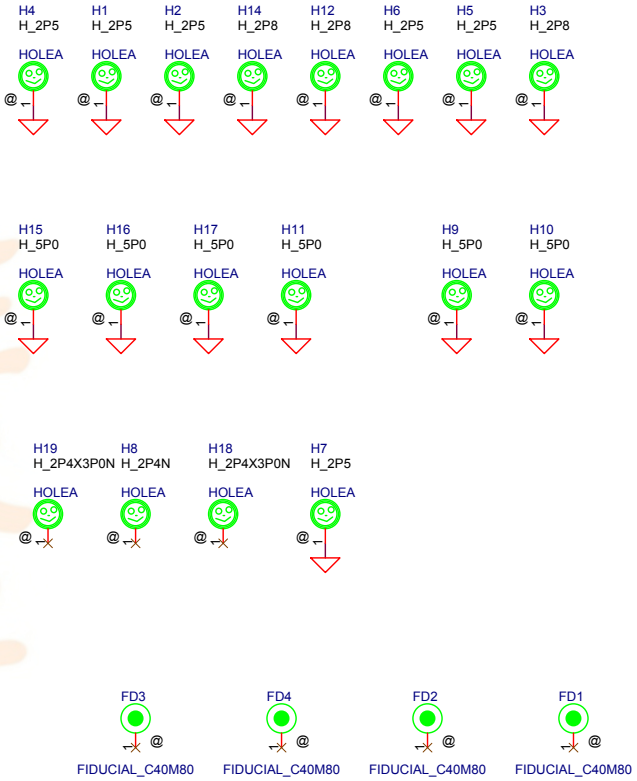
Title	KB/TP	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 27 of 60	

TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **TPM/Screw**

Size	Document Number	Rev
	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 28 of 60

BOM control

Plat f or m	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	GCLKPX@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: GCLK

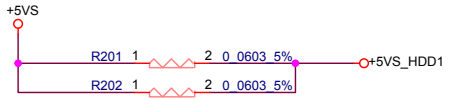
Size | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 29 of 60

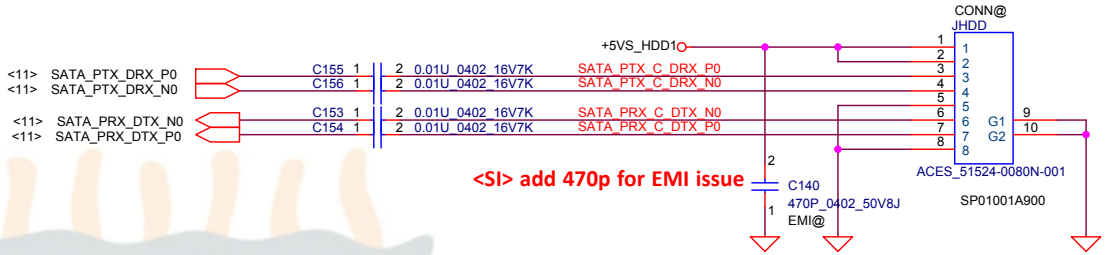
2.5" SATA HDD

<20,21,24,26,27,34,35,52,53,56> +5VS
<12,13,20,27,31,33,35,38,48,49> +5VALW
<7,13,20,23,26,27,33,35,48,49,50,51,55> +3VALW
<32> +3VS_WLAN_R

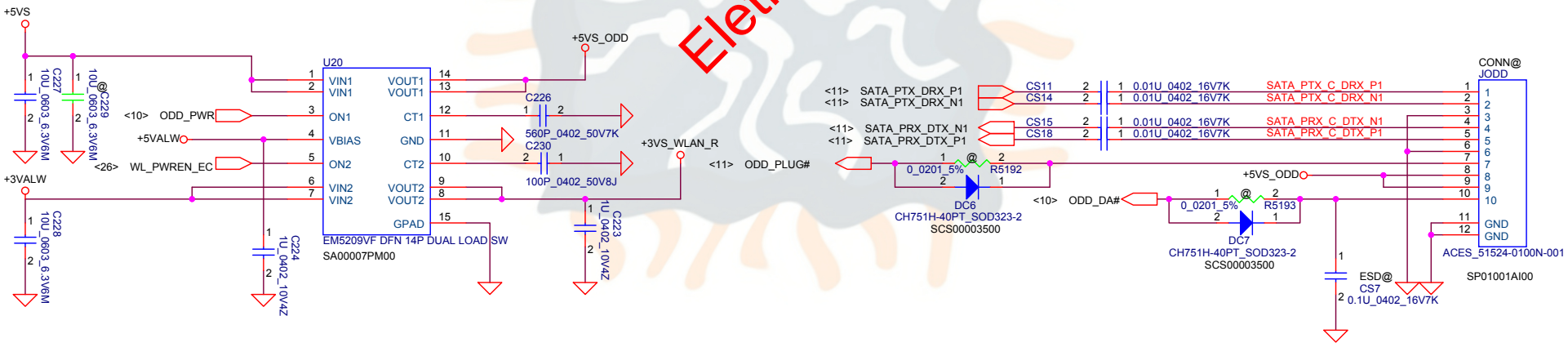
<PV> change short pad



<DB> change JHDD pin define



2.5" SATA ODD



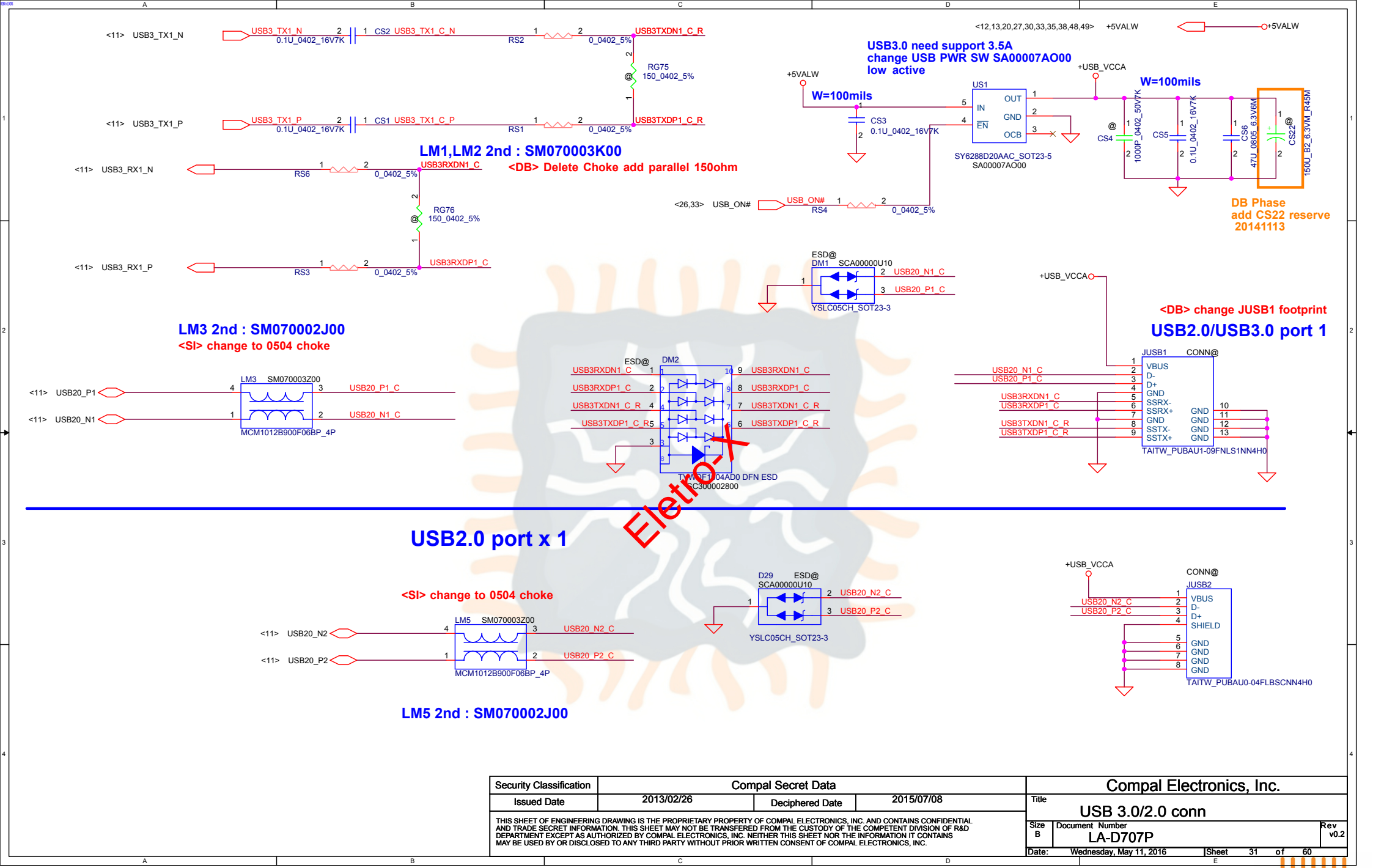
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: HDD/ODD Conn

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 30 of 60



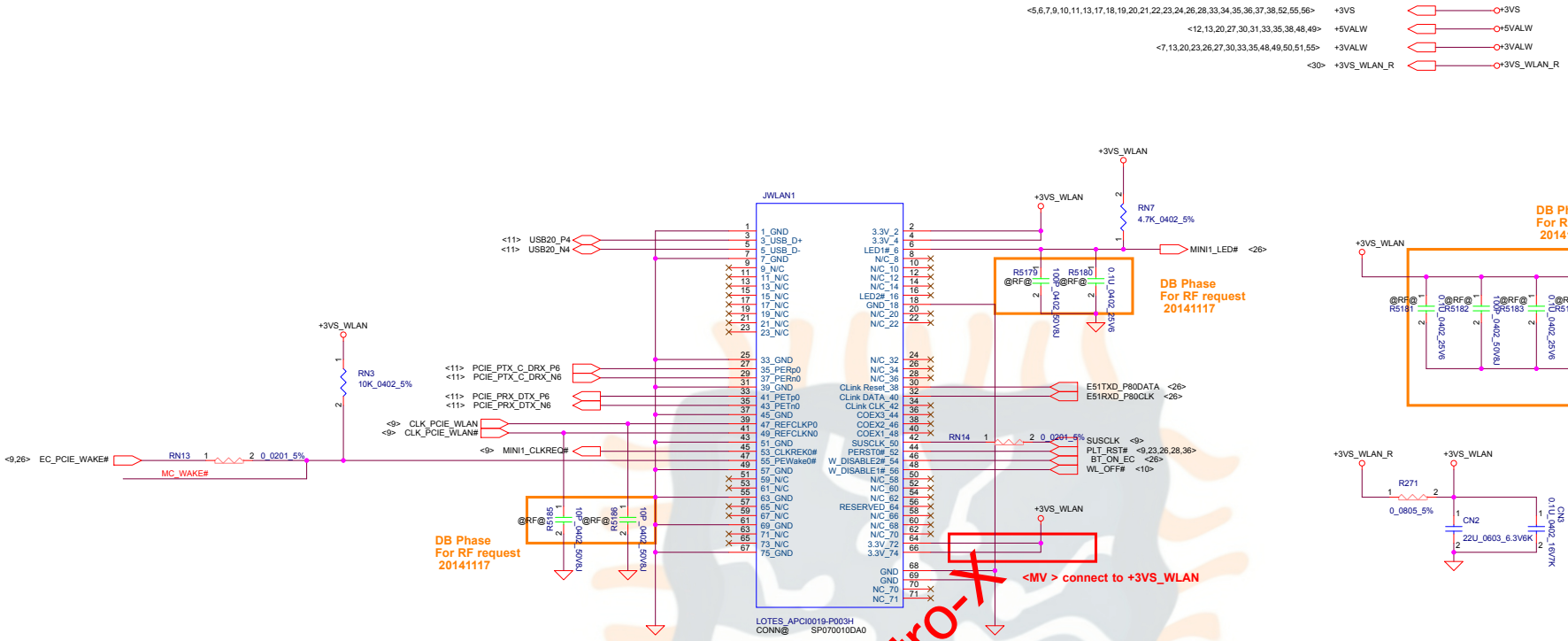
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

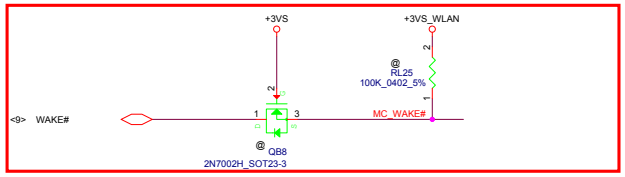
Title: USB 3.0/2.0 conn

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 31 of 60



NGFF and WLAN



Unpop QB4 and RL23 for not support OBFF

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

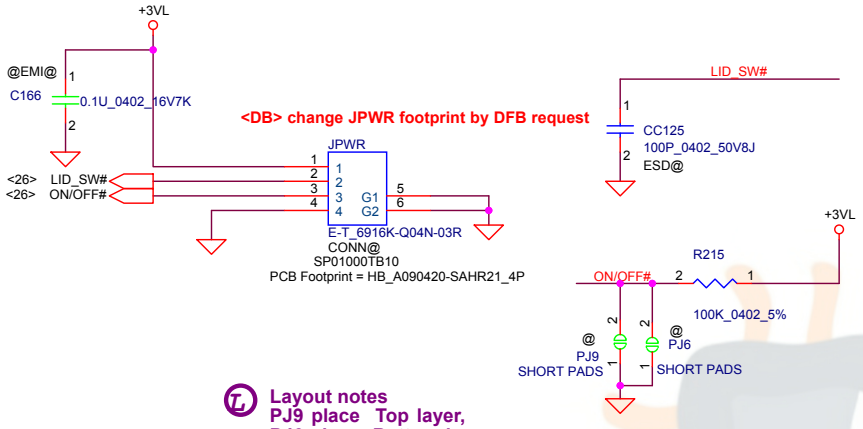
Compal Electronics, Inc.

Title: WLAN-BT

Size	Document Number	Rev
	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 32 of 60

Powert Button Connector



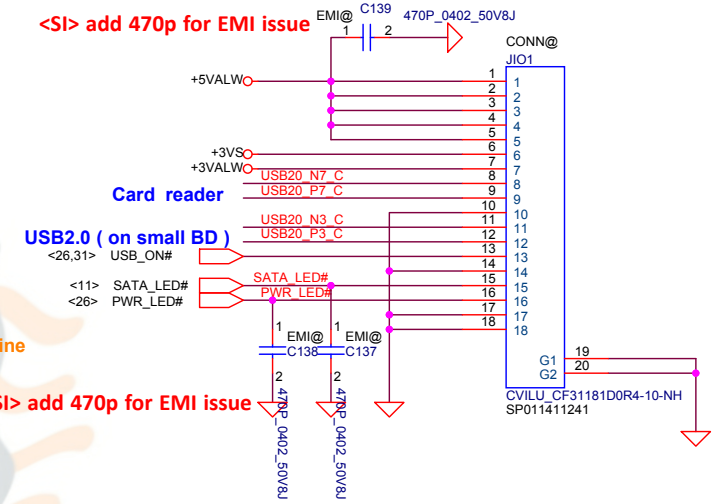
Layout notes
PJ9 place Top layer,
PJ6 place Bottom layer

<13,26,46,47,48> +3VL
<12,13,20,27,30,31,35,38,48,49> +5VALW
<5,6,7,9,10,11,13,17,18,19,20,21,22,23,24,26,28,32,34,35,36,37,38,52,55,56> +3VS
<7,13,20,23,26,27,30,35,48,49,50,51,55> +3VALW

11/26 change CONN.

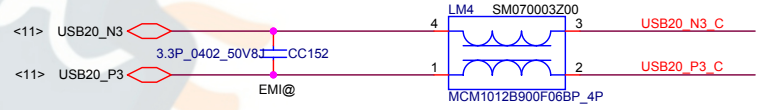
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

<SI> add 470p for EMI issue



DB phase :
modify pin define
20141114

<SI> add 470p for EMI issue



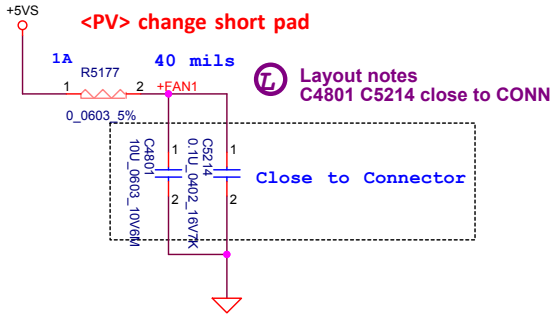
<MV> add AC cap

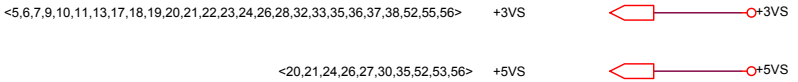
<SI> change to 0504 choke

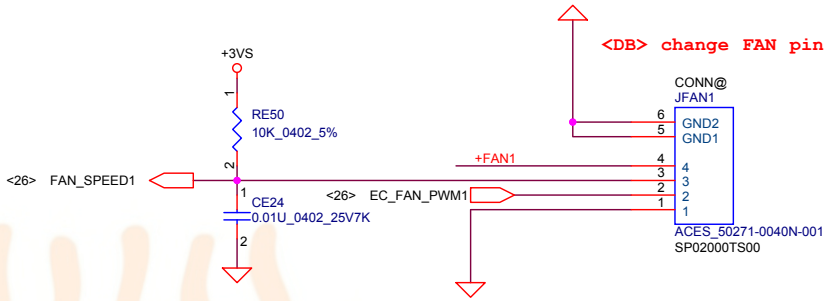
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title	IO CON	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 33 of 60	







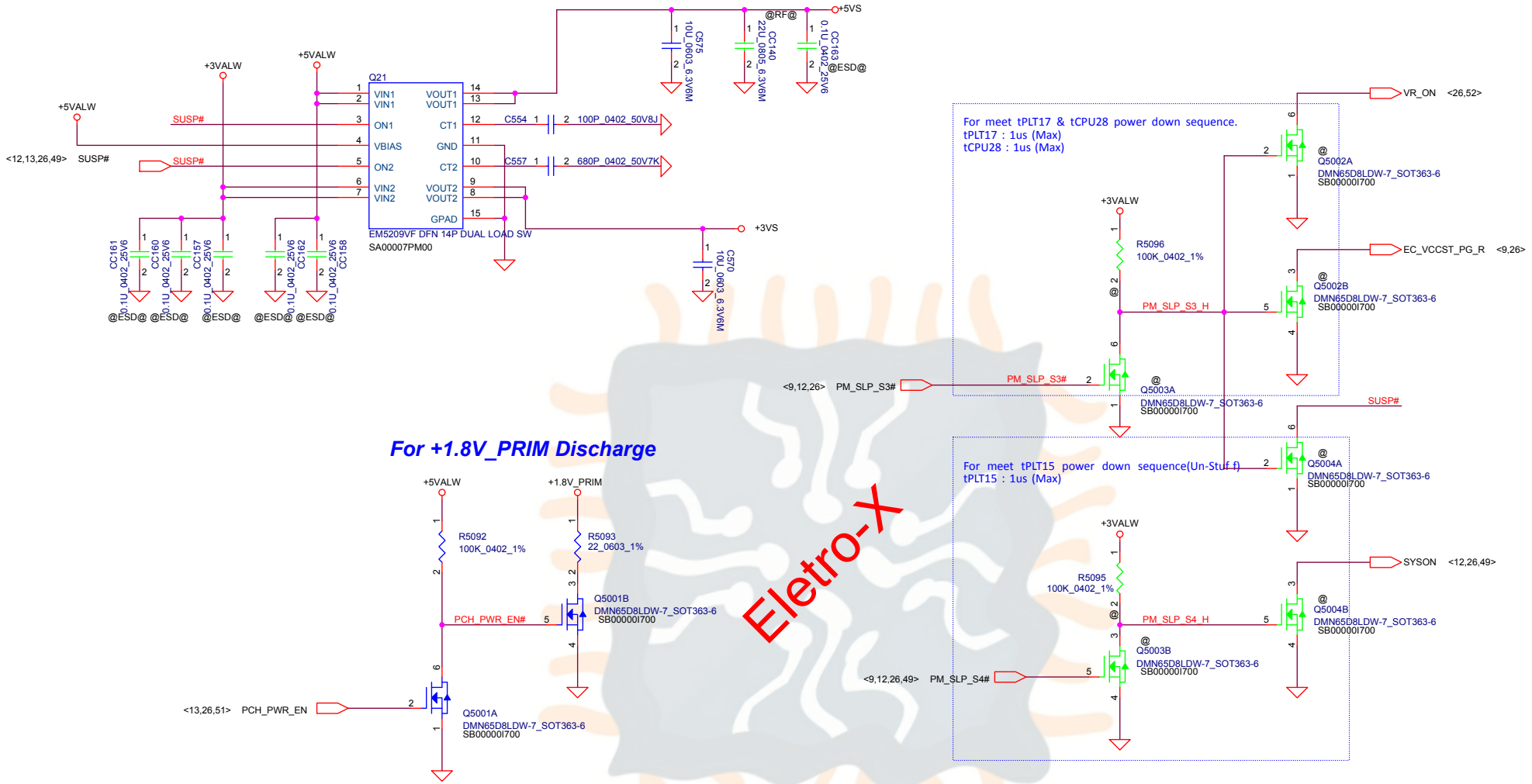
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FAN

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 | Sheet 34 of 60



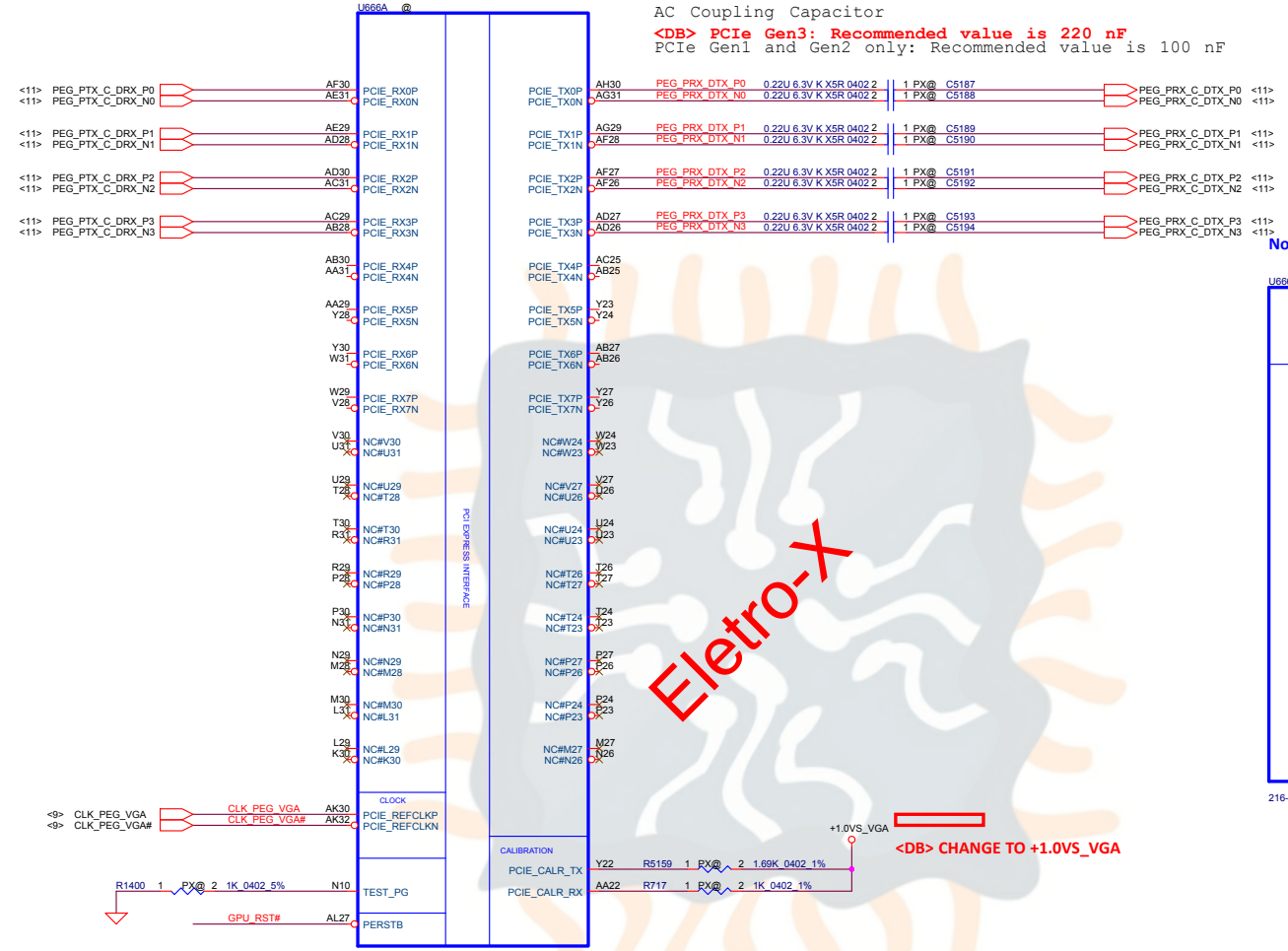
Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: LA-D707P	Rev: 1.0	
Date: Wednesday, May 11, 2016	Sheet 35 of 60		

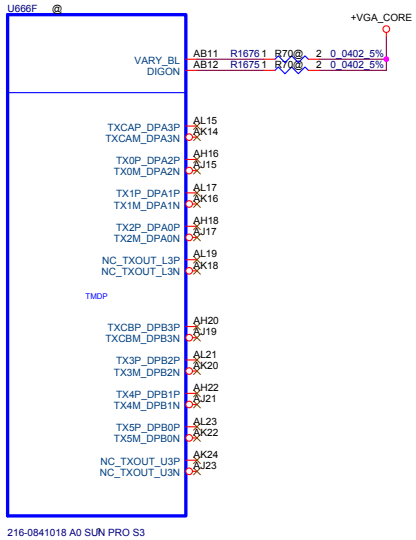
AC Coupling Capacitor

<DB> PCIe Gen3: Recommended value is 220 nF

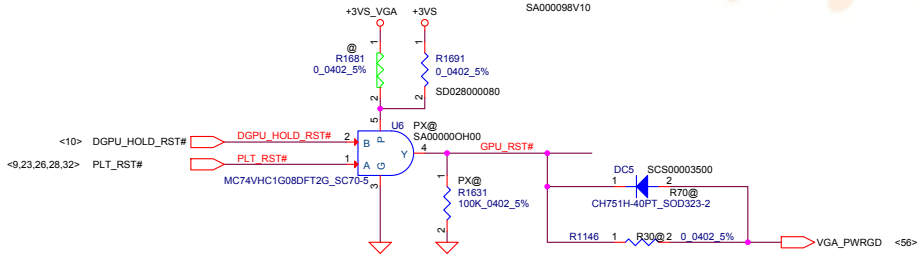
PCIe Gen1 and Gen2 only: Recommended value is 100 nF



No Use GPU Display Port outpud



<DB> CHANGE TO +1.0VS_VGA



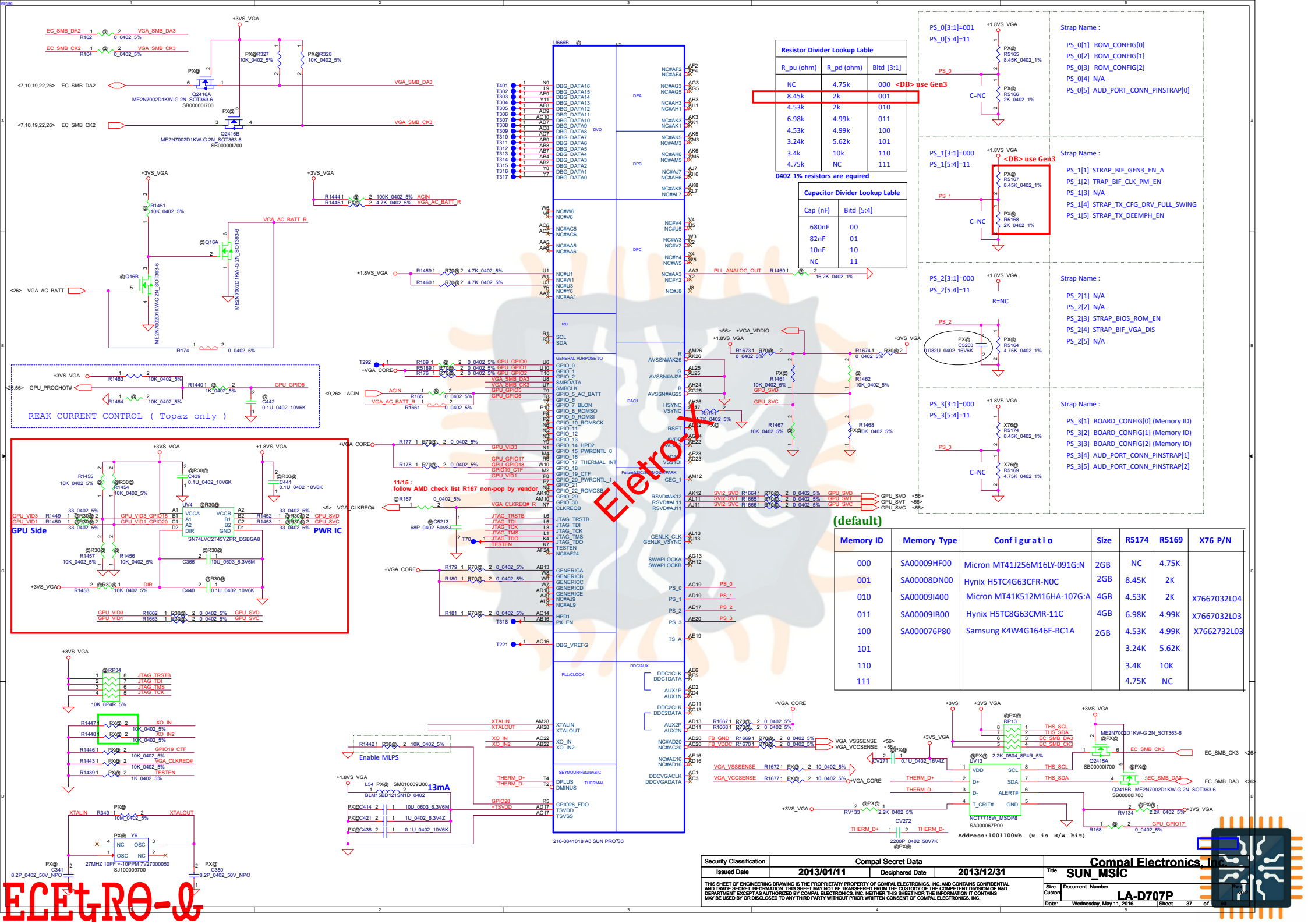
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_PCIE/DP

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 36 of 60


Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000 <DB> use Gen3
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
<DB> use Gen3
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
R=NC
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
REAK CURRENT CONTROL (Topaz only)
GPU Side
PWR IC
11/15 :
follow AMD check list R167 non-pop by vendor
Enable MLPS
13mA
Eletroy
(default)
Memory ID | Memory Type | Configuration | Size | R5174 | R5169 | X76 P/N
000 | SA00009HF00 | Micron MT41J256M16LY-091G:N | 2GB | NC | 4.75K |
001 | SA00008DN00 | Hynix H5TC4G63CFR-N0C | 2GB | 8.45K | 2K |
010 | SA00009I400 | Micron MT41K512M16HA-107G:A | 4GB | 4.53K | 2K | X7667032L04
011 | SA00009IB00 | Hynix H5TC8G63CMR-11C | 4GB | 6.98K | 4.99K | X7667032L03
100 | SA000076P80 | Samsung K4W4G1646E-BC1A | 2GB | 4.53K | 4.99K | X7662732L03
101 | | | | 3.24K | 5.62K |
110 | | | | 3.4K | 10K |
111 | | | | 4.75K | NC |
Address:1001100xb (x is R/W bit)
216-0841018 A0 SUN PRO'S3
Security Classification | Compal Secret Data
Issued Date | 2013/01/11 | Deciphered Date | 2013/12/31
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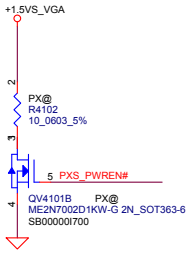
Compal Electronics, Inc.
Title SUN_MSIC
Size Custom | Document Number LA-D707P | Rev 1.0
Date: Wednesday, May 11, 2016 | Sheet 37 of 50
ECE-RO-L

+1.5VS to +1.5VS_VGA (2.096A)

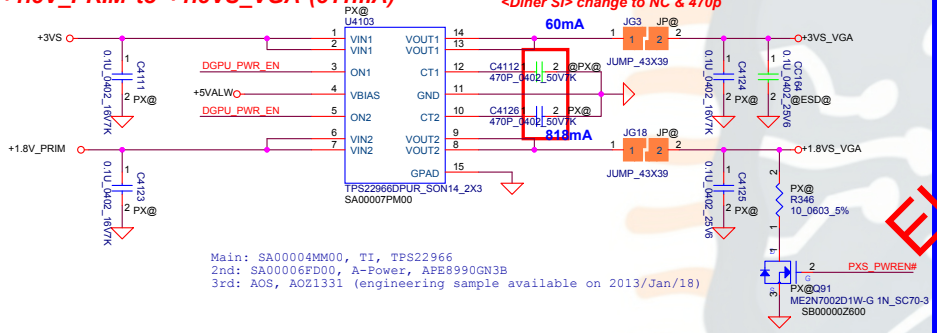
Delete +1.5VS to +1.5VS_VGA power switch



+3VS to +3VS_VGA (25mA)

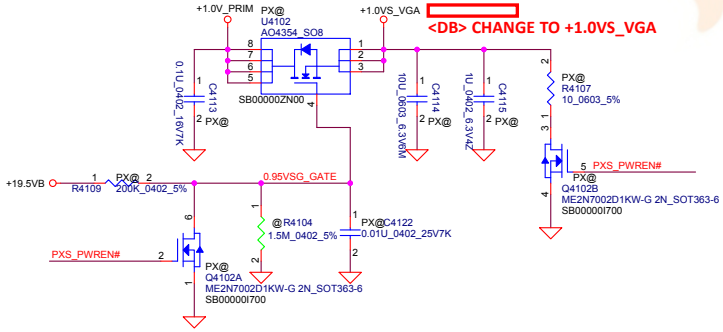
+1.8V_PRIM to +1.8VS_VGA (311mA)

<Diner SI> change to NC & 470p



Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: AOS, AO21331 (engineering sample available on 2013/Jan/18)

+1.0V_PRIM to +1.0VS_VGA (4.016A)

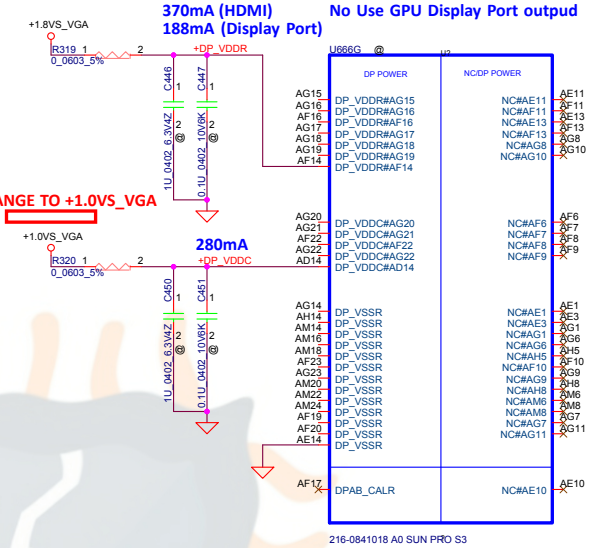


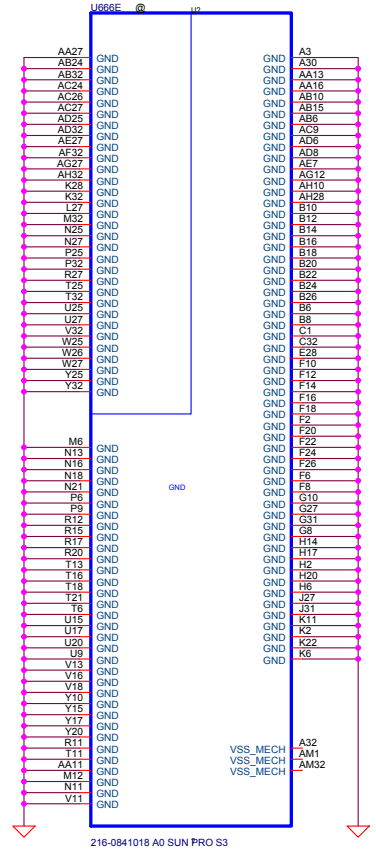
370mA (HDMI) 188mA (Display Port)

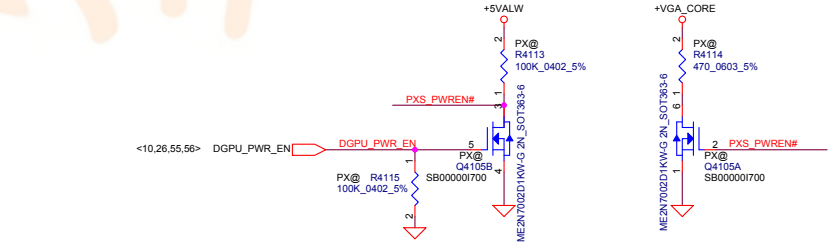
No Use GPU Display Port outpud

<DB> CHANGE TO +1.0VS_VGA

280mA







Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 38 of 60

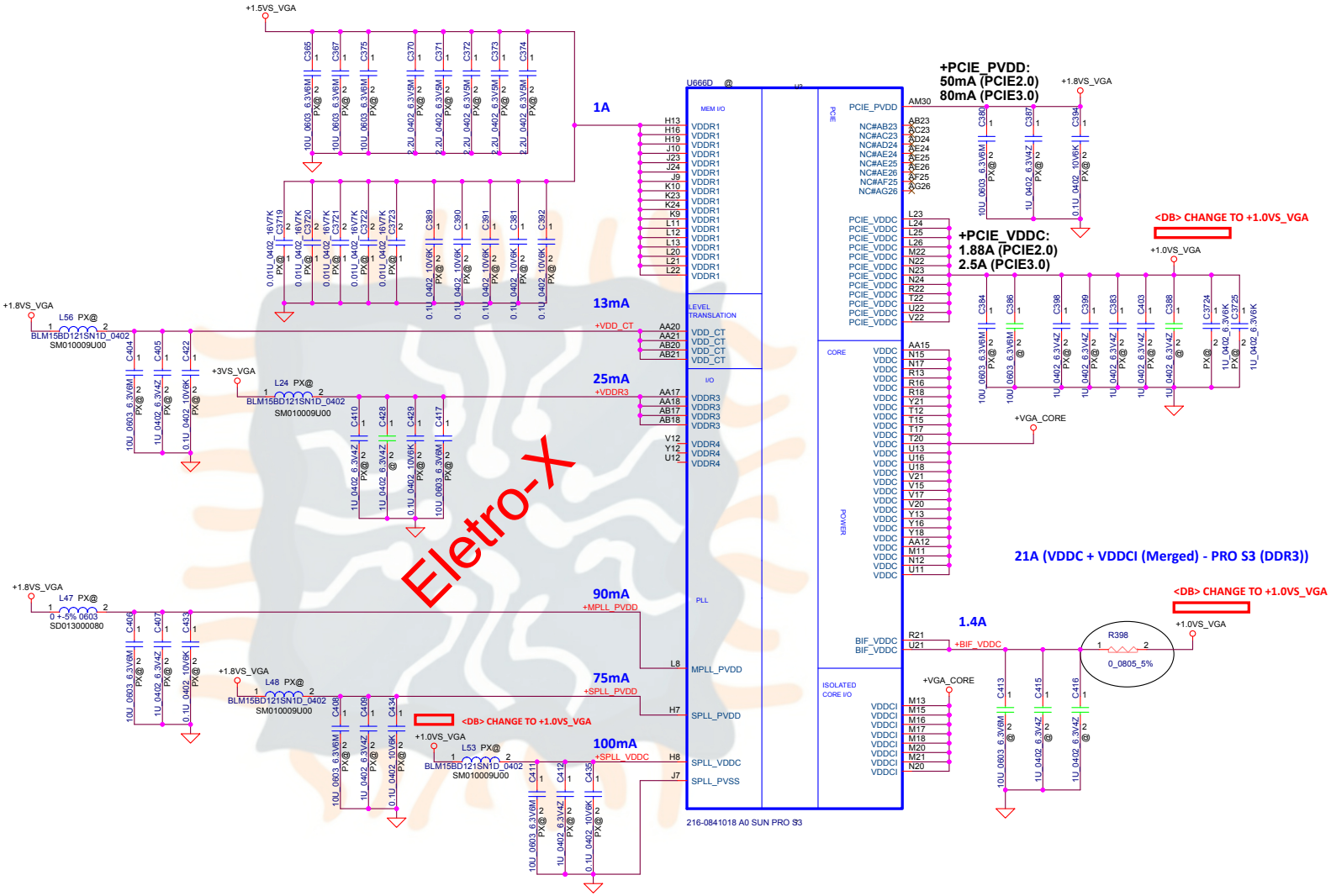
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+1.0VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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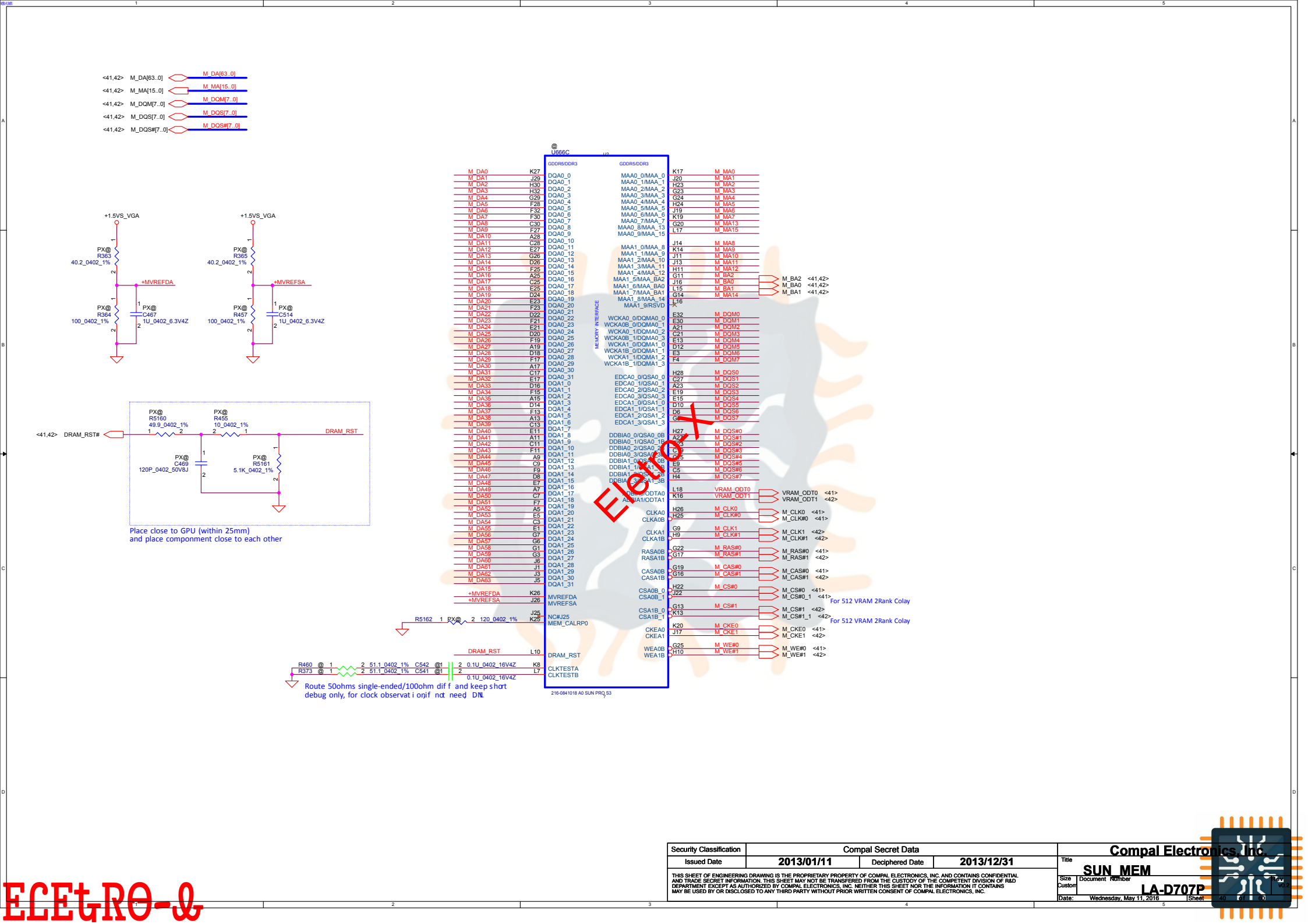
Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 39 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

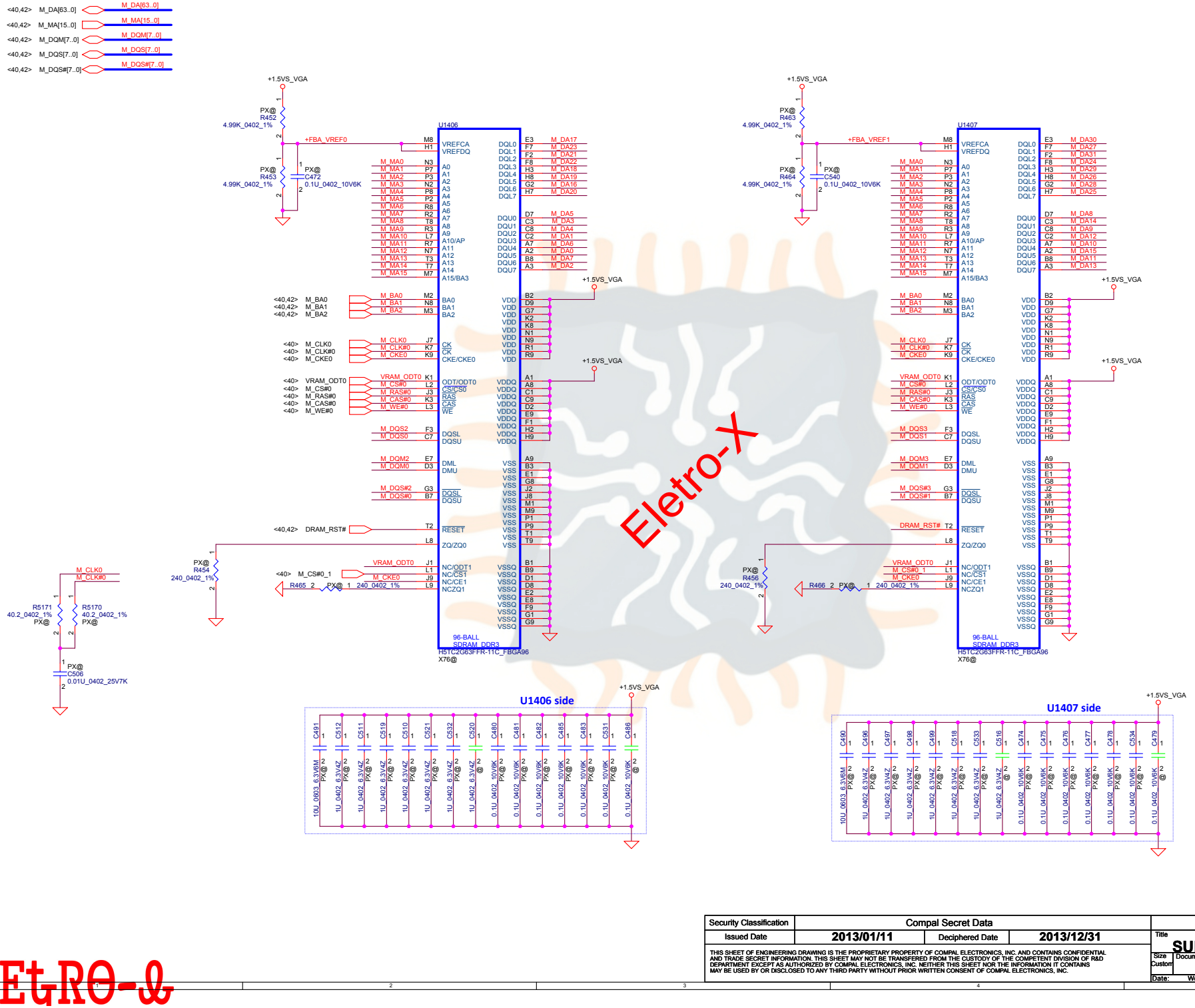
Title: SUN_MEM

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 40 of 60

ECEtRO-Q

Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

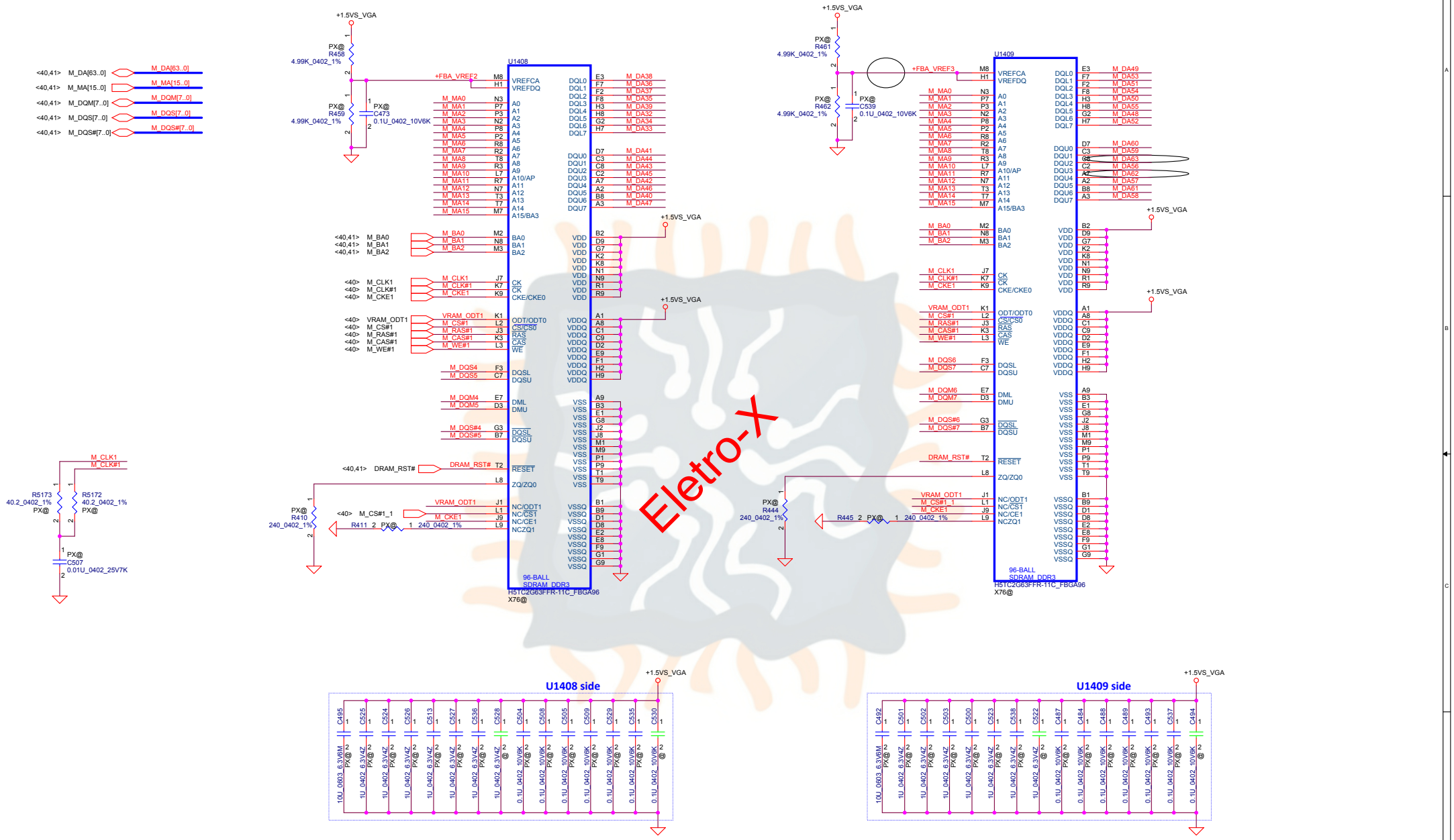
Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 41 of 60

Memory Partition A - Upper 32 bits



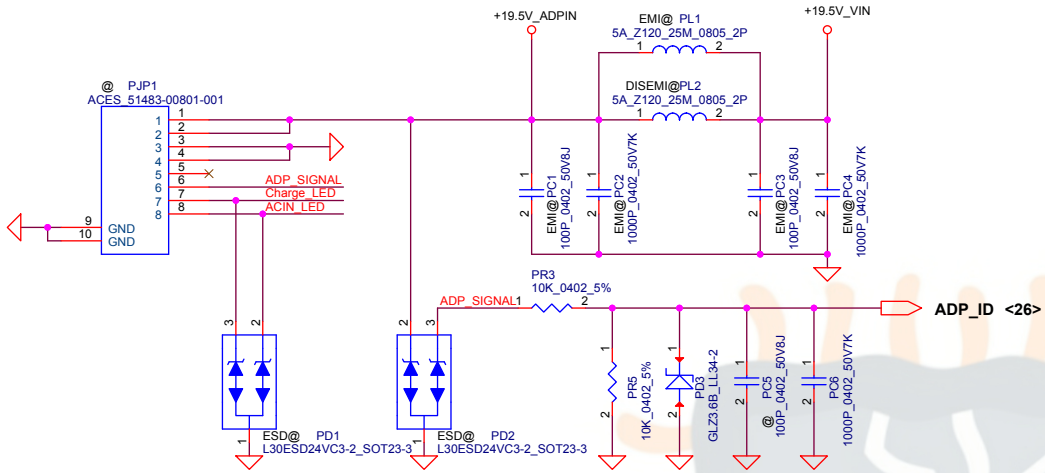
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

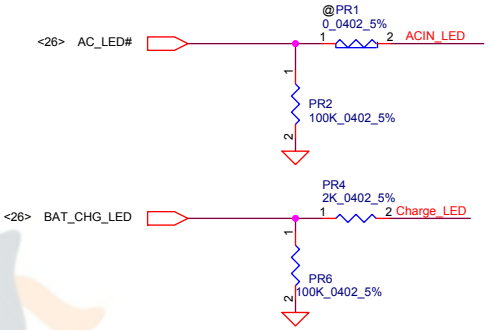
Compal Electronics, Inc.

Title: SUN_VRAM A Upper

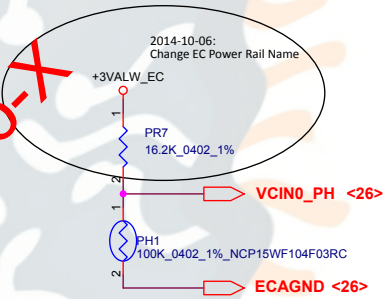
Size: Custom | Document Number: LA-D707P | Rev: 1.0

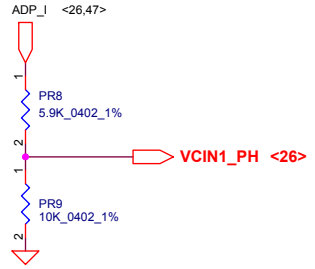
Date: Wednesday, May 11, 2016 | Sheet 42 of 60





ADP_ID			
Adapter Type		Voltage Range (Dec)	Voltage Range (Hex)
None	Normal Adapter	<0.211V	< 10
	Air-Line Apdater	<0.334V	< 1A
40W	Normal Adapter	>=0.211V ;<0.349V	>= 10 < 1A
45W	Normal Adapter	>=0.349 ;<0.442	>= 1A < 20
65W	Normal Adapter	>=0.442V ;<0.549V	>=20 <2A
	Air-Line Apdater	>=0.334V ;<0.425V	>= 1A < 21
90W	Normal Adapter	>=0.549V ;<0.710V	>= 2A < 36
	Air-Line Apdater	>=0.425 ;<1.391V	>= 21 < 6A
120W	Normal Adapter	>=0.710V ;<1.391V	>= 36 < 6A
ID is shorted to VIN		>=1.391V with Normal and Air-Line	>= 6A



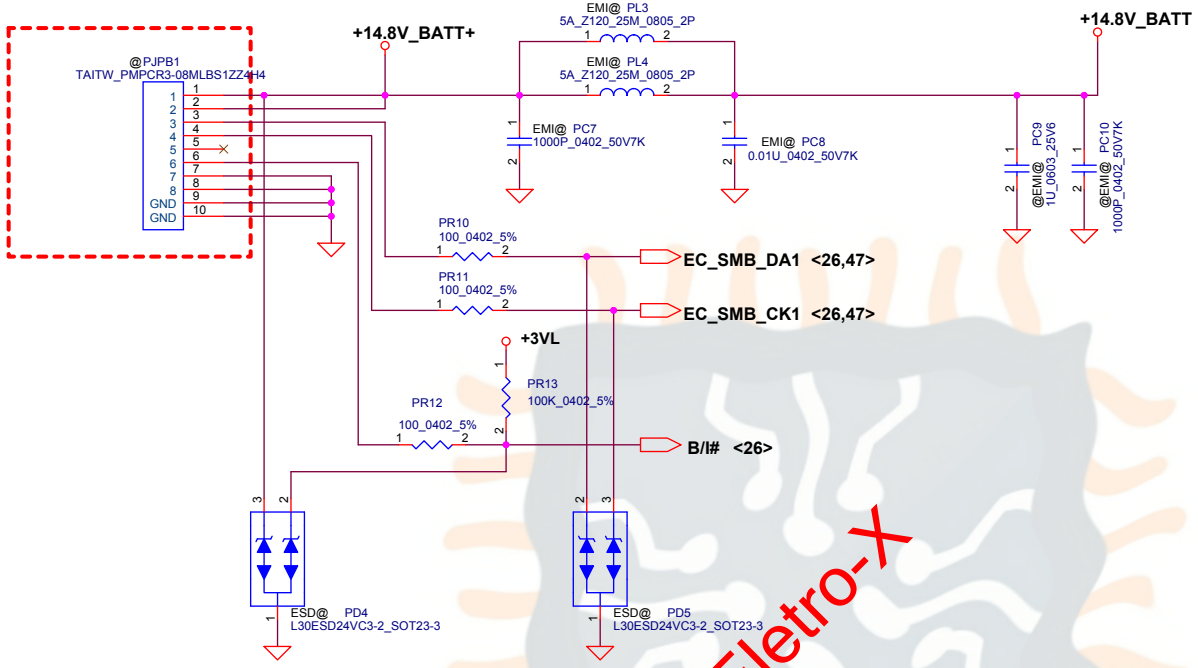


	Initail	Recovery
OTP	92 C	56 C

	Initail	Recovery
45W UMA	0.65V	0.45V
65W DIS	0.95V	0.67V

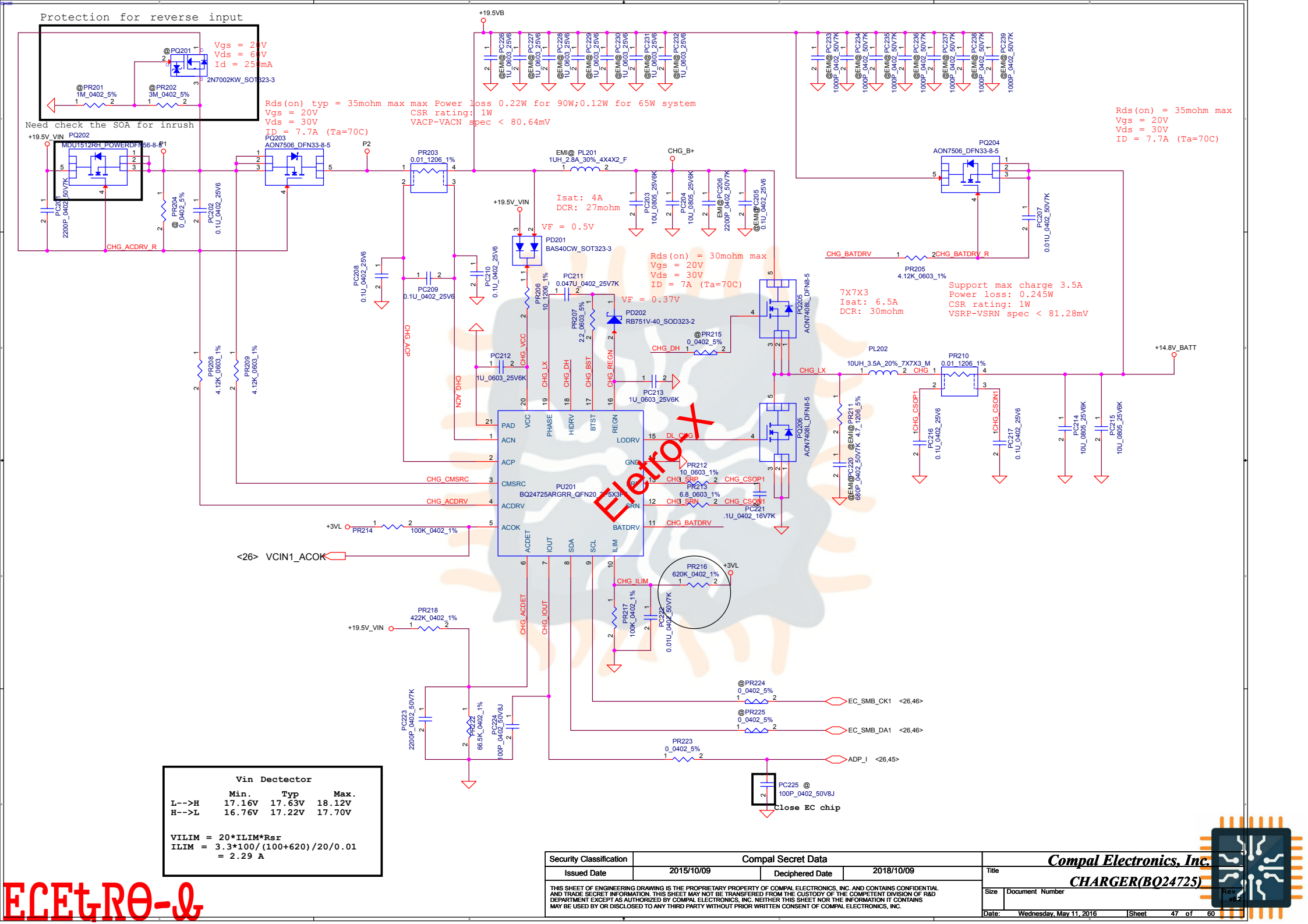
Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.			
Title	DC Conn		
Size	Document Number LA-D707P		Rev 0.2
Date: Wednesday, May 11, 2016	Sheet 45 of 60		



Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.			
Title	BATT Conn		
Size	Document Number	LA-D707P	Rev 0.2
Date:	Wednesday, May 11, 2016	Sheet 46 of 60	


Protection for reverse input
Vgs = 20V
Vds = 65V
Id = 250mA
2N7002KW_SOT323-3
Need check the SOA for inrush
Rds(on) typ = 35mohm max max Power loss 0.22W for 90W;0.12W for 65W system
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
CSR rating: 1W
VACP-VACN spec < 80.64mV
Isat: 4A
DCR: 27mohm
VF = 0.5V
Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)
VF = 0.37V
Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
7X7X3
Isat: 6.5A
DCR: 30mohm
Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV
Eletro-X
<26> VCIN1_ACOK
EC_SMB_CK1 <26,46>
EC_SMB_DA1 <26,46>
ADP_I <26,45>
Close EC chip
Vin Dectector
Min. Typ Max.
L-->H 17.16V 17.63V 18.12V
H-->L 16.76V 17.22V 17.70V
VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.01
= 2.29 A
Security Classification
Compal Secret Data
Issued Date
2015/10/09
Deciphered Date
2018/10/09
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Compal Electronics, Inc.
Title
CHARGER(BQ24725)
Size
Document Number
Rev
Date: Wednesday, May 11, 2016
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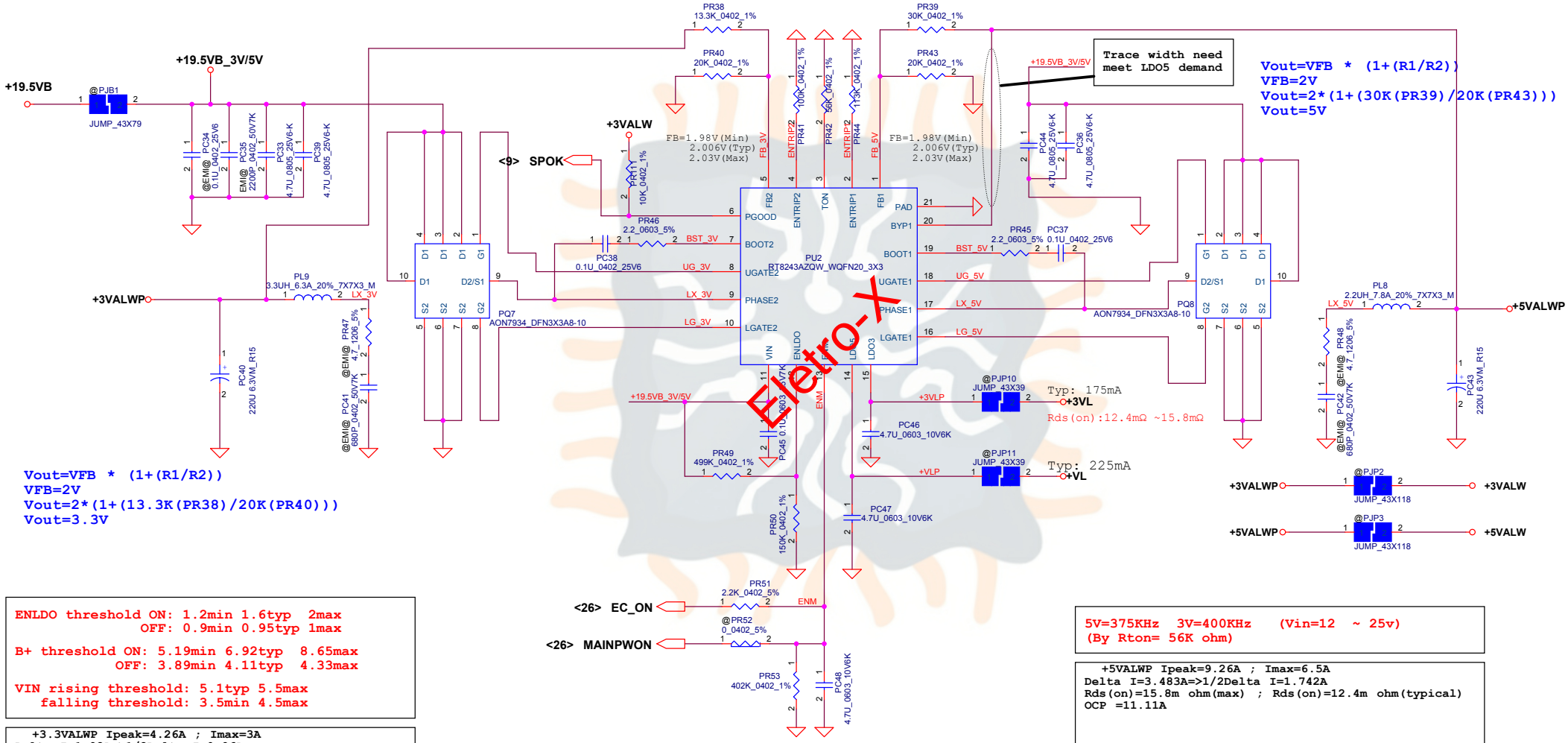
Module model information

RT8243A_V1.mdd

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.92A=>1/2Delta I=0.96A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP = 5.1A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W Δ T:12℃
L-MOS PD:0.2713W Δ T:7.9℃
Choke PD:1.5158W Δ T:23℃
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=3.483A=>1/2Delta I=1.742A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP =11.11A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W Δ T:13.3℃
L-MOS PD:0.3442W Δ T:10℃
Choke PD:1.9613W Δ T:30℃
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-D707P | Rev: 1.0

Date: Wednesday, May 11, 2016 | Sheet 48 of 60

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

+19.5VB

@PJB2 JUMP_43X79

+19.5VB_1.35VP

@EMI@ PC48 220P_0402_50V7K
PC50 10U_0805_25V6K
PC51 10U_0805_25V6K

BST_1.35VP_R

PR54 2.2_0603_5%

BST_1.35VP

+1.2VP

PC52 0.1U_0603_25V7K

UG_1.35VP

LX_1.35VP

+0.6VSP

PC53 10U_0603_6.3V6M
PC54 10U_0603_6.3V6M

LG_1.35VP

+1.2VP

PL11 1UH_11A_20%_7X7X3_M

LX_1.35VP

@EMI@ PR56 4.7_1206_5%

@EMI@ PC64 680P_0402_50V7K

PC56 22U_0603_6.3V6M
PC57 22U_0603_6.3V6M
PC58 22U_0603_6.3V6M
PC59 22U_0603_6.3V6M
PC61 22U_0603_6.3V6M
PC62 22U_0603_6.3V6M

PQ11 AON7934_DFN3X3A8-10

Rds(on):12.4mΩ ~15.8mΩ

PR55 11.5K_0402_1%

CS_1.35VP

PC55 1U_0402_6.3V6K

PR57 5.1_0603_5%

+5VALW

VDD_1.35VP

PC63 1U_0402_6.3V6K

PR65 5.1_0603_5%

@DDR_PWROK PAD

PU3 RT8207PGQW_WQFN20_3X3

LGATE PHASE UGATE BOOT VLDOIN VTT PAD
PGND VTTGND
CS VTTSNS
VDDP GND
VTTREF
VDD VDDQ
PGOOD TON SS S3 FB

VTTREF_1.35VP

+1.2VP

PC60 0.033U_0402_16V7K

PR58 6.04K_0402_1%

+1.2VP

VFB=0.75V

PR60 10K_0402_1%

Vout=Vref * (1+(R1/R2))
Vref=0.75V
Vout=0.75*(1+(6.04K(PR58)/10K(PR60)))
Vout=1.2V

+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)

OCP = 8.88

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp=13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V

2.5V PG Enable 1.2V

+2.5V_PG

@PR1815 0_0402_5%

<12,26,35,49> SYSON

@PR61 0_0402_5%

@PC65 0.1U_0402_10V7K

2014/12/23
change from SUSP# to SM_PG_CTRL

@PR62 0_0402_5%

<12,13,26,35> SUSP#

+1.2VP

@PJP4 JUMP_43X118

+1.2V_VDDQ

@PR63 0_0402_5%

<6> SM_PG_CTRL

@PC66 0.1U_0402_10V7K

+0.6VSP

@PJP5 JUMP_43X39

+0.6V_0.6VS

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information

SY8032_V2.mdd

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

+2.5VP

@PJM5 JUMP_43X39

+2.5V

PCM21 22U_0603_6.3V6M

+3VALW

@PJM4 JUMP_43X39

+3VALW

PUM2 SY8032ABC_SOT23-6

IN LX
PG GND
FB EN

LX_2.5V

PLM3 1UH_2.3A_+-20%_2.5X2X1.2_F

+2.5VP

@PRM27 0_0402_5%

<9,12,26,35> PM_SLP_S4#

PRM21 100K_0402_5%

Enable 1.2V

+2.5V_PG

@PRM24 0_0402_5%

<12,26,35,49> SYSON

EN_2.5V

PRM25 1M_0402_1%

@PCM25 0.1U_0402_16V7K

@EMI@ PRM22 4.7_0402_5%

PRM23 32.4K_0402_1%

Rup

PCM22 68P_0402_50V8J

PCM23 22U_0603_6.3V6M

PCM24 22U_0603_6.3V6M

FB_2.5V

@EMI@ PCM26 680P_0402_50V7K

PRM26 10K_0402_1%

Rdown

Vout=0.6V * (1+(R1/R2))
Vout=0.6*(1+(32.4K(PRM23)/10K(PRM26)))
Vout=2.5V

Imax= 2A, Ipeak= 3A
FB=0.6V

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5VP(RT8207P/SY8032A)

Size: Custom | Document Number | Rev: v0.2

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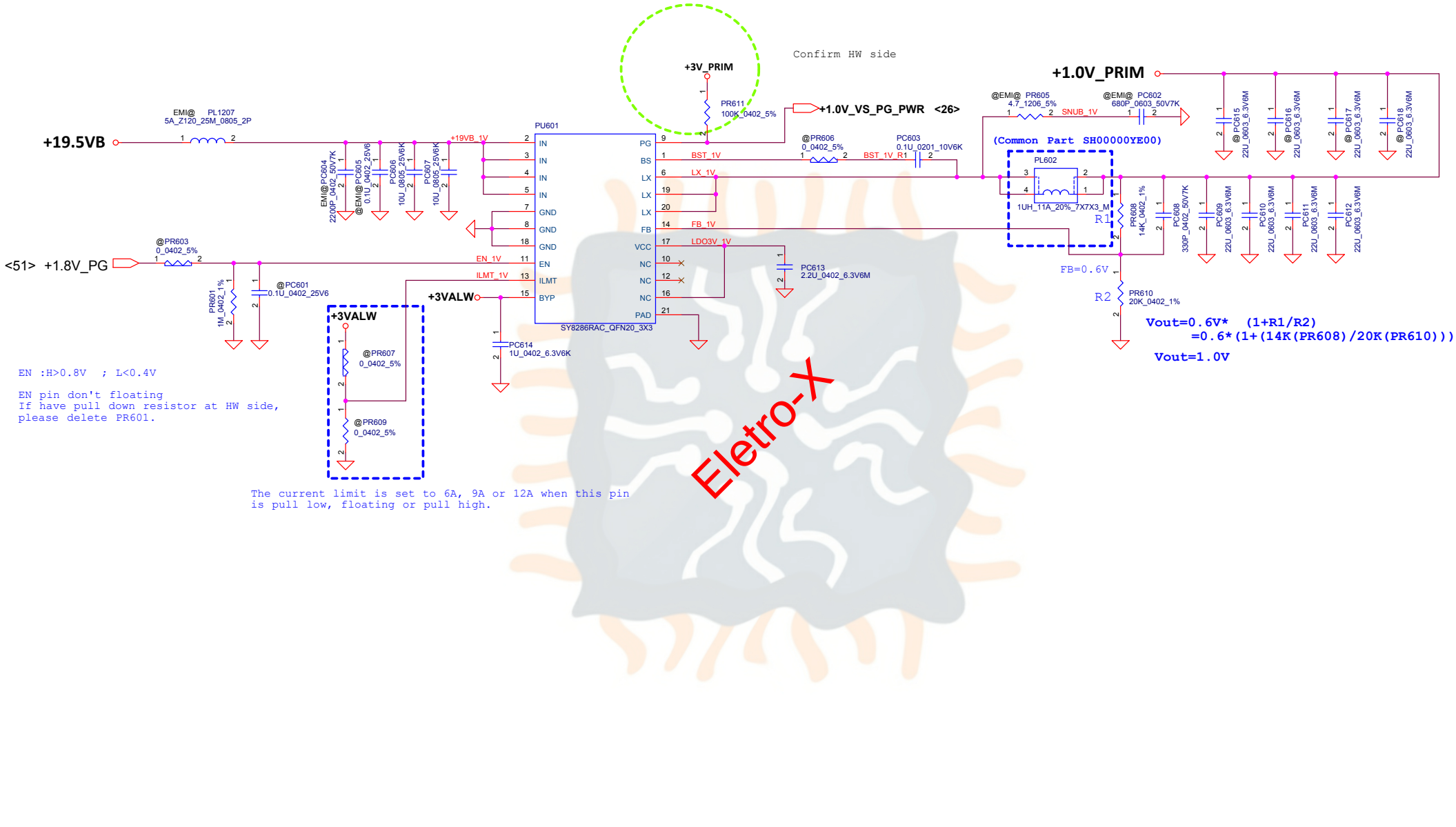
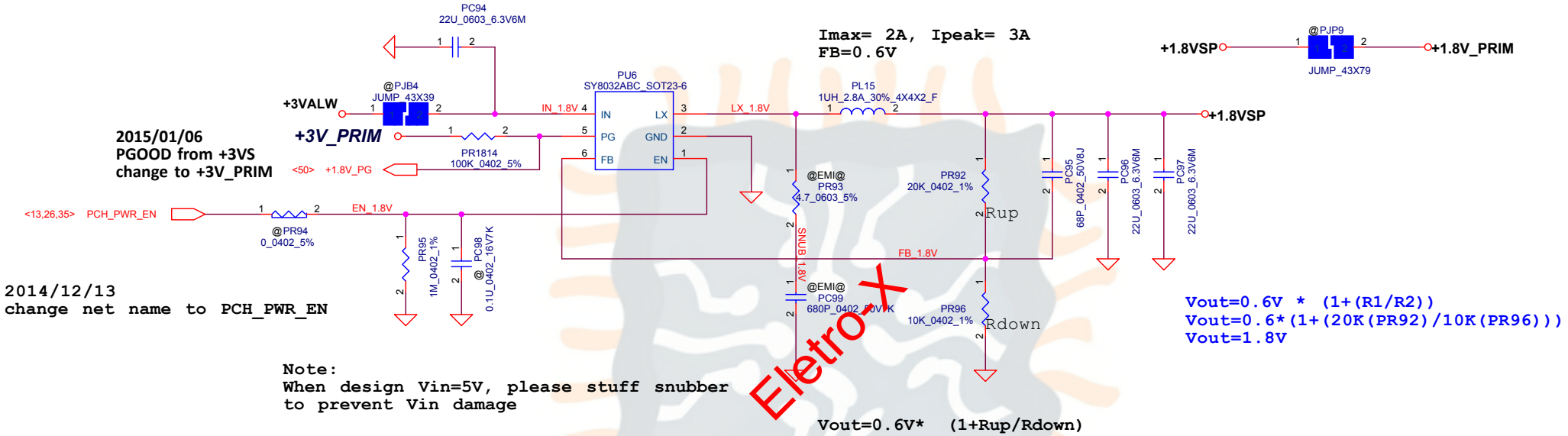


Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Title	1.0VS(SY8286)		
Size	Document Number		Rev
Custom			0B.2
Date:	Wednesday, May 11, 2016	Sheet	50 of 60



2015/01/06
PGOOD from +3VS
change to +3V_PRIM

2014/12/13
change net name to PCH_PWR_EN

Imax= 2A, Ipeak= 3A
FB=0.6V

Vout=0.6V * (1+(R1/R2))
Vout=0.6*(1+(20K(PR92)/10K(PR96)))
Vout=1.8V

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *1.8VS(SY8032A)*

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: | Sheet 51 of 60

PR1101=2*PR1106/(10*IOUTmax*Load line)
U22 Iout@GT=31A
PR1101=25.5kohm

PR1106=Iout limit*Load line/10
U22 OCP@GT=40A
PR1106=12.4kohm

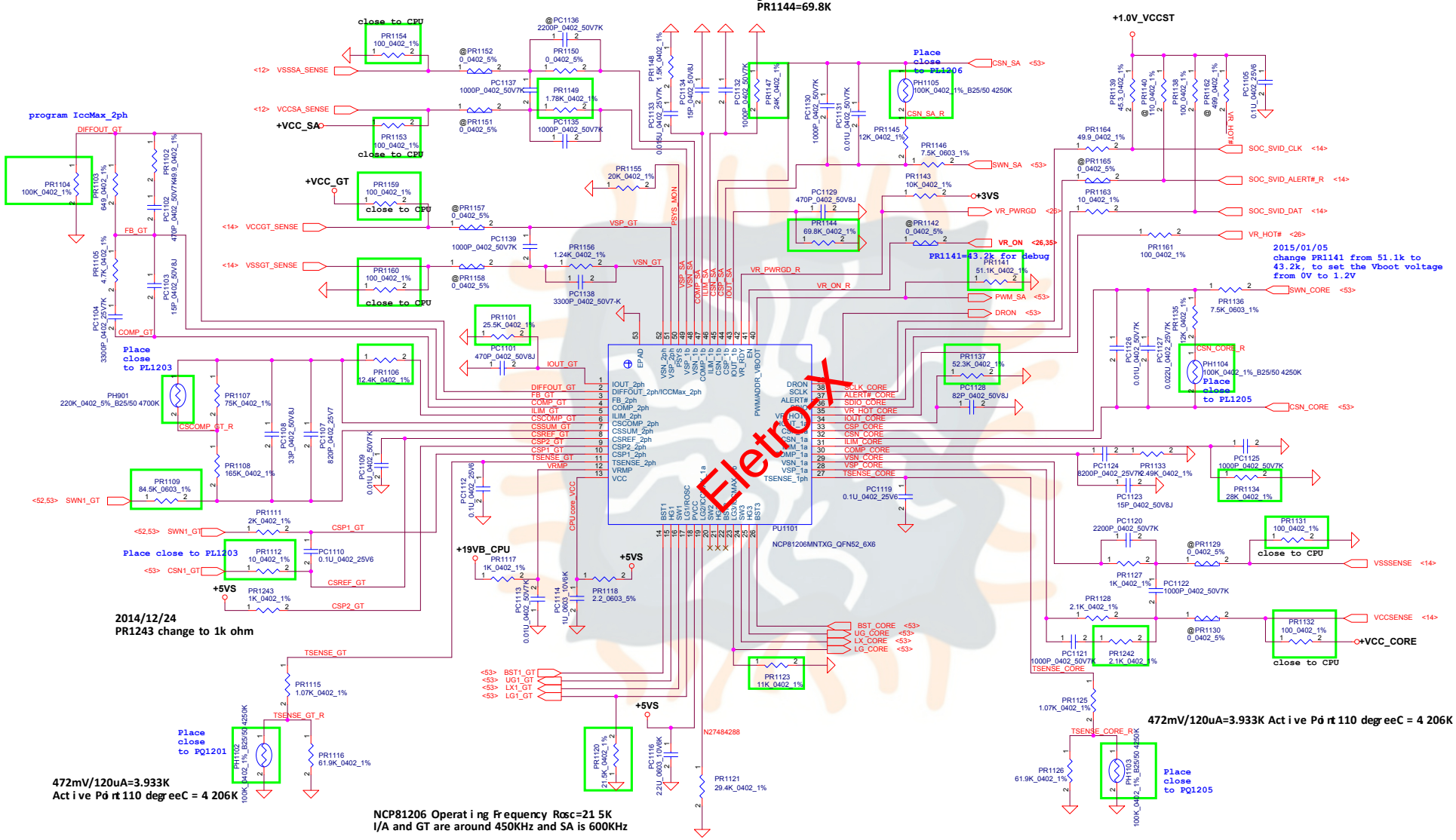
RIccMAX2ph(PR1104)= (IccMAX2Ph+32)*200kohm/ 127
U22 IccMAX@GT= 31A
PR1104= 100K

Load line=(PR1108+(PR1107+PH901/(PR1107*PH901)))*Iout tltal*DCR/PR1109
U22 Load line@GT= 3.1m
PR1109 , PR1110@GT=84.5K

RDRPSP(PR1149)= Load line*(PR1146+PH1105+PR1145)/(gm * DCR) /(PH1105+PR1145)
Load line@SA= 10.3m
gm=1mS
PR1149=1.78K

RLIMSP(PR1147)= 1.3V/(gm*(PH1105+PR1145)*IoutLIMIT*DCR/(PR1146+PH1105+PR1145))
OCP@SA= 9.6A
gm=1mS
PR1147=24K

RIOUTSP(PR1144)= 2V/(gm*(PH1105+PR1145)*ICCMAX*DCR/(PR1146+PH1105+PR1146))
IOUTSP@SA= 5A
gm=1mS
PR1144=69.8K



IccMAX@SA= 5A
PR1123= 11K
Refer IccMAX table in datasheet

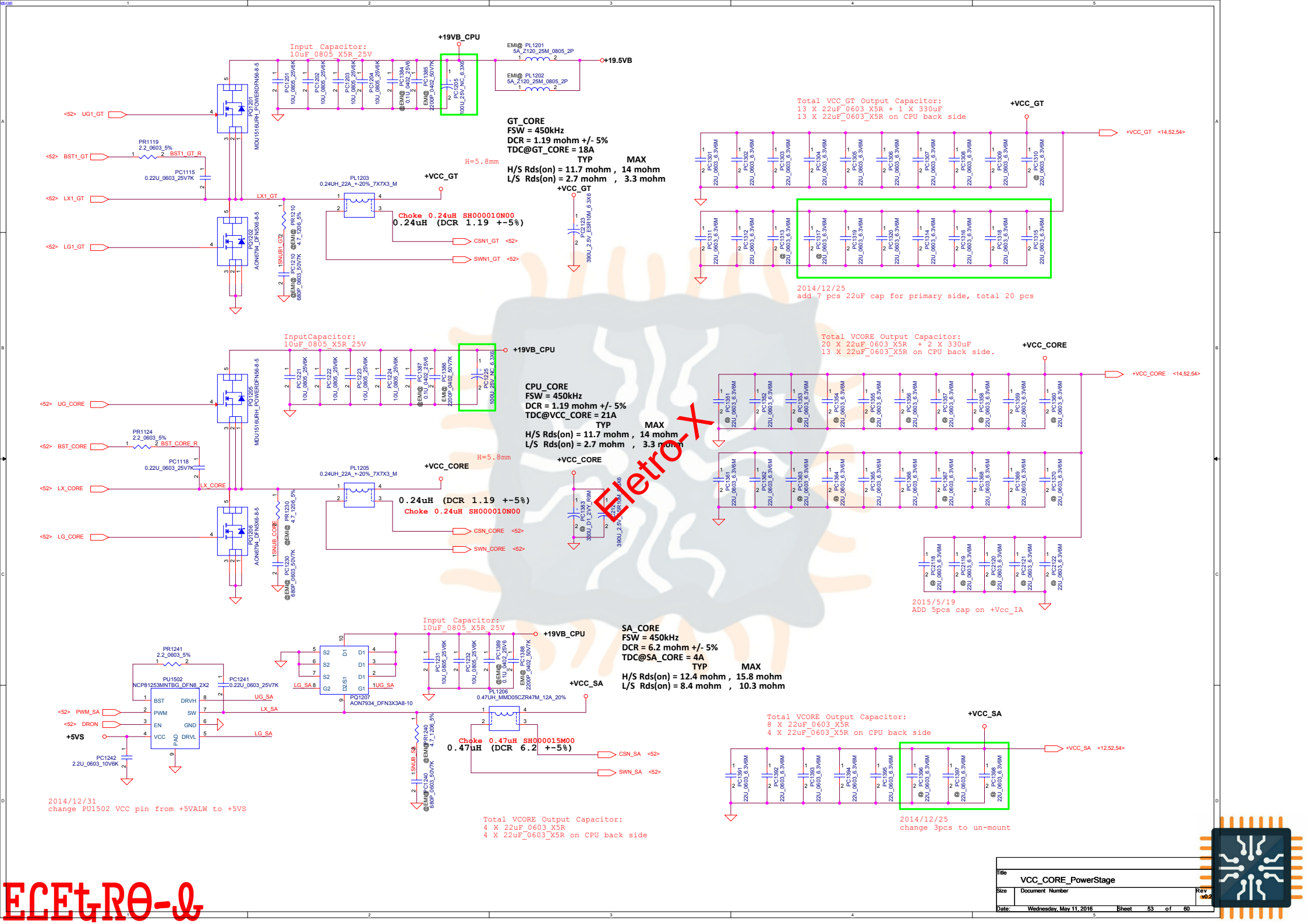
IccMAX@VCORE= 28A
RIccMAX@VCORE= 24.9K
Refer IccMAX table in datasheet

RDRPSP(PR1128)= Load line*(PR1136+PH1104+PR1135)/(gm * DCR) /(PH1104+PR1135)
Load line@VCORE= 2.1m
gm=1mS
PR1128=2.1K

RIOUTSP(PR1137)= 2V/(gm*(PH1104+PR1135)*ICCMAX*DCR/(PR1136+PH1104+PR1135))
IOUTSP@VCORE= 28A
gm=1mS
PR1137=64.9K

RLIMSP(PR1134)= 1.3V/(gm*(PH1104+PR1135)*IoutLIMIT*DCR/(PR1136+PH1104+PR1135))
OCP@VCORE= 35A
gm=1mS
PR1134=33.2K

Title	VCC_CORE_U22(NCP81206)		
Size	Document Number		Rev v0.2
Date:	Wednesday, May 11, 2016	Sheet 52 of 60	



VCC_CORE Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*12 pcs

2014/12/25
add 1 pcs 1uF cap for back side, total 13 pcs

+VCC_CORE

+VCC_GT

20150324
add 6 pcs cap for transient test

VCC_SA Place on CPU Back Side.
22U_0603 * 4 pcs + 1U_0201 * 7 pcs

+VCC_SA

+VCC_SA

Eletro-X

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: VCC_CORE_PROCESSOR DECOUPLING

Size: | Document Number: LA-D707P | Rev: v0.2

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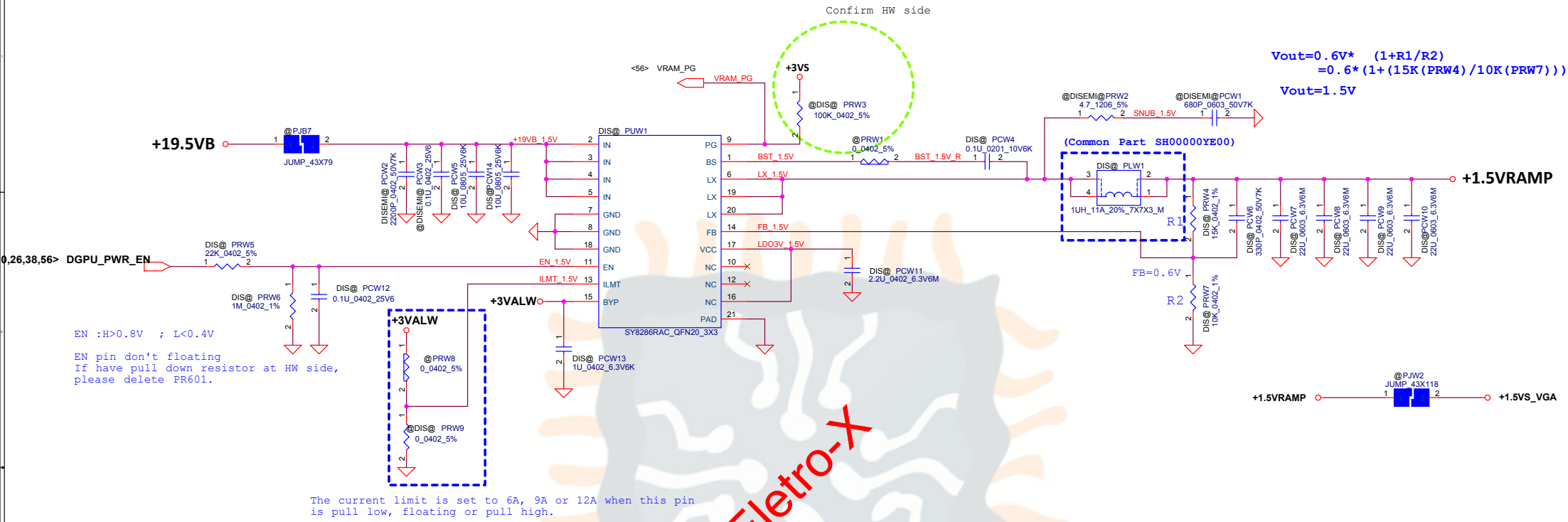

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.	
Title	*1.5VS_VGA(SY8286)*
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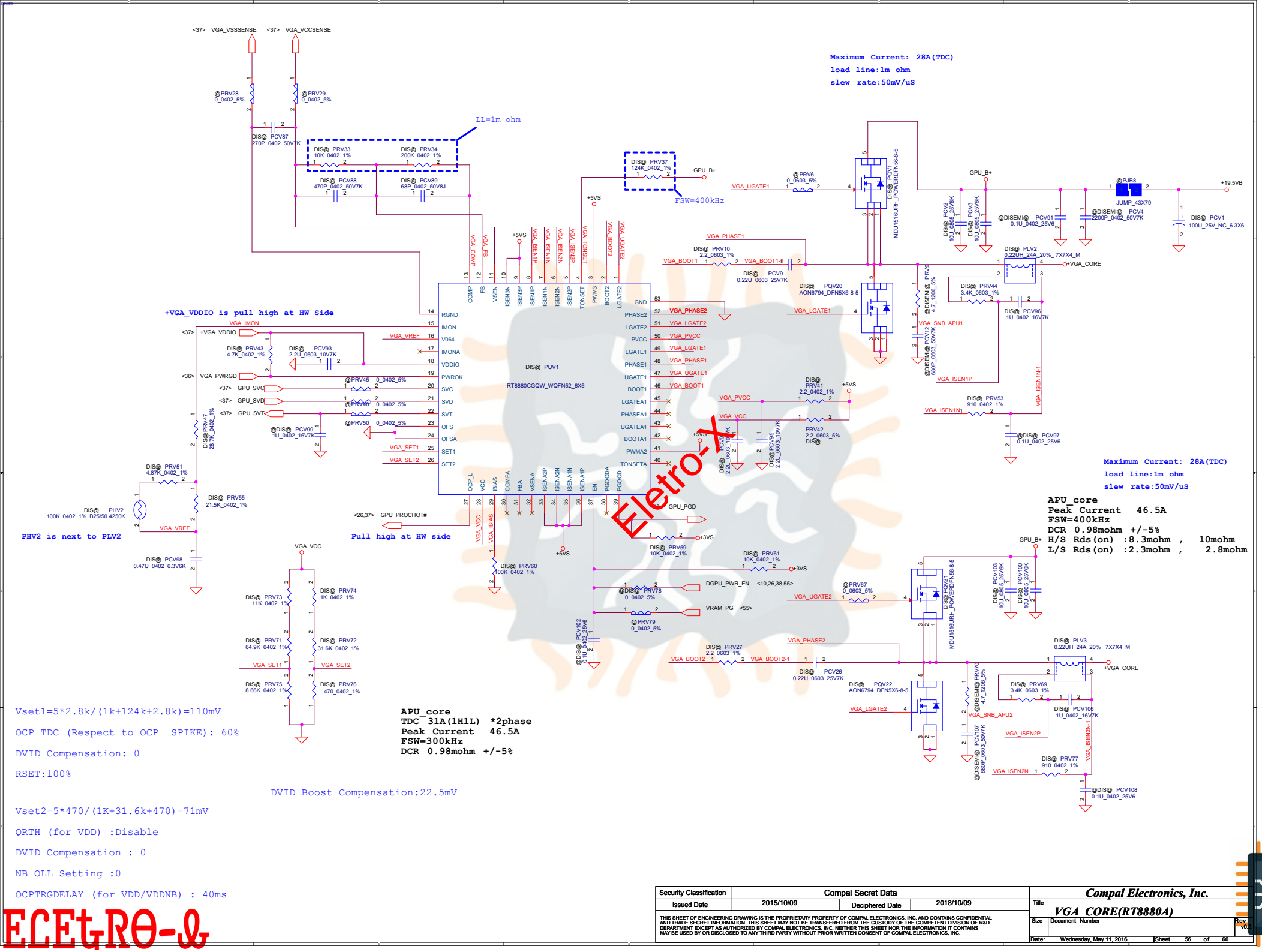
Maximum Current: 28A(TDC)
load line:1m ohm
slew rate:50mV/uS
LL=1m ohm
FSW=400kHz
+VGA_VDDIO is pull high at HW Side
PHV2 is next to PLV2
Pull high at HW side
APU_core
Peak Current 46.5A
FSW=400kHz
DCR 0.98mohm +/-5%
H/S Rds(on) :8.3mohm , 10mohm
L/S Rds(on) :2.3mohm , 2.8mohm
APU_core
TDC 31A(1H1L) *2phase
Peak Current 46.5A
FSW=300kHz
DCR 0.98mohm +/-5%
Vset1=5*2.8k/(1k+124k+2.8k)=110mV
OCP_TDC (Respect to OCP_ SPIKE): 60%
DVID Compensation: 0
RSET:100%
DVID Boost Compensation:22.5mV
Vset2=5*470/(1K+31.6k+470)=71mV
QRTH (for VDD) :Disable
DVID Compensation : 0
NB OLL Setting :0
OCPTRGDELAY (for VDD/VDDNB) : 40ms
RT8880CGQW_WQFN52_6X6
MDU1516URH_POWERDFN56-8-5
AON6794_DFN5X6-8-5
JUMP_43X79
Security Classification
Compal Secret Data
Issued Date
2015/10/09
Deciphered Date
2018/10/09
Compal Electronics, Inc.
VGA_CORE(RT8880A)
Wednesday, May 11, 2016
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Eletro-X
ECEtRO-L

SKL_SI

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	Change Value	11/06	Power	(Set VR prochot# from 110C to 120C)	Change PR1115 and PR1125 Value 0 ohm to 1.07K ohm	
2	50	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PL602 part number from SH00000Z200 to SH00000YE00	
3	55	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PLW1 part number from SH00000Z200 to SH00000YE00	
4	48	Add Jump	11/18	Power	For easy debug	+3VL and +VL add Jump	
5	55	Add Net	11/18	EE	For VGA CORE sequence and VID error issue	Delete PG pin test point VRAM_PG Add Net VRAM_PG	
6	56	pop to unpop unpop to pop	11/18	EE	For VGA CORE sequence and VID error issue	PRV61 from unpop to pop PRV78 and PCV102 from pop to unpop	
7	56	Add Net and R	11/18	EE	For VGA CORE sequence and VID error issue	Add Net VRAM_PG Add PRV79	
8	47	Change jump to ISN choke	11/24	EMI	EMI ISN issue	Delete jump PJB9 Add ISN choke PL201	
9	48	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL7	
10	49	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL10	
11	50	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB3 Add Bead PL1207	
12	53	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB5 Add Bead PL1201 PL1202	
13	55	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1208	
14	56	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1209 and PL1210	
15	55	Change R Value Change C unpop to pop	11/24	EE	HW fi net une VRA Mpo wer sequence	Change PRW5 value from 0 ohm to 22K ohm Change PCW12 from unpop to pop (VGA sequence)	
16	53	Change Common part	11/6	Power	(Change to Common part)	Change PC1331 PC1383 PC1390 from SGA20331E10 to SGA00009S00	

SKL_PV

Item	Page	Title	Change Description	Date
1	56	Modify VGA_CORE OCP	1.Change PRV73 Value 1K ohm to 11K ohm 2.Change PRV71 Value 124K ohm to 64.9K ohm 3.Change PRV75 Value 2.8K ohm to 8.66K ohm	2015-12-12
2	47	space saving	Change PC221 0603 to 0402 size	2015-12-12
3	47,49,50,51,52,56	Change 0 ohm to short pad	Change PR63,PR94,PR215,PR603,PR1129,PR1130,PR1142,PR1151,PR1152,PR1157,PR1158,PR1165,PR1815,PRM27,PRV45,PRV48,PRV50,PRV79,PRV6,PRV67 from 0 ohm to short pad	2016-1-4
4	48,49,55,56	Delete Jump or Bead(Co-lay)	Delete Co-Lay Bead PL7,PL10,PL1208,PL1209,PL1210	2016-1-7
5	53	Delete VCC_GT,VCC_CORE Co-Lay caps	Delete Location PC1331 Footprint,PC2123 from unpop to pop Delete Location PC1390 Footprint,PC2124 from unpop to pop	2015-12-12
6	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800	2015-12-12
7	52,53,54	CPU transient request	Change PC1353,PC1363,PC1355,PC1356,PC1357,PC1354,PC1364,PC1358,PC1351,PC1370,PC1360,PC2010,PC2013,PC2011,PC1367 from pop to unpop Change PC1107 from 1000P to 820P PC1108 from 390P to 33P,PC1108 from unpop to pop PC1104 from 2200P to 3300P PR1103 from 1K to 649	2015-12-12
8	50	1V OVP issue (HW Low switch second source issue)	Delete jump PJ601 and add output MLCC PC615,PC616,PC617,PC618 PR607 from unpop to pop	2016-1-7

Title	Power_PIR(SI)	
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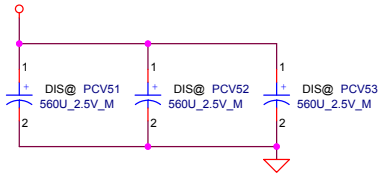
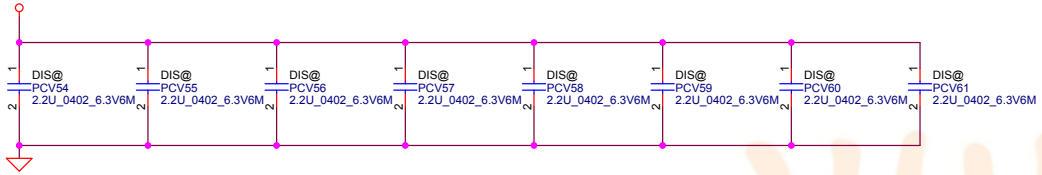
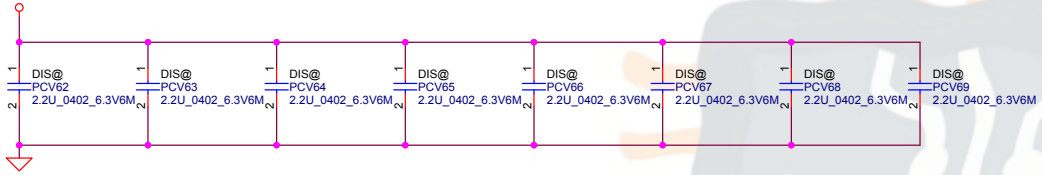
+VGA_CORE



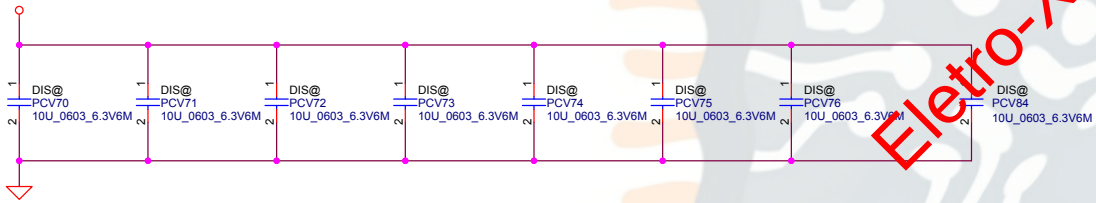
+VGA_CORE



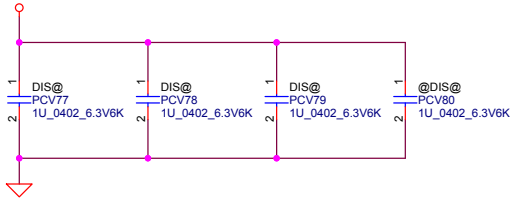
+VGA_CORE



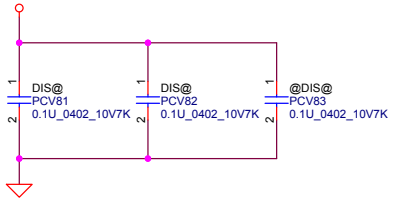
+VGA_CORE



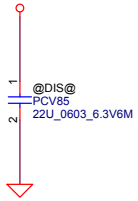
+VGA_CORE



+VGA_CORE



+VGA_CORE



560u X 3
2.2u X 16
10u X 8
1u X 3
0.1u X 2

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title	*VGA_CORE_CHIP DECOUPLING*		
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P. I. R. List

KBL_SI

Item	Page	Title	Change Description	Date
1	50,55	Change 0 ohm to short pad	Change PR607,PRV28,PRV29 from 0 ohm to short pad PRW8 from unpop to pop , change PRW8 from 0 ohm to short pad	2016-2-19
2	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000S800 to SB00000JZ00(Change to Main source)	2016-2-19
3	54	Add IA_Core Output capacitor	Add IA_Core Output capacitor 0603 22uF(PC2014) for IccMAX=32A	2016-2-24

KBL_PV

Item	Page	Title	Change Description	Date
1	47	ADP_I resistance	Change PR223 from short pad to 0 ohm	2016-4-28
2	52	ICCmax from 29A to 32A	Change PR1121 from 20.5K to 29.4K Change PR1137 from 61.9K to 52.3K Change PR1134 from 33.2K to 28K	2016-4-28
3	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800(Change to 2nd source)	2016-4-28
4	49	Add 2nd source	Change PU3 from RT8207P (SA00007IH00) to G5616B (SA0008PH00)	2016-4-28
5	48	Add 2nd source	Change PU2 from RT8243A(SA00005VH00) to UP1590PQKF(SA0007DS00)	2016-4-28

Title	Power_PIR(PV)		
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