Wistron-KBLU Schematics

BA30

REV : -3

DY : None Installed

per MP

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Title: Cover Page

Size: A3 | Document Number: Mihawk MB | Rev: -3

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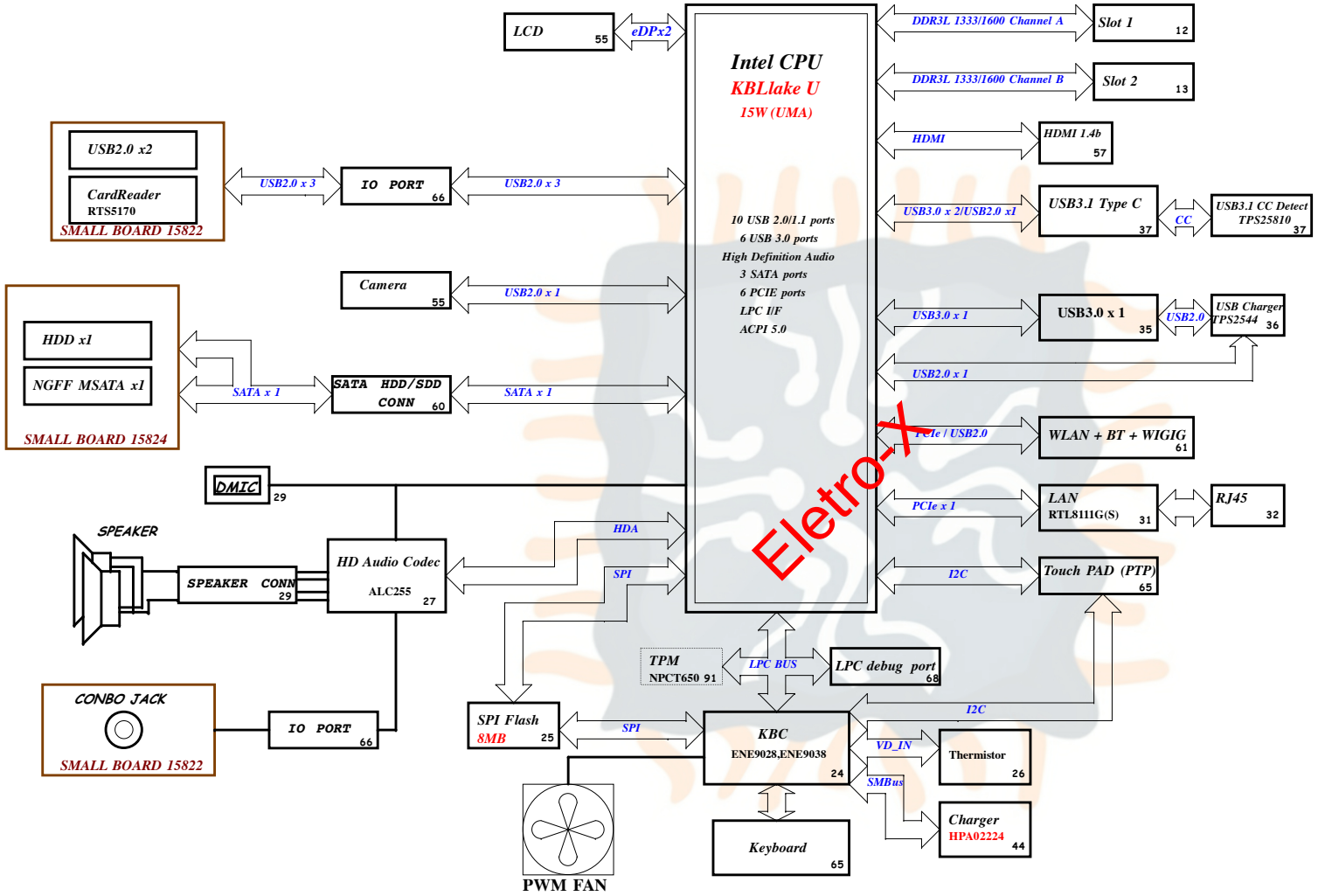
Project code:
Mihawk SL 13 --> 4PD06J010001
PCB P/N:15208
Revision: -1



CHARGER HPA02224	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6575D	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power ISL95857HRTZ-T-GP	46
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS RT8231AGQW-GP	51
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU 1D0V_S5 RT8231AGQW-GP	52
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

CPU 1.8V_S5 RT8068AZQWID-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5

Switches	40
INPUTS	OUTPUTS
1D0V_S5	1D0V_EOPIO_EDRAM
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D0V_S5	1V_VCCIO
	1V_VCCST

PCB LAYER

8-1.0-16d

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Signal
L7:GND
L8:Bottom

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Title: Block Diagram

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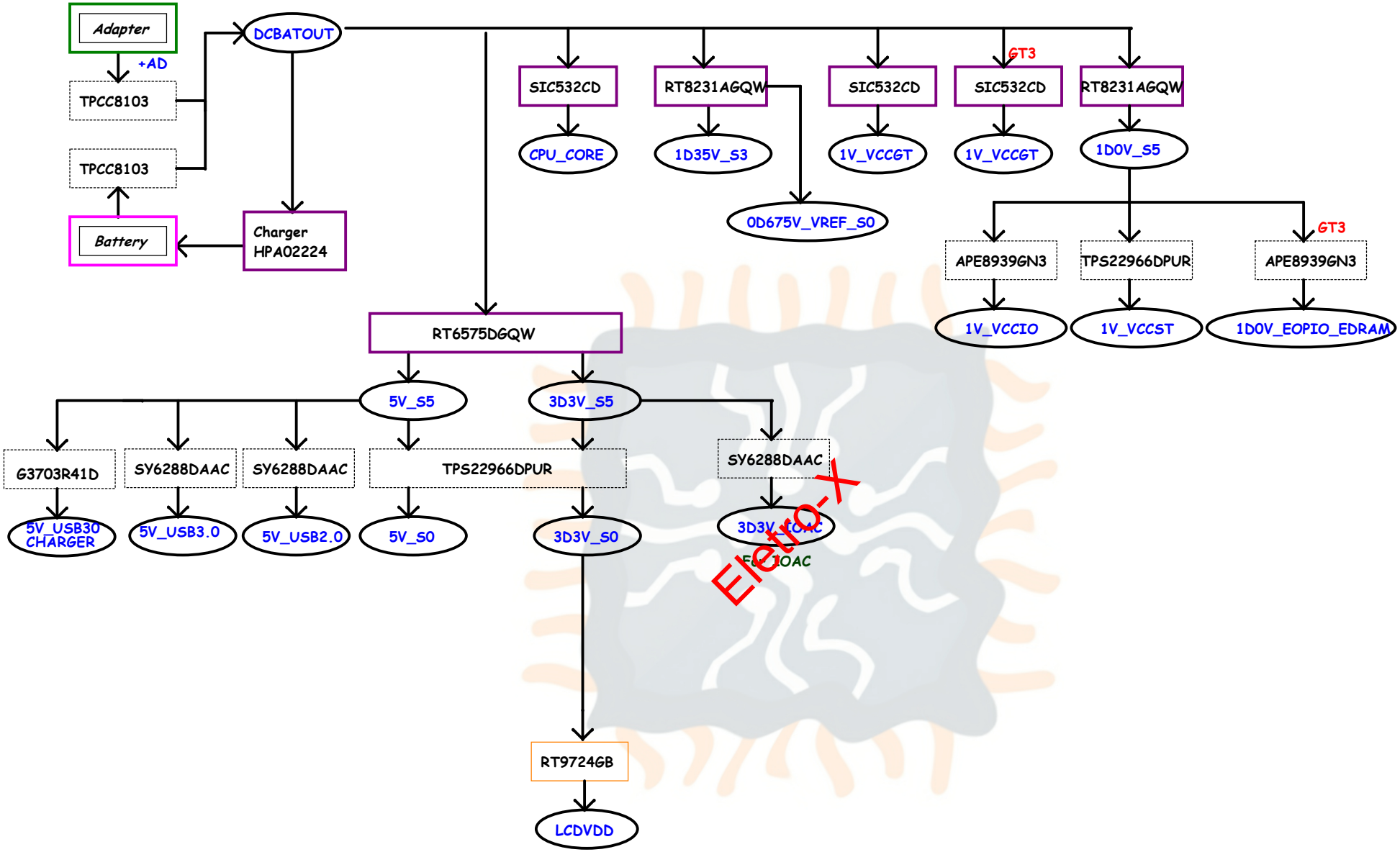

Power Shape

Regulator | LDO | Switch

per MP

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Title: Power Block Diagram

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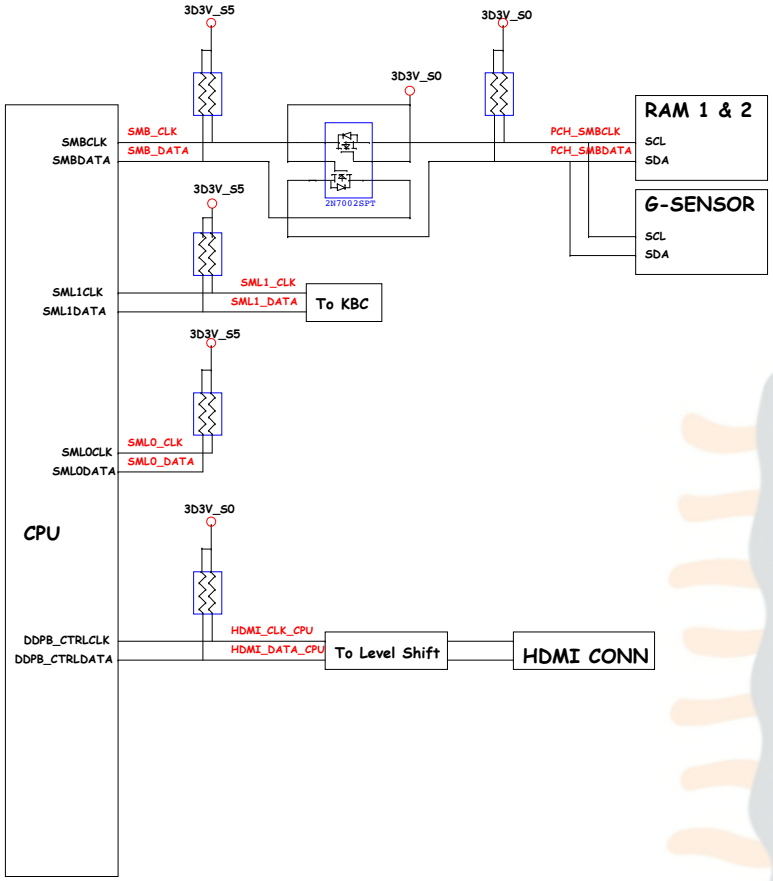
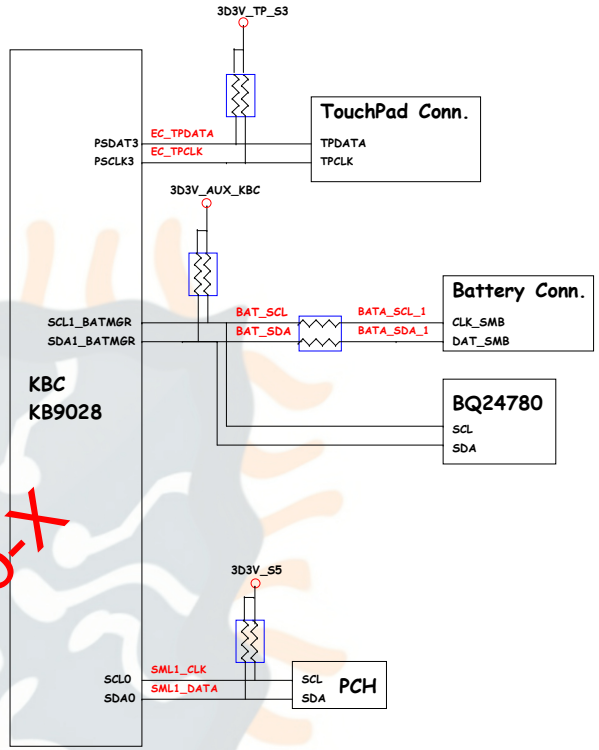
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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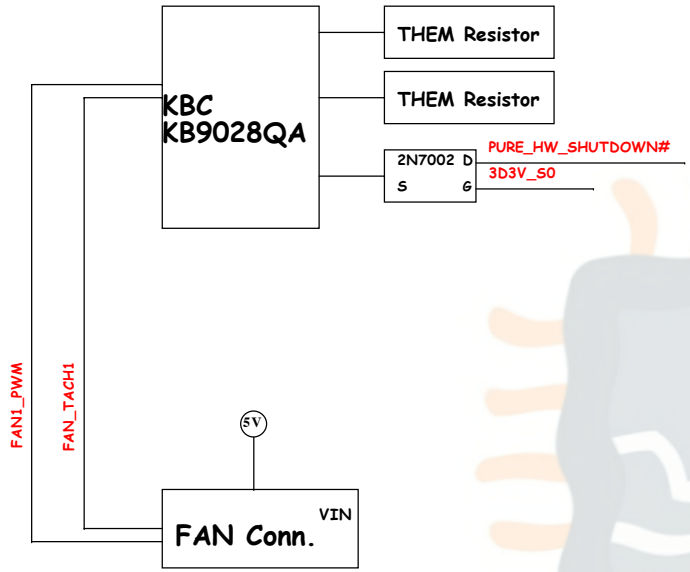
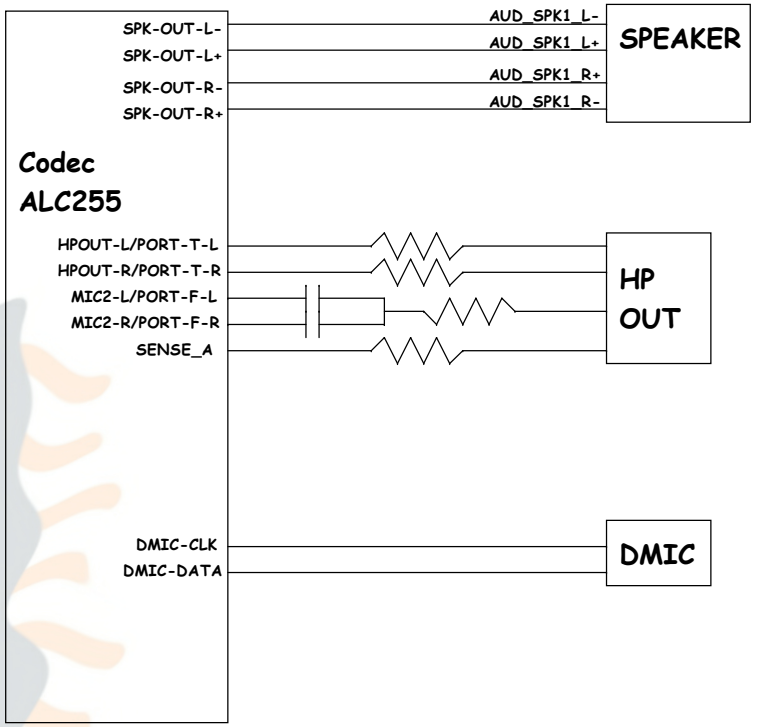
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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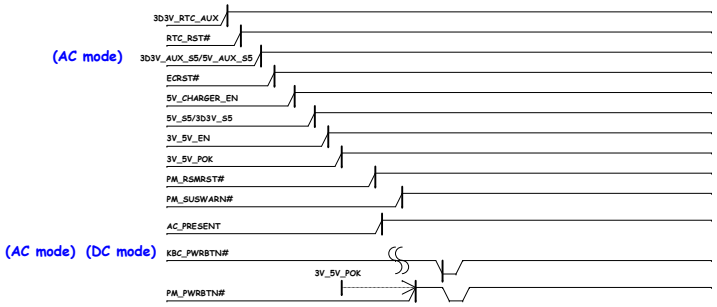
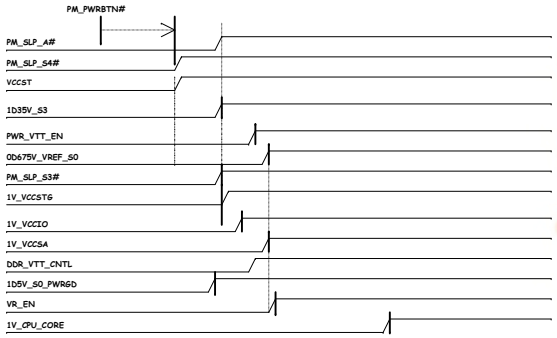
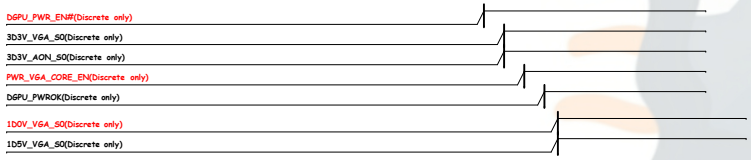
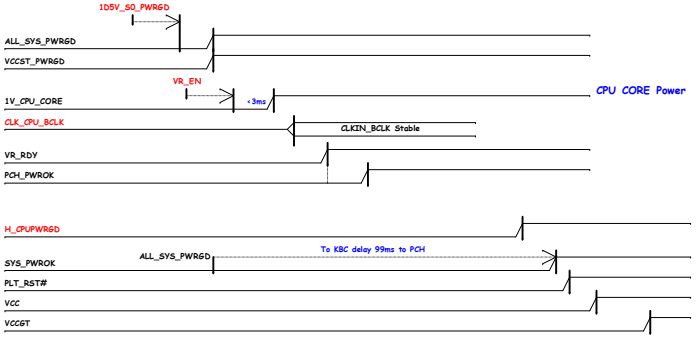
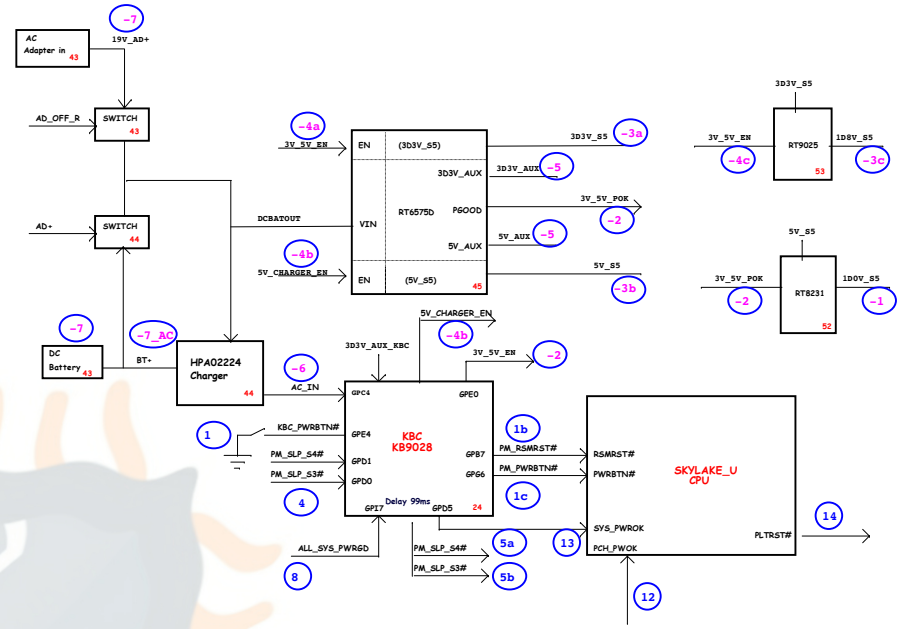
Intel-Power Up Sequence

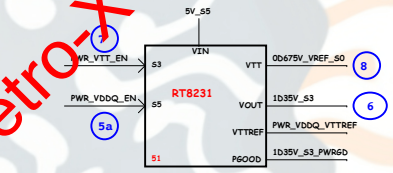


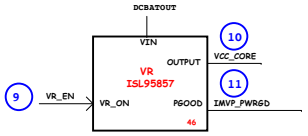


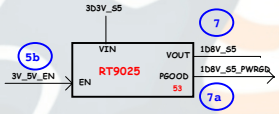


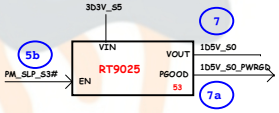


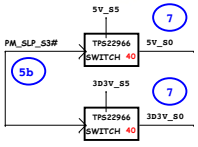






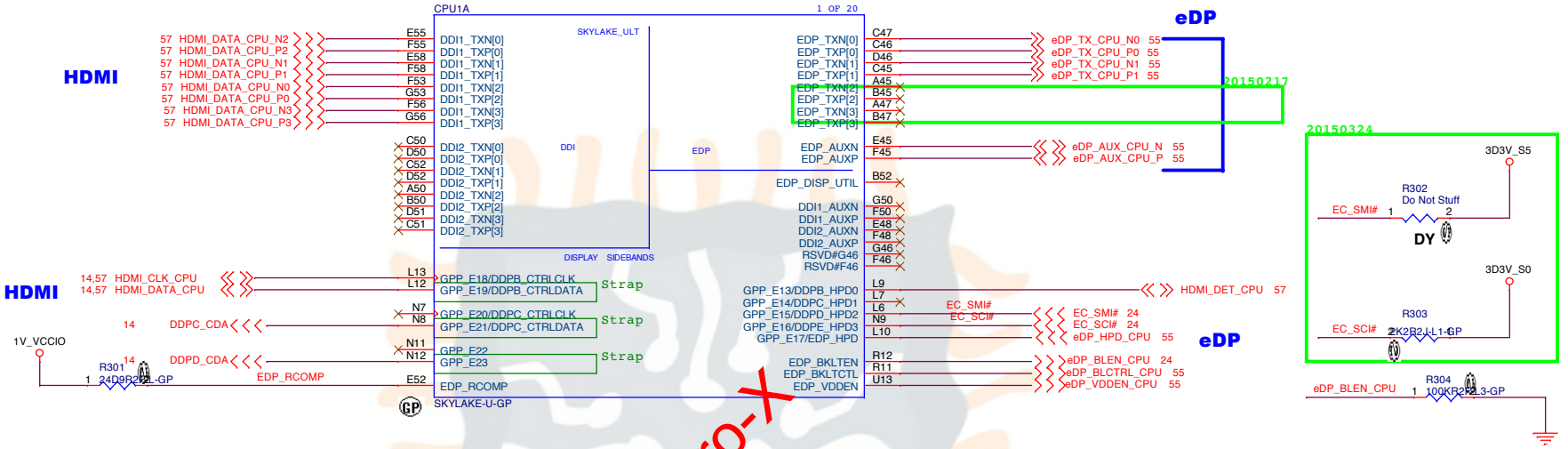






Wistron Corporation
緯創資通
Power Sequence
Mihawk MB
-3

Main Func = CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor.

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Title	CPU_(DISPLAY)
Size A3	Document Number: Mihawk MB
Rev	-3
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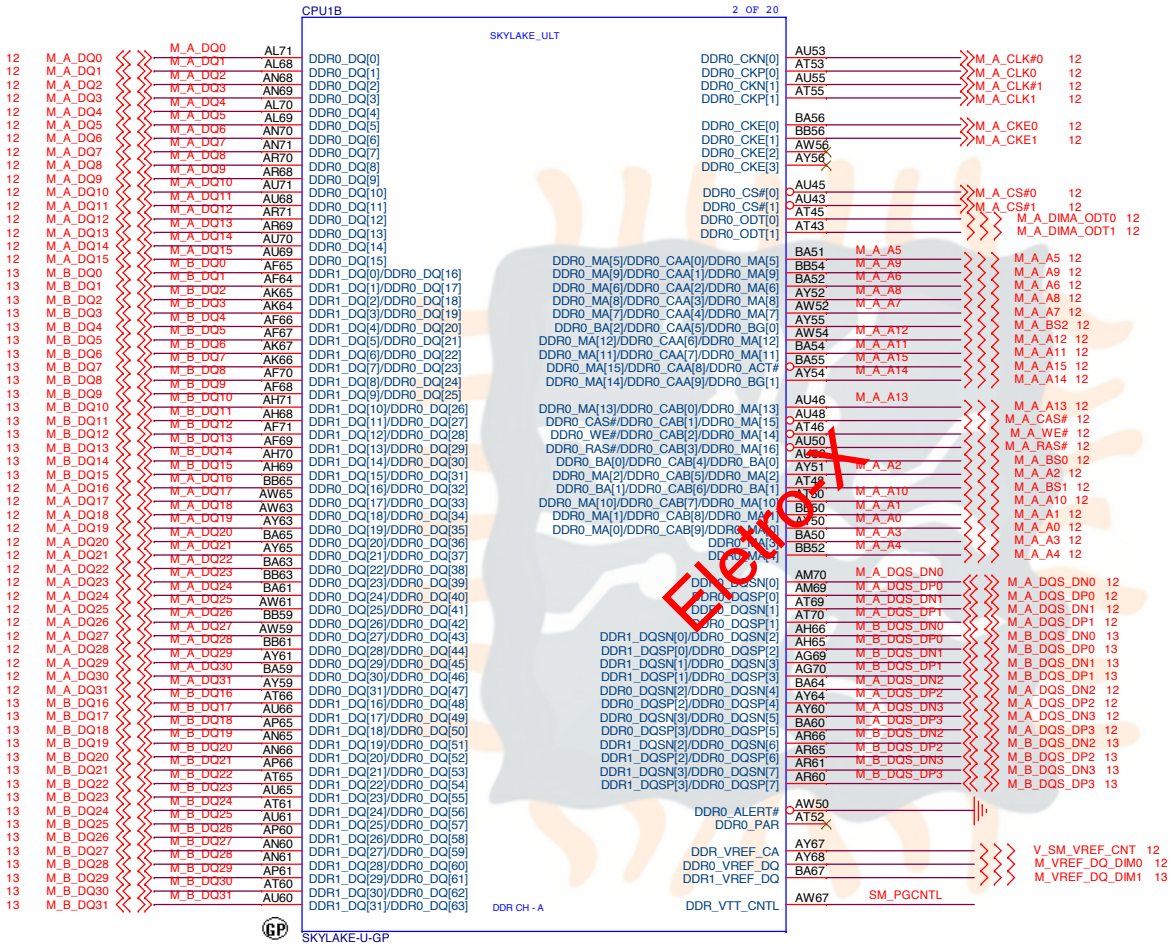
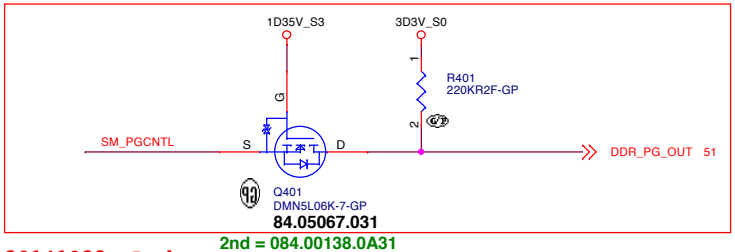
Main Func = CPU

DDR3L ball type: Interleaved Type





20141023 Jack

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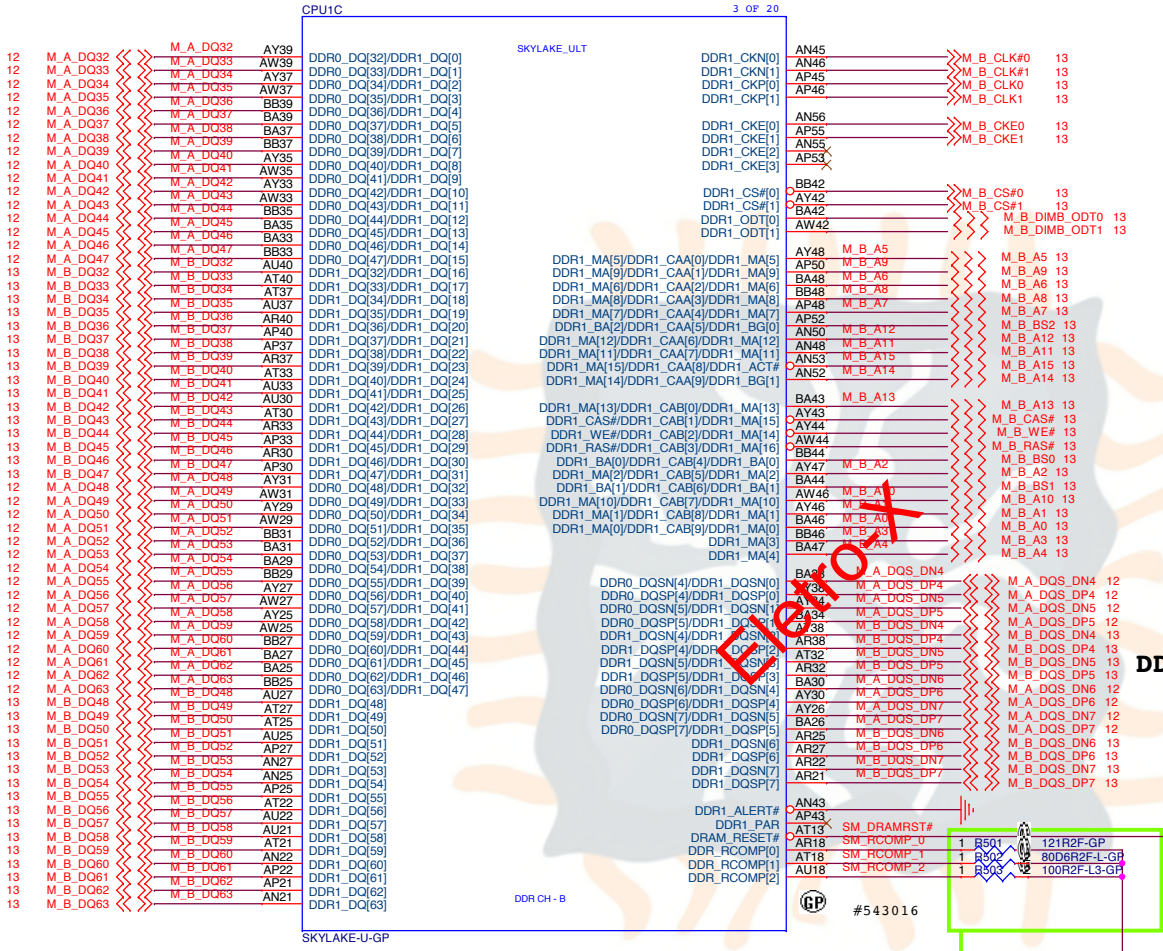
Title	CPU_(DDR)	
Size A3	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017	Sheet 4 of 105	

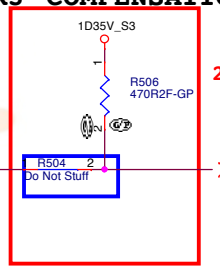
ECEtGR0-L

Main Func = CPU



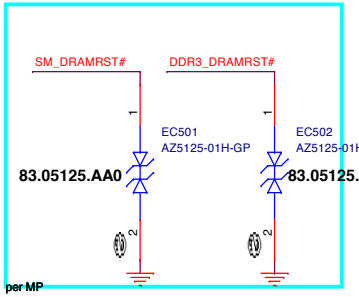
Pending

DDR3 COMPENSATION AND RESET SIGNALS



20140922

20150528 PD



Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

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Title	CPU_(DDR)
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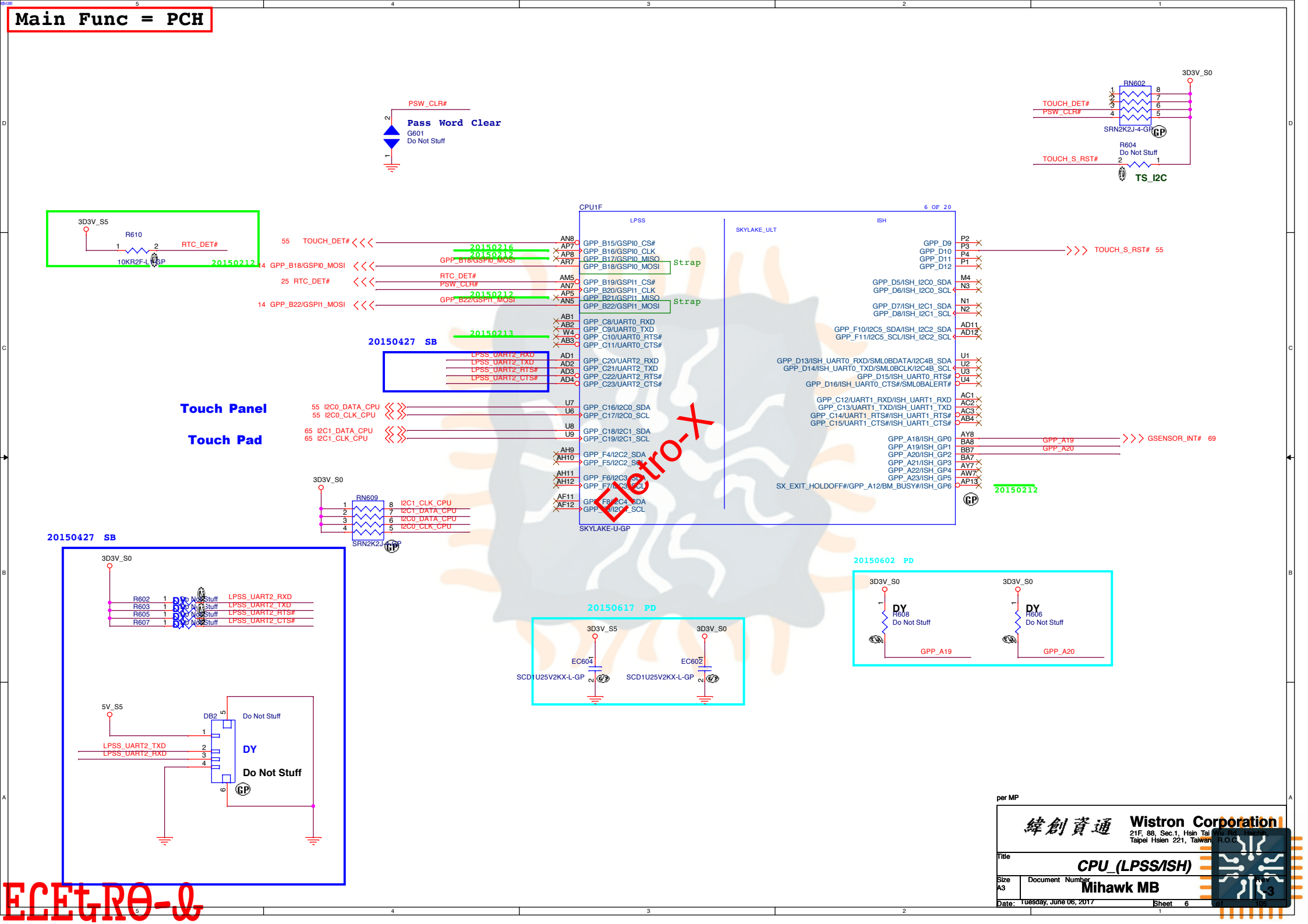
ECEtRO-L

Main Func = PCH



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Title	CPU_(LPSS/ISH)	
Size A3	Document Number Mihawk MB	Rev -3
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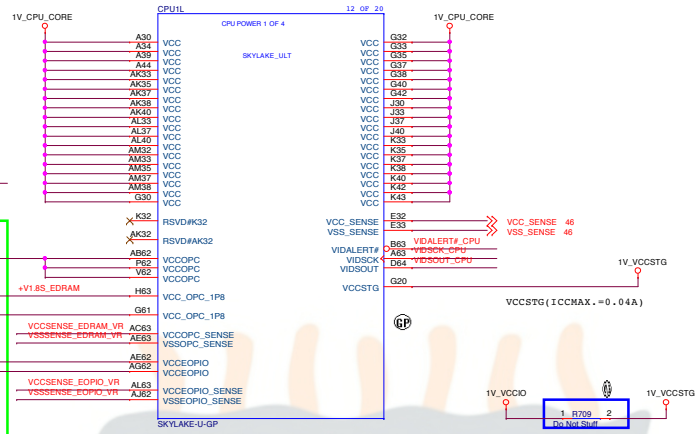
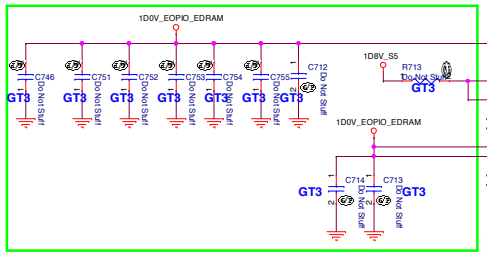
ECE-GR0-L

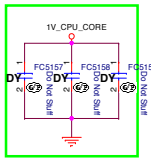
Main Func = CPU



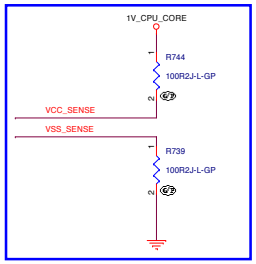
20150320



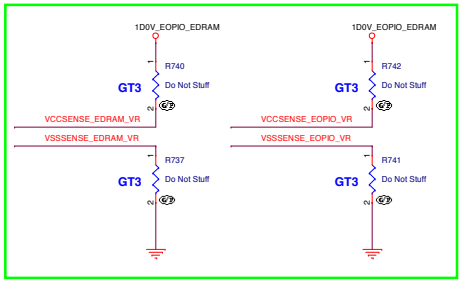
20150322

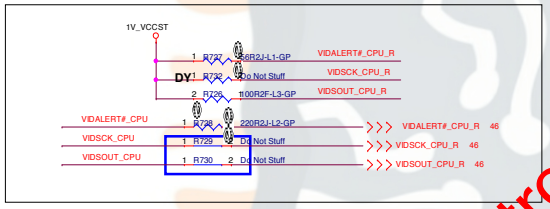


20150505 SB



20150319





CLOSE CPU

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

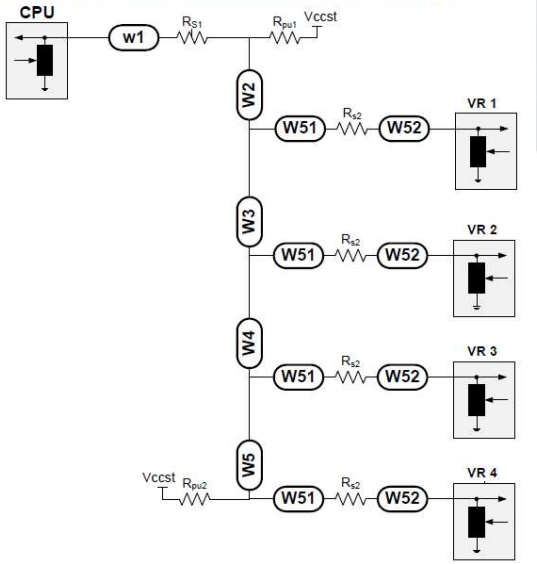


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{BT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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Title: CPU_POWER1

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

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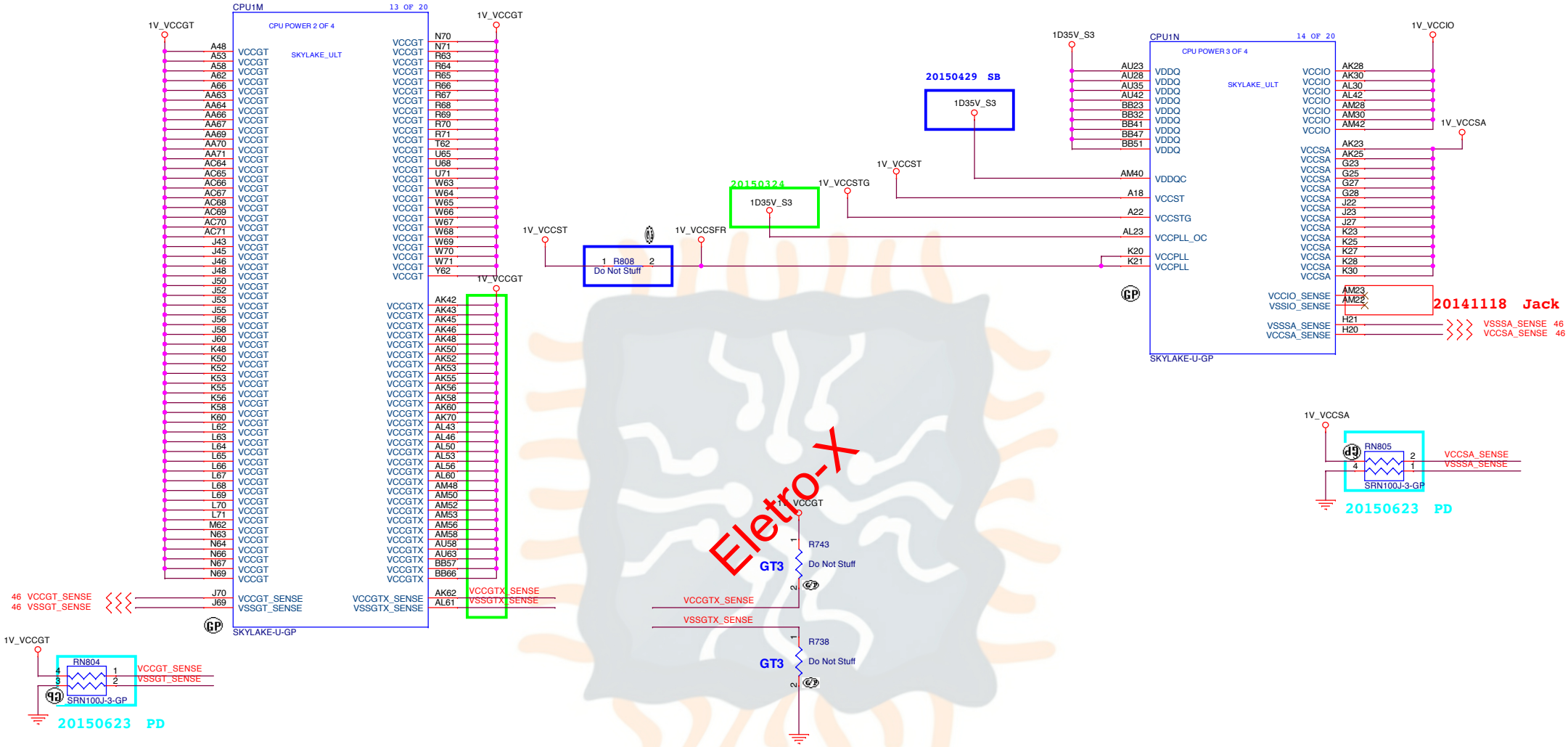
Main Func = CPU



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Title	CPU_POWER1
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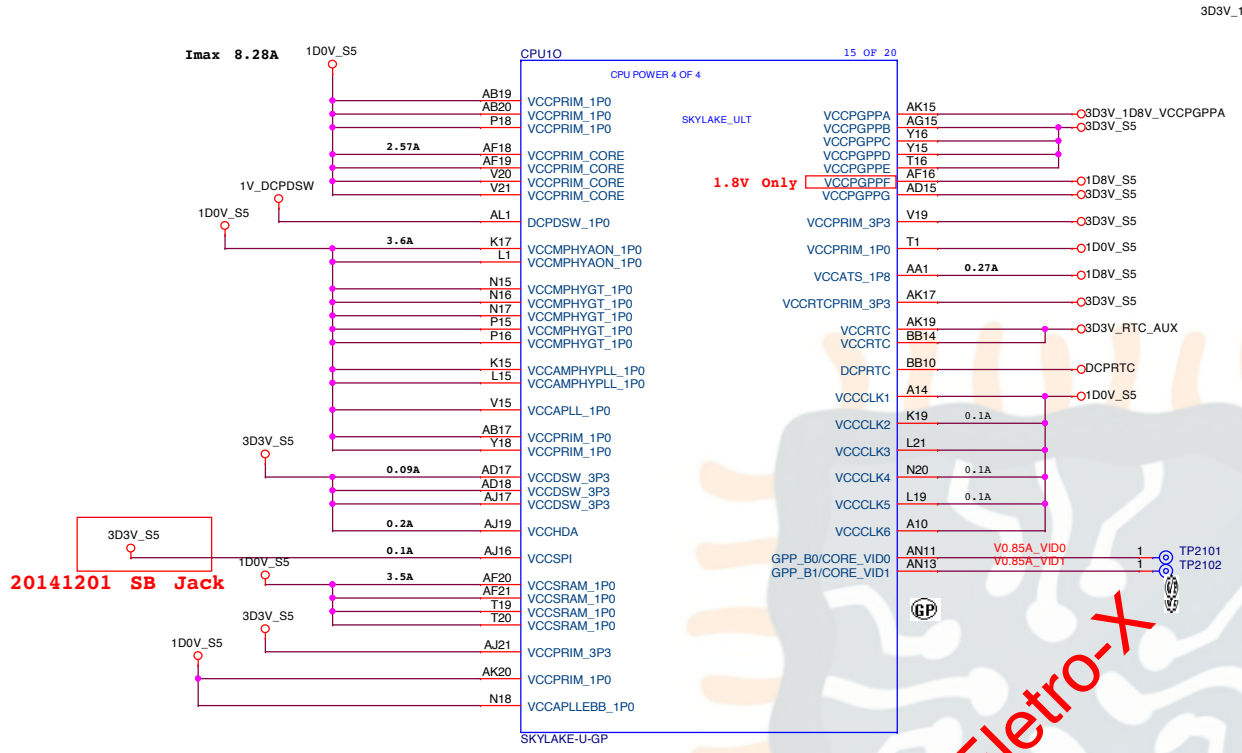
Main Func = PCH



eSPI_508740:

Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM L0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

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Title	CPU_(POWER1)	
Size A3	Document Number Mihawk MB	Rev -3
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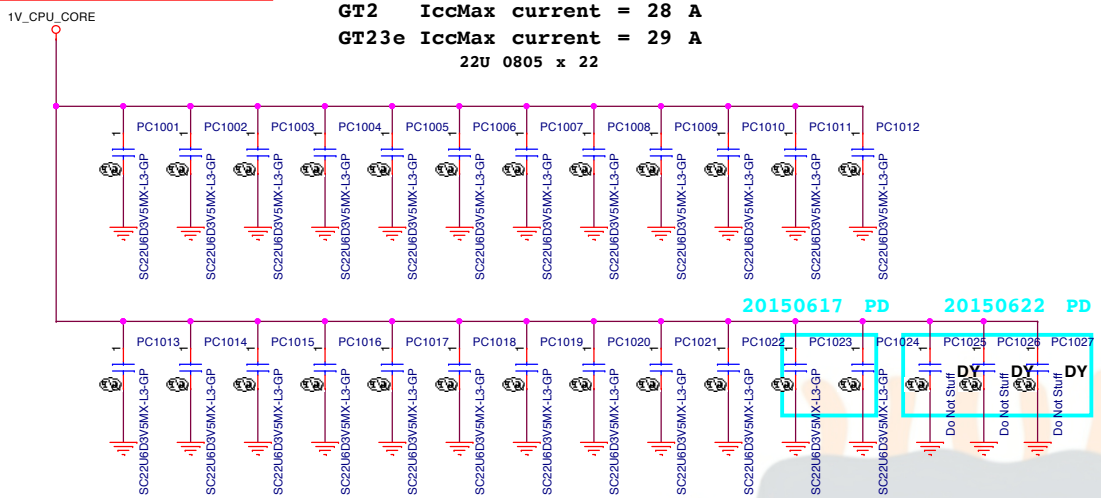
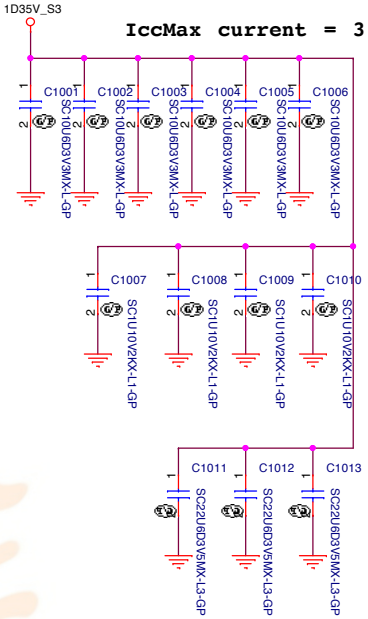
Main Func = CPU

GT2 IccMax current = 28 A
GT23e IccMax current = 29 A
22U 0805 x 22

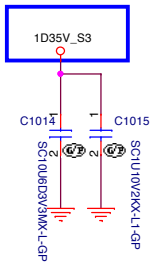




U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	10X22uF
								0r	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								0r	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

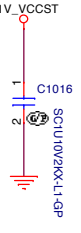
V_{DDQ}	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)		
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible

20150429 SB



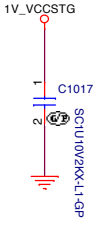
CLOSE CPU AM40

IccMax = 0.04 A



CLOSE CPU A18

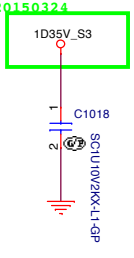
IccMax = 0.04 A



CLOSE CPU A22

IccMax = 0.26 A

20150324



CLOSE CPU AL23

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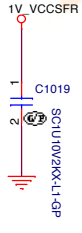
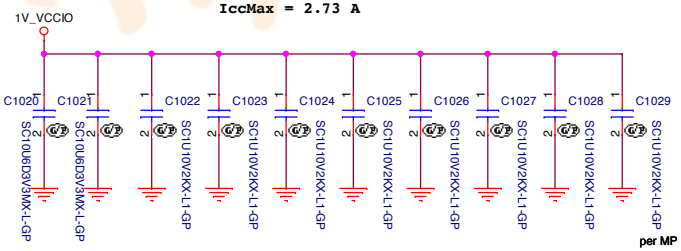


CLOSE CPU K20,K21

IccMax = 2.73 A



per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

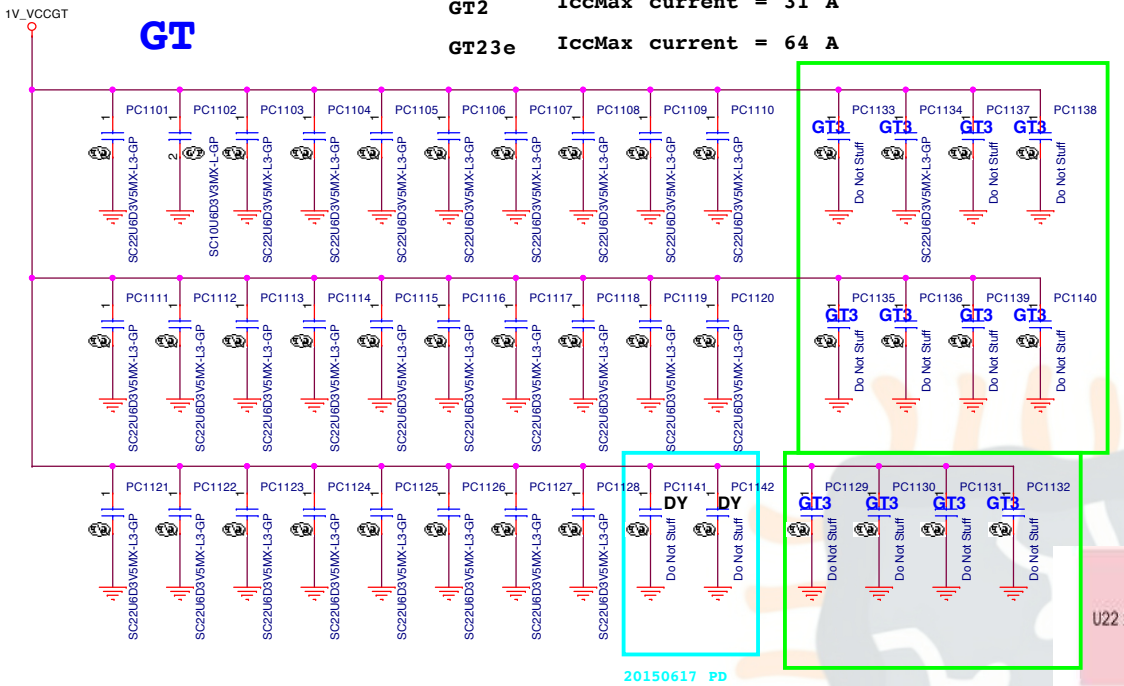
Title: CPU_(Power CAP1)
Size: A3 | Document Number: Mihawk MB | Rev: -3
Date: Tuesday, June 06, 2017 | Sheet 10 of 105

Main Func = CPU

GT

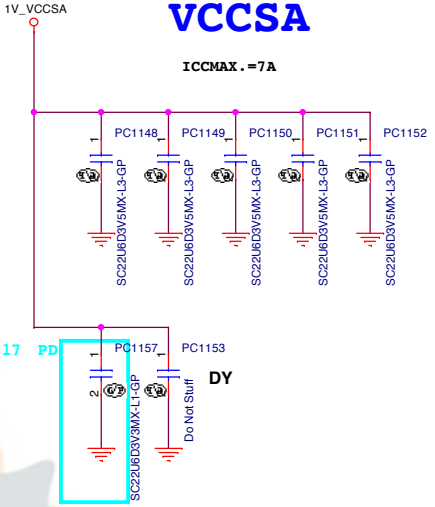
GT2 IccMax current = 31 A

GT23e IccMax current = 64 A

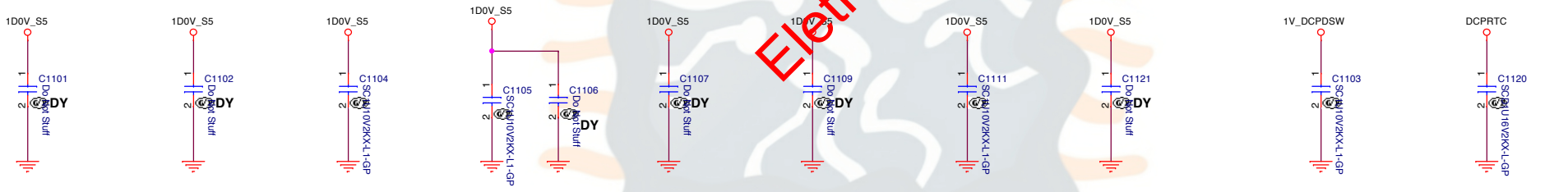


VCCSA

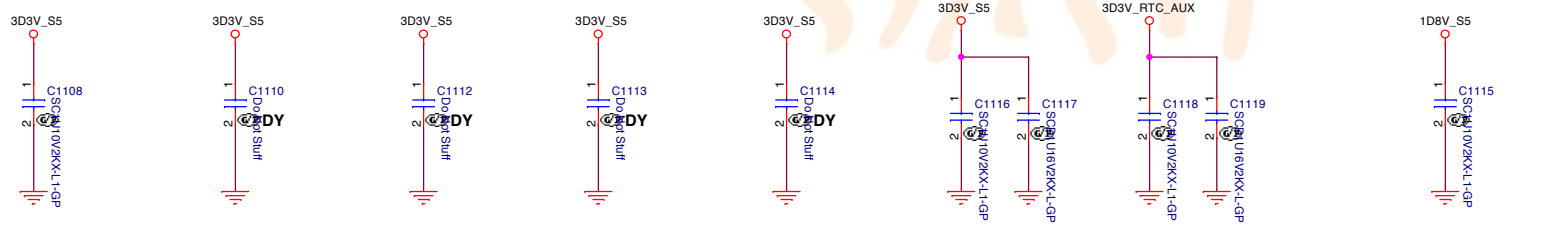
ICCMAX.=7A



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



CLOSE CPU AB19 CLOSE CPU AF18 CLOSE CPU K17 CLOSE CPU N15 CLOSE CPU K15 CLOSE CPU AF20 CLOSE CPU N18 CLOSE CPU A10 CLOSE CPU AL1 CLOSE CPU BB10



CLOSE CPU AJ19 CLOSE CPU V19 CLOSE CPU AG15 CLOSE CPU Y16 CLOSE CPU T16 CLOSE CPU AK17 CLOSE CPU AK19 CLOSE CPU AA1

per MP

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(Power CAP2)	
Size A3	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017	Sheet 11 of 105	

Main Func = DDR SODIMM

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

20150217

20140919
Thermal EVENT
R1211 Do Not Stuff
TS#_DIMM0_1
3D3V_S0

20140919

20150312

Layout Note:
Place these Caps near DIMM1.

SA_DIMM_VREFDQ
M_VREF_CA_DIMMA
V_SM_VREF_CNT
M_VREF_DQ_DIMMA

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Place these caps close to DM1 PIN126
20140926 JACK

Place these caps close to DM1 PIN1
20140926 JACK

close to dimm

62.10024.S61
2nd = 62.10024.M51
3rd = 62.10024.Q71
4th = 62.10017.I21

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Title: DDR3-SODIMM1
Size: A2
Document Number: Mihawk MB
Rev: X3
Date: Tuesday, June 06, 2017
Sheet 12 of 45

ECEtRO-Q

Main Func = DDR SODIMM

20150217

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

DM2

DDR3-204P-262-GP-U
62.10024.S21
2nd = 62.10024.M31
3rd = 62.10024.Q61
4th = 62.10017.I31

20140919

Thermal EVENT

20140919

Layout Note:
Place these caps near DIMM2.

20150429 SB

20150312

20150312

20150312

Layout Note:
Place these caps close to DM2 PIN126

20140926 JACK

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

Layout Note:
Place these caps close to DM2 PIN1

20140926 JACK

close to dimm

Layout Note:
Place Close DIMM2

Eletro-X

ECEtRO-X

per MP

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Taipei Hsien 221, Taiwan, R.O.C.

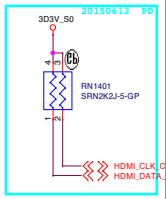
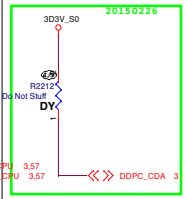
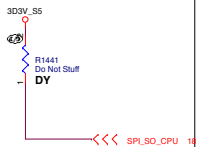
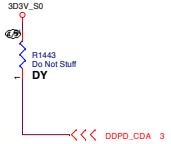
Title: DDR3-SODIMM2

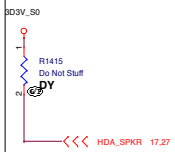
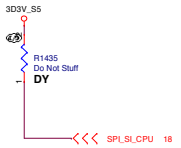
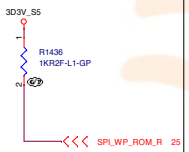
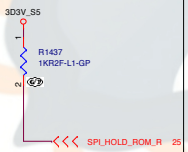
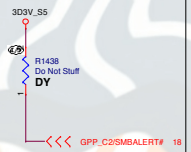
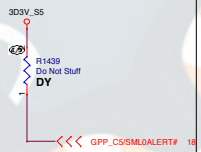
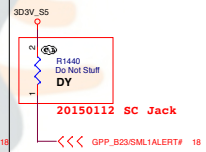
Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 13 of 45

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected		Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected		Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TPM Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
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Title: (Reserved)_SODIMM _SODIMM4

Size: A2 | Document Number: Mihawk MB | Rev: 1.0

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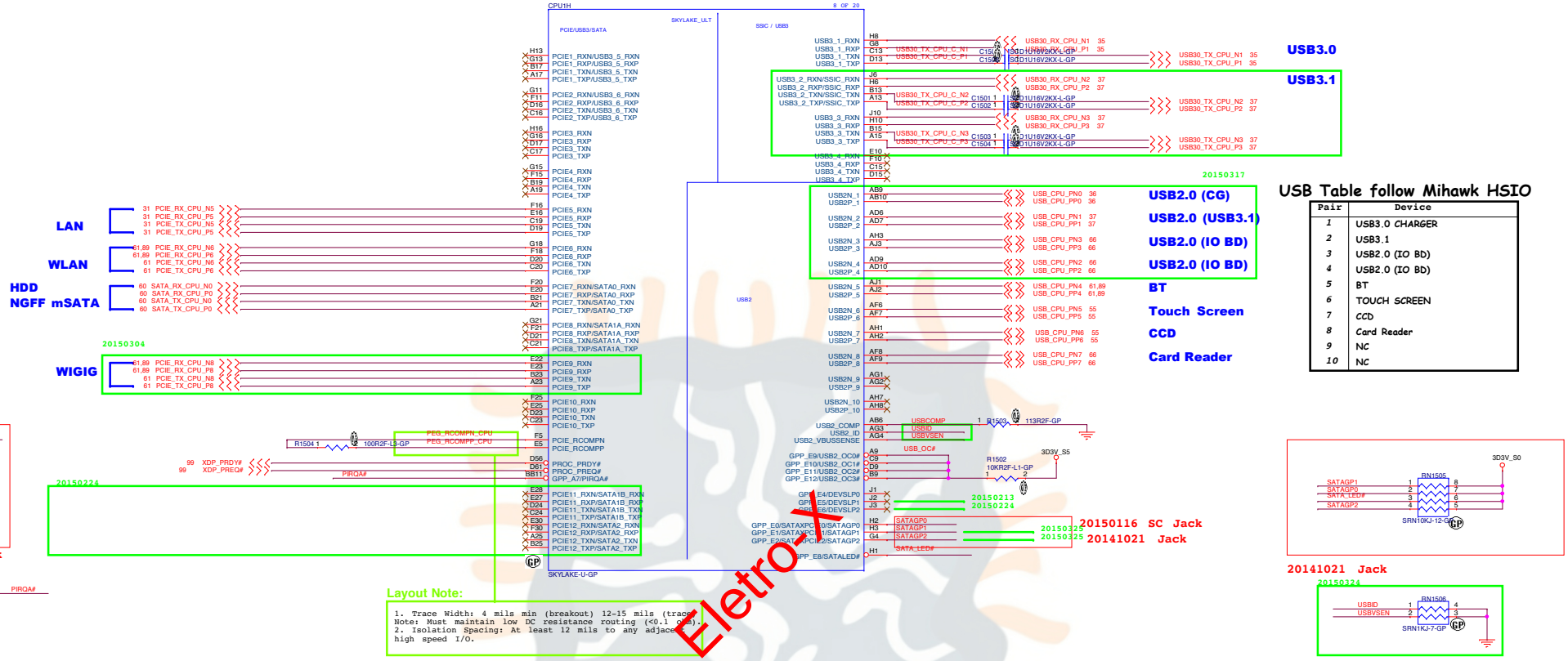
Main Func = PCH



USB Table follow Mihawk HSIO

Pair	Device
1	USB3.0 CHARGER
2	USB3.1
3	USB2.0 (IO BD)
4	USB2.0 (IO BD)
5	BT
6	TOUCH SCREEN
7	CCD
8	Card Reader
9	NC
10	NC

SKL Premium U			Acer 2015		Mihawk_SL
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3(Type C)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3(Type C)
Lane4	USB3 Port4				
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		
Lane6	USB3 Port6 (Premium)	PCIe Port2			
Lane7		PCIe Port3			
Lane8		PCIe Port4			
Lane9		PCIe Port5	LAN		LAN
Lane10		PCIe Port6	WIFI		WIFI
Lane11	SATA0(Base/Premium)	PCIe Port7 (Premium)	HDD		HDD / M.2 SSD (SATA)
Lane12	SATA1(Base/Premium)	PCIe Port8 (Premium)	ODD		
Lane13		PCIe Port9	NA	M.2 SSD (PCIeX4) * BIOS needs to set PCIE x4 Lane reversal	WIGIG (PCIe x1)
Lane14		PCIe Port10			
Land15	SATA1 (Premium)	PCIe Port11			
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x 1)		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O)
	USB2 Port2		USB 3 (I/O)		USB 2 (Type C)
	USB2 Port3		USB 3 (I/O)		USB 2 (I/O) for DB
	USB2 Port4		USB 2 (I/O)/Sensor Hub		USB 2 (I/O) for DB
	USB2 Port5		BT		BT
	USB2 Port6		TS		TS
	USB2 Port7		CCD		CCD
	USB2 Port8		CR(USB)/FP		CR
	USB2 Port9 (Premium)		3G		
	USB2 Port10 (Premium)				

per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

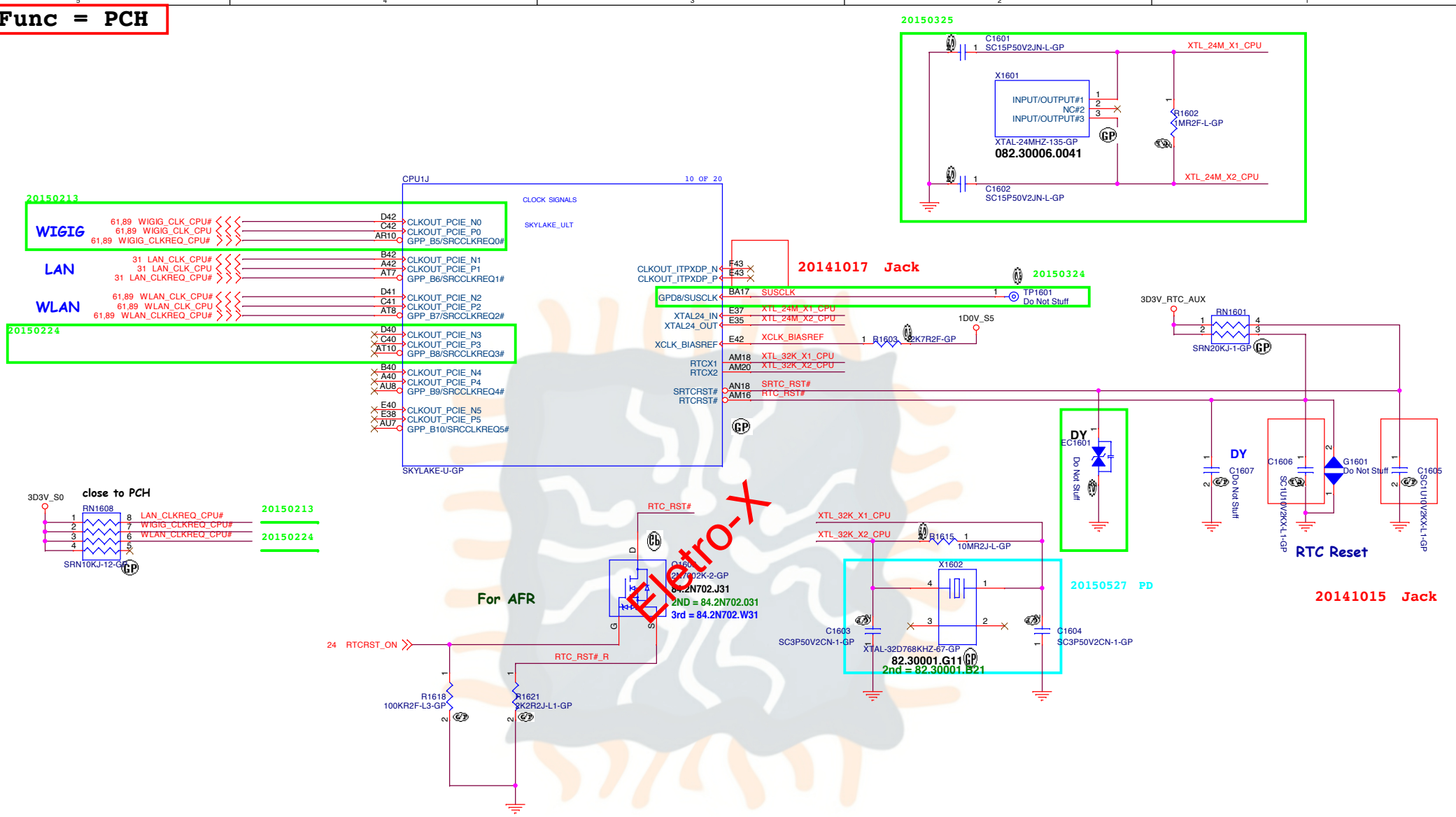
Title: CPU_(PCIE/SATA/USB)

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 15 of 103

ECEtRO-Q

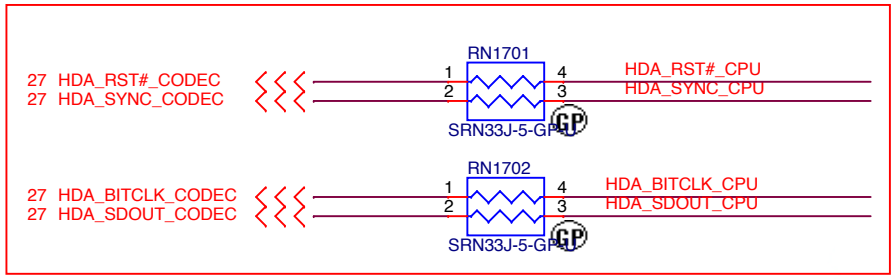
Main Func = PCH



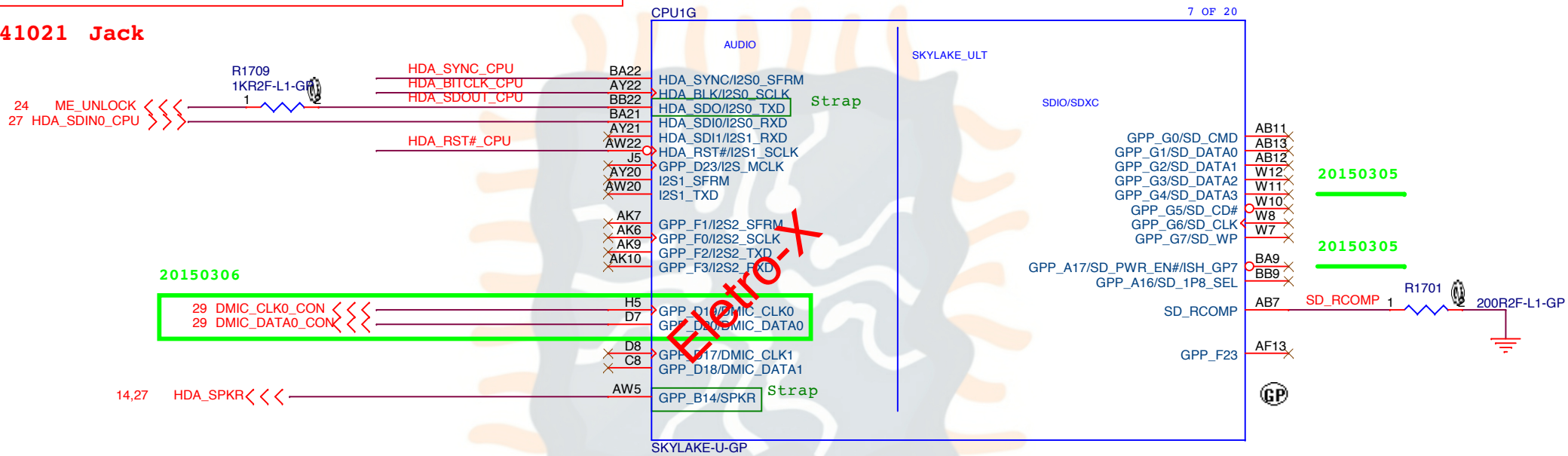
per MP

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MCP_CLOCK
Size: A3	Document Number: Mihawk MB
Rev	1.3
Date: Tuesday, June 06, 2017	Sheet 16 of 106

Main Func = PCH



20141021 Jack



per MP

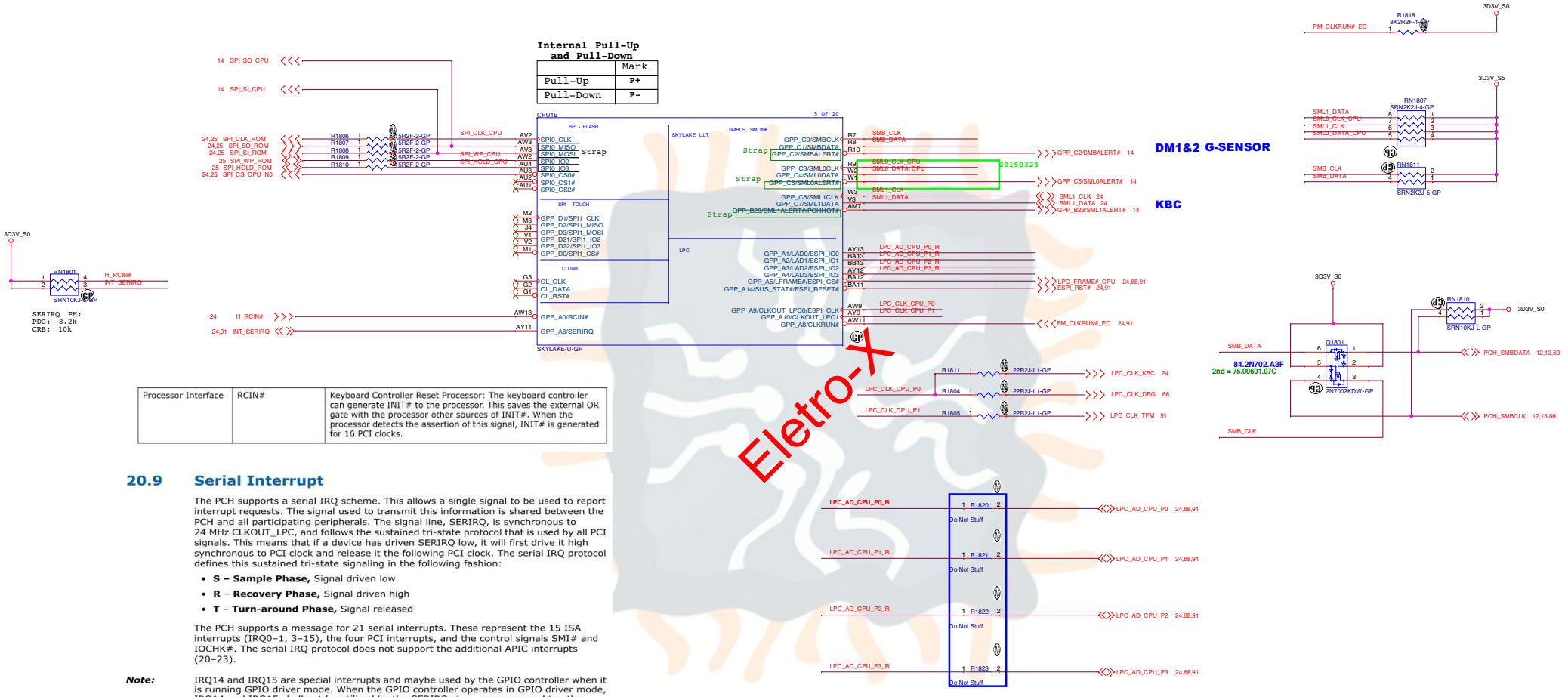
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size: A4 | Document Number: Mihawk MB | Rev: -3

Date: Tuesday, June 06, 2017 | Sheet 17 of 105

Main Func = PCH



Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

per MP

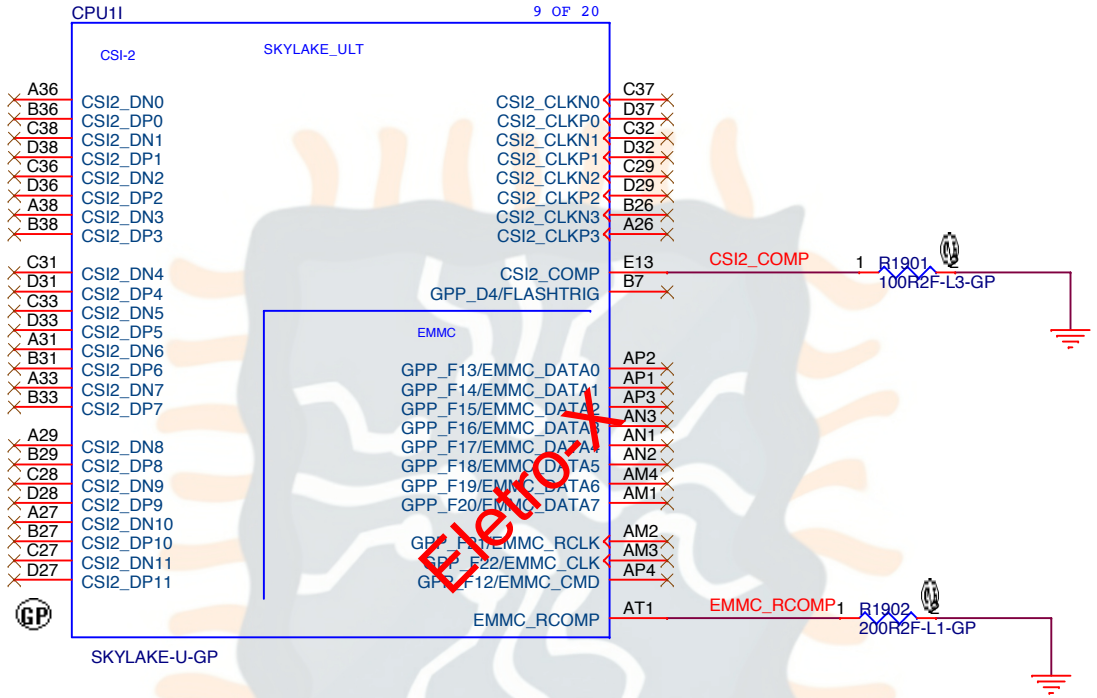
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPC,SPI,SMBUS,CLINK

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 18 of 105

Main Func = PCH

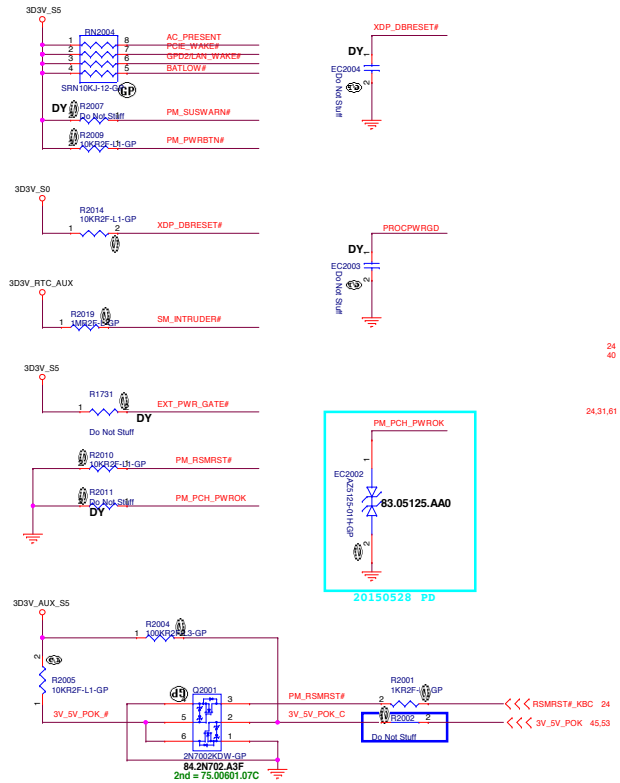


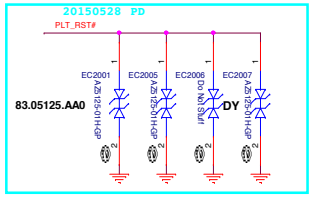
per MP

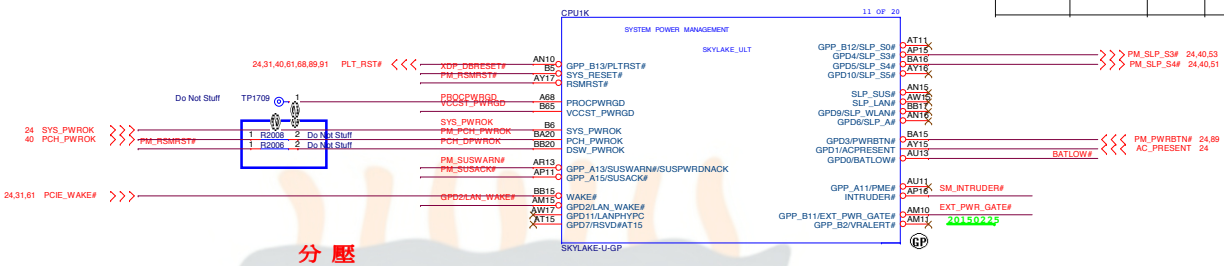
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_(CS-2/EMMC)	
Size A4	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017	Sheet 19 of 103	

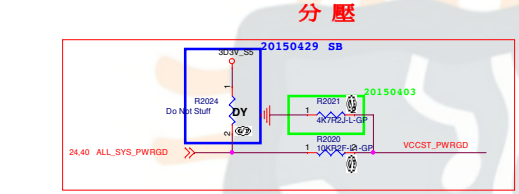
ECEtRO-L

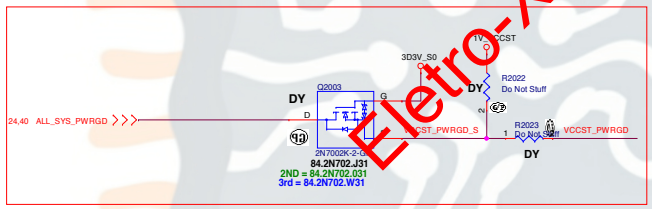
Main Func = PCH





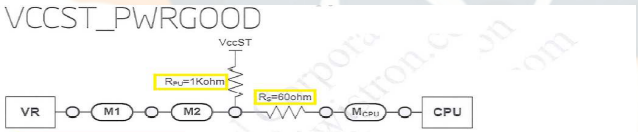






#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

VCCST_PWRGD / HWM201:



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

GPP_A13-15 pin(LPC/eSPI):

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

per MP

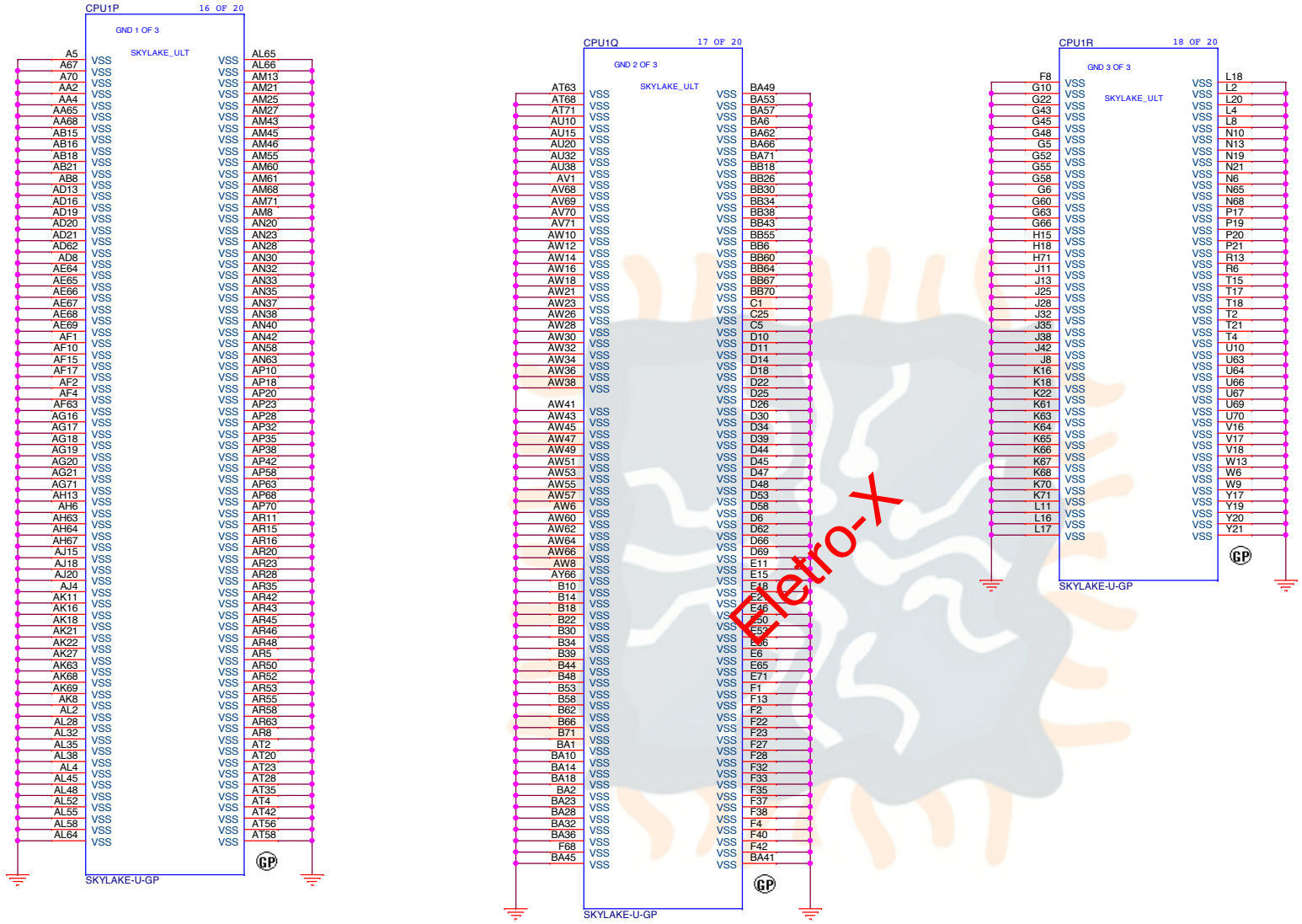
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 20 of 45

Main Func = PCH



per MP

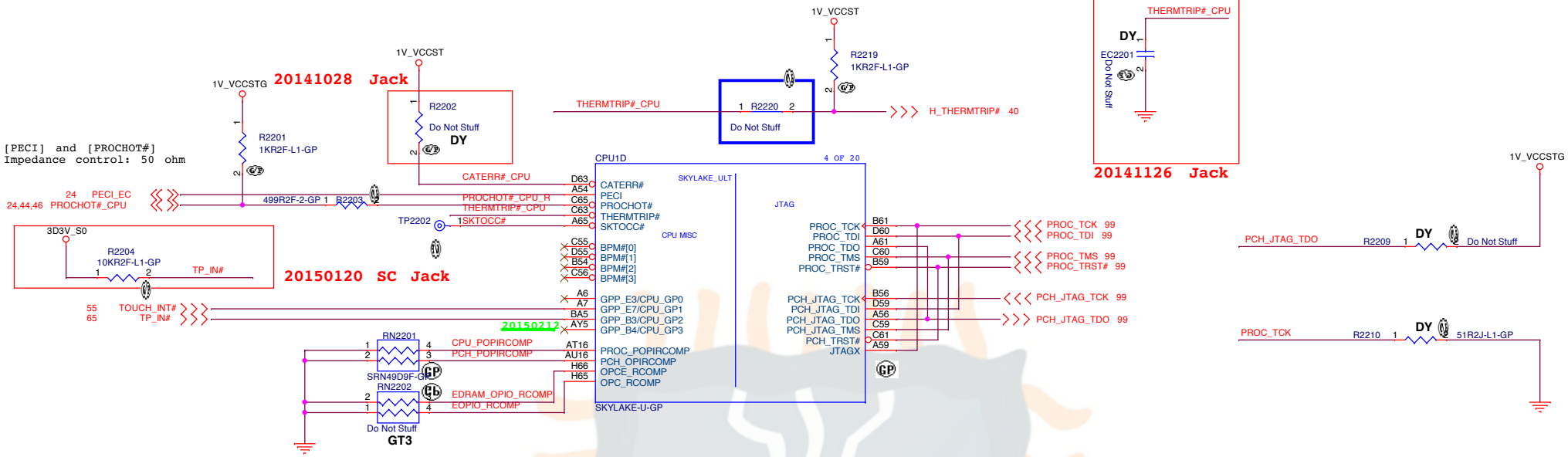
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A3 | Document Number: Mihawk MB | Rev: -3

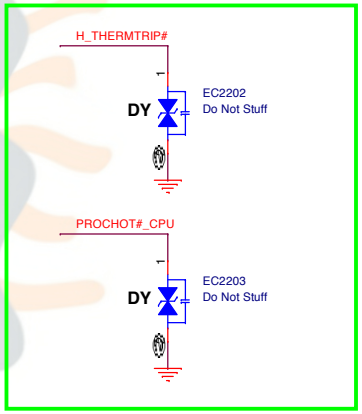
Date: Tuesday, June 06, 2017 | Sheet 21 of 105

Main Func = CPU



PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

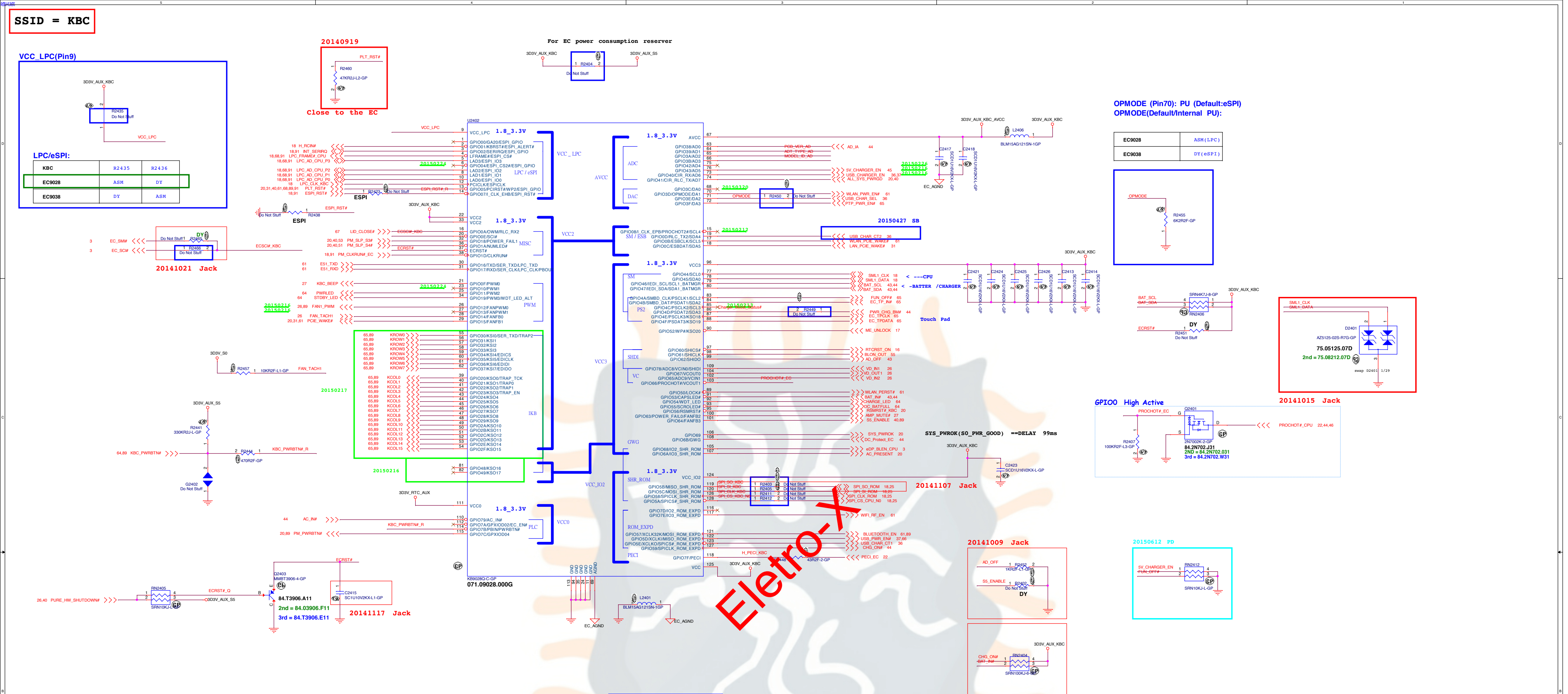
20150324

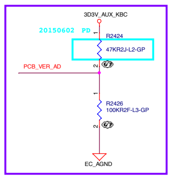


per MP

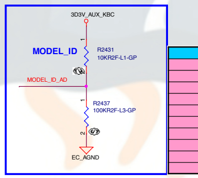
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_(JTAG/CPU SIDE BAND)
Size A3	Document Number: Mihawk MB
Rev	-3
Date: Tuesday, June 06, 2017	Sheet 22 of 105

SSID = KBC

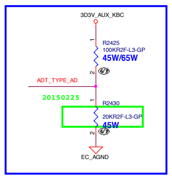




PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V



MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
UMA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
Reserved for project use	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
Reserved for project use	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
Reserved for project use	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V



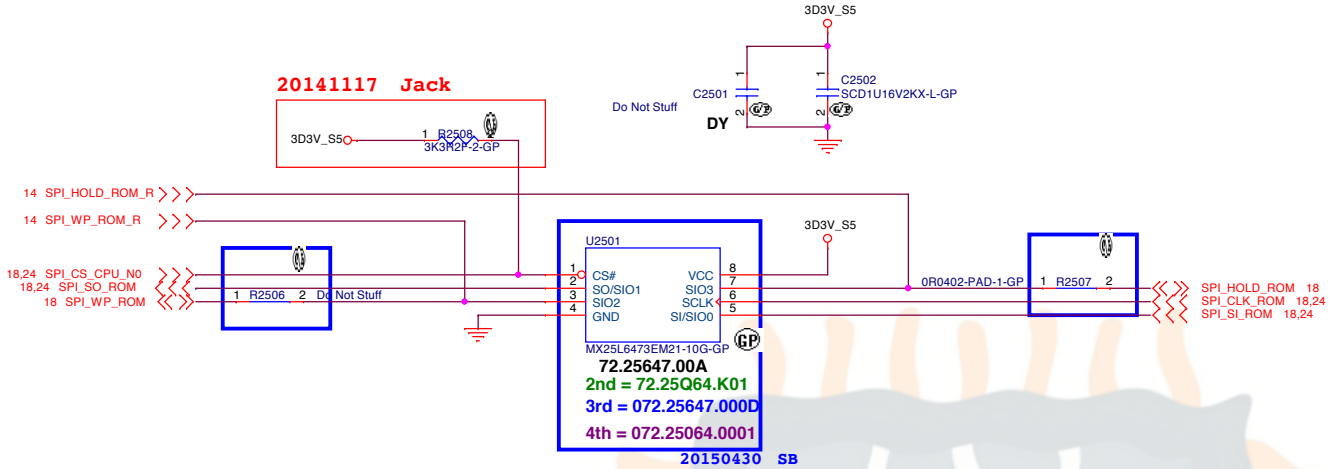
ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

緯創資通 Wistron Corporation

EC CONTROLLER

Mihawk MB

Main Func = SPI Flash



SPI FLASH ROM (8M byte) for PCH

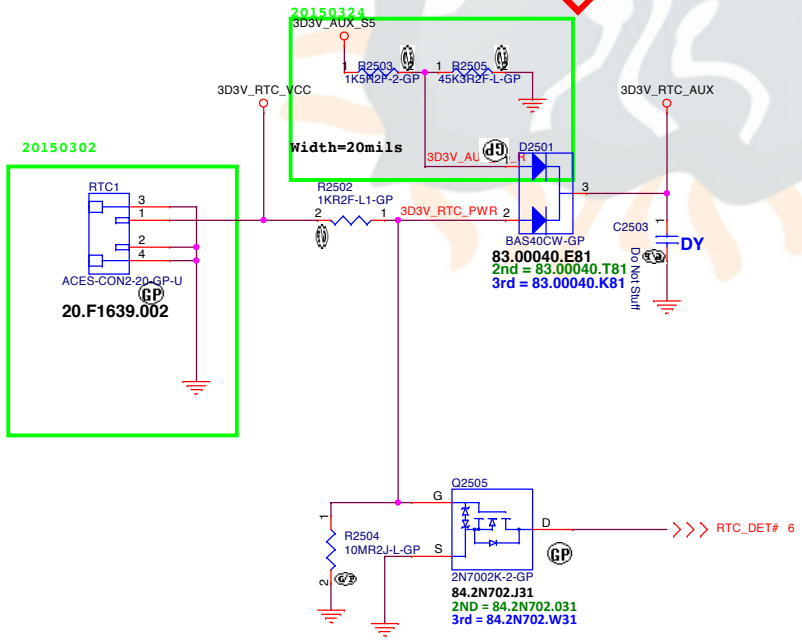
SPI ROM Equal length need to less than 500mil

20150312

```
SPI FLASH ROM (8M byte)

1st=72.25647.00A  (MXIC  MX25L6473EM2I-10G)
2nd=72.25Q64.K01  (WINBOND  W25Q64FVSSIQ)
3rd=072.25647.000D(MXIC   MX25L6473F)
4th=072.25064.0001(ISSI  IC25LP064A-QBLE)
```


Main Func = RTC



per MP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Flash(KBC+PCH)/RTC		
Size: A3	Document Number: Mihawk MB	Rev: 3
Date: Tuesday, June 06, 2017	Sheet 25 of 105	

Main Func = Thermal Sensor

AFTP TESTPOINT

89 FAN_TACH1_C <<< FAN_TACH1_C

5V_S0

Layout 15 mil

C2603 SC4D7U25V5KX-L2-GP

C2602 SCD1U16V2KX-L-GP

D2601 CH551H-30PT-GP

83.R5003.C8F

2nd = 83.R5003.H8H

20150217

FAN1

D2602 CH551H-30PT-GP

24 FAN_TACH1 <<< FAN_TACH1_C

20150216 24,89 FAN1_PWM >>>

83.R5003.C8F

2nd = 83.R5003.H8H

ACES-CON4-7-GP-U

20.F0772.004

2nd = 20.F1804.004

3D3V_AUX_S5

R2611 16KR2F-GP

RT2601 NTC-100K-11-GP-U

C2607 SCD1U16V2KX-L-GP

C2608 SC100P50V2JN-L-GP

VD_IN1 24

RT2601 close CPU for CPU

3D3V_AUX_S5 20150302

R2612 Do Not Stuff

RT2602 Do Not Stuff

C2610 Do Not Stuff

C2609 Do Not Stuff

VD_IN2 24

RT2602 close CPU and memory for system

Eletro-X

3D3V_S0

R2606 2KR2F-L1-GP

R2610 Do Not Stuff

VD_OUT1 24

Q2603 2N7002K-2-GP

84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31

THERM_SYS_SHDN#_R

IMVP_PWRGD_G

24,40 PURE_HW_SHUTDOWN#

R2608 Do Not Stuff

C2606 Do Not Stuff

R2609 Do Not Stuff

VR_RDY 40,46

per MP

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G788P81/Fan Controllor P2793

Size: A3 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 26 of 105

ECEtRO-L

SSID = 104C

20150617 PD

Close to Pin46

Close to Pin41

20141009 Jack

FOR EMI

Close pin36

20141015 Jack

Close pin40

AUD_AGND close to codec IC

placed nearby codec PIN12

20150121 SC Jack

20141030 Jack

Layout Note:
Place close to Pin 26

Layout Note:
Place close to Pin 13

071.00255.0003

ALC255-CG-GP-U

R2708 is need to connect.To prvent the beep sound

20141009 Jack

Close to Pin1

20141009 Jack

75.05125.07D

2nd = 75.08212.07D

Layout Note:

75.05125.07D

2nd = 75.08212.07D

Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Elero-X

per MP

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC255

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 27 of 45

ECEtRO-Q

SSID = AUDIO

Speaker

AUD_SPK1_L-_CON — AUD_SPK1_L-_CON 89
AUD_SPK1_L+_CON — AUD_SPK1_L+_CON 89
AUD_SPK1_R-_CON — AUD_SPK1_R-_CON 89
AUD_SPK1_R+_CON — AUD_SPK1_R+_CON 89

AFTP TESTPOINT

20150602 PD

27 AUD_SPK_R+ — R2914 1 2 Do Not Stuff
27 AUD_SPK_R- — R2915 1 2 Do Not Stuff
27 AUD_SPK_L- — R2916 1 2 Do Not Stuff
27 AUD_SPK_L+ — R2917 1 2 Do Not Stuff

AUD_SPK1_R+_CON
AUD_SPK1_R-_CON
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON

EC2901 1 2 Do Not Stuff DY
EC2902 1 2 Do Not Stuff DY
EC2915 1 2 Do Not Stuff DY
EC2920 1 2 Do Not Stuff DY

Layout Note:
Trace width=40mil

20150224

SPK1
6 4 3 2 1 5
ACES-CON4-17-GP-U1
20.F1621.004
2nd = 20.F1937.004

20150325

AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON

ED2901
AZ5125-02S-R7G-GP
75.05125.07D
2nd = 75.08212.07D

ED2902
AZ5125-02S-R7G-GP
75.05125.07D
2nd = 75.08212.07D

DMIC

20150427 SB

3D3V_S0
C2903
SCD1U16V2KX-L-GP
DMIC1
VDD CS CLK DATA GND GND
DMIC_CLK_CON_R
DMIC_DATA_CON_R
MICROPHONE-93-GP-U
082.40006.0001
2ND = 082.40002.0031
3rd = 082.40011.0011

20150427 SB

DMIC_CLK_CON_R
DMIC_DATA_CON_R

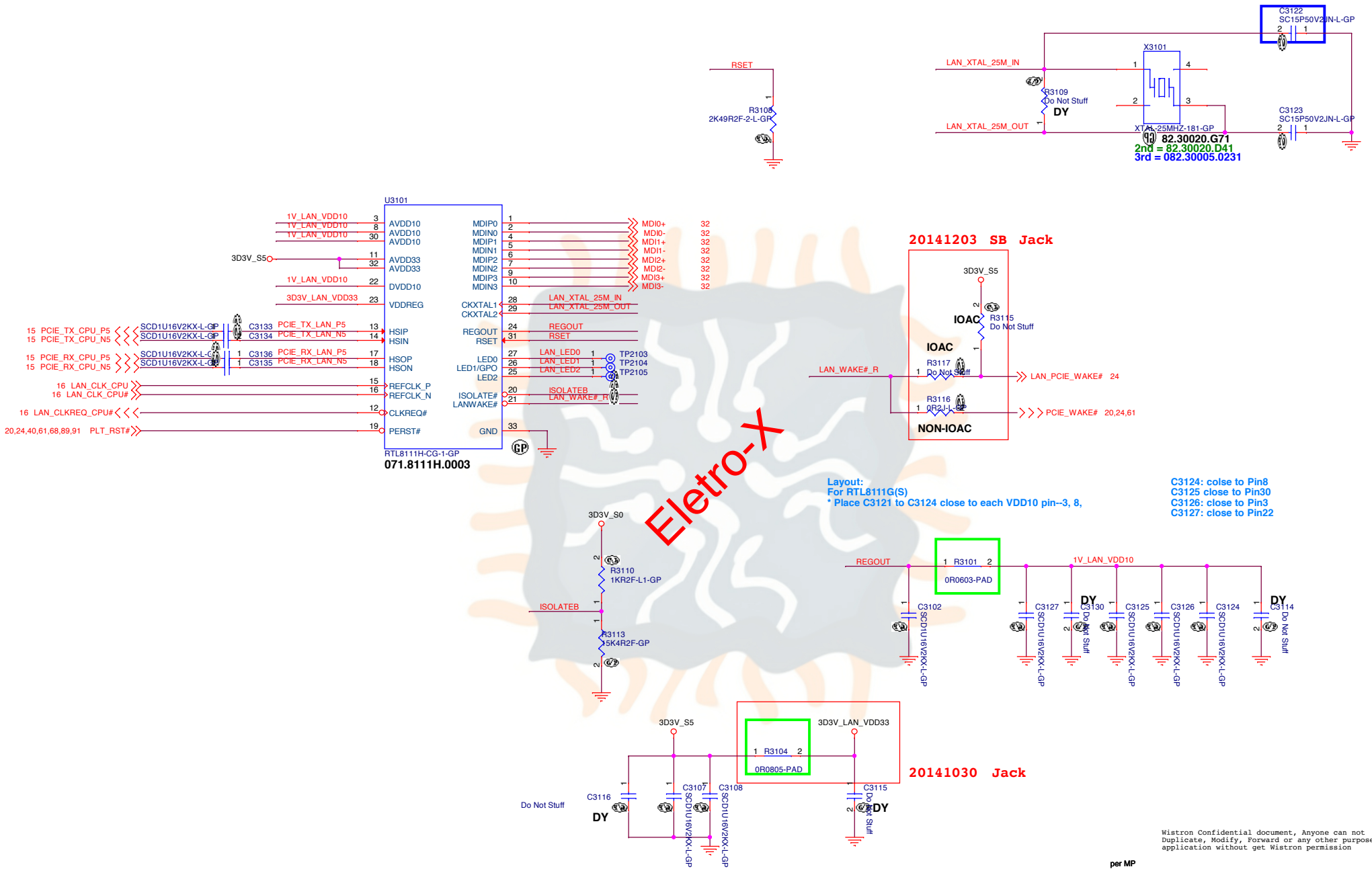
DY R2926 Do Not Stuff — DMIC_DATA0_CON 17
DY R2925 Do Not Stuff — DMIC_CLK0_CON 17
R2909 0R2J-L-GP — DMIC_CLK_CON 27
R2911 0R2J-L-GP — DMIC_DATA_CON 27

EC2903 EC2904
SC22P50V2JN-L-GP
SC22P50V2JN-L-GP

per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC
Size: A3
Document Number: Mihawk MB
Rev: 1.3
Date: Tuesday, June 06, 2017
Sheet 29 of 100



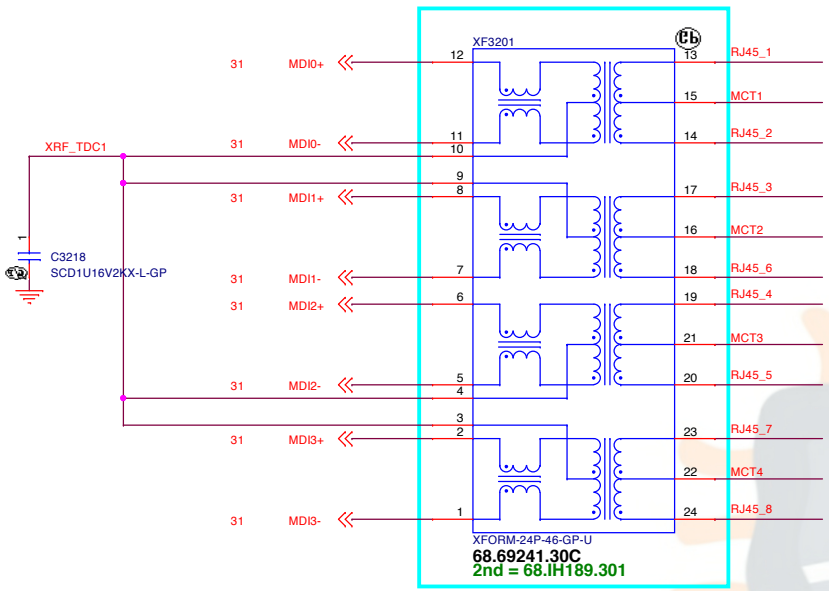
per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

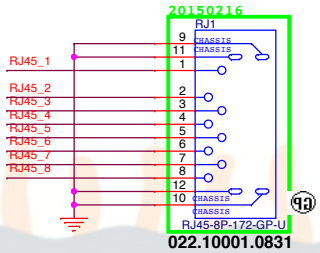
Title	LAN(RTL8111H)	
Size A3	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017	Sheet 31 of 105	

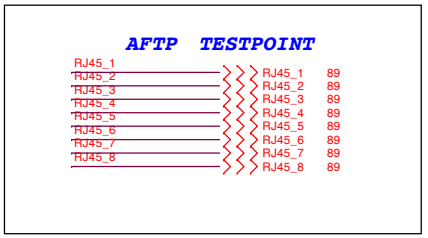
SSID = LAN

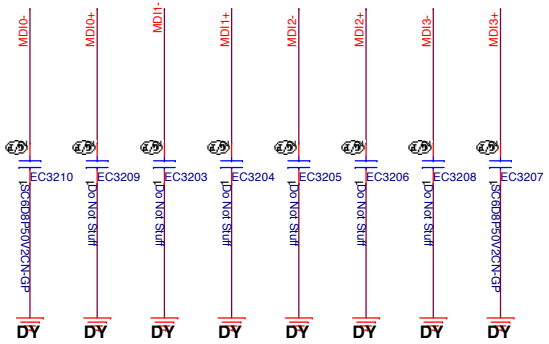
20150623 PD

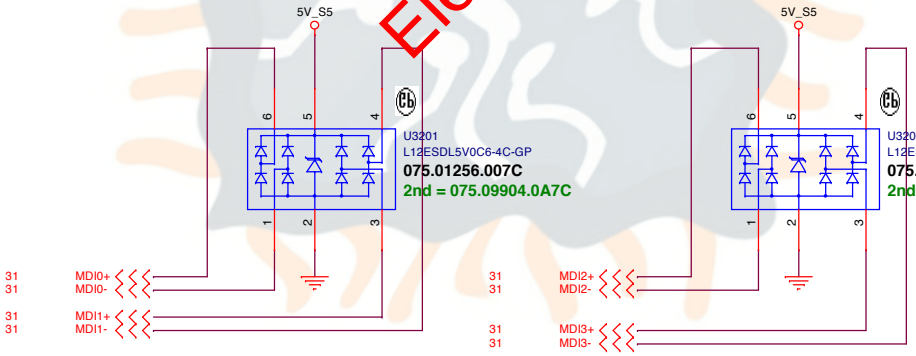


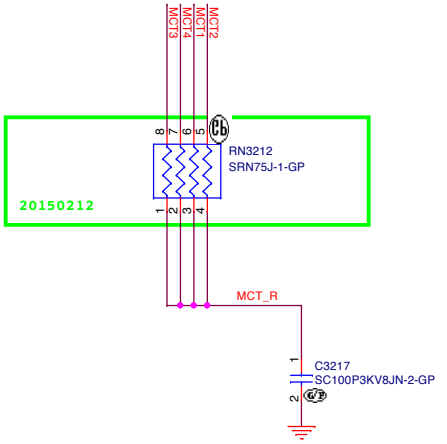
20150216











Eletro-X

per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (LAN+VGA) CONNECTOR

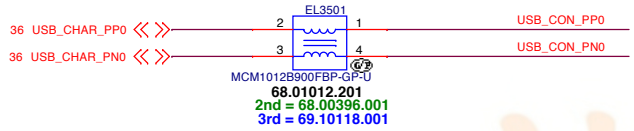
Size: A3 | Document Number: Mihawk MB | Rev: -3

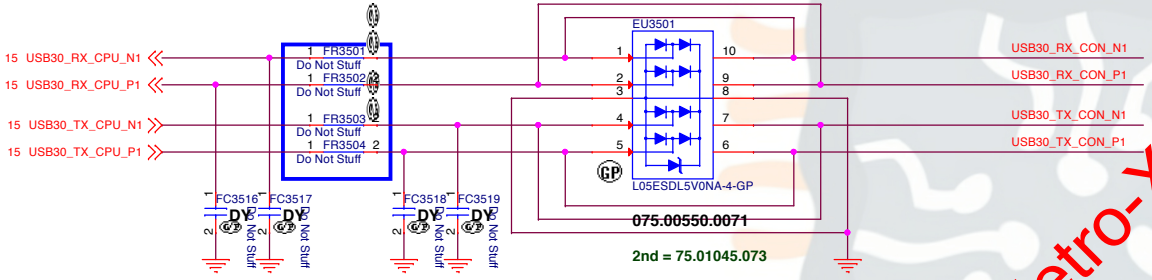
Date: Tuesday, June 06, 2017 | Sheet 32 of 105

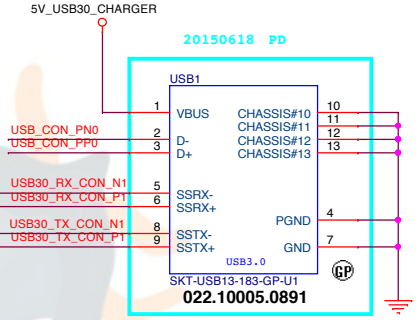
ECEtRO-L

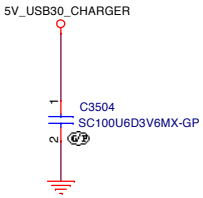
USB 3.0 Connector Pin definition

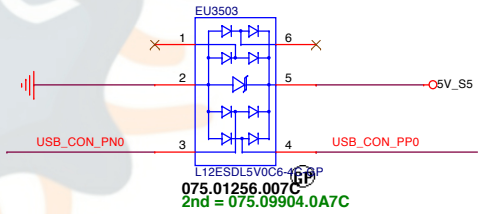
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+











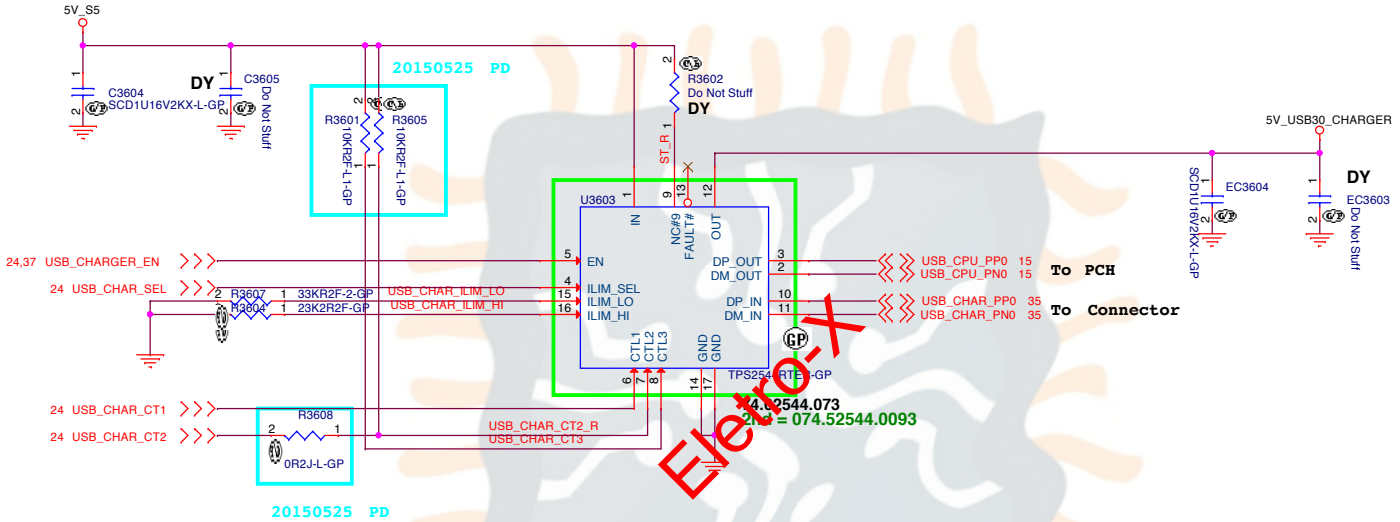
per MP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 CONN

Size: A3 | Document Number: Mihawk MB | Rev: L3

Date: Tuesday, June 06, 2017 | Sheet 35 of 100



	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A ~ 2.4 A).

per MP

緯創資通 Wistron Corporation

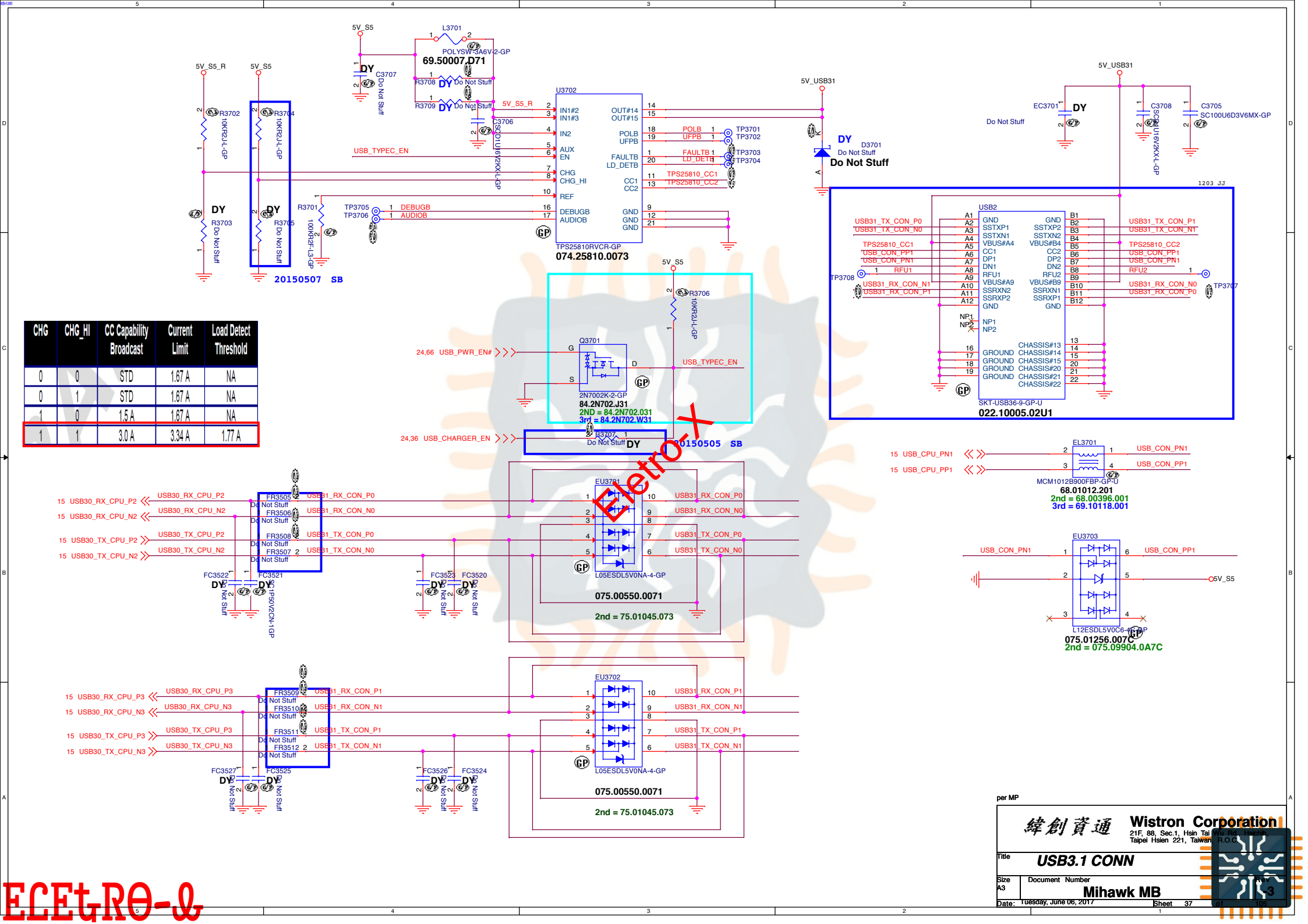
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size: A3 | Document Number: Mihawk MB | Rev: -3

Date: Tuesday, June 06, 2017 | Sheet 36 of 105

ECE-RO-L



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

per MP

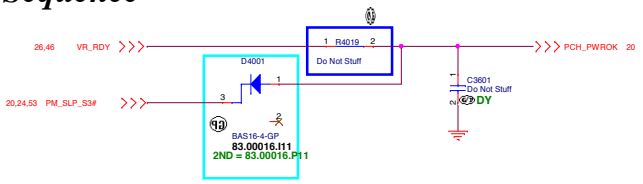
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

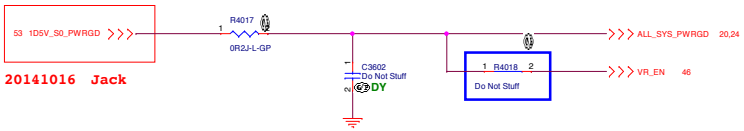
Title: USB3.1 CONN

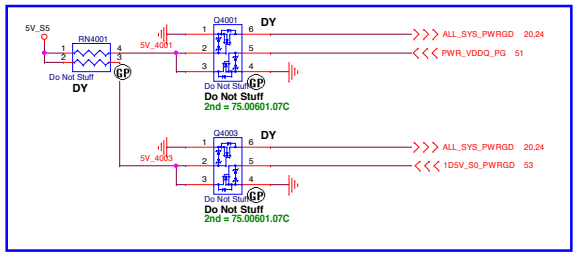
Size: A3 | Document Number: Mihawk MB | Rev: -3

Date: Tuesday, June 06, 2017 | Sheet 37 of 105

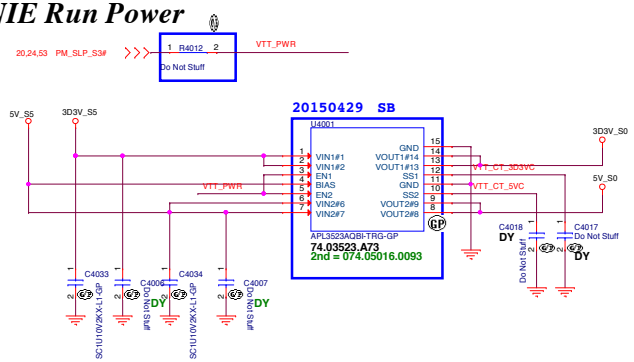
Power Sequence

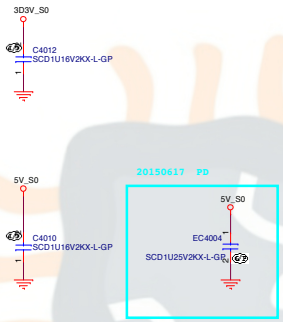


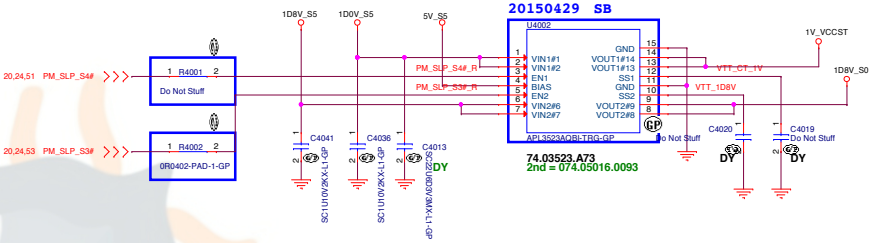


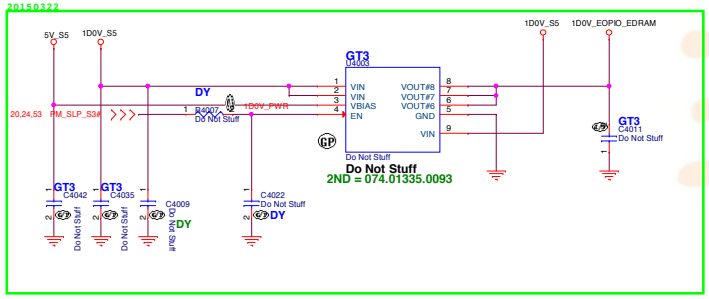


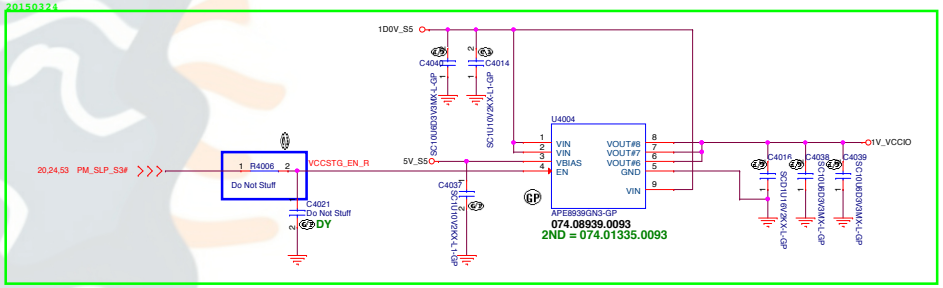
ANNIE Run Power

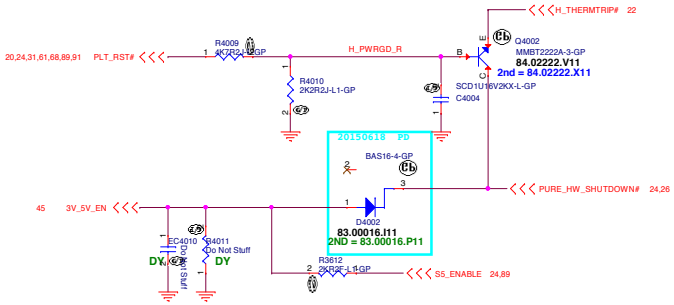


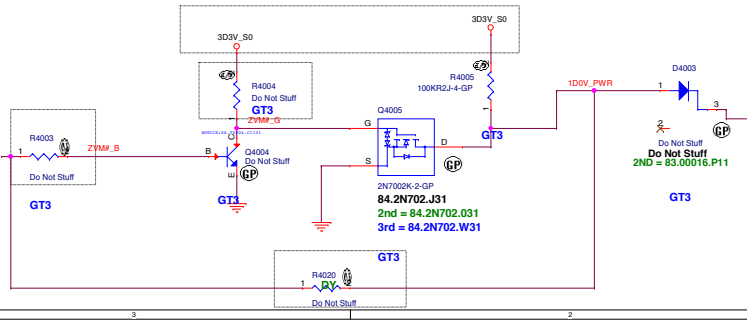










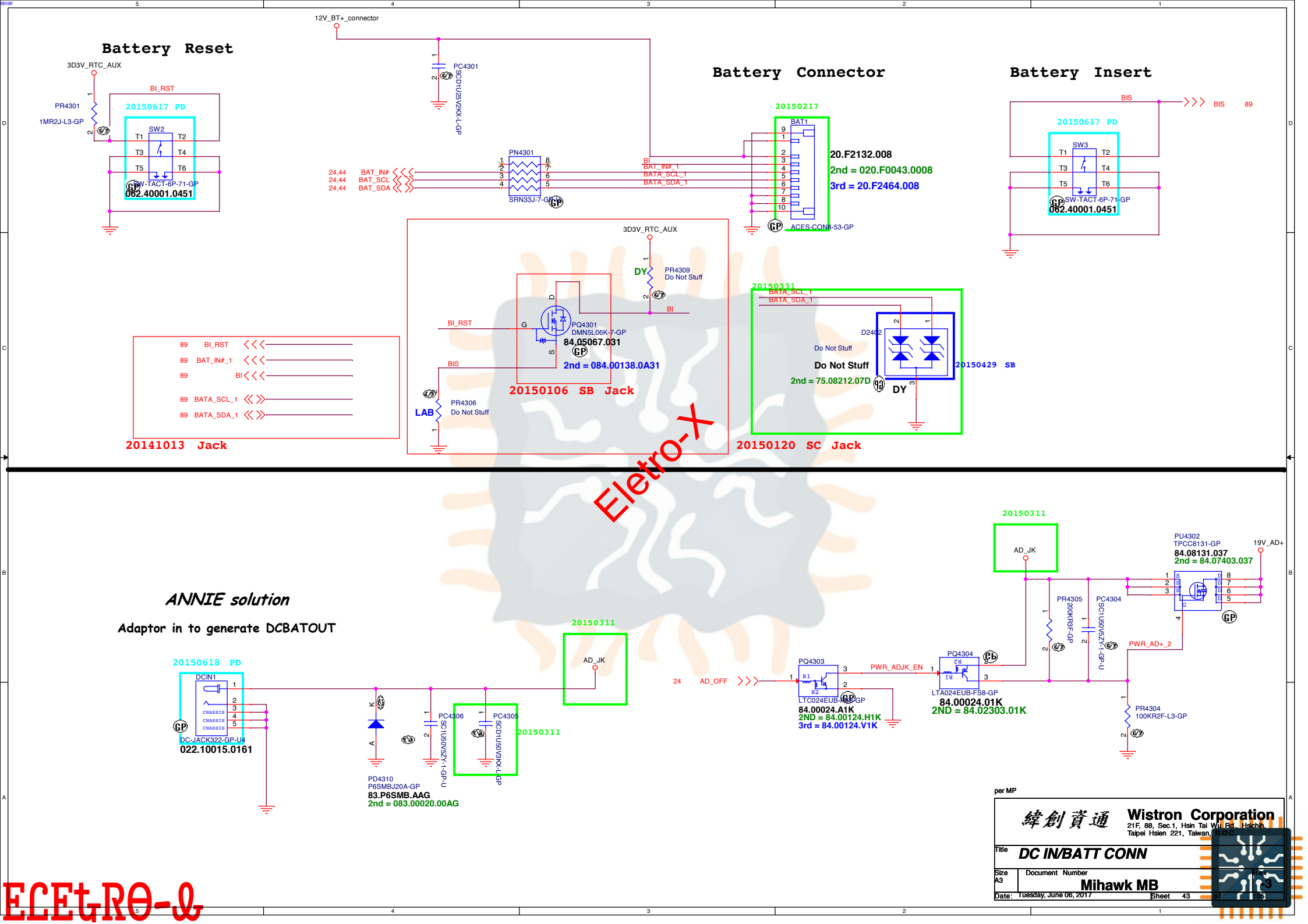


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 40 of 43


Battery Reset
3D3V_RTC_AUX
BI_RST
PR4301
1MR2J-L3-GP
20150617 PD
SW2
T1 T2 T3 T4 T5 T6
SW-TACT-6P-71-GP
082.40001.0451
12V_BT+_connector
PC4301
SCD1U25V2KX-L-GP
Battery Connector
20150217
BAT1
ACES-CON8-53-GP
20.F2132.008
2nd = 020.F0043.0008
3rd = 20.F2464.008
PN4301
SRN33J-7-GP
24,44 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA
BI
BATA_SCL_1
BATA_SDA_1
Battery Insert
BIS
20150617 PD
SW3
SW-TACT-6P-71-GP
082.40001.0451
3D3V_RTC_AUX
DY
PR4309
Do Not Stuff
PQ4301
DMN5L06K-7-GP
84.05067.031
2nd = 084.00138.0A31
BI_RST
BIS
LAB
PR4306
Do Not Stuff
20150106 SB Jack
20150231
D2402
Do Not Stuff
Do Not Stuff
2nd = 75.08212.07D
20150429 SB
20150120 SC Jack
89 BI_RST
89 BAT_IN#_1
89 BI
89 BATA_SCL_1
89 BATA_SDA_1
20141013 Jack
Eletro-X
ANNIE solution
Adaptor in to generate DCBATOUT
20150618 PD
DCIN1
DC-JACK322-GP-U4
022.10015.0161
20150311
AD_JK
PC4306
SC1U50V5ZY-1-GP-U
PC4305
SCD1U50V3KX-L-GP
20150311
PD4310
P6SMBJ20A-GP
83.P6SMB.AAG
2nd = 083.00020.00AG
24 AD_OFF
PQ4303
LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.00124.V1K
PWR_ADJK_EN
PQ4304
LTA024EUB-FS8-GP
84.00024.01K
2ND = 84.02303.01K
20150311
AD_JK
PR4305
200KR3F-GP
PC4304
SC1U50V5ZY-1-GP-U
PWR_AD+_2
PU4302
TPCC8131-GP
84.08131.037
2nd = 84.07403.037
19V_AD+
PR4304
100KR2F-L3-GP
per MP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC IN/BATT CONN
Size A3
Document Number
Mihawk MB
Rev 3
Date: Tuesday, June 06, 2017
Sheet 43 of 105
ECEtRO-L

SSID = Charger

The 45W adapter AC protect can change to 120% (2.84A)

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect preset (85% x 120%)	AC_protect Current	PR4404 Sense resitor	Current to Voltage	R1 PR4407	R2 PR4401
65W	AC+Battery	High	3.1	102%	3.162	10mOhm	0.9696	41.2	100
45W	AC+Battery	High	2.37	102%	2.4174	20mOhm	0.9696	88.7	100
65W	AC+Battery	Low	3.42	102%	3.4884	10mOhm	0.69768	16.2	100
90W	AC+Battery	High	4.74	102%	4.8348	10mOhm	0.9696	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10mOhm	1.28724	113	100
135W	AC+Battery	High	7.1	102%	7.242	10mOhm	1.4484	180	100

	45W	65W
PR4404	20m(64.R0205.7FL)	10m(64.R0105.7FL)
PR4407	88.7K(64.88725.6DL	16.2K(64.16225.6DL
PR4401	100K(64.10035.L3L)	100K(64.10035.L3L)

adapter 45W and 65W
AC mode (default:120%):
set up the value by PR4401 and PR4407

20150612 PD

AC adapter detect current :
Ac input current = 20 x (Vacp - Vacn) / 10mohm

20150413 SB

20150507 SB

20150504 SB

20150402

CYNTEC 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Charger Current=1.4-3.6A

Battery I Sense

Layout Note:
1. Place PR4403, PG4409 and PG4411 near to BTY connector
2. Place PC4429, PC4430 and PC4431 near to PU4407

Battery OCP	R3	R4
6 Cell (3S2P)	7A	71.5K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery OCP setting

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery UVP setting

Battery OVP	R7	R8
6 Cell (3S2P)	14V	80.6K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

Battery OVP setting

Degliath Time Setting
125K -> Deglitch time : 5us
375K -> Deglitch time : 15us

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Title: CHARGER BQ24780
Size: Custom | Document Number: Mihawk MB | Rev: -3
Date: Tuesday, June 06, 2017 | Sheet 44 of 105

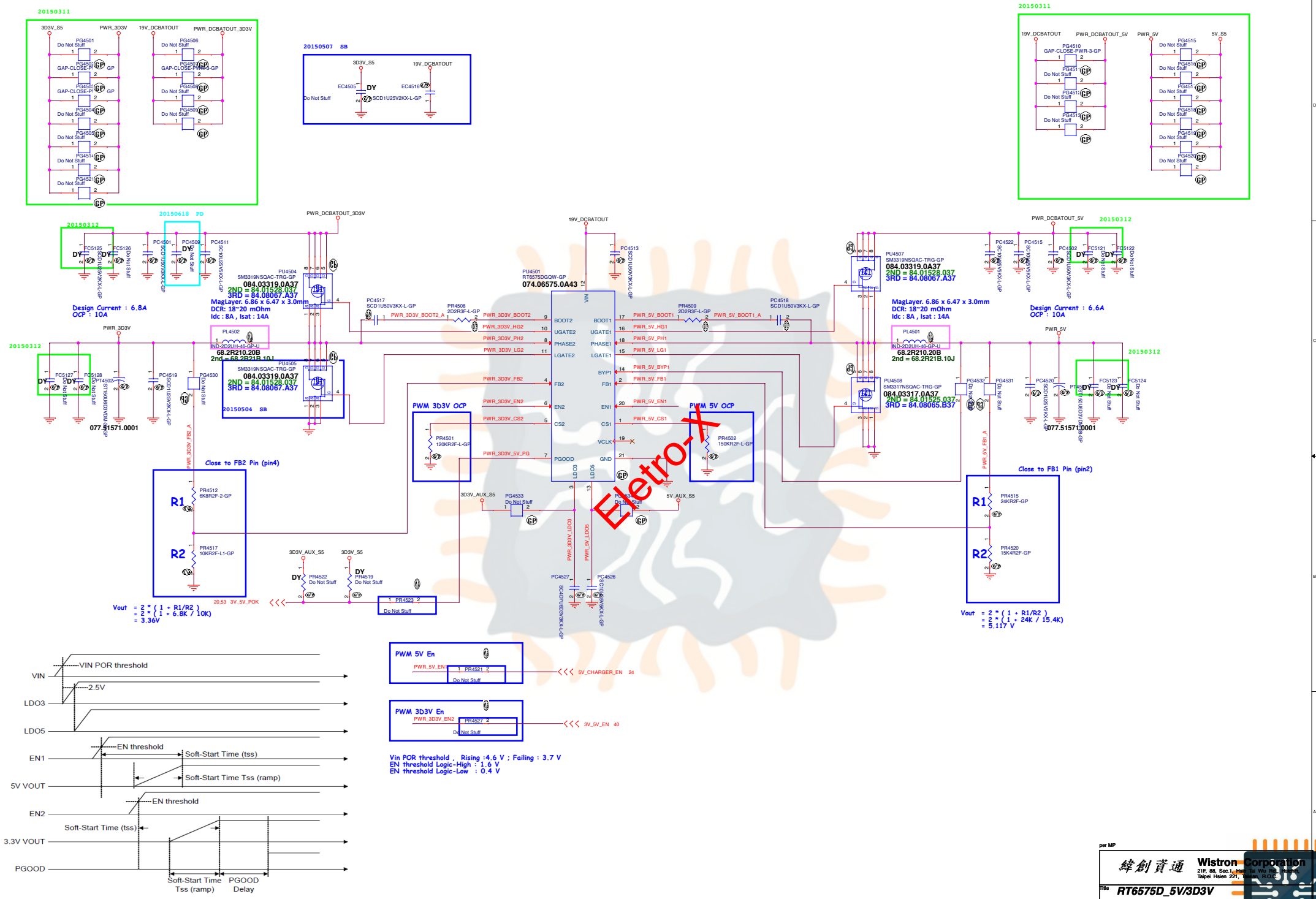
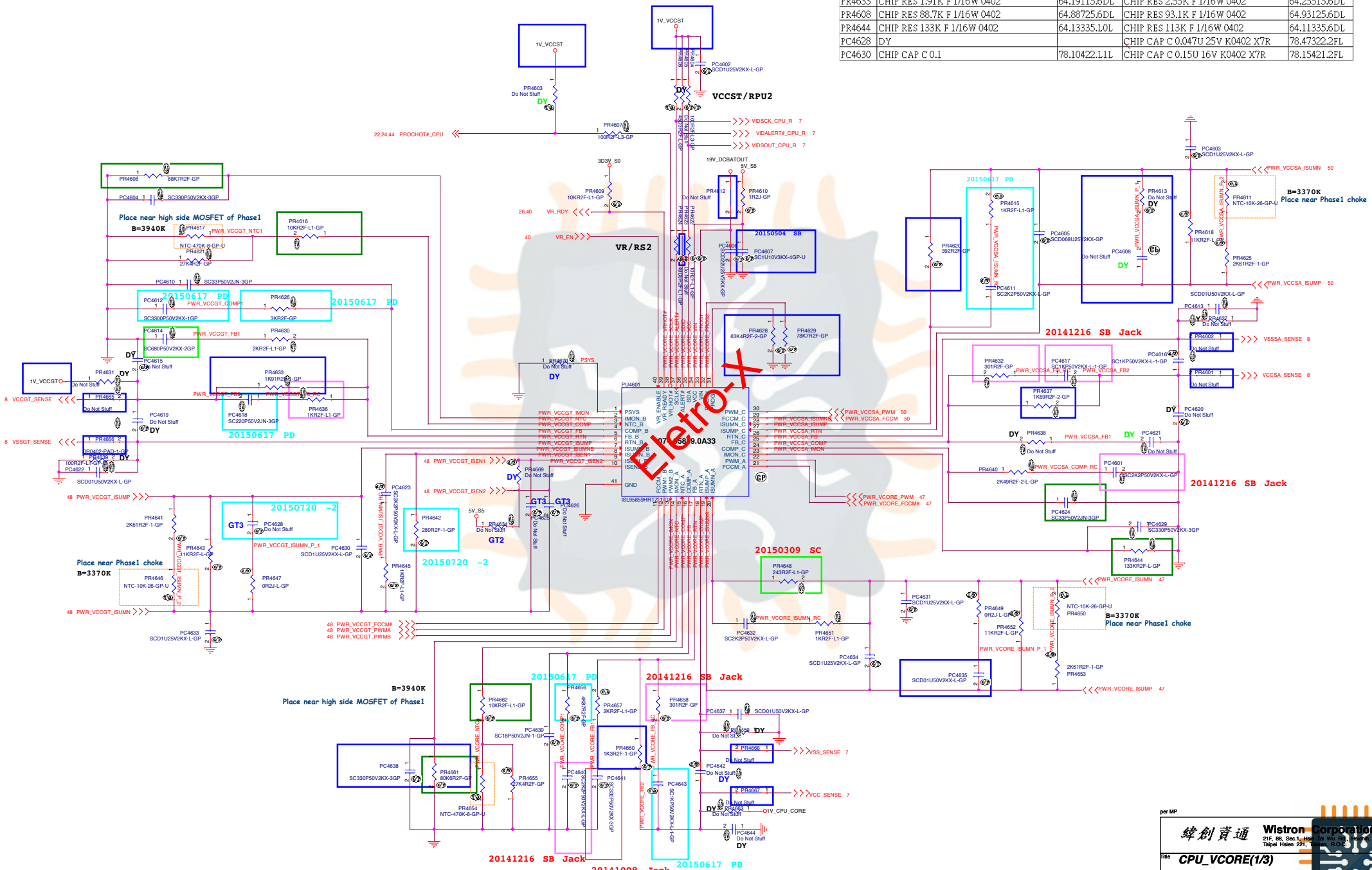


Figure 6. RT6575B Timing

Wistron Corporation	Title	RT6575D_5V/3D3V	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size A2	Document Number Mihawk MB	Rev 1.3
	Date: Tuesday, June 06, 2017	Sheet 45 of 53	

Main Func = CPU_CORE

	U22		U23e	
PR4629	CHIP RES 78.7K F 1/16W 0402	64.78725.6DL	CHIP RES 88.7K F 1/16W 0402	64.88725.6DL
PR4634	CHIP RES 100K F 1/16W 0402 13" REEL	64.10035.L3L	DY	
PR4642	CHIP RES 280 F 1/16W 0402	64.28005.6DL	CHIP RES 357K F 1/16W 0402	64.35705.6DL
PR4633	CHIP RES 1.91K F 1/16W 0402	64.19115.6DL	CHIP RES 2.55K F 1/16W 0402	64.25515.6DL
PR4608	CHIP RES 88.7K F 1/16W 0402	64.88725.6DL	CHIP RES 93.1K F 1/16W 0402	64.93125.6DL
PR4644	CHIP RES 133K F 1/16W 0402	64.13335.L0L	CHIP RES 113K F 1/16W 0402	64.11335.6DL
PC4628	DY		CHIP CAP C 0.047U 25V K0402 X7R	78.47322.2FL
PC4630	CHIP CAP C 0.1	78.10422.L1L	CHIP CAP C 0.15U 16V K0402 X7R	78.15421.2FL



per MP

Wistron Corporation
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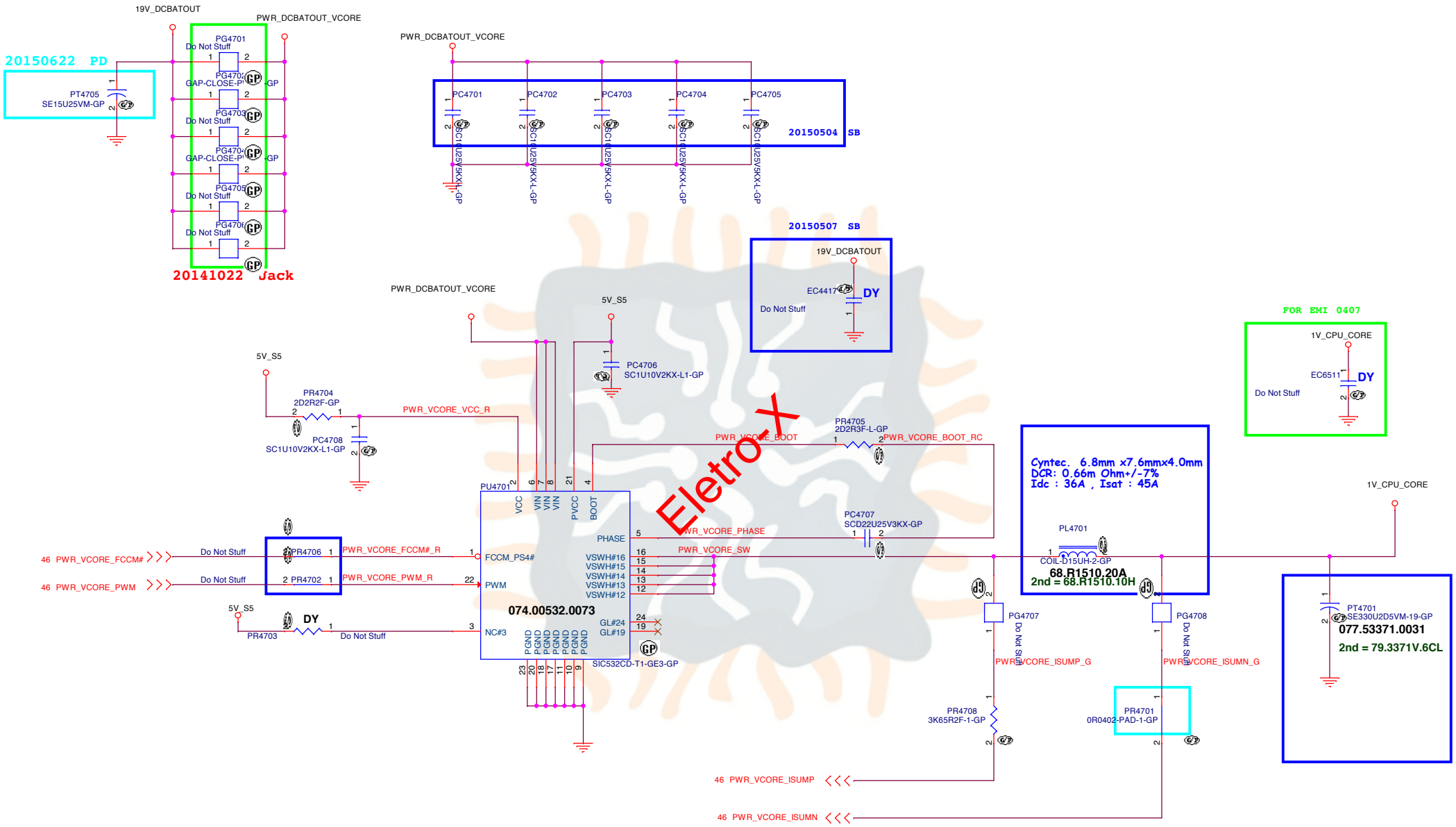
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 40 of 60

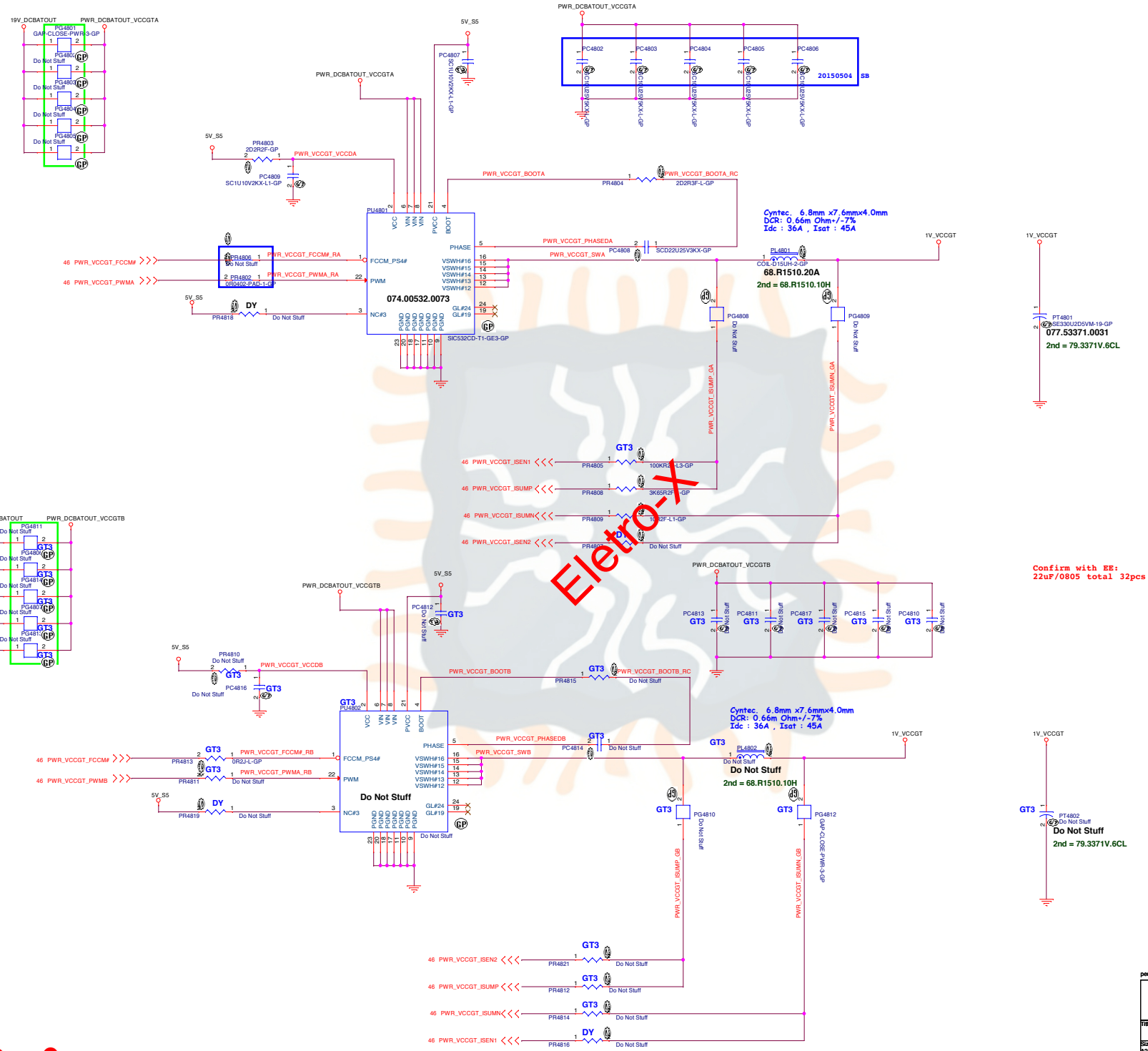
Main Func = CPU_CORE



per MP

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_VCORE(2/3)	
Size: A3	Document Number: Mihawk MB
Rev: 1.3	
Date: Tuesday, June 06, 2017	Sheet 47 of 106

Main Func = CPU_CORE



per MP

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

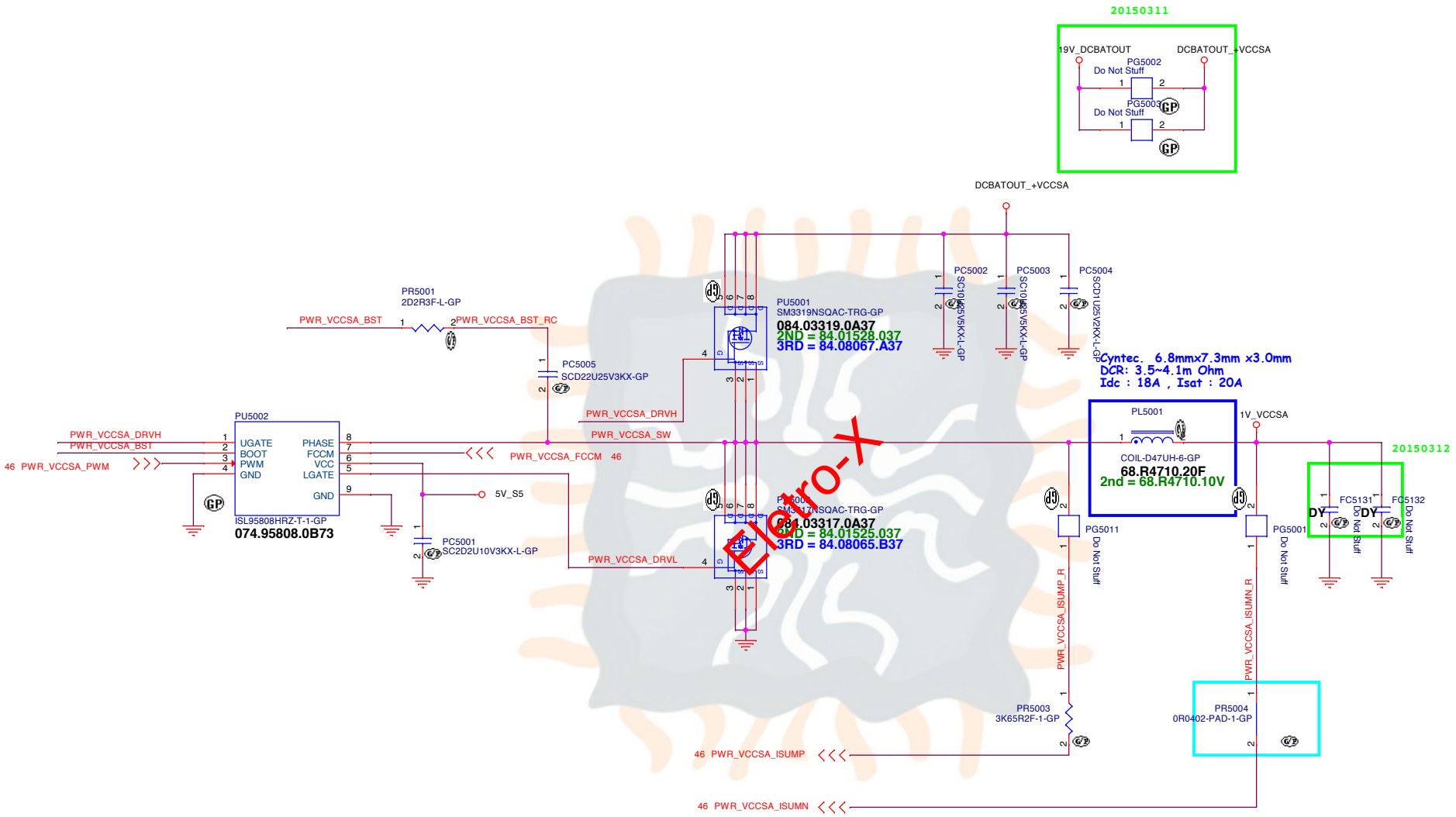
Title: CPU_VCCGT(3/3)

Size: A2 | Document Number: Mihawk MB | Rev: 1.3

Date: Tuesday, June 06, 2017 | Sheet 48 of 63

ECEtRO-Q

Main Func = CPU_CORE



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Wistron Corporation
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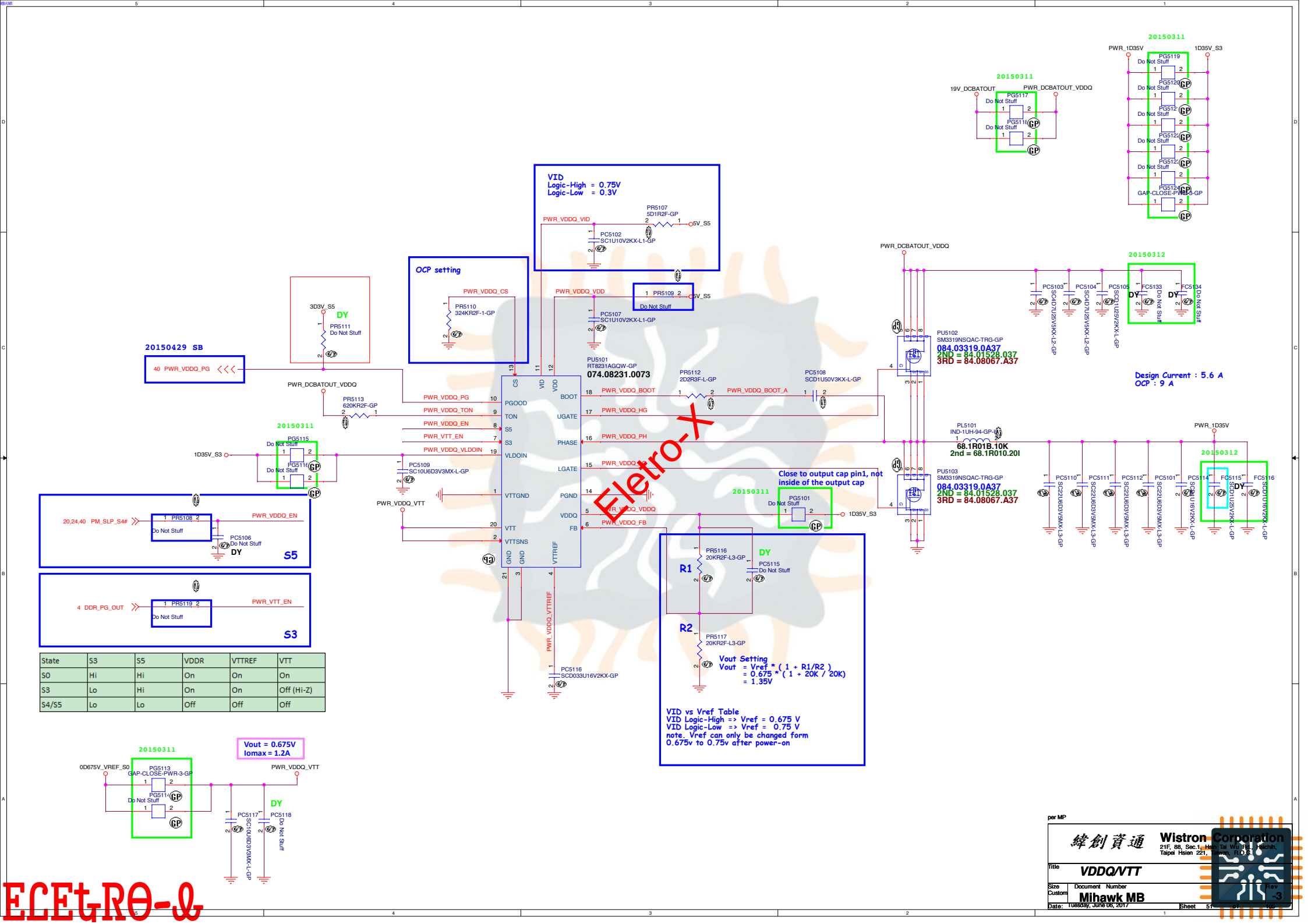
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA	
Size A3	Document Number Mihawk MB	Rev 3
Date: Tuesday, June 06, 2017	Sheet 50	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

per MP

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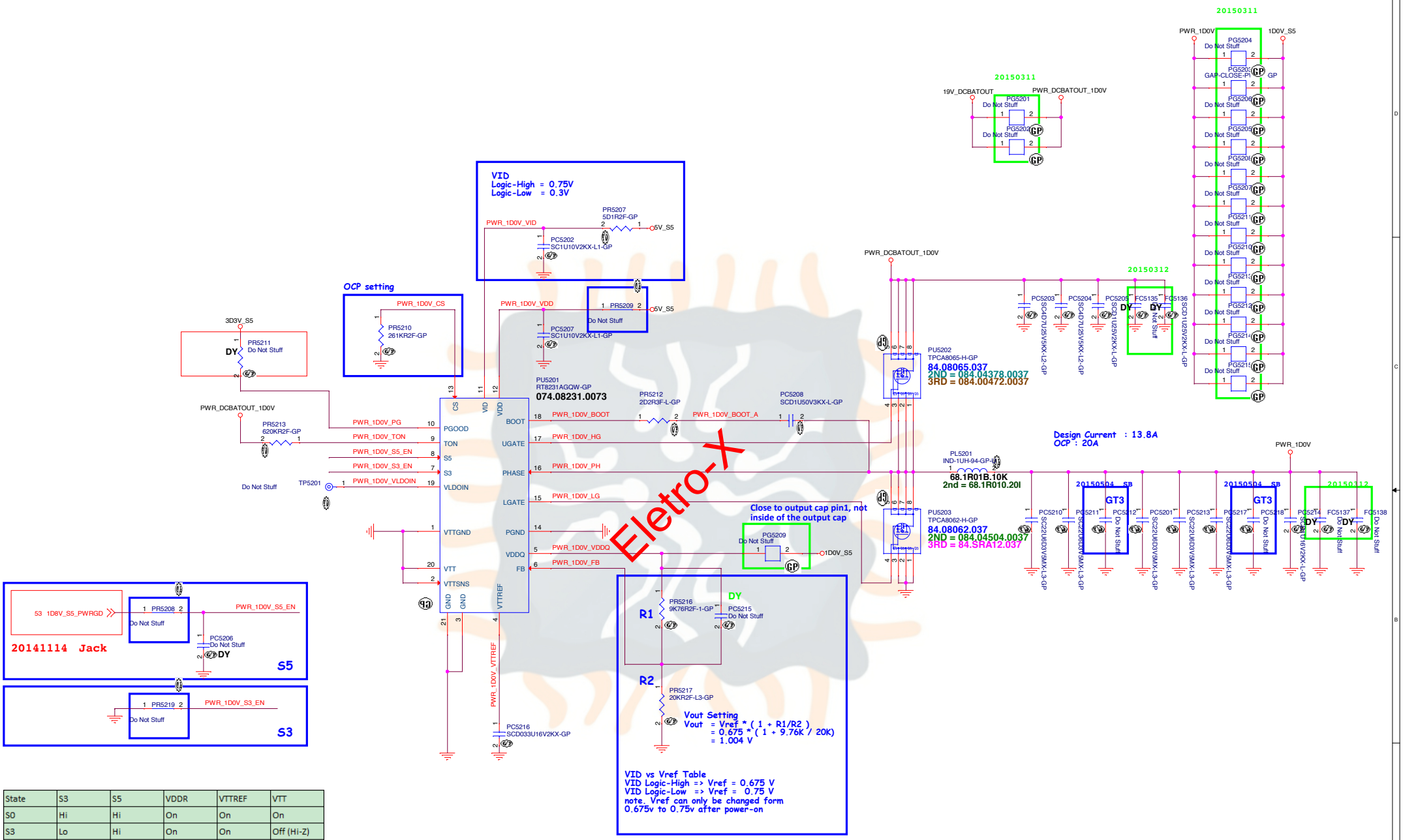
Title: VDDQ/VTT

Size: Custom | Document Number: Mihawk MB | Rev: -3

Date: Tuesday, June 06, 2017 | Sheet 51



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

per MP

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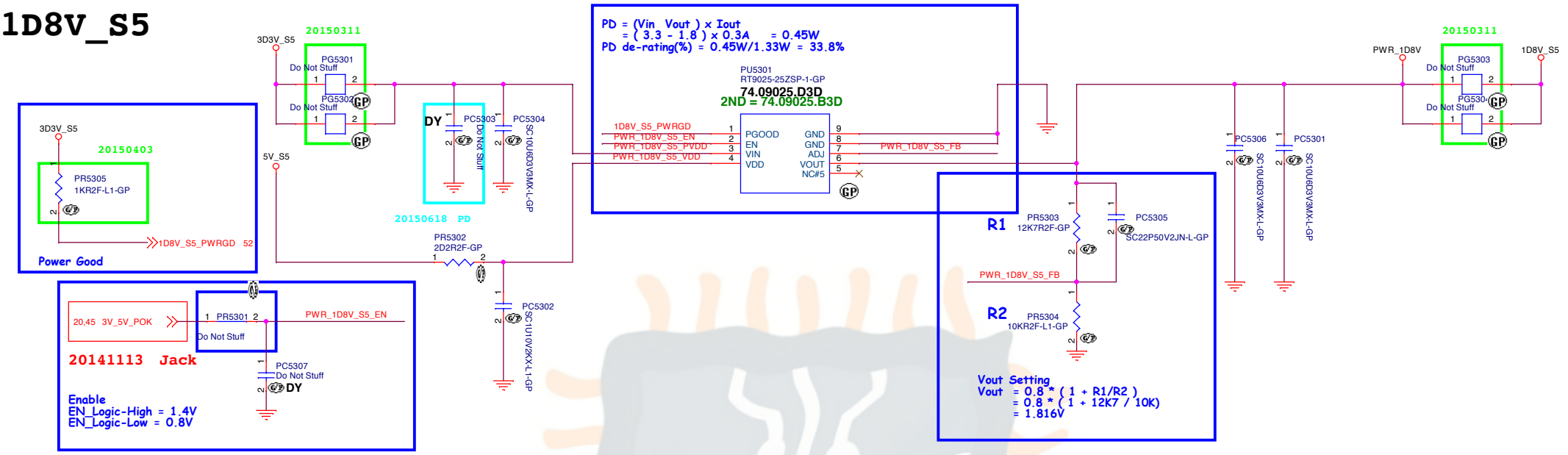
Title: RT8231_1D0V

Size: Custom | Document Number: Mihawk MB | Rev: -3

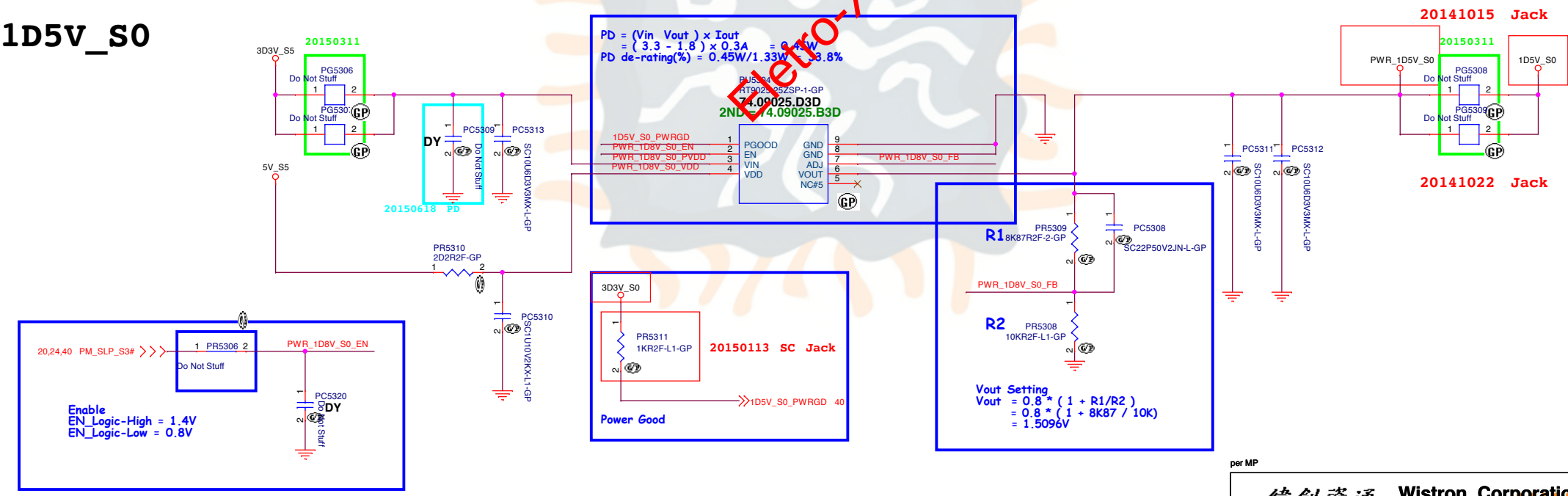
Date: Tuesday, June 06, 2017 | Sheet 52

ECEtRO-L

1D8V_S5



1D5V_S0



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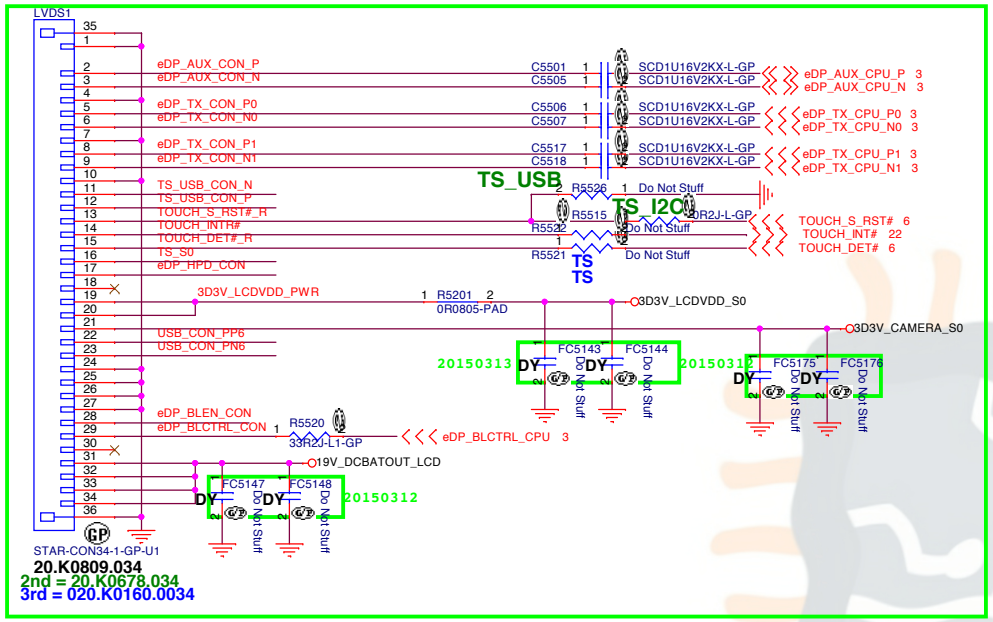
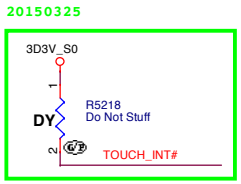
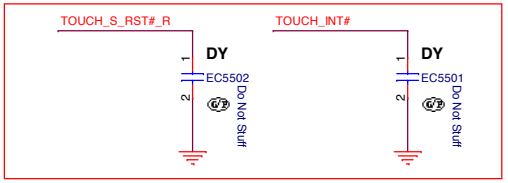
Title	RT8068_1D8V	
Size A3	Document Number Mihawk MB	Rev 3
Date: Tuesday, June 06, 2017	Sheet 53	

Main Func = LCD

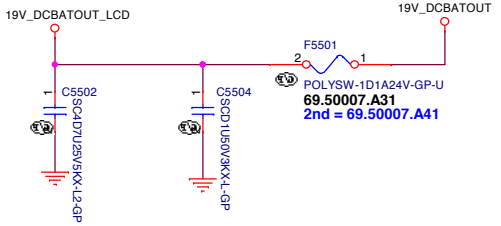


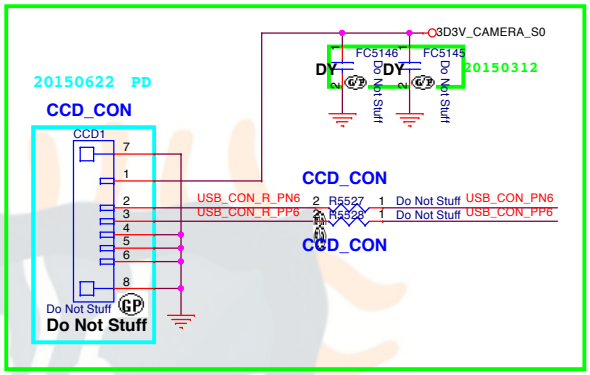


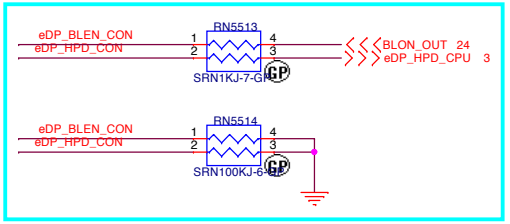


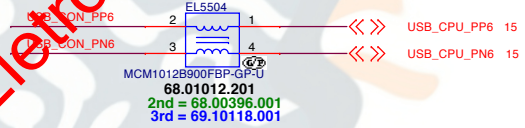
20141016 Jack

Inverter Power

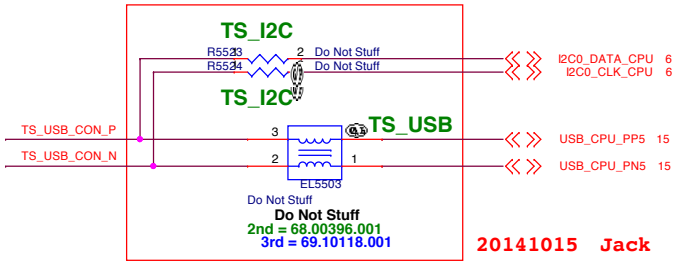




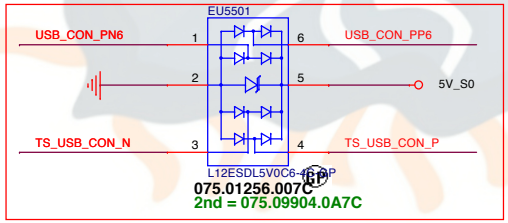




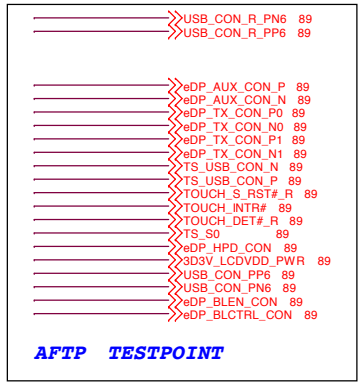
Elero-X



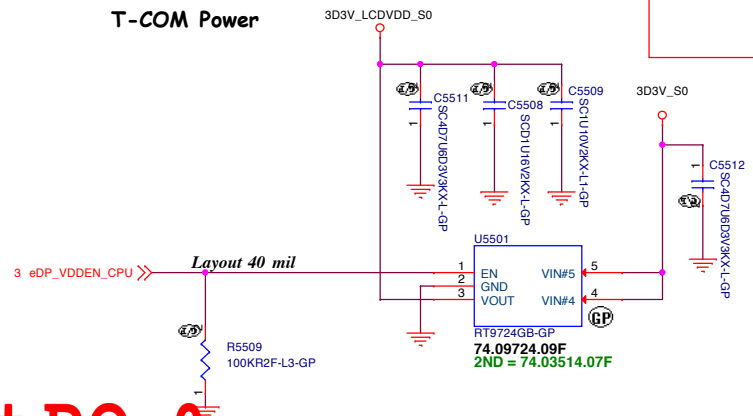
20141015 Jack



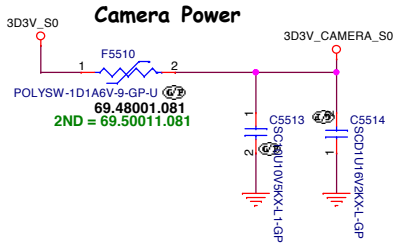
20141016 Jack



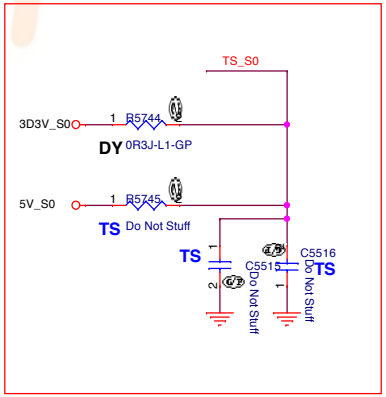
T-COM Power



Camera Power



Touch panel Power



20141015 Jack

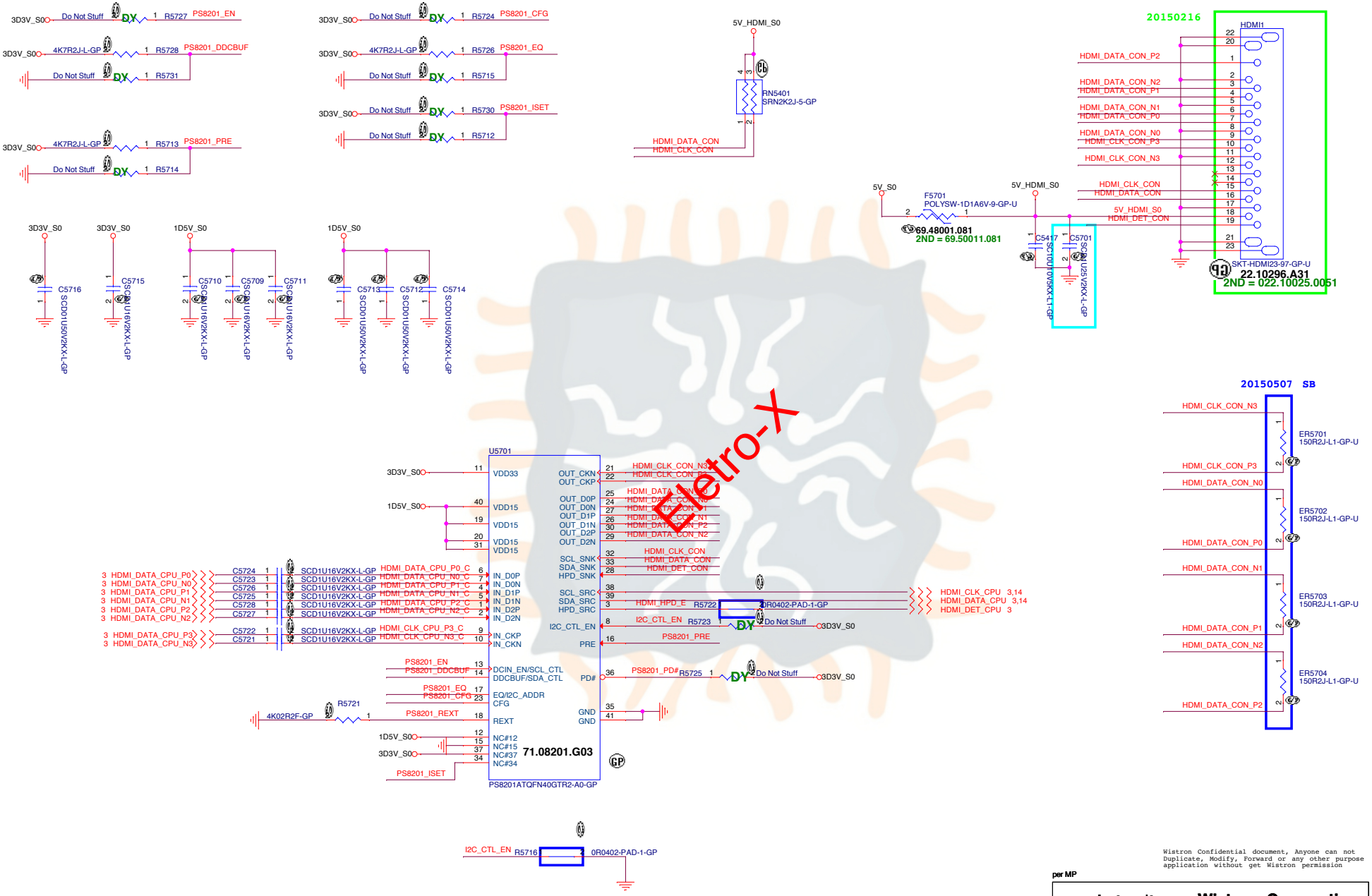
per MP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size: A3	Document Number: Mihawk MB	Rev: -3
Date: Tuesday, June 06, 2017	Sheet 55 of 105	

ECEtR0-L

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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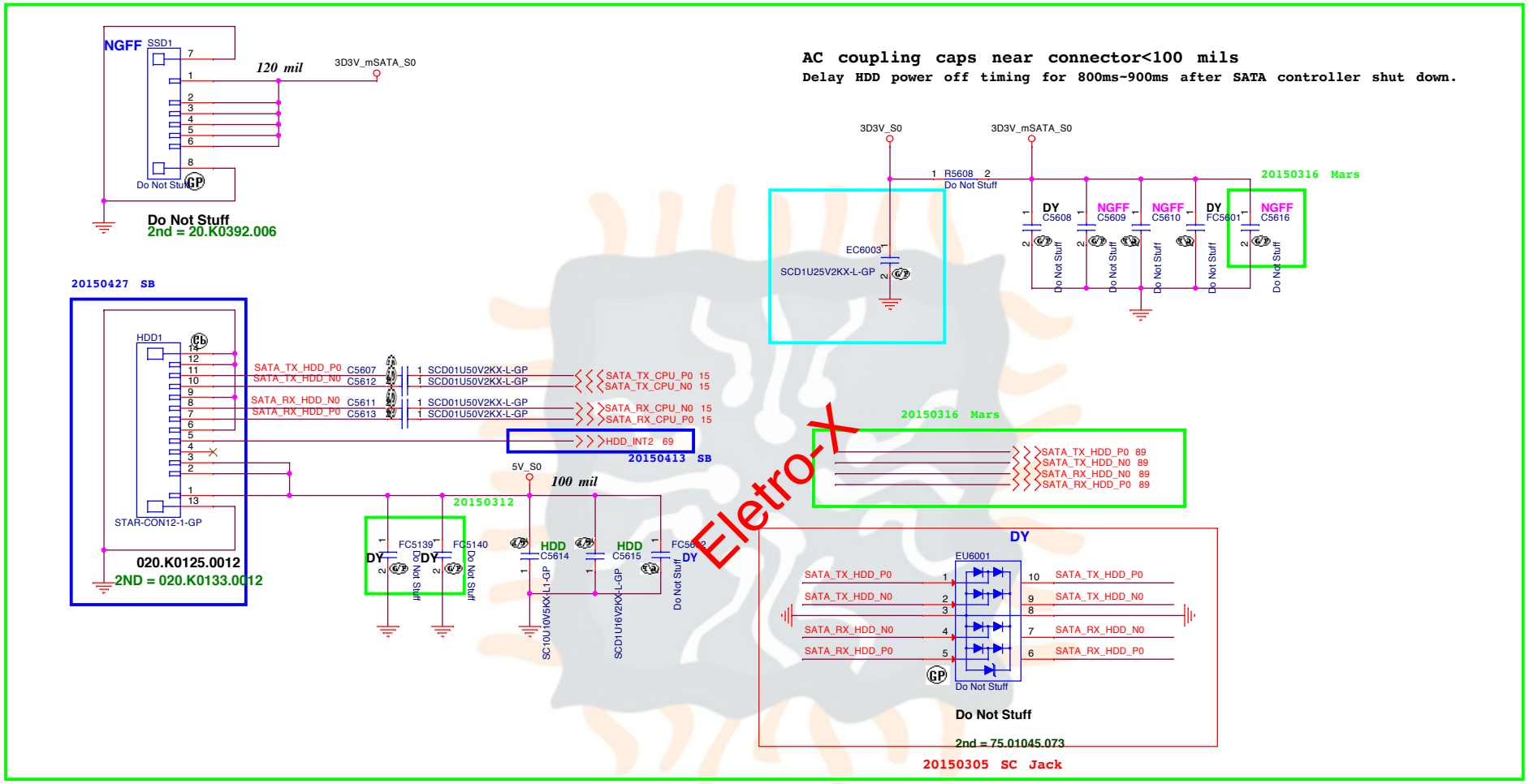
Title	HDMI Level Shifter/Conn	
Size: Custom	Document Number: Mihawk MB	Rev: -3
Date: Tuesday, June 06, 2017	Sheet 57 of 105	

ECEtRO-X

SATA HDD / SSD Connector

20150216



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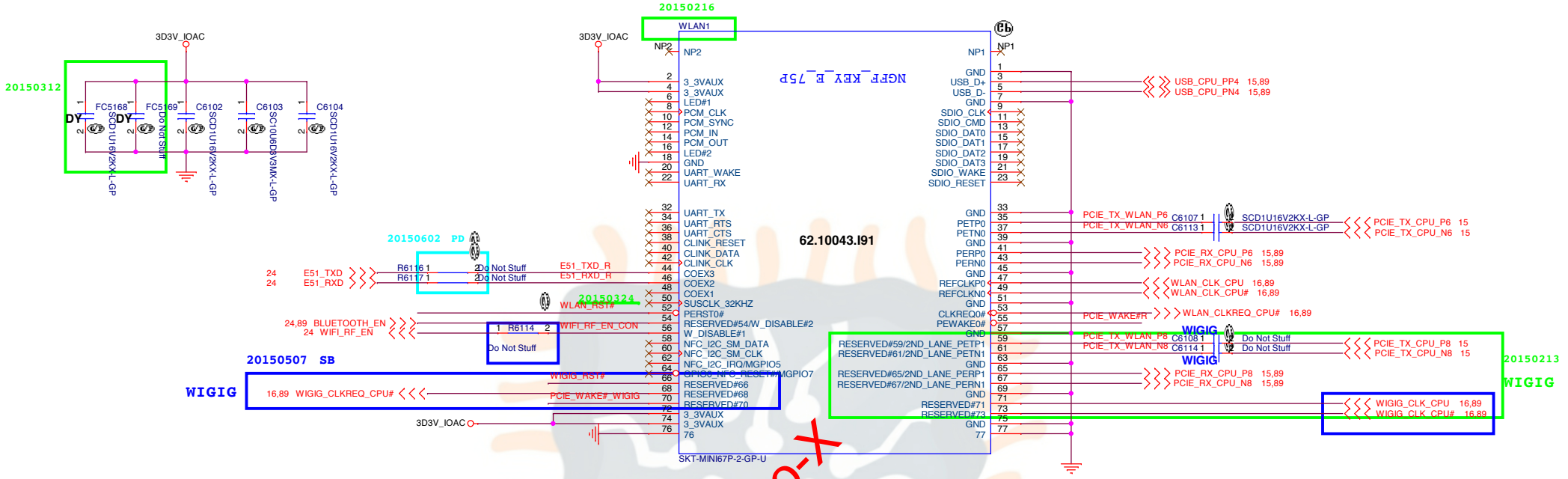
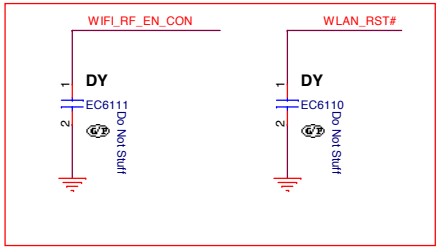
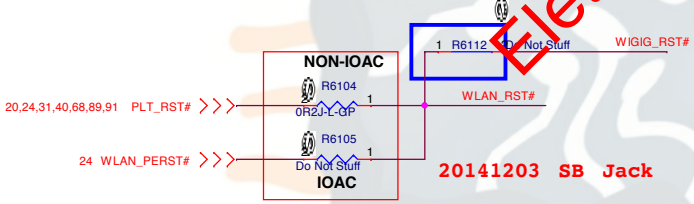
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD / NGFF SSD		
Size: A3	Document Number: Mihawk MB	Rev: -3
Date: Tuesday, June 06, 2017	Sheet 60 of 100	

SSID = Wireless Mini Card Connector(802.11a/b/g/n)

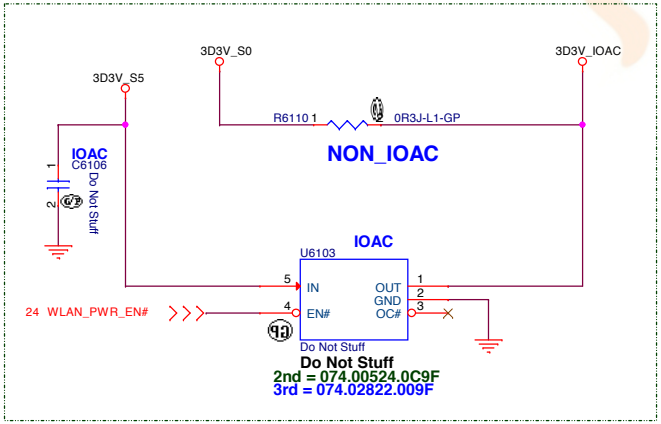


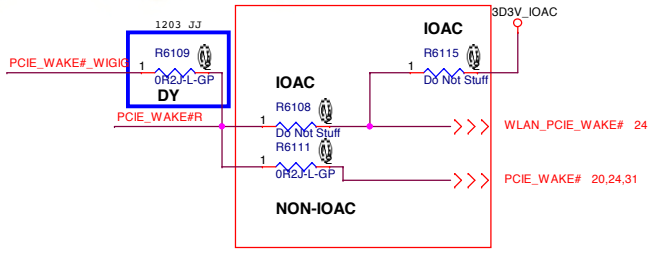


20141016 Jack

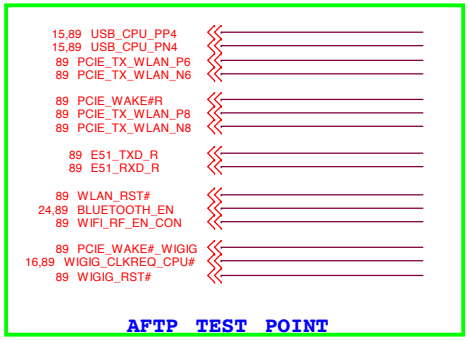


20141203 SB Jack





20141203 SB Jack



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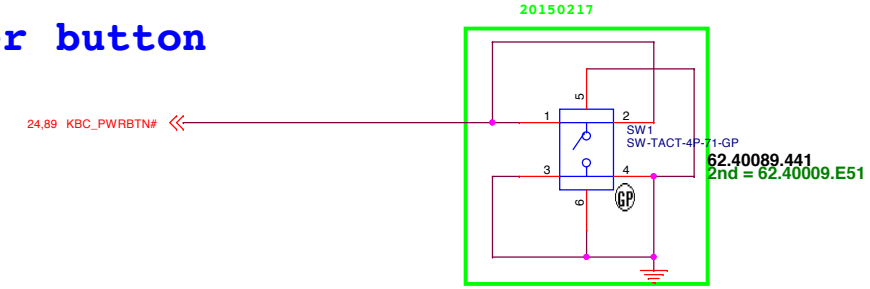
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Mini Card-WLAN	
Size A3	Document Number Mihawk MB	Rev 1.3
Date: Tuesday, June 06, 2017	Sheet 61 of 100	

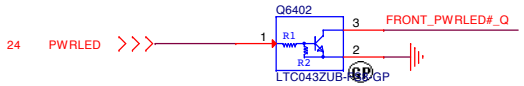
Main Func = Power BTN

Power button

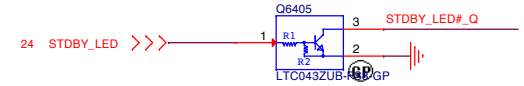


Main Func = Battery LED

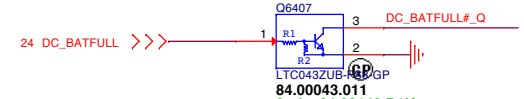
Power Button_LED



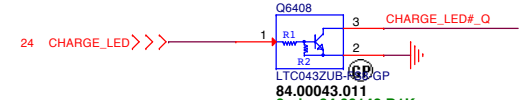
Power STDBY_LED

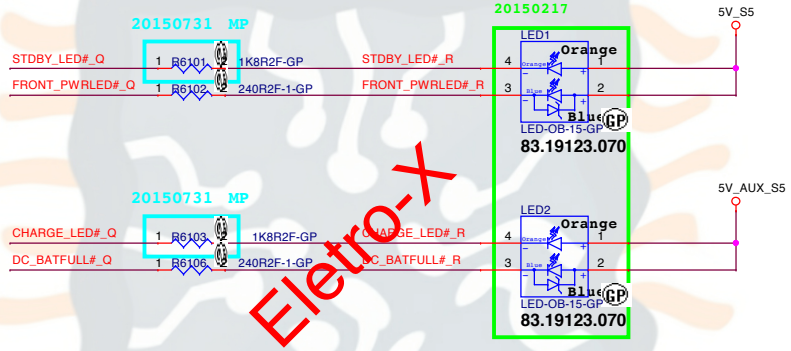


Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)





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Title: LED Bard/Power Button

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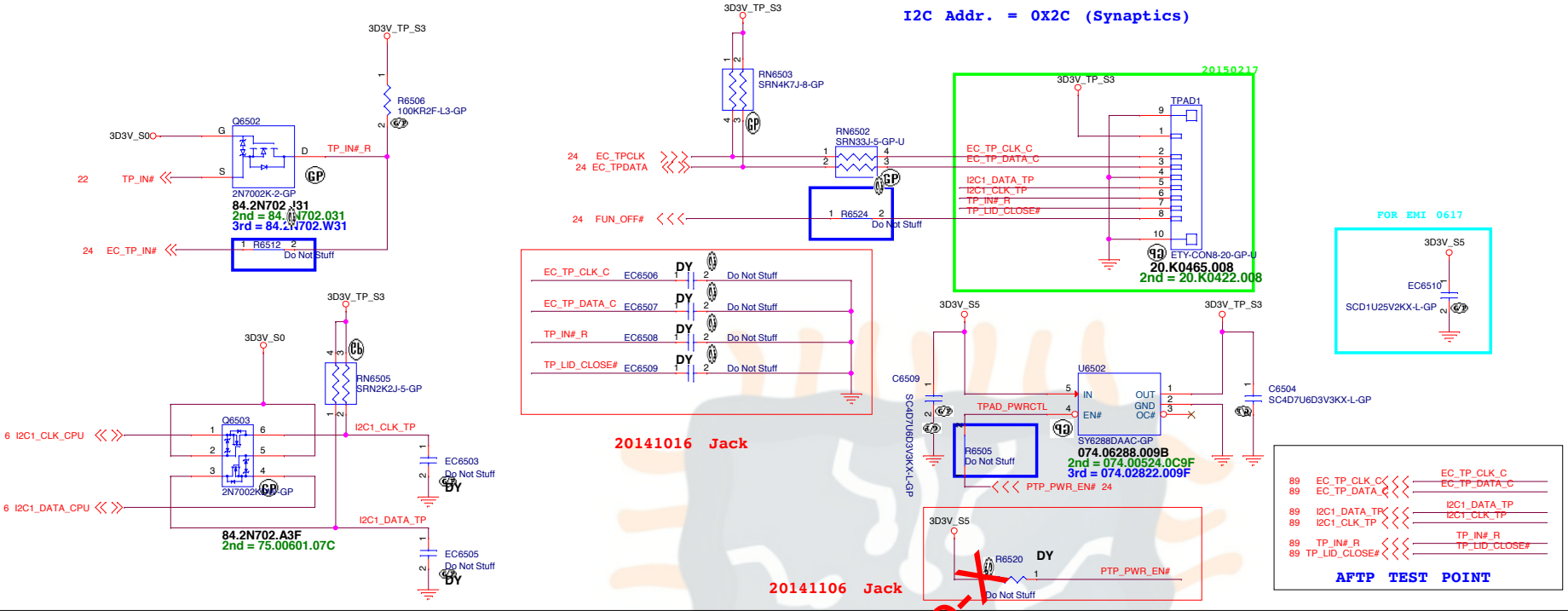
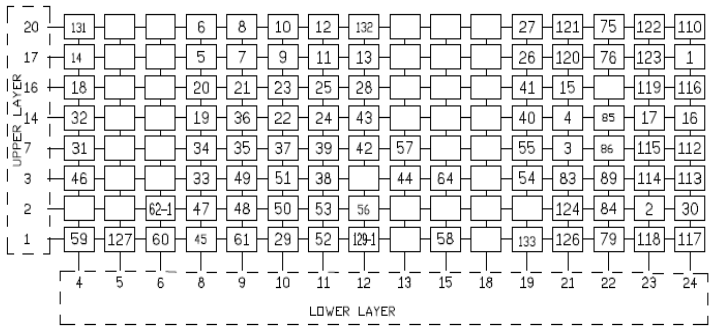
Precision Touch Pad

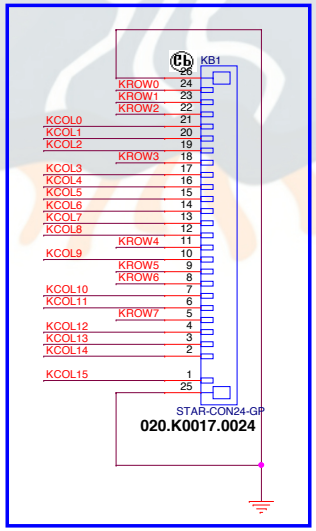
I2C Addr. = 0X2C (Synaptics)



Internal KeyBoard Connector

20150429 SB





KROW0 24,89
KROW1 24,89
KROW2 24,89
KROW3 24,89
KROW4 24,89
KROW5 24,89
KROW6 24,89
KROW7 24,89

KCOL0 24,89
KCOL1 24,89
KCOL2 24,89
KCOL3 24,89
KCOL4 24,89
KCOL5 24,89
KCOL6 24,89
KCOL7 24,89
KCOL8 24,89
KCOL9 24,89
KCOL10 24,89
KCOL11 24,89
KCOL12 24,89
KCOL13 24,89
KCOL14 24,89
KCOL15 24,89

per MP

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Title: Key Board/Touch Pad

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Low Active 2A
RDSon = 80mΩ (Typ)

5V_S5
U6601
IN
EN#
OUT
GND
OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
C6609
SC1U10V2KX-L1-GP
C6604
SCD1U16V2KX-L-GP
DY
C6603
Do Not Stuff
5V_USB
24,37 USB_PWR_EN#

20150331

EU401
USB_CON_PN1_R
USB_CON_PP1_R
USB_CON_PN2_R
USB_CON_PP2_R
5V_USB
L12ESDL5V0C6-4-GP
075.01256.007C
2nd = 075.09904.0A7C

20150511 SB

68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
EL6601
MCM1012B900FBP-GP-U
EL6602
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
15 USB_CPU_PP2
15 USB_CPU_PN2
15 USB_CPU_PP3
15 USB_CPU_PN3
15 USB_CPU_PP7
15 USB_CPU_PN7
ER3304 0R0402-PAD-1-GP
ER3303 Do Not Stuff
USB_CON_PP7_R
USB_CON_PN7_R
3D3V_S0
5V_USB
CRBD1
PTWO-CON26-7-GP
20.K0426.026
AUD_AGND
27,89 RING2
27 AUD_HP1_JD#
27 AUD_HP1_JACK_L2
27 AUD_HP1_JACK_R2
R2921 Do Not Stuff
R2922 63D4R3F-GP
R2923 63D4R3F-GP
AUD_HP1_JD#_R
AUD_HP1_JACK_L2_R
AUD_HP1_JACK_R2_R
20150304
27,89 SELEEVE

Elettro-X

20150310

USB_CON_PN1_R 89
USB_CON_PP1_R 89
USB_CON_PN2_R 89
USB_CON_PP2_R 89
USB_CON_PN7_R 89
USB_CON_PP7_R 89
RING2 27,89
AUD_HP1_JD#_R 89
AUD_HP1_JACK_L2_R 89
AUD_HP1_JACK_R2_R 89

AFTP TESTPOINT

3D3V_S0
EC6603
SCD1U25V2KX-L-GP
EC6604
SCD1U25V2KX-L-GP

per MP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad
Size: A4
Document Number: Mihawk MB
Rev: -3
Date: Tuesday, June 06, 2017
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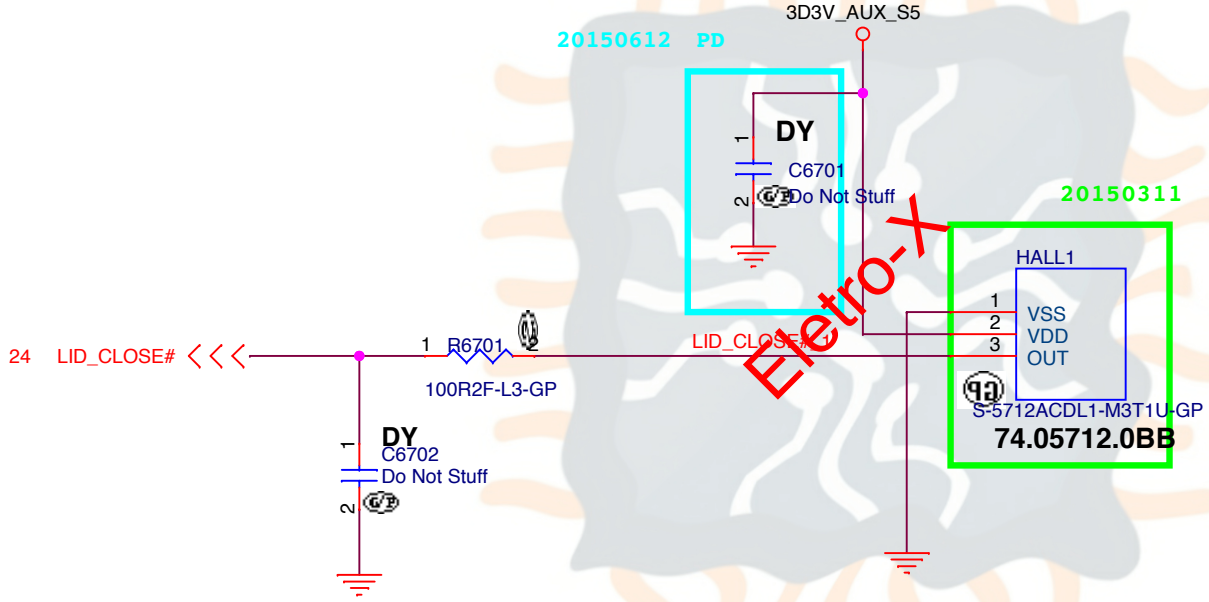
ECEtRO-L



per MP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Security Guard connector***

Size	Document Number	Rev
A	**Mihawk MB**	-3

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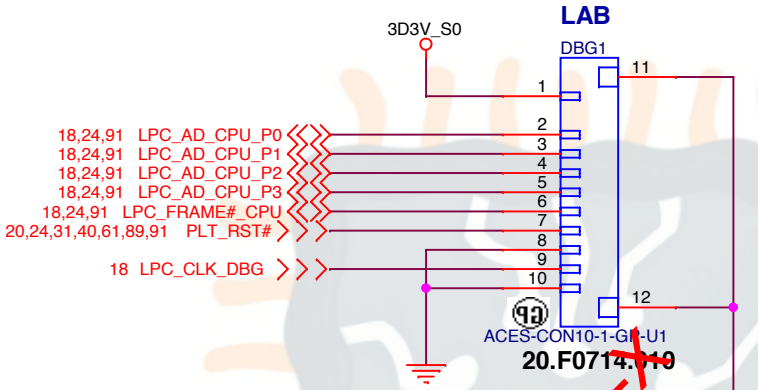

per MP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Dubug connector***
Size A4	Document Number **Mihawk MB** Rev -3
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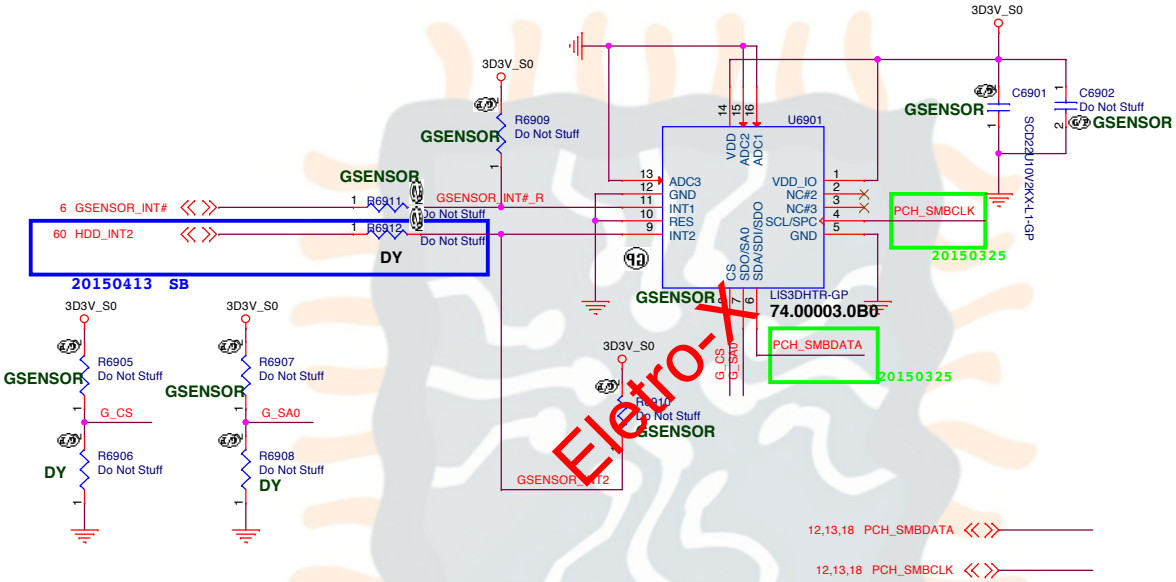
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title	G-SENSOR	
Size A3	Document Number Mihawk MB	Rev 1.3
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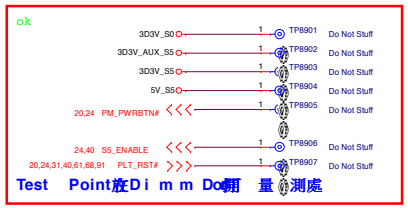
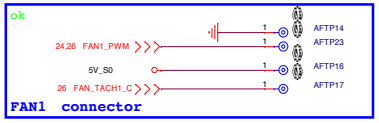
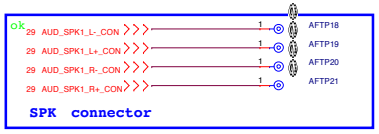
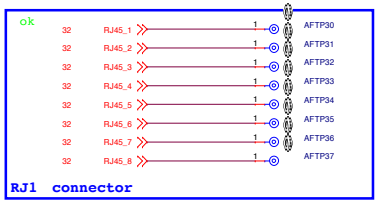
Check test point

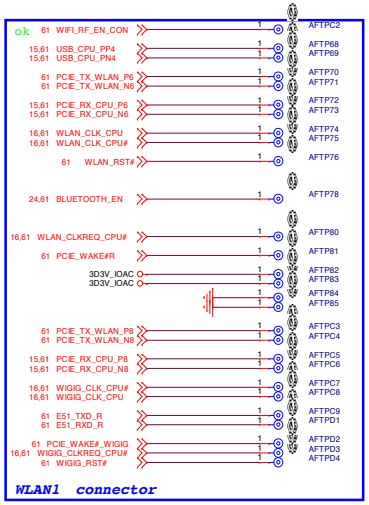


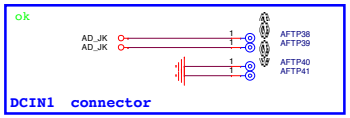
20141103 Jack

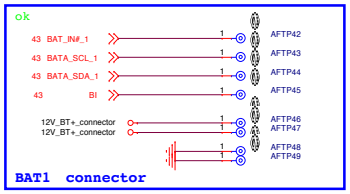


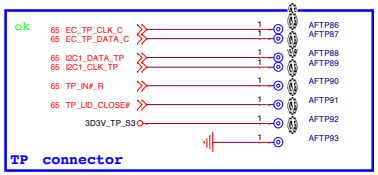


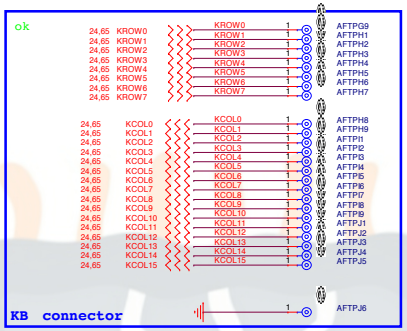


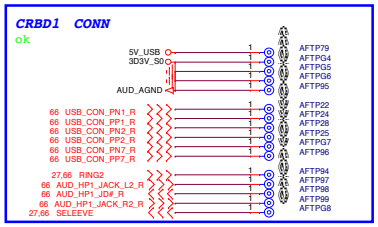


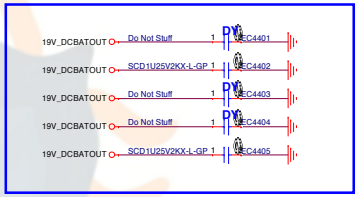


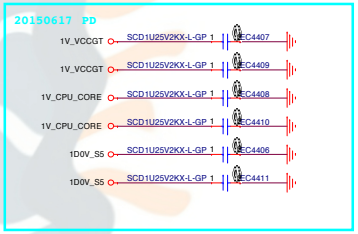


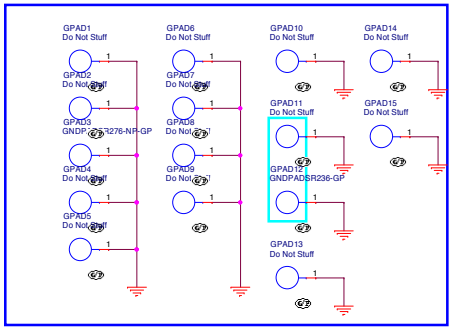


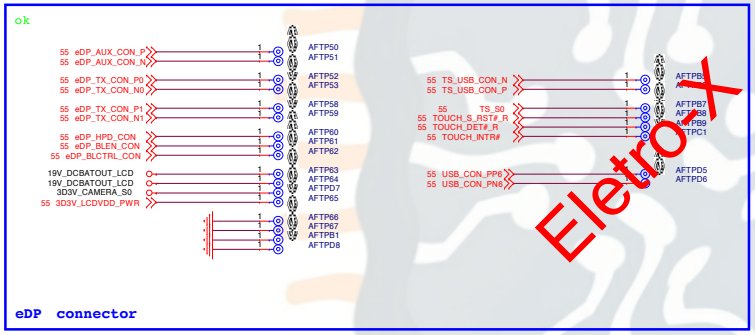


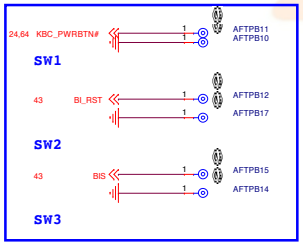


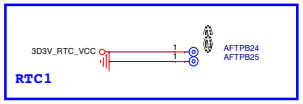






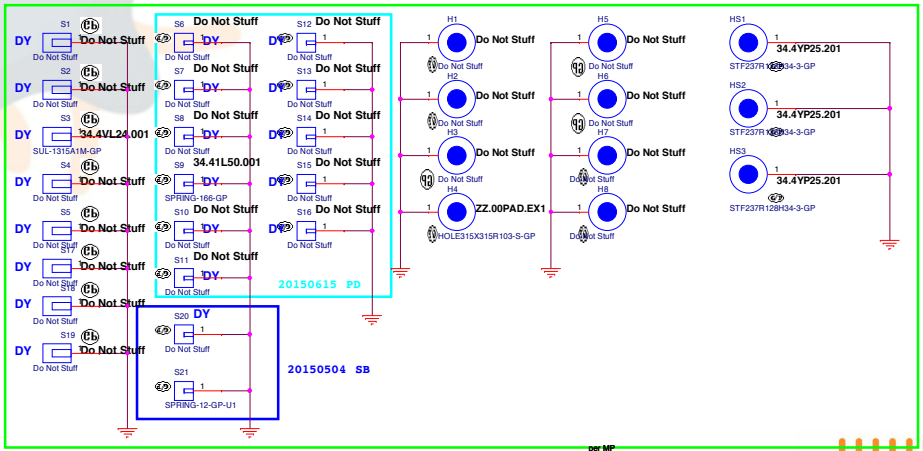






Elettro X

USB RF CLIP SO-DIMM RF CLIP 20150408



per MF

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Title: UNUSED PARTS/EMI Capacitors

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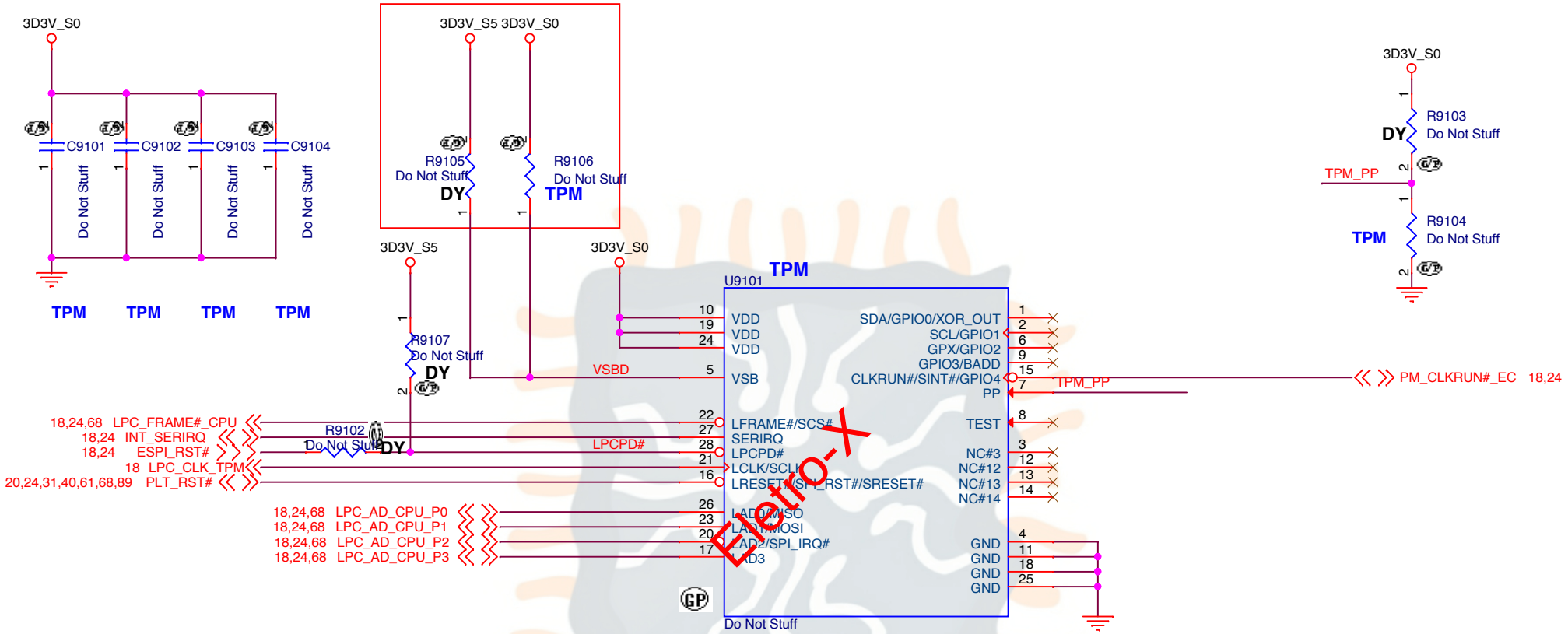
ECEtRO-Q



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Title	TPM	
Size A4	Document Number Mihawk MB	Rev -3
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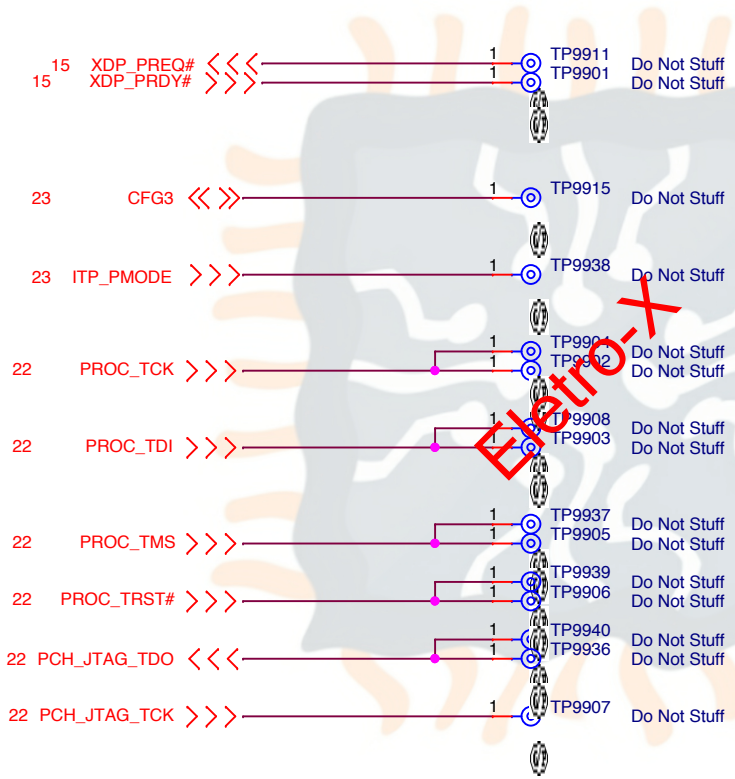
ECEtRO-L

Main Func = Debug



per MP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_XDP***

Size: A4 | Document Number: **Mihawk MB** | Rev: -3

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