Page	Title of schematic page	Rev.	Date
01	Page List	1A	
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03	Change List	1A	
04	IVY 1/4(HOST&PCIE)	1A	
05	IVY 2/4(DDR3 I/F)	1A	
06	IVY 3/4(POWER)	1A	
07	IVY 4/4(GND/Strap)	1A	
08	PCH 1/6(DMI/FDI/VIDEO)	1A	
09	PCH 2/6(SATA/RTC/HDA/LPC)	1A	
10	PCH 3/6(PCIE/USB/CLK/NV)	1A	
11	PCH 4/6(GPIO/CPU/STRAP)	1A	
12	PCH 5/6(POWER)	1A	
13	PCH 6/6 (GND)	1A	
14	DDR3 DIMM-0-STD	1A	
15	DDR3 DIMM-1-STD	1A	
16	WPCE985L & FLASH	1A	
17	LVDS/CAMERA	1A	
18	CARD READER(RTS5209)	1A	
19	HDMI/THERMAL	1A	
20	USB	1A	
21	LAN (RTL8111GS)	1A	
22	WLAN/KB-BL	1A	
23	HDD/ODD/G-SENSOR/TP/FAN	1A	
24	Audio ALC233-CG	1A	
25	LED/PS/DMIC	1A	
26	POWER +VCC_CORE (ISL95835)	1A	
27	POWER 3VPCU&RVCC5(PM6686)	1A	
28	POWER 1.5VSUS/VTT_MEM	1A	
29	POWER +1.05V(G5602R41U)-15A	1A	
30	POWER VCCSA/VCCIO	1A	
31	POWER VCC1.8/Thermal	1A	
32	POWER(BAT IN / ADA IN/ UL)	1A	
33	POWER CHARGER (ISL88731C)	1A	
34	POWER VGA_CORE(RT8812A)	1A	
35	POWER VCC1.5_VRAM/1.05V	1A	
36	NVIDIA N14 GB2-64 PCIE 1/4	1A	
37	NVIDIA N14 GB2-64 TMDS 2/4	1A	
38	NVIDIA N14 GB2-64 VRAM 3/4	1A	
39	NVIDIA N14 GB2-64 VRAM 4/4	1A	

Page	Title of schematic page	Rev.	Date
42	HOLE/EMI/KB	1A	
43	AUDIO Woofer	1A	
44	IO PORT LIST	1A	
		1A	

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

1

Chief River ULV BLOCK DIAGRAM

02

DDR3L : 1.35V
DDR3 : 1.5V

Dual Channel

P14~P15

DDR SYSTEM MEMORY

intel

Ivy Bridge

PCI-E X16

BGA1023

(31mm X 24mm)

FDI DMI

P4~P7

PCIE3 5GT/s

Nvidia

N14P-GV2 P36 ~ P39

VRAM 1GB / 2GB P38~P39

X8 2.7GT/s FDI

DMI X4 5GT/s

TOUCH SCREEN P17 PORT8

Camera P17 PORT10

WiMax/BT P22 PORT9

USB I/O P20 PORT3

USB I/O P20 PORT2

USB I/O P20 PORT1

USB I/O P20 PORT0

USB 2.0

USB 3.0

P23 HDD SATA0 6Gb/s

P23 ODD SATA3 3Gb/s

intel

<PCH>

Panther Point

mBGA 989

(25mm X 25mm)

FDI DMI

SATA Gen3

SATA Gen2

USB

HDA

SPI

iGFX Interfaces

P8~P13

Elettro-X

LVDS/eDP

P17

HDMI

P19

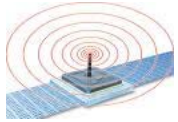
5GT/s PCI-Express Gen2

PCIE3 PCIE1 PCIE4

Giga-LAN RTL8111GS P21

RJ45

P21



WLAN/BT P21

Card Reader RTS5209 P18

SD-XC

NFC

I2C

Azalia

Audio CODEC ALC233-CG P24

HP Jack MIC Jack SPK DMIC

P24

P24

P24

P24

SPI ROM 8MB P9

LPC

EC NPCE985L P16

Touch Pad P23

Keyboard P42

Power LED
Sleep LED
SATA LED
Battery LED
CAPSLED
NUMLED

Button
ASSIST#
Power SW

ECEtRO-X

Change List

MB_SCH_PVT_001

P22-Add R333 0_6S.

P22- U15 don't mount

P22-Add Q32(2N7002).

P22-Add R335(100K_4).

Reason : Modify circuit for KB Backlight.
Possible Risk: No.

MB_SCH_PVT_002

P23-CON11.11 delete net"DATA_ODD_DA#

P10-U17.G40 delete net"SATA_ODD_DA#".

P10-Delete R64(10K_4).

Reason : Modify circuit for Zero Power ODD.
Possible Risk: No.

MB_SCH_PVT_002

P08-ADD 0.1UF on "PCH_PWROK_EC"

Reason : Modify circuit for ESD.
Possible Risk: No.

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PROJECT : Chief River

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	Change List	1A
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Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

04

U16A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

eDP

IC,IVB_2CBGA,0P7

U16B

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,IVB_2CBGA,0P7

SNB_IVB#:
- It is NC when using Sandy Bridge.(1.05V)
- For next generation processor it will be grounded in package.(1.0V)

FDI Disabling (Discrete Only)

-FDI_FSYNC (J18/J17/J19/H17) can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).
- FDI_INT connect to GND with 1K ohm.

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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PROJECT :Chief River

Size	Document Number	Rev
	SNB/IVB 1/4	1A
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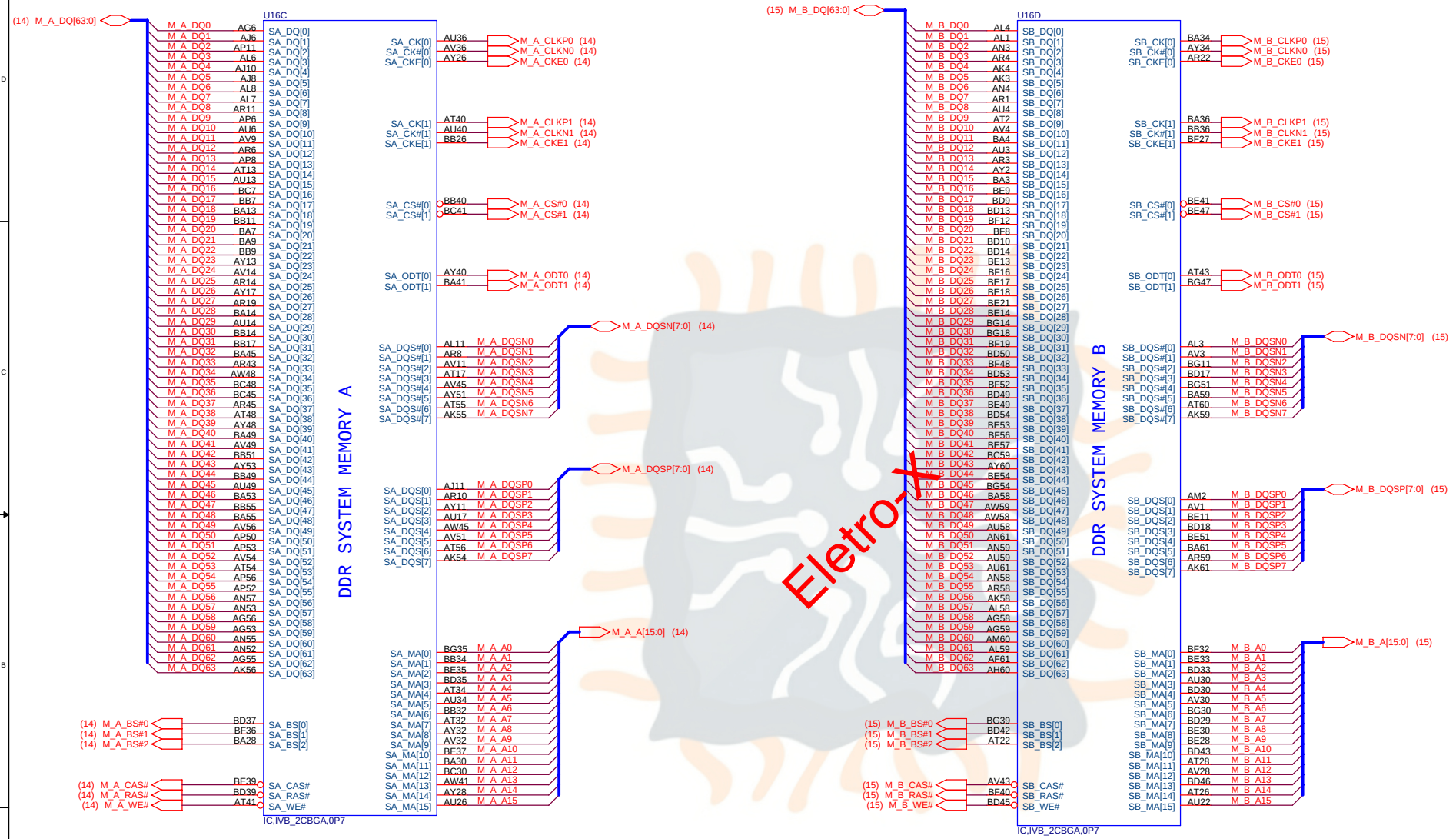
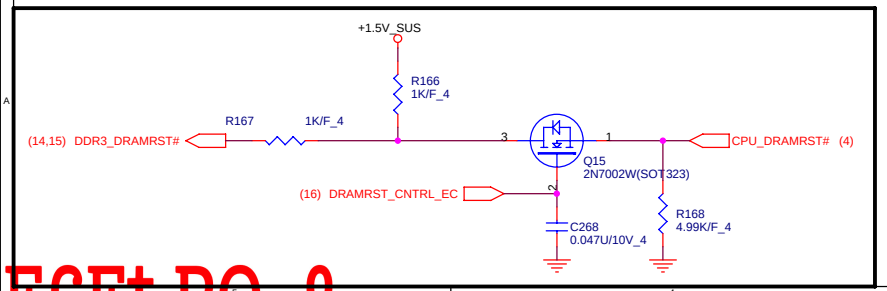
Ivy Bridge Processor (DDR3)





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	SNB/IVB 2/4	1A
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ECEtRO-X

Ivy Bridge Processor (POWER)

Ivy Bridge Processor (GRAPHIC POWER)

06

POWER

CPU Core Power

(33A)

+VCC_CORE

U16F

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

+1.05V

(7.1A)

C90 10U/6.3V/X5R_6
C110 10U/6.3V/X5R_6
C91 10U/6.3V/X5R_6
C118 10U/6.3V/X5R_6
C89 10U/6.3V/X5R_6
C85 10U/6.3V/X5R_6

C127 10U/6.3V/X5R_6
C129 10U/6.3V/X5R_6
C130 10U/6.3V/X5R_6
C88 10U/6.3V/X5R_6
C111 10U/6.3V/X5R_6
C117 10U/6.3V/X5R_6
C132 10U/6.3V/X5R_6
C128 10U/6.3V/X5R_6
C87 10U/6.3V/X5R_6
C86 10U/6.3V/X5R_6
C92 10U/6.3V/X5R_6
C108 10U/6.3V/X5R_6
C131 10U/6.3V/X5R_6
C119 10U/6.3V/X5R_6

C397 10U/6.3V/X5R_6
C142 10U/6.3V/X5R_6
C204 10U/6.3V/X5R_6
C202 10U/6.3V/X5R_6
C161 10U/6.3V/X5R_6
C153 10U/6.3V/X5R_6
C154 10U/6.3V/X5R_6
C191 10U/6.3V/X5R_6
C398 10U/6.3V/X5R_6
C146 10U/6.3V/X5R_6

C145 1U/6.3V/X5R_4
C192 1U/6.3V/X5R_4
C200 1U/6.3V/X5R_4
C172 1U/6.3V/X5R_4
C174 1U/6.3V/X5R_4
C411 1U/6.3V/X5R_4
C402 1U/6.3V/X5R_4
C420 1U/6.3V/X5R_4
C421 1U/6.3V/X5R_4
C188 1U/6.3V/X5R_4

C177 1U/6.3V/X5R_4
C184 1U/6.3V/X5R_4
C168 1U/6.3V/X5R_4

C179 1U/6.3V/X5R_4
C136 1U/6.3V/X5R_4
C171 1U/6.3V/X5R_4
C141 1U/6.3V/X5R_4
C158 1U/6.3V/X5R_4
C181 1U/6.3V/X5R_4

VCCIO_SEL — Output for +1.05V or +1.0V

VCCPQE[1] VCCPQE[2] — 0.4A — +1.05V — C156 1U/6.3V/X5R_4

VIDALERT# — H_CPU_SVIDALRT#
VIDSCLK — H_CPU_SVIDCLK
VIDSOUT — H_CPU_SVIDDAT

R32 100/F_4 +VCC_CORE — VCC_SENSE (26)
R31 100/F_4 — VSS_SENSE (26)

R81 10/F_4 +1.05V — VCCP_SENSE (29)
R79 10/F_4 — VSSP_SENSE (29)

HOLE1

*Intel-CPU-bracket

IC,IVB_2CBGA,0P7

POWER

U16G

(25A)

+VCC_GFX

PDC: 10ux8

C427 10U/6.3V/X5R_6
C122 10U/6.3V/X5R_6
C418 10U/6.3V/X5R_6
C417 22U/6.3V/X5R_8
C137 22U/6.3V/X5R_8
C157 22U/6.3V/X5R_8
C148 10U/6.3V/X5R_6
C166 22U/6.3V/X5R_8

C175 10U/6.3V/X5R_6
C426 22U/6.3V_8

VREF

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

R89 1K/F_4 +1.5V_CPU
(Trace=10mil) +VDDR_REF_CPU
R83 1K/F_4
C207 0.1U/10V/X5R_4

(4.75A)

+1.5V_CPU

C149 10U/6.3V/X5R_6
C240 10U/6.3V/X5R_6
C176 10U/6.3V/X5R_6
C150 10U/6.3V/X5R_6
C152 10U/6.3V/X5R_6
C151 10U/6.3V/X5R_6

C189 1U/6.3V/X5R_4
C187 1U/6.3V/X5R_4
C164 1U/6.3V/X5R_4
C193 1U/6.3V/X5R_4

GRAPHICS DDR3 - 1.5V RAILS

+VCC_GFX R39 100_4 — (26) VCC_AXG_SENSE
(26) VSS_AXG_SENSE
R38 100_4

SENSE LINES

QUIET RAILS

(0.6A) — +1.5V_CPU

C165 1U/6.3V/X5R_4

(0.93A)

+1.8V

C432 10U/6.3V/X5R_6
C433 1U/6.3V/X5R_4
C434 1U/6.3V/X5R_4

1.8V RAIL

+VCCSA

(4.5A)

C115 10U/6.3V/X5R_6
C125 10U/6.3V/X5R_6
C391 10U/6.3V/X5R_6
C392 *10U/6.3V/X5R_6

C113 1U/6.3V/X5R_4
C114 1U/6.3V/X5R_4
C124 1U/6.3V/X5R_4

SA RAIL

SENSE LINES

VCCSA_SENSE — U10 — VCCUSA_SENSE (30)

VCCSA VID lines

VCCSA_VID[0] — D48 — VCCSA_VID0 (30)
VCCSA_VID[1] — D49 — VCCSA_VID1 (30)

IC,IVB_2CBGA,0P7

HR/CR: HR(VID1 only) CR(VID0&VID1)

VCCIO_SEL:
Sandy is High = 1.05V
Ivy is Low = 1.0V

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
+1.05V
Close to VR
R57 54.9/F_4
H_CPU_SVIDCLK R211 0_4 VR_SVID_CLK (26)
(50 ohm)

Place PU resistor close to CPU
SVID DATA
+1.05V
R212 130/F_4
Close to VR
R66 130/F_4
H_CPU_SVIDDAT R213 0_4 VR_SVID_DATA (26)
(50 ohm)

Place PU resistor close to CPU
SVID ALERT
+1.05V
R215 75/J_4
H_CPU_SVIDALRT# R214 43_4 R216 0_4 VR_SVID_ALERT# (26)
(50 ohm)

SNB:6A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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PROJECT :Chief River

Size	Document Number	Rev
	SNB/IVB 3/4	1A
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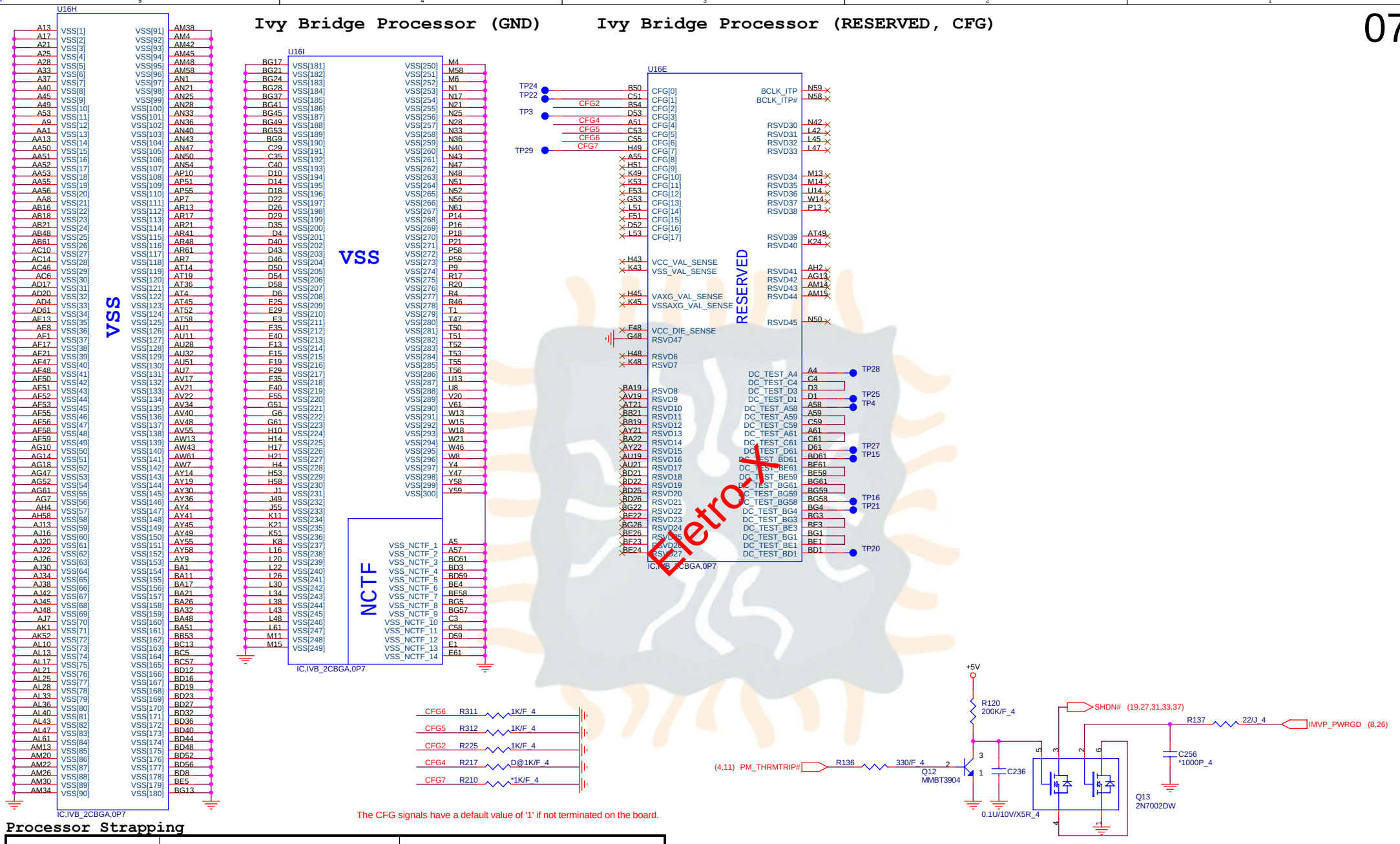
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)



The CFG signals have a default value of '1' if not terminated on the board.

Processor Strapping

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enableddisabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Size	Document Number	Rev
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CPT/PPT (DMI,FDI,PM)

U17C

DMI0RXN BC24 ← (4) DMI_RXN0
DMI1RXN BE20 ← (4) DMI_RXN1
DMI2RXN BG18 ← (4) DMI_RXN2
DMI3RXN BG20 ← (4) DMI_RXN3
DMI0RXP BE24 ← (4) DMI_RXP0
DMI1RXP BC20 ← (4) DMI_RXP1
DMI2RXP BJ18 ← (4) DMI_RXP2
DMI3RXP BJ20 ← (4) DMI_RXP3
DMI0TXN AW24 ← (4) DMI_TXN0
DMI1TXN AW20 ← (4) DMI_TXN1
DMI2TXN BB18 ← (4) DMI_TXN2
DMI3TXN AV18 ← (4) DMI_TXN3
DMI0TXP AY24 ← (4) DMI_TXP0
DMI1TXP AY20 ← (4) DMI_TXP1
DMI2TXP AY18 ← (4) DMI_TXP2
DMI3TXP AU18 ← (4) DMI_TXP3

DMI_ZCOMP BJ24 — R251 49.9/F_4 — DMI_COMP — +1.05V
DMI_IRCOMP BG25
DMI2RBIAS BH21 — R252 750/F_4 — DMI2RBIAS

DMI

FDI_RXN0 BJ14 → FDI_TXN0 (4)
FDI_RXN1 AY14 → FDI_TXN1 (4)
FDI_RXN2 BE14 → FDI_TXN2 (4)
FDI_RXN3 BH13 → FDI_TXN3 (4)
FDI_RXN4 BC12 → FDI_TXN4 (4)
FDI_RXN5 BJ12 → FDI_TXN5 (4)
FDI_RXN6 BG10 → FDI_TXN6 (4)
FDI_RXN7 BG9 → FDI_TXN7 (4)
FDI_RXP0 BG14 → FDI_TXP0 (4)
FDI_RXP1 BB14 → FDI_TXP1 (4)
FDI_RXP2 BF14 → FDI_TXP2 (4)
FDI_RXP3 BG13 → FDI_TXP3 (4)
FDI_RXP4 BE12 → FDI_TXP4 (4)
FDI_RXP5 BG12 → FDI_TXP5 (4)
FDI_RXP6 BJ10 → FDI_TXP6 (4)
FDI_RXP7 BH9 → FDI_TXP7 (4)

FDI

FDI_INT AW16 → FDI_INT (4)
FDI_FSYNC0 AV12 → FDI_FSYNC0 (4)
FDI_FSYNC1 BC10 → FDI_FSYNC1 (4)
FDI_LSYNC0 AV14 → FDI_LSYNC0 (4)
FDI_LSYNC1 BB10 → FDI_LSYNC1 (4)

DSWVRMEN A18 ← DSWVREN

System Power Management

(16) SUSACK# C12 ← SUSACK#
(4) XDP_DBRST# ← XDP_DBRST# K3 ← SYS_RESET#
(7,26) IMVP_PWRGD — R117 22/J_4 — C231 1000P/50V/X7R/10% 4 — SYS_PWROK P12 ← SYS_PWROK
PWROK_R — R161 0_4 — PWROK L22 ← PWROK
(16) PCH_PWROK_EC — C483 0.1U/10V/X5R_4 — APWROK L10 ← APWROK
(4) PM_DRAM_PWRGD ← PM_DRAM_PWRGD B13 ← DRAMPWROK
(16) RSMRST# ← RSMRST# C21
(16) SUSWARN# ← SUSWARN# K16 ← SUSWARN#/SUSPWRDNACK/GPIO30
(16) EC_PWRBTN# ← PWRBTN# E20
(16) AC_PRESENT ← AC_PRESENT H20 ← ACPRESENT / GPIO31
PM_BATLOW# ← PM_BATLOW# E10 ← BATLOW# / GPIO72
PM_RI# ← RI# A10

+3V
+3V_S5
+3V_S5
+3V_S5
+3V_S5
DSW
DSW
+3V_S5
+3V_S5
+3V_S5

CLKRUN# / GPIO32 N3 → CLKRUN#
SUS_STAT# / GPIO61 G8 → T5
SUSCLK / GPIO62 N14 → T3
SLP_S5# / GPIO63 D10 → T4
SLP_S4# H4 → T7 → SLP_S4# (16)
SLP_S3# F4 → T6 → SLP_S3# (16)
SLP_A# G10 → T2
SLP_SUS# G16 → SLP_SUS# (16)
PMSYNCH AP14 → PM_SYNC (4)
SLP_LAN# / GPIO29 K14

DSW
DPWROK E22 ← DPWROK (16)
WAKE# B9 ← PCIE_WAKE# (21,22)

CPT_PPT_Rev_0p5

CPT/PPT (LVDS,DDI)

U17D

R46 2.2K_4 — INT_EDIDCLK
R41 2.2K_4 — INT_EDIDDAT — +3V

(16) INT_LVDS_BLON → L_BKLTEN J47
(17) INT_LVDS_VDDEN → L_VDD_EN M45
(17) INT_LVDS_BRIGHT → L_BKLTCTL P45
(17) INT_EDIDCLK → L_DDC_CLK T40
(17) INT_EDIDDAT → L_DDC_DATA K47
+3V — R53 2.2K_4 — R74 2.2K_4 → L_CTRL_CLK T45
L_CTRL_DATA P39
R73 2.37K/F_4 — LVDS_IBG — T1 → LVD_IBG AF37
LVD_VBG AF36
LVD_VREFH AE48
LVD_VREFL AE47

(17) INT_TXLCLKOUTN → LVDSA_CLK# AK39
(17) INT_TXLCLKOUTP → LVDSA_CLK AK40
(17) INT_TXLOUTN0 → LVDSA_DATA#0 AN48
(17) INT_TXLOUTN1 → LVDSA_DATA#1 AM47
(17) INT_TXLOUTN2 → LVDSA_DATA#2 AK47
LVDSA_DATA#3 AJ48
(17) INT_TXLOUTP0 → LVDSA_DATA0 AN47
(17) INT_TXLOUTP1 → LVDSA_DATA1 AM49
(17) INT_TXLOUTP2 → LVDSA_DATA2 AK49
LVDSA_DATA3 AJ47

LVDS

(17) INT_TXUCLKOUTN → LVDSB_CLK# AF40
(17) INT_TXUCLKOUTP → LVDSB_CLK AF39
(17) INT_TXUOUTN0 → LVDSB_DATA#0 AH45
(17) INT_TXUOUTN1 → LVDSB_DATA#1 AH47
(17) INT_TXUOUTN2 → LVDSB_DATA#2 AF49
LVDSB_DATA#3 AF45
(17) INT_TXUOUTP0 → LVDSB_DATA0 AH43
(17) INT_TXUOUTP1 → LVDSB_DATA1 AH49
(17) INT_TXUOUTP2 → LVDSB_DATA2 AF47
LVDSB_DATA3 AF43

Digital Display Interface

CRT_BLUE N48
CRT_GREEN P49
CRT_RED T49
CRT_DDC_CLK T39
CRT_DDC_DATA M40
CRT_HSYNC M47
CRT_VSYNC M49

CRT

DAC_IREF T43 — R60 1K/D_4
DAC_IREF T42
CRT_IRTN

CPT_PPT_Rev_0p5

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 → INT_HDMI_SCL (19)
SDVO_CTRLDATA M39 → INT_HDMI_SDA (19)
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 → INT_HDMI_HPD_Q (19)
DDPB_0N AV42 — INT_HDMI_TXDN2_C C419 — 0.1U/10V/X5R_4 → INT_HDMI_TXDN2 (19)
DDPB_0P AV40 — INT_HDMI_TXDP2_C C416 — 0.1U/10V/X5R_4 → INT_HDMI_TXDP2 (19)
DDPB_1N AV45 — INT_HDMI_TXDN1_C C415 — 0.1U/10V/X5R_4 → INT_HDMI_TXDN1 (19)
DDPB_1P AV46 — INT_HDMI_TXDP1_C C413 — 0.1U/10V/X5R_4 → INT_HDMI_TXDP1 (19)
DDPB_2N AU48 — INT_HDMI_TXDN0_C C404 — 0.1U/10V/X5R_4 → INT_HDMI_TXDN0 (19)
DDPB_2P AU47 — INT_HDMI_TXDP0_C C403 — 0.1U/10V/X5R_4 → INT_HDMI_TXDP0 (19)
DDPB_3N AV47 — INT_HDMI_TXCN_C C406 — 0.1U/10V/X5R_4 → INT_HDMI_TXCN (19)
DDPB_3P AV49 — INT_HDMI_TXCP_C C405 — 0.1U/10V/X5R_4 → INT_HDMI_TXCP (19)

TMDS

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

INT. DP

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BE44
DDPD_1P BE44
DDPD_2N BE42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

CPT_PPT_Rev_0p5

PCH Pull-high/low(CLG)

+3V
CLKRUN# — R148 8.2K/J_4
XDP_DBRST# — R278 1K/J_4
PWROK_R — R169 47K_4

+3V_S5
PM_RI# — R267 10K/J_4
SUSWARN# — R108 10K/J_4
PM_BATLOW# — R135 8.2K/J_4

AC_PRESENT — R105 *10K/J_4 — +3V_S5_DSW
PM_DRAM_PWRGD — R265 200/F_4 — +3V_SUS
PCIE_WAKE# — R269 10K/J_4 — +3V_S5

+3V_RTC
R254 330K/J_4
DSWVREN

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

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2.Recycled Resin and Coated Wire should be procured from Green Partners.

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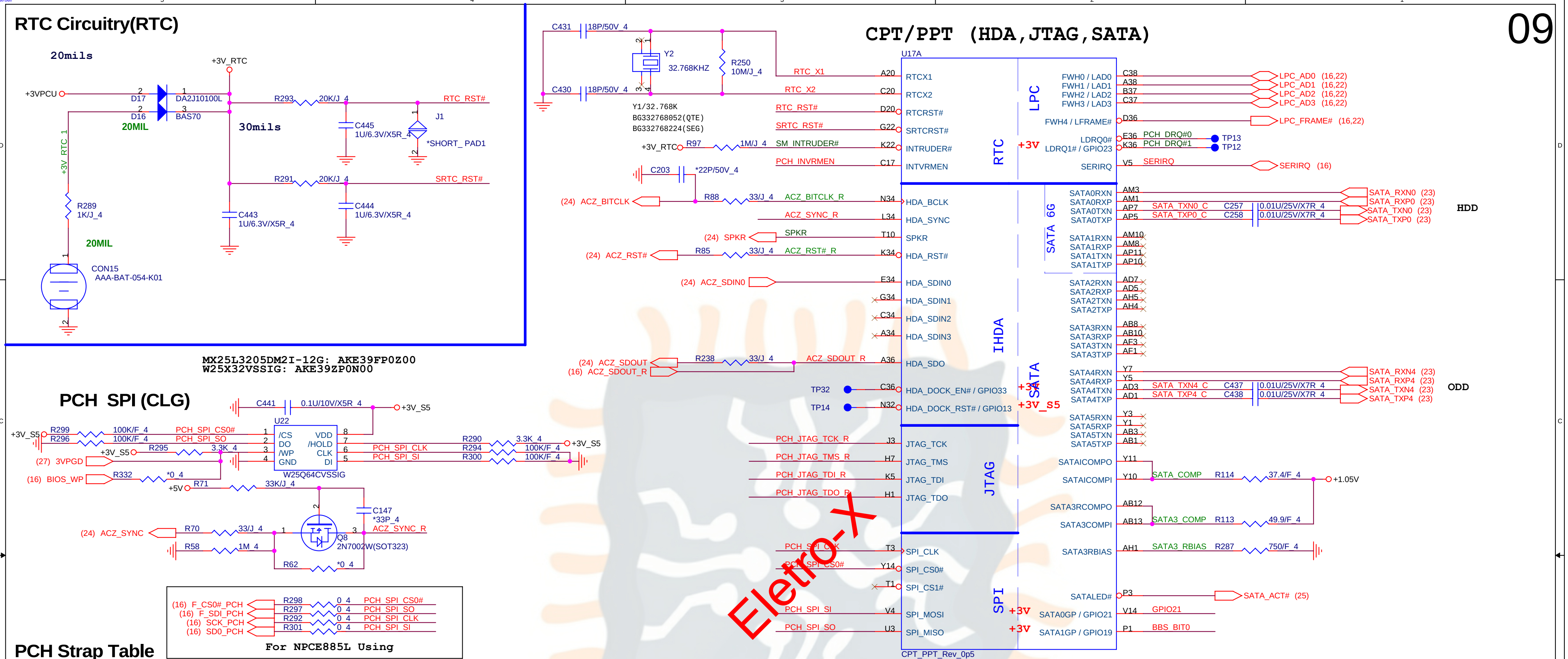
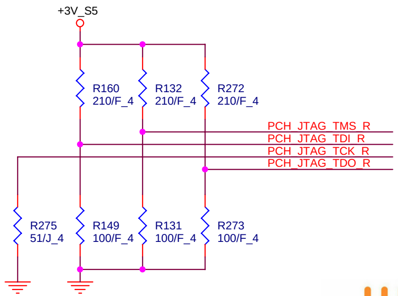
CPT/PPT (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	**0 = Default (weak pull-down 20K)** 1 = Setting to No-Reboot mode	SPKR
PCI_GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode **1 = Default (weak pull-up 20K)**	TP7 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+3V_RTC R255 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI * 0 / 0 / LPC	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		TP30 BBS_BIT1 (10) TP33 BBS_BIT0
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss for Ivy Bridge 1 = Set to Vcc for Sandy Bridge (weak pull-down 20K)	R282 2.2K_4 +1.8V R276 1K/J_4 NV_CLE (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	TP19 PLL_ODVR_EN (11)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R65 1K/J_4 ACZ_SYNC_R

PCH JTAG Debug (CLG)



HR/CR: PROCSEL#

SERIRQ R24 8.2K/J_4 +3V
GPIO21 R142 10K/J_4

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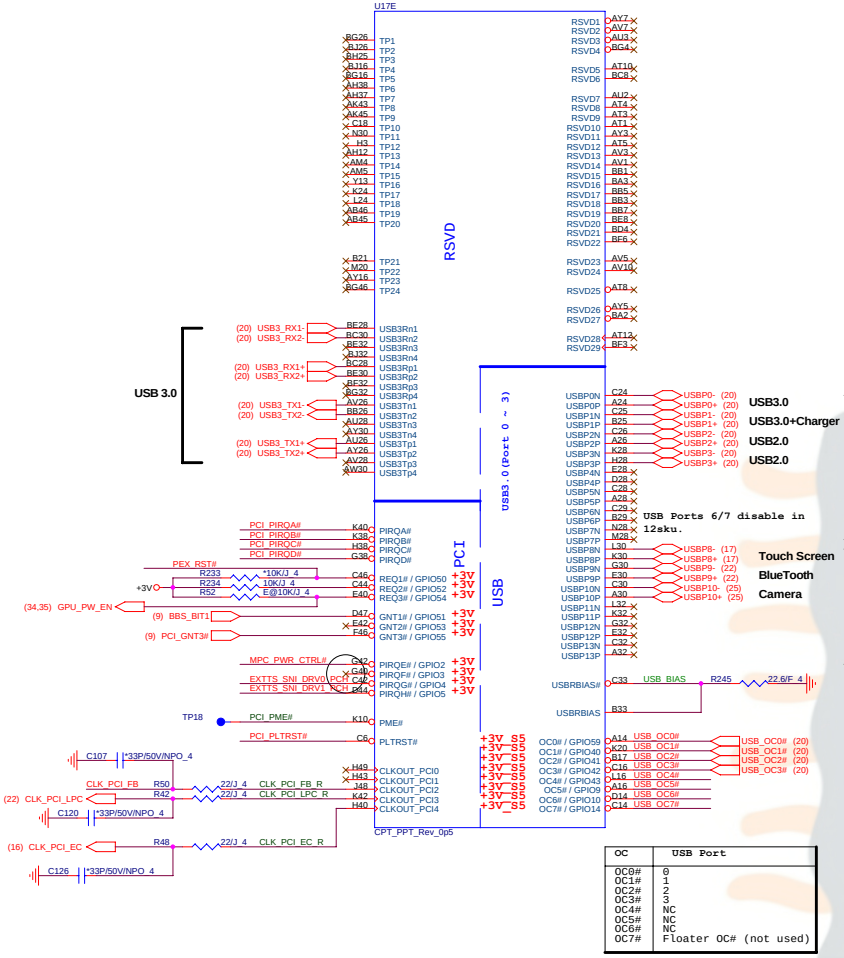
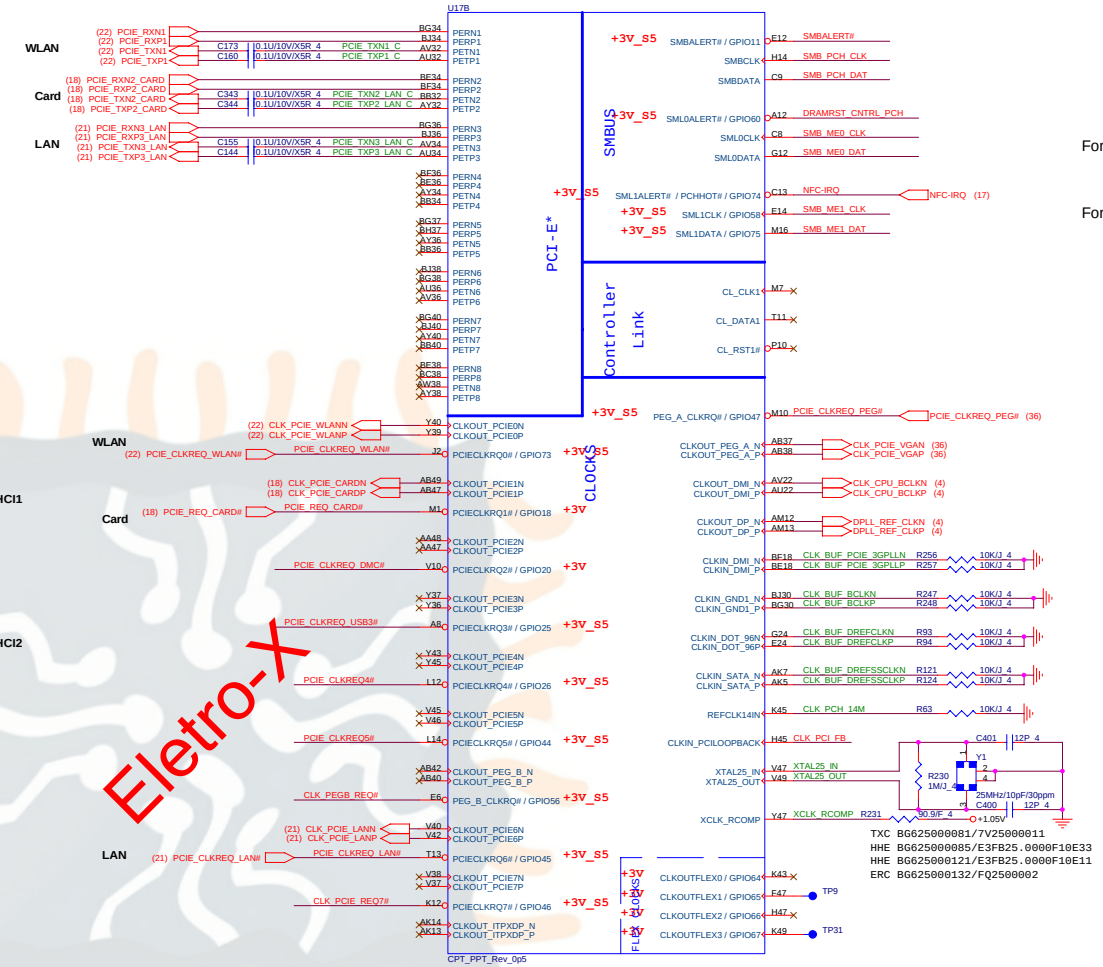
CPT/PPT (PCI,USB,NVRAM)



OC	USB Port
OC0#	0
OC1#	1
OC2#	2
OC3#	3
OC4#	NC
OC5#	NC
OC6#	NC
OC7#	Floater OC# (not used)

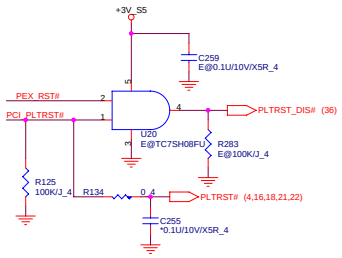
CPT/PPT (PCI-E,SMBUS,CLK)



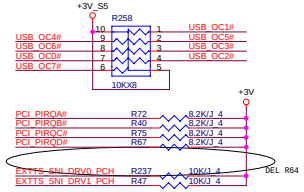
TXC BG625000081/7V25000011
HHE BG625000085/E3FB25.0000F10E33
HHE BG625000121/E3FB25.0000F10E11
ERC BG625000132/FQ2500002

Eletro-X

PLTRST#(CLG)



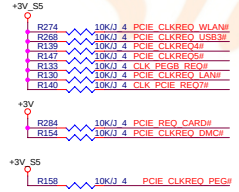
PCI/USBOC# Pull-up(CLG)



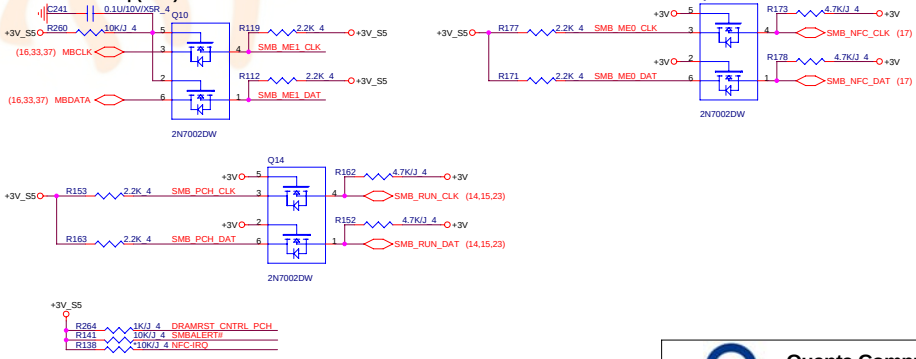
MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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PROJECT :Chief River

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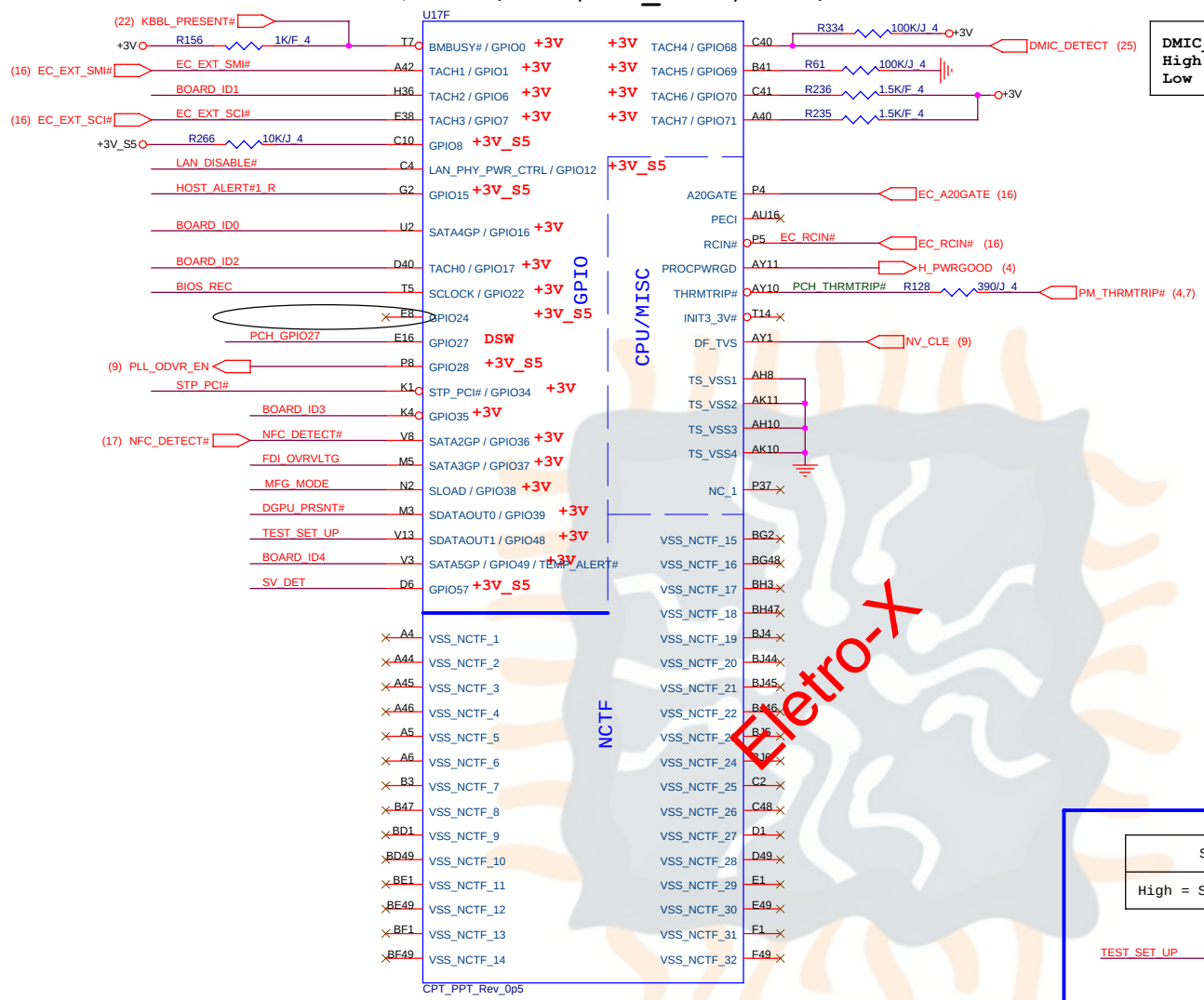
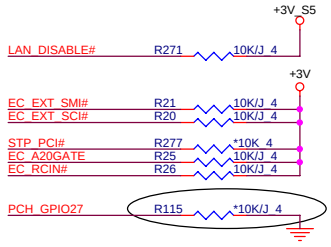
CPT/PPT (GPIO,VSS_NCTF,RSVD)



DMIC_DETECT:
High : Single DMIC
Low : Dual DMIC

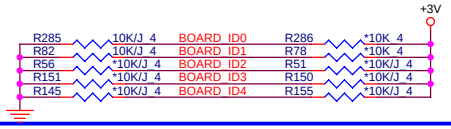
GPIO Pull-up/Pull-down(CLG)

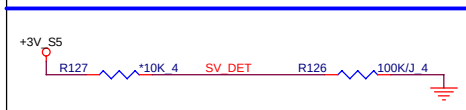


Change to no mount

	0	1
Board ID0	CaspiCRA1-CaspiCRB1 HK8-HK9	SuperiorCRA1-SuperiorCRB1 GD5-GD6
Board ID1	HK8/GD5 14"	HK9/GD6 15"

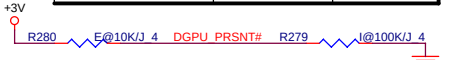
SV_SET_UP
High = Strong (Default)



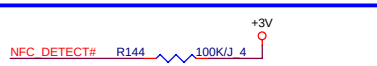


Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



NFC Detect	High : No NFC Module Plug Low : NFC Module Plug

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

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Quanta Computer Inc.
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PCH5 (CLG) CPT/PPT (POWER)

CPT/PPT (POWER)

VccCORE =1.3 A(60mils)

(VccIO =2.925A (140mils))

VCCVRM: 1.8V (Destop)
1.5V (Mobile)

VCCSPI = 20mA(8mils)

VCCPNAND = 190 mA(15mils)

VCCDMI = 42mA(10mils)

VCCCLKDMI = 20mA(8mils)

1mA(8mils)

60mA(10mils)

Change footprint 0805 to 0603

VccASW =1.01 A(60mils)

VCCDSW3_3= 3mA

VCCSUS3_3 = 119mA(15mils)

VCC5REFSUS=1mA

V5REF= 1mA

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCME = 1.01A(60mils)

VCCSUSHDA= 10mA(8mils)

65mA(10mils)

8mA(8mils)

VCCDIFFCLKN= 55mA(10mils)

VCCSSC= 95mA(10mils)

VCCRTC<1mA(8mils)

DEEP STANDBY

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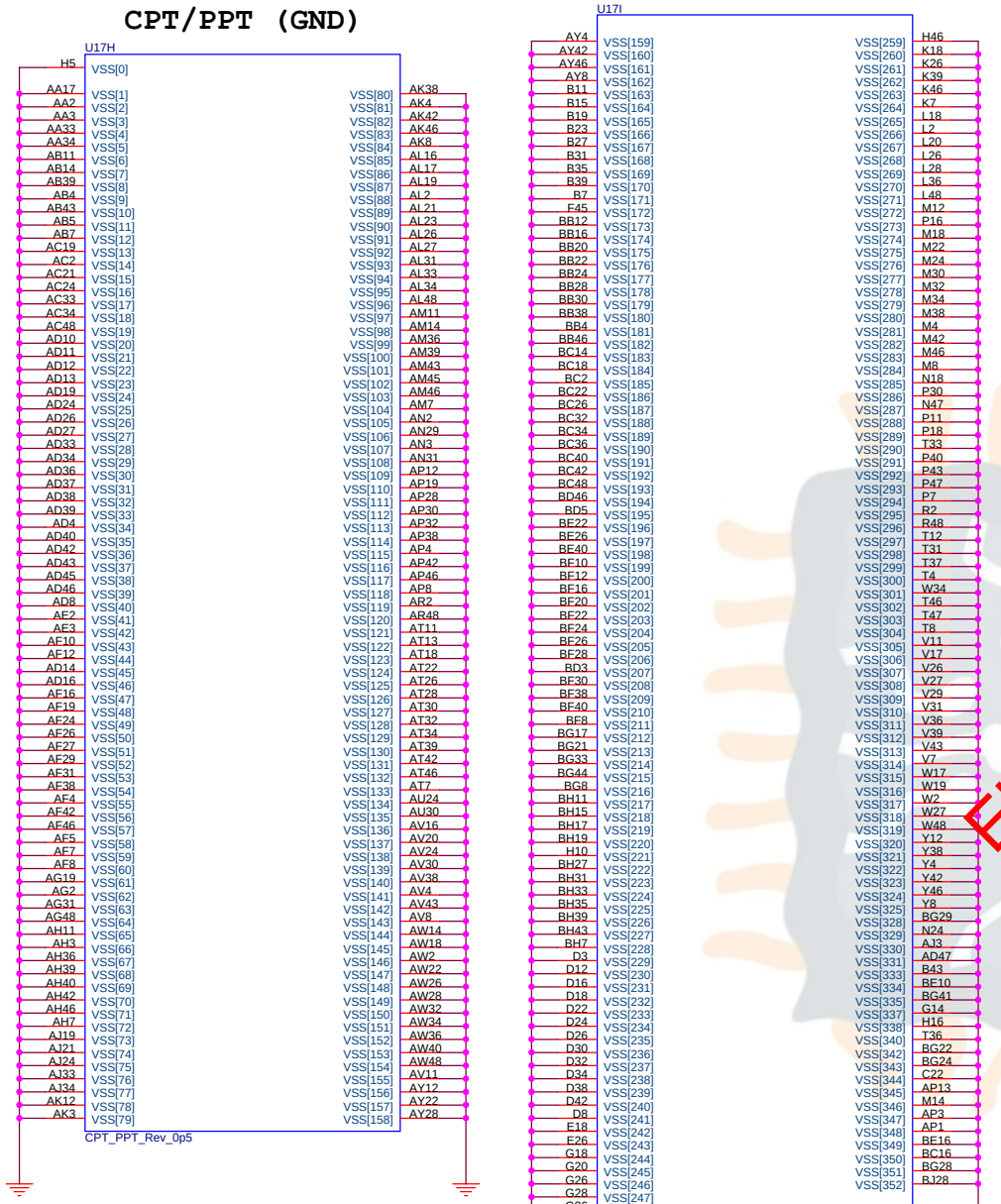
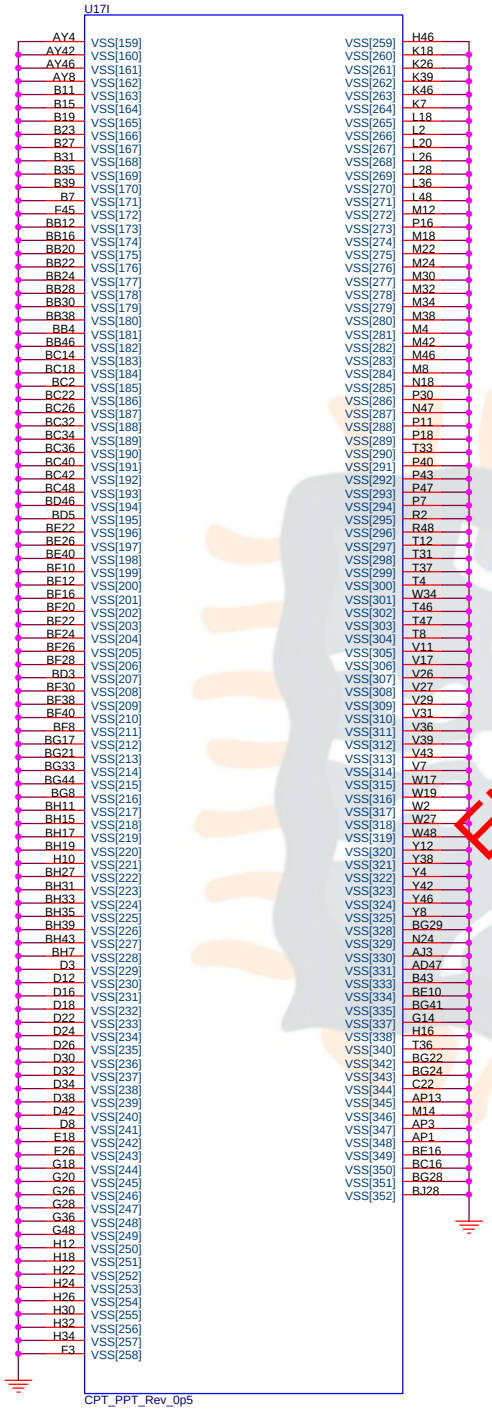
CPT/PPT (GND)





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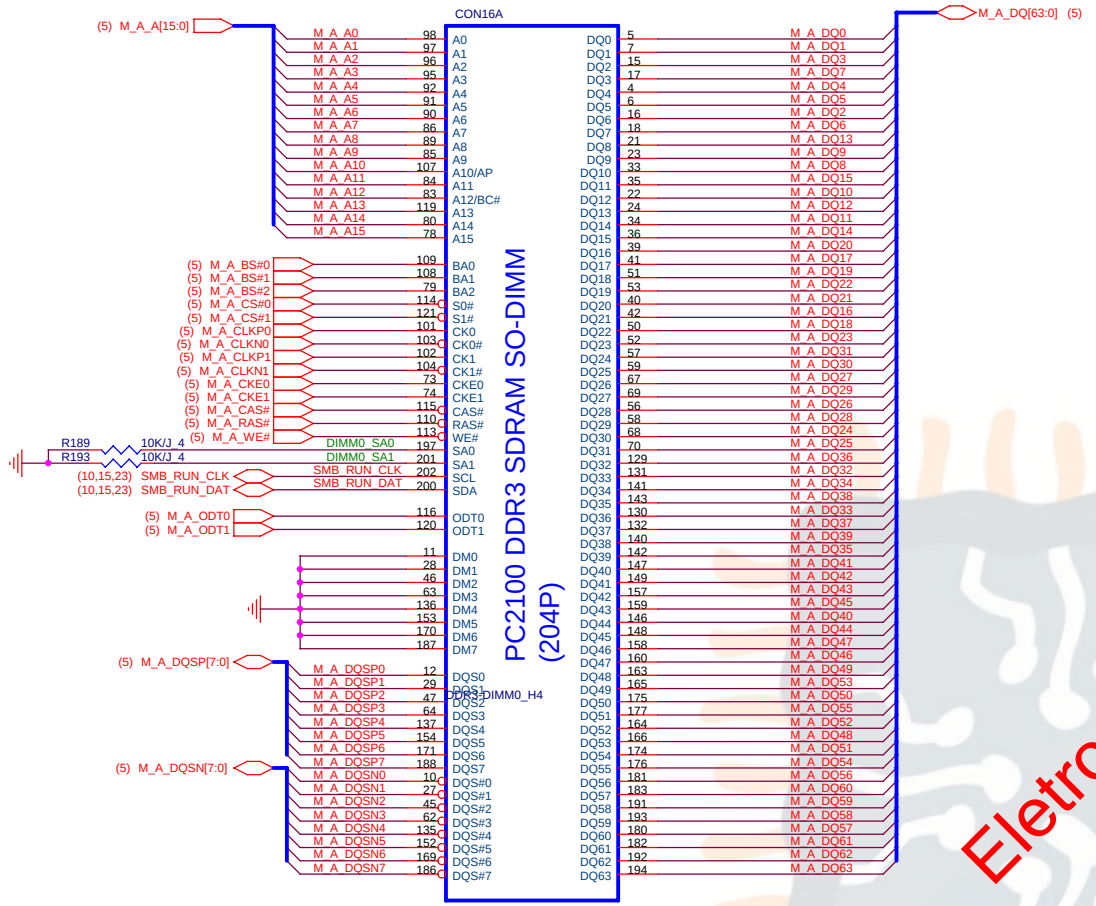
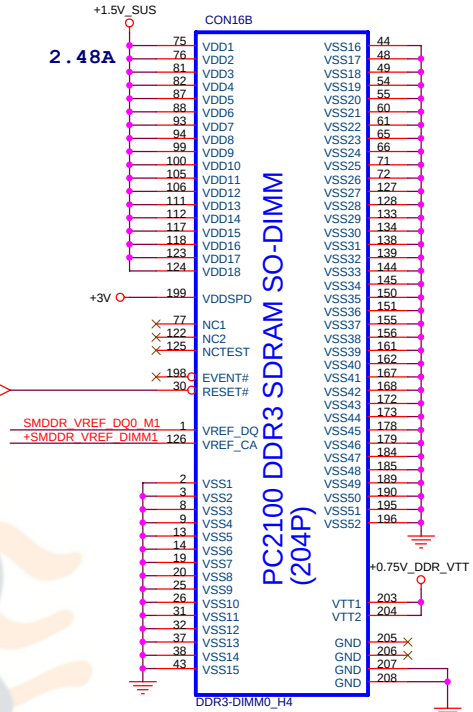
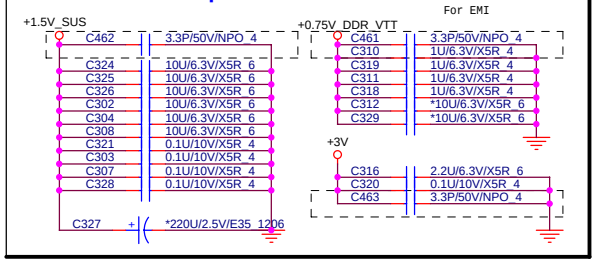


RUV Type

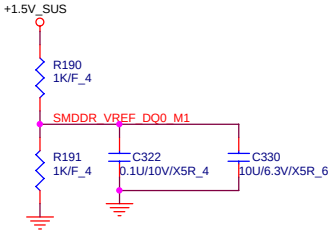


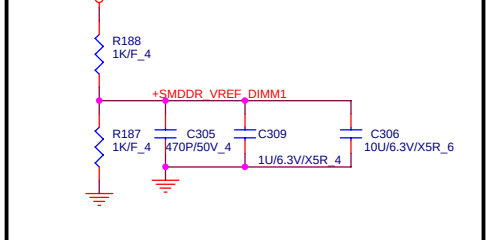
RUV Type

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution





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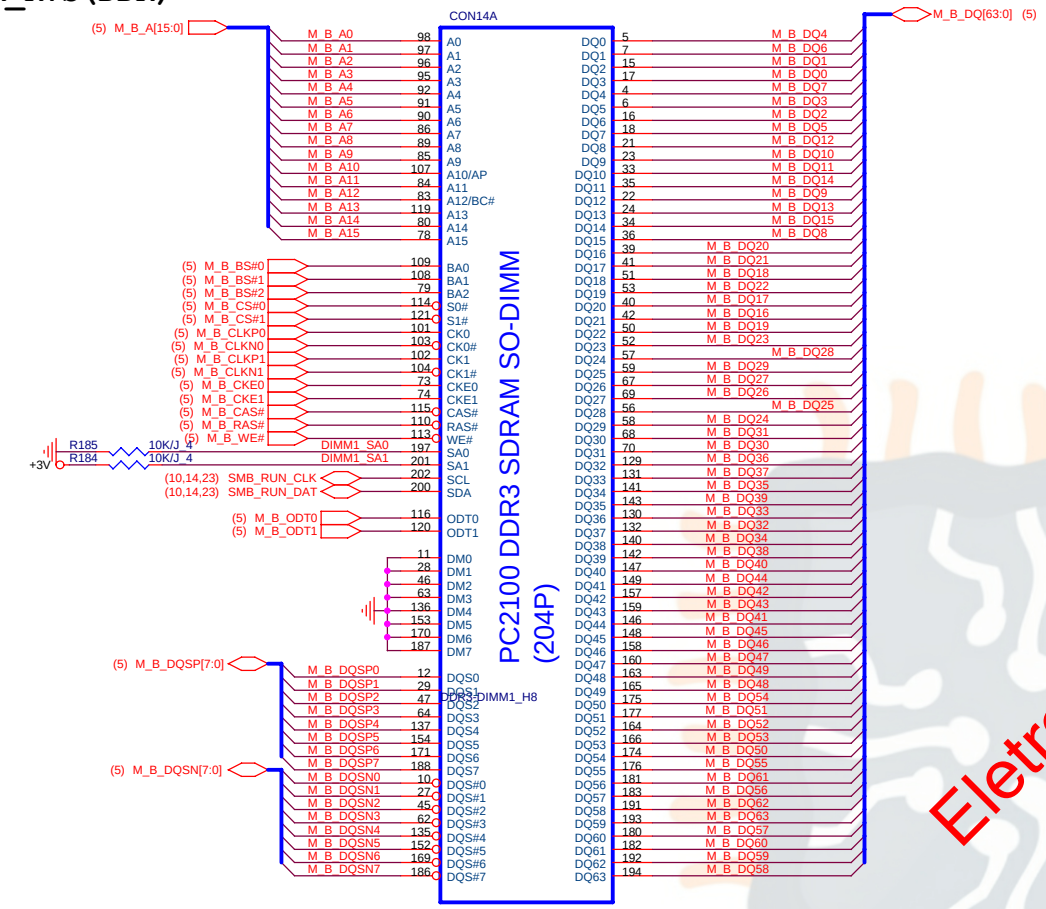
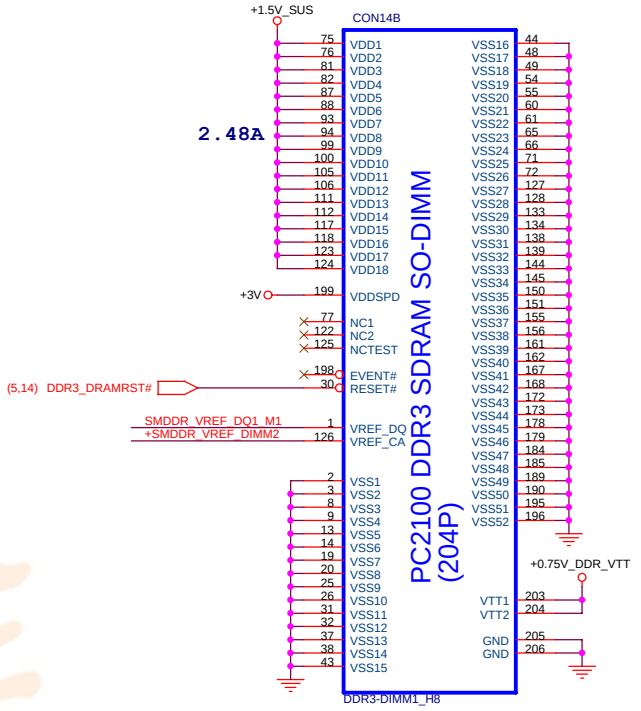
ECEtRO-X

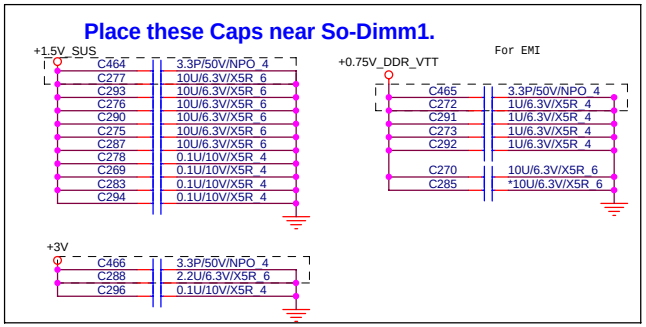
DDR_RVS (DDR)

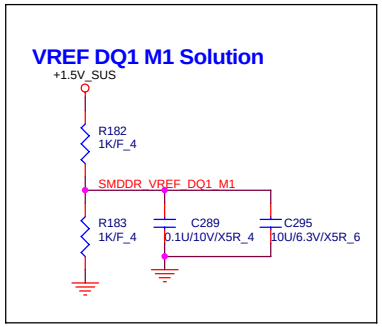


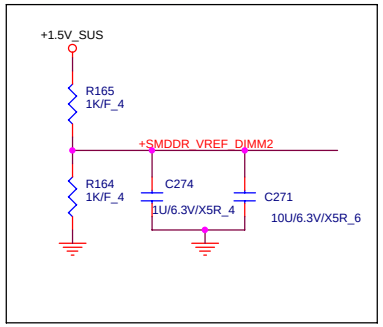
RUV Type



RUV Type







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** Straping Pin,Can not pull low.
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

Magnetic Lid Switch

KU3 — IN / OUT / GND — LID# — E-CMOS

E-CMOS :AL002618001/EC2618NLB1GR
PROLIFIC : AL003661003/PT3661-BB
BCD : AL009249000/AH9249NTR-G1

DRAM_VOLTAGE_SET

Low: 1.5V
High : 1.35V

MODEL ID

High	HK8/HK9(KR29 mount KR30 no mount)
Low	GD5/GD6(KR29 no mount KR30 mount)

VCC POWER ON RESET

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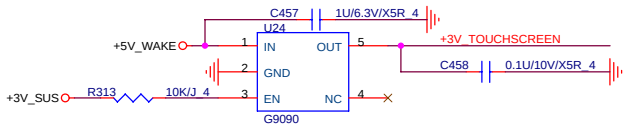
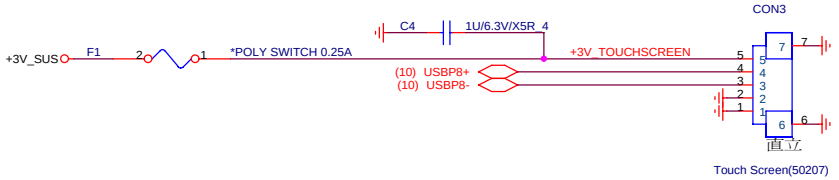
Touch Screen

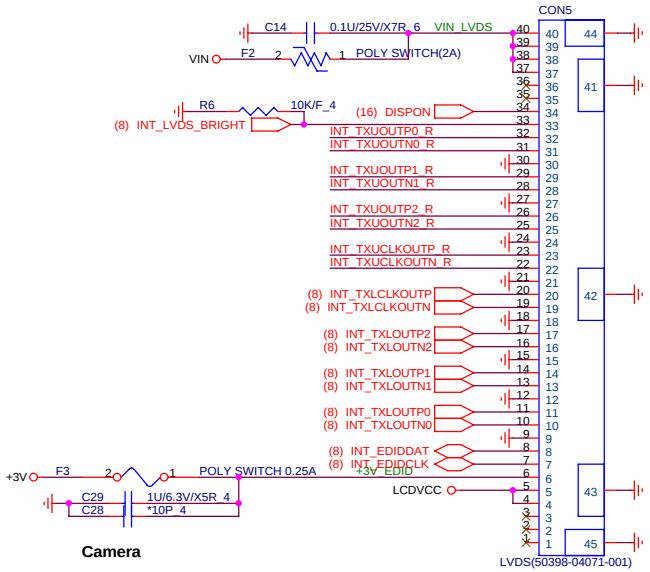


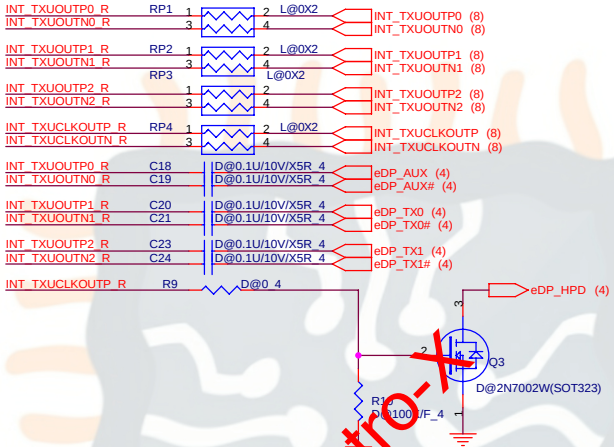


NFC module :
Vender : Samsung SNC-i20
Power consumption : Max. 160mW/48mA
Power Ripple +/- 50mV

LVDS

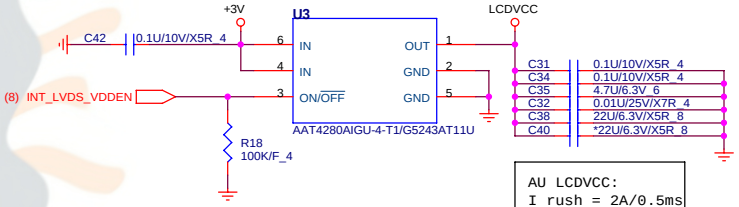
FAST,UL/CSA





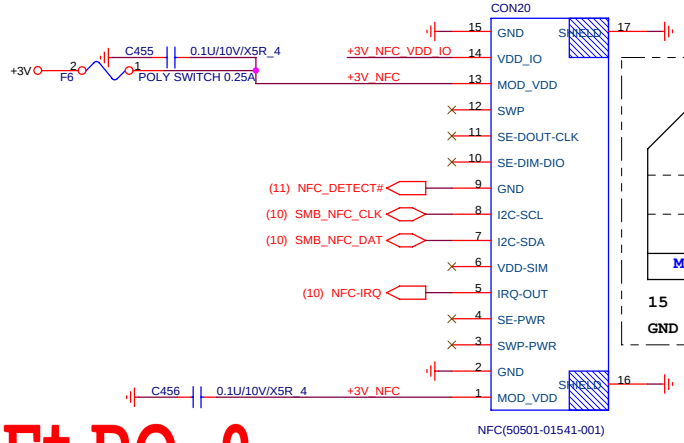
Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

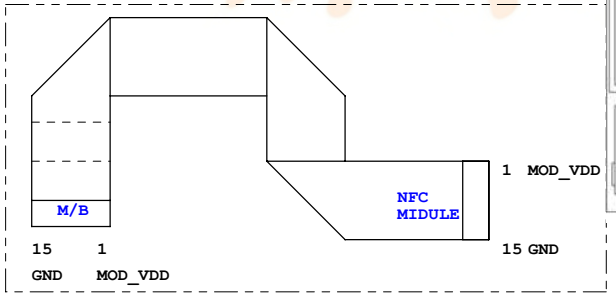
NB LVDS enable

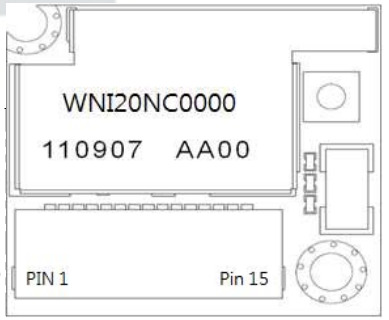


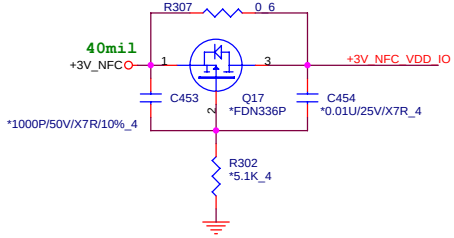
AU LCDVCC:
I rush = 2A/0.5ms
IDD = 0.3A

NFC









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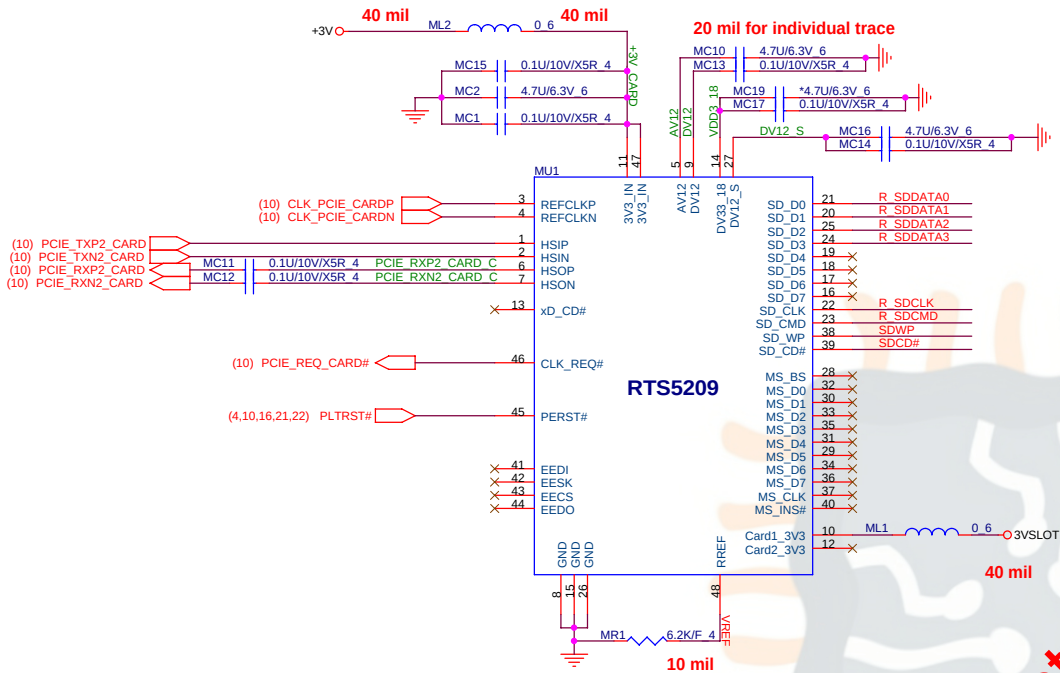
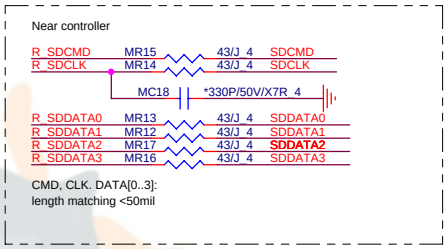
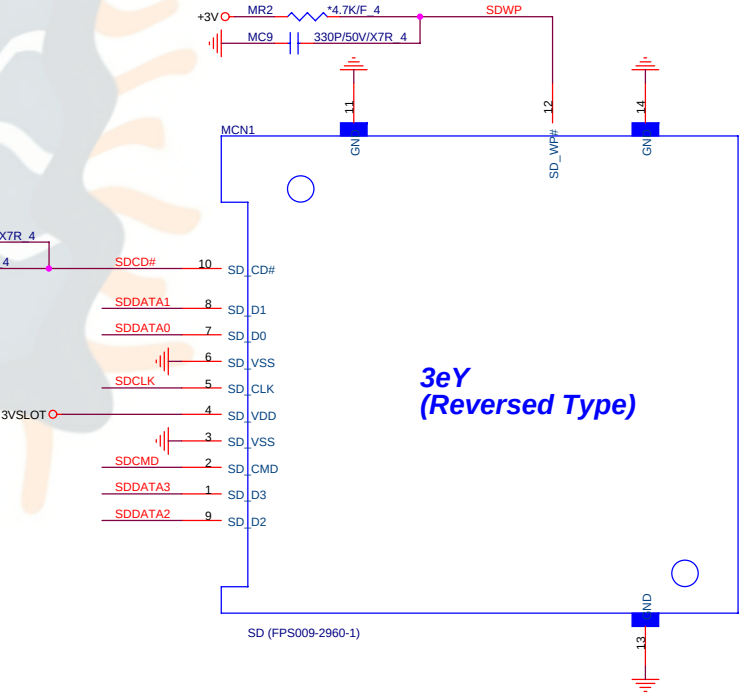
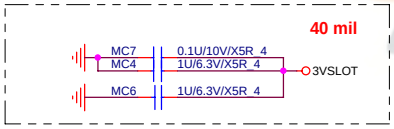






These component need to close to Slot



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :ChiefRiver

Size	Document Number	Rev
	CARD	1A
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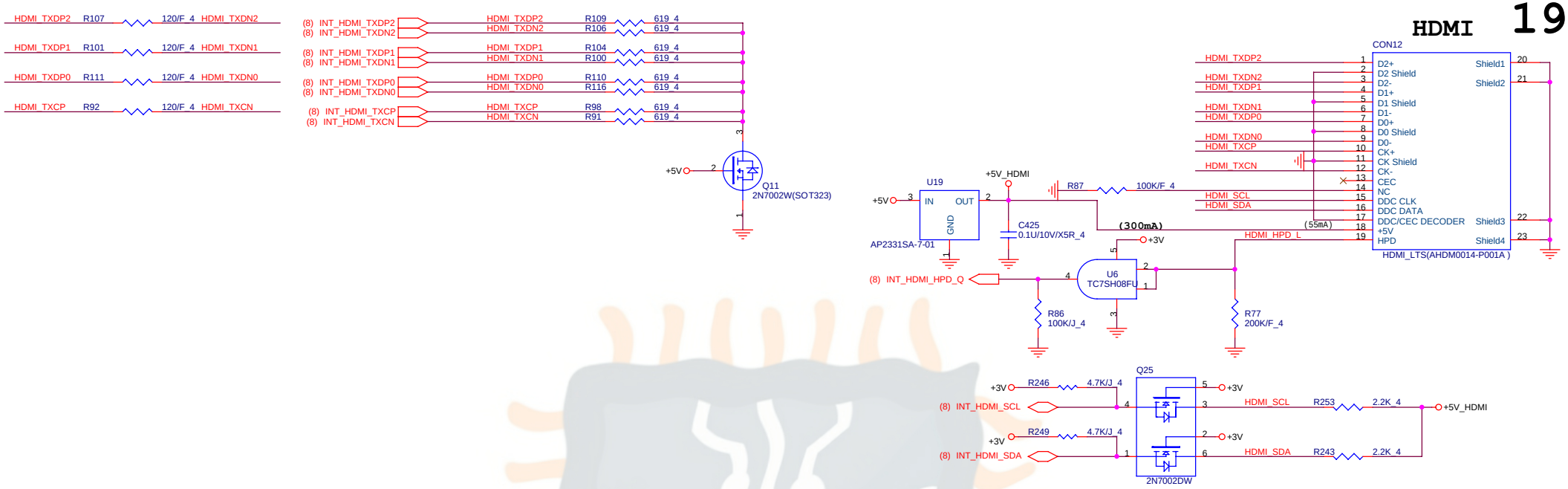
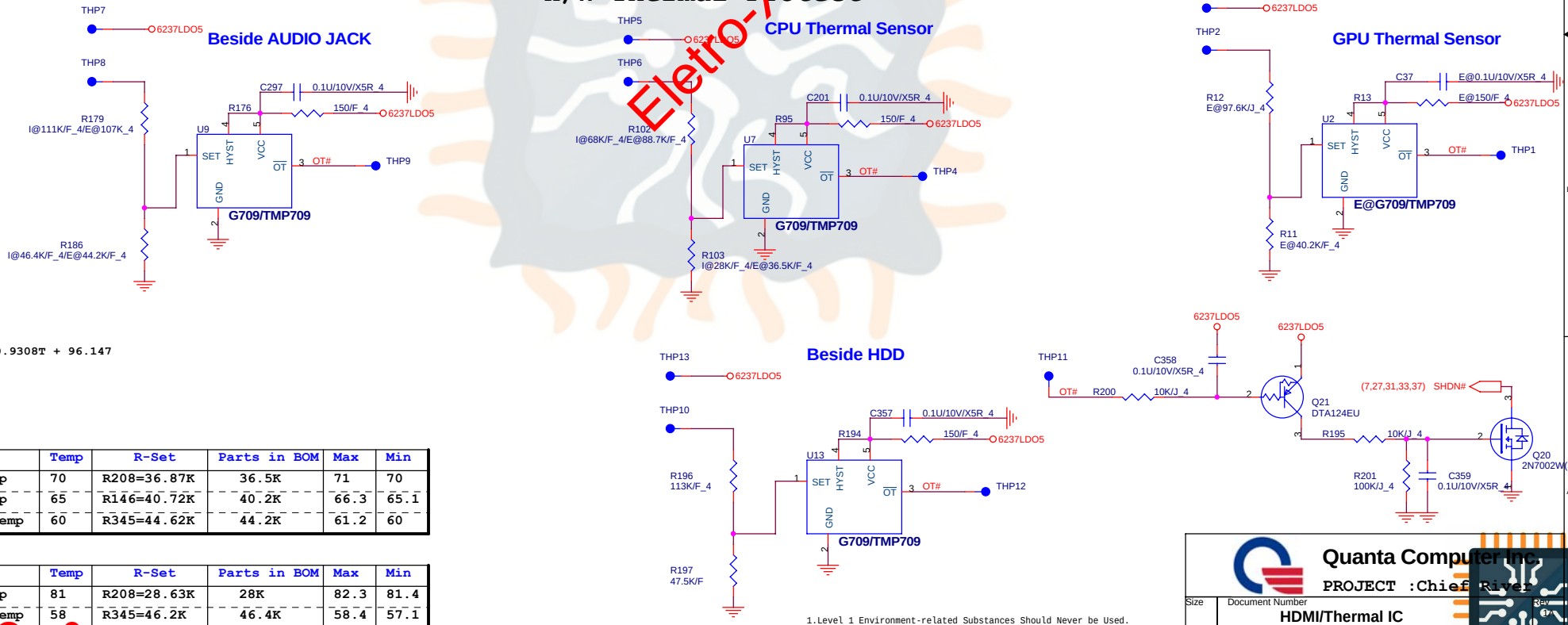
HDMI



H/W Thermal Protect



RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

95	18.5K
100	15K
107	10.3K
110	8.2K

DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	70	R208=36.87K	36.5K	71	70
Near GFX sensor temp	65	R146=40.72K	40.2K	66.3	65.1
Near AUDIO sensor temp	60	R345=44.62K	44.2K	61.2	60

UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	81	R208=28.63K	28K	82.3	81.4
Near AUDIO sensor temp	58	R345=46.2K	46.4K	58.4	57.1

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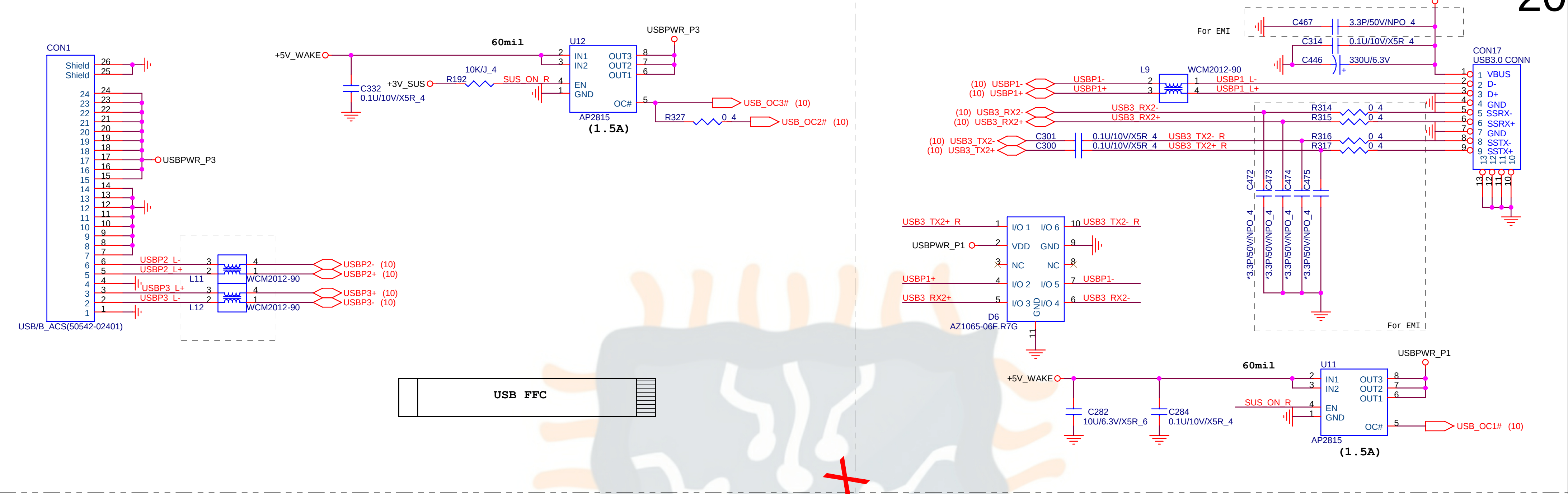
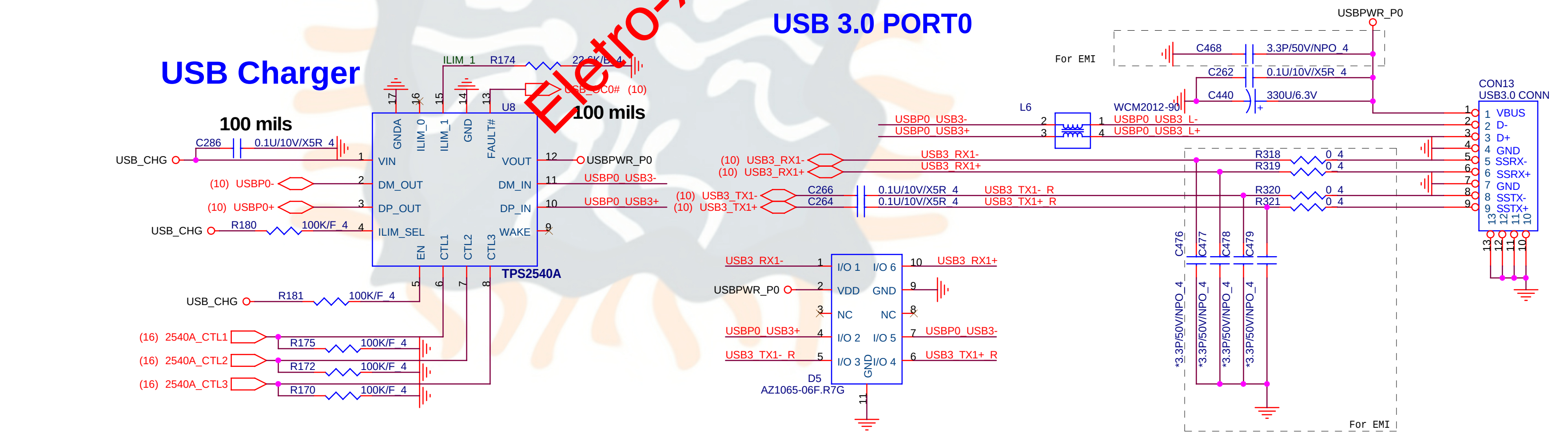
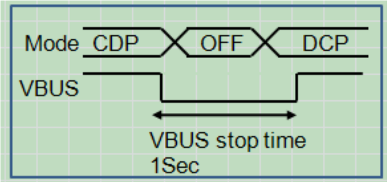
Quanta Computer Inc.
PROJECT :Chief River
Size | Document Number | Rev
HDMI/Thermal IC
Date: Thursday, January 17, 2013 | Sheet 19 of 47

MB to USB board





SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



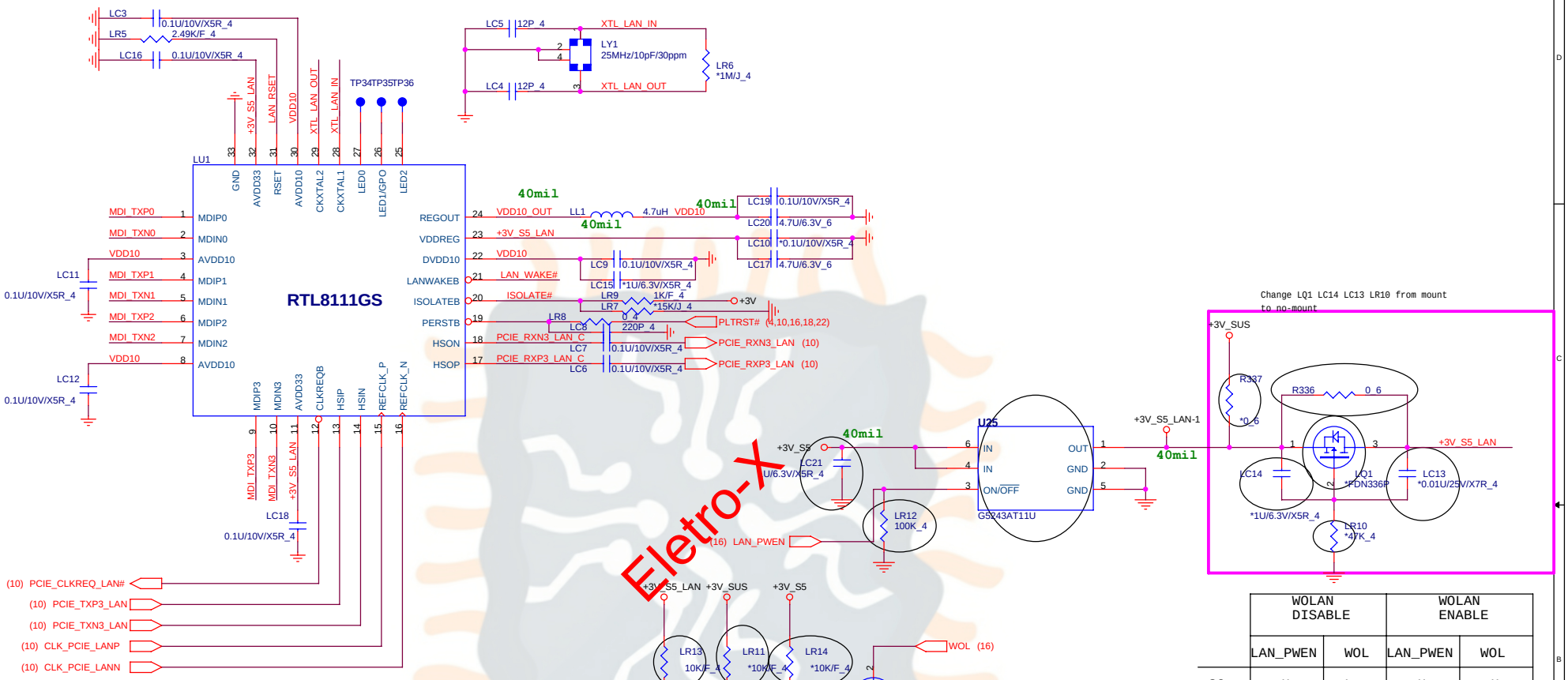
CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting			
	Disable	C(1 2 3)	Enable	C(1 2 3)
S0	SDP	(X 1 0)	CDP	(1 1 1)
S3	SDP	(X 1 0)	DCP BC	(1 0 0)
DS3	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S4	Charger OFF	(0 0 0)	DCP BC	(1 0 0)
S5	Charger OFF	(0 0 0)	DCP BC	(1 0 0)

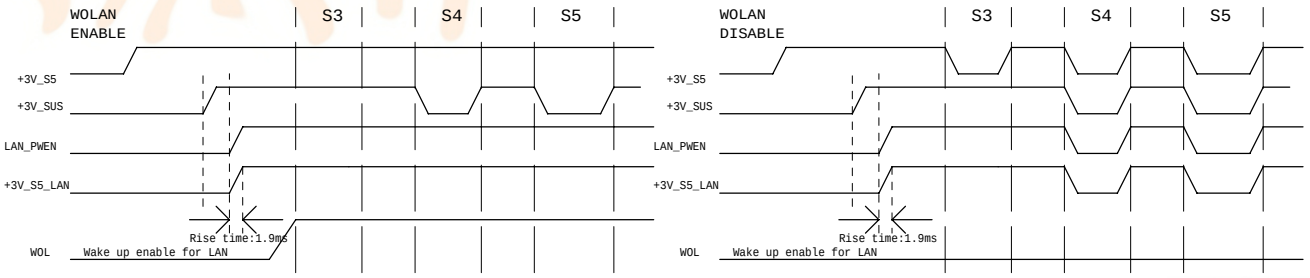
ILIM_SEL	(I LIMIT(A)= 48000/R)	
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Chief River
Size | Document Number: USB/USB Charger | Rev 1A
Date: Thursday, January 17, 2013 | Sheet 20 of 41



	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	L	H	H
S4	L	L	H	H
S5	L	L	H	H



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Quanta Computer Inc.
PROJECT : Chief River
Size | Document Number | Rev
Giga LAN RTL8111GS | 1A
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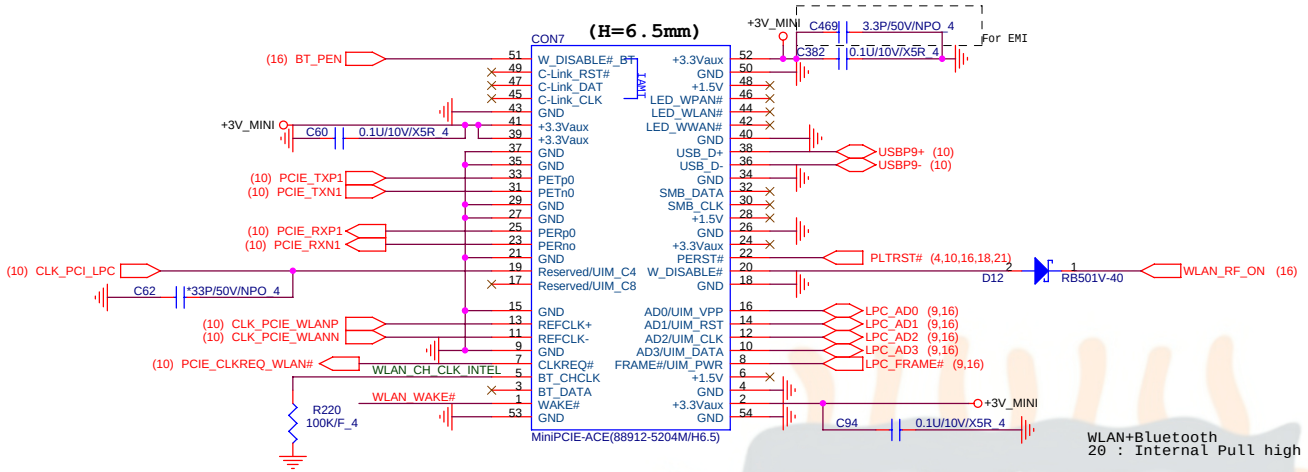
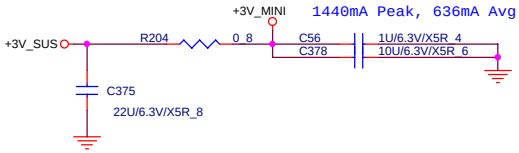
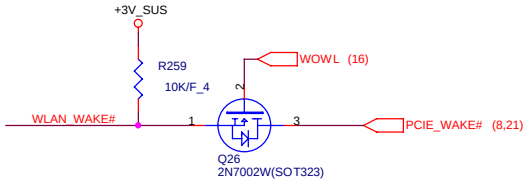
WLAN/WIMAX/WIDI



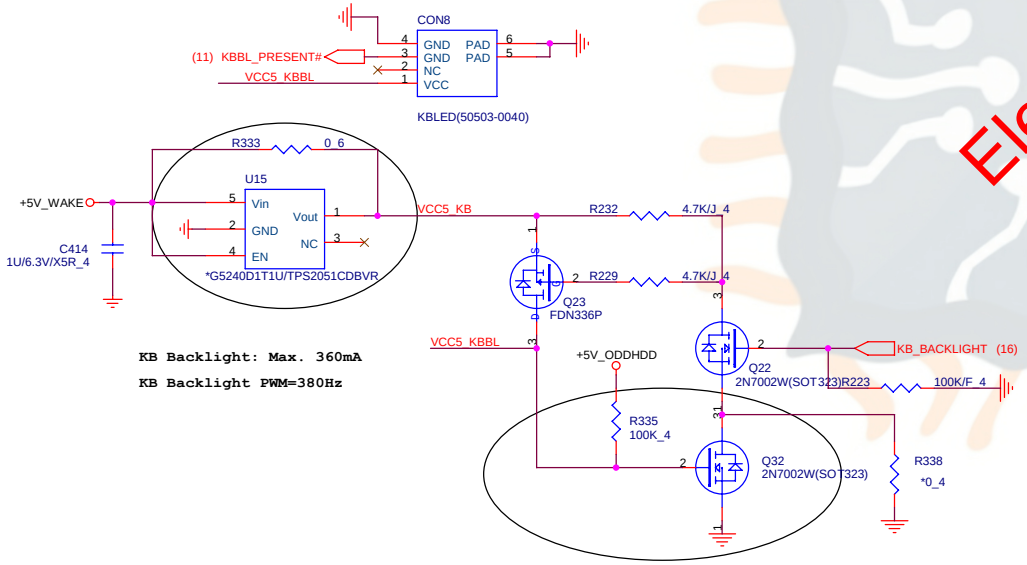
WLAN+Bluetooth
20 : Internal Pull high 25K ~ 58K





AC Mode : Support Wake on WLAN
DC Mode : Don't support wake on WLAN

KB BACKLIGHT



KB Backlight: Max. 360mA
KB Backlight PWM=380Hz

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :ChiefRiver

Size	Document Number	Rev
	WLAN/KB BL	1A
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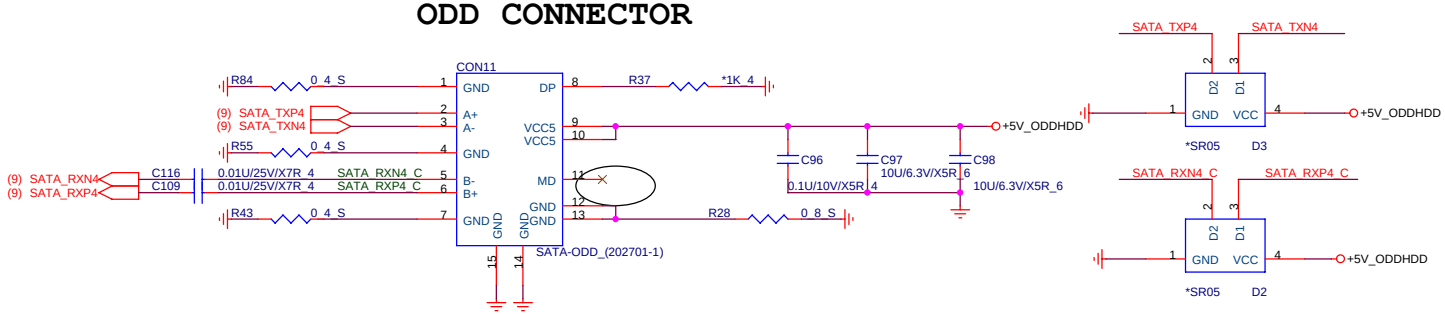
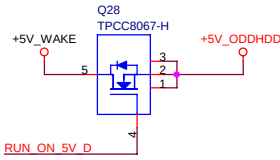
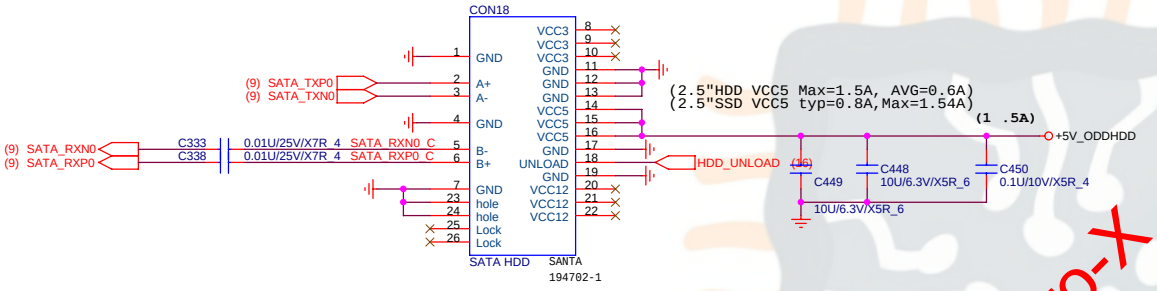
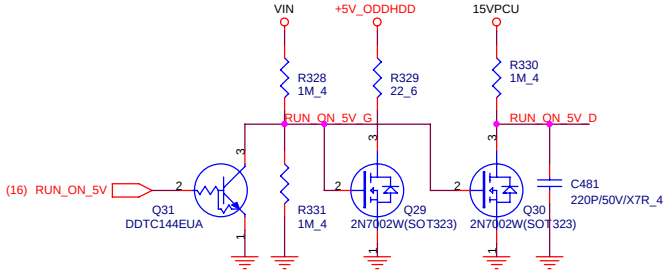
ODD CONNECTOR

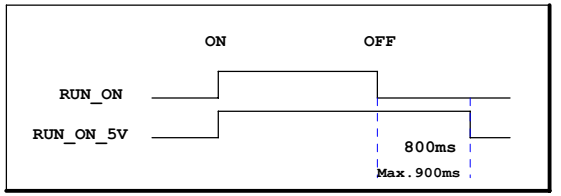




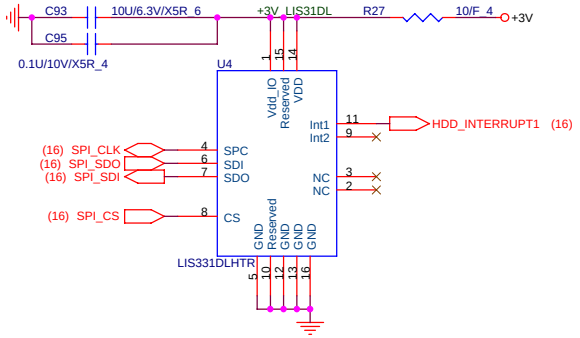
HDD CONNECTOR

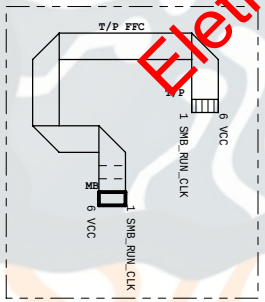




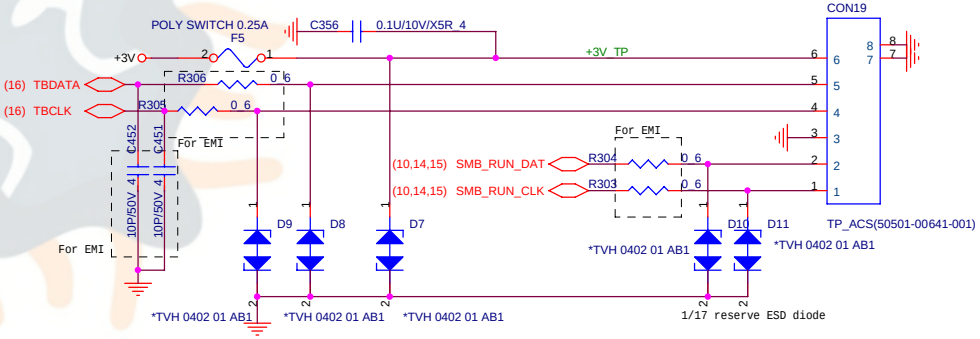


HDD PROTECT SPI INTERFACE

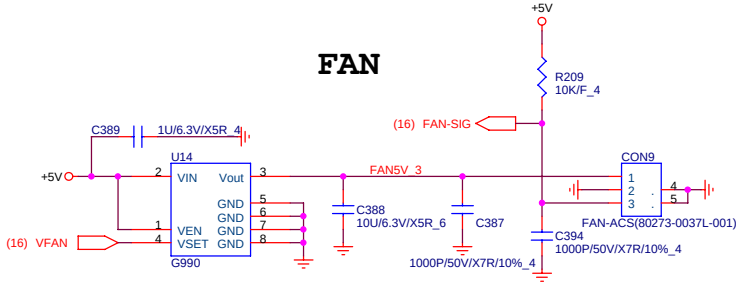




T/P Board to T/P



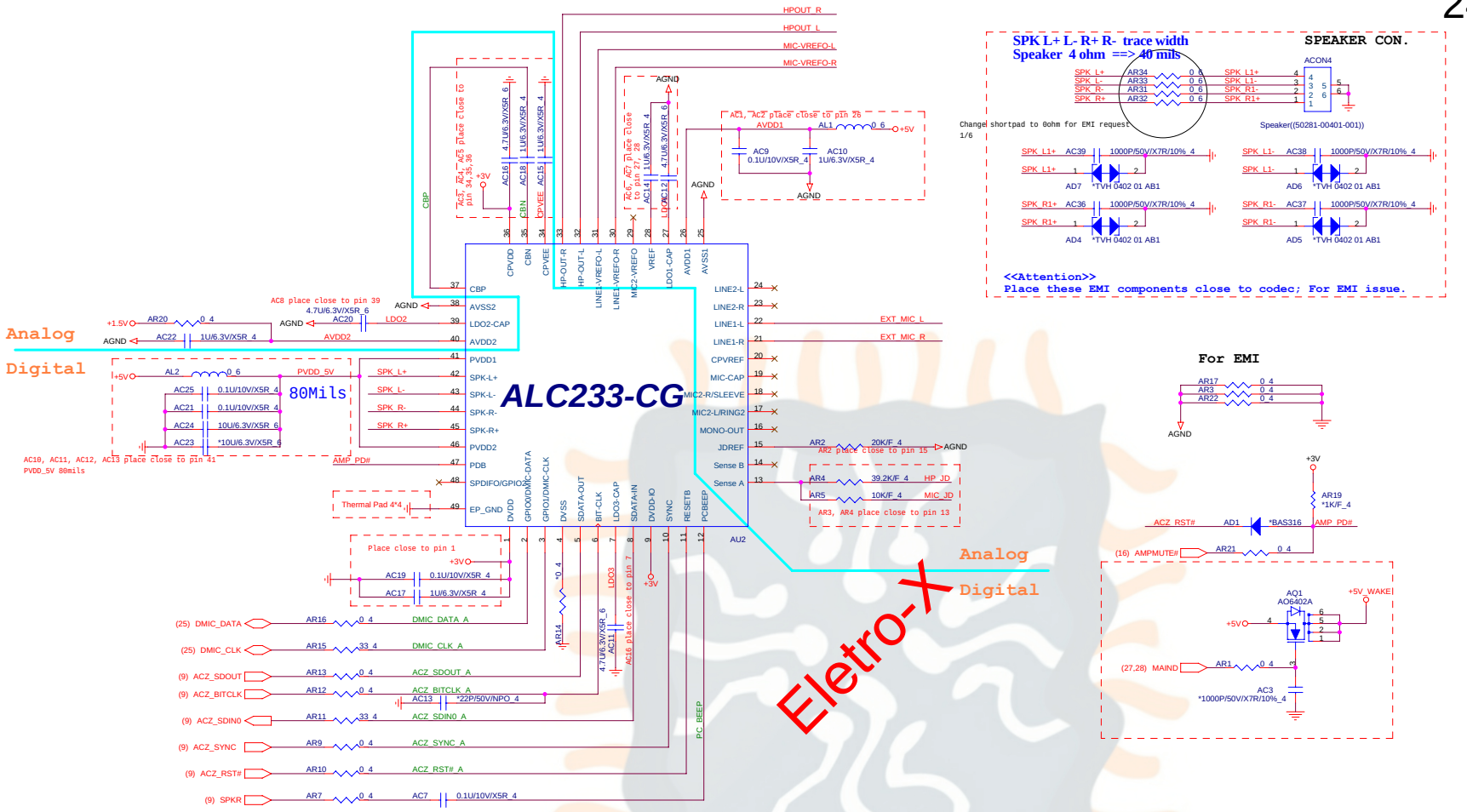
FAN

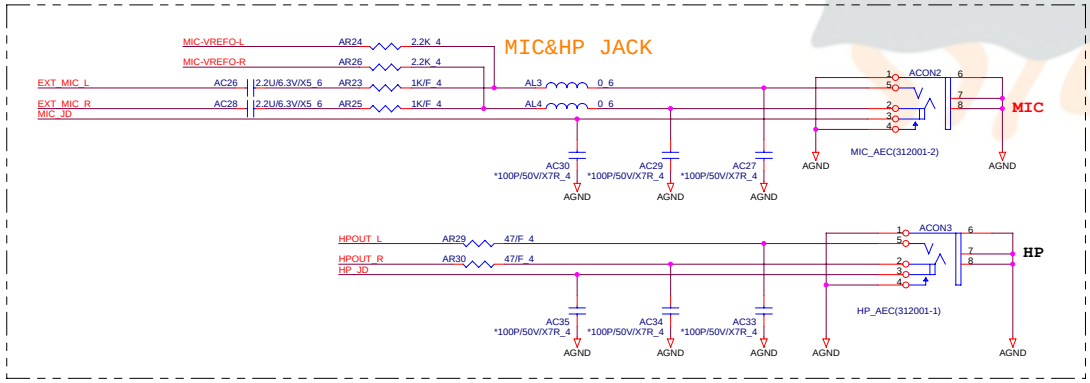


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	HDD/ODD/TP/FAN	1A
Date: Thursday, January 17, 2013	Sheet 23 of 47	





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Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	Audio Codec ALC233-CG	1A
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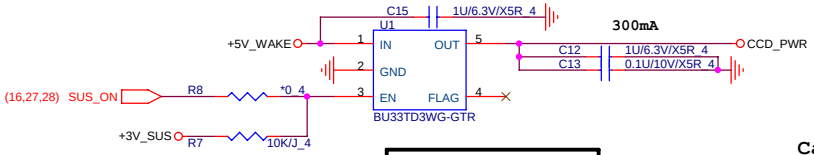
ECEtRO-X

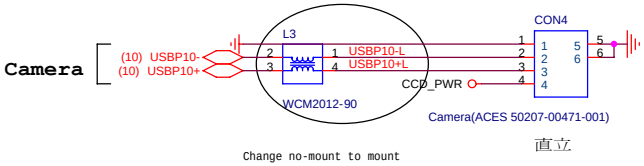
Camera

USB Camera Power



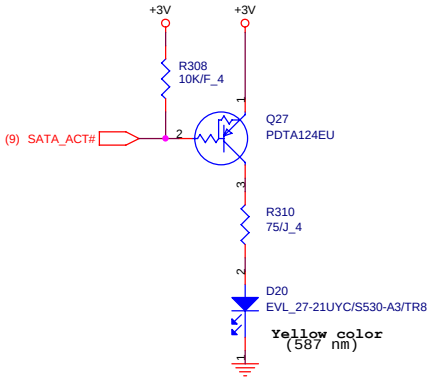
Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA

Camera

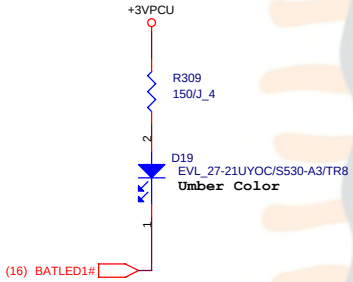


Change no-mount to mount

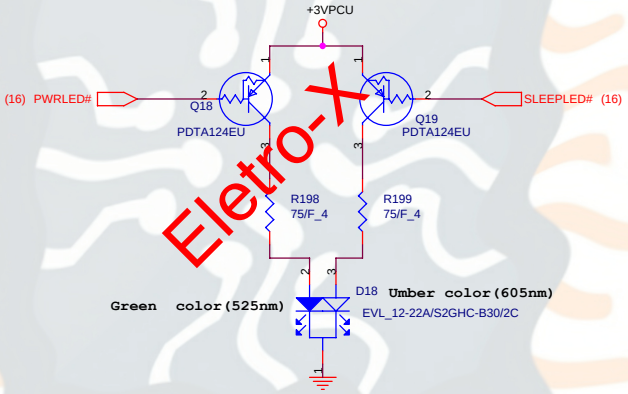
SATA LED



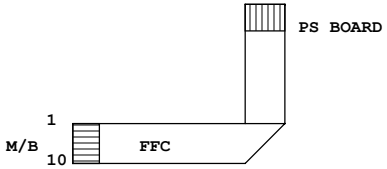
BATTERY LED



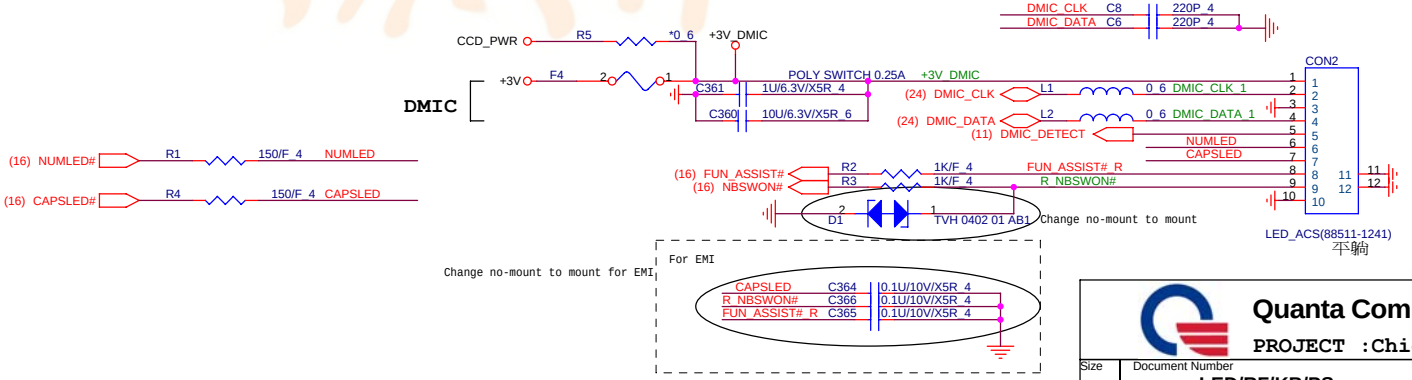
Power/Sleep LED



PS BOARD



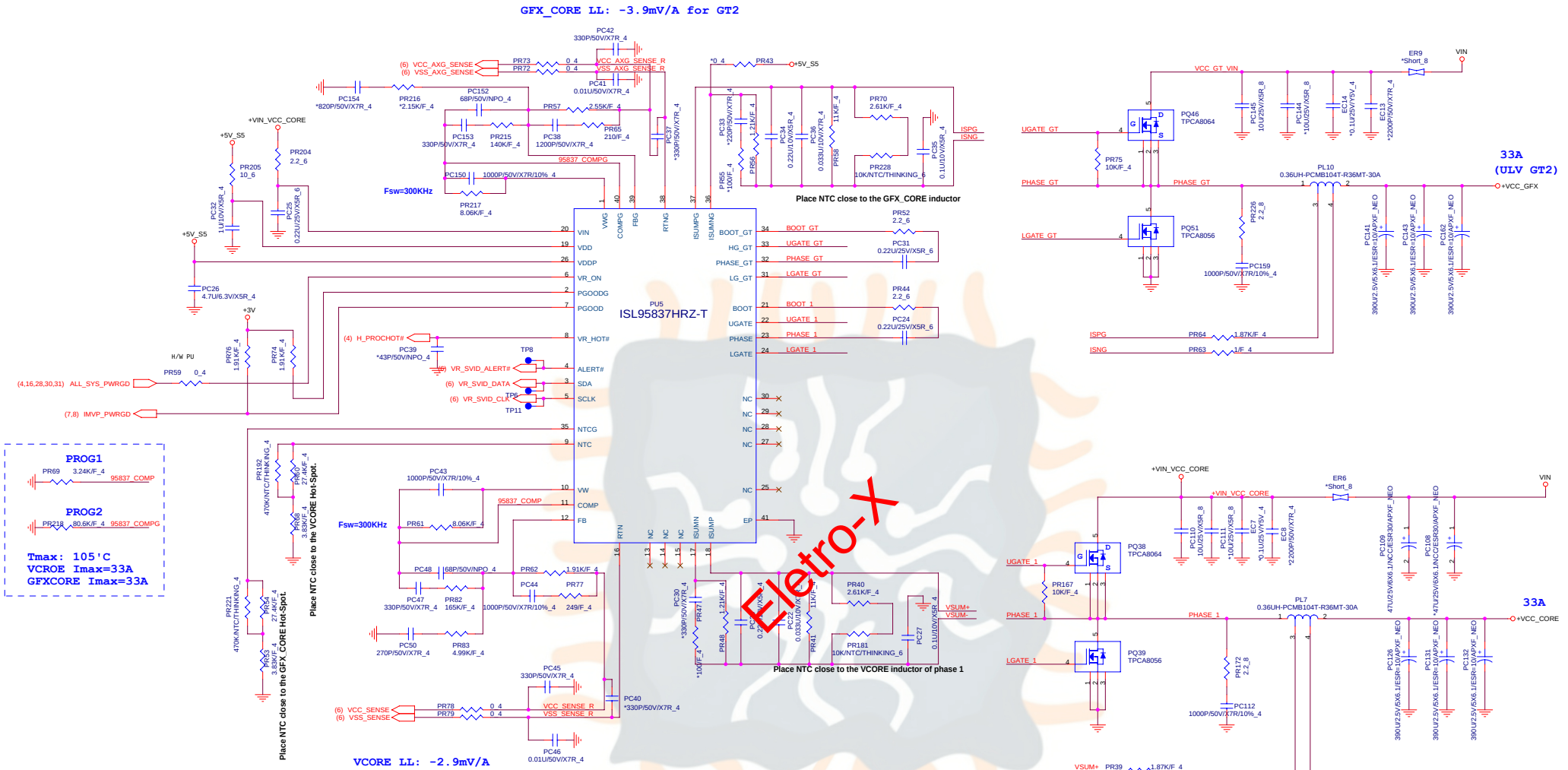
Power SW Board Connector



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	LED/RF/KB/PS	1A
Date: Thursday, January 17, 2013	Sheet 25 of 45	



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Quanta Computer Inc.
PROJECT : XXX
Size | Document Number: +VCC_CORE (ISL95837) | Rev: 1A
Date: Thursday, January 17, 2013 | Sheet

ELEtRO-L

3.3V & 5V

FREQ: 400KHZ

FREQ: 500KHZ

0.6A

10mil

7.5A

5A

2.0A

1.2A

1.5A

+3V_SUS for DS3

For EuP Lot 6 (2nd stage)

Quanta Computer Inc.

PROJECT : Chief River

3VPCU&5VPCU(TPS51427A)

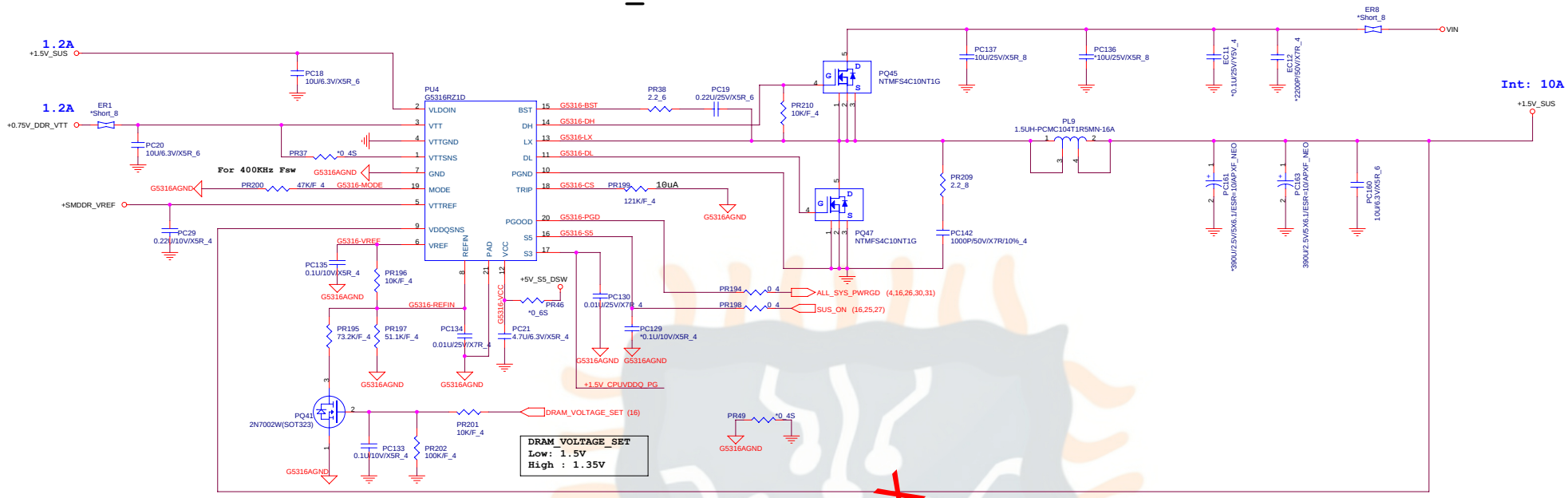
Size | Document Number | Rev

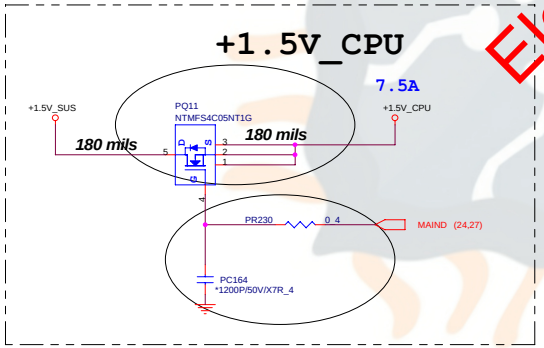
Date: Thursday, January 17, 2013 | Sheet

1.Level 1 Environment-related Substances Should Never be Used.

2.Recycled Resin and Coated Wire should be procured from Green Partners.

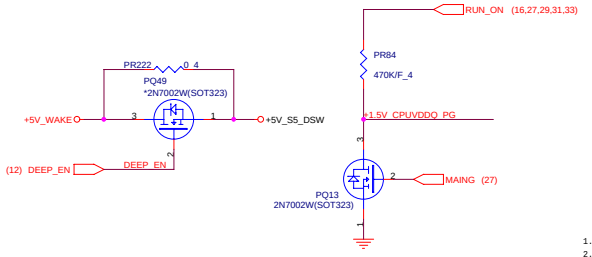
1.5VSUS & VTT_MEM

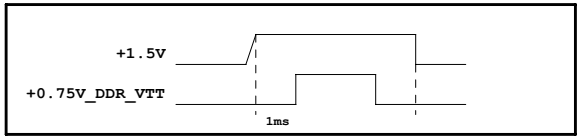




MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off





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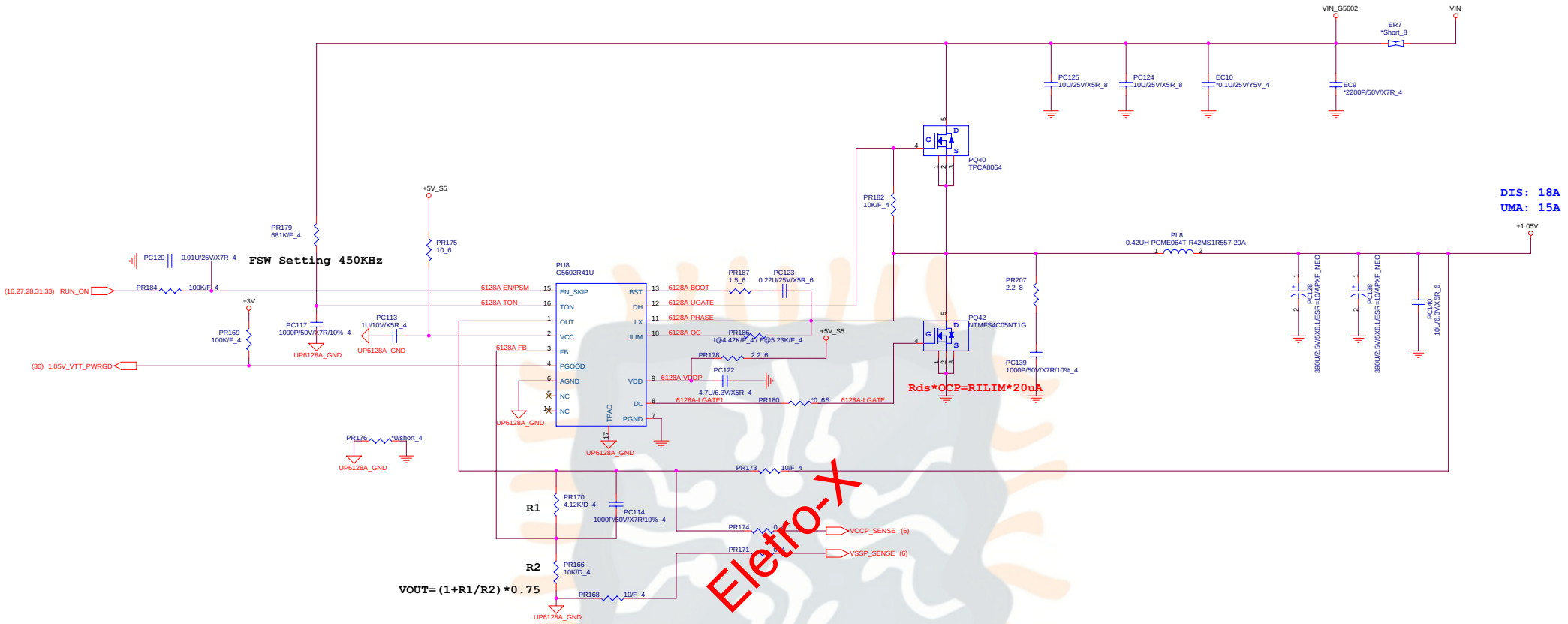
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	1.5VSUS/VTT_MEM	1A
Date: Thursday, January 17, 2013	Sheet	

+1.05V / 15.0A



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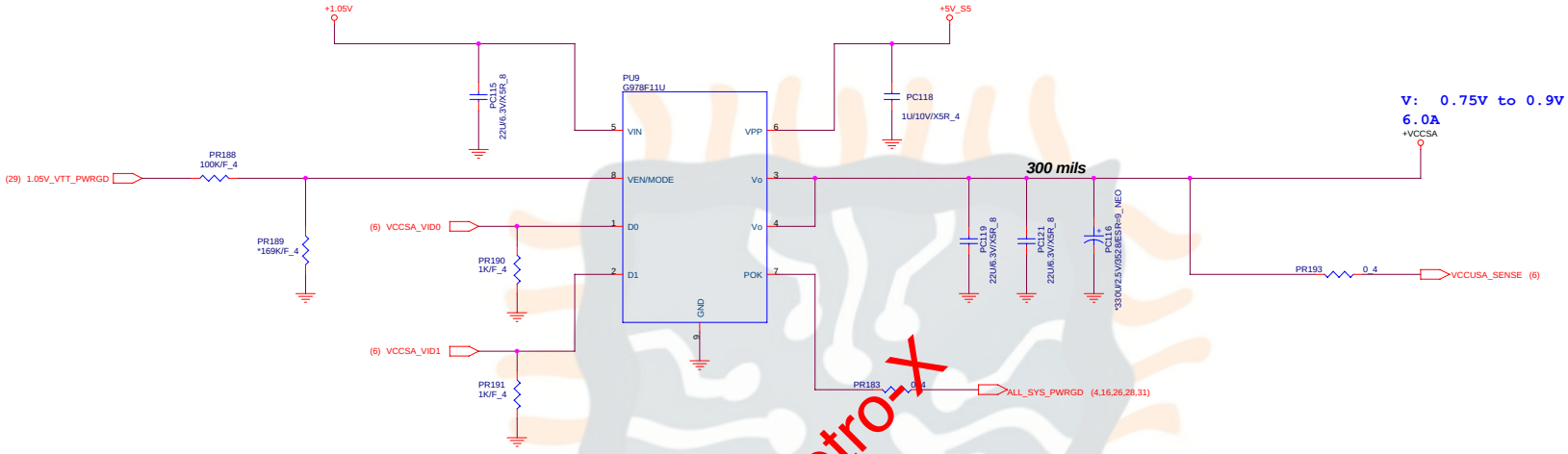
Quanta Computer Inc.
PROJECT : Chief River
Size | Document Number | Rev
+1.05V (UP1522RQDD)
Date: Thursday, January 17, 2013 | Sheet

+VCCSA



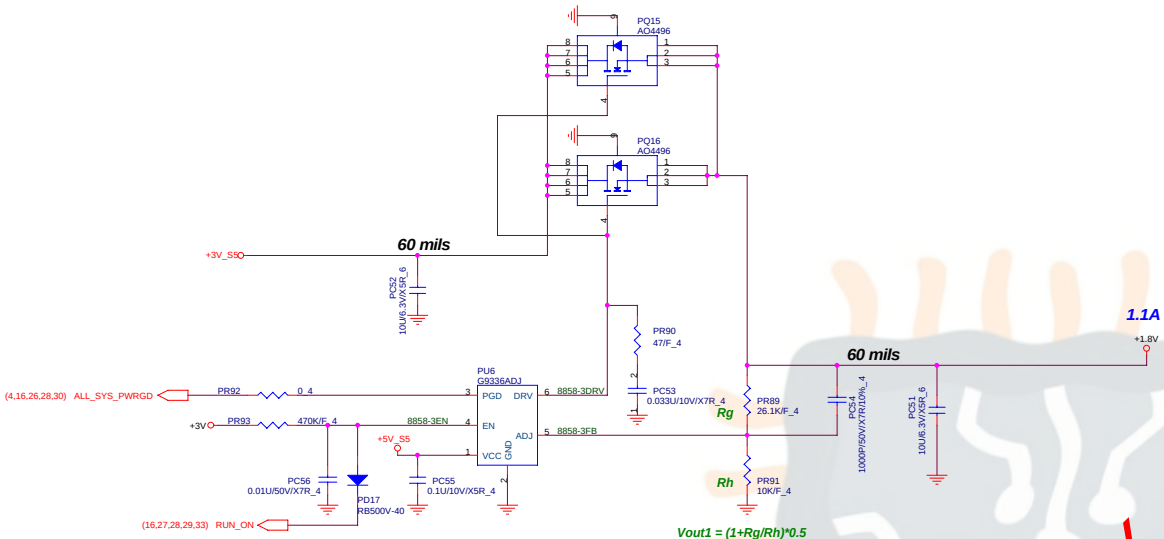
For Chief River ULV

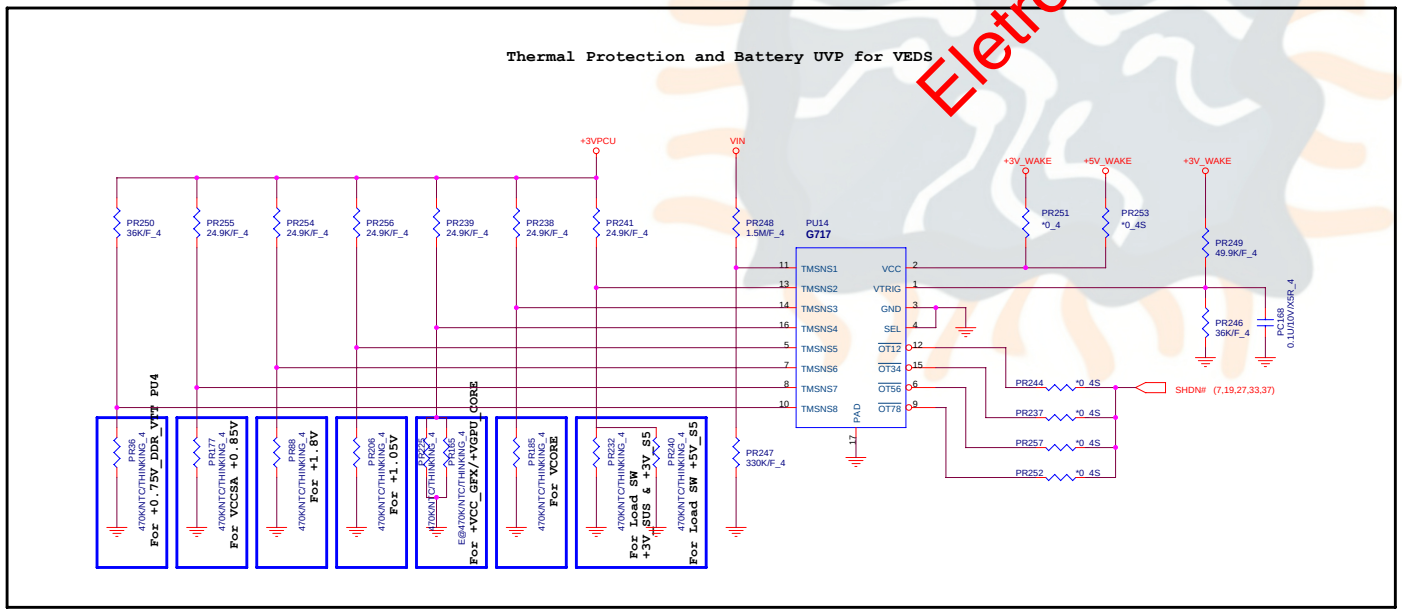
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : Chief River
Size | Document Number | Rev 1A
VCCSA / VCCIO
Date: Thursday, January 17, 2013 | Sheet

VCC1.8





Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	VCC1.8	1A
Date: Thursday, January 17, 2013	Sheet	

1.Level 1 Environment-related Substances Should Never be Used.
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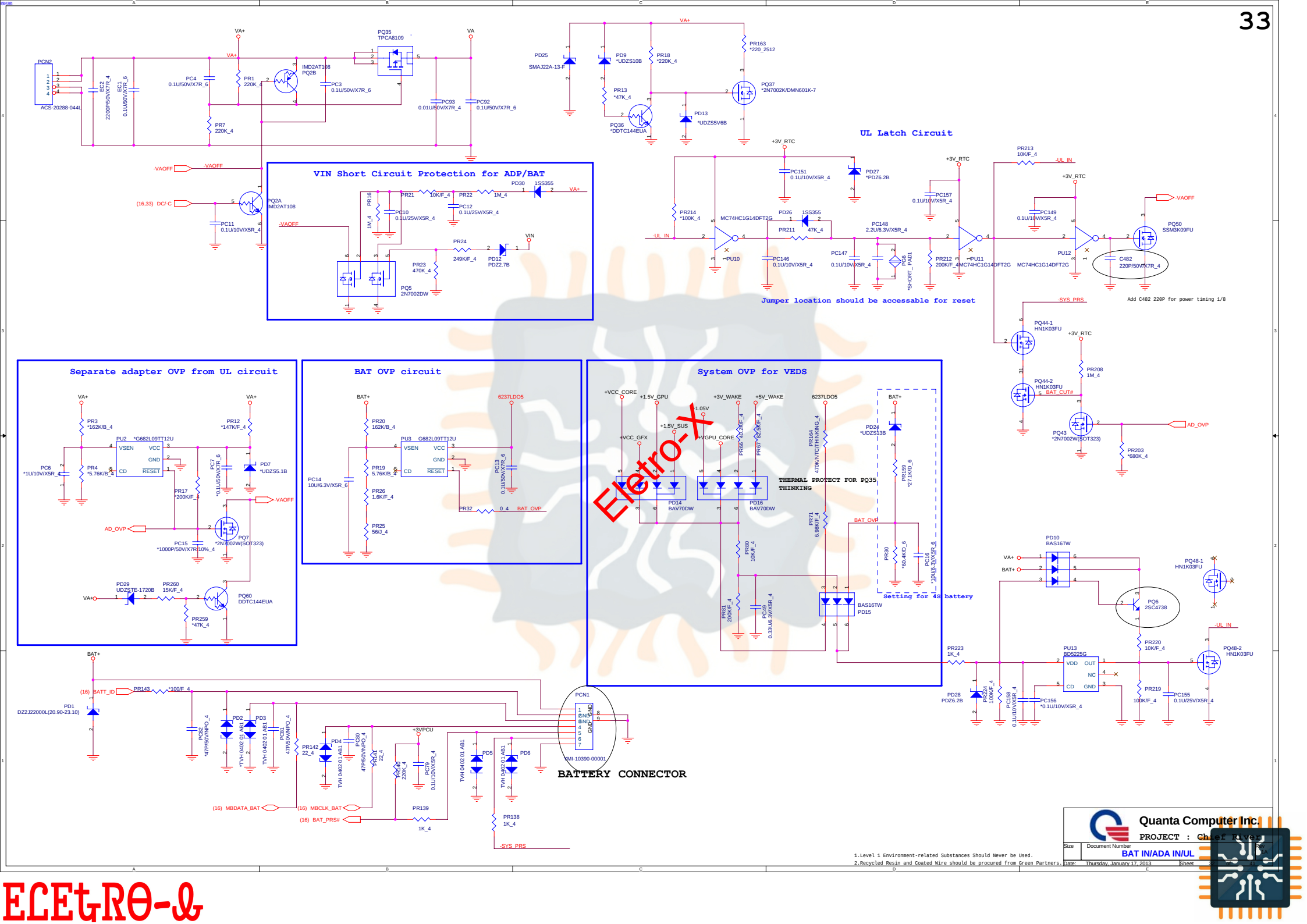
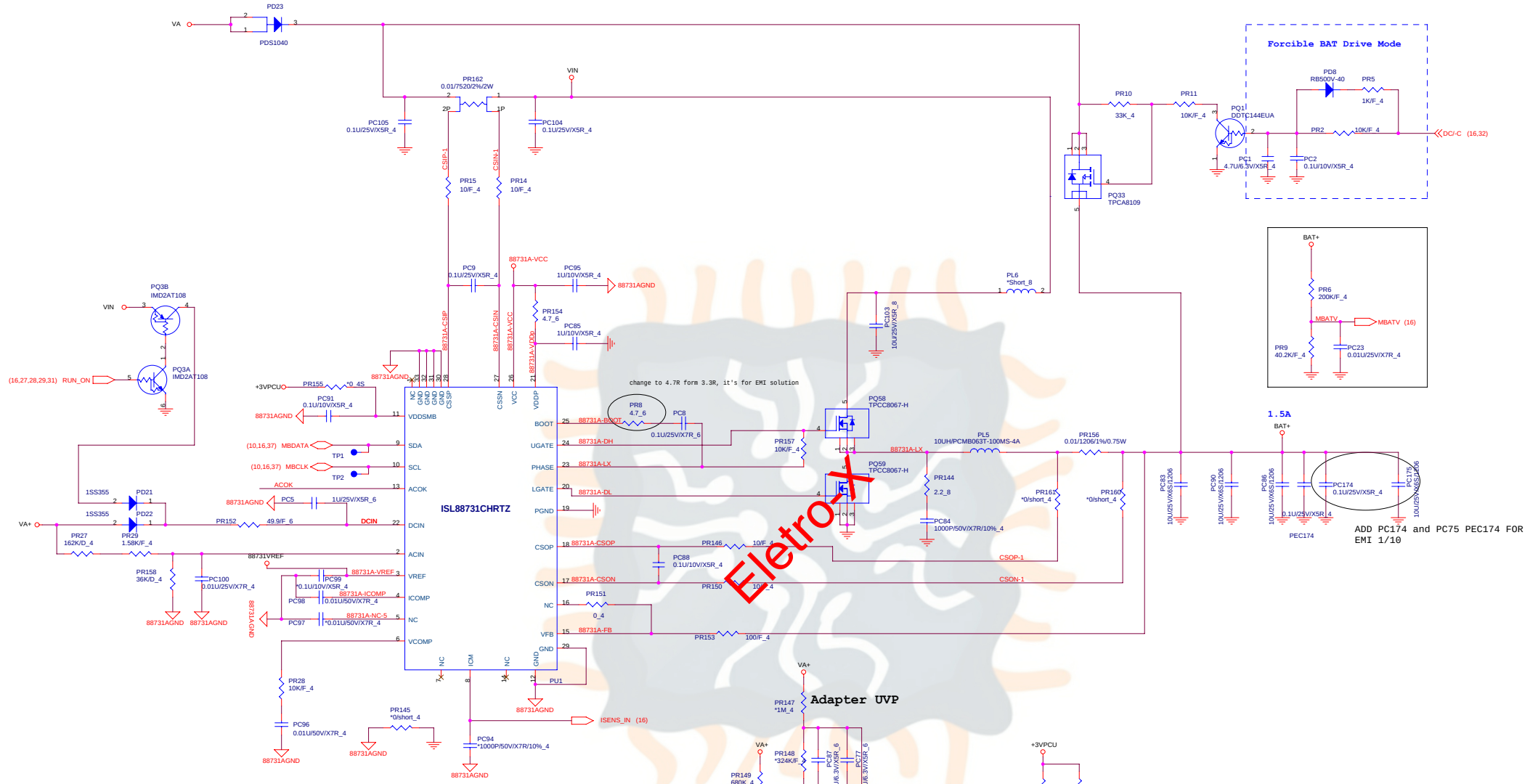

VIN Short Circuit Protection for ADP/BAT
UL Latch Circuit
Jumper location should be accessable for reset
Separate adapter OVP from UL circuit
BAT OVP circuit
System OVP for VEDS
THERMAL PROTECT FOR PQ35
THINKING
Setting for 4S battery
BATTERY CONNECTOR
Eletro-X
Quanta Computer Inc.
PROJECT : Chief River
BAT IN/ADA IN/UL
Thursday, January 17, 2013
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

ELETRO-L



	ACOK	SHDN#	ACIN
ADP Normal	1	1	1
ADP UVP	0	0	0

1.Level 1 Environment-related Substances Should Never be Used.
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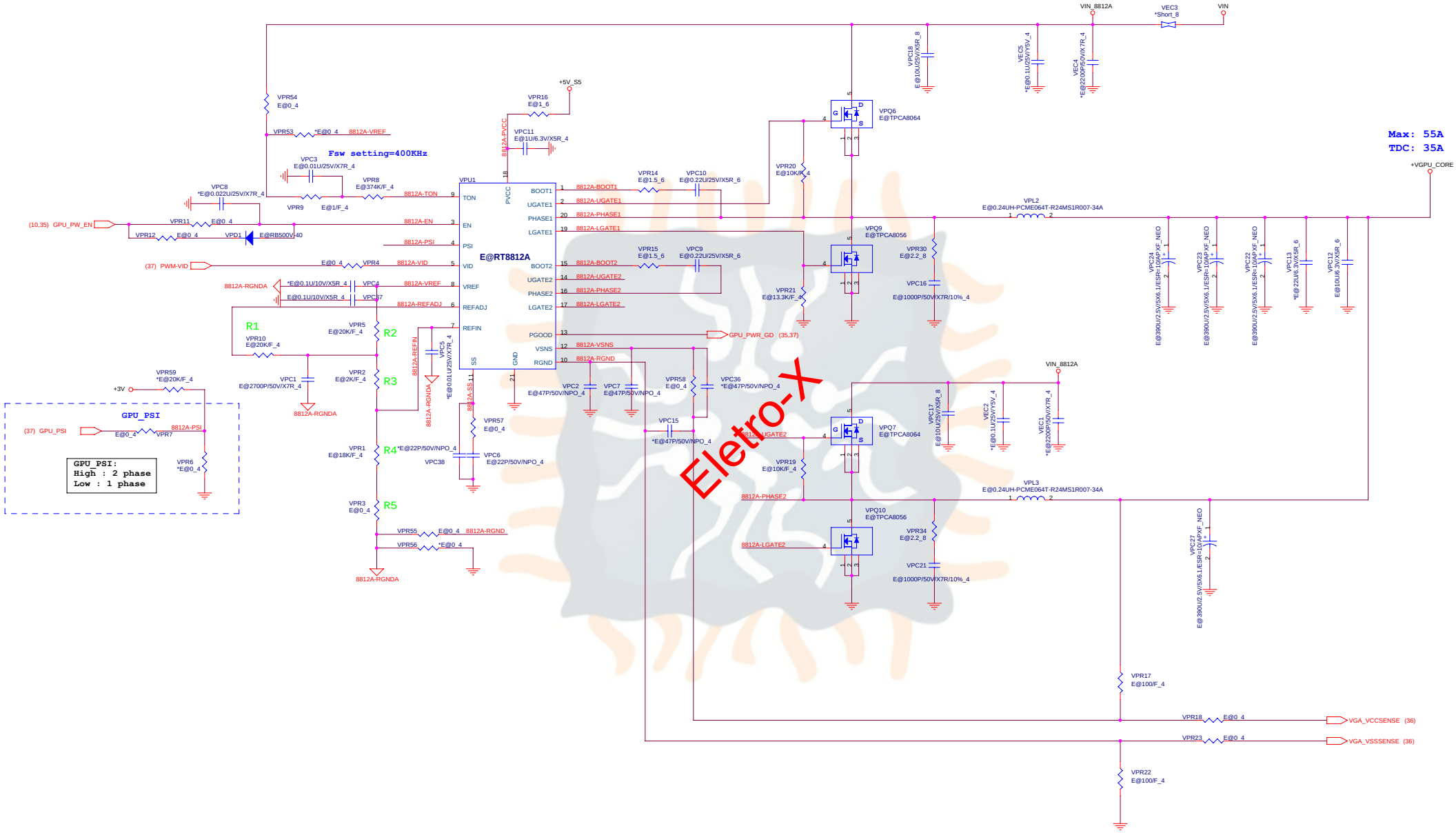
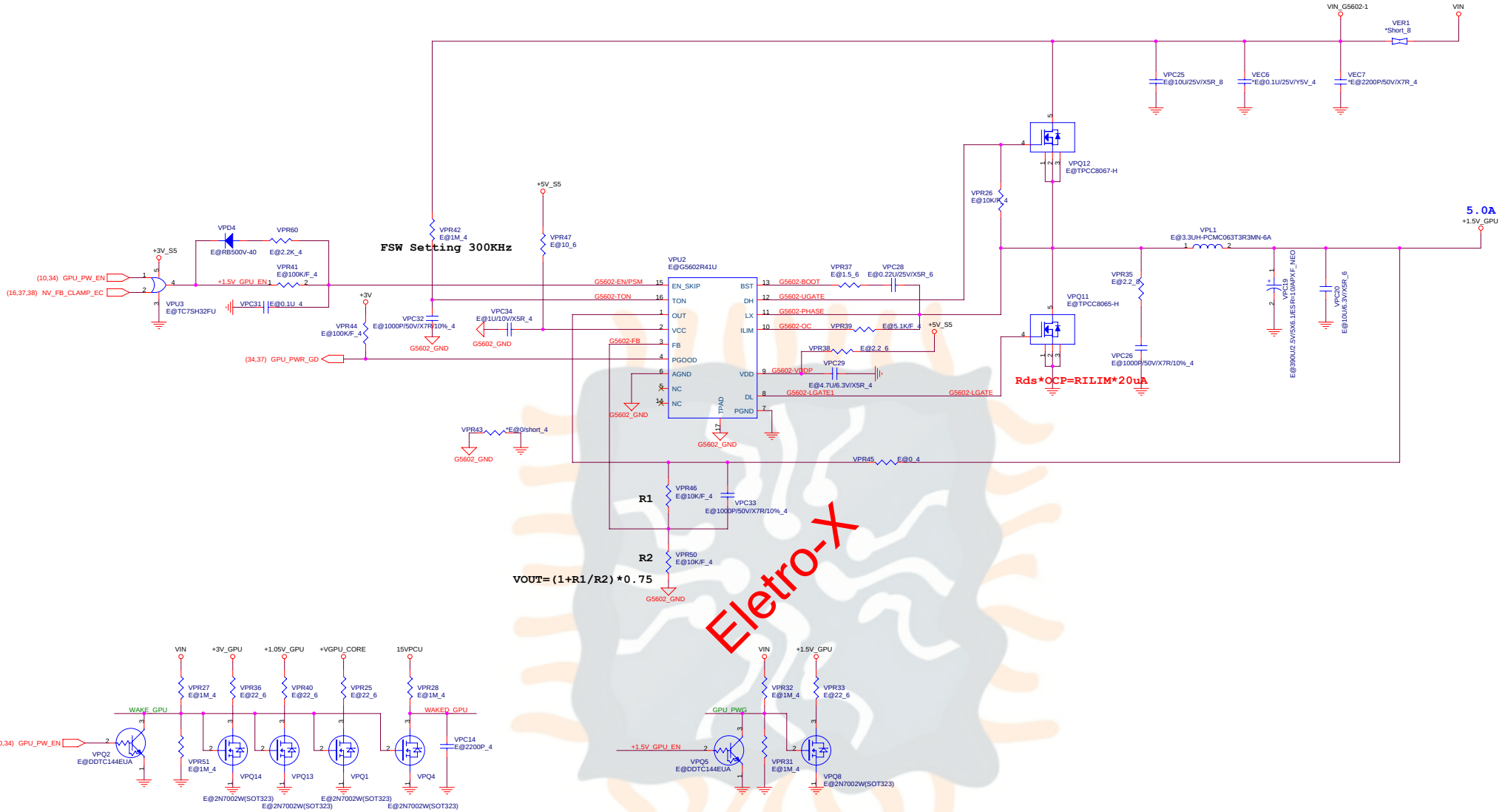
PROJECT : Chief River
Size | Document Number | Rev
CHARGER(ISL88731C)
Date: Thursday, January 17, 2013 | Sheet

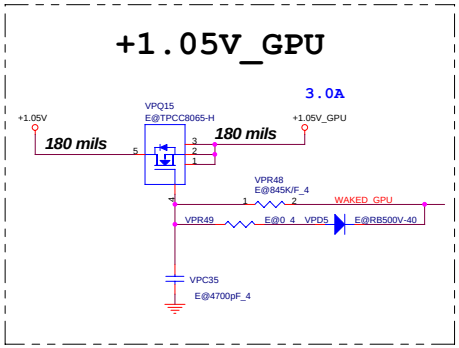
VGA-CORE

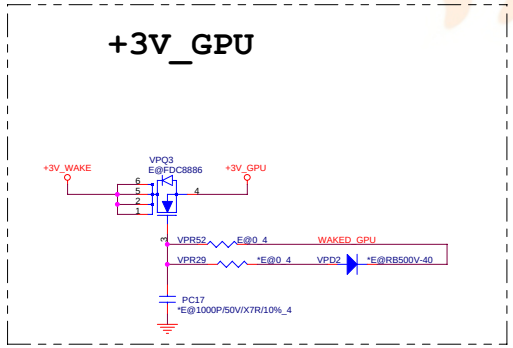


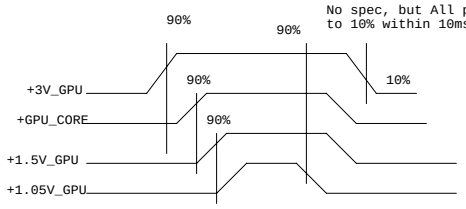
Quanta Computer Inc.	
PROJECT : Chief River	
Size	Document Number: VGA_CORE (RT8812A)
Date: Thursday, January 17, 2013	Sheet

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.









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PROJECT : Chief River

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	1.8_GPU / 1.0_GPU	1A
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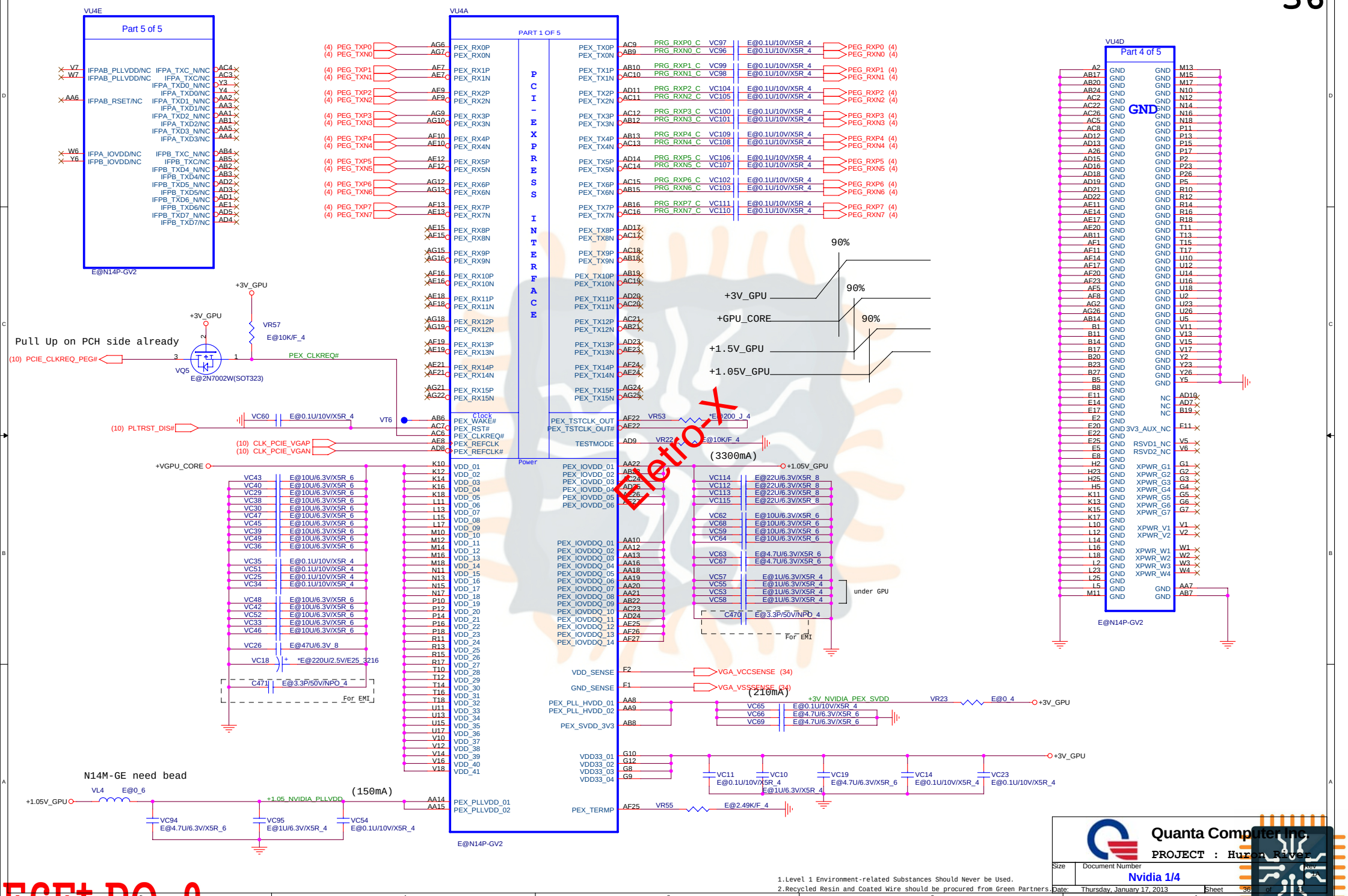

1.Level 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	Nvidia 1/4	

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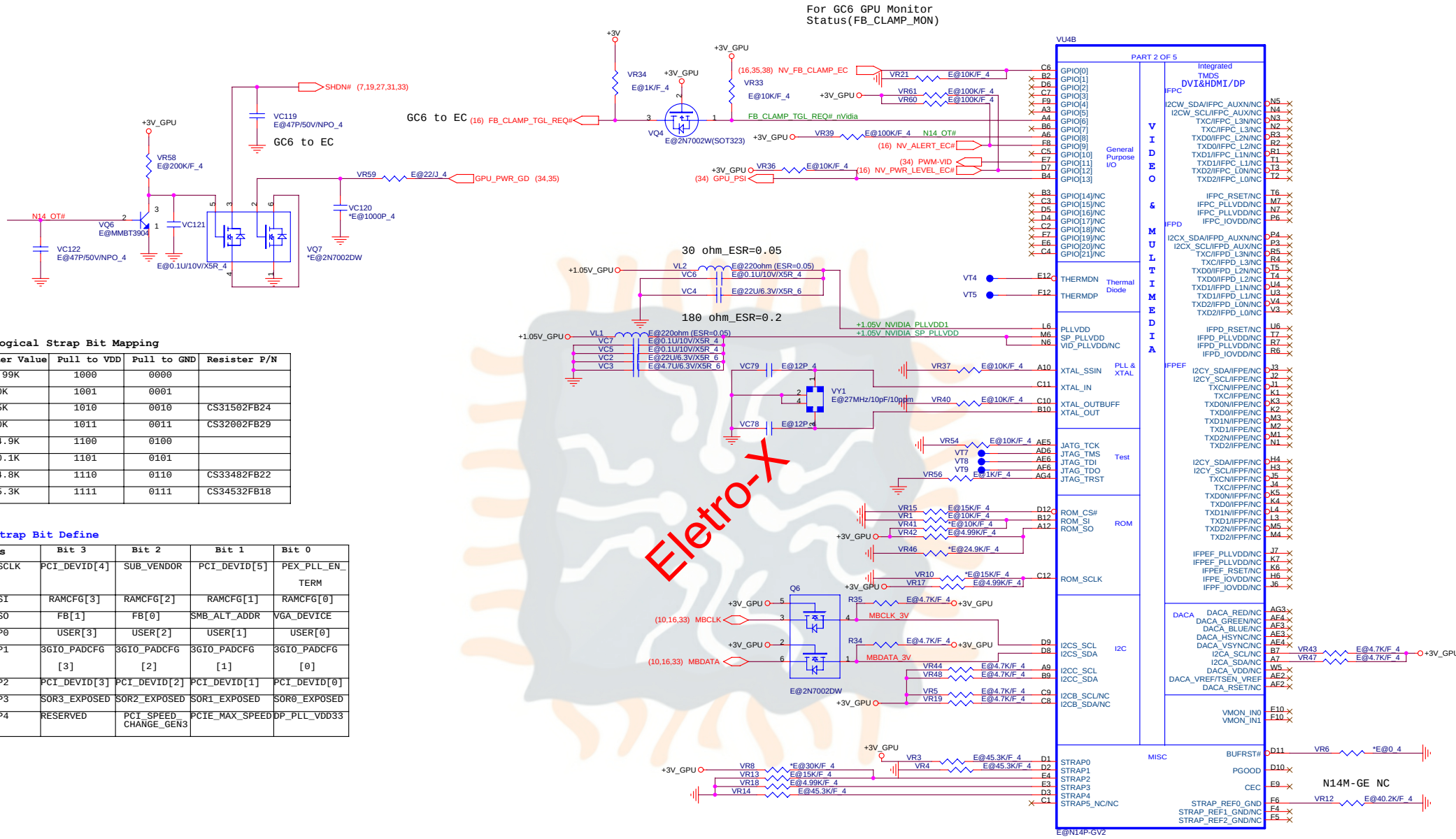

N14 Logical Strap Bit Mapping

Resister Value	Pull to VDD	Pull to GND	Resister P/N
4.99K	1000	0000	
10K	1001	0001	
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	
30.1K	1101	0101	
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

N14 Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33

	VRAM Capacity	VRAM Vender	ID	VR1	Mfr P/N	Quanta P/N
N14M-LP N14P-GV2	128Mx16 DDR3	Samsung	0111	PD45.3K	K4W2G1646E-BC11	AKD5MGGT525
		Hynix	0110	PD34.8K	H5TQ2G63DFR-11C	AKD5MGWTW15
	256Mx16 DDR3	Samsung	0011	PD20K	K4W4G1646B-HC11	AKD5MGWT525
		Hynix	0010(TBD)	PD15K	H5TC4G63AFR-11C	AKD5PGWTW10

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	Nvidia 2/4	1A
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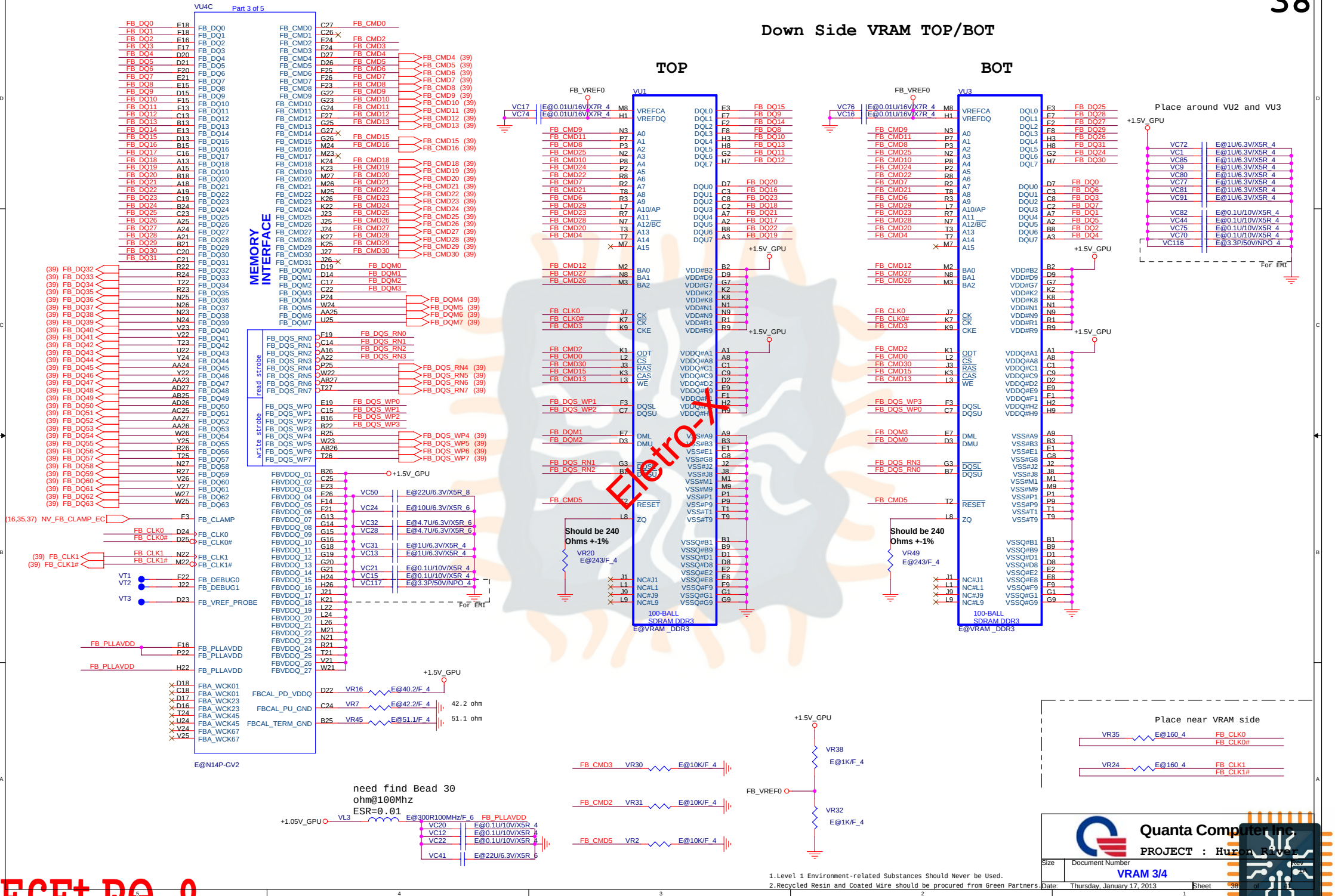
N14M-GE NC

Down Side VRAM TOP/BOT



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PROJECT : Huron River

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	VRAM 3/4	

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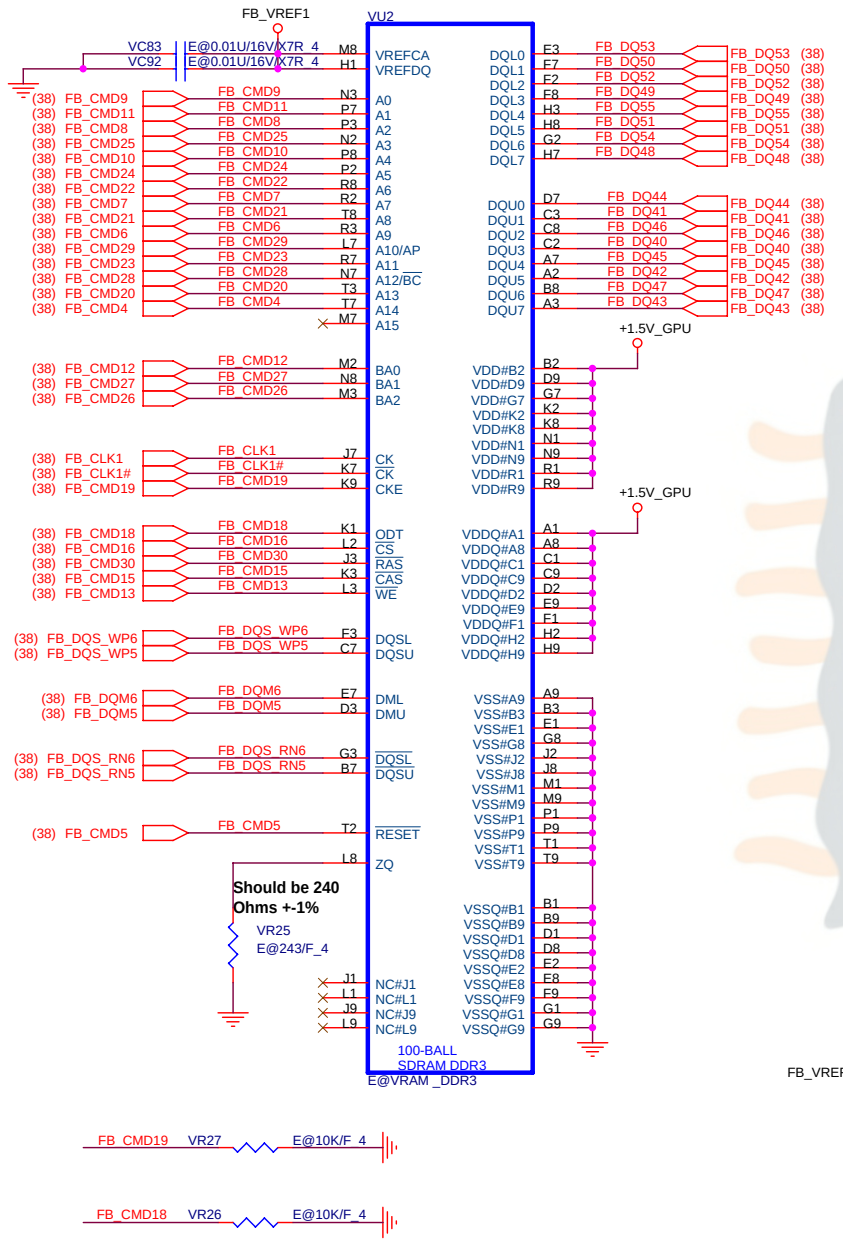
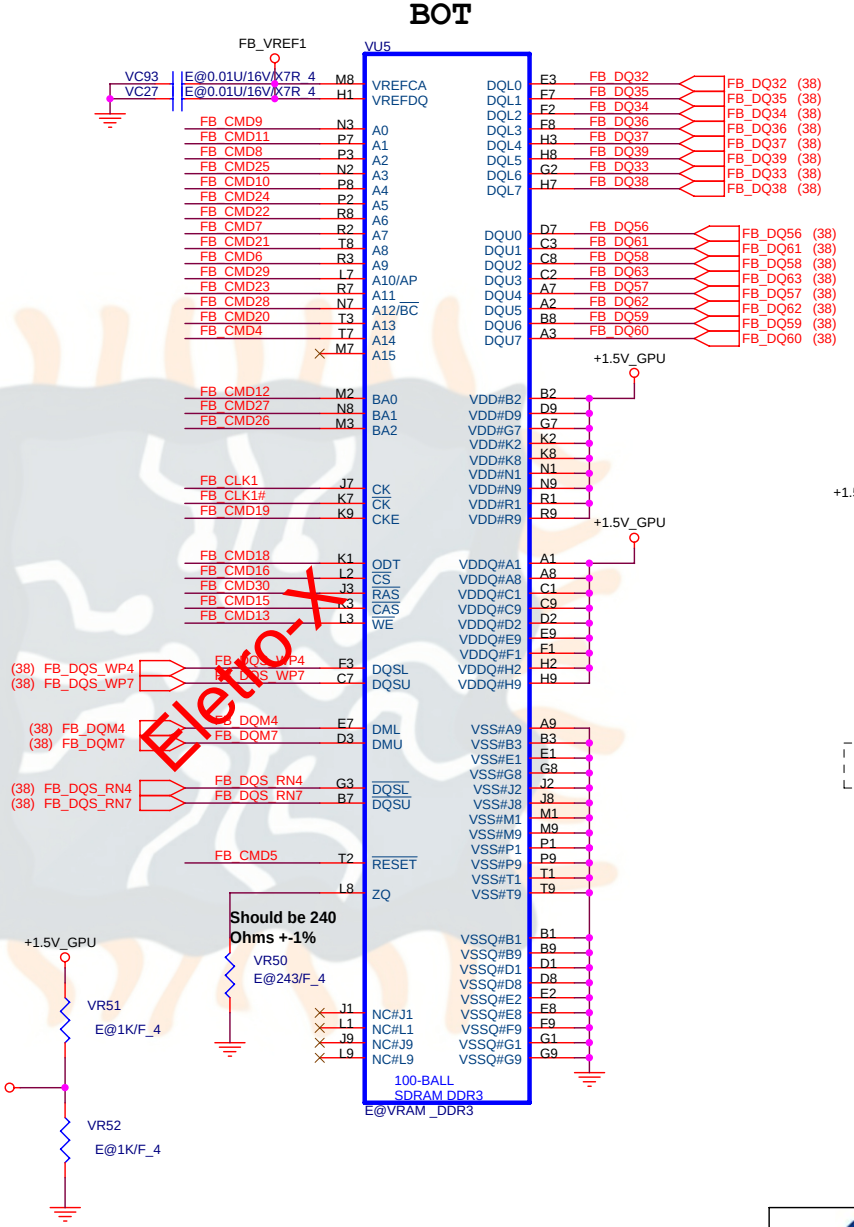
Up Side VRAM TOP/BOT

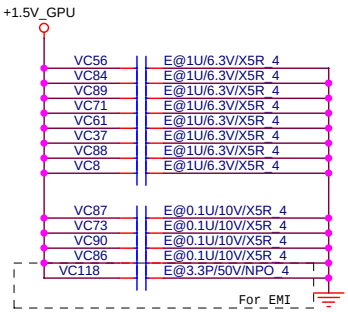
TOP



BOT



Place around VU4 and VU5



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Quanta Computer Inc.
PROJECT : Huron River

Size	Document Number	Rev
	VRAM 4/4	1A
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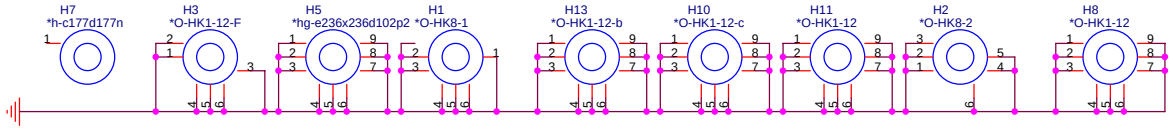
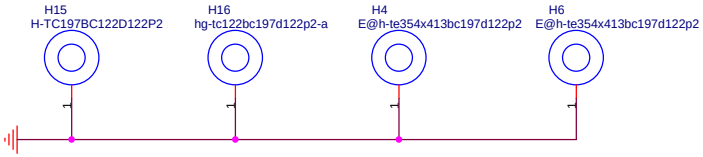
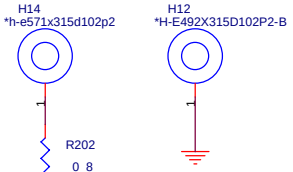
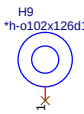
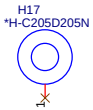
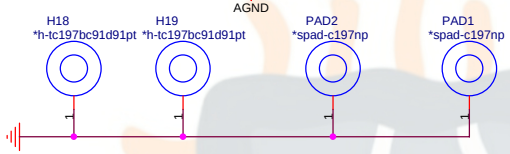




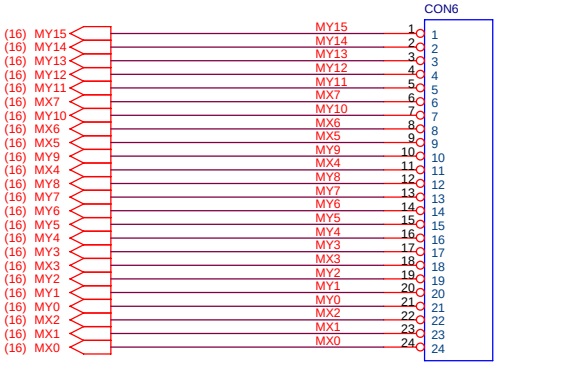








KEY BOARD Connector



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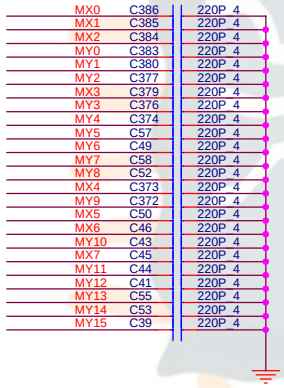

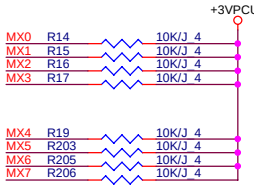

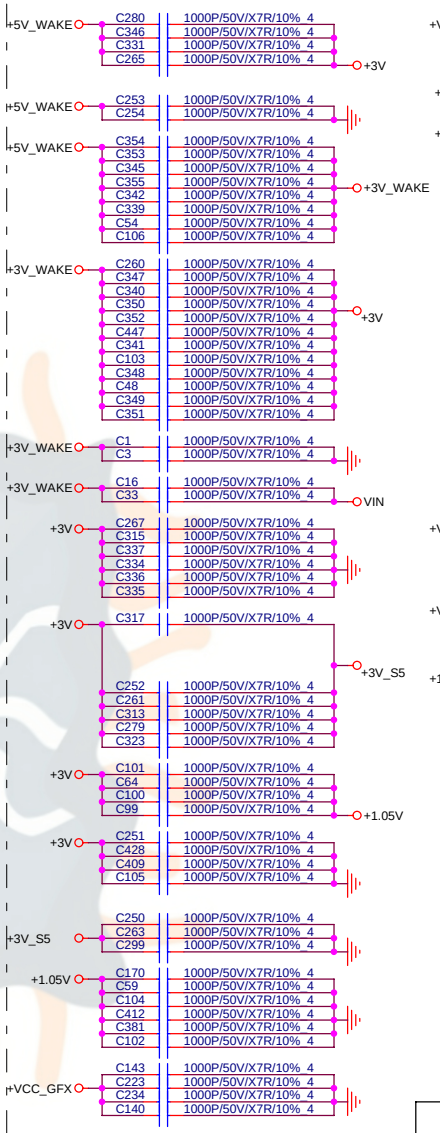

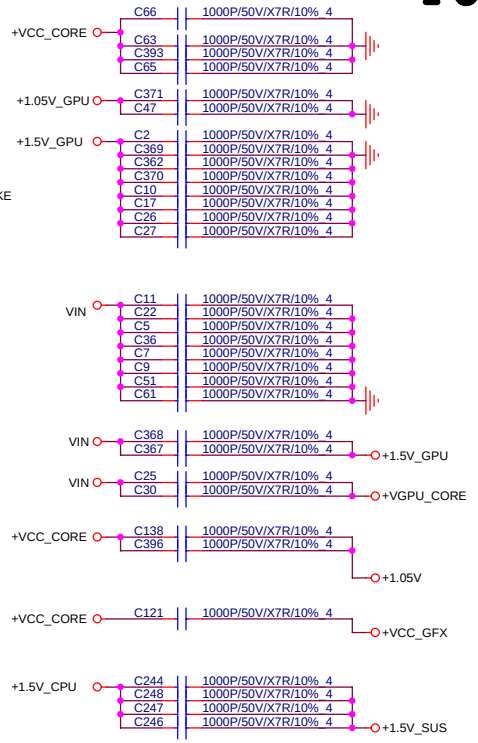

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : HK5

Size	Document Number	Rev
	HOLE/EMI/KB	1A
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USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN3.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	NFC
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	Card Reader
PORT 12	Touch Screen
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111G)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
Nvidia	1001 1110	-	1001 1110	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS35A	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	0	1
Board ID0	CaspiCRA1-CaspiCRB1 HK8-HK9	SuperiorCRA1-SuperiorCRB1 GD5-GD6
Board ID1	HK8/GD5 14"	HK9/GD6 15"

PCBA SKU	Discrete	UMA
R280(Pull High)	Stuff	No Stuff
R279(Pull Low)	No Stuff	Stuff

	S0	S3	DS3	S4	S5 (Charger Enable)	S5 (Charger Disable)	S5 (Soft OFF) (WoL Disable)	S5 (Soft OFF) (WoL Enable)
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+1.8V	H	L	L	L	L	L	L	L
+1.8V_GPU	H	L	L	L	L	L	L	L
+1.0V_GPU	H	L	L	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.5V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	H	L	L	H
+3V_WAKE	H	H	H	H	H	L	L	H
+5V_WAKE	H	H	H	H	H	L	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L