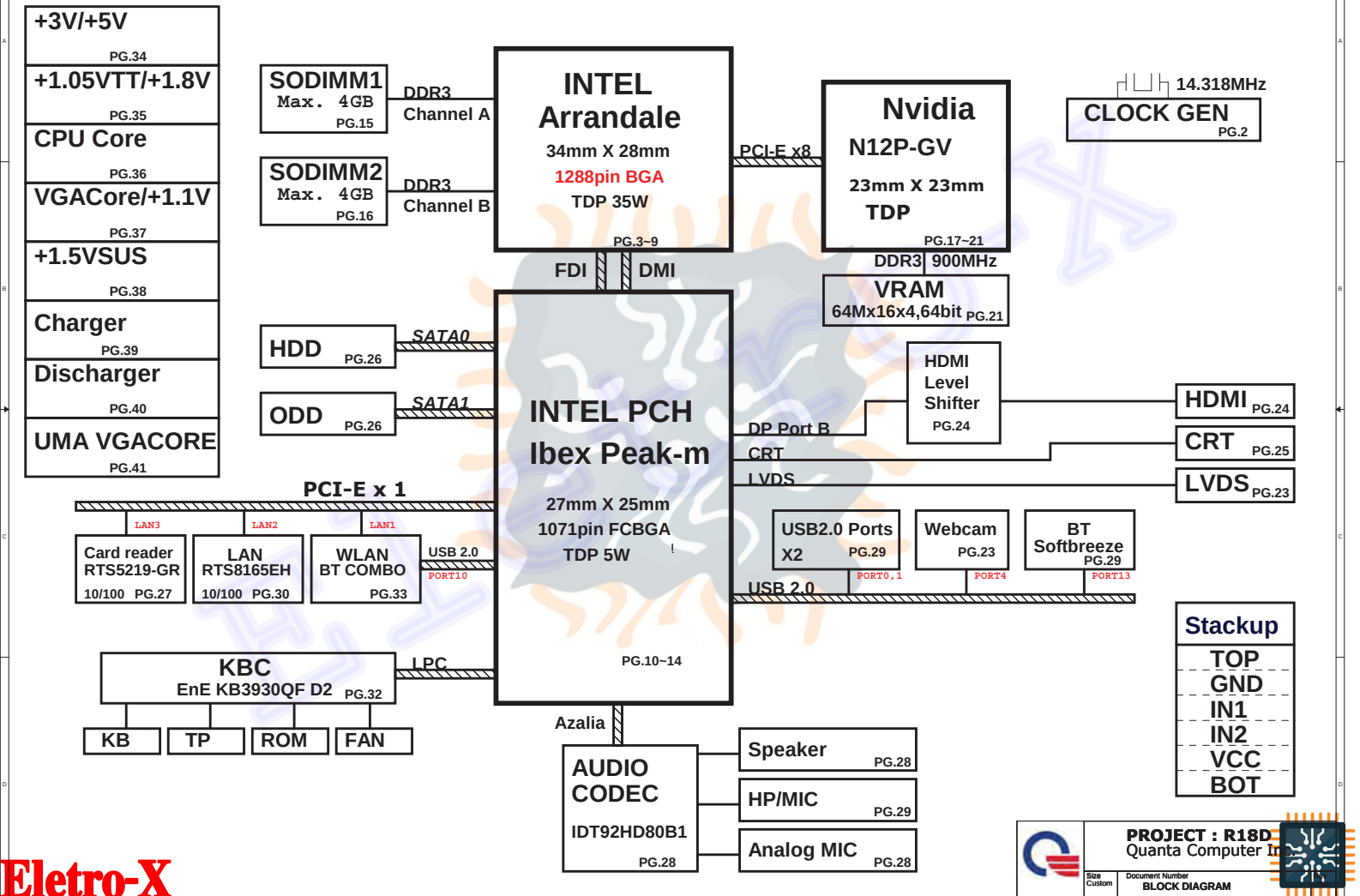
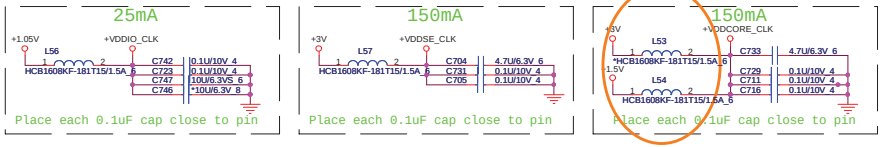
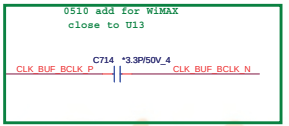
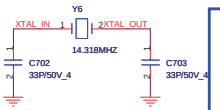
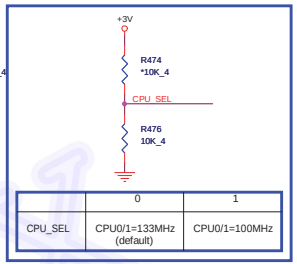
R18D INTEL UMA/DISCRETE SYSTEM DIAGRAM

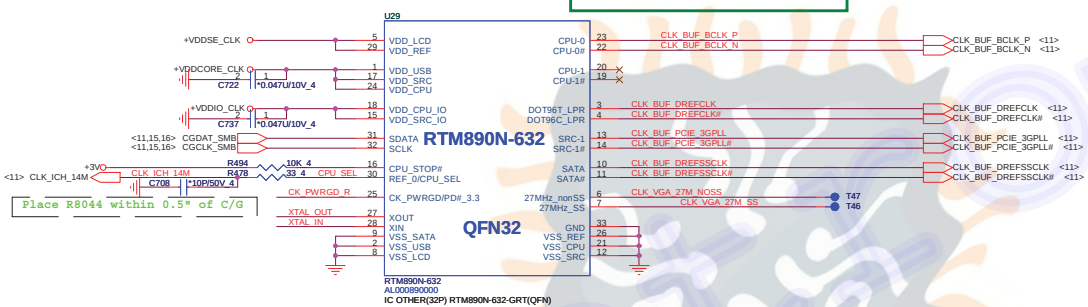


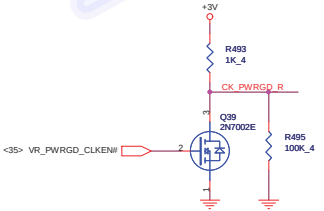








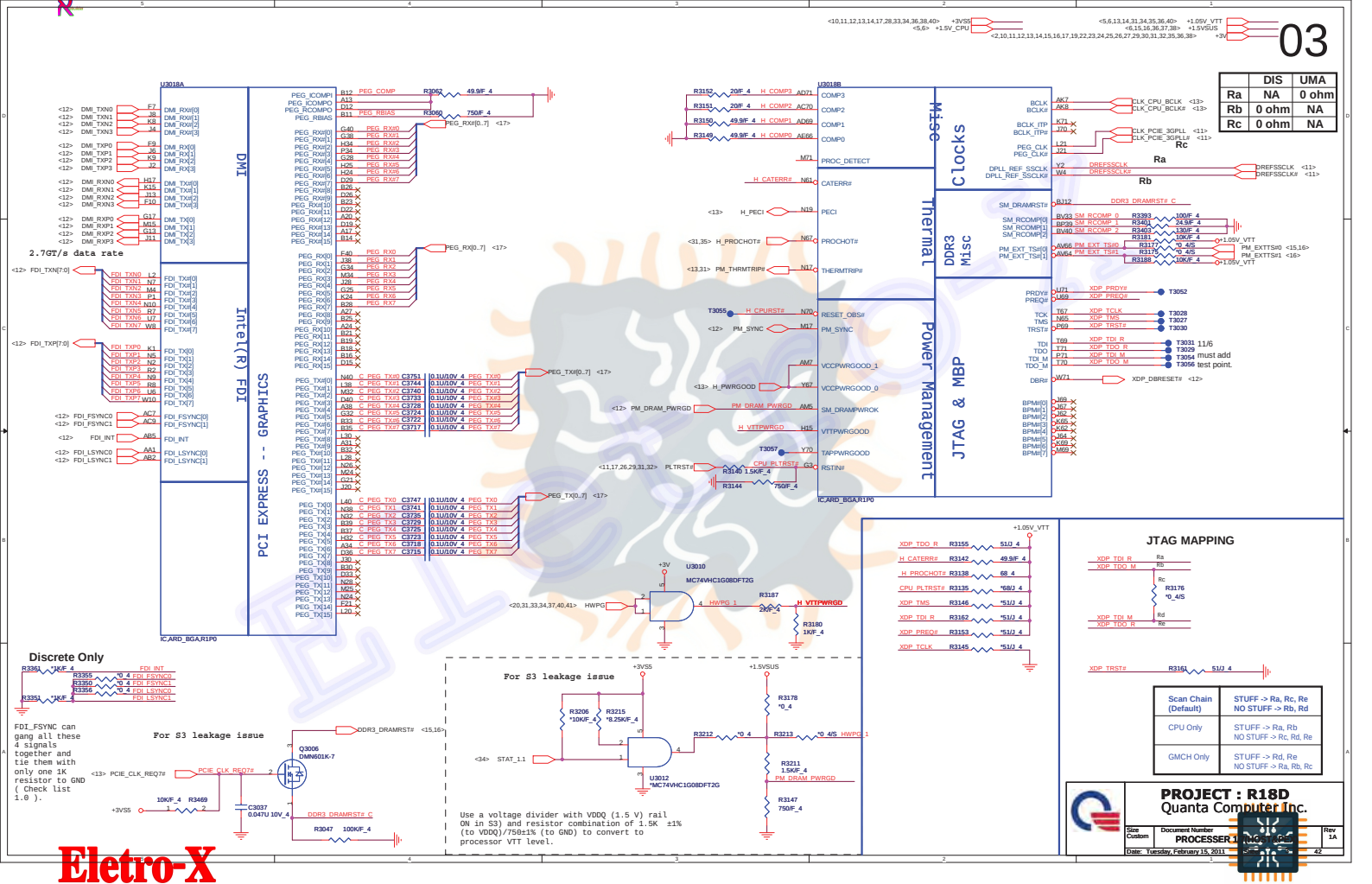




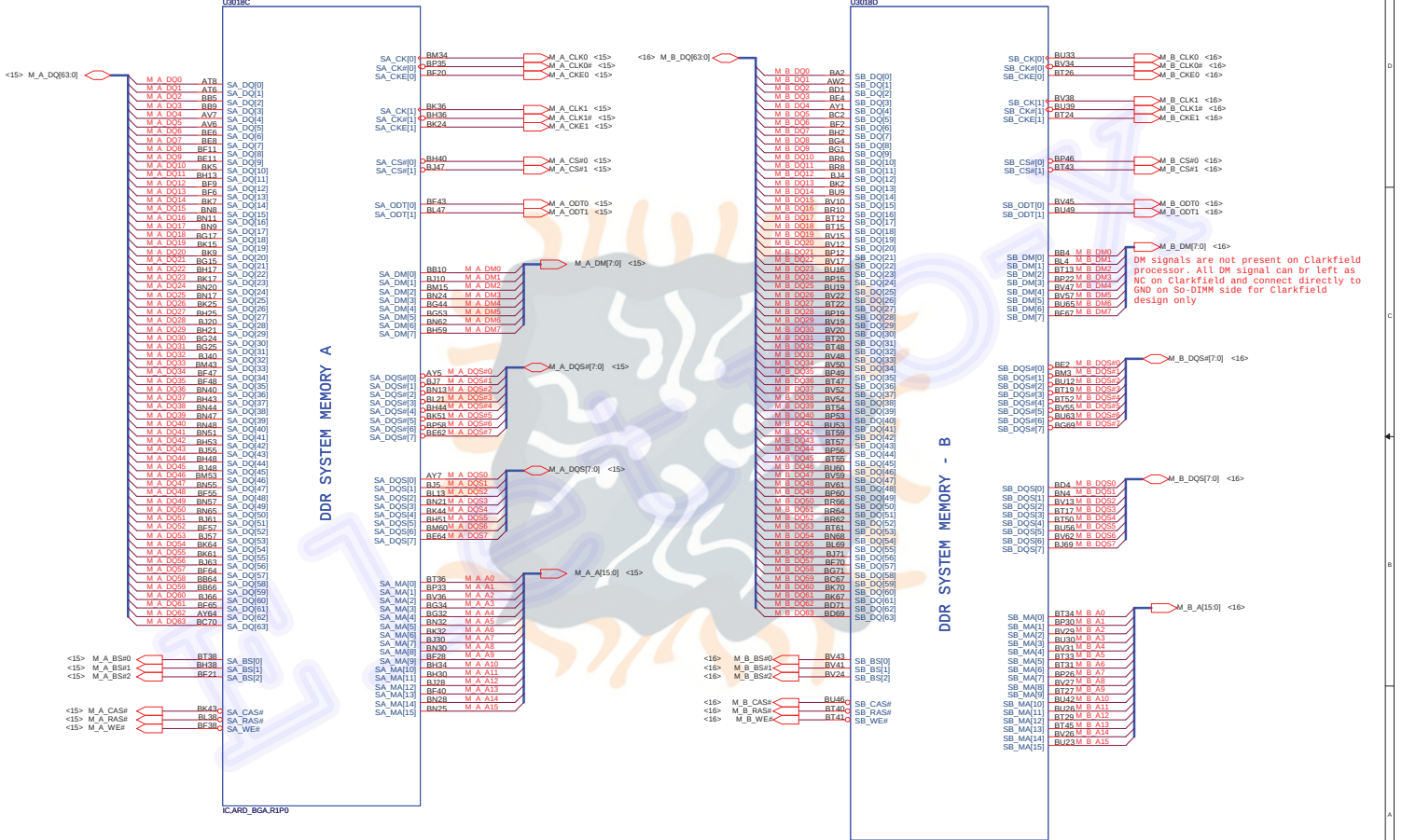
Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197001	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

PROJECT : R18D
Quanta Computer Inc.

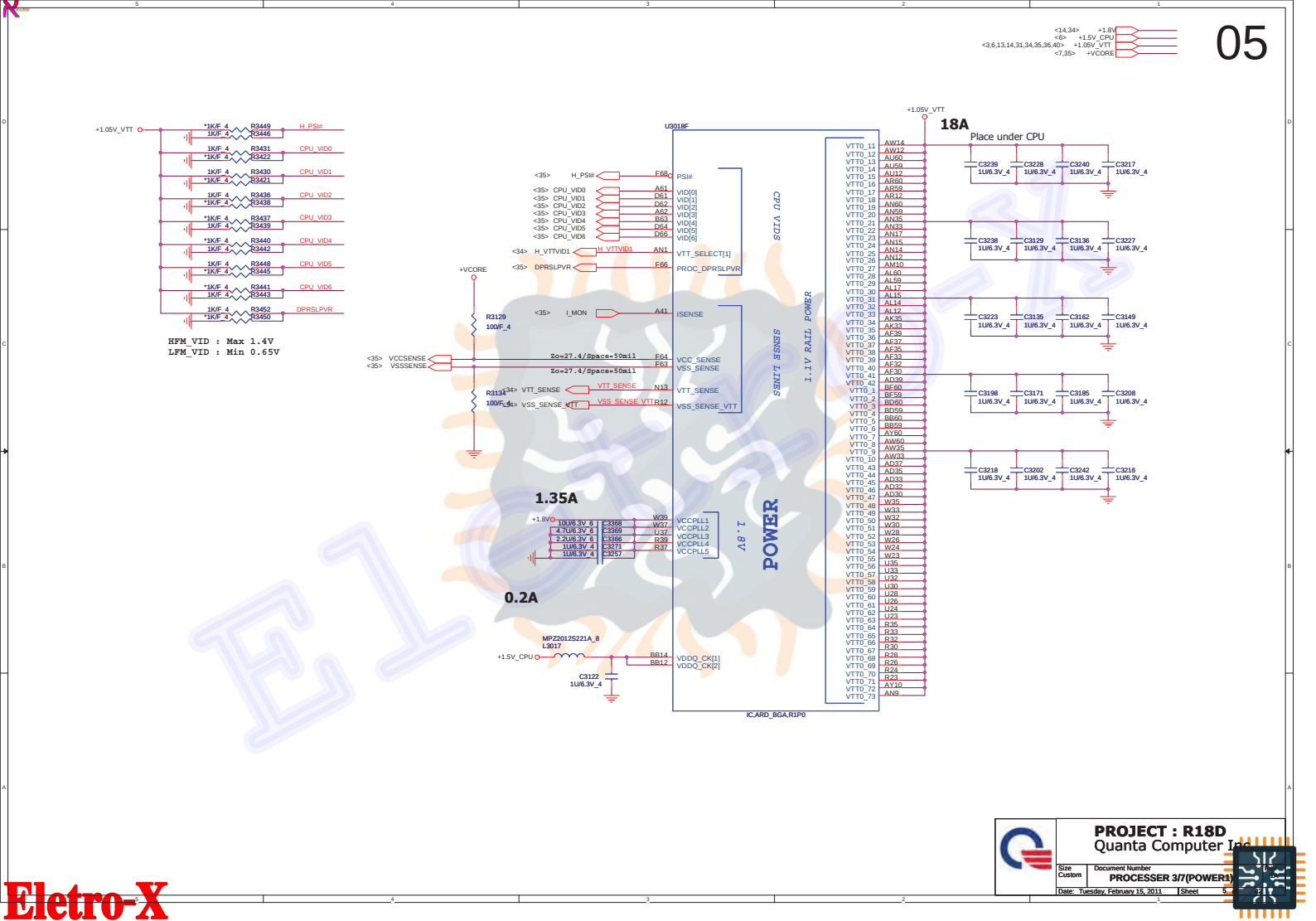
Size	Document Number	
Custom	Clock Gen(9LRS3197)	
Date: Tuesday, February 15, 2011	Sheet 2 of 42	

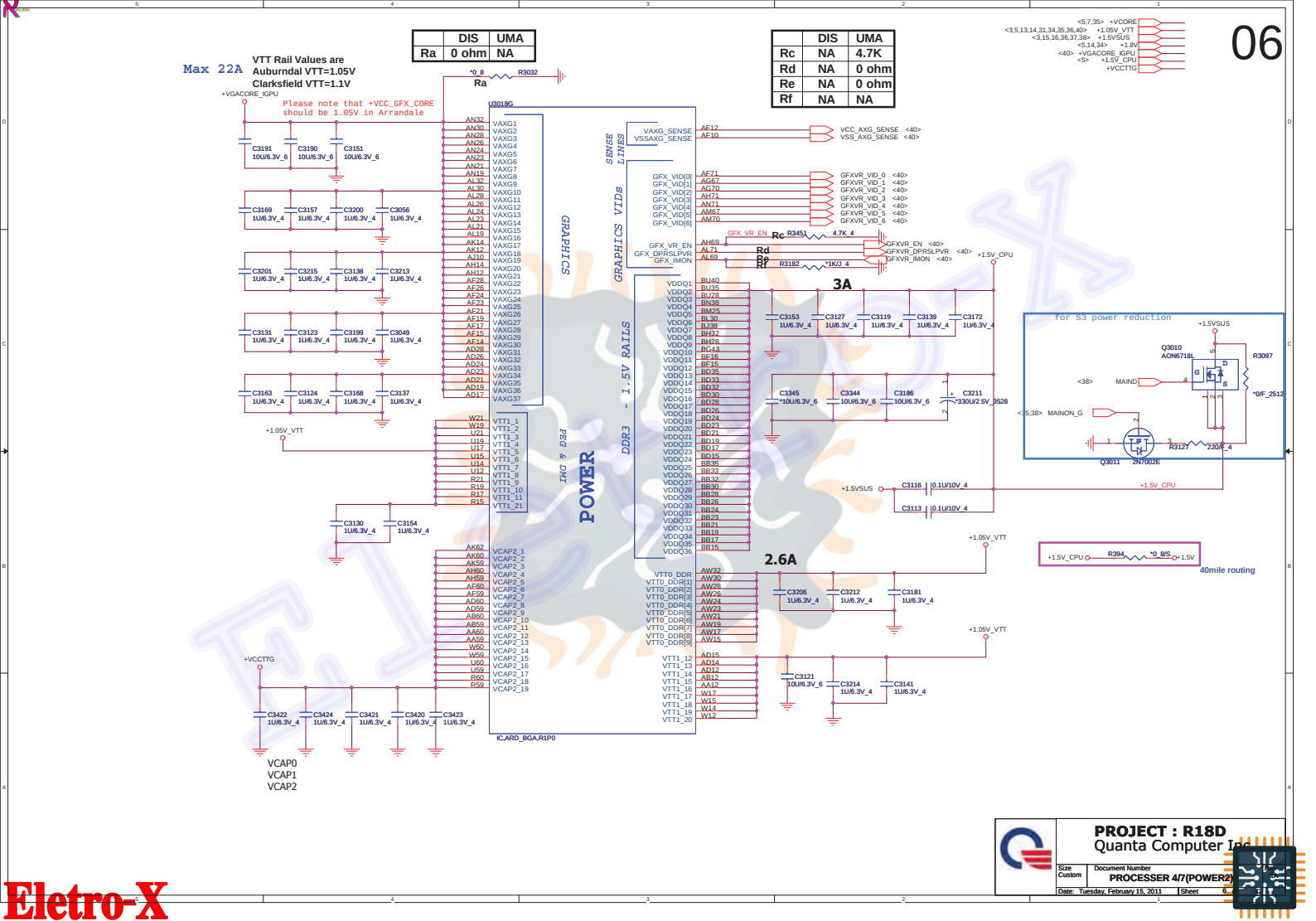

03
DIS UMA
Ra NA 0 ohm
Rb 0 ohm NA
Rc 0 ohm NA
U3018A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
2.7GT/s data rate
IC,ARD_BGA,R1P0
U3018B
Misc
Clocks
DDR3 Misc
Thermal
Power Management
JTAG & MBP
IC,ARD_BGA,R1P0
U3010
MC74VHC1G08DFT2G
Discrete Only
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).
For S3 leakage issue
Q3006
DMN601K-7
For S3 leakage issue
U3012
*MC74VHC1G08DFT2G
Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/75Ω±1% (to GND) to convert to processor VTT level.
+1.05V_VTT
JTAG MAPPING
Scan Chain (Default) STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc
PROJECT : R18D
Quanta Computer Inc.
PROCESSER (1 OF 6)
Size Custom
Document Number
Rev 1A
Date: Tuesday, February 15, 2011
Sheet 42
Eletro-X

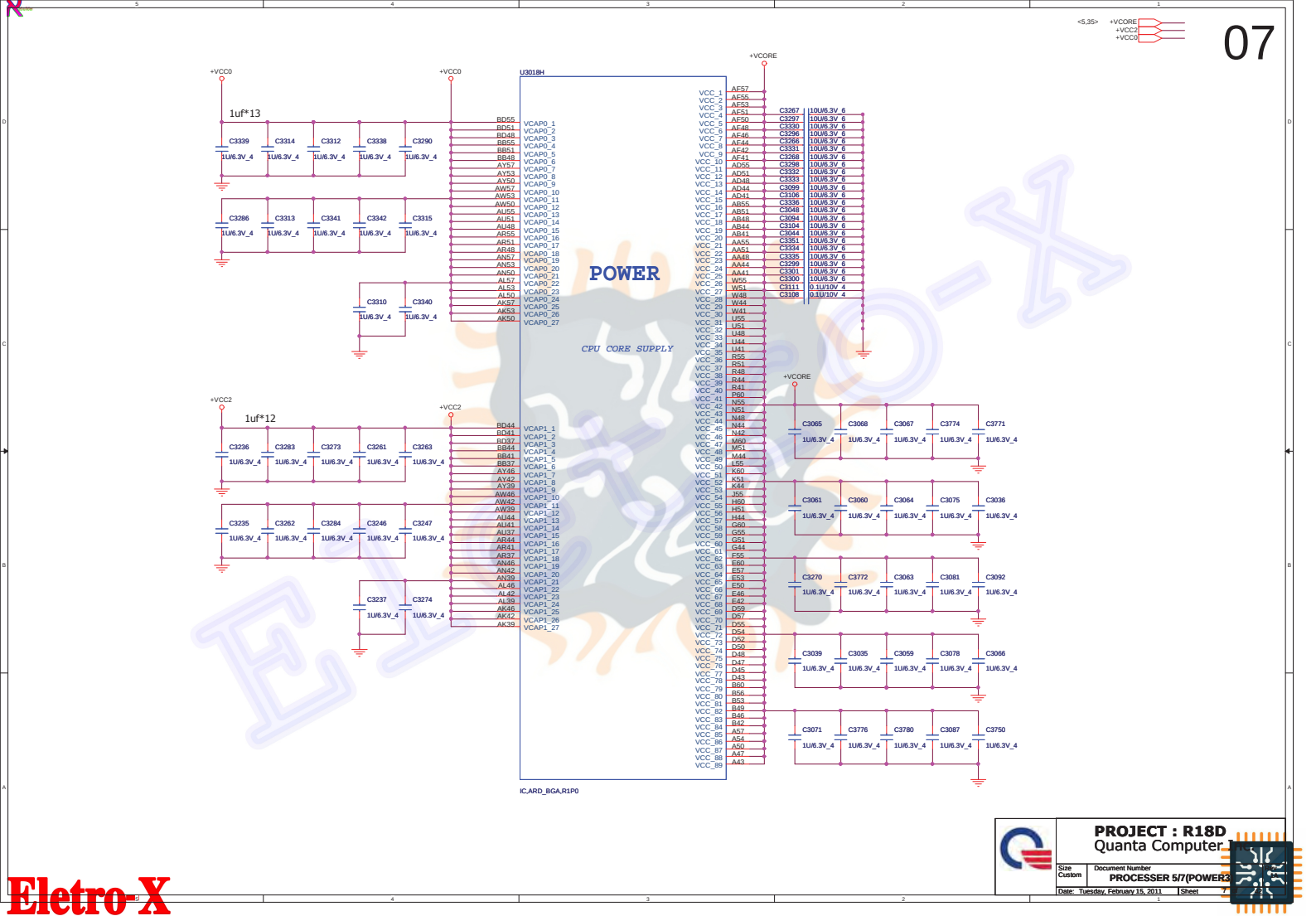
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : R18D		
Quanta Computer I		
Size: Custom	Document Number: PROCESSER 2/7(DDR3)	
Date: Tuesday, February 15, 2011	Sheet: 4	

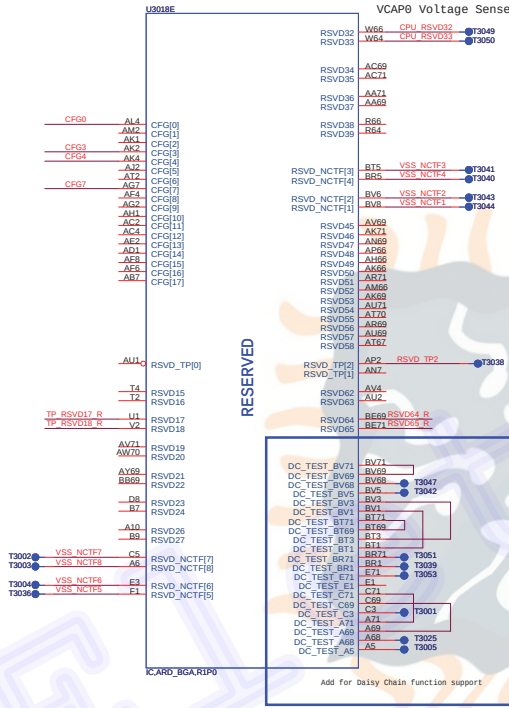

+1.05V_VTT
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
H_PSI#
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
DPRSLPVR
U3018F
CPU VIDS
SENSE LINES
1.1V RAIL POWER
1.8V POWER
18A
Place under CPU
1.35A
0.2A
+VCORE
+1.8V
+1.5V_CPU
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
VTT_SELECT[1]
PROC_DPRSLPVR
ISENSE
VCCPLL1
VCCPLL2
VCCPLL3
VCCPLL4
VCCPLL5
VDDQ_CK[1]
VDDQ_CK[2]
MPZ2012S221A_8
L3017
IC,ARD_BGA,R1P0

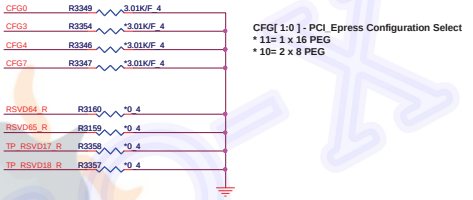

06
Max 22A
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
Please note that +VCC_GFX_CORE should be 1.05V in Arrandale
+VGACORE_IGPU
U3018G
GRAPHICS
POWER
DDR3 - 1.5V RAILS
GRAPHICS VIDs
SENSE LINES
PEG & DMI
IC,ARD_BGA,R1P0
3A
2.6A
for S3 power reduction
+1.5VSUS
+1.05V_VTT
+1.5V_CPU
+VCCTTG
VCAP0
VCAP1
VCAP2
40mile routing
PROJECT : R18D
Quanta Computer Inc.
PROCESSER 4/7(POWER2)
Tuesday, February 15, 2011
Electro-X



PROJECT : R18D
Quanta Computer

Size	Document Number	
Custom	PROCESSER 5/7(POWER3	
Date: Tuesday, February 15, 2011	Sheet	7





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

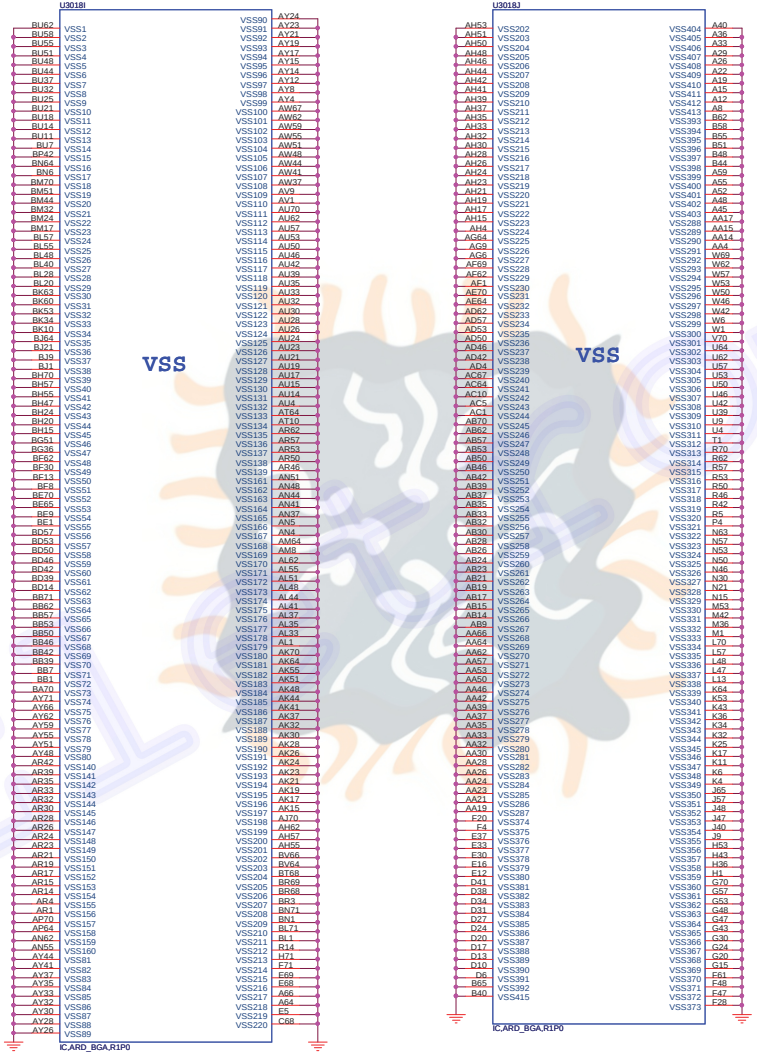
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 6/7(CFG)	
Date: Friday, January 14, 2011	Sheet 8	

ARRANDALE PROCESSOR (GND)

09



PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 7/7(GND)
Date: Thursday, January 13, 2011	Sheet: 9

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (HDA,JTAG,SATA)

IBEX PEAK-M (LVDS,DDI)

HDD0 (SATA3 6.0Gb/s)

MV add for connect EC to PCH (GPIO33_E)

must add test point.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

For ES1 ONLY.NI for ES2

For ES1 ONLY.NI for ES2

UMA HDMI signals

10/25 PV modify

10/25 PV modify

Part
Part Number
Part Description

For AUDIO

For MDC

RTC

1mA

8/25 SI for M/E.

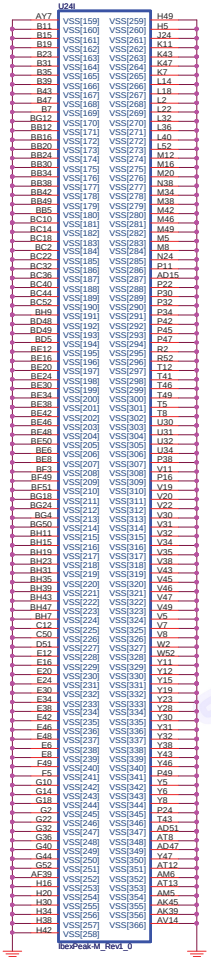
4M byte SPI ROM

Vender
Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

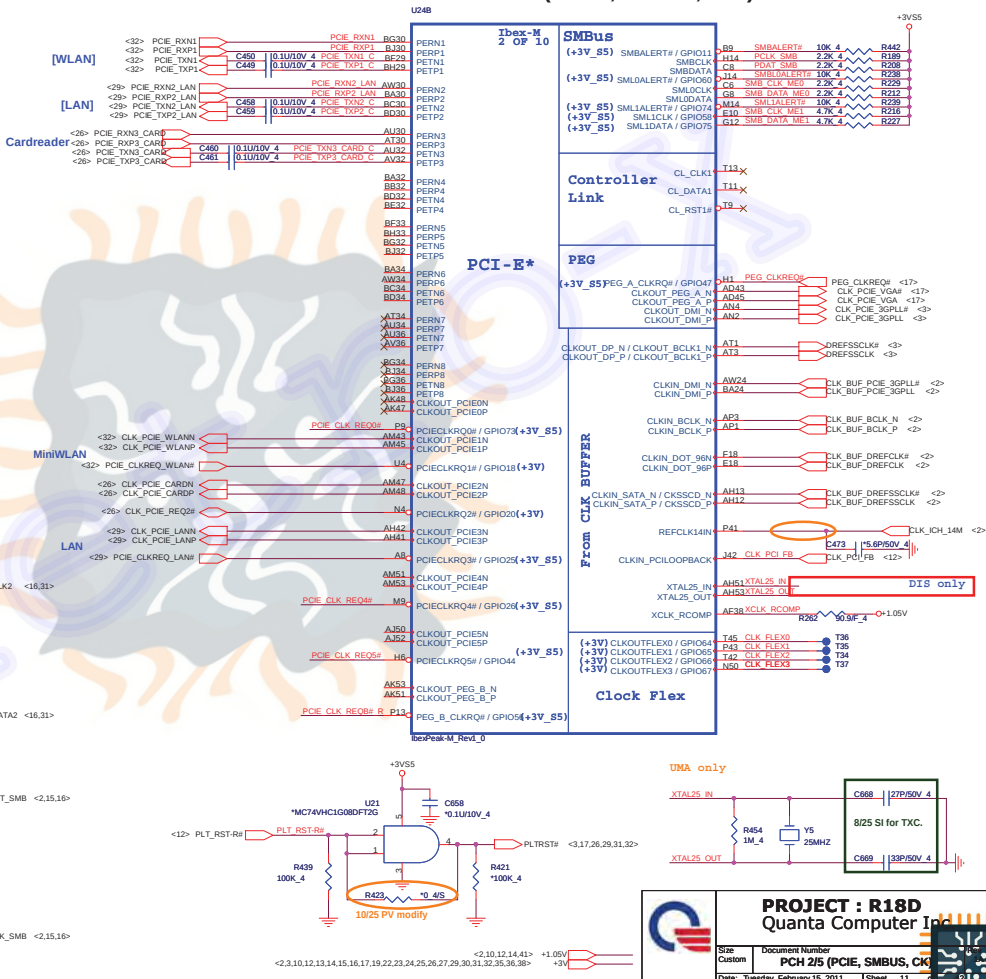
PROJECT : R18D
Quanta Computer Inc

Size: Custom | Document Number: PCH 1/5 (SATA,HDA,LPC) | Rev: 1A
Date: Tuesday, February 15, 2011 | Sheet 10 of 42

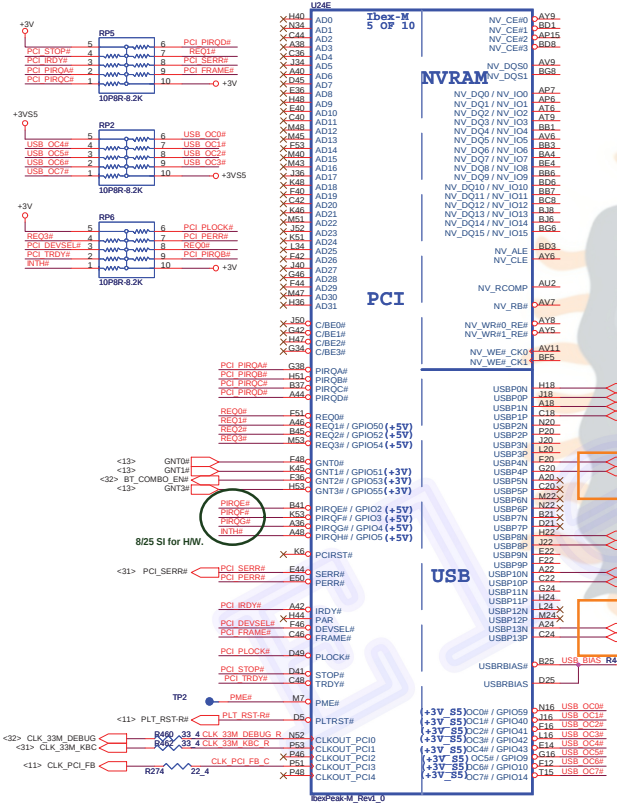
IBEX PEAK-M (GND)



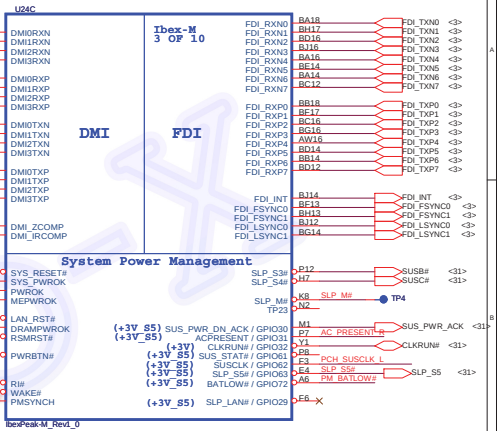
IBEX PEAK-M (PCI-E,SMBUS,CLK)

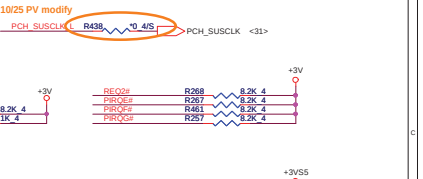


IBEX PEAK-M (PCI,USB,NVRAM)



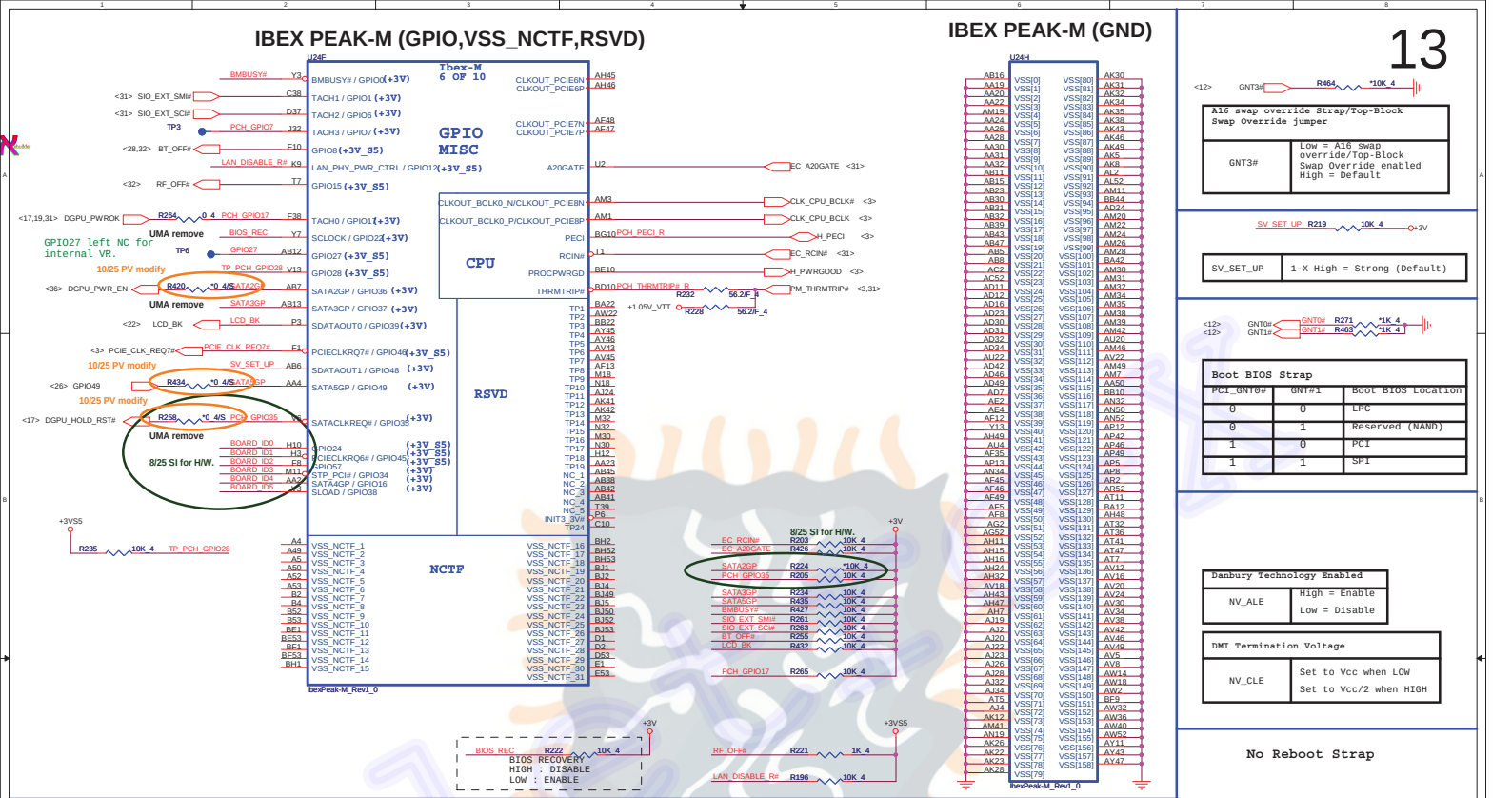
IBEX PEAK-M (DMI,FDI,GPIO)





SI Modify
Change Port2 to Port4
Change Port4 to Port12
change Port5 to Port13

<2,10,11,13,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38> +1.05V
<2,3,10,11,13,14,17,28,33,34,36,38,40> +3V
<3,10,11,13,14,17,28,33,34,36,38,40> +3VS5


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)
IBEX PEAK-M (GND)
13
U24F
Ibex-M
6 OF 10
GPIO MISC
CPU
RSVD
NCTF
BMBUSY# Y3
SIO_EXT_SMI# C38
SIO_EXT_SCI# D37
PCH_GPIO7 J32
BT_OFF# F10
LAN_DISABLE_R# K9
RF_OFF# T7
DGPU_PWROK R264 0_4 PCH_GPIO17 F38
UMA remove
BIOS_REC Y7
GPIO27 AB12
10/25 PV modify
TP_PCH_GPIO28 V13
DGPU_PWR_EN R420 *0_4/S ATA2GP AB7
UMA remove
SATA3GP AB13
LCD_BK P3
PCIE_CLK_REQ7# F1
10/25 PV modify
SV_SET_UP AB6
GPIO49 R434 *0_4/S ATA4GP AA4
10/25 PV modify
DGPU_HOLD_RST# R258 *0_4/S PCH_GPIO35 F5
UMA remove
8/25 SI for H/W.
BOARD_ID0 H10
BOARD_ID1 H3
BOARD_ID2 F8
BOARD_ID3 M11
BOARD_ID4 AA2
BOARD_ID5 F2
GPIO24 (+3V_S5)
PCIECLKRQ6# / GPIO45 (+3V_S5)
GPIO67 (+3V)
STP_PCI# / GPIO34 (+3V)
SATA4GP / GPIO16 (+3V)
SLOAD / GPIO38 (+3V)
SATACLKREQ# / GPIO33 (+3V)
CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2
CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3
CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1
PECI BG10
RCIN# T1
PROCPWRGD BE10
THRMTRIP# BD10
PCH_PECI_R
PCH_THRMTRIP#_R R232 56.2/F_4
+1.05V_VTT R228 56.2/F_4
EC_A20GATE <31>
CLK_CPU_BCLK# <3>
CLK_CPU_BCLK <3>
H_PECI <3>
EC_RCIN# <31>
H_PWRGOOD <3>
PM_THRMTRIP# <3,31>
TP1 BA22
TP2 AW22
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41
NC_5 T39
INIT3_3V# P6
TP24 C10
VSS_NCTF_1 A4
VSS_NCTF_2 A49
VSS_NCTF_3 A5
VSS_NCTF_4 A50
VSS_NCTF_5 A52
VSS_NCTF_6 A53
VSS_NCTF_7 B2
VSS_NCTF_8 B4
VSS_NCTF_9 B52
VSS_NCTF_10 B53
VSS_NCTF_11 BE1
VSS_NCTF_12 BE53
VSS_NCTF_13 BF1
VSS_NCTF_14 BF53
VSS_NCTF_15 BH1
VSS_NCTF_16 BH2
VSS_NCTF_17 BH52
VSS_NCTF_18 BH53
VSS_NCTF_19 BJ1
VSS_NCTF_20 BJ2
VSS_NCTF_21 BJ4
VSS_NCTF_22 BJ49
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ50
VSS_NCTF_25 BJ52
VSS_NCTF_26 BJ53
VSS_NCTF_27 D1
VSS_NCTF_28 D2
VSS_NCTF_29 D53
VSS_NCTF_30 E1
VSS_NCTF_31 E53
IbexPeak-M_Rev1_0
U24H
VSS[0] AB16
VSS[1] AA19
VSS[2] AA20
VSS[3] AA22
VSS[4] AM19
VSS[5] AA24
VSS[6] AA26
VSS[7] AA28
VSS[8] AA30
VSS[9] AA31
VSS[10] AA32
VSS[11] AB11
VSS[12] AB15
VSS[13] AB23
VSS[14] AB30
VSS[15] AB31
VSS[16] AB32
VSS[17] AB39
VSS[18] AB43
VSS[19] AB47
VSS[20] AB5
VSS[21] AB8
VSS[22] AC2
VSS[23] AC52
VSS[24] AD11
VSS[25] AD12
VSS[26] AD16
VSS[27] AD23
VSS[28] AD30
VSS[29] AD31
VSS[30] AD32
VSS[31] AD34
VSS[32] AU22
VSS[33] AD42
VSS[34] AD46
VSS[35] AD48
VSS[36] AD7
VSS[37] AE2
VSS[38] AE52
VSS[39] AF12
VSS[40] Y13
VSS[41] AH49
VSS[42] AU4
VSS[43] AF35
VSS[44] AP13
VSS[45] AN34
VSS[46] AF45
VSS[47] AF46
VSS[48] AF49
VSS[49] AF5
VSS[50] AF8
VSS[51] AG2
VSS[52] AG52
VSS[53] AH11
VSS[54] AH15
VSS[55] AH16
VSS[56] AH24
VSS[57] AH32
VSS[58] AH43
VSS[59] AH47
VSS[60] AH7
VSS[61] AJ19
VSS[62] A12
VSS[63] AJ20
VSS[64] AJ22
VSS[65] AJ23
VSS[66] AJ26
VSS[67] AJ28
VSS[68] AJ32
VSS[69] AJ34
VSS[70] AT5
VSS[71] AJ4
VSS[72] AK12
VSS[73] AM41
VSS[74] AN19
VSS[75] AN26
VSS[76] AK22
VSS[77] AK23
VSS[78] AK28
VSS[79]
VSS[80] AK30
VSS[81] AK31
VSS[82] AK32
VSS[83] AK34
VSS[84] AK35
VSS[85] AK38
VSS[86] AK43
VSS[87] AK46
VSS[88] AK49
VSS[89] AK5
VSS[90] AK8
VSS[91] AL2
VSS[92] AL52
VSS[93] AM11
VSS[94] BB44
VSS[95] AD24
VSS[96] AM20
VSS[97] AM22
VSS[98] AM24
VSS[99] AM26
VSS[100] AM28
VSS[101] BA42
VSS[102] AM30
VSS[103] AM31
VSS[104] AM32
VSS[105] AM34
VSS[106] AM35
VSS[107] AM38
VSS[108] AM39
VSS[109] AM42
VSS[110] AU20
VSS[111] AM46
VSS[112] AV22
VSS[113] AM49
VSS[114] AM7
VSS[115] AN50
VSS[116] BB10
VSS[117] AN32
VSS[118] AN50
VSS[119] AN52
VSS[120] AP12
VSS[121] AP42
VSS[122] AP46
VSS[123] AP49
VSS[124] AP5
VSS[125] AP8
VSS[126] AR2
VSS[127] AR52
VSS[128] AT11
VSS[129] BA12
VSS[130] AH48
VSS[131] AT32
VSS[132] AT36
VSS[133] AT41
VSS[134] AT47
VSS[135] AT7
VSS[136] AV12
VSS[137] AV16
VSS[138] AV20
VSS[139] AV24
VSS[140] AV30
VSS[141] AV34
VSS[142] AV38
VSS[143] AV42
VSS[144] AV46
VSS[145] AV49
VSS[146] AV5
VSS[147] AV8
VSS[148] AW14
VSS[149] AW18
VSS[150] AW2
VSS[151] BF9
VSS[152] AW32
VSS[153] AW36
VSS[154] AW40
VSS[155] AW52
VSS[156] AY11
VSS[157] AY43
VSS[158] AY47
IbexPeak-M_Rev1_0
GNT3# R464 *10K_4
A16 swap override Strap/Top-Block Swap Override jumper
GNT3# | Low = A16 swap override/Top-Block Swap Override enabled; High = Default
SV_SET_UP R219 10K_4 +3V
SV_SET_UP | 1-X High = Strong (Default)
GNT0# R271 *1K_4
GNT1# R463 *1K_4
Boot BIOS Strap
PCI_GNT0# | GNT#1 | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
Danbury Technology Enabled
NV_ALE | High = Enable; Low = Disable
DMI Termination Voltage
NV_CLE | Set to Vcc when LOW; Set to Vcc/2 when HIGH
No Reboot Strap
ACZ_SPKR R430 *1K_4 +3V
GPIO33_E R253 *100K_4
+3VS5
R235 10K_4 TP_PCH_GPIO28
8/25 SI for H/W.
EC_RCIN# R203 10K_4
EC_A20GATE R426 10K_4
SATA2GP R224 *10K_4
PCH_GPIO35 R205 10K_4
SATA3GP R234 10K_4
SATA5GP R435 10K_4
BMBUSY# R427 10K_4
SIO_EXT_SMI# R261 10K_4
SIO_EXT_SCI# R263 10K_4
BT_OFF# R255 10K_4
LCD_BK R432 10K_4
PCH_GPIO17 R265 10K_4
BIOS_REC R222 10K_4
BIOS RECOVERY
HIGH : DISABLE
LOW : ENABLE
RF_OFF# R221 1K_4
LAN_DISABLE_R# R196 10K_4
RU0 RD0
RU1 RD1
RU2 RD2
RU3 RD3
RU4 RD4
RU5 RD5
R207 R206 R419 R437 R214 R213 R202 R218 R424 R204 R428 R431
BOARD_ID0 BOARD_ID1 BOARD_ID2 BOARD_ID3 BOARD_ID4 BOARD_ID5
10K_4 *10K_4
8/25 SI for H/W.
<2,3,10,11,12,14,15,16,17,19,22,23,24,25,26,27,29,30,31,32,35,36,38>
<3,5,6,14,31,34,35,36,40> +1.05V_VTT
<5,14,34> +1.8V
<3,10,11,12,14,17,28,33,34,36,38,40> +3V
+3VSS
R12 MB P/N | ID0 | ID1 | ID2 | ID3 | ID4 | ID5
UMA
31R12MB0000 (PIM) 0 0 0 0 0 0
31R12MB0010 (PDT) 0 0 0 0 0 0
Seymour XT
Hynix 512
31R12MB0020 (PIM) 1 0 0 0 0 0
31R12MB0030 (PDT) 1 0 0 0 0 0
Samsung 512
31R12MB0040 (PIM) 1 0 0 0 0 0
31R12MB0050 (PDT) 1 0 0 0 0 0
Hynix 1G
31R12MB0060 (PIM) 1 0 0 0 0 0
31R12MB0070 (PDT) 1 0 0 0 0 0
Samsung 1G
31R12MB0080 (PIM) 1 0 0 0 0 0
31R12MB0090 (PDT) 1 0 0 0 0 0
Board ID | ID0 GPIO24 | ID1 GPIO45 | ID2 GPIO57 | ID3 GPIO34 | ID4 GPIO35 | ID5 GPIO38
UMA/DIS | 0=UMA 1=Dis.
1.1/1.0 | 1=1.1 0=1.0
Reserve | 0=No 1=Yes
Reserve | 0=No 1=Yes
Reserve | 0=No 1=Yes
Reserve | 0=No 1=Yes
BOARD_ID1設成HIGH代表Rockey 1.1
Eletro-X
PROJECT : R18D
Quanta Computer Inc.
Size Custom
Document Number PCH 4/5 (GPIO & Strap)
Rev 1A
Date: Tuesday, February 15, 2011
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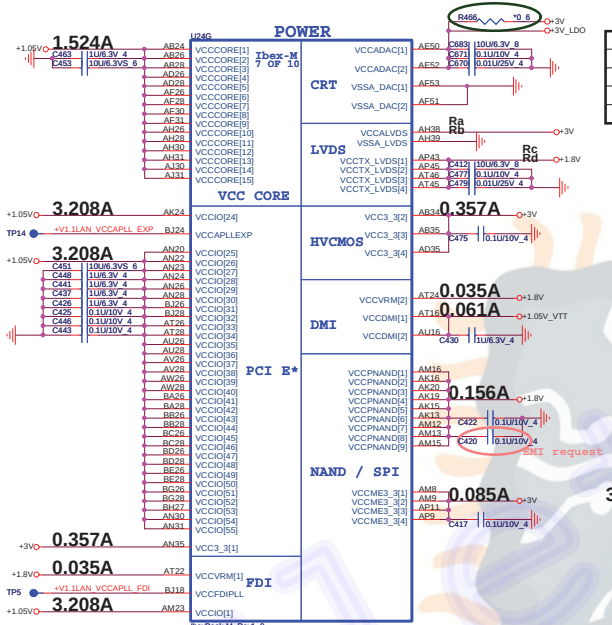
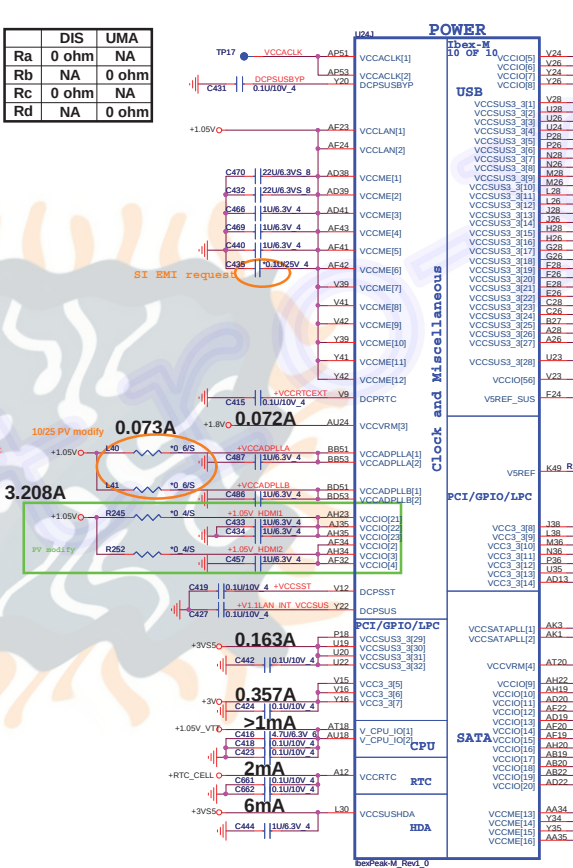
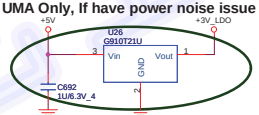
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

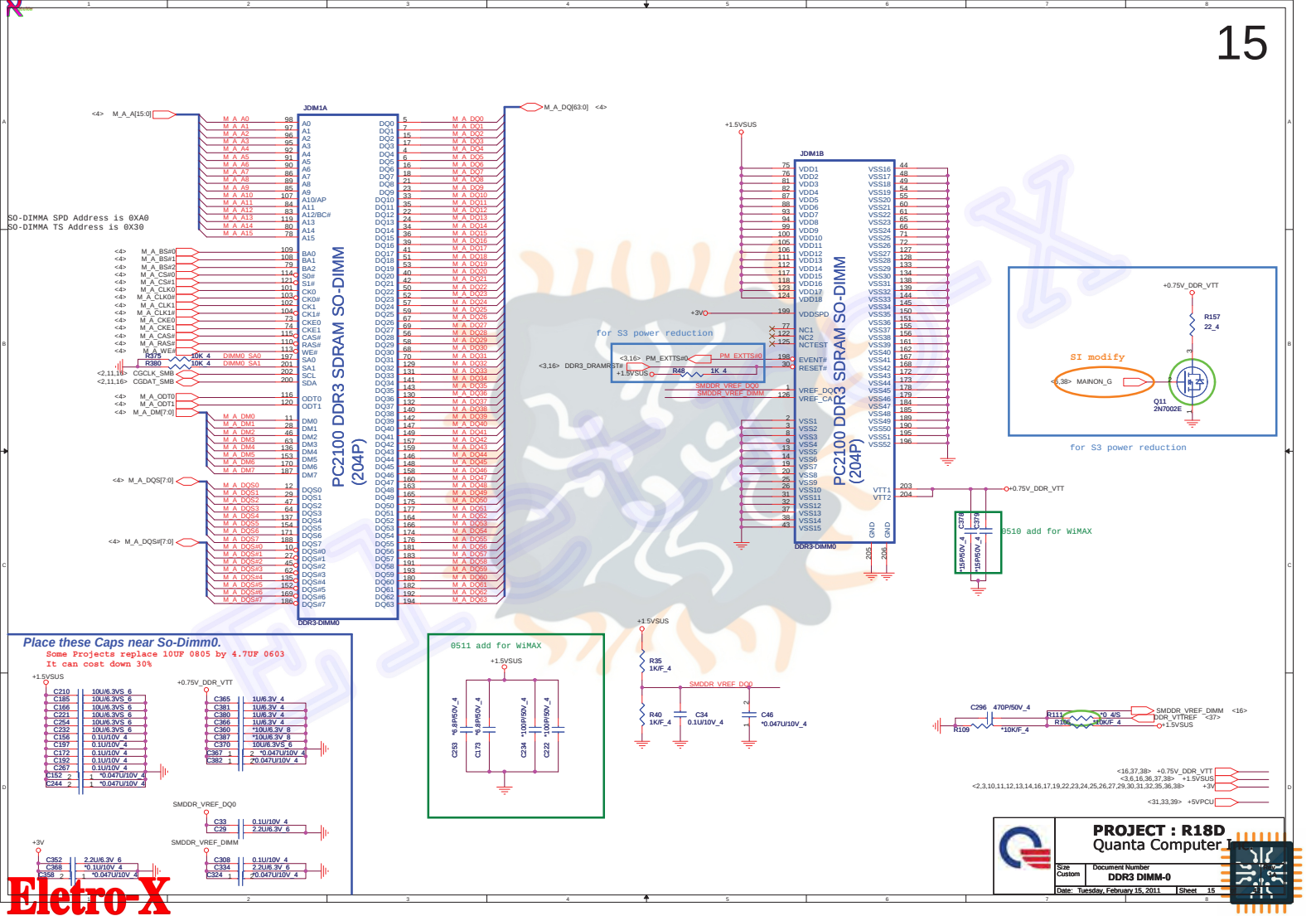


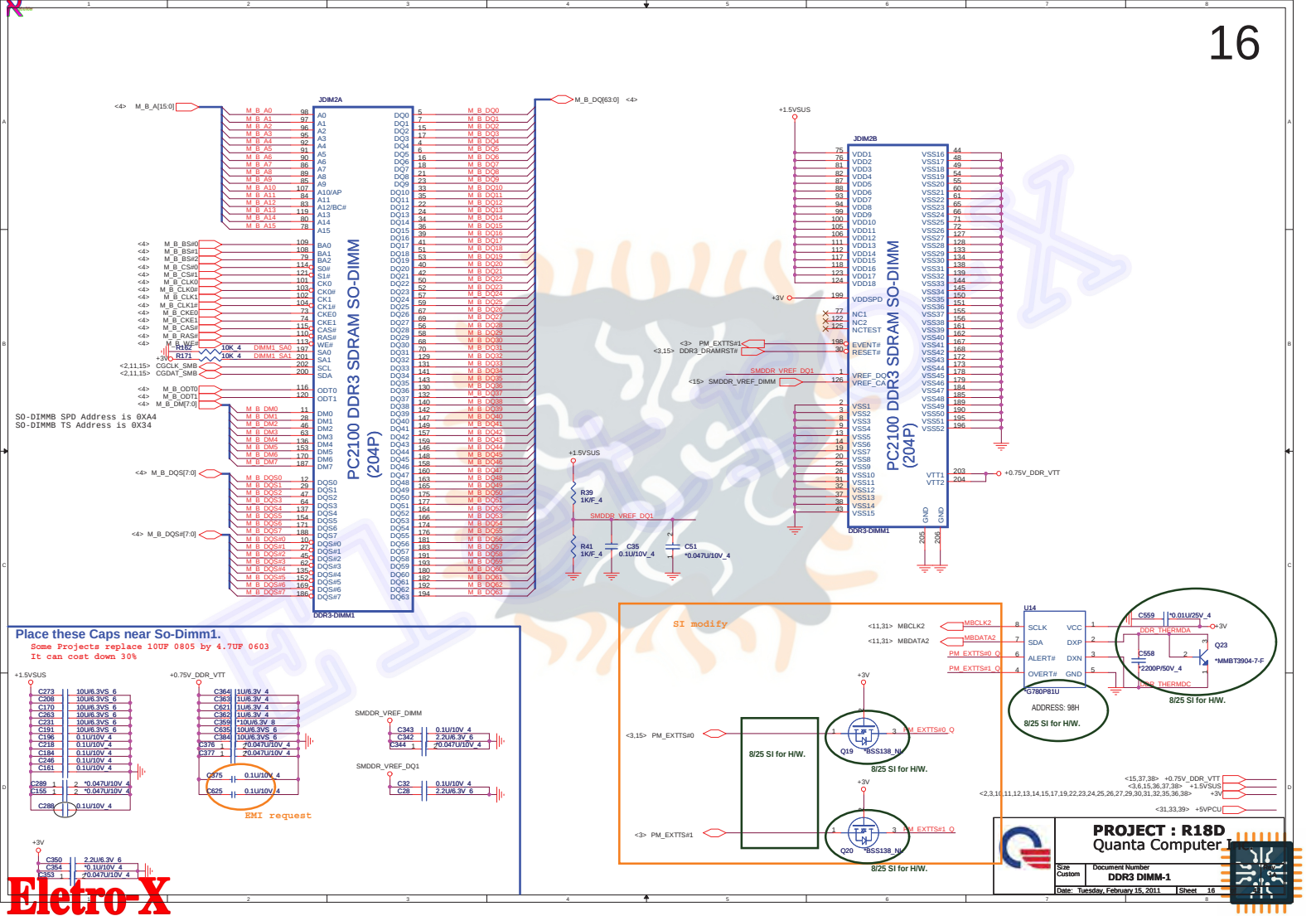


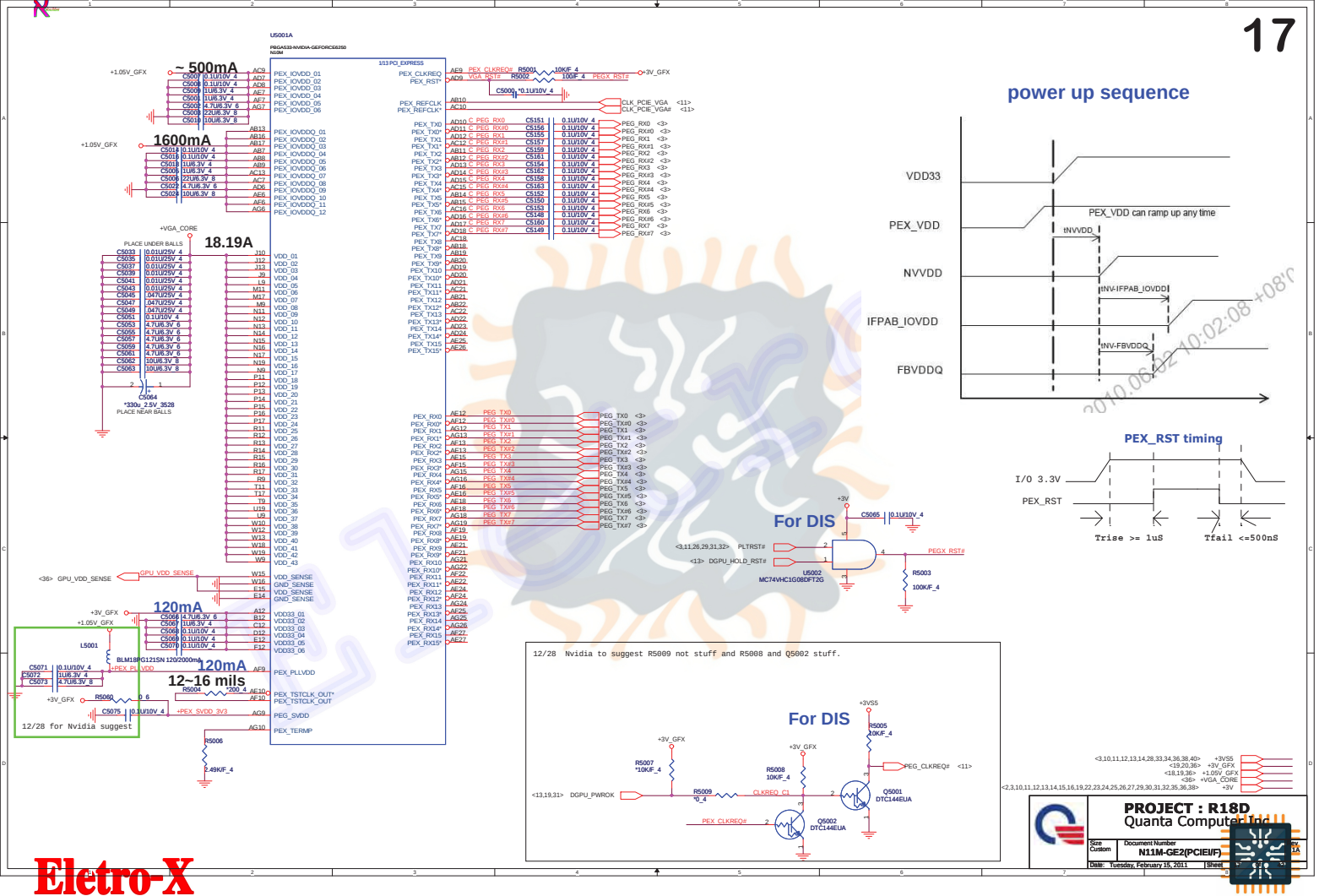
UMA Only, If have power noise issue then stuff it.



8/25 SI modify
Install LDO when UMA


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
for S3 power reduction
SI modify
Q11
2N7002E
0510 add for WiMAX
0511 add for WiMAX
Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
SMDDR_VREF_DQ0
SMDDR_VREF_DIMM
PROJECT : R18D
Quanta Computer Inc.
DDR3 DIMM-0
Tuesday, February 15, 2011
Sheet 15


JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
EMI request
SI modify
8/25 SI for H/W.
ADDRESS: 98H
PROJECT : R18D
Quanta Computer I
DDR3 DIMM-1
Tuesday, February 15, 2011


~ 500mA
1600mA
18.19A
120mA
120mA
12~16 mils
power up sequence
VDD33
PEX_VDD
NVVDD
IFPAB_IOVDD
FBVDDQ
PEX_VDD can ramp up any time
tNVVDD
tNV-IFPAB_IOVDD
tNV-FBVDDQ
PEX_RST timing
I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS
For DIS
For DIS
12/28 for Nvidia suggest
12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.
PROJECT : R18D
Quanta Computer Inc.
N11M-GE2(PCIEI/F)
Tuesday, February 15, 2011

2.16A

U5001B
PBGA533-NVIDIA-GEFORCE6250
N10M

+1.5V_GFX

C5076 .047U/25V_4
C5077 .047U/25V_4
C5083 .047U/25V_4
C5078 0.01U/25V_4
C5079 0.01U/25V_4
C5080 0.01U/25V_4
C5082 4.7U/6.3V_6
C5081 4.7U/6.3V_6

2/13 FRAME_BUFFER

FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 E14
FBVDDQ_09 E15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 E19
FBVDDQ_13 F22
FBVDDQ_14 H26
FBVDDQ_15 J15
FBVDDQ_16 J16
FBVDDQ_17 J18
FBVDDQ_18 J19
FBVDDQ_19 L19
FBVDDQ_20 L23
FBVDDQ_21 L26
FBVDDQ_22 M19
FBVDDQ_23 N22
FBVDDQ_24 U22
FBVDDQ_25 Y22
FBVDDQ_26

FBA_D0 D22 VMA_DQ0
FBA_D1 E24 VMA_DQ1
FBA_D2 E22 VMA_DQ2
FBA_D3 D24 VMA_DQ3
FBA_D4 D26 VMA_DQ4
FBA_D5 D27 VMA_DQ5
FBA_D6 C27 VMA_DQ6
FBA_D7 B27 VMA_DQ7
FBA_D8 A21 VMA_DQ8
FBA_D9 B21 VMA_DQ9
FBA_D10 C21 VMA_DQ10
FBA_D11 C19 VMA_DQ11
FBA_D12 C18 VMA_DQ12
FBA_D13 D18 VMA_DQ13
FBA_D14 B18 VMA_DQ14
FBA_D15 C16 VMA_DQ15
FBA_D16 E21 VMA_DQ16
FBA_D17 F21 VMA_DQ17
FBA_D18 D20 VMA_DQ18
FBA_D19 F20 VMA_DQ19
FBA_D20 D17 VMA_DQ20
FBA_D21 F18 VMA_DQ21
FBA_D22 D16 VMA_DQ22
FBA_D23 E16 VMA_DQ23
FBA_D24 A22 VMA_DQ24
FBA_D25 C24 VMA_DQ25
FBA_D26 D21 VMA_DQ26
FBA_D27 B22 VMA_DQ27
FBA_D28 C22 VMA_DQ28
FBA_D29 A25 VMA_DQ29
FBA_D30 B25 VMA_DQ30
FBA_D31 A26 VMA_DQ31
FBA_D32 U24 VMA_DQ32
FBA_D33 V24 VMA_DQ33
FBA_D34 V23 VMA_DQ34
FBA_D35 R24 VMA_DQ35
FBA_D36 T23 VMA_DQ36
FBA_D37 R23 VMA_DQ37
FBA_D38 P24 VMA_DQ38
FBA_D39 P22 VMA_DQ39
FBA_D40 AC24 VMA_DQ40
FBA_D41 AB23 VMA_DQ41
FBA_D42 AB24 VMA_DQ42
FBA_D43 W24 VMA_DQ43
FBA_D44 AA22 VMA_DQ44
FBA_D45 W23 VMA_DQ45
FBA_D46 W22 VMA_DQ46
FBA_D47 V22 VMA_DQ47
FBA_D48 AA25 VMA_DQ48
FBA_D49 W27 VMA_DQ49
FBA_D50 W26 VMA_DQ50
FBA_D51 W25 VMA_DQ51
FBA_D52 AB25 VMA_DQ52
FBA_D53 AB26 VMA_DQ53
FBA_D54 AD26 VMA_DQ54
FBA_D55 AD27 VMA_DQ55
FBA_D56 V25 VMA_DQ56
FBA_D57 R25 VMA_DQ57
FBA_D58 V26 VMA_DQ58
FBA_D59 V27 VMA_DQ59
FBA_D60 R26 VMA_DQ60
FBA_D61 T25 VMA_DQ61
FBA_D62 N25 VMA_DQ62
FBA_D63 N26 VMA_DQ63

FBA_DQM0 C26 VMA_DM0
FBA_DQM1 B19 VMA_DM1
FBA_DQM2 D19 VMA_DM2
FBA_DQM3 D23 VMA_DM3
FBA_DQM4 T24 VMA_DM4
FBA_DQM5 AA23 VMA_DM5
FBA_DQM6 AB27 VMA_DM6
FBA_DQM7 T26 VMA_DM7

FBA_DQS_WP0 C25 VMA_WDQS0
FBA_DQS_WP1 A19 VMA_WDQS1
FBA_DQS_WP2 E19 VMA_WDQS2
FBA_DQS_WP3 A24 VMA_WDQS3
FBA_DQS_WP4 T22 VMA_WDQS4
FBA_DQS_WP5 AA24 VMA_WDQS5
FBA_DQS_WP6 AA26 VMA_WDQS6
FBA_DQS_WP7 T27 VMA_WDQS7

FBA_DQS_RN0 D25 VMA_RDQS0
FBA_DQS_RN1 A18 VMA_RDQS1
FBA_DQS_RN2 E18 VMA_RDQS2
FBA_DQS_RN3 B24 VMA_RDQS3
FBA_DQS_RN4 R22 VMA_RDQS4
FBA_DQS_RN5 Y24 VMA_RDQS5
FBA_DQS_RN6 AA27 VMA_RDQS6
FBA_DQS_RN7 R27 VMA_RDQS7

FB_VREF A16 +FB_VREF1 TP18

TP20 FBA_CMD1

<21> FBA_CMD0 G24
(FBA_CMD25)FBA_CMD0 F27
(FBA_CMD23)FBA_CMD1
FBA_CMD2 F25
<21> FBA_CMD2 E26
(FBA_CMD0)FBA_CMD3 G26
<21> FBA_CMD3 (FBA_CMD10)FBA_CMD4 G27
<21> FBA_CMD4 (FBA_CMD26)FBA_CMD5 G25
<21> FBA_CMD5 (FBA_CMD14)FBA_CMD6 J25
<21> FBA_CMD6 FBA_CMD7 J24
<21> FBA_CMD7 (FBA_CMD11)FBA_CMD8 H24
<21> FBA_CMD8 (FBA_CMD22)FBA_CMD9 H22
<21> FBA_CMD9 (FBA_CMD20)FBA_CMD10 J26
<21> FBA_CMD10 (FBA_CMD24)FBA_CMD11 G22
<21> FBA_CMD11 (FBA_CMD18)FBA_CMD12 G23
<21> FBA_CMD12 (FBA_CMD9)FBA_CMD13 J22
<21> FBA_CMD13 (FBA_CMD29)FBA_CMD14 J27
<21> FBA_CMD14 (FBA_CMD8)FBA_CMD15 M24
<21> FBA_CMD15 (FBA_CMD27)FBA_CMD16 L24
<21> FBA_CMD16 (FBA_CMD15)FBA_CMD17 J23
<21> FBA_CMD17 (FBA_CMD11)FBA_CMD18 K23
<21> FBA_CMD18 (FBA_CMD19)FBA_CMD19 K22
<21> FBA_CMD19 (FBA_CMD28)FBA_CMD20 M23
<21> FBA_CMD20 (FBA_CMD3)FBA_CMD21 K24
<21> FBA_CMD21 (FBA_CMD17)FBA_CMD22 M27
<21> FBA_CMD22 (FBA_CMD5)FBA_CMD23 N27
<21> FBA_CMD23 (FBA_CMD4)FBA_CMD24 M26
<21> FBA_CMD24 (FBA_CMD21)FBA_CMD25 K26
<21> FBA_CMD25 (FBA_CMD6)FBA_CMD26 K27
<21> FBA_CMD26 (FBA_CMD13)FBA_CMD27 K25
<21> FBA_CMD27 (FBA_CMD19)FBA_CMD28 M25
<21> FBA_CMD28 (FBA_CMD12)FBA_CMD29 L22
<21> FBA_CMD29 FBA_CMD30

TP19 FBA_CMD17

<21> FBA_CMD30

<21> VMA_CLK0 VMA_CLK0 F24 FBA_CLK0
<21> VMA_CLK0# VMA_CLK0# F23 FBA_CLK0*
<21> VMA_CLK1 VMA_CLK1 N24 FBA_CLK1
<21> VMA_CLK1# VMA_CLK1# N23 FBA_CLK1*

+1.5V_GFX R5016 40.2/F_4 FB_CAL_PD_VDDQ B15 FB_CAL_PD_VDDQ
R5017 40.2/F_4 FB_CAL_PU_GND A15 FB_CAL_PU_GND
R5018 60.4/F_4 FB_CAL_TERM_GND B16 FB_CAL_TERM_GND
+1.5V_GFX R5019 10K/F_4 FBA_DEBUG M22 (FBA_DEBUG)FBA_DEBUG0

For debug only
10mA

+1.05V_GFX 15mils width 200mA
L5003 PBY160808T-300Y-N +FB_PLLAVDD F19 FB_PLLAVDD
30 ohm/100MHz ESR=0.03ohm
C5085 1U/6.3V_4
C5086 0.1U/10V_4
C5087 10U/6.3V_8
T19 FB_DLLAVDD
AC19 FB_PLLAVDD

12/28 Nvidia recommend

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

<21> VMA_DQ[63..0]
<21> VMA_DM[7..0]
<21> VMA_WDQ[7..0]
<21> VMA_RDQS[7..0]

FBA_CMD0 R5012 10K/F_4
FBA_CMD3 R5010 10K/F_4
FBA_CMD16 R5013 10K/F_4
FBA_CMD19 R5014 10K/F_4
FBA_CMD20 R5015 10K/F_4

US001I
N10M
PBGA533-NVIDIA-GEFORCE6250
13/13 GND_NC

AC11 AC14 AC17 AC2 AC20 AC23 AC26 AC5 AC8 AF11 AF14 AF17 AF2 AF20 AF23 AF26 AF5 AF8 B11 B14 B17 B2 B20 B23 B26 B5 B8 E11 E17 E2 E20 E23 E26 E5 E8 H2 H5 J11 J14 J17 K19 K9 L11 L12 L13 L14 L15 L16 L17 L2 L5 M12 M13 M14 M15 M18 P19 P2 P23 P26 P5 P9 T12 T13 T14 T15 T16 U11 U12 U13 U14 U15 U16 U17 U2 U23 U26 U5 V19 V9 W11 W14 W17 Y2 Y23 Y26 Y5

GND_01 GND_02 GND_03 GND_04 GND_05 GND_06 GND_07 GND_08 GND_09 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88

NC_01 C15
NC_02 D15
(NC_03)PGOOD R5013 10K/F_4

nVIDIA comment 8/18

<17,19,36> +1.05V_GFX
<19,21,36> +1.5V_GFX

PROJECT : R18D
Quanta Computer Inc.
Size Custom
Document Number N11M-GE2(MEMORY)
Date: Tuesday, February 15, 2011
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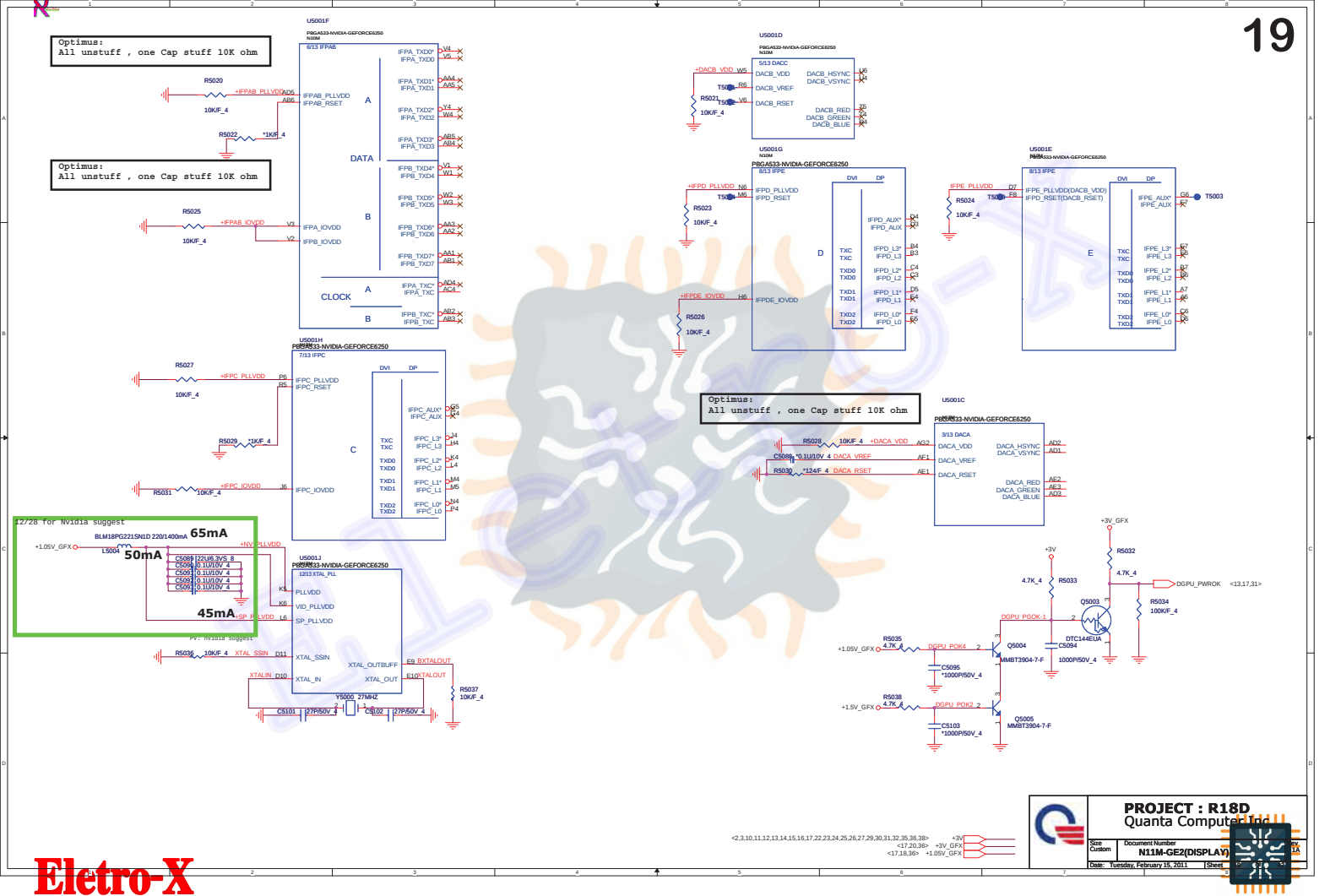
Eletro-X


Optimus:
All unstuff , one Cap stuff 10K ohm
Optimus:
All unstuff , one Cap stuff 10K ohm
Optimus:
All unstuff , one Cap stuff 10K ohm
U5001F
P8G4533-NVIDIA-GEFORCE6250
N10M
6/13 IFPAB
IFPA_TXD0*
IFPA_TXD0
IFPA_TXD1*
IFPA_TXD1
IFPA_TXD2*
IFPA_TXD2
IFPA_TXD3*
IFPA_TXD3
IFPB_TXD4*
IFPB_TXD4
IFPB_TXD5*
IFPB_TXD5
IFPB_TXD6*
IFPB_TXD6
IFPB_TXD7*
IFPB_TXD7
IFPA_TXC*
IFPA_TXC
IFPB_TXC*
IFPB_TXC
DATA
CLOCK
A
B
R5020
10K/F_4
+IFPAB_PLLVDD
IFPAB_PLLVDD
IFPAB_RSET
R5022
*1K/F_4
R5025
10K/F_4
+IFPAB_IOVDD
IFPA_IOVDD
IFPB_IOVDD
U5001H
P8G4533-NVIDIA-GEFORCE6250
7/13 IFPC
DVI
DP
IFPC_PLLVDD
IFPC_RSET
IFPC_AUX*
IFPC_AUX
TXC
TXC
TXD0
TXD0
TXD1
TXD1
TXD2
TXD2
IFPC_L3*
IFPC_L3
IFPC_L2*
IFPC_L2
IFPC_L1*
IFPC_L1
IFPC_L0*
IFPC_L0
C
R5027
10K/F_4
+IFPC_PLLVDD
R5029
*1K/F_4
R5031
10K/F_4
+IFPC_IOVDD
U5001J
P8G4533-NVIDIA-GEFORCE6250
12/13 XTAL PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
XTALIN
XTALOUT
Y5000 27MHZ
C5101 27P/50V_4
C5102 27P/50V_4
R5036 10K/F_4
R5037 10K/F_4
12/28 for Nvidia suggest
65mA
50mA
45mA
+1.05V_GFX
L5004
BLM18PG221SN1D 220/1400mA
+NV_PLLVDD
C5088 22U/6.3V/5_8
C5089 0.1U/10V_4
C5091 0.1U/10V_4
C5092 0.1U/10V_4
C5093 0.1U/10V_4
+SP_PLLVDD
FY: Nvidia suggest
U5001D
P8G4533-NVIDIA-GEFORCE6250
N10M
5/13 DACC
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
R5021
10K/F_4
+DACB_VDD
U5001G
N10M
P8G4533-NVIDIA-GEFORCE6250
8/13 IFPE
IFPD_PLLVDD
IFPD_RSET
IFPD_AUX*
IFPD_AUX
IFPD_L3*
IFPD_L3
IFPD_L2*
IFPD_L2
IFPD_L1*
IFPD_L1
IFPD_L0*
IFPD_L0
IFPDE_IOVDD
D
R5023
10K/F_4
+IFPD_PLLVDD
R5026
10K/F_4
+IFPDE_IOVDD
U5001E
P8G4533-NVIDIA-GEFORCE6250
8/13 IFPE
IFPE_PLLVDD(DACB_VDD)
IFPD_RSET(DACB_RSET)
IFPE_AUX*
IFPE_AUX
IFPE_L3*
IFPE_L3
IFPE_L2*
IFPE_L2
IFPE_L1*
IFPE_L1
IFPE_L0*
IFPE_L0
E
R5024
10K/F_4
IFPE_PLLVDD
T5003
U5001C
P8G4533-NVIDIA-GEFORCE6250
3/13 DACA
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
R5028
10K/F_4
+DACA_VDD
C5086 *0.1U/10V_4
DACA_VREF
R5030
*124/F_4
DACA_RSET
+3V_GFX
+3V
R5032
4.7K_4
R5033
4.7K_4
DGPU_PWROK
<13,17,31>
R5034
100K/F_4
Q5003
DTC144EUA
C5094
1000P/50V_4
DGPU_PGOK
DGPU_POK4
DGPU_POK2
R5035
4.7K_4
+1.05V_GFX
Q5004
MMBT3904-7-F
C5095
*1000P/50V_4
R5038
4.7K_4
+1.5V_GFX
Q5005
MMBT3904-7-F
C5103
*1000P/50V_4
<2,3,10,11,12,13,14,15,16,17,22,23,24,25,26,27,29,30,31,32,35,36,38>
+3V
<17,20,36>
+3V_GFX
<17,18,36>
+1.05V_GFX
PROJECT : R18D
Quanta Computer Inc.
Size
Custom
Document Number
N11M-GE2(DISPLAY)
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N12P-GV -> 0x17F
N12M-GE -> 0xA7A 1010 ->PU15K

4.99K/F_ 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_ 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_ 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_ 4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_ 4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

ROM_SI -> based on VRAM.
ROM_SO -> PU 10K
ROM_SCLK -> PU 5K
STRAP0 -> PU 45K
STRAP1 -> PD 35K
STRAP2 -> PD 5K
STRAP3 -> PD 5K
STRAP 4 -> PD 10K.

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

PCI_DEVID[4]/SUBVENDOR

(Ra)

Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

12/28 for Nvidia suggest

12/28 for Nvidia suggest

N12P-GV default boot up voltage should be set to 0.85V. Therefore, please add 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

12/29 Nvidia suggest for AC/Batt# function

12/29 Nvidia suggest

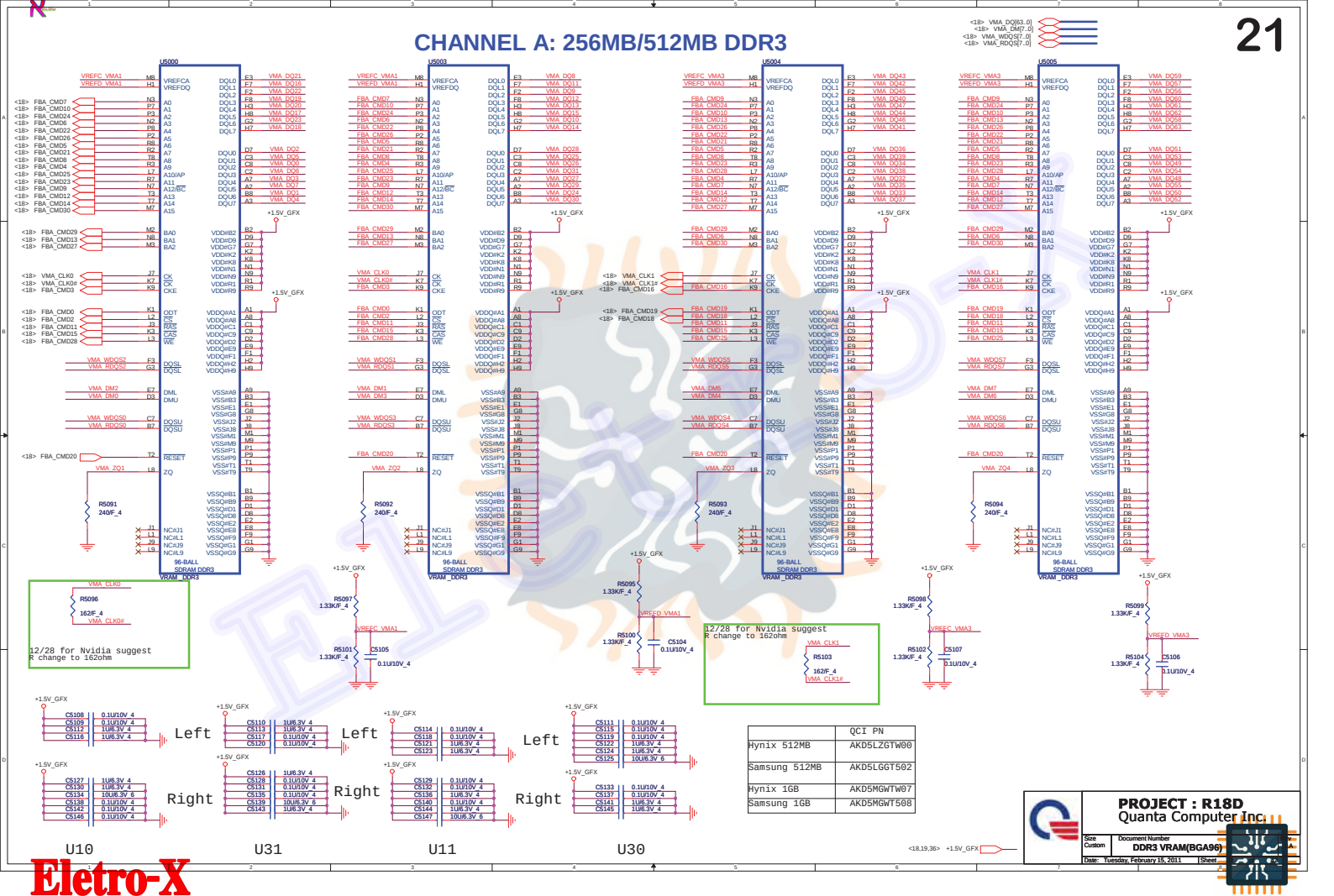
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

PROJECT : R18D
Quanta Computer Inc.

Size: Custom | Document Number: N12P-GV(GPIO/STRAPS)
Date: Tuesday, February 15, 2011 | Sheet 20

CHANNEL A: 256MB/512MB DDR3



	QCI PN
Hynix 512MB	AKD5LZGTW00
Samsung 512MB	AKD5LGGT502
Hynix 1GB	AKD5MGWTW07
Samsung 1GB	AKD5MGWT508

PROJECT : R18D
Quanta Computer Inc.
Size: Custom | Document Number: DDR3 VRAM(BGA96) | Rev: A
Date: Tuesday, February 15, 2011 | Sheet

Eletro-X

LID Switch

10/25 PV modify

<31> EMU_LID — R54 *0 4/S — PN_BLON — D3 RB500V-40 — BLON_CON — C101 22P/50V_4 — R69 100K_4

R50 47K_4 — +3VPCU

LVDS_BLON — R49 1K_4 — D2 *RB500V-40 — LID_EC# <30,31>

Close to EC

<13> LCD_BK — Q2 *DTC144EUA

EMI request — C65 100P/50V_4

DISP_ON — R57 100K_4

LVDS_BLON — R45 100K_4

100mA

+VIN_BLIGHT

+VIN — L8 FBM2125 HM330-T/4A_8 — +VIN_BLIGHT

C78 0.1U/25V_4

C77 0.01U/25V_4

EMI & RF

+VIN

C73 *4.7U/25V_8

C96 0.1U/25V_4

8/25 SI for H/W.

Coupling CAP.

+VIN

C751 *0.1U/25V_4
C752 *0.1U/25V_4
C753 *0.1U/25V_4
C754 *0.1U/25V_4
C755 *0.1U/25V_4
C756 *0.1U/25V_4
C757 *0.1U/25V_4
C758 *0.1U/25V_4
C759 *0.1U/25V_4
C760 *0.1U/25V_4

+VIN

C761 *0.1U/25V_4
C762 *0.1U/25V_4
C763 *0.1U/25V_4
C764 *0.1U/25V_4
C765 *0.1U/25V_4
C766 *0.1U/25V_4
C767 *0.1U/25V_4
C768 *0.1U/25V_4
C769 *0.1U/25V_4
C770 *0.1U/25V_4

8/25 SI for H/W.

<10> TXLCLKOUT+ → TXLCLKOUT+
<10> TXLCLKOUT- → TXLCLKOUT-
<10> TXLOUT0+ → TXLOUT0+
<10> TXLOUT0- → TXLOUT0-
<10> TXLOUT1+ → TXLOUT1+
<10> TXLOUT1- → TXLOUT1-
<10> TXLOUT2+ → TXLOUT2+
<10> TXLOUT2- → TXLOUT2-

<10> TXUCLKOUT- → TXUCLKOUT-
<10> TXUCLKOUT+ → TXUCLKOUT+
<10> TXUOUT0+ → TXUOUT0+
<10> TXUOUT0- → TXUOUT0-
<10> TXUOUT1+ → TXUOUT1+
<10> TXUOUT1- → TXUOUT1-
<10> TXUOUT2+ → TXUOUT2+
<10> TXUOUT2- → TXUOUT2-

<10> EDIDCLK → EDIDCLK
<10> EDIDDATA → EDIDDATA

<10> LVDS_BLON → LVDS_BLON
<10> DISP_ON → DISP_ON
<10> DPST_PWM → DPST_PWM

10/25 PV modify

+3V — R43 *0 4/S — +3V_CAM

C48 *0.01U/25V_4

C45 *4.7U/6.3V_6

Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L4 location

USBP4- — R44 0_4 — USBP4- R

USBP4+ — R46 0_4 — USBP4+ R

change to +5VS5

+12VALW

+5VS5

14.5v

R65 100K_4

R24 330K_6

AO3404 ID current 5.8A

Q1 AO3404

LCDONG

Q3 2N7002E

C13 0.022U/25V_4

Q4 DTC144EUA

DISP_ON

+3V

+3VLCD

R72 22_8

LCDDISCHG

LCDON#

Q5 2N7002E

+3VLCD_CON

L4 HCB2012KF-600T30/3A_8

C14 *0.01U/25V_4

C12 0.1U/10V_4

1A

<10,30,31,33,39> +3VPCU
<2,3,10,11,12,13,14,15,16,17,19,23,24,25,26,27,29,30,31,32,35,36,38> +3V
<25,36,38,39> +12VALW
<33,34,35,36,37,38,39,40,41> +VIN

+3V — R25 2.2K_4 EDIDCLK — R26 2.2K_4 EDIDDATA

RF

C17 10P/50V_4 — C20 10P/50V_4

+3VLCD_CON

+3V — C18 1000P/50V_4

+3VLCD_CON

C190 0.47U/10V_4 — C180 0.47U/10V_4

EDIDCLK
EDIDDATA
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

10/26 PV modify

9/25 SI for H/W.

<27> DIGITAL_D1
<27> DIGITAL_CLK

EMI

R36 *0 4/S — DIGITAL_CLK_L

L6 SBK160808T-601Y-N/0.2A_6 — +3V_CAM

C40 *10P/50V_4 — C44 *10P/50V_4

<12> USBP4-
<12> USBP4+

L7 4 — USBP4- R — USBP4+ R

*WCM-2012-900T(400mA)

VADJ1

BLON_CON

+VIN_BLIGHT

8/25 SI for M/E.

CN2 GS12401-1011 DFHS40FS036 GS12401-1011-40P-R-NH-SMT

10/25 PV modify

DPST_PWM — R51 *0 4/S — R52 *1K_4 — VADJ1

<31> PWM_VADJ — C61 33P/50V_4

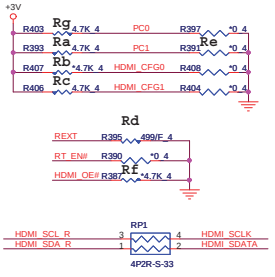
SI modify

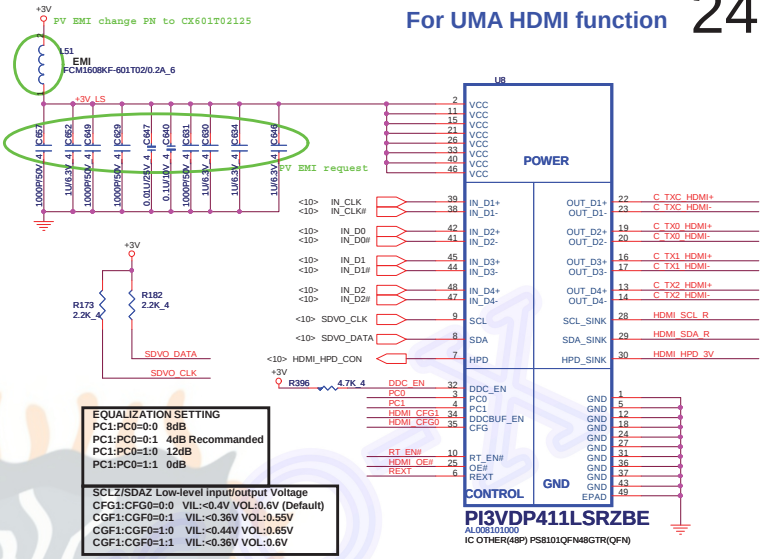
PROJECT : R18D
Quanta Computer Inc.

Size: Custom
Document Number: LCD CONN/LID/CAM
1A

Date: Tuesday, February 15, 2011 — Sheet 22 of 42

Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K





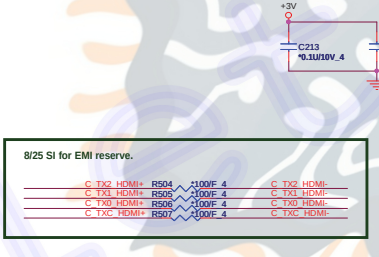
Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

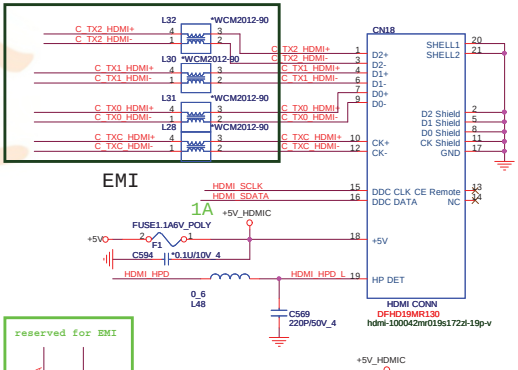
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

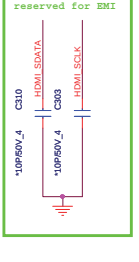
CHR : need Na R1182, add R1027 for capella

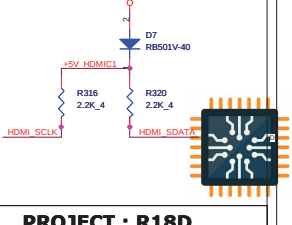
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

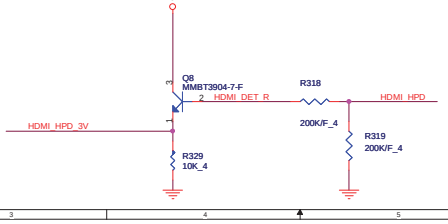
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V











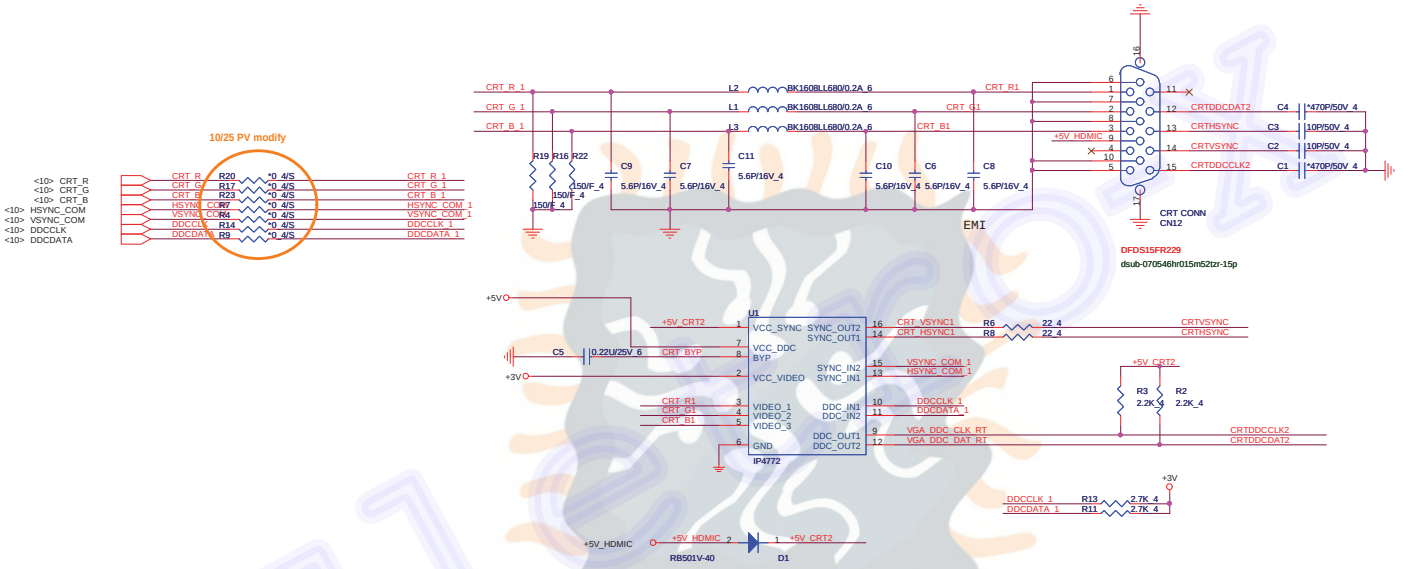
Eletro-X

PROJECT : R18D
Quanta Computer Inc.

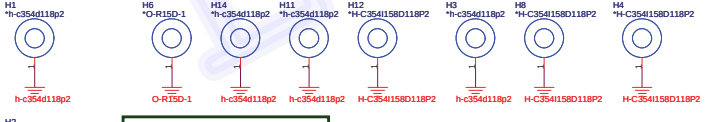
Size	Document Number	Rev
Custom	HDMI CONN	1A

Date: Tuesday, February 15, 2011 Sheet 23 of 42

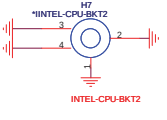
CRT PORT



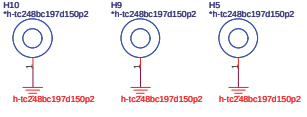
HOLE



CPU



VGA

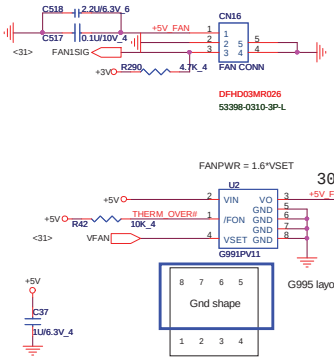


Eletro-X

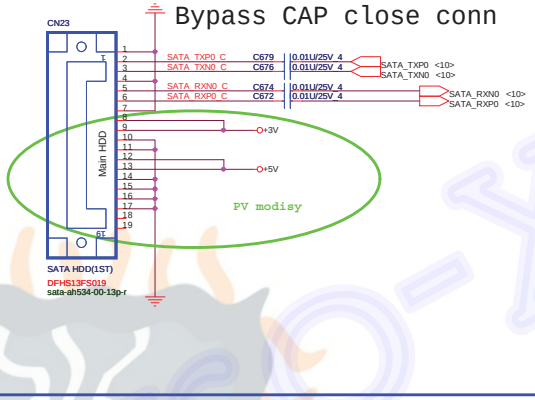
PROJECT : R18D
Quanta Computer Inc.

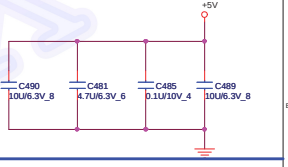
Size	Document Number	Rev
Custom	CRT,Hole	1A
Date: Tuesday, February 15, 2011	Sheet 24 of 42	

CPU FAN

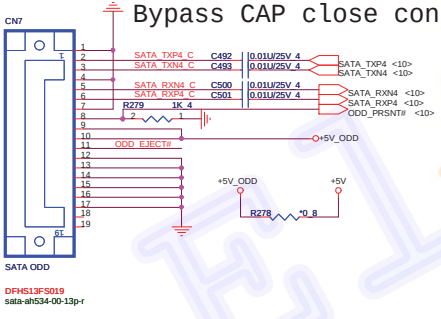


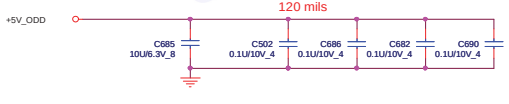
SATA HDD CONNECTOR

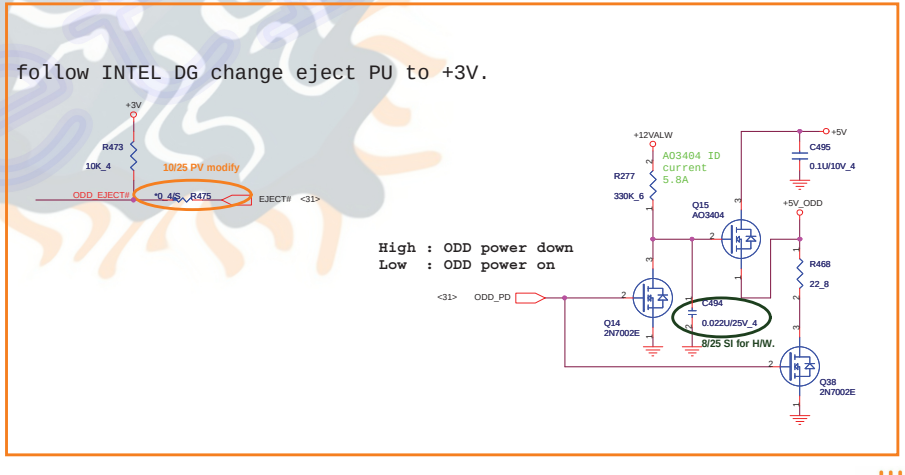


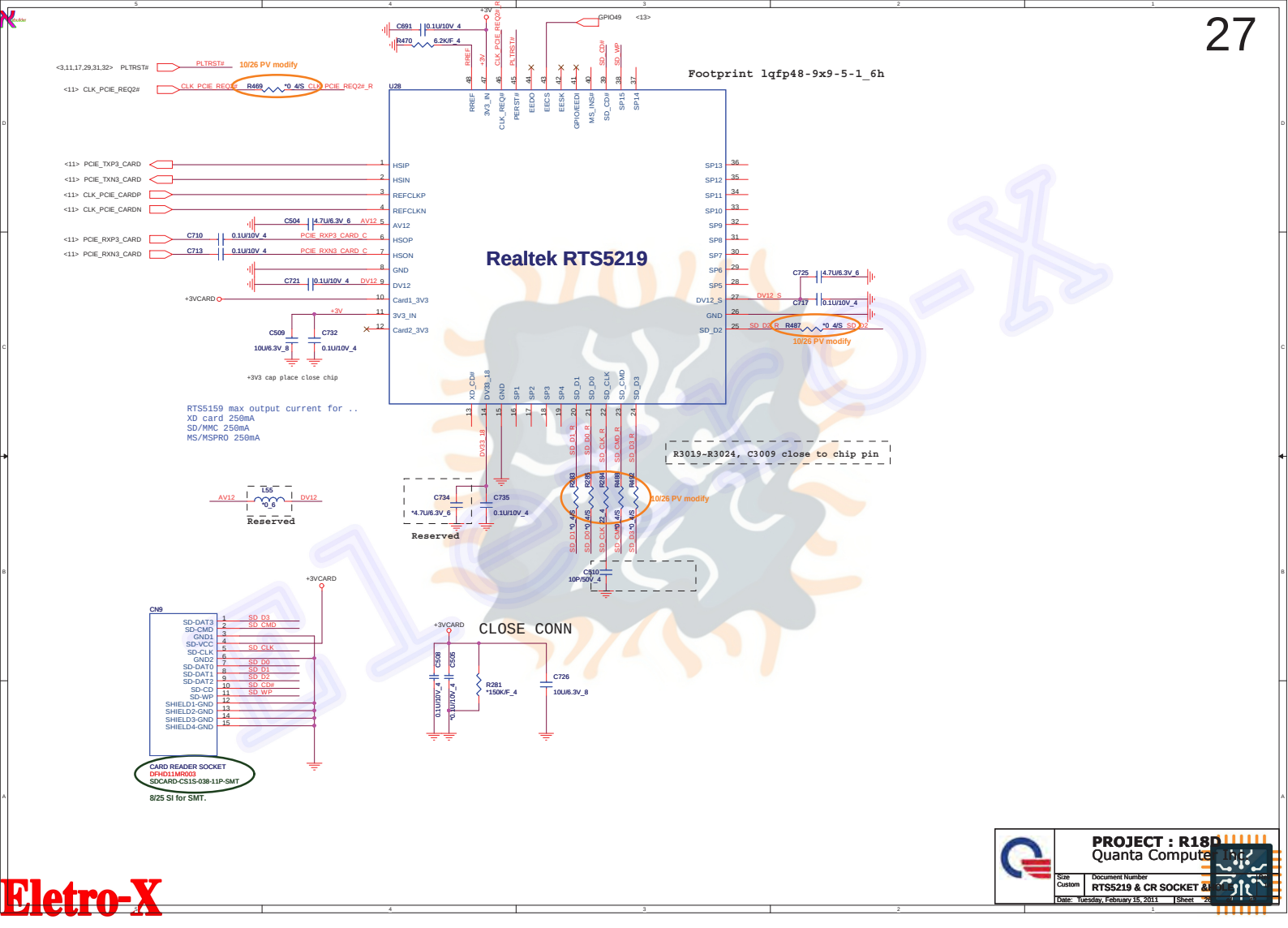


SATA ODD CONNECTOR



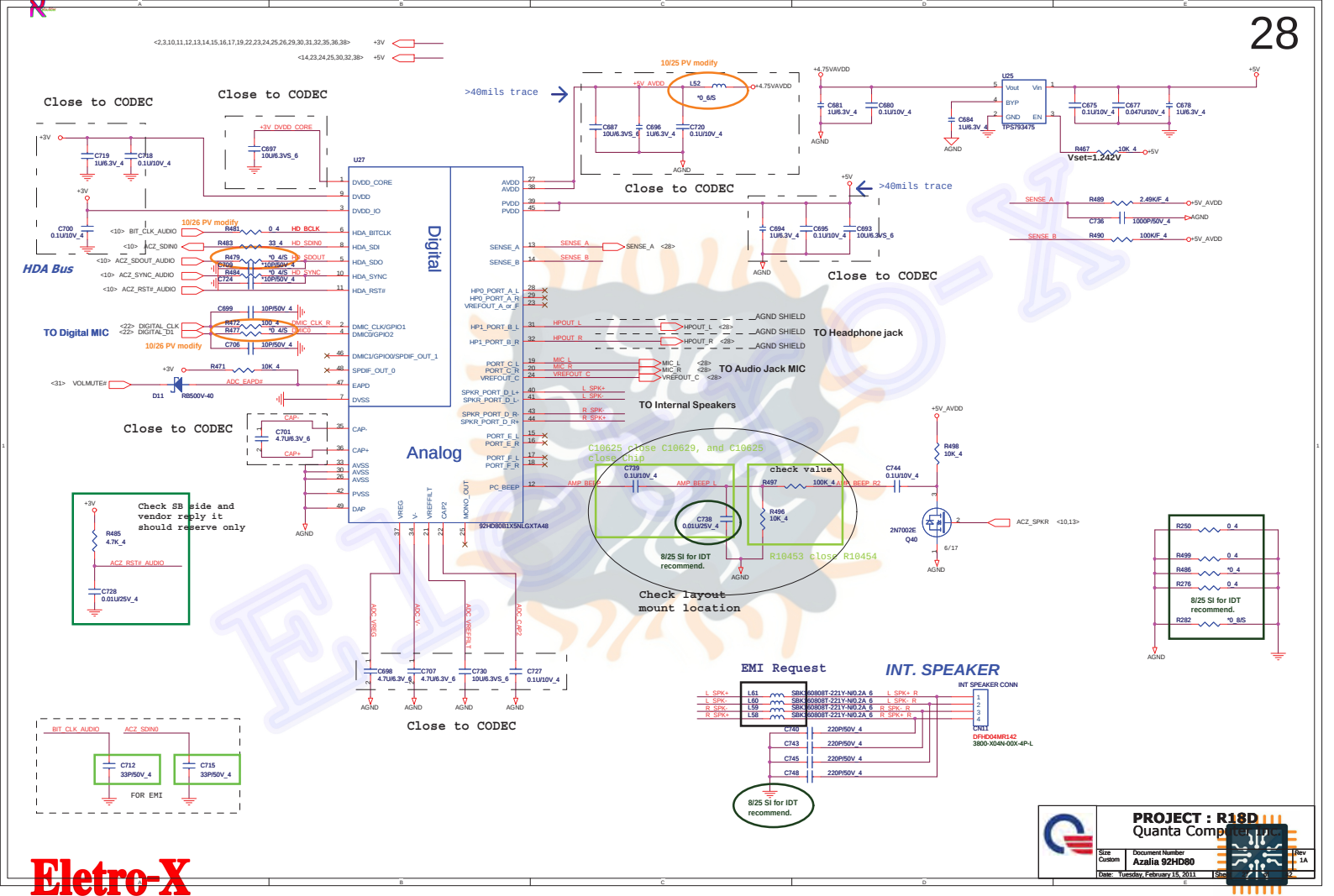






PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	
Custom	RTS5219 & CR SOCKET & CONN	
Date: Tuesday, February 15, 2011	Sheet 26	


Close to CODEC
Close to CODEC
>40mils trace
10/25 PV modify
Close to CODEC
>40mils trace
Close to CODEC
HDA Bus
TO Digital MIC
10/26 PV modify
Close to CODEC
Digital
Analog
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
C10625 close C10629, and C10625 close chip
check value
8/25 SI for IDT recommend.
R10453 close R10454
Check layout mount location
Check SB side and vendor reply it should reserve only
Close to CODEC
EMI Request
INT. SPEAKER
8/25 SI for IDT recommend.
8/25 SI for IDT recommend.
FOR EMI
PROJECT : R18D
Quanta Computer Inc.
Azalia 92HD80
Tuesday, February 15, 2011

Eletro-X

BLUETOOTH

EMI request
BLUELED C496 *1000P/50V_4

300mA
change to +3VS5

+3VS5 R280 4.7K_4 Q16 ME2303-G
24mil 300mA
Q17 DTC144EUA C503 *0.01U/25V_4
+3VPCU_BT C498 0.1U/10V_4 C499 *10U/6.3V_8
<13,32> BT_OFF#

CN8 BLUE TOOTH CONN 87213-0600-6P-L DFHD06MR055
C497 *1000P/50V_4
T38
BTCON_P1
BLUELED <31,32>
USBP2- <12>
USBP2+ <12>
+3VPCU_BT

LEFT SIDE USBX2

change to AL000547005

2A
change to +5VS5
+5VS5 U23 80 mils (Iout=2A) 2A +5V_USBP0
VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC
G547E2P81U
<31> USBPW_ON#
C664 1U/6.3V_4
C348 470P/50V_4
C351 0.1U/10V_4
C414 470P/50V_4
C413 0.1U/10V_4
C660 100U/25V
8/25 SI for H/W.

change to ELEC CAP

C356 *0.1U/10V_4
1A
R149 *0_4 L23 +5V_USBP0
USBP0- R
USBP0+ R
WCM2012-90
R152 *0_4
8/25 SI for EMI.
CN19 USB CONN DFHD04MR133 usb-020173mr004s53qzl-4p-r-v
<12> USBP0-
<12> USBP0+

C411 *0.1U/10V_4
1A
R225 *0_4 L36 +5V_USBP0
USBP1- R
USBP1+ R
WCM2012-90
R226 *0_4
8/25 SI for EMI.
CN20 USB CONN DFHD04MR133 usb-020173mr004s53qzl-4p-r-v
<12> USBP1-
<12> USBP1+

Right SIDE USBX1

C27 0.1U/10V_4 +5VS5
<31> USBPW_ON#
CN1
R502 *0_4
USBP8- R
USBP8+ R
L5 WCM2012-90
R503 *0_4
8/25 SI for EMI.
USB board DFFC06MR001 88513-0601-6P-L-SMT
<32> USBP8-
<32> USBP8+

EMI request
USBPW_ON# C19 220P/50V_4

Line out

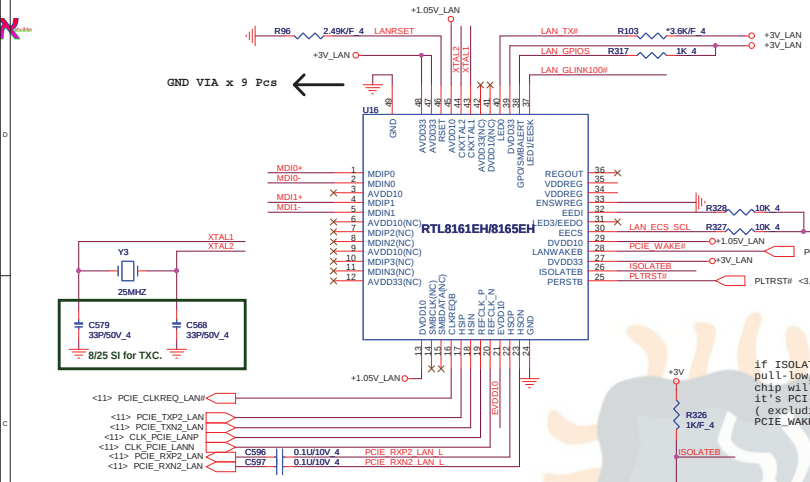
SENSE_PHONE R465 20K/F_4 SENSE_A
SENSE_MIC R256 10K/F_4 SENSE_A
SENSE_A <27>
AGND SHIELD
AGND SHIELD
AGND SHIELD
<27> HPOUT_L HPOUT_L
<27> HPOUT_R HPOUT_R
R482 16/F_4 HPOUT_L1 L39 SBK160808T-301Y-N/0.2A_6 HPOUT_L2
R480 16/F_4 HPOUT_R1 L42 SBK160808T-301Y-N/0.2A_6 HPOUT_R2
R275 20K/F_4
R270 20K/F_4
C491 1000P/50V_4
C476 1000P/50V_4
AGND
C483 0.1U/10V_4 C488 0.1U/10V_4
AGND
CN22 DFTJ06FR342 audio-311105-2-6p-smt
AEC_311105-2 Normal Open
AGND
SENSE_PHONE

MIC

C455 1U/6.3V_4 AGND
<27> VREFOUT_C VREFOUT_C R248 3.9K/F_4
R246 3.9K/F_4
<27> MIC_L MIC_L C688 2.2U/6.3V_6 MIC_L1 L37 SBK160808T-301Y-N/0.2A_6 MIC_IN_L
<27> MIC_R MIC_R C689 2.2U/6.3V_6 MIC_R1 L38 SBK160808T-301Y-N/0.2A_6 MIC_IN_R
C456 220P/50V_4
C436 220P/50V_4
AGND
CN21 DFTJ06FR342 audio-311105-2-6p-smt
AEC_311105-2 Normal Open
AGND
SENSE_MIC

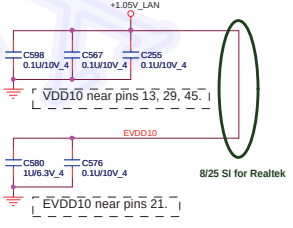
Eletro-X

PROJECT : R18D
Quanta Computer Inc.
Size: Custom
Document Number: USB/BT/Audio JacK
1A
Date: Tuesday, February 15, 2011 Sheet 28 of 42



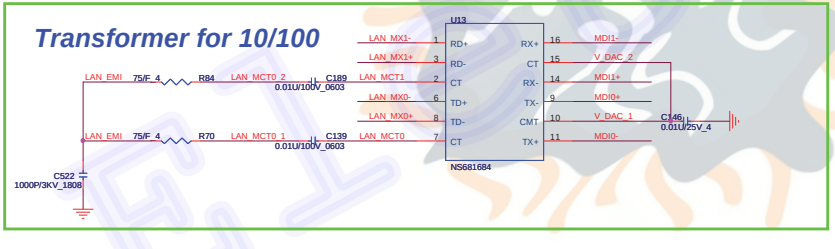
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

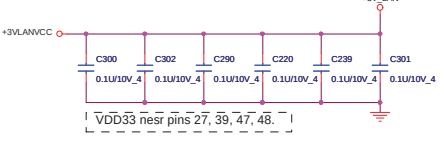
Power trace Layout 寬度> 60mil
>60mil



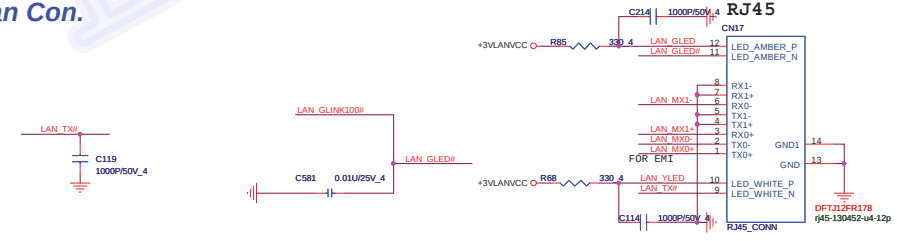
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Transformer for 10/100





Lan Con.



<3B> +3VLANVCC
<2,3,10,11,12,13,14,15,16,17,19,22,23,24,25,26,27,30,31,32,35,36,38> +3V

Eletro-X

PROJECT : R18D
Quanta Computer In

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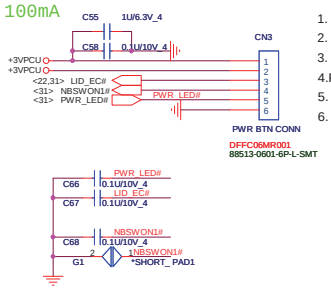
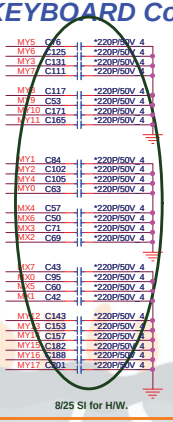
POWER BOTTON CONNECT

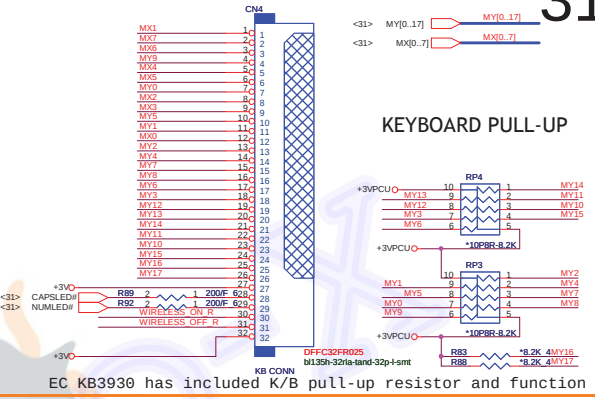


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.



8/25 SI for H/W.

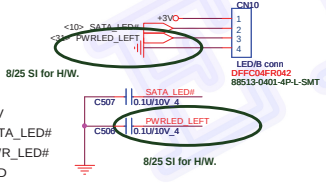


KEYBOARD PULL-UP

EC KB3930 has included K/B pull-up resistor and function

SI Modify

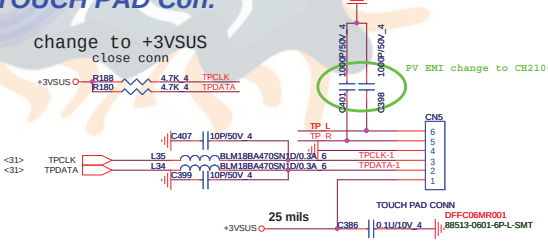
LED Con.



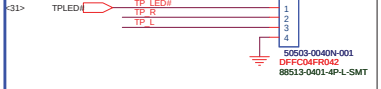
1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



PROJECT : R18D		
Quanta Computer In		
Size: Custom	Document Number: LED/KB/SW/TP	
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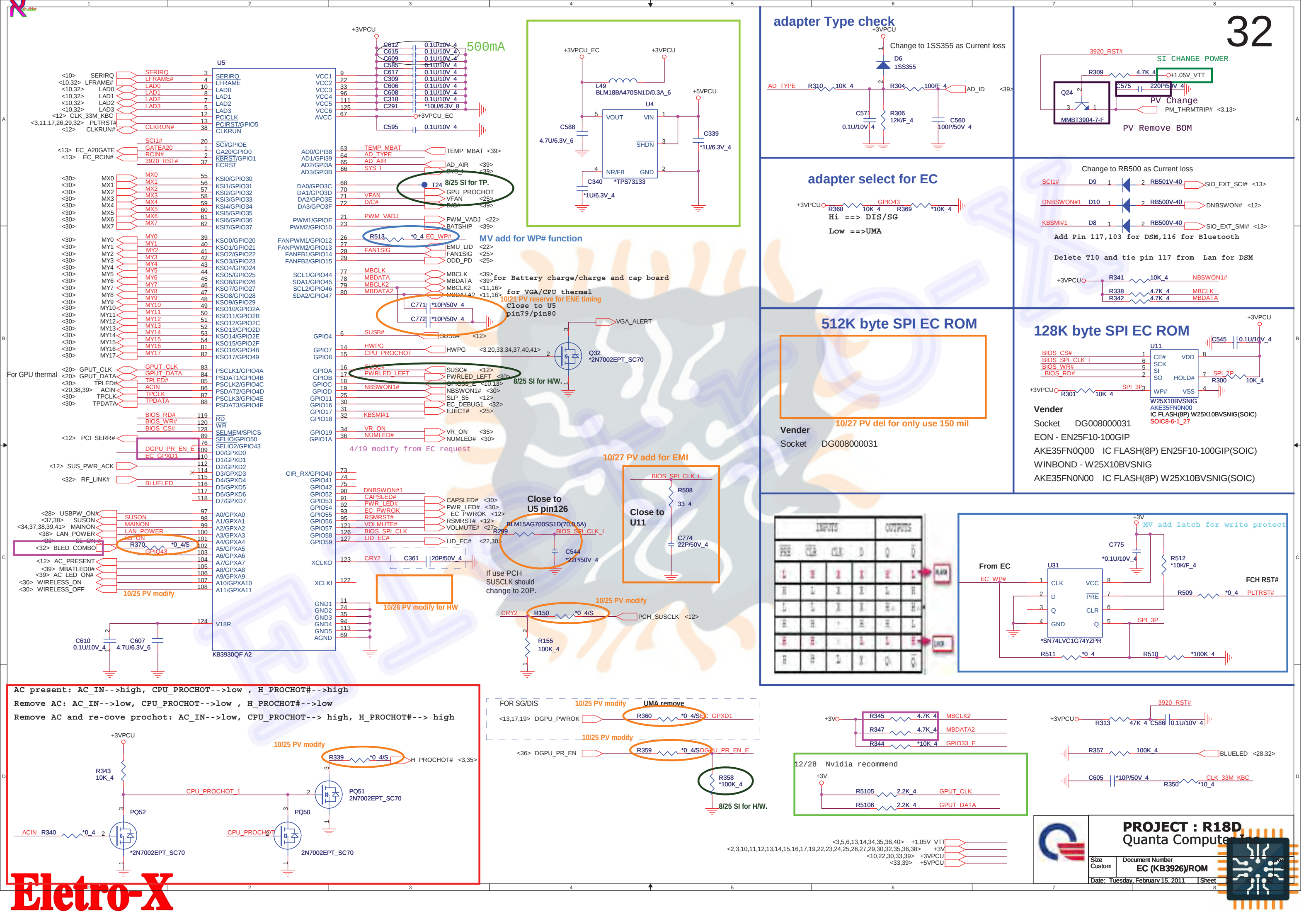
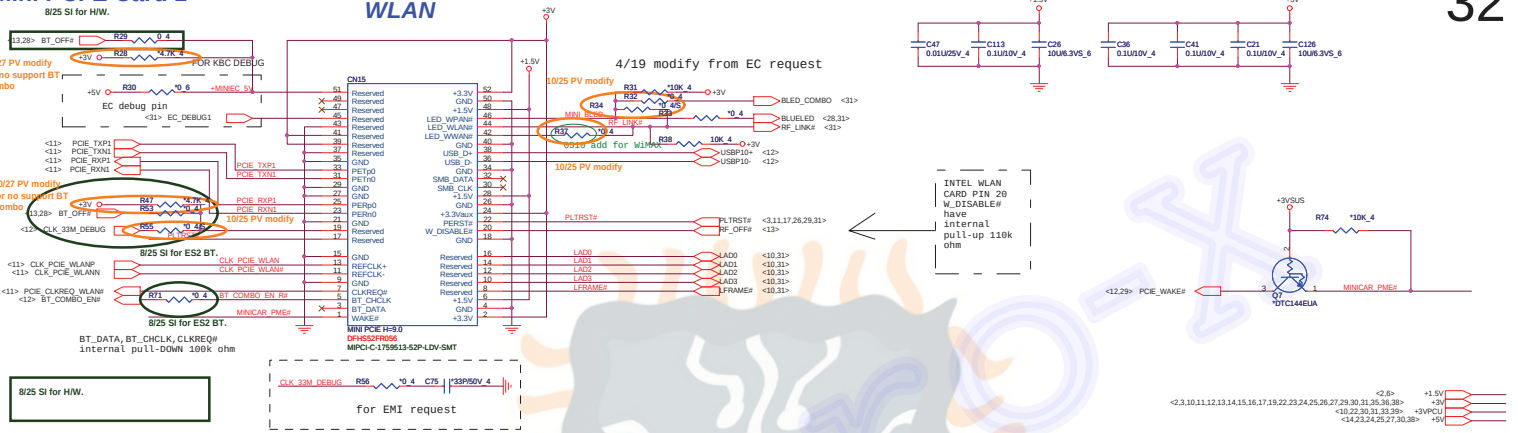


32
adapter Type check
Change to 1SS355 as Current loss
D6 1SS355
AD_TYPE R310 10K_4 R304 100/F_4 AD_ID <39>
C571 0.1U/10V_4 R306 12K/F_4 C560 100P/50V_4
3920_RST#
SI CHANGE POWER
R309 4.7K_4 +1.05V_VTT
Q24 C575 220P/50V_4
PV Change
PM_THRMTRIP# <3,13>
MMBT3904-7-F
PV Remove BOM
adapter select for EC
+3VPCU R368 10K_4 GPIO43 R369 *10K_4
Hi ==> DIS/SG
Low ==>UMA
Change to RB500 as Current loss
SCI1# D9 RB501V-40 SIO_EXT_SCI# <13>
DNBSWON#1 D10 RB500V-40 DNBSWON# <12>
KBSMI#1 D8 RB500V-40 SIO_EXT_SMI# <13>
Add Pin 117,103 for DSM,116 for Bluetooth
Delete T10 and tie pin 117 from Lan for DSM
+3VPCU R341 10K_4 NBSWON1#
R338 4.7K_4 MBCLK
R342 4.7K_4 MBDATA
512K byte SPI EC ROM
10/27 PV del for only use 150 mil
Vender
Socket DG008000031
128K byte SPI EC ROM
U11 CE# VDD SCK SI SO HOLD# WP# VSS
BIOS_CS# BIOS_SPI_CLK_I BIOS_WR# BIOS_RD#
C545 0.1U/10V_4 SPI_?P R300 10K_4 SPI_3P R301 10K_4
W25X10BVSNIG AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC) SOIC8-6-1_27
Vender
Socket DG008000031
EON - EN25F10-100GIP
AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)
WINBOND - W25X10BVSNIG
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)
U5 KB3930QF A2
SERIRQ LFRAME LAD0 LAD1 LAD2 LAD3 PCICLK PCIRST/GPIO5 CLKRUN
SCI/GPIOE GA20/GPIO0 KBRST/GPIO1 ECRST
KSI0/GPIO30 ... KSI7/GPIO37
KSO0/GPIO20 ... KSO17/GPIO49
PSCLK1/GPIO4A PSDAT1/GPIO4B PSCLK2/GPIO4C PSDAT2/GPIO4D PSCLK3/GPIO4E PSDAT3/GPIO4F
RD WR SELMEM/SPICS SELIO/GPIO50 SELIO2/GPIO43
D0/GPXD0 ... D7/GPXD7
A0/GPXA0 ... A11/GPXA11
V18R
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 AVCC
AD0/GPI38 AD1/GPI39 AD2/GPI3A AD3/GPI3B
DA0/GPO3C DA1/GPO3D DA2/GPO3E DA3/GPO3F
PWM1/GPIOE PWM2/GPIO10
FANPWM1/GPIO12 FANPWM2/GPIO13 FANFB1/GPIO14 FANFB2/GPIO15
SCL1/GPIO44 SDA1/GPIO45 SCL2/GPIO46 SDA2/GPIO47
GPIO4 GPIO7 GPIO8 GPIOA GPIOB GPIOC GPIOD GPIO11 GPIO16 GPIO17 GPIO18 GPIO19 GPIO1A
CIR_RX/GPIO40 GPIO41 ... GPIO59
XCLKO XCLKI
GND1 GND2 GND3 GND4 GND5 AGND
500mA
C612 C615 C609 C585 C617 C309 C606 C608 C318 C291 0.1U/10V_4 *10U/6.3V_8
C595 0.1U/10V_4
TEMP_MBAT <39> AD_TYPE AD_AIR <39> SYS_I <39>
T24 8/25 SI for TP. GPU_PROCHOT VFAN D/C#
PWM_VADJ <22> BATSHIP <39>
R513 *0_4 EC_WP#
MV add for WP# function
EMU_LID <22> FAN1SIG <25> ODD_PD <25>
MBCLK MBDATA MBCLK2 MBDATA2
for Battery charge/charge and cap board
for VGA/CPU thermal
10/21 PV reserve for ENE timing
Close to U5 pin79/pin80
C771 *10P/50V_4 C772 *10P/50V_4
VGA_ALERT
Q32 *2N7002EPT_SC70
SUSB# HWPG <3,20,33,34,37,40,41> CPU_PROCHOT
SUSC# PWRLED_LEFT <30> 8/25 SI for H/W.
NBSWON1# SLP_S5 <12> EC_DEBUG1 <32> EJECT# <25>
VR_ON <35> NUMLED# <30>
4/19 modify from EC request
For GPU thermal
10/27 PV add for EMI
BIOS_SPI_CLK_I R508 33_4 C774 22P/50V_4
Close to U11
Close to U5 pin126
BLM15AG700SS1D(70,0.5A) R299 BIOS_SPI_CLK_I C544 *22P/50V_4
If use PCH SUSCLK should change to 20P.
CAPSLED# <30> PWR_LED# <30> EC_PWROK <12> RSMRST# <12> VOLMUTE# <27> LID_EC# <22,30>
CRY2 C361 20P/50V_4
10/26 PV modify for HW
10/25 PV modify
CRY2 R150 *0_4/S PCH_SUSCLK <12>
R155 100K_4
C610 0.1U/10V_4 C607 4.7U/6.3V_6
10/25 PV modify
+3VPCU_EC +3VPCU +5VPCU
L49 BLM18BA470SN1D/0.3A_6
U4 VOUT VIN SHDN NR/FB GND *TPS73133
C588 4.7U/6.3V_6 C339 *1U/6.3V_4 C340 *1U/6.3V_4
MV add latch for write protect
From EC EC_WP# U31 CLK D Q GND VCC PRE CLR Q
C775 *0.1U/10V_4 R512 *10K/F_4
FCH RST# R509 *0_4 PLTRST#
SPI_3P *SN74LVC1G74YZPR R511 *0_4 R510 *100K_4
INPUTS OUTPUTS
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
+3VPCU R343 10K_4 CPU_PROCHOT_1
10/25 PV modify R339 *0_4/S H_PROCHOT# <3,35>
PQ51 2N7002EPT_SC70 PQ52 PQ50 *2N7002EPT_SC70 2N7002EPT_SC70
ACIN R340 *0_4 CPU_PROCHOT
FOR SG/DIS 10/25 PV modify UMA remove
<13,17,19> DGPU_PWROK R360 *0_4/S EC_GPXD1
10/25 PV modify
<36> DGPU_PR_EN R359 *0_4/S DGPU_PR_EN_E
R358 *100K_4 8/25 SI for H/W.
+3V R345 4.7K_4 MBCLK2 R347 4.7K_4 MBDATA2 R344 *10K_4 GPIO33_E
12/28 Nvidia recommend
+3V R5105 2.2K_4 GPUT_CLK R5106 2.2K_4 GPUT_DATA
3920_RST# +3VPCU R313 47K_4 C586 0.1U/10V_4
R357 100K_4 BLUELED <28,32>
C605 *10P/50V_4 R350 *10_4 CLK_33M_KBC
<3,5,6,13,14,34,35,36,40> +1.05V_VTT
+3V +3VPCU +5VPCU
PROJECT : R18D
Quanta Computer Inc.
Size Custom Document Number EC (KB3926)/ROM
Date: Tuesday, February 15, 2011 Sheet
Eletro-X

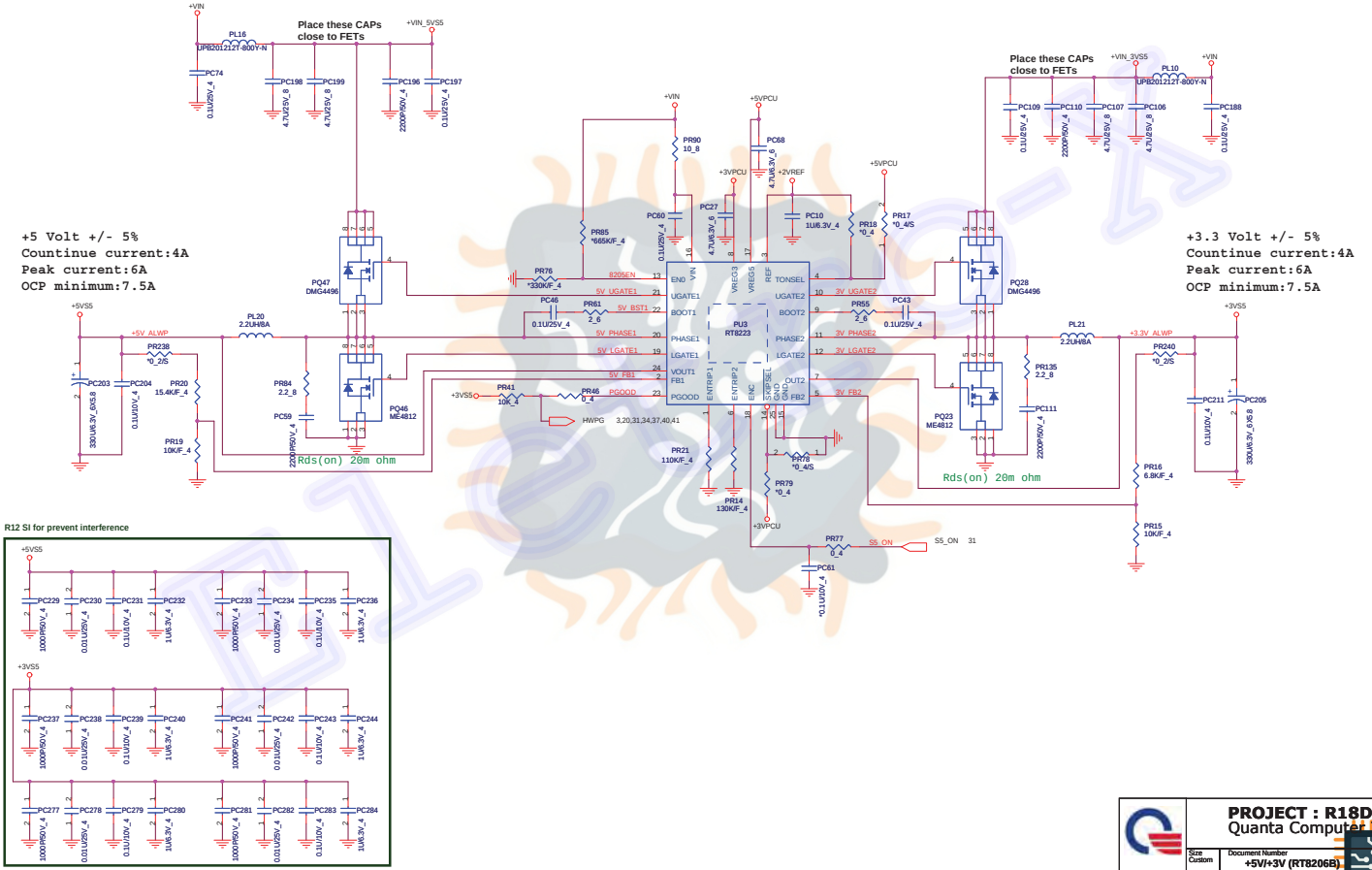
Mini PCI-E Card 1

WLAN

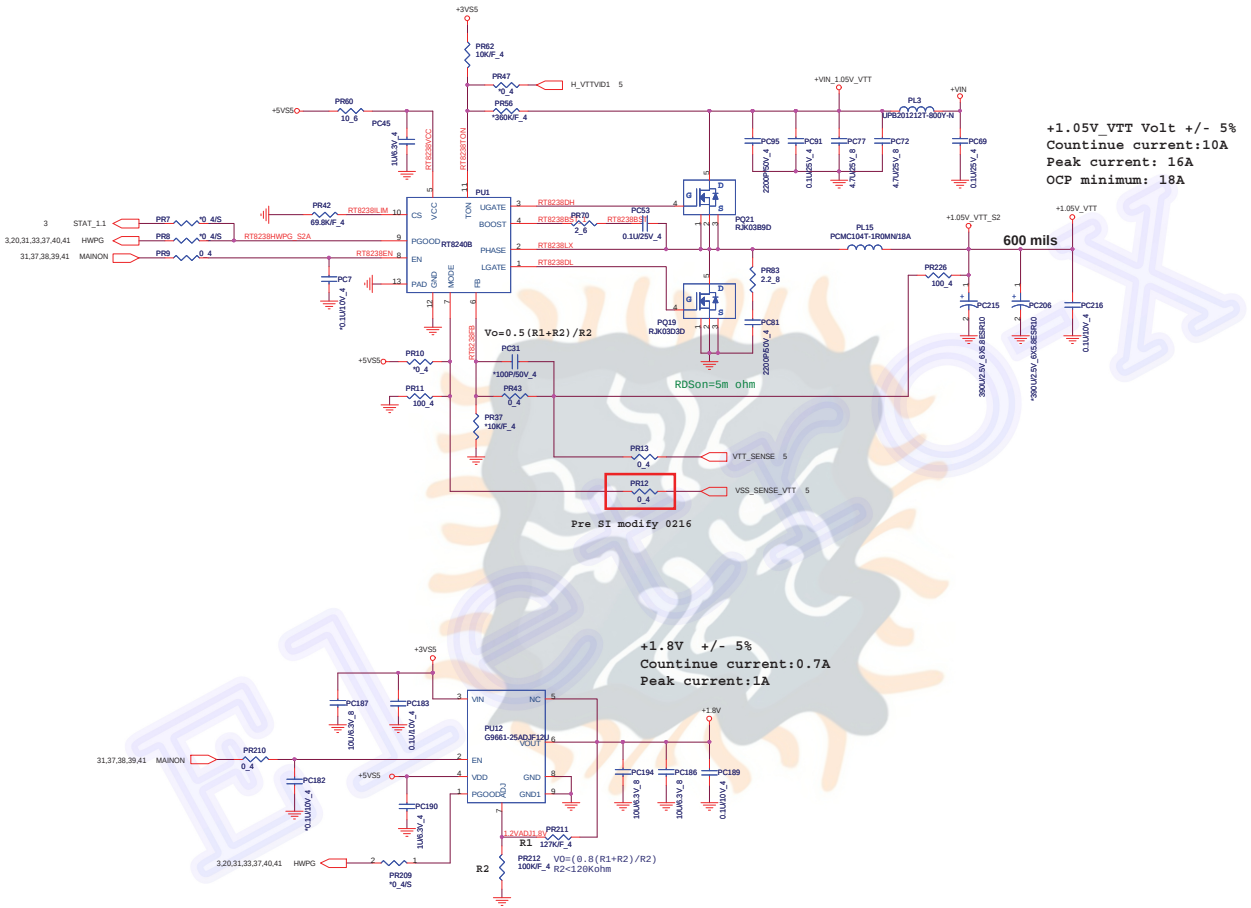
8/25 SI for H/W.

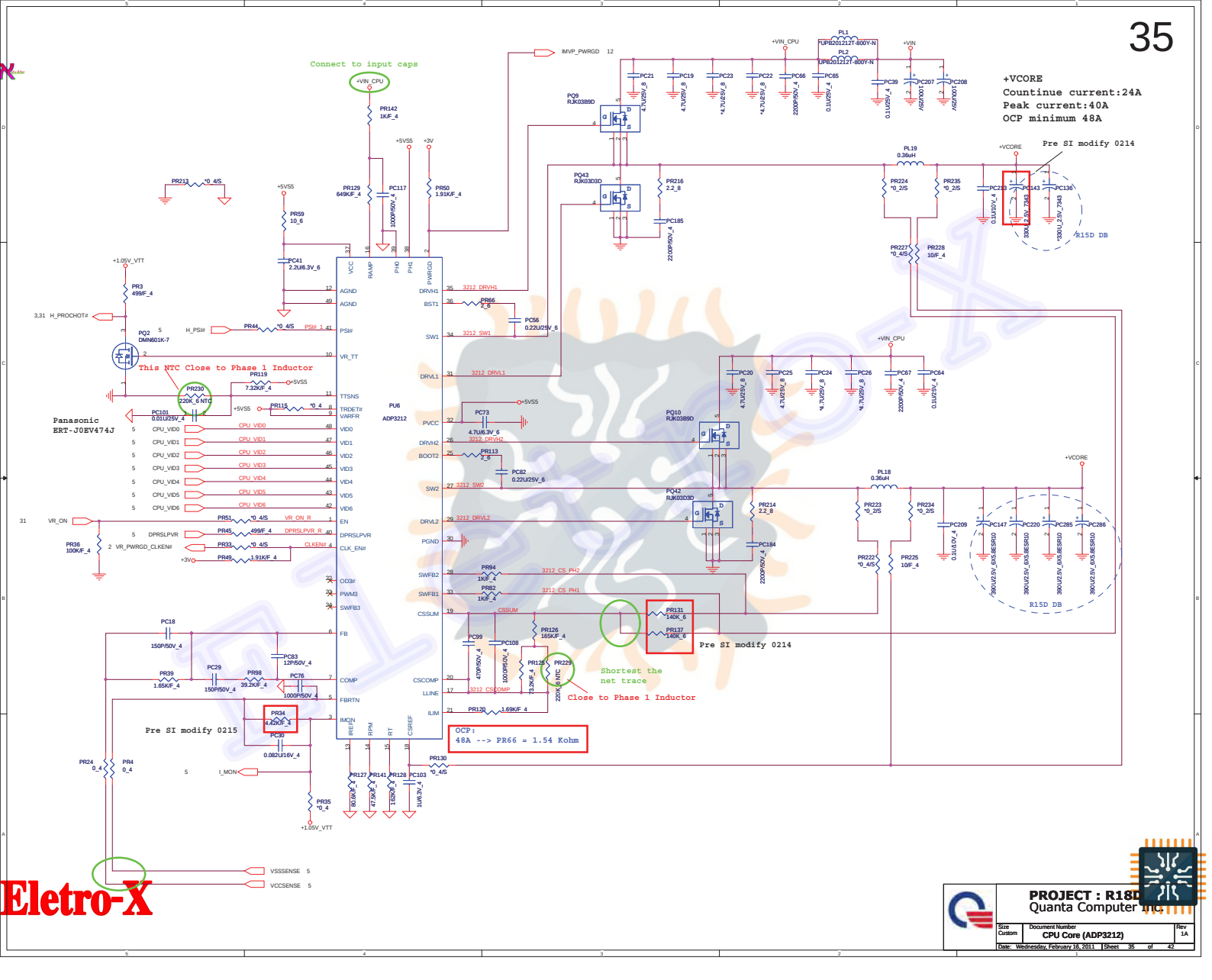


PROJECT : R18D	
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X1
Date: Tuesday, February 15, 2011	Sheet



PROJECT : R18D
Quanta Computer Inc.
Size: Custom | Document Number: +5V/+3V (RT8206B) | Rev: 1A
Date: Wednesday, February 16, 2011 | Sheet 2


+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A
600 mils
Vo=0.5(R1+R2)/R2
RDSon=5m ohm
Pre SI modify 0216
+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A
R2<120Kohm
PROJECT : R18D
Quanta Computer Inc.
+1.1V VTT / PCH
Wednesday, February 16, 2011


+VCORE
Countinue current:24A
Peak current:40A
OCP minimum 48A
Connect to input caps
Pre SI modify 0214
Pre SI modify 0215
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Shortest the
net trace
Close to Phase 1 Inductor
OCP:
48A --> PR66 = 1.54 Kohm
R15D DB
PU6
ADP3212
PQ2
DMN601K-7
PQ9
RJK03B9D
PQ43
RJK03D3D
PQ10
RJK0389D
PQ42
RJK03D3D
PL1
PL2
PL19
0.36uH
PL18
0.36uH
VCC
AGND
PSI#
VR_TT
TTSNS
TRDET#
VARFR
VID0
VID1
VID2
VID3
VID4
VID5
VID6
EN
DPRSLPVR
CLK_EN#
OD3#
PWM3
SWFB3
FB
COMP
FBRTN
IMON
IREF
RPM
RT
CSREF
PWRGD
DRVH1
BST1
SW1
DRVL1
PVCC
DRVH2
BOOT2
SW2
DRVL2
PGND
SWFB2
SWFB1
CSSUM
CSCOMP
LLINE
ILIM
RAMP
PH0
PH1
VR_ON
VR_PWRGD_CLKEN#
H_PROCHOT#
H_PSI#
I_MON
VSSSENSE
VCCSENSE
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
IMVP_PWRGD
+VIN_CPU
+VIN
+5VS5
+3V
+1.05V_VTT
PR142 1K/F_4
PR129 649K/F_4
PC117 1000P/50V_4
PR50 1.91K/F_4
PR59 10_6
PC41 2.2U/6.3V_6
PR213 *0_4/S
PR3 499/F_4
PR44 *0_4/S
PR119 7.32K/F_4
PR230 220K_6 NTC
PC101 0.01U/25V_4
PR115 *0_4
PR51 *0_4/S
PR45 499/F_4
PR33 *0_4/S
PR45 1.91K/F_4
PR36 100K/F_4
PC18 150P/50V_4
PC29 150P/50V_4
PR39 1.65K/F_4
PC83 12P/50V_4
PR98 39.2K/F_4
PC76 1000P/50V_4
PR34 4.42K/F_4
PC30 0.082U/16V_4
PR24 0_4
PR4 0_4
PR35 *0_4
PR127 80.6K/F_4
PR141 47.5K/F_4
PR128 165K/F_4
PC103 1U/6.3V_4
PR130 *0_4/S
PC73 4.7U/6.3V_6
PR66 2_6
PC56 0.22U/25V_6
PR113 2_6
PC82 0.22U/25V_6
PR94 1K/F_4
PR82 1K/F_4
PC99 470P/50V_4
PC108 100P/50V_4
PR125 72.2K/F_4
PR229 220K_6 NTC
PR126 165K/F_4
PR120 1.69K/F_4
PR131 140K_6
PR137 140K_6
PC21 4.7U/25V_6
PC19 4.7U/25V_6
PC23 4.7U/25V_6
PC22 4.7U/25V_6
PC86 2200P/50V_4
PC65 0.1U/25V_4
PC39 0.1U/25V_4
PC207 470U/2V_10X12
PC208 470U/2V_10X12
PR216 2.2_8
PC185 2200P/50V_4
PR224 *0_2/S
PR235 *0_2/S
PR227 *0_4/S
PR228 10/F_4
PC223 0.1U/10V_4
PC143 330U_2.5V_7343
PC136 330U_2.5V_7343
PC20 4.7U/25V_6
PC25 4.7U/25V_6
PC24 4.7U/25V_6
PC26 4.7U/25V_6
PC87 2200P/50V_4
PC64 0.1U/25V_4
PR214 2.2_8
PC184 2200P/50V_4
PR223 *0_2/S
PR234 *0_2/S
PR222 *0_4/S
PR225 10/F_4
PC209 0.1U/10V_4
PC147 390U/2.5V_6X5.8ESR10
PC220 390U/2.5V_6X5.8ESR10
PC285 390U/2.5V_6X5.8ESR10
PC286 390U/2.5V_6X5.8ESR10
Eletro-X
PROJECT : R18D
Quanta Computer Inc.
CPU Core (ADP3212)
Size Custom
Document Number
Rev 1A
Date: Wednesday, February 16, 2011
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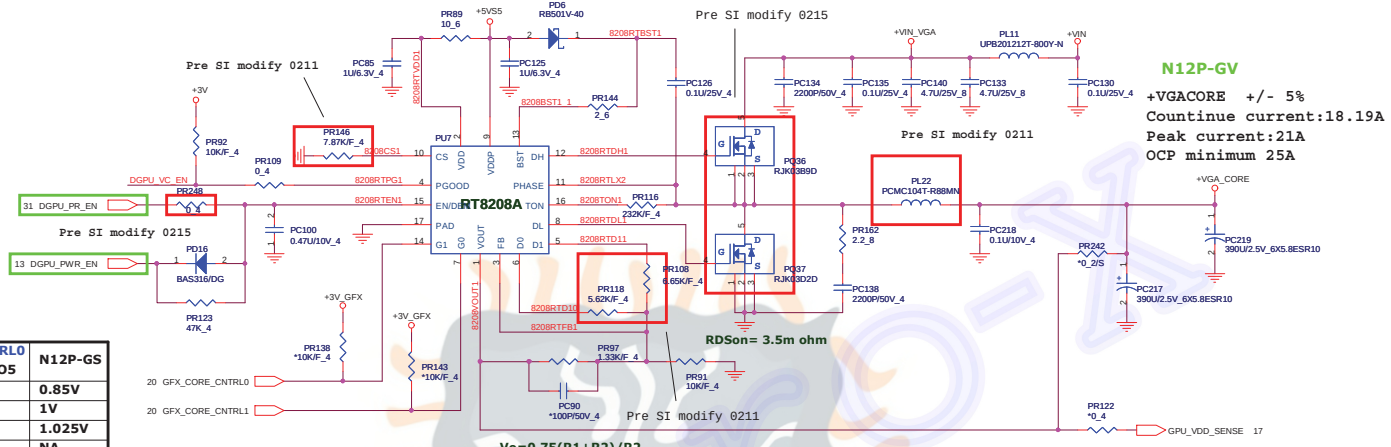
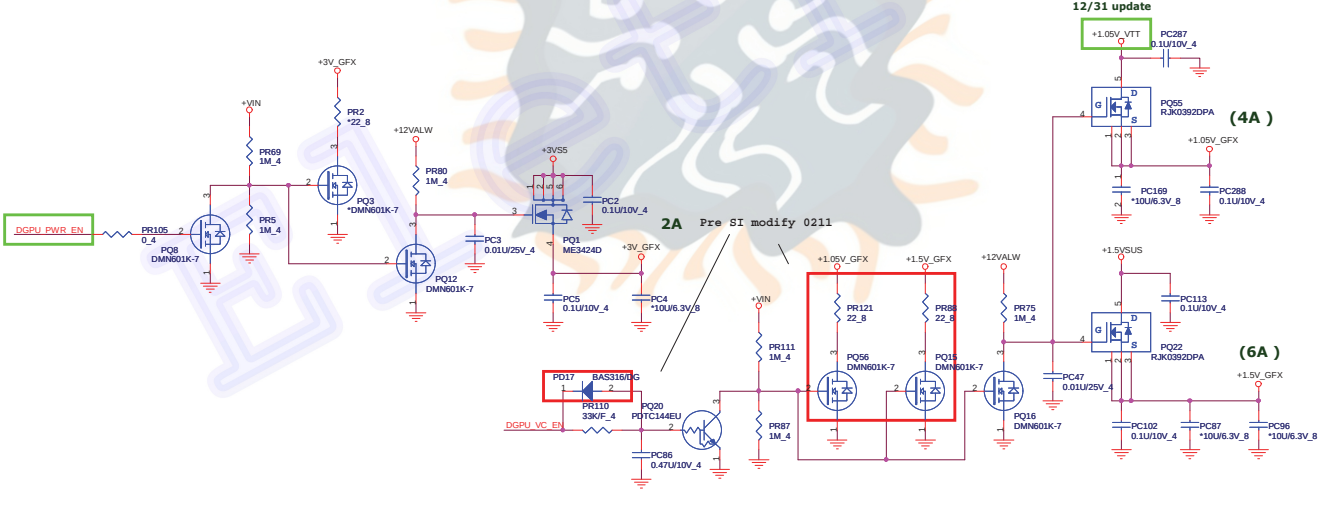
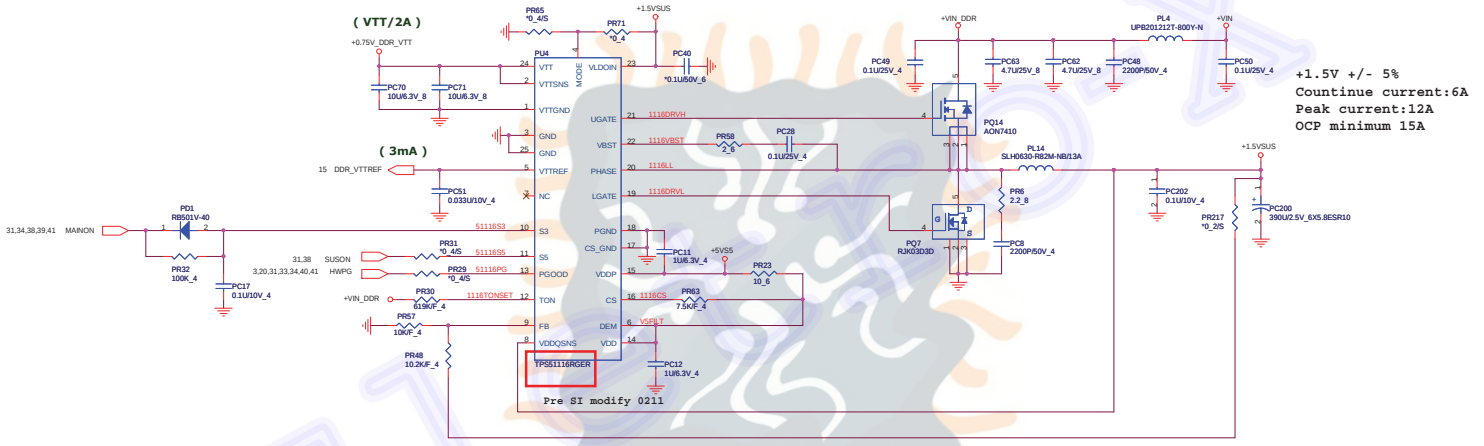


CNTRL1 GPIO6	CNTRL0 GPIO5	N12P-GS
0	0	0.85V
0	1	1V
1	0	1.025V
1	1	NA



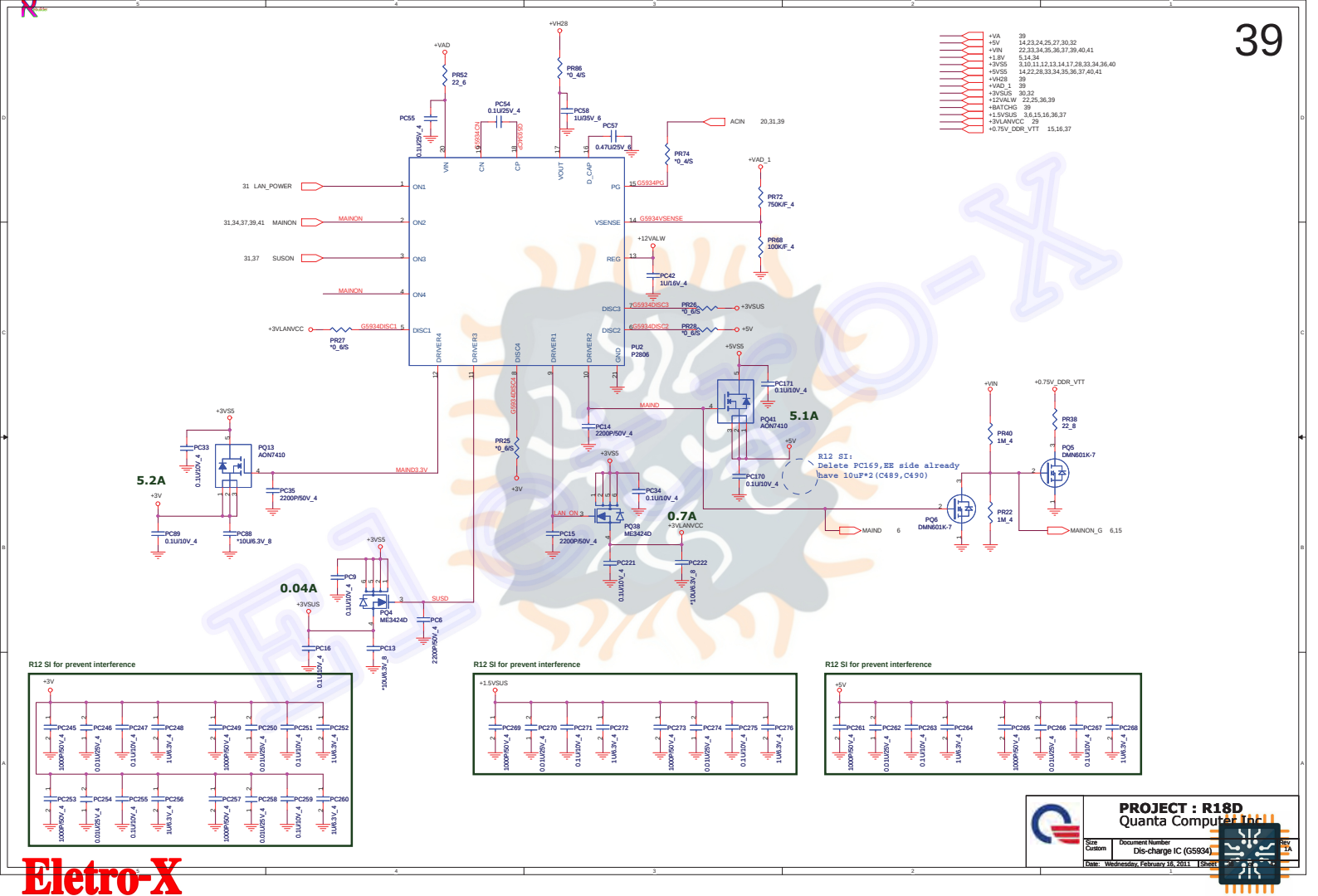


+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

PROJECT : R18D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

Date: Wednesday, February 16, 2011 | Sheet


+VA 39
+5V 14,23,24,25,27,30,32
+VIN 22,33,34,35,36,37,39,40,41
+1.8V 5,14,34
+3VS5 3,10,11,12,13,14,17,28,33,34,36,40
+5VS5 14,22,28,33,34,35,36,37,40,41
+VH28 39
+VAD_1 39
+3VSUS 20,22
+12VALW 22,25,36,39
+BATCHG 39
+1.5VSUS 3,6,15,16,36,37
+3VLANVCC 29
+0.75V_DDR_VTT 15,16,37
+VAD
PR52 22_6
+VH28
PR86 *0_4/S
PC54 0.1U/25V_4
PC55 0.1U/25V_4
PC58 1U/35V_6
PC57 0.47U/25V_6
ACIN 20,31,39
PR74 *0_4/S
+VAD_1
PR72 750K/F_4
PR68 100K/F_4
31 LAN_POWER
31,34,37,39,41 MAINON
31,37 SUSON
MAINON
+3VLANVCC
G5934DISC1
PR27 *0_6/S
ON1
ON2
ON3
ON4
DISC1
VIN
CN
CP
VOUT
D_CAP
PG
VSENSE
REG
DISC3
DISC2
DRIVER4
DRIVER3
DISC4
DRIVER1
DRIVER2
GND
G5934PG
G5934VSENSE
+12VALW
PC42 1U/16V_4
G5934DISC3
G5934DISC2
PR26 *0_6/S
PR28 *0_6/S
+3VSUS
+5V
PU2 P2806
+5VS5
PC171 0.1U/10V_4
PQ41 AON7410
5.1A
MAIND
PC14 2200P/50V_4
PR25 *0_6/S
G5934DISC2
+3VS5
PC33 0.1U/10V_4
PQ13 AON7410
5.2A
MAIND3.3V
PC35 2200P/50V_4
+3V
PC89 0.1U/10V_4
PC88 *10U/6.3V_8
PC34 0.1U/10V_4
PC170 0.1U/10V_4
R12 SI:
Delete PC169,EE side already
have 10uF*2(C489,C490)
LAN_ON 3
PC15 2200P/50V_4
PQ38 ME3424D
0.7A
+3VLANVCC
PC221 0.1U/10V_4
PC222 *10U/6.3V_8
MAIND 6
+VIN
+0.75V_DDR_VTT
PR40 1M_4
PR38 22_8
PQ5 DMN601K-7
PQ6 DMN601K-7
PR22 1M_4
MAINON_G 6,15
+3VS5
PC9 0.1U/10V_4
PQ4 ME3424D
0.04A
SUSD
PC6 2200P/50V_4
+3VSUS
PC16 0.1U/10V_4
PC13 *10U/6.3V_8
R12 SI for prevent interference
+3V
PC245 PC246 PC247 PC248 PC249 PC250 PC251 PC252
PC253 PC254 PC255 PC256 PC257 PC258 PC259 PC260
1000P/50V_4
0.01U/25V_4
0.1U/10V_4
1U/6.3V_4
R12 SI for prevent interference
+1.5VSUS
PC269 PC270 PC271 PC272 PC273 PC274 PC275 PC276
R12 SI for prevent interference
+5V
PC261 PC262 PC263 PC264 PC265 PC266 PC267 PC268
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Quanta Computer Inc.
Size Custom
Document Number
Dis-charge IC (G5934)
Rev 1A
Date: Wednesday, February 16, 2011
Sheet

DC_JACK
90W

R12 PV:
change footprint.
R12 SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

R12 SI:
M/E modify.

To PWR LED

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

PU9
OZ8681

+VA	
+VH28	38
+VAD_1	38
+3VPCU	10,22,30,31,33
+5VPCU	31,33
+BATCHG	

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Custom	Charger (OZ8681)	1A
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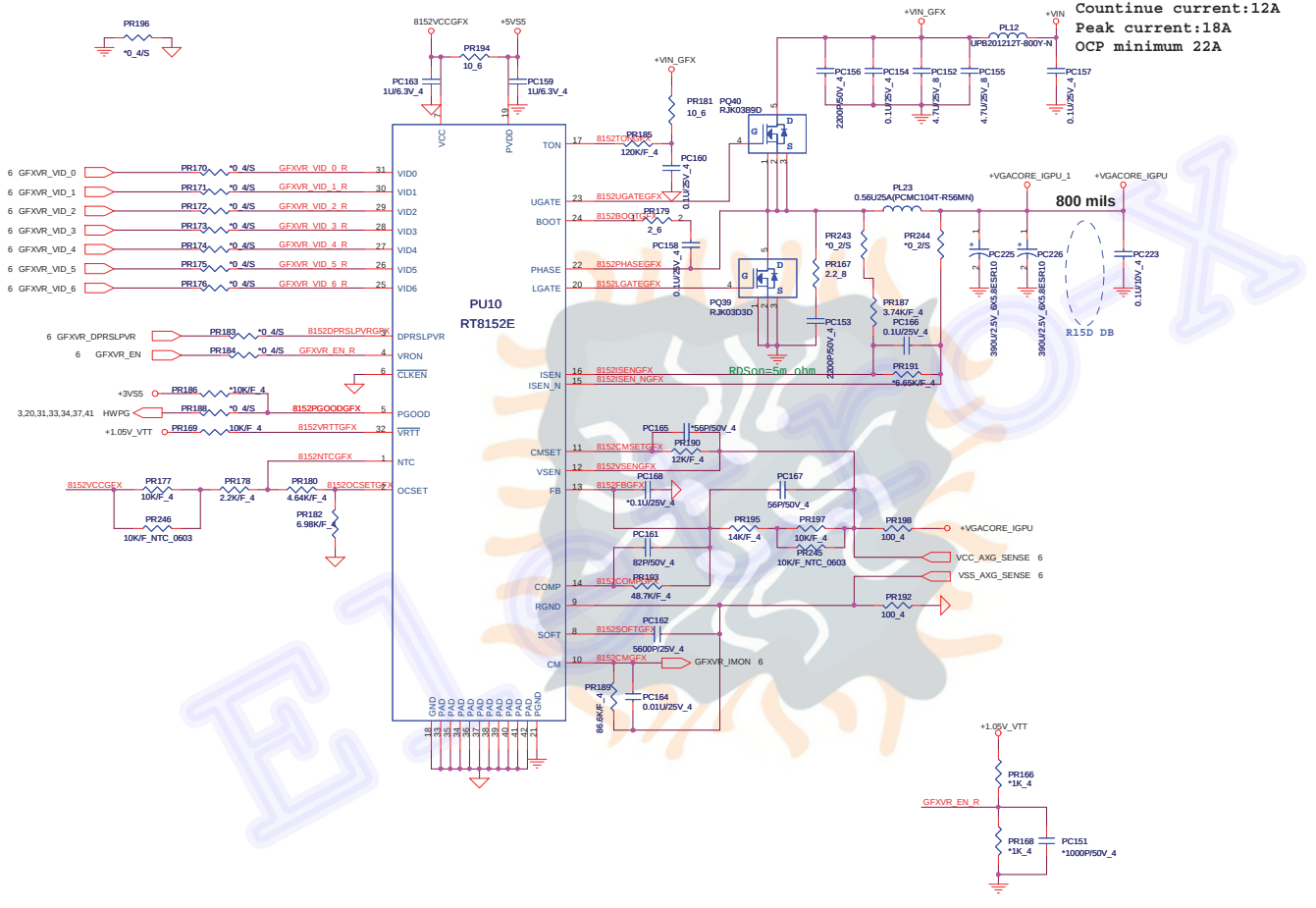
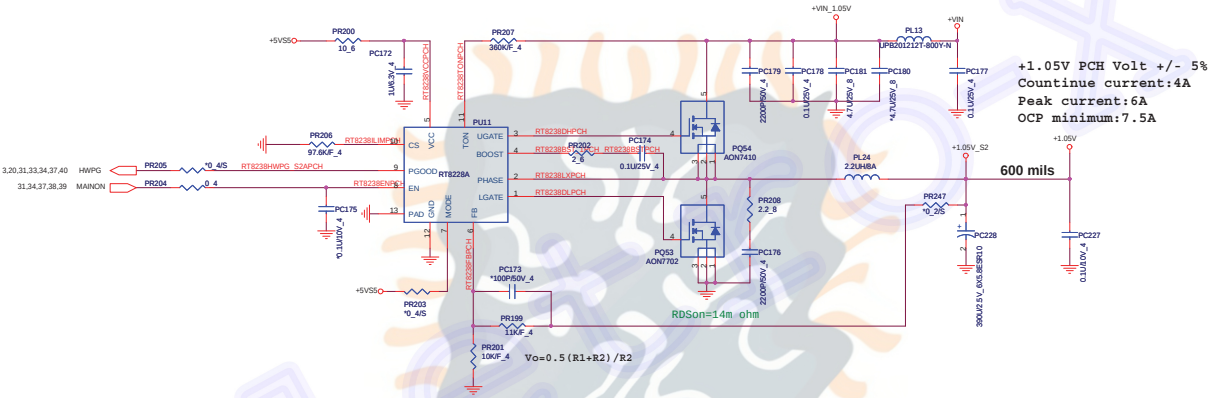
+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A





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Size	Document Number	Rev
Custom	+1.05V (RT8238A)	1A
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-->Pre SI

Page 19

1.Delete L5005, C5096,C5097,C5098,C5099,C5100 and connect +SP_PLLVDD to +NV_PLLVDD

2.L5004 change to bead 220ohm (ESR=0.5) 0603.
3.C5089 change to 22uF_0805

Page 11

1.delete Q35.

Page 17

1.delete L5000 and C5074.
2.connect +3V_GFX to GPU ball AG9 with a 0.1uF cap C5075.
3.New add R5060 for test

4.L5001 change to bead 120ohm@100MHz (ESR=0.18ohm) 0603.
5.C5073 should be 4.7uF_X7R_0805.
6.C5072 should be 1uF_X7R_0603.
7.C5071 should be 0.1uF_X7R_0402.

8.PCIE change to PEX_TX0~7 and PEX_RX0~7 on GPU side for X8 lane configuration
9.unstuff R5009 and R5008 Q5002 stuff for test
9.delete L5002 for Nvidai recommend

Page 18

1.L5003 change to bead 30ohm (ESR=0.01) 0603.
2.C5085 change to 1uF_X7R_0603
3.Delete C5084.

Page 21

1.R5096 and R5103 change to 162ohm_1%.

Page 31

1.New add R5105 and R5106 2.2K pull up resistors to +3V for GPUT_CLK and GPUT_DATA on EC side.

2.Delete D20,Q25,D19,R500.

Page 20

1.delete R5081,R5082,R5082.

2.New add R5085 and R5086 10K pull down resistors to GFX_CORE_CNTRL0 and GFX_CORE_CNTRL1

3.Change R5047 to 5K pull up for ROM_SCLK

4.Change R5080 to 10K for JTAG_TRST# pull down.
5.R5084 can be no stuff for JTAG_TCK
6.New add Q5010 for AC/Batt# function.

7.New add Q5011.

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Size: C | Document Number: Change list | Rev: 2A

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