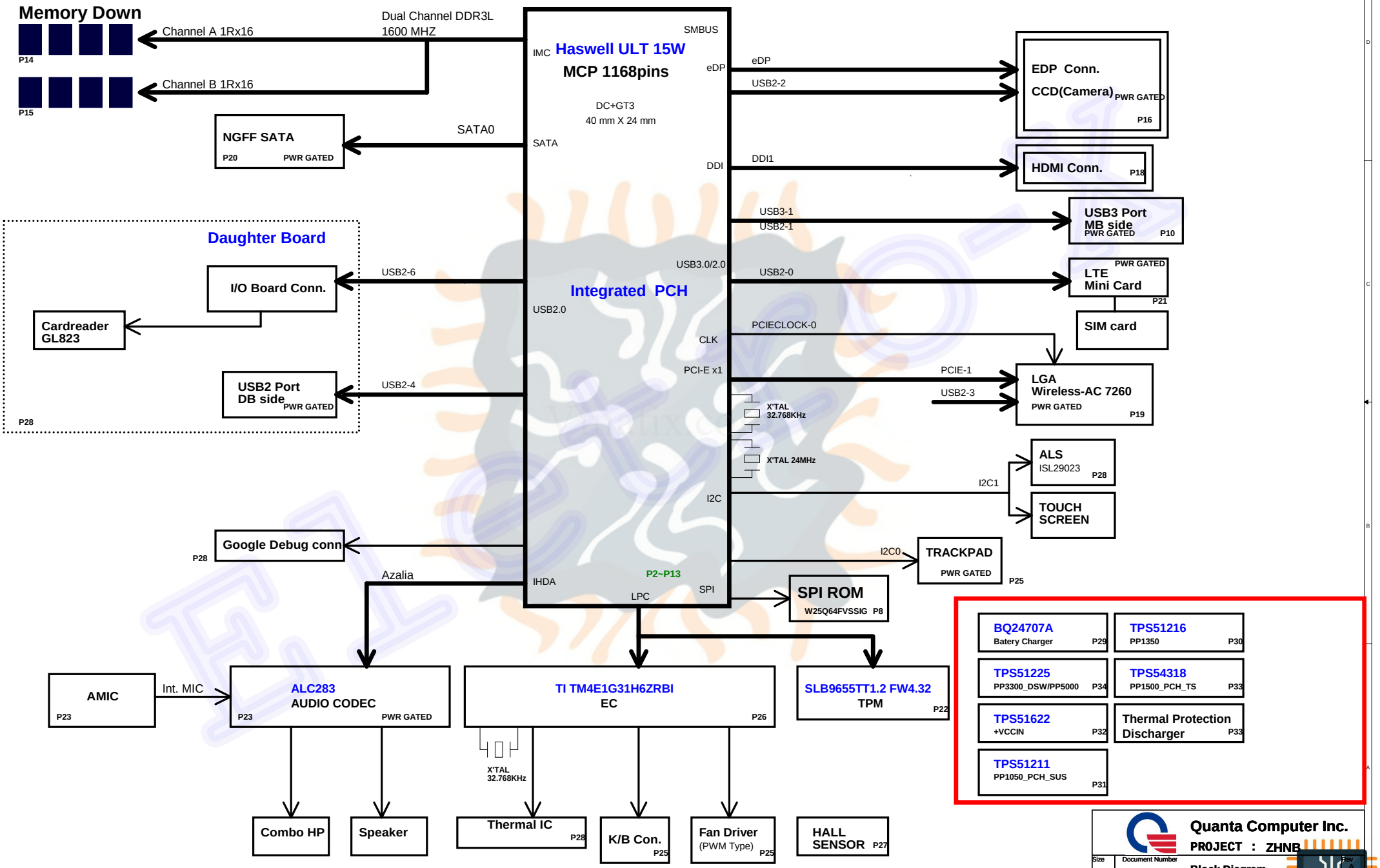
Benetton_EDU(ZHNB) SHB ULT SYSTEM BLOCK DIAGRAM

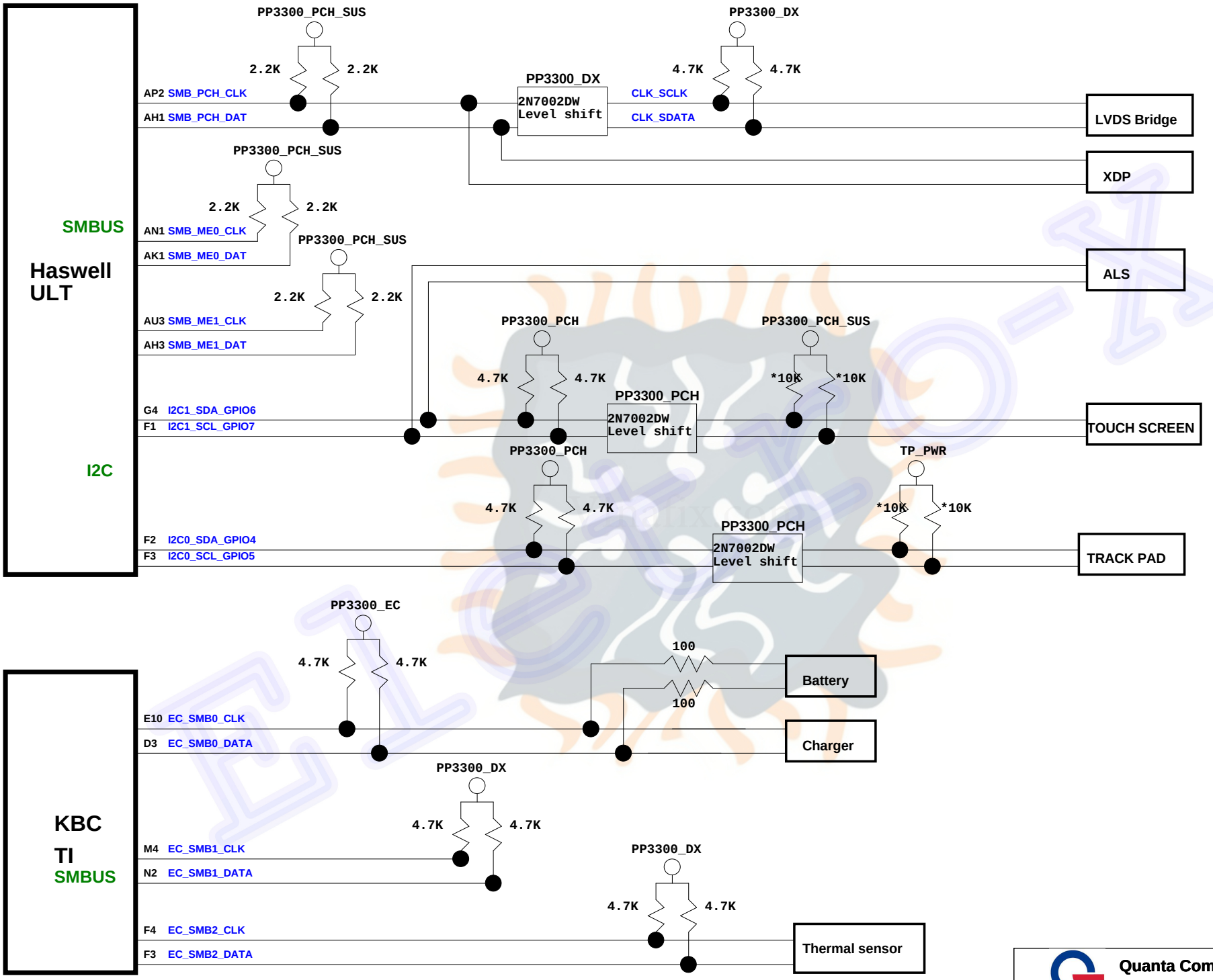
01



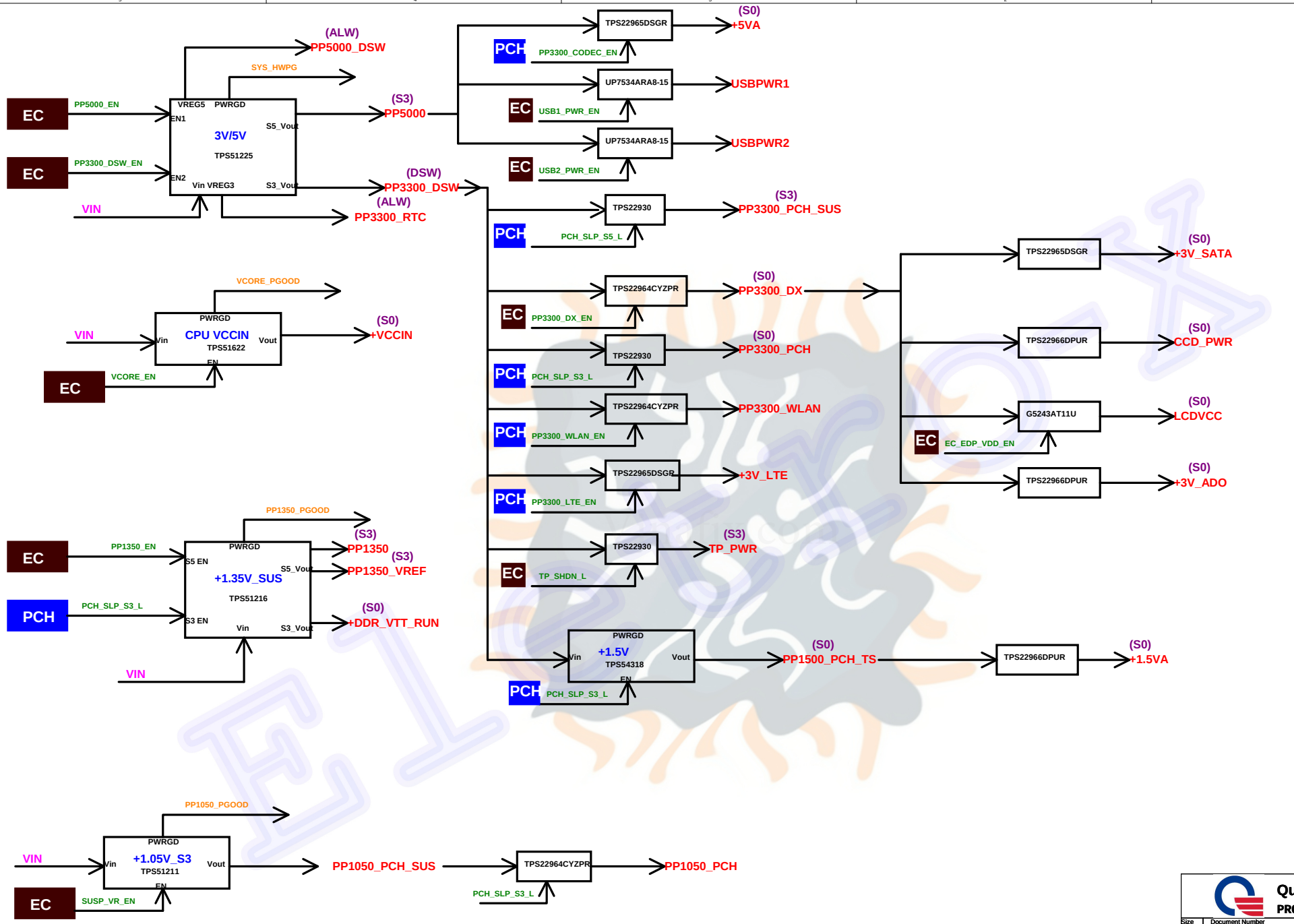
Quanta Computer Inc.

PROJECT : ZHNB

Size	Document Number	Rev
	Block Diagram	A
Date: Thursday, December 04, 2014	Sheet 1	of 39



Quanta Computer Inc.
PROJECT : ZHNB
Size | Document Number SMBUS_I2C | Rev A
Date: Thursday, December 04, 2014 Sheet 37 of 39



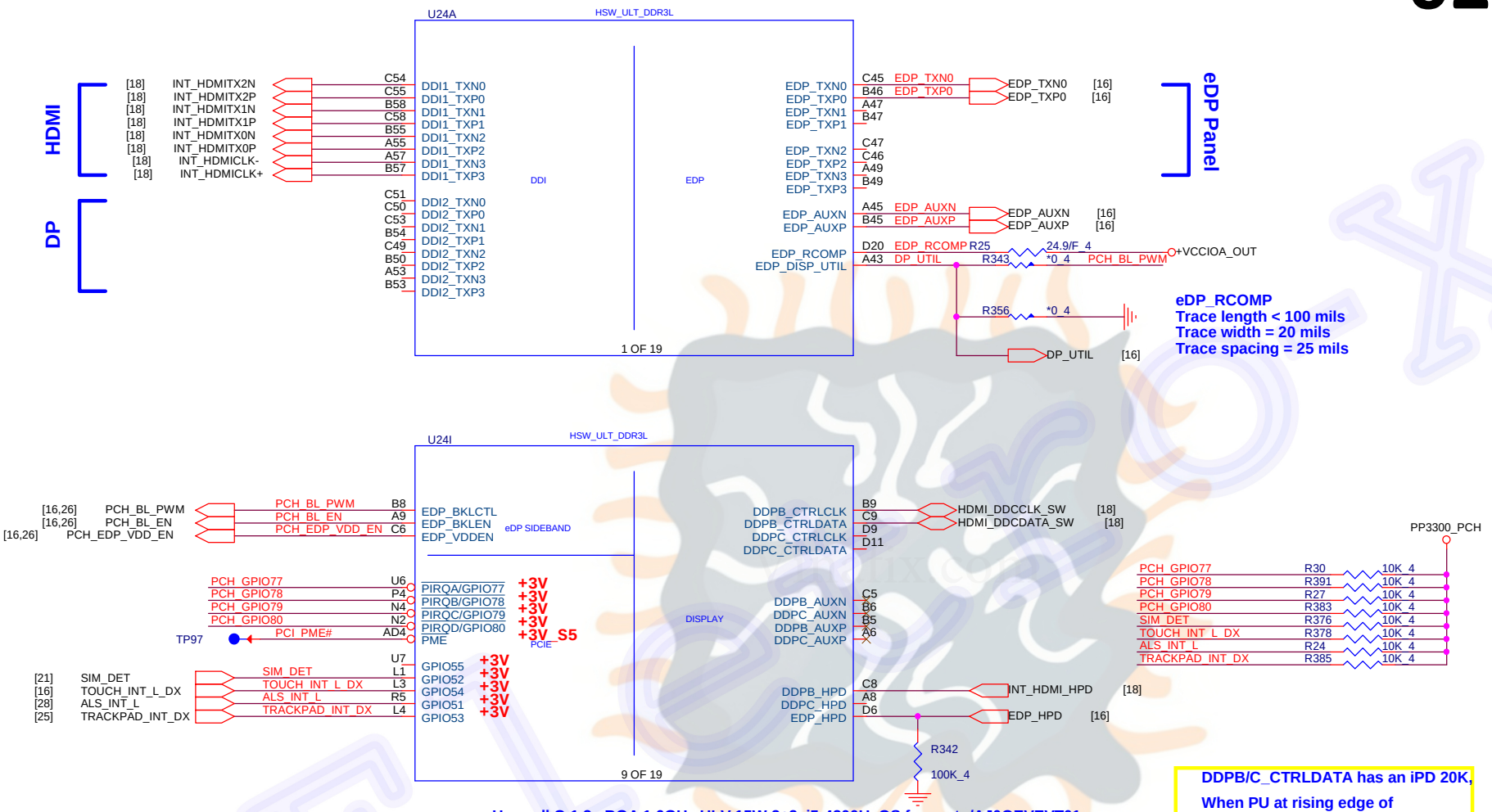
Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	ULT PWR CONTROL	A

Date: Thursday, December 04, 2014 Sheet 38 of 39

Haswell ULT (DISPLAY,eDP)

02

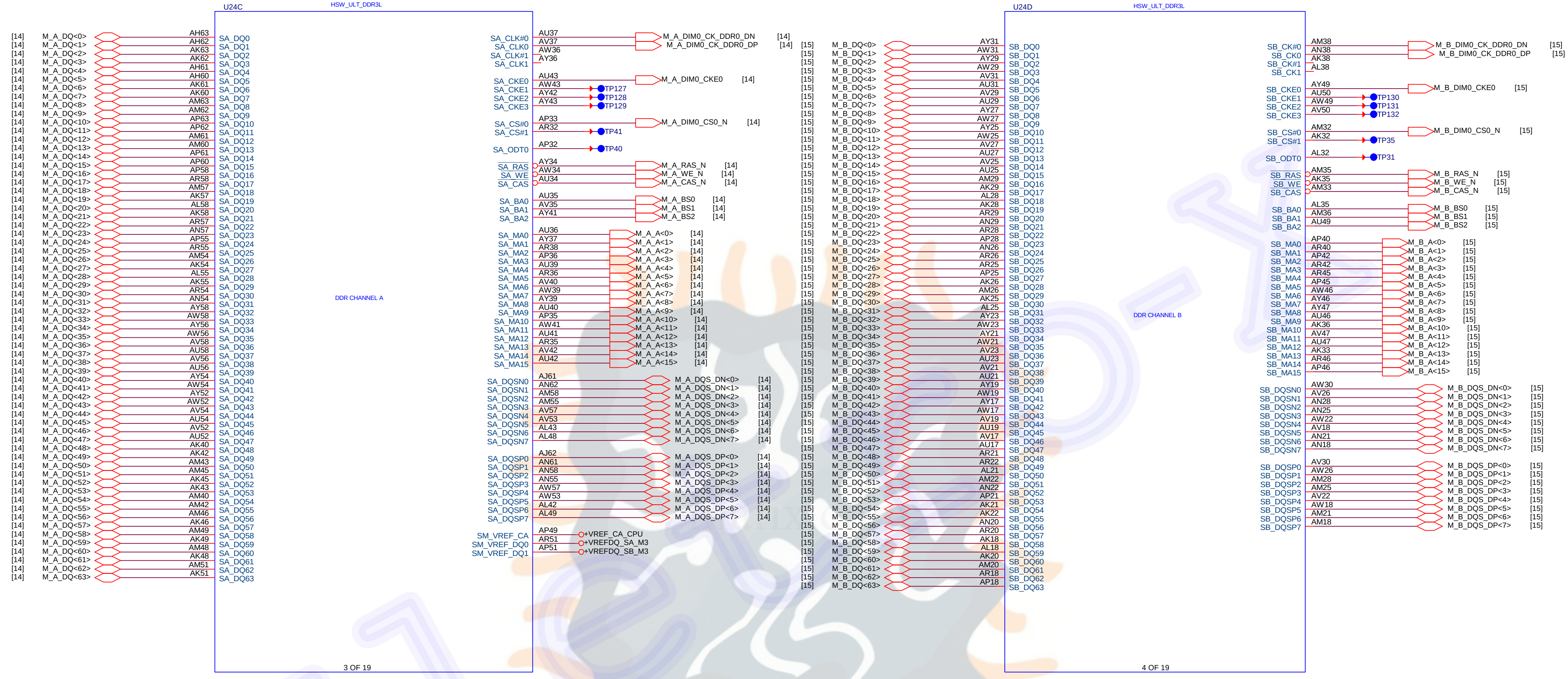


Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: Haswell 1/5 (DDI/eDP)	Rev A
Date: Thursday, December 04, 2014	Sheet 2 of 39	

Haswell ULT (DDR3L)

Haswell Processor (DDR3L)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SA_CKE3 AY43 TP129
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SA_ODT0 AP32 TP40
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SM_VREF_DQ1 AP51 +VREFDQ_SB_M3
3 OF 19
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4 OF 19

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PROJECT : ZHNB

Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	A

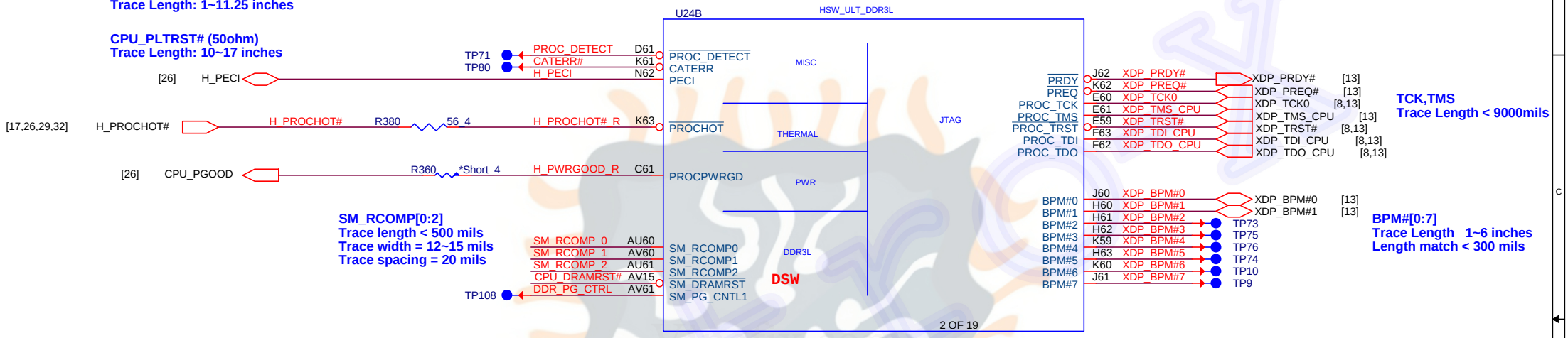
Date: Thursday, December 04, 2014 | Sheet 3 of 39

Haswell ULT (SIDEBAND)

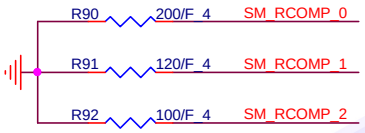
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

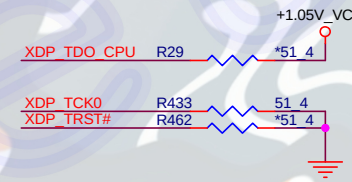
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



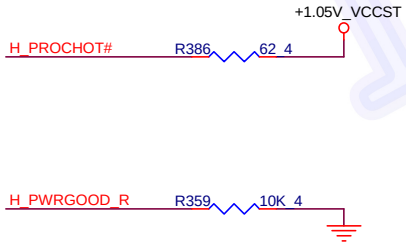
DRAM COMP



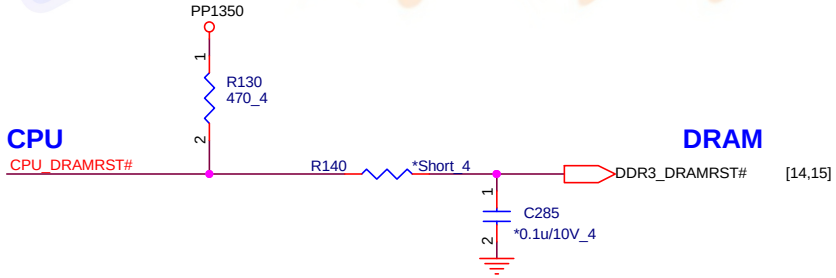
XDP PU/PD



PU/PD of CPU



DRAMRST



Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: Haswell 3/5 (SideBand)	Rev: A
Date: Thursday, December 04, 2014	Sheet 4 of 39	

Haswell ULT (POWER)

05

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

VCCST PWRGD

Quanta Computer Inc.

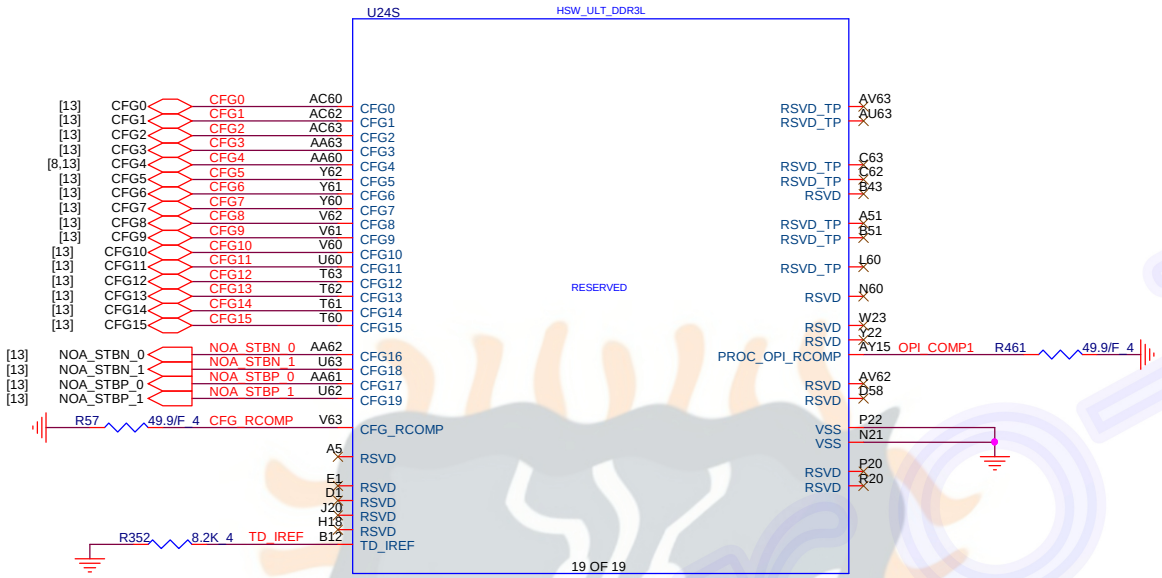
PROJECT : ZHNB

Size	Document Number	Rev
	Haswell 4/5 (POWER)	A

Date: Thursday, December 04, 2014 Sheet 5 of 39

Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R417 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R423 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K_4

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PROJECT : ZHNB

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	A

Date: Thursday, December 04, 2014 Sheet 6 of 39

Haswell ULT PCH (PM)

07

U24H HSW_ULT_DDR3L

SYSTEM POWER MANAGEMENT

8 OF 19

[26] PCH_SUSACK_L — R428 *0_4 — SUSACK#_R — AK2 SUSACK
[13,17] SYS_RESET# — SYS_RESET# — AC3 SYS_RESET
[5,13,26] SYS_PWROK — SYS_PWROK — C265 *1u/6.3V_4 — R421 *Short_4 — SYS_PWROK_R — AG2 SYS_PWROK
PCH_PWROK — R482 *Short_4 — PCH_PWROK_R — AY7 PCH_PWROK
APWROK_R — AB5 APWROK
PCI_PLTRST# — AG7 PLTRST

+3V_S5

[26] PCH_RSMRST_L — R478 *Short_4 — PCH_RSMRST# — AW6 RSMRST
[26] PCH_SUSWARN_L — R453 *0_4 — PCH_SUSPWRACK — AV4 SUSWARN/SUSPWRDNACK/GPIO30
[26] PCH_PWRBTN_L — R147 *Short_4 — PCH_PWRBTN# — AL7 PWRBTN
[29] ACPRESENT — R61 *Short_4 — PCH_ACPRESENT — AJ8 ACPRESENT/GPIO31
PCH_BATLOW# — AN4 BATLOW/GPIO72
[13,26] PCH_SLP_S0_L — R415 *Short_4 — PCH_SLP_S0#_R — AF3 SLP_S0
TP37 — AM5 SLP_WLAN/GPIO29

+3V_S5
DSW
+3V_S5
DSW
+3V_S5
DSW

PCH_SUSPWRACK — R427 0_4 — SUSACK#_R

4/22 modify, default skip EC control

DSWVRMEN
DPWROK
WAKE

Deep Sx

AW7 DSWVREN — DSWVREN [8]
AV5 DPWROK_R — R477 *Short_4 — PCH_DPWROK [26]
AJ5 PCIE_PCH_WAKE# — R74 *Short_4 — PCH_WAKE_L [26]

DSW

CLKRUN/GPIO32
SUS_STAT/GPIO61
SUSCLK/GPIO62
SLP_S5/GPIO63

V5 CLKRUN# R38 *Short_4 LPC_CLKRUN_L — LPC_CLKRUN_L [26]
AG4 PCH_SUS_STAT — TP27
AE6 PCH_SUSCLK — PCH_SUSCLK [19]
AP5 PCH_SLP_S5_L — PCH_SLP_S5_L [13,26,30,35]

DSW
DSW
DSW
DSW
DSW
DSW

SLP_S4
SLP_S3
SLP_A
SLP_SUS
SLP_LAN

AJ6 PCH_SLP_S4_L — PCH_SLP_S4_L [13]
AT4 PCH_SLP_S3_L — PCH_SLP_S3_L [13,26,30,31,33,35]
AL5 PCH_SLP_A_L — PCH_SLP_A_L [13]
AP4 PCH_SLP_SUS_L — PCH_SLP_SUS_L [26,35]
AJ7 PCH_SLP_LAN# — TP38

PCH PM PU/PD

PP3300_PCH
CLKRUN# R37 8.2K_4
SYS_RESET# R406 10K_4

PCH_RSMRST# R479 10K_4
SYS_PWROK R80 *10K_4
DPWROK_R R473 100K/F_4

PP3300_PCH_SUS
PCH_SUSPWRACK R454 10K_4
SYS_PWROK R426 *1K_4

PP3300_DSW
PCH_ACPRESENT R62 10K_4
PCH_BATLOW# R444 8.2K_4
PCIE_PCH_WAKE# R75 10K_4
PCH_PWRBTN# R151 *10K_4

PCH PWROK

[5,26] PCH_PWROK — PCH_PWROK — R483 *Short_4 — PCH_PWROK_R
R487 100K_4
PCH_RSMRST — R474 *0_4 — DPWROK_R

Non Deep Sx

PLTRST# Buffer

PCI_PLTRST# — R152 *Short_4 — PLTRST#
PP3300_PCH
C94 *0.1u/10V_4
U6 *TC7SH08FU
PCI_PLTRST# — PLTRST# [13,19,21,22,26]
R155 100K_4

4/22 modify, default is bypass PLTRST#

Quanta Computer Inc.
PROJECT : ZHNB

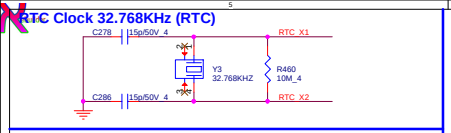
Size	Document Number	Rev
	PCH 1/6 (PM)	A
Date: Thursday, December 04, 2014	Sheet 7 of 39	

Haswell ULT PCH (RTC/HDA/SATA/SPI)

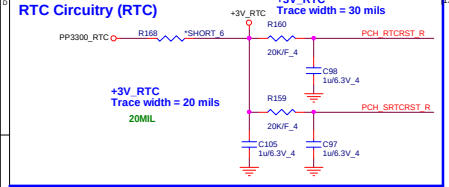
Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

08

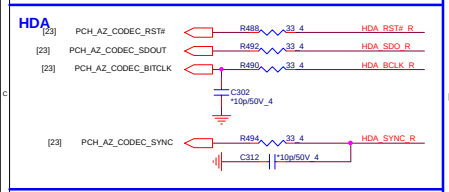
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)



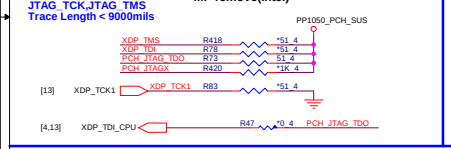
HDA



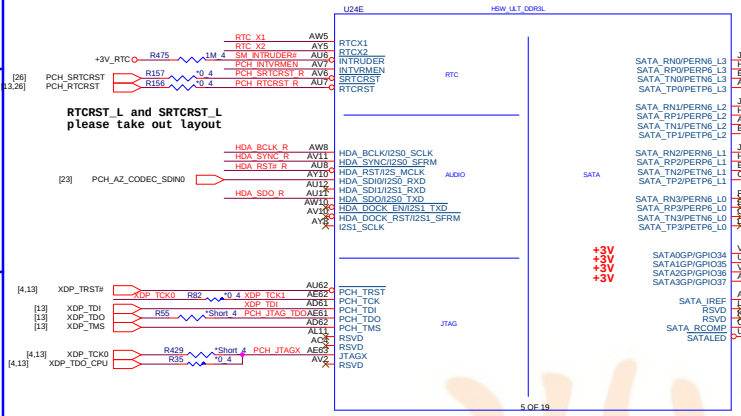
PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

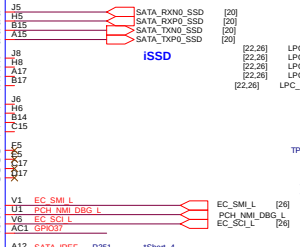
MP remove(Intel)



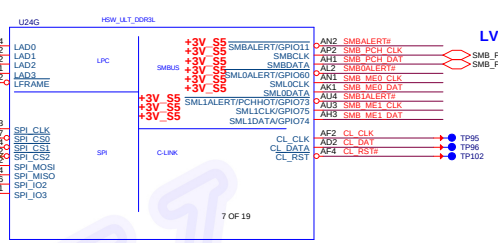
RTCRST_L and SRTCRST_L please take out layout



iSSD

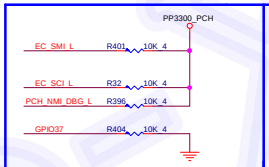


LVDS Bridge

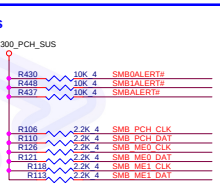


SATA_RCOMP

Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

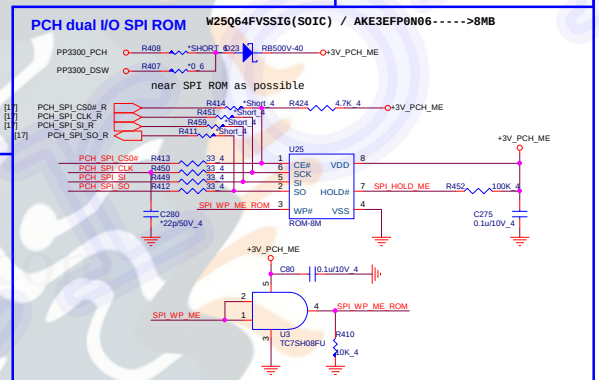


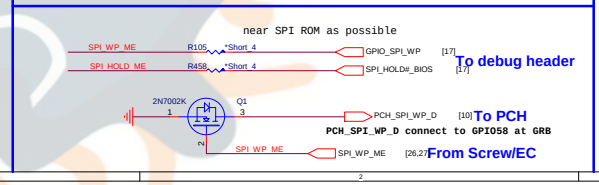
SMBus



PCH dual I/O SPI ROM

W25Q64FVSSIG(SOIC) / AKE3EFP0N06------>8MB

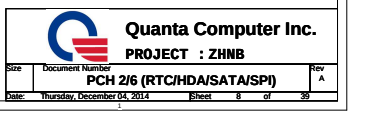




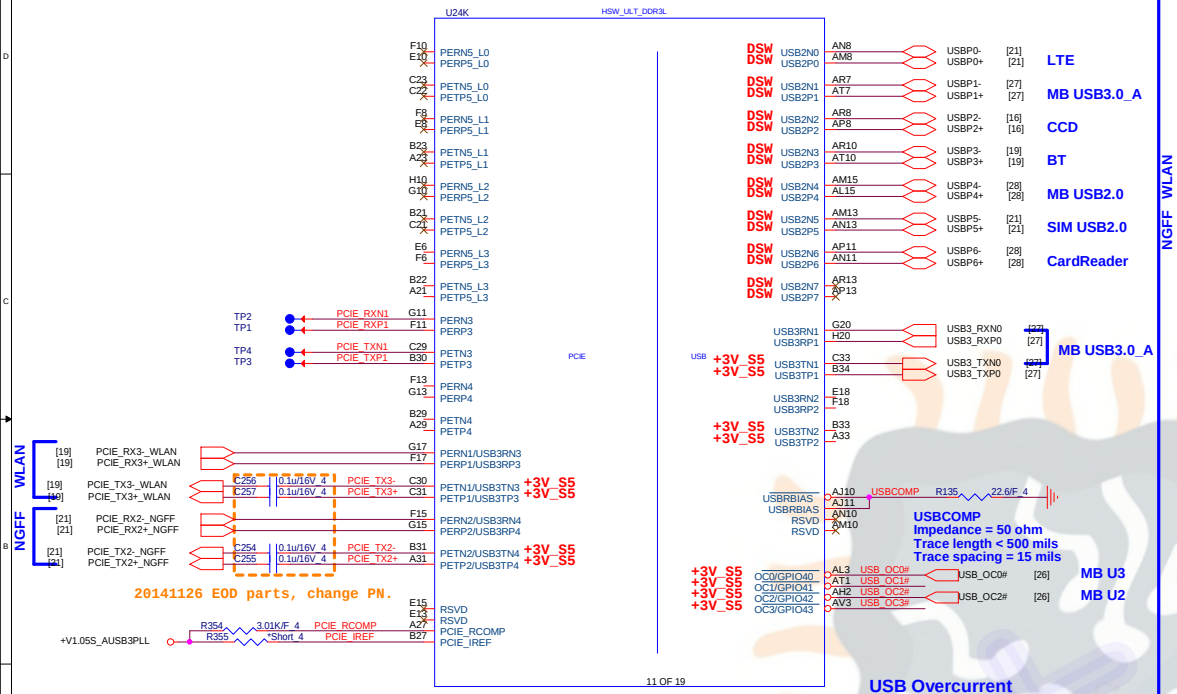
ULT Strapping Table

Note: R493 need stuff on MP.

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	PP3300_PCH R400 *1K_4 SPKR SPKR [10,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R493 *0_4 PCH_HDA_SDO [26]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R484 330K_4 PCH_INTVRMEN R485 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	[10] GPIO66 PP3300_PCH R330 *1K_4 GPIO66 R340 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	[10] GPIO86 PP3300_PCH R1 *1K_4 GPIO86 R7 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	[10] GPIO15 PP3300_PCH_SUS R50 *8.2K_4 GPIO15 R58 *1K_4 x86 stuff
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	[6,13] CFG4 CFG4 R64 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	[7] DSWVREN +3V_RTC R476 330K_4 DSWVREN R472 *330K_4



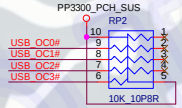
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



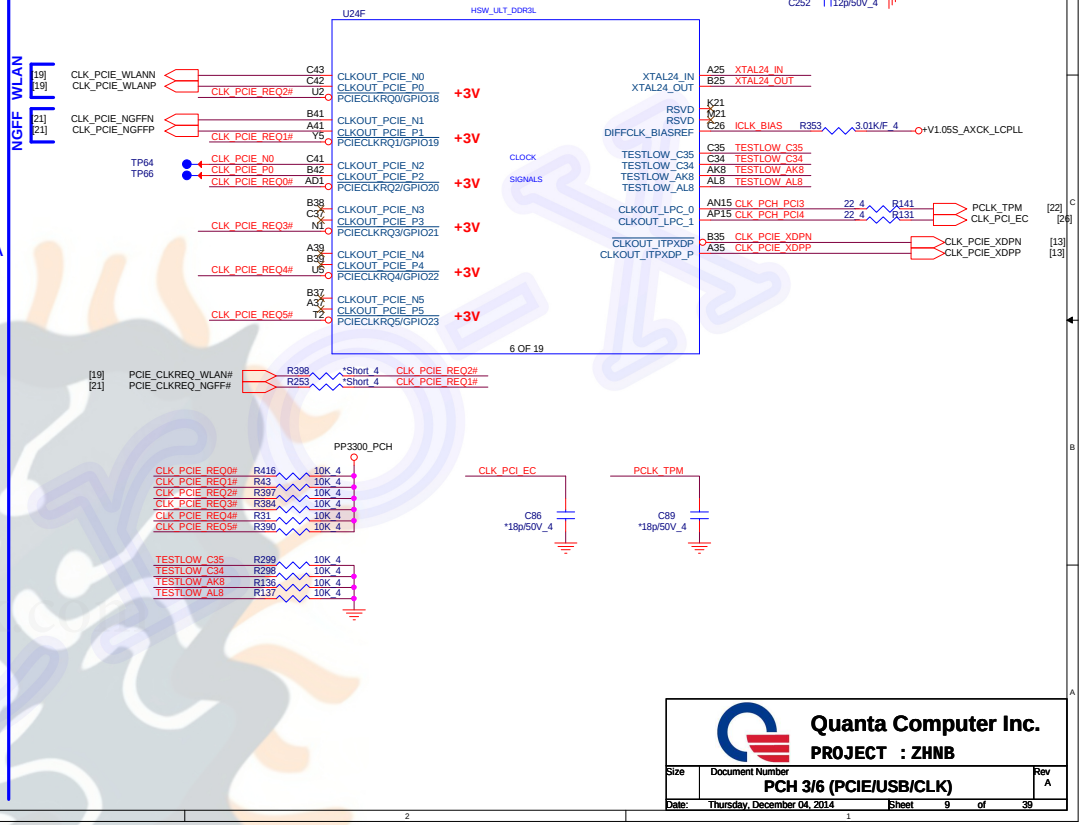
20141126 EOD parts, change PN.

USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

USB Overcurrent



Haswell ULT PCH (CLOCK)



09

Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U24J — HSW_ULT_DDR3L — 10 OF 19

PCH GPIO PU/PD

4/23 modify, those 3 power enable pin are PD 100K already

4/23 modify, follow Intel suggestion to un-stuff for unused GPIO

LTE_DISABLE_L need PU to +3V_LTE

6/24 Connect DEVSLP0 to SSD.

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

RAM ID

Vender	RAM_ID ID2	ID1	ID0	Q PN	Mfr. PN	Freq.
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(4G)	0	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(2G)	1	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz

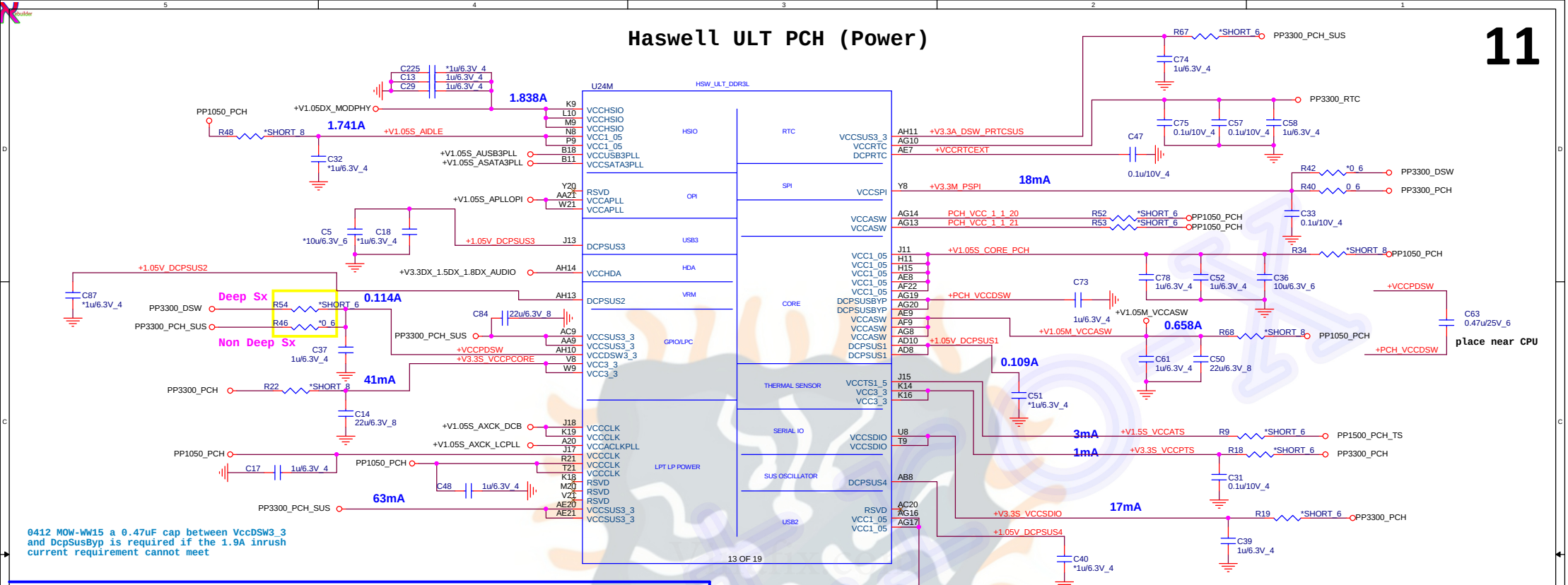
CPU thermal trip

Q11 FDV301N — Q12 MMBT3904-7-F — U23 74AUP1G07GW — Q23 2N7002DW

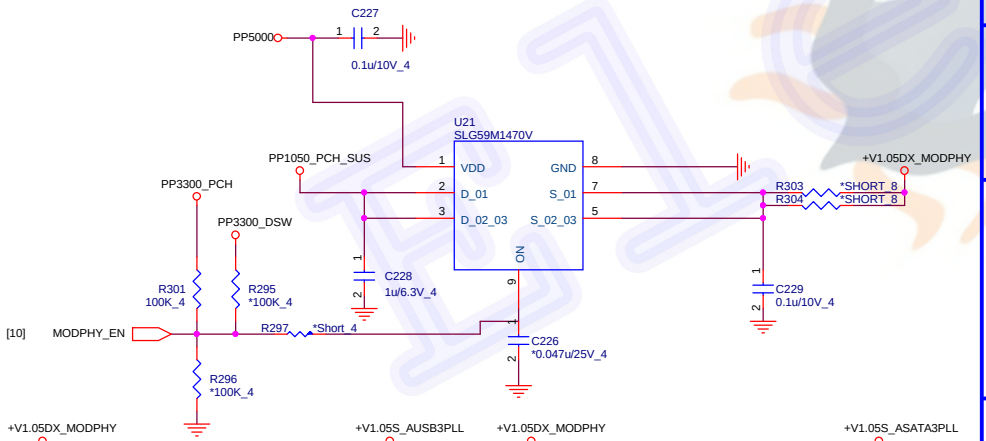
Quanta Computer Inc.	
PROJECT : ZHNB	
Size	Document Number: PCH 4/6 (GPIO/MISC) — Rev
Date: Thursday, December 04, 2014	Sheet 10 of 39

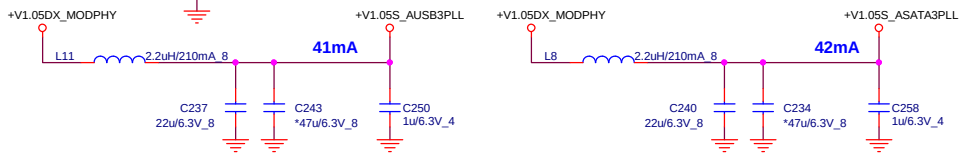
Eletro-X

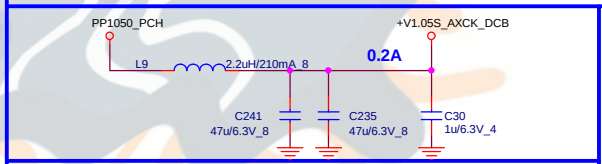
Haswell ULT PCH (Power)



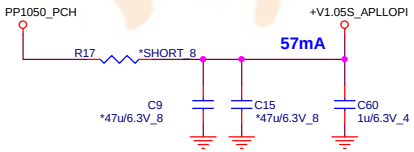
PCH VCCHSIO Power



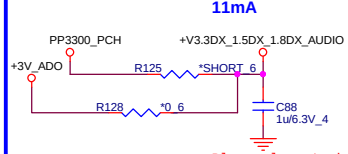


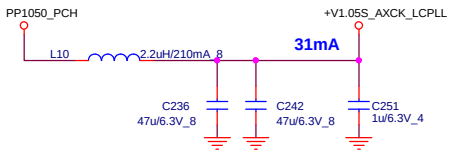


VCCAPLL power



PCH HDA Power

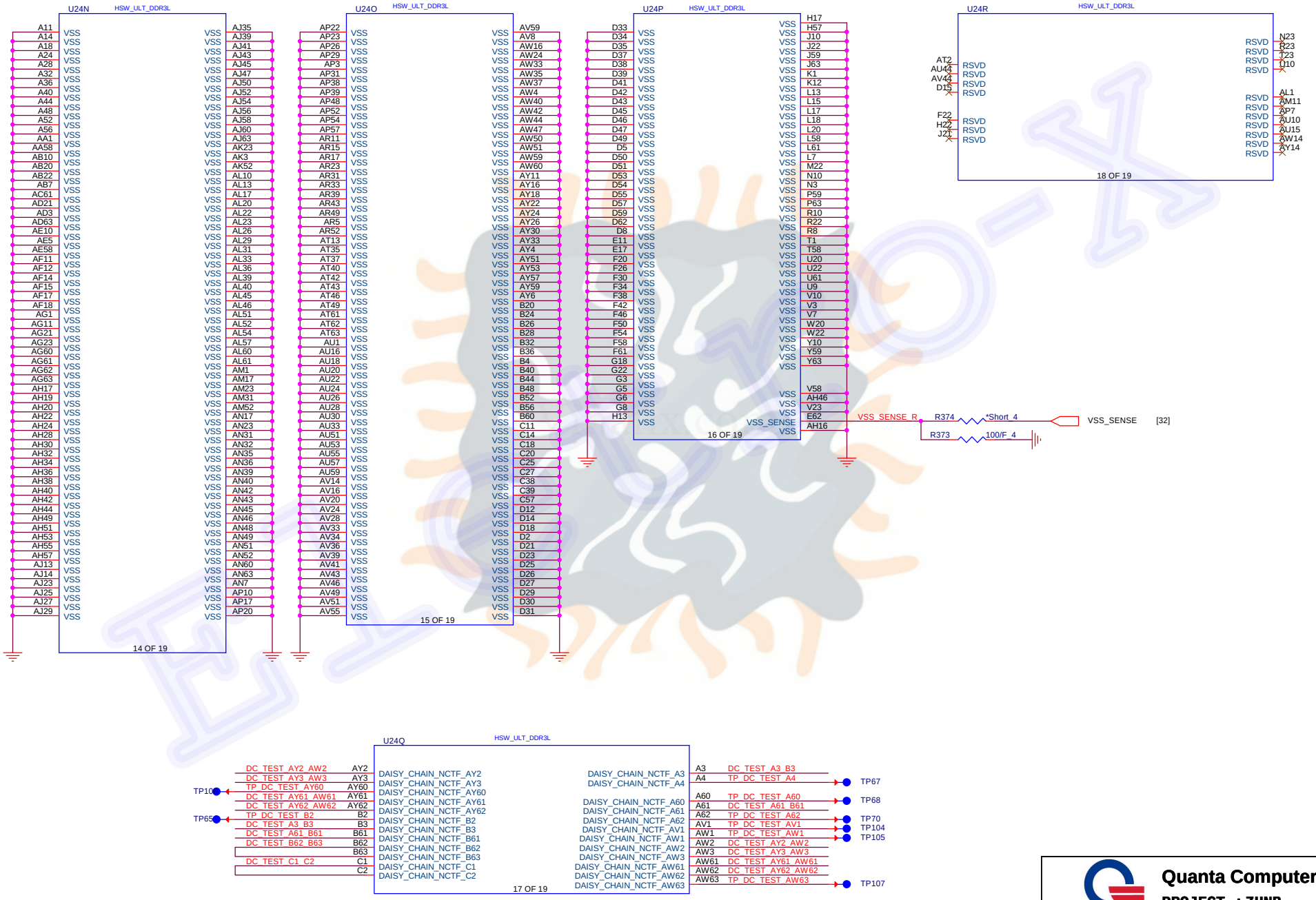




Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	PCH 5/6 (POWER)	
Date: Thursday, December 04, 2014	Sheet 11 of	

Haswell ULT (GND)

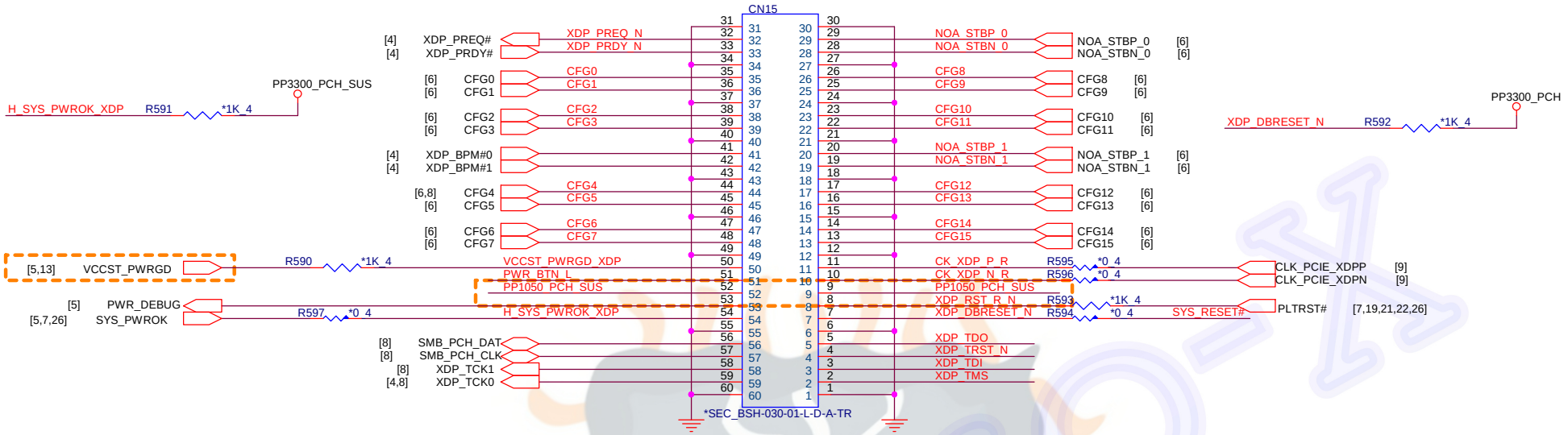


Quanta Computer Inc.

PROJECT : ZHNB

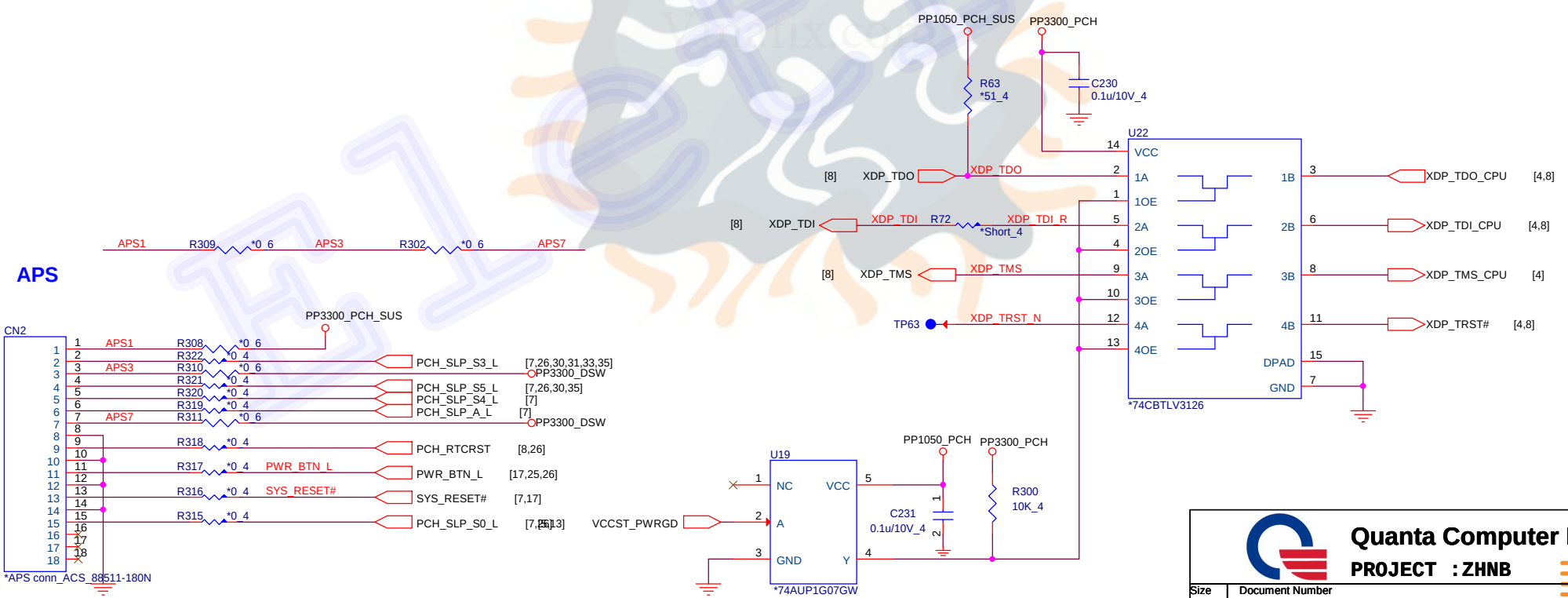
Size	Document Number	Rev
	PCH 6/6 (GND)	A

Date: Thursday, December 04, 2014 Sheet 12 of 39



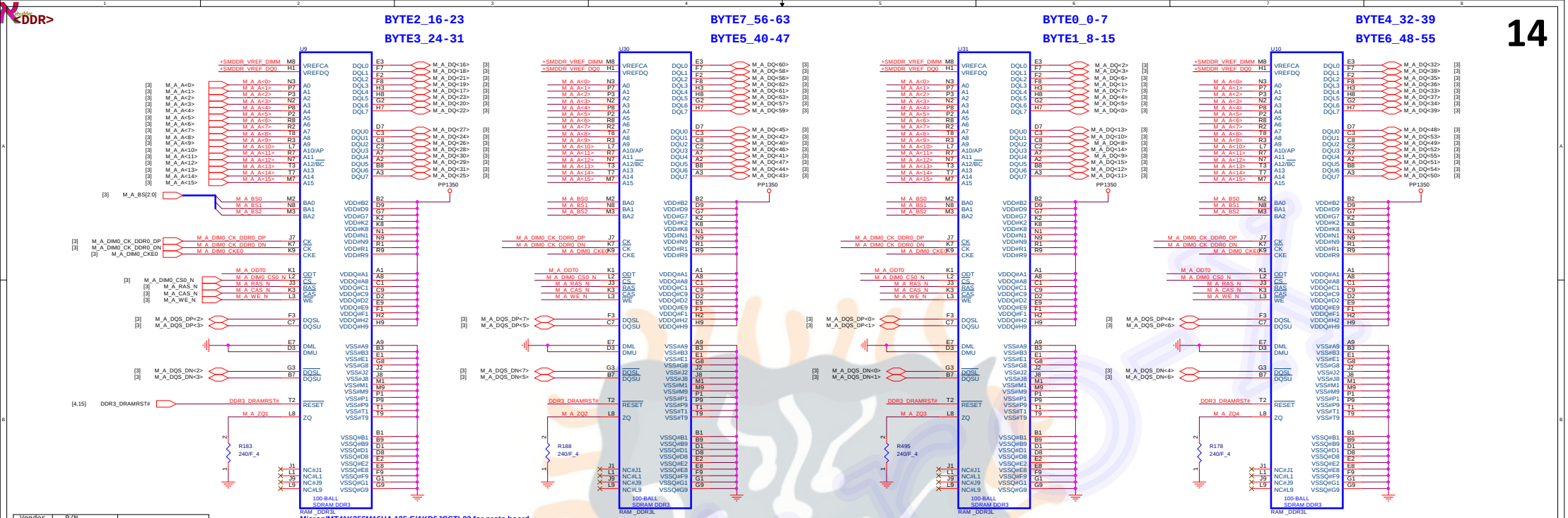
20141021 Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.

APS



Quanta Computer Inc.			
PROJECT : ZHNB			
Size	Document Number		Rev
	CPU/PCH XDP		A
Date: Thursday, December 04, 2014	Sheet 13 of 39		

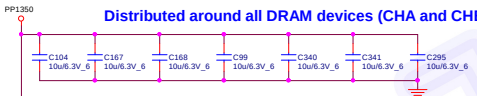
BYTE2_16-23
BYTE3_24-31
BYTE7_56-63
BYTE5_40-47
BYTE0_0-7
BYTE1_8-15
BYTE4_32-39
BYTE6_48-55



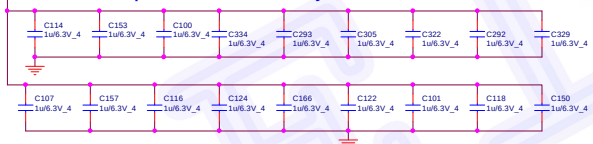
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

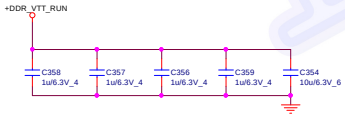
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

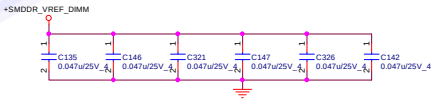
Distributed around all DRAM devices (CHA and CHB)

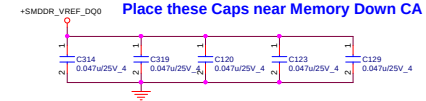


Place these Caps near each X16 Memory Down

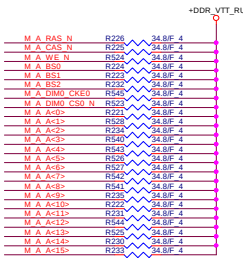


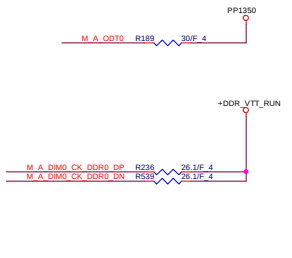




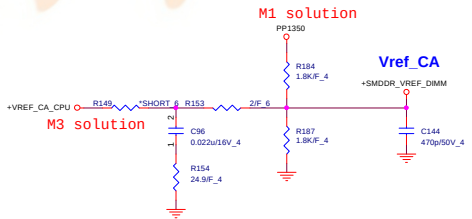


Place these Caps near Memory Down CA & DQ pin

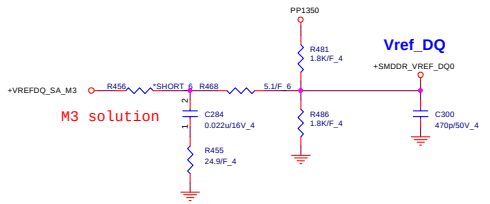




M1 solution



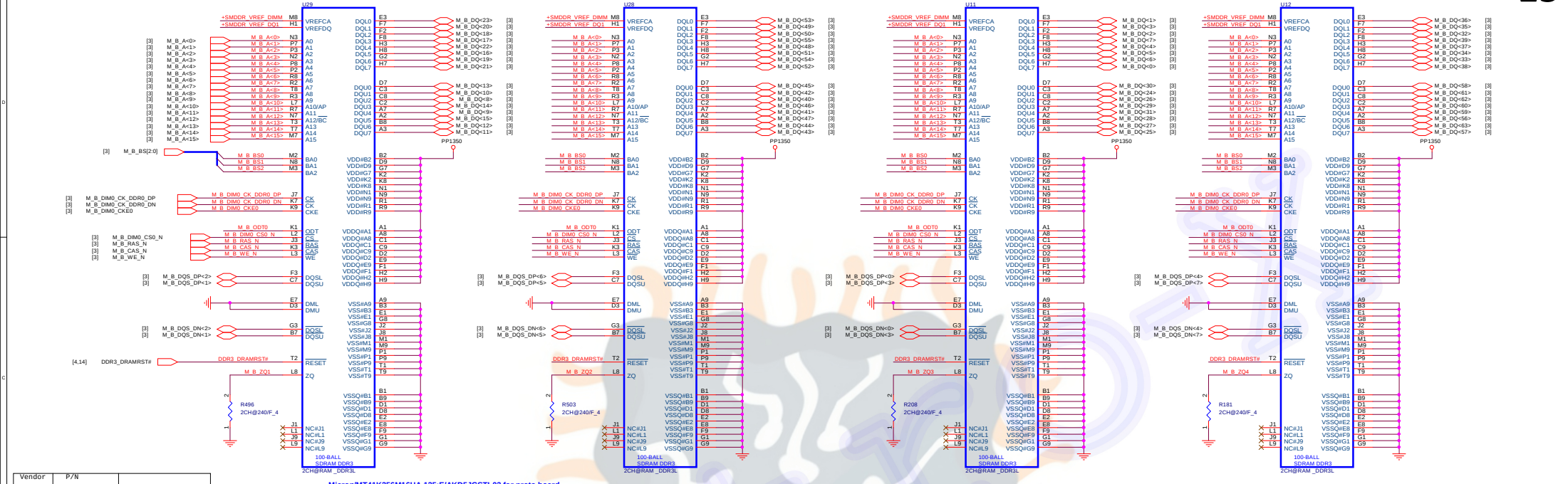
M1 solution



S_CLIP1 *SUL-12A2M
S_CLIP3 *SUL-12A2M
S_CLIP2 *SUL-12A2M
S_CLIP4 *SUL-12A2M

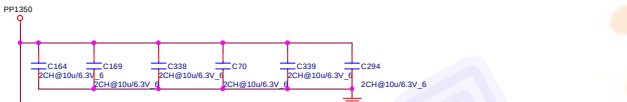
Quanta Computer Inc.
PROJECT : ZHNB
Size | Document Number | DDR3L MEMORY DOWN16 A
Date: Thursday, December 04, 2014 | Sheet

BYTE1_8-15
BYTE2_16-23
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE7_56-63

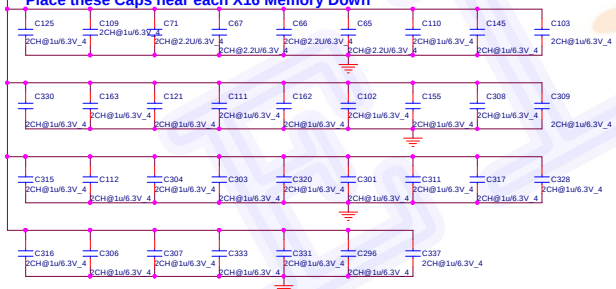


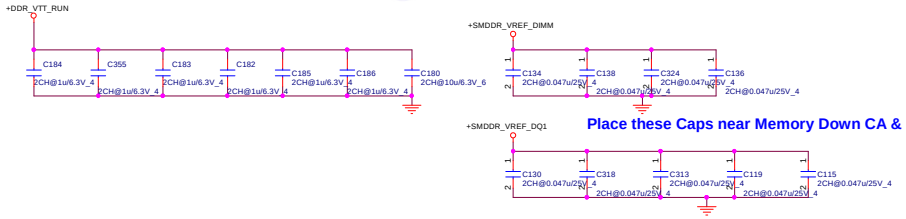
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST407	DDR3L 1600Mhz 4Gb
Micron	AKD5JGSTL10	DDR3L 1600Mhz 4Gb

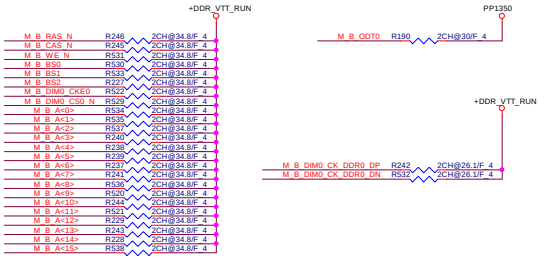


Place these Caps near each X16 Memory Down

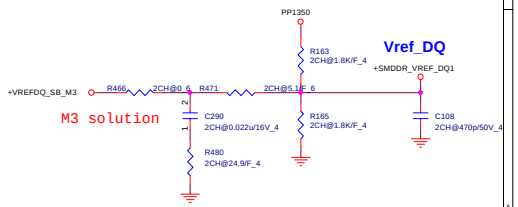




Place these Caps near Memory Down CA & DQ pin

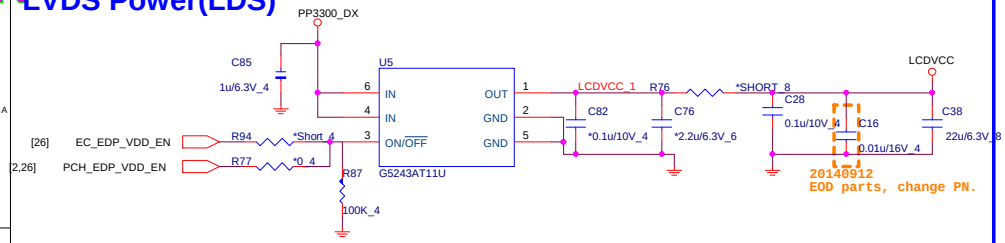


M1 solution



Quanta Computer Inc.
PROJECT : ZHN
Size | Document Number | DDR3L MEMORY DOWNx16 B
Date: Thursday, December 04, 2014 | Sheet

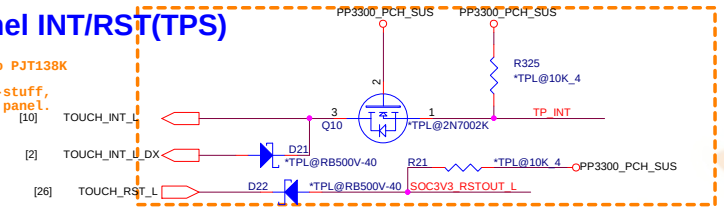
LVDS Power(LDS)



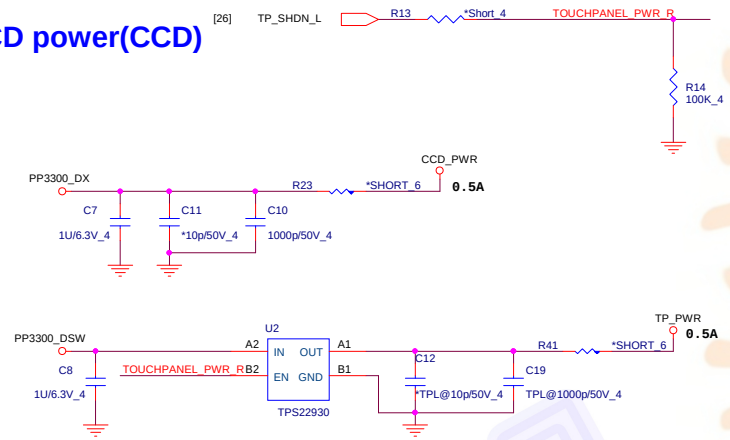
20140912
EOD parts, change PN.

Touch Panel INT/RST(TPS)

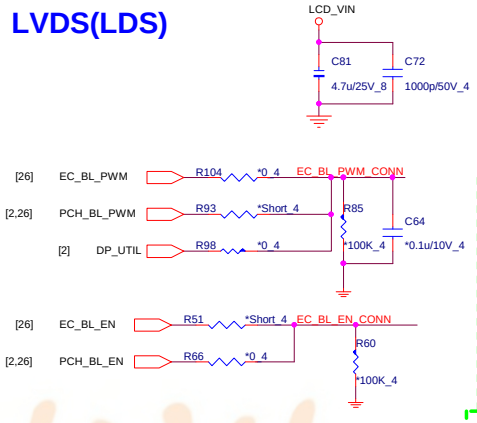
20140821
Q13 FET change to PJT138K
20141125
Change TPS to un-stuff,
because no touch panel.



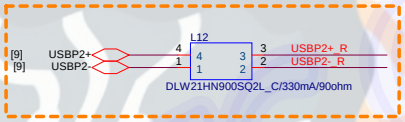
CCD power(CCD)



LVDS(LDS)



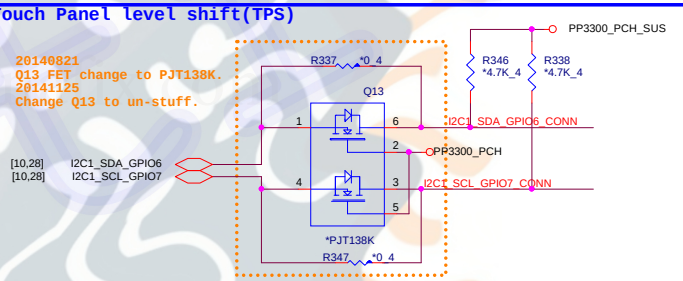
CCD(CCD)



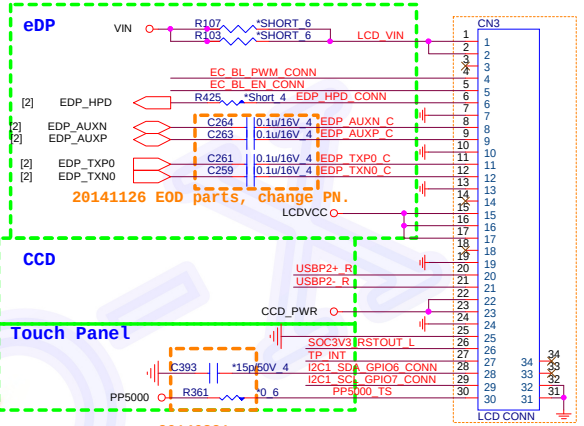
20141201 Stuff L12, remove R371/R372.

Touch Panel level shift(TPS)

20140821
Q13 FET change to PJT138K.
20141125
Change Q13 to un-stuff.



eDP



20141126 EOD parts, change PN.

CCD

Touch Panel

20140821
Reserve C393 capacitor.
20141125
Change R361 to un-stuff.
because no touch panel.

20140827 Change CN3 footprint.

16

LVDS CONN (follow zqk)
DFHS40FS095
DFHS40FS063
footprint gs12401-1011-40p-r-nh-smt

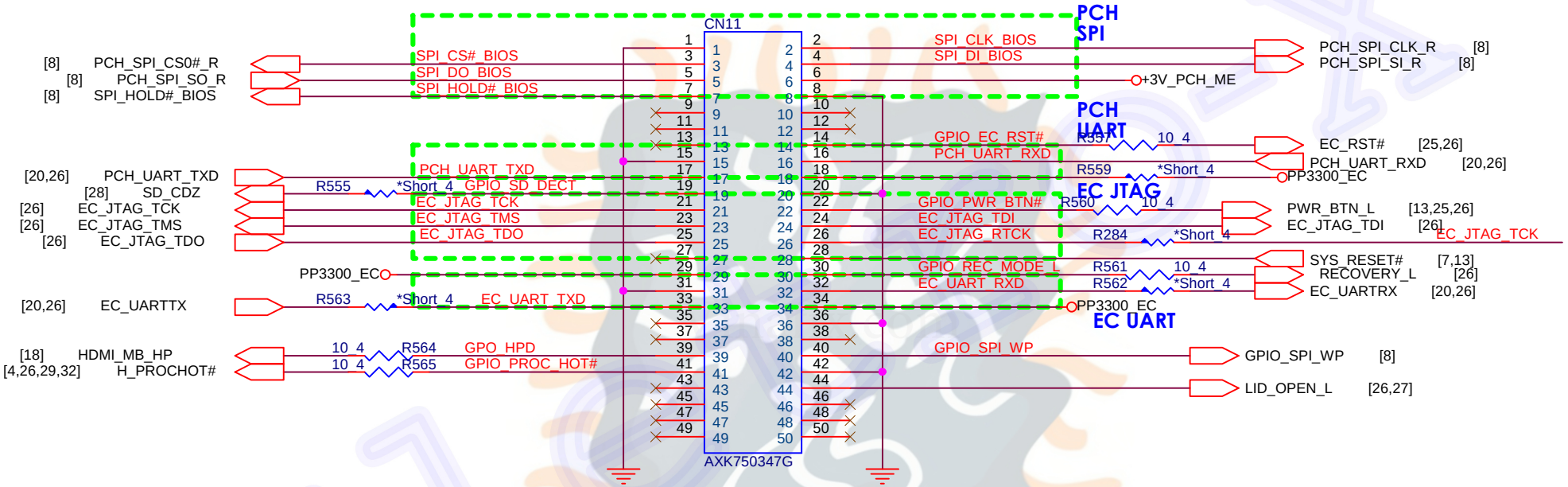
Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	A

Date: Thursday, December 04, 2014 Sheet 16 of 39

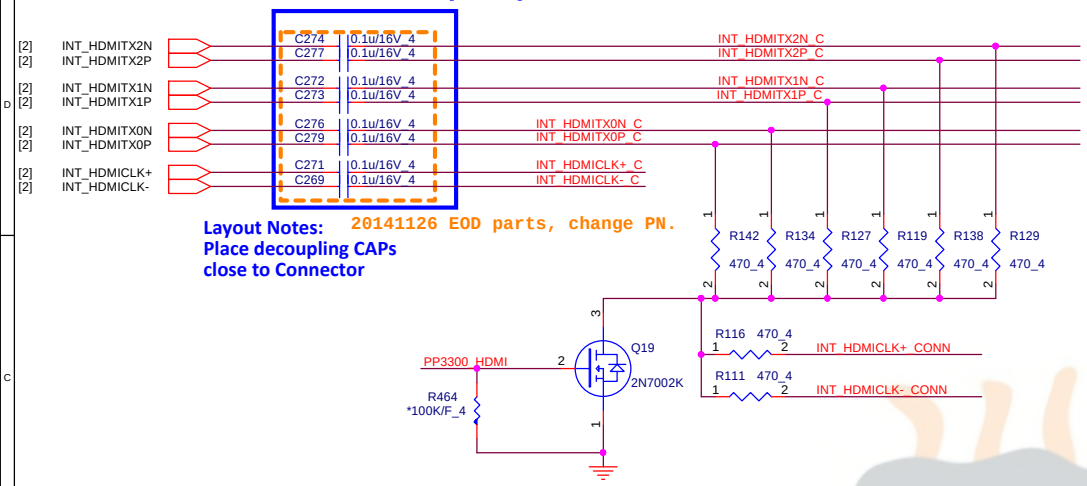
Debug Port(DBG)

```
PIN7 OD      PIN39 OD   PIN49 OD
PIN14 OD     PIN41 OD   PIN50 OD
PIN19 OD     PIN43 OD
PIN22 OD     PIN44 OD
PIN28 OD     PIN45 OD
PIN30 OD     PIN46 OD
PIN37 OD     PIN47 OD
PIN38 OD     PIN48 OD
```



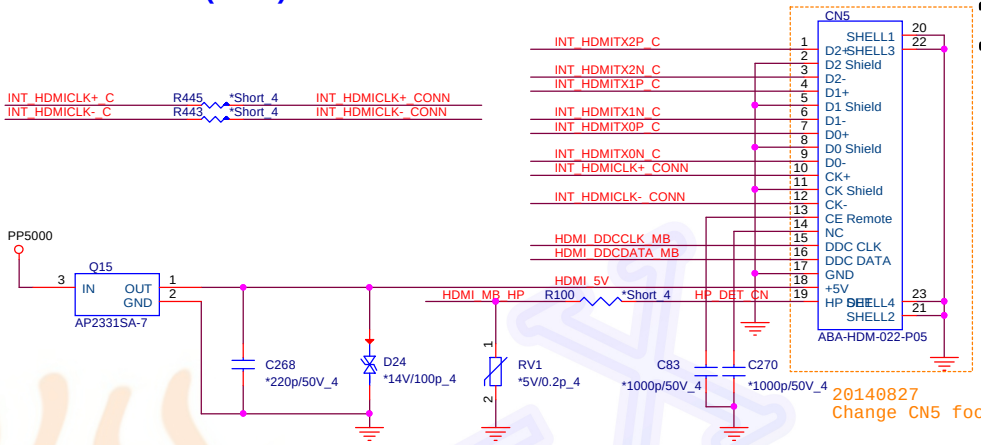
Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: Google Debug	Rev: A
Date: Thursday, December 04, 2014	Sheet 17 of 39	

HDMI Cost Reduced level shift (HDM)



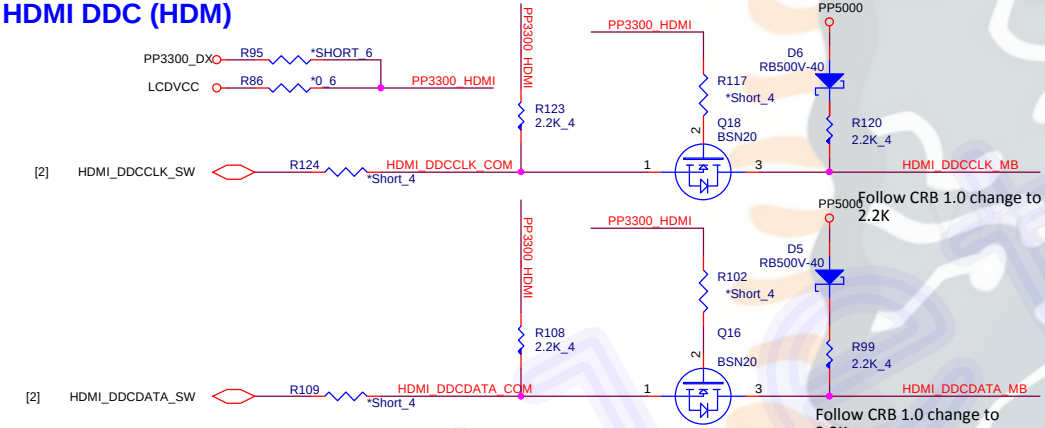
Layout Notes: 20141126 EOD parts, change PN.
Place decoupling CAPs close to Connector

HDMI connector (HDM)

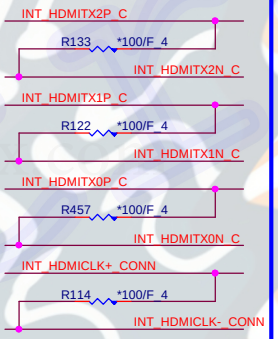


20140827
Change CN5 footprint.

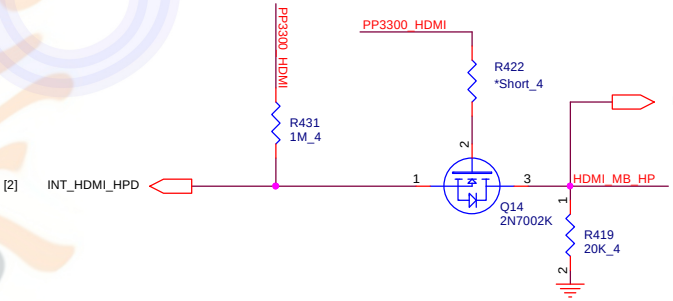
HDMI DDC (HDM)



EMI (EMC)

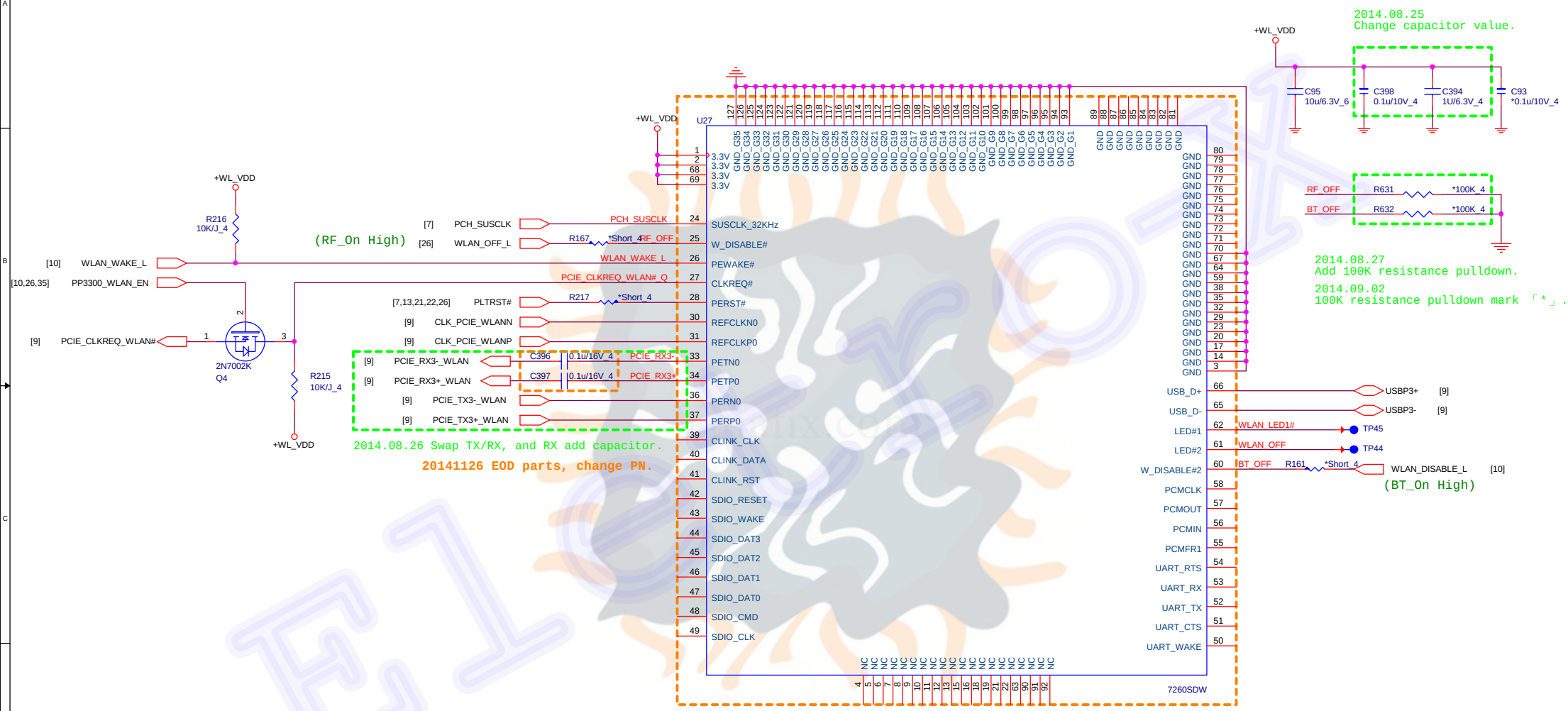


HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	HDMI	A
Date: Thursday, December 04, 2014	Sheet 18 of 39	

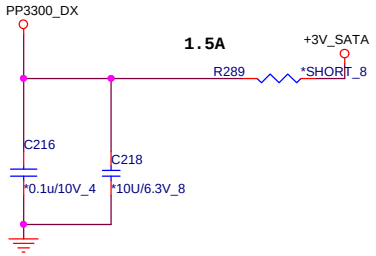


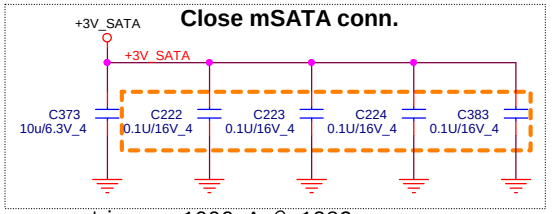
20140820 On board IC change to same as ZS8 connector
20140822 Return to another wifi onboard module 7260SDW
20140826 Change wifi onboard module 7260SDW footprint
20140909 Change wifi onboard module 7260SDW footprint
20141014 Change wifi onboard module 7260SDW PN.

Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number	Rev
	WIFI / BT	A
Date: Thursday, December 04, 2014	Sheet 19	of 38

NGFF SSD connector.

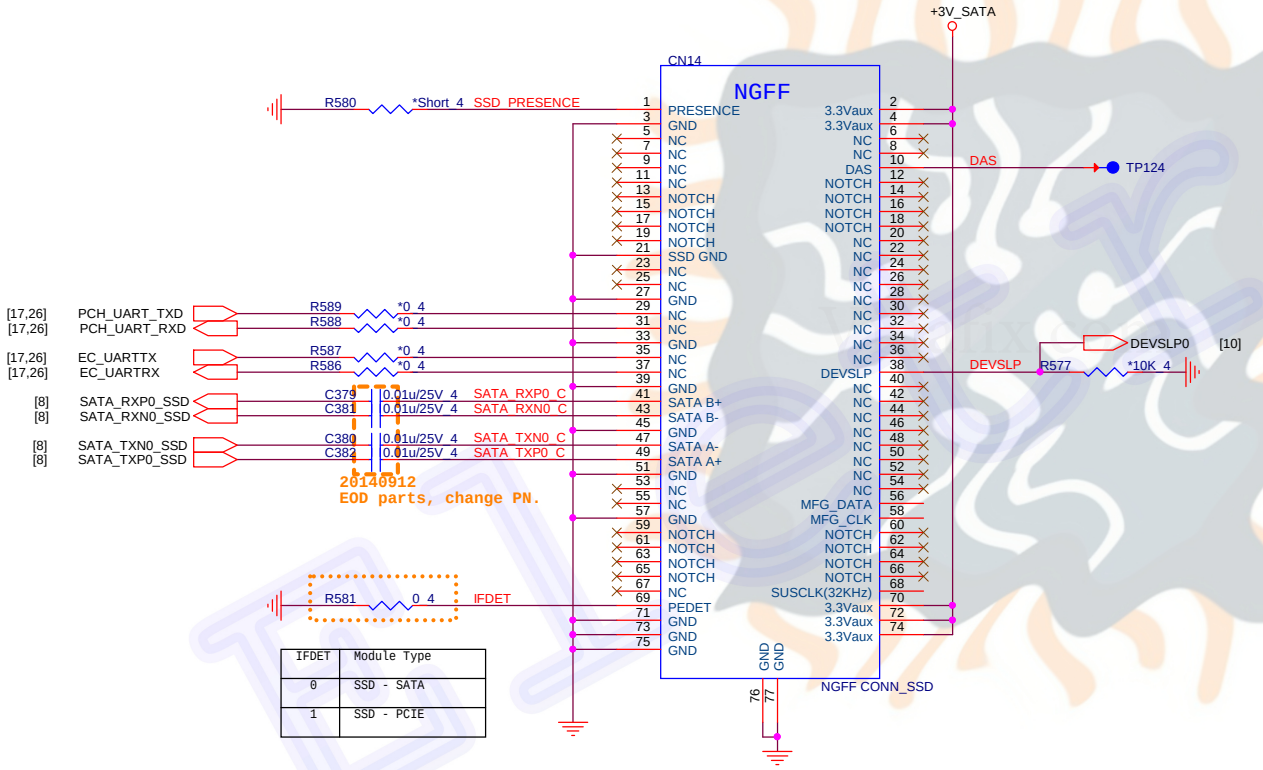
San Disk SSD Card.





20141126 EOD parts, change PN.

rating = 1000mA @ 128G



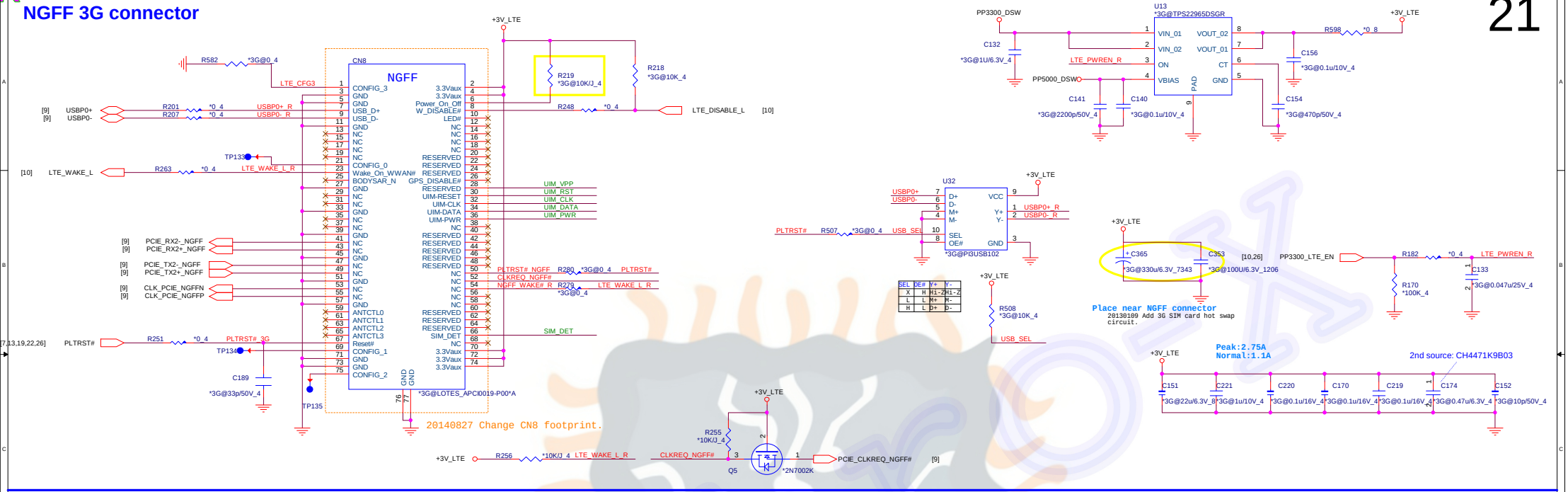
IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE

Quanta Computer Inc.

PROJECT : ZHNB

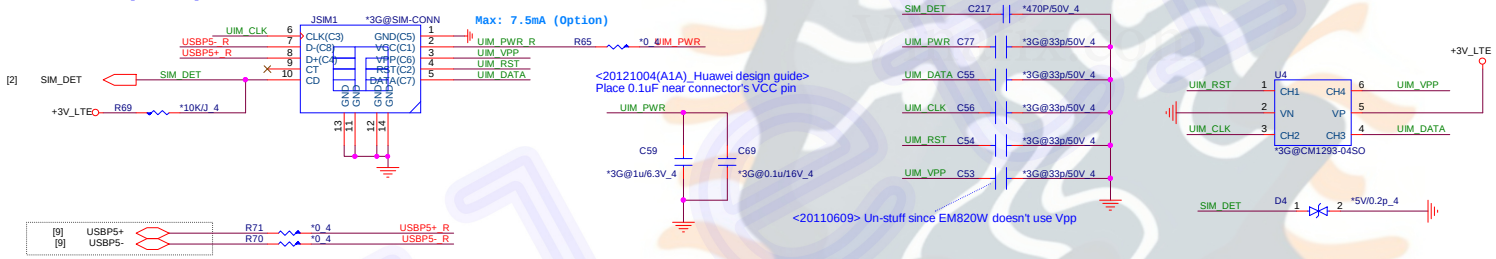
Size	Document Number	Rev
	NGFF SSD	A
Date: Thursday, December 04, 2014	Sheet 20 of 39	

NGFF 3G connector



MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.

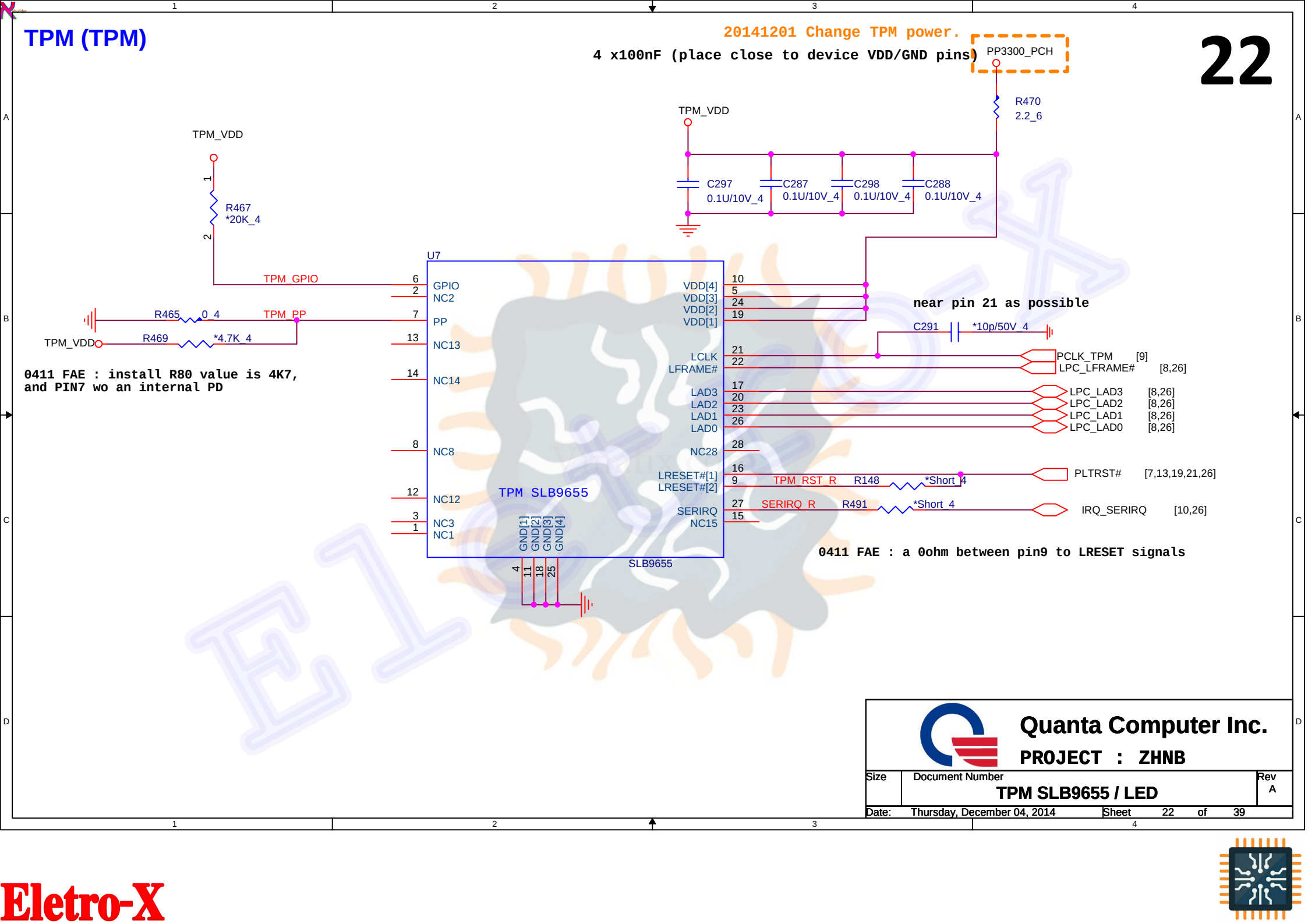


Quanta Computer Inc.			
PROJECT : ZHNB			
Size	Document Number		Rev
	NGFF/ SIM conn		A
Date: Thursday, December 04, 2014	Sheet 21 of 39		

TPM (TPM)

20141201 Change TPM power.

4 x100nF (place close to device VDD/GND pins)



0411 FAE : install R80 value is 4K7, and PIN7 wo an internal PD

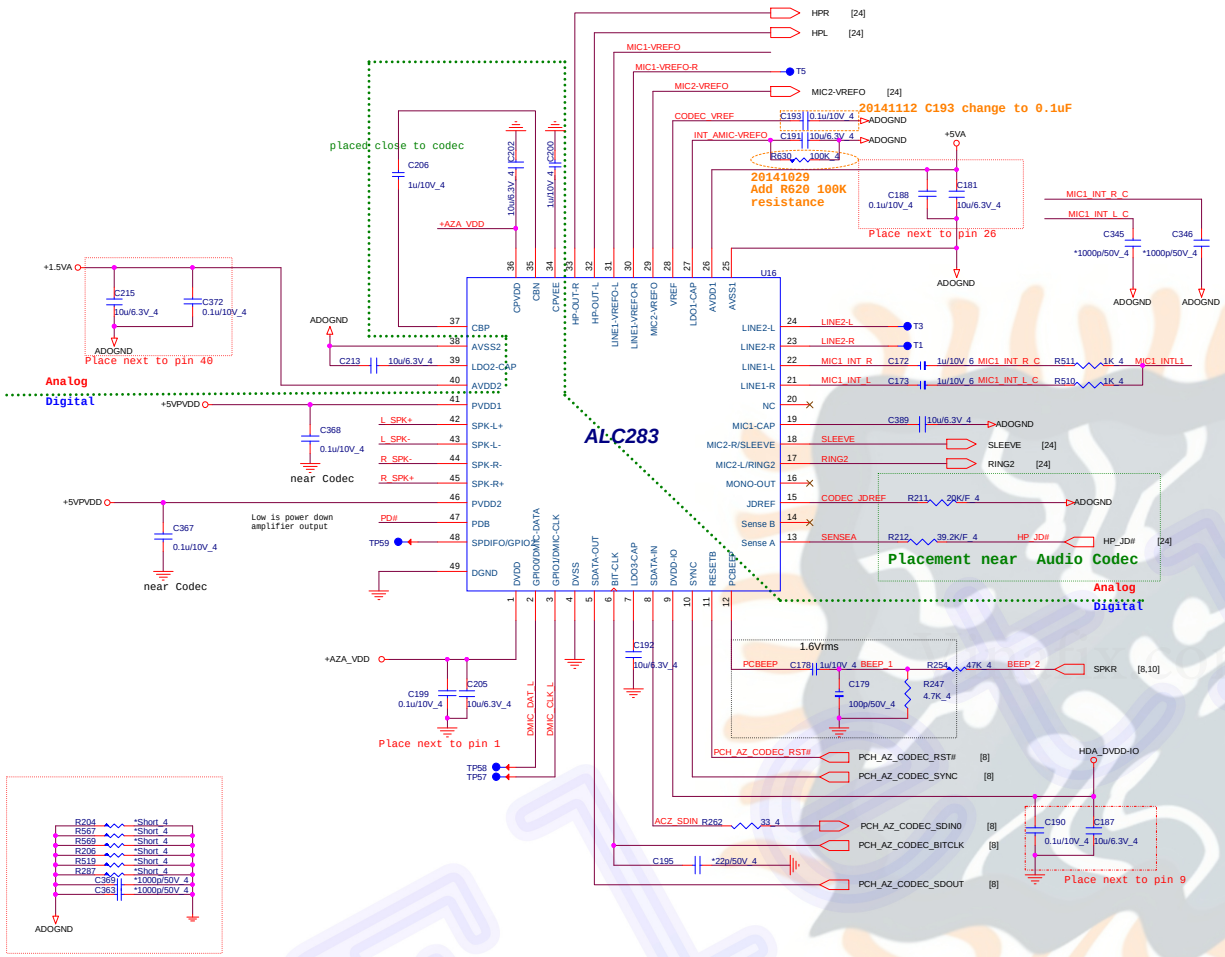
0411 FAE : a 0ohm between pin9 to LRESET signals

Quanta Computer Inc.

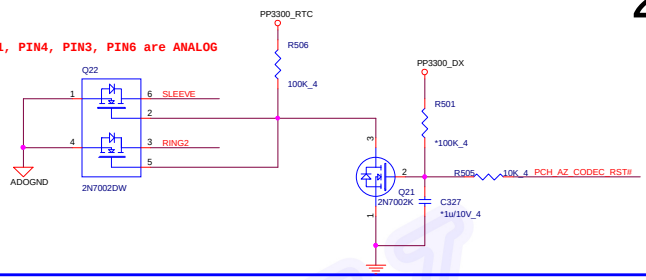
PROJECT : ZHNB

Size	Document Number	Rev
	TPM SLB9655 / LED	A
Date: Thursday, December 04, 2014	Sheet 22 of 39	

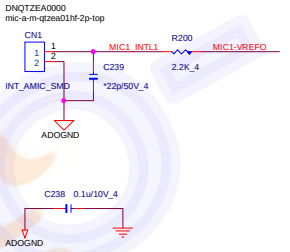
Codec(ADO)



Grounding circuit(ADO)

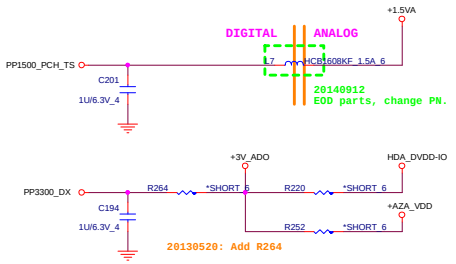


INT MIC array

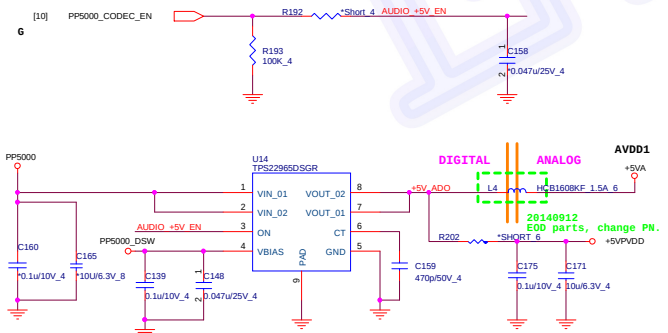


cap place close to MIC-connector

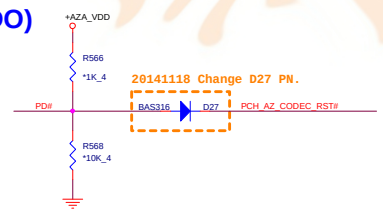
Codec PWR 3V/1.5V(ADO)



Codec PWR 5V(ADO)



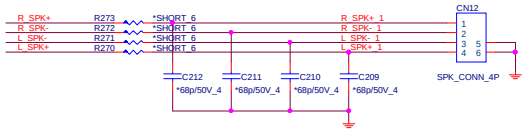
Mute(ADO)



Internal Speaker

40mil for each signal

footprint 88266-040xx-xxx-4p-l

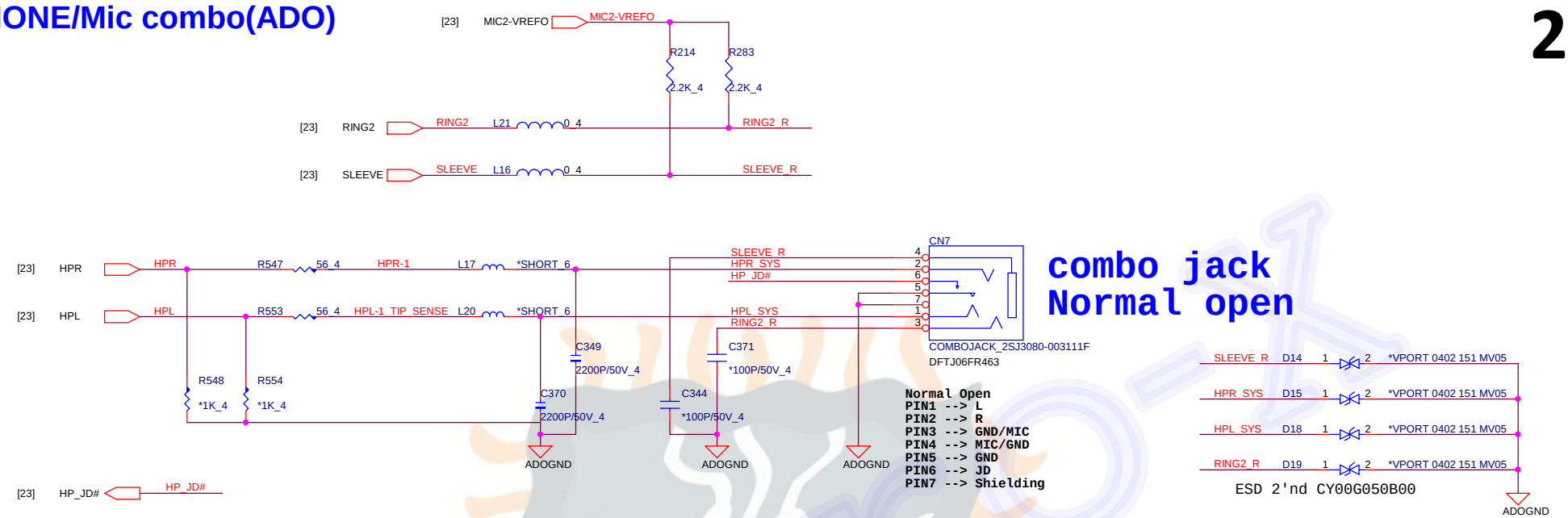


Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	ALC283/HP/SPK	A

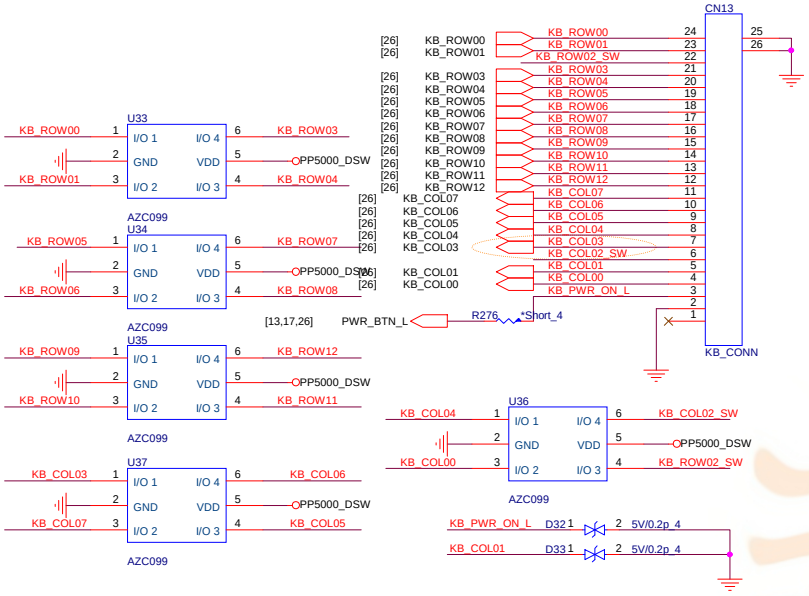
Date: Thursday, December 04, 2014 Sheet 23 of 39

HEADPHONE/Mic combo(ADO)

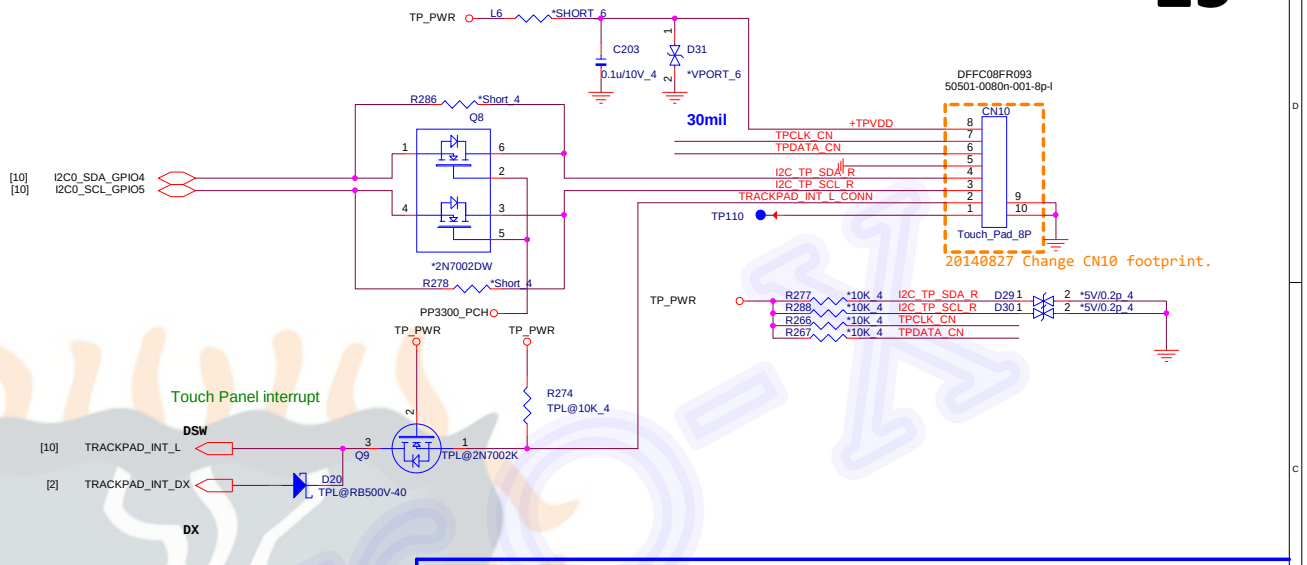


Quanta Computer Inc. PROJECT : ZHNB			
Size	Document Number: Audio Headset SW		Rev A
Date: Thursday, December 04, 2014	Sheet 24 of 39		

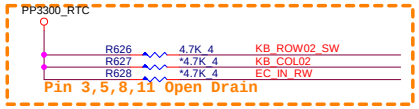
K/B (KBC)

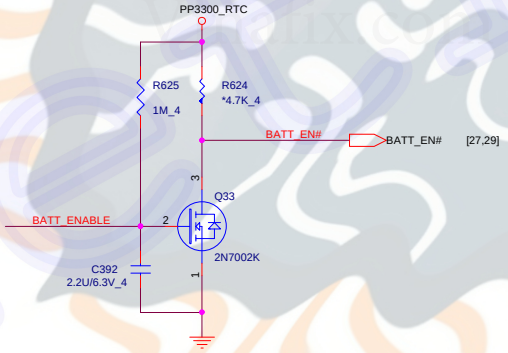


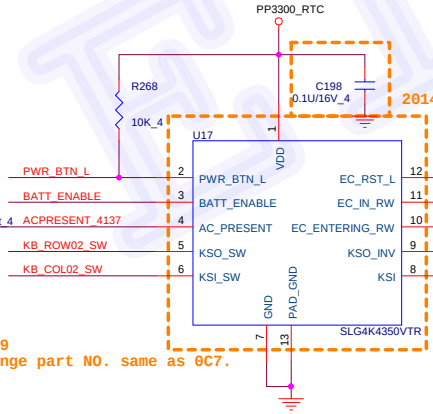
TOUCHPAD BOARD CONN (TPD)



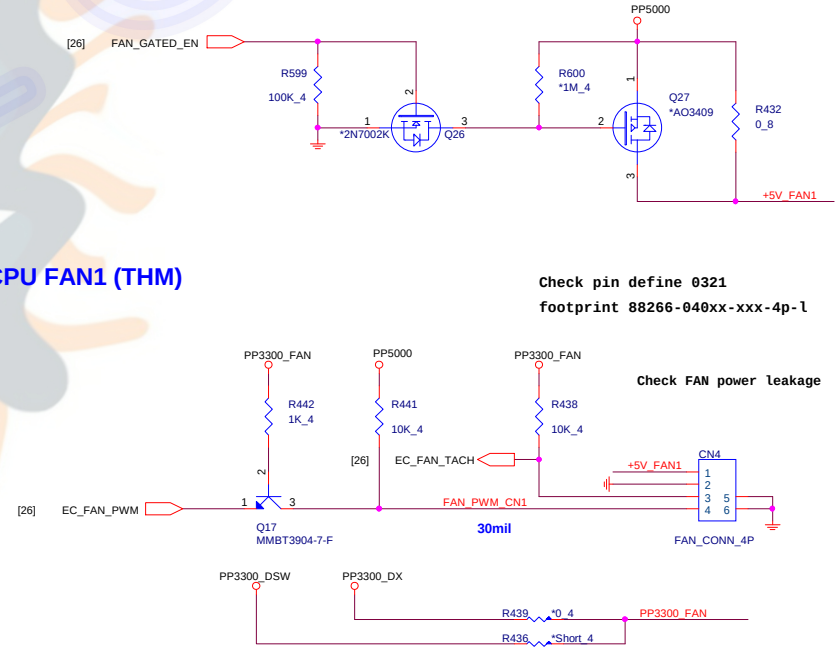
HOLELESS RESET 2-CHIP(KBC)







CPU FAN1 (THM)



Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	KB/TP/FAN/HW Reset	A
Date: Thursday, December 04, 2014	Sheet 25 of 36	

EC(KBC)

20141107 Change U5 PN.
20141201 Change U5 new PN.

20140912 EOD parts, change PN.

20140912 EOD parts, change PN.

20140912 EOD parts, change PN.

SM BUS/I2C PU(KBC)

BATT and CHARGER / LCD BL

Light BAR

THERMAL SENSOR

EC HIB WAKE SOURCES

20140912 EOD parts, change PN.

20141120 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.

20141118 Change D28 PN.

SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

For test only

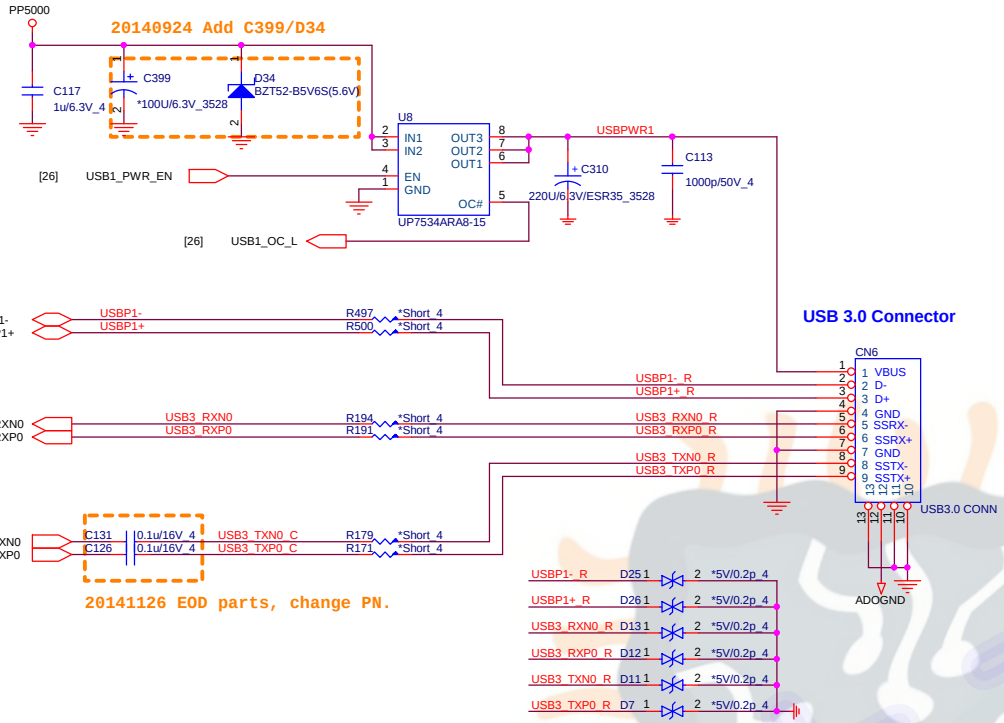
Quanta Computer Inc.

PROJECT : ZHNB

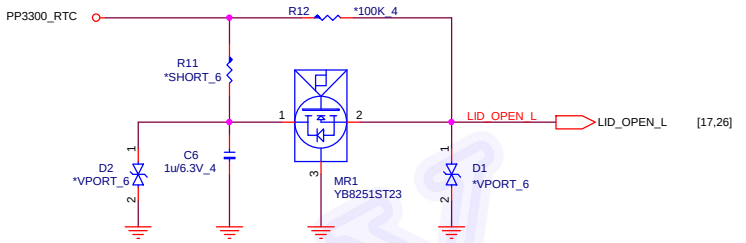
Size | Document Number: KBC TI TM4E1G31H6ZRBI | Rev

Date: Thursday, December 04, 2014 | Sheet 26 of 31

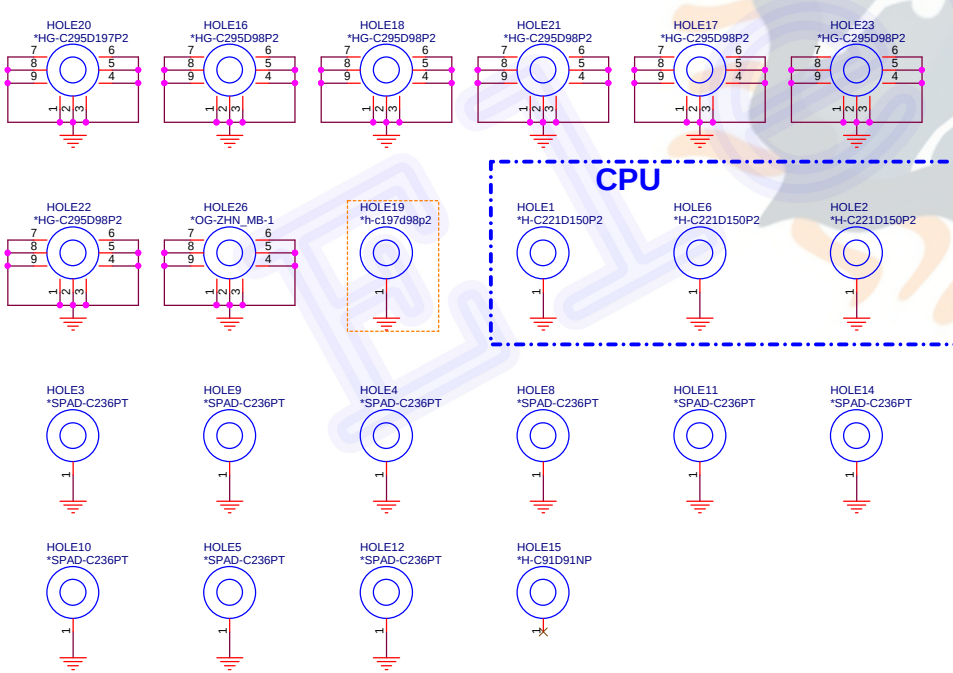
USB3.0(USB)



Lid Switch (HSR)



HOLE(OTH)

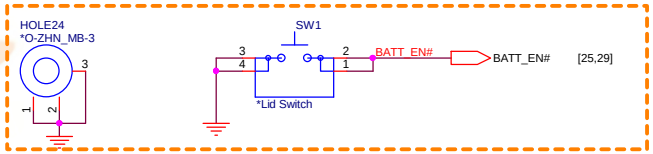


20140909 Change HOLE19 footprint.

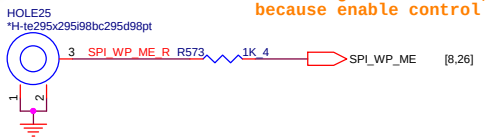
CPU

ROM WP#

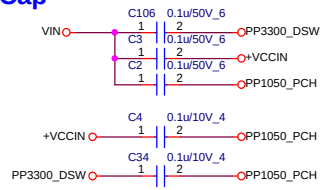
BATT Enable short pad



20141119 HOLE24 remove BATT_EN# pin3.
SW1 change to un-stuff,
because enable control by U17.

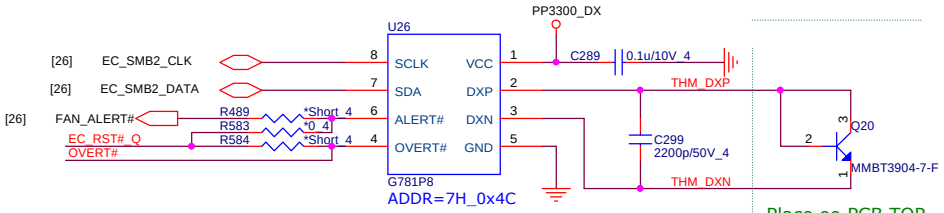


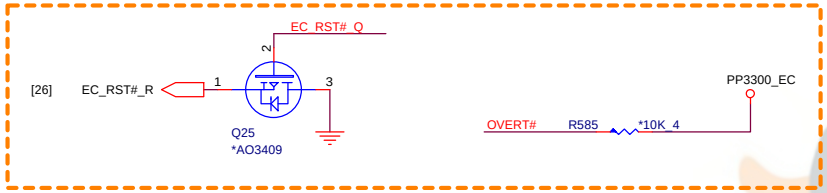
EMI Cap



Quanta Computer Inc
PROJECT : ZHNB
Size | Document Number | Rev
USB3/Hole | A
Date: Thursday, December 04, 2014 | Sheet 27 | of 38

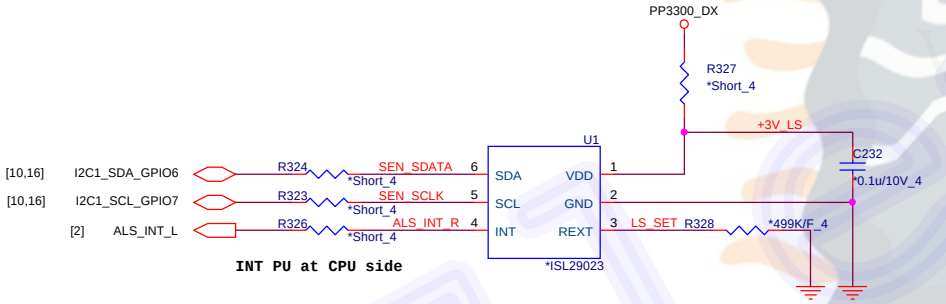
Thermal Sensor(THM)





20140925 Q25/R585 mark 「*」un-stuff.
OVERT# power PP3300_DX change to PP3300_EC.

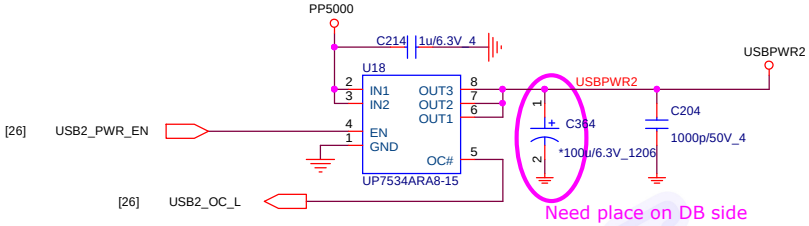
Light sensor & TP (SER)

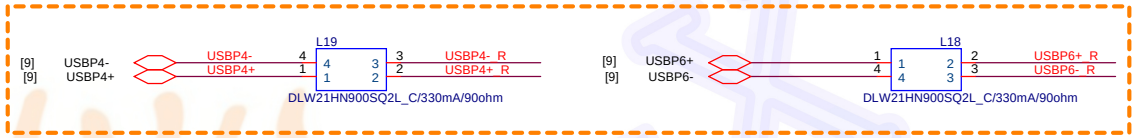


INT PU at CPU side

ADDR: 1000100

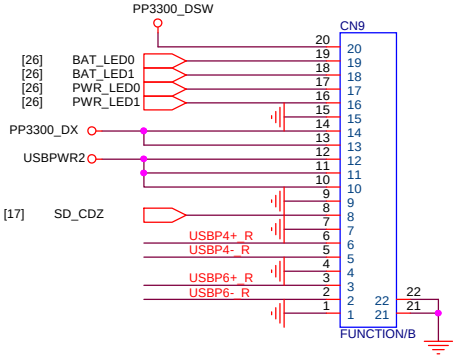
FUNCTION DB





20141201 stuff L18/L19, remove R549/R550/R551/R552.

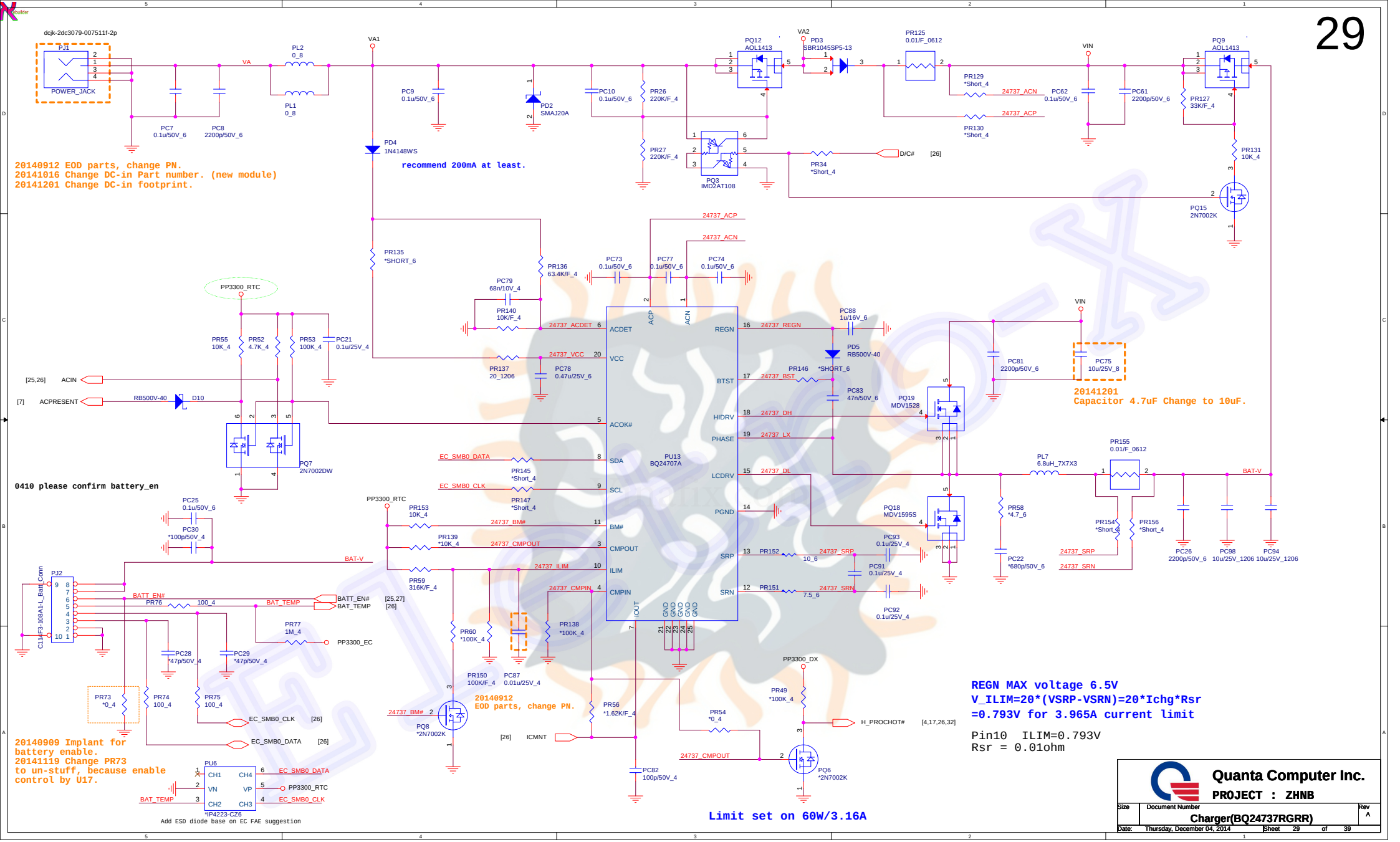
footprint 88511-2001-20p-l
DFFC20FR043

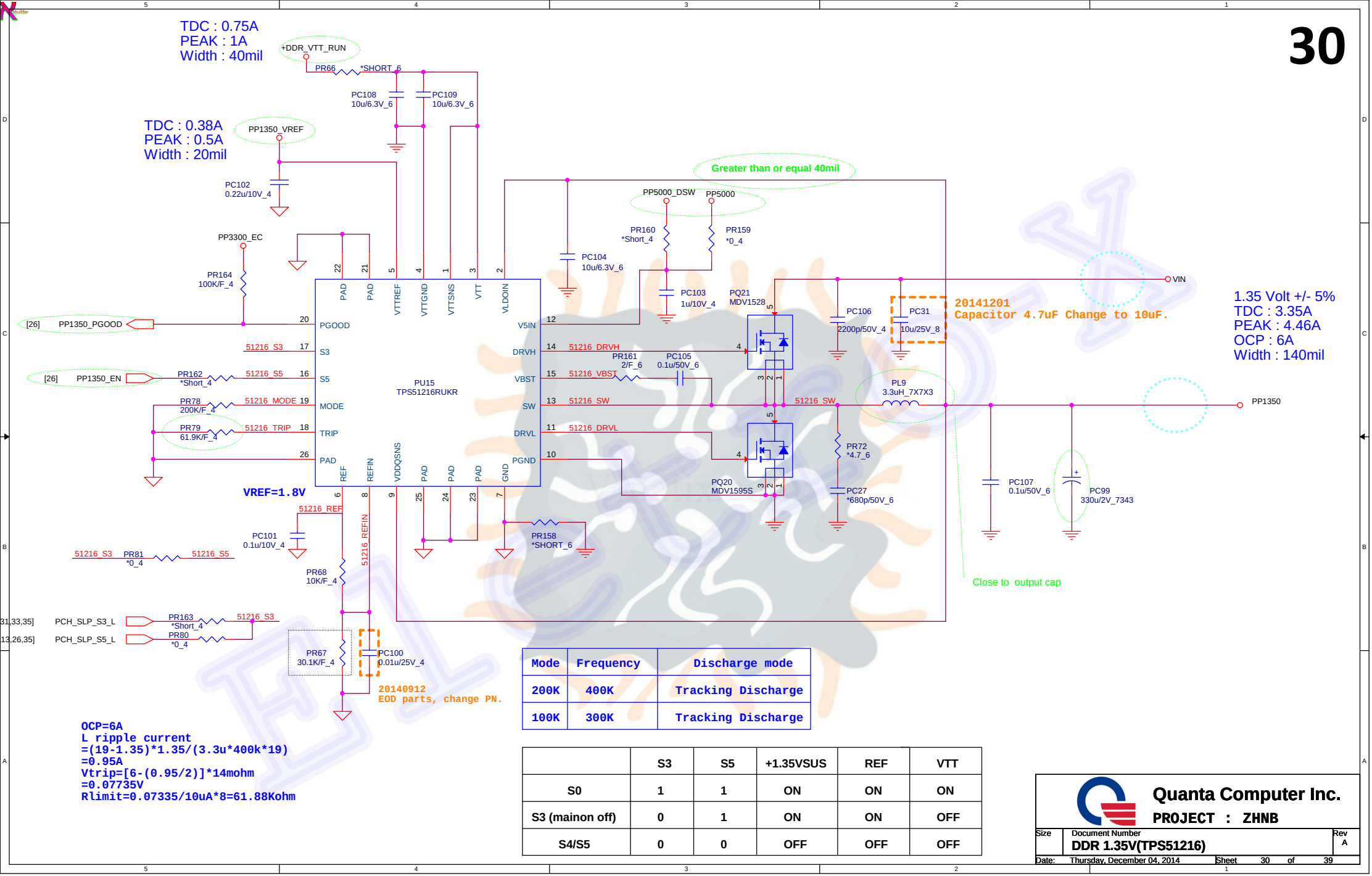


HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2

Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	DB/ALS/Thermal sensor	A
Date: Thursday, December 04, 2014	Sheet 28 of 39	


dcjk-2dc3079-007511f-2p
PJ1
POWER_JACK
VA
PL2 0_8
PL1 0_8
PC7 0.1u/50V_6
PC8 2200p/50V_6
VA1
PC9 0.1u/50V_6
PD4 1N4148WS
PD2 SMAJ20A
PC10 0.1u/50V_6
PR26 220K/F_4
PR27 220K/F_4
PQ12 AOL1413
PQ3 IMD2AT108
VA2
PD3 SBR1045SP5-13
PR125 0.01/F_0612
PR129 *Short_4
PR130 *Short_4
24737_ACN
24737_ACP
PC62 0.1u/50V_6
VIN
PC61 2200p/50V_6
PQ9 AOL1413
PR127 33K/F_4
PR131 10K_4
PQ15 2N7002K
D/C# [26]
PR34 *Short_4
20140912 EOD parts, change PN.
20141016 Change DC-in Part number. (new module)
20141201 Change DC-in footprint.
recommend 200mA at least.
PR135 *SHORT_6
PR136 63.4K/F_4
PC73 0.1u/50V_6
PC77 0.1u/50V_6
PC74 0.1u/50V_6
PC79 68n/10V_4
PR140 10K/F_4
PP3300_RTC
PR55 10K_4
PR52 4.7K_4
PR53 100K_4
PC21 0.1u/25V_4
[25,26] ACIN
[7] ACPRESENT
RB500V-40
D10
PQ7 2N7002DW
0410 please confirm battery_en
PU13 BQ24707A
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
IOUT
GND
24737_ACDET
24737_VCC
24737_REGN
24737_BST
24737_DH
24737_LX
24737_DL
PR137 20_1206
PC78 0.47u/25V_6
PC88 1u/16V_6
PD5 RB500V-40
PR146 *SHORT_6
PC83 47n/50V_6
PQ19 MDV1528
PC81 2200p/50V_6
PC75 10u/25V_8
20141201
Capacitor 4.7uF Change to 10uF.
PR155 0.01/F_0612
PL7 6.8uH_7X7X3
BAT-V
PR58 *4.7_6
PC22 *680p/50V_6
PR154 *Short_4
PR156 *Short_4
PC26 2200p/50V_6
PC98 10u/25V_1206
PC94 10u/25V_1206
PQ18 MDV1595S
PC93 0.1u/25V_4
PC91 0.1u/25V_4
PC92 0.1u/25V_4
PR152 10_6
PR151 7.5_6
24737_SRP
24737_SRN
EC_SMB0_DATA
EC_SMB0_CLK
PR145 *Short_4
PR147 *Short_4
PR153 10K_4
PR139 *10K_4
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
PR59 316K/F_4
PR60 *100K_4
PR138 *100K_4
PR150 100K/F_4
PC87 0.01u/25V_4
PR56 *1.62K/F_4
PC82 100p/50V_4
PQ8 *2N7002K
PQ6 *2N7002K
PR54 *0_4
PR49 *100K_4
PP3300_DX
H_PROCHOT# [4,17,26,32]
ICMNT [26]
PC25 0.1u/50V_6
PC30 *100p/50V_4
BAT-V
PJ2
C114F73-108A1-L_Batt_Conn
BATT_EN#
BAT_TEMP
PR76 100_4
PR77 1M_4
PP3300_EC
PC28 *47p/50V_4
PC29 *47p/50V_4
PR73 *0_4
PR74 100_4
PR75 100_4
[25,27] [26]
20140909 Implant for battery enable.
20141119 Change PR73 to un-stuff, because enable control by U17.
PU6
CH1
CH2
CH3
CH4
VN
VP
*IP4223-CZ6
Add ESD diode base on EC FAE suggestion
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : ZHNB
Size
Document Number
Charger(BQ24737RGRR)
Rev A
Date: Thursday, December 04, 2014
Sheet 29 of 39



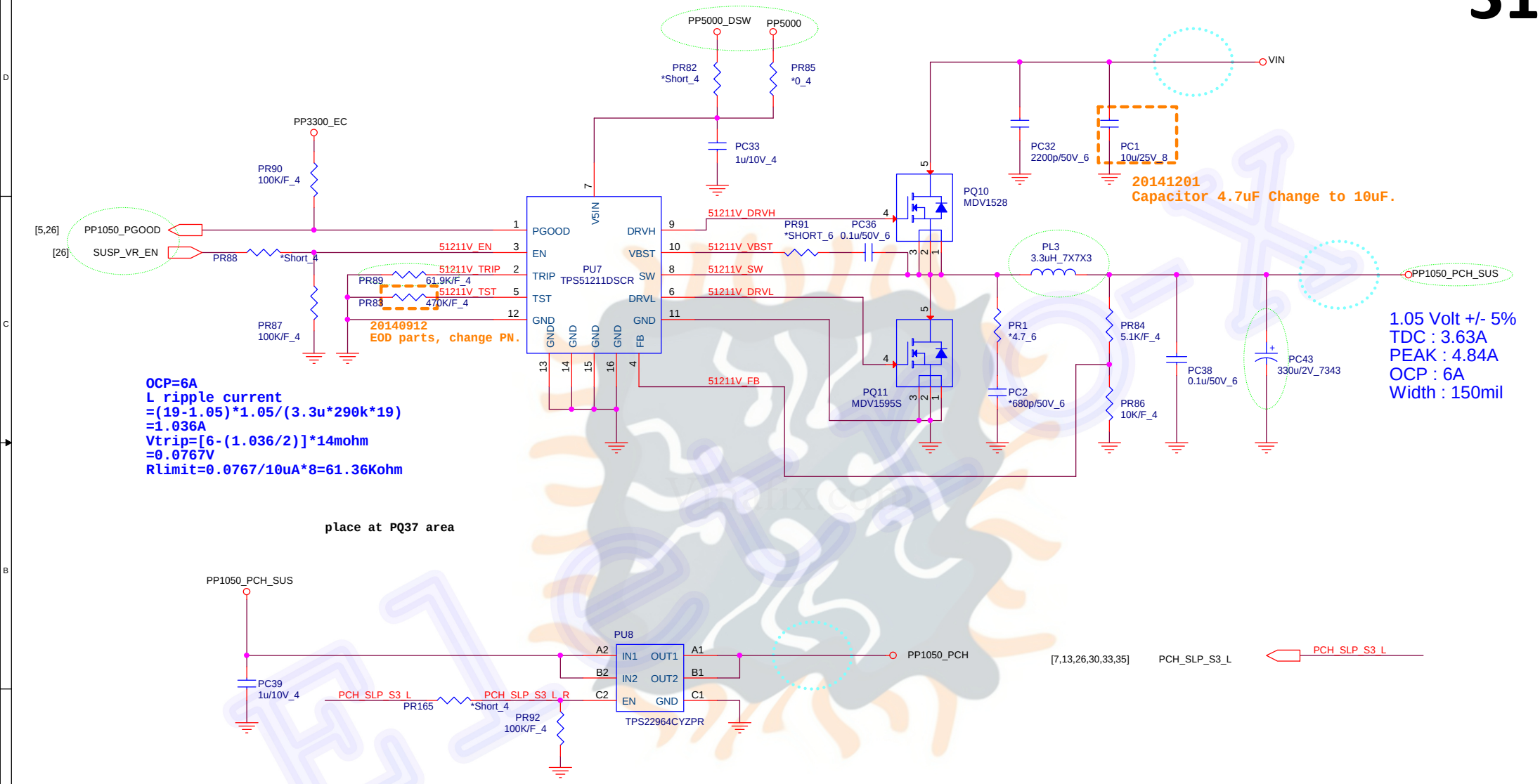
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

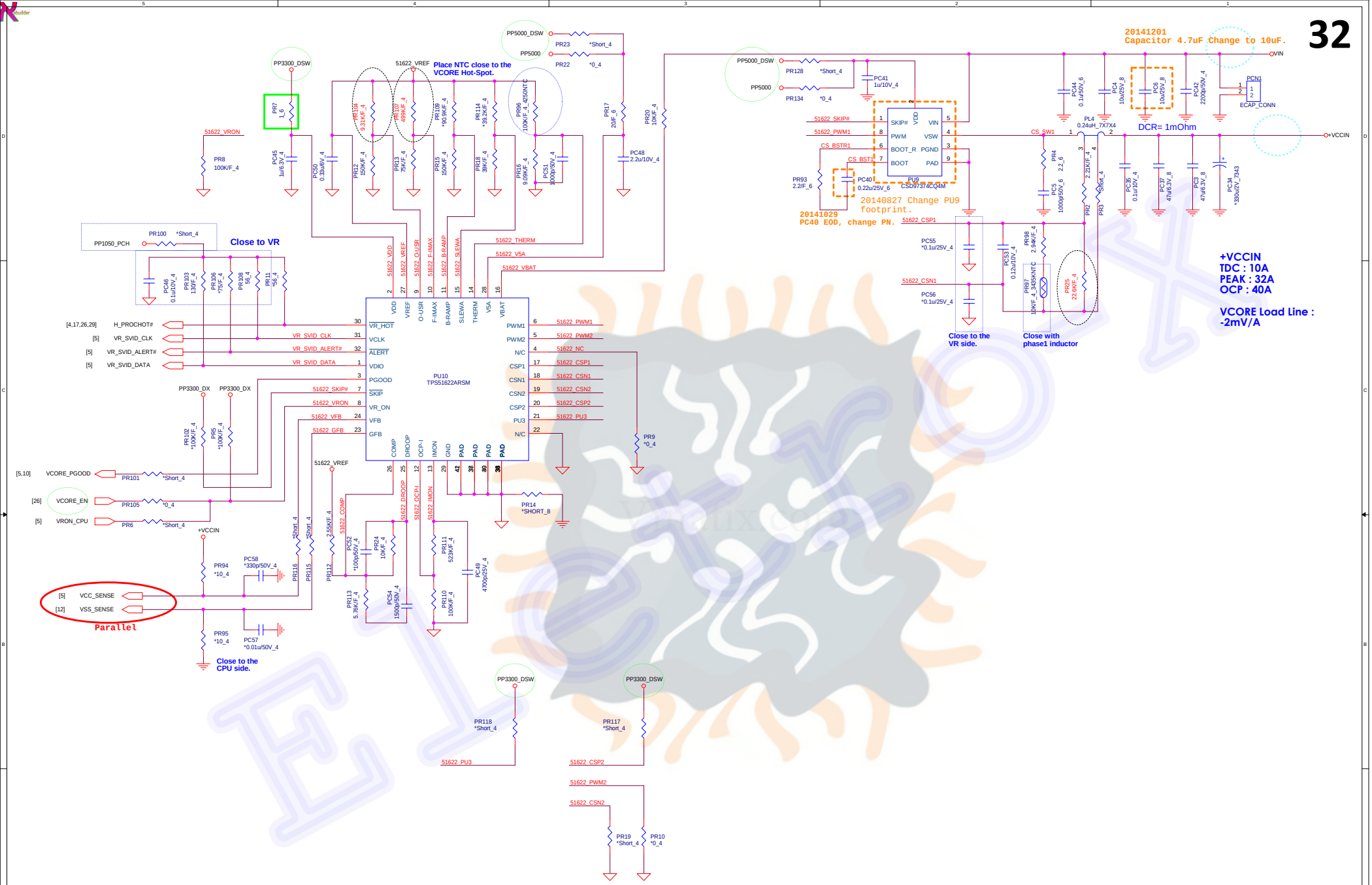
Quanta Computer Inc.
PROJECT : ZHNB

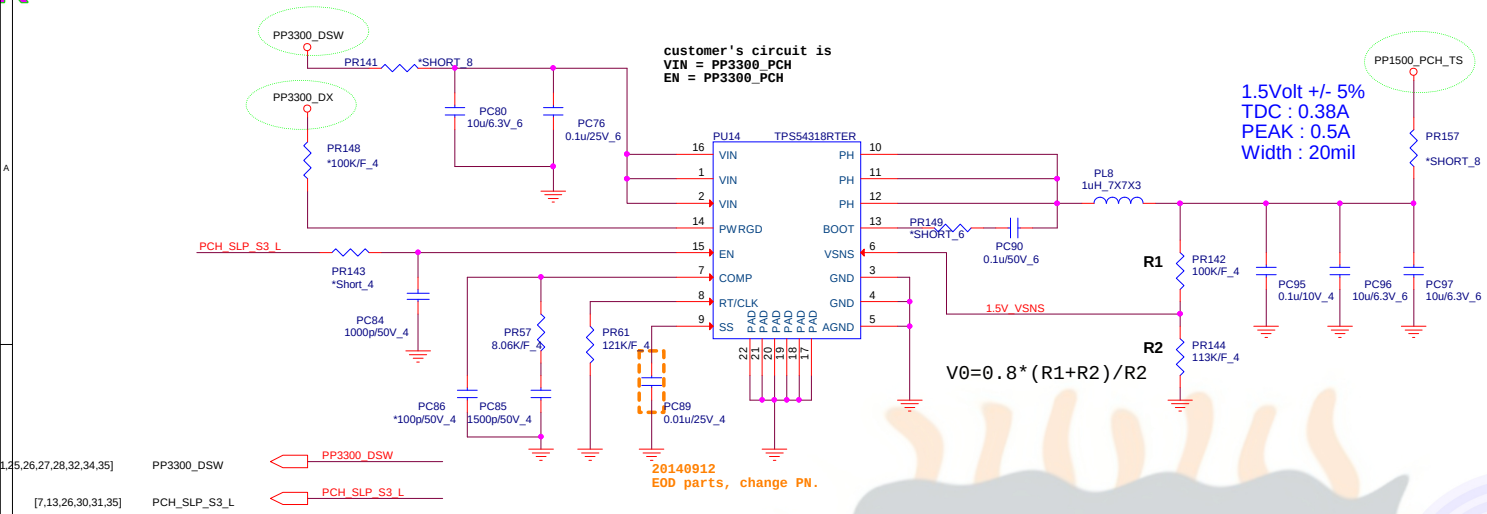
Size	Document Number	Rev
	DDR 1.35V(TPS51216)	A

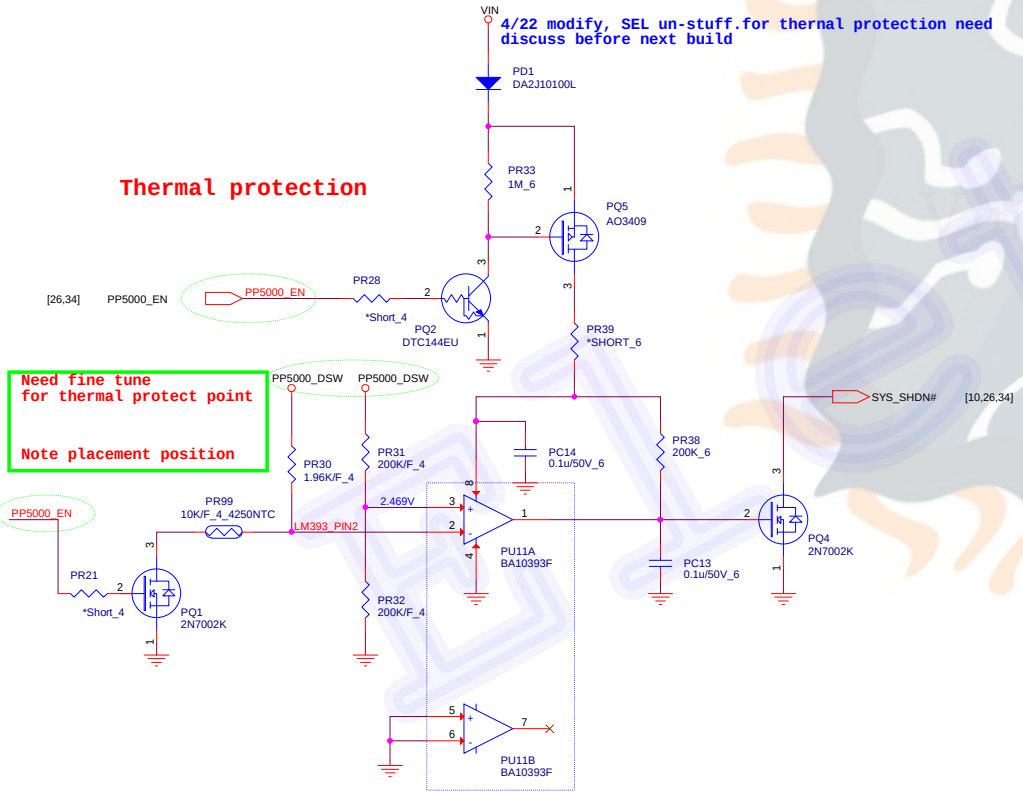
Date: Thursday, December 04, 2014 Sheet 30 of 39



Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: +1.05V(TPS51211)	Rev: A
Date: Thursday, December 04, 2014	Sheet 31 of 39	

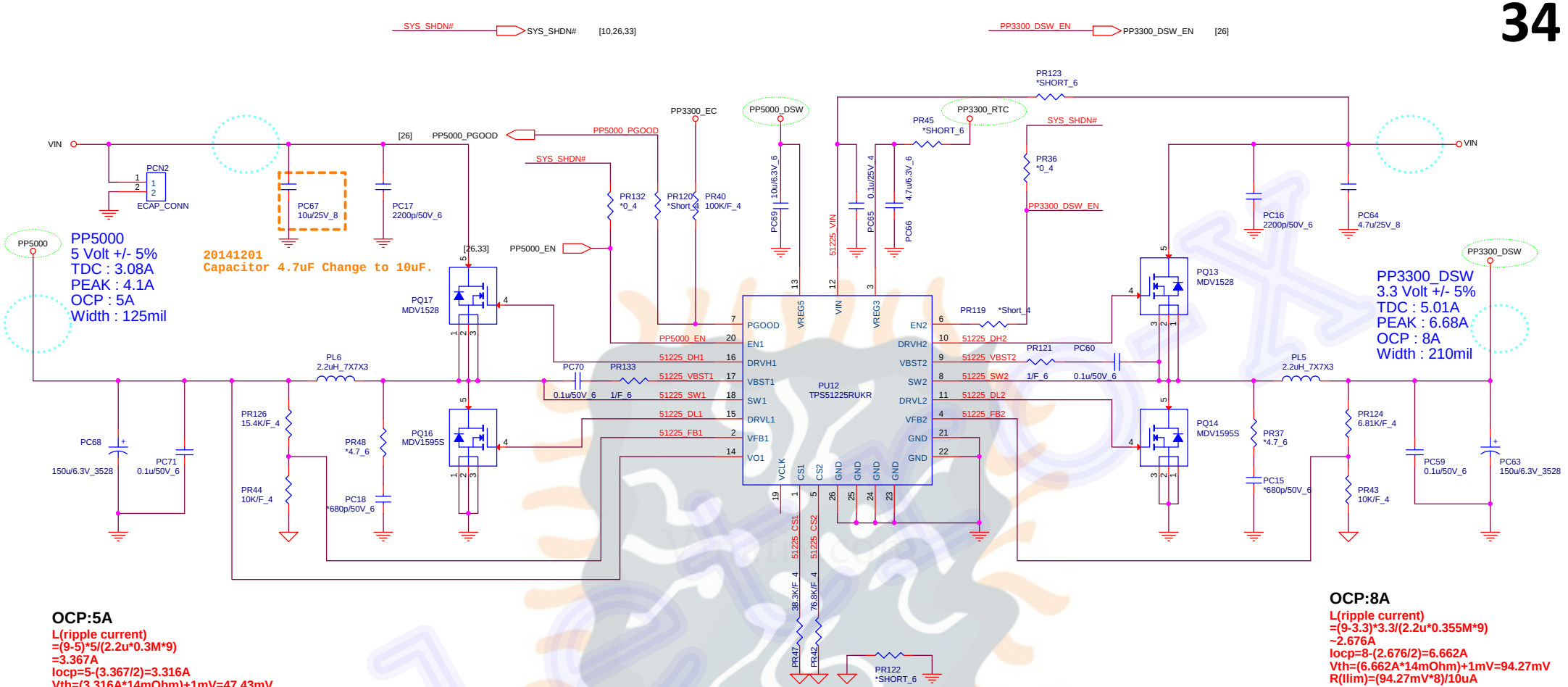

20141201
Capacitor 4.7uF Change to 10uF.
Place NTC close to the VCORE Hot-Spot.
Close to VR
20140827 Change PU9 footprint.
20141029
PC40 EOD, change PN.
DCR= 1mOhm
+VCCIN
TDC : 10A
PEAK : 32A
OCP : 40A
VCORE Load Line : -2mV/A
Close to the VR side.
Close with phase1 inductor
Close to the CPU side.
Parallel
PU10
TPS51622ARSM
PU9
CSD97374CQ4M





For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number	Rev
	+1.2V/+1.5V/+1.8V/Thermal protect	A
Date: Thursday, December 04, 2014	Sheet 33	of 86

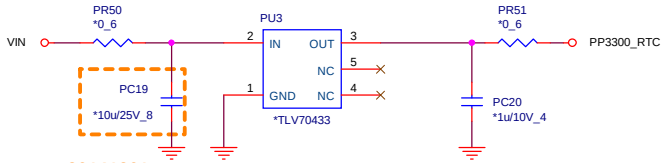


OCP:5A

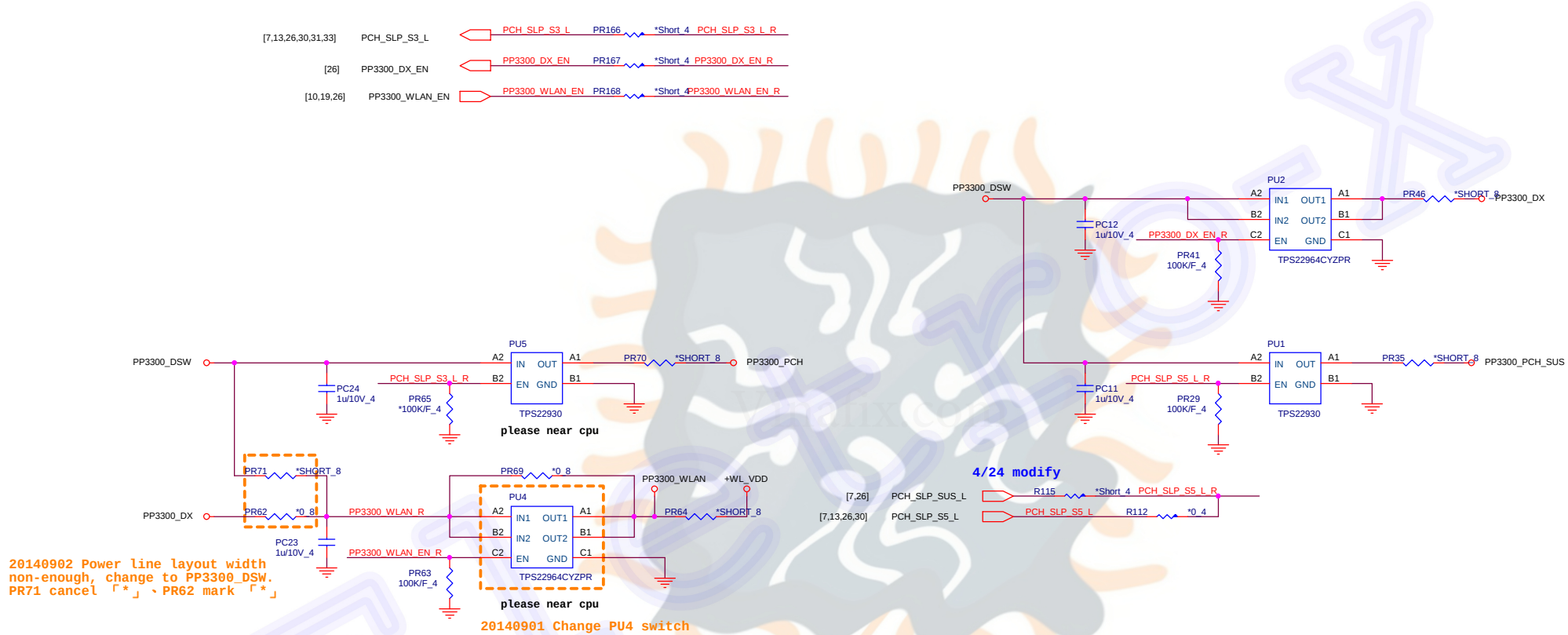
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=5-(3.367/2)=3.316A
Vth=(3.316A*14mOhm)+1mV=47.43mV
R(Ilim)=(47.43mV*8)/10uA
=37.94K

OCP:8A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=8-(2.676/2)=6.662A
Vth=(6.662A*14mOhm)+1mV=94.27mV
R(Ilim)=(94.27mV*8)/10uA
=75.41K



Quanta Computer Inc
PROJECT : ZHNB
Size: Document Number: SYSTEM 5V/3V (TPS51225) Rev: A
Date: Thursday, December 04, 2014 Sheet 34 of 43



Quanta Computer Inc
PROJECT : ZHNB

Size	Document Number	Rev
	Load Switch	A

Date: Thursday, December 04, 2014 Sheet 35 of 43

Model	Version	CHANGE LIST
ZHNB	1A-1	2014/08/21 Page16: LCD conn. I2C1_SDA_GPIO6_CONN pin reserve a 15pF capacitor. 2014/08/21 Page16: Touch panel level shift Q13 FET change to PJT138K. 2014/08/22 Page19: Will U27 change to another onboard module 7260SDW. 2014/08/22 Page21: NGFF 3G / SIM mark 「*」.
	1A-2	2014/08/27 Page19: Change wifi onboard module 7260SDW footprint. 2014/08/27 Page19: Pin W_DISABLE# / W_DISABLE#2 add 100K resistance pulldown. 2014/08/27 Page16: Change LVDS conn. CN3 footprint. 2014/08/27 Page18: Change HDMI conn. CN5 footprint. 2014/08/27 Page21: Change NGFF 3G conn. CN8 footprint. 2014/08/27 Page25: Change touchpad board conn. CN10 footprint. 2014/08/27 Page32: Change VCORE PU9 footprint.
	1A-3	2014/09/1 Page34: Change LDO PU4 switch.
	1A-4	2014/09/2 Page35: LDO PR71 cancel 「*」, PR62 mark 「*」. 2014/09/2 Page19: Will 100K resistance R831/R832 mark 「*」.
	1A-5	2014/09/9 Page29: Implant PR73 for battery enable. 2014/09/9 Page19: Change wifi onboard module 7260SDW footprint.
	1A-6	2014/09/12 Page16: C16 EOD, change PN. 2014/09/12 Page21: C379/C380/C381/C382 EOD, change PN. 2014/09/12 Page23: L4/L7 EOD, change PN. 2014/09/12 Page26: C208/C352/C360/L15 EOD, change PN. 2014/09/12 Page29: PC87/P31 EOD, change PN. 2014/09/12 Page30: PC100 EOD, change PN. 2014/09/12 Page31: PR83 EOD, change PN. 2014/09/12 Page33: PR89 EOD, change PN.
	1B-1	2014/09/24 Page26: USB3.0 U8 P1/P2 add C399/D34.
	1B-2	2014/09/25 Page28: Thermal MOSFET Q25/Resistance R585 mark 「*」 un-stuff. OVERT# power PP3300_DX change to PP3300_EC.
	1B-3	
	1B-4	2014/10/14 Page19: Change wifi onboard module 7260SDW PN.
	1B-5	2014/10/16 Page29: Change DC-in PN. (new module)
	1C-1	2014/10/21 Page15: Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.
	1C-2	2014/10/29 Page23: Codec pin27 add 100K resistance 2014/10/29 Page31: PC40 EOD, change PN.
	1C-3	2014/11/07 Page26: Change U5 EC PN.
	1C-4	2014/11/12 Page23: C193 change to 0.1uF. 2014/11/12 Page all: 0 ohm resistance change to short pad.
	1C-5	2014/11/18 Page25/Page26: change D27/D28 PN.
	1C-6	2014/11/19 Page25: U17 change part NO. same as 0C7, add MOSFET Q33. 2014/11/19 Page27: Remove HOLE24 BATT_EN# pin3, because enable control by U17. 2014/11/19 Page27: Lid SW change to un-stuff, because enable by U17. 2014/11/19 Page26: PR73 change to un-stuff, because enable control by U17.
	1C-7	2014/11/20 Page26 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.
	1C-8	2014/11/25 Page16 Change TPS/R561/Q13 to un-stuff, because no touch panel.
	1D-1	2014/11/26 CH4102K1B03 EOS parts, change to CH4103K1B08
		2014/12/01 Page22 Change TPM power. 2014/12/01 Page26 Change EC new PN. 2014/12/01 Page27 Stuff L121.1R/L19, remove R371/R372/R549/R550/R551/R552. 2014/12/01 Page29 Change DC-in footprint. 2014/12/01 PC1/PC19/PC31/PC6/P67/PC75 4.7uF change to 10uF.
	2A	
	3A	

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	Quanta Computer Inc.
	PART NUMBER:		DRAWING BY:		REVISON:	PROJECT : ZHNB

Change list